

# **EFFICIENT DESIGN OF LINEAR HIGH-FREQUENCY FILTERS**

An Honors Fellow Thesis

by

DIGANTO CHOUDHURY

Submitted to Honors and Undergraduate Research  
Texas A&M University  
in partial fulfillment of the requirements for the designation as

HONORS UNDERGRADUATE RESEARCH FELLOW

May 2012

Major: Electrical Engineering

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Approved by:

Research Advisor:

Associate Director, Honors and Undergraduate Research:

Aydin Karsilayan

Duncan MacKenzie

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## ABSTRACT

Efficient Design Of Linear High-Frequency Filters. (May 2012)

Diganto Choudhury  
Department of Electrical Engineering  
Texas A&M University

Research Advisor: Dr. Aydin Karsilayan  
Department of Electrical Engineering

Direct-conversion receivers are becoming more and more popular in wireless communication systems because they promise superior performance in power consumption, size, and cost over existing heterodyne-based receivers. Theoretically, direct-conversion receivers offer the advantage of omitting the intermediate stage required in heterodyne architectures, thereby greatly reducing the hardware complexity of receiver design. In this research, a higher order filtering technique is proposed to attenuate out-of-band blockers in a direct-conversion receiver without deteriorating the desired signal present in the band of interest. The proposed filter structure is based on a current-mode biquadratic pipe filter cell, which originally allows the implementation of only all-pole filter functions such as Butterworth. With the aim to achieve a flat magnitude response in pass-band and steep rate of attenuation in transition-band, the base structure is modified to implement higher order Inverse-Chebyshev transfer function, which requires realization of arbitrary complex zeros in the stopband. A third

order prototype has been realized in a 0.18 $\mu\text{m}$  CMOS process using 1.8V supply voltage.

## ACKNOWLEDGMENTS

I wish to acknowledge my great debts to all those who have contributed to the development of radio-frequency communication systems. Understanding the basics of wireless communications from several books, publications and online resources aided my understanding of the scope of the research project.

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Last but not the least, I would like to express my love and gratitude to my family and close friends for their incessant understanding, continuous support and endless love that abetted the successful completion of this project.

## NOMENCLATURE

ADC	Analog-to-Digital Convertors
FM	Frequency Modulation
IF	Intermediate Frequency
INC	Inverse-Chebyshev
LO	Local Oscillator
LPF	Low Pass Filters
RF	Radio Frequency
TIA	Transimpedance Amplifier
VGA	Variable Gain Amplifier

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# CHAPTER I

## INTRODUCTION

Wireless technology came into existence in 1901, when Marconi successfully transmitted radio signals across the Atlantic. From a simple experiment established to transmit data over wireless medium, the use of wireless technology has revolutionized modern communications. While simple FM circuits can be used in sending out wireless signals, modern RF communication devices have highly complex circuits.

The receiver architecture is a key part of any RF communication device and proper design of wireless receiver is required for an accurate detection of the required signal. Various architectures of receivers has been proposed in literature [1] and some of the most widely used structures include the Heterodyne, Wideband-IF, Low-IF and the Zero-IF architectures. The latest trend in receiver design is to simplify the analog front-end and get into the digital domain as early as possible. Zero-IF architectures convert the channel of interest directly from RF to baseband in a single stage and thus, in zero-IF architectures, the use of an intermediate IF stage is omitted and the hardware complexity is reduced. Because of the lack of an IF stage, a low pass filter alone can potentially filter out all the out-of-band signals. Hence, among the different receiver architectures mentioned above, the use of ‘direct-conversion’ or zero-IF receivers are addressed here.

For frequency and phase modulated signals, down-conversion must provide quadrature outputs so as to avoid loss of information. The block diagram of direct-conversion receiver architecture is shown in figure 1.

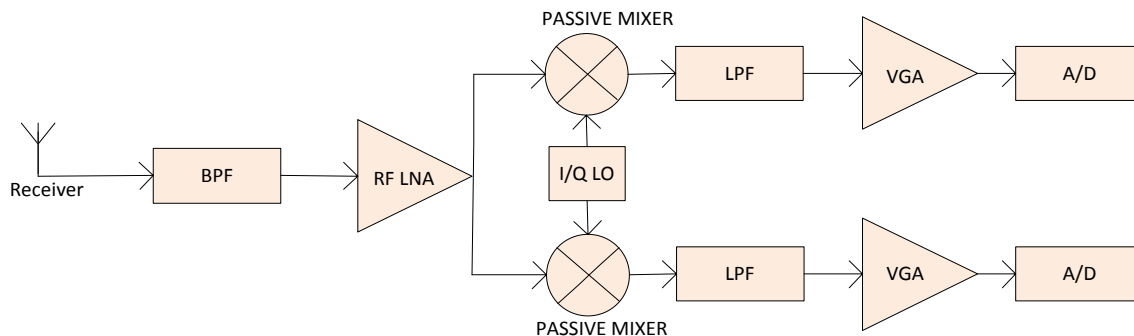


Fig. 1. Direct-Conversion Receiver Architecture

From the incoming RF signal, the pre-selection bandpass (BPF) filter removes out-of-band signal. The low power RF signal is then boosted by the LNA to suppress the contribution of noise from the succeeding stages. After the LNA, the signal passes through the mixer where the signal is down-converted from the RF band to baseband. After low-pass filtering (LPF), the signal is passed through a variable gain amplifier to match the full-scale signal range of the analog-to-digital convertor (A/D).

Due to its simplicity and reduced number of components, the use of direct-conversion receivers seems very appealing. In addition, converting the RF signal directly into baseband eliminates the problem of image frequency and the need for image-rejection filters that increase design effort and complexity [2]. The main goal is to detect the

desired signal, which could be very low power, among the large interferer signals present across the spectrum. The major challenge is to develop a minimally-invasive linear filter design that is capable of passing the small signal while rejecting the large blockers. In addition, designs that greatly increase the complexity of the analog front-end need to be avoided; the added circuitry should be justifiable against increasing the performance requirements in the A/D used in the receiver path.

In the ideal case, the direct-conversion receivers use a local-oscillator (LO) synchronized to the exact frequency of the carrier in order to directly translate the input signals to baseband frequencies. In other words, the desired signal can be obtained by tuning the LO to the required signal frequency. The remaining unwanted frequencies that appear after down-conversion stay at the higher frequency bands and can be removed by a low-pass filter placed after the mixer stage. However, the non-linear mixing of the two signals leads to several non-idealities that complicate the use of direct-conversion receivers. When the weak desired signal surrounded by strong interferers is passed through a non-linear mixer, the output exhibits several components that are the cross-modulation products of the desired signal with the nearby interferers. This phenomenon of intermodulation leads to corruption of the desired signal. The main task is to maintain the integrity of the desired signal while mitigating the interference in nearby frequency bands.

In [3], the structure of a broadband direct-conversion receiver front-end is described. A current-mode passive mixer is used in order to achieve high-linearity and low noise, which is followed by a transimpedance amplifier (TIA) with a single, real pole. This TIA provides the low impedance required for the linear operation of the passive mixer. However, the above topology only provides a first-order filtering of the blockers. The higher order filtering of unwanted out-of-band signals without affecting the signal strength of the desired signal is a difficult task. This research aims at developing minimally invasive filtering functions that can sufficiently remove the out-of-band blockers. A schematic showing the general structure of the receiver path is shown in figure2.

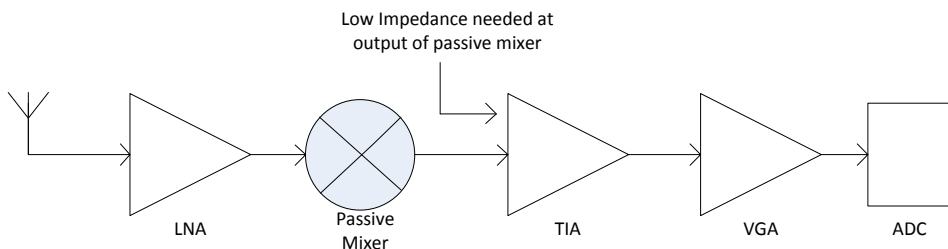


Fig. 2. Incorporation of Low-Pass Filter in Receiver Front-End

One method of filtering out the unwanted signals is demonstrated in [4], where, an active feedback network is used in the TIA that diverts blockers away while keeping the in-band characteristics unaltered. Although this method was shown reduce the blocker levels, the added feedback network added significant complexity to the receiver architecture. Moreover, the power consumption of the TIA will increase considerably with the added active feedback network.

Another approach described the use of a LPF at the output of the passive mixer. Such a filter should have low input impedance in order to satisfy the linearity requirement of the passive current-mode mixer. The concept of implementing a 4th order low-pass filter with low very low input impedance is illustrated in [5]. This filter is shown to operate in current mode, In [6], a similar transistor configuration of a 4th order filter is discussed that operates in voltage mode. However, in both [5] and [6], an all-pole transfer function with a relatively high power-supply is implemented. No transmission zeros are inserted in the LPF transfer function.

In this research, a low pass filter configuration to be placed in the receiver path will be designed. Methods to implement transmission zeros in the transfer function will be investigated and efforts will be made to reduce the supply voltage required to operate the filter.

## CHAPTER II

### METHODS

The concept of a pipe-filter is used to implement the filter function required for the project. The model of a first-order low pass (LP) pipe filter that produces a high-pass shaped output current noise spectrum is shown in figure 3.

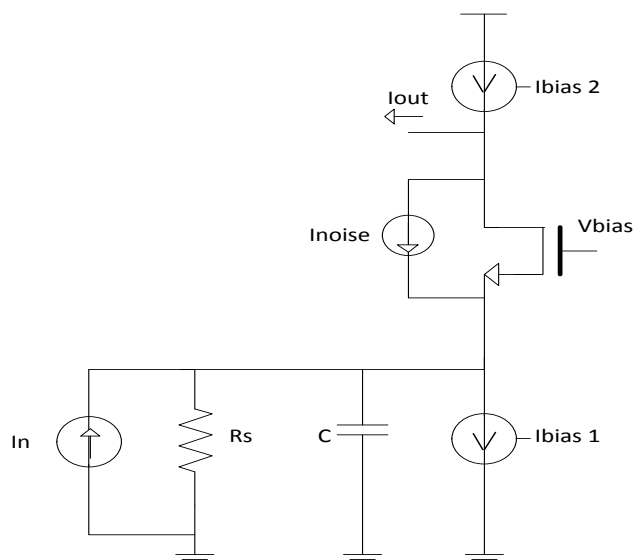


Fig. 3. First-Order Low Pass RC Filter

At low frequencies, the capacitor  $C$  provides high-impedance and the noise from the transistor circulates within the transistor. At high frequencies, the capacitor provides very low impedance and all the current noise from the transistor flows to the output. According to the above model, in the passband (low frequencies), the filter works as a lossless pipe where the input current is almost equal to the output current while in the

stopband (high frequencies), the distortion due to noise reaches the output. Thus, in general, it needs to be ensured that the noise level in the circuit is kept to a minimum in the passband. Since any operation performed on the input current can introduce noise, the filter function is selected to have unitary input to output transfer characteristics.

In order to create high-order filters, the required pipe filter needs to have complex poles which can be implemented through a RLC circuit network. For our research, an active circuit with an inductive frequency behavior is used. As seen in figure 4, this active inductor is implemented by creating a negative feedback between the drain and gate of the M1 such that there is a virtual short between the source of M1 and the gate of M2 at DC; at higher frequencies, the effect of capacitor C2 becomes evident and the voltage at the gate of M2 reduces. In other words, as the frequency increases, the input impedance of the circuit rises thereby acting as a virtual inductor.



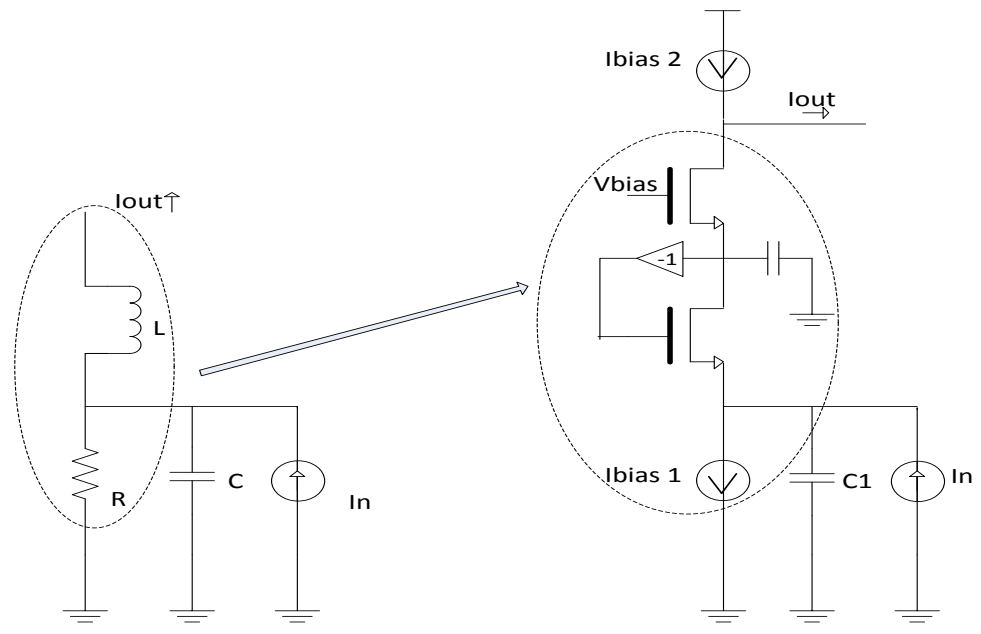


Fig. 4. Current Biquad Cell

Assuming that both transistors have equal transconductance ( $g_{m1} = g_{m2} = g_m$ ), the impedance value of Z versus frequency is calculated as shown below:

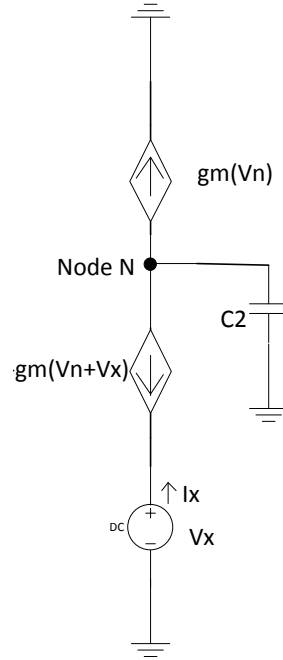


Fig. 5. Small Signal Equivalent to Find Z

In figure 5,

$$I_x = g_m V_n + g_m V_x \quad (1)$$

Applying node-voltage at node N,

$$V_n (sC_2) = g_m (V_x), \quad (2)$$

$$\Rightarrow V_n = \left( \frac{g_m}{sC_2} \right) V_x \quad (3)$$

Substituting (3) in (1),

$$I_x = g_m \left( \frac{g_m}{sC_2} \right) V_x + g_m V_x \quad (4)$$

$$I_x = \frac{g_m^2 \left(1 + \frac{sC_2}{g_m}\right)}{sC_2} V_x, \quad (5)$$

$$Z = \frac{V_x}{I_x} = \frac{sC_2}{g_m^2 \left(1 + \frac{sC_2}{g_m}\right)} \quad (6)$$

The small signal model of the current biquad cell is shown in figure 6.

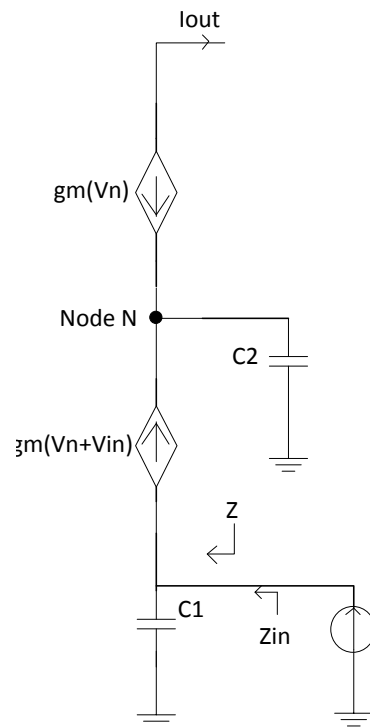


Fig. 6. Small Signal Equivalent to Find Transfer Function and Input Impedance

Due to the presence of the active inductor, the circuit acts as a second order low-pass filter. The transfer function of the circuit is derived below:

In figure 6, applying node voltage at node A,

$$I_{in} = V_{in}(sC_1 + g_m) + g_m V_n \quad (7)$$

Applying node voltage at node B,

$$V_{in} = V_n \left( \frac{sC_2}{g_m} \right) \quad (8)$$

Substituting (8) in (7),

$$I_{in} = V_n \left( \frac{sC_2}{g_m} (sC_1 + g_m) + g_m \right), \quad (9)$$

$$\Rightarrow I_{in} = \frac{I_{out}}{g_m} \left( s^2 \frac{C_1 C_2}{g_m} + sC_2 + g_m \right), \quad (10)$$

$$\Rightarrow \frac{I_{out}}{I_{in}} = \frac{\frac{g_m^2}{C_1 C_2}}{s^2 + \frac{g_m}{C_1} s + \frac{g_m^2}{C_1 C_2}} \quad (11)$$

From the transfer function (11), it can be obtained that the passband current ratio is equal to one. Thus, no additional current is injected into the output current and the circuit behaves as a lossless pipe as described in the beginning of this chapter.

Having assumed the same transconductance ( $g_m$ ) for the two transistors, the cut-off frequency ( $\omega_o$ ) is found to depend only on  $g_m$  and the product of the capacitances,  $C_1$  and  $C_2$ ; the quality factor (Q) is found to depend only on the ratio of capacitances  $C_1$  and  $C_2$ . The equations for the cut-off frequency and the quality factor are given by

$$\omega_o = \frac{g_m}{\sqrt{C_1 C_2}} \quad (12)$$

$$Q = \sqrt{\frac{C_1}{C_2}} \quad (13)$$

The low input impedance of this current-mode biquad LPF (fig.4) makes it ideal for use in the receiver path to satisfy the linearity requirement of the passive current-mode mixer. The equation of the input impedance ( $Z_{in}$ ) is derived below:

From equation (6)

$$Z = \frac{sC_2}{g_m^2 \left(1 + \frac{sC_2}{g_m}\right)} \quad (14)$$

$$Z_{in} = Z \parallel \frac{1}{sC_1}, \quad (15)$$

$$= \frac{sC_1}{s^2 + s\left(\frac{g_m}{C_1}\right) + \frac{g_m^2}{C_1 C_2}} \quad (16)$$

From the equation  $Z_{in}$ , it can be observed that at DC and at very high frequencies, the input impedance is very low (ideally zero); at the cut-off frequency ( $\omega_0$ ), the input impedance has a maximum value of  $1/g_m$ .

Now to implement a 4<sup>th</sup> order filter, two current biquad cells are cascaded. In order to easily implement a negative transconductance, a fully differential architecture is adopted. Figure 7 shows the schematic of a fourth-order low pass filter. The circuit

operates in current mode and can be easily placed after the passive current mixer in the direct-conversion receiver front end architecture described in [3].

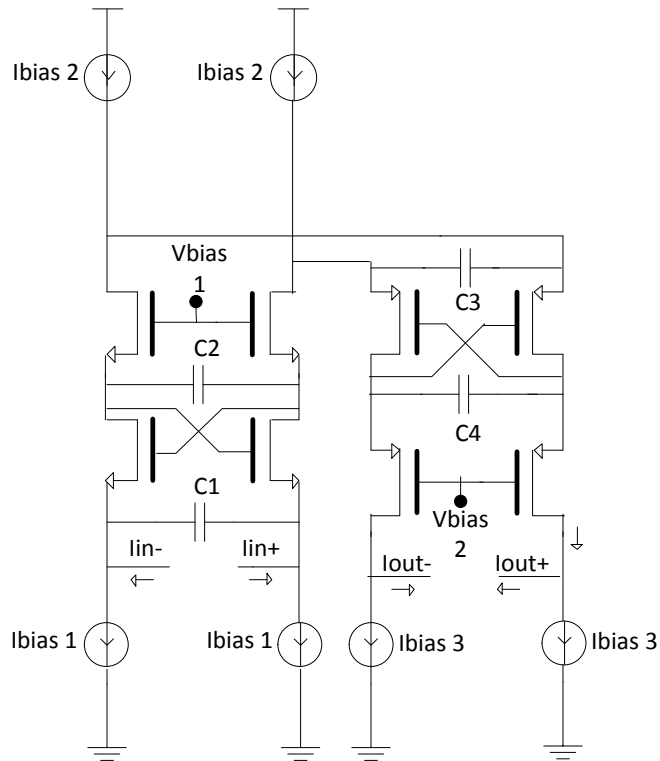


Fig. 7. Fourth-Order LPF schematic

After implementing the fourth-order low pass filter, possible methods of adding arbitrary transmission zeros to the circuit are explored and the appropriate technique is then implemented [7]. The general transfer function of a second order biquadratic function is given below.

$$T(s) = \frac{N(s)}{D(s)} = \frac{k_2 s^2 + k_1 s + k_0}{s^2 + s(\omega_o/Q) + \omega_o^2} \quad (17)$$

The first method of adding transmission zero involves the summing of different filter output. In this technique, the signals from appropriate nodes are copied and then added to the output node. In the case of voltage, a separate summing amplifier is used to perform the addition of different voltage signals. The output of this amplifier can be used to implement a transfer function of the desired form of equation (17). Figure 8 shows the method of voltage addition. The use of the summing amplifier is not required while adding current signals. The current from the desired nodes can be directly added to the output node as shown in figure 9.

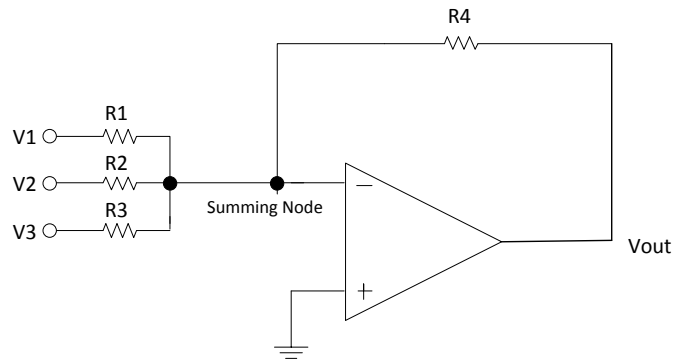


Fig. 8. Voltage Summing

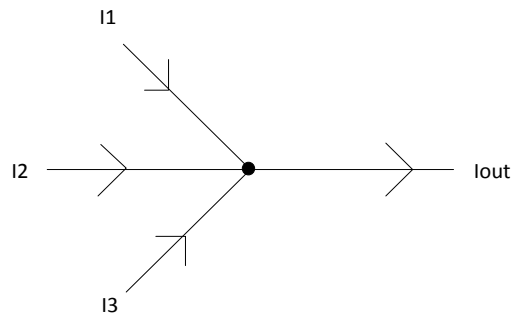


Fig. 9. Current Summing

The second method requires the injection of input signals into appropriate nodes and thereby achieving some desired polynomial  $N(s)$  in equation (17) without disturbing the roots  $D(s)$ . This technique, also called voltage feedforward, involves feeding an input voltage signal into a node that is created by lifting any component completely or partially off ground. Figure 10 illustrates the process of voltage feedforward. Both circuits in the figure are equivalent when the inputs are set to zero, and thus, have the same pole location.

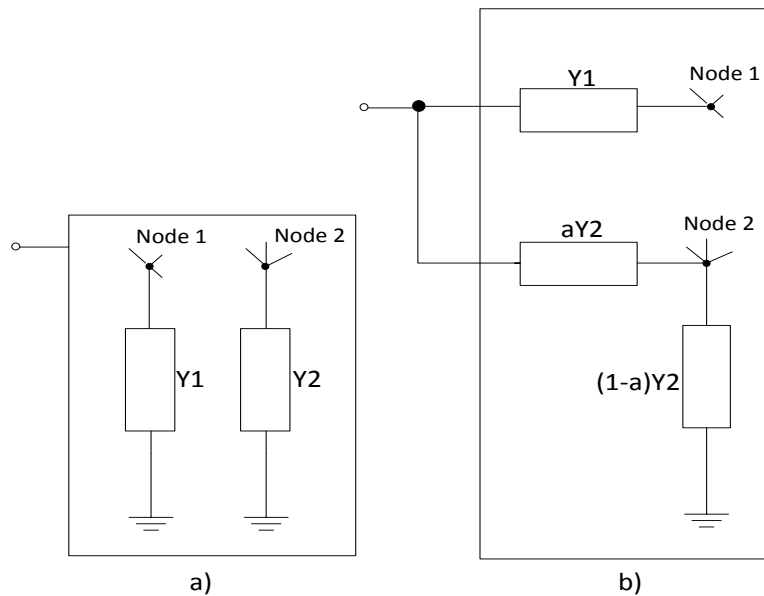


Fig. 10. Voltage Feedforward: (a) A pole generating circuit with two components connected between node 1 and 2, respectively and ground. (b) Y1 is lifted off ground completely and connected to the input; Y2 is lifted off ground partially and connected to the input.

In addition to inserting transmission zeros to the circuit, several low-power circuit design techniques are considered to minimize power consumption. An easy way is to reduce the



differential pair bias current. This could be achieved by resizing the transistors and adjusting the bias voltage while keeping the transistors in saturation [8]. Another technique to reduce the power consumption is to reduce the supply voltage of the circuit by using folded cascodes [8]. In the circuit shown in figure 7, the supply voltage can be reduced by folding the two NMOS transistors in the first biquad and the two PMOS transistors of the second biquad.

## CHAPTER III

### RESULTS

In chapter II, we discuss two main ways to insert transmission zeroes to an existing all-pole filter structure without altering its original pole position. These two methods, namely summing and feedforward, were studied in detail to understand the background necessary to implement an Inverse-Chebyshev filter function from the pre-existing low pass Butterworth filter function.

Filter structure based on a current-mode biquadratic pipe filter cell originally allowed the implementation of only all-pole filter functions such as Butterworth. In order to achieve a flat magnitude response in pass-band and steep rate of attenuation in transition-band, we want to insert arbitrary complex zeroes in the stop band and thereby implement an Inverse-Chebyshev filter function.

The biquadratic pipe filter studied in this research operates in current mode; hence, the use of current summing techniques (Chapter II) to insert arbitrary transmission zeroes seemed most promising for our study. Additionally, the functionality of the biquadratic filter cell can be explained through a simple RLC model (figure 4).

We use the RLC model from figure 4 to derive the transfer characteristics of the current  $\left(\frac{I_{out}}{I_{in}}\right)$  through each element of the RLC network. Figure 11 shows the input ( $I_{in}$ ) and the output current ( $I_{out}$ ) through each of the circuit element. We have derived the transfer functions below:

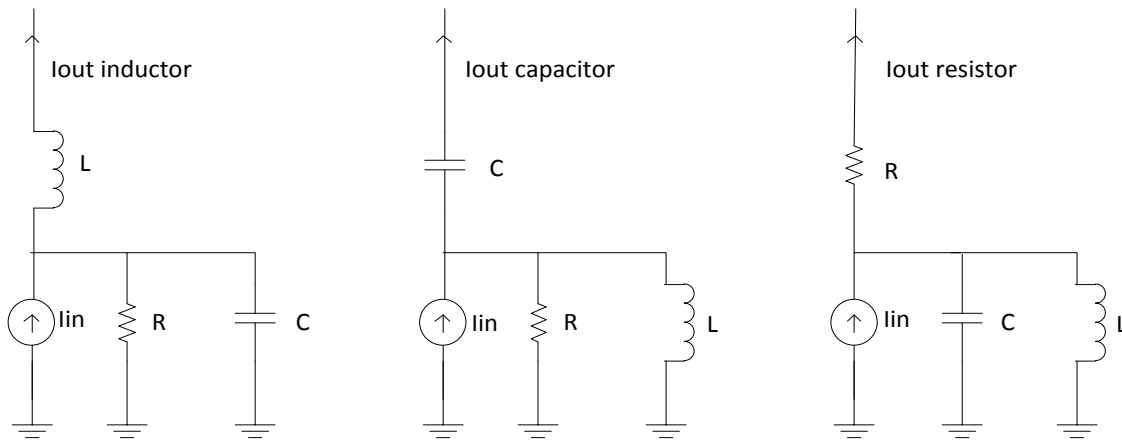


Fig. 11. Transfer Function of Current through each Element of a RLC Network

$$\frac{I_{outC}}{I_{in}} = \frac{sL||R}{sL||R+\frac{1}{sC}} \quad (18)$$

$$= \frac{s^2}{s^2+s\left(\frac{1}{RC}\right)+\frac{1}{LC}} \quad (19)$$

$$\frac{I_{outl}}{I_{in}} = \frac{\frac{1}{sC}||R}{\frac{1}{sC}||R+sL} \quad (20)$$

$$= \frac{\frac{1}{LC}}{s^2 + s\left(\frac{1}{RC}\right) + \frac{1}{LC}} \quad (21)$$

$$\frac{I_{outr}}{I_{in}} = \frac{\frac{1}{sC} || sL}{\frac{1}{sC} || sL + R} \quad (22)$$

$$= \frac{\frac{s}{RC}}{s^2 + s\left(\frac{1}{RC}\right) + \frac{1}{LC}} \quad (23)$$

From the equations derived above, we observe that the output current through the inductor has 2<sup>nd</sup> order low-pass characteristics while the output current through the capacitor has 2<sup>nd</sup> order high-pass characteristics. We also find that both the output current ( $I_{out}$  inductor and  $I_{out}$  capacitor) have the same complex poles.

In order to implement an Inverse-Chebyshev filter function, we need to implement a filter function of the form :

$$\frac{k_1 s^2 + k_0}{s^2 + s\left(\frac{\omega_0}{Q}\right) + \omega_0^2} \quad (24)$$

Theoretically, we can implement this function by summing the output current from the inductor and the capacitor after some appropriate scaling (figure 12).

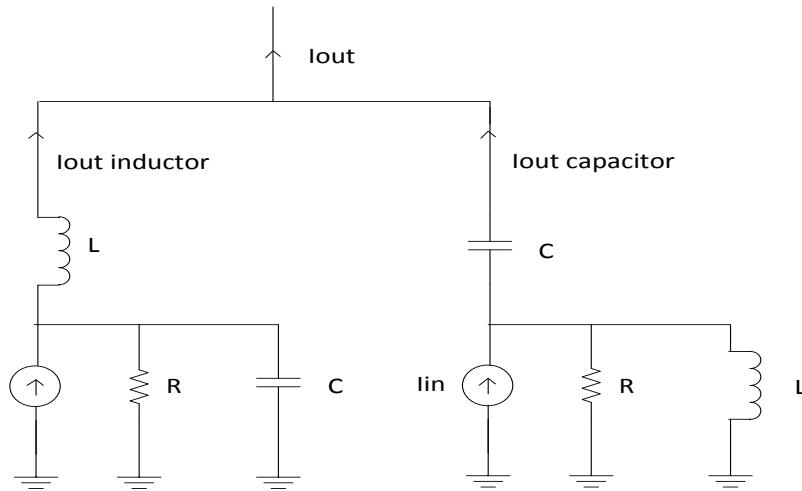


Fig. 12. Implementation of Inverse-Chebyshev Transfer Function using RLC Model

$$I_{out} = I_{out\text{inductor}} + I_{out\text{capacitor}} \quad (25)$$

$$= \left( \frac{\frac{1}{LC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}} \right) I_{in} + \left( \frac{s^2}{s^2 + s\frac{1}{RC} + \frac{1}{LC}} \right) I_{in} \quad (26)$$

$$= \left( \frac{\frac{1}{LC}}{s^2 + s\frac{1}{RC} + \frac{1}{LC}} + \frac{s^2}{s^2 + s\frac{1}{RC} + \frac{1}{LC}} \right) I_{in} \quad (27)$$

$$= \left( \frac{\frac{1}{LC} + s^2}{s^2 + s\frac{1}{RC} + \frac{1}{LC}} \right) I_{in} \quad (28)$$

We first propose a filter structure to mimic the model shown in figure 12. This structure has an  $I_{out}$  equal to the value shown in equation 28 which represents the transfer function of a notch filter function. The proposed structure is shown in figure 13.

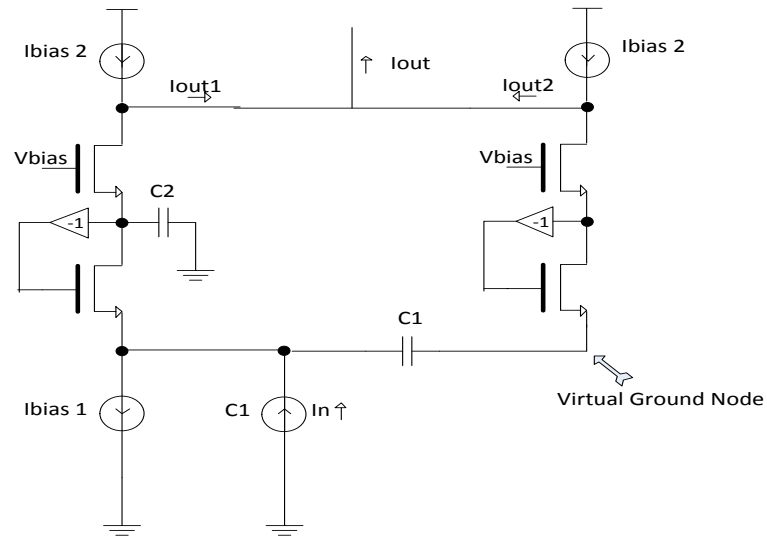


Fig. 13. Second-Order Notch Filter Function

The transfer function ( $I_{out} / I_{in}$ ) using ideal model of MOS transistors is derived below with the help of the small signal equivalent model shown in figure 14.

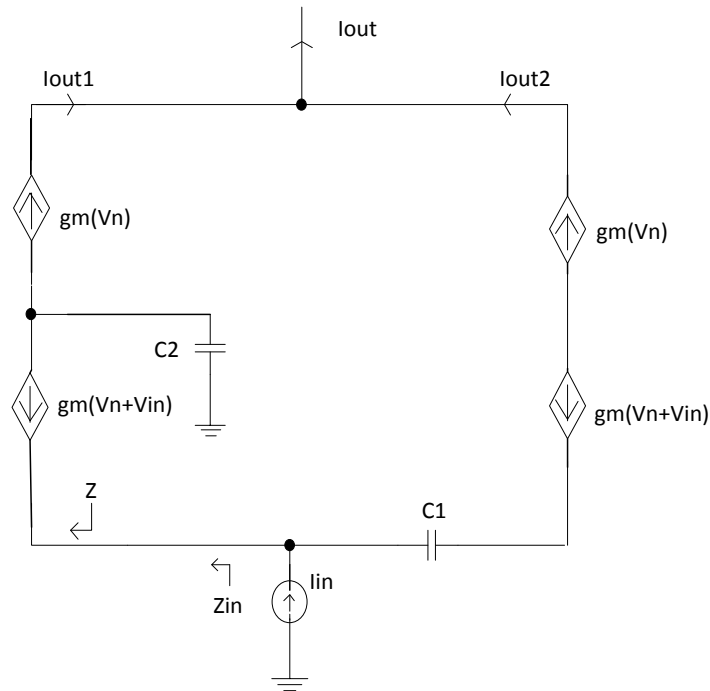


Fig. 14. Small Signal Model to derive Final Transfer Function

From equation (11) and (14), we already have the value of the current  $I_{out1}$  and the input impedance  $Z$ .

$$\frac{I_{out1}}{I_{in}} = \frac{\frac{g_m^2}{C_1 C_2}}{s^2 + \frac{g_m}{C_1} s + \frac{g_m^2}{C_1 C_2}} \quad (29)$$

$$Z = \frac{s C_2}{g_m^2 \left(1 + \frac{s C_2}{g_m}\right)} \quad (30)$$

Using the value of  $Z$  and the impedance through the capacitor  $C_1$ , we derive the transfer function from input current  $I_{in}$  to output current  $I_{out2}$ .

$$I_{out2} = \left( \frac{Z}{Z + \frac{1}{sC_1}} \right) I_{in} \quad (31)$$

$$= \left( \frac{\frac{sC_2}{gm^2 \left(1 + \frac{sC_2}{gm}\right)}}{\frac{sC_2}{gm^2 \left(1 + \frac{sC_2}{gm}\right)} + \frac{1}{sC_1}} \right) I_{in} \quad (32)$$

$$= \left( \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + gm^2 + s gm C_2} \right) I_{in} \quad (33)$$

$$= \left( \frac{s^2}{s^2 + s \frac{gm}{C_1} + \frac{gm^2}{C_1 C_2}} \right) I_{in} \quad (34)$$

Therefore,

$$\frac{I_{out}}{I_{in}} = \frac{I_{out1}}{I_{in}} + \frac{I_{out2}}{I_{in}} \quad (35)$$

$$\frac{I_{out}}{I_{in}} = \frac{\frac{gm^2}{C_1 C_2} + s^2}{s^2 + s \frac{gm}{C_1} + \frac{gm^2}{C_1 C_2}} \quad (36)$$

Equation (36) confirms the theoretical possibility of adding complex zeroes to the transfer function derived in Chapter II without disturbing the original pole location. To



further support our claim, we first realize a second-order notch filter, and consequently a third order Inverse-Chebyshev filter in  $0.18\mu\text{m}$  CMOS process using 1.8V supply voltage. We compare results between ideal and real responses of these transfer function. We also compare the rate of attenuation first between a notch filter function and a Butterworth filter function and then between an Inverse-Chebyshev filter function and Butterworth filter function.

The schematic of the circuit that has a notch in its transfer characteristics is shown in figure 15. The circuit consists of two NMOS current mirror blocks. One of the blocks is designed to behave as a second order low pass filter and the other block is design to behave as a second order high pass filter. The outputs from the two circuit blocks are combined, and the net output is observed to have a notch in its transfer characteristics as predicted by equation (36).

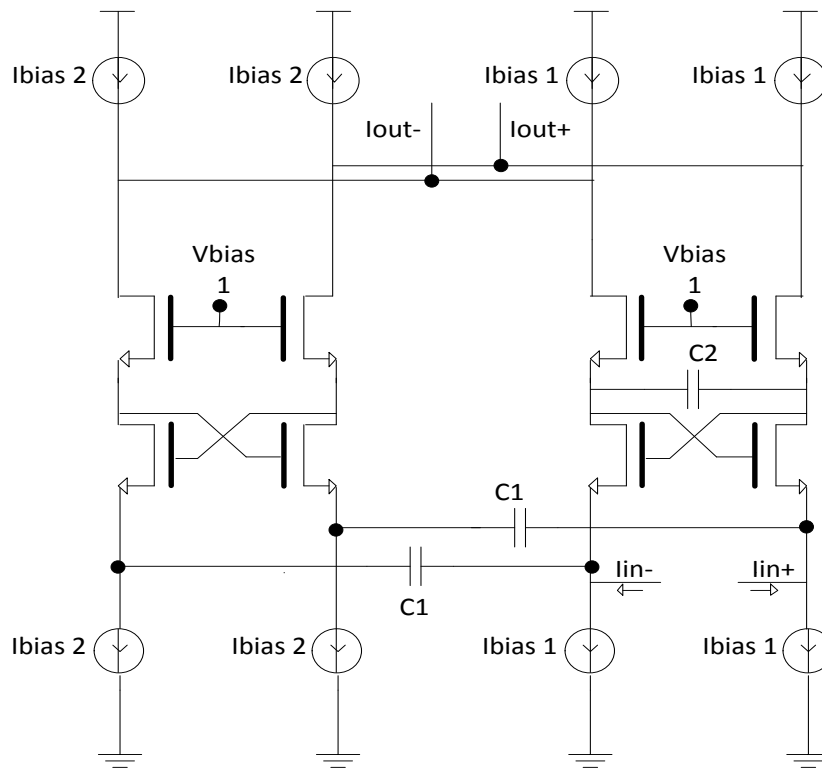


Fig. 15. Second-Order Notch Circuit Schematic

The comparison between ideal and real notch function is shown in figure 16. It can be observed that the notch occurs at a lower frequency in the case of a real response. This is because of the presence of parasitic capacitance associated with the transistors used in our implementation. These parasitic capacitors add to value of capacitances  $C_1$  and  $C_2$ , and shift the pole location to lower frequencies. We can easily shift the pole location in our design to match the ideal response.

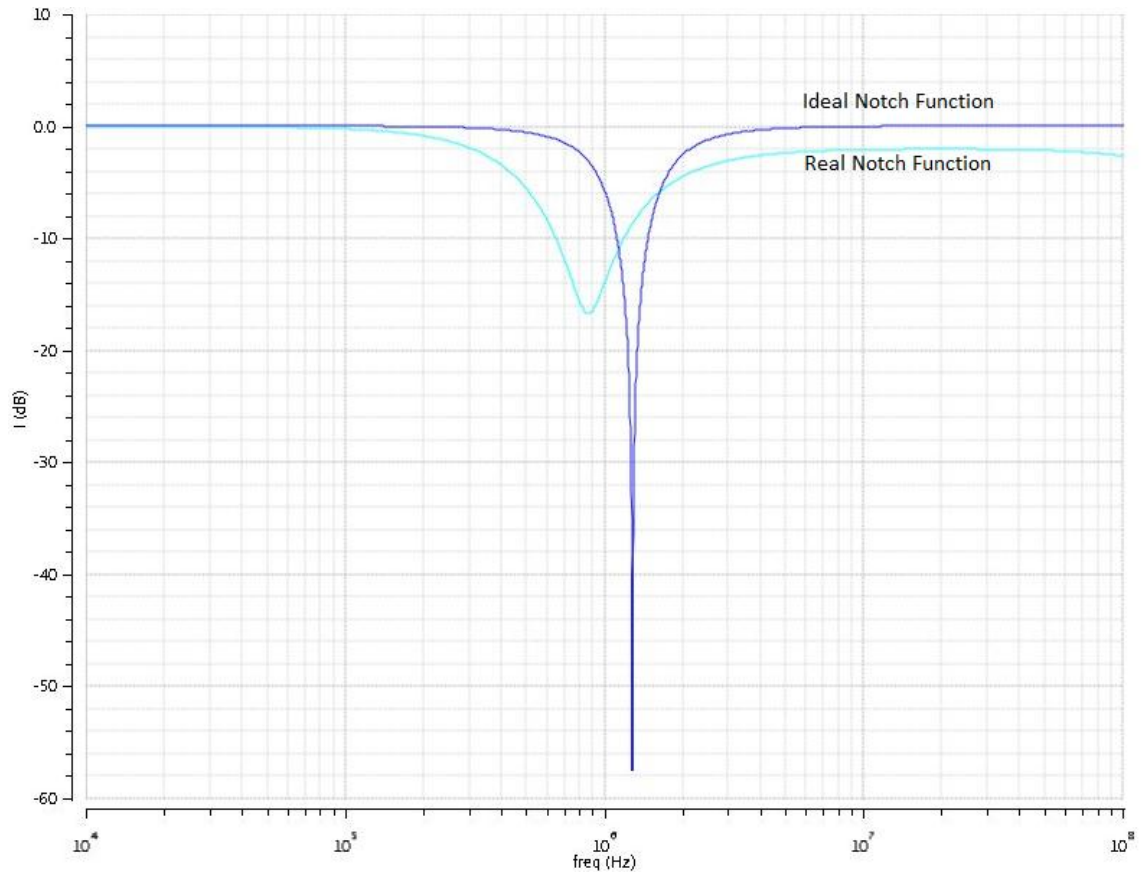


Fig. 16. Notch Filter Function Response for Ideal and Real Case

The comparison between a Butterworth filter response and Notch function filter response is shown in figure 17. As expected, we find that notch filter function has a steeper rate of attenuation in transition-band.

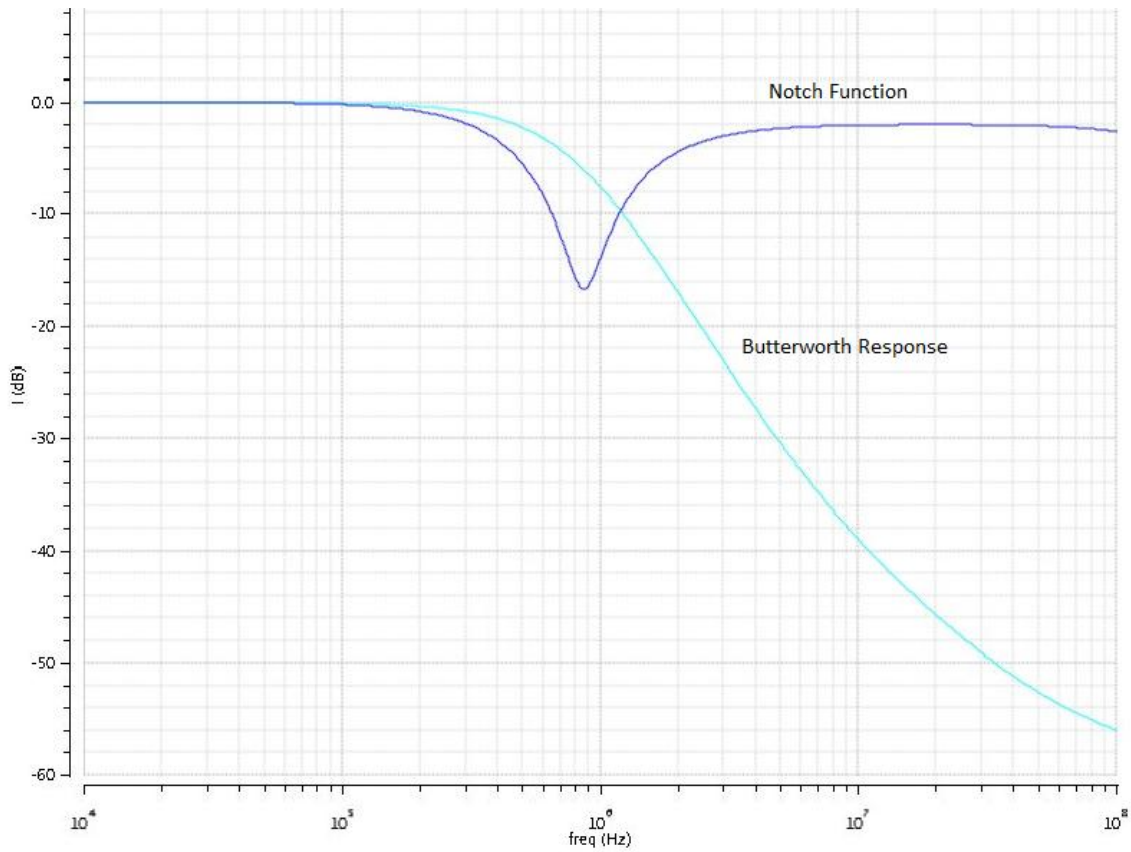


Fig. 17. Notch Filter Function Response vs. Butterworth Response

Next, we implement a second order Inverse-Chebyshev filter function. To implement this function, we developed a method to copy the current ( $I_{out2}$  in figure 14) through a PMOS current mirror and scale the current appropriately to match the coefficients for an Invere-Chebyshev transfer function.

The PMOS current mirror that is used is shown in figure 18.

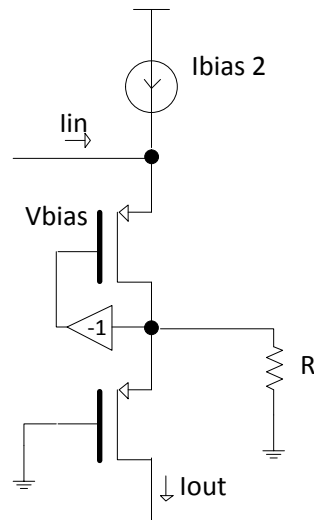


Fig. 18. PMOS Current Mirror Block with Current Scaling

The relation between  $I_{out}$  and  $I_{in}$  is derived below:

$$I_{out} = \frac{R}{\frac{1}{g_m} + R} I_{in} \quad (36)$$

Finally, we design a third order Inverse-Chebyshev filter function by inserting an additional first order filter block to our second order Inverse Chebyshev filter function. This first order filtering is performed by inserting a capacitor in the PMOS current mirror block as shown in figure 19.

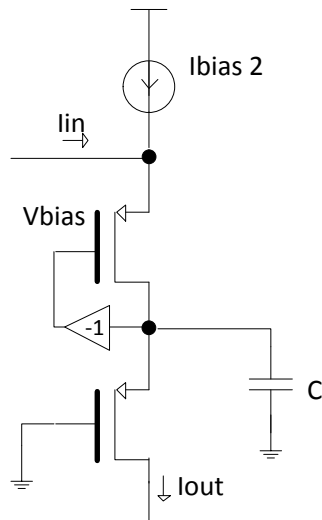


Fig. 19. PMOS Current Mirror Block with First-Order Filtering

The relation between  $I_{out}$  and  $I_{in}$  is derived below:

$$I_{out} = \frac{g_m}{g_m + sC_1} I_{in} \quad (37)$$

Figure 20 shows the schematic of a third order Inverse-Chebyshev filter function that was implemented in Cadence Analog Design Environment. This circuit has the two NMOS current mirror blocks shown in figure 15. In addition, there are two PMOS current mirror blocks needed to realize a third order Inverse-Chebyshev transfer function.

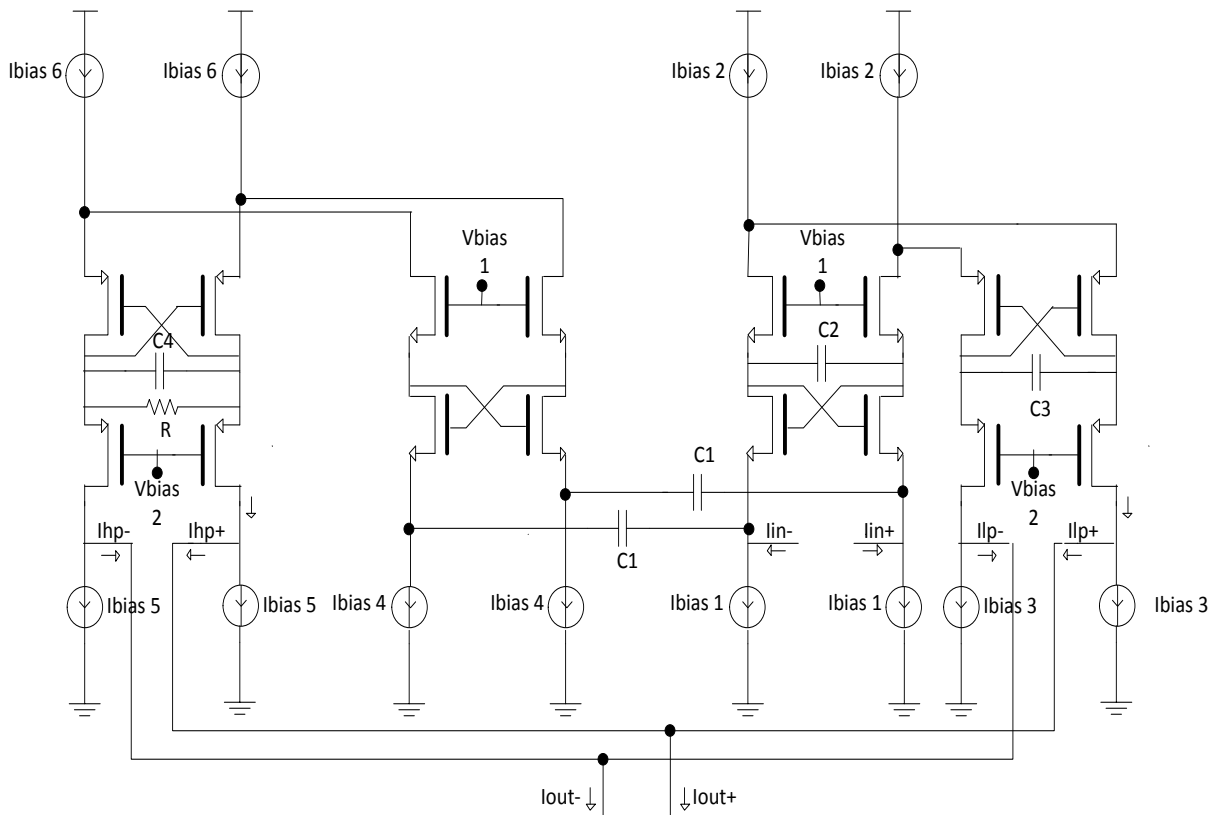


Fig. 20. Third-Order Inverse-Chebyshev Filter Schematic

As mentioned earlier, we first realize a second order Inverse-Chebyshev from the notch function described in figure 15. A comparison between a real and ideal second order Inverse Chebyshev filter response is shown in figure 21.

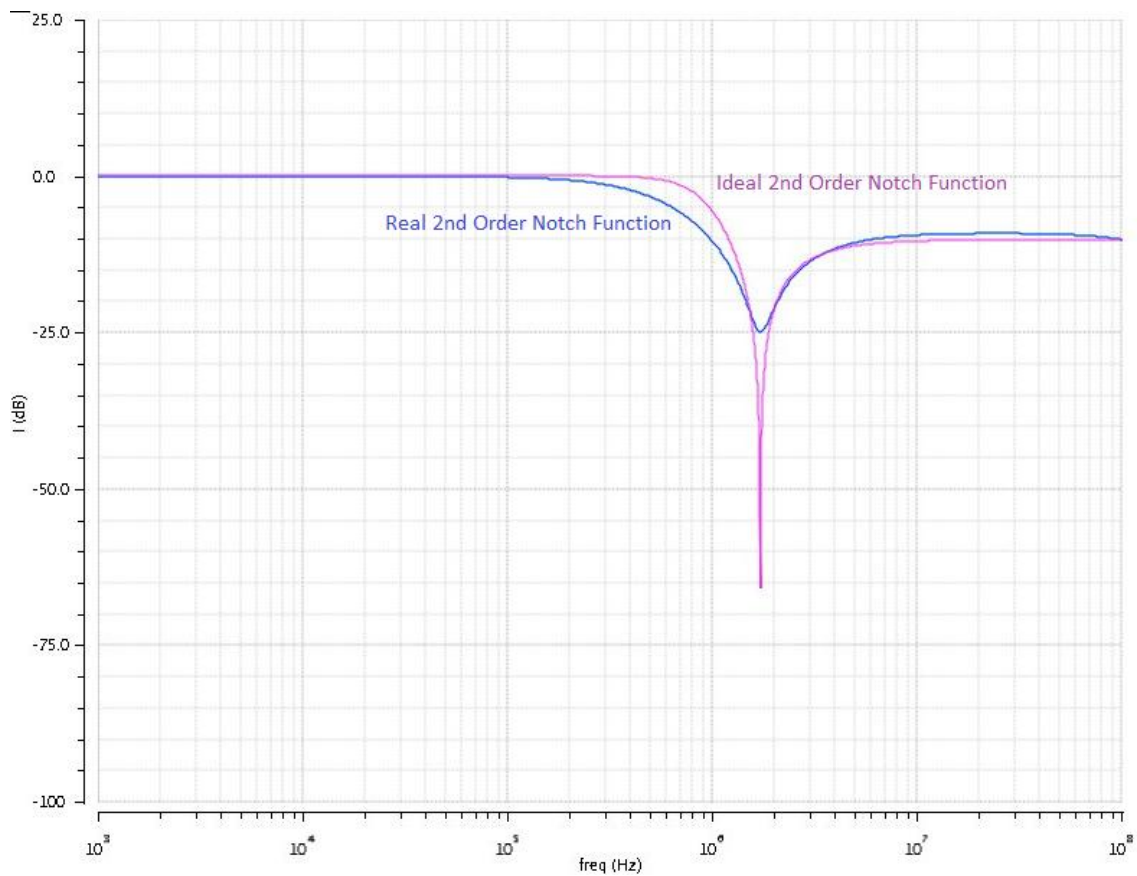


Fig. 21. Second-Order Inverse-Chebyshev Filter Response for Ideal and Real Case

After comparing the real and the ideal Inverse-Chebyshev Response, we compare the notch filter response with the Inverse-Chebyshev filter response in figure 22. From this figure, we observe that the notch function has a steep drop followed by a steep rise in its magnitude response. However, we want to attenuate all the signals in the stopband and pass only the signals in the passband. The Inverse-Chebyshev response has a much lower magnitude response in the stopband and is thus a more suitable implementation.



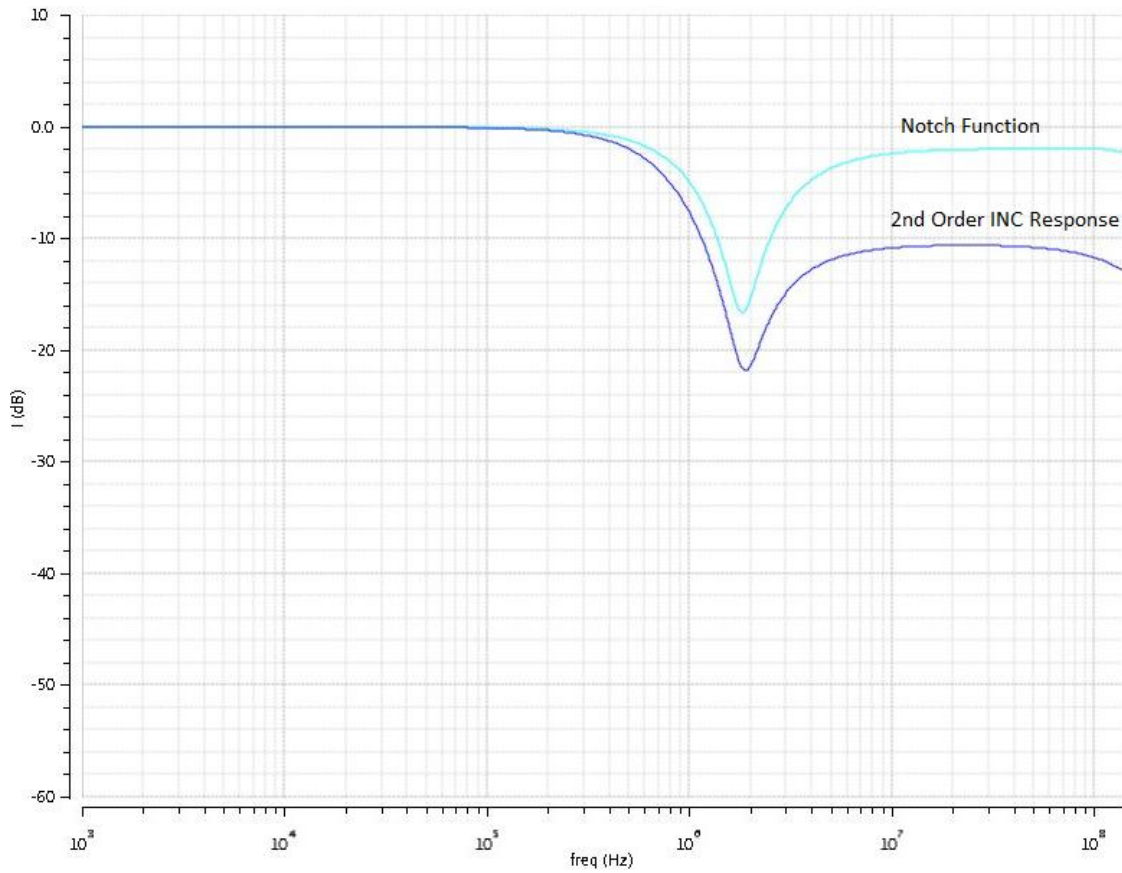


Fig. 22. Notch Response vs. Second-Order Inverse-Chebyshev Filter Response

Next, we implement a third order Inverse-Chebyshev filter function in order to achieve a much lower rate of attenuation in the stopband. Figure 23 shows a comparison between a second and third order Inverse-Chebyshev filter response.

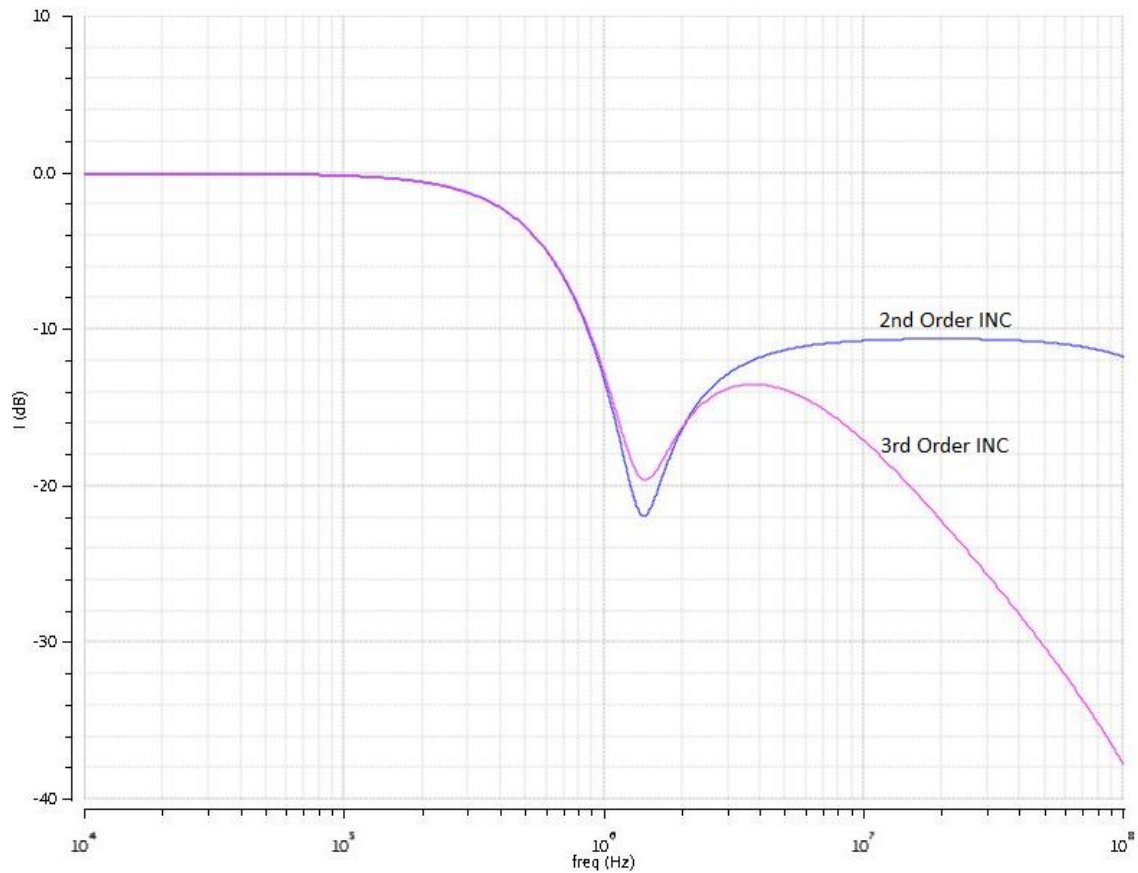


Fig. 23. Second-Order vs. Third-Order Inverse-Chebyshev Filter Response

Following our comparison between second and third order Inverse-Chebyshev filter function, we evaluate the difference between a third order Butterworth response and third order Inverse-Chebyshev response. We find that the Inverse-Chebyshev filter function has a steeper attenuation rate in the transition band and a lower group delay factor. We also find that a Butterworth response has greater suppression of unwanted signals at higher frequencies. Figure 24 confirms our results.

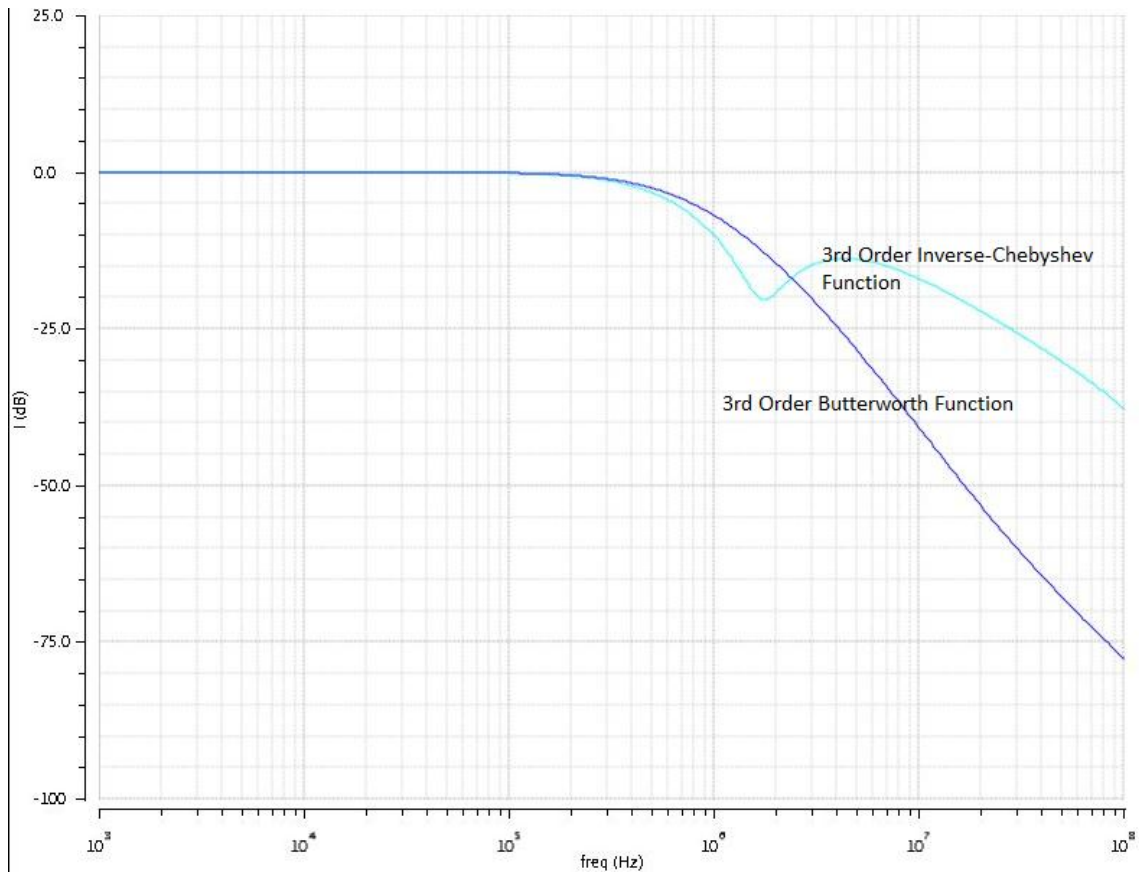


Fig. 24. Third-Order Inverse-Chebyshev Filter Response vs. Third-Order Butterworth Response

Finally, we first plot the real third order Inverse-Chebyshev transfer function in figure 25 and then we compare the real response with the ideal response of a third order Inverse-Chebyshev filter function in figure 26.

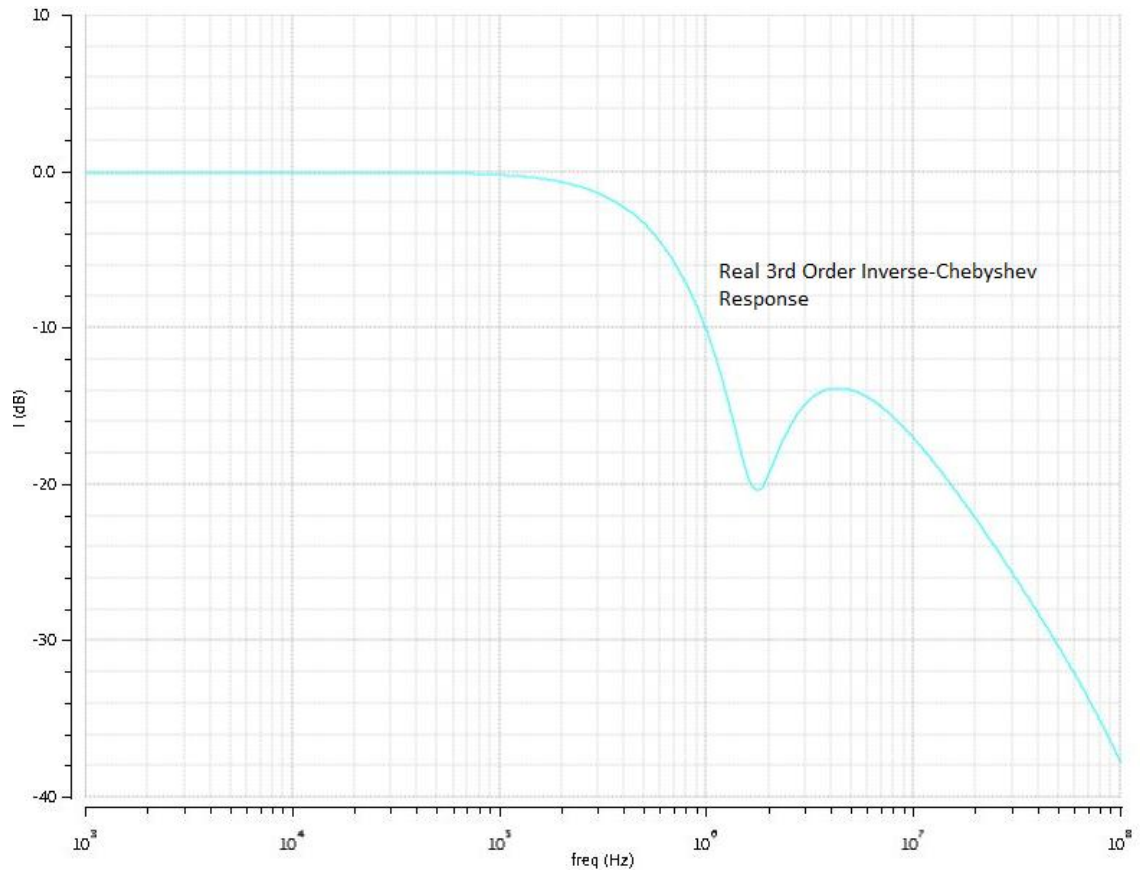


Fig. 25. Real Third-Order Inverse-Chebyshev Transfer Function

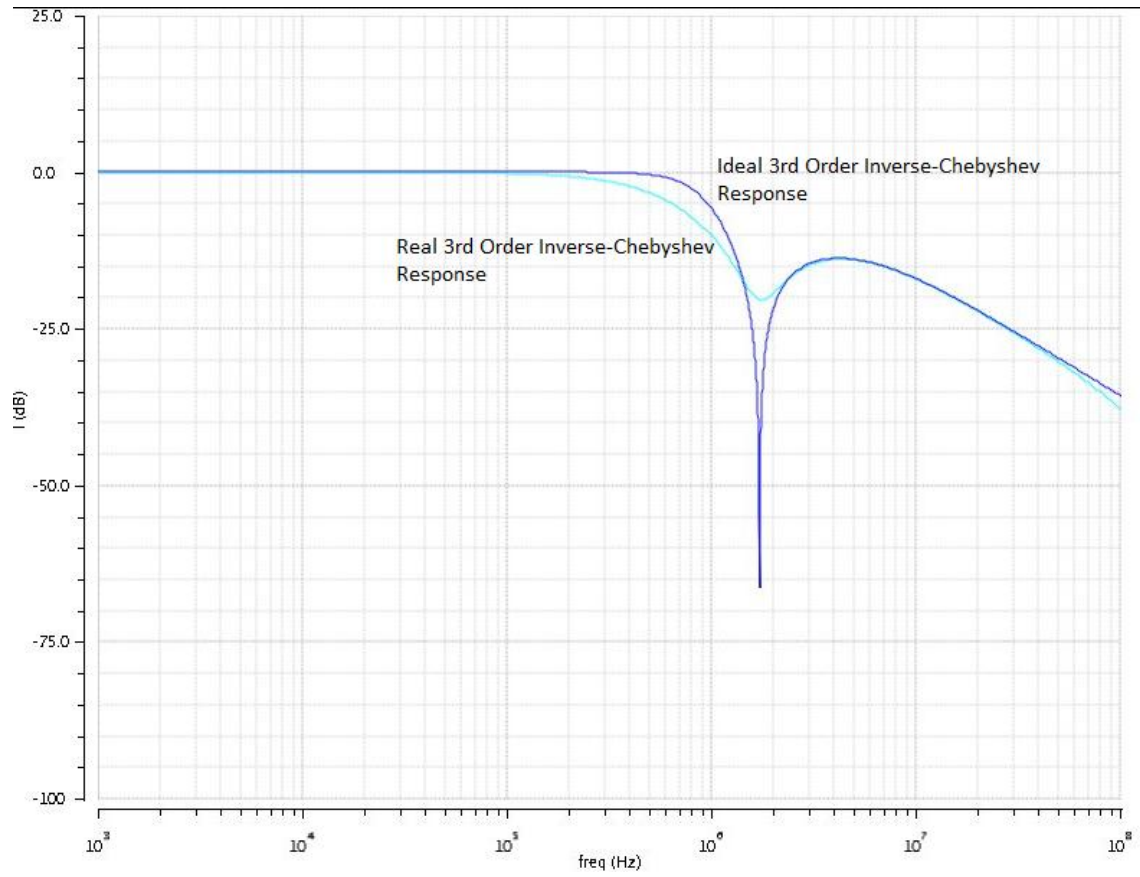


Fig. 26. Third-Order Inverse-Chebyshev Filter Response for Ideal and Real Case

## CHAPTER IV

### SUMMARY AND CONCLUSIONS

Low-pass all pole current-mode filter structure is implemented in the signal path of a direct-conversion receiver architecture to perform higher order filtering of unwanted out-of-band signals. A modified filter structure is then designed by adding arbitrary transmission zeroes in the transfer function. With the aim to achieve a flatter magnitude response in the passband and a steeper rate of attenuation in the transition band, we designed a third order Inverse Chebyshev Transfer function

It is important to note that higher order filtering function can be easily realized by cascading several NMOS and PMOS filtering structures. For example, a fifth order Inverse-Chebyshev function can be realized by cascading a second order NMOS block, with a second order PMOS block followed by a first order NMOS block.

The addition of arbitrary zeroes to the all pole filter function makes it possible for us to implement any desired filter function. For example, we can easily implement an elliptical filter function if we desire a much steeper transition for a comparatively lower filter order. However, these elliptical filters have ripples in the passband and the stopband. Our filter structure gives us the freedom to compare different filter functions.

Apart from designing a more general filter function, we may adapt different methods to further optimize our design. Several low-power circuit design techniques may be considered to minimize power consumption. For example, we can minimize the power consumption by reducing the supply voltage of the circuit by using folded cascodes within each biquad block.

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## CONTACT INFORMATION

Name: Diganto Choudhury

Professional Address: c/o Dr. Aydin Karsilayan  
Department of Electrical and Computer Engineering  
318-C WERC  
Texas A&M University  
College Station, TX 77843

Email Address: digantochoudhury@gmail.com

Education: B.S., Electrical Engineering, Texas A&M University,  
May 2012  
Honors Undergraduate Research Fellow  
Engineering Scholars' Program  
Eta Kappa NU