LOW POWER ARCHITECTURE AND CIRCUIT TECHNIQUES FOR HIGH BOOST WIDEBAND GM-C FILTERS

A Thesis

by

MANISHA GAMBHIR

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2006

Major Subject: Electrical Engineering

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ABSTRACT

Low Power Architecture and Circuit Techniques for High Boost Wideband Gm-C Filters. (May 2006)

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Dr. Jose Silva-Martinez

With the current trend towards integration and higher data rates, read channel design needs to incorporate significant boost for a wider signal bandwidth. This dissertation explores the analog design problems associated with design of such 'Equalizing Filter' (boost filter) for read channel applications.

Specifically, a 330MHz, 5^{th} order Gm-C continuous time lowpass filter with 24dB boost is designed. Existing architectures are found to be unsuitable for low power, wideband and high boost operation. The proposed solution realizes boosting zeros by efficiently combining available transfer functions associated with all nodes of cascaded biquad cells. Further, circuit techniques suitable for high frequency filter design are elaborated such as: application of the Gilbert cell as a variable transconductor and a new Common-Mode-Feedback (CMFB) error amplifier that improves common mode accuracy without compromising on bandwidth or circuit complexity. A prototype is fabricated in a standard 0.35μm CMOS process. Experimental results show -41dB of IM3 for 250mV peak to peak swing with 8.6mW/pole of power dissipation.

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CHAPTER I

INTRODUCTION

Popularity of portable applications for consumer electronics has set the focus of the modern design on low power systems. At the same time, increased demand of personal computers and interest in gadgets like portable music players, DVD-CD players, digital cameras and portable notebooks have triggered the rapid evolution of storage devices.

Storage devices can be classified on the basis of their performance, cost and maximum capacity. Applications and popularity of a particular medium is mostly decided by these parameters. Optical disk based storage systems are pervasive in the segment of software and music distribution. However large access time renders them ineffective for real time applications. On the other hand flash based systems have access time in the order of nanoseconds; but are too expensive for storage of Giga-bytes of data [1]. While recent advances in optical disks systems and flash storage have been significant, the area of mass storage is still ruled by magnetic disk drives. Hard-disk drives employed in ever ubiquitous personal-computers, portable notebooks and high end music players are just few of its applications**.** In the modern world of portability and speed, factors like low power consumption, small form factor, high density, and faster access have become the driving factors for the evolution of Hard Disk Systems.

This thesis follows the format of *IEEE Journal of Solid State Circuits.*

A. Read Channel Architectures

Fig. 1 shows a typical read channel for a disk drive system. It consists of a magnetic head which relays the read signals to the preamplifier. A variable gain amplifier is used to control the channel gain. In some architectures, it is also used to introduce some pre-distortion for MRA (Magnetic Resonance Asymmetry) [2]. Low pass filter provides necessary anti-aliasing filtering before digitization and may also embed the equalization gain. Since the dynamic range of the system is quite moderate (around 40dB) 6 bit of digitization is done using an ADC and the digital bits are passed to the digital signal processing core. This core adaptively controls the channel gain and timing loops.

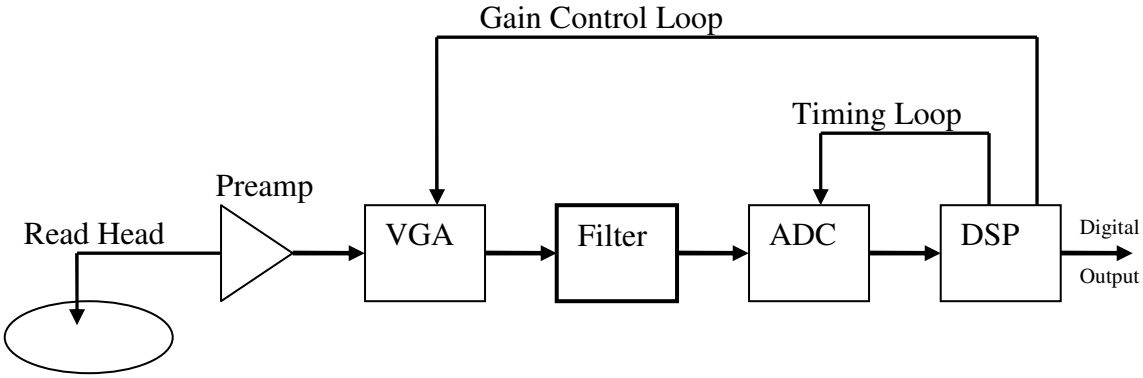

Fig. 1. Disk-Drive read channel system

The magnetic pulses read from the media are essentially Non-Return-to-Zero (NRZ) format. Earlier read channels used to employ a synchronized peak detector to

detect the polarity of the pulses. However modern advancements in the read channel Systems have led to more sophisticated pulse formats and detectors including Partial-Response-Maximum-Likelihood (PRML) or Extended-PRML (EPRML) detection. Thus, with increasing recording densities more complex equalization targets have been used [3]. Further, ever increasing bandwidth implies that the transition between read pulses have become smaller to give rise to significant Inter Symbol Interference (ISI). In order to compensate for the channel losses and effectively slim the data pulses, high frequency boosting is commonly employed in such systems. Channel equalization could be carried out in the analog and/or digital domain; the partitioning of equalization gain between analog and digital domains is dictated by system integration issues, complexity of design and power trade-offs. Any magnitude equalization carried in digital domain results in boosting of the quantization noise of the ADC that follows the filter [1], thus degrading the SNR. Therefore it is desirable to embed the maximum boost in the analog filter. Boost filters provide the necessary low pass filtering before the ADC along with a programmable high frequency gain for equalization around the cut-off frequency. This research focuses on different aspects concerning design of this critical block.

B. Current Trends in Boost Filter Design

Need to support high data rates imply wide bandwidths. CMOS wideband gm-C filters have been reported with bandwidth up to 550MHz [4]; but the boost filter designs reported so far have confined to the bandwidth of 100-200MHz [5-8] and up to 14dB

boost. For high speed, high density data systems, it is desirable to have maximum boost gain up to 24dB [9]. The design complexity lies with the difficulties associated with achieving high boost gains for a wideband structure with a reasonable power budget. For example, a 24dB boost with 330MHz of bandwidth has equivalent gain-bandwidth product of 5.2GHz while f_T of NMOS devices in a typical 0.35μm technology is less than 15GHz. The design reported here is a fifth order Butterworth filter with 3dB bandwidth of 330MHz, a programmable boost of up to 24dB and power dissipation of 43mW.

C. Organization of the Thesis

The thesis has been organized to provide design perspective for architecture as well as circuit techniques for high frequency filters with programmable boost. The focus has been kept on the analysis of the new techniques proposed and the issues like programmability and tuning which can be employed using standard techniques have only been briefly touched. Chapter II of this paper analyzes previously reported boost architectures with the aim of finding causes of power efficiency loss in different approaches. This also forms the basis of deriving a new and power-efficient architecture. Chapter III outlines the design of transconductors as basic building blocks. Different considerations regarding the design of core and boost transconductors (OTAs) are discussed. And application of Gilbert cell as a widely programmable OTA, with constant input and output parasitic, is illustrated. In Chapter IV a CMFB technique suitable for

wideband low power design is introduced. Chapter V elaborates on the simulation and experimental results obtained while comparing the performance with other reported filters. It is shown that the reported solution is the most power efficient structure with the highest boost and bandwidth in the class of filters with similar dynamic range. In Chapter VI conclusions and future directions are presented.

CHAPTER II

FILTER ARCHITECTURE

Choice of filter architecture is dependent on the desired magnitude and phase response. read channel filters typically use seventh order Equiripple phase approximation with up to 14dB boost [5-8]. Such choice is based on the fact that Equiripple response has a flat group delay in the pass band and much beyond. For fast high data density systems, it is desirable to have maximum boost gain up to 24dB [9]. Approximation with higher magnitude roll-off rate such as Butterworth, or Inverse Chebyshef approximation may be used provided that the in-band phase error is corrected using Digital Signal Processing [2].

Fig. 2(a) shows the magnitude response of the 5^{th} order Butterworth, a 7^{th} order Equiripple delay and a 4^{th} order Inverse Chebyshev approximation (with stop band rejection of -37dB). Fig. 2(b)-(c) shows the pole zero locations for the seventh order Equiripple delay and fourth order Inverse Chebyshev transfer function. While the 4^{th} order Inverse Chebyshev provides a similar attenuation as the 5^{th} order Butterworth at three times the corner frequency, the later is preferred because of its better group delay properties. Further, realization of Inverse Chebyshev response requires additional hardware for the transmission zeros. As illustrated from the plotted responses, a seventh-order Equiripple delay filter provides an attenuation of -35dB at three times the corner frequency while a fifth-order Butterworth approximation provides a stop band rejection of -47dB at such frequency. The filter's order reduction saves power, die area, and

device noise. Thus a 5th order Butterworth approximation is selected over a typical 7th order Equiripple. The entire magnitude equalization is done in analog while the phase response of the Butterworth approximation is compensated in the digital domain. Shifting the phase equalization in digital domain also has the advantage of ease in scaling with newer technological nodes. Comparisons of these three different filter approximations are illustrated in table 1.

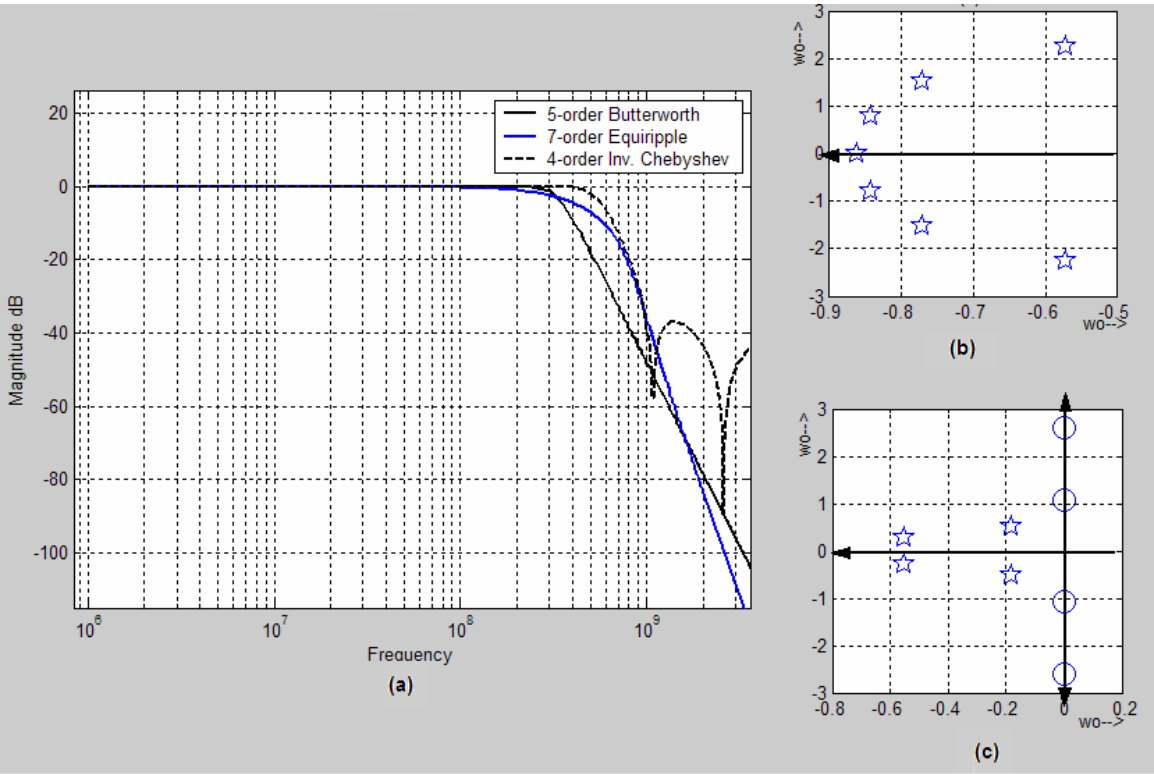

Fig. 2. (a) Magnitude response of 5th order Butterworth, 7th order Equiripple delay and a 4th order Inverse Chebyshev filter (ω_o = 330MHz) (b) Pole location of the Equiripple delay filter (c) Pole and zero location for the Inverse Chebyshev filter

TABLE 1

COMPARISON OF DIFFERENT FILTER APPROXIMATIONS

	Attenuation (at $3\omega_o$)	Group Delay flatness	Other factors
5th Order Butterworth	-47dB	Corrected in digital	All pole transfer function
7th Order Equiripple	-37dB	Best	All pole transfer function
4th order Inv-Chebyshev	-37dB	Worst	Transmission zeros in transfer function

It is desirable that the filter's group delay response does not change with the applied boost. For this reason, boosting is done using two real zeros symmetrically placed around $j\omega$ axis. Phase of these symmetrically placed zeros cancels each other so that the phase response of the filter remains independent of the boost setting. This also enables the phase calibration to be independent of boost setting. Fig. 3 shows the location of implemented poles and zeros in the complex frequency plane. For a Butterworth response, all poles are placed on a circle in the s-plane that is centered at the origin and has a radius ω_o. It can be shown that for a 24dB (0dB) boost gain, zeros are to be placed at $\pm\frac{\omega o}{4}(\infty)$.

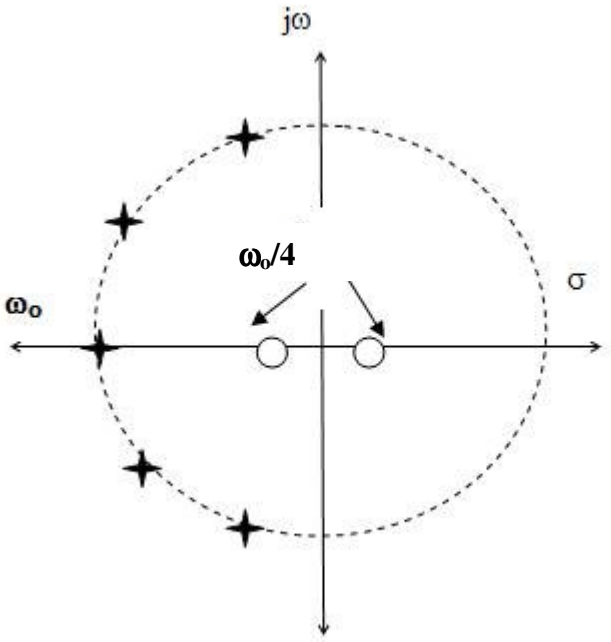

Fig. 3. S-plane location of poles and zeros for 5th order Butterworth, boost filter

Having determined filter's approximation and the pole-zero constellation, problem of implementing high boost for wideband structures is analyzed on an architectural level. Following section focuses on the preciously reported boost architectures, their analysis from power efficiency perspective and derivation of a power-efficient architecture which is suitable for implementing high boost gain.

A. Previous Work on Boost Filter Architectures

Filter architectures reported in [5-8] implement boost gain of 12-14dB in 43MHz to 200MHz bandwidth. This section examines the drawbacks associated with these

structures when used for boost gain around 24dB and a bandwidth that exceeds 300MHz.

A single terminated ladder based boost filter is reported in [5] for DVD applications. The fifth order representation of the reported filter is shown in Fig. 4. Boost is realized using a feed forward path injecting the current proportional to the input into the third integrating node.

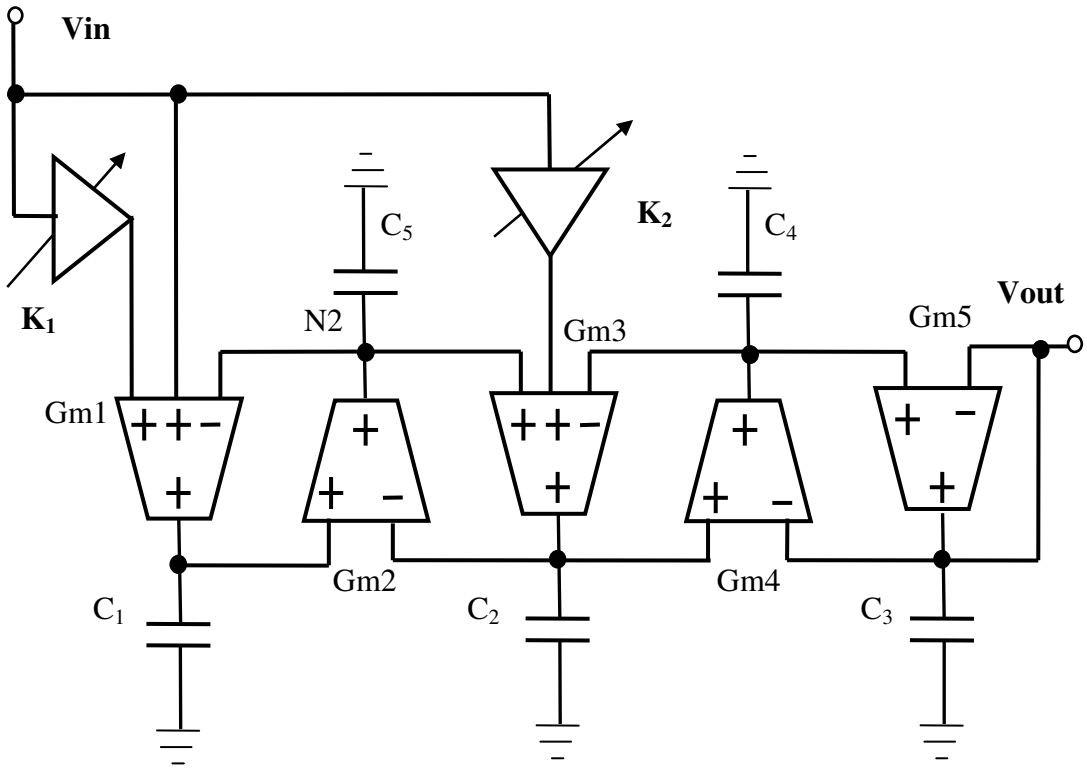

Fig. 4. Singly terminated ladder based boost architecture

Ladder based architecture are typically less sensitive towards temperature and process variations [10]. However, ladder structures consist of OTA's that are connected 'back-to-back' forming feedback loop amongst two OTA's. Any transfer-function shaping using feedforward injection becomes complex as the feedforward path does not always touches all the feedback loops of the ladder structure. This fact can be easily followed from Mason's rule [11] and is mathematically illustrated in context of the architecture in Fig. 4. The normalized transfer function H(s) for this architecture is given by:

$$H(s) = \frac{K_2\left(s^2 - 1\right) + K_1 - 1}{D(s)} = \frac{K_2 s^2 - 1 + \left(K_1 - K_2\right)}{D(s)} \tag{2.1}$$

where K_1 and K_2 are the first and second feedforward path gains respectively and D(s) represents a fifth order function. The intended numerator is of the form: $K_2 s^2 - 1$. The input is directly gained and injected into the third integrating node to create the desired $K_2 s^2$ term in numerator of (2.1). However K_2 path also introduces a low pass feed-through term $-K_2$ which needs to be cancelled through the additional feedforward path consisting of K_1 ($K_1 = K_2$). Since unfiltered input is amplified and injected, all frequencies see a large gain. Creating large gains at frequencies much lower than the filter's cut-off frequency and then canceling this undesired component (using an additional K_1 path) results in loss of power efficiency.

Apart from having an additional cancellation path, injecting amplified low frequency components through the feedforward path (K_2) also has an implication that the intermediate node such as N2 (Fig. 4) experiences large gains at low frequencies. Fig. 5

shows the node swings at intermediate nodes. It is to be noted that the node scaling can be done to prevent large swings at N2, but only at expense of additional power.

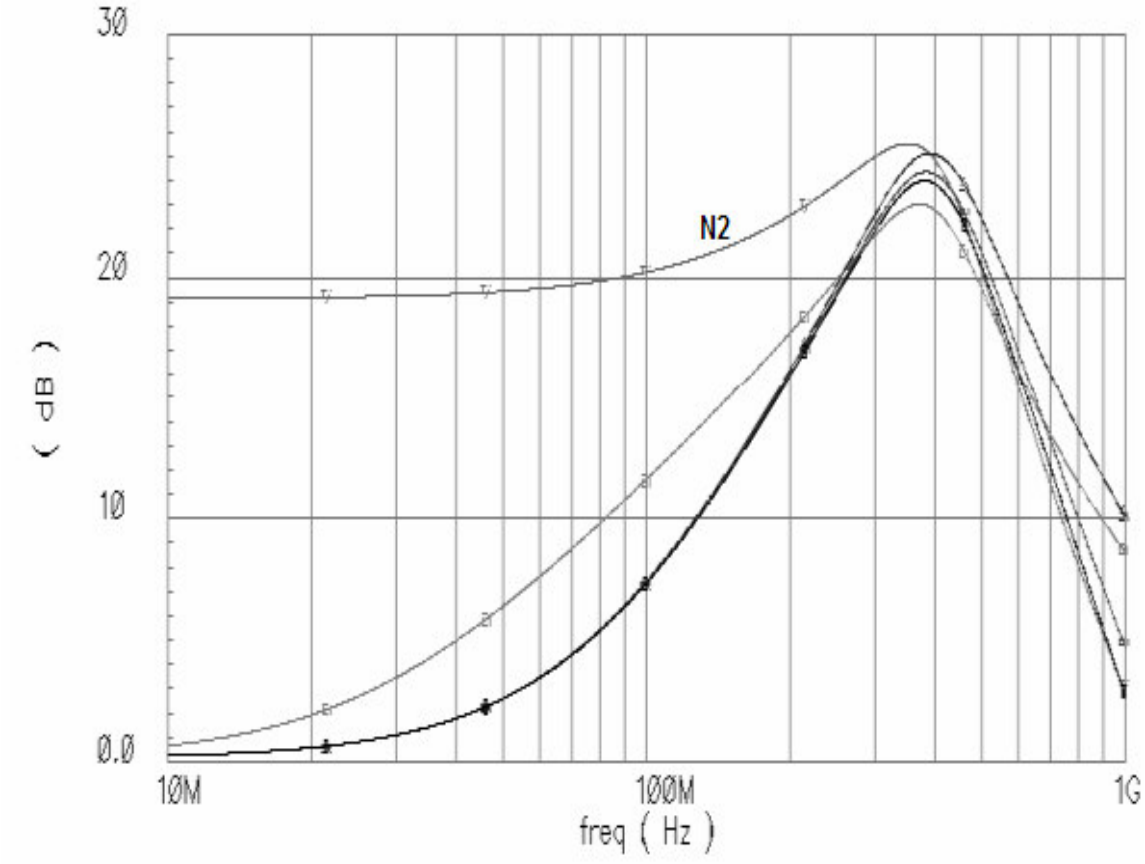

Fig. 5. Node Swings at intermediate nodes of the boost architecture based on ladder structure of Fig. 4.

The third drawback of such scheme is the fact that the entire boost gain is embedded in a single gain stage constituting of K_2. This implies that for 24dB boost gain, the transconductance of the boost OTA needs to be 16 times of that of main path OTA that injects current in to the same node.

Another class of boost filters use differentiation as one of the signal shaping function. A differentiator is used in [6] to inject differentiated input signal into the low pass node of the biquad to generate two real zeros. While there is no injection of large low frequency signal currents, keeping the differentiator parasitic poles far away from ω_o significantly increases the power consumption [7]. Also, the entire boost gain is realized in a single stage using two zeros created by the differentiator, imposing large power requirements on its realization. The topology employed in [7] makes use of the differentiator pole as a part of a third order cell and two such cells are used to realize the complete transfer function. Note that, this topology splits the boost gain amongst two cells. However, this scheme introduces one real pole for each zero realized by the differentiator, limiting the types of filter responses that may be realized. For example a fifth order Butterworth filter cannot be realized using this scheme.

A cascade structure reported in [8] splits the boost gain amongst two biquads, realizing a zero each. Fig. 6(a) shows the biquad section of this architecture which implements a single programmable zero apart from second order filtering. The equivalent representation for this structure using integrators is shown in Fig. 6(b).

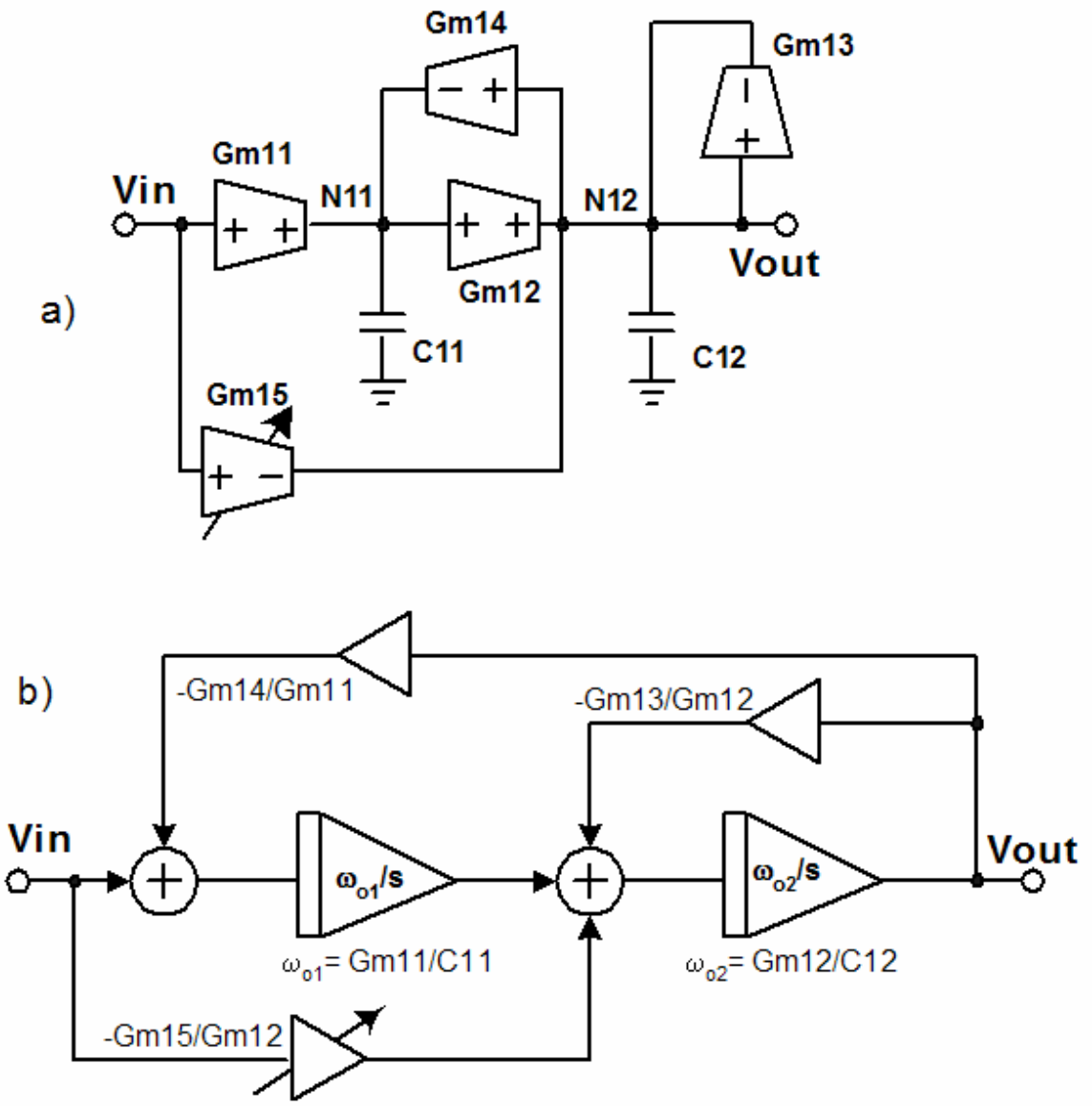

Fig. 6 (a) Biquad section of the filter reported in [8] (b) The equivalent integrator based representation

For a better understanding, biquad of Fig. 6(a) can be represented by an '*equivalent-impedance'* model by observing the emulated impedance at node N12. The lossy OTA Gm13 is replaced by a resistor (1/Gm13) and the gyrator (Gm12, Gm14,

C11) is replaced by an equivalent inductor. Note that, for the simplifying assumption that node N11 is lossless the gyrator emulates an ideal grounded inductor. Further, the feedforward integrating path and the programmable boost path of Fig. 6(a) are preserved to arrive at representation in Fig. 7.

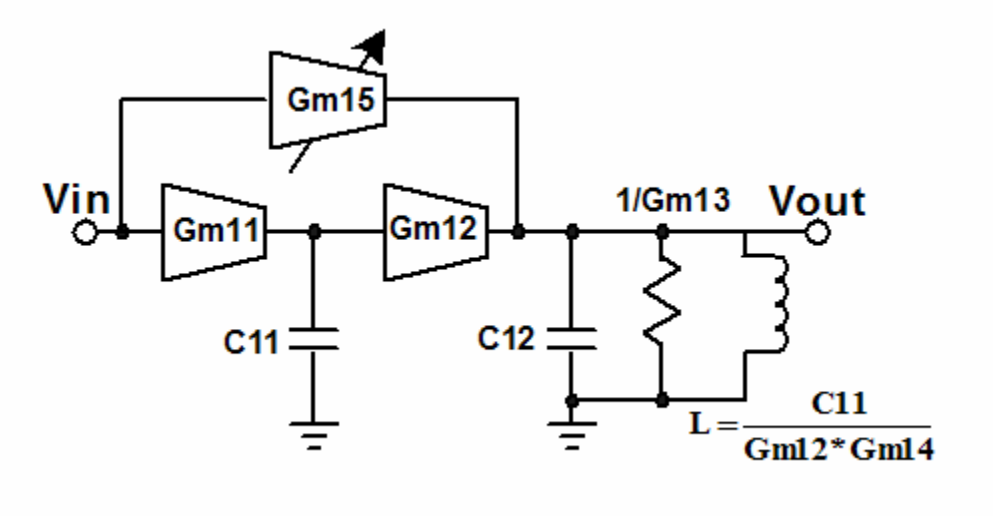

Fig. 7. Equivalent representation of the biquadratic section of Fig. 6(a)

Boost OTA Gm15 injects unfiltered signal current from the input of the biquad into the output node N12. Low frequency component of this injected current is absorbed almost entirely by the emulated inductor. This superfluous low frequency current has an indirect impact on power efficiency. Writing the current equation at low frequency or DC for node N12 under the simplifying assumption that node N11 is lossless:

$$Gm15\ Vin = Gm12\ V_{N11} \qquad @\ \text{low frequencies} \qquad (2.2)$$

Thus, in absence of any node scaling, the low frequency swing at node N11 increases from the nominal value of unity in accordance to the boost setting.

Analytically, the low frequency component of the current generated by Gm15 is supplied by the gyrator, which makes node N11 experience gain at lower frequencies. The response of different node for this structure (without node scaling) has been shown in Fig. 8.

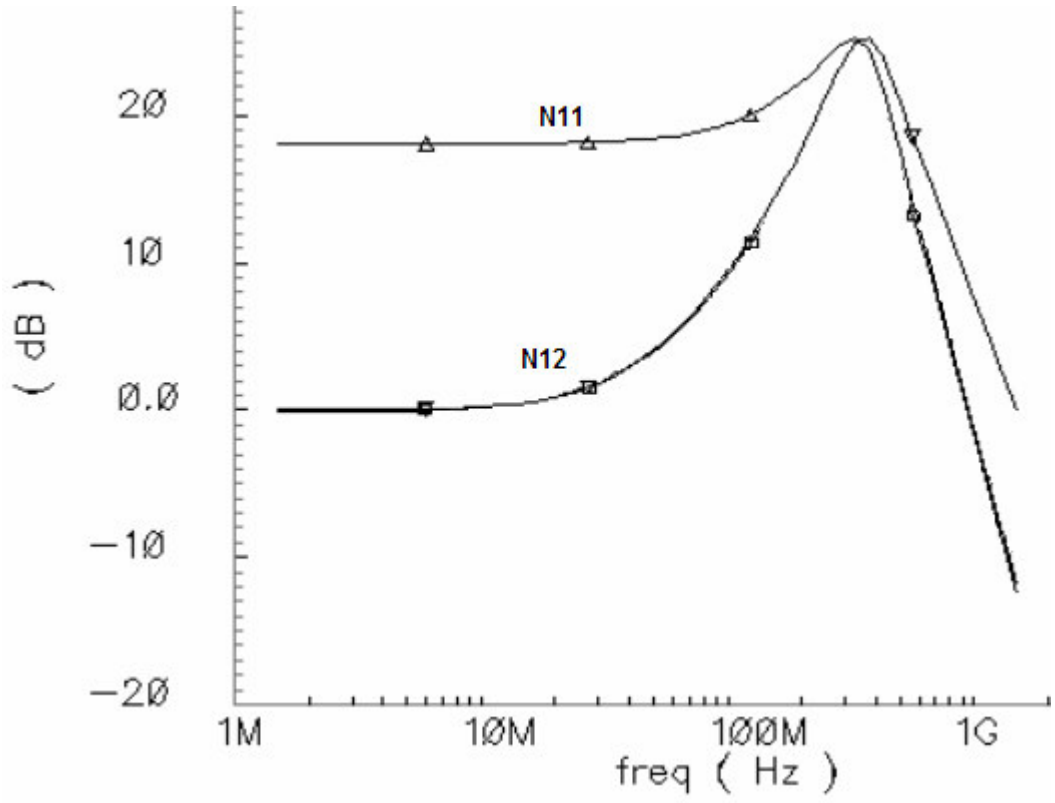

Fig. 8. Node swings for the biquadratic section shown in Fig. 6

If node scaling is employed to alleviate this problem, the transconductor Gm12 has to be as large as the boost OTA, to maintain swings similar to Vin at node N11. Notice that for 24dB boost, boost OTA is about four times as large as the input OTA and there are two such biquadratic blocks in the entire filter. Further, parasitic capacitance at

node N12 become prohibitively large as it is driven by two large OTAs (Gm15 and Gm12). Thus, this scaling up of transconductors adversely affects the power efficiency of this architecture especially when used for wideband filters

B. A Power Efficient Boost Architecture

A power efficient boost filter architecture is derived based on careful analysis of the demerits of previously discussed architectures. In order to be able to split the boost gain into two gain stages, cascade based architecture is preferred. The cascaded representation of the transfer function is given by:

$$H_{boost}(s) = \frac{\omega_o s\sqrt{K} + \omega_o^2}{s^2 + \frac{\omega_o}{Q1}s + \omega_o^2} * \frac{\omega_o s\sqrt{K} - \omega_o^2}{s^2 + \frac{\omega_o}{Q2}s + \omega_o^2} * \frac{\omega_o}{s + \omega_o} \qquad (2.3\text{-a})$$

here, Q1 and Q2 refer to the quality factor of biquad 1 and 2 and their values are 0.618 and 1.618 respectively. K determines the placement of zeros and its value ranges from 0 to 16 for 0 to 24dB high frequency boost. Each biquad realizes a real axis zero in addition to two poles and the gain is split between two stages in cascade.

One way to implement the zeros is to add (subtract) lowpass and bandpass voltage signals. This is done in [8] by injecting amplified current proportional to the unfiltered input voltage into the bandpass impedance node (with parallel resonator of a resistor, capacitor and emulated inductor as in Fig. 7). Alternately, if bandpass current is added (subtracted) from lowpass current, zeros can be directly constructed without creating the superfluous low frequency current. Thus, scaling up the transconductors, as

explained in previously, is avoided. Conceptual realization (using integrators and weighted summers) of this scheme is shown in Fig. 9. First four integrators (INT1-4) and two summers (S1-2) can be realized using cascade of two standard biquads. $V_{LP1,2}$ and $V_{BP1,2}$ in Fig. 9. refer to the lowpass and bandpass nodes of biquad 1,2 respectively and the variable gain block implements a gain of √K. Bandpass voltage is available in a standard biquad (by making the first integrator a lossy one) and it can be converted to a bandpass signal current using a variable boost transconductor. Thus, addition of bandpass and lowpass signals can be done in current mode by injecting them in the next integrating node. Since actual summing of lowpass and bandpass signals generated in biquad1 and biquad2 occur in biquad2 and first order section respectively, equation 2.3-a can be rewritten as:

$$H_{boost}(s) = \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q1}s + \omega_o^2} * \frac{(s\sqrt{K}/\omega_o + 1)\omega_o^2}{s^2 + \frac{\omega_o}{Q2}s + \omega_o^2} * \frac{(-s\sqrt{K}/\omega_o + 1)\omega_o}{s + \omega_o} \qquad (2.3\text{-b})$$

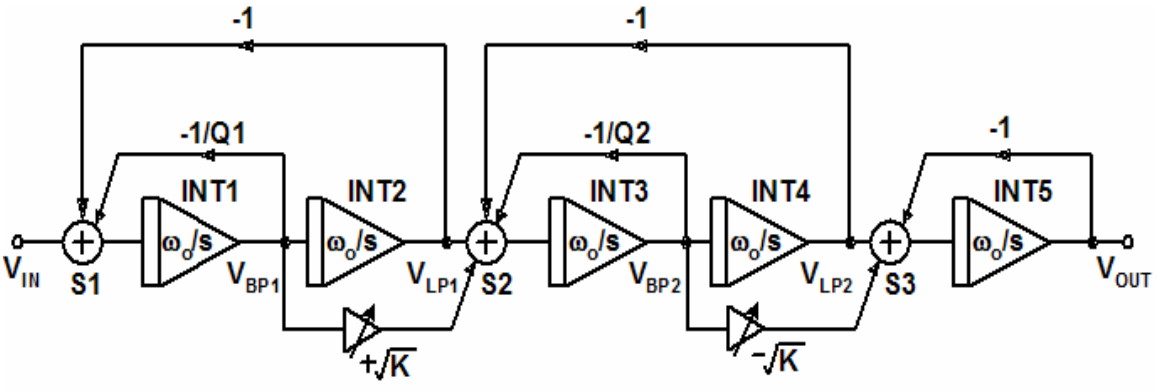

Fig. 9. Conceptual illustration of proposed boost filter architecture

The detailed OTA-C implementation (shown as single-ended for easy reading) of the proposed architecture is shown in Fig. 10. Although biquad 1 and biquad 2 generate lowpass and bandpass signals for zeros, the actual summing of the signals (in current domain) occurs at inputs of the biquad 2 and the first order section respectively.

This architecture has two salient features pertaining to power efficiency. Firstly, each stage realizes a 12dB boost gain and hence the boost path OTAs need only be $K^{1/2}$ (=4) times Gm12, Gm13. Secondly, there is no cancellation of unwanted currents at low frequencies. Since the boost OTA injects the band pass current in the next stage, low frequency swing is always maintained around unity for all the intermediate nodes. Thus, this architecture does not require scaling up the transconductors as against the one reported in [8].

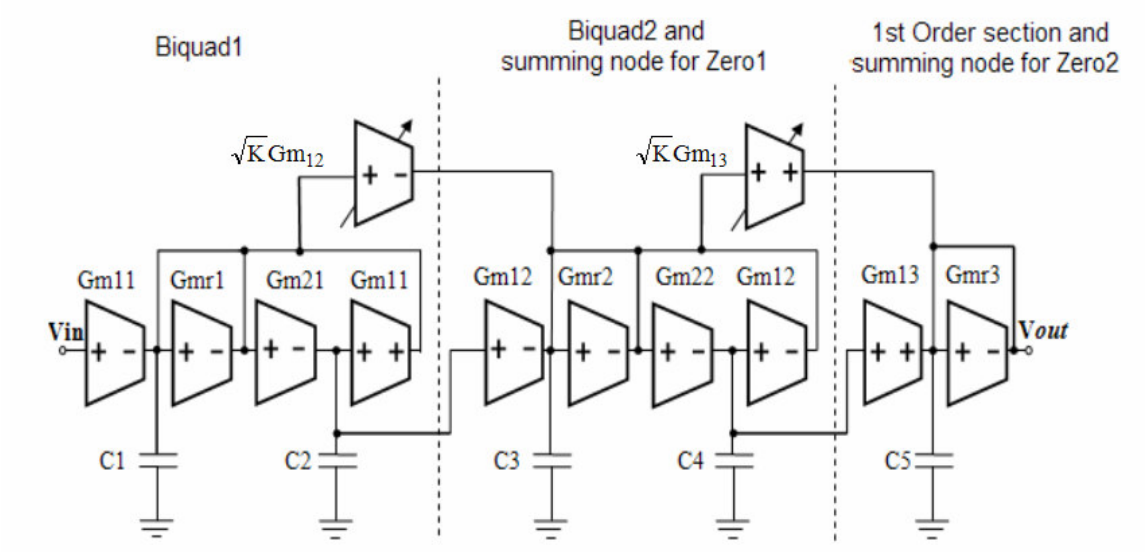

Fig. 10. Single ended representation of OTA-C implementation of the boost filter

Implementation of this architecture without additional summers requires the 1st order section to be the last one to provide the current summing node after biquad 2. The low Q biquad has higher input capacitance than the other biquad (its input OTA is sized to drive a larger loss-OTA). It is power efficient to keep it at the input of the filter since the low output impedance of the preceding driver will push the pole location to high frequency. Given these factors, the order of the sections is optimum if chosen as in Fig. 10, with biquad 1 being the low Q section and 1st order being the last section.

For maximum boost zeros are placed at ωo/4. Hence, the value of K for 24dB boost is given by:

$$\frac{\omega_o}{\sqrt{K}} = 2\pi * \frac{350}{4}\text{MRad} \quad / \text{S} \qquad (2.4)$$

$$K = 16$$

As a generic case, the value of K for a given boost is given by:

$$K = 2^{\left(\frac{\text{Boost}}{6}\right)} \qquad (2.5)$$

where, boost is expressed in dB. Table 2 shows the values of K for different boost settings.

TABLE 2

BOOST GAINS VS K

Boost (dB)	K
2	1.26
4	1.5876
8	2.5198
16	6.3496
24	16

It is instructive to examine the effect of mismatch between the input transconductance of lowpass and bandpass path of the second and third stage ($\sqrt{K}Gm12 : Gm12$ and $\sqrt{K}Gm13 : Gm13$). Assuming that a small additive mismatch factor Δ is introduced such that the transconductance ratio in the second stage is $(1+\Delta)\sqrt{K}$ (instead of $\sqrt{K}$) and $(1-\Delta)\sqrt{K}$ in the third stage, the modified transfer function becomes:

$$H_{Mismatch}(j\omega) \approx H_{boost}(j\omega) * \left(1 + j\frac{2\sqrt{K}\omega_o\omega\Delta}{K\omega^2 + \omega_o^2}\right) \tag{2.6}$$

For reasonable mismatch factors (Δ within +/-5%), the effect of change in overall magnitude response is found to be insignificant. However, zeros influence the phase and group delay behavior especially at low frequencies. A simulation is performed to numerically assess the influence of mismatch up to +/-5%. The highest value for K (=16), is chosen to get maximum group delay sensitivity. Fig. 11 shows that the group delay error for 5% mismatch is about 85pS for a nominal value of 1560pS at 50MHz

(5.45% error). At frequencies higher than this, the error reaches a maximum of 25pS (1.6% error) and asymptotically vanishes at higher frequencies. Due to adaptive delay calibration, such small group delay error is easily tolerated in our application.

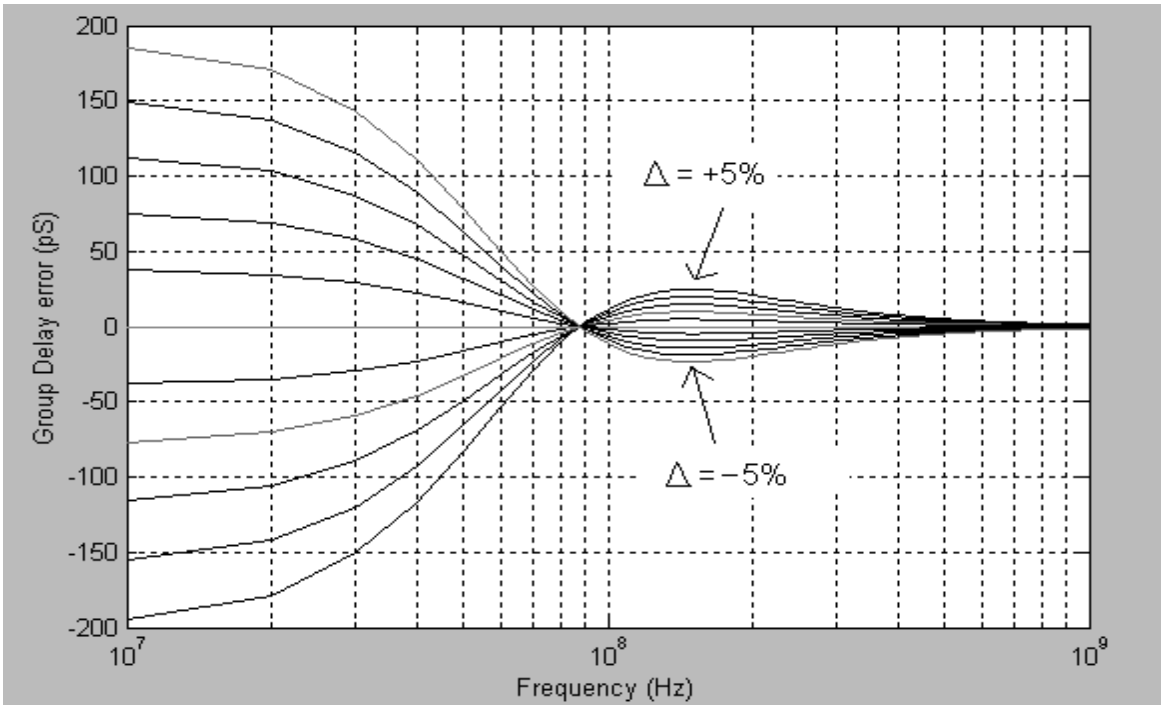

Fig. 11. Group delay error across frequency for -5% to +5% mismatches (varied in steps of 1%)

C. Design of Filter's Parameters

Having determined the filter's approximation and the architecture, the transconductances can be expressed in terms of integrating capacitances for given ω_o. Choice of individual transconductance values and capacitance depends on factors like

noise consideration, distortion, matching and power budgeting. Table 3 shows the relationship between different time constants ω_i (Gm_i/C_i) for the implemented fifth order Butterworth filter shown in Fig. 10.

TABLE 3

RELATIONSHIP BETWEEN TRANSCONDUCTANCE AND CAPACITANCES

$Gm_{11}/C_1 = Gm_{21}/C_2 = Gm_{12}/C_3 = Gm_{22}/C_4 = Gm_{13}/C_5 = \omega_o$
$Gmr_1/C_1 = \omega_o/Q1 \quad Gmr_2/C_3 = \omega_o/Q2 \quad Gmr_3 = Gm_{13}$
$\omega_o = 2\pi*330$ M rad/s Q1 = 0.618 Q2 =1.618 Boost OTAs's transconductance = $\sqrt{K}Gm_{12}$, $\sqrt{K}Gm_{12}$ K = 16

For a signal swing of 250mV p-p differential, integrated noise power in the signal bandwidth of 350MHz needs to be less than 0.78 μV^2 to meet SNR specification of 40dB. For a first hand assumption that all twelve OTAs contribute equally to the noise power and each OTA has a noise figure of 10, transconductance of each OTA from noise perspective is calculated to be 737uS. For a maximum gm/C given by table 3 minimum value of capacitance needed to meet noise consideration can be evaluated. For gm/C of

8.8 Grad/s (boost OTA), minimum integrating capacitance of 83 fF is required to meet -40dB noise specifications.

In general, capacitor values should be minimized in order to increase the power efficiency. However, one needs to keep in mind the ramifications of choosing small capacitors. For example, 83 fF integrating capacitance is quite small to meet matching requirements for a capacitor fabricated in 0.35 μm technology. Further, this also makes the circuit prone to nonlinearity due significant nonlinear parasitic. It is to be noted that above analysis is approximate in nature as it assumes all OTAs contribute equal noise power and does not account for any noise shaping. However, it is does give insight into the fact that minimum capacitance required for the design of the filter is not noise-limited; rather it is dictated by considerations such as matching and distortion.

To achieve reasonable matching, minimum fabricated capacitance of 300 fF is chosen for this technology. Total integration capacitance at a particular node is given by intentional fabricated capacitor and the parasitic loading capacitances associated with the node. If loading capacitance at a given node forms a large portion of the total capacitance, the distortion performance gets severely affected by the loading. It has been shown that if the parasitic capacitance are kept smaller than one third of the total integrating capacitance, the effect on the distortion performance is minimum [12].

Having determined the minimum capacitor to be fabricated for the filter, the individual transconductance and capacitance values need to be determined. Care has been taken to keep intentional to parasitic capacitance ratio approximately around 3. Taking into account the parasitic capacitance at various nodes, transconductance and

capacitance values can be evaluated for gmi/Ci given in table 4. Individual transconductance and capacitors are tabulated in table 4.

TABLE 4

TRANSCONDUCTANCE AND CAPACITOR VALUES

Stage	Gm (mS)		Capacitor pF	
Biquad1	Gm11	2.66	C1	1.15
	Gmr1	4.30	C2	0.55
	Gm21	1.27		
Biquad2	Gm21	1.27	C3	0.55
	Gmr2	0.785	C4	1.15
	Gm22	2.66		
Stage3	Gm13	1.16	C5	0.5
	Gmr3	1.16		

CHAPTER III

CIRCUIT IMPLEMENTATION OF OTAS

A. Core OTA

1. Requirements for the Core OTA

OTA based structures have been highly popular for filters in MHz range due to the open-loop nature that facilitates the realization of the high frequency functions. One of the main requirements of the core OTA is its frequency response. It should not have any poles close to ω_o (or the pole frequency of the filter), otherwise the filter's frequency response is affected. This requirement stems for the necessity of keeping the filter's response 'butter-worth like'. This also implies that any additional internal high impedance nodes in the core OTA could be detrimental to the filter's characteristic.

An ideal OTA has infinite output impedance. Output impedance of the OTA together with its transconductance gain dictates its DC voltage gain for the resultant integrator. The DC gain requirement for the OTA for this fifth order Butterworth filter is quite moderate. It can be shown that for low Q filters, such as Butterworth, filter's response is not very sensitive to the DC gain of the integrator [10]. DC gain > 25dB is sufficient for our application. Further requirements for the OTA include a linearity specification. Under the assumption that all transconductors contribute equally to the distortion power, on an average each OTA can contribute up to -49 dB of non-linearity.

2. Proposed Implementation of the Core OTA

For moderate dynamic range requirements, a single transistor operating in strong inversion and saturation region is shown to have highest gm and reasonable tuning range for a given W/L [13]. Hence, an OTA based on simple differential pair is desired. One such OTA, based on complementary differential pair is as shown in Fig. 12, is used as the main transconductor in the filter. Source degenerated version of this OTA has been reported in [14].

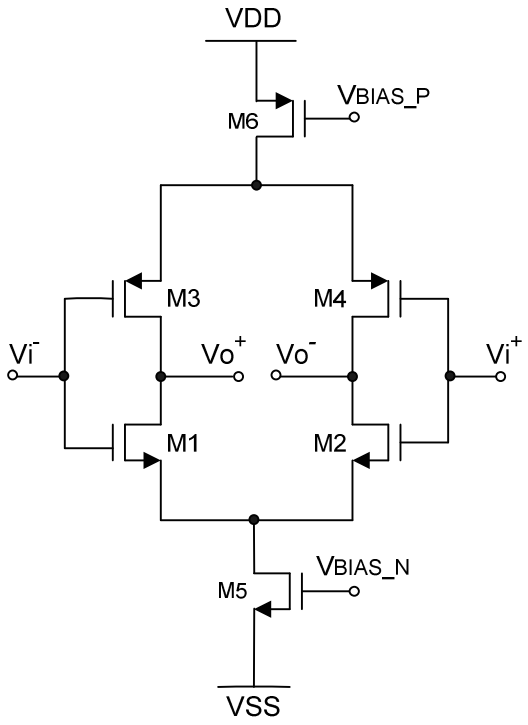

Fig. 12. Circuit schematic of the core OTA

The CMOS OTA can be viewed as a NMOS OTA connected in parallel with a PMOS OTA; so as to facilitate reuse of bias current. One of the most important features of this OTA is the absence of any internal signal nodes due to its single stage configuration. This ensures that no additional parasitic poles are introduced. Since the supply of the overall system is +-1.65V (which gives enough headroom for the complementary differential pair), complementary differential-pair is an ideal choice for power-efficiency reasons as well. This structure generates higher value of transconductance than an NMOS-only differential pair for a given bias current. However, this does result in increase of the input parasitic capacitance, which could potentially increase the power requirements of the filter (as increased capacitance implies increase in transconductance to preserve same ω_o). But for the case of OTA-C filters where parasitic are a fraction of the total integrating capacitance at a given node, there is an overall increase in power efficiency because of this complementary structure.

It can be shown (using square-law V-I relationship of MOSFET) that the third harmonic distortion component for a simple differential pair is given by

$$HD_3 = \frac{V_P^2}{32 * V_{GST}^2} \tag{3.1}$$

where V_P is the peak input signal voltage and V_{GST} is the overdrive voltage (V_{GS}-V_T) fixed based on HD3 requirement (<-52dB per OTA for this case). Table 5 compares simple NMOS differential pair OTA with CMOS OTA (Fig. 12) for a given gm. Let m be the ratio of PMOS W/L to NMOS W/L of the CMOS OTA. NMOS transistors (for both the OTAs) are sized so that its V_{GST} is based on minimum value predicted by (3.1)

and the total transconductance of the two OTAs is same. Based on these conditions, if the NMOS transistor of the CMOS OTA is sized W/L, size of NMOS transistors in NMOS OTA would be $(1+\sqrt{\frac{m}{3}})W/L$. For small values of m, headroom requirement of PMOS differential pair (M3,4) increases drastically (partly due to mobility degradation). On the other hand, for m greater than 3, V_{GST} of the PMOS differential pair becomes less than the minimum value mentioned above. As a good trade-off between headroom, power efficiency and total input capacitance, m is chosen to be 1.5. With this value of m, gm/Id improves by 70% for additional input capacitance of 46% (relative to simple NMOS OTA) while meeting headroom and HD3 constraints.

TABLE 5

COMPARISON OF NMOS AND CMOS OTA

Parameter	NMOS OTA	CMOS OTA
$\frac{W}{L}$	$\left(1+\sqrt{\frac{m}{3}}\right)\frac{W}{L}$	NMOS =W/L, PMOS = m(W/L)
Id	$\frac{1}{2}gmV_{GSTN}$	$\frac{\frac{1}{2}gmV_{GSTN}}{\left(1+\sqrt{\frac{m}{3}}\right)}$
C_{INPUT}	$\left(1+\sqrt{\frac{m}{3}}\right)WLC_{OX}$	$(1+m)WLC_{OX}$
gm/Id	$\frac{2}{V_{GSTN}}$	$\frac{2}{V_{GSTN}}\left(1+\sqrt{\frac{m}{3}}\right)$
$Supply_{(MIN)}$	$V_{DSATN5}+V_{GSN1,2}+2V_P+V_{DSATP3,4}$	$V_{DSATN10}+V_{GSN6,7}+2V_P+V_{DSATP11}+V_{GSP8,9}$

Additional advantage of this structure is that the presence of tail current sources, at both positive and negative supply ends, preserves the supply rejection properties of a simple differential pair. Its inherent fully-differential nature and the tail current sources ensure a good low-medium frequency PSRR that is limited only by systematic and random mismatches amongst the devices. It is to be noted that at higher frequencies, supply rejection degrades due to the parasitic attributed to the tail current sources. However, this holds true for a simple differential pair as well.

3. Design for Linearity

It is to be observed that the previously reported implementations of this structure employed a source degeneration scheme to achieve linearity specifications [14]. However it can be proven that in presence of sufficient headroom, merely increasing V_{dsat} with no source degeneration is a more power efficient solution for moderate linearity applications.

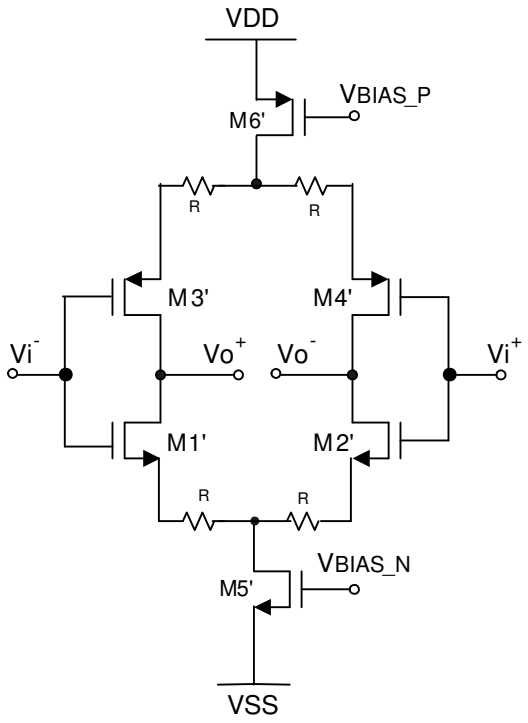

Fig. 13. Source degenerated version of the core OTA

Fig. 13 shows the source degenerated version of the complementary OTA. HD3 for a source degenerated simple differential pair can be roughly given by:

$$HD_3 = \frac{V_P^2}{32 * V_{GST}{}^2 (1+\eta)^2} \tag{3.2}$$

where, $1+\eta = 1+gmR$ is the source degeneration factor and V_P is the peak amplitude. For the CMOS OTA, if NMOS and CMOS differential pair are designed with similar overdrive voltage (V_{GST}) and degeneration factor (η), the HD3 is expressed as in (3.2). For PMOS and NMOS differential pair to contribute equally to distortion power, the overdrive voltages as well as the source degeneration factors are kept same. For equal

transconductance of PMOS and NMOS differential pair, this translates to equal values of source degeneration resistors.

To achieve lower distortion, either source degeneration in form of η can be introduced or the overdrive voltage can be increased. Assuming that for the case of no source degeneration i.e. $\eta = 0$ (Fig.12), $V_{GST\_PMOS} = V_{GST\_NMOS} = V_{dsat1}$ is required to achieve a given HD3 specification. Now if we introduce a degeneration of factor $1+\eta$, the requirement for the overdrive voltage drops to $V'_{GST\_PMOS} = V'_{GST\_NMOS} = V_{dsat1}/(1+\eta)$. Keeping the same transconductance for both the cases and using the following square law representation [15], relative sizes and currents for the two cases ($\eta=0$ and finite η), are evaluated:

$$I = \frac{\mu C_{ox} W V^2_{GST}}{2L(1+\theta V_{GST})} \tag{3.3}$$

$$gm = \frac{\mu C_{ox} W V_{GST}}{L(1+\theta V_{GST})(1+\eta)} - \frac{\theta \mu C_{ox} W V^2_{GST}}{2L(1+\theta V_{GST})^2(1+\eta)} \approx \frac{\mu C_{ox} W V_{GST}}{L(1+\theta V_{GST})(1+\eta)} \tag{3.4}$$

where, θ is the fitting parameter that models the mobility degradation due to vertical electric field. For limiting case of $\theta = 0$, it can be shown that while the current requirement remains same, size of the driver transistors increase significantly for the case of the source degenerated differential pair as compared to one with $\eta = 0$. Introduction of additional resistors also results in increase the input referred noise. Relative expressions for these quantities are tabulated in table 6.

TABLE 6

COMPARISON OF SOURCE DEGENERATED (Fig. 12) AND NON-DEGENERATED (Fig. 13) DIFFERENTIAL PAIR FOR EQUAL GM AND HD3

Parameter	Source degenerated	No degeneration $\eta = 0$
Overdrive	$V_{GST}/(1+\eta)$	V_{GST}
W/L	$W/L*(1+\eta)^2$	W/L
Drain current (Id)	Id	Id
Noise (Vn^2)	$Vn^2 (1+2\eta)/(1+\eta)$	Vn^2

Hence, to achieve required distortion for a given gm, noise and parasitic are less for the case of increased overdrive voltage as compared to the source-degenerated case. Increased parasitic for the later case can affect the linearity and indirectly increase the power consumption of the overall filter. So if head room constraints are met with increased overdrive voltage, it is preferable not to use any source degeneration. It is to be noted that choice of increasing the overdrive is advantageous only for the case when linearity requirements are moderate. For very high overdrive the effect of mobility degradation becomes pronounced and the headroom becomes prohibitive. For the read-channel applications a moderate linearity of 40dB is required. For this specification and 0.35μm process, it is possible to design the complementary OTA to meet the distortion requirements solely by large over-drive voltages rather than resorting to additional linearization techniques

4. Design Implementation of the Core OTA

As mentioned previously, in absence of any additional internal nodes, there are no parasitic poles associated with this OTA structure. However gate-drain parasitic capacitors do introduce a feedforward zero that results in negative excess phase. A simplified small signal model for the OTA is as shown in Fig 14.

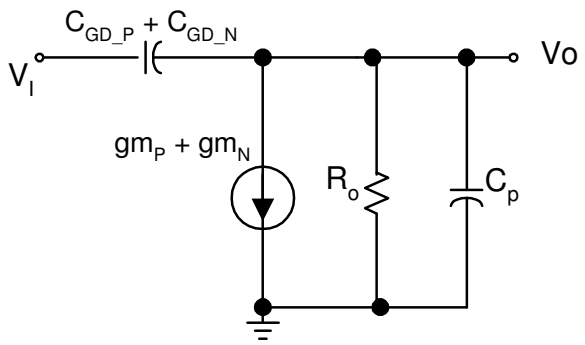

Fig. 14. Small signal model for the core OTA

Using this model, small signal parameters such as overall transconductance (Gm), output impedance (R_o) and location of feedforward zero (ω_z) can be obtained as following.

$$Gm = gm_N + gm_P \tag{3.5}$$

$$R_o = \frac{1}{go_N + go_P} \tag{3.6}$$

$$\omega_z = \frac{gm_N + gm_P}{C_{gd\_P} + C_{gd\_N}} \tag{3.7}$$

where gm_P and gm_N refer to transconductance of P and N type driver devices, go_P and go_N refer to output conductance and C_{gd_P} and C_{gd_N} refer to the corresponding Gate-Drain capacitances. Output load and parasitic capacitance are lumped into C_p.

As discussed earlier linearity specifications (-49dB for each of the OTA) is attained by choosing appropriate overdrive voltage (V_{dsat}) through equation (3.1). Overdrive voltage used for the NMOS and PMOS driver transistor in this design is about 250mV. Thus ratio between V_P and V_{dsat} is around 0.5. The transconductance (gm) requirements for each of the five OTAs have already been specified in Chapter II. For a specified gm and the overdrive voltage, the size and the bias current for each of the five OTA can be calculated using the square law approximations in (3.3)-(3.4). A square law approximation can be used here with fair bit of accuracy because of the fact that V_{dsat} is relatively high, thus driver transistors are biased deep in saturation region. Note that mobility degradation is quite pronounced in this design due to usage of high V_{GST}, however this effect is captured in the design equations (3.3)-(3.4). Table 7 tabulates bias current and the size of the driver transistors for all five OTAs. The gm/go for each of the OTAs is around 100 and parasitic capacitance mostly constituting of C_{gs} varies from 35 to 150 fF.

TABLE 7

ASPECT RATIOS AND CURRENTS FOR CORE OTAS

	Gm mS	Bias Current μA	Aspect Ratios W/L μm			
			M1	M3	M5	M6
OTA1 (gm11)	2.66	630	4*4.5/0.4	4*7.5/0.4	14*3/0.2	14*30/2
OTA2 (gmr1)	4.3	900	10*2.6/0.4	10*5.2/0.4	20*3/0.4	20*30/2
OTA3 (gm21)	1.27	315	4*2.6/0.4	4*5.2/0.4	7*3/0.4	7*30/2
OTA4 (gm22)	0.78	585	4*3.8/0.4	4*7.5/0.4	13*3/0.4	13*30/2
OTA5 (gm13)	1.16	225	5*1.3/0.4	5*2.5 /0.4	5*3/0.4	5*30/2

Fig. 15 shows the transconductance for OTA 1. The plot is obtained using a 'short-circuit load' test, under which the short circuit AC current normalized for 1V AC input is treated as the transconductance of the OTA. Also shown is the excess phase for this OTA. Note that the excess phase is less than 4 degree around ω_o.

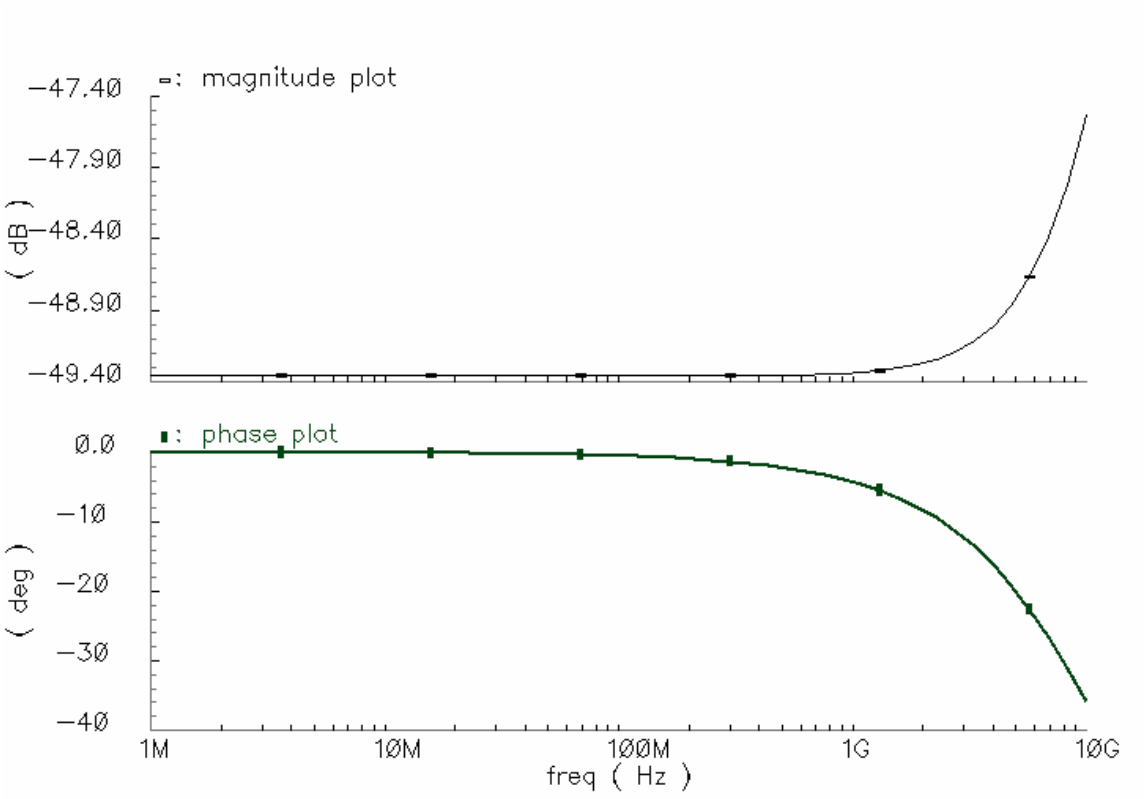

Fig. 15. Magnitude and the phase response of the core OTA

B. Boost OTA

Boost OTA is one of the most important building blocks in the entire design. A high gain associated with the boost path underlines its importance for the performance of the entire filter. For example, signal passing through the low pass path of the filter sees a nominal gain of 0dB, however through the boost path it experiences a gain of 24dB (12 db in each biquad).

1. Basic Requirements of the Boost OTA

As mentioned in Chapter I, the read channel system can be trained to choose the best boost gain to minimize the ISI and compensate the channel losses associated with the programmed data rate. This requirement implies that the boost gain needs to be programmable and controllable with fine accuracy. For this applications boost gain needs to be varied from 0 to 24dB with step resolution better than 2dB. Highest boost setting corresponds to the maximum transconductance of the boost OTA which is 5.1mS as indicated in Chapter II. Thus, the boost OTA must be programmable over a wide range: 0 to 5.1mS (0dB boost to 24dB boost) with gain resolution of at least 2dB. Further requirements for the boost OTA include a stringent linearity specification. It was earlier shown that on an average each OTA can contribute up to -49 dB as distortion power.

2. Possible Implementation of Boost OTA and Previously Reported Structures

There have been various techniques proposed for widely programmable high frequency OTAs [7]-[8]. For these OTAs current through the driver transistor varies in accordance with the controlled degeneration factor. Hence, as control input (to control gm) is varied, the input and the output capacitance offered by these OTAs change a lot. For wideband applications, parasitic capacitors form a significant proportion of the overall integration capacitance at a given node. Given this premises, use of OTAs whose

input or output capacitance varies significantly with control input would be detrimental to the filter's performance in two different ways. Firstly the linearity of the filter would change with boost settings. Secondly Q at the various integrating nodes would change with boost settings, which manifests itself as change in the shape of the filter's magnitude response and a poor group delay. To demonstrate this effect, boost OTA consisting of multiple sections of complementary differential-pair-OTA, described earlier in this chapter, are used as boost OTA. Depending on boost setting sections of this OTA are switched in and out. The filter's group delay response is plotted for 0dB boost and maximum boost setting and is shown in Fig. 16. It is evident from this figure that as input and output capacitance of such boost OTA varies with the boost setting, the shape of the filter's response and Q change significantly across boost. Hence it is desirable to use a programmable OTA whose input and output capacitance remains invariant across control.

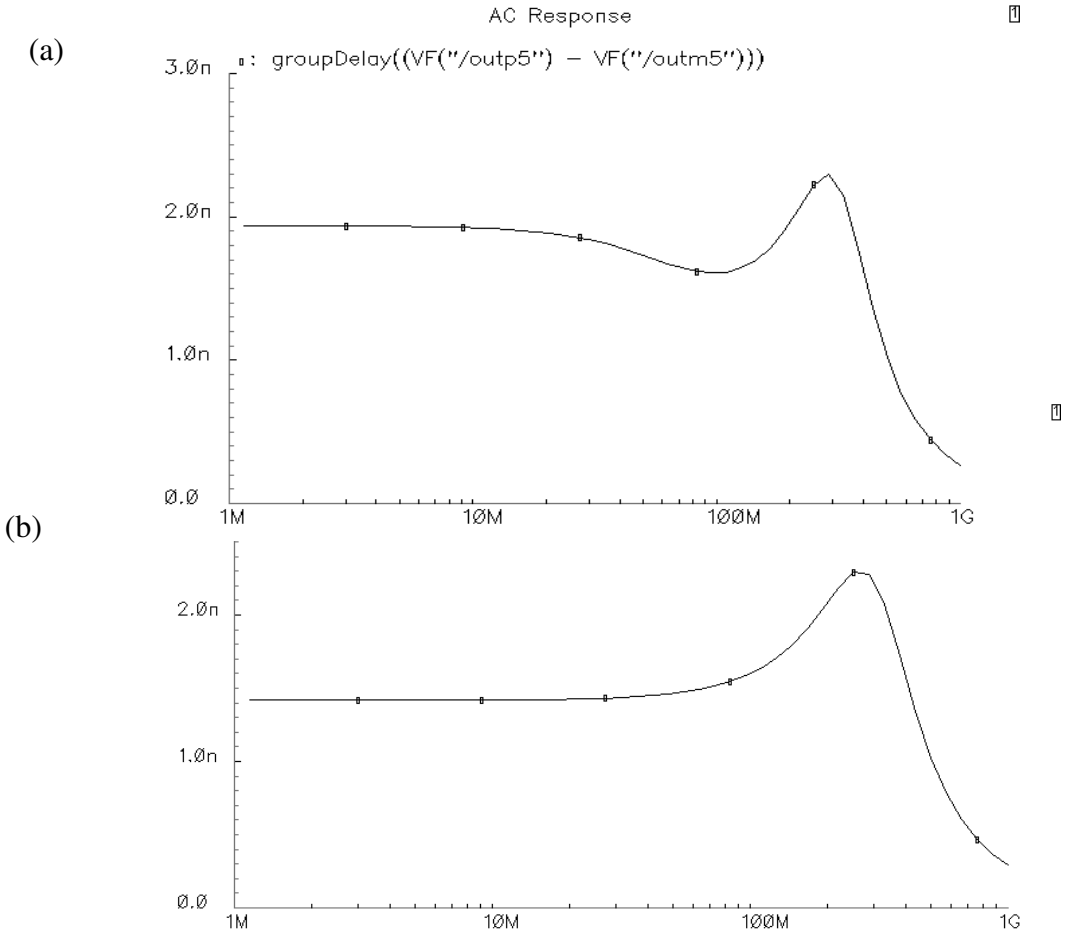

Fig. 16. Group delay response for a filter with switched OTAs as boost transconductors

(a) 0dB boost (b) 24dB boost setting

Ratios of controlled impedance can be used to control the transconductance gain. Fig. 17 shows the block representation of this concept. A widely tunable integrator based on this concept is used in [16] and is illustrated in Fig. 18.

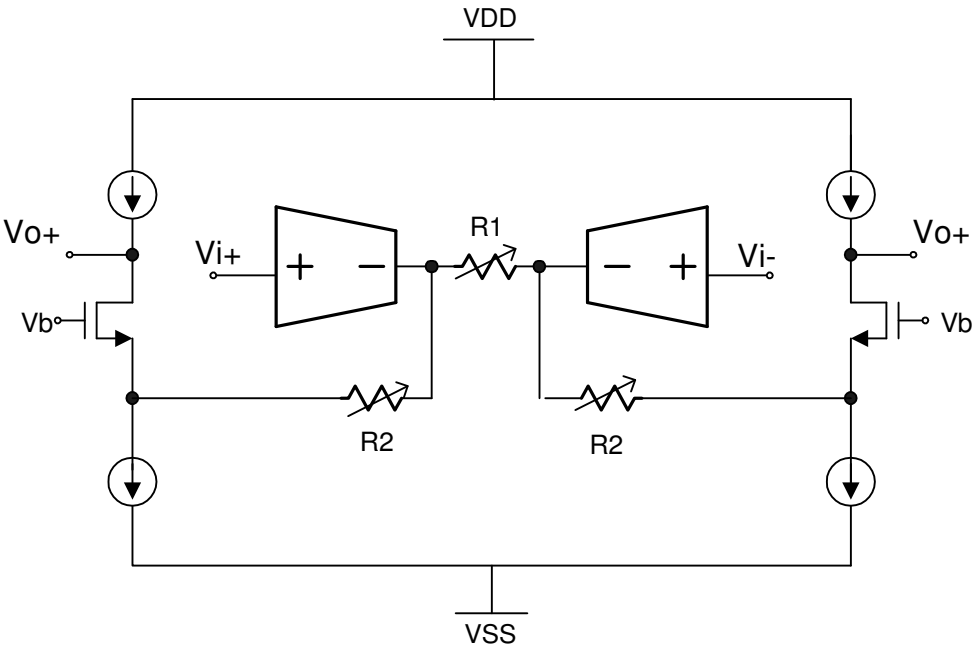

Fig. 17. Conceptual diagram for the programmable integrator

The key property of this structure is that it does not change bias condition of the circuit across the wide tuning range. Thus, it was considered as a potential candidate as the boost OTA. It is based on steering of the signal current to either the output (through FETS M2 and M3) or the cancellation path (through FET M1), in inverse proportion of controlled impedances. Where M1, M2 and M3 are the transistors operated in triode region whose impedances are controlled through control voltages VC1 and VC2. However, the frequency of operation of this structure is limited due to the presence of multiple nodes and internal feedback.

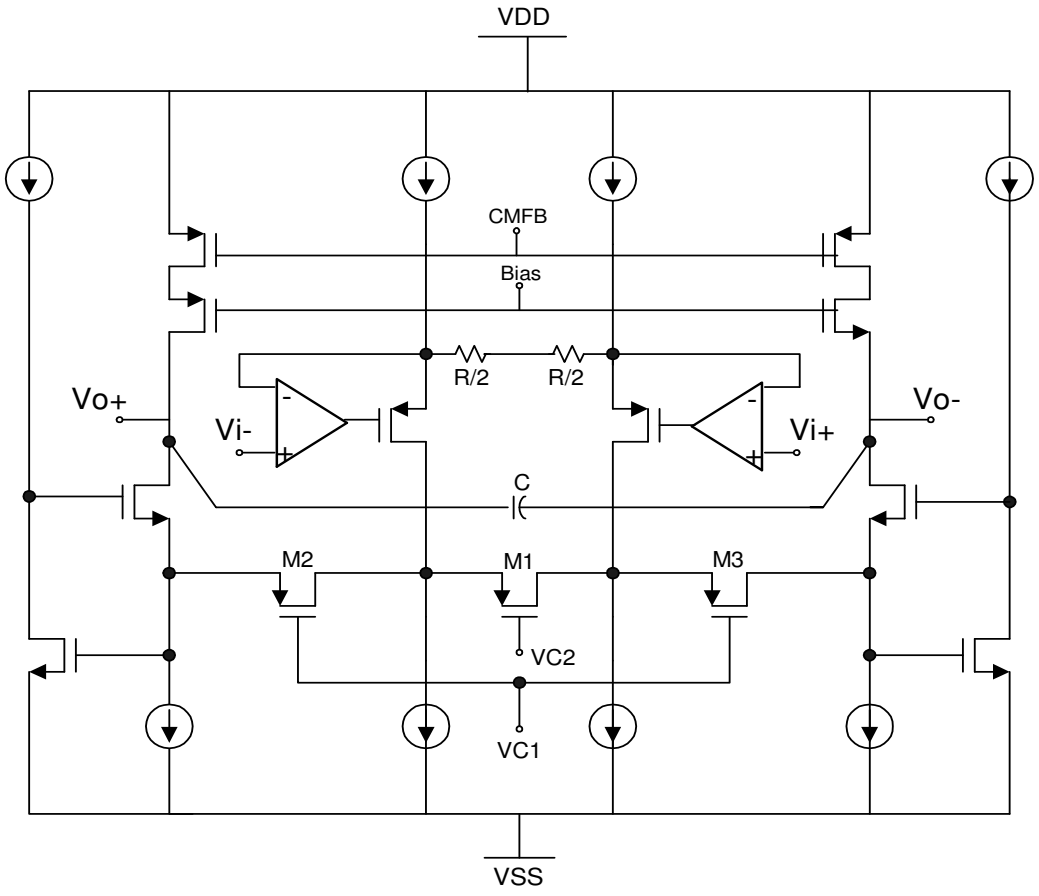

Fig. 18. A programmable integrator with fixed bias conditions of the circuit reported in [16]

Introduced in [17], is a widely programmable OTA based on a four quadrant multiplier. The bandwidth of this structure is limited; the use of drivers in linear region makes this OTA not suitable for wideband operations. In [18], an interesting approach of using dummy transistor pairs is introduced. Wide programmability of the transconductor is achieved by switching multiple transconductors connected in parallel (Fig. 19).

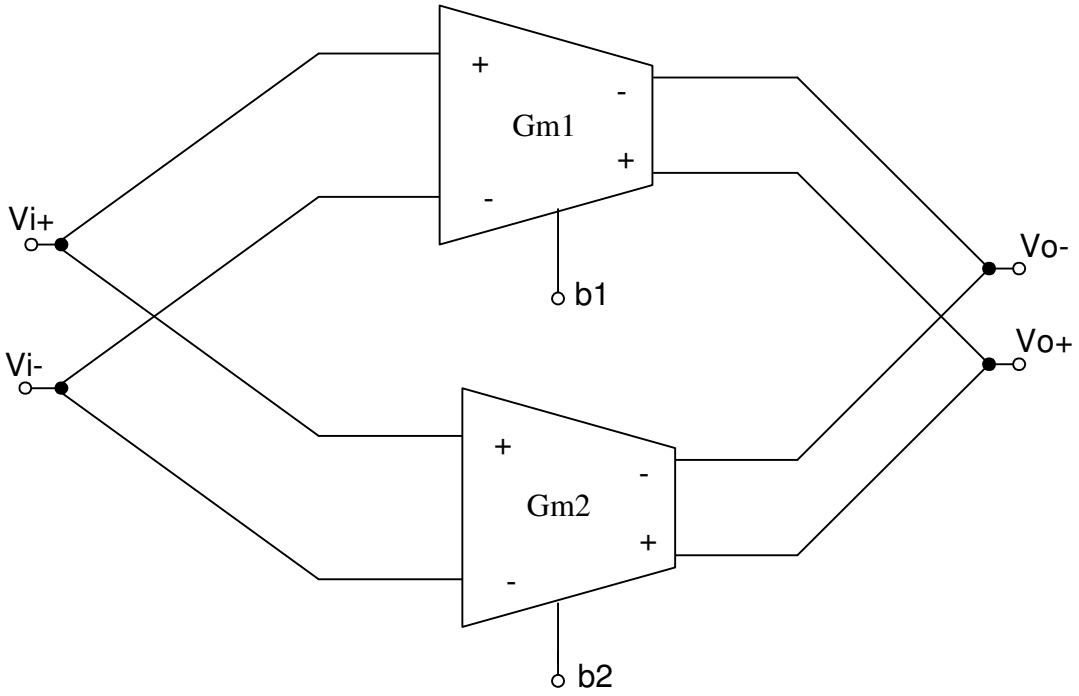

Fig. 19. Multiple transconductors in parallel to realize a programmable OTA [18]

Control inputs (b1 and b2) are used to switch the unit transconductor (Gm1 and Gm2) in or out of the signal path. The unit transconductor cell is designed such as the input and output parasitic offered by it remain constant irrespective of the fact whether that OTA is switched in or not.

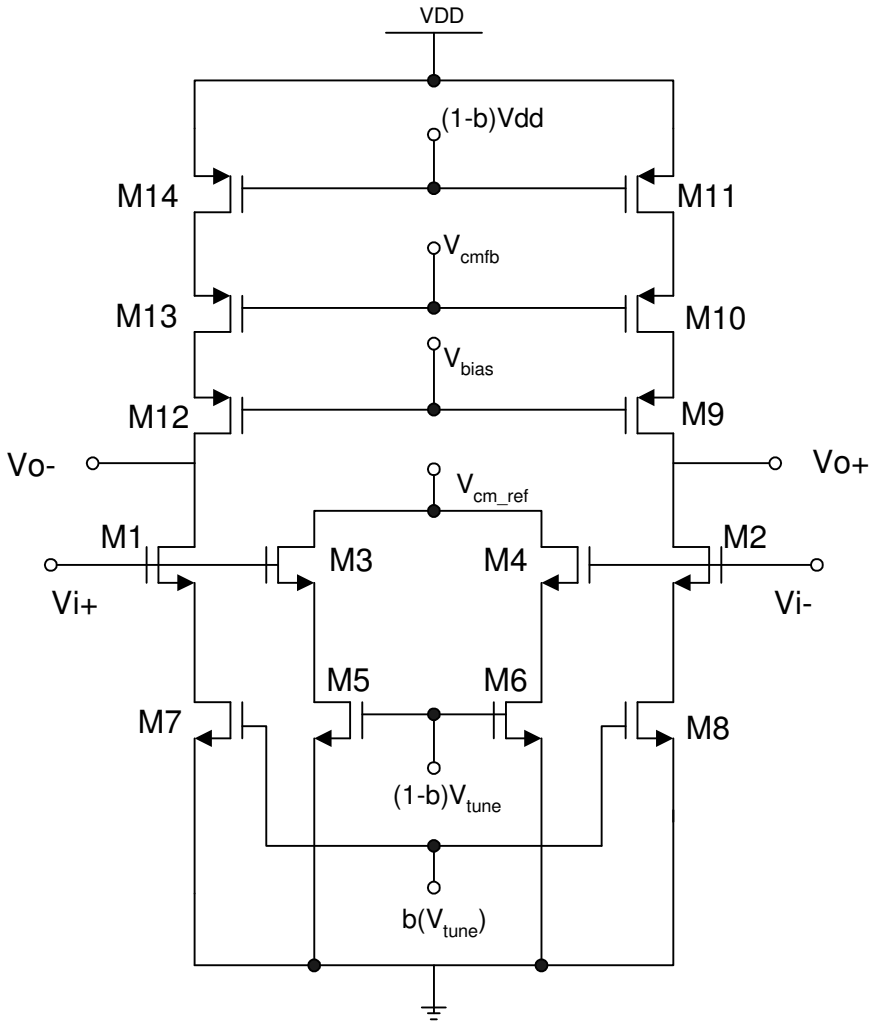

Fig. 20. Switchable unit transconductor cell [18] with constant input and output parasitic

The unit transconductor cell that uses an additional dummy transistor pair connected at the input is shown in Fig. 20. The sum of the bias currents of the main input pair and the dummy pair is made constant so that the total gate capacitance ($C_{GS\text{-}total}$) remains same across control setting (b = 0 or 1). However, the signal current generated in the dummy path does not reach the output. Multiple of such unit cells connected in parallel are configured to achieve variable transconductance with 'constant-capacitance'

approach. However, if this transconductor is to be used as a boost OTA and the boost gain is to be varied in fine steps, it would involve many of such elements. This would not only increases the total gate capacitance (since the overlap capacitances and C_{GB} is present even in off conditions) but also add to the routing capacitance. Such increase in parasitic capacitance would seriously impair the bandwidth of the filter, especially when it is required to drive a large transconductor in the boost path.

3. Proposed Implementations of the Boost OTA

The structure reported here is based on principles of current steering and cancellation and resembles the well-known Gilbert-cell based mixer. There are two salient features of this structure: firstly it is widely and continuously programmable. Its transconductance can easily be programmed from 0 to its maximum value using a continuous time differential control. Secondly, it preserves the same input and output capacitance across all boost settings. Fig. 21 shows the schematic of the boost OTA.

The voltage to current conversion is done using the main differential pair (M1-M2). Two pairs of common-gate control transistors (M3=M4=M5=M6) are used to steer the signal current generated in the differential pair. These control transistors are driven by differential boost control voltage (V_{CNTRL_N},V_{CNTRL_P}) riding over the required common mode. This common mode signal is generated on chip using a replica circuit. A differential control voltage is added over this common mode externally to generate V_{CNTRL_N} and V_{CNTRL_P} on-board.

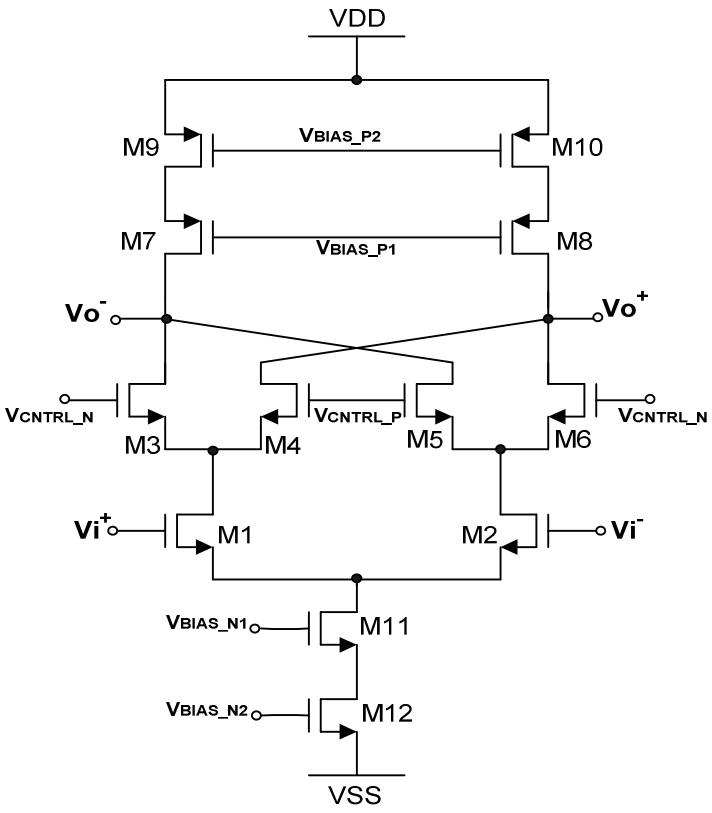

Fig. 21. Circuit diagram of boost OTA

Referring to Fig. 21, for case of 0dB boost the differential input to the control transistors is zero. Signal current generated by M1-M2 divides between M3-M4 and M5-M6 equally to the extent to which these devices are matching. Under ideal conditions, cancellation of the cross-coupled currents in this case implies that no signal current is output for this setting. Similarly for the highest boost setting, a sufficiently large differential input at the control port ($V_{CNTRL\_N,}$ V_{CNTRL_P}) ensures that the transistors M3 and M6 are fully on and conduct almost entire of the signal current, while transistors M4 and M5 slip into cut-off region. Thus, by varying the differential input to

the control transistor pairs the fraction of the generated differential signal current that is allowed to reach the output is controlled. Hence, the OTA can be programmable from 0 to $gm_{\_MAX}$, where $gm_{\_MAX}$ is the OTA transconductance when no cancellation occurs. In contrast, a typical differential pair based practical OTAs provide tuning range of 10-50% [13].

It is instructive to examine the input and the output capacitance across the boost setting for the proposed OTA. Ignoring secondary effects, the bias conditions for the driver transistors (M1-M2) remain the same across boost settings. Therefore, the input capacitance does not vary across 24dB boost and is roughly given as:

$$C_{in} = C_{gs\ M1,\ M2} \tag{3.8}$$

Note that the gate-drain capacitance, looking in from the input port, is amplified by the voltage gain at the drain nodes of driver transistors (M1, M2) due to miller effect. However since the drains of the driver transistors are low impedance node (Vo has a large integrating capacitor), the effect of gate-drain capacitance on (3.8) is negligible. Further the outputs of the boost OTA are well controlled through a common mode feedback loop and are held at a common mode potential of 0V. The output capacitance mostly constituting of C_{db}, C_{gd} is given as:

$$C_{out} = C_{db\ M3,\ M5/\ M4,\ M6} + C_{db\ M7/M8} + C_{gd\ M3,\ M5/\ M4,\ M6} \tag{3.9}$$

C_{db} is the voltage dependent junction capacitance which can be modeled as:

$$C_{db} = \frac{C_{jo}}{\left(1 + \frac{v}{V_{DB} + 2\phi}\right)^{mj}} \tag{3.10}$$

where C_{j0} is the zero bias junction capacitor and V_{DB} is the junction bias voltage, ϕ is the work function, mj is the technological coefficient and v is the instantaneous voltage across the capacitor. It is to be noted that swing supported by the filter does not change across the boost setting, thus C_{db} component of the output capacitance shows similar behavior across the boost setting.

Another important characteristic of the boost OTA is its wideband operation. For realization of 24dB gain (12 dB in each stage) around 300MHz, the theoretical requirement on unity gain bandwidth of each of the boost OTA is 4*300MHz = 1.2GHz. However to ensure a 'Butterworth-like' phase response and group delay response, the parasitic poles need to be place even beyond this limit. The proposed boost OTA does have an internal node: at the source of common-gate control transistors: M3-M6. However, this is a low impedance node and the pole due to this node is much beyond the signal bandwidth. The frequency of this pole is given by impedance (capacitive and resistive) associated with this node and varies with the boost control. The lowest frequency of this pole occurs when the large boost control voltage steers the current of M1/M2 through a single transistor; e.g. M3/M6; in this case, the conductance looking into this node is roughly given by gm_3, where gm_3 is the transconductance of transistor M3 specified for the case of highest boost. Frequency of the additional pole (ω_p) is given by:

$$\omega_P \approx \frac{gm_3}{C_{gs3} + 2C_{sb3} + C_{db1} + C_{gs4}} \tag{3.11}$$

C_{gs3} and C_{sb3} represent gate-source and source-bulk capacitance of M3 and C_{db1} represents drain-bulk capacitance of the driver transistor M1. In practice this pole is designed to be around 2 GHz.

In a practical implementation, a digital control of the boost can be implemented using a low resolution on-chip DAC. The concept is illustrated in Fig. 22, where a digital word is used control the boost in discrete pre-programmed steps.

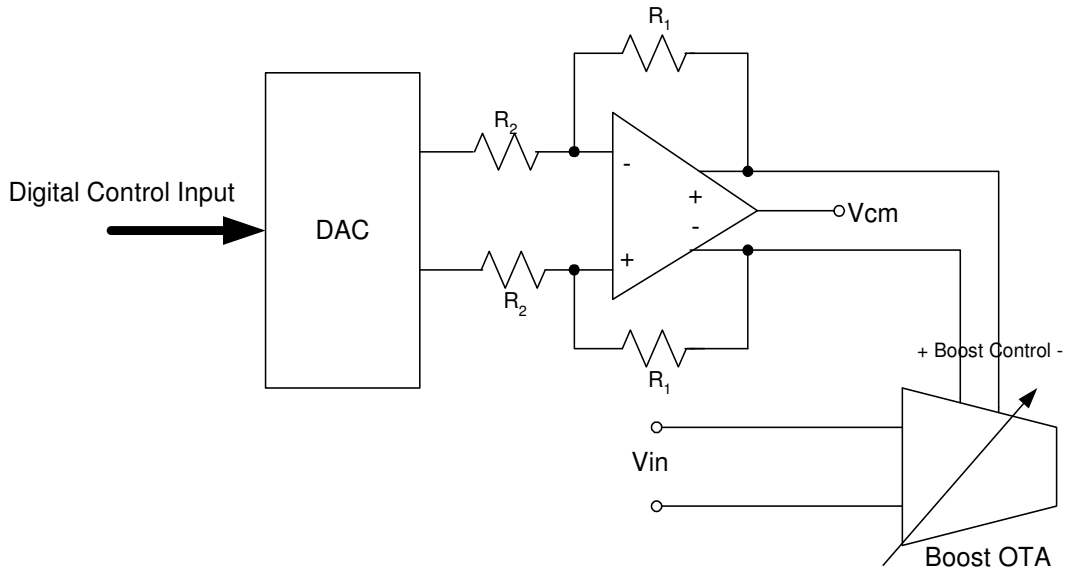

Fig. 22. A possible scheme for discrete control of boost using on-chip DAC

4. Design Implementation of the Boost OTA

Procedural details for implementation of the boost OTA follow a similar outline as that for the core OTA. Gm or the transconductance of the boost cell is specified earlier in Chapter II. We need a transconductance of 5mS and 3mS for the two boost

stages. To meet the distortion specifications, two aspects have been examined. Firstly the signal current generated through the boost OTA should be sufficiently linear; secondly the ratio of the intentional to parasitic non linear capacitor at the output node should be sufficiently large for a linear current to voltage conversion. As discussed earlier, in this design this ratio is kept at about 3:1. V_{GST} of the driver transistors is around 200mV. However current source transistors have smaller V_{GST} (≈100mV) to meet the headroom given by ±1.65V supply and input and output swing of 125mV (single-ended). Given transconductance and V_{GST}, the size (W/L) and the current of the driver devices are computed using a square law model (3.3)–(3.4) while taking mobility degradation due to vertical field into account.

For design of the control transistor, the location of the parasitic pole as specified by equation (3.11) is taken into account. It is to be noted that this equation needs to be evaluated only for the case of maximum boost, when entire current passing through M1 or M2 (half of the main tail current) passes through one of the control transistors. For the evaluated transconductance and the current, size of the control transistors are computed using (3.3)-(3.4). The size of the driver and control transistors are tabulated in table 8.

TABLE 8

ASPECT RATIOS AND CURRENTS FOR BOOST OTA

	Width (μm) $M_{1,2}$	Length (μm) $M_{1,2}$	Width (μm) $M_{3,4,5,6}$	Length (μm) $M_{3,4,5,6}$	Tail Current mA
Boost OTA1	90	0.4	54	0.4	1.5
Boost OTA2	108	0.4	45	0.4	1.2

Fig. 23 shows the magnitude and the phase response for the transconductance of the first boost OTA. The transconductance of the boost OTA is simulated using a 'short-circuit load' test. Since the maximum transconductance of the boost OTA is to be obtained, the boost was set to highest level for this test. From the figure it is evident that the parasitic pole introduced at the source of the control transistors is around 3GHz. The error introduced in the group delay due to such pole can be computed to be less than 2%. Hence it does not affect the system performance much.

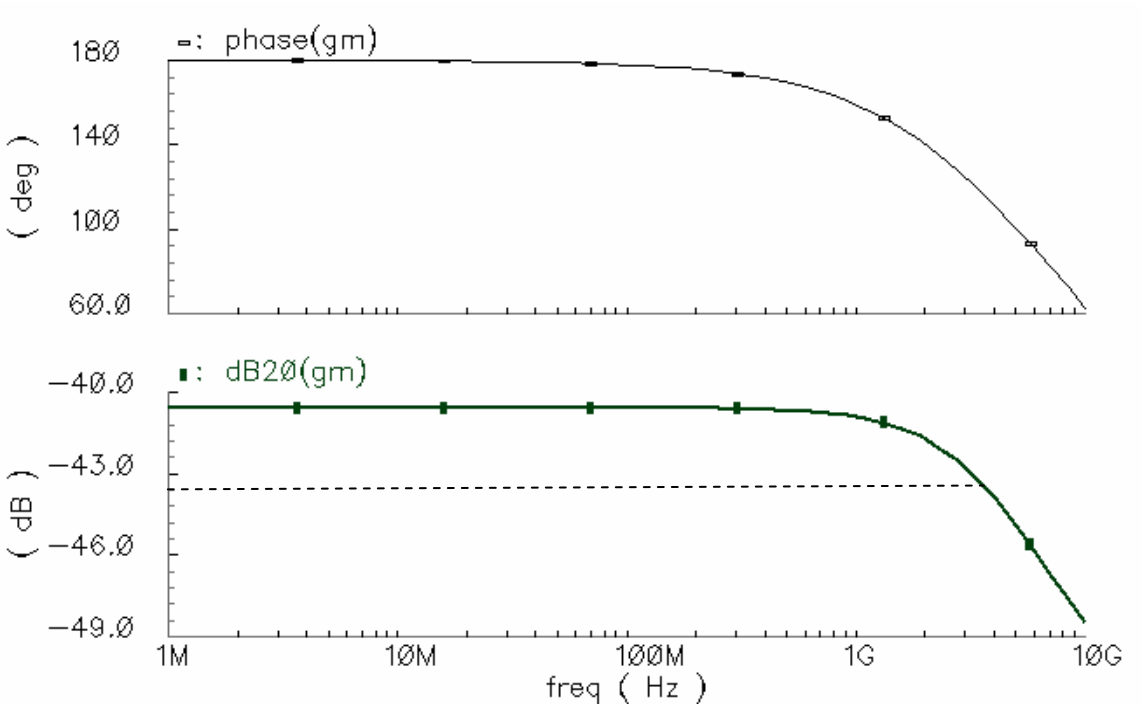

Fig. 23. Transconductance and phase response of the boost OTA

CHAPTER IV

CMFB IMPLEMENTATION

A. Common Mode Feedback Scheme

One of the important aspects of the fully differential circuits is the common mode control. While the differential mode negative feedback is done to shape the transfer function, the common mode loop ensures that the circuits operate in a linear region. To achieve robust Q for the biquads, it is important to maintain constant operating currents for the OTAs across supply voltage variations, process corners and mismatches. To keep the current sources from entering the triode region, the common mode voltages must be maintained accurately. A typical common-mode feedback (CMFB) loop used in the context of an OTA-C filter is shown in Fig. 24.

The output common mode voltage of OTA1 is sensed at the common source node of M1' and M2'. The CMFB error amplifier (A_C) compares the sensed common mode to the ideal common mode voltage and the correction voltage is applied to the gate of M5. This controls the tail current of the OTA1 which adjusts the common mode voltage for OTA1. The overall common mode loop is kept under negative feedback for a stable common mode operation. V_{cmref} is to be maintained $V_{GS\_M1'}$ lower than the ideal common mode voltage. A replica of OTA2 is used to generate reference (V_{cmref}) for the CMFB amplifier.

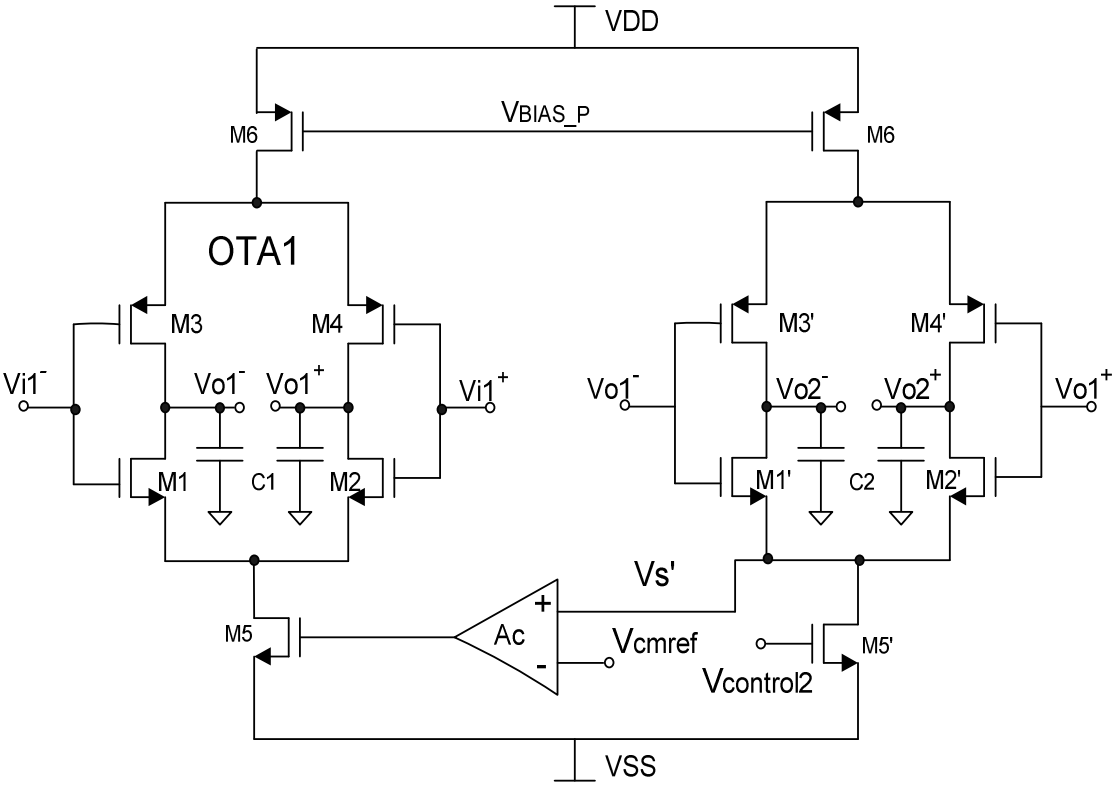

Fig. 24. CMFB loop involving two OTAs and a CMFB amplifier

Thus the CM accuracy of a system is determined by the common-mode transconductance gain and the fact that the OTA output has large CM gain is irrelevant [19]. This fact can be explained as below. Suppose ΔI is the difference between the currents M5 and M6 (current source transistors of main OTA1 in Fig. 24) would pass under short circuit load condition. In other words if ΔI is the offset current between the NMOS and PMOS current source and $A_C(0)$ is the DC gain of the EA, the error in the output CM voltage of OTA1 under closed loop condition is simply given by:

$$V_{CM\_ERROR} = \frac{\Delta I}{gm5 * AC(0)} \tag{4.1}$$

This can be viewed as the offset current being absorbed by the offset voltage times the DC transconductance gain of the loop ($gm5*A_C(0)$). Thus, the two important aspects of the CMFB loop design are its DC transconductance gain ($gm5*A_C(0)$) and open loop unity-gain-bandwidth achieved for a stable loop phase margin. The DC gain of the error amplifier determines the controllability and accuracy of the DC operating point while bandwidth determines the frequency range for which the common mode noise would be effectively rejected. As a conservative specification bandwidth of the common mode loop can be kept as high as the signal band-width. This ensures that the CMFB loop would govern the common-mode rejection for the entire signal band. However, taking into account that the next stage, which is differential in nature, would also have a finite common mode rejection, the band width specifications can be relaxed. A common mode band-width of half the signal bandwidth can be chosen as specification.

B. Conventional CMFB Amplifier

For the typical CMFB loop explained above, the dominant pole is at the output of the OTA1. All other loop poles need to be placed beyond unity gain bandwidth for a stable operation. Thus, if a single pole CMFB amplifier is used, its output should be a low impedance node to maintain pole frequency beyond the unity gain bandwidth of the loop. This requirement means that typically a low gain amplifier is used as an amplifier to drive the error to zero where a dominant integrating pole is present in the system. Fig.

25 shows a conventional CMFB amplifier. However, with such amplifier it is observed that the common mode voltages can be in an error of up to +/-100mV for some filter nodes due to its limited DC gain and offset contribution from several OTAs connected to those nodes; e,g, the bandpass output of the biquads have the offset contribution of 3 OTAs. Due to limited control of the DC operating point across process corners and supply voltages, the quality factor associated with different nodes of the filter vary. To preserve the Butterworth-like shape, an additional Q tuning loop would need to be introduced if the conventional CMFB amplifier is used.

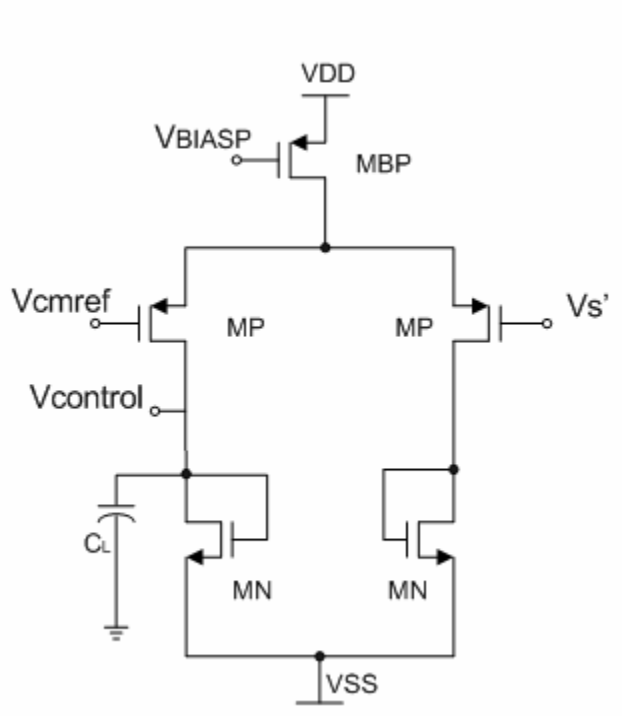

Fig. 25. Circuit Diagram for a conventional CMFB Amplifier

C. Proposed CMFB Amplifier and Comparison

A CMFB amplifier, that is designed to alleviate the above problem by enhancing the DC gain without compromising on bandwidth and stability, is introduced. The proposed EA, shown in Fig. 26(a), consists of PMOS input pair (M7,8) with NMOS load (M9,10) provided with an auxiliary network consisting of a triode-MOS transistor (M12) with resistance R and a poly capacitor C. The equivalent circuit in Fig. 26(b) shows two parallel paths. The fast path ($1/2*gm_7$) and the slow path (A2 and gm_9) together determine the DC gain of the EA. At low frequencies, both slow and fast path contribute to signal gain while at high frequencies only the fast path is active. The low frequency and high frequency representation of the circuit is illustrated in Fig. 26(c) and Fig. 26(d) respectively. The purpose of the network around gm_9 is to provide high impedance at low frequencies and low output resistance ($1/gm_9$) at frequencies close to the unity gain bandwidth of the complete CMFB loop. This characteristic manifests as a low frequency pole and a zero pair.

If R (M12) is designed such that $R >> 1/gm_{9,10}$ then the transfer function of the proposed EA is approximately given by:

$$\frac{V_{CONTROL}}{V_S'} = \frac{-gm_{7,8}R_0\left(1+s\frac{RC}{2}\right)}{1+s[RC(1+R_0gm_{9,10})+R_0C_L]+s^2RR_0CC_L} \tag{4.2}$$

where $R_O = 1/(gds_7+gds_9)$ and $C_L = Cgs_5+Cdb_9+Cdb_7$. The poles and zero of the error amplifier are located at:

$$\omega_{p\_nw} \approx \frac{1}{gm_{9,10}R_0RC} \quad , \quad \omega_{z\_nw} \approx \frac{2}{RC} \quad , \quad \omega_{p\_nd1} \approx \frac{gm_{9,10}}{C_L} \tag{4.3}$$

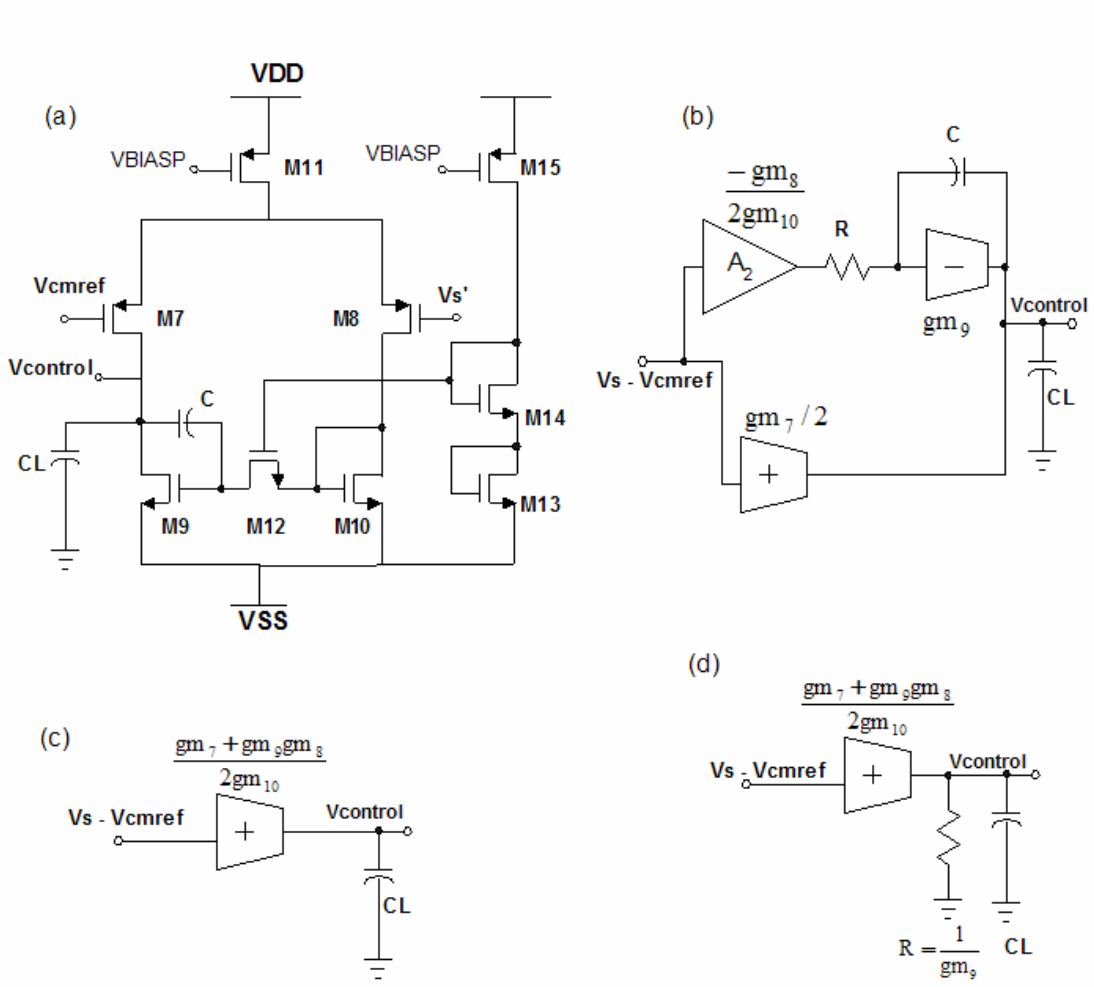

Fig.26. (a) Circuit Diagram for the proposed CMFB error Amplifier (b) Its equivalent representation (c) Low frequency representation (d) High frequency representation

The amplifier's DC gain is given by $-gm_{7,8}R_0$. ω_{p_nw} is located at low frequency while ω_{z_nw} is placed at medium frequency. The bode plots of the conventional and the

proposed EA are shown in Fig. 27(a) and 27(b) respectively. The proposed EA displays high DC gain. However, at frequencies greater than ω_{z_nw}, it behaves like the conventional EA thus retaining similar unity gain bandwidth.

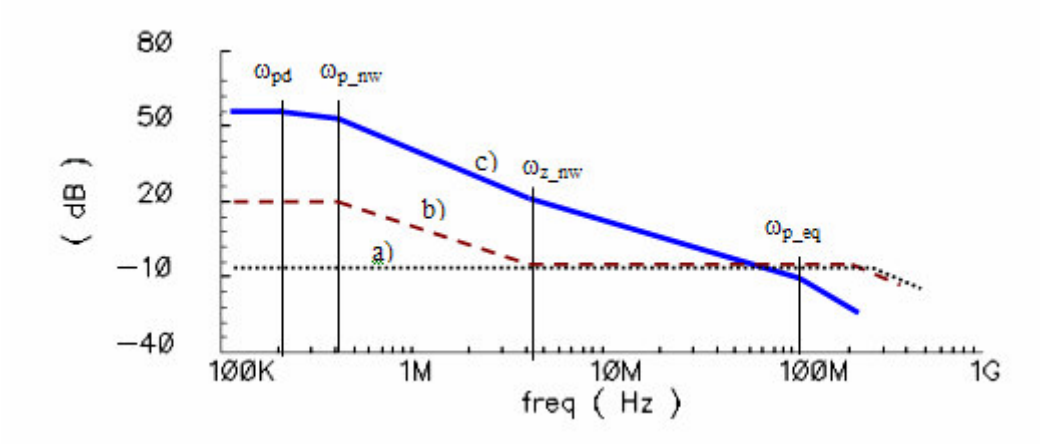

Fig. 27. Bode plot for (a) conventional CMFB error amplifier (b) proposed CMFB error amplifier (c) complete CMFB loop

In addition to EA's poles and zeros, overall CMFB loop (see Fig. 24) has a low frequency pole (ω_{p_d}) at OTA output node and two more non-dominant (high frequency) poles at common-source node of M1,2 (ω_{p_nd2}) and M1',2' (ω_{p_nd3}).

$$\omega_{p\_d} \approx \frac{gds_5 * gds_{1,2}}{2 * gm_{1,2} * C_1} + \frac{gds_6 * gds_{3,4}}{2 * gm_{3,4} * C_1}, \quad \omega_{p\_nd2} \approx \frac{2 * gm_{1',2'}}{2 * Cgs_{1',2'} + Cdb_{5'} + Cgs_8},$$

$$\omega_{p\_nd3} \approx \frac{2 * gm_{1,2}}{2 * Cgs_{1,2} + Cdb_5} \tag{4.4}$$

The overall open-loop gain of the proposed CMFB loop is shown in Figure 27(c). From the bode plot in trace (c), it can be seen that there are 2 low frequency poles (ω_{p_d},

ω_{p_nw}), 1 zero ω_{z_nw} below unity gain frequency (ω_u) and 1 equivalent non-dominant pole (ω_{p_eq}) above ω_u, where ω_{p_eq} represents the combined effect of ω_{p_nd1}, ω_{p_nd2}, and ω_{p_nd3}. For a typical CMFB loop in this filter, the pole and zero frequencies are: f_{p_d}~200KHz, f_{p_nw}~400KHz, f_{z_nw}~8MHz, f_{p_nd1}~1GHz, f_{p_nd2}~1.2GHz and f_{p_nd3}>4GHz.

With detailed analysis, it can be shown that ω_{p_nw} and ω_{z_nw} can be designed such that the following condition for 60^0 of phase margin holds, hence

$$\frac{\omega_{z\_nw} - \omega_{p\_nw}}{\omega_u} \le \tan\left(60 + \tan^{-1}\left(\frac{\omega_u}{\omega_{p\_nd1}}\right) + \tan^{-1}\left(\frac{\omega_u}{\omega_{p\_nd2}}\right) + \tan^{-1}\left(\frac{\omega_u}{\omega_{p\_nd3}}\right)\right) \qquad (4.5)$$

ω_u is about 200MHZ for the same CMFB loop mentioned above. Since ω_{p_nw} tracks ω_{z_nw} (equation 4.3), ω_{z_nw} value of about $1/10^{th}$ of ω_u (or less) is required to satisfy the inequality (4.5). In order to minimize disturbance in the relative placement of ω_{p_nw}, ω_{z_nw} and the non-dominant poles across process corners, M12 is biased using a commonly used circuit shown in Fig. 26(a).

Fig. 28 shows the ac response of the complete CMFB loop under nominal and extreme corner conditions. The worst case phase margin was observed to be 59.6^0, while the worst case unity gain bandwidth is around 180MHz.

Small signal AC response is a good measure of relative stability. But transient step response is the true test for the absolute stability of a system. Thus a step common mode disturbance is applied to the CMFB loop to determine its settling behavior. Further, the common mode current step should be large enough to reflect the realistic offset and mismatch currents encountered in an IC.

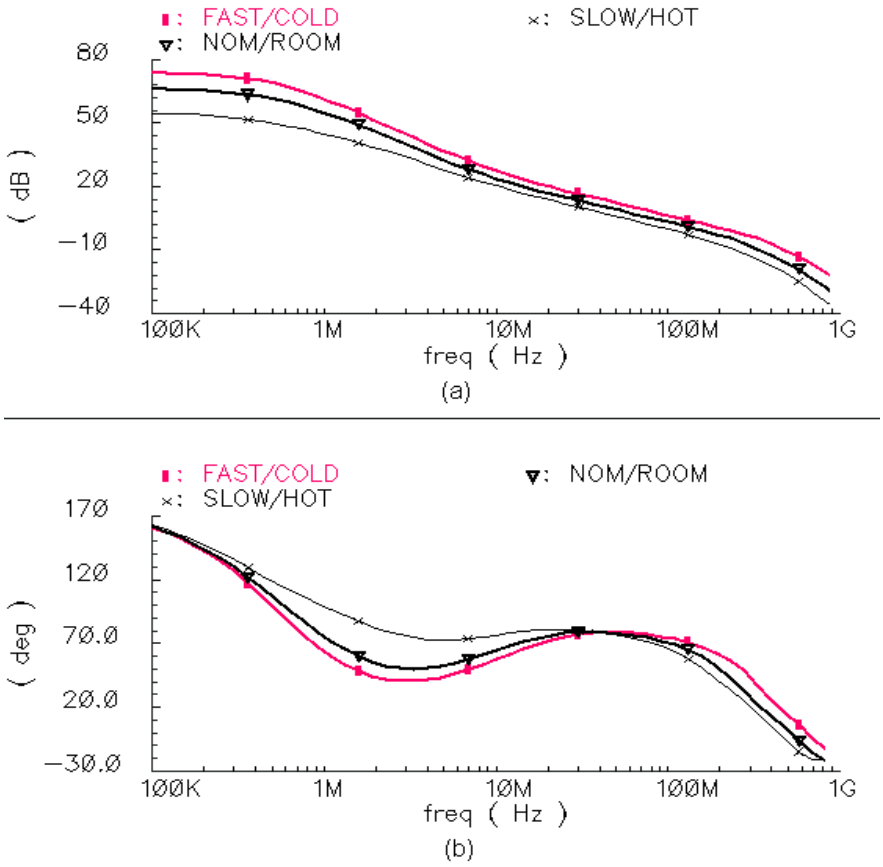

Fig. 28. AC response of complete CMFB loop

Common-mode current step equivalent to 25% of the bias current of $M_{1,2}$ is applied to each of the nodes $Vo1^+$ and $Vo1^-$ in Fig. 24 , and the settling of the presented CMFB loop is studied. It can be seen from Fig. 29 that the presented amplifier tends to behave like a single-pole amplifier designed with same bias current for initial few nanoseconds. However, the final value is more accurate for the proposed amplifier

owing to its superior DC gain. The loop's settling time is around 75 nsecs, which shows that the zero located at 8 MHz is dominating loop's transient behavior.

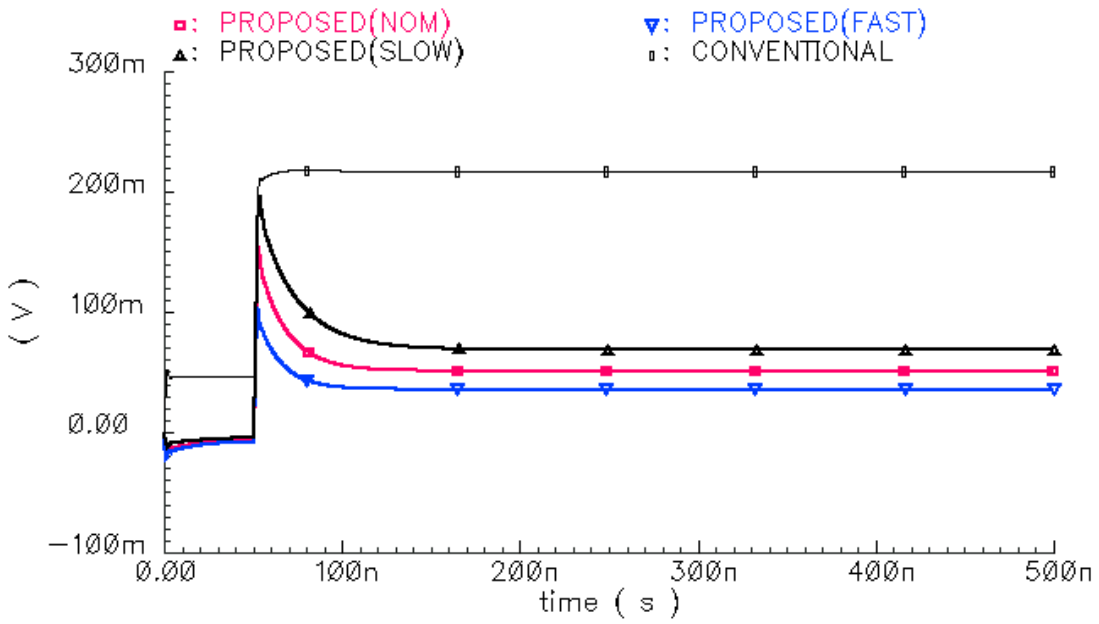

Fig. 29. Comparison of settling behavior of conventional and proposed CMFB amplifier

CHAPTER V

SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

Schematic and post layout simulations are performed for verification of the filter's performance. Basic simulations of the filter include functionality tests such as AC response, boost response, transient etc, while performance verification is done using multi-tone transient simulations with and without boost.

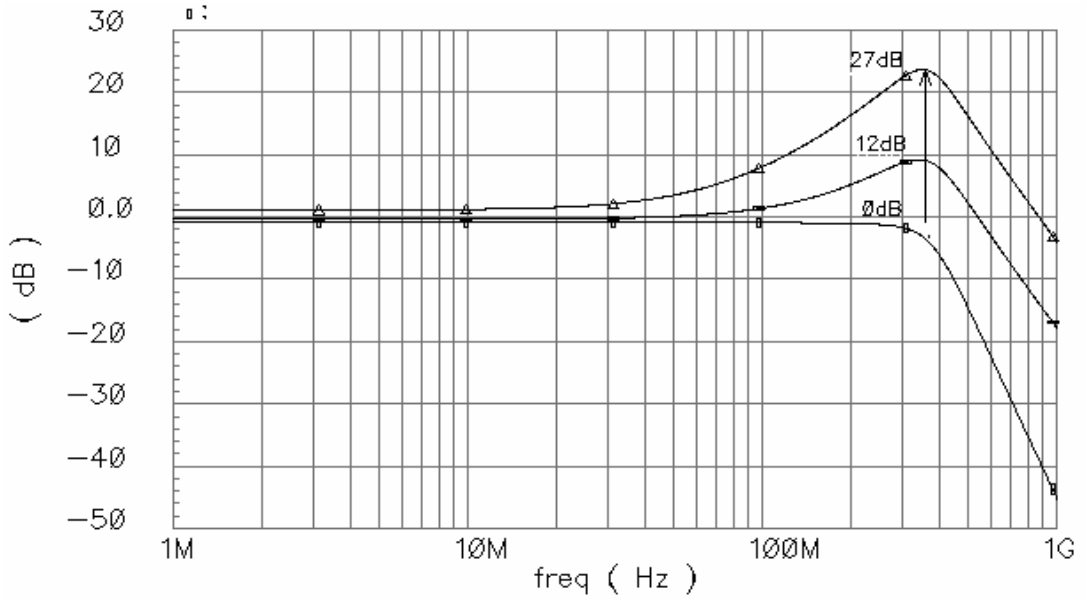

Fig. 30. Magnitude response of the filter with 0-27dB boost

Fig. 30 shows the boost characteristic of the filter using AC simulations. It is shown that the boost can be varied in continuous steps up to a maximum value of 27dB.

Although, the specifications for the maximum boost are 24dB, boost transconductors are over designed a little bit to meet the specifications across process shifts. Also evident in the figure is -3dB bandwidth of the filter which is 355MHz. Temperature and process variations of the magnitude response are shown in Fig. 31. Filter provides at least 24dB of boost across these variations, while ω_o changes from 290MHz to 410MHz.

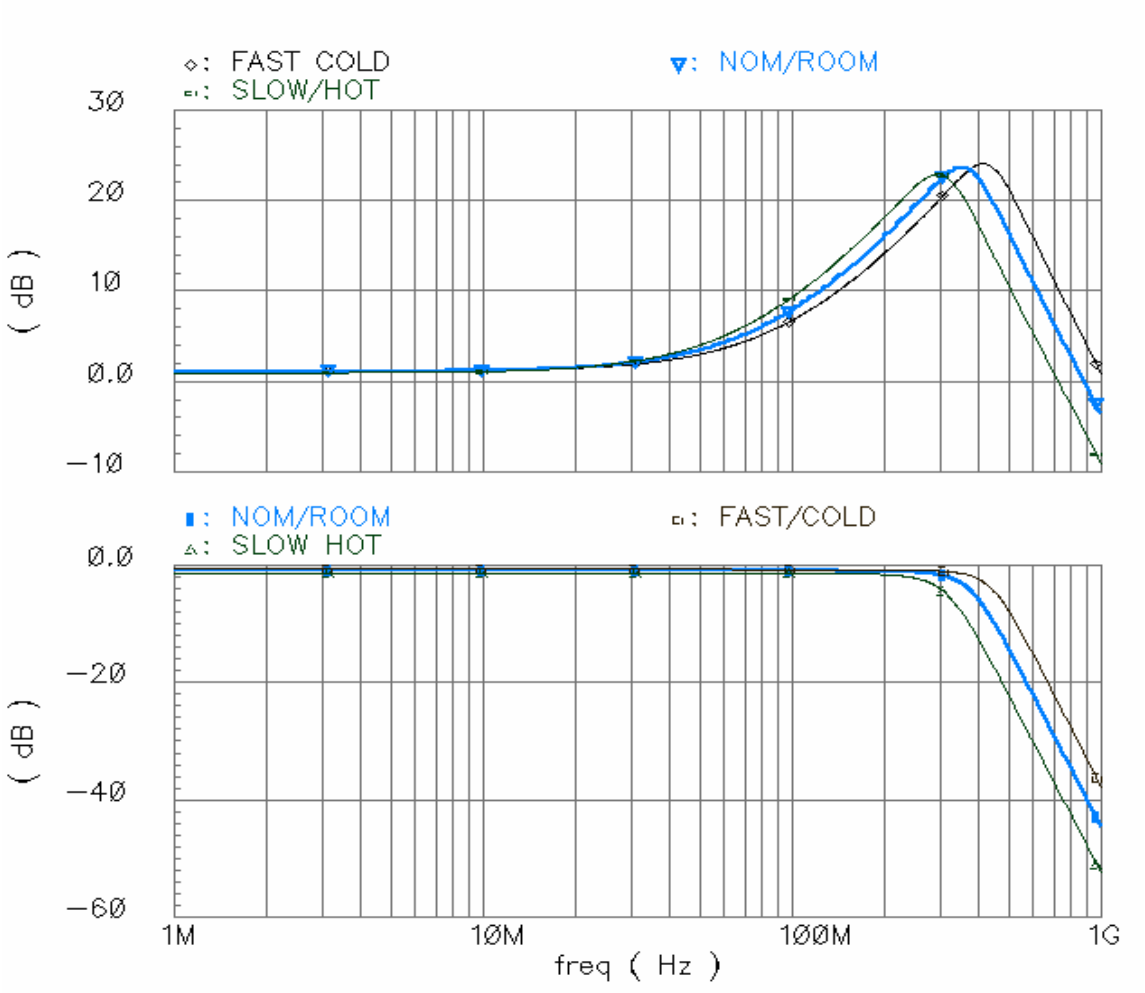

Fig. 31 Magnitude response of the boost filter across corners

Magnitude response serves as a coarse indication of filter's response. However how close the realized filter is to a true Butterworth transfer function, can be gauged by the phase or group delay response of the filter as compared to an ideal model. Fig. 32 shows the group delay response of the filter as compared to an ideal fifth order Butterworth model based on schematic simulations. Group delay error is within 8% of the ideal value, which indicates that quality factors of the various nodes are quite close to the designed values.

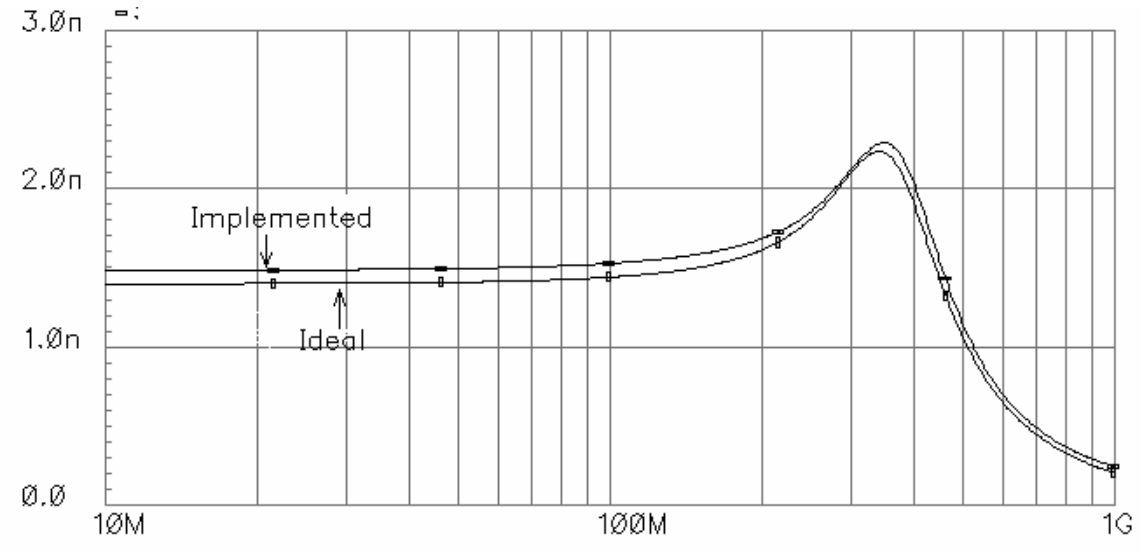

Fig. 32. Group delay of the ideal vs. the implemented Butterworth filter (0dB boost setting)

As discussed earlier, one of the important features of this architecture was preservation of 'Butterworth-like' transfer function across all boost settings. This property is verified by observing the group delay response across boost. Fig. 33 shows

the group delay plot for boost settings of 24dB. Group delay error across boost is < 15% and can be tolerated in a typical read channel application where adaptive phase equalization is performed.

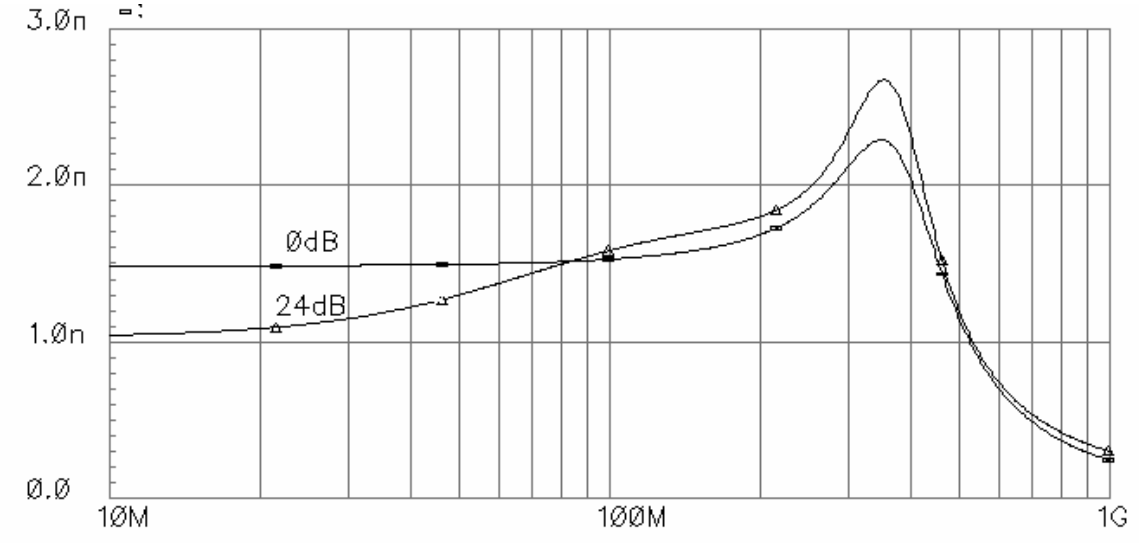

Fig. 33. Group delay of the filter for 0dB and 24dB boost setting

While AC simulations are only a representation of the filter's frequency selectivity, its true performance can only be ascertained using the transient response to real world signals. Fig. 34 shows the transient output of the filter when a 250mV p-p differential sine wave of 100MHz is applied at the input ports. Note that since the filter has a -1dB gain around 100MHz, for 0dB boost setting, the output swing is at 225mV peak-peak.

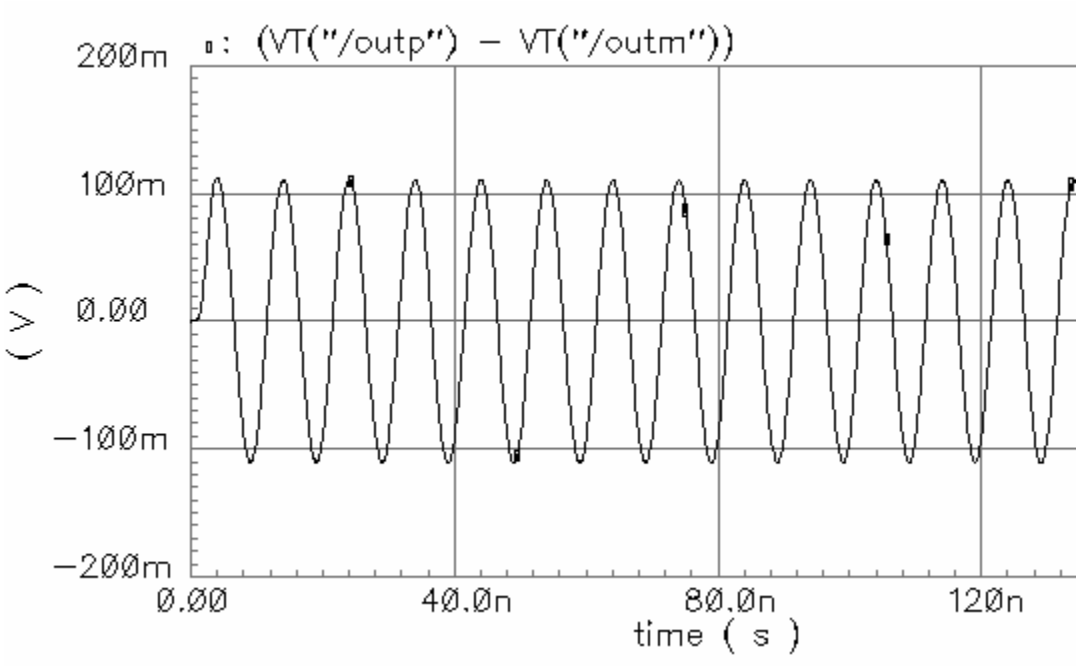

Fig. 34. Transient output for 100MHz sine wave at 0dB boost setting

In the end application, the filter is used as an equalizer for read channel where data pulses are read from magnetic media. Hence, the real-world input to the filter should be the pulses that are similar to those read from magnetic media. However, sine wave input can be used to check the harmonic distortion response of the filter. Fig. 35 shows the FFT of the output for the input of 100MHz full swing sine wave. Note that since filter starts attenuating around 300MHz, a sine wave of frequency 100MHz or less should be applied for the distortion test, so that at least the third harmonic component is in-band. The third harmonic distortion is less than -44dB.

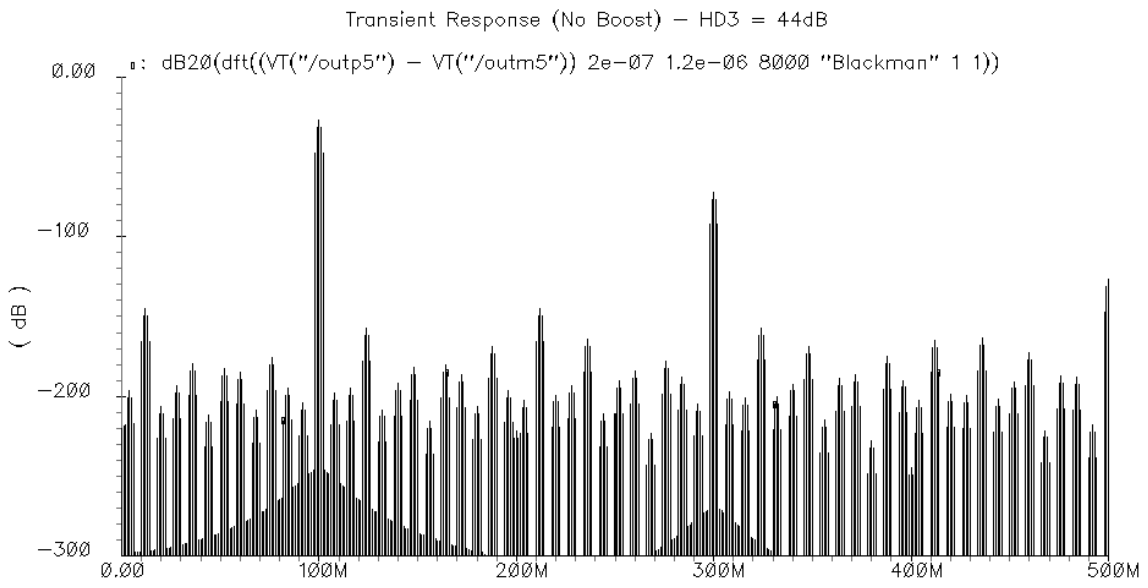

Fig. 35. Output spectrum for 100MHz sine wave at 0dB boost setting

Distortion specifications are specified for the highest signal frequency and the largest supported swing. These are the conditions where linearity is worst in a typical system. Since a single tone test cannot be used to accurately estimate distortion power at higher end of frequencies (as the third harmonic would fall in the stop-band), multi-tone tests are used to find intermodulation distortion. A two-tone simulation setup is used here to find intermodulation distortion. As the maximum possible output swing has already been specified, the amplitudes of both the inputs are scaled down to half of that of the single tone source. This ensures that Peak-to-Average ratio (PAR) as well as peak amplitude remains same as the single-tone test. The two tone chosen are at 300MHz and 310MHz. Their third order intermodulation component is expected to be at 320MHz and

290MHz. Fig. 36 shows the resultant FFT obtained when such two tone input is passed through the filter configured for 0dB boost gain. The obtained IM3 is -45dB.

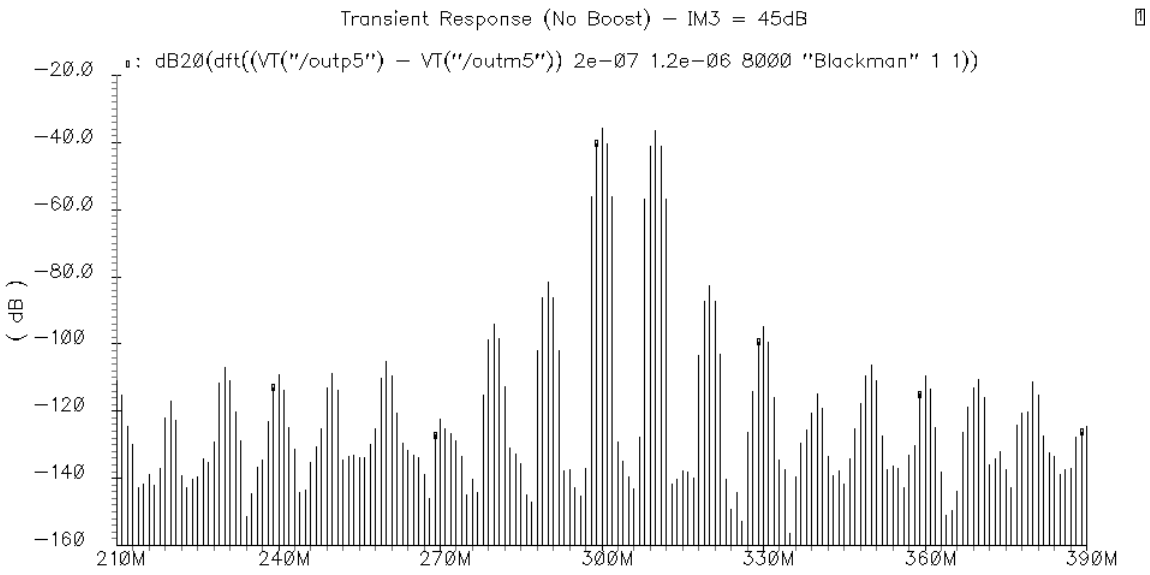

Fig. 36. Output spectrum obtained for intermodulation test at 0dB boost setting

To qualify the distortion performance across boost, two-tone test was done at the highest boost setting. It is to be noted that since the output swing of the filter is well defined at 250mV peak-peak, it should not be made to swing beyond this limit under any boost setting. For a given boost setting input amplitude should be decreased such that output signal swing is maintained at this value. Thus, while performing transient simulations with maximum boost setting, amplitude of both the tones is decreased by 24dB. Fig. 37 shows the results obtained. The third order intermodulation distortion is at -51dB. Note that IM3 performance seems better for 24dB boost setting than that for 0dB

setting. This can be explained as following: With 24dB boost setting, input is scaled down to maintain nominal swing at the output of the filter, but not all OTAs in the filter experience a nominal gain. For example input to the biquad 1 would be -24dB down from the nominal voltage and input to the biquad 2 would be -12 dB down the nominal voltage. Thus IM3 performance for boost setting seems to be better than the one with 0dB boost setting. Also note that, this is just a simulation-set-up artifact. In the actual system one does not have to scale down the input at highest boost setting. (As boost gain cancels the channel attenuation).

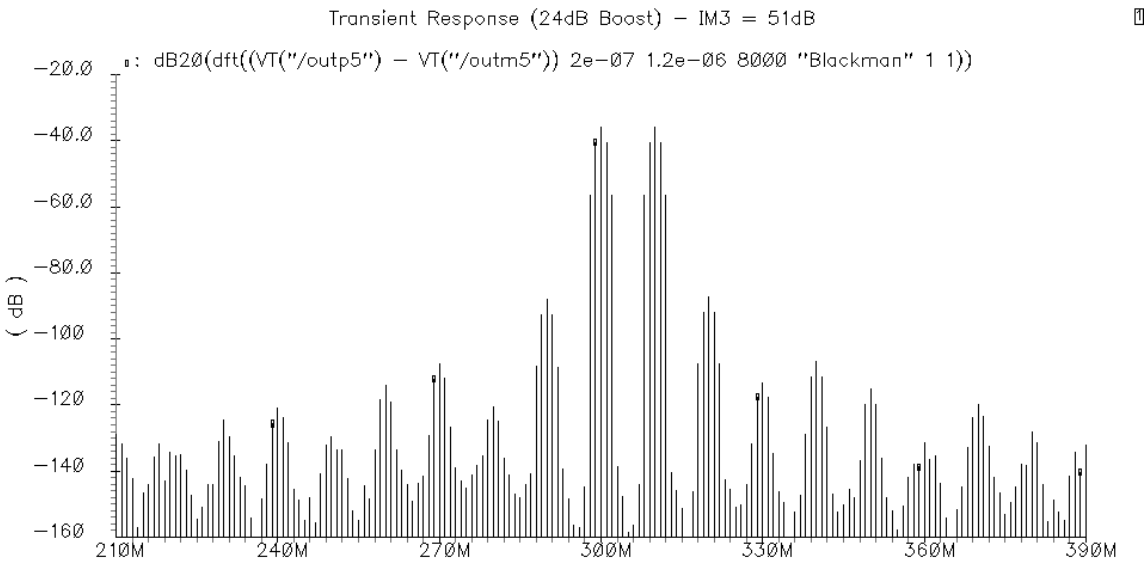

Fig. 37. Output spectrum obtained for intermodulation test at 24dB boost setting

B. Layout and Fabrication

Layout of the entire filter was done using Cadence Layout Artist software. Before the layout was done, an elaborate floorplan was designed. The outline of each sub-block was decided based on the rough estimated area. These outlines were used to draw a floorplan optimizing the placement of sub-blocks, signal path and power distribution. Fig. 38 shows the designed floorplan. Notice that the signal path consisting of Biquad1, Biquad2 and the first order section is folded twice in order to minimize the total silicon area.

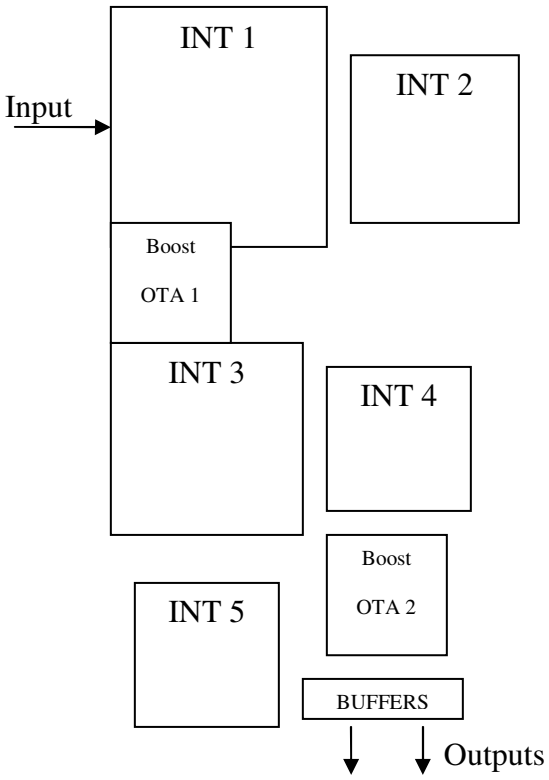

Fig. 38. The floorplan of the boost filter IC (not to scale)

Signal lines pass through the middle each sub-block and signal path is kept clean of any large parasitic. The power lines are routed along the top and bottom boundaries of the sub-blocks. Since boost transconductors are the largest OTAs, these are placed such that the parasitic are minimized for their inputs as well as outputs. To drive the input impedance offered by typical test equipment (50 Ohms), a buffer transconductor is placed after the filter. A similar buffer is also used in stand-alone calibration path in order to de-embed the filter's response from the overall response obtained through the buffer. Most importantly, the inputs and outputs of the filter as well as calibration path are placed as near as possible to pad locations. Capacitors are fabricated using 2 poly layers available in this technology. In order to maintain capacitor ratios across different nodes, all capacitors are fabricated using arrays of unit cells. Unit cell of 50fF is used. Rest of the capacitors are array of this unit cells, where the routing pattern is kept similar across different capacitors to have a true scaling of routing parasitic as well. Dummy unit cells are used whenever appropriate and array is arranged in the common centroid patterns. Layout of all the OTAs is done with interleaved fingers of input differential pair in a common centroid fashion.

The chip micrograph with picture of the filter's layout in inset is shown in Fig. 39. The power routing was done using thick top metal lines. This not only minimizes the I-R drop on supplies but also help meet the electromigration rules for high current density lines. Layout pattern and length of input and the output lines of the main filter are matched to that of the calibration path in order to minimize mismatches between the two paths. Finally, dummy metal cells are placed throughout the layout to meet local as

well as global metal density rules. This prevents over-etching of any isolated thin metal line when CMP (chemical-mechanical polishing) is performed as the fabrication step. The chip was packaged in the LQFP 48 pin package.

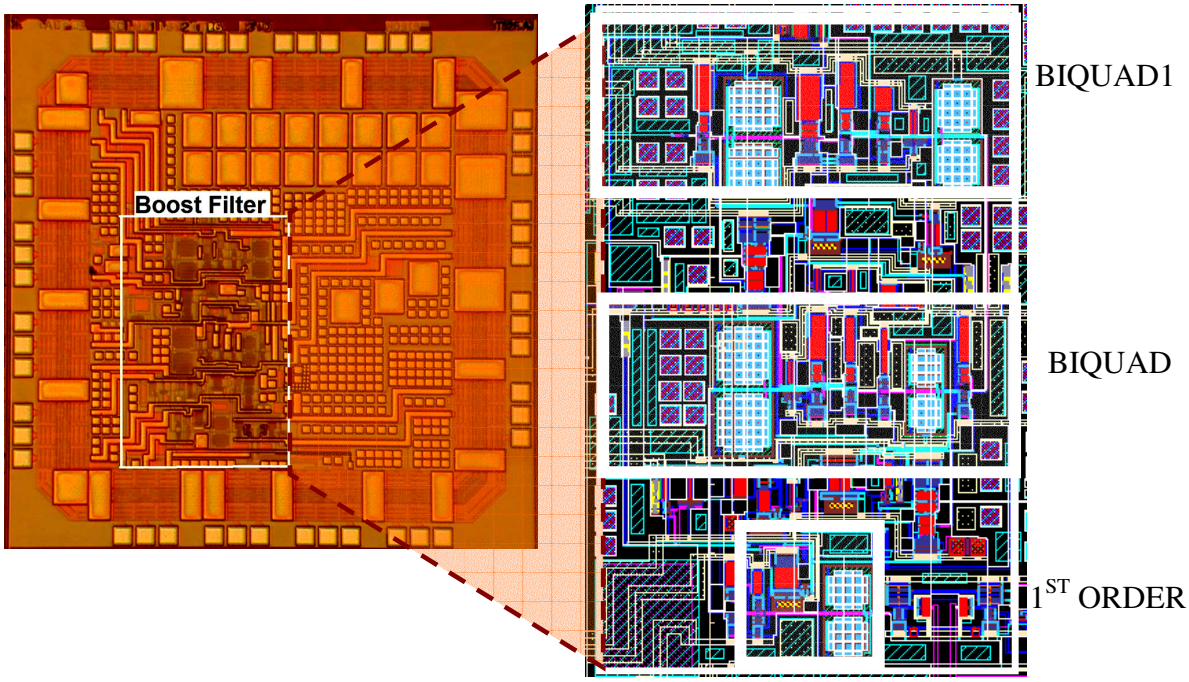

Fig. 39 Chip micrograph with layout inset

C. Experimental Results

A dual supply of +/-1.65V is used for all experiments. Most of the measurements were performed using a 500MHz network analyzer. Both signal paths: main filter and the buffer are characterized. Buffer's gain is de-embedded from the observed filter's response. Fig. 40 shows the picture of the measurement board.

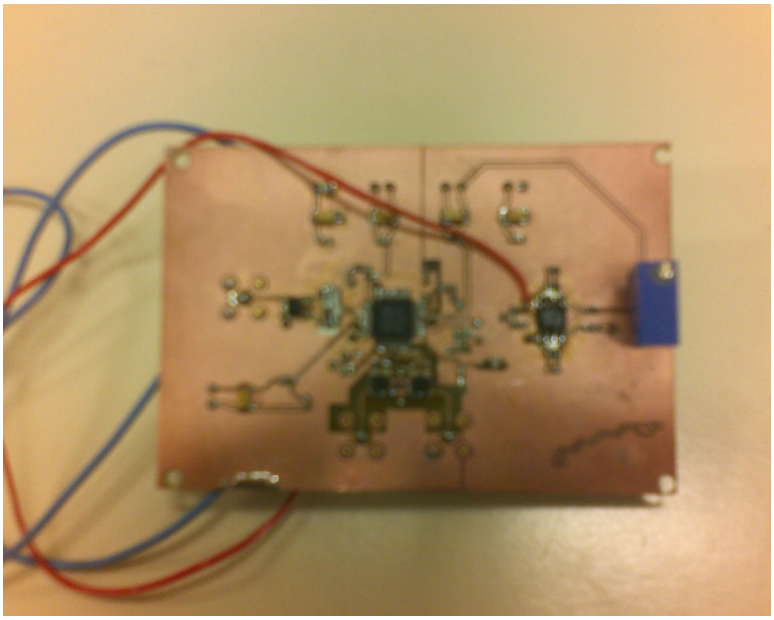

Fig. 40. The measurement board

Fig. 41 shows the filter transfer function obtained across various boost settings after calibration. The -3dB bandwidth measured with 0dB boost setting is 330MHz and the maximum achievable boost is about 28dB. Fig. 42 shows the group delay response of the filter; the group delay around cutoff frequency varies by 400pS (16%) between 0dB to 24dB boost. This is attributed to finite output impedance of OTAs.

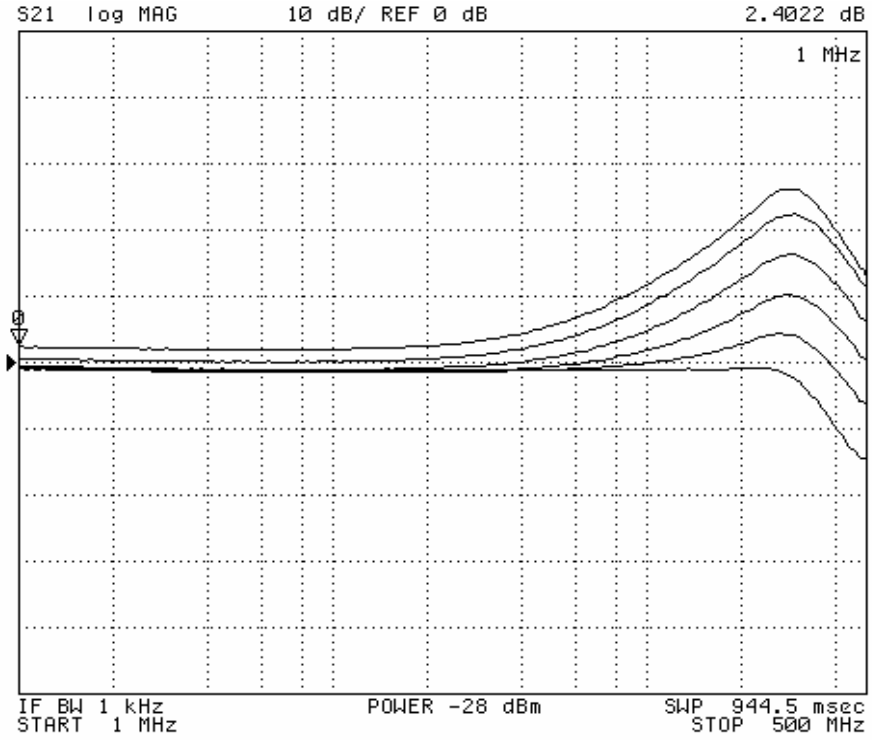

Fig. 41. Measured transfer function (magnitude) of the filter for varying boost settings

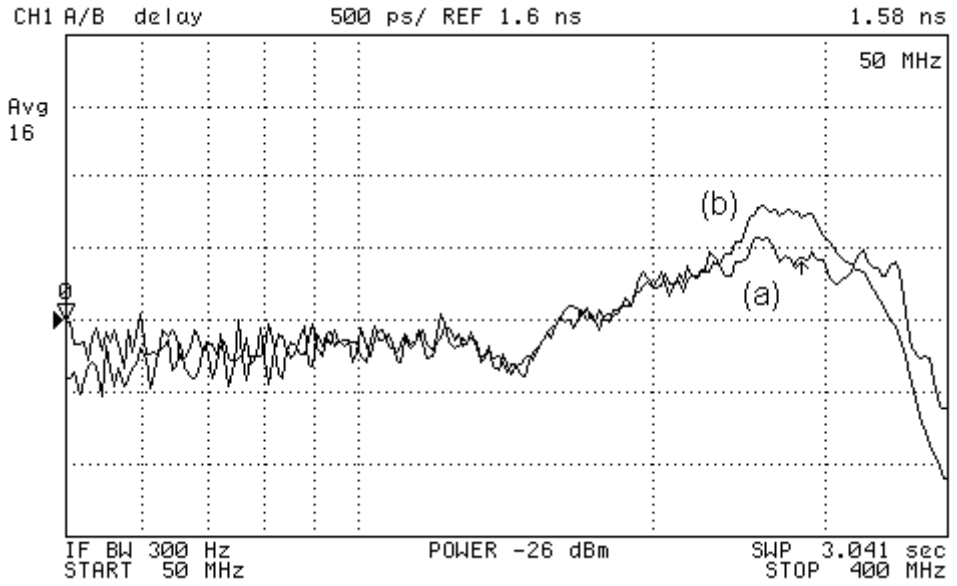

Fig. 42. Measured Group delay for 0dB (trace a) and 24dB boost conditions (trace b)

Filter's linearity performance was measured around the highest frequency of interest using two-tone intermodulation tests. Fig. 43 shows the spectrum obtained from this test: two tones are applied at 304MHz and at 307MHz with 250mV of total peak to peak swing; the boost gain was set at 0dB. The measured third intermodulation distortion (IM3) is around -41 dB.

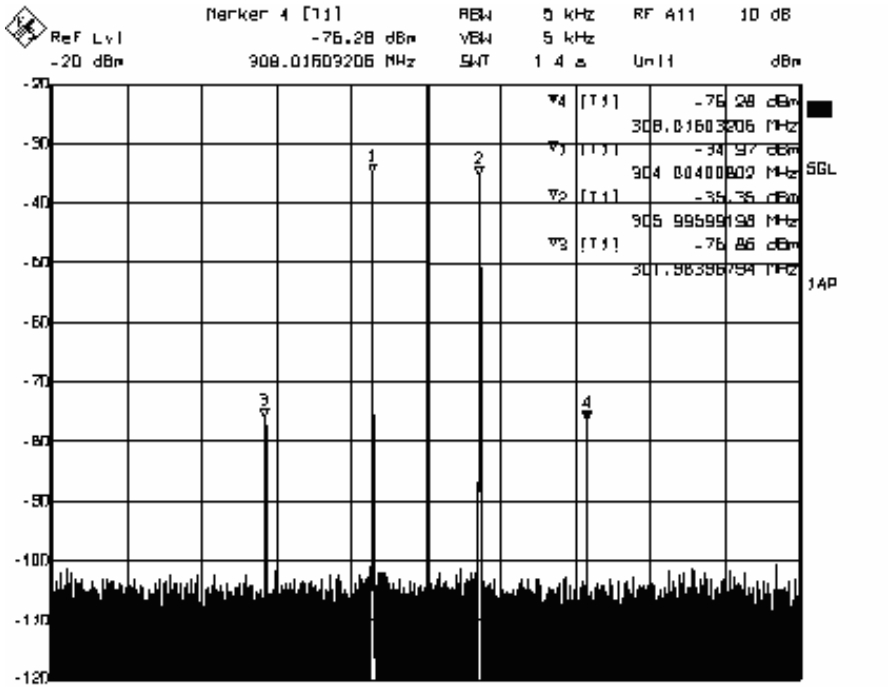

Fig. 43. Intermodulation test for the boost filter with tones at: f_{O1}=304MHz and f_{O2}=307MHz

Intermodulation distortion is characterized for the entire signal band. The two tones are swept from 100 MHz to 300MHz. Fig. 44 depicts the variation of IM3 for different frequencies; the frequency spacing of the two tones was 3MHz in all cases.

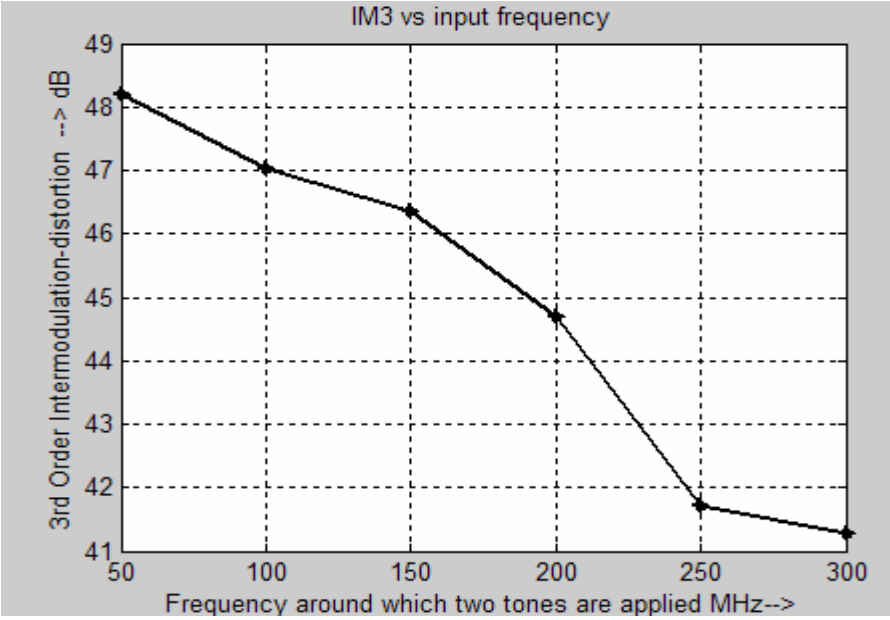

Fig.44. IM3 as a function of average test frequency $(f_{O1}+ f_{O2})/2$

The experimental results are summarized in Table 9.

TABLE 9

PERFORMANCE SUMMARY BASED ON EXPERIMENTAL RESULTS

Parameter	Value
Bandwidth at no boost	330MHz
Maximum Boost	25dB
Power	43mW
IM3* (Boost=0dB)	-41dB
Output Swing	250mVp-p
SNR (Boost=0dB)	49dB
Technology	0.35µm
Total Area	$0.5mm^2$

* Measured with two-tones centered at 305MHz and total peak to peak magnitude of 250mV

Although it is very difficult to have a fair method of comparison, a reasonable figure of merit is developed to roughly compare this design with other OTA-C filters with different boosting factors. A generic figure of merit for continuous time filters in terms of bandwidth, SNDR, order and power is defined in [20]. In order to accommodate different boost gains, we need to modify the generic figure of merit. Based on the power consumption of various blocks it was found that each octave of boost costs as much power as one of the poles of the filter. Hence, a boost factor equal to the maximum boost expressed in number of octaves is added to the order of the filter and figure of merit (FOM) is defined as:

$$FOM = \frac{BW * L * DR * (Order + Boost\ \ Factor)}{Power} \tag{5.1}$$

where BW is the filter's bandwidth expressed in MHz, SNDR is filter's signal to noise + distortion power ratio in linear scale and power is expressed in watts. The minimum technology size in meter (L) is also included in FOM in order to make a fair comparison of filters designed in different technologies [21]. Table 10 highlights the comparison between the design reported here and other filters with boost. It is shown that the design reported here is a power efficient solution with highest f_{3dB} and highest boosting factor.

TABLE 10

READ CHANNEL FILTERS: A COMPARISON

Ref.	BW (MHz)	Boost (dB)	Filter's order	SNDR (dB)	Technology Feature (μm)	Power (mW)	FOM
[5]	200	13	7	40	0.25	210	22
[6]	50	13	7	40	0.7	40	80.2
[7]**	120	14	8	42	0.25	120	41
[8]*	43	12	7	40	0.6	90	26
This Work	**330**	**24**	**5**	**40**	**0.35**	**43**	242

* Power includes automatic tuning circuit

** Power includes gm stabilization loop

CHAPTER VI

SUMMARY AND CONCLUSIONS

Increasing demand of high data rate systems has driven the rapid evolution of disk drive technology. Low power, high performance read channel systems have become critical for this development. This dissertation analyzes one of the most important blocks of the read channel: a boost filter. Existing architectures for implementation of boost filters have been analyzed for their merits and demerits and an architectural solution that can be used to realize low power, high boost wideband filters has been proposed. Building blocks for the OTA-C filters: the OTA and CMFB loop have been examined in circuit details with aim to increase the power efficiency of the system. The most popular wideband OTAs are analyzed and it has been demonstrated that a complementary OTA is an optimum choice for its power efficiency. A widely programmable OTA for the boost transconductor, which keeps input and the output capacitance constant across the boost range, has been designed using well known Gilbert cell. A wideband CMFB amplifier with high DC gain is also introduced. The architecture and the design concepts were demonstrated with a silicon prototype of fifth-order Butterworth filter fabricated using 0.35μm CMOS technology. A 330MHz bandwidth with 24dB boost is obtained for the power dissipation of 43mW from a 3.3V supply. Third order intermodulation is obtained to be -41dB. The experimental results are found to agree well with the simulations.

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VITA

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