IMPLEMENTATION OF A 1GHZ FRONT END USING TRANSFORM DOMAIN CHARGE SAMPLING TECHNIQUES

A Thesis

by

MANDAR SHASHIKANT KULKARNI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2008

Major Subject: Electrical Engineering

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ABSTRACT

Implementation of a 1GHz Front End Using
Transform Domain Charge Sampling Techniques. (December 2008)
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The recent popularity and convenience of Wireless communication and the need for integration demands the development of Software Defined Radio (SDR). First defined by Mitoal, the SDR processed the entire bandwidth using a high resolution and high speed ADC and remaining operations were done in DSP. The current trend in SDRs is to design highly reconfigurable analog front ends which can handle narrowband and wideband standards, one at a time. Charge sampling has been widely used in these architectures due to the built in antialiasing capabilities, jitter robustness at high signal frequencies and flexibility in filter design.

This work proposed a 1GHz wideband front end aimed at SDR applications using Transform Domain (TD) sampling techniques. Frequency Domain (FD) sampling, a special case of TD sampling, efficiently parallelizes the signal for digital processing, relaxing the sampling requirements and enabling parallel digital processing at a much lower rate and is a potential candidate for SDR. The proposed front end converts the RF signal into current and then it is downconverted using passive mixers. The front end has five parallel paths, each acting on a part of the spectrum effectively parallelizing the front end and relaxing the requirements. An overlap introduced between successive integration windows for jitter robustness was exploited to create a novel $sinc^2$ downsample by two filter topology. This topology was compared to a

conventional topology and found to be equivalent and area efficient by about 44%. The proposed topology was used as a baseband filter for all paths in the front end.

The chip was sent for fabrication in 45nm technology. The active area of the chip was $6.6mm^2$. The testing and measurement of the chip still remains to be done.

To Aai and Baba

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CHAPTER I

INTRODUCTION

The advent of wireless era has made access to information easier than ever before. Several wireless standards exist today and new standards are being defined for better data rates and range. As the need for all these standards to be integrated on a single handset arises, putting a transceiver for each standard makes the handset bulky as well as costly. The Software Defined Radio (SDR) shows a promising path towards the integration of multiple standards.SDR was first defined by Mitola [1] where the approach was to push the ADC and DAC towards the antennas and then perform all other operations such as downconversion, filtering etc. in the digital domain. This approach would require an extremely high speed and high dynamic range ADC. Such an ADC would require enormous amount of power. The approach in recent research has been to create a reconfigurable multistandard receiver with hardware reuse. Such architectures have been reported in [2], [3], [4] with highly tunable baseband filtering schemes. Multistandard ADCs have also been published [5] [6] that are aimed to follow such tunable baseband topologies.The approach described before is a step away from the original concept of Mitola's architecture. This work is an attempt to create a wideband front end which would simultaneously process the information. Transform Domain (TD) sampling has been proposed for UWB and multicarrier receivers [7] [8] and is very promising for implementation of an SDR. Frequency Domain (FD) Sampling; a special case of TD sampling, is a practical solution for circuit level implementation. FD sampling also makes use of Charge sampling which has been widely used in above mentioned SDR implementations.

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Charge sampling is also known to offer several advantages over conventional voltage sampling [9]. The multipath topology of the FD sampler makes it a natural choice for SDR, wherein the number paths can be chosen according to the bandwidth of the input channel [10].

A. Motivation

Charge sampling can be used to create FIR and IIR type of filter functions, a combination of these techniques have been effectively used to meet the required filter specifications [2],[11]. Charge sampling is known to have a built in sinc antialiasing filter with nulls at multiples of the sampling frequency.

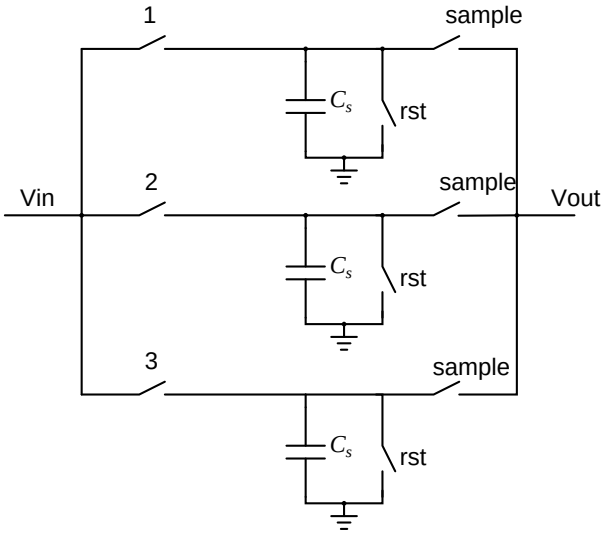


Fig. 1. An example of a *Sinc* downsample by 3 circuit

The null depth of the sinc is determined by the sampling rate and thus the antialiasing specifications sets the initial sampling rate which is usually much higher than required at the output and hence the need for downsampling arises. However, after downsampling the sampling frequency changes and the spectrum folds back. Thus, downsampling must be coupled with antialiasing filter. Since the signal is

already sampled, the downsampling can be easily achieved by adding the sampled voltages together using capacitors and switches. A downsampling by three circuit is shown in the Fig. 1. It is easy to see that the summing operation creates an FIR filter with a sinc type filter response with nulls at one thirds of the original sampling frequency. Now the sampling frequency is also one thirds of the original sampling frequency. Thus the nulls of the sinc are at the multiples of the new sampling frequency. Thus, this FIR filter now acts as an antialiasing filter for the new sampling frequency.

This approach although fairly easy, might not be sufficient to meet the filter requirement after the downsampling operation. The need to do better than sinc downsampling filter can be easily achieved by sizing the capacitors in the downsampling circuit. $Sinc^2$ and $Sinc^3$ type of downsampling has been demonstrated in [2],[12]. A novel topology has been proposed in this work to perform a $Sinc^2$ and downsampling by a factor of two. This topology makes use of the overlap introduced between successive integration windows and realizes the $Sinc^2$ filter response. This topology was compared to a conventional topology [12] and found to be equivalent and area efficient by about 44%.

In this work, a 1GHz front end has been implemented using FD sampling techniques. The proposed front end converts the RF signal into current and then it is downconverted using passive mixers. The front end has five parallel paths, each acting on a part of the spectrum effectively parallelizing the front end and relaxing the requirements. The proposed filter topology was used as a baseband filter for all paths in the front end.

B. Organization of Thesis

Chapter II presets an overview of Software Defined Radio (SDR). The first definition of SDR proposed by Mitola and the current state of progress in the field is discussed. Transform Domain (TD) sampling is discussed as a potential candidate for SDR using multipath architecture. Frequency domain sampling with charge sampling technique is proposed for the implementation of the front end.

In Chapter III, charge sampling is compared to voltage sampling and its advantages in terms of antialiasing filtering and jitter robustness is discussed. Basic FIR and IIR filter topologies and their frequency responses are discussed.

Chapter IV, the Frequency Domain (FD) receiver is discussed. Matlab simulations comparing the proposed receiver and an OFDM receiver with same specifications are presented. The optimum number of paths and the required LO frequencies for the FD receiver are determined. Blocks necessary for circuit level implementation of the FD receiver are briefly discussed.

The highly linear transconductance (Gm) stage is presented in Chapter V. The need for high linearity are explained and the criteria for selecting the topology are discussed. The linearity is verified using simulation results.

Chapter VI discusses the pros and cons of the passive mixer as compared to the active mixer. Passive mixers offer low flicker noise, zero power dissipation and high linearity, all of which are suitable for proposed front end.

In Chapter VII, a novel topology is proposed to implement a $sinc^2$ downconversion by 2 filter. This topology is compared to a conventional topology to implement such a filter. The filter responses of both are plotted and compared. An active integrator implementation for the proposed filter is discussed in detail for the front end. The active integrator OTA design is discussed in detail with simulation results.

Overall noise calculations for the baseband filter are presented.

Chapter VIII discusses the digital circuits used for to generate necessary clocks for the baseband filter. The I-Q generation circuit for generation of I and Q LO frequencies is also discussed. The operation of these circuits is explained using clock waveforms.

Finally, Chapter IX shows the layout snapshot for the chip. Some layout considerations for certain blocks of the front end are discussed.

CHAPTER II

BACKGROUND

The popularity and convenience of Wireless communication services is well known. Every device today is now capable of wirelessly transmitting and receiving data from other devices or from towers. New wireless standards come up from time to time for a certain specific application and the consumers demand it to be included in their handsets. To add a separate transmitter and receiver for every standard means increase in the handset size and cost as well. Thus, the need for a programmable Software Defined Radio (SDR) arises.

A. Software Defined Radio (SDR)

Software-Defined Radio was defined by Mitola [1] which pushed the ADC and DAC towards the antenna and the filtering and all other operations were done in digital domain (Software). This means that the SDR would require an extremely high resolution and fast ADC which would require very high power dissipation. As technology progresses, it might be possible to realize a practical ADC for the SDR. However, for now the general trend in the field of SDR has been to design highly reconfigurable analog front ends which can handle several standards [2],[4]. In [2], the SDR is restricted to processing of one standard at a time and reconfigurability of the baseband has been effectively shown for narrowband GSM standard with channel bandwidth of 1MHz and broadband 802.11g standard with channel bandwidth of 20MHz. In [4], a novel approach is adopted in employing the widely used sinc FIR filter and it is followed by a Discrete Time (DT) Low-pass filter. In both these publications and many others related to SDR, Charge Sampling has been extensively used for the advantages it offers over the conventional voltage sampling techniques [9],[13],[14]. Charge sam-

pling provides an inherent anti-aliasing filter along with much easier filter design just with switches and capacitors. This will be explained in the later section. There also has been a significant push towards reconfigurable ADCs to suit such SDRs [5],[6]. However, the maximum channel bandwidth addressed does not exceed 20MHz which is that of WLAN. It can be seen that these SDR topologies are specific to current standards and cannot handle concurrent reception of two or more standards. This approach a step away from that proposed by Mitola where the aim is to improve the ADC and push it as close to the antenna as possible.

Transform Domain (TD) sampling techniques have been proposed for UWB and multicarrier receivers [7],[8]. Frequency Domain (FD) sampling, a special case of TD sampling, efficiently parallelizes the signal for digital processing, relaxing the sampling requirements and enabling parallel digital processing at a much lower rate [10],[15]. This technique can be effectively used to process a wide band of frequencies and hence is a potential candidate for SDR. The TD sampling is discussed in the next section.

B. Transform Domain (TD) Sampling

In conventional time domain sampling, the signal is sampled at particular intervals of time. In case of Transform Domain (TD) sampling [15] the signal is expanded over a set of basis functions and then sampled. The time-domain signal may be reconstructed via a linear digital computation, or signal processing can be carried out directly with the basis coefficients. Frequency Domain (FD) sampling is the specific case of TD sampling where the basis functions are a set of sinusoidal frequencies or hard switched square clocks. The signal information symbols can be reconstructed using FD estimators, including matched filter estimator, least square estimator and linear MMSE estimator [8]. In case of compressed sensing which is one of the poten-

tial application, is applied, the basis functions can be random [16],[17]. To accomplish digital TD processing, a wideband input signal is first mixed with N basis function $\phi_n(t)|_{n=0}^{N-1}$ which determine the number of parallel paths in the receiver. The mixed signal and then integrated for a duration T_c . Then, a set of coefficients are computed in each window via signal expansion over the basis functions. The expansion coefficients become the Fourier series coefficients, hence, the receiver is referred to as the Frequency domain (FD) receiver. The output of the integrators in the 'N' parallel paths at the end of each window provides the N basis coefficients. The windows are overlapped by a small amount (T_{ov}) to provide robustness to jitter and to eliminate the high frequency artifacts. The M overlapped windows that cover the entire signal block provide a total of MN coefficients $R_{m,n}|_{m=0}^{M-1}|_{n=0}^{N-1}$, that are computed as,

$$R_{m,n} = \int_{mT_s}^{mT_s+T_c} r(t)\Phi_n^*(t)dt$$

Where $T_s = T_c - T_{ov}$; $r(t)$ is the received wideband signal, $m = 0$ to $M-1$ indicates the indicates the m^{th} segment in each parallel path and $n = 0$ to refers to the n^{th} parallel path. The projection of the received signal onto different $N-1$ basis functions in each parallel path means that each path operates only on a fraction of the input signal bandwidth. This relaxes the tracking bandwidth requirements for the ADC that quantizes the basis coefficients thus minimizing power consumption. These quantized co-efficients are processed digitally to estimate the symbols directly using different estimation techniques mentioned before. The direct estimation of symbols from these coefficients eliminates the need to reconstruct the time-domain signal which greatly reduces the complexity of the receiver.

The FD receiver was implemented using Charge sampling. Charge sampling offers many advantages over conventional voltage sampling. A brief discussion of Charge domain sampling techniques is done when the baseband filter section.

CHAPTER III

CHARGE SAMPLING

In charge sampling, the signal current in integrated on a capacitor C for a certain time window T and then read out at the end of integration.

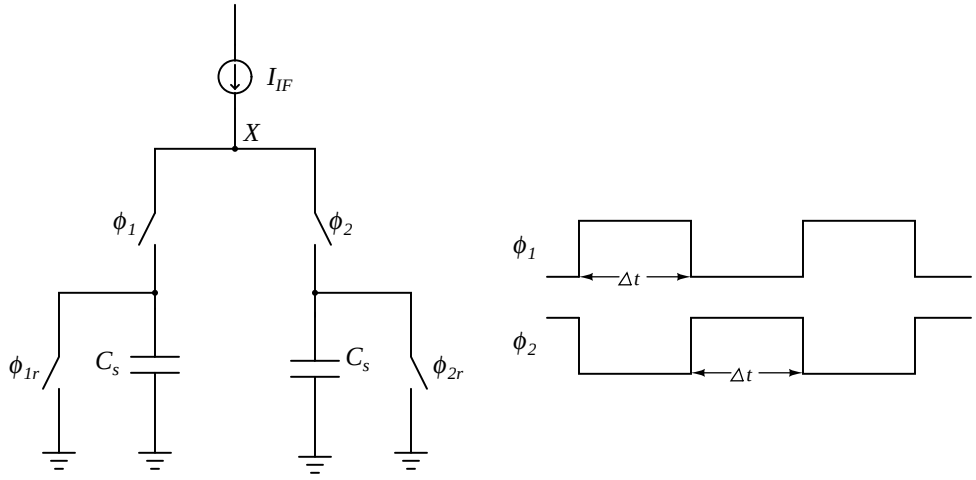


Fig. 2. Schematic and clock scheme for charge sampling

This operation creates a sinc filter with nulls at multiples of sampling frequency [9] . The capacitor is discharged at the end of the read out operation. The schematic of the sampling scheme and the clock phases are shown in the Fig. 2.

The discharge phases are not shown. For the ease of reading out and discharging operations, the signal is integrated on two separate capacitors in alternate time windows and the output is interleaved between them. The frequency response of the windowed integration is given as,

$$H(f) = \frac{Gm\Delta t}{C} sinc(\pi f \Delta t)$$

The sinc filter response is shown in Fig. 3, where $fs = 1/\Delta t$. It can be seen that the positions of the nulls is independent of the capacitor size or the value of the

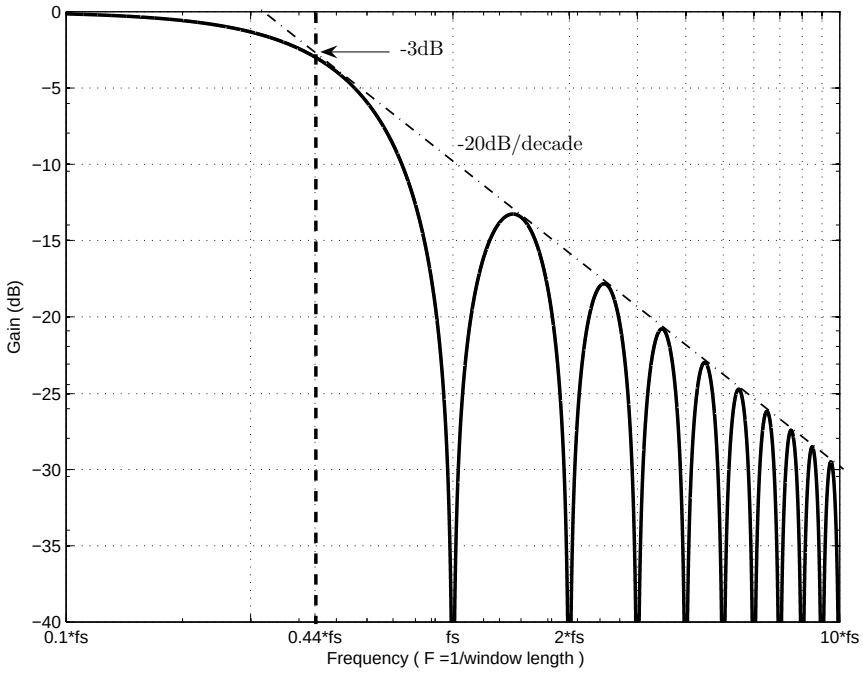


Fig. 3. Sinc filter response

transconductance and solely depends on the length of the integration widow. This gives us great flexibility in terms of the sampling rate. The sinc filter response has a slope of -20dB/Decade, however the nulls at the multiples of the sampling frequencies make it an antialiasing filter. In comparison to other filter topologies where the filter needs to have much larger slope to fulfill the antialiasing requirement at fs. The discharging of the capacitor at the end of each integration phase removes any memory and creates an FIR filter.

However, the addition of the history capacitor can be use to realize an IIR type of filter response as shown in Fig. 4. The IIR filter response can be seen in Fig. 5. Along with the original sinc filter response, the history capacitor produces a response which has poles at the multiples of the sampling frequency. Ideally, the poles completely cancel with the nulls and the response is smooth and the gain at DC is infinite. This is true only when the value of history capacitor is much greater than the sampling

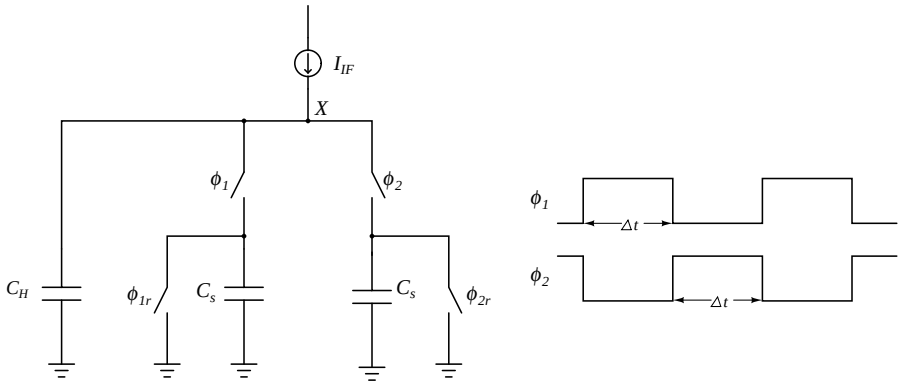


Fig. 4. Addition of a history capacitor to charge sampling ciruit

capacitor. Otherwise, the nulls and poles are slightly off with respect to each other and do not completely cancel out and the DC gain is also limited as seen in the figure.

A combination of these techniques can be effectively used to meet the required filter specifications [2],[11]. The initial sampling rate for the sinc filter is usually much higher than required at the output and hence the need for downsampling arises. However, after downsampling the sampling frequency changes and the spectrum folds back. Thus, downsampling must be coupled with antialiasing filter. Since the signal is already sampled, the downsampling can be easily achieved by adding the sampled voltages together using capacitors and switches. An example of such a downsampling was shown in the introduction.

In comparison to voltage sampling, charge sampling is shown to have better clock jitter tolerance as the frequency of the clock signal increases [9]. The total integrated noise in case of voltage sampling is kT/C, however the noise in case of charge sampling can be more that kT/C if not properly designed.

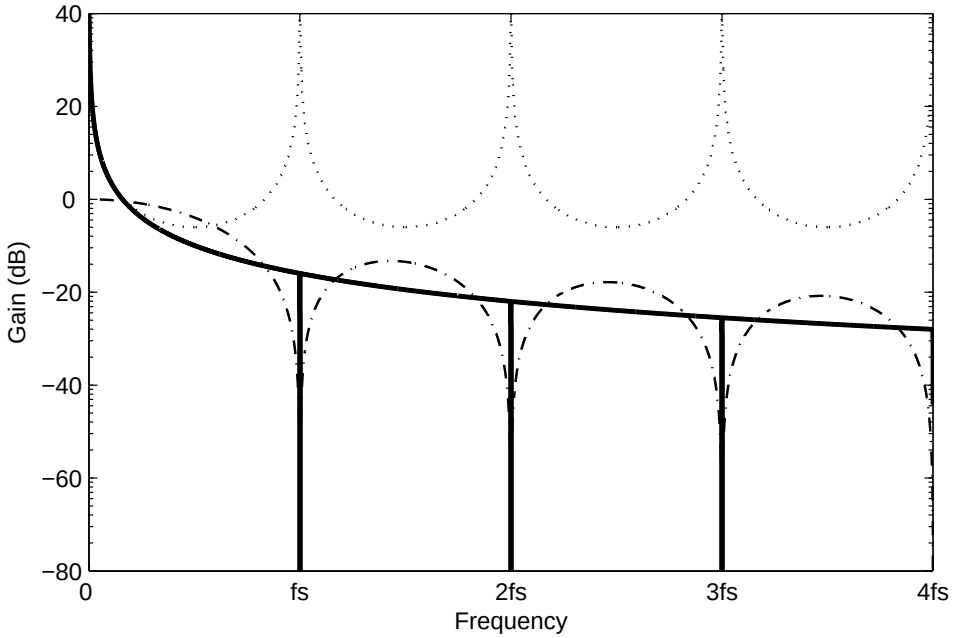


Fig. 5. IIR filter response

CHAPTER IV

FRONT END ARCHITECTURE

The front end was aimed to receive a wide range of input frequencies. The input bandwidth to be processed was decided to be 1GHz. Flicker noise is a serious problem in subnanometer technologies and the corner frequency for the noise can extend up to a Gigahertz. To tackle this issue the input range of frequencies was set to be 1GHz to 2GHz. The FD receiver was extensively simulated in MATLAB for optimum performance. The number of parallel paths was determined to be 5 with I and Q channels in each path.

A. System Simulations in MATLAB

The overall block level system architecture is shown in Fig. 6. The system performance was compared with an OFDM receiver with conventional voltage sampling. The input to the system was a quadrature phase-shift key (QPSK) modulated signal of 128 carriers with bandwidth of 1 GHz from 1-2 GHz. The quadrature mixing signals (I and Q) used in each path form the basis functions. The five LO frequencies were chosen to be orthogonal to the carrier frequencies. The downconverted signals were filtered by a second-order RC filter with cutoff of 100 MHz as each path operates only on a subband of the entire bandwidth. The output of the baseband filter is integrated over a time window of duration 6 ns. Each window is overlapped by 2ns to its previous and next window, which introduces oversampling and also increases jitter robustness. The integrated outputs form the FD basis coefficients were processed digitally to recover the data. The same multicarrier signal is applied to a conventional OFDM receiver. The OFDM system had a single I and Q path has a single square mixing signal at 1.5 GHz. The baseband filter ws a second-order RC filter whose

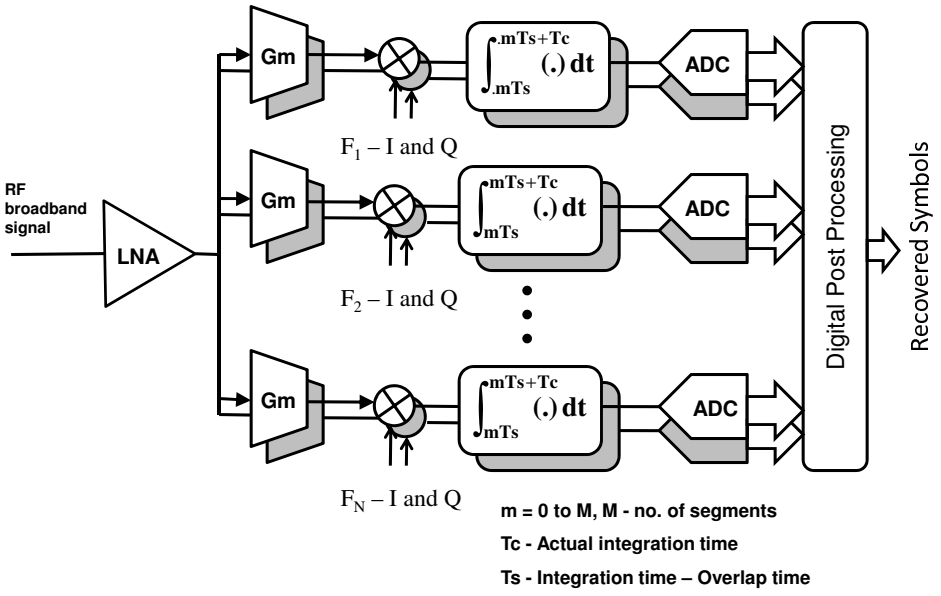


Fig. 6. FD multipath system architecture

cutoff frequency is chosen to be 500 MHz to cover the entire signal bandwidth. The output of the baseband filter was sampled with the same effective sampling rate of the FD receiver.

The detection of symbols was carried out using the FFT algorithm. Jitter with a standard deviation of 1ps was introduced in both receivers. In the FD receiver, jitter was introduced in all the 5 mixing signals (I and Q) and also at both edges of the integration window. In the OFDM receiver, jitter was introduced in the mixing signal and also in the sampling clock. Fig. 7(a) shows the comparison of the performance of FD receiver and OFDM [15]. In this plot, signal-to-noise-distortion ratio (SNDR) of the recovered symbols is plotted across carrier frequencies. In this case, jitter in mixing signals and sampling clocks is the only source of distortion.It can be seen that the FD receiver shows no significant deterioration in performance despite the

presence of more jitter sources. This is because of the superior anti-aliasing filtering in each path. The dominant jitter source in each path is the mixing signal at the center of the corresponding subband and the distortion from other jitter sources is mitigated by the filter. Due to parallelization, the sampling clocks are slower in the FD receiver than in the OFDM receiver. This translates to a greater jitter tolerance in the sampling clocks in the FD receiver. In the above example, for the same overall performance, the FD receiver can tolerate rms jitter of about 15 ps in the sampling clocks, but the OFDM receiver can tolerate only 5 ps of rms jitter. This results in considerable power savings in the design of buffers for the clocks in the FD receivers. In order to demonstrate the additional anti-aliasing filtering provided by the windowed integration in FD receiver, the baseband anti-aliasing filters were removed in both the FD and OFDM receivers and the performance is analyzed in the presence of jitter. Fig. 7 shows the performance of the FD receiver and OFDM receiver in the absence of any baseband filter.

B. Circuit Level Implementation

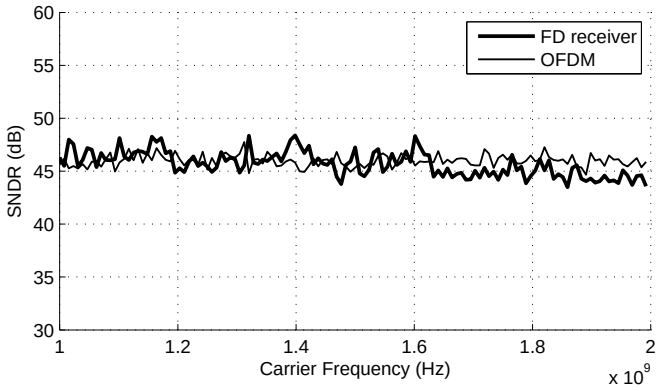
The FD receiver was implemented at the circuit level in 45nm technology. Since the input bandwidth is 1GHz, for a wireless system, the input noise can be calculated as,

$$\begin{aligned} \text{Input Noise Level}((N_{in})_{dBm}) &= -174 + 10log_{10}(BW) \\ &= -84dBm \end{aligned} \tag{4.1}$$

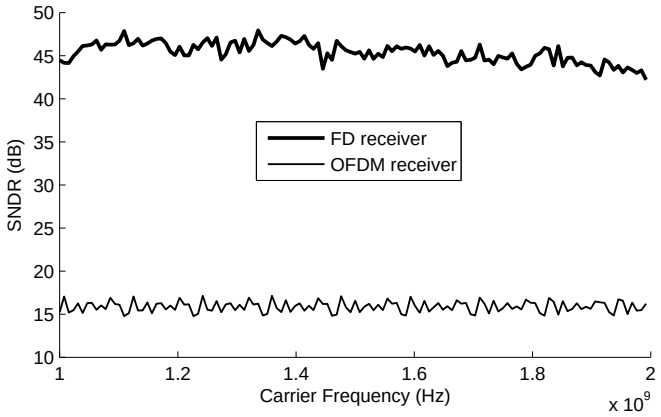
It can be seen that, as a wireless system the front end will have very less sensitivity. Therefore, the LNA was removed from the front end and the system will not be a wireless system. The first stage will be a highly linear transconductance stage.

The transconductance stage was implemented using conventional schemes. A passive mixer was chosen as it offers several advantages over active mixer which suited the receiver needs. The I-Q mixing signal will be generated by using a divide by two circuit which requires twice the mixing frequency as input. These signals were assumed to be off-chip differential sinusoids generated by accurate equipment. The sinusoids were converted to square using a comparator and then divide by two circuit is implemented using Flip-Flops. The signal current is then integrated on a capacitor and then read-out. An active integrator topology is chosen as it provides more linearity. The clock phases required for the baseband filter are generated using a Johnson counter. Each block will be discussed in detail in later sections.

The system was aimed to give about 10 bit performance. Thus, each block was designed for more than 10 bits of linearity. The noise contributions, linearity requirements and design details for each block are discussed in detail in their individual sections.



(a) Performance of FD receiver and OFDM in the presence of jitter with a second-order filter used after downconversion



(b) Performance of FD receiver and OFDM in the presence of jitter without any baseband filter after downconversion

Fig. 7. Performance comparison of OFDM and FD receiver

CHAPTER V

HIGHLY LINEAR TRANSCONDUCTANCE (GM) STAGE

The RF input signal is directly converted to current using a highly linear Gm stage. As the linearity requirement for the Gm stage are very high, the topology chosen was a resistive degenerated MOSFET.

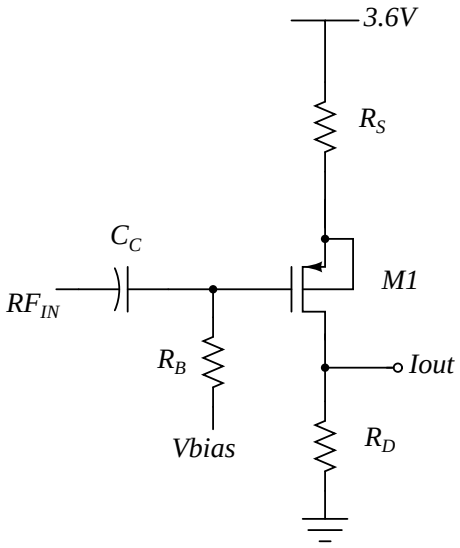


Fig. 8. Topology of the transconductance (Gm) stage - single ended

The topology of the Gm stage is shown in Fig. 8. The schematic is single-ended however the actual implementation is differential. The RF input is capacitively coupled to the gate of the transistor and the biasing voltage is provided through R_B. The input transistor is chosen to be PMOS as the bulk can be connected directly to the source removing the body effect and increasing linearity in comparison to an NMOS, where the body terminal is always connected to ground. PMOS transistors generally have less flicker noise compared to NMOS transistors. However, the flicker noise may be comparable as the technology scales down. The value of the transconductance is nearly equal to $1/R_S$ provided that $gm_{M1} * R_S$ is much more than 1. The load

of the PMOS is also a resistor R_D so as to reduce flicker noise. This topology has the minimum flicker noise possible as the only source of flicker noise is the input transistor. There is also no need of a CMFB circuit to control the output voltage of the transistor as the DC level is fixed by the resistors. The supply voltage needs to be pushed up so as to accommodate for the drop across R_S and R_D. However, the biasing is such that the voltage across any two terminals of the transistor does not exceed the rated breakdown voltage. This is another reason for not using an NMOS input transistor as in case of this topology, the gate-bulk voltage would have exceeded the breakdown.

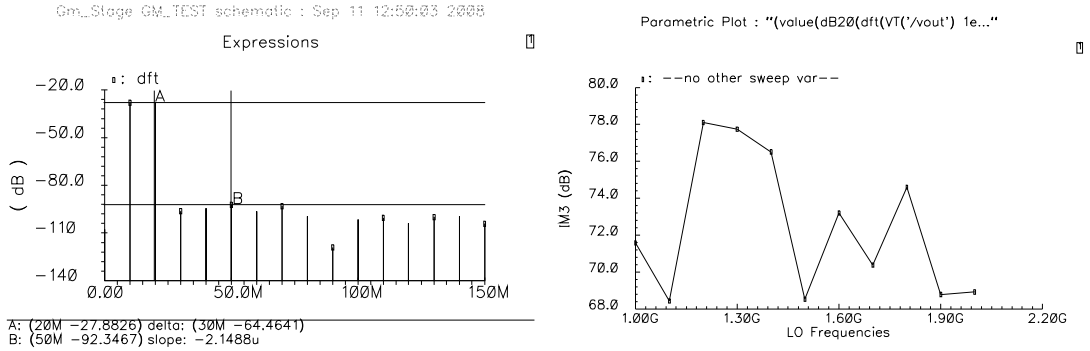
A. Simulation Results

The Gm stage was designed to have an effective transconductance of 1mS. The bias voltage and resistance values were adjusted accordingly. The design parameters are summarized in Table I below,

Table I. Design summary of the Gm stage

Parameter	Value
Vdd	$3.6V$
$Vbias$	$1.6V$
R_S	$1.1k\Omega$
R_D	$1.2k\Omega$
R_B	50Ω
$(W/L)_{M1}$	184(2/0.08)
GM_{eff}	$1mS$

For simplification of measurement, the RF signal was downcoverted using ideal mixer with a LO frequency and IM3 is measured at the baseband frequencies. The IM3



(a) DFT of output current after ideal downconversion, f_1=1.11GHz, f_2=1.12GHz, f_{LO}=1.1GHz

(b) IM3 over the entire signal bandwidth

Fig. 9. Simulation results for the Gm stage

of the Gm stage was measured to be 66dB and almost remains constant over the entire band of input frequencies from 1GHz-2GHz.The simulation results for the Gm stage are plotted in Fig. 9. The Fig. 9(a) shows the IM3 when the two input frequencies are 1.11GHz and 1.12GHz. The output DFT is plotted after ideal downconversion with a LO of 1.1GHz. It can be seen that the fifth order component is dominant. The IM3 over entire bandwidth is plotted in Fig. 9(b). It seems that IM3 is much better at some frequencies. However, other orders are dominant at these frequencies as shown in DFT plot. Even then, the overall IM3 over the entire bandwidth is better than 60dB.

There are some drawbacks of the proposed Gm topology. The absolute value of the resistors in most of the CMOS technologies is very poorly controlled and can vary up to 50%. Thus the biasing of the Gm stage is not very well controlled. However, the supply voltage and the gate bias in externally controlled and can be adjusted to reach the desired bias condition.

CHAPTER VI

PASSIVE MIXER

The basis functions in case of FD sampling are sinusoids or square waves. The expansion of the input signal over the basis functions can be done using a mixer. Passive mixer topology has been used in this front end implementation. Passive mixer has been extensively studied in literature and have been used with charge sampling techniques in[2],[4],[11]. Passive mixers have higher linearity and no power consumption however suffer from conversion loss as compared to its active counterpart [18]. The mixer switches need to be driven with square LO signals so the transistors act like switches. Since there is no DC current in passive mixers, the flicker noise is very low. In the nanometer technology where flicker noise is a major issue, this property of passive mixers makes them an ideal candidate for implementation.

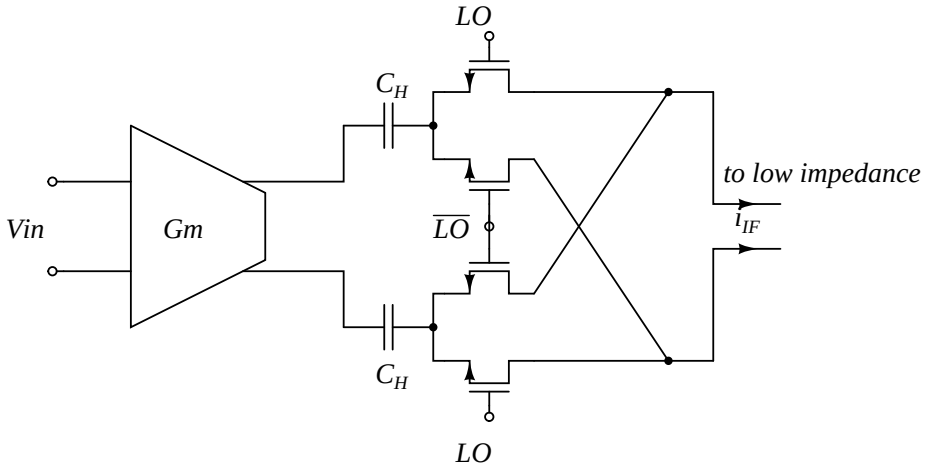


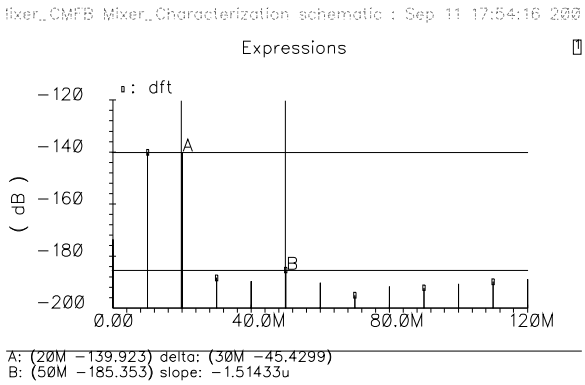
Fig. 10. Passive mixer following the Gm stage

The passive mixer topology is shown in Fig. 10. The output of the Gm stage is capacitively coupled to the passive mixer. This means that the mixer only commutates signal current with zero DC current. The output of the mixer is given to a low

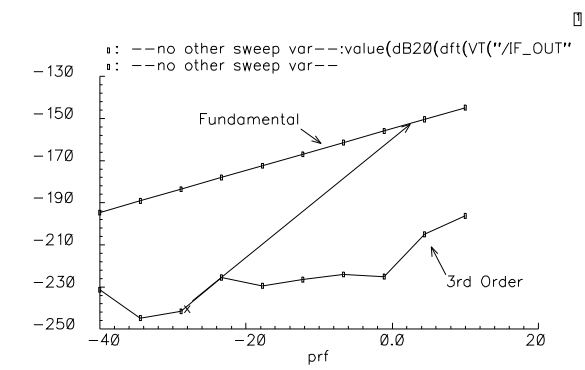
impedance stage. This reduces the signal swing at the output of the Gm stage and hence helps improve linearity. The low impedance stage was implemented using an active integrator circuit which consists of an OTA with sampling capacitor connected between the output and the input terminals. The Miller effect causes the Gm stage and mixer to see very high capacitor or effectively low impedance at its output. Since the DC is blocked by the coupling capacitors, the common mode level of the mixer is determined by the input common mode of the OTA. Since the voltage supply is limited in the nanometer technologies, the input common mode of the OTA is kept low so as to provide more overdrive for the switches of the mixer, increasing linearity. Low input common mode means that the input stage of the OTA will be PMOS input.

A. Simulation Results

The IIP3 of the passive mixer was measured at three different frequency pairs in the band. Due to simulator limitations, the usual IIP3 plot with extrapolation of first and third order component could not be plotted. The following plots were obtained by running the transient simulation and then taking the DFT at the output. The magnitudes of first and third order components were plotted versus the input power level. The common mode level was set to be 420mV and the Vdd was 1.6V. Fig. 11 shows simulation results for the passive mixer. The figure 11(a) shows the DFT of the mixer output with the specified input and LO frequencies. The IM3 is about 45.4dB and was found to be the same over entire signal bandwidth. The IIP3 plot was plotted in 11(b) with specified frequencies. Due to simulator limitations, the extrapolation was done manually in the waveform window. The IIP3 was found to be close to 1dBm and was constant over the entire bandwidth.



(a) DFT of mixer output f_1=1.11GHz, f_2=1.12GHz, f_{LO}=1.1GHz



(b) IIP3 plot for f_1=1.91GHz, f_2=1.92GHz, f_{LO}=1.9GHz

Fig. 11. Simulation results for the passive mixer

CHAPTER VII

BASEBAND FILTER

As mentioned in previous chapters, the successive integration windows were overlapped by time T_{ov}. This overlap was exploited in the baseband filter to create a novel filtering topology. The new filter achieved a $Sinc^2$ downsample by 2 filter with less number of capacitors and switches, resulting in area saving. As there are five paths, each path effectively operates on 200MHz of the frequency band. Each path consists of I-Q paths, hence 100MHz bandwidth is processed by I and Q requiring a sampling rate of at least 200MHz in each. The integration window was chosen to be 6ns and an overlap of 2ns is introduced between successive windows. The data is thus available at the end of 4ns which means the sampling rate is 250MHz for each I/Q path.

A. Implementation of Overlap

As we are performing charge sampling, the output voltage value is the integration of the signal current in the time window. By overlapping two successive windows, it can be seen that there is no loss of signal information as long as the jitter in the windows is less than the overlap period.

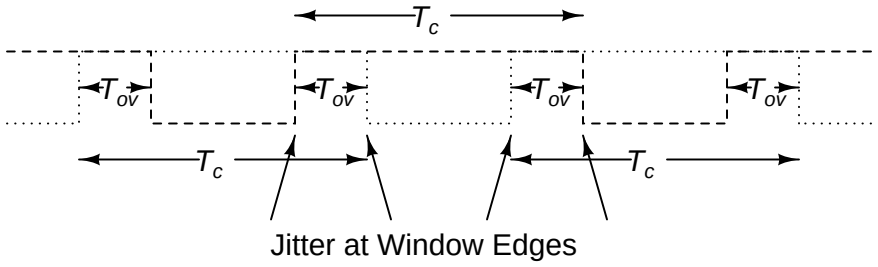
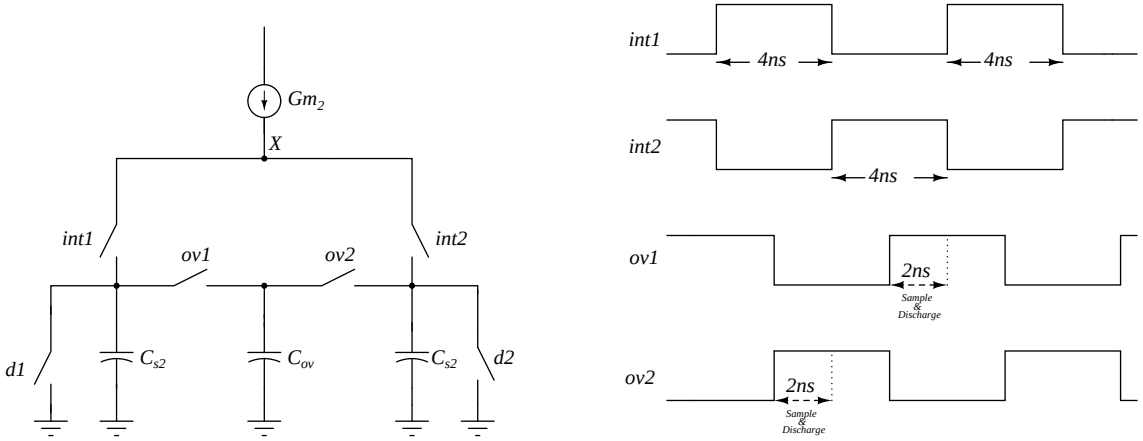


Fig. 12. Overlap between successive windows

The reason for overlapping two successive windows can be clearly understood with the help of Fig. 12. Implementing the overlap with a conventional charge sampling circuit as shown in Fig. 2 in Chapter IV; there will be charge sharing between the two sampling capacitors during the overlap time. This would result in loss of data and the sampling would be ineffective.



(a) (b)

Fig. 13. (a)Novel topology for implementation of overlap (b) Clock scheme for the topology

To overcome this limitation , the overlap was implemented as shown in the Fig. 13. An extra capacitor, C_{ov} with the same size as that of the sampling capacitor, C_s was added to the circuit. Two extra switches with clock phases Φ_{s1} and Φ_{s2} are added to connect the overlap capacitor to the sampling capacitors.

The signal current is integrated for an overall time window of 6ns. The first and last 2ns of this window are shared with the previous and the next window. The overlap capacitor is connected to first sampling capacitors for 2ns after which it is disconnected. The first sampling capacitor still integrates the current for next 2ns, however with double the gain, as capacitor value is halved. The overlap capacitor and the second sampling capacitor is readout and discharged in the meantime. These

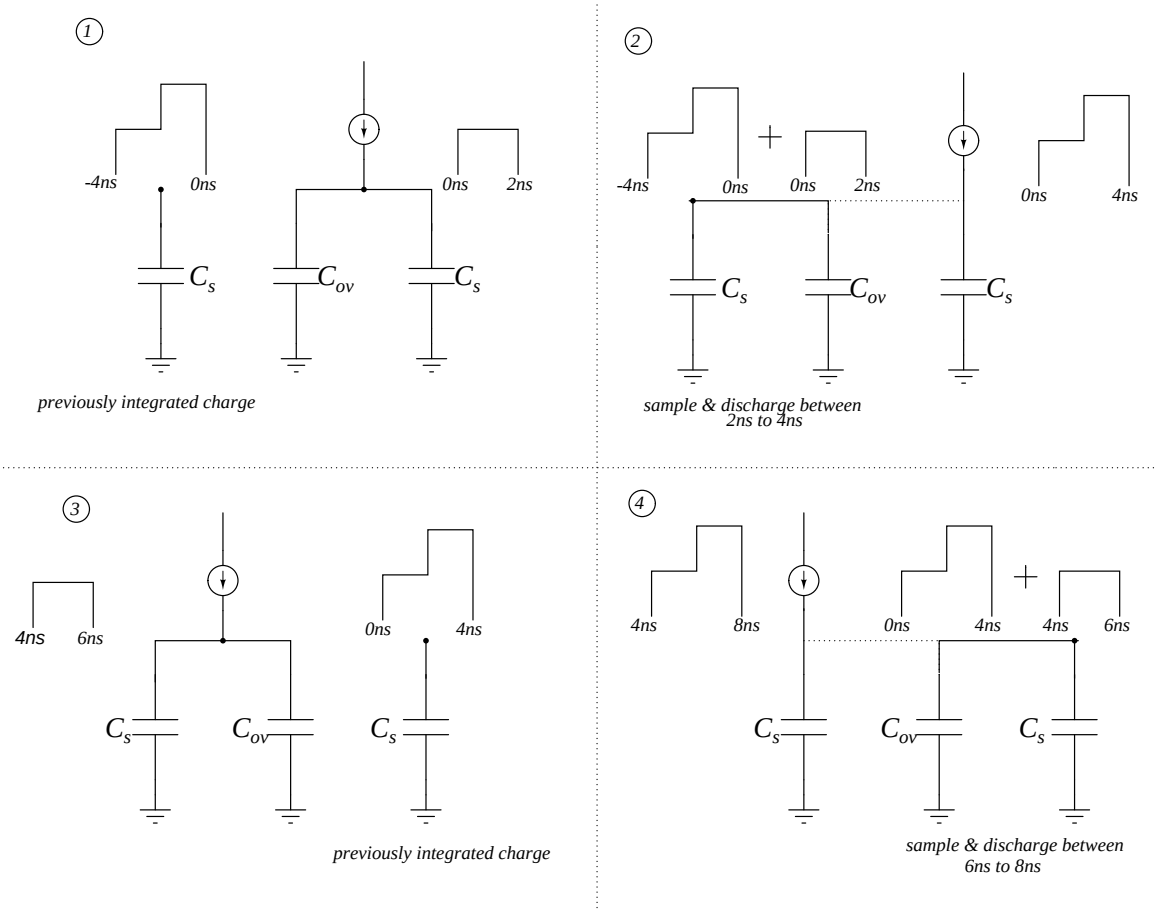


Fig. 14. Step by step topology operation

two capacitors then integrate the charge for 2ns while the charge on first sampling is held. The overlap capacitor is again connected back to the first sampling capacitor completing the 6ns window and making the voltage ready for readout. The operation can be understood from the four steps shown in Fig. 14.

The effective integration window now looks like a stepwise approximation of a triangular window. From signal processing, it is known that the frequency response of a triangular window will be a $Sinc^2$ response in the frequency domain. Thus, the response of the window in Fig. 15 should also be close to a $Sinc^2$ type of response. This can be readily verified from MATLAB.

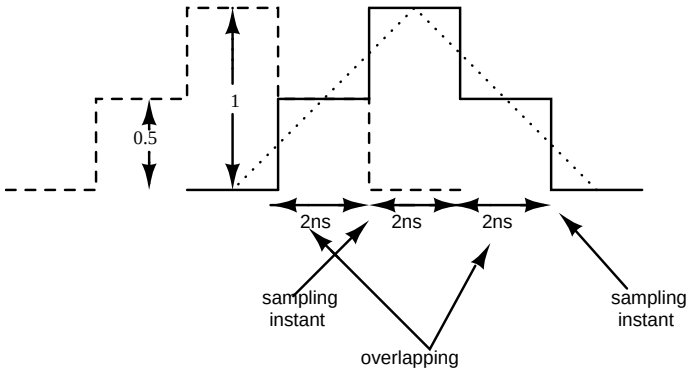


Fig. 15. Triangular approximation of the integration window for the overlap topology

In MATLAB, the frequency response of a window of certain length was compared to a triangular window of twice the length and a window of twice the length with shape as shown in Fig. 15. It can be seen from Fig. 16 that the response of the topology proposed closely follows the $Sinc^2$ response till the first null and then goes back to original $Sinc$ response. However, the sampling rate is $1/T_c$ and the spectrum after $1/T_c$ folds back, the nature of the response till the first null is of importance. Thus, it can be claimed that the topology achieves a $Sinc^2$ response.

In the explanation above, the downsampling operation achieved by the filter is not very clear. This will be explained in the next section by comparing it with conventional method of realizing the downsampling filter.

B. Comparison to Conventional Downsampling Topology

In charge sampling, the initial sampling rate for the sinc sampler is determined by the stopband attenuation required for antialiasing. However, some specifications might require much higher sampling rate which might not be practical. In [2], IIR filtering is performed along with a cascaded two pole RC filter, to meet the specifications.

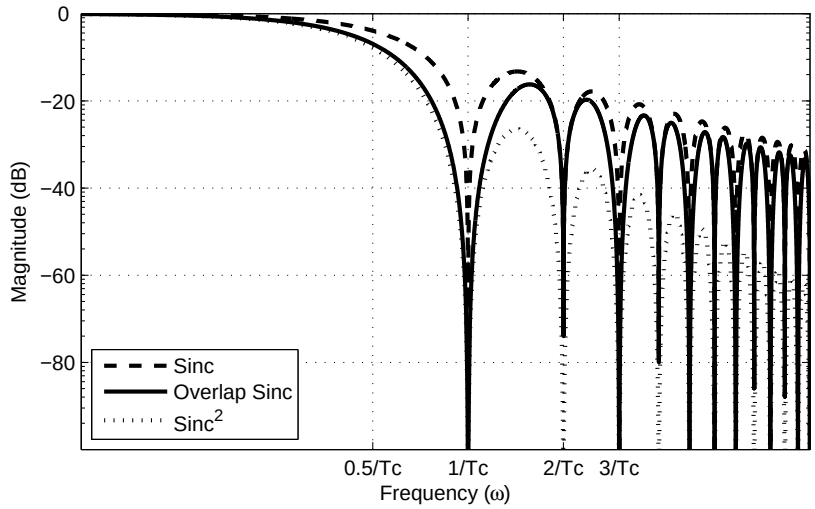
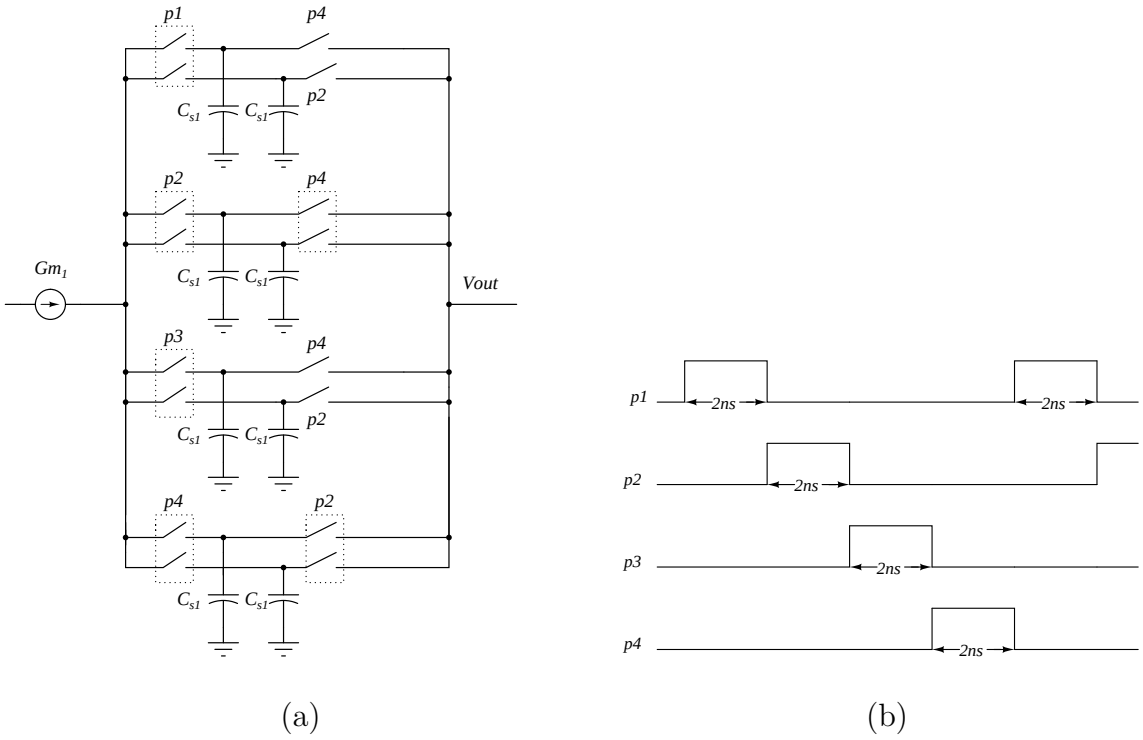


Fig. 16. MATLAB comparison of frequency response of the new topology with ideal $Sinc$ and $Sinc^2$ responses

The need for downsampling arises as the baseband ADC can be operated at a much lower rate than the initial sampling rate, which relaxes its specifications. After downsampling, the spectrum folds back again with the new sampling frequency equaling the sampling rate divided by the downsampling factor. The antialiasing specification now should be met at the multiples of this new sampling frequency. As explained in Chapter IV, the simple approach is to create a sinc type downsampling filter. This can be achieved by just summing up samples and reading them out at the same time as shown in Figure 1. However, only sinc downsampling might not be enough and better filtering might be necessary. $Sinc^2$ and $Sinc^3$ downsampling filters can be created by weighting the samples before summing them together [2],[4].

The proposed topology is compared with the conventional downsampling topology reported in [4]. To have a fair comparison, the final sampling rate of both the circuits is set to be 250MHz.

Fig. 17 shows the conventional topology of downsampling filter. The current



(a) (b)

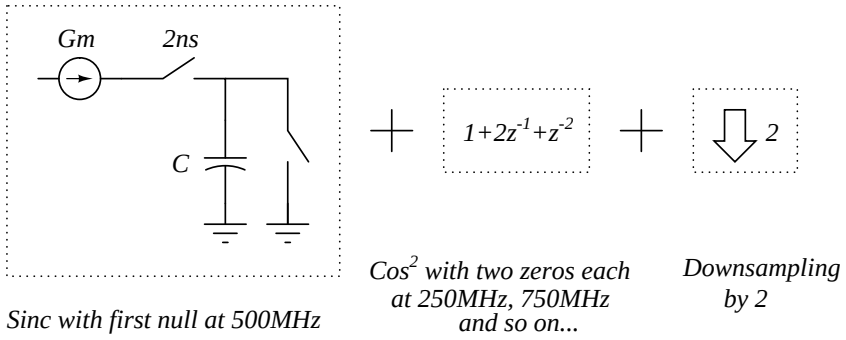
Fig. 17. (a)Conventional topology for $Sinc^2$ downsample by 2 filter (b) Clock scheme

is integrated for a time window of 2ns on each capacitor. In phase p1 and p3, it is integrated on single unit capacitor C, while during p2, it is integrated on two capacitors. In phase p4, these four capacitors are connected together for readout. As the singal is sampled already, the filter function can be written in Z-domain as,

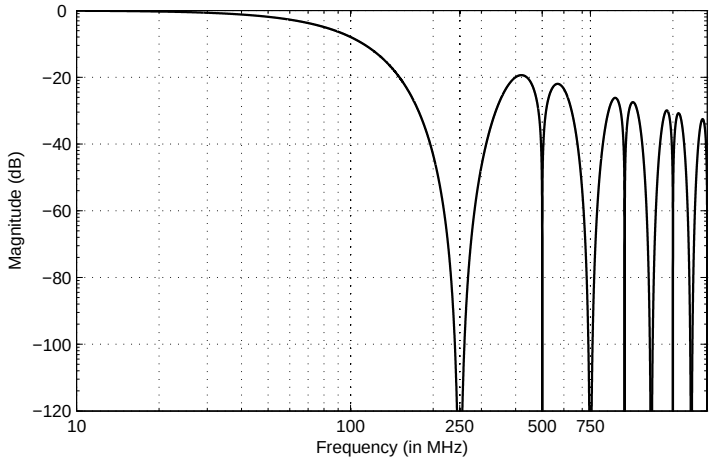
$$H(z) = \frac{1}{4}[1 + 2z^{-1} + z^{-2}]$$

The factor 1/4 comes from the fact that four unit capacitors are connected together during readout. The integration for 2ns will create a $Sinc$ filter with first null at 500MHz. The filter response for $H(z)$ is $Sinc^2$ and will have two nulls at half the sampling frequency, i.e. at 250MHz and will repeat after an interval of 500MHz.

The operation of the filter is clear from Fig. 18(a). The overall filter response will be a cascade of the two filter responses mentioned before and is plotted in Fig. 18(b).



(a)



(b)

Fig. 18. (a)Step by step explanation for conventional $Sinc^2$ downsample by 2 filter (b) Frequency response

The wider nulls at 250MHz, 750MHz and so on, are due to the $Sinc^2$ downsampling filter. It can be seen that this response is the same as that of the proposed topology, shown in Fig. 16.

However, the equivalence can be clearly seen in Fig. 19. Each black dot is the charge at the end of integration of 2ns. The valid outputs after they are sampled are the 1-2-1 filter outputs after decimation by 2. The overlap for 2ns between successive windows can be seen in the figure.

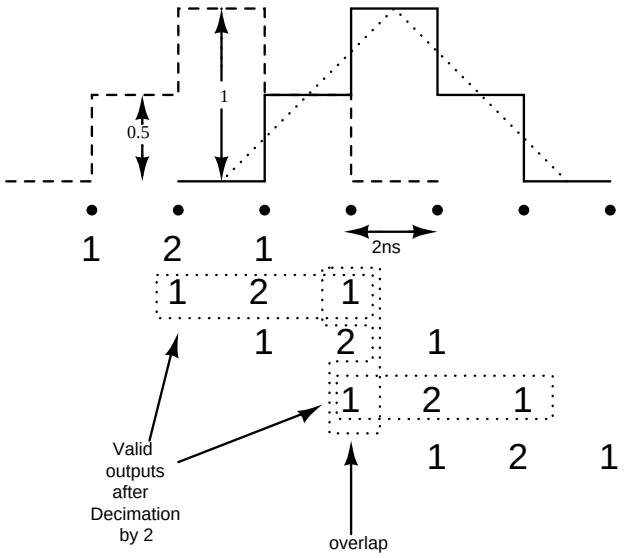
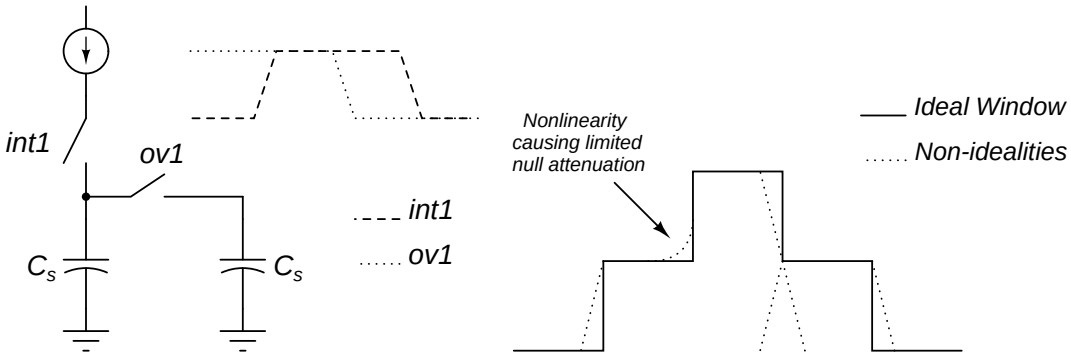


Fig. 19. $Sinc^2$ 1-2-1 filter explanation for proposed topology

C. Non-idealities in the Integration Window

The filter implementation in the conventional topology is a completely digital FIR filter where the previous samples are weighted and summed up. If the switch and sampling capacitor time constants are small enough, the non-linearities due to the switches do not affect the summing operation. Thus, the simulated performance in this case matches the MATLAB simulations. However, in proposed topology, when the overlap switch opens, the signal current will not instantaneously change to another value. The transition will be much smoother and will give rise to nonidealities in the shape of the window as explained in Fig. 20. In Fig. 20(a), the integration and overlapping clocks are shown. As explained in the operation before, the overlapping switch turns off while the integration still continues on one of the sampling capacitor.



(a) (b)

Fig. 20. (a)Non-ideal integration and overlap clocks (b)Window shape due to non-ideal switch transitions

This turning off is ideally assumed to be instantaneous but in reality will be smoother and will give rise to the integration window as shown in Fig. 20(b). This effect was

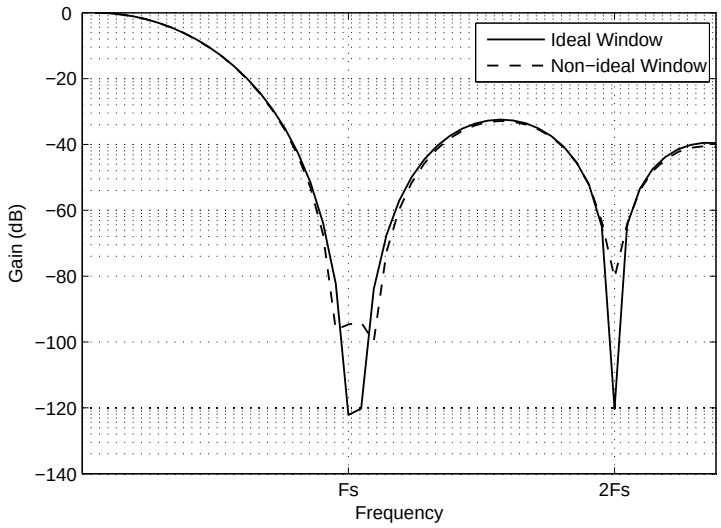
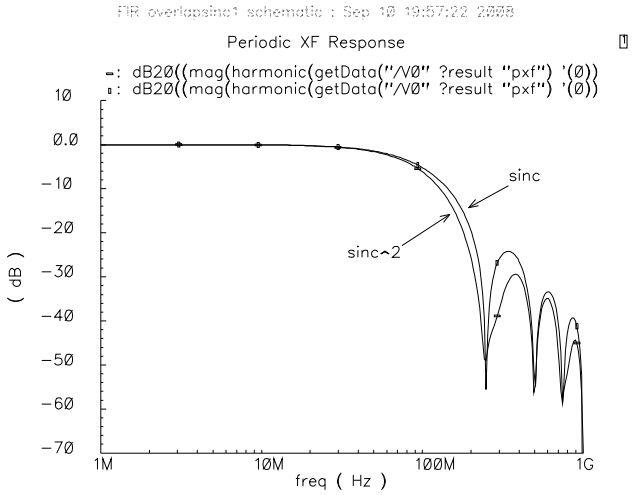


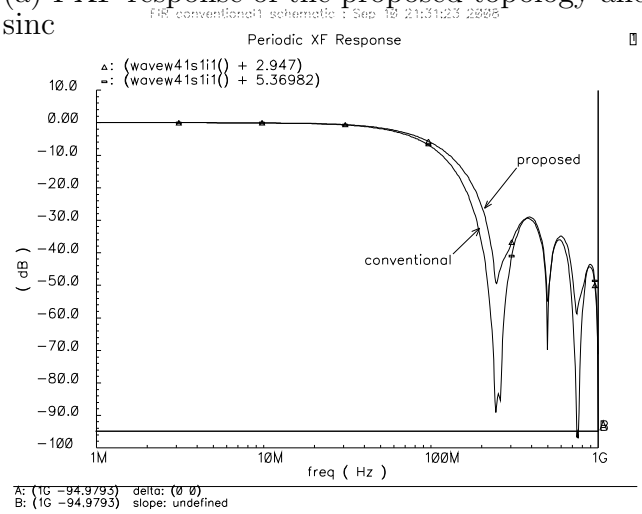
Fig. 21. MATLAB comparison of frequency response for ideal and non-ideal windows

simulated in MATLAB and the frequency response was plotted. From Fig. 21, its clear that the attenuation at the nulls is limited for non-ideal windows. Both topologies were simulated in Cadence and the frequency responses were plotted using

PXF simulations.The frequency response from the PXF simulations are compared to each other.



(a) PXF response of the proposed topology and sinc



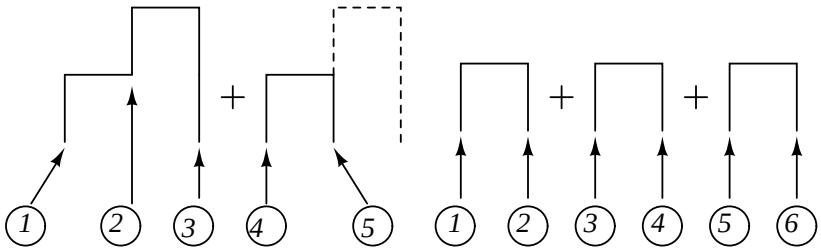
(b) PXF response for the proposed topology to conventional

Fig. 22. Frequency response comparison using PXF in Cadence

From Fig. 22, it can be seen that the proposed topology does better than a sinc downsampling filter. The null at the new sampling frequency is much wider. When compared to the conventional topology for $sinc^2$ implementation in Fig. 22(b), the proposed topology does not provide the same amount of attenuation at the first

null as explained before. However, the attenuation provided is still around 50dB. If this attenuation is sufficient, then the proposed topology can be implemented at the advantage of area saving as explained .

D. Effect of Clock Jitter



(a) (b)

Fig. 23. (a)Jitter sources in the integration window for proposed topology (b)Jitter sources in the integration window for conventional topology

The propose topology also does better in terms of jitter robustness. The integration windows for both the topologies along with sources of jitter are shown in Fig. 23. It can be seen that the integration window for the proposed filter has five jitter sources as compared to six in case of the conventional topology. The jitter in the middle, as shown in Fig. 23(a) by source 2, will not affect the window as the signal current continuously integrates on the capacitor.

The effect of jitter on the signal in case of these two topologies was verified in MATLAB. In case of the conventional topology, the input signal was windowed with a unit window having jitter at both its edges. After that 1-2-1 $sinc^2$ digital filtering was performed and then downsampled by a factor of two. The SNR of the output was plotted against varying clock jitter values. For the proposed topology however, it can be seen that the number of jitter sources are less. In this case, two unit windows

of the same length as before were taken and jitter was added at its edges. However, the jitter at the end of first and start of the second window will be the same.

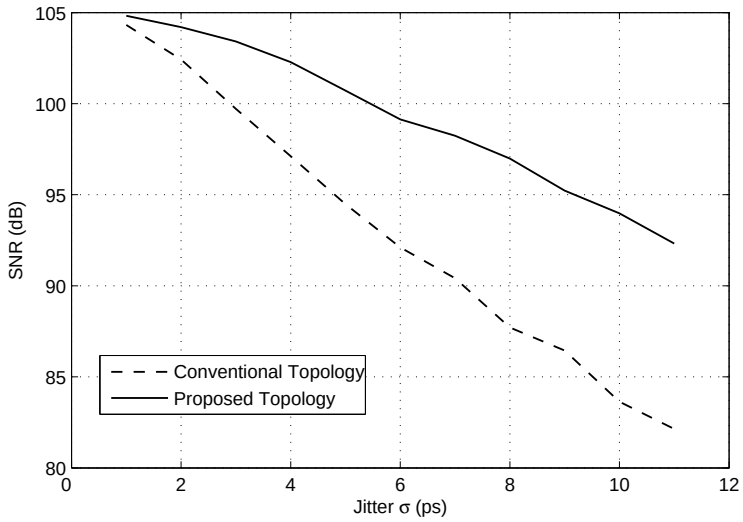


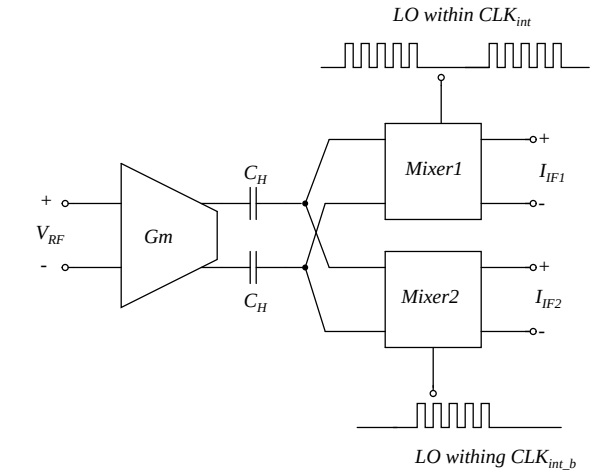
Fig. 24. SNR vs. Jitter σ for conventional and proposed filters

The signal was windowed using these two windows at a time to mimic the proposed topology. The same digital filtering and downsampling was performed as for the proposed topology and SNR of the signal was plotted. The plot in Fig. 24 confirms the jitter robustness of the proposed topology.

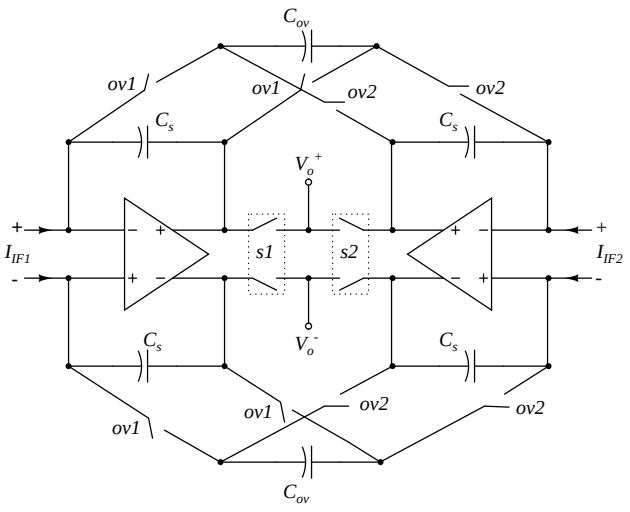
In conclusion, the proposed topology achieves the same $Sinc^2$ downsample by 2 operation as the conventional topology by using just three capacitors as compared to eight. The size of the unit sampling capacitor is determined by the noise requirements at the output. For the same peak to peak voltage range and the same SNR specification, it can be shown that the sampling capacitor for the proposed topology should be 1.5 times that for the conventional one. Even then there is a saving of about 44% in terms of area for the same specifications (See Appendix A).

E. Circuit Implementation

The actual implementation of the filter was fully differential and using an active integrator topology.To readout the voltage, the integration of the signal current must be interleaved.This is achieved by having two sets of mixer and active integrator circuits. The LO signals are combined with the integrating clocks.



(a)



(b)

Fig. 25. (a)Two mixers for interleaving (b)Fully differential active integrator topology of the proposed filter

As it can be seen in Fig. 25(a) only one mixer and integrator is operating during the clock phase CLK_{int} and other in CLK_{int_b}. The output of the integrators is interleaved using $s1$ and $s2$. The proposed overlap topology, implemented differentially with OTAs, is shown in Fig. 25(b). The clock scheme is shown Fig. 26. The discharge

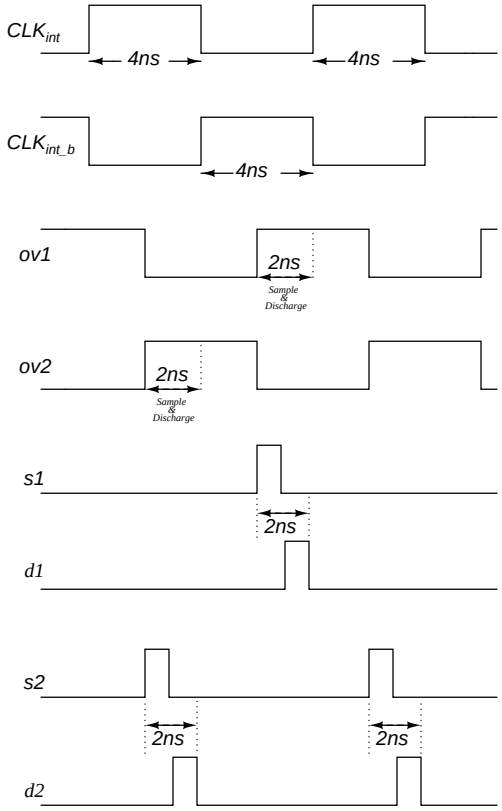


Fig. 26. Clock scheme for the differential active integrator topology

of the sampling capacitors is achieved during reset phases $d1$ and $d2$. During the reset phases, the input and output common mode voltage for OTA is set using switched capacitor common mode feedback [19]. As the voltages across the sampling and overlap capacitor are fixed to the common mode voltages during this time, these capacitors are discharged. Thus, common mode control and discharge are both achieved by this technique.

The CMFB circuit used in the is shown in Fig. 27. The output common mode

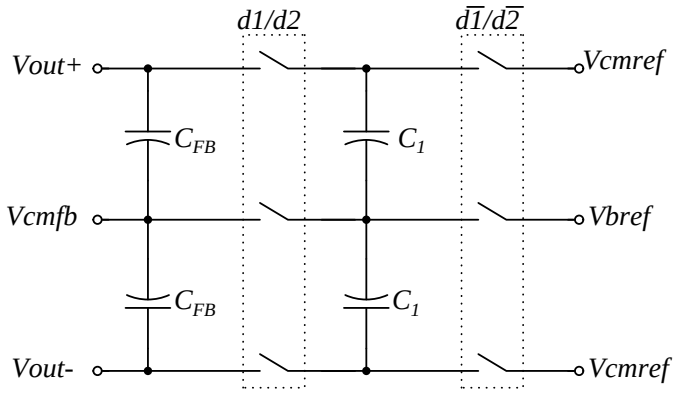


Fig. 27. Switched capacitor common mode feedback circuit used for the OTAs

voltage and the reference voltage is sampled during the discharge phase on the two capacitors. These capacitors get precharged to the required DC voltage. In the amplifying phase, there is a feedback loop as the two output voltages are averaged by the capacitors and connected to the reference voltage. In steady state, the feedback loop fixes the common mode and bias voltages to the reference voltages sampled during the reset phase.

F. OTA Design

The OTA gain and bandwidth are important parameters while designing the active integrator topology. The OTA DC gain provides the Miller effect to the sampling capacitor across it. This is the first pole of the sampler which should be much lower in comparison to other poles. For an ideal integrator, this pole should be at DC. The DC gain also comes in the expression for the overall gain of the sampler. [20]. Finite DC gain just means that the overall gain of the sampler is reduced by a factor. The DC gain also determines the signal swing at the input of the OTA. This swing needs to be minimized in order to linearize the mixer and the Gm stage before it. The second pole of the integrator is usually near the GBW of the OTA and needs to be maximized

in order to transfer the entire charge to the sampling capacitor. Otherwise, part of the charge is stored on the input capacitance of the OTA. Usually, an amount of settling time is provided so that this charge is transferred to the sampling capacitor. The charge residue on the input capacitance can be minimized by increasing the GBW and minimizing the capacitance itself. With all these constraints in mind, a telescopic

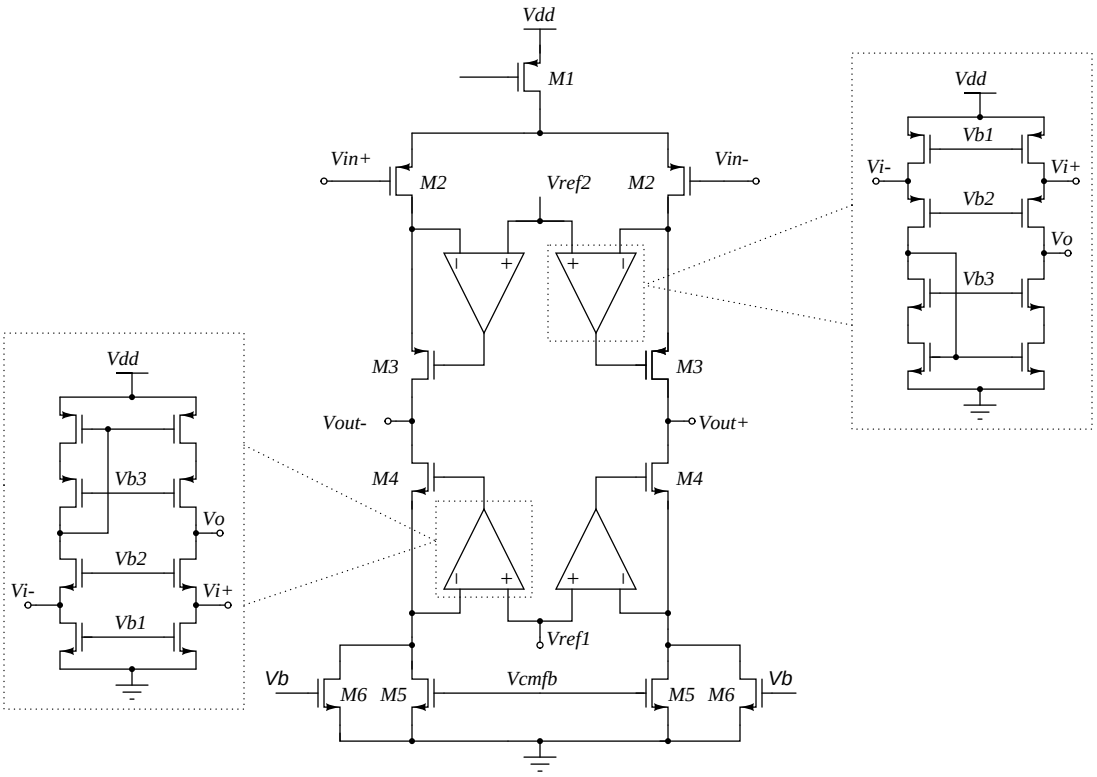


Fig. 28. Gain boosted OTA topology

gain boosted OTA topology with PMOS input was chosen. The telescopic topology is chosen over folded cascode as it offers less power consumption for the same GBW. The boosting amplifiers chosen were common gate cascode amplifiers with PMOS and NMOS input for the NMOS and PMOS sections of the main amplifier, respectively. The OTA schematic is shown in Fig. 28. The input stage is PMOS as the input common mode needs to be low to provide enough overdrive for the passive mixer

switches. Moreover, PMOS transistors have less flicker noise as compared to NMOS transistors, however suffer in terms of speed. The boosting amplifiers are chosen to be single ended as there is no need for another CMFB circuit. The reference voltages can be easily generated by replicating the branch of the main OTA with much lesser current.

As it will be seen in the next section, the flicker noise of the OTA is one of the major contributors to the overall noise of the sampling circuit and therefore needs to be minimized. The main contributors of the flicker noise will be the input pair (M2) and the current source (M5, M6) transistors in the main amplifier and the current source transistors in the boosting amplifiers. The only way to reduce the flicker noise is to use higher sizes for the transistors. For the main amplifier, size of the input pair cannot be increased too much as the input capacitance needs to be minimized. The length and width of M5 and M6 is increased proportionally till the noise is within required limits. This increases the loading at the $Vcmfb$ node. This is the reason why the bottom current source is split in two transistors. The size of M5 is adjusted till the loading and CMFB loop gain is is acceptable. For the boosting amplifiers, the current sources need to be sized up. However, the current sources performing the single-ended conversion cannot be sized up too much as the parasitic pole at that point can affect the stability of the amplifier.

The value of the sampling capacitor for the baseband filter was set to be 0.5pF. The switched capacitor CMFB circuit added another 0.2pF capacitor at the output of the OTA. Combined, the OTA was designed with a load capacitance of 0.7pF. The increase in length of the bottom current source increases the overall gain of the NMOS cascode stage compared to the PMOS cascode stage in the main amplifier. Therefore, the gain even after adding boosting stages is limited by the gain of the PMOS cascode stage. The gain boosting effect is thus limited. This penalty has to

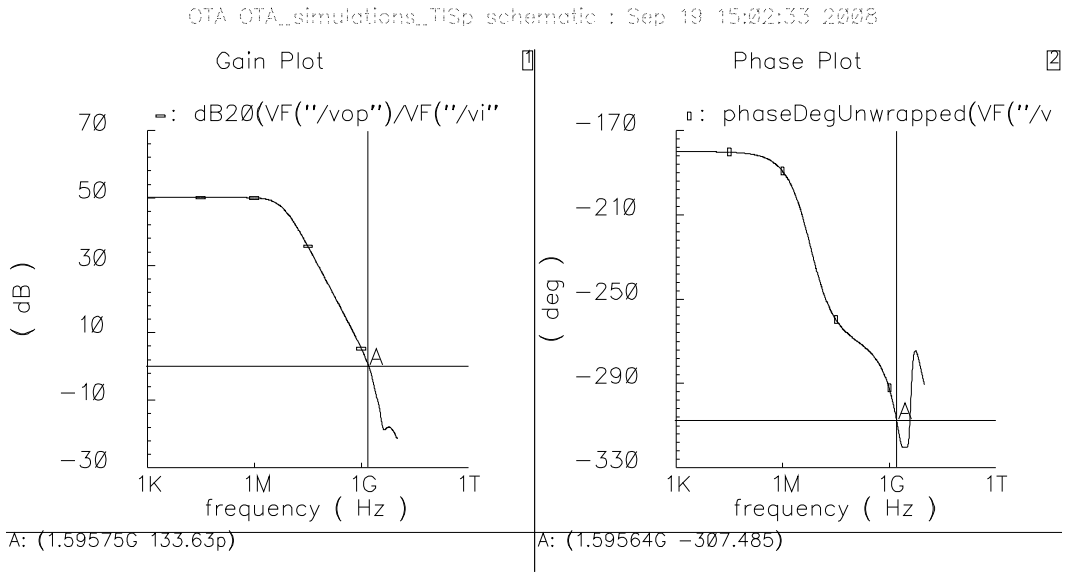


Fig. 29. Gain and phase plot of the OTA

be paid to contain the impact of flicker noise. The gain of the OTA was simulated to be 50dB and the GBW was 1.8GHz and is plotted in Fig. 29. The power of the OTA along with biasing was around 12mW.

The input referred noise plot is shown in Fig. 30. It can be seen that flicker noise extends up to hundreds of megahertz and is the dominant noise source. The maximum flicker noise density is at 1Hz is $7.925nV^2/Hz$ and the thermal noise density, when the curve almost becomes flat, is $32.5aV^2/Hz$. These numbers will be used in the later section to calculate the noise contribution of the OTA to the sampling circuit.

G. Overall Noise Calculations

For the baseband filter, the main noise contributors are the Gm stage and the OTA. The total integrated noise from each of this sources was be calculated and SNR of the signal was determined [20]. The output differential peak to peak range was set to be 0.8V. The effective transconductance of the Gm stage is 1mS and the sampling

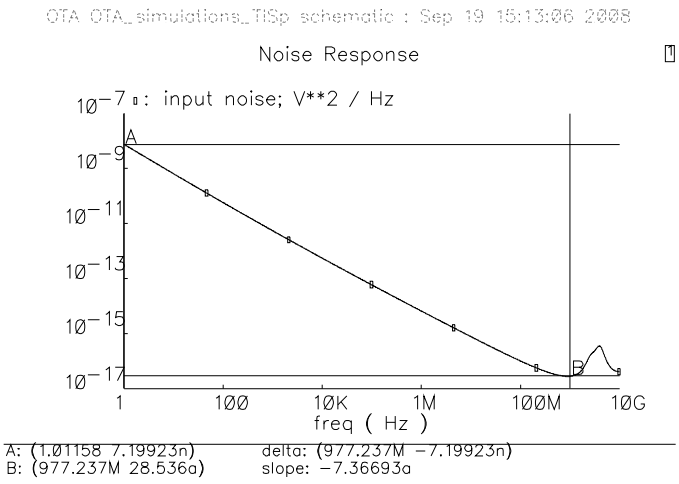


Fig. 30. Input referred noise for the OTA

capacitor (C_s) is 0.5pF. It is known that the total integrated noise of the sampling circuit due to the Gm stage is given by,

$$N = \frac{kT * 2Gm\Delta t}{C_s^2}$$

The noise with the window described for topology above comes out to be (See Appendix A),

$$N_{Gm} = 2 * \frac{3kT}{4}\left(\frac{Gm\Delta t}{C_s^2}\right)$$

The additional factor of two comes due to differential operation. The second source of noise is the noise sampled during the reset phase. The total integrated noise here will be,

$$N_{Reset} = \frac{kT}{C_s}$$

In this case, the capacitance is $2 * C_s$ as both overlap and sampling capacitor are discharged. This factor of 2 cancels with the factor of 2 in the numerator arising

due to differential operation. The flicker noise of the Gm stage is neglected as the coupling capacitors after the Gm stage and its output impedance, form a high pass filter, killing most of the Gm flicker noise.

The thermal and flicker noise of the OTA are significant contributors to the overall output noise. The total integrated output noise due to OTA thermal noise, during both integration and reset phase, is given by,

$$N_{OTA,Thermal} = 4 * \left(\frac{\omega_t}{4}\right) S_{in,OTA,Thermal}$$

Where, $S_{in,OTA,Thermal}$ is the input referred thermal noise density of the OTA, ω_t is the GBW of the OTA. The expression is multiplied by a factor of 4 as the noise is the same for reset phase and doubles for differential operation. The GBW and input thermal noise density for the OTA is found to be 1.8GHz and $32.5aV^2/Hz$ respectively in the previous section.

The calculation of the effect of flicker noise of the OTA is more involved. The total integrated output noise due to the input referred flicker noise of the OTA, $S_{in,OTA-Flicker}$ is given as,

$$N_{OTA,Flicker} = \int_0^\infty |H_{n,OTA}(f)|^2 * S_{in,OTA,Flicker}$$

Here, $H_{n,OTA}(f)$ is the discrete time transfer function for the input referred noise of the OTA (See Appendix B). The input referred flicker noise for the OTA can be characterized as,

$$S_{in,OTA,Thermal} = \frac{K_f}{f} V^2/Hz$$

K_f is the flicker noise coefficient and is the value at unity frequency in the input referred noise density plot. It was measured to be $7.925nV^2$ in the previous section.The integration goes to infinity at DC and hence is numerically evaluated using MATLAB

for the bandwidth of interest from 1MHz to 125MHz.

The noise contribution from each source, total noise, signal power and the SNR are given in Table II below.

Table II. Noise contributions

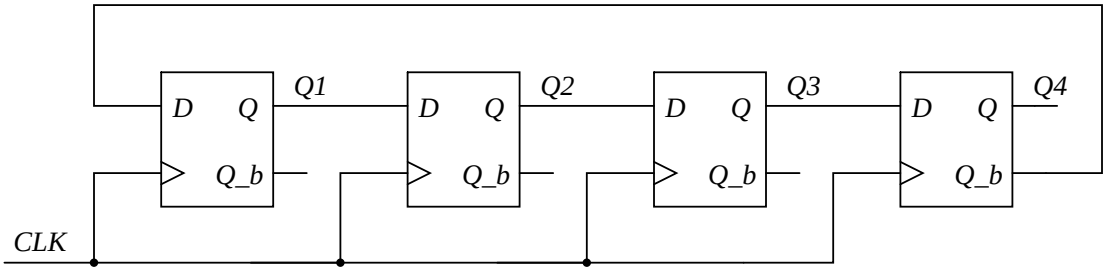
N_{Gm}	$4.8e-8$
N_{Reset}	$8e-9$
$N_{OTA,Thermal}$	$3.17e-7$
$N_{OTA,Flicker}$	$2.89e-7$
$TotalNoise$	$6.62e-7$
$SignalPower$	0.08
$SNRestimate(dB)$	50.82

CHAPTER VIII

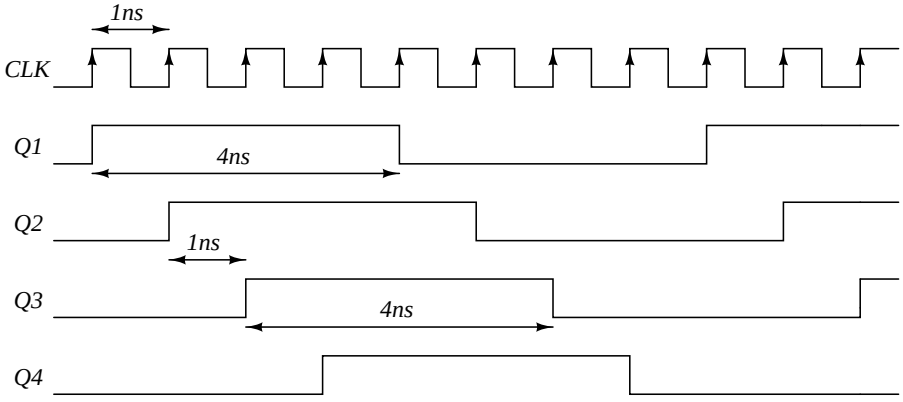
ADDITIONAL CIRCUITS

A. Clock Generation Circuit

The clocks needed for the baseband filter are generated using the Johnson Counter. The Johnson counter consists of four D flip-flops connected in series as shown in Fig.



(a) Johnson counter used for clock generation



(b) Output waveforms of the clock generator

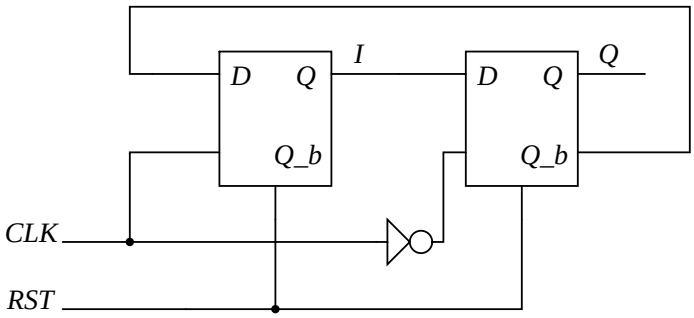
Fig. 31. On chip clock generation scheme

31(a). The inverted output of the last flip-flop is connected as an input to the first. The circuit essentially performs a divide by 8 operation and hence to get a 125MHz output clock, the reference clock is set at 1GHz. The delay between two successive outputs is equal to the clock period of the reference clock which is 1ns. From Fig.

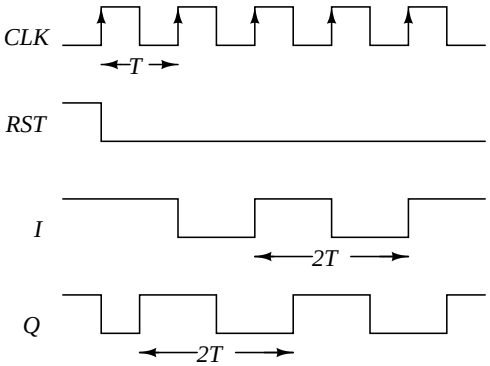
31(b), it can be seen that Q1 and Q3 with their inverted outputs can be used to as the integration and overlapping clocks. The discharge and sampling clocks can be created by adding delays and then performing logical operations.

B. I-Q Generation Circuit

The I-Q generation for the LO frequencies is achieved by using two latches connected in feedback. The input clock to these latches is double the required frequency. It



(a) Schematic for the I-Q generator



(b) Output waveforms of the I-Q generator

Fig. 32. On chip I-Q generation scheme

can be seen from Fig. 32, that the I-Q generator outputs indeed have twice the clock time period (T) and have a delay of T/2.

It can be observed in both the above mentioned topologies that as long as the period of the input clock is exact, the output clocks will have a duty cycle of 50%. The duty cycle of the clock should be sufficient for the operation of the circuit and not exactly 50%.

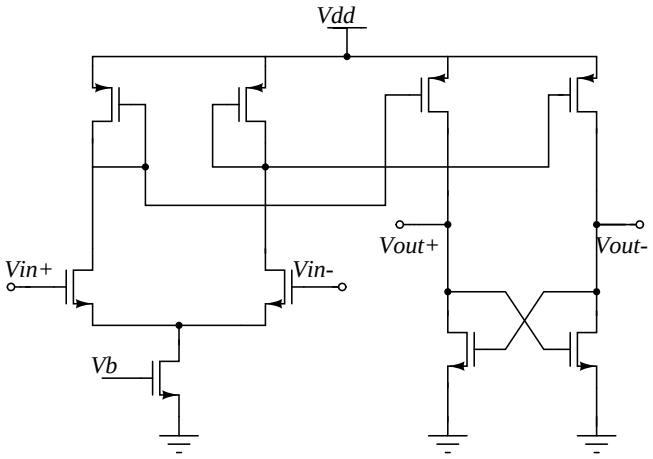


Fig. 33. Comparator schematic used for sin to square conversion

The input reference clock of 1GHz and the 2*LO frequencies will be generated off-chip as sinusoids. A balun will be used for each to convert them into differential signals and then fed to the chip. On chip, the differential sinusoids are converted to a square waveform using a comparator.The schematic used is given in the Fig. 33. This topology is fairly standard and consists of a preamplifier followed by a latch using cross-coupled NMOS. Only one of the output of the latch is needed for the digital circuit following it. The other output is connected to ta low pass filter and the voltage on the capacitor is read-out. This voltage is an estimate of the duty cycle of the clock e.g. a DC value of Vdd/2 corresponds to a duty cycle of 50%. The input DC level of the differential pair can be adjusted to change the duty cycle. This DC level comes through the balun used for differential conversion.

C. Output Buffer

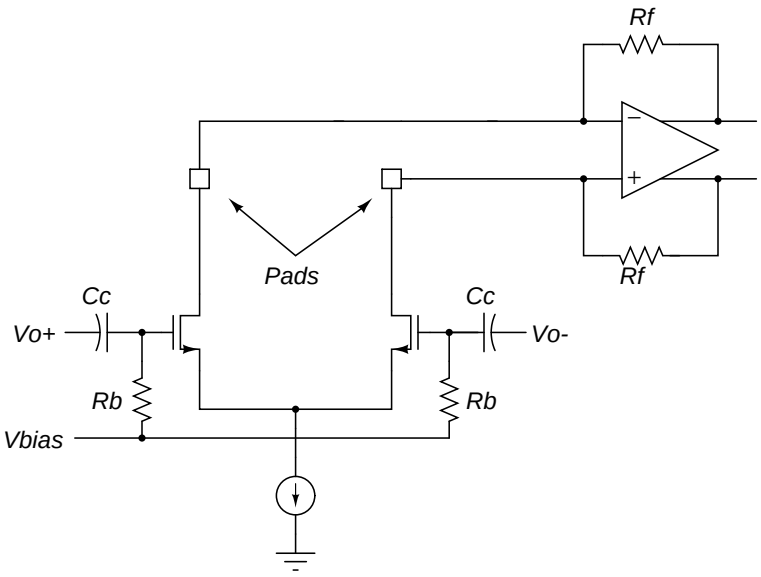


Fig. 34. Output buffer schematic

The schematic of the output buffer is shown in Fig. 34. The open drain differential buffer configuration is used for buffering the output to offchip. Transimpedance amplifiers are used offchip to convert signal back to voltage.

CHAPTER IX

LAYOUT

The layout of the system was done in 45nm technology. The layout for all transconductance stages was done together and placed in one corner of the chip to minimize the path of input RF voltage. The output of the Gm stages is current and hence it doesn't matter how long the path from the Gm stage to the mixers is. All of the signal current will still go to the baseband and will be integrated. Special layout layers were placed on the RF routing layers to avoid extra coupling capacitance arising due to dummy fill. The clock generator was placed in the center of the chip and the five

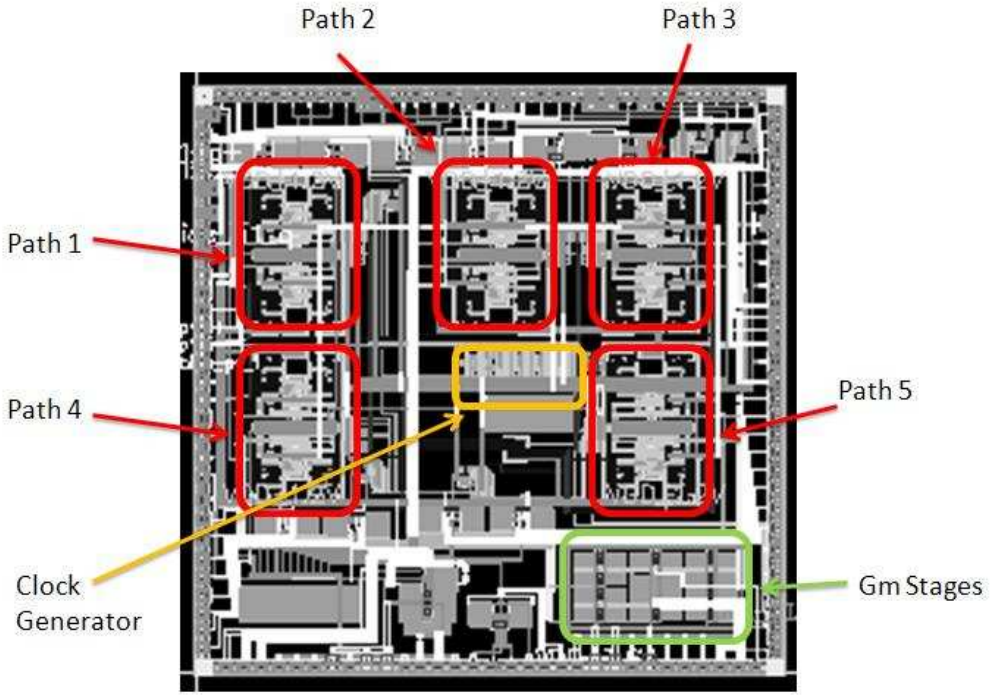


Fig. 35. Layout

paths were placed such that the distance to each path from the clock generator is the same. This ensured that all the paths start integration at the same instant. The

output buffers, I-Q generation circuits for each path were placed close to the path and the output pads. The bias current required for the baseband and comparators were locally replicated and routed over the chip as current. This takes care of the resistive drop due to lengthy routing. Good layout practices such as common centroid were used wherever good matching was required. Guard rings were placed around mixers, biasing circuits and individual paths for good isolation.

The overall area of the chip was about $6.6mm^2$. The layout snapshot can be seen in Fig. 35.

CHAPTER X

CONCLUSIONS

Transform Domain (TD) sampling was proposed as an alternative for the implementation of Software Defined Radio (SDR). Frequency Domain (FD) Sampling, a special case of TD sampling was actually implemented. Charge sampling was used as it offered several advantages over conventional voltage sampling techniques. The overall system specifications and architecture was proposed. A novel charge sampling filter topology with a downsampling factor of two was proposed and the operation was explained. This topology was compared to a conventional $sinc^2$ downsampling filter and the operation of both was shown to be equivalent. The sources of non-idealities in the proposed topology were explored and their effect on the filter response was simulated and confirmed with Cadence simulation. The null attenuation for proposed filter was about 50dB which was less as compared to the conventional filter however the overall roll-off was -20dB/dec. The proposed topology was shown to have less jitter sources and hence was more robust to jitter. The noise analysis for both topologies was done in detail and it was shown that for the same specifications, the proposed topology can be implemented with 44% less area and 25% less power in the transconductance stage. The layout for the entire system was done in 45nm technology and chip was sent for fabrication. The testing of the chip still remains to be performed.

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APPENDIX A

SAMPLING CAPACITOR CALCULATION FOR PROPOSED AND CONVENTIONAL TOPOLOGY

It is known that the total integrated noise of the sampling circuit is given by,

$$N = \frac{kT * 2Gm\Delta t}{C_s^2}$$

Whereas, the gain of the sampling circuit is given as,

$$G = \frac{Gm\Delta t}{C_s}$$

Now lets assume that Gm_{conv} and $C_{s,conv}$ are the transconductance and sampling capacitors for the conventional topology and Gm_{prop} and $C_{s,prop}$ for the proposed topology respectively.

To compare the two, it is assumed that both have same input voltages to their Gm stages and have the same SNR requirement. To get the same SNR, the signal gain and overall noise of both the samplers should be the same. The SNR expression can also be compared to each other and will yield the same result. The signal peak to peak voltage is limited by supply/circuit, then only way to reduce noise is to increase capacitance. The Gm needs to be increased proportionally to keep the gain and hence the output peak to peak range constant. From the noise expression, it can be seen that, integrated output noise is inversely proportional to square of the sampling capacitor and proportional to Gm. Therefore, the total noise reduces and overall SNR increases.

For conventional topology, three windows of 2ns are added together with a scaling factor of 1/4 due to charge sharing. If the topology is carefully inspected, it can be

seen that only half of the current is integrated on each sampling capacitor. This means that the effective transconductance will be half of the actual value i.e. $Gm_{conv}/2$.

$$\begin{aligned} G_{conv} &= \frac{1}{4}\left(\frac{Gm_{conv}\Delta t}{2C_{s,conv}} + \frac{2Gm_{conv}\Delta t}{2C_{s,conv}} + \frac{Gm_{conv}\Delta t}{2C_{s,conv}}\right) \\ &= \frac{1}{2}\left(\frac{Gm_{conv}\Delta t}{C_{s,conv}}\right) \end{aligned} \tag{A.1}$$

In case of proposed topology,the signal integrates on $2C_{s,prop}$ for first 2ns, then integrates on $C_{s,prop}$ for next 2ns and finally again integrates on $2C_{s,prop}$ for last 2ns. A factor of 1/2 is introduced during the readout operation. (See Chapter VII for explanation.) Therefore,

$$\begin{aligned} G_{prop} &= \frac{1}{2}\left(\frac{Gm_{prop}\Delta t}{2C_{s,prop}} + \frac{Gm_{prop}\Delta t}{C_{s,prop}} + \frac{Gm_{prop}\Delta t}{2C_{s,prop}}\right) \\ &= \frac{Gm_{prop}\Delta t}{C_{s,prop}} \end{aligned} \tag{A.2}$$

Equating the two yields,

$$\frac{Gm_{conv}}{C_{s,conv}} = 2\left(\frac{Gm_{prop}}{C_{s,prop}}\right) \tag{A.3}$$

Similarly the noise for each topology can be calculated as,

$$\begin{aligned} N_{conv} &= \frac{2kT}{16}\left(\frac{Gm_{conv}\Delta t}{2C_{s,conv}^2} + \frac{2Gm_{conv}\Delta t}{2C_{s,conv}^2} + \frac{Gm_{conv}\Delta t}{2C_{s,conv}^2}\right) \\ &= \frac{kT}{4}\left(\frac{Gm_{conv}\Delta t}{C_{s,conv}^2}\right) \end{aligned} \tag{A.4}$$

The factor of 16 here is the square of the gain 1/4.

$$\begin{aligned} N_{prop} &= \frac{2kT}{4}\left(\frac{Gm_{prop}\Delta t}{4C_{s,prop}^2} + \frac{Gm_{prop}\Delta t}{C_{s,prop}^2} + \frac{Gm_{prop}\Delta t}{4C_{s,prop}^2}\right) \\ &= \frac{3kT}{4}\left(\frac{Gm_{prop}\Delta t}{C_{s,prop}^2}\right) \end{aligned} \tag{A.5}$$

The factor of 4 here is the square of the gain 1/2. Equating the two,

$$\frac{Gm_{conv}}{C_{s,conv}^2} = 3\left(\frac{Gm_{prop}}{C_{s,prop}^2}\right) \tag{A.6}$$

Substituting A.3 into A.6,

$$C_{s,prop} = 1.5 * C_{s,conv} \tag{A.7}$$

Which gives,

$$Gm_{prop} = 0.75 * Gm_{conv} \tag{A.8}$$

Hence, the proposed topology requires lesser Gm and higher sampling capacitor as compared to the conventional topology. However, 8 capacitors are needed for the conventional topology as compared to 3 for the proposed. This translates to an area saving of about 44%. Assuming same Gm/I_D ratio in the transconductance design, the lower Gm_{conv} translates to 25% power saving.

In this calculation, it was assumed that the noise due to the Gm stage was the dominant noise compared to other noise sources, which is generally true.

APPENDIX B

EFFECT OF OTA FLICKER NOISE ON THE BASEBAND FILTER

The $H_{n,OTA}(f)$ is the transfer function for the OTA input referred noise and is given by [20],

$$H_{n,OTA}(f) = \left(\frac{A_0(C_s + C_{in})}{C_{in} + (A_0 + 1)C_s} . \frac{\sqrt{1 - 2cos(\omega T_i)e^{-T_i/\tau_p 2} + e^{-2T_i/\tau_p 2}}}{\sqrt{\omega^2 \tau_{p2}^2 + 1}} \right)$$

Here,

$$\begin{aligned} A_0 &= \text{DC gain of the OTA} \\ T_i &= \text{Total integration time} \\ C_s &= \text{Sampling Capacitor} \\ C_{in} &= \text{Input parasitic capacitance of the OTA} \\ \tau_{p2} &= 1/\omega_t \\ \omega_t &= \text{GBW of the OTA} \end{aligned}$$

The total integrated noise at the output is given by,

$$N_{OTA,Flicker} = \int_0^\infty |H_{n,OTA}(f)|^2 * S_{in,OTA,Flicker}$$

Here, $H_{n,OTA}(f)$ is the discrete time transfer function for the input referred noise of the OTA The input referred flicker noise for the OTA can be characterized as,

$$S_{in,OTA,Thermal} = \frac{K_f}{f} V^2/Hz$$

K_f is the flicker noise coefficient and is the value at unity frequency in the input referred noise density plot. It was measured to be $7.925nV^2$. The integration goes to

infinity at DC and hence is numerically evaluated using MATLAB for the bandwidth of interest from 1MHz to 125MHz.

VITA

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