DEVELOPMENT OF RF CMOS RECEIVER FRONT-ENDS FOR ULTRA-WIDEBAND COMMUNICATIONS

A Dissertation

by

XIN GUAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2008

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Cam Nguyen
Committee Members,	Jose Silva-Martinez
	Laszlo Kish
	Mark Everett
Head of Department,	Costas N. Georghiades

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ABSTRACT

Development of RF CMOS Receiver Front-Ends for Ultra-Wideband Communications.

(May 2008)

Xin Guan, B.Eng., Tsinghua University, Beijing, China;

M.S., Tsinghua University, Beijing, China

Chair of Advisory Committee: Dr. Cam Nguyen

Ultra-Wideband (UWB) technology has become one of the hottest topics in wireless communications, for it provides cost-effective, power-efficient, high bandwidth solution for relaying data in the immediate area (up to 10 meters). This work demonstrates two different solutions for the RF front-end designs in the UWB receivers, one is distributed topology, and the other is based on traditional lumped element topology.

The distributed amplifier is one of the attractive candidates for UWB Low Noise Amplifier (LNA). The design, analysis and operation of the distributed amplifiers will be presented. A distributed amplifier is designed with Coplanar Waveguide (CPW) transmission lines in 0.25-μm CMOS process for time domain UWB applications. New design techniques and new topologies are developed to enhance the power-efficiency and reduce the chip area. A compact and high performance distributed amplifier with Patterned Grounded Shield (PGS) inductors is developed in 0.25-μm CMOS process. The amplifier has a measurement result of 7.2dB gain, 4.2-6dB noise figure, and less

than -10dB return loss through 0-11GHz. A new distributed amplifier implementing cascade common source gain cells is presented in 0.18-μm CMOS. The new amplifier demonstrates a high gain of 16dB at a power consumption of 100mW, and a gain of 10dB at a low power consumption of 19mW.

A UWB LNA utilizing resistive shunt feedback technique is reported in 0.18-μm CMOS process. The measurement results of the UWB LNA demonstrate a maximum gain of 10.5dB and a noise figure of 3.3-4.5dB from 3-9.5GHz, while only consuming 9mW power.

Based on the distributed amplifier and resistive shunt-feedback amplifier designs, two UWB RF front-ends are developed. One is a distributed LNA-Mixer. Unlike the conventional distributed mixer, which can only deliver low gain and high noise figure, the proposed distributed LNA-Mixer demonstrates 12-14dB gain ,4-5dB noise figure and higher than 10dB return loss at RF and LO ports over 2-16GHz. To overcome the power consumption and chip area problems encountered in distributed circuits, another UWB RF front-end is also designed with lumped elements. This front-end, employing resistive shunt-feedback technique into its LNA design, can achieve a gain of 12dB and noise figure of 8-10dB through 3-10GHz, the return loss of less than -10dB from 3-10GHz at RF port, and less than -7dB at LO port, while only consuming 25mA current from 1.8V voltage supply.

DEDICATION

To My Dear Grandma, and my parents…

ACKNOWLEDGEMENTS

This is a long journey, lonely and helpless, sometimes. When it finally came to an end, here, I hope that I could express my appreciation to all those who have helped my professional as well as personal life in the past few years.

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TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

FIGURE Page

FIGURE Page

FIGURE Page

FIGURE Page

LIST OF TABLES

1. INTRODUCTION

Driven by the largely explosive growth in wireless communications, the advancement of sophistication in wireless circuit design has progressed at an unprecedented speed in recent years. Miniature and low-cost portable devices, such as cellular phones, personal digital assistants (PDA), mp3 players, have invaded the market and people's everyday life. Technology improvements and market growth are forcing for higher quality of service in transmission and reception of information at fast data rates and lower cost.

1.1 Motivation

The rapid development in the wireless technology introduces new design challenges, such as low power consumption, high data rate, low cost, small dimension and multi-standard programmability.

According to Shannon's theorem, the channel capacity (C) characterized by the highest data rate of reliable transmission in bits per second (bps), is given by [1]

$$C = B \times \log_2(1 + S/N) \tag{1.1}$$

which indicates two fundamental factors setting the upper bound on the information transmission speed: the channel bandwidth B and the link signal to noise ratio (SNR) S/N. While the improvement of S/N is subject to various natural and implementation limitations, increasing B looks like a direct way to enhance achievable data-rate. This inspired the emergence of ultra-wideband (UWB) technology.

This dissertation follows the style of *IEEE Transactions on Microwave Theory and Techniques*.

Being used in military applications, such as radar and covert communication, for several decades, UWB is "sparked" only recently by an FCC Notice of Inquiry in 1998 [2] and a subsequent Report and Order in February 2002 [3], when the FCC agreed to allocate 7500 MHz of spectrum for unlicensed use of ultra-wideband (UWB) devices for communication applications in the 3.1-10.6-GHz frequency band. To avoid interference with other wireless services operating under different rules, the power spectral density (PSD) measured in 1-MHz bandwidth must not exceed -41.25dBm. Consequently, UWB can provide dramatic channel capacity at short range.

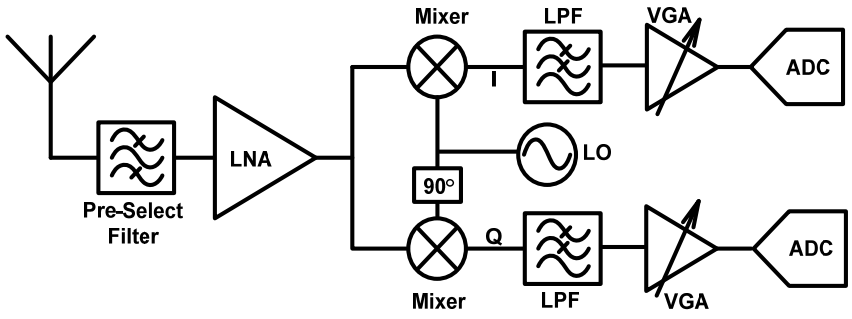


Fig. 1.1 Block diagram of a UWB RF receiver front-end

A UWB front-end for Multi Band-Orthogonal Frequency-Division Multiplexing (MB-OFDM) receiver, diagrammed in fig.1.1, will feature a pre-select band pass filter after the antenna, followed by a low noise amplifier (LNA) and a quadrature mixer, which brings the RF signal directly into the base-band. The analog-digital converter

(ADC) is after the low pass filter (LPF) and variable gain amplifier (VGA), to allow for digital signal processing in the back-end.

This dissertation will present design, analysis and performance of the distributed amplifier in CMOS process. The same technique can be used also in distributed mixer designs. A UWB LNA utilizing resistive shunt feedback technique will also be reported. Based on the distributed amplifier and resistive shunt feedback amplifier designs, two UWB RF front-ends are developed. One is a distributed LNA-Mixer, the other UWB RF front-end, employing resistive shunt-feedback technique into its LNA design, is also designed and presented CMOS process. Various innovations developed along the way will be revealed in detail together with measurement verifications.

1.2 Organization

In this dissertation, some fundamental concept and design considerations of low noise amplifiers will be discussed in section 2. Section 3 focus on distributed amplifier designs. The basic principle of distributed amplification is introduced at first. Then three different CMOS distributed amplifiers are presented. A resistive shunt feedback UWB LNA is presented in section 4. In section 5, two CMOS UWB front-ends are developed. These two front-ends utilized the distributed low noise amplifier and resistive shunt feedback amplifier respectively. The conclusion will be drawn in section 6.

2. FUNDAMENTALS OF LOW NOISE AMPLIFIERS

The objective of this section is to provide a basic theory of noise mechanism and LNA design for discussions in the following sections, and a review of the existing theory and technologies.

2.1 Noise Mechanisms

From the time when the world's first radio system was invented by Guglielmo Marconies, people are battling with electronic noise that blurs the signal and causes erroneous or even failed information transmission. In the following part, we will briefly go over the different kinds of noise mechanisms in the electronic circuits.

2.1.1 Types of Electronic Noise

Noise in electronic systems is generated from the random fluctuation in current flows. There are typically three types of noise sources: thermal noise, short noise and flicker noise.

The thermal noise originates from the random thermal motion of the carrier charges. Thus, the spectrum of thermal noise is proportional to the absolute temperature of the component. The most common example of thermal noise is resistor noise. Even without any current, the AC voltage across a resistor could be observed as a random voltage fluctuation with zero mean and Gaussian amplitude distribution. The thermal

noise of the a resistor R can be modeled by a voltage source series connecting with a noiseless resistor, with the one-sided spectral density

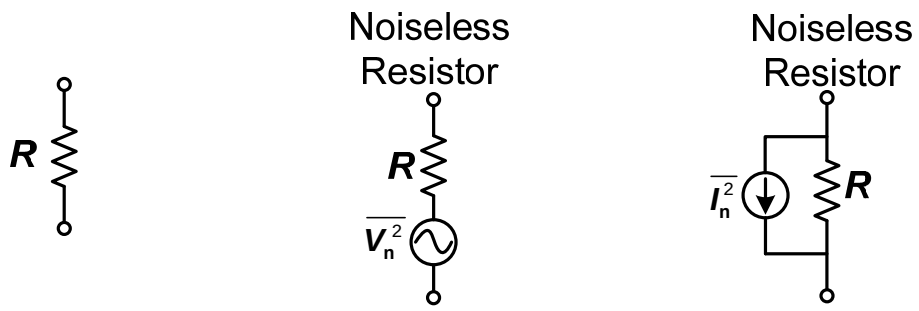
$$S_v(f) = 4kTR, \quad f \geq 0 \tag{2.1}$$

where R is the resistance, T is the absolute temperature in Kelvin and $k = 1.38 \times 10^{-23}$ *Joules / Kelvin* is the Bolztzmann constant. Since the unit of $S_v(f)$ is V^2/Hz, we could write

$$\overline{V_n^2} = 4kTR \tag{2.2}$$

where the $\overline{V_n^2}$ indicates the average noise voltage square. Equivalently, as shown in figure 2.1, the noisy resistor can be presented by a noiseless resistor with a parallel current noise generator, with

$$\overline{I_n^2} = 4kT / R \tag{2.3}$$



(a) (b) (c)

Fig. 2.1 Noise model of a resistor: (a) A noisy resistor (b) Representation of resistor thermal noise by a voltage source (c) Representation of resistor thermal noise by a current source

The maximum noise power that a resistor can pass to its load is delivered when the load impedance is matched to the source, which is also called available noise power, is given

$$P_{av} = kBT \tag{2.4}$$

where B is the noise bandwidth. It should be noticed that the available noise power is independent of the resistance value. In the receiver system whose input impedance is always matched to that of the load to obtain the maximum power delivery, but this also results in the maximum noise power.

As we see from (2.2) and (2.3), the noise spectrum density is constant across the frequency, which also implies that the noise power in the interval between 1MHz and 2MHz is the same as between 1GHz and 1.001GHz. Because of this constancy, the thermal noise is often described as “white noise”, by analog with white light. However, the resistors thermal noise has a finite bandwidth, which is on the order of 1 Terahertz [4], indicating the total noise power is not infinite. This indicates that in the frequency range of our interests, which is typically much lower than 1 Teraherz, it can be treated as purely white.

Another noise mechanism is known as shot noise. Shot noise arises from random variations of a DC current, and is especially associated with current carried by active devices. There are two conditions for the short noise to occur. First, there must be a DC current flowing second there must also be a potential barrier over which the charge carriers hop, for example, p-n juctions. Its power spectrum can be written as [5]

$$\overline{i_n^2} = 2qI_{DC}\Delta f \tag{2.5}$$

where $\overline{i_n}$ is the rms noise current, q is the electronic charge (1.6×10^{-19} Coulomb), I_{dc} is the DC current and Δf is the bandwidth. One should notice that, like the thermal noise, ideally, shot noise is white, but is temperature independent.

Flicker noise, also known as $1/f$ noise, happens from a number of different complex mechanisms. But its main cause is believed to be some random trap and release of the carriers at the interface of different materials in semiconductors. Different from thermal noise and shot noise, the average power of flicker noise can't be predicted easily and can be different from different devices. The flicker noise in a CMOS transistor can be modeled as a voltage source in series with the gate and roughly given by

$$\overline{V_n^2} = \frac{K}{C_{ox}WL}\cdot\frac{1}{f} \tag{2.6}$$

where K is a process-dependent constant on the order of 10^{-25} Volt · Farad, C_{ox} is the gate-oxide capacitance per unit area, W and L are the width and length of the device.

A very important parameter for the flicker noise is the "corner frequency", which is the intersection frequency point, below which the measure noise is mostly dominated by flicker noise. The corner frequency, f_c, generally depends on device dimensions and bias current. Nonetheless, for a given CMOS technology with certain channel length (L), it is relatively constant; f_c is within 500 kHz-1 MHz [6] for submicron transistors. That is why flicker noise is usually not a big concern in RF designs, when operation frequency is much higher than the corner frequency, f_c. Although, flicker noise still can be a dominant part in RF frequencies because of the frequency translation, it is normally not considered in low noise amplifier designs.

2.1.2 Noise in CMOS Transistors

In a CMOS transistor, there are several sources to generate noise. For simplicity, the noise sources could be divided into two main parts: drain noise and gate noise. The drain noise, characterized by an inherent noise source at the drain of the transistor, consists of channel noise and flicker noise. Since in the RF frequencies, channel noise dominants drain noise. Flicker noise will not be included in the later analysis.

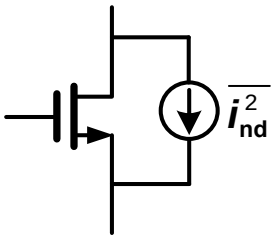


Fig. 2.2 Channel noise model of a NMOS transistor

As CMOS transistors are basically voltage-controlled resistors, they exhibit thermal noise. This noise is called channel noise, which could be modeled by a parallel current source connected between drain and source terminals, as shown in fig. 2.2, with a spectrum density

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \cdot \Delta f \tag{2.7}$$

where γ is the coefficient, which is around 2/3 for long-channel transistors, and as big as 2.5 for short-channel transistors [7]. g_{d0} is the channel conductance when V_{ds}=0 V. From the current equation of a NMOS transistor in triode region,

$$I_d = \mu_n C_{ox} \frac{W}{L}\left((V_{gs} - V_T)V_{ds} - \frac{V_{ds}^2}{2}\right) \tag{2.8}$$

Where I_d is the drain current of the NMOS transistor, μ_n is the average electron mobility in the channel, V_{gs} is gate-source voltage, V_T is the threshold voltage, V_{ds} is the drain to source voltage g_{d0} can be found from

$$g_{d0} = \left.\frac{dI_d}{dV_{ds}}\right|_{Vds=0} = \mu_n C_{ox} \frac{W}{L}\left(V_{gs} - V_T\right) \tag{2.9}$$

(2.9) reveals that g_{d0} has the same expression as g_m, however this is only valid for long channel devices. For short channel device [7]

$$g_{d0} = \frac{g_m}{\alpha} \tag{2.10}$$

where α is used to characterize the discrepancy between g_m and g_{d0} in short channel devices. The same expressions for NMOS also apply to the PMOS devices.

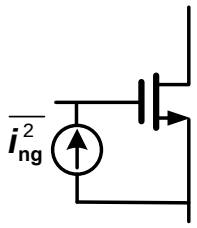


Fig. 2.3 Gate noise model of a NMOS transistor

The gate noise is caused mainly by two parts, as shown in fig.2.3. The first part of the noise is generated by the parasitic resistance at the gate of the CMOS transistors, including the resistance of the metal routing and vias connected to the polysilicon gate. Although this part can usually play a critical role in an amplifier's noise figure, it can be minimized with proper layout, such as devices with multiple figures for the same width. The second part of the noise is induced by the channel noise. Its noise spectrum density can be written as

$$\overline{i_{ng}^2} = 4kT\delta g_g \cdot \Delta f \tag{2.11}$$

where δ is the gate noise coefficient, and is about twice the value of γ for long channel devices and typically 1-2 for short channel devices, the parameter g_g is [8]

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{2.12}$$

Since both the drain noise and gate noise are originated from the thermal agitation of channel charge, they are correlated. The correlation coefficient is defined by

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} \tag{2.13}$$

For long channel devices, $c=j0.395$. The pure imaginary value implies that the correlation is due to the capacitive coupling from channel to gate.

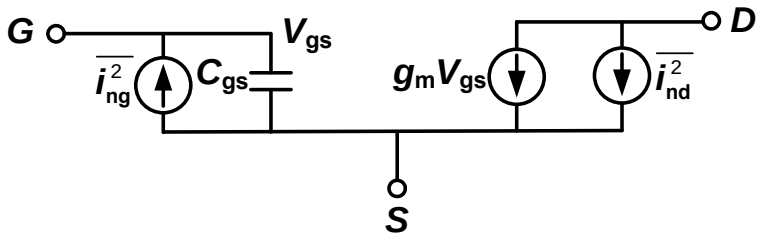


Fig. 2.4 Small signal model for noise analysis of a NMOS transistor

Fig 2.4 shows a small signal model for noise analysis of a NMOS transistor. Cgs is the gate-source capacitor. The gate noise source $\overline{i_{ng}^2}$ and channel noise source $\overline{i_{nd}^2}$ are located at gate and drain of the NMOS transistor. For simplicity, this model does not include C_{gd}, which is gate-drain capacitance, and r_{ds}, which is drain-source resistance. In the later analysis, the noise figure derivation will be based mainly on this model. All the models and expressions for the noise analysis of NMOS are the same for PMOS devices .

2.2 Noise Figure

The noise performance of the receiver is characterized by its noise factor (F), which is defined as the ratio of input signal to noise ratio, to the output signal to noise ratio.

$$F = \frac{SNR_{IN}}{SNR_{OUT}} \tag{2.14}$$

Noise figure (NF) is just the logarithm form of noise factor (F), its unit is dB

$$NF = 10\log F \tag{2.15}$$

In order to calculate noise figure of a circuit, SNR_{in} and SNR_{out} could both be calculated as

$$SNR_{in} = \frac{P_{in}}{N_S} \tag{2.16}$$

where P_{in} is the power of input signal and N_s is the noise from the source

$$SNR_{out} = \frac{P_{out}}{N_{out}} = \frac{GP_{in}}{GN_S + N_{n,out}} \tag{2.17}$$

where P_{out} is the power of the output signal, N_{out} is the total noise power at the output, G is the power gain of the amplifier, $N_{n,out}$ is the output noise generated by the amplifier without any input noise.

Therefore, the noise factor can be written as

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{P_{in}}{N_S}\frac{GN_S + N_{n,out}}{GP_{in}} = 1 + \frac{N_{n,out}}{GN_S} = 1 + \frac{N_{n,in}}{N_S} > 1 \tag{2.18}$$

where $N_{n,in}$ is the total amplifier noise refer to the input. This equation reveals that any real system will degrade the SNR since all circuit blocks add additional noise.

The noise factor F can also be presented as

$$F = \frac{GN_S + N_{n,out}}{GN_S} = \frac{N_{total,out}}{GN_S} = \frac{total\ output\ noise\ power}{output\ noise\ due\ to\ input} \tag{2.19}$$

(2.19) is commonly used equation for calculating noise figure of an amplifier.

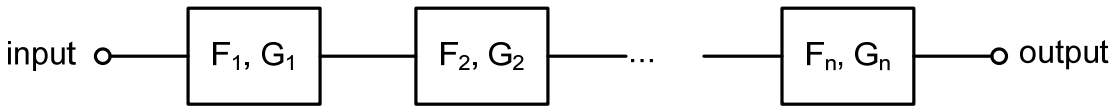


Fig. 2.5 A n-stage cascade system

Consider the total noise figure of cascaded blocks shown in fig 2.5. From equation (2.18), the noise added by each stage to the input is given by

$$N_{n,in} = N_S(F-1) \tag{2.20}$$

For simplicity, let's first consider the situation of n=2. The total input referred noise of the cascaded blocks can be found

$$N_{n,total,in} = N_S(F_1-1) + \frac{N_S(F_2-1)}{G_1} \tag{2.21}$$

The total noise figure can be calculated using (2.18) as

$$F = 1 + \frac{N_{n,total,in}}{N_S} = 1 + (F_1-1) + \frac{F_2-1}{G_1} \tag{2.22}$$

Apply the formula to general condition, we can get

$$F = 1 + (F_1-1) + \frac{F_2-1}{G_1} + \frac{F_3-1}{G_1G_2} + \frac{F_4-1}{G_1G_2G_3} + \ldots \tag{2.23}$$

which means the total noise figure of the cascade system is dominated by the noise figure of the first stage, if the gain of the first stage G_1 is sufficiently large.

2.3 Low Noise Amplifier Design Considerations

Since low noise amplifier is normally the first stage of an RF receiver, its performance will be very critical for the whole receiver system. There are several

specifications, such as input matching, gain, noise figure and 3rd-order intercept points, to characterize the performance of a low noise amplifier.

2.3.1 Input Matching

One task in LNA design is to create a 50-Ohm input impedance. As it is shown in fig 1.1, LNA is the first stage after the antenna, to have its input impedance matched to the impedance of the source will lead to the maximum power delivery. That is why the input match is also called power match. Another important reason for the impedance matching is to guarantee that the preceding components before the LNA function properly.. For instance, in some receiver topologies, a band-pass filter is placed before the LNA. Its key specifications, such as insertion loss, pass band ripple, stop band attenuation, are only guaranteed to be met over a specified range of terminating impedance, which is around 50-Ohm.

The input matching of a LNA is normally characterized by its S_{11}, which can be defined by

$$S_{11} = 20\log\frac{Reflected\ voltage}{Incident\ voltage} \tag{2.24}$$

In the low noise amplifier design, we want to minimize the power reflected by the input of the LNA. Hence, very low S_{11} is desired in the design.

2.3.2 Gain

The whole receiver system is actually an amplifier chain, amplifying the wanted signal to a certain level that allows the demodulator to detect and process it.

Several gain definitions exist for an amplifier. Power gain (G) is defined as the power delivered to the load divided by the power input to the network. Available power gain (G_A), defined as the power available from the network over the power available from the source, shows the maximum possible power gain of an amplifier. The transducer power gain (G_T) is calculated by the ratio of the power delivered to the load over the power available from the source. Among the three, the power gain (G) is the most widely used term because that it characterizes the actual power amplification of an amplifier. Since each block in the receiver system contributes to the gain, the gain of LNA is very important. High gain reduces impact of noise from components that followed, and sets the noise figure of the whole receiver chain at a certain low level, which can be seen from (2.23).

2.3.3 Noise Figure

As shown in (2.23), the noise figure of the LNA will be a dominant factor of the whole receiver chain. The noise figure of a RF receiver will finally determine its sensitivity. That is why noise figure is so important in the receiver designs.

The sensitivity P_s represents the smallest input signal power that can be reliably detected by the system [9]

$$P_s = -174dBm + 10\log BW + SNR + NF \tag{2.25}$$

The sum of the first two terms in (2.25) refers to power of the in-band noise floor. BW is the system operating bandwidth, which is determined by a specific application. System SNR is determined by the bit-error-rate (BER) requirement of the communication system. The SNR is usually different from different applications and modulation schemes. NF is the noise figure of the receiver system. Hence, the higher noise figure the receiver system has, the lower sensitivity the system will suffer.

2.3.4 Linearity

The output response with respect to the input of an ideal amplifier is strictly linear. However, in reality, every amplifier is a non-linear system. It can be modeled using a linear model around its operation point only when the input signal is sufficient small.

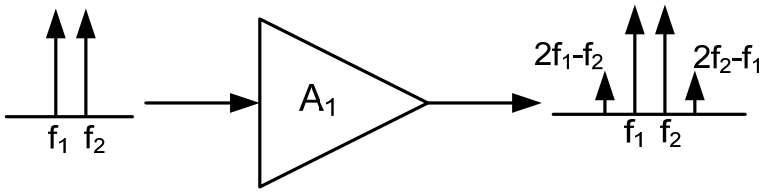


Fig. 2.6 Two tone test

The non-linearity performance is characterized by the two-tone test, depicted in fig 2.6. Two adjacent tones are input into a none-linear system A_1. Because of the 3rd order distortion, their inter-modulation products fall into the frequency of $2f_1$-f_2 and $2f_2$-f_1, which are in-band with the two fundamental tones f_1 and f_2. The cause of the inter-

modulation product can be explained mathematically using Taylor expansion. Any none-linear system could be described as

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \ldots \tag{2.26}$$

The two-tone input could be written as

$$x(t) = A_1 \cos \omega_1 t + A_2 \cos \omega_2 t \tag{2.27}$$

Then its output can be found as

$$\begin{aligned} y(t) = {} & a_1(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t) + a_2(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^2 \\ & + a_3(A_1 \cos \omega_1 t + A_2 \cos \omega_2 t)^3 \end{aligned} \tag{2.28}$$

By expanding the right side and discarding DC terms and harmonics, we can obtain the 3rd order inter-modulation products as

$$\frac{3a_3 A_1^{\,2} A_2}{4} \cos(2\omega_1 - \omega_2)t + \frac{3a_3 A_2^{\,2} A_1}{4} \cos(2\omega_2 - \omega_1)t \tag{2.29}$$

The 3rd order intercept point (IP3) is obtained as extrapolating the fundamental tone output with the slope=1 and the 3rd order inter-modulation (IM_3) tones with the slope=3 from a very low input power level until they intercept each other, shown in fig 2.7. The x-coordinate of the intersection point is called input referred 3rd order intercept point (IIP3), and the y-coordinate is called the output referred 3rd order intercept point (OIP3).

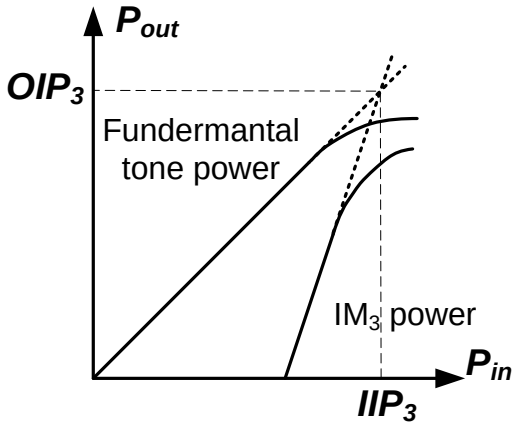


Fig. 2.7 3rd order intercept point

Linearity is important because it represents how a receiver can deal with interferers. The power of the interferers can be orders of magnitude higher than the power of the desired signal and corrupt the wanted signal if the linearity of the receiver is not high enough.

Gain, noise figure, input matching and linearity are the main considerations for the low noise amplifier designs. Besides, low power consumption and small chip area are also desired, as they may determine the battery life and the cost of the product.

2.4 Inductive Source Degeneration Low Noise Amplifiers

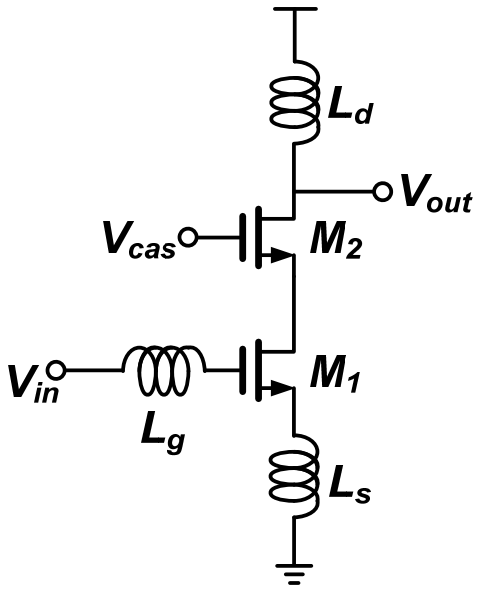
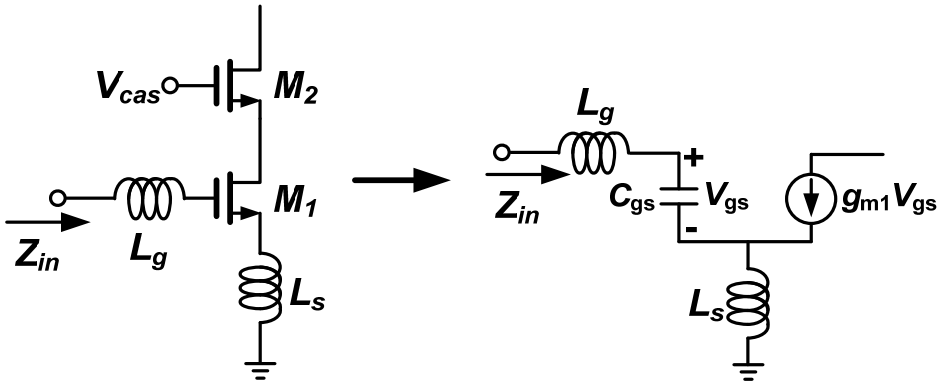
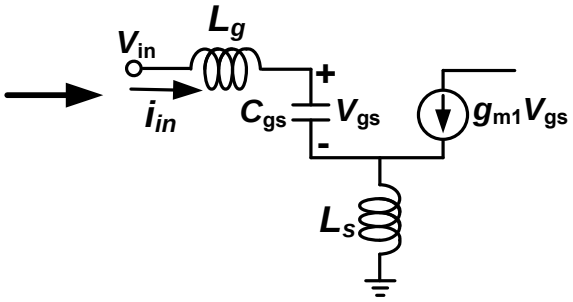


Fig 2.8 Schematic of an inductive source degeneration LNA

Among all the LNA designs, perhaps the most widely used LNA topology is the inductive source degeneration LNA, which is shown in fig 2.8. For it can provide very good input matching, low noise figure, high gain and decent linearity simultaneously.



(a) (b)



(c)

Fig 2.9 Small signal model for the analysis the input impedance of the inductive source degeneration LNA

The input impedance of the inductive source degeneration LNA could be analyzed using small signal model in fig 2.9(b), which is derived from fig 2.9 (a), by applying a current i_{in} at the input and found the voltage v_{in} at input node, shown in fig 2.9 (c) . Fig. 2.9(a) was obtained from Fig. 2.8 neglecting M_2 an L_d due to the small capacitance C_{gd} of M_1 that approximately prohibits signal from going from M_1 to M_2.

$$v_{in} = (j\omega L_g + \frac{1}{j\omega C_{gs}})\, i_{in} + (\, i_{in} + g_{m1} v_{gs})\, j\omega L_s \tag{2.30}$$

Since

$$v_{gs} = \frac{1}{j\omega C_{gs}}\, i_{in} \tag{2.31}$$

We have

$$v_{in} = (j\omega L_g + \frac{1}{j\omega C_{gs}})\, i_{in} + (1 + g_{m1}\frac{1}{j\omega C_{gs}}) j\omega L_s\, i_{in}$$

$$= (j\omega L_g + \frac{1}{j\omega C_{gs}} + j\omega L_s)\, i_{in} + \frac{g_{m1}}{C_{gs}} L_s\, i_{in} \tag{2.32}$$

Hence, the input impedance could be calculated as

$$Z_{in} = \frac{v_{in}}{i_{in}} = j\omega L_g + j\omega L_s + \frac{1}{j\omega C_{gs}} + \frac{g_{m1}}{C_{gs}} L_s \tag{2.33}$$

At the frequency of interested, C_{gs} and L_g+L_s resonant out, the input impedance is

$$Z_{in} = \frac{g_{m1}}{C_{gs}} L_s = \omega_T L_s \tag{2.34}$$

where $\omega_T = g_m/C_{gs}$ is the transit frequency, which is determined by processing and biasing condition of the CMOS transistor. (2.34) shows that at the resonant frequency, the input impedance of the inductive source degeneration LNA is purely resistive. And it is proportional to L_s. By choosing L_s appropriately, this real term can be made equal to 50-Ohm. It is also interesting that this real part shown in (2.34) is frequency independent, which makes it possible to be used for the wideband matching.

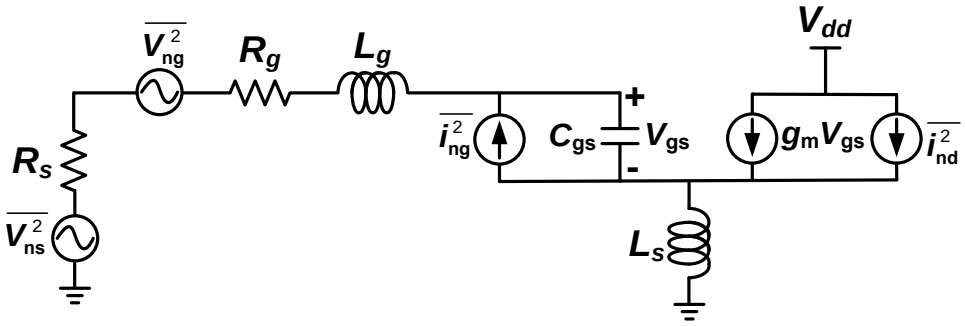


Fig 2.10 Small signal model for noise analysis of the inductive source degeneration LNA

The noise figure of the inductive source degeneration LNA can be analyzed using the small signal model for noise analysis in fig 2.10. The total noise Power

Spectrum Density (PSD), $S_{noise,gdc}$, caused by i_{nd}, i_{ng} and the correlated part between the two can be written from Fig. 2.10 [10]

$$S_{noise,gdc} = \kappa S_{noise,i_d} = \frac{4kT\gamma\kappa g_{d0}}{(1+\frac{\omega_T L_S}{R_S})^2} \tag{2.35}$$

where

$$\kappa = \frac{\delta\alpha^2}{5\gamma}|c|^2 + \left[1+|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}}\right]^2 \tag{2.36}$$

$$Q_L = \frac{\omega_0(L_s+L_g)}{R_s} = \frac{1}{\omega_0 R_s C_{gs}} \tag{2.37}$$

The noise part contributed by the uncorrelated portion of the gate noise can be written as

$$S_{\alpha,i_g,u} = \xi S_{noise,i_d} = \frac{4kT\gamma\xi g_{d0}}{(1+\frac{\omega_T L_S}{R_S})^2} \tag{2.38}$$

where

$$\xi = \frac{\delta\alpha^2}{5\gamma}(1-|c|^2)(1+{Q_L}^2) \tag{2.39}$$

Combining (2.35) and (3.39), we have

$$S_{a,M_1} = \chi S_{a,i_d} = \frac{4kT\gamma\chi g_{d0}}{(1+\frac{\omega_T L_S}{R_S})^2} \tag{2.40}$$

where

$$\chi = \kappa + \xi = 1 + 2|c|Q_L\sqrt{\frac{\delta\alpha^2}{5\gamma}} + \frac{\delta\alpha^2}{5\gamma}(1+Q_L^2) \tag{2.41}$$

From (2.40) and (2.41), we have

$$F = 1 + \frac{R_l}{R_s} + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\frac{\chi}{Q_L}\left(\frac{\omega_0}{\omega_T}\right) \tag{2.42}$$

where R_l is the parasitic resistance of L_g, R_g is the parasitic resistance at the gate of the transistor, R_s is the source resistance, which is 50-Ohm.

3. DISTRIBUTED LOW NOISE AMPLIFIERS

As a solution for extremely wide-band amplification for several decades, distributed amplifiers have been widely used in many applications. The recent emergence of the CMOS technology had led to a new revolution of wireless communication because of its low-cost and high level of integration. A lot of research has been done on implementing distributed amplifiers in CMOS.

In this section, we are going to investigate the design of distributed amplifier with the commercial available CMOS process and the possibility of using a CMOS distributed amplifier as the candidate for UWB applications. To that end, several distributed amplifiers were designed and fabricated in commercial CMOS process. The design of these novel structures along with their measurement results will be presented.

3.1 History and Motivation

The concept of distributed amplification has been around for over a half century. Its origin can be traced back to a patent by Percival in 1936 [11] as an attempt to produce an amplifier without the usual gain-bandwidth constraint. The term distributed amplifier first appeared in a paper by Ginzon et al. in 1948 [12]. Since then, it has been widely used in various circuits from vacuum tubes to silicon and Gallium Arsenide (GaAs) monolithic microwave integrated circuits (MMICs), e.g., [13-16].

Distributed amplifiers, because of their intrinsic wide bandwidth, find many applications, including television, pulsed radar, radio astronomy, satellite

communications, nuclear research, oscillography, and network test equipment systems. Early distributed amplifiers were implemented using vacuum tubes and high speed GaAs MESFETs. The recent emergence of silicon as a valuable alternative for realizing low-cost and highly-integrated MMICs has created great interests in the implementation of broadband amplifiers in technologies such as silicon-germanium (SiGe) and CMOS. One major difficulty associated with implementing distributed amplifiers in CMOS owes to deleterious substrate coupling effects, especially, the highly doped substrate losses in planar monolithic inductors at frequencies above a few gigahertz. Early design of distributed amplifiers in CMOS technology involved different kinds of transmission lines [17-18] as substitutes for inductive elements to alleviate the low quality factor (Q) of on-chip inductors which degrades the over-all performance of amplifiers. However, the layouts of these circuits consume large die areas due to the use of transmission lines.

Recently, with the dimensions of CMOS transistors continually scaling down, on-chip inductors with very small inductance in the range of several hundred pico-Henrys can be used in CMOS distributed amplifiers. These small inductance values facilitate not only the design, but also the Q-enhancement of on-chip inductors. Additionally, the availability of thick top metal layers in advanced CMOS processes also leads to Q improvement for on-chip inductors. Altogether, these make it possible for CMOS distributed amplifiers with on-chip inductors to achieve simultaneously good performance and small die area. Many fully-integrated CMOS distributed amplifiers with relatively flat gain over very wide bandwidths, from DC up to 40 GHz, have been recently reported. [19-23]

3.2 Principle of Distributed Amplification

The basic design principle of distributed amplifiers is based on forming two artificial transmission lines at the input and output ports of the constituting gain cells by periodically combining serial inductive components with the parasitic capacitors of the gain cells. Essentially, the input and output capacitances are absorbed into the artificial transmission lines, resulting in an extremely wideband performance.

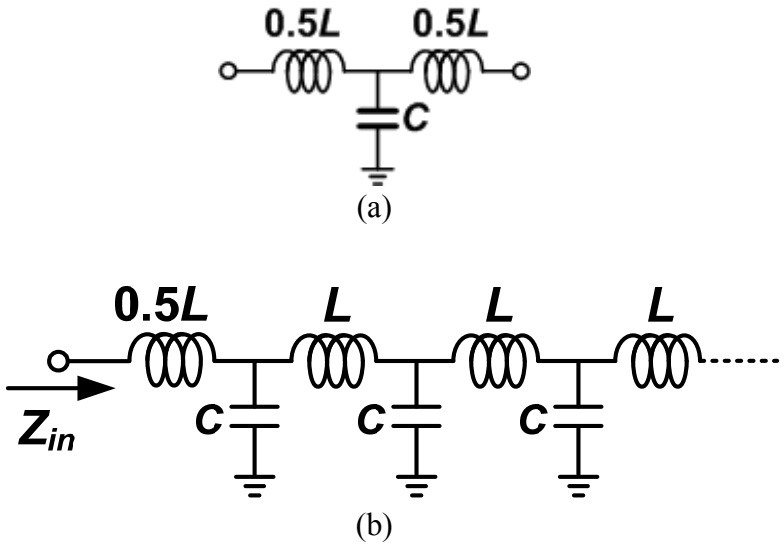


Fig. 3.1 Lumped-element model of artificial transmission lines: (a) Lumped-element network representing one element of the artificial transmission line (b) An artificial transmission line consists of infinite number of elements in (a)

Consider a simple lumped element network shown in fig. 3.1(a), an artificial transmission line, depict in fig. 3.1(b) can be formed by connecting multiple number of this kind of networks in serious. Specifically, assuming there are infinite number elements in the artificial transmission line, let's find out the impedance of this artificial transmission line.

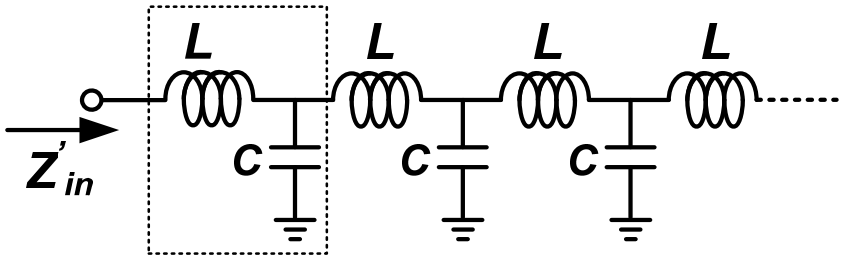


Fig. 3.2 Infinite ladder network to calculate the impedance of the artificial transmission line

For simplicity, consider an infinite ladder network shown in fig. 3.2, its impedance $Z_{in}^{'}$ could be derived using

$$Z_{in}^{'} = j\omega L + \frac{1}{j\omega C} // Z_{in}^{'} \tag{3.1}$$

Solving for $Z_{in}^{'}$ yields

$$Z_{in}^{'} = \frac{j\omega L}{2}\left(1 \pm \sqrt{1 - \frac{4}{\omega^2 LC}}\right) \tag{3.2}$$

Since

$$Z_{in} = Z_{in}^{'} - \frac{j\omega L}{2} \tag{3.3}$$

Z_{in} can be expressed

$$Z_{in} = Z_{in}^{'} - \frac{j\omega L}{2} = -\frac{j\omega L}{2} \cdot \sqrt{1 - \frac{4}{\omega^2 LC}} \tag{3.4}$$

When $\omega \ll \frac{1}{\sqrt{LC}}$, we have

$$Z_{in} \approx -\frac{j\omega L}{2} \cdot (-j)\frac{2}{\omega\sqrt{LC}} = \sqrt{\frac{L}{C}} \tag{3.5}$$

This equation shows that the artificial transmission line presents a real, frequency independent, constant impedance. However, this only is valid over a finite bandwidth.

As the frequency increases, Z_{in} becomes smaller and smaller. When ω increases to a certain level ω_c, where

$$\omega_c = \frac{2}{\sqrt{LC}} \tag{3.6}$$

Z_{in} becomes to zero. No power could be delivered to the line. This frequency is called cut-off frequency of the artificial transmission line.

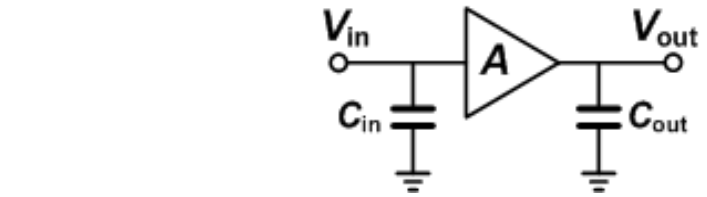
$$f_c = \frac{1}{\pi\sqrt{L \cdot C}} \tag{3.7}$$

where f_C is the cut-off frequency of the artificial transmission line, which normally determines the bandwidth of the distributed amplifier.

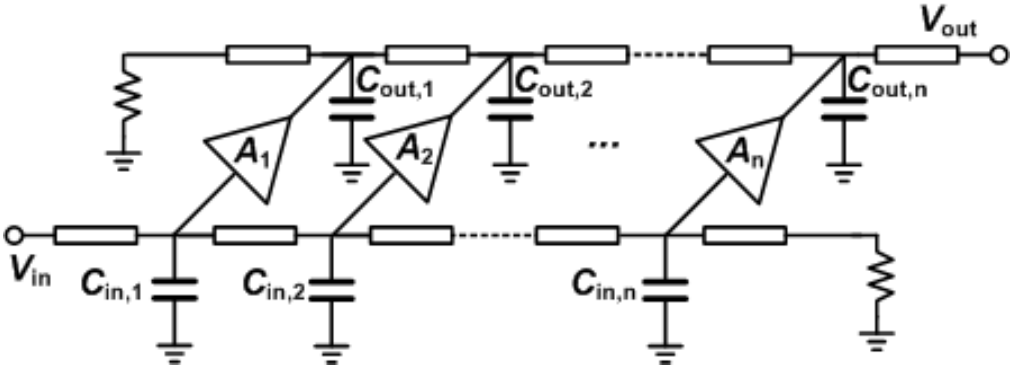
If the desired impedance Z of the transmission line is fixed, the cut-off frequency f_c can be expressed as

$$f_c = \frac{1}{\pi \cdot C \cdot Z} \tag{3.8}$$

Equation (4) shows that the bandwidth of a distributed amplifier decreases as value of the (parasitic) capacitance C increases. Since this capacitance is proportional to the dimension of the employed MOSFET transistors, the gain of the distributed amplifier is determined by the transconductance of each transistor, which could be increased by increasing its gate width. Equation (4) also shows possible trade-off between gain and bandwidth in distributed amplifier design.



(a)



(b)

Fig.3.3 Principle of distributed amplifiers: (a) A simple amplifier with input and output capacitors (b) A distributed amplifier implementing the simple amplifiers as gain cells

We consider a simple amplifier as shown in Fig. 3.3 (a). C_{in} and C_{out} are the parasitic capacitors at the input and output node the amplifier A. From the simple circuit analysis, these two parasitic capacitors will form two poles that will limit the bandwidth of this amplifier. As several of these amplifiers, acting as gain cells, are parallel-connected in distributed amplifiers, as shown in Fig. 3.3 (b), their input and output capacitors are absorbed into the artificial transmission lines of the distributed amplifiers. The two poles are then pushed far away from their original locations, which are at very low frequencies, to the cut-off frequency of the two artificial transmission lines.

As the input signal travels through the input line, each gain cell's input is excited

by the traveling voltage wave and transfers the amplified signal to its output. If the velocity and phase of the input line are equal to those of the output line, the signals on the output line add in the forward direction and arrive at the amplifier's output. The signal traveling in the reverse direction will be absorbed by the drain-line termination. To accommodate the respective loading input and output capacitance, the transmission line's characteristic impedance must be greater than the desired characteristic impedance of the artificial line, which is often 50-Ohm for matching purpose. Low loss is needed to maintain well-behave artificial transmission lines, which are critical for realizing distributed amplifiers.

The gain G of the conventional distributed amplifier has been analyzed in [23] and can be estimated, in a loss-free case, by

$$G = \frac{n^2 g_m^2 Z_{0g} Z_{0d}}{4} \tag{3.9}$$

where n is the number of the stages, g_m is the transconductance of each gain cell, Z_{0g} and Z_{0d} are the characteristic impedance of the gate line and drain line, which are also known as input line and output line, respective. Equation (3.9) shows that, if Z_{0g} and Z_{0d} are fixed to a certain value, the gain of the distributed amplifier is only affected by n and g_m. And one could always increase the gain of the distributed amplifier by increasing the number of stages, in lossless case.

However, in the real case, the loss of the transmission line can't be ignored, especially for the transmission lines in CMOS, because the lossy silicon substrate and

narrow lines. When the loss of the transmission lines are taking into account, the gain of the distributed amplifier can be written as [24]

$$A_V = \frac{g_m^2 \cdot Z_g e^{-N\cdot\alpha_g} \cdot Z_d e^{-N\cdot\alpha_d}}{4(\alpha_g - \alpha_d)^2} \tag{3.10}$$

where g_m is the transconductance of each gain cell, N is the number of stages, and Z_g and Z_d are the characteristic impedances of the input and output lines, respectively. α_d and α_g are the attenuation constants per section of the gate and drain lines. Equation (3.10) implies that when more stages are used in the distributed amplifier, more loss will also be introduced. Thus the gain can not be increased by simply increasing the number of stages. In stead, there will be an optimum number of stages that gives the maximum gain. The optimum number of stages, N_{opt}, can be found [24].

$$N_{opt} = \frac{\ln(\alpha_d / \alpha_g)}{\alpha_d - \alpha_g} \tag{3.11}$$

The gain of the distributed amplifier with optimized number of stages is only the function of Z_d, Z_g, α_d, α_g and g_m. However, in practice, the artificial transmission lines at input and output have to match to the impedance of the input and output, which is normally 50-Ohm. In other words, Z_d and Z_g have to be around 50-Ohm. Hence, the keys to optimize the gain of a distributed amplifier rely only on two things, one is to minimize the loss on the artificial transmission lines, and the other is to increase the transconductance of each gain cell.

3.3 A 0.25-μm CMOS UWB Amplifier for Time-Domain UWB Application

3.3.1 Motivation

In February 2002, the Federal Communications Commission (FCC) assigned the frequency range from 3.1 to 10.6 GHz for potential uses of ultra wideband (UWB) systems. This has made UWB a focal point for many wireless applications. The origin of UWB technology can be traced back to the early 1960's on time-domain electromagnetics [25], when the study of electromagnetic-wave propagation was viewed from the time domain perspective, rather than from the more common frequency domain.

UWB technology, based on the transmission and reception of trains of short pulses having very low power, can achieve very good time and spatial resolutions. This makes UWB an ideal candidate for many applications, such as accurate locating, high data rate communication, radar, etc. Several commercial applications now employ UWB technique [26]. These applications require the use of CMOS or CMOS related technology for low system cost and ease in direct integration with digital circuits on single chips.

Distributed amplifier, because of its extremely wide bandwidth, became a good candidate of the LNA of the UWB systems. In this sub-section, we report on the development of an ultra-wideband CMOS distributed amplifier and its unprecedented non-sinusoidal time-domain performance for UWB applications. The developed UWB CMOS amplifier is realized with finite-ground coplanar waveguide (CPW) and operated over the full ultra-wide bandwidth of 3.1-10.6 GHz under non-sinusoidal signal

environment. We also demonstrate that good performance can be achieved for UWB applications using a standard low-cost 0.25-μm CMOS process. The amplifier was characterized both theoretically and experimentally in the time domain using monocycle and impulse signals. Measured results show that the amplifier has a gain of around 6 dB and a return loss of more than 13 dB. The measured output waveforms also resemble closely those of the input signals, demonstrating that the developed UWB amplifier can reproduce faithfully the waveform of a UWB non-sinusoidal pulse signal. This high signal fidelity is a critical requirement for time-domain UWB systems, as the UWB pulse signal carrying information must be transmitted with minimum distortion.

3.3.2 Circuit Design

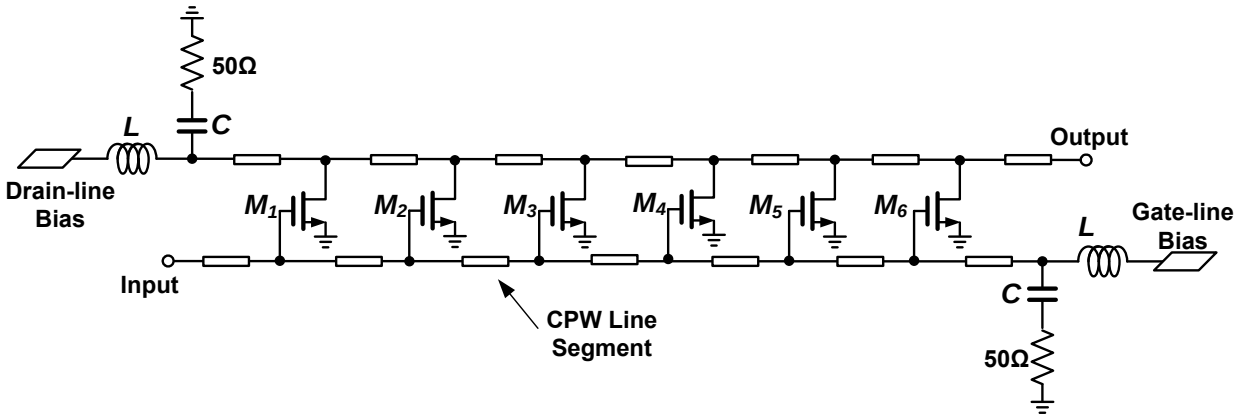


Fig. 3.4 schematic of the UWB distributed amplifier using six NMOS transistors

Fig. 3.4 shows the schematic of the UWB distributed amplifier using six NMOS transistors. The transmission line connecting the gates and that connecting the drains are

periodically loaded with the NMOS gate-source and drain-source capacitance, respectively. Together, they form artificial transmission lines at the gates (gate line) and drains (drain line) of the NMOS transistors. The gate line and drain line are terminated with resistors having resistances of 50-Ohm, which are the artificial transmission lines' characteristic impedances. On-chip capacitor C blocks the DC path from the bias to the terminal resistors. On-chip inductors L, acting as a RF choke, feed the DC voltage and current to the circuit, while stopping the RF signals from going through it. Finite-ground CPW is used to allow easy connection of the sources of the NMOS transistors to the ground while maintaining a compact size for the amplifier. CPW also facilitates wider central strip for high characteristic impedance than its microstrip line counterpart, thus lowering the conductor loss. Low loss is needed to maintain well-behave artificial transmission lines, which are critical for realizing distributed amplifiers.

3.3.3 Fabrication and Performance

The UWB amplifier was fabricated using the TSMC 0.25-μm CMOS process [27]. The topmost metal layer is chosen for the CPW to obtain low loss due to its thickest metallization and farthest distance from the silicon substrate. Bias circuits are formed by on-chip inductors and capacitors. IE3D [28] was used to calculate S-parameters of the CPW structure, which was then imported into the Agilent's Advanced Design System (ADS) [29] along with the NMOS transistor's measured S-parameters for time-domain simulation. Bent CPW is used for size reduction. Its characteristic impedance is mainly determined by the line width, gap and thickness of the conductor

and dielectric underneath it.

Fig. 3.5 and 3.6 shows the bent CPW transmission line structure, which was modeled in IE3D. The total length of the bent CPW transmission line structure is 1 mm. With the width of the signal line of 30 μm and gap between the signal line and finite ground plane of 45 μm, two finite ground plans with a width of 35 μm was used for the size reduction. The bent CPW line was designed to have a characteristic impedance of around 75-Ohm to accommodate the parasitic capacitance of the NMOS transistors.

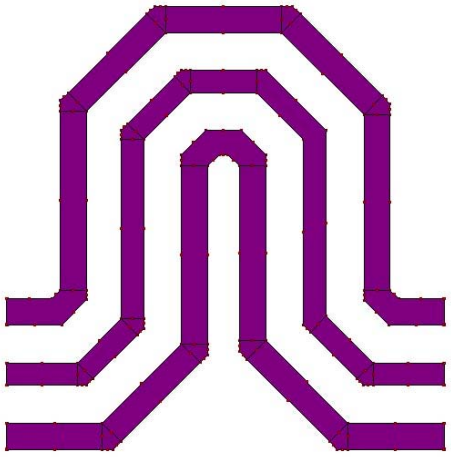


Fig. 3.5 Bent CPW line modeled in IE3D

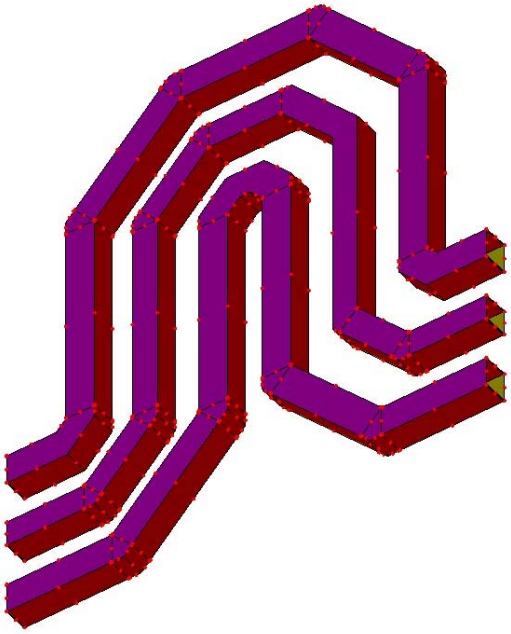


Fig. 3.6 3D View of the bent CPW line modeled in IE3D

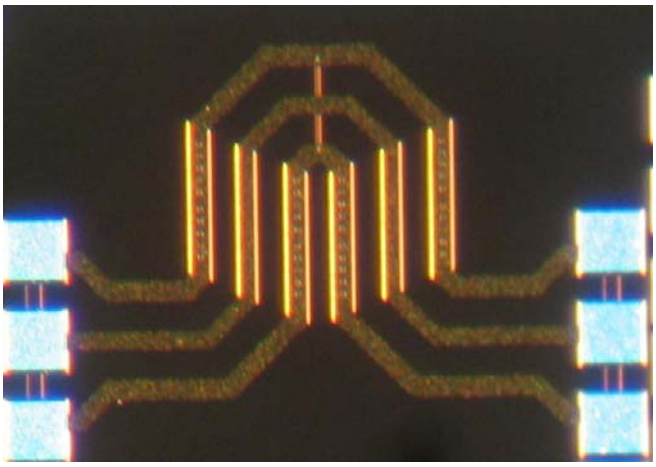


Fig. 3.7 Microphotograph of the test structure of the bent CPW with finite ground plan

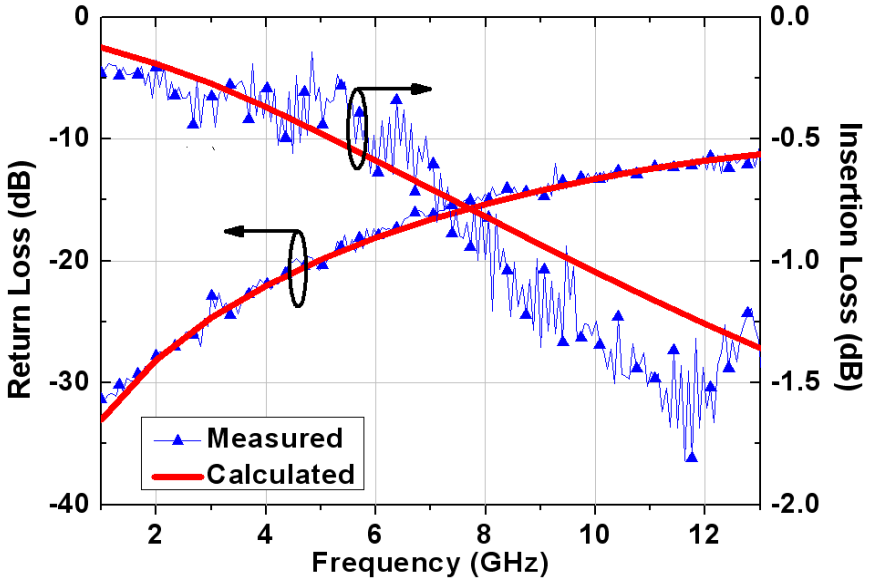


Fig. 3.8 Measured and calculated insertion and return losses of the bent CPW

To assess on-chip performance of the bent CPW with finite ground plan, one bent CPW structure was also fabricated in the same wafer with the distributed amplifier. Fig. 3.7 is the microphotograph of testing structure. On-wafer measurement was performed on this structure with on-wafer probes and a network analyzer. The measurement results together with the simulation results are plotted in fig. 3.8. Less than 1.5 dB and more than 12 dB are obtained for the insertion and return losses, respectively, over the entire ultra-wide bandwidth of 3.1-10.6 GHz. The simulation results and measurement results matched very well within 10 GHz. These results are similar to those of the straight CPW.

Fig. 3.9 shows the calculated and measured phase responses of the UWB amplifier. The results show that the amplifier exhibits very linear phase response within the entire UWB frequency range with good agreement between the calculated and

measured phase. Linear phase response and, hence, constant group velocity across a circuit are very critical for UWB applications.

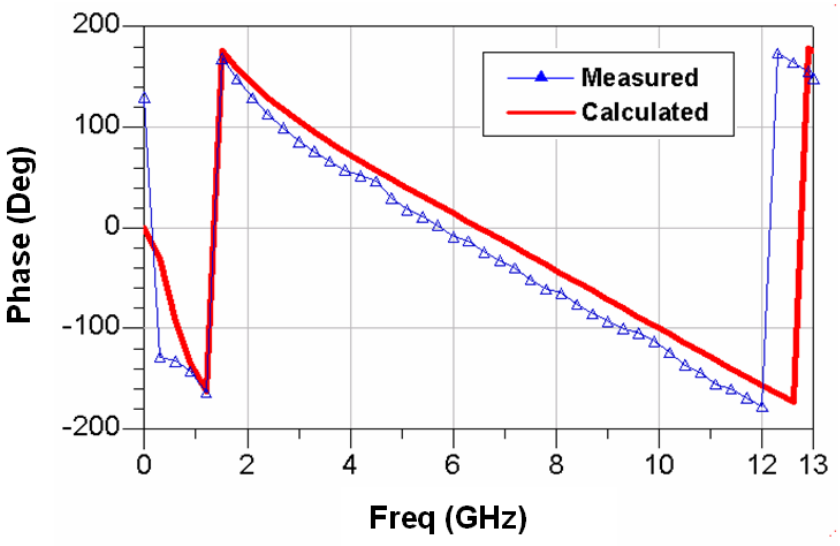


Fig. 3.9 Phase response of the UWB CMOS amplifier

To assess performance of the amplifier and its suitability for UWB applications, both simulation and measurement have been conducted in the time domain. Fig. 3.10 shows the calculated waveform of the output signal for an input impulse of 100-ps 3-dB pulse-width. The output waveform is distorted as expected due to the fact that the amplifier does not pass the low-frequency and DC components of the input impulse. Fig. 3.11 shows the calculated output waveform for an input monocycle pulse with 200-ps 3-dB pulse-width. The time-domain measurement was performed on-wafer using on-wafer probes, impulse and monocycle pulse generators, and digitizing oscilloscope. A broadband directional coupler was also used to measure the reflection at the input port of the UWB amplifier. Figs. 3.12 and 3.13 show the measured output signals for a 100-ps impulse and 200-ps monocycle pulse input, respectively. The measured gain is around 6

dB for the monocycle pulse input. The gain is lower for the impulse input signal because the amplifier does not pass the low-frequency and DC components outside the desired ultra-wide frequency range of 3.1-10.6 GHz, as indicated earlier. As can be seen, the output waveforms match closely those at the input with similar pulse duration and very little distortion. This faithful reproduction of the signal waveforms demonstrates that the developed UWB amplifier fulfills one of the most critical requirements for time-domain UWB applications, namely retaining the shape and duration of a transmitted pulse. The agreement between calculated and measured pulses, as seen from Figs. 3.10-3.13, is also reasonably good. Figs. 3.14 and 3.15 show the measured reflected signals at the input port for the 100-ps impulse and 200-ps monocycle pulse input, respectively. More than 13-dB return loss is obtained. The input pulses displayed in the figures are the signals reflected from an open circuit. Both the input and reflected signals were measured at the same coupling port of the directional coupler.

The UWB amplifier was driven from a 3.3-V power supply and has a power consumption of 68 mW.

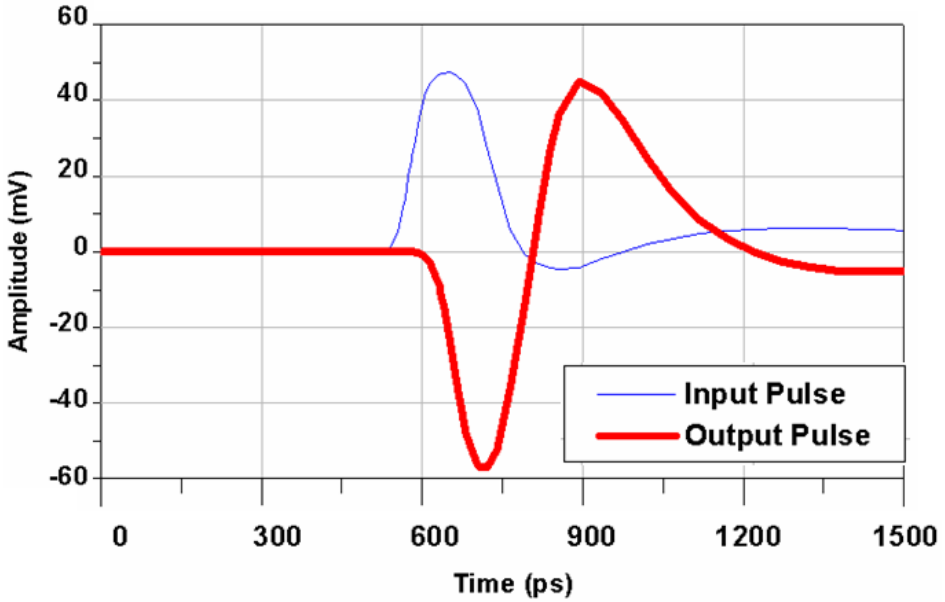


Fig. 3.10 Time domain simulation result with impulse input

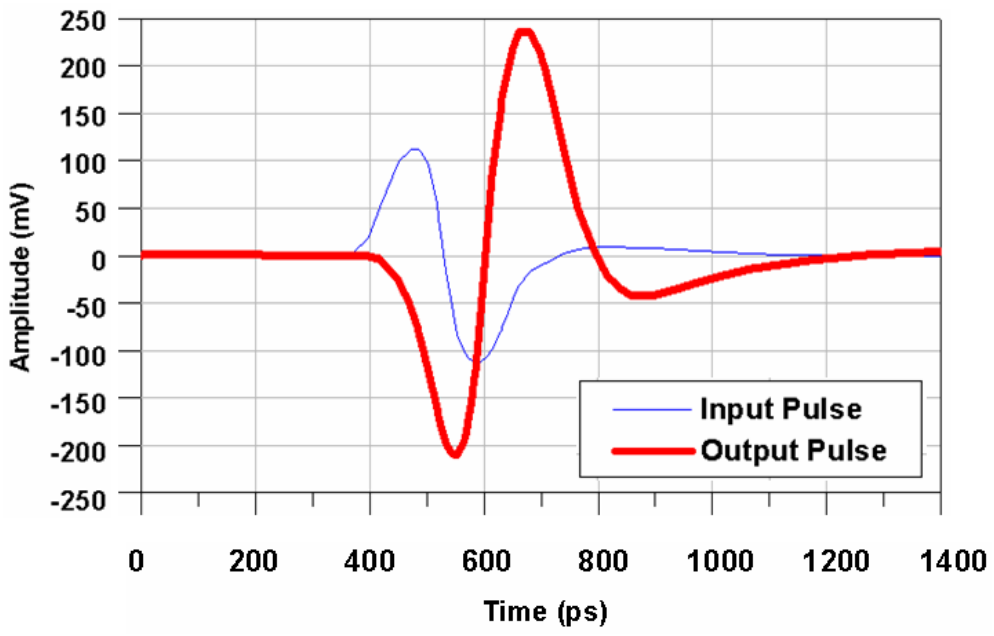


Fig. 3.11 Time domain simulation result with monocycle pulse input

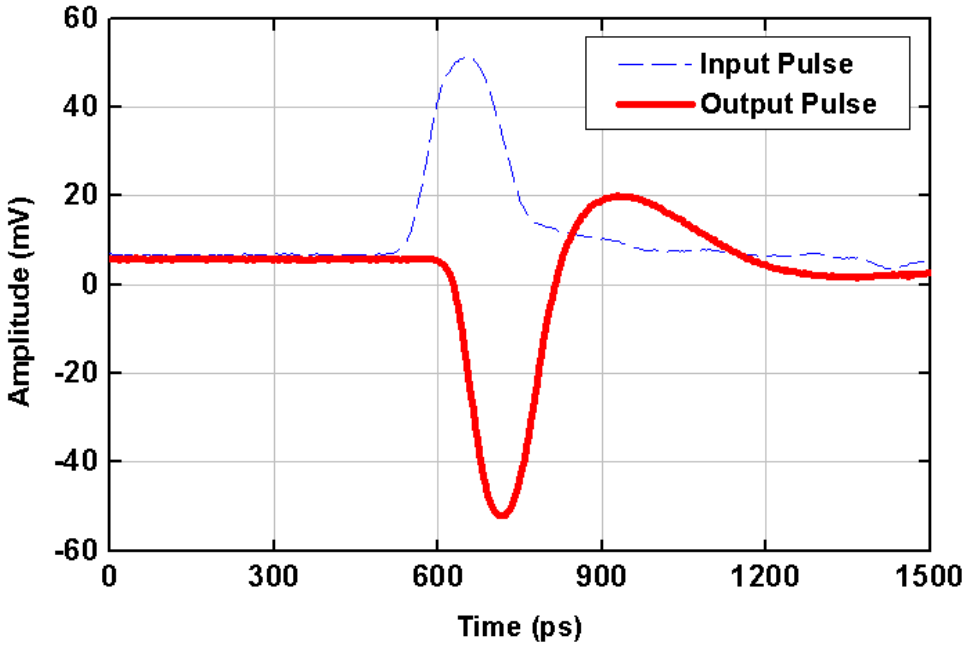


Fig. 3.12 Measured output pulse with 100-ps impulse input

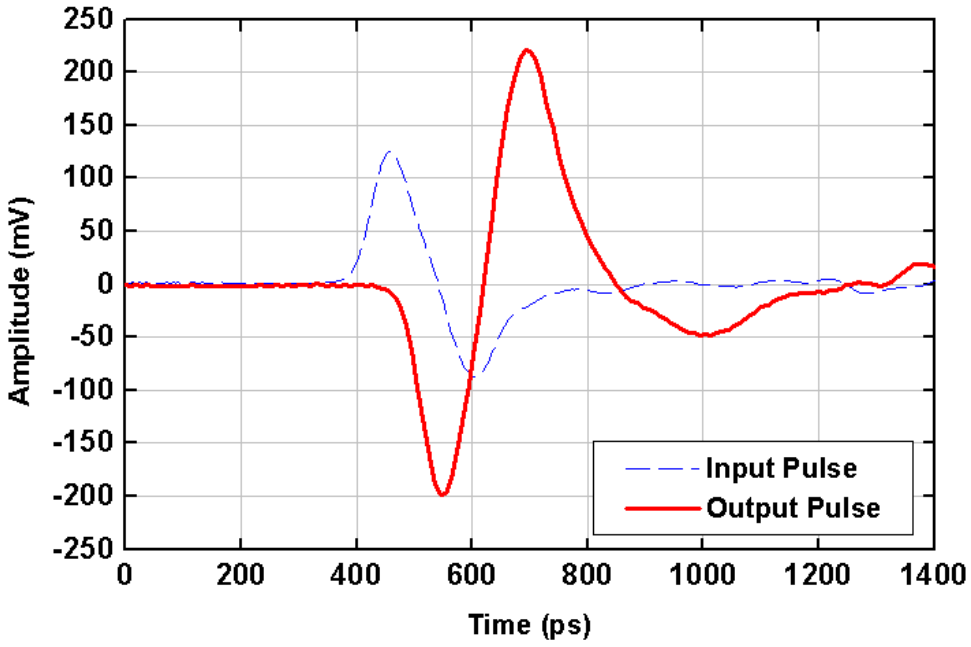


Fig. 3.13 Measured output pulse with 200-ps monocycle pulse input

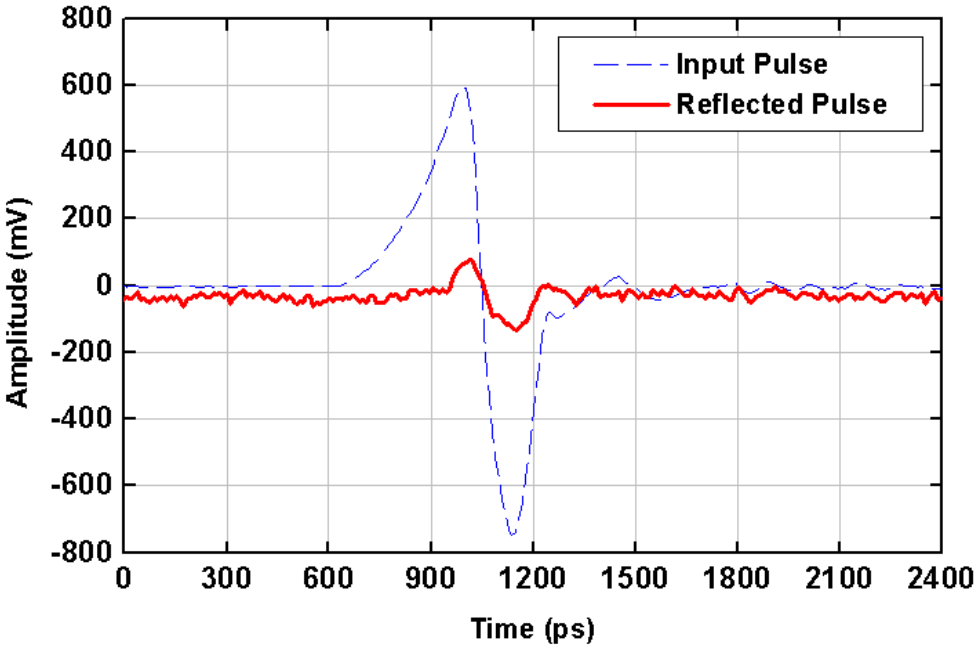


Fig. 3.14 Measured reflected signal at the input port for 200-ps monocycle pulse input signal

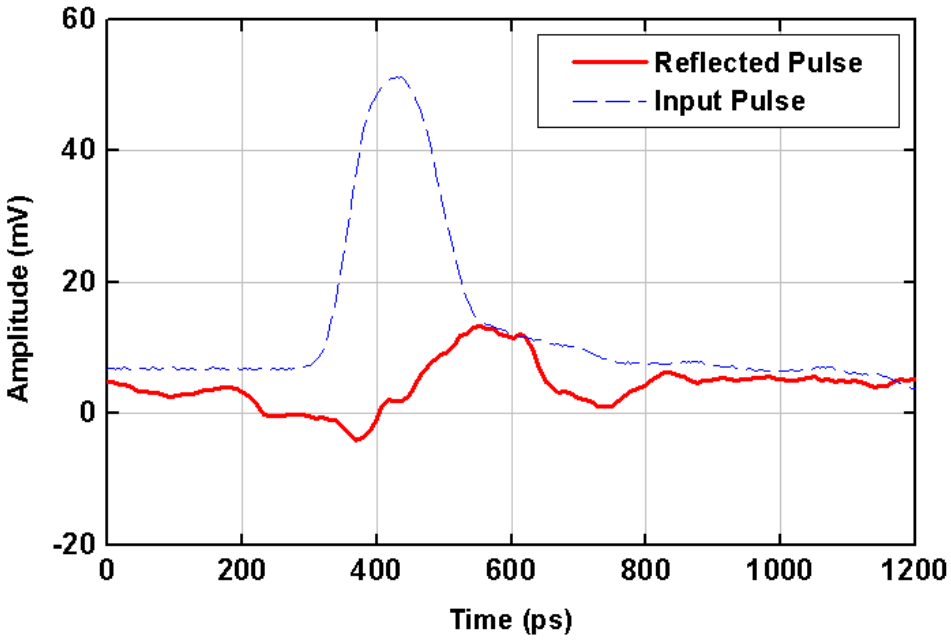


Fig. 3.15 Measured reflected signal at the input port for 100-ps impulse input signal

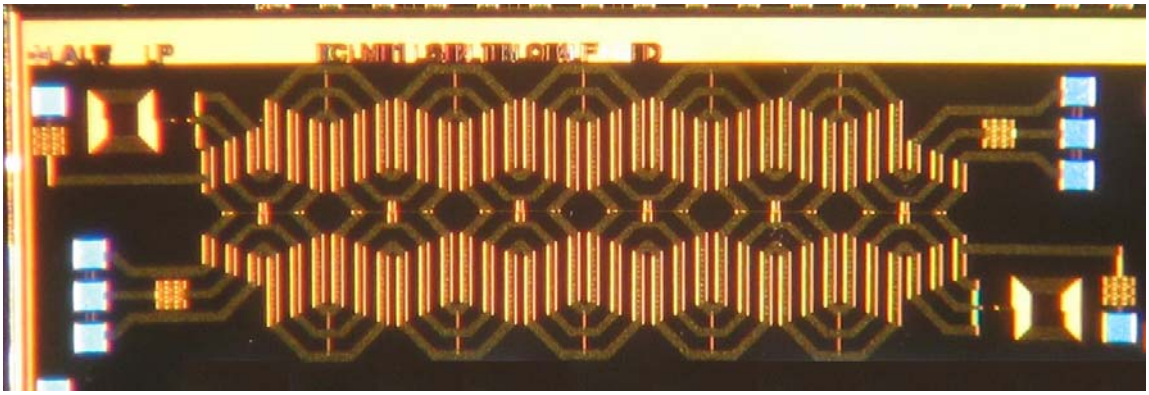


Fig. 3.16 Microphotograph of the Distributed UWB amplifier with CPW

Fig 3.16 shows the microphotograph of the distributed UWB amplifier with CPW transmission lines. The chip area is $0.8\times2.6mm^2$.

3.3.4 Conclusion

A CPW UWB amplifier has been designed and fabricated using a standard low-cost 0.25-μm CMOS process for UWB applications. The amplifier was characterized completely in the time domain under non-sinusoidal signal operation necessary for UWB applications. It has 6-dB gain and more than 13-dB return loss. The amplifier's output waveforms resemble closely those at the input with very little distortion, proving that it is appropriate for time-domain UWB applications. This UWB CMOS amplifier is ready to be integrated with other CMOS RFIC building clocks for UWB wireless communication systems.

3.4 A High-Performance, Compact, Ultra-Wideband CMOS Distributed Amplifiers with On-Chip Patterned-Ground-Shield Inductors

3.4.1 Motivation

Using typical on-chip inductors for CMOS distributed amplifiers poses major challenges in the design. Traditional on-chip inductors on standard CMOS processes normally have very low Q due to large parasitics [30]. These low-Q inductors, when used in distributed amplifiers, greatly degrade the performance of amplifiers, especially the gain and noise figure at high frequencies. Although this problem could be minimized by using CAD optimization techniques that involve optimizing the amplifier design with different inductor models [31, 32], it is still inconvenient and time-consuming for RF designers to go through such procedures. Furthermore, sufficient distances between on-chip inductors, or between on-chip inductors and other circuit elements, must be allowed to avoid unwanted effects resulting from electric or magnetic coupling through the silicon substrate. The required distances among elements particularly affect the layout of distributed amplifiers, due to the fact that they typically employ more inductors, especially adjacent inductors, than other CMOS RFIC's, hence resulting in large die areas. It is always desirable in RFIC design to implement on-chip inductors, which not only have high Q, but also require less spacing between them, to improve the circuit performance and size.

Patterned ground shield (PGS) [33] is an efficient technique to achieve high-Q on-chip inductors and reduced substrate coupling between them. However, PGS

inductors have not been used in distributed amplifiers and other wide-band RFICs due to several issues resulting from parasitic capacitances introduced by the PGS layer.

In this part, we report a CMOS distributed amplifier implementing PGS on-chip inductors. We demonstrate a practical design showing that using PGS inductors in CMOS distributed amplifiers not only helps achieve good performance over extremely wide bandwidths, but also reduce the die area, even in low-cost standard 0.25-μm CMOS processes.

3.4.2 Patterned Ground Shield (PGS) Inductors in Distributed Amplifier Design

Silicon substrates with conductivity around 1-20 Ω·cm, typically used in commercial CMOS processes, produce large signal loss in passive elements. This loss, particularly, makes on-chip inductors one of the bottle necks in many CMOS RFIC designs. PGS produces high Q for on-chip spiral inductors by isolating the inductors from a lossy silicon substrate with ground shields having slots orthogonal to the spiral traces. In PGS inductors, most of generated electric fields are short-circuited to the ground by the PGS layer, while inducing only a small amount of eddy currents. This results in significantly less substrate effects due to electric fields and hence helps increase the Q of PGS inductors. As reported in [33], the Q of on-chip PGS spiral inductors is improved by 33% as compared to that of on-chip inductors without shield. Moreover, the PGS can also reduce the substrate coupling between two adjacent inductors by as much as 25 dB [33]. PGS inductors have been used in lumped-element voltage-controlled oscillators [34] and narrow-band low noise amplifiers [35].

PGS on-chip inductors are also particularly attractive for CMOS distributed amplifiers, as they can lead to not only good performance, resulting from relatively high-Q inductors, but also very compact size, due to close spacing between adjacent inductors without severe coupling effects, for distributed amplifiers. PGS inductors, however, have several problems resulting from unwanted parasitic capacitances produced by the PGS layer, which have prevented them from being used in CMOS distributed amplifiers and other wide-band RFIC's, Firstly, the existence of the PGS layer inevitably introduces additional parasitic capacitance into the inductors, resulting in lower resonant frequencies than those of inductors without PGS. This may lead to serious problems in distributed amplifier design, whose bandwidth is so wide that its upper frequency end is near or beyond the PGS inductors' resonant frequencies. Secondly, to maintain constant characteristic impedance for the artificial transmission lines, a higher inductance for the PGS inductors is needed to accommodate the increase in parasitic capacitance. This, together with the increased parasitic capacitance, will, however, reduce the bandwidth, according to (3.8). Thirdly, the characteristic impedance of the artificial transmission lines decreases at high frequencies due to the increase and decrease of the capacitance and inductance, respectively, which affects the matching at both the input and output ports. Finally, as can be seen in Figs. 3.20 and reported in [30], the inductance and Q of a PGS inductor vary more than those of inductors without PGS from DC to resonant frequency. This adds another challenge to the implementation of PGS inductors for CMOS distributed amplifier design.

Despite all these challenges, as will be seen later, PGS inductors have been used successfully in the design of an ultra-wideband CMOS distributed amplifier, achieving not only improved gain and noise figure but also small die size, and demonstrating their usefulness for the design of wide-band CMOS RFICs.

3.4.3 Design of CMOS Distributed Amplifiers Using Patterned Ground Shield Inductors

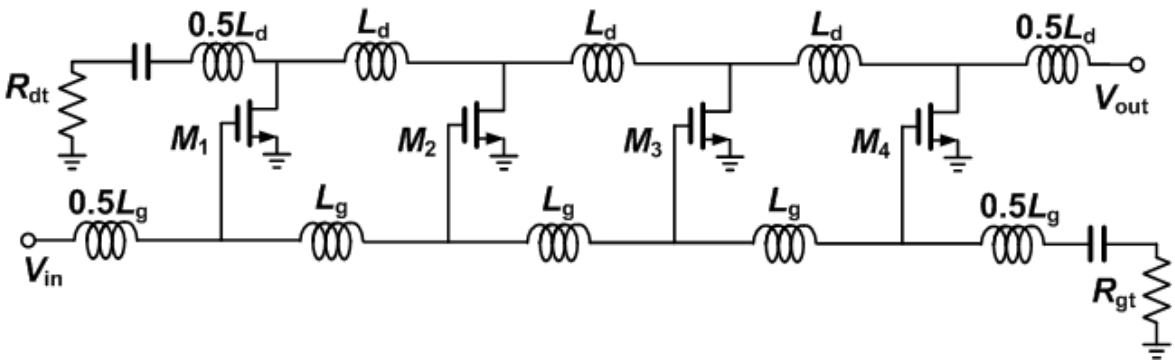


Fig. 3.17 Schematic of a four-stage distributed amplifier

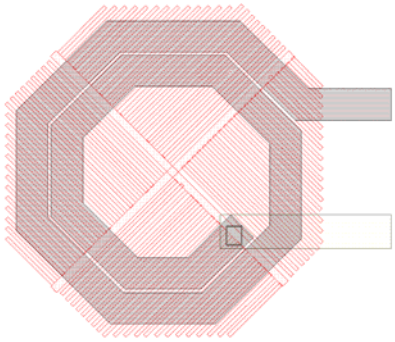
The design of CMOS distributed amplifiers starts from a trade-off between gain and bandwidth. For a given process, the maximum achievable gain will also be fixed for a desired bandwidth. Our distributed amplifier design was carried out in the TSMC's standard low-cost 0.25-μm CMOS process [27]. The desired band width was chosen to be DC-11GHz for possible applications in ultra-wideband (UWB) wireless communications.

Fig. 3.17 shows the distributed amplifier's schematic. Four stages, with each transistor having a width of 160 μm, are used in the design, considering trade-off

between gain, bandwidth and chip area. The characteristic impedance of the two artificial transmission lines at the input and output ports and their corresponding terminating resistors R_{dt} and R_{gt} were designed to be 50 Ohms. To obtain the desired bandwidth and satisfy the input and output matching conditions, the inductances (L_g and L_d) were estimated as 1 nH and 0.85 nH, respectively, after calculations and optimization, to accommodate the parasitic capacitances of the employed CMOS transistors. However, in order to make the design simple, L_d was also chosen as 1 nH. Calculations show that using this increased value for L_d boosts the gain a little bit (0.9 dB), while causing only a small degradation at the output matching, which is still acceptable.

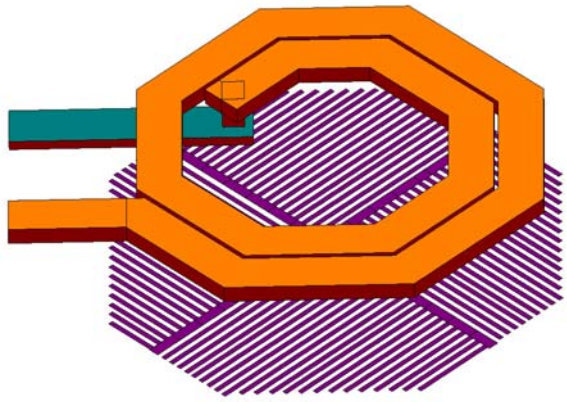
It is known that the inductance, Q, and resonant frequency f_{rec}, of a spiral inductor are determined by its shape, size, number of turns, and strip width and spacing [30]. When a PGS is added into the inductor, its inductance will drop slightly as the frequency goes higher, while its resonant frequency will be reduced much lower than that of the inductor without PGS. Since it takes much longer time for EM simulators to calculate a PGS inductor, it would be convenient to design the spiral inductor without PGS first and then adding a PGS layer. In this design, an octagonal spiral inductor having 2 turns was chosen to obtain a relatively high Q and resonant frequency f_{rec}, while still maintaining a compact size. The PGS was then incorporated into the inductor. The top-most and next metal layers are used for the spiral strip and under-path, respectively, while the lowest metal layer is used for the PGS. To make sure this inductor works well as an inductor across the designed frequency range, it is also desired

to have a resonant frequency higher than the cut-off frequency of the distributed amplifier, which is 14 GHz. Several inductors with different dimensions have been designed simulated and modeled in IE3D [28] to extract their inductance and resonant frequencies. Finally, an octagonal spiral inductor with PGS having a resonant frequency of 16.6 GHz was chosen for the design. Fig. 3.18 shows the layout of the PGS spiral inductor.



(a)

Fig. 3.18 PGS inductor designed for the distributed amplifier: (a) Layout of the PGS inductor designed for the distributed amplifier



(b)

Fig. 3.18 continued (b) 3D-view of the PGS inductor designed for the distributed amplifier

The Q's of the inductors with and without PGS were extracted from the calculated results and are shown in Fig 3.19. The result shows that the Q of the PGS inductor is much higher than that of the inductor without PGS from 5 to 15 GHz, beyond which the substrate loss due to magnetic fields induced within the silicon substrate plays a dominant role in the overall performance. Although the Q decreases quickly after its peak at around 8 GHz, it still maintains a higher value than that of the inductor without PGS until 15 GHz, which is higher than the designed amplifier's upper frequency of 11 GHz. This makes it possible that the distributed amplifier implementing the PGS inductors can work well despite the inductors' large Q-variation. The series inductance and shunt capacitance of the Π-network lumped-element models of the inductors with

and without PGS are plotted in Fig. 3.20. The results show that the inductance of the PGS inductor at 15 GHz drops around 20% (0.80 nH) from that at 1 GHz, while the inductor without PGS shows an almost constant inductance. This variation of inductance may cause potential problems in some wideband circuit designs. A simulation was then made with ideal inductors to evaluate the effect of this change on the performance of the distributed amplifier. The simulated results of the distributed amplifier's gain and input return loss are shown in Fig. 3.21.

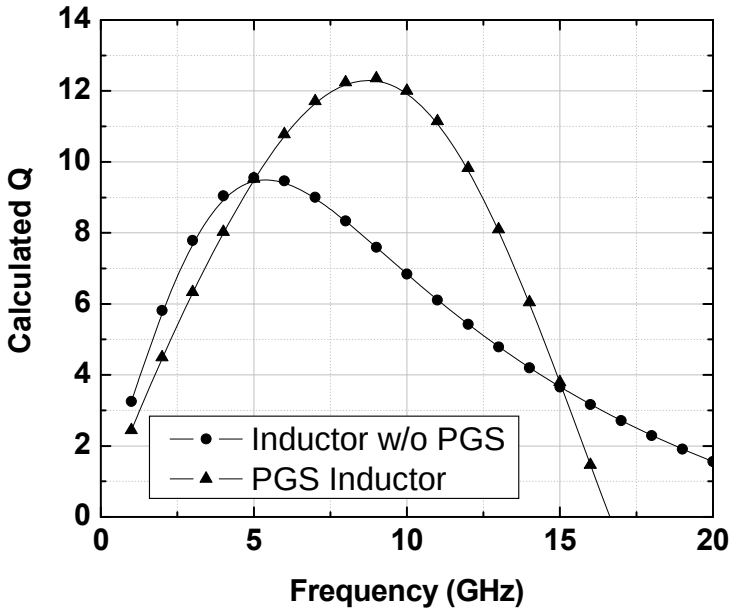


Fig.3.19 Calculated Q of the on-chip spiral inductors with and without PGS

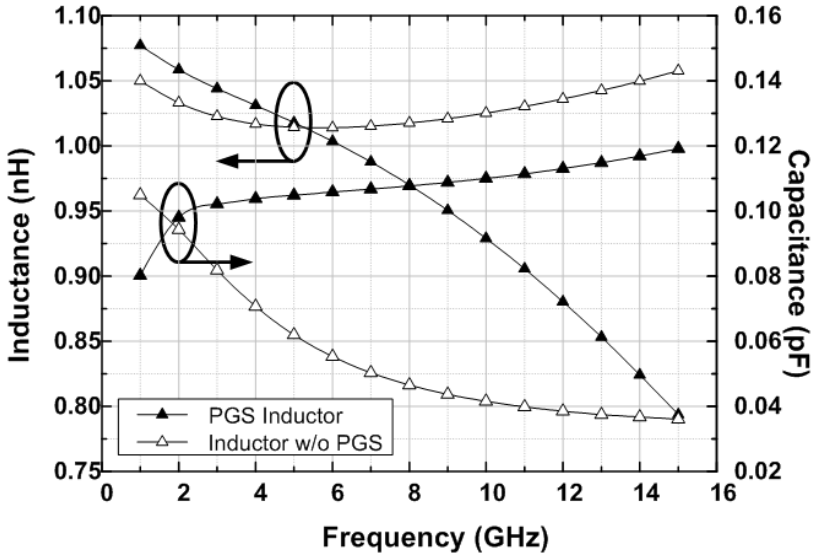


Fig.3.20 Calculated PI equivalent network serious Inductance and shunt capacitance of the on-chip inductors with PGS and without PGS

The results show that the change of inductance from 1.075 nH to 0.8 nH across 1-15 GHz only has a slight effect on the amplifier's gain and input matching. As expected, the decrease in inductance lowers the gain and relaxes the bandwidth a little bit. These resultant gain and bandwidth, however, are tolerable in the design.

Four more inductors, each having an inductance of 500pH, are needed in the design. Since it is easy to get high Q for conventional on-chip inductors with such a small inductance, one-turn rectangular inductors without PGS are used.

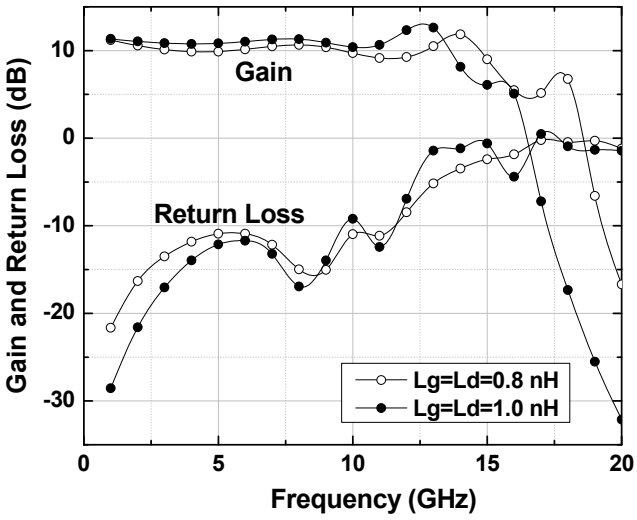


Fig.3.21 Simulated gain and input return loss of the distributed amplifier with different values for ideal inductors

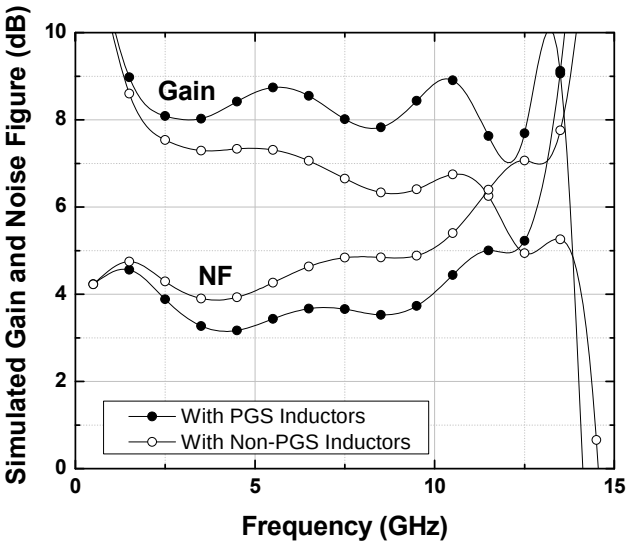


Fig.3.22 Calculated gain and noise figure of the distributed amplifier using inductors with and without PGS

The calculated S-parameters of all the inductors from IE3D were imported into the Agilent Advanced Design System [29] and simulated along with other circuit elements as a whole amplifier circuit. To show the effect of the PGS inductors on the over-all performance of the distributed amplifier, simulation with inductors having no PGS was also made. Fig. 3.22 shows the calculated gain and noise figure of the distributed amplifier using PGS and non-PGS inductors. Overall, the distributed amplifier with PGS inductors has a higher and flatter gain as well as a lower and less varying noise figure than those with non-PGS inductors. Particularly, the gain and noise figure are improved between 0-2.1 dB and 0-1.3 dB, respectively, across 1-14 GHz for the amplifier with PGS inductors. In general, the improvement is more significant at high frequencies due to the improved Q of the PGS inductors at these frequencies, as expected.

As shown in Fig. 3.20, the equivalent shunt capacitance of the PGS inductor is much higher than that of the inductor without PGS. However, Fig. 3.22 shows that the bandwidth of the distributed amplifier with PGS inductors is not affected much by the increase in parasitic capacitance. Both of the two amplifiers have almost the same cut-off frequencies at around 14 GHz.

The four-stage distributed amplifier using PGS inductors has been designed and fabricated in the low-cost standard TSMC 0.25-μm CMOS technology. The distributed amplifier uses six PGS inductors, each having a diameter of 220 μm and strip width of 30 μm. To take advantage of the inherent isolation between PGS inductors created by the shield layer, adjacent PGS inductors were placed as close as 30 μm, which is the

same as the strip width of each PGS inductors. This close spacing has never been achieved in any CMOS distributed amplifier design. To verify the performance the distributed amplifier having such close-distance PGS inductors, the whole passive structures at the input and output lines, each including three octagonal PGS inductors and two rectangular non-PGS inductors, were modeled as two 6-port structures and calculated using IE3D. Simulations, made in ADS based on these calculated results, show that the distributed amplifier works fine. Fig. 3.26 shows the microphotograph of the designed distributed amplifier. The circuit's die area is only 1.2×0.8 mm^2.

3.4.4 Measurement Results

The fabricated CMOS distributed amplifier was measured using on-wafer probes. Two bias-tees were used to bias the circuit at both input and output. Figs. 3.23 and 3.24 show the measured and calculated S-parameters. The amplifier exhibits a measured gain of around 7 dB with a little fluctuation, input and output return losses higher than 10 dB, and reverse isolation below 15 dB from DC-11 GHz. These results agree reasonably well with those calculated, except the bandwidth of the measured S_{21} is 2 GHz lower than that of the simulated one. This discrepancy may be caused by unwanted parasitic capacitances in the layout, which were not taken into account in the simulation. The simulated and measured S_{21} have a small peak before the cut-off frequency, which is due to a pair of poles formed by some inductors and capacitors in the circuit located just before the cut-off frequency of the artificial transmission lines.

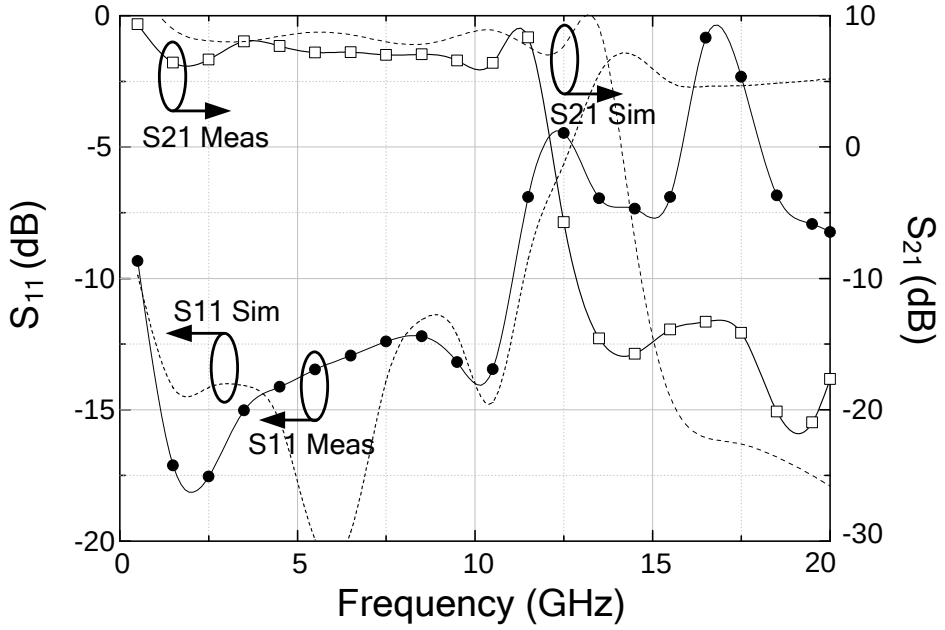


Fig.3.23 Simulated and measured input reflection coefficient (S_{11}) and power gain (S_{21})

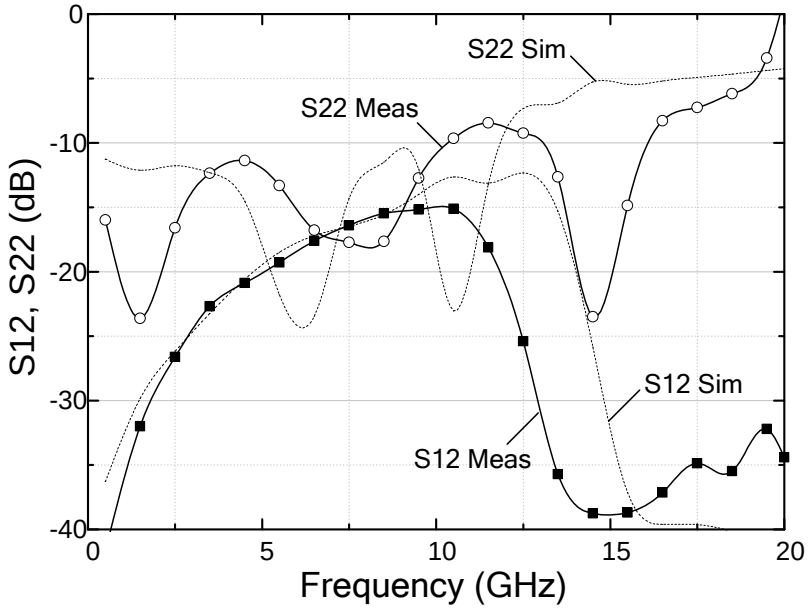


Fig.3.24 Simulated and measured output reflection coefficient (S_{22}) and reverse isolation (S_{12})

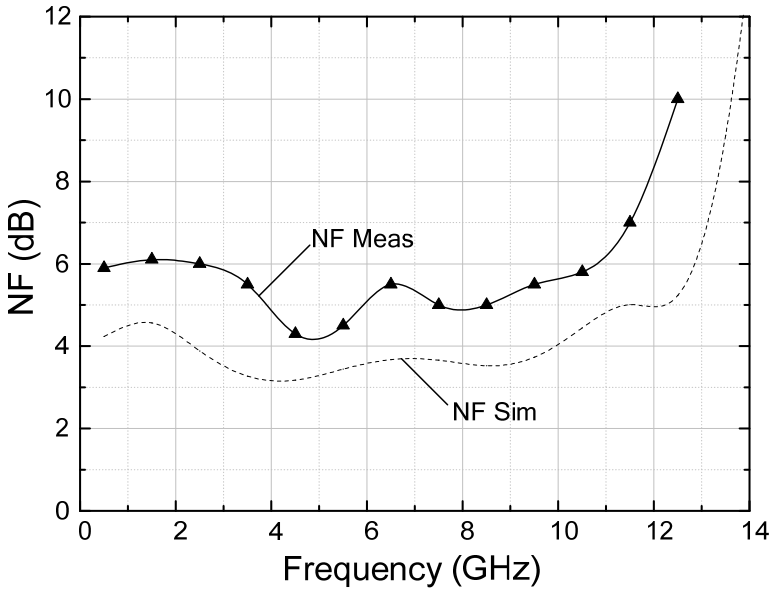


Fig.3.25 Simulated and measured noise figure

Fig. 3.25 shows the noise figure of this distributed amplifier. It has a measured noise figure of 4.1-6.1dB from 0.5 to 11 GHz. The measured power consumption is 78 mW using a voltage supply of 2 V. The chip's microphotograph is shown in fig. 3.26.

Table 3.1 compares performance of the new CMOS distributed amplifier with those of recently published CMOS distributed amplifiers. The proposed distributed amplifier with PGS inductors demonstrates the highest gain and smallest die area among the distributed amplifiers reported in 0.25 μm CMOS processes. It even has a comparable gain and smaller die area as compared to the best reported CMOS distributed amplifiers in 0.18 μm processes.

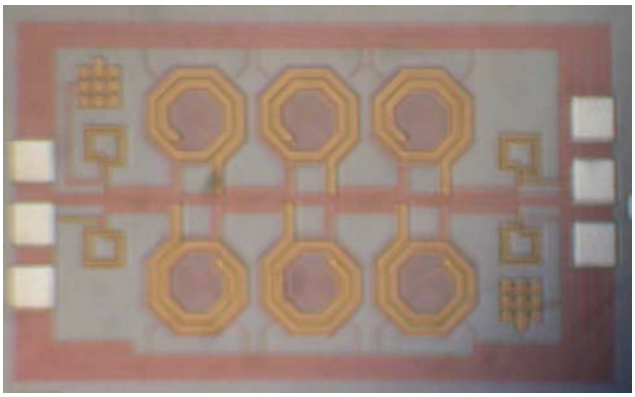


Fig. 3.26 Microphotograph of the proposed four stage distributed amplifier with PGS inductors

Table 3.1 Performance summary of the proposed CMOS distributed amplifier

Reference	Technology	Input Matching (dB)	Avg. Gain (dB)	Bandwidth (GHz)	Die Area (mm^2)	Number of Inductive Elements
[20]	0.6-µm CMOS	<-7	6.1	0.5-5.5	0.8×1.4	10
[18]	0.25-µm CMOS	<-10	6	0-12	N/A	14
[36]	0.25-µm CMOS	<-10	5	1-11.4	N/A	6
[37]	0.18-µm CMOS	<-9	7.3	0-22	1.0×1.6	8
[38]	0.18-µm CMOS	<-20	10	0-11	0.9×1.6	11
This Work	0.25-µm CMOS	<-10	7.2	0-11	0.8×1.2	10

3.4.5 Conclusion

A compact CMOS distributed amplifier utilizing PGS on-chip spiral inductors has been developed in the low-cost TSMC 0.25-μm CMOS process. The increased isolation obtained with the PGS inductors makes it possible for the inductors to be placed very close to each other, resulting in significant reduction of circuit area. With the high Q achieved by the PGS inductors, the distributed amplifier also exhibits good performance with a relatively flat gain of 7 dB and input and output return losses of higher than 10 dB from DC-11 GHz, which could possibly be the best performance that can be achieved in standard low-cost 0.25-μm CMOS processes. The developed CMOS distributed amplifier demonstrates a useful approach in designing compact, high-performance wide-band CMOS distributed amplifiers as well as other broadband CMOS RFICs by using on-chip PGS inductors, particularly for those containing many inductors.

3.5 Low-Power-Consumption and High-Gain CMOS Distributed Amplifiers Using Cascade of Inductively Coupled Common-Source Gain Cells for UWB Systems

3.5.1 Motivation

Distributed amplifiers are attractive candidates for UWB systems due to its inherently ultra-wide bandwidth. A major drawback of distributed amplifiers for UWB applications is their large dc power consumption, severely limiting their usage in wireless portable devices. This is due to the fact that several parallel transistors, with each transistor draining current from the source, are needed to form the required artificial transmission lines and to achieve a reasonable gain on a 50-ohm load. Recently, the design of low-power distributed amplifier in CMOS has been addressed [39-41]. Most of these designs are based on the gain-cell topology presented in [19-20] and do not provide enough gain and bandwidth at very low power consumption.

In this part, we report a new CMOS distributed amplifier having very low power consumption for UWB applications, particularly suitable for portable UWB wireless devices. Significant performance advantages of the low-power distributed amplifier design are demonstrated. The UWB distributed amplifier is fabricated using a standard TSMC 0.18-μm CMOS process [38]. It achieves the highest gain (in high-gain mode) and lowest power consumption (in low-power mode) ever reported across the UWB frequency range of 3.1-10.6 GHz. The measured noise figure is similar to the best published noise figure.

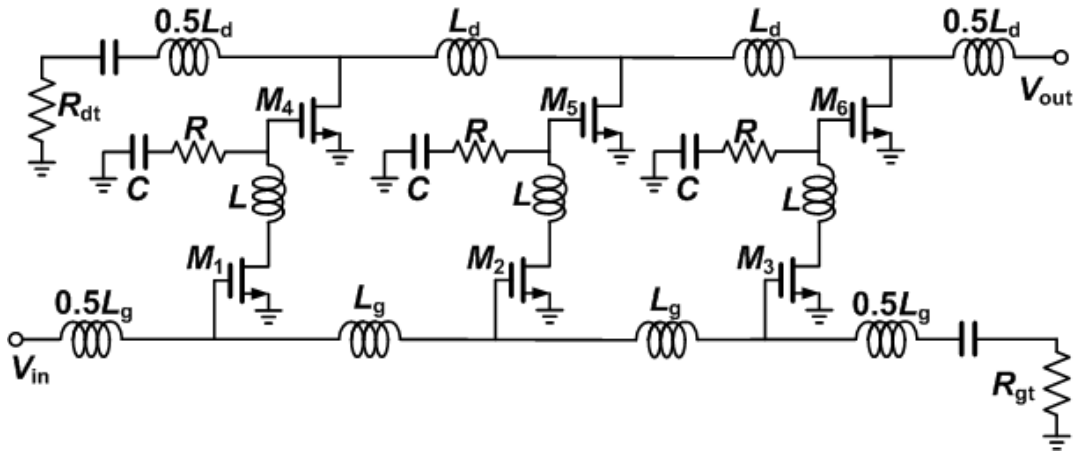


Fig.3.27 Simplified schematic of the new low-power distributed amplifier

3.5.2 Circuit Analysis

The major challenge in designing a low-power-consumption distributed amplifier is the trade-off between power consumption and gain. In order to lower the power consumption, each transistor has to be biased at a very low overdrive voltage. This, however, leads to insufficient gain for the whole amplifier. To address this issue, we propose a new distributed amplifier topology, as shown in Fig. 3.27. New gain cells, each consisting of two cascade common-source transistors with peaking inductor, are used. This new gain-cell configuration improves the gain significantly with similar power consumption or similar gain with substantially reduced power consumption, over the entire UWB band of 3.1-10.6 GHz, as compared to the conventional distributed amplifiers.

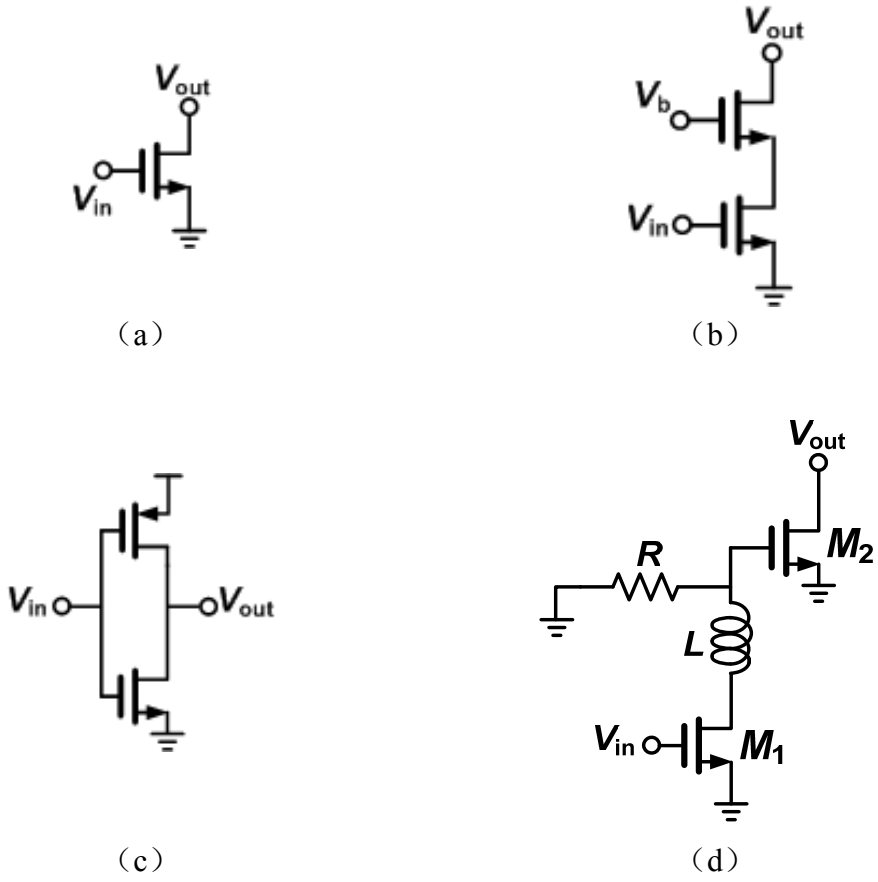


Fig. 3.28 Gain cell configurations used in CMOS distributed amplifiers: (a) Traditional common source gain cell (b) Cascode gain cell (c) Current reuse gain cell (d) Proposed cascade common-source gain cell

As it has been analyzed in 3.1, the gain can be increased by simply increasing the number of stages before it reaches a maximum number, as given in [23], limited by the increasing losses of the artificial transmission lines. This increase is obtained at the cost of larger die area and higher power consumption, which are not very desirable, particular for commercial CMOS-based portable devices. Apparently, the transconductance of each gain cell is the most important issue for the gain. It should be noted that the intrinsic gain, which is defined as g_m times R_{out}, of each gain cell is no longer important, because each

gain cell in the distributed amplifier is driving a small resistive load, which is 50-Ohm. Furthermore, these gain cells can not take advantages of their large output impedance for gain enhancement because of the small resistive load at output. The capability to provide sufficiently large current at the output of the gain cells will determine the gain of the distributed amplifier.

Figs. 3.28(a)-(c) show several gain-cell configurations used in CMOS distributed amplifiers [15-24, 39-41]. Fig. 3.28(a) is a common-source stage, which has been used in distributed amplifier designs for a very long time. It provides a decent gain and very large bandwidth. Fig. 3.28(b) is a cascode structure used to enhance reverse isolation. This structure does not provide significantly higher g_m than a single common-source transistor, and thus does not have considerable gain advantage over that in Fig. 3.28(a). In Fig. 3.28(c), a current reuse gain cell is formed by NMOS and PMOS transistors. This configuration is supposed to have higher transconductance at proper bias voltages and transistor dimensions. However, because of the mobility difference of NMOS and PMOS devices, the bias and dimensions for this structure are very difficult to be determined. Fig. 3.28(d) shows the proposed cascade common-source gain cell. Two common-source transistors are connected with each other through a peaking inductor. A resistor is connected to the gate of the second transistor. Passive inductors are used, instead of active inductors, to avoid possible variation of inductance and increase in noise over extremely wide bandwidths such as the UWB band of 3.1-10.6 GHz. As will be seen, this new structure enhances the transconductance significantly and hence the amplifier's gain.

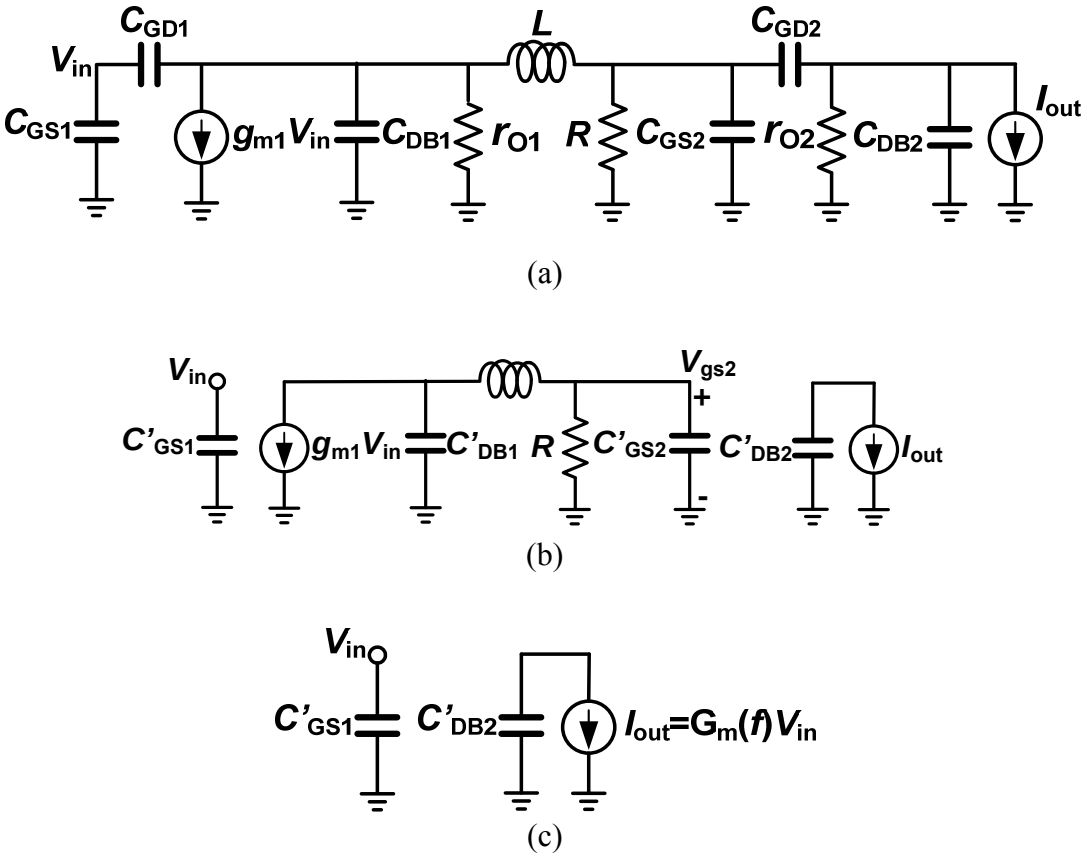


Fig. 3.29 Small-signal model for gain analysis: (a) Small-signal model of the proposed cascade gain cell (b) Simplified small-signal model (c) Equivalent-circuit model for the gain and bandwidth analysis

Fig. 3.29(a) shows a small-signal equivalent circuit of the new cascade common-source gain cell in fig 3.28(d). C_{GSi}, C_{DBi}, and C_{GDi} (i=1, 2) are the respective gate-to-source, drain-to-bulk, and gate-to-drain capacitances of the NMOS transistor with M_1 (i=1) and M_2 (i=2) in each gain cell. g_{m1}, g_{m2} and r_{O1}, r_{O2} are the transconductances and output resistances of M_1 and M_2, respectively. R and L are the resistance and inductance used in each gain cell, as shown in Fig. 3.28(d), respectively. Typically, r_{O1} and r_{O2} are

relatively large and therefore can be neglected. Neglecting r_{O1} and r_{O2} and combining C_{GD1}, C_{GD2} with C_{GS1}, C_{GS2} and C_{DB1}, C_{DB2} to form C'_{GS} and C'_{DB}, which are the Miller equivalent capacitance observed at the gate and drain of the first transistor. The small signal model could be simplified and is shown in fig. 3.29(b). To analyze the gain of the proposed distributed amplifier, we only need to find out the transconductance of each gain cell, because the gain of the distributed amplifier is only a function of the transconductance of each gain cell. In the following analysis, we are going to find out the Gm in fig. 3.29(c) based on the small signal model in fig. 3.29(a).

The I_{out} in fig. 3.29(c) can be expressed as

$$I_{\text{out}}=g_{m2}V_{gs2} \tag{3.12}$$

where Vgs2, depict in fig.3.29 (b), is the gate-source voltage of M_2.

Since

$$V_{gs2}=I_{\text{L}}(R//\frac{1}{sC'_{\text{GS2}}})=g_{m1}V_{gs1}\frac{\frac{1}{sC'_{\text{DB1}}}}{\frac{1}{sC'_{\text{DB1}}}+sL+R//\frac{1}{sC'_{\text{GS2}}}}\cdot(R//\frac{1}{sC'_{\text{GS2}}} \tag{3.13}$$

We have

$$I_{out}=g_{m2}V_{gs2}=g_{m1}g_{m2}V_{gs1}\frac{\frac{1}{sC'_{\text{DB1}}}}{\frac{1}{sC'_{\text{DB1}}}+sL+R//\frac{1}{sC'_{\text{GS2}}}}\cdot(R//\frac{1}{sC'_{\text{GS2}}}) \tag{3.14}$$

Because

$$V_{gs1}=V_{in} \tag{3.15}$$

we can derive the transconductance as

$$G_m = \frac{\partial I_{out}}{\partial V_{in}} = g_{m1}g_{m2} \frac{R // \frac{1}{sC'_{GS2}}}{\frac{1}{sC'_{DB1}} + sL + R // \frac{1}{sC'_{GS2}}} \frac{1}{sC'_{DB1}} \tag{3.16}$$

Expand the right part in equation (3.16),

$$G_m = g_{m1}g_{m2} \frac{\frac{R \cdot \frac{1}{sC'_{GS2}}}{R + \frac{1}{sC'_{GS2}}}}{1 + s^2 LC'_{DB1} + \left(\frac{R \cdot \frac{1}{sC'_{GS2}}}{R + \frac{1}{sC'_{GS2}}}\right) \cdot sC'_{DB1}} \tag{3.17}$$

$$= g_{m1}g_{m2} \frac{R}{\left(1 + s^2 LC'_{DB1} + \frac{R}{sC'_{GS2}R + 1} \cdot sC'_{DB1}\right) \cdot \left(sC'_{GS2}R + 1\right)} \tag{3.18}$$

$$= g_{m1}g_{m2} \frac{R}{LC'_{DB1}C'_{GS2}Rs^3 + LC'_{DB1}s^2 + RC'_{DB1}s + RC'_{GS2}s + 1} \tag{3.19}$$

Usually, $C'_{DB1} << C'_{GS2}$, and so the transconductance expression can be further simplified as

$$G_m \approx g_{m1}g_{m2} \frac{R}{LC'_{DB1}C'_{GS2}Rs^3 + LC'_{DB1}s^2 + RC'_{GS2}s + 1} \tag{3.20}$$

$$= g_{m1}g_{m2} \frac{R}{(LC'_{DB1}s^2 + 1)(RC'_{GS2}s + 1)} \tag{3.21}$$

From Eq. (3.21), three poles can be observed. One pole is formed by the input capacitor of the upper transistor. This pole normally dominates the low-frequency response due to the fact that the value of the gate-to-source capacitance of a transistor is usually large. The other two complex conjugate poles are created by some inductance and output capacitance of the lower transistor. In practice, these two poles are located on the left *s*-plane instead of exactly on the complex axis because of the loss incurred in real circuits.

The presence of these two poles will boost up the transconductance of this gain cell at frequency

$$f_C = \frac{1}{\sqrt{LC'_{DB1}}} \tag{3.22}$$

which can also be considered as the cut-off frequency of the proposed gain cell's transconductance.

By properly choosing the inductance and resistance in the cascade common-source gain cell, a nearly constant transconductance can be obtained between the first-pole frequency and the cut-off frequency f_c in (3.22). Unlike a single-transistor gain cell, whose transconductance remains fairly constant over a particular frequency range, the proposed gain cell exhibits more frequency variation for its transconductance (see Fig. 3.28 for various designed cells). Considering this and the fact that the gain of distributed amplifiers is proportional to the transconductance of each gain cell, the cut-off frequency of a distributed amplifier employing the proposed gain cell is determined by the cut-off frequency of each gain cell's transconductance, instead of that of the artificial transmission lines at the input and output of the amplifier, provided that the former is lower than the latter. Fig. 3.30 shows the calculated transconductance of the new cascade gain cell and that of a single common-source transistor.

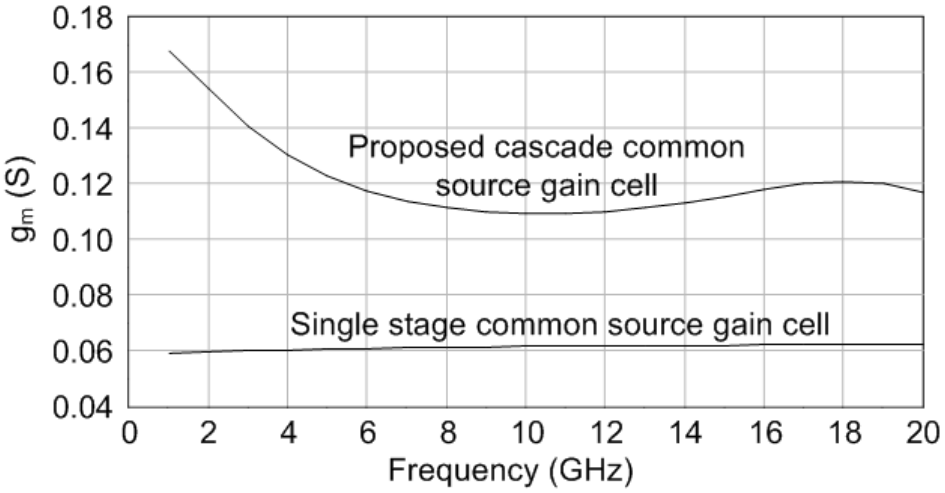


Fig.3.30 Calculated transconductance of the proposed gain cell and a common-source gain cell stage

Compared to the single common-source transistor, this cascade common-source gain cell provides a significantly higher transconductance, which is expected to lead to a significantly higher gain. Exploiting this resultant unique capability of providing high transconductance, the cascade common-source gain cells can be biased at a very low voltage to consume a very small amount of power, while still providing enough transconductance to obtain a decent gain for the entire amplifier.

The new distributed amplifier topology facilitates the enhancement of stability. The cascade structure used in each gain cell stage results in higher reverse isolation as compared to a single-transistor cell, while maintaining good input and output matching,

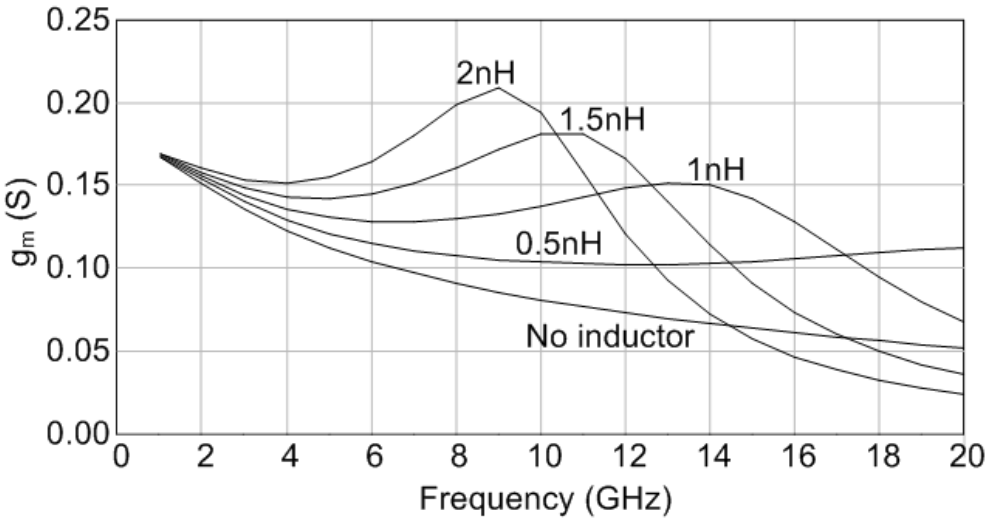


Fig.3.31 Calculated frequency response of the transconductance of the proposed gain cell for different values of inductance

which may help improve the stability of the distributed amplifier. Although the inductors used in the gain cells may resonate with the input gate capacitors of some transistors, as long as the negative resistance is lower than 80-Ohms, the circuit will remain stable, due to the facts that all the transistors are grounded at the source and an 80-ohm resistor is used in each gain cell. Our simulations of the designed distributed amplifier show that the stability factor *K* is greater than 1 across dc to 18 GHz, demonstrating its expected unconditional stability.

3.5.3 Circuit Design

The new distributed amplifier is designed and fabricated using the TSMC 0.18-μm CMOS process. The gate width of each transistor is optimized for gain and power consumption. The inductance L in each gain cell determines the bandwidth of the

distributed amplifier. The calculated frequency response with different values of inductance is shown in Fig. 3.31. 1 nH is chosen for the inductance to obtain a reasonably flat gain over the considered UWB frequency range of 3.1-10.6 GHz.

On-chip inductors are used for the inductive elements of the artificial transmission lines in the distributed amplifier. Very small inductance values are used in order to have high Q resulting from less eddy current loss in the silicon substrate. The full-wave EM simulator IE3D is used for simulations of all passive components including bends, interconnects, and spiral inductors. The two artificial transmission lines are terminated with 50-ohm resistors and ac-coupling capacitors to minimize reflections.

The new CMOS distributed amplifier design uses 3 stages to ensure a decent gain, reasonable die area and small power consumption. The designed amplifier has a chip size of 1.6×0.9 mm^2. Fig. 3.32 shows its microphotograph.

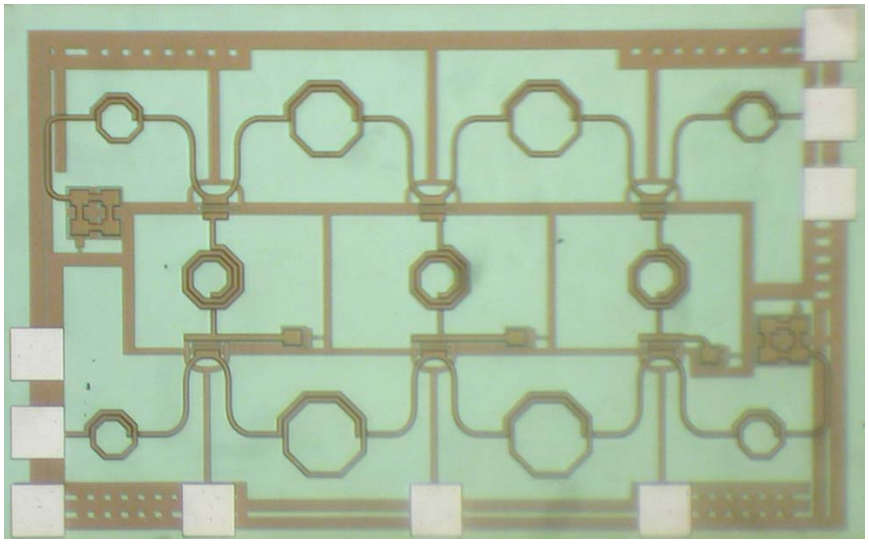


Fig.3.32 Microphotograph of the low power distributed LNA (1.6×0.9mm^2)

3.5.4 Measurement Results

The fabricated CMOS distributed amplifier was measured using on-wafer probes. Bias-tees and dc biasing probes were used to bias the circuit.

Fig. 3.33 shows the calculation and measurement results for the power gain and input return loss. The amplifier exhibits a measured gain of around 10 dB and input return loss less than 20 dB across the entire UWB of 3.1-10.6 GHz, which agree reasonable with those calculated. The power consumption was measured at 19.6 mW with the entire circuit biased at an extremely low voltage of 0.7V. Fig. 3.34 shows the calculated and measured gain and input return loss at a high-gain mode. As can be seen, the distributed amplifier demonstrates a high gain of around 16 dB and return loss below 20 dB, measured across the UWB 3.1-10.6-GHz range, with a power consumption of 100 mW. The measured and calculated results also agree fairly well. A very high gain near-dc is observed from both Figs. 3.33 and 3.34. This is due to the L, R and C network that appears between the two transistors in each gain cell, as expected from the simulations. The measured gain shows a lower cut-off frequency than that of simulation. This may be attributed to the parasitics resulting from the layout that were not taken into account in the simulations.

Fig. 3.35 shows the measured and simulated results for the isolation and return loss at the output. Both calculated and measured results show that there is only a very small difference between the high-gain mode and low-power mode. It is also noted that use of the new cascade gain cells results in high isolation of more than 30 dB for the distributed amplifier. The noise observed in the measured S_{11} and S_{22} data shown in Figs.

3.33-35 were due to calibration of the vector network analyzer. Nevertheless, multiple measurements for different chips have been performed and, despite this noise, the results are very consistent. The abnormal peak in the measured S_{22} near 6.5 GHz seen in Fig. 3.35 may be due to some unexpected parasitics at the output port of the fabricated amplifier.

The noise figure of the CMOS distributed amplifier at both high-gain and low-power modes has also been measured using the Agilent noise figure analyzer. The measured and simulated results are plotted in Fig. 3.36. The noise figure in the low-power mode is slightly higher than that in the high-gain mode both in simulation and measurement. Since sufficient gain is provided by the lower transistor in each gain cell, the new distributed amplifier with cascade gain cell configuration does not give higher noise figure than that of traditional distributed amplifiers.

The IIP3 was also measured on the proposed distributed amplifier. Two input tones with 10 MHz adjacent to each other were combined by a power combiner and input into the amplifier. In the output spectrum, two fundamental tones and two IM3 products can be observed. Fig. 3.37 shows the output spectrum when IIP3 was measured at high gain mode and 6GHz. Two fundamental tones located at 5.99GHz and 6.01GHz with a power of -12dBm. Two IM3 products located at 5.97GHz and 6.03GHz with the power of -61dBm. The IIP3 of the proposed distributed amplifier was measurement at both high gain and low power mode from 2-10GHz. The results are plotted in fig. 3.38, shows the IIP3 of 0-2dBm at high gain mode and -9.5- -3.5dBm at low power mode.

Table 3.2 compares performance of the new CMOS distributed amplifier with those of recently published CMOS distributed amplifiers. The new distributed amplifier demonstrates both the highest gain (in high-gain mode) and lowest power consumption (in low-power mode) with gain comparable to the best reported gain across the UWB frequency range of 3.1-10.6 GHz. The measured noise figure is also similar to the best published noise figure.

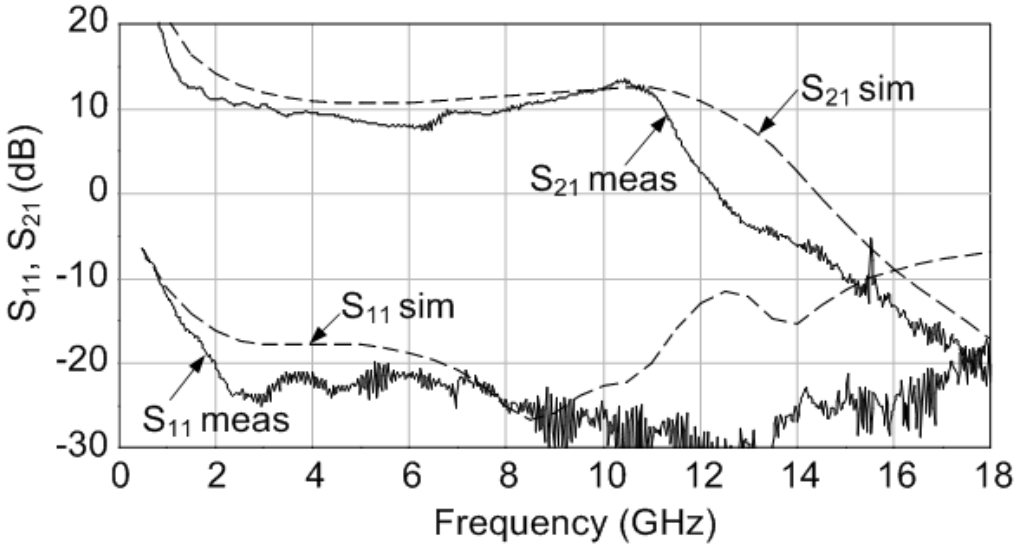


Fig.3.33 Measured and simulated power gain (S_{21}) and input return loss (S_{11}) at low power consumption mode (measured P_{dc}=19.6mW)

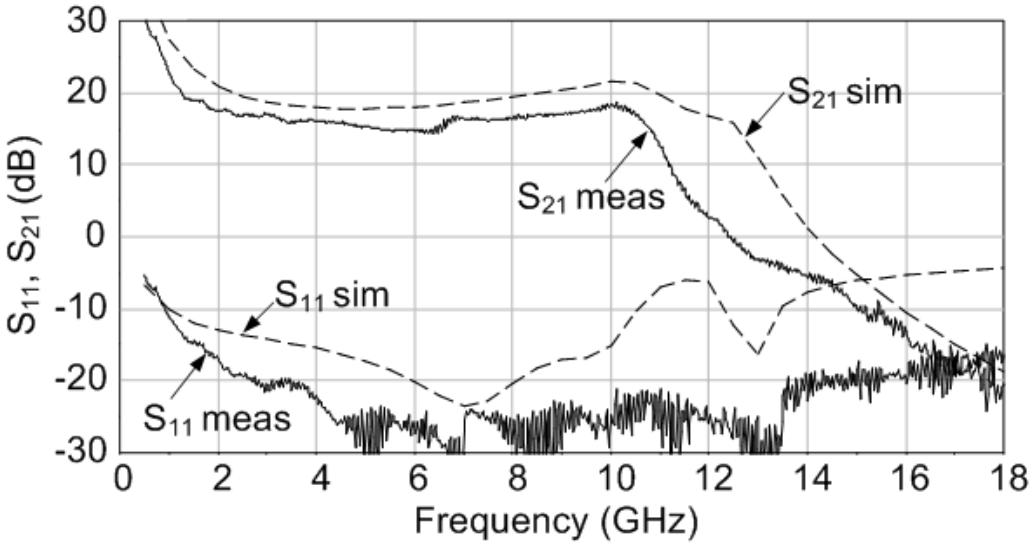


Fig. 3.34 Measured and simulated power gain and input return loss at high gain mode (measured P_{dc}=100mW)

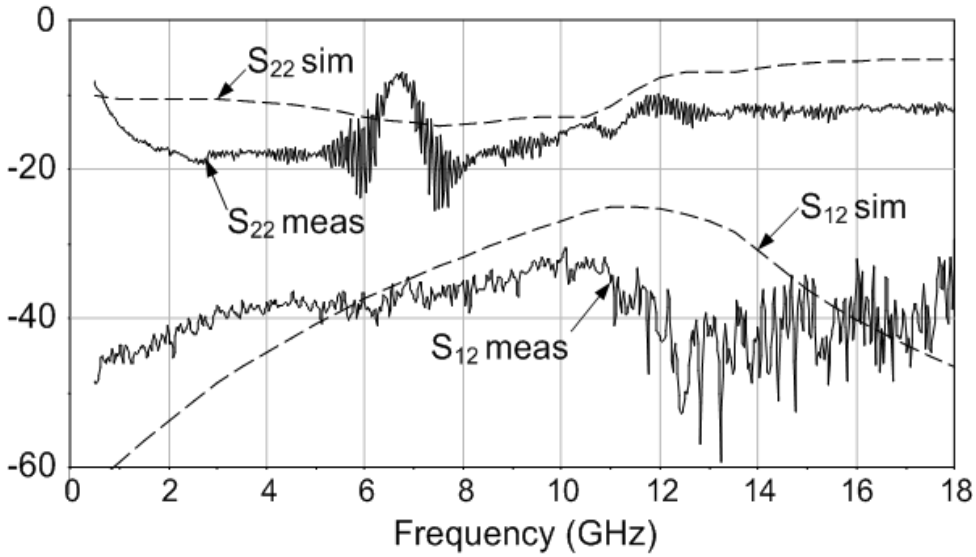


Fig.3.35 Measured and simulated output return loss (S_{22}) and isolation (S_{12})

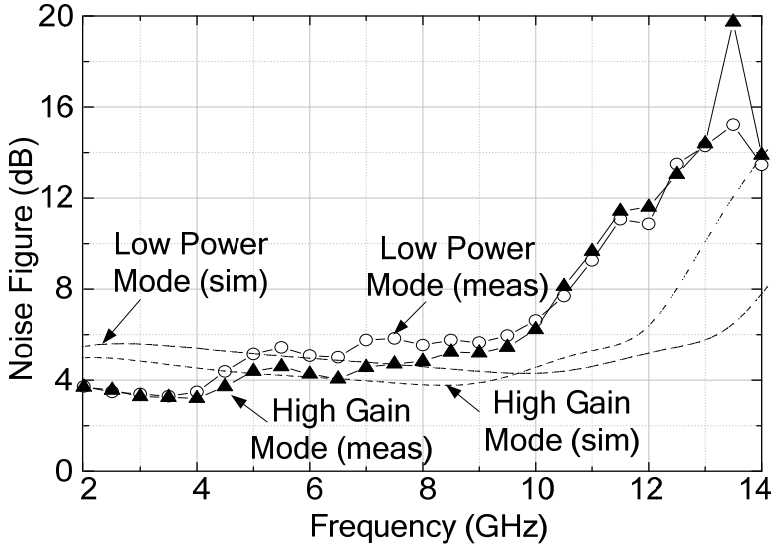


Fig. 3.36 Measured and simulated noise figure at high gain and low power modes

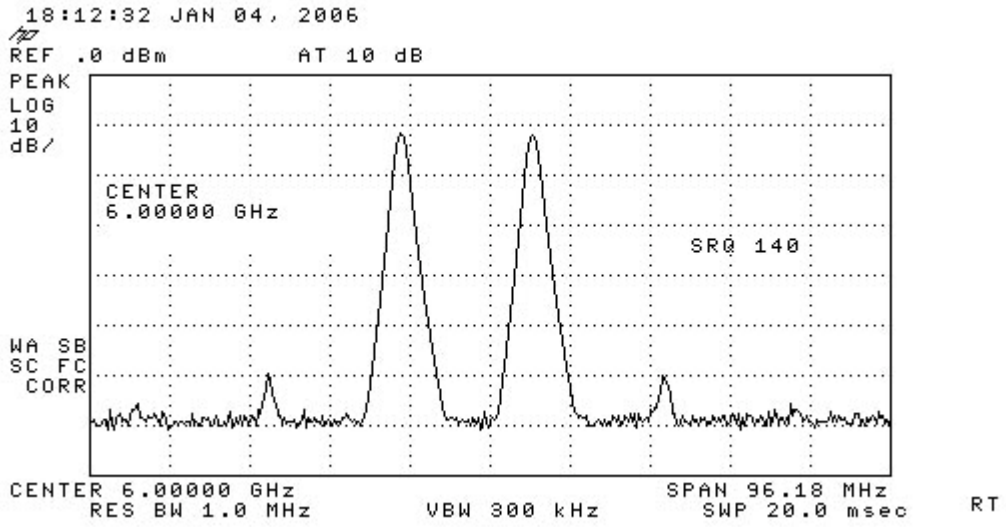


Fig.3.37 Output spectrum of the proposed distributed amplifier with input tones at 5.99GHz and 6.01GHz

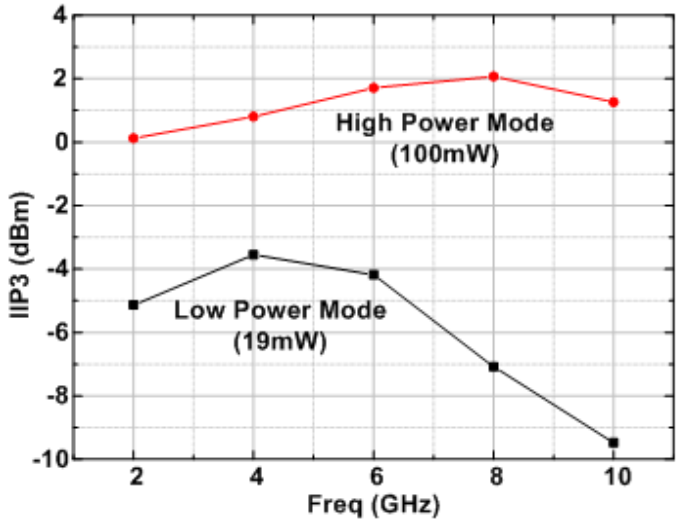


Fig. 3.38 Measured IIP3 of the distributed amplifier at both high gain and low power mode

Table 3.2 Performance summary of the proposed CMOS distributed amplifier

Reference	Technology	Input Matching (dB)	Avg. Gain (dB)	Bandwidth (GHz)	NF (dB)	Die Area (mm^2)	Power Consumption (mW)
[31]	0.6μm CMOS	<-7	6.1	0.5-5.5	5.4-8.2	1.4×0.8	83.4
[32]	0.6μm CMOS	<-10	5.5	0.5-8.5	8.7-13	1.3×2.2	216
[19]	0.18μm CMOS	<-9	7.3	0-22	4.3-6.1	1.0×1.6	52
[20]	0.18μm CMOS	<-13	10.6	0-14	3.4-5.3	0.9×1.5	52
[17]	0.18μm CMOS	<-11	6	1-27	6	0.9×1.8	68.1
[22]	0.18μm CMOS	<-10	4	39	N/A	1.1×3	140
[18]	0.25μm CMOS	<-10	6	0-12	N/A	1×3	120
[39]	0.18μm CMOS	<-10	5.2	0-8.5	4.7-6.1	0.7×1.2	23
This Work	0.18μm CMOS	<-20	10	0-11	3.3-6.1	0.9×1.6	19.6
			16		3.2-6		100

3.5.5 Conclusion

A new low power-consumption design approach along with its analysis for CMOS distributed amplifiers has been presented. The new design employs cascade of common-source gain cells with peaking inductance to provide substantially enhanced transconductance and gain over the entire UWB frequency of 3.1-10.6 GHz. The new 0.18-μm CMOS distributed amplifier implementing these gain cells achieves the lowest power consumption, with decent gain comparable to the best gain reported, over the entire UWB band, good input match, and good noise figure similar to the best published noise figure. The new CMOS distributed amplifier also exhibits the highest gain ever reported across the UWB range with good noise figure when operated in the high-gain mode. The performance confirms the suitability of the developed CMOS amplifier for UWB systems.

4. ANALYSIS AND DESIGN OF A 0.18-µm CMOS RESISTIVE SHUNT FEEDBACK LOW-NOISE AMPLIFIER FOR 3.1-10.6 GHz UWB RECEIVERS

CMOS distributed amplifiers have been discussed and investigated as an attractive candidate for the low noise amplifiers of UWB systems. However, the distributed amplifiers also have their drawbacks, such as high power-consumptions and large chip-area. Although both the power consumption and chip area can be reduced, these two problems cannot be eliminated.

In this section, a 0.18-µm CMOS low-noise amplifier (LNA) employing resistive shunt feedback has been designed to operate over the entire ultra-wideband (UWB) frequency range of 3.1-10.6 GHz. The UWB LNA achieves a measurement power gain of 7-10 dB, a minimum input matching of -8dB, a noise figure from 3.9-6.6 dB, and an IIP3 of -8- -2dBm, while consuming only 9mW over 3-10 GHz. The design uses only two on-chip inductors, one of which could be replaced by a bonding wire. The gain, noise figure, and matching of the amplifier are also analyzed. With its simple design, miniature size, and competitive performance, this LNA is expected to be valuable for many wireless CMOS UWB receivers.

4.1 Motivation

The design of the LNA is one of the biggest challenges in a UWB receiver system. It demands not only sufficient gain and low noise figure, but also good

matching, over the entire UWB frequency range from 3.1-10.6 GHz. Moreover, power consumption and linearity are two critical issues that need to be considered in the design, as the former may limit the usage of UWB technology in portable devices and the latter restricts the ability to handle interferences.

Several solutions of UWB LNA design in CMOS have been reported in literatures. The distributed amplifiers can easily provide extremely wide bandwidth up to 40 GHz and a relatively flat gain, by absorbing the parasitic capacitance of the transistors into the two artificial transmission lines at both input and output. Many CMOS distributed amplifiers have been designed and published. While distributed amplifiers are attractive considering their extremely wide bandwidths, several drawbacks, however, hinder their usage as LNA in UWB systems, particularly those implemented in CMOS processes. Firstly, many inductors or transmission lines need to be used as inductive elements to form the artificial transmission lines required for distributed amplifiers, leading to large die areas and hence increasing the cost of UWB systems. Secondly, distributed amplifiers normally have very high power consumptions due to their topology that employs many MOSFETs. Although efforts have been done to reduce the power consumptions of CMOS distributed amplifier [38], the current consumption is still relatively high. Thirdly, distributed amplifiers are normally designed to match the input and output ports to 50 Ohms simultaneously. This, while facilitating the measurement and typical integration with other 50-Ohm components in a system, is not suitable to be co-designed with other stages of a receiver in order to optimize the entire receiver for optimum performance. Finally, despite their good linearity, distributed

amplifiers normally have high noise figure and, due to the distributed topology, it is very difficult to optimize their noise figure, particularly while still maintaining a decent gain.

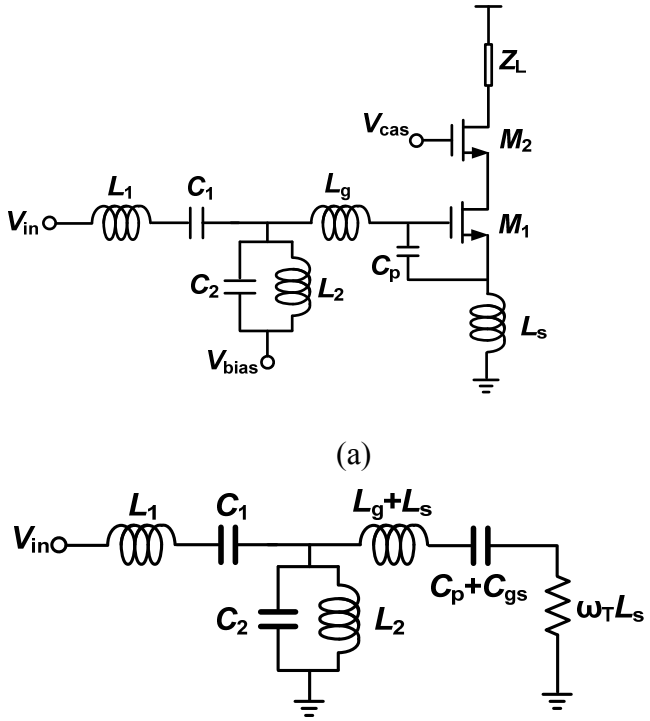


Fig. 4.1 UWB LNA employs filter design techniques: (a) Schematic of the UWB LNA implementing Chebyshev filter as input matching network (b) Schematic of the equivalent input matching network

In [44], a new CMOS LNA was developed for UWB receivers. This UWB LNA, depicted in fig. 4.1, employs filter design techniques, has a maximum gain of 10.4 dB over 2.4-9.5 GHz, while consuming only 9 mW. Due to its simplicity, low power consumption and ease for integration, it has been used in several UWB receiver front-ends [45-46]. This topology, however, uses too many inductors (total five in the reported

design), and hence consuming a relatively large chip area. More importantly, three of the five inductors are located at the gate of the transistor in the input stage, resulting in high noise figure at high frequencies. The reported measured noise figure is more than 6 and 8 dB at 8 and 10 GHz, respectively.

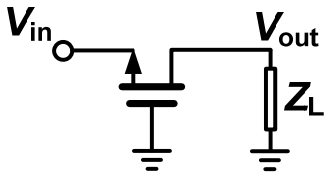


Fig. 4.2 Schematic of a simple common-gate amplifier

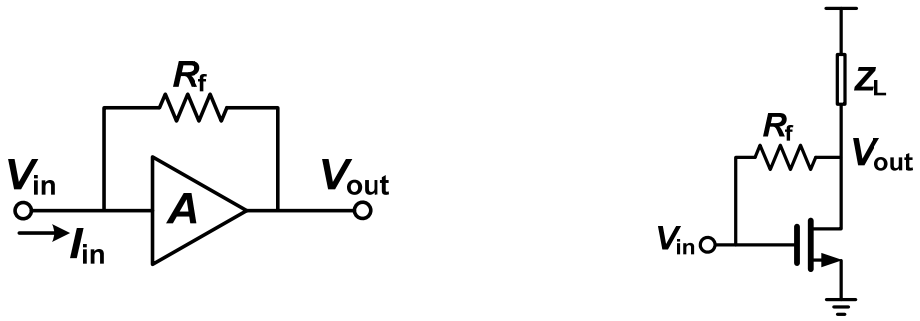
Common-gate configuration can easily provide a very wideband input matching. As show in fig.4.2, the input impedance of a common-gate amplifier can be estimated as $1/g_m$. Therefore, if the transistor is properly biased to produce a low transconductance – for example, g_m=20 mS – good input matching can be achieved. However, low transconductance such as this normally leads to a low gain. Also, the noise figure F is limited by [10]

$$F > 1 + \frac{\gamma}{\alpha R_S g_m} = 1 + \frac{\gamma}{\alpha} \tag{4.1}$$

where γ is the MOS transistor's coefficient of channel thermal noise and α is defined as the ratio of the transconductance g_m and the zero-bias drain conductance g_{d0}.

Several UWB LNA's with multiple stages were recently reported [46-47]. Each of these stages only provides gain over a frequency range of 2-3 GHz, enabling the gain

of the whole LNA's to cover the entire UWB frequency band of 3.1-10.6 GHz. In these designs, the wideband input and output matching are performed by the first and last stages. These amplifiers can provide high gain up to 15 dB and low noise figure around 3 dB over the UWB band. However, the use of multiples stages increases the power consumptions and limits the amplifiers' linearity.



(a) (b)

Fig. 4.3 Resistive shunt feedback amplifiers: (a) Schematic resistive feedback amplifier (b) CMOS transistor with shunt resistive feedback configuration

Resistive shunt feedback is a conventional approach in designing wideband amplifiers. Fig. 4.3(a) shows simple schematics of a resistive shunt feedback amplifier. The input impedance of the amplifier shown in Fig. 4.3 (b) can be estimated

$$Z_{in} = \frac{v_{in}}{i_{in}} = \frac{v_{in}}{\frac{v_{in} - v_{out}}{R_f}} = \frac{R_f}{1 - \frac{v_{out}}{v_{in}}} = \frac{R_f}{1 + |A|} \tag{4.2}$$

As seen in (4.2), with properly chosen values for the gain A and feedback resistance R_f, Z_{in} can be theoretically made to be around 50-Ohms or any other impedance needed for matching. Unfortunately, in practice, the problem is more complicated, especially at RF frequencies. Since the gain of the amplifier is a function of the feedback resistance, load

impedance, and frequency, (4.2) can thus only give an approximation for Z_{in} valid at low frequencies. Although some CMOS UWB LNA's using the shunt resistive feedback technique have been designed [48-50], none of them has good input matching and gain over the entire UWB bandwidth of 3.1-10.6 GHz. Moreover, it was indicated that the resistive shunt feedback is not feasible for LNA's operating over the entire UWB range. As will be seen, we demonstrate that, using a simple resistive feedback technique, we have successfully designed a CMOS UWB LNA with decent gain and noise figure across 3.1-10.6 GHz.

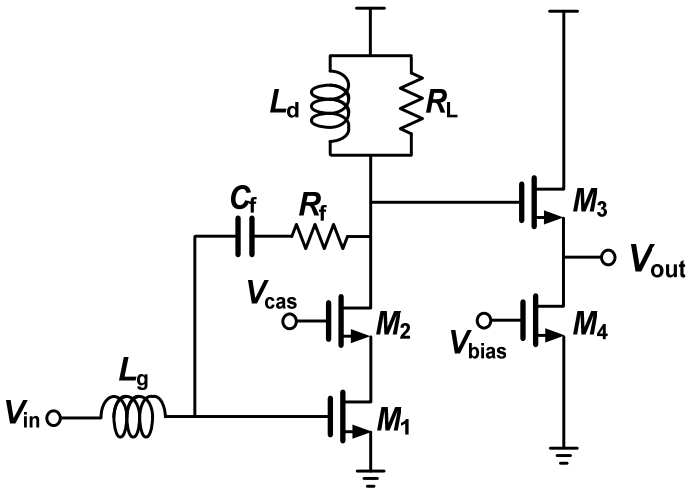
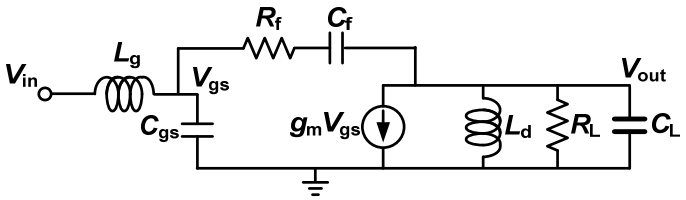


Fig. 4.4 Schematic of proposed UWB LNA with resistive shunt feedback technique

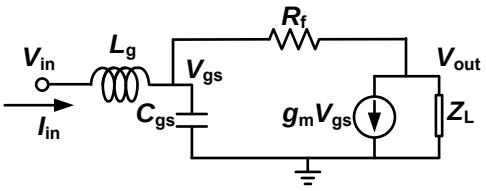
4.2 Circuit Analysis

Fig. 4.4 shows the schematic of the proposed CMOS UWB LNA. As can be seen, this low noise amplifier topology is very simple. This simplicity makes it ideally suited for low-cost CMOS UWB applications. The first stage has two transistors connected in

cascode with a resistive shunt feedback. In this stage, R_f is the feedback resistor, C_f is the blocking capacitor, and L_g is the inductor connecting the gate of the transistor M_1 to the input of the amplifier for input matching purpose. This stage also contains a loading element formed by a resistor parallel with an inductor. This loading element in the feedback amplifier is important because the amplifier's input impedance also depends on it. The second stage is a source follower, which primarily contributes to the output matching and provides a sufficient current to drive a 50-Ohm load. In the following, the proposed amplifier will be analyzed for its input and output matching, gain, and noise figure.



(a)



(b)

Fig. 4.5 Small Signal model for proposed UWB LNA

4.2.1 Input Matching

To analyze the input matching of the proposed UWB LNA, a small-signal model for the first stage, which primarily affects the input matching, as shown in Fig. 4.5(a), is used. C_L is the load capacitance representing the sum of the total parasitic capacitance at the output node of the first stage and the input capacitance of the second stage. L_d and R_L constitute the parallel load at the drain of M_2. g_m is the transconductance of M_1. The gate-drain capacitance C_{gd1} of M_1 and the small-signal resistance between the source of M_1 and the drain of M_2, r_{ds12}, are not considered in this small signal model as the cascode configuration almost eliminates the impact of these elements. Since C_f is a blocking capacitor, it can also be ignored in the small-signal analysis. For simplicity, we let Z_L represent the parallel RLC network as the load impedance. Fig. 4.5(b) shows the resultant simplified small-signal model used for input-matching analysis.

Applying Kirchoff Current Law (KCL) to Fig. 4(b), we can write

$$\frac{v_{gs} - v_{out}}{R_f} + jwC_{gs}v_{gs} = i_{in} \tag{4.3}$$

$$g_m v_{gs} + \frac{v_{out}}{Z_L} = \frac{v_{gs} - v_{out}}{R_f} \tag{4.4}$$

Solving for v_{out} in (4.4) and substituting into (4.3) give

$$v_{out} = \frac{Z_L(1 - Z_f g_m)}{Z_L + Z_f} v_{gs} \tag{4.5}$$

Eliminate v_{out} from (4.3) using (4.5)

$$v_{gs}\left[1-\frac{Z_L(1-R_f g_m)}{Z_L+R_f}\right]+jwC_{gs}R_f v_{gs}=i_{in}R_f \tag{4.6}$$

$$v_{gs}\frac{1+Z_L g_m}{Z_L+R_f}+jwC_{gs}v_{gs}=i_{in} \tag{4.7}$$

$$\frac{i_{in}}{v_{gs}}=jwC_{gs}+\frac{1+Z_L g_m}{Z_L+R_f}=Y'_{in} \tag{4.8}$$

where Y'_{in} is the admittance looking into the gate of M_1. Assuming Z_L is such large at the frequencies of interest that $Z_L g_m >> 1$, (5) can be simplified as

$$Y'_{in}\approx j\omega C_{gs}+\frac{Z_L g_m}{Z_L+R_f}=jwC_{gs}+\frac{1}{\frac{1}{g_m}+\frac{R_f/g_m}{Z_L}} \tag{4.9}$$

Substituting

$$\frac{1}{Z_L}=\frac{1}{R_L}+j\omega C_L+\frac{1}{j\omega L_d} \tag{4.10}$$

We have

$$Y'_{in}\approx jwC_{gs}+\frac{1}{\frac{1}{g_m}+\frac{R_f}{g_m}(\frac{1}{R_L}+j\omega C_L+\frac{1}{j\omega L_d})} \tag{4.11}$$

Defining $k=\frac{R_f}{g_m}$ lead to

$$Y'_{in}\approx jwC_{gs}+\frac{1}{\frac{1}{g_m}(\frac{R_f}{R_L}+1)+j\omega\cdot kC_L+\frac{1}{j\omega\cdot\frac{L_d}{k}}} \tag{4.12}$$

The first part of Y'_{in} is contributed by the parasitic capacitance at the gate of M_1, while its second part is formed by the load impedance coupled through the feedback resistor R_f.

Note that this part of impedance is just like that of a serial RLC network, consisting of resistance $R' = \frac{1}{g_m}(\frac{R_f}{R_L}+1)$, capacitance $C' = \frac{L_d}{k}$, and inductance $L' = kC_L$, representing the equivalent impedance seen at the input port through the feedback resistor.

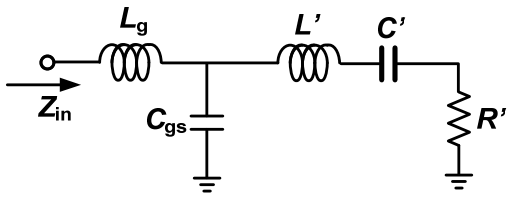


Fig. 4.6 Equivalent schematic of the input network of the proposed UWB LNA

With this equivalent impedance, an equivalent circuit of the input network of the proposed UWB LNA can be formed as shown in Fig. 4.6. Under the assumption of $R_f \simeq R_L$, R' only depends upon g_m and, with proper value for g_m obtained with specific bias voltages, R' can be made to approximately equal 50 Ohms. Consequently, the input network behaves just like a lumped-elements band-pass filter. A wideband matching can thus be easily achieved with a proper design.

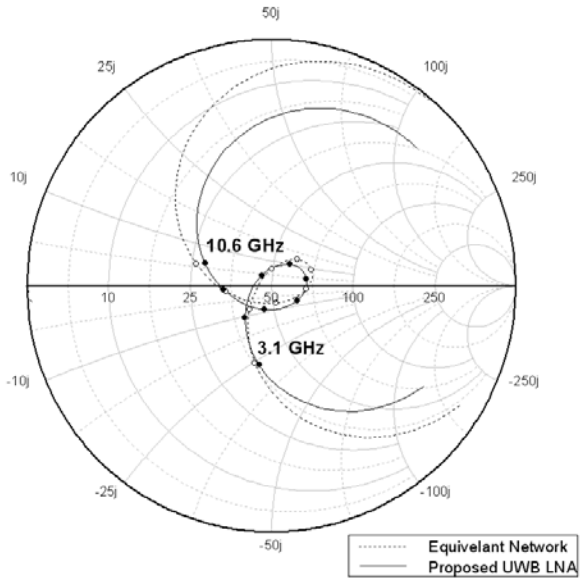


Fig. 4.7 Calculated input reflection coefficient of proposed UWB LNA and the equivalent input network

Fig. 4.7 shows the calculated input reflection coefficients of the equivalent input network shown in Fig.4.6 and the proposed UWB LNA versus frequency from 1 to 20 GHz. The transistors used in the calculations are the standard MOSFETs available in the Jazz's 0.18-µm CMOS process and the values of other circuit elements are L_g=1.0 nH and R_f=R_L=400 Ohms, The results show that good input matching is achieved from 3.1-10.6 GHz with very good match between those calculated from the input equivalent circuit and the LNA. Furthermore, the simulated results of these two circuits have similar pattern across 1-20 GHz. The deviation of the results between the two circuits gradually increases below 3 GHz and beyond 10 GHz and is due to the fact that the assumption of $Z_L g_m$>>1, which we've previously made, is no long valid at those frequencies.

4.2.2 Gain

The gain of the proposed UWB LNA can also be derived from the small signal model shown in fig. 4.5(b):

$$v_{in} = v_{gs} + i_{in} \cdot jwL_g = v_{gs} + \frac{v_{in}}{Z_{in}} \cdot jwL_g \tag{4.13}$$

From which,

$$v_{gs} = v_{in}(1 - \frac{jwL_g}{Z_{in}}) = v_{in} \cdot \frac{Z_{in} - jwL_g}{Z_{in}} \tag{4.14}$$

Solving (4.5) for v_{out} and making use of (4.14) give

$$v_{out} = \frac{Z_L(1 - R_f g_m)}{Z_L + R_f} v_{gs} = \frac{Z_L(1 - R_f g_m)}{Z_L + R_f} \cdot v_{in} \cdot \frac{Z_{in} - jwL_g}{Z_{in}} \tag{4.15}$$

The gain of the UWB LNA can now be written from (4.15) as

$$G = \frac{v_{out}}{v_{in}} = \frac{Z_L(1 - R_f g_m)}{Z_L + R_f} \cdot \frac{Z_{in} - jwL_g}{Z_{in}} \tag{4.16}$$

Notice that

$$Z_{in} - jwL_g = \frac{1}{Y'_{in}} = \frac{1}{j\omega C_{gs} + \frac{Z_L g_m + 1}{Z_L + R_f}} \tag{4.17}$$

$$G = \frac{v_{out}}{v_{in}} = \frac{1}{Z_{in}} \cdot \frac{Z_L(1 - R_f g_m)}{Z_L + R_f} \cdot \frac{1}{j\omega C_{gs} + \frac{Z_L g_m + 1}{Z_L + R_f}}$$

$$= \frac{1}{Z_{in}} \cdot \frac{Z_L(1 - R_f g_m)}{j\omega C_{gs}(Z_L + R_f) + (Z_L g_m + 1)} \tag{4.18}$$

Assuming $R_f g_m \gg 1$ and $Z_L g_m \gg 1$, which could achieve by choosing the proper value of R_f, Z_L and g_m, we have

$$G \approx \frac{1}{Z_{in}} \cdot \frac{-Z_L R_f g_m}{j\omega C_{gs}(Z_L + R_f) + Z_L g_m}$$

$$= -\frac{R_f}{Z_{in}} \cdot \frac{1}{1 + j(1 + \frac{R_f}{Z_L}) \cdot \frac{\omega}{\omega_T}} \tag{4.19}$$

It is known that the f_t of commercial 0.18μm CMOS transistors is around 70 GHz, which is still much higher comparing with the UWB frequency range (3-11GHz). $R_f/Z_L \approx R_f/R_L$ when L_d resonant with C_L. As R_f and R_L are comparable in resistance, R_f/Z_L could also be comparable with 1, and the part $j(1+\frac{R_f}{Z_L}) \cdot \frac{\omega}{\omega_T}$ can be ignored, when $\omega < \frac{\omega_T}{2} = 35GHz$. Then, the gain of the UWB LNA could be simply be estimated by

$$G \approx -\frac{R_f}{Z_{in}} \tag{4.20}$$

Since Z_{in} is approximately 50 Ohm, the gain of the proposed LNA is mainly determined by the R_f, the feedback resistance. In (19), $j(1+\frac{R_f}{Z_L}) \cdot \frac{\omega}{\omega_T}$ reflects how the frequency can affect the gain of the LNA and how the RLC parallel network helps to boost up the gain.

4.2.3 Noise Figure

The noise of the proposed resistive feedback UWB LNA is dominated by two parts, the noise from M_1 and noise of the feedback resistor R_f. The small signal model

for the noise analysis is shown in fig. 4.8. $e_{n,Rf}$ models the thermal noise of the feedback resistor R_f, whose Power Spectrum Density (PSD) can be expressed as

$$\overline{e_{n,Rf}^2} = 4kTR_f \cdot \Delta f \tag{4.21}$$

where k is the Boltzmann constant, T is the absolute temperature in Kelvin, Δf is the bandwidth over which the noise figure is measured. The PSD of the induced gate noise and channel thermal noise are given by

$$\overline{i_{ng}^2} = 4kT\delta g_g \cdot \Delta f \tag{4.22}$$

where δ is the coefficient of the induced gate noise and g_g is the equivalent shunt gate conductance, which is given by

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} \tag{4.23}$$

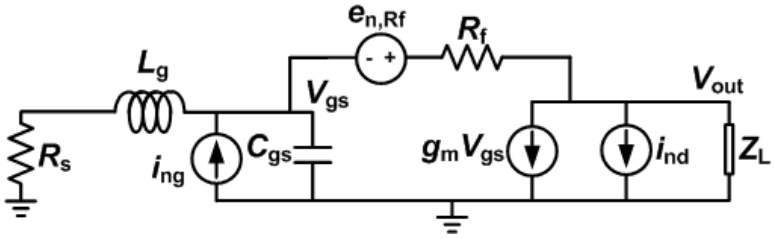


Fig. 4.8 Small signal model of the proposed UWB LNA for the noise analysis

$$\overline{i_{nd}^2} = 4kT\gamma g_{d0} \cdot \Delta f \tag{4.24}$$

where γ is the coefficient, which is around 2/3 for long-channel transistors, and as big as 2.5 for short-channel transistors. g_{d0} is the channel conductance when V_{ds}=0 V. The

induced gate noise is correlated with the channel thermal noise, with a correlation coefficient c, defined as

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^{*}}}{\sqrt{\overline{i_{ng}^{2}} \cdot \overline{i_{nd}^{2}}}} \tag{4.25}$$

For long-channel devices, c=-*j*0.395.

To calculate the noise figure of the whole LNA, the output noise PSD contributed by the source resistor will be derived first. Fig 4.9 shows the small signal model for analysis the noise contribution of source resistance.

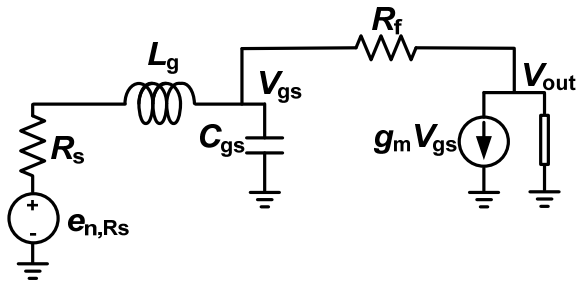


Fig. 4.9 Small signal model for analysis the noise contribution of source resistance

By applying KCL, we have

$$\frac{e_{n,Rs} - v_{gs}}{R_s + j\omega L_g} = j\omega C_{gs} \cdot v_{gs} + \frac{v_{gs} - v_{out}}{R_f} \tag{4.26}$$

$$\frac{v_{gs} - v_{out}}{R_f} = g_m v_{gs} + \frac{v_{out}}{Z_L} \tag{4.27}$$

From (4.27),

$$v_{gs} = \frac{Z_L + R_f}{Z_f(1 - g_m R_f)} \cdot v_{out} \tag{4.28}$$

Substitute v_{gs} in (4.26) with (4.28),

$$v_{out} = -\frac{g_m}{\frac{1}{Z_L} + \frac{1}{R_f}} \cdot \frac{1}{1 + (R_S + jwL_g)(\frac{1}{R_f} + jwC_{gs})} e_{n,Rs} \tag{4.29}$$

Define

$$t = (R_S + jwL_g)(\frac{1}{R_f} + jwC_{gs}) \tag{4.30}$$

Then the output noise PSD contributed by the source can be derived from (4.29) and (2.2) as

$$S_{n,Rs} = {v_{out}}^2 = \frac{4kTR_S}{\frac{1}{g_m^2}\left|\frac{1}{Z_L} + \frac{1}{R_f}\right|^2 |1 + t|^2} \tag{4.31}$$

To calculate the output noise PSD contributed by the feedback resistor R_f, fig. 4.9 is used for the analysis, using KCL, we have

$$\frac{e_{n,R_f} + v_{gs} - v_{out}}{R_f} = g_m v_{gs} + \frac{v_{out}}{Z_L} = -\frac{v_{gs}}{(R_s + j\omega L_g) // \frac{1}{j\omega C_{gs}}} \tag{4.32}$$

Eliminate v_{gs} in (4.32), we have

$$e_{n,R_f} = (1 + \frac{R_f}{Z_L} \cdot \frac{j\omega C_{gs} + \frac{1}{R_s + j\omega L_g}}{g_m + j\omega C_{gs} + \frac{1}{R_s + j\omega L_g}}) \cdot v_{out} \tag{4.33}$$

Define

$$p = j\frac{\omega}{\omega_T} + \frac{1}{g_m(R_S + j\omega L_g)} \tag{4.34}$$

We have

$$v_{out} = \frac{e_{n,R_f}}{1 + \frac{R_f}{Z_L} \cdot \frac{p}{1+p}} \tag{4.35}$$

Then the output noise PSD contributed by the feedback resistor can be calculated from the definition as

$$S_{n,R_f} = v_{out}^2 = \frac{4kTR_f}{\left|1 + \frac{R_f}{Z_L} \cdot \frac{p}{1+p}\right|^2} \tag{4.36}$$

Since the transistor is normally biased to produce large transconductance g_m needed for gain and ω/ω_T is typically small, p is considered small. Furthermore, since Z_L and R_f are comparable within 3.1-10.6 GHz, $S_{n,Rf}$ can be approximated as $4kTR_f$ with very little fluctuation within this frequency range. The frequency response of $S_{n,Rf}$ is mainly caused by that of p and Z_L representing a RLC parallel network. The noise contribution of the feedback resistor to the overall noise factor of the UWB LNA can be derived from

$$F_{R_f} = \frac{S_{n,R_f}}{S_{n,R_S}} \tag{4.37}$$

Substitute (4.31) and (4.36) into (4.37)

$$F_{R_f} = \frac{R_f}{R_s} \cdot \frac{1}{g_m^2} \left| \frac{1}{Z_L} + \frac{1}{R_f} \right|^2 \cdot \frac{|1+k|^2}{\left| 1 + \frac{R_f}{Z_L} \cdot \frac{p}{1+p} \right|^2} \tag{4.38}$$

To simplify (4.38), notice that output noise PSD contributed by the source resistor can also be derived from the Gain expression in (4.19).

Since,

$$v_{out} = G \cdot v_{in} \tag{4.39}$$

$$v_{out} = G \cdot \frac{Z_{in}}{R_S + Z_{in}} e_{n,R_s} \tag{4.40}$$

Substitute (4.19) into (4.40),

$$v_{out} = -\frac{R_f}{R_S + Z_{in}} \cdot \frac{1}{1 + j(1 + \frac{R_f}{Z_L}) \cdot \frac{\omega}{\omega_T}} \cdot e_{n,R_s} \tag{4.41}$$

Then the output noise PSD contributed by the source can be given as

$$S_{n,Rs} = 4kTR_S \left| \frac{R_f}{Z_{in} + R_S} \cdot \frac{1}{1 + j(1 + \frac{R_f}{Z_L}) \cdot \frac{\omega}{\omega_T}} \right|^2 \tag{4.42}$$

F_{Rf} could also be given as

$$F_{R_f} = \frac{S_{n,R_f}}{S_{n,R_S}} = \frac{1}{R_f} \cdot \frac{\left| 1 + j(1 + \frac{R_f}{Z_L}) \cdot \frac{\omega}{\omega_T} \right|^2}{\left| 1 + \frac{R_f}{Z_L} \cdot \frac{p}{1+p} \right|^2} \frac{\left| Z_{in} + R_S \right|^2}{R_S} \tag{4.43}$$

When the LNA is matched to 50-Ohm, $Z_{in} \approx R_S$,

$$F_{R_f} = 4\frac{R_S}{R_f}\cdot\frac{\left|1+j(1+\frac{R_f}{Z_L})\cdot\frac{\omega}{\omega_T}\right|^2}{\left|1+\frac{R_f}{Z_L}\cdot\frac{p}{1+p}\right|^2} \tag{4.44}$$

Notice that $G \approx -\frac{R_f}{Z_{in}}$ from (4.20)

$$F_{R_f} = \frac{4}{|G|}\cdot\frac{\left|1+j(1+\frac{R_f}{Z_L})\cdot\frac{\omega}{\omega_T}\right|}{\left|1+\frac{R_f}{Z_L}\cdot\frac{p}{1+p}\right|^2} \approx \frac{4}{|G|} \tag{4.45}$$

This express shows that the noise contribution of the feedback resistor to the noise figure of UWB LNA does not increase as its resistance increases. On the contrary, output noise will be lower as the feedback resistance increases. It seems that a bigger R_f could lead to both a higher gain and a lower noise figure. However, because of the trade-off between the gain and bandwidth, R_f could not be too large as it will lower the bandwidth.

To calculate the output noise contributed by the induced gate noise, we can write from the small signal model, using KCL

$$i_{ng} = \frac{v_{gs}}{Z_g} + \frac{v_{gs} - v_{out}}{Z_f} \tag{4.46}$$

$$\frac{v_{gs} - v_{out}}{Z_f} = g_m v_{gs} + \frac{v_{out}}{Z_L} \tag{4.47}$$

Where

$$Z_g = (R_S + j\omega L_g) // \left(\frac{1}{j\omega C_{gs}} \right) \tag{4.48}$$

Eliminate v_{gs} in (4.46) using (4.47), we have

$$i_{ng} = \left[\frac{R_f + Z_L}{Z_L Z_g (1 - R_f g_m)} + \frac{1 + Z_L g_m}{Z_L (1 - R_f g_m)} \right] \cdot v_{out} \tag{4.49}$$

Again, assuming $Z_L g_m \gg 1$,

$$i_{ng} \approx -\left[\frac{R_f + Z_L + Z_g}{-Z_L Z_g R_f g_m} + \frac{1}{R_f} \right] \cdot v_{out} \tag{4.50}$$

Substituting (4.48) and (4.34) into (4.50),

$$i_{ng} \approx (\frac{p}{Z_L} + \frac{1+p}{R_f}) \cdot v_{out} \tag{4.51}$$

Hence, the output noise PSD due to the gate inducted noise of M_1 is

$$S_{ng} = v_{out}^2 = \frac{4kT\delta g_g}{\left| \frac{p}{Z_L} + \frac{1+p}{R_f} \right|^2} \tag{4.52}$$

To calculate the output noise contributed by the channel thermal noise, from the small signal model, using KCL, we have

$$\frac{v_{gs} - v_{out}}{Z_f} = j\omega C_{gs} \cdot v_{gs} + \frac{v_{gs}}{R + j\omega L_g} \tag{4.53}$$

$$\frac{v_{out}}{Z_L} + i_{nd} + g_m v_{gs} = \frac{v_{gs} - v_{out}}{Z_L} \tag{4.54}$$

Eliminate v_{gs} in (4.54) using (4.53),

$$v_{out} = -\frac{1}{\frac{1}{Z_L} + \frac{Z_g g_m + 1}{R_f + Z_g}} \cdot i_{nd} \tag{4.55}$$

Substituting (4.48) and (4.34) into (4.50),

$$v_{out} = -\frac{i_{nd}}{\frac{1}{Z_L} + \frac{1+p}{R_f \cdot p + 1/g_m}} \tag{4.56}$$

Hence, the output noise PSD contributed by channel noise is

$$S_{nd} = \frac{4kT\gamma g_{d0}}{\left| \frac{1}{Z_L} + \frac{1+p}{R_f \cdot p + 1/g_m} \right|^2} \tag{4.57}$$

The induced gate noise and thermal channel noise of the transistor are correlated. There is another amount of noise due to the correlation of these two parts, which could be derived from,

$$v_{out,total\ noise} = v_{out,ng} + v_{out,nd} = a \cdot i_{ng} + b \cdot i_{nd} \tag{4.58}$$

Where $v_{out,total\ noise}$ is the total output noise due to the sum of gate inducted noise and channel thermal noise, $v_{out,ng}$ and $v_{out,nd}$ are the output noise due to gate inducted noise and channel thermal noise respectively, a and b are the noise impedance reflecting the relation between the output noise voltage and current noise source in the transistor M_1. In the considered LNA, we have from (4.51) and (4.56)

$$a = \frac{1}{\frac{p}{Z_L} + \frac{1+p}{R_f}} \tag{4.59}$$

$$b = -\frac{1}{\frac{1}{Z_L} + \frac{1+p}{R_f \cdot p + 1/g_m}}$$

The PSD of output noise due to the sum of gate induced noise and channel thermal noise is

$$\overline{v_{out,total\ noise}^2} = (v_{out,ng} + v_{out,nd}) \cdot (v_{out,ng} + v_{out,nd})^* \tag{4.60}$$

$$\begin{aligned}
\overline{v_{out,total\ noise}^2} &= (a \cdot i_{ng} + b \cdot i_{nd}) \cdot (a \cdot i_{ng} + b \cdot i_{nd})^* \\
&= (a \cdot i_{ng} + b \cdot i_{nd}) \cdot (a^* \cdot i_{ng}{}^* + b^* \cdot i_{nd}{}^*) \\
&= |a|^2 \cdot \overline{i_{ng}^2} + |b|^2 \cdot \overline{i_{nd}^2} + a i_{ng} \cdot b^* i_{nd}^* + a^* i_{ng}{}^* \cdot b i_{nd} \\
&= |a|^2 \cdot \overline{i_{ng}^2} + |b|^2 \cdot \overline{i_{nd}^2} + 2\,\mathrm{Re}[a b^* i_{ng} i_{nd}^*] \\
&= \overline{i_{nd}^2} \cdot \left[|a|^2 \cdot \frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}} + |b|^2 + 2\,\mathrm{Re}[a b^* \cdot c \sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}}] \right]
\end{aligned} \tag{4.61}$$

Where

$$c = \frac{\overline{i_{ng} \cdot i_{nd}^*}}{\sqrt{\overline{i_{ng}^2} \cdot \overline{i_{nd}^2}}} \tag{4.62}$$

In (4.61), the first two parts are output noise PSD due to the gate induced noise and channel noise, the last term is caused by the correlation of gate induced noise and channel noise. This part of noise can be written as $S_{ndg,c}$

$$S_{ndg,c} = 2\overline{i_{nd}^2} \cdot \mathrm{Re}\left[ab^* \cdot c \sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}} \right] \tag{4.63}$$

For NMOS device M_1, $\sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}}$ could be calculated from (4.22), (4.23) and (4.24) as

$$\sqrt{\frac{\overline{i_{ng}^2}}{\overline{i_{nd}^2}}} = \sqrt{\frac{\delta\omega^2 C_{gs}^2}{5\gamma g_{d0}^2}} = \frac{\omega C_{gs}}{g_{d0}} \sqrt{\frac{\delta}{5\gamma}} \tag{4.64}$$

Substitute (4.64) into (4.63), the output noise PSD contributed by the correlation of gate induced noise and channel noise can be written as

$$S_{ndg,c} = 8kTwC_{gs} \sqrt{\frac{\delta\gamma}{5}} \cdot \mathrm{Re}\left[\frac{c}{\left[\left(\frac{1}{Z_L} + \frac{1+p}{R_f \cdot p + 1/g_m} \right) \left(\frac{p}{Z_L} + \frac{1+p}{R_f} \right)^* \right]} \right] \tag{4.65}$$

So, the noise factor of the proposed resistive feedback UWB LNA could be derived by its definition, as

$$F = \frac{S_{n,total}}{S_{n,Rs}} = 1 + \frac{S_{n,R_f}}{S_{n,Rs}} + \frac{S_{ng}}{S_{n,Rs}} + \frac{S_{nd}}{S_{n,Rs}} + \frac{S_{ndg,c}}{S_{n,Rs}} \tag{4.66}$$

$$F = 1 + \frac{R_f}{R_s} \cdot \frac{1}{g_m^2} \left| \frac{1}{Z_L} + \frac{1}{R_f} \right|^2 \cdot \frac{|1+k|^2}{\left| 1 + \frac{R_f}{Z_L} \cdot \frac{p}{1+p} \right|^2}$$

$$+ \frac{\delta}{g_{d0} R_S} \left(\frac{\omega}{\omega_T} \right)^2 \frac{\left| 1 + \frac{R_f}{Z_L} \right|^2}{\left| 1 + p + p\frac{R_f}{Z_{L\,f}} \right|^2} |1+k|^2$$

$$+\frac{1}{g_m^2}\frac{\gamma g_{d0}}{R_S}\frac{\left|1+\frac{Z_L}{R_f}\right|^2}{\left|1+\frac{1+p}{p+1/g_m R_f}\cdot\frac{Z_L}{R_f}\right|^2}|1+k|^2$$

$$+\frac{2wC_{gs}}{R_S}\sqrt{\frac{\delta\gamma}{5}}\cdot\mathrm{Re}\left[\frac{c}{\left[(\frac{1}{Z_L}+\frac{1+p}{R_f\cdot p+1/g_m})(\frac{p}{Z_L}+\frac{1+p}{R_f})^*\right]}\right]\left|\frac{1}{Z_L}+\frac{1}{R_f}\right|^2| \tag{4.67}$$

4.2.4 Output Matching

The second stage of the UWB LNA is just a source follower, which can provide output matching and current to drive a 50-Ohm load. For a source follower in CMOS, its voltage gain can be derived as [6]

$$\frac{v_{out}}{v_{in}}=\frac{R_L g_m}{1+R_L g_m} \tag{4.68}$$

Where R_L is load resistance, g_m is the transconductance of M_3. Since its output impedance is roughly $1/g_m$, when it is matched to R_L, which is 50-Ohm, we have

$$R_L g_m \approx 1 \tag{4.69}$$

Then, the voltage gain dropped to

$$\frac{v_{out}}{v_{in}}=\frac{R_L g_m}{1+R_L g_m}\approx\frac{1}{2} \tag{4.70}$$

which is -6dB.

4.3 Circuit Design

The proposed resistive feedback UWB LNA is designed and fabricated in Jazz 0.18-μm RF CMOS process [51]. The gate width of M_1 is set to be 160 μm for the optimized gain, noise figure and power consumptions. The feedback resistor R_f with a resistance of 400-Ohm is used in the design for the trade-off between gain and bandwidth. To achieve both matching and gain over the UWB band, the load impedance is formed by an RLC parallel network. For the gain, bandwidth and noise consideration, R_L is set as R_L=R_f=400-Ohm. And L_d is chosen to be 4.5-nH to be resonant with the load capacitance of the first stage, which is parasitic capacitance at the drain of M_2. The input matching of the LNA is completed by L_g, with an inductance of 1.0nH. Since the Q of the gate inductor is always critical as it has great impact on the over-all noise performance of the whole LNA, a high Q inductor is designed and simulated in IE3D. Its simulated S-parameter result is imported for the simulation of the whole LNA.

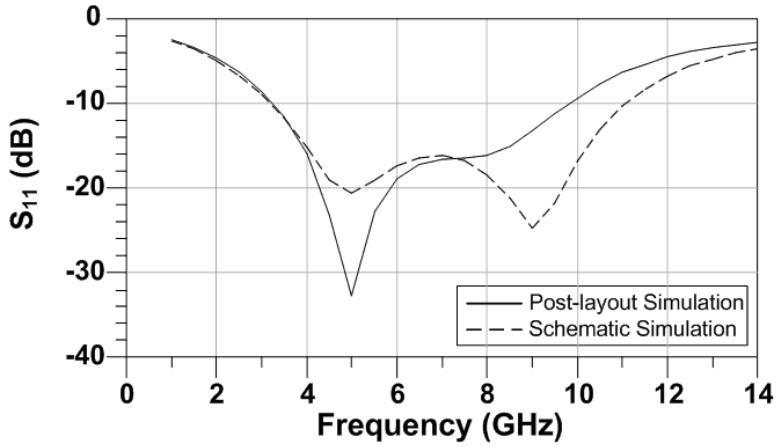
The cascode device M_2 is chosen to be identical with M_1 in dimensions. Its gate is biased at V_{dd}, which is 1.8 V. The source follower is formed by two transistors with gate width of 80 μm to compromise the gain and output matching. The g_m of M_3 and M_4 are biased by the DC biasing voltage at the gate of M_4, which is around 0.9V.

The whole design only includes two inductors, L_g and L_d. The gate inductor L_g, which has an inductance of 1.0nH, could be replaced by a bond-wire. For this design, L_g and L_d are both on chip inductors, the whole UWB LNA only consumes a chip area of

0.75×0.6 mm^2 including RF and DC pads.

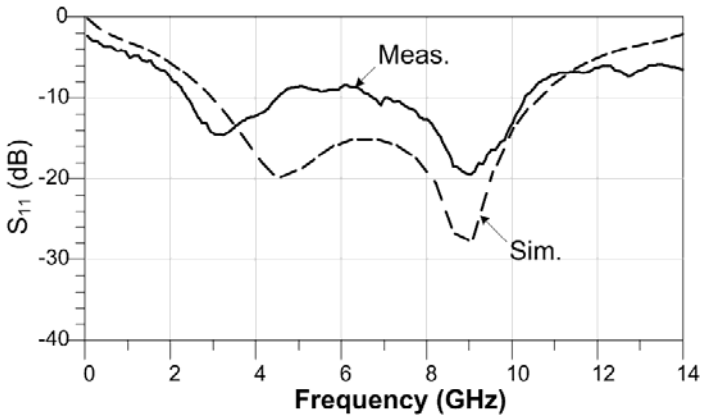
4.4 Circuit Performance

The proposed resistive shunt feedback CMOS UWB LNA is simulated using Cadence SpectreRF. The parasitic effects have been extracted from the layout and taken into account in the post-layout simulation. The measurement of the developed CMOS UWB LNA was done with on-wafer RF probes. Transistor M_1 was biased externally using a bias-T at the input of the LNA. The V_{dd} and the gate of M_4 were also externally biased using two on-wafer DC probes.



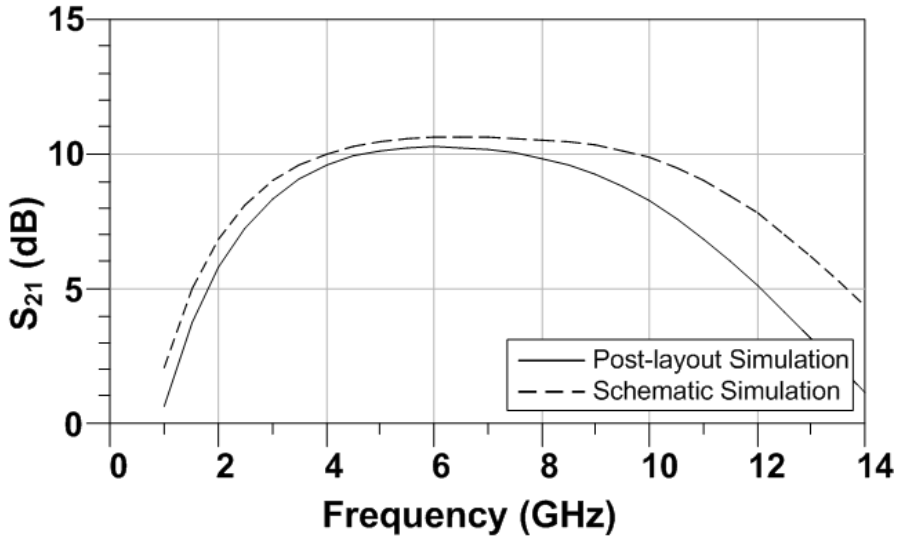
(a)

Fig. 4.10 Simulation and measurement results of the input reflection coefficient (S_{11}) of the developed UWB LNA: (a) Post-layout simulation results of the input reflection coefficient of the proposed UWB LNA



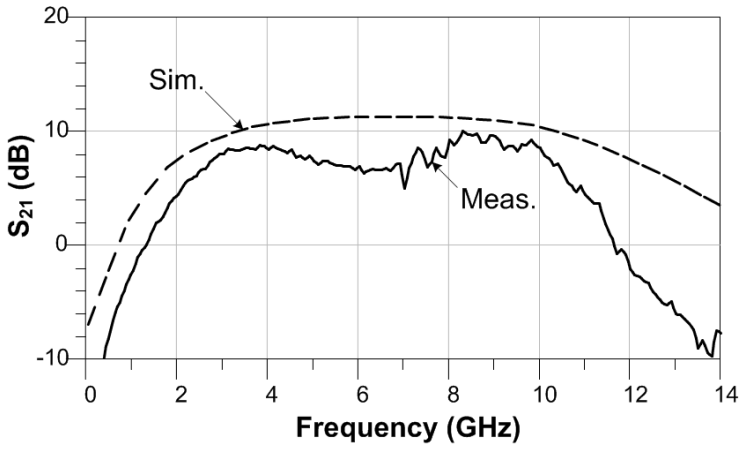
(b)

Fig.4.10 continued (b) Measurement and calculation results of the input reflection coefficient (S_{11}) of the developed UWB LNA



(a)

Fig. 4.11 Simulation and measurement results of the forward gain (S_{21}) of the developed UWB LNA: (a) Post-layout simulation results of the forward gain of the proposed UWB LNA



(b)

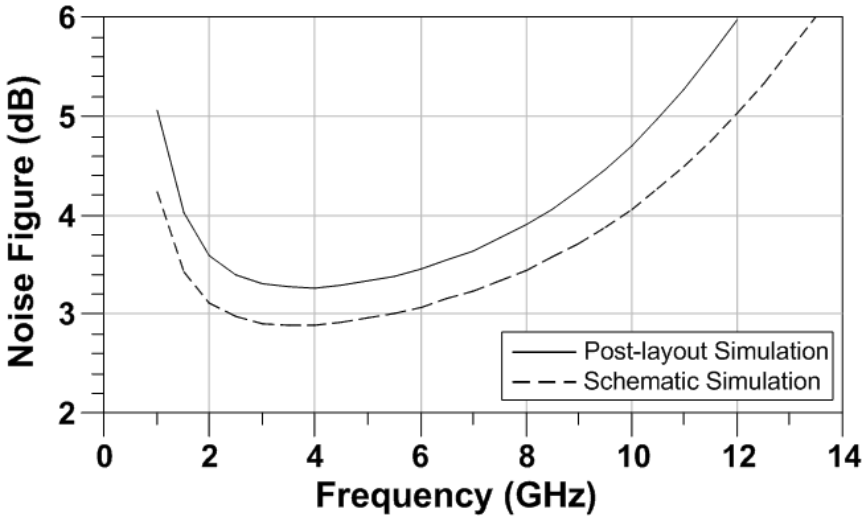
Fig.4.11 continued (b) Measurement and calculation results of the forward gain (S_{21}) of the developed UWB LNA

Fig. 4.10(a) shows the input reflection coefficient in both schematic and post-layout simulations. In the schematic simulation, the S_{11} is lower than -10dB through 3-11 GHz. But the post-layout simulation result shows that this bandwidth changed to 3-10 GHz. This is mainly due to the parasitic capacitance of the input pad at the gate the M1. One approach to alleviate this problem is to change L_g and R_f a little bit to cancel the effects of the parasitic capacitance. Nevertheless, S_{11} in the post-layout simulation results is below -9 dB over 3-11 GHz bandwidth, indicating an acceptable input matching. The simulated and measured input reflection coefficients (S11) are plotted in Fig. 4.10(b). The measurement results, while showing similar trend with those of simulated, have some discrepancy with the calculated performance, S_{11} is still lower than -10 dB across 2.5-10.3 GHz with the exception of around -8 dB between 5-6.3 GHz. This discrepancy is mainly due to the parasitic capacitance of the input RF pads and that at the gate of the M_1, which is typically expected in the design.

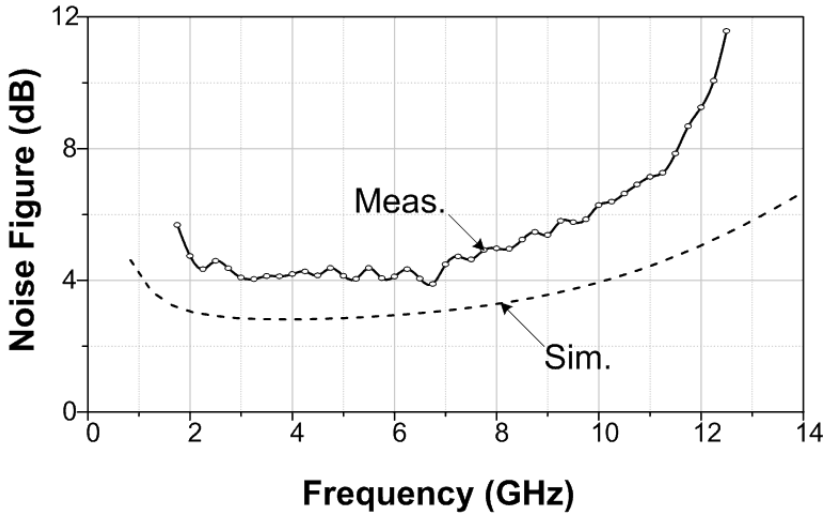
The gains of the proposed UWB LNA are plotted in fig. 4.11. The proposed UWB LNA exhibits a gain of 9.5-11 dB from 3-11 GHz in the schematic simulation, 8-10.5dB from 3-10 GHz in the post-layout simulation and 8-10 dB between 3-10 GHz in the measurement, draining only 5mA current from 1.8V voltage supply for the amplifier core of M_1 and M_2. It is noted that both the gain and bandwidth could be improved by increasing the biasing voltage at the gate of M_1 but at an expense of the power consumption. The measurement also shows that the amplifier provides a gain of 9-11 dB from 3-12 GHz with a current consumption of 12 mA.

Fig. 4.12 shows the noise performance of the proposed design. In the schematic simulation result, the noise figure drops to as low as 2.7 dB at around 3.5 GHz, keeps going up as frequency goes high, passes 4dB at 10 GHz. The post-layout simulation result and the measurement results indicate roughly 0.5dB and 1-2dB higher than those obtained from the simulations. Similar to gain, the noise performance can also be improved at the cost of the power consumptions. When draining a current of 12 mA from M_1, this amplifier shows a measured noise figure of only 3.5-5.5 dB from 3-10 GHz.

The reverse isolation will be an important part of a feedback amplifier, as poor reverse isolation may lead to oscillation. In fig. 4.13, a very low S_{12} of -50 to -30 dB can be observed in both the schematic and post-layout simulations, and -55 to -19 dB in the measurement across 1-11 GHz, which suggests that the resistive shunt feed technique doesn't damage on the reverse isolation of the UWB amplifier.

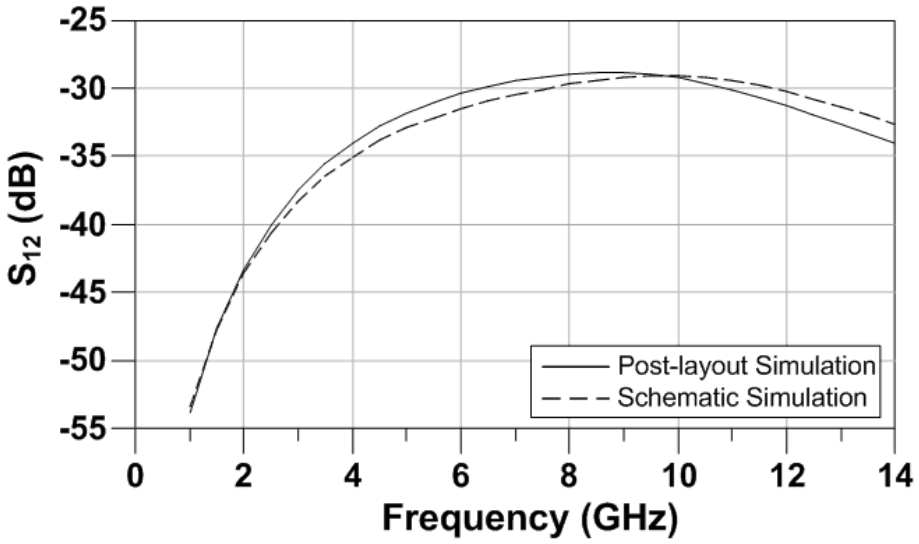


(a)

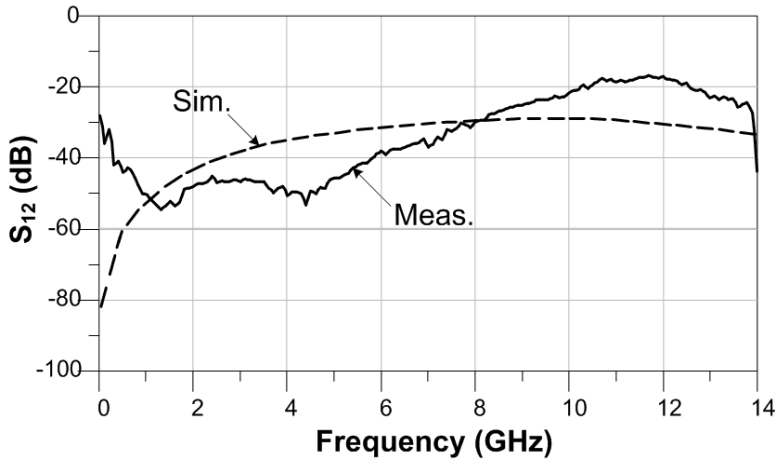


(b)

Fig. 4.12 Simulation and measurement results of the noise figure of the developed UWB LNA: (a) Post-layout simulation results of the noise figure of the proposed UWB LNA (b) Measurement and calculation results of the noise figure of the developed UWB LNA



(a)

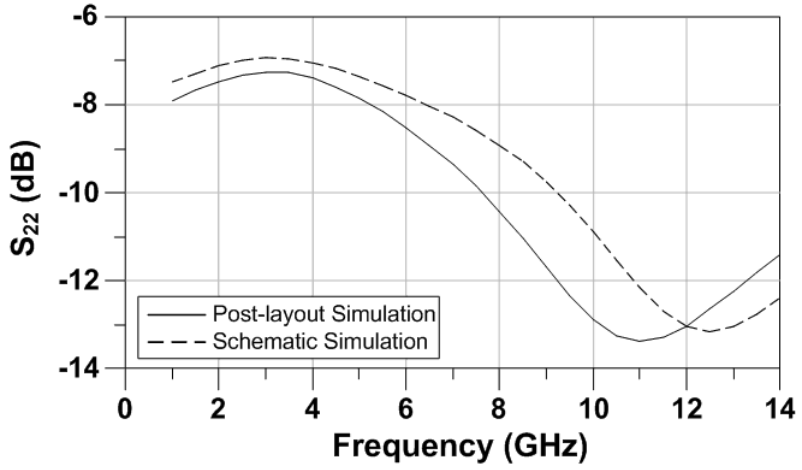


(b)

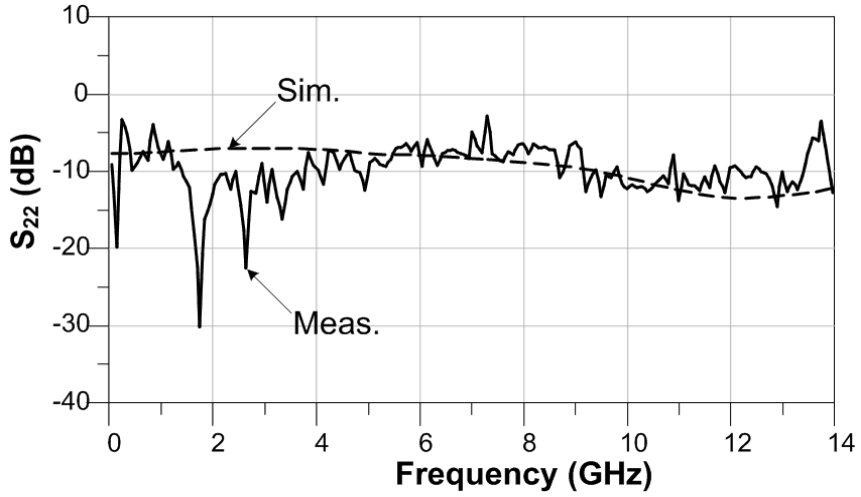
Fig. 4.13 Simulation and measurement results of the proposed UWB LNA: (a) Post-layout simulation results of the reverse isolation of the proposed UWB LNA (b) Measurement and calculation results of the reverse isolation (S_{12}) of the developed UWB LNA

The output matching of the proposed amplifier is shown in fig. 4.14. Both the schematic and post-layout simulation results show S_{22} is lower than -7dB. Although some fluctuation is observed in the measurement results, it still matches reasonably well

with the calculated results, which is lower than -8 dB from DC-14 GHz. As the output matching is mainly determined by the bias current in transistor M_3 and M_4, 5mA is chosen to trade off between the gain and S_{22}.



(a)



(b)

Fig. 4.14 Simulation and measurement results of the proposed UWB LNA: (a) Post-layout simulation results of the output reflection coefficient of the proposed UWB LNA (b) Measurement and calculation results of the output reflection coefficient (S_{22}) of the developed UWB LNA

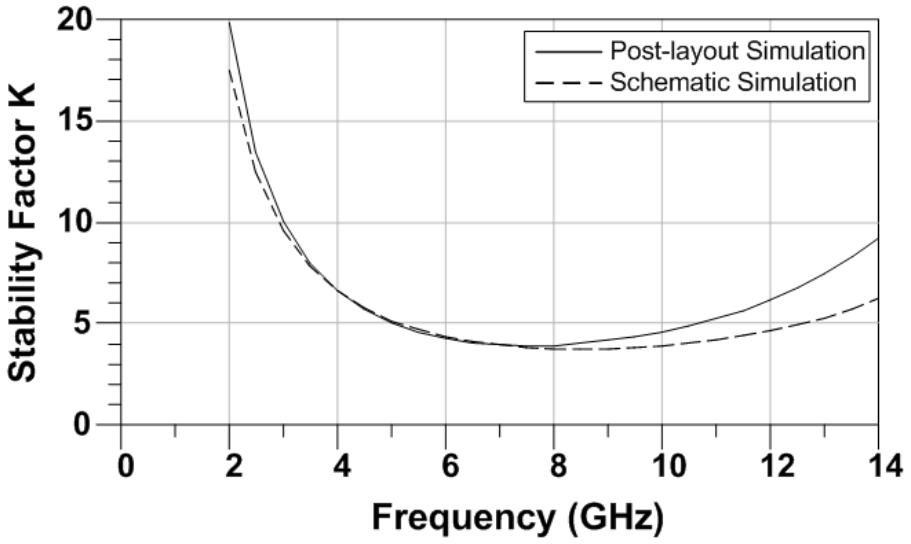


Fig. 4.15 Stability Factor K of the proposed UWB LNA

Stability is a very important issue for amplifier designs especially for the amplifier with feedback technique. The stability factor K of the proposed amplifier has been calculated and plotted in fig. 4.15. Both the schematic and post-layout simulation results show the stability factors K>3.8 from DC-14 GHz.

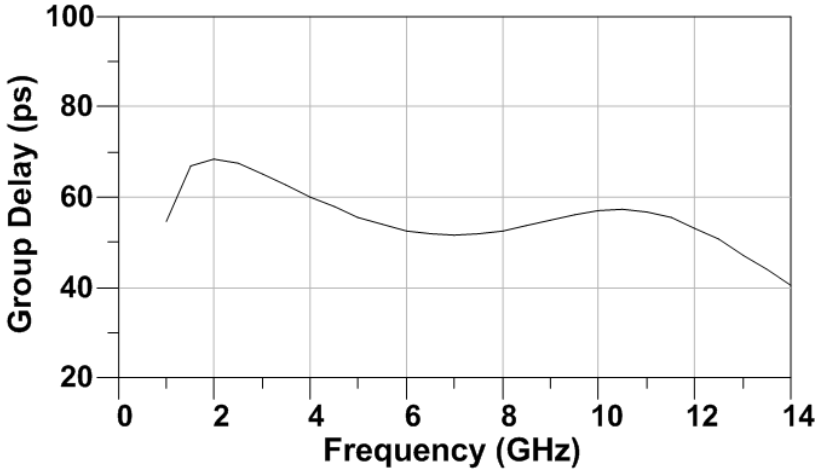


Fig. 4.16 Group Delay of the proposed UWB LNA

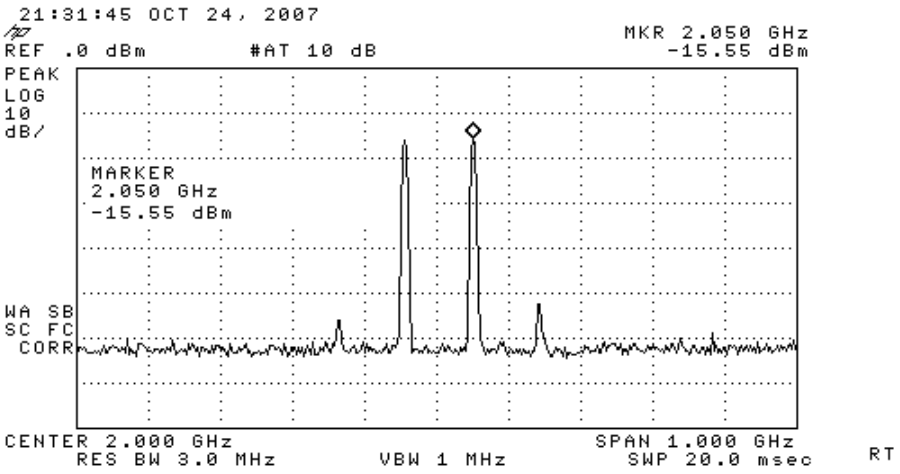


Fig. 4.17 Spectrum of the output of the UWB LNA in a two-tone test

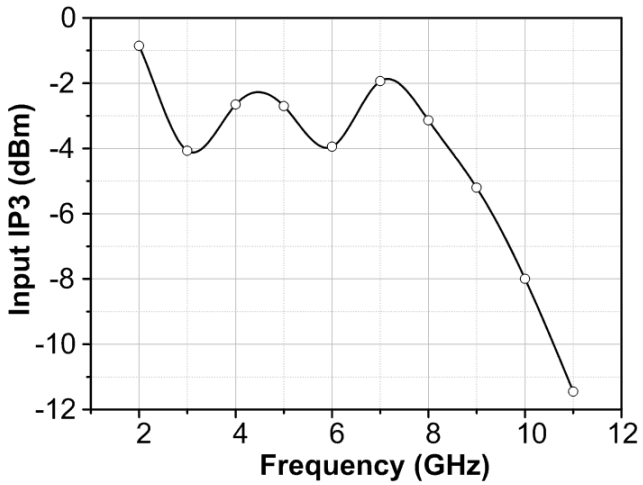


Fig. 4.18 Measured Input Third-Order Intercept point of the proposed UWB LNA

The group delay of the proposed UWB LNA is also calculated from the simulation results. Fig. 4.16 shows a group delay of 55ps within only ±10ps fluctuation from 3-12GHz.

Linearity is another important specification for LNA's. To measure the IIP3 of the proposed UWB LNA, a two tone test was performed. Two fundamental tones with 100MHz adjacent to each other were input to the UWB LNA through a power combiner. Fig. 4.17 shows the output spectrum of the UWB LNA with two input tones at the frequency of 1.95 GHz and 2.05 GHz. Measurement was made at 9 frequency points through 2-10GHz. Due to the feedback configuration, the designed UWB LNA has a good linearity as can be seen in Fig. 4.18. The IIP3 of the LNA varies from -2.1 to -11.4 dBm across 3-11 GHz.

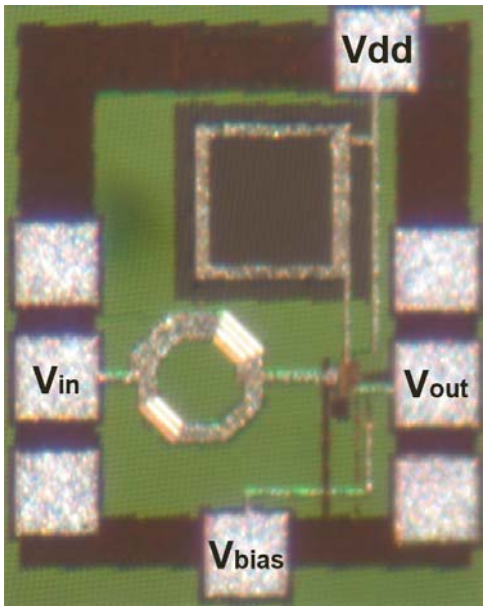


Fig.4.19 Microphotograph of the proposed UWB LNA

Fig. 4.19 shows the microphotograph of the designed 0.18-µm CMOS UWB LNA. The die size of the whole LNA is only 0.75×0.6 mm^2 including all RF and DC pads, or 0.55×0.4 mm^2 without pads, signifying again its miniaturization suitable for low-cost CMOS UWB applications.

Table 4.1 summarizes the performance of the designed CMOS UWB LNA and compares with those of recently published UWB LNA's. It is noted that our designed LNA is the only one using the resistive feedback technique that can operate over the entire UWB range of 3.1-10.6 GHz.

Table 4.1 Summarizes the Performance of the Proposed CMOS UWB LNA

	Tech.	S11 (dB)	G_{max} (dB)	B (GHz)	NF (dB)	P (mW)	Chip Area (mm^2)
[19]	0.18 µm CMOS	<-8	8.1	0.6 ~ 22	4.3 ~ 6.1	52	0.9×1.5
[43]	0.18 µm CMOS	<-20	10	0 ~ 11	3.3 ~ 6.1	19.5	0.9×1.6
[44]	0.18 µm CMOS	<-9.4	10.4	2.4 ~ 9.5	4.2 ~ 7.5	9	1.1
[47]	0.18 µm CMOS	<-11.24	12.02	3.1 ~ 10.6	4.7 ~ 5.6	10.57	0.665
[48]	0.18 µm CMOS	<-9	17.5	3.1 ~ 10.6	3.1~5.7	33.2	0.74×0.67
[52]	0.18 µm CMOS	<-2	12.4	0.4 ~ 10	4.4 ~ 6.5	12	0.42
[53]	0.18 µm CMOS	<-11	9.7	1.2 ~ 11.9	4.5 ~ 5.1	20	0.59
[54]	0.13 µm CMOS	<-9.9	15.1	3 ~ 11	2.5 ± 0.43	9	0.87
This Work	0.18 µm CMOS	<-8	10	3 ~ 10	3.9 ~ 6.3	9	0.75×0.6

4.5 Conclusion

In this sub section, we reports for the first time the design approach for UWB LNA's based on a simple resistive shunt feedback technique that can perform well over the entire UWB band of 3.1-10.6 GHz. More importantly, we demonstrate successfully

that good matching along with decent gain, noise figure and IIP3 could be achieved simultaneously over ultra-wide bandwidths using a relatively simple resistive shunt feedback topology for LNA. The proposed UWB LNA employs only two inductors, one of which could possibly be replaced with a bonding wire. The simplicity of the design makes possible low power consumption, low noise figure, and high linearity and, more significantly, provides an attractive alternative for realizing low-cost, high-performance CMOS UWB receivers and systems.

5. CMOS ULTRA-WIDEBAND FRONT-END FOR 3.1-10.6 GHz WIRELESS RECEIVERS

As the first stage of an Ultra-wideband receiver, low noise amplifier is one of the most critical blocks in the entire receiver designs. In the previous two sections, different kinds of CMOS Ultra-wideband low noise amplifiers have been discussed. These low noise amplifiers employ different techniques to meet the large bandwidth requirement for gain, noise figure, and input matching. When they are used in different UWB receivers, proper receiver configurations should be used. In this section, the design of UWB front-ends with two different low noise amplifiers will be investigated. Based on the two types of low noise amplifiers, which are discussed in the prior two sections, two new Ultra-wideband front-ends were developed. Both of them were designed in Jazz 0.18-μm CMOS, covering the whole UWB range of 3.1-10.6 GHz.

5.1 Motivation

UWB has been discussed and standardized in several IEEE bodies. IEEE 802.15.3a [55] includes two technology proposals for UWB: the OFDM proposal [56] of the Multiband OFDM Alliance (MBOA) and the direct sequence (DS) proposal. In a manner similar to IEEE 802.11a/g, MBOA divides the spectrum from 3-10 GHz into 528 MHz sub-bands and employs OFDM in each sub-band to transmit data rates as high as 480 Mb/s. To meet the FCC requirements of power-emission limitation at the transmitters, reduce power consumptions and lower the cost, MB-OFDM uses

frequency-hopping schemes across the sub-bands. Although the quarreling between the two sides will never come to an end, impulse based communication systems has become less attractive. More and more UWB applications in industry are based on more traditional DS-CDMA and multi-band OFDM.

Inspired by the two UWB LNA described in the previous two sections, two different UWB front-ends were designed in Jazz 0.18-μm CMOS process. Both of the two UWB front-ends working through 3.1-10.6 GHz are proven to be suitable for the UWB applications.

5.2 A UWB Distributed Front-End

Distributed amplifiers have been studied and analyzed as an attractive candidate for UWB applications in the previous sections. In a practical UWB receiver, a LNA is followed by a mixer, which down-converts the RF input signal into the IF signal. By utilizing the same ideal in mixer designs, several distributed mixers have been reported [56]. Most of the distributed mixer's topologies are combining several single-balanced mixers together and matching the RF input, LO input and IF output ports using distributed technique. The schematic is shown in fig.5.1.

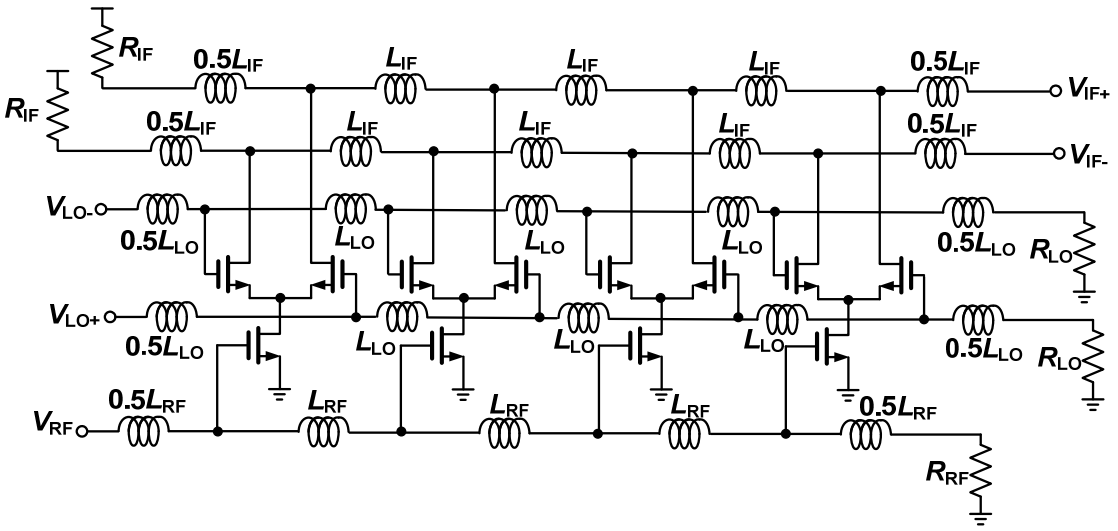


Fig. 5.1 Schematic of a CMOS distributed mixer

The distributed mixers can easily achieve a very wideband matching at RF, LO and IF ports, and can also provide a flat gain of 2.5-5dB [57] across 4-8.72 GHz. However, it also has some disadvantages. Firstly, it is difficult to integrate the distributed mixer with a low noise amplifier. Since the gain and noise performance of the distributed mixer is not good enough, a low noise amplifier is needed to provide enough gain and compress the noise power. But the artificial transmission line at the input of the mixer makes it difficult to integrate the distributed mixer with a low noise amplifier. Secondly, too many inductors are used in the design. In the distributed mixer shown in fig. 5.1, totally 25 inductors are used, which will result in a very large chip area.

In the following sub-section, a new distributed LNA integrated with mixer will be proposed. The new design integrated the distributed LNA and mixer together in one

circuit which leads to a much smaller chip area and lower power consumptions. By integrating the LNA and mixer, a much better noise figure and gain can also be achieved.

5.2.1 Circuit Analysis

An ideal distributed front-end is to integrate the distributed LNA with a mixer together, forming a single circuit that can provide not only amplification, but also frequency translation. The traditional single balanced mixers or double balanced mixers are no longer a good choice because of their low gain and the differential RF and/or differential LO input, which will result in an extremely large chip area. The cascode mixers, shown in fig. 5.2, working like multi-gate mixers, simply use two cascode transistors. RF and LO inputs are going through the gates of M_1 and M_2 transistors. Because of its simplicity and single-ended for RF and LO, cascode mixers can be an ideal candidate for distributed mixers designs.

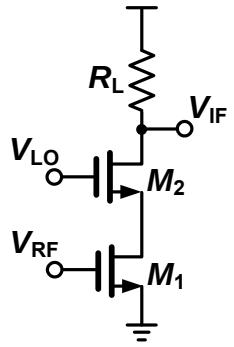


Fig.5.2 Schematic of a cascode mixer

However, similar to the Gilbert cells, the cascode mixers can only provide a low gain. To overcome this issue, the same idea of high gain distributed amplifier discussed in section 3.5 is utilized in distributed mixer design. Two cascade common source stages provide the high gain. A cascode transistor provides the frequency translation. The proposed distributed front-end is shown in fig. 5.3

There are totally three artificial transmission lines at RF, LO and IF ports in the proposed design. The ultra wideband matching at RF and LO ports can be automatically achieved by the proper design of the artificial transmission lines. Since the IF frequency is low, output matching at IF port could be easily satisfied. Three terminal resistors are connected at the terminations of the three artificial transmission lines to prevent the signal from reflecting back. There are totally three stages in each mixing element. Each mixing element consists of a common source transistor and two cascode transistors. The

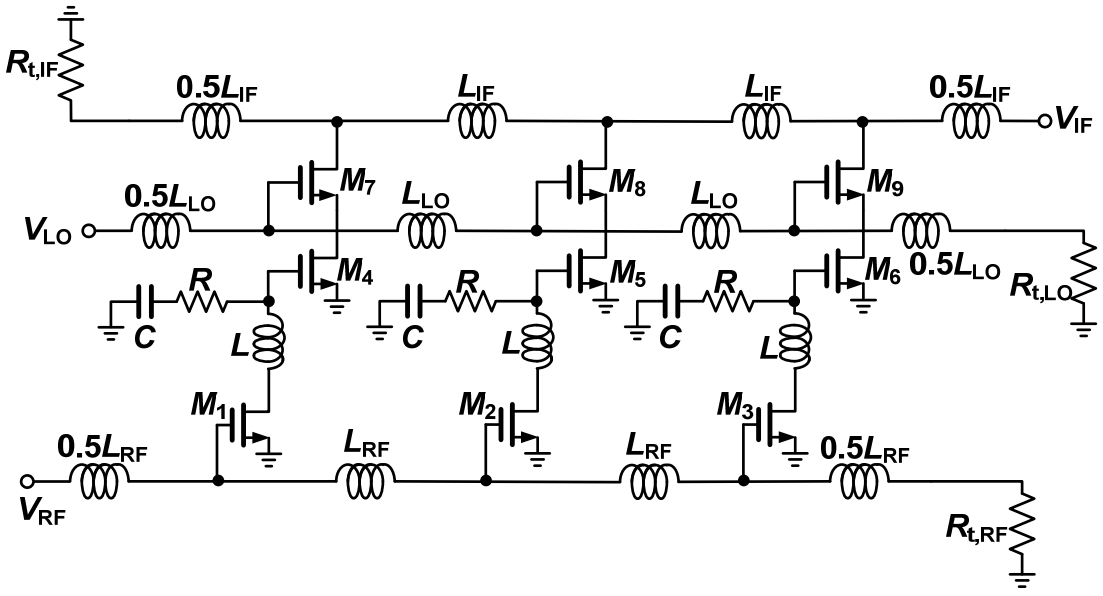


Fig. 5.3 Schematic of the proposed distributed front-end

common source transistor is mainly for low noise amplification, providing a gain and lessening the noise effect from the following stages. The lower transistors in the cascode structure also contribute some gain, while the upper one works as a switch, performing the frequency translation by turning the current on and off at the frequency of LO. Hence, the RF input signal is amplified by M_1 and M_4, and mixed with LO signal at M_7, then the IF signal goes to the output port.

Compared with the distributed mixer shown in fig. 5.1, the proposed distributed frond-end can provide much higher gain, and lower noise figure because of the existence of one more common source transistor at RF input. And also, since only signal-ended RF and LO inputs are required, only three artificial transmission lines are needed, while five artificial transmission lines have to be designed in the distributed mixer shown in fig. 5.1. The less number of artificial transmission lines leads to the less number of inductors, and hence, small chip area. However, it also has drawbacks. Since only single-ended RF and LO are used at the input, they will inevitably appear at the IF output. While for a double balanced mixer, the RF and LO components appear at IF port only as common mode signals and can be cancelled by the differential IF configuration. Although the leakage from RF and LO to IF port can be huge, it can be easily eliminated by a low pass filter, as either RF or LO is at a much higher frequencies comparing with that of the IF. For example, the RF input frequency for the UWB application is 3.1-10.6 GHz. The LO frequency is in the same range as RF, while the IF signal is only 512MHz around DC. This makes it extremely easily for a low-pass filter to attenuate the RF and LO signals at the IF output.

The conversion gain of the proposed distributed front-end can be estimated as the same as that of the distributed amplifier in section 3.5, based on the assumption that the cascode transistors are acting like perfect switches. However, in most situations, the cascode transistors are not acting like perfect switches. The mixer actually acts some what like a multiplier, which has an output of

$$v_{out} = A \cdot V_{RF} \cos(\omega_{RF} t + \phi) \cdot V_{LO} \cos(\omega_{LO} t) \tag{5.1}$$

where V_{RF} is the RF amplitude, V_{LO} is the LO amplitude, ω_{RF} and ω_{LO} are the frequency of RF and LO signals, A is the gain from RF port to the IF port, which is normally proportional to the transconductance and load resistance of the mixers. It would be easy to say that the conversion gain of this mixer is also affected by the voltage swing of the LO signal.

The bandwidth of the proposed distributed front-end is the same as the bandwidth of the distributed amplifier in section 3.5, since the dominant factor to determine the bandwidth is the R,L and C network between M_1 and M_4, M_2 and M_5, M_3 and M_6, instead of the cut off frequency of the artificial transmission lines.

5.2.2 Circuit Performance

The proposed distributed front-end was designed and fabricated in Jazz 0.18μm CMOS process. All inductors were designed and calculated in IE3D. The simulation was made with ADS harmonic balance.

The simulated conversion gain of the proposed distributed front-end is shown in fig. 5.4. The simulation was made by fixing the IF frequency at 500 MHz, and making

LO frequency to be 500 MHz lower than RF frequency. When the RF frequency changes from 2 GHz to 20GHz, the LO frequency keeps tracking the RF frequency and maintains 500 MHz lower than RF frequency. By assuming a LO power of 5 dBm, a relatively flat gain of 12-14dB can be observed from 2-17 GHz. Compared with the distributed mixer in fig.5.1, which has a gain of 2.5-5dB from 4-8.72 GHz, the gain and bandwidth of the proposed distributed front-end are quite good.

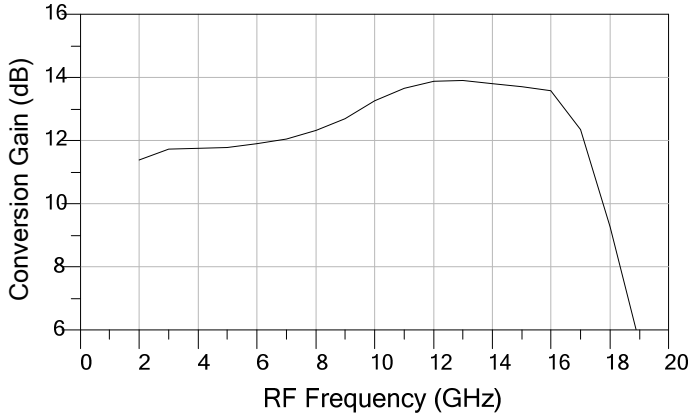


Fig. 5.4 Simulated conversion gain of the proposed distributed front-end (P_{LO}=5dBm, P_{RF}=-30dBm)

The matching at RF, LO and IF ports is plotted in fig. 5.5. The simulation is made with the whole circuit properly biased. Like all the distributed circuit, wideband matching can be easily acquired. The results show that the return loss at both LO and RF port through 2-12GHz is less than -10dB. Since the IF port handles only low frequencies, output matching at high frequencies can be sacrificed for the gain. Nonetheless, it also has a return loss less than -10dB at frequencies lower than 1GHz.

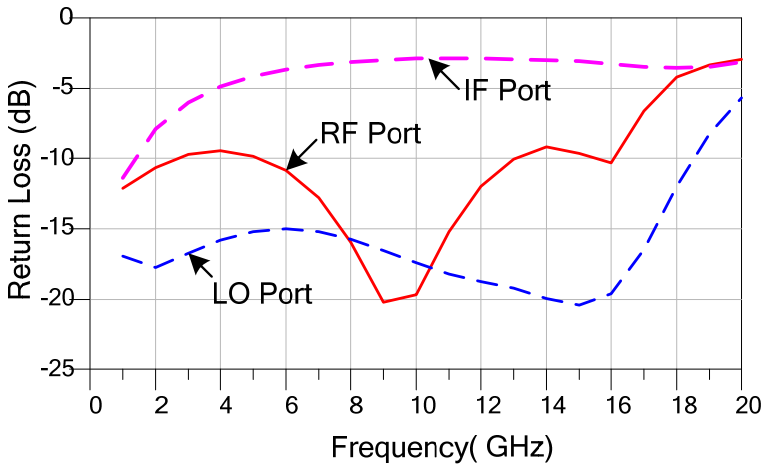


Fig. 5.5 Return loss of the proposed distributed front-end
(With each port proper biased)

The noise figure of the distributed front-end is shown in fig 5.6. Around 5-6dB noise figure can be achieved from 3-12GHz.

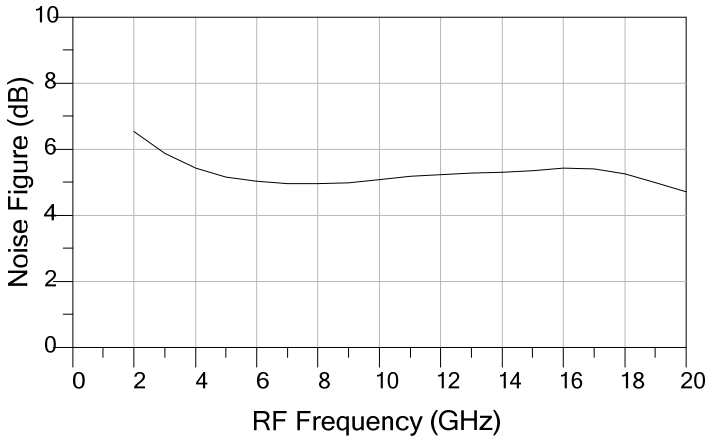
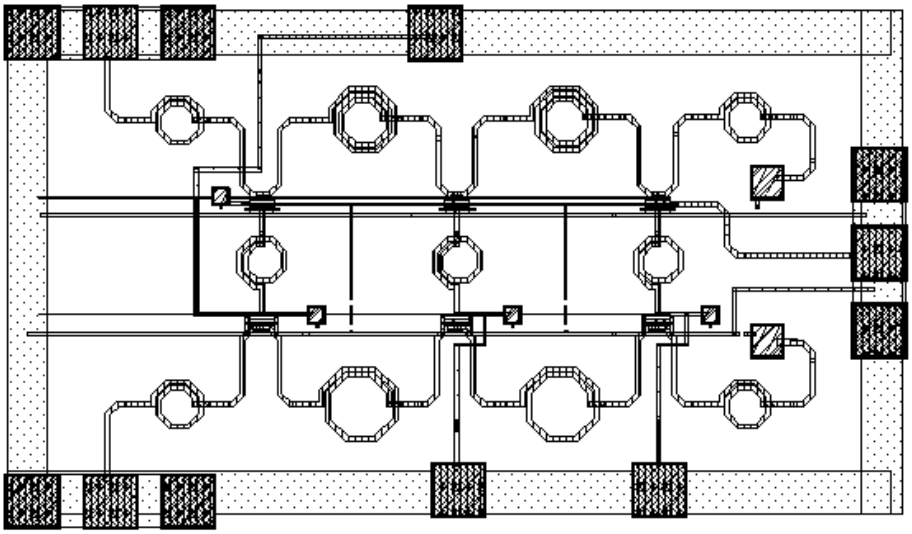


Fig. 5.6 Simulated Noise figure of the proposed distributed front-end

All the simulation was made at LO power of 5dBm and current consumption of 170mA. The microphotograph of the distributed front-end is shown in fig. 5.7. The total chip area is $1.7\times1.0mm^2$.



(a)

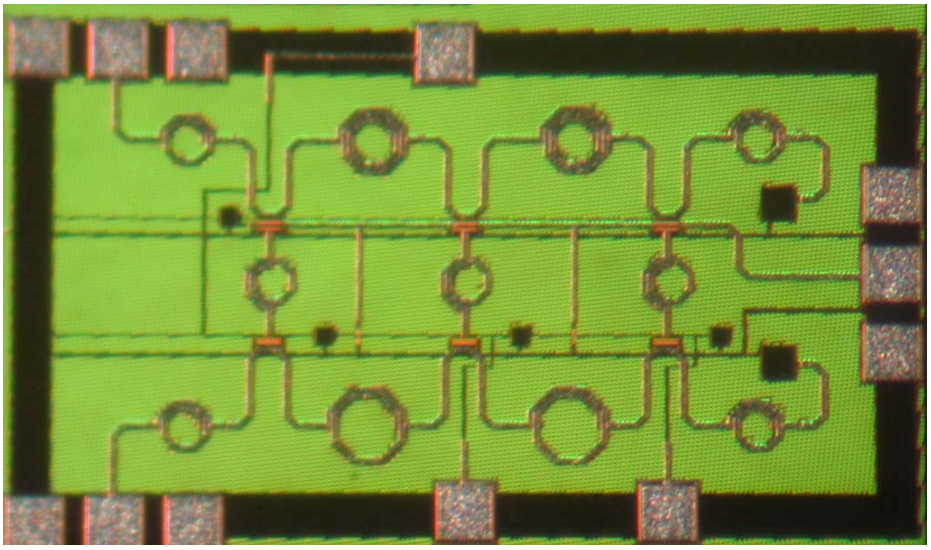


Fig. 5.7 Layout and microphotograph of the developed distributed front-end: (a) Layout of the developed distributed front-end (b) Microphotograph of the developed distributed front-end

5.3 A CMOS Front-End for UWB Application

As discussed in the previous sections, distributed circuits can easily overcome the gain bandwidth limit and extend the bandwidth beyond the UWB requirement by the idea of artificial transmission lines. However, the costs are high power consumptions and large chip areas. With the CMOS technology continuously improved, CMOS transistors with much higher f_t and high Q inductors are available for the RF designers. These make it possible for the design of the UWB receiver circuit without using distributed structures. The wideband matching network can be constructed with on-chip lump elements.

In section 4, a CMOS UWB LNA with resistive shunt feedback technique has been developed. The proposed LNA with only two inductors in the design can also achieve UWB bandwidth at a current consumption of only 5mA. Based on this UWB LNA, a new UWB front-end has been developed.

5.3.1 Circuit Design

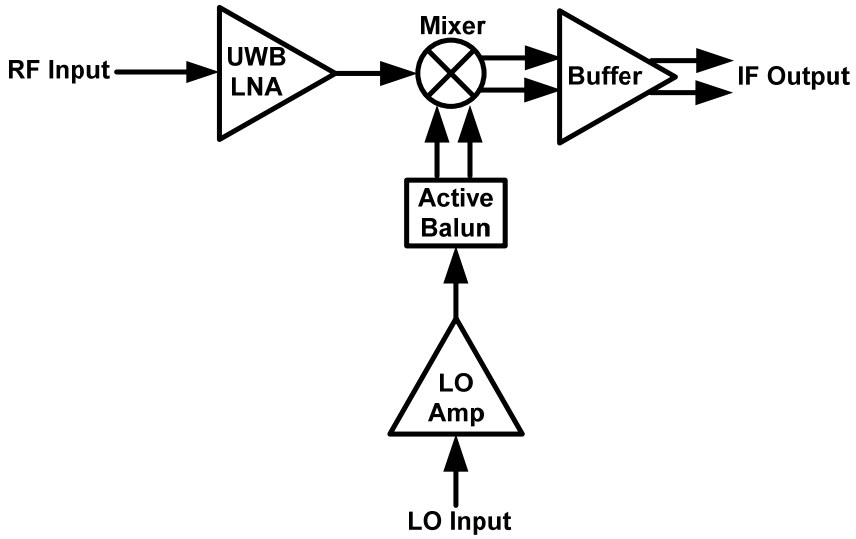


Fig. 5.8 Block Diagram of the proposed UWB front-end

The proposed UWB front-end, depicted in fig.5.8, consists of a UWB LNA and a single-balanced mixer. The advantage of using a single balanced mixer is that the single-ended RF input from the antenna can directly go through from the UWB LNA to the RF input of the mixer, which is also single-ended. Hence, no single-ended to differential circuit will be needed. As we know the single-ended to differential circuit is difficult to design over the entire UWB frequency range, for its frequency is relatively high and extremely wide bandwidth. However, the mixer does need differential LO signal to generate differential IF output. In the real receiver, differential LO signal can be acquired directly from the integrated frequency synthesizer by implementing differential VCO. In our design, an integrated frequency synthesizer will not be included. The differential LO input at the mixer has to be generated from the frequency synthesizer in

the lab, which only has a single-ended output. A balun working through the UWB frequencies has to be designed for the testing. Also because the LO generator is off-chip, the LO input port impedance matching must be considered to maintain the maximum power transfer. In order to compensate the possible loss through the cable and PCB board, a LO amplifier is placed at the input of the LO, before the balun. This LO amplifier will provide both the input matching and gain to compensate the loss. At the output of the mixer, a buffer is used to drive the 50-Ohm load, which is the input impedance of the measurement equipment.

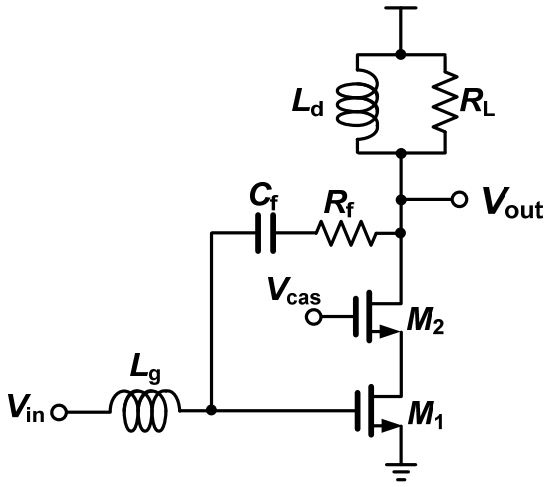


Fig. 5.9 Schematic of the UWB LNA

The schematic of the UWB LNA is shown in fig.5.9. It has been discussed in the previous section. Since the output of the UWB LNA is directly connected with the RF input of the mixer, which is high impedance, no output buffer is needed.

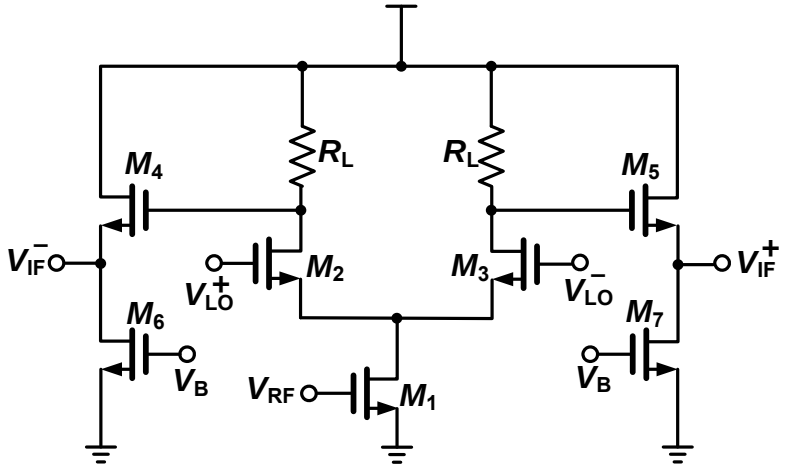


Fig. 5.10 Schematic of the single balanced mixer with the output buffer

The single balanced mixer, integrated with an output buffer, which is simply a source follower, is shown in fig.5.10. The single balanced mixer allows the usage of the single-ended RF signal and facilitates the front-end design by eliminating on-chip balun in the receiver circuit. The output of the UWB goes directly into the RF input of the mixer. The transistor M_1 acts as a transconductance amplifier, which transfers the input voltage into the current that flows through its drain and source. As the differential LO signal comes into the gate of transistors M_2 and M_3, the current in them is turned on and off at the frequency of LO. In this way, the RF and LO signals are mixed and all of their mixing products appear in the currents through M_2 and M_3. The load resistor R_L transfer this current into the voltage, which is known as the IF output. From the analysis above, it is easy to get a conclusion that the conversion gain of the mixer is mainly depend on the transconductance of M_1 and the load resistance R_L. However, the assumption is M_2 and

M_3 are acting like perfect switches. To that end, higher LO signal swing and wider devices are desired.

In this design, the second stage of the mixer is simply a source follower to provide some output current in order to drive a 50-Ohm load.

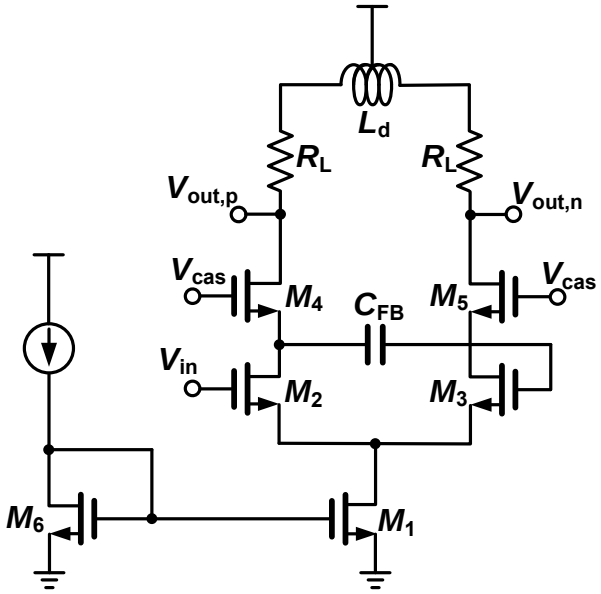


Fig. 5.11 Schematic of the active balun

The active balun, shown in fig. 5.11, is used to bring the single-ended LO signal into differential signals. The circuit is just a differential amplifier driven by a single-ended signal. If the operation condition is ideal, the circuit can give a perfect differential output. However, the impedance of the non-ideal current source is not high enough, resulting in unequal signal distribution in M_2 and M_3, thereby leading to imbalance in the differential output. The imbalance can be mitigated by the feedback path formed by a capacitor C_{FB}. A Cascode topology is used in order to isolate the active balun circuit from variations in the load. The inductor L_d in the load of the active

balun compensates for the effect of the parasitic capacitance at high frequencies and increases the impedance, leading to increased gain. A differential inductor is used as L_d for its high Q and easy integration.

5.3.2 Circuit Performance

The proposed UWB front-end was designed and fabricated in Jazz 0.18μm CMOS process. All the inductors were designed and calculated in IE3D. The simulation was made both with Cadence spectrum and ADS harmonic balance.

The simulated and measured conversion gain is plotted in fig 5.12. The simulation and measurement are made with the RF power of -30dBm and LO power of -10dBm. Same as before, the IF frequency is fixed at 250 MHz. RF frequency and LO frequency are changing from 2-20 GHz. Unlike the distributed front-end, the gain of the proposed front-end is not flat over UWB frequencies. This is because that the parasitic capacitance at each node in the circuits could not be cancelled out by lumped elements, as compared to distributed topologies. The measurement results show the gain dropped by 2-3dB at around 6GHz. This may be because the input matching is not very good at the same frequency, which leads to less power into the input port. Nonetheless, the gain is over 12dB through 3-10 GHz. While the measurement shows 10-14dB gain through 2-10 GHz.

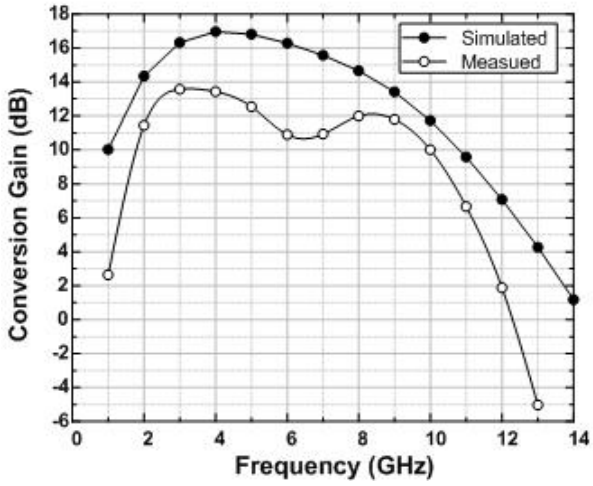


Fig. 5.12 Measurement conversion gain of the UWB front-end
(P_{RF}= -30dBm and P_{LO}= -10dBm)

Fig 5.13 shows the measurement input matching at both RF and LO ports at the power level of -10dBm. As the same UWB LNA was used at both the RF and LO ports, they gave the same input matching results. RF port matching is very important in receiver designs, since it allows the maximum power transfer from the antenna. The LO port matching is also very important. By using the resistive shunt feedback, the proposed UWB front-end can achieve a return loss of less than -8dB from 3-10GHz at both RF port and LO port. The difference between the measurement results and the simulation one may be caused by the parasitic capacitance of the input pads, which is taken into the effect in simulations.

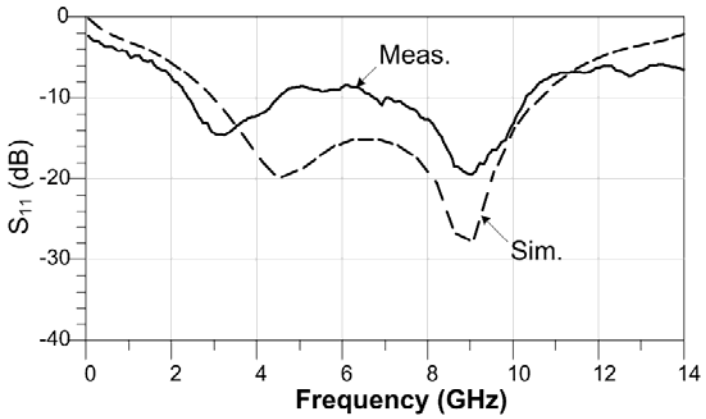


Fig. 5.13 Measurement Return loss of the proposed UWB front-end

The noise figure of the developed UWB front-end is shown in fig 5.14. The simulation results show that the noise figure is around 8-10dB. While the measurement results are roughly 2dB higher. This is because that the actual gain is lower than the gain in simulations. Compared with the noise figure of the distributed front-end, the noise figure of the proposed UWB front-end is a little bit high. However, the power consumption is only 25mA when comparing to 170 mA for distributed structure.

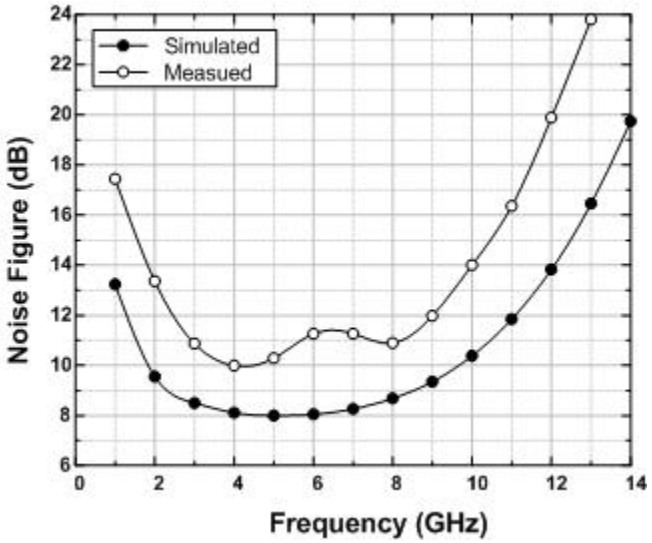
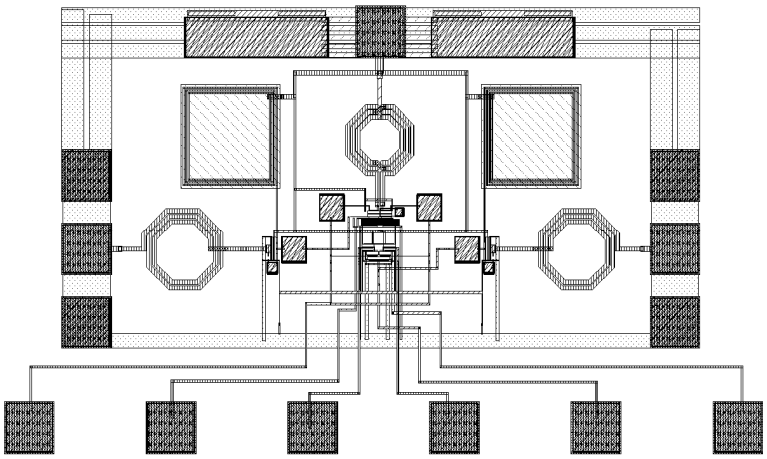


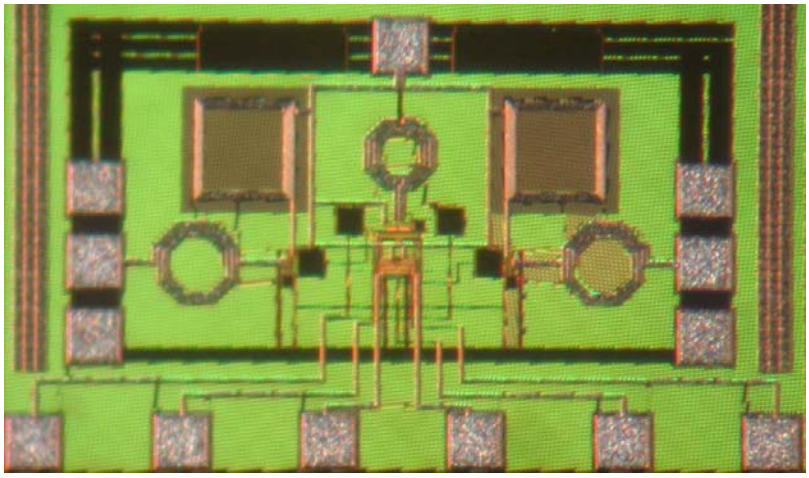
Fig. 5.14 Measurement Noise Figure of the proposed UWB front-end
(P_{RF}= -30dBm and P_{LO}= -10dBm)

The layout and microphotograph of the proposed UWB front-end is shown in fig 5.15(a) and 5.15(b), respectively. The total chip area is 1.0×1.7mm^2.



(a)

Fig. 5.15 Layout and microphotograph of the developed UWB front-end: (a) layout of the developed UWB front-end



(b)

Fig. 5.15 continued (b) Microphotograph of the developed UWB front-end

5.4 Conclusion

In this section, two UWB front-ends with two different topologies have been proposed and investigated. A distributed LNA-Mixer is presented. Unlike the conventional distributed mixer, which can only deliver low gain and high noise figure, the proposed distributed LNA-Mixer demonstrates 12-14dB gain ,4-5dB noise figure and higher than 10dB return loss at RF and LO ports over 2-16GHz, with a fixed IF frequency of 250 MHz and LO power of 5dBm. The entire circuit consumes 170mA from 1.8V voltage supply. To overcome the power consumption and chip area problems encountered in distributed circuits, another UWB RF front-end is also designed with lumped elements. This front-end, employing resistive shunt-feedback technique into its LNA design, can achieve a gain of 14dB, noise figure of 10-14dB through 2-10GHz, and return loss of less than -8dB from 3-10GHz at both RF and LO port, while only consuming 25mA current from 1.8V power supply.

6. CONCLUSION AND SUMMARY

The Ultra-Wideband communication system provides a large bandwidth and extremely high data rate, but also posts a very big challenge for the CMOS designers. This dissertation explores various techniques to implement such systems in low-cost, high integration level, and high yield silicon-based technologies.

Distributed amplifiers in CMOS process have been investigated from different aspects. A traditional distributed amplifier utilizing CPW transmission lines has been designed, demonstrated in commercial available 0.25-μm CMOS process. This amplifier can achieve 6dB gain and more than 13dB return loss. Measurement results performed in time domain demonstrate this amplifier's output waveforms resemble closely those at the input with very little distortion, proving that it is appropriate for time-domain UWB applications. Some efforts have been focused on reducing the chip area and minimizing the power consumptions. A compact CMOS distributed amplifier with Patterned Grounded Shield (PGS) inductor was developed. The increased isolation obtained with the PGS inductors makes it possible for the inductors to be placed very close to each other, resulting in significant reduction of circuit area. With the high Q achieved by the PGS inductors, the distributed amplifier exhibits good performance with a relatively flat gain of 7 dB and input, output return losses higher than 10 dB from DC-11 GHz, which could possibly be the best performance that can be achieved in standard low-cost 0.25-μm CMOS processes. The developed CMOS distributed amplifier demonstrates a useful approach in designing compact, high-performance wide-band CMOS distributed

amplifiers as well as other broadband CMOS RFICs by using on-chip PGS inductors, particularly for those containing many inductors. To address the high power consumption suffered in distributed amplifiers, a new low power-consumption design approach has been presented. The new design employs cascade of common-source gain cells with peaking inductance to provide substantially enhanced transconductance and gain over the entire UWB frequency of 3.1-10.6 GHz. This 0.18-μm CMOS distributed amplifier can achieve the lowest power consumption, with decent gain compared to the best gain reported, over the entire UWB band. It can also achieve good input match, and good noise figure similar to the best published noise figure. It exhibits the highest gain ever reported across the UWB range with good noise figure when operated in the high-gain mode.

A resistive shunt feedback low noise amplifier has been implemented in CMOS 0.18-μm process. With only two inductors and only 9mW power consumption, this UWB LNA can provide a maximum gain of 10.5dB, noise figure of 3.3-4.5 dB and -8dB input matching through 3-10GHz. The performance of the proposed UWB LNA is among the best published results.

Based on the distributed amplifier and resistive shunt feedback amplifier designs, two UWB RF front-ends were developed. One is a distributed LNA-Mixer. Unlike the conventional distributed mixer, which can only deliver low gain and high noise figure, the proposed distributed LNA-Mixer demonstrates 12-14dB gain, 4-5dB noise figure and higher than 10dB return loss at RF and LO ports over 2-16GHz, with a fixed IF frequency of 500 MHz and LO power of 5dBm. The entire circuit consumes 170mA

from 1.8V voltage supply. To overcome the power consumption and chip area problems encountered in distributed circuits, another UWB RF front-end was also designed with lumped elements. This front-end, employing resistive shunt-feedback technique into its LNA design, can achieve a gain of 12dB and noise figure of 8-10dB through 3-10GHz, the return loss of less than -10dB from 3-10GHz at RF port, and less than -7dB at LO port, while only consuming 25mA current from 1.8V voltage supply.

6.1 Recommendations for future works

Our research work has proven the feasibility of the fully integrated distributed circuits being low-power and compact in chip area. With the CMOS process continuously improving, extremely wideband, low power distributed circuits can be implemented in the future. Distributed circuit, with its special architecture and intrinsic wideband character, will find more and more applications, such as power amplifiers and oscillators. And also, to design a distributed amplifier with extremely low noise will still be a very good topic.

For UWB communications, different techniques have been investigated to achieve the wideband power match and gain. Future work can be done to investigate the optimization of the noise performance in the wideband.

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VITA

Xin Guan was born in Beijing, China. He received his B.S. and M.S. degrees in Electrical Engineering from Tsinghua University, Beijing, China in 1999 and 2002 respectively. In Aug 2002, he joined the Sensing, Imaging and Communications Lab at Texas A&M University, College Station, Texas, to pursue his Ph.D. in the field of CMOS RFIC design. From May 2007 to August 2007, he did his internship as an RFIC design engineer at Axiom Microdevices Inc, Irvine, California. He received his Ph.D. in May 2008. He has focused his research interests on RF, microwave and millimeter-wave RFICs for wireless communications and sensing applications.

Dr. Xin Guan may be reached via Professor Cam Nguyen, Department of Electrical and Computer Engineering, Texas A&M University, College Station, TX 77843-3128.

The typist for this dissertation was Xin Guan.