

**A LOW POWER PRESCALER, PHASE FREQUENCY DETECTOR, AND  
CHARGE PUMP FOR A 12 GHZ FREQUENCY SYNTHESIZER**

A Thesis

by

EVAN LEE ESCHENKO

Submitted to the Office of Graduate Studies of  
Texas A&M University  
in partial fulfillment of the requirements for the degree of  
MASTER OF SCIENCE

December 2007

Major Subject: Electrical Engineering

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**ABSTRACT**

A Low Power Prescaler, Phase Frequency Detector, and Charge Pump for a 12 GHz  
Frequency Synthesizer. (December 2007)

Evan Lee Eschenko, B.S., Texas A&M University

Chair of Advisory Committee: Dr. Kamran Entesari

A low power implementation of a CMOS frequency synthesizer at 12 GHz is an important step to improve the efficiency of a wireless transceiver in this frequency band. Since synthesizers are often employed as reference frequency sources such as local oscillators for up or down-conversion in communications system, their design is especially important for high performance transceiver applications. CMOS PLLs operating at high frequencies consume large amounts of power for proper operation, making power efficiency a top priority in transceiver implementation. In response, this thesis presents a low power phase and frequency detector with True Single Phase Clocking by employing the  $.18\mu$  TSMC process with a 1.8 V supply voltage. A conventional but extremely power efficient nano-watt charge pump is also implemented for additional power savings. Furthermore, a state of the art 16/17 prescaler using Current Mode Logic (CML) D-Flip Flops, CMOS inverters, and transmission gates has been optimized for maximum power savings. The prescaler consists of a 4/5 synchronous core and a feedback loop which modulates the 4/5 core to produce a division ratio of 16/17. Instead of employing power hungry CML, the feedback circuit takes advantage of low power NOR and AND gates realized in Transmission Gate Logic (TGL) to reduce the power consumption. To the best of my knowledge, this technique has never been used in a high frequency prescaler before.

## **DEDICATION**

To my parents Hal and Lindy Eschenko, grandparents George and Maxine Bellos  
and my sister Tina Everett and her family and of course Thu Ho

## ACKNOWLEDGMENTS

I would like to thank Dr. Kamran Entesari for his guidance and support throughout the course of my thesis work. The weekly meetings I had with him gave me invaluable insights into mixed signal design and helped me appreciate the joint effort that goes into the design of a complex system.

I would like to express my sincere gratitude to Dr. Jose Silva for strengthening my understanding of prescaler design. The numerous discussions I had with him have greatly contributed toward the successful completion of my thesis.

Also, I would like to thank Dr. Peng Li and Dr. May Boggess for participating on my committee.

I am deeply thankful for all the support of my family and friends.

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## I INTRODUCTION

### 1. Frequency Synthesizers and Their Building Blocks

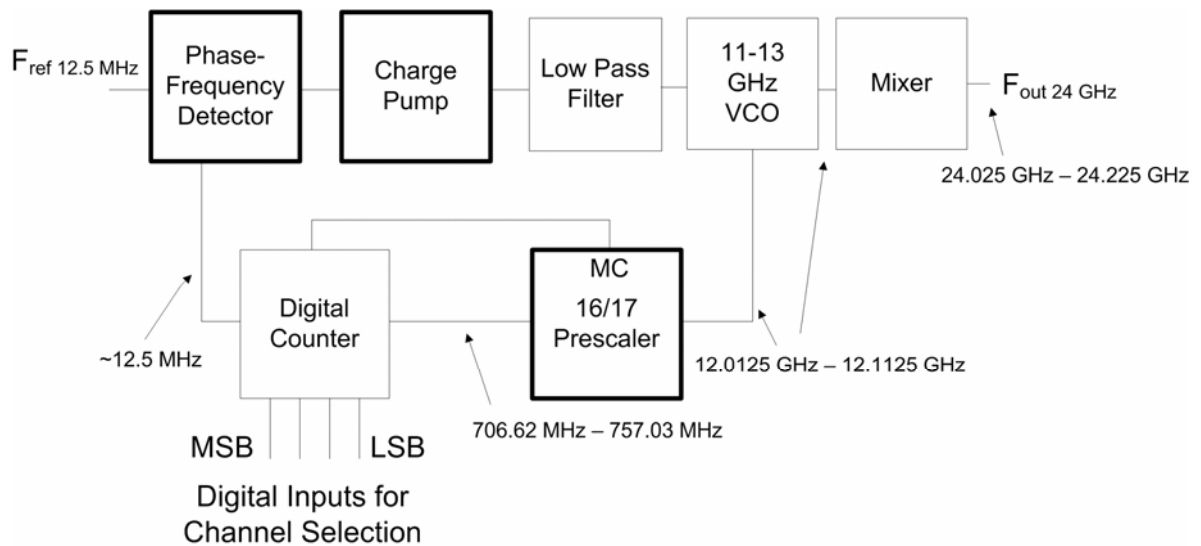
Frequency synthesizers are found in a variety of circuits such as wireless communication transceivers [1]. They provide the stable reference frequency source for RF mixers and the central processing units found in all computers [2]. Without synthesizers, stable frequencies could not be produced higher than frequencies achievable from the excitation of crystals into oscillators. The frequency synthesizers can take a low frequency generated from a crystal oscillator and multiply it by an adjustable number to produce a much higher frequency[2]. The accuracy of frequency generated is very close to the high precision of a crystal oscillator. The frequency multiplication factor can be made adjustable to create communication transceivers with multiple channels [2-3]. Furthermore, synthesizers are used to synchronize clock signals between communication devices to allow digital information transfer[2].

### 2. Research Objectives

The primary objective of this thesis is to design a robust, low noise, high frequency prescaler, a phase frequency detector (PFD) and a low power and accurate charge pump as part of a larger project under Dr. Kamran Entesari, which entails an entire 24 GHz frequency synthesizer. The high frequency nature of the synthesizer calls for a phase-locked loop (PLL) implementation at the transistor-level for the .18u TSMC process with a 1.8 V supply voltage. All three blocks will strive for low power consumption and state of the art operation. The blocks must also satisfy the system level behavior for the 24 GHz ISM wireless band (24.025 GHz - 24.225 GHz). The system level analysis was performed by Dr. Gang Bu and is summarized in Table 1.

**Table 1: Desired System Performance**

Frequency Band	24.025 GHz – 24.225 GHz
Channels	9
Channel Spacing	25 MHz
Channel Frequencies	24 GHz + n*25 MHz, n=1~9
Settling time	< 50 uS
Accuracy	20 ppm (480 KHz)

**Figure 1: Block Diagram for 24 GHz Frequency Synthesizer**

The highlighted blocks in Figure 1 are the responsibility of this research project with specific emphasis on the 16/17 prescaler due to difficulty of implementing a prescaler at frequencies above 10 GHz with a .18  $\mu\text{m}$  CMOS process. The PFD and charge pump are less challenging as they operate at much lower frequencies. The prescaler layout will be generated and simulated using Cadence, then fabricated and

tested on chip. The phase frequency detector and charge pump will be verified only through simulation.

### **Primary Objective**

Desired System Performance for all corners (fast, typical and slow)

### **Secondary Objectives**

1) Low Noise

Small Number of Noise Generating Components

Limited Noise Bandwidth

High Slew Rate

2) Low Power Consumption

Minimize DC Current usage

Arrange layout to minimize parasitics on signal path

Reduces required transconductance and therefore bias current

Avoid over-design of subcircuits with low performance requirements

3) Small Chip Area

Use minimum size devices if possible

4) Small Input Capacitance to Reduce VCO Power Consumption

Multiple Stage Pre-amplifier

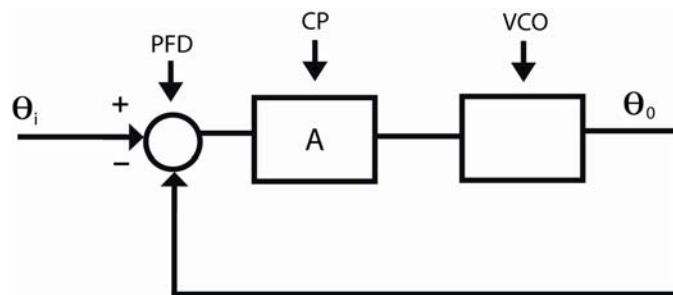
The following sections will introduce the individual blocks and their functions. The last section highlights some important practical considerations about the design of the individual blocks, which are deduced from the system level specifications.

### 3. Phase-Frequency Detectors

The general function the phase-frequency detector (PFD) is to compare the input reference signal to the VCO output signal and output is a representation of the time or phase difference of the changes in the signals [4]. The primary measure of the effectiveness of a PFD is the size of the dead zone [5]. Dead zone can be defined as the situation where there is a difference between the VCO output signal and the input reference signal but the PFD output does not change. The effect of employing a PFD with a dead zone is reduced frequency stability manifested as sub reference spurs appearing in the frequency content of the VCO output. When the phase difference enters the dead zone, the VCO control voltage is not updated on for that cycle of the reference frequency. The usual periodic updating of the VCO control voltage results in a reference spurs which are located in the frequency spectrum a distance of one reference frequency away from the carrier [6].

### 4. Charge Pumps for Phase Locked Loop

The general function for the charge pump (CP) in a PLL is to provide a large open-loop gain by pumping charge into the loop filter [7]. The amount of charge pump is proportional to the amount of phase difference detected by the PFD. Since the capacitor is an open circuit for direct current (DC), charge accumulates very quickly and results in a large DC gain, which causes the final steady state phase error between the input and the output to be very small [8].



**Figure 2: Simplified Block Diagram of PLL**



A simplified diagram of a phase locked loop is shown Figure 2. Note that the low pass filter is considered as part of the charge pump. If  $A$  represents the open-loop gain of a phase-locked loop then the relationship between the input and output phase is shown in the following equation.

$$\frac{\theta_{out}}{\theta_{in}} = \frac{A}{1 + A} \quad (1)$$

The theoretical DC gain for a charge pump based PLL is infinite however in practice this is impossible [9].

## 5. Dual-Modulus Prescaler

A high frequency prescaler is arguably the most challenging block in phase-locked loop (PLL) design especially in the gigahertz range. Common benchmarks for performance are focused on wide input bandwidth for greater PLL acquisition range, low phase noise for PLL frequency stability and low power consumption for mobile applications[10-14]. LC injection locked dividers can provide very high frequency operation but their small locking bandwidth is impractical and comes at the large area cost of inductors [15-16]. Most low power dynamic dividers fail at high frequencies [17] and miller dividers are typically power hungry [18]. Therefore, a middle ground is found by employing current mode logic which balances speed with power [19].

Efficient high speed circuits can be realized by careful matching of the type of logic employed to the expected operating frequency. The proposed 16/17 prescaler has a feedback loop that operates at a much lower frequency than the core. For maximum efficiency, the core will be composed of CML while the feedback loop can take advantage of the much lower power TGL.

In PLL design, a low noise solution is of utmost importance because it will generate a more stable reference frequency. The phase noise of the prescaler can be minimized by maximizing the slew rate of the prescaler output stage [20]. Neither CML

nor TGL produce signals suitable for a maximum slew rail-to-rail output stage. CML does not provide rail to rail operation and TGL can just drive high impedance nodes because it merely passes or holds current with no current-producing capability in itself. The most efficient and natural choice for the output stage in this prescaler is employing CMOS inverters.

## 6. Individual Block Design Considerations

The phase locked loop system level behavior provides insight into how each block must operate for smooth functioning of the entire system. For instance, the phase frequency detector must operate within minimum frequency range (11.9 MHz to 13 MHz), the charge pump must provide a certain current flow (0 or +/- 40  $\mu$ A) and the prescaler must maintain a correct division ratio (16/17). Table 2 provides information regarding the different synthesizer block specifications under research for this thesis and a more detailed explanation follows the table.

**Table 2: Required Block Specifications**

Parameter	Value
Charge Pump Current	40 $\mu$ A
VCO Gain	500 MHz/V
Range of Selectable Division Ratio From VCO to PFD	961-969
PFD Operating Frequency Range	11.9-13 MHz
Minimum Prescaler Division Ratio	9/10
Minimum Prescaler Input Range	11 GHz to 13 GHz

The charge pump current value is a result of the entire system-level phase locked loop analysis.

The selectable division ratio can be computed by dividing the desired VCO output frequency by the reference frequency. The target VCO output frequency is given at 12.0125 GHz and the desired channel spacing is 12.5 MHz due to the ISM band standard, leading to division ratios of 961 to 969.

For a reference frequency of 12.5 MHz, a VCO gain of 500 MHz/V and a power supply of 1.8 V, the maximum frequency seen by the phase-frequency detector can be computed by the following formula.

$$f_{\max@PFD} = \frac{f_{VCO\ Free\ Running} + (Max\ Swing\ VCO\ Control \times VCO\ Gain)}{Minimum\ Division\ Ratio} \quad (2)$$

$$= \frac{12\ GHz + \left( .9V \times 500 \frac{MHz}{V} \right)}{961} = 12.96\ MHz \quad (3)$$

The Max Swing on the VCO control line is set to .9 V because VCO control voltage is limited to values between zero and 1.8 V and the synthesizer is designed to operate at the center of the supply voltage. The maximum PFD operating frequency is close to the nominal operating reference frequency (12.5 MHz) and can be easily managed by most PFD architectures. To allow for some margin, the minimum PFD operating frequency will be set slightly higher than the previously calculated value to 13 MHz. Due of the relative ease in achieving this performance the main design considerations for the PFD are power consumption and chip area.

The prescaler input frequency range should be large enough to accept any frequency the VCO can generate so that the acquisition range limitation is due to VCO and not the prescaler. Ideally for this application, the VCO should have a free running frequency of approximately 12 GHz when the VCO control voltage is center between the power supply rails or  $V_{dd}/2$ . Also, the VCO control voltage is limited by the rails so the maximum VCO control voltage offset is  $V_{dd}/2$ . Therefore, the VCO gain determines the maximum variation in frequency. The maximum frequency change is .9 V times 500 MHz/V or 450 MHz. The expected VCO output frequencies are 12 GHz +/- 450 MHz or 11.55 GHz to 12.45 GHz, however to allow for some margin the prescaler bandwidth will be larger at approximately 11 to 13 GHz.

The minimum prescaler division ratio can be determined by researching typical operating frequencies for digital counters. Most reported counters operate at frequencies less than 2 GHz [17]. If the prescaler division ratio is set to 9/10 the highest output frequency the digital counter will see is 13 GHz divided by 9 or 1.44 GHz, which provides some margin for proper counter operation.

This thesis contains 3 main sections. Section I discusses the phase frequency detector behavior, section II explains the charge pump and finally section III is about the prescaler implementation. Each section contains subsections that explain in detail the design taken from the gate level through the transistor level and ending in simulation results for the PFD and charge pump and measurement results for the prescaler.

## II DESIGN OF PHASE-FREQUENCY DETECTOR

### 1. Gate Level Architecture

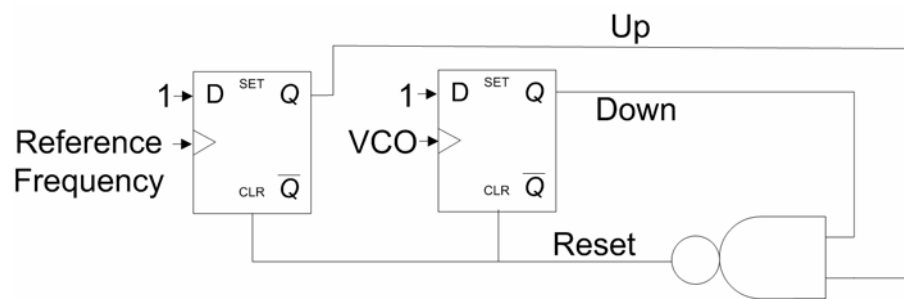
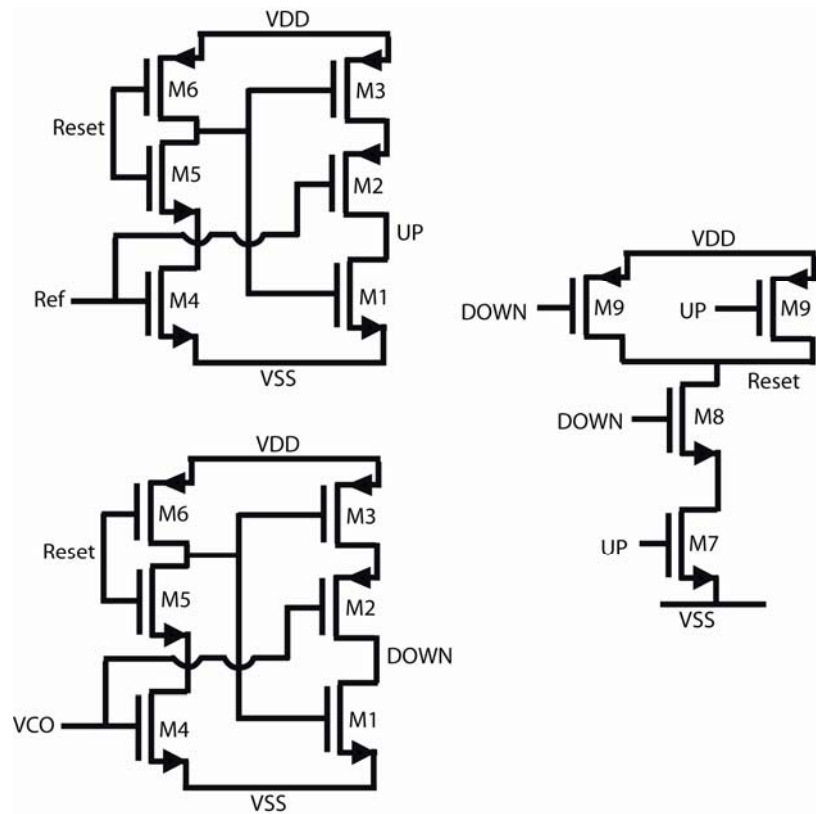


Figure 3: Reset-able Phase-Frequency Detector

In Figure 3, a digital D Flip Flop based phase detector is shown. A digital phase detector was chosen for this design because it provides low power consumption than analog based phase detectors [21] and most transistors in the circuit can be made with minimum size. The input reference frequency to the PLL is very low compared to the unity gain frequency of the technology process in most PLLs [17,19]. Because of this fact, phase frequency detectors can be implemented with minimal power and area resources and still provide a large margin in performance over required system specifications. An analog gilbert mixer phase frequency detector would provide a much higher maximum operating frequency [22] but this is not necessary and it only consumes additional power without noticeable benefit.

The explanation of the general operation of the PFD begins by describing the initial state of the device. First, the Up and Down signals are reset to low or zero and assume both the reference frequency signal and the VCO signal are high or one. Additionally, the reference frequency waveform is slightly leading the VCO waveform. When a falling edge occurs on the reference frequency input, the high or one on the D input is transmitted to the Q output or Up. A short time later, the VCO waveform experiences a falling edge and the Q output or Down of the other flip flop is set. Once both Up and Down are high or one, the NAND gate experiences a transition to force the Reset signal to zero. The flip flop are designed so that zero on the Reset signal resets the Q outputs to zero.

## 2. Transistor Level Architecture



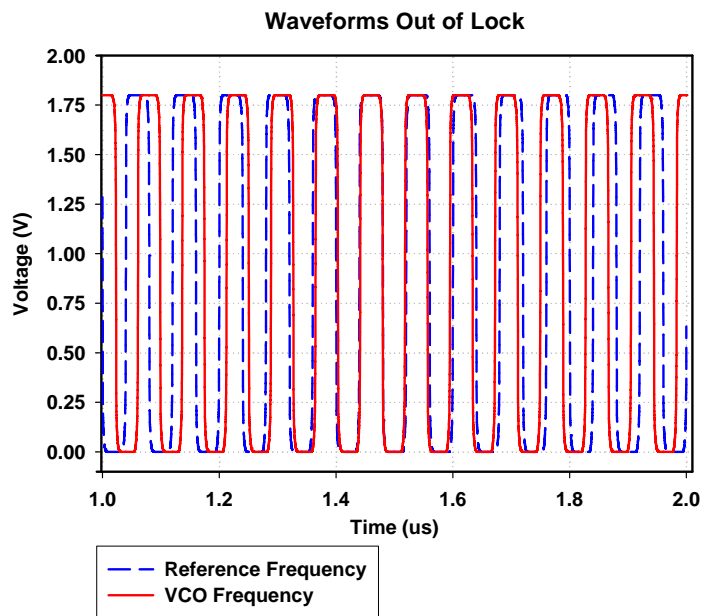
**Figure 4: True Single Phase Clocked PFD**

The PFD is implemented with True Single Phase Clocked logic as shown in Figure 4. The design strategy is to minimize the number of transistors and the amount of power consumed. However, not all of the transistors can be implemented with minimum width such as those involved in the reset operation. In Table 3, the transistor sizes for the PFD are given. Note that since the operating frequency of the PFD is quite low compared to the cutoff frequency of the technology process, most transistors can be made minimum size.

**Table 3: Transistor Sizes for Phase-Frequency Detector**

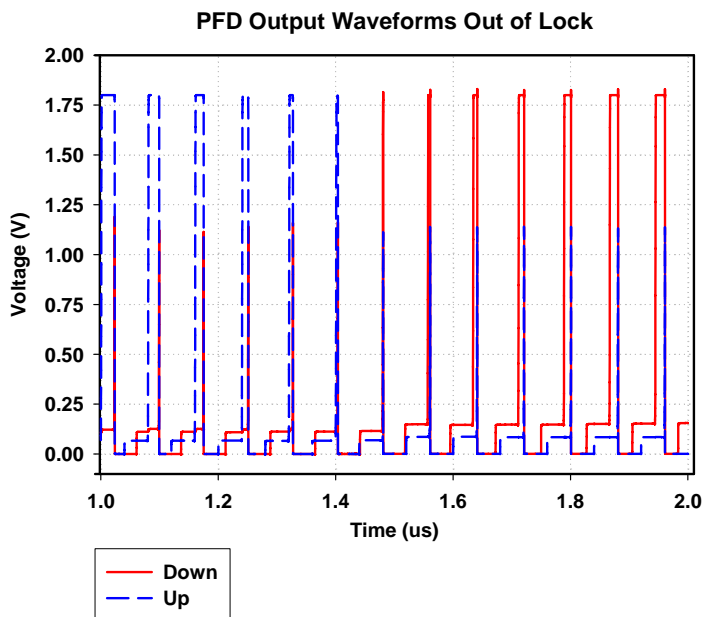
	W/L
<b>M1</b>	<b>2.2u/.18u</b>
<b>M2</b>	<b>.27u/.18u</b>
<b>M3</b>	<b>.27u/.18u</b>
<b>M4</b>	<b>.27u/.18u</b>
<b>M5</b>	<b>.27u/.18u</b>
<b>M6</b>	<b>1.35u/.18u</b>
<b>M7</b>	<b>.27u/.18u</b>
<b>M8</b>	<b>.27u/.18u</b>
<b>M9</b>	<b>.54u/.18u</b>

### 3. Phase Detector Simulation Results



**Figure 5: Input Waveform to PFD**





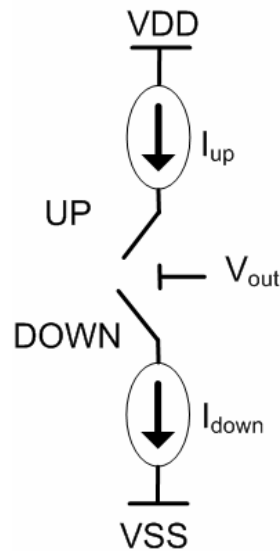
**Figure 6: Output Waveforms from PFD**

In Figure 5, we can notice that phase difference of the input waveforms of the input of the PFD changes with time. On the left side of the plot, the reference frequency leads the VCO frequency but on the right side, the VCO is leading the reference frequency. In order for the PLL to be driven to lock when the reference leads the VCO, the PFD must produce a wider pulse width on the up signal. This will cause the charge pump to raise the VCO control voltage which increases the VCO frequency. This increase in frequency will cause the VCO phase to accumulate faster than the reference phase. In a PLL, this will effectively reduce the current phase difference between the two signals.

It can be seen from Figure 6 that PFD output waveforms are correct in their relation to phase of the input signals. On the left side, the VCO would be pushed up to make up for the phase lag and on the right, we have the opposite. In the following section, the design of the charge pump will be discussed and the simulation of the joint operation of the PFD and charge pump will be shown.

### III DESIGN OF CHARGE PUMP

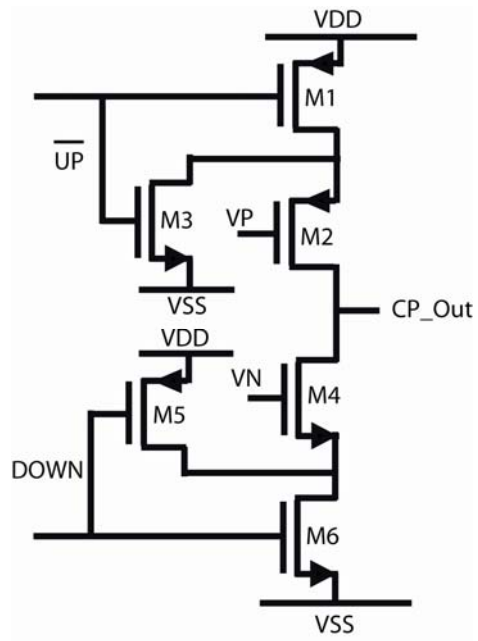
#### 1. Gate Level Architecture



**Figure 7: Conceptual Charge Pump**

The basic idea of a charge pump is to add or subtract current from the  $V_{out}$  node. The charge pump circuit and the choice of impedance to ground at  $V_{out}$ , which is also the VCO control voltage determine the dynamics of the PLL, such as DC Loop gain and tracking bandwidth [23]. Ideally,  $I_{up}$  and  $I_{down}$  should be exactly equal and there are many literatures on methods to force current matching [24]. Circuit noise at  $V_{out}$  directly appears at the output spectrum of the VCO. To limit the effect of noise at the output spectrum, the bandwidth is usually limited at  $V_{out}$  with a second order low-pass filter [25].

## 2. Transistor Level Architecture



**Figure 8: Transistor Level Charge Pump**

The implemented architecture for the charge pump is shown in Figure 8. Notice there is a cascode transistor (M2 or M4) between the input transistor (M1 or M6) and the output node, CP\_Out. These cascode transistors raise the output impedance of the charge pump which makes the charge pump circuit perform more closely to an ideal current source. The two transistors on the left (M3, M5) are not necessary for rudimentary operation but they help to absorb some of the transient currents during switching [26]. M1 provides the charge up current and M2 acts as a cascode transistor because  $V_p$  is a DC bias voltage. This cascode transistor and the NMOS transistor with gate attached to the UP bar signal (M3) help to reduce the charge injected into the CP\_Out node. Charge injection effects due to the UP bar signal can be significant because this signal typically has a high slew rate. If these extra transistors are not included, the transient current flowing through the parasitic capacitors will alter the charge at the high impedance output node, CP\_Out. This will significantly disrupt the output voltage at the CP\_Out node and should be minimized [27]. The bottom charge down (current sinking) section operates in a complementary fashion to the top charge up (current sourcing) section. The ideal function of this block is to provide an ideal supply of current to or from the output node, CP\_Out. If a current source has a low output impedance then the supplied current will vary significantly with the node voltage at the output of the current source. This variation is undesirable because we would like to provide a stable and accurate current source with the charge pump. We do that by increasing the channel lengths of the cascode transistors (M2,M4) because this will result in a higher output impedance at the CP\_Out node.

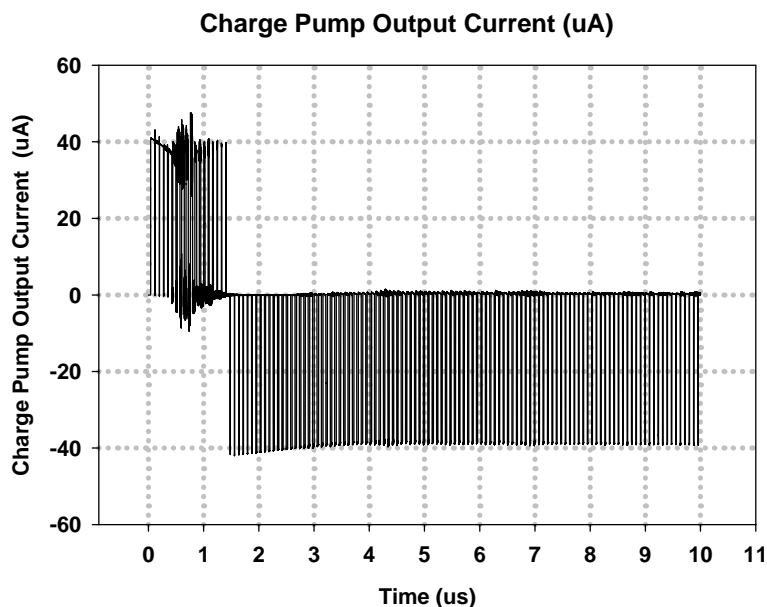
**Table 4: Charge Pump Transistor Sizes**

	<b>W/L</b>
<b>M1</b>	<b>1.35u/.18u</b>
<b>M2</b>	<b>1.11u/.36u</b>
<b>M3</b>	<b>.27u/.18u</b>
<b>M4</b>	<b>.27u/.36u</b>
<b>M5</b>	<b>1.35u/.18u</b>
<b>M6</b>	<b>.27u/.18u</b>

In Table 4, the transistor dimensions of the charge pump are shown.

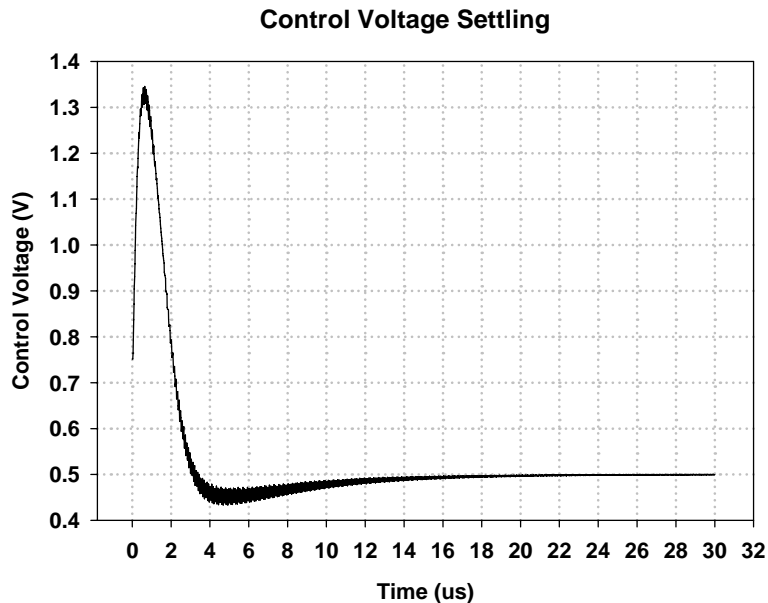
### 3. Simulation Results

The charge pump and PFD were simulated in a phase locked loop similar to Figure 2. An ideal reference frequency source and an ideal VCO were used for the simulation. Also there was no divider in the feedback loop. This was done to minimize other circuit effects, making the PFD and CP performance more visible to inspection. The input reference frequency source is set to 10 MHz and since there is no divider in the feedback loop, the VCO should settle into phase lock at a frequency of 10 MHz.



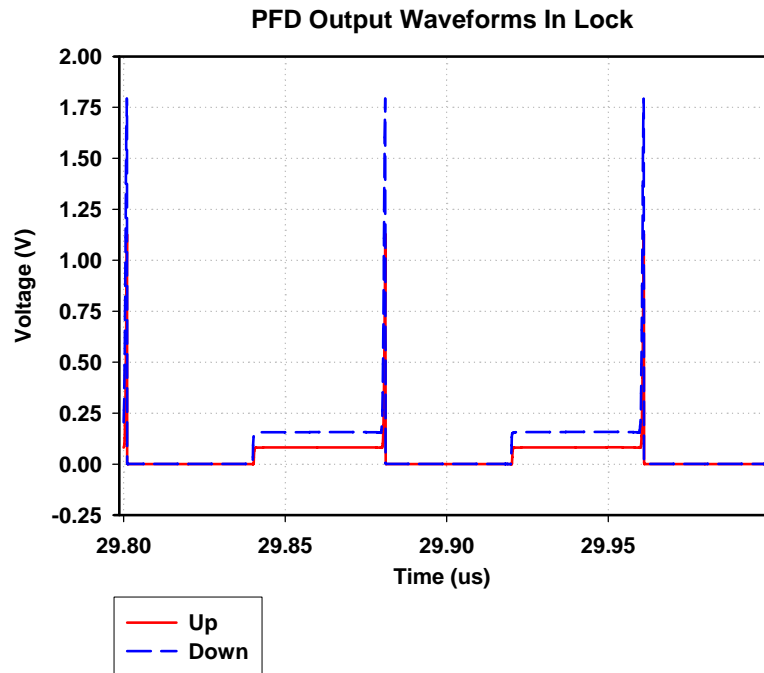
**Figure 9: Verification of Charge Pump Current**

In Figure 9, it is shown that the charge pump has been designed to produce a 40 uA current in either the positive or negative direction. This is the primary specification for the charge pump block as it directly affects the entire PLL loop gain. Even though the VCO, during the simulation, is already at a higher frequency, the initial falling edge of the VCO frequency was placed later than the initial falling edge of the reference frequency. In other words, the initial phase of the system is such that the VCO frequency is lagging behind the reference frequency. This initial difference is detected by the PFD and fed through the charge pump which pumps positive current from top supply rail to force the VCO control higher. This causes an increase in VCO frequency in order to make up the initial phase difference. The phase difference is made up relatively quickly by the frequency difference and soon the VCO phase is leading the reference frequency phase. Once the VCO frequency leads in phase the current switches polarity and begins to reduce the VCO control voltage. This explains why the current switches polarity in Figure 9.



**Figure 10: Control Voltage Settling Waveform**

The VCO should lock to the same frequency as the input reference frequency. Since the VCO is ideal, the VCO control voltage is a direct representation of the VCO output frequency. Therefore, if the VCO control voltage is settled and not changing, then VCO output frequency is also stationary and the PLL is locked. In Figure 10, we can see that the VCO control voltage has settled which verifies the operation of the PFD and charge pump circuits together. The free running frequency of the VCO, when the control voltage is set to .9V, is 11 MHz. The VCO gain is 2.5 MHz per volt. In the figure, the voltage settles to .5 volts, this is expected because  $2.5 \text{ MHz/V} \times .4 \text{ V}$  is equal to 1 MHz and this is exactly the required correction to move the VCO frequency from 11 MHz to 10 MHz.



**Figure 11: Phase Detector Output Waveforms while Test PLL is Locked**

Notice in Figure 11, the up and down signals (the output of PFD) are raised at the same time and immediately reset. The small step visible on the graph is a characteristic of True Single Phase Logic operating at very low power. It could be minimized by using larger CMOS devices but that would increase power consumption. The small step is well below the 900mV threshold voltage of the following inverter and therefore has no minimal effect on PFD and charge pump operation.



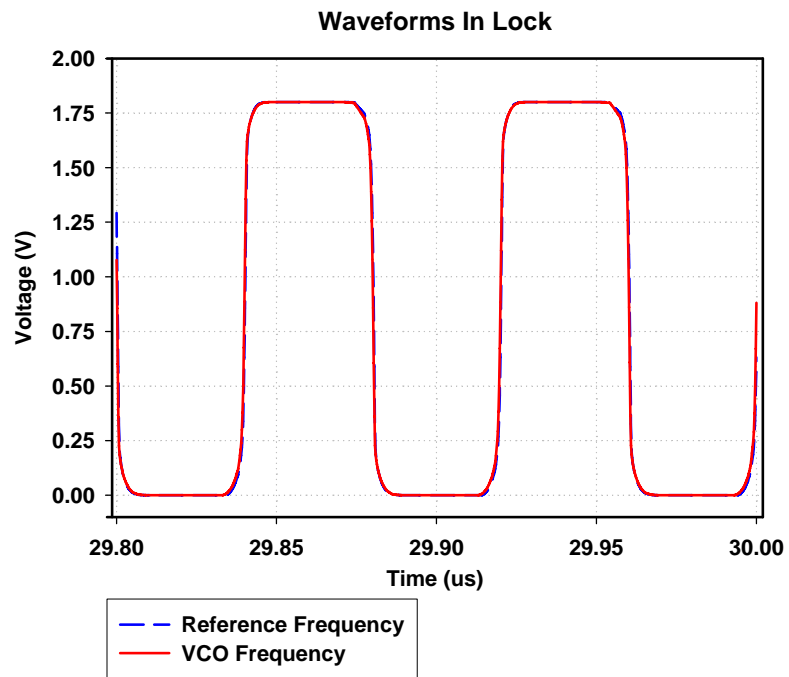
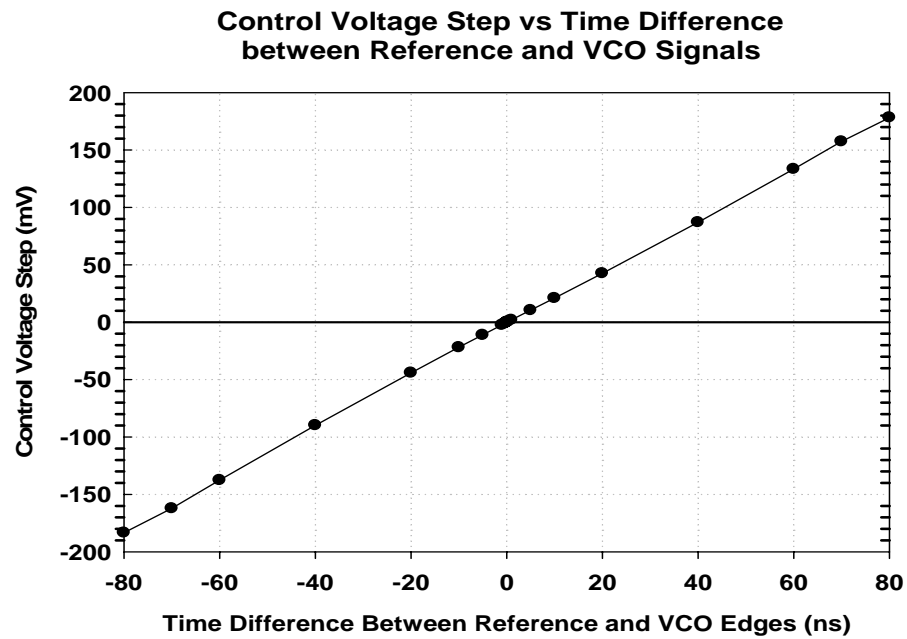


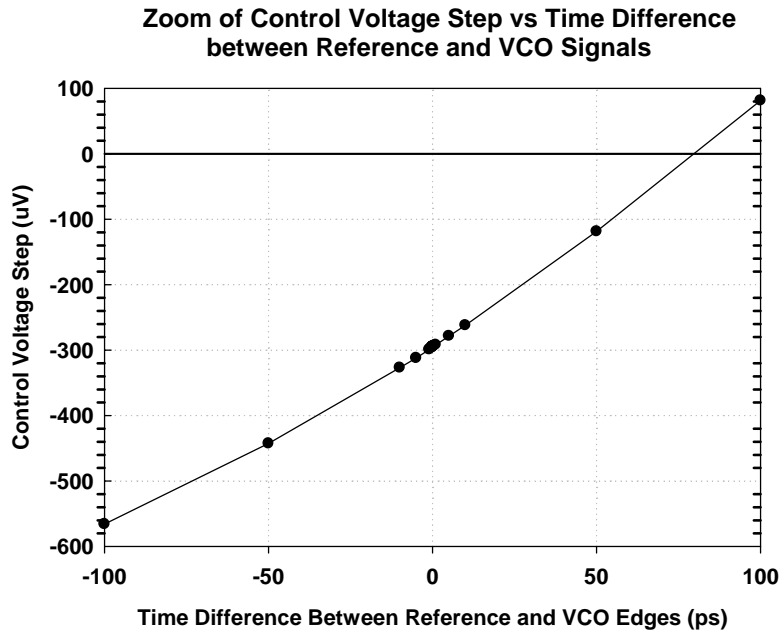
Figure 12: Locked Waveforms

In Figure 12, we can see the locked waveforms at the input and output of the PLL. There is no divider in the feedback loop so there is no static phase offset between the input and output.



**Figure 13: Change in VCO Control Voltage vs Waveform Edge Offset**

Figure 13 shows the amplitude of the step on the VCO control when a certain phase offset is detected. Notice phase is given in nanoseconds.

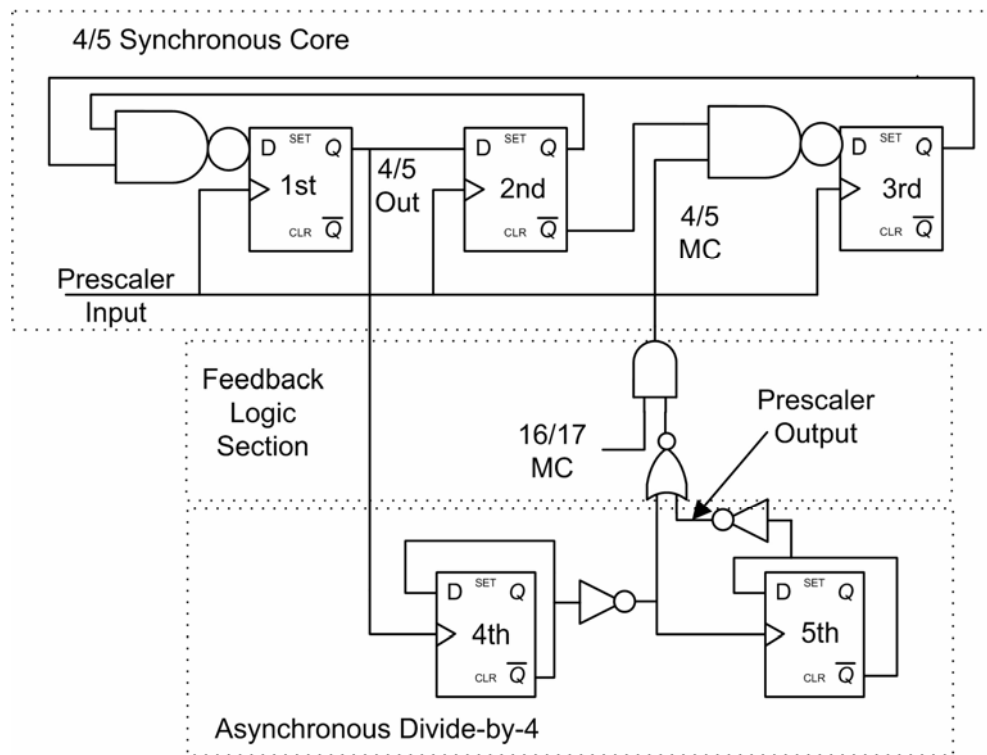


**Figure 14: Zoom of Figure 13**

Figure 14 zooms the VCO control voltage to show the effect of a current mismatch in the charge pump. In this particular plot, when the VCO and reference frequency have zero phase offset there is still a slight negative voltage step. This implies that the NMOS charge down section is slightly overpowered compared to the PMOS charge up section. This effect can be eliminated by adjusting the cascode bias voltages in the charge pump.

## IV DESIGN OF DUAL-MODULUS PRESCALER

### 1. Gate Level Architecture



**Figure 15: 16/17 Gate Level Prescaler Schematic**

A 16/17 prescaler typically consists of a divide-by-4/5 synchronous core, a divide-by-4 asynchronous divider and a feedback logic section (Figure 15)[19]. The 4/5 MC signal controls how many DFFs the prescaler input signal must travel through and therefore determines the division ratio. When the 4/5 MC is held low, the core always divides the input signal by 4 which then travels through asynchronous divide-by-4 circuit, resulting in a total division ratio of 16. If the 4/5 MC signal is high, the core will divide by 5. If feedback is produced such that the core is modulated to divide-by-5 once and by 4 three times the resulting division ratio is 17.



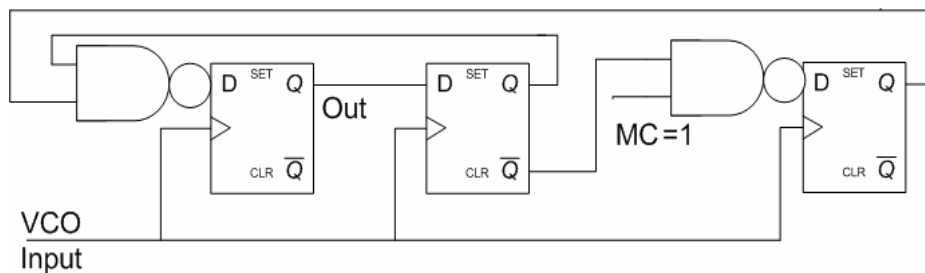
The bit sequence of all the nodes is shown in Table 5. The 4 clock cycle bit sequence will continue indefinitely, if MC is left at zero.

**Table 5: Bit Sequence in Divide by 4 Mode**

MC=0							
Clk Cycle	NAND1	Q1	Q2	Q2_b	NAND2	Q3	Cycle #
1	1	0	0	1	1	0	
2	1	1	0	1	1	1	*1
3	0	1	1	0	1	1	2
4	0	0	1	0	1	1	3
5	1	0	0	1	1	1	4
6	1	1	0	1	1	1	*1
7	0	1	1	0	1	1	2
8	0	0	1	0	1	1	3
9	1	0	0	1	1	1	4

## 2.2 Divide by 5

The 4/5 core is shown separate from the rest of the prescaler in Figure 18. Note here that during divide by 5 operation the output of the D Flip-Flop does change and now only the right NAND gate can be simplified.



**Figure 18: Schematic of Logic Levels in Core for Divide by 5 Mode**

In Figure 19, the simplified schematic is shown and it becomes clear that the 4/5 core resembles a shift register where the last bits are NANDed together and the result is fed into the first bit.

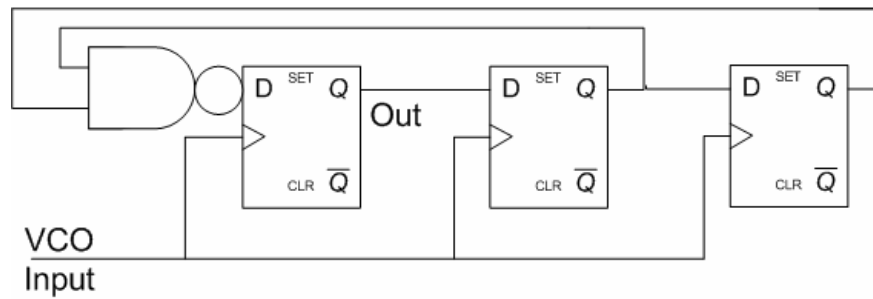
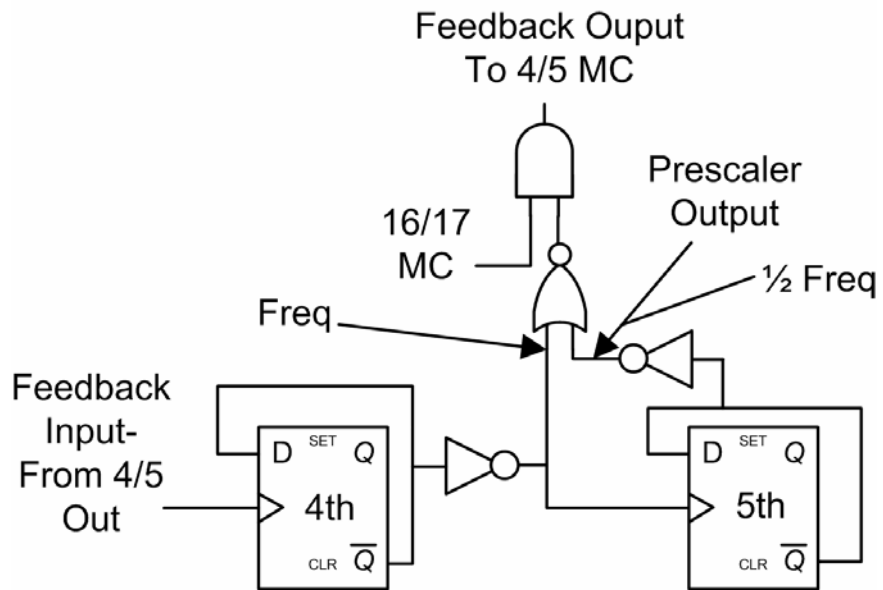


Figure 19: Simplified Schematic of Core for Divide by 5 Mode

In Table 6, the bit sequence of divide by 5 operation is shown.

Table 6: Bit Sequence in Divide by 5 Mode

MC=1							
Clk Cycle	NAND1	Q1	Q2	Q2_b	NAND2	Q3	Cycle #
1	1	0	0	1	0	0	-
2	1	1	0	1	0	0	-
3	1	1	1	0	1	0	-
4	0	1	1	0	1	1	-
5	0	0	1	0	1	1	-
6	1	0	0	1	0	1	*1
7	1	1	0	1	0	0	2
8	1	1	1	0	1	0	3
9	0	1	1	0	1	1	4
10	0	0	1	0	1	1	5
11	1	0	0	1	0	1	*1



**Figure 20: Output and Feedback Section**

A topology that can provide both steady and modulated feedback and also be controlled with a single digital bit is shown in Figure 20.

Freq	█	□	█	□	█	□	█	□
1/2 Freq	█	█	□	█	█	□	█	█
NOR	□	□	█	□	□	█	□	█

**Figure 21: Output of a NOR Gate with Inputs of 2 Frequencies**

Figure 21 shows the result of performing NOR operation for two digital signals when one signal is half the frequency of the other signal. The output of the NOR has the same frequency as the lower frequency section but the duty cycle is now 25% as



opposed to a usual duty cycle of 50%. The next section will present the Current Mode Logic D Flip-Flops at the transistor level.

### 3. Transistor-Level Architecture

#### 3.1 Edge-Triggered D-Flip Flop Implementation

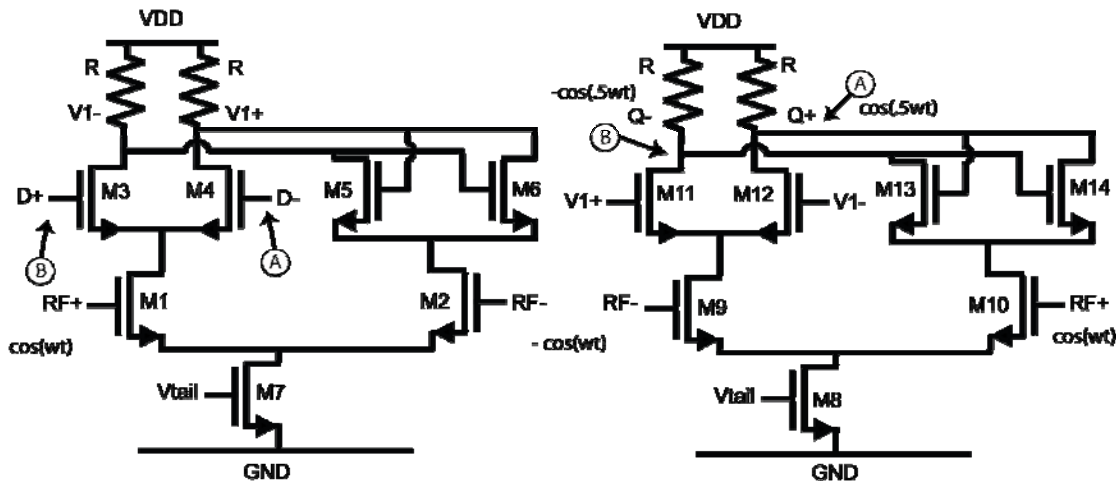


Figure 22: CML Master-Slave D-Flip Flop

Current mode logic is the choice for high speed mixed signal devices [11]. The constant current flow through the transistors biases the circuit a point where the transistors are already active and therefore can react quickly producing low time constants for maximum speed. The current mode logic architecture shown in Figure 22 eliminates slow PMOS transistors and their large parasitics as load elements and replaces them with either resistors with low parasitic or even inductors for maximum speed applications. One advantage of the differential nature of circuit is larger signal swing that results in a higher signal to noise ratio which is important to reduce phase noise in PLL design. Fortunately, extra power hungry common-mode feedback is not

necessary as circuit operates in a digital fashion with complete current switching from one side of the differential pair to the other during any transition.

The master-slave CML DFF is a well-studied topology but some important considerations are worthwhile to mention. The D-input differential pair must provide enough transconductance for complete current switching in one transition. The negative resistance formed by the cross-coupled pair can be small, even a gain slightly less than one is acceptable because input is periodic and voltage levels do not need to be stored for a long run of zeros or ones. Size minimization of this cross-coupled pair is necessary to reduce the capacitance at the output nodes ( $V_{1+/-}$  and  $Q_{+/-}$ ) due to the relatively large gate-source capacitances.

The architecture is similar to a single balanced analog mixer and therefore transconductance of the RF input transistors should be maximized to reduce the effect of noise from the negative resistor, load resistors, and the differential pair. More transconductance in this stage also means more conversion gain ( $G_{conv}$ ) and therefore signal current ( $I_{RF}$ ) passing through M1 transfer to output nodes leading to wider bandwidths. Furthermore, amplitude of signal applied to the D input pair ( $V_{LO}$ ) can be increased by increasing the transconductance of the same D input pair in the previous DFF. A larger  $V_{LO}$  will improve noise immunity and also  $G_{conv}$ . As the transconductance in the bottom half of the circuit increases, the voltage bias point at the output nodes began to fall and less headroom is available for the transistors. To regain headroom, the pull up resistors can be made smaller at the cost of increased current flow and therefore power usage. A trade off arises between power consumption versus frequency response, specifically input bandwidth and maximum operating frequency. Careful selection of this trade-off is critical for optimal efficiency. The relationships are summarized in the following equations.

$$Bandwidth \propto G_{conv} \quad (4)$$

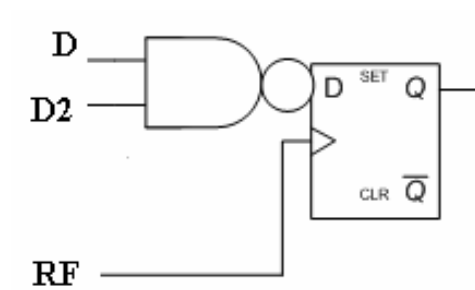
$$G_{conv} \propto I_{RF} \cdot V_{LO} \quad (5)$$

$$V_{LO} \propto g_m D\text{-input diff pair}(M3-M4) \quad (6)$$

$$I_{RF} \propto g_m RF \text{ pair}(M1-M2) \quad (7)$$

$$\text{Power Consumption} \propto I_{RF} \quad (8)$$

$$\text{Output Noise Current} \propto \frac{1}{(V_{LO})^2} \quad (9)$$



**Figure 23: Gate Level D-Flip Flop**

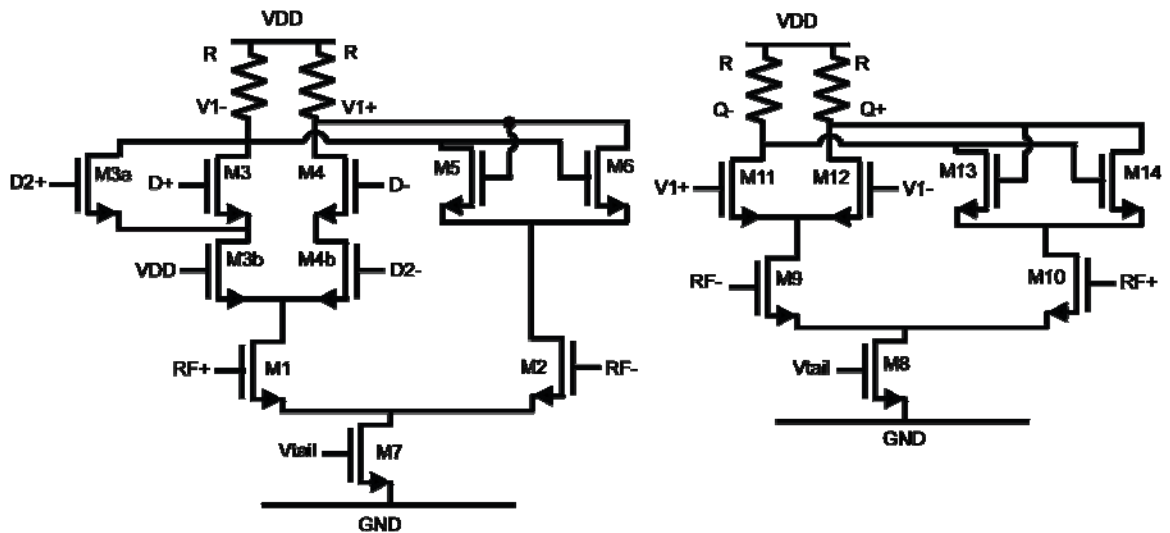


Figure 24: CML D-Flip Flop with Merged CML NAND

Previously, it was shown that the 4/5 Prescaler needs 3 DFFs and 2 NAND gates. Recently reported work [10] has shown that the NAND gates can be merged with the DFFs as shown in Figure 23 to reduce power consumption, decrease delay and reduce complexity. The transistors that add the NAND functionality are M3a and M4b (Figure 24). However, this merged circuit introduces an asymmetry in the architecture. To remedy this asymmetry, we propose adding a degeneration transistor (M3b) in the master latch under the D input differential pair to the architecture (Figure 24). For further clarity, the gate of this degeneration transistor is connected to VDD. By adding this transistor, offsets can be prevented at the output nodes (V1+/-), an undesirable characteristic in the previously reported asymmetrical topology. Since CML logic does not have the wide rail to rail swings like CMOS logic and the signal travels around a loop in almost identical stages much like a ring oscillator, any offset in one stage can easily grow to disrupt the circuit. Close examination of the input section in the master latch shows that in NAND merging process, one side of the differential pair requires stacked transistors (M4, M4b) while the other side parallel transistors (M3, M3a). This causes the top stacked transistor to experience source degeneration and produces a disparity in inversion level and current flow. The final result is a fraction of a bit symbol

sitting on the output nodes ( $V_{1+/-}$ ), which is the input of the slave latch. However, the slave latch is designed for symmetrical inputs because this maximizes transconductance. The addition of source degeneration transistor (M3b) will ensure the input of the slave latch is fully symmetrical and truly differential, maximizing the efficiency of the slave latch. The DFFs in the feedback loop are both realized in the standard master-slave CML previously mentioned.

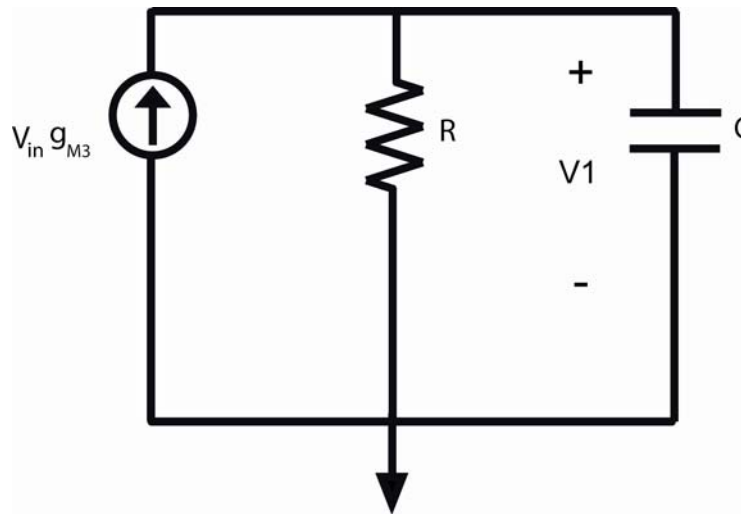
Before proceeding to the design equation section, it is important to note that there are two effects driving the output voltage as the signal propagates through the latch, the preamp step response in the first phase and the positive feedback during the second phase. We must maximize the preamp effect because it is the source of the switching and by doing this we can ensure the next stage already has a strong digital signal for the entire positive feedback phase which creates a predictable input for following circuit that happens to be another preamp. Indeed, the cross coupled pair only adds parasitics during the preamp phase and should be minimized to only flow enough current to delay the collapse of the output voltage by the pull-up resistors, during the second phase.

### 3.1.1 Design Equations for Current Mode Logic D-Flip Flop in Figure 22

#### 3.1.1.1 Latch Design Equations for Either Master or Slave

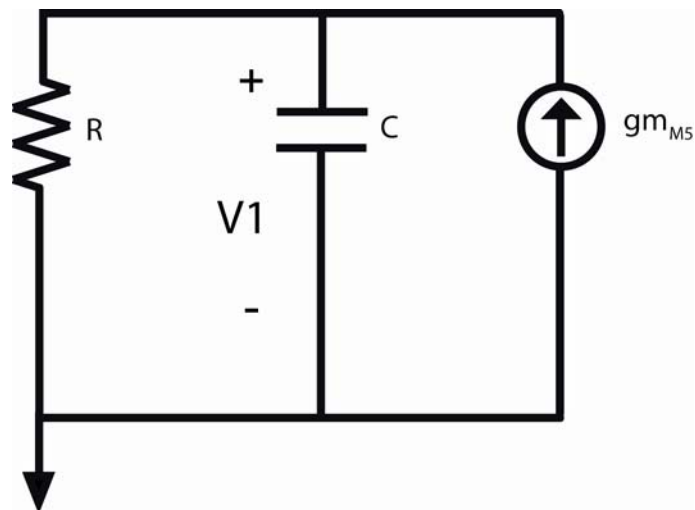
The D-flip flop latch is designed to provide the optimal drain current and transistor size ratio for maximum gain at the operating frequency. A single latch is analyzed in two phases, a preamp phase and a regeneration or latch phase. Both phases will be modeled as first order exponential networks. First order approximations are a necessity because higher order effects can only be well modeled on a computer. In the second phase of the latch, the regeneration phase, the output voltage must be held while the following stage senses the output voltage of the latch. The primary advantage of this analysis is providing the designer with an analytical procedure to calculate device sizes. When deciding among a variety of possible transistor setups, the designer can be sure to select a setup that is most efficient for a given transistor size and power consumption.

First, we will show the linear small signal model of the circuit during each phase.



**Figure 25: Simplified Schematic of Circuit during Preamp Phase**

In Figure 25, the small signal model during the preamp phase is shown. Notice that the transconductance of the latch conductance is not present because the latch should be completely off.



**Figure 26: Simplified Schematic of Circuit during Latch or Holding Phase**

In Figure 26, the schematic of the circuit during the latch phase is shown. Notice here that the transconductance of the preamp is not shown because it should be off during this phase. The next step is to translate the schematics into equations, but first we will define the time in each phase.

$$\text{frequency of RF input signal} = F_{in} \quad (10)$$

$$T_{\text{one phase}} = \frac{1}{2F_{in}} \quad (11)$$

The frequency domain transfer function of the preamp is basically a single-pole amplifier and is given by

$$V_{\text{preamp}} = V_{in} g_m M_3 \left( \frac{R}{RCs + 1} \right) \quad (12)$$

Where R is the load resistance at V1 in Figure 22 and C is the equivalent capacitance to ground at V1 in Figure 22. The C parameter varies significantly with transistor dimensions. The equivalent time domain representation is given by

$$V_{\text{preamp}} = V_{in} g_m M_3 R \left( 1 - e^{-t/RC} \right) \quad (13)$$

Plugging the length of the input preamp phase, we can calculate the expected voltage at the latch output,  $V_{\text{preamp}}$  or V1 in Figure 22, after the preamp cycle finishes. It is assumed that the input voltage is constant.

$$V_{preamp} = V_{in} g_{m_{M3}} R \left( 1 - e^{\left( -\frac{1}{2F_{in} RC} \right)} \right) \quad (14)$$

The latch phase starts after the preamp phase so we will use the output voltage at the end of the preamp phase as the starting point for the regeneration phase. The frequency domain transfer function for the regeneration or holding phase is given by

$$V_{latch} = V_{preamp} \left( \frac{1}{s - \frac{\left( g_{m_{M5}} - \frac{1}{R} \right)}{C}} \right) \quad (15)$$

Where  $C$  is the same as before. Notice how the transconductance of  $M5$  and the conductance of  $R$ , the load resistor, work against each other. This means that depending on the value of each of these two parameters, the pole may be either positive or negative. The equivalent time domain representation is given by

$$V_{latch} = V_{preamp} e^{\left( \frac{t \cdot \left( g_{m_{M5}} - \frac{1}{R} \right)}{C} \right)} \quad (16)$$

Here we see that depending on the two conductances, the output voltage at  $V1$  may either increase or decrease during the latch phase. Plugging in the time period through which the latch operates on the output voltage we have,



$$V_{latch} = V_{preamp} e^{\left( \frac{gm_{M5} \frac{1}{R}}{2F_{in} C} \right)} \quad (17)$$

We can substitute the preamp voltage in into to obtain the final two-phase latch output voltage at V1 in Figure 22.

$$V_1 = V_{in} gm_{M3} R \left( 1 - e^{\left( -\frac{1}{2F_{in} RC} \right)} \right) e^{\left( \frac{gm_{M5} \frac{1}{R}}{2F_{in} C} \right)} \quad (18)$$

Leaving off the DC gain term,  $gm_{M3}R$ , the two exponential terms can be seperated into two terms as follows.

$$Preamp \ Exponential \ Decay \ Term = \left( 1 - e^{\left( -\frac{1}{2F_{in} RC} \right)} \right) \quad (19)$$

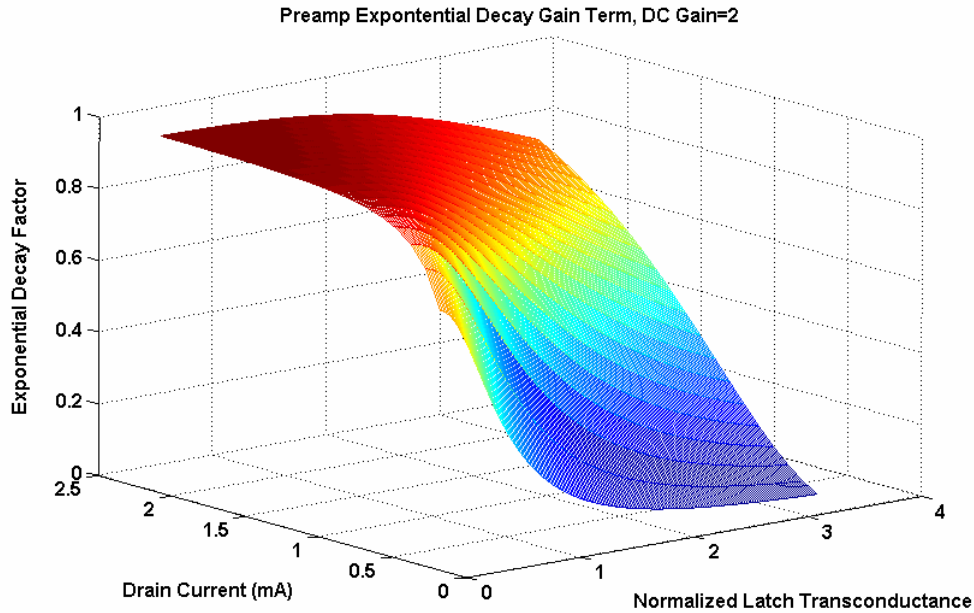
$$Latch \ Exponential \ Growth \ Term = e^{\left( \frac{gm_{M5} \frac{1}{R}}{2F_{in} C} \right)} \quad (20)$$

Optimization of the exponential terms is helpful in determining the effect of each subcircuit on the effective voltage gain for the overall latch. We will use MATLAB to evalutate each exponential term seperately for possible choices of drain currents and transconductances. The headroom of the transistor and DC gain of the preamp is held constant while current level and normalized latch transconductance are varied. The

normalized latch transconductance is a ratio of latch transconductance to resistor conductance. Establishment of device ratios is often more helpful when compared to absolute values because the device ratios provide a rule of thumb for the designer.

$$g_{m_{latch\_normalized}} = \frac{g_{m_{latch}}}{g_{resistor}} = (g_{m_{latch}})R \quad (21)$$

Since we are varying the current, the device sizes must also vary accordingly to maintain DC gain and headroom and therefore the required transistor dimensions are calculated. We then use these dimensions along with process parameters obtained from MOSIS's website at [www.MOSIS.org](http://www.MOSIS.org), for 0.18um TSMC to estimate the capacitive parasitics from transistors. Then from the parasitics, the time constants for each exponential are calculated. The actual time the circuit has in each phase for a 13 GHz input signal is  $1/(2*13e9)$ . This actual time is normalized by the time constant, and the normalized result, which are the number of time constants, are plugged in to their respective exponential terms and plotted. This is a measure of the time domain performance for a particular transistor power and size setup. Note that we will use the term Latch to reference the cross-coupled negative resistor (M5-M6), because it is responsible for the latching or holding effect. The first plot is the preamp exponential decay term and it shows the effect of device sizes in the cross coupled negative resistor. When the sizes are larger, the voltage regeneration is powerful but it is harder for the preamp to drive the voltage to the opposite polarity.



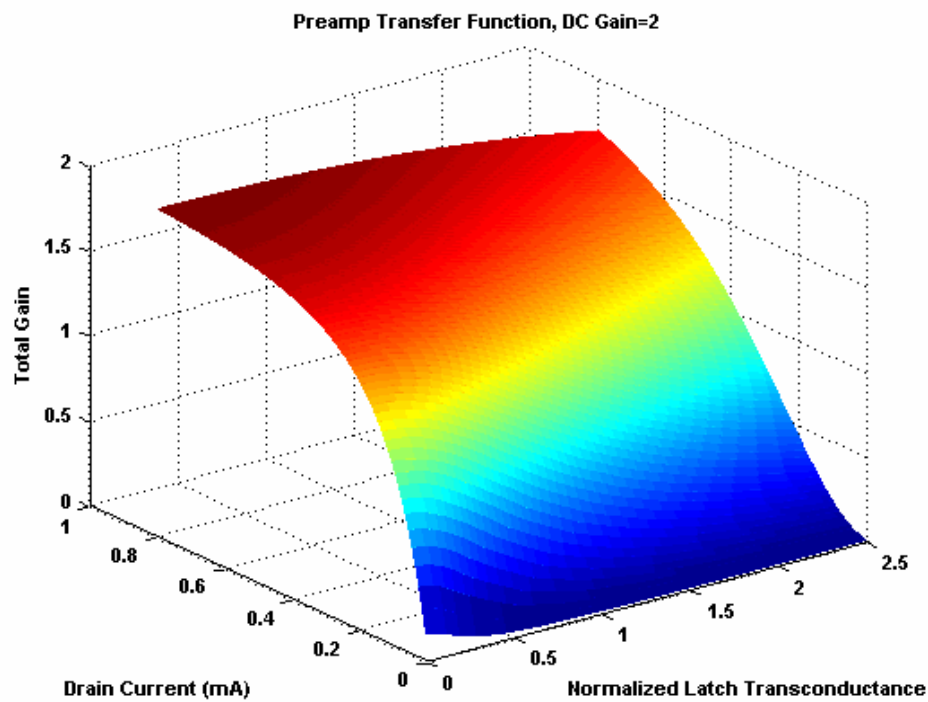
**Figure 27: Preamp Exponential Decay Term**

In Figure 27 the preamp gain clearly decreases as latch transconductance (transistor width) increases. The preamp transfer function is also highly dependent on current because as current increases the load resistance must reduce to maintain the output DC level fixed, which in turn reduces the time constant for the first section. On the drain current axis, the plot shows a sharp increase at about .5 mA and then saturates. An optimal choice would therefore be the region just when the plot saturates as further increase offers little benefit. It is clear that if only 70-80 percent of the signal is transferred, due to exponential decay term during the preamp phase, the preamp DC gain must be increased so that the gain is not less than unity. The following expressions show this relationship.

$$A_{v\ dc\ preamp} = \frac{1}{\text{Exponential Decay Factor}} \quad (22)$$

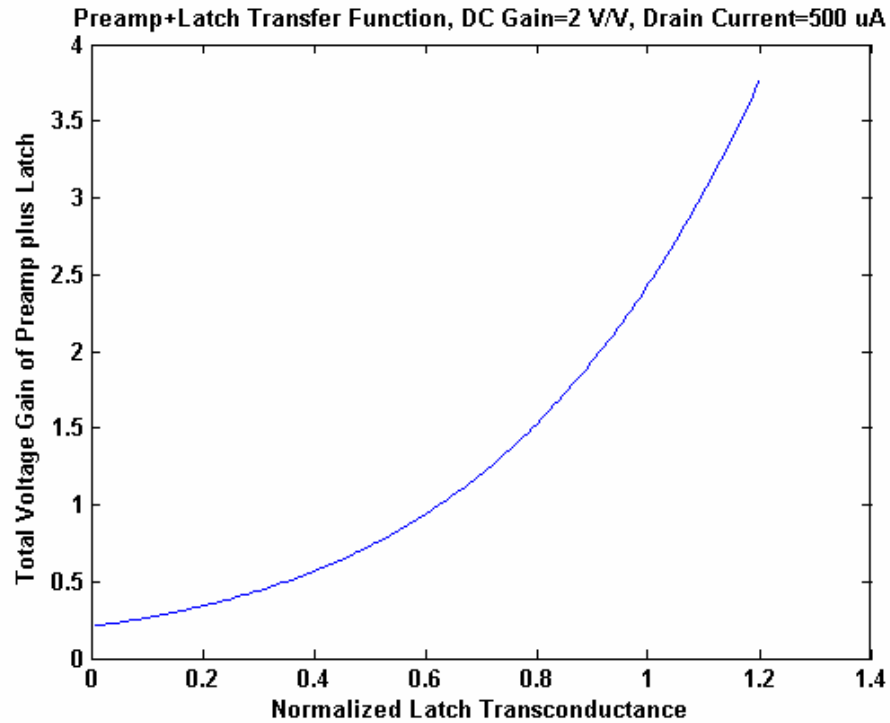
For example if exponential decay term is .5, the required DC preamp gain is

$$A_{v_{dc \text{ preamp}}} = \frac{1}{.5} = 2 \frac{V}{V} = g_{m_{M3}} R \quad (23)$$



**Figure 28: Actual Preamp Gain**

The actual preamp gain, which is the combined effect of DC gain and exponential decay is shown in Figure 28. The gain is slightly reduced from the DC value of 2 V/V because of inadequate settling time.



**Figure 29: Selection of Normalized Latch Transconductance**

In Figure 29, the overall gain of the preamp plus the latch is shown as a function of normalized latch transconductance. Note that the drain current is held at 500 uA, which was previously selected as an efficient choice for the preamp. From the graph, we can see that the output voltage is significantly attenuated when the normalized latch transconductance is small. This means that the pull up load resistors are causing the output voltage to collapse because the holding effect of the latch is too weak. To hold the output voltage of the latch exactly, the normalized latch transconductance should be equal to 1. This is true because if conductances are equal, then any charge flowing out of the node through the resistors is replaced by current flowing into the node through the latching transistors (M5-M6). We can verify on this graph that if the normalized latch transconductance is set to 1, then the overall gain will be approximately 2 V/V and this is exactly the gain of the preamp. This results in a transistor size that can be calculated by the following equation.

$$\frac{W}{L} = \frac{(g_{m_{latch}})^2}{2I_D u_n C_{ox}} = \frac{(g_{m_{latch\_normalized}})^2 R^2}{2I_D u_n C_{ox}} \quad (24)$$

We now have an idea how to ratio out the transistor current and transistor aspect ratio for the latch.

This type of analysis is adequate for schematic simulation and determining approximate device sizes but during layout, the transistor parasitics will greatly increase the time constant of the output node. This translates into similar latch regeneration design requirements because two types of parasitics, capacitive and resistive, tend to cancel the effect of each other on latch performance. Note that holding the voltage is enhanced with a longer time constant because of the increased capacitive effects. However, the resistive gate polysilicon parasitics form a voltage divider and attenuate the actual voltage on the input of the latch which decreases the holding ability of the latch. Therefore, for the latch, the two parasitic effects, capacitive and resistive cancel to some degree. For the preamp, both types of parasitics work against the switching effect of the preamp. This causes the preamp design requirements to become more strict because the output voltage must be driven with more current to sufficiently change the voltage in the time allocated. Therefore during layout, a designer should expect a similar to calculated value for the size of the cross coupled pair (M5-M6) but an increase in the size of the preamp transistors (M3-M4).

This concludes the latch design section. The following section will provide some traditional performance plots used by analog designers during amplifier design. This will serve as a verification of the previous analysis.

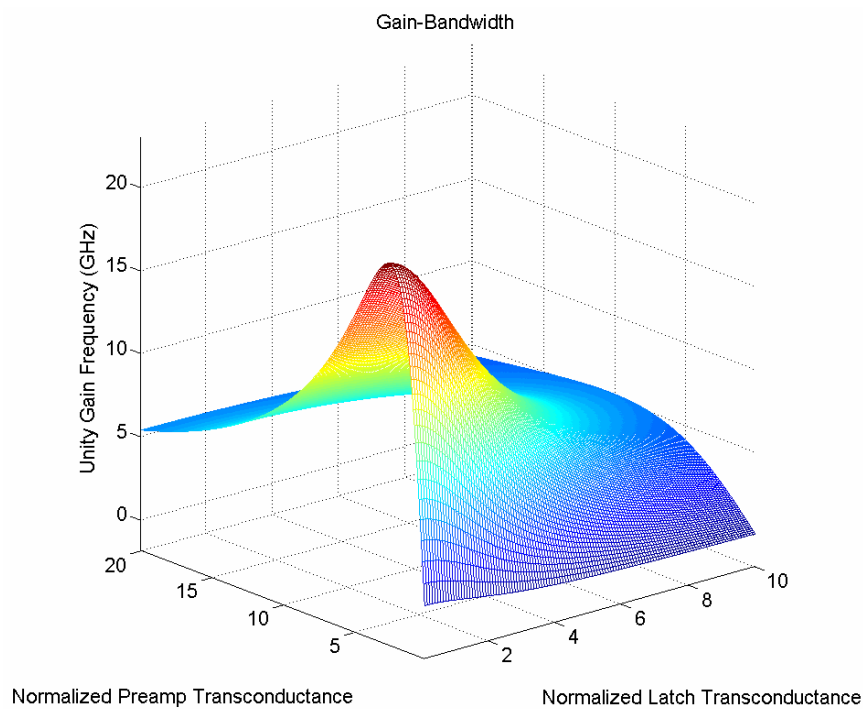
### 3.1.1.2 Preamp Design Equations

#### 3.1.1.2.1 Gain Bandwidth

The gain bandwidth is the most pertinent to preamp performance because the preamp will be mostly operating with low gain at a high frequency and also the gain

bandwidth determines the ultimate settling time. Gain bandwidth product can be calculated by the following expression. Note that C is same as before.

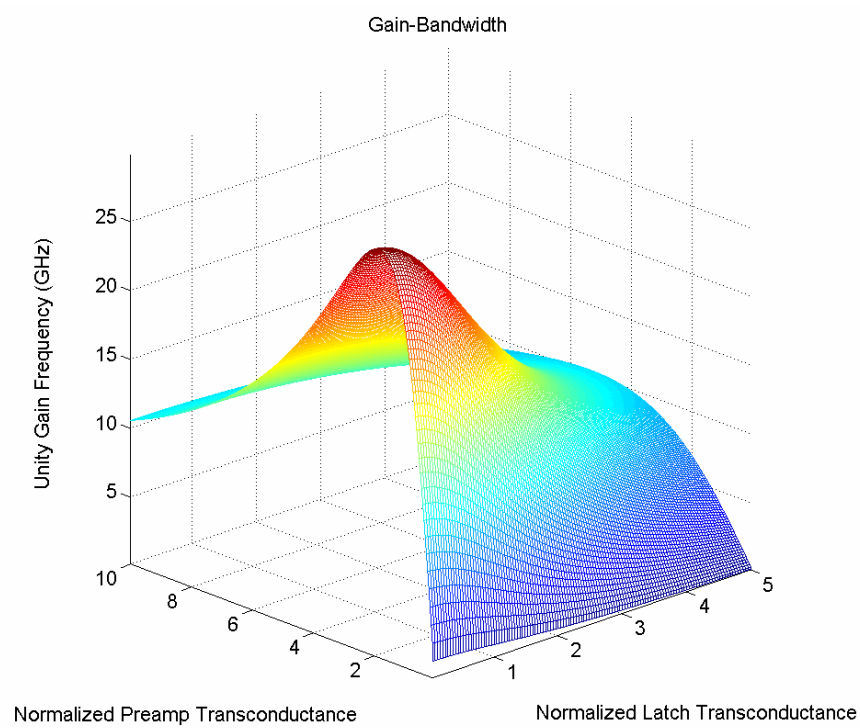
$$\text{Gain Bandwidth} = \frac{g^m M_3}{2\pi C} [\text{Hz}] \quad (25)$$



**Figure 30: Preamp Gain Bandwidth Drain Current=500 uA**

Figure 30 shows the gain bandwidth of the preamp as a function of preamp and latch transconductances. This will give an idea of the optimal ratio between the preamp and the latch transconductance. The optimal parameters for maximum gain bandwidth are a normalized preamp transconductance of 2 and a normalized latch transconductance as small as allowable. The maximum unity gain frequency occurs around 15 GHz. Note that both the drain currents of the preamp and latch sections are set to 500uA and a

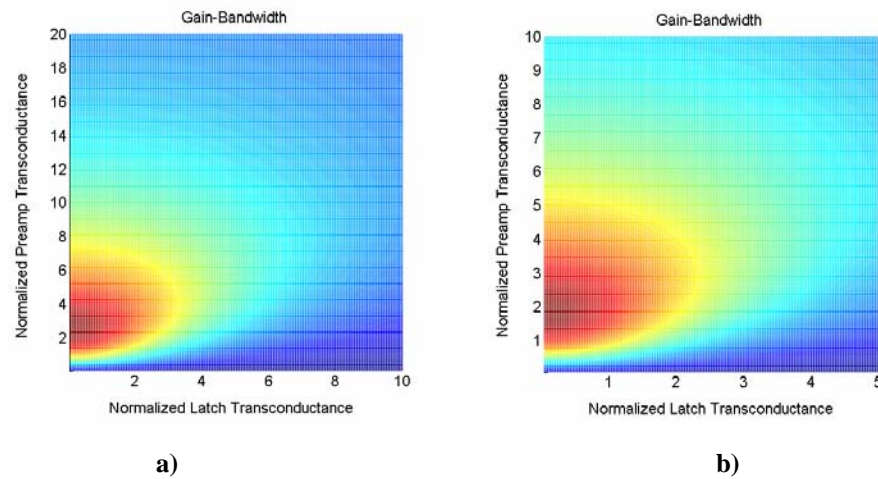
normalized preamp transconductance of 2 implies a DC gain of 2 V/V which agrees with the previous section.



**Figure 31: Gain Bandwidth Drain Current=1 mA**

Figure 31 shows the same plot when the drain current level is doubled. The gain of the preamp increases approximately 8 GHz compared to the first case, however, the expected operating frequency of the latch is only 3.25 GHz. Therefore, a preamp unity gain frequency around 20-25 GHz which is nearly 20 GHz higher seems to be over-design. Although in a layout implementation, this may not be over-design. In any case, we will base the rest of the preamp performance plots on a drain current of 500  $\mu$ A.





**Figure 32: Alternate Top Views of a) Figure 30 and b) Figure 31**

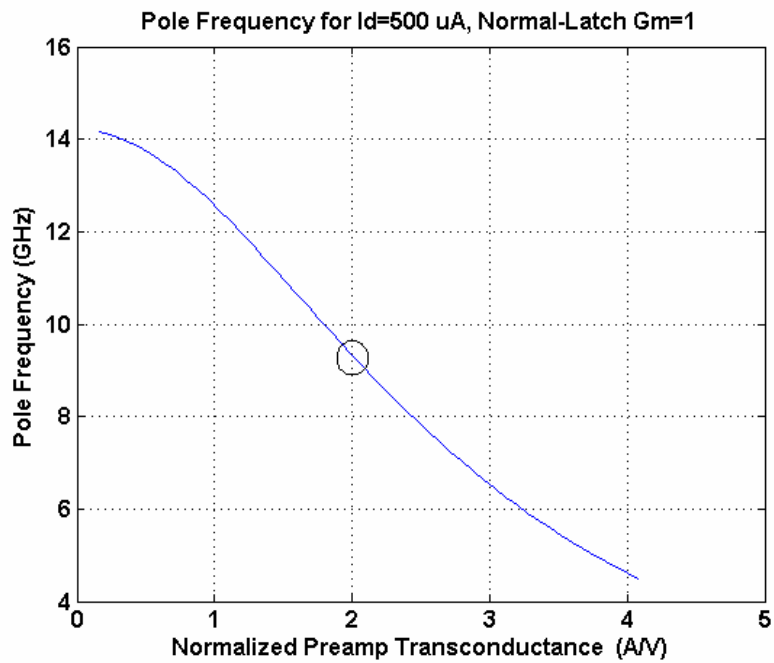
As further confirmation of the previous conclusion, Figure 32 shows top views of the previous 3-D mesh plots which reduces to a colored contour graph. It shows that the best value of the preamp transconductance should be in the vicinity of two times the conductance of a resistor. If the current is doubled to 1 mA, the best value of the preamp transconductance is still about 2 times the conductance of a resistor but the actual bandwidth increases. Therefore, we will keep for design values a drain current of 500  $\mu$ A and set the normalized preamp transconductance to 2. This is because for any current level and for low normalized latch transconductances, this configuration is optimal. Note that if the normalized latch transconductance is less than one then the preamp circuit will maintain high Gain Bandwidth. On the other hand, if the preamp transconductance is less than 2, then the preamp circuit is under-powered and not optimal. One other thing to notice is that if normalized latch transconductance is equal to 1 or less then the preamp transconductance can be increased up to approximately 4 before gain bandwidth begins to drop significantly.

### 3.1.1.2.2 Pole Frequency

The pole or 3-dB frequency can also be plotted for a given transistor setup.

$$|A_V(\omega)| = \frac{|g_{m \text{ preamp}} R|}{\sqrt{1 + \left(\frac{\omega}{\omega_{3-dB}}\right)^2}} = \frac{|g_{m \text{ preamp}} R|}{\sqrt{1 + (\omega RC)^2}} \quad (26)$$

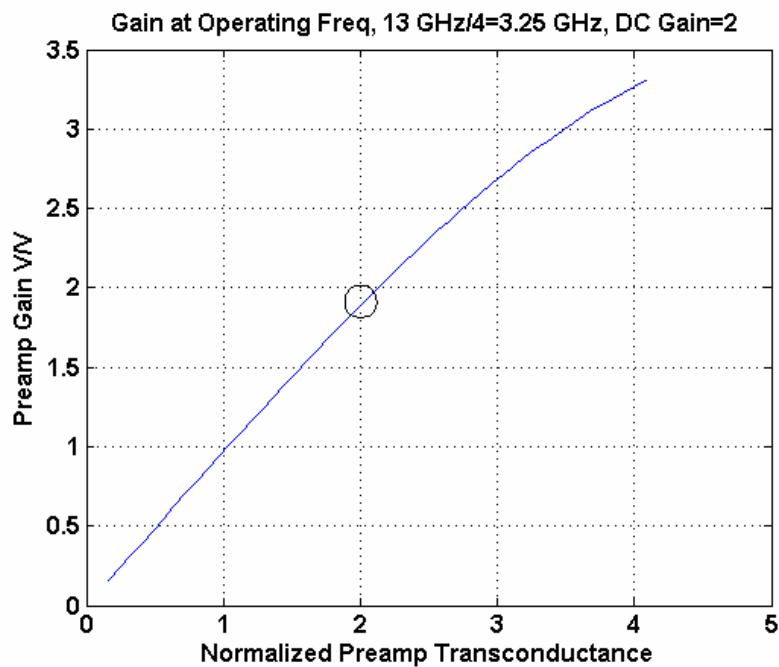
$$f_{3-dB} = \frac{1}{2\pi RC} \text{ [Hz]} \quad (27)$$



**Figure 33: Pole Frequency vs Normalized Preamp Transconductance**

With a drain current of 500  $\mu\text{A}$ , a normalized latch transconductance of 1 and normalized preamp transconductance of 2, the expected pole frequency is approximately 9 GHz as shown in Figure 33 which is well above the 3.5 GHz expected output frequency of the 4/5 synchronous prescaler core. We must now be sure that the gain at this frequency is at least unity plus some margin. The pole frequency is defined in the following equation.

$$A_v(\omega_{3-dB}) = \frac{gmM3^R}{\sqrt{2}} \quad (28)$$



**Figure 34: Gain at Expected Operating Frequency**

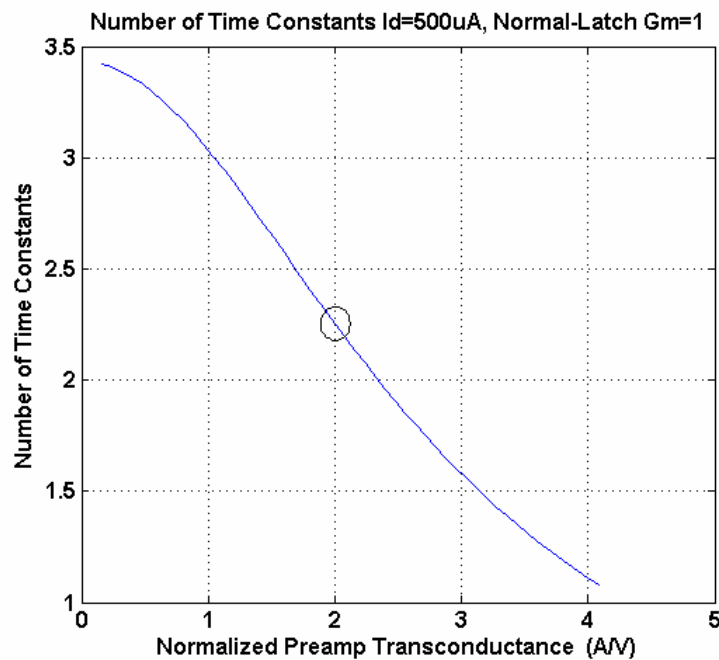
The expected gain at that pole frequency for our setup is approximately 1.8 V/V as shown in Figure 34 which is greater than the required 1 V/V by a factor of 1.8 giving some gain margin.

### 3.1.1.2.3 Preamp Time Constant

The number of time constants over which the preamp will have to settle is a time domain representation of the previous section results. This is true in the sense that these two calculations show the gain variation with frequency compared to DC gain value. The expression is given in the following equation.

$$\text{Number of } \tau = \frac{2\pi}{2F_{in}RC} = \frac{\pi}{F_{in}RC} \quad (29)$$

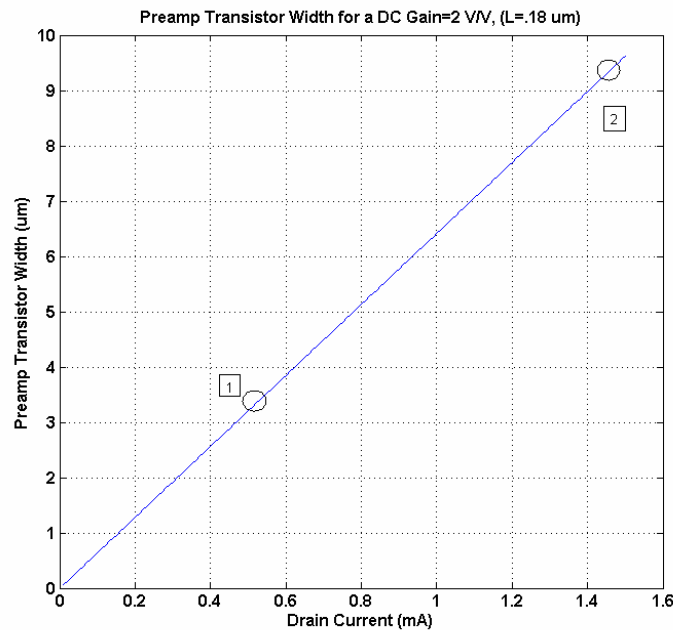
In this expression, the input frequency is a given and the only design parameters are the load resistance and capacitance which are minimized with additional current.



**Figure 35: Number of Time Constants**

The number of time constants over which the preamp will be allowed to settle vs normalized preamp transconductance is shown in Figure 35. As expected, for a given current level, both the preamp and latch transconductances (transistor widths) should be minimized to allow the most number of time constants. For our previous design choices for transconductances, the circuit will have approximately 2.25 time constants to settle which should be sufficient to establish a valid digital symbol.

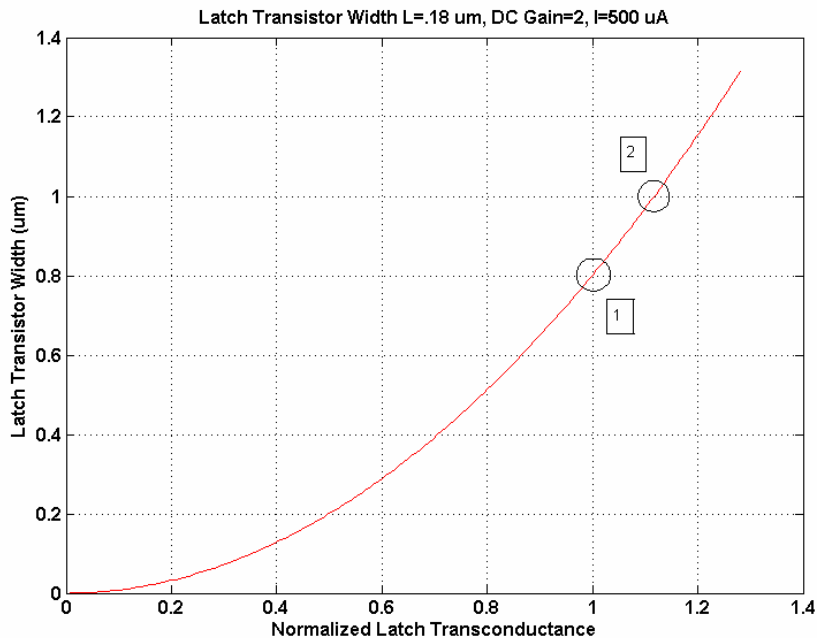
$$(1 - e^{-2.25}) = .89 \quad (30)$$



**Figure 36: Preamp Transistor Sizing (M3-M4)**

In Figure 36, the required size of the transistor can be read right off the graph. Earlier we choose a normalized preamp transconductance of 2 which is equivalent to a DC gain of 2 V/V. We stated that the drain current should be .5 mA. The graph corresponds to a DC gain of 2 V/V and shows we should select a transistor width of just

over  $3.5 \mu\text{m}$  at point 1. The preamp transistor sizing setup for the layout is shown at point 2 to highlight the large effect of layout extracted parasitics on circuits operating at  $3.25 \text{ GHz}$ .



**Figure 37: Latch Width vs Latch Transconductance**

In Figure 37, the width of the latch transistor is chosen. The current is set to  $500 \mu\text{A}$ , the preamp transistors are sized such that the DC gain of the preamp is  $2 \text{ V/V}$ , and the length is minimum size. The design choice of a normalized latch transconductance of 1 can be realized if the latch transistors are  $.8 \mu\text{m}$  wide as shown at point 1. The setup for layout is shown at point 2, which is a much smaller shift compared to the preamp. This disparity in layout size shift is expected as discussed previously in the conclusion of the latch design section.

**Table 7: Typical Values from Design Equations**

	<b>4/5 Core</b>
<b>Input Freq</b>	<b>13 GHz</b>
<b>Output Freq</b>	<b>3.25 GHz</b>
<b>M3, M4</b>	<b>3.5 u</b>
<b>M5, M6</b>	<b>.8 u</b>
<b>Id</b>	<b>500 A</b>
<b>R</b>	<b>800 Ohms</b>

In Table 7, the calculated values of the most critical device sizes are shown. M1, M2 and M7 were not included because their drain node is attached to low impedance nodes. This means the time constants at those nodes is already very low and will not be the limiting factor in performance. This group of transistor should be sized large enough to flow enough current, about 500 uA to M3-M4 or M5-M6. This can easily be found in simulation. In this way, they are the power limiters of the circuit. If they are sized too small, operating bandwidth can suffer significantly. If sized too large, power consumption will be very high and the circuit will have greater than required bandwidth. The lower frequency D-flip flips are not arranged in ring oscillator fashion like the 4/5 core. Therefore, the load impedance of the the lower frequency dividers is very different which means the a new small signal model would have to be derived for the new circuit architecture and this task will be left to the reader.

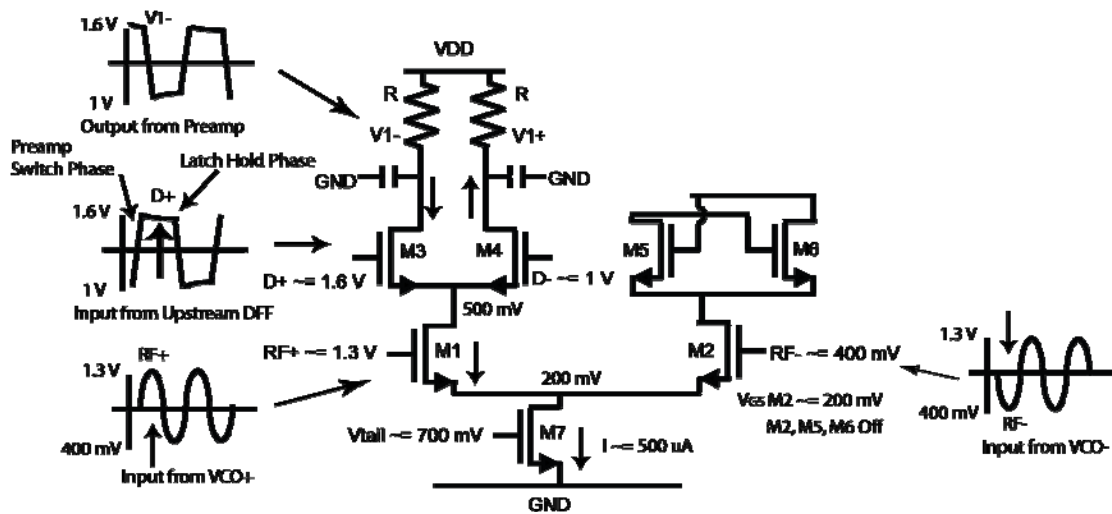


Figure 38: Preamp Phase of 4/5 Core

In Figure 38, typical voltages and currents during the preamp phase are shown. Note that ideally, the sine wave input is converted into a square wave at lower frequency.

In Table 8, the actual transistor widths used in the final layout are given. All lengths are set to minimum which is .18  $\mu\text{m}$ .

Table 8: Typical Layout Values for D Flip Flops

	4/5 Core	1st Async	2nd Async
Input Freq	13 GHz	3.25 GHz	1.625 GHz
Output Freq	3.25 GHz	1.625 GHz	812.5 MHz
M1, M2	15 u	.9 u	1.2 u
M3, M4	10 u	3 u	3 u
M5, M6	1.08 u	1.9 u	4 u
M7	50 u	40 u	40 u
Id	1.4 mA	280 uA	85 uA
R	850 Ohms	3 kOhms	3.7 kOhms



The values are for layout and therefore take into account a large number of parasitics. If these values were placed directly into Cadence simulator, the operating frequency band would be significantly shifted to higher frequencies. Notice from the table that the lower the frequency of operation, the larger the load resistor can be. A larger load resistor can provide sufficient voltage swing for the following circuit with less current. This explains the large power consumption disparity between the core dividers and the feedback dividers. The size of the M1,M2 differential pair determines the operating bandwidth of the divider because they act as the current source for the M3,M4 differential pair. If the M3,M4 differential pair can completely switch the current during one phase, then an increase in M3,M4 width will not provide any benefit but instead add parasitic capacitance. However increasing the width of M1, M2 will increase the available drain current for switching, which effectively reduces the output resistance of M3,M4 lowering the time constant at the output. Additionally, the increase of M1,M2 width will increase the parasitic capacitance and the drains of M1,M2 but this effect is not important that node is already a low impedance node. This fact rises this question of why not make M1,M2 very wide for maximum bandwidth? The answer is a very wide M1, M2 will significantly load the preceding circuit which happens to be a VCO trying to achieve a very high operating frequency. Furthermore, due to the limited tuning range of the VCO, the VCO probably cannot produce frequencies in most of that maximum bandwidth.

This concludes the design section of the CML D. All optimal transistor sizes have been determined as a function of drain current.

### 3.2 Feedback Logic Implementation

The implementation of the feedback logic will be discussed in the following pages. Most high frequency prescaler use current mode logic for the entire device [28]. This implementation will use transmission gate logic (TGL) to reduce the static power dissipation. We will first discuss the TGL NOR gate which is the heart of the feedback logic. Then we will proceed to add other parts of the logic until the entire logic section is discussed.



The basic operation of a generic differential TGL OR Gate (Figure 40) can be understood through a few key elements. Depending on the level of differential (In+/-) input the output (Out+/-) will be connected to either (In2+/-) or the power rails for a one. If (In+/-) is a one then the right TGs are open while the left TGs are closed and the output becomes a one. If (In+/-) is a zero, then the right TGs are closed while the left are open and the output follows the (In2+/-) input. The advantage of such a topology is the lack of static power dissipation as opposed to a CML NOR gate which would require differential pairs and tail currents. Since the operating frequency is 755 MHz in this section, the high speed of CML is not required. The circuit can also be configured as a NOR gate as shown in the gate level schematic by taking the differential outputs with opposite polarity.

The following pages will walk the reader through the step by step modifications made to the transmission gate logic NOR gate.

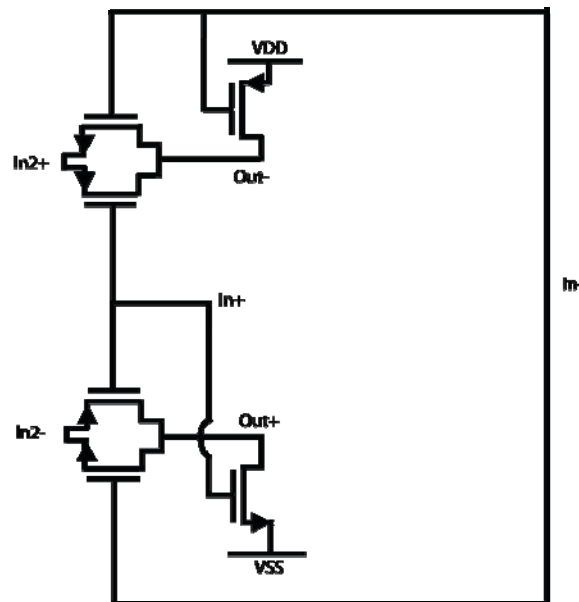
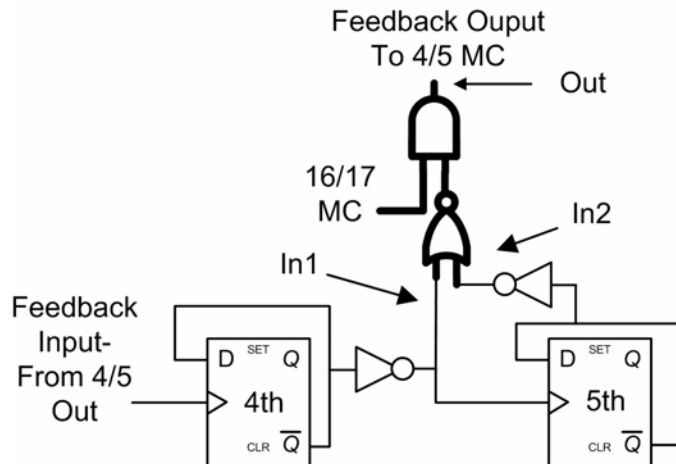


Figure 41: NOR Gate Modification 1

The first modification, shown in Figure 41, was noticing that the right hand transmission gates were connected to a supply rail. This means they are operating in a pull-up or pull-down mode as opposed to left hand transmission gates which are passing a bi-directional signal. Therefore, depending on which supply rail the source is connected to, one transistor can be eliminated from each transmission gate. The PMOS transistor, with source connected to the ground, and the NMOS transistor, with source connected to VDD, will never turn on and are unnecessary. Now, we will add the AND gate into our circuit, it is shown in Figure 42.



**Figure 42: Gate Level Representation of Figure 43**

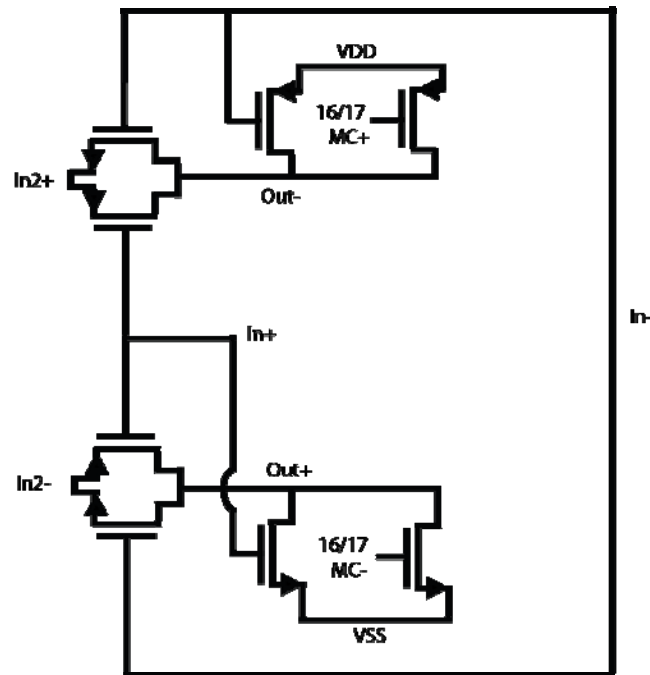


Figure 43: NOR Gate Modification 2

After the first modification, we have a TGL NOR gate with no extra inactive transistors. If this NOR gate is placed into the prescaler directly, it would lead to a divide by 17 only divider with no way to change to divide by 16. There must a way to disconnect the NOR gate from the 4/5 core or at least force the output nodes of the NOR gate to the desired value in Figure 43. This is accomplished by adding two more transistors which are sized large enough to hold the NOR output voltage to a certain polarity. In Figure 43, the transistors with their gates attached to 16/17 MC +/- provide this functionality. Note that Figure 42 is a gate level representation of Figure 43. Forcing the 16/17 MC +/- signal to zero allows disconnection of modulated feedback and provides a constant zero feedback resulting in a division ratio of 16. Therefore, the 16/17 MC +/- signal controls the overall division ratio of the prescaler. The next section is about the inverters highlighted in Figure 44 and shown at transistor level in Figure 45.

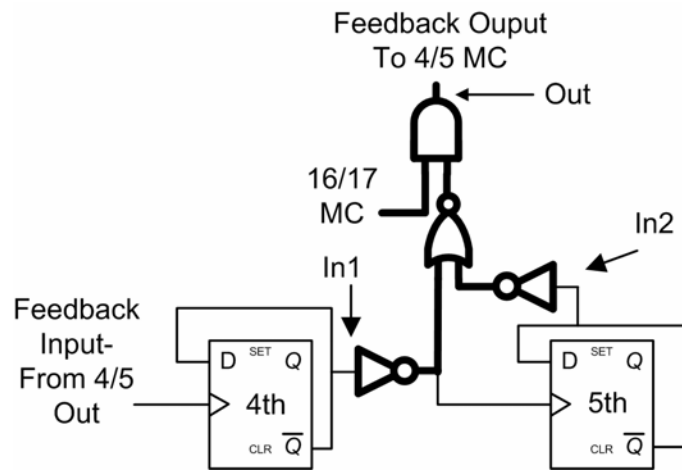


Figure 44: Gate Level Representation of Figure 45

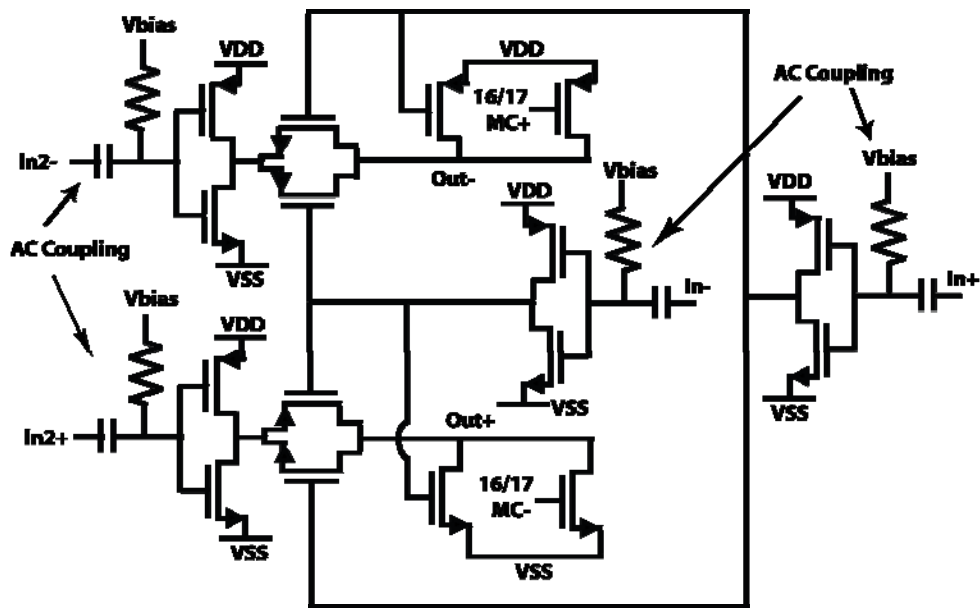


Figure 45: NOR Gate Modification 3

These inverters serve as the overall prescaler output buffer, level shifter and amplifier from CML to TGL. They also decouple the output impedance of the CML divider from the input impedance of the TGL\_CMOS. To convert from low voltage swing CML to large voltage swing TGL, it is necessary to re-center the DFF output signal at  $V_{DD}/2$ . CML requires transistors with highly inverted channels which leads to large overdrive voltages. This means that the DFF output signal is usually centered well above  $V_{DD}/2$ , typically at 1.4 V. The ac coupling ensures the input of the CMOS inverters will be centered at  $V_{DD}/2$  or 900 mV. These CMOS inverters use very little static power, have the largest signal gain of any amplifier and create a better rail to rail signal for the TGL NOR gate output (Out-/+). The output of TGL (Out -/+) is applied directly to the high impedance input of the 4/5 core with no buffering. Transistor size in this section is as small as possible to minimize parasitics and chip area. However, the on-resistance of the transmission gate is proportional to the width of the transistors and this places a restriction on their minimum sizes. Decoupling of the impedances is a critical feature because the operation of the divider is highly dependent on the load impedance of the divider. The load impedance is the input impedance of a transmission gate which intentionally varies greatly depending on whether it is on or off.

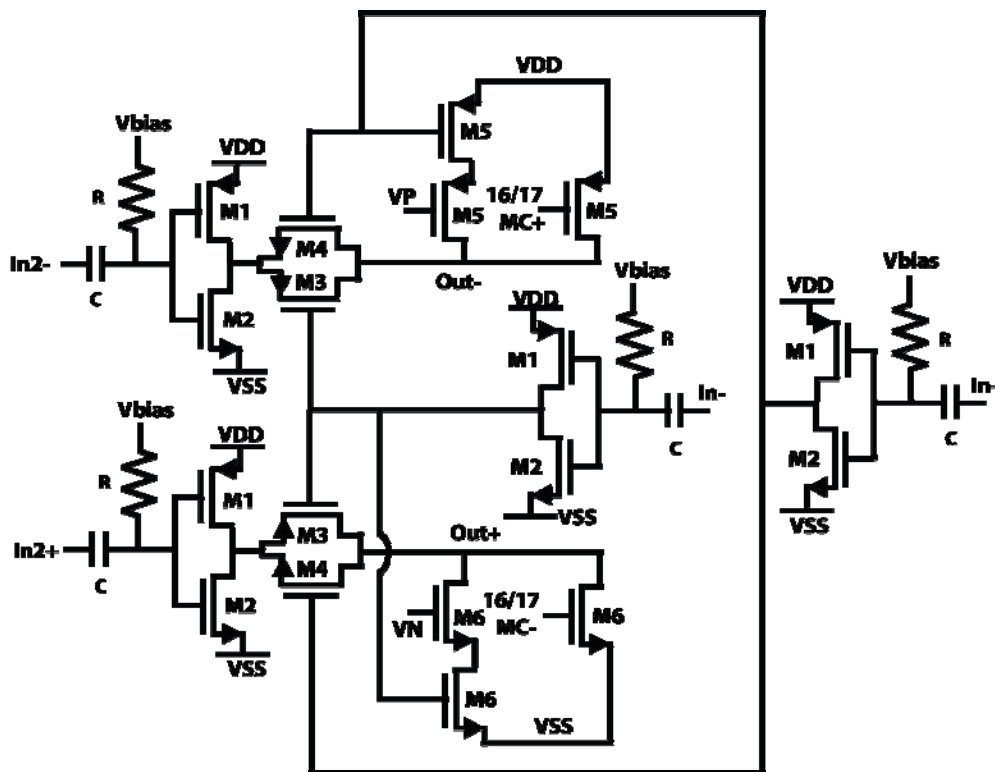


Figure 46: Implemented TGL OR Gate with Inverter Buffers

The final modification is included solely as a precaution to ensure NOR operation in the event that the fabrication process results in corner silicon. The cascode transistors M5, M6 are included to allow control over the driving strength of the pull up and pull down transistors, added in Figure 46. If the process is slow and the output voltage (Out-/+ ) cannot be effectively pulled up and/or pulled down, then the 4/5 core will not ever shift into divide by 5 mode resulting in divide by 16 mode only. However, if the process is fast and the output voltage is overdriven, then the 4/5 core will take too long to recover and return from divide by 5 mode. The net result is that instead of divide by 17 mode, the circuit will divide by 18. The adjustment can be performed by adjusting VN and VP. For instance, if the process is very slow VN will be set to VDD and VP will be set to VSS. If the process is fast then the VN can be decreased while VP is increased until the desired division ratio of 17 is achieved.



### 3.2.1 Design Equations for Feedback Logic Section

The inverters and transmission gates can be modelled by an inverter with a second order RC low pass filter as shown in Figure 47.

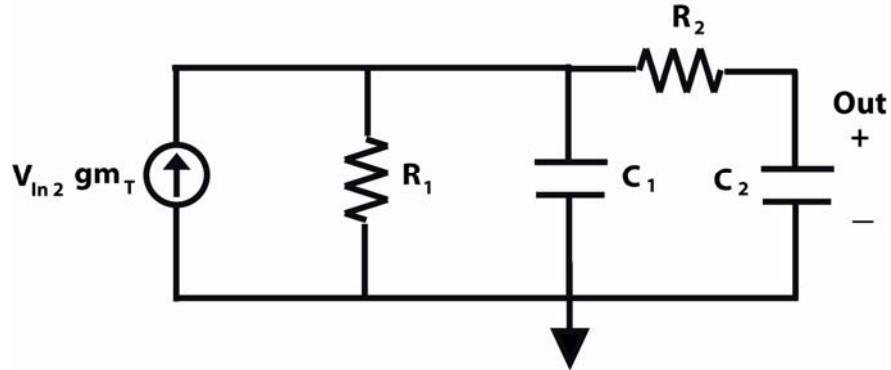


Figure 47: Small Signal Model of TGL NOR Gate

The input transconductance,  $gm_T$ , is the total transconductance of the NMOS and PMOS transistors, M1-M2, in the inverters. Note that this analysis neglects the  $C_{gs}$  and  $C_{gd}$  of the transmission gates for simplicity as the addition of two more capacitors to the model would result in a fourth order system.

$$\frac{V_O}{V_i} = (gm_{NMOS} + gm_{PMOS}) \left( \frac{\frac{s}{R_1 C_1} + \frac{1}{R_1 C_1 R_2 C_2}}{s^2 \frac{1}{R_1 R_2} + s \left( \frac{1}{C_1 R_2} + \frac{1}{C_2 R_2} + \frac{1}{C_1 R_1} \right) + \frac{1}{R_1 C_1 R_2 C_2}} \right) \quad (31)$$

Where  $R_1$  is the total output resistance of the inverter on the In2- input and given by the following expression.

$$R_1 = \frac{(R_{out\_NMOS} \parallel R_{out\_PMOS})}{R_{out\_NMOS} + R_{out\_PMOS}} \quad (32)$$

$R_2$  is the on resistance of the transmission gate, which is the parallel combination of M3 and M4 channel resistances. The on-resistance of M3 is given by the following expression.

$$R_2 = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{M3} (V_{gs} - V_{th})} \quad (33)$$

$C_1$ , which is the grounded capacitance at the output of the inverters composed of both the parasitic capacitors,  $C_{db}$  and  $C_{sb}$  and given by the following expression.

$$C_1 = C_{dbn\_M2} + C_{dbp\_M1} + C_{sbn\_M3} + C_{sbp\_M4} \quad (34)$$

Finally,  $C_2$  is the grounded capacitance at the output node, Out-, and is composed of both  $C_{db}$  of the transmission gates, both  $C_{db}$  of the PMOS pull up transistors and the  $C_{gs}$  of the input pair of the D Flip-Flop on the 4/5 core. The capacitance is summed at output node, Out-, where PMOS transistors are attached to provide an estimate that is accurate for the node with the largest time constant. If we used the node with NMOS transistors attached, Out+, we would overestimate the frequency response of the circuit.

$$C_2 = C_{gs\_4/5\_Core} + C_{dbn\_M4} + C_{dbp\_M3} + 2C_{dbp\_M5} \quad (35)$$

The preceding analysis was performed to gain an intuitive understanding of the circuit and an exact calculation of device sizes will be left to the reader. The primary conclusion is that the inverter must drive a second order RC filter, while most of the

other sections of the prescaler must drive only first order filters. This means the inverter must be large enough to supply enough current for fast voltage switching. The transmission gates should be sized large enough so that the resistance of the gate is not too large and nor is the parasitic capacitance too large. When both of these parameters are small, the time constant of the gate is small and the operating frequency is increased. Clearly, there is a trade-off between the two parameters, resistance and capacitance, however a balance can be found to provide an optimal value. As transistor width increases, the resistance drops quickly at first and then levels off. At the same time, the transistor width increase causes the parasitic capacitance to increase slowly at first then later begins to increase much more quickly because of the parasitics. Therefore, transistors, with a size that is a few times larger than minimum size, are a good starting point for the design. The size can be fine tuned using the simulator. The pull up or down transistors should be only large enough to ensure they can logically change the voltage when necessary. This is because they contribute parasitics at the output node, especially, the pull-up PMOS transistors. The operating frequency in the feedback section is significantly lower than other prescaler sections such as the 4/5 core and therefore the design values are more relaxed. The Out- node in Figure 46 is the critical node, because the PMOS pull-up transistors (M5) contribute significantly more parasitics than their NMOS counterparts (M6) at Out+.

In Table 9, the actual transistor size used for the feedback section in the layout are shown. The length of all transistors is set to the minimum at .18um.

**Table 9: Element Values for the Feedback Section after Post Layout Simulations**

M1-Inverter PMOS	8 u
M2-Inverter NMOS	2.3 u
M3-TG PMOS	5 u
M4-TG NMOS	2 u
M5-PMOS Pull Up	1 u
M6-NMOS Pull Down	.27 u
C	112 fF
R	9 kOhms

The feedback logic section was simulated in Cadence and all element values have been optimized during post layout simulations. The overall transistor-level schematic of the prescaler is shown in Figure 48.

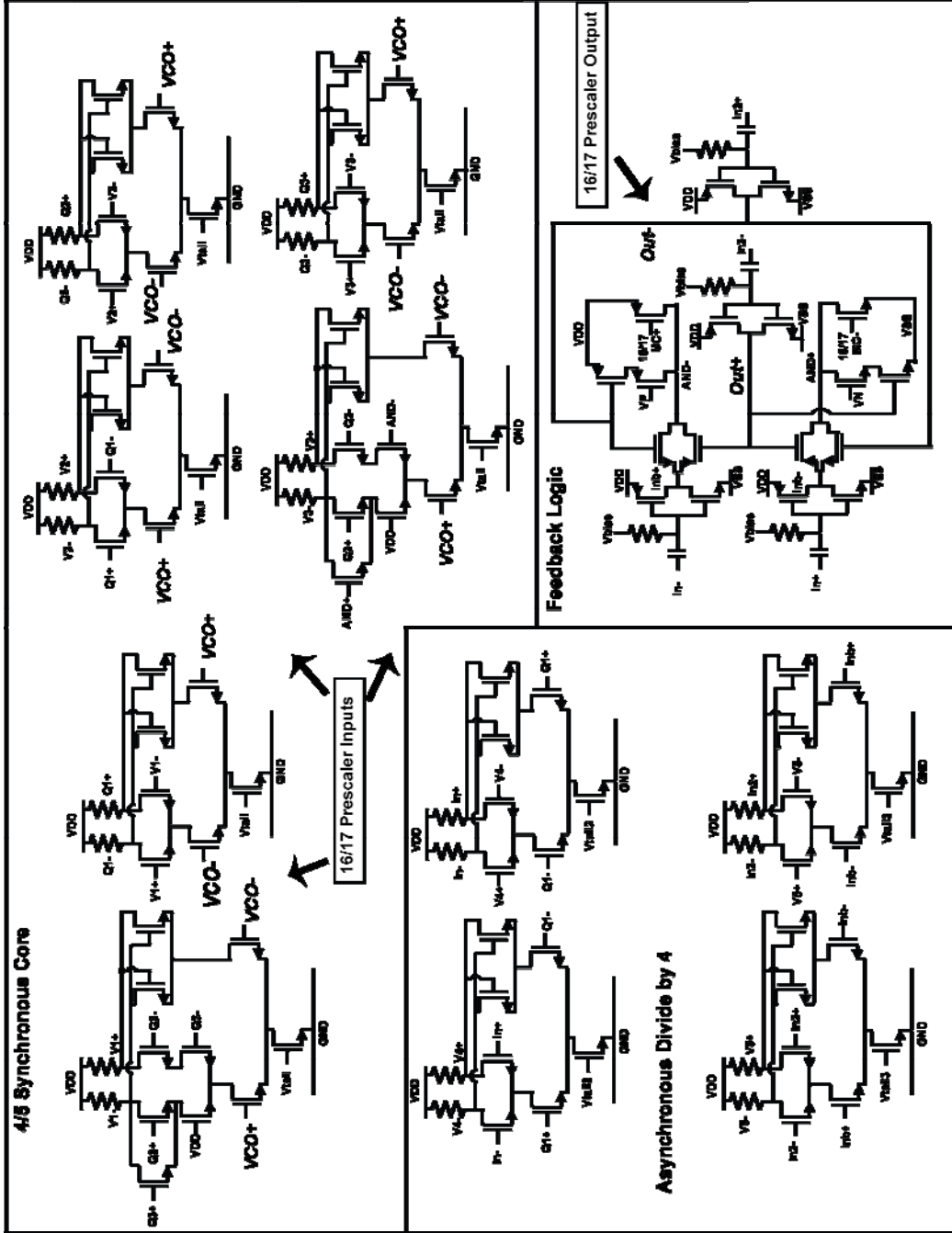


Figure 48: Overall Schematic of 16/17 Prescaler

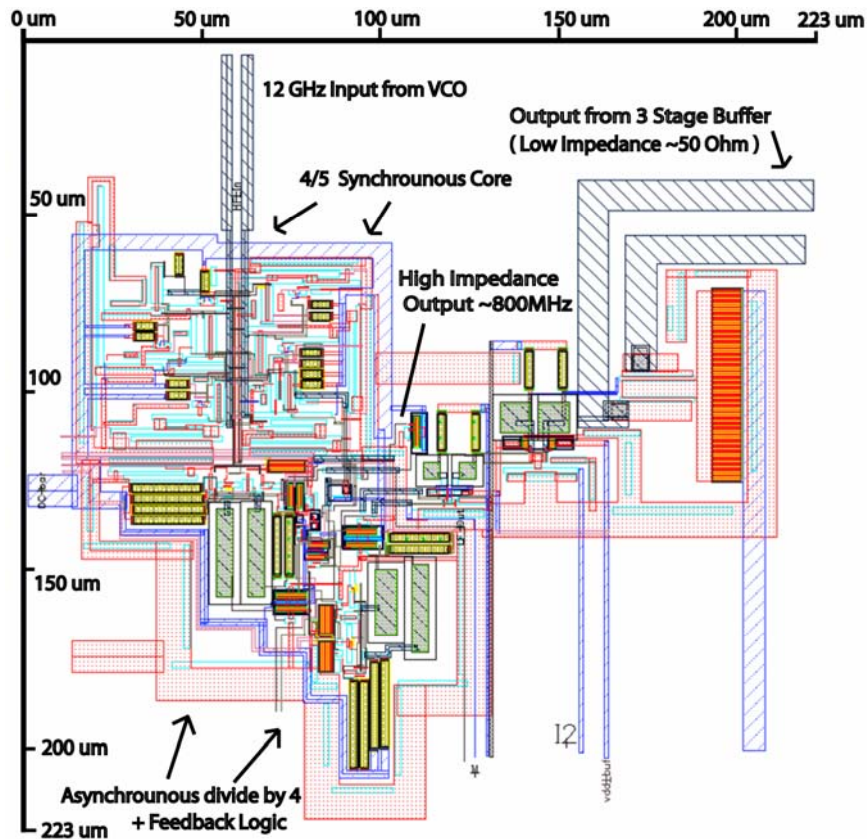


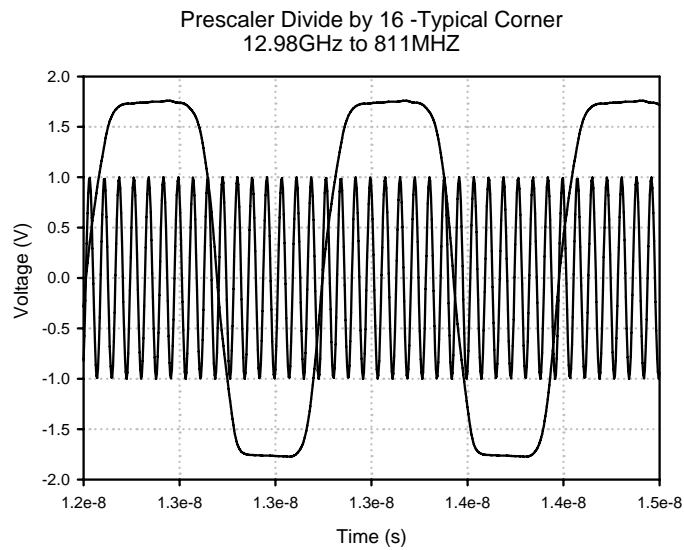
Figure 48: Layout of 16/17 Prescaler

The entire prescaler layout, shown in Figure 48, has been optimized using CADENCE to distribute capacitance evenly throughout the circuit but extra care is necessary for the high frequency core. The 4/5 core DFFs are located in the square section on the right in a circular arrangement. The high frequency prescaler input is located on the right in the middle of the circle of core DFFs. The feedback loop is located in the left section. The feedback loops senses the core output in the center of the layout and returns the feedback to the core at the bottom middle of the layout which is also the location of the prescaler output. The output buffer, shown on the right side, is used only for measurement purposes and would not be present in an actual frequency synthesizer. The prescaler-only layout area is approximately  $160 \mu\text{m}$  by  $125 \mu\text{m}$  ( $.02 \text{ mm}^2$ ).

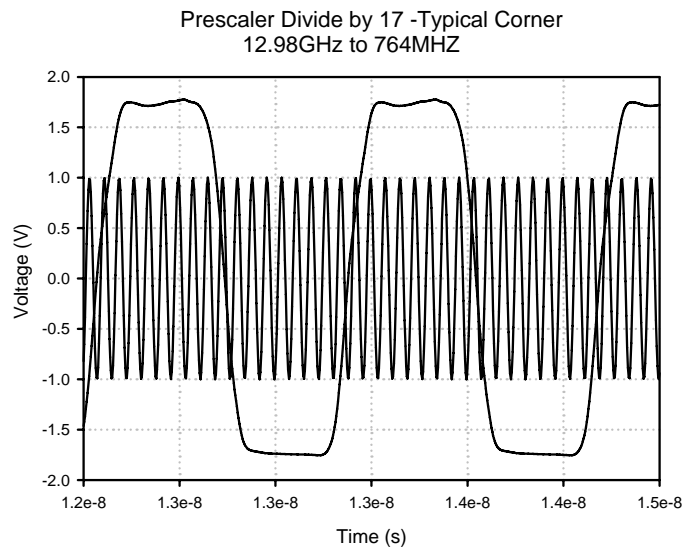
## 4. Prescaler Simulator Results

### 4.1 Post Layout Simulations

The following plots show simulation results obtained from the extracted layout.

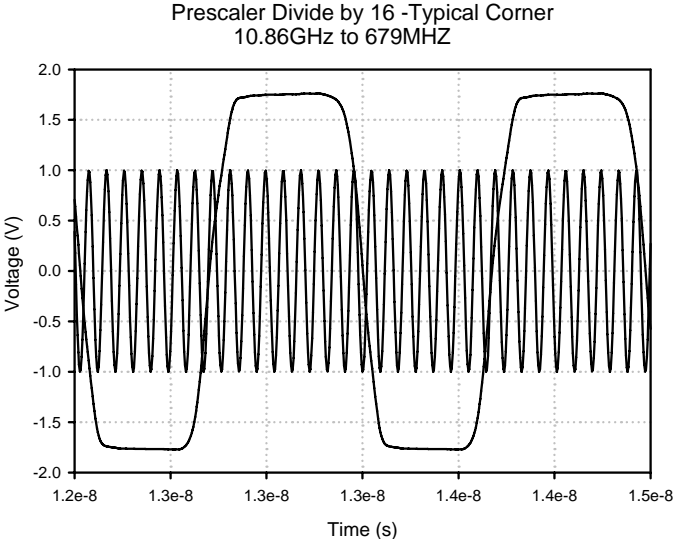


**Figure 49: Divide by 16 Simulated Transient Response-Upper Frequency Limit**



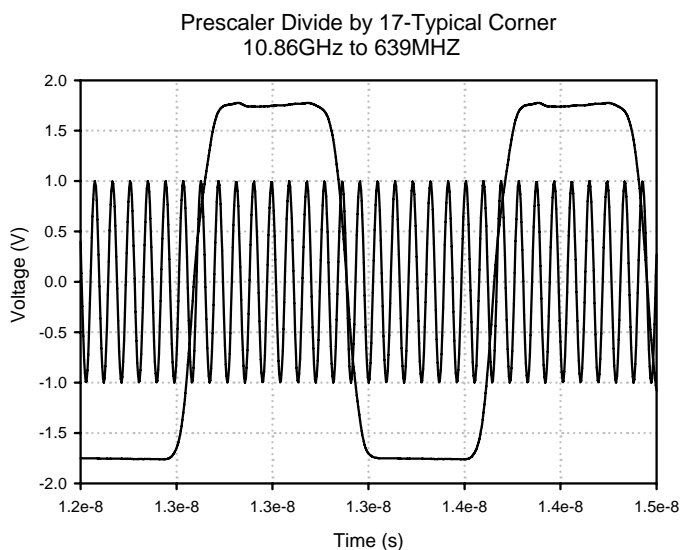
**Figure 50: Divide by 17 Simulated Transient Response-Upper Frequency Limit**

The prescaler input signal transient response is shown together with the divided output waveform for division ratios of 16 and 17 at 12.98 GHz (Figure 49 and Figure 50), which represents the maximum operating frequency for the typical corner. It is notable that the output waveform is not only divided in frequency but also amplified in amplitude.



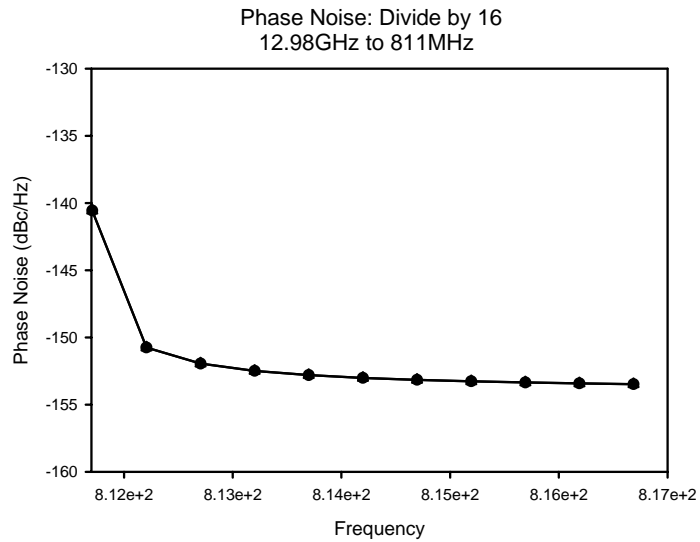
**Figure 51: Divide by 16 Simulated Transient Response-Lower Frequency Limit**



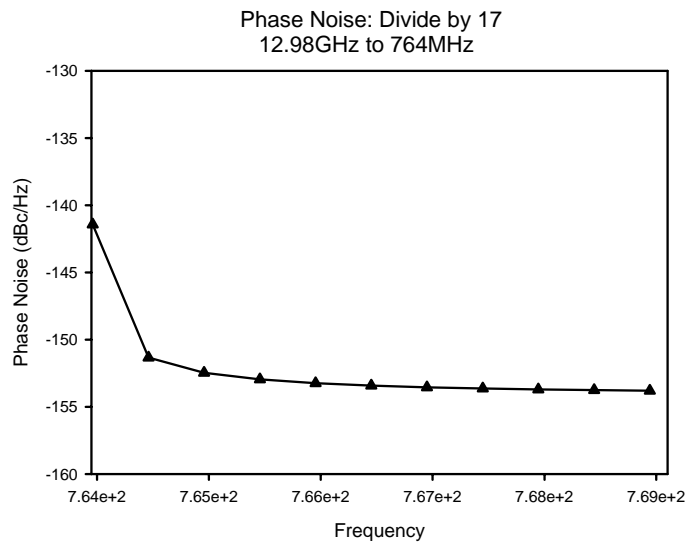


**Figure 52: Divide by 17 Simulated Transient Response-Lower Frequency Limit**

The correct division ratio is maintained for prescaler input signals down to 10.86 GHz as shown in Figure 51 and Figure 52 which is the minimum operating frequency for the typical corner. This results in a prescaler bandwidth of approximately 2 GHz. The following plots show the simulated phase noise of the divided signal at the output of the prescaler after post-layout simulations. Here it is assumed that the input of the prescaler is a noise-free source in circuit simulations. The worst-case phase noise happens at the maximum operating frequency, 12.98 GHz, due to signal attenuation because of parasitics. The 12.98 GHz input signal is divided by 16 to provide the 811.25 MHz signal and is divided by 17 to provide the 763.53 MHz signal at the output of the prescaler. The phase noise @ 1 MHz offset is shown for both division ratios in Figure 53 for divide by 16, -151 dBc/Hz at 812.25 MHz and Figure 54 for divide by 17, -151.5 dBc/Hz at 764.53 MHz. Note that the second circle or triangle from the left in each plot is exactly 1 MHz off the carrier.



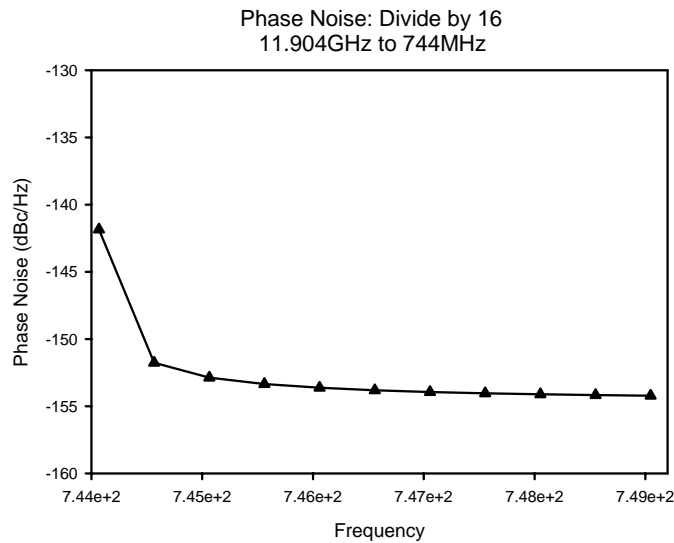
**Figure 53: Divide by 16 Simulated Phase Noise -Upper Frequency Limit**



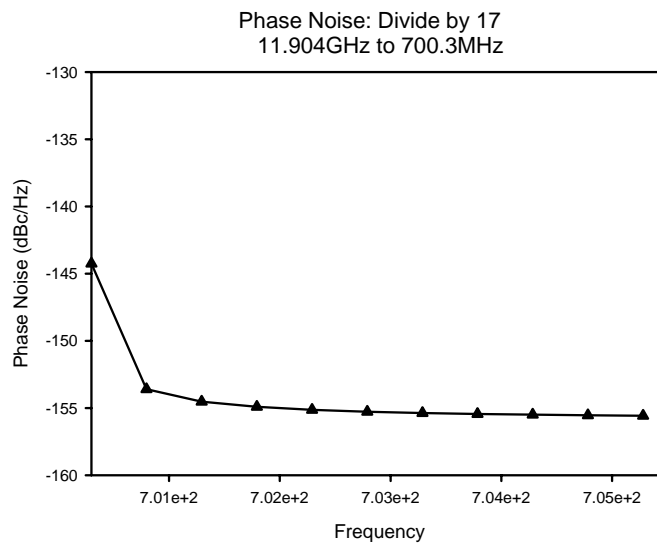
**Figure 54: Divide by 17 Simulated Phase Noise -Upper Frequency Limit**

The PLL is supposed to lock to a frequency closer to the center band of the prescaler and therefore the phase noise at the center of the band is the most pertinent for

our application. The 11.904 GHz input signal is divided by 16 to provide the 744 MHz signal and divided by 17 to provide the 700.23 MHz signal. The phase noise @ 1 MHz offset is shown for both division ratios in Figure 55 for divide by 16, -152.25 dBc/Hz at 745 MHz and Figure 56 for divide by 17, -154 dBc/Hz at 701.23 MHz.

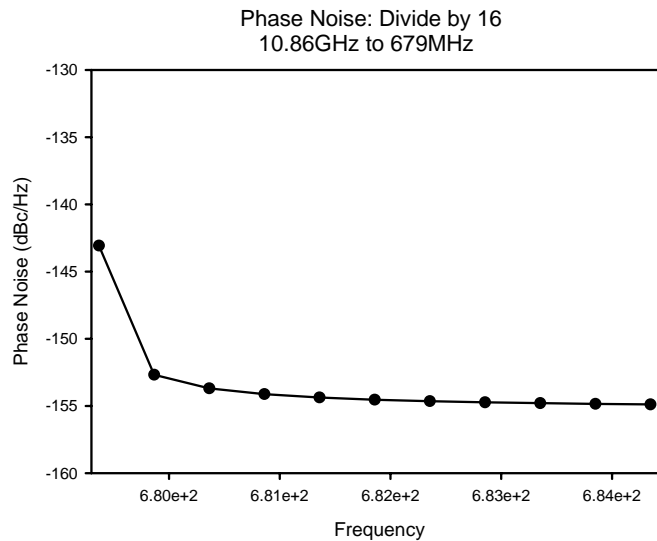


**Figure 55: Divide by 16 Simulated Phase Noise–Center Band Frequency**

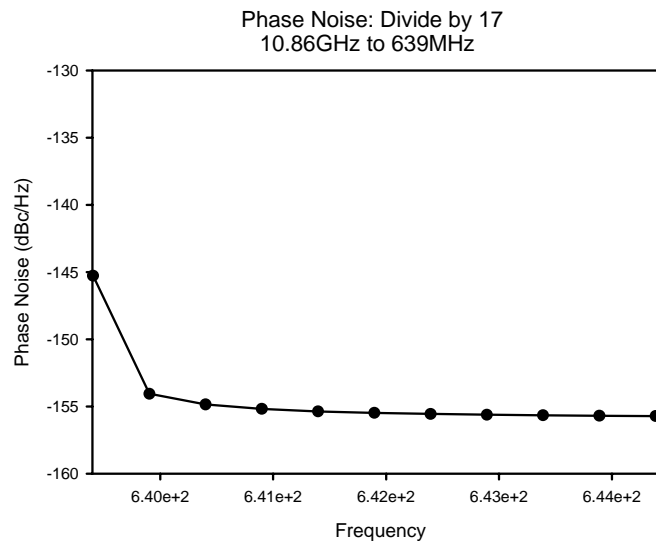


**Figure 56: Divide by 17 Simulated Phase Noise–Center Band Frequency**

The 10.86 GHz input signal is divided by 16 to provide the 678.75 MHz signal and divided by 17 to provide the 638.82 MHz signal. The phase noise @ 1 MHz offset is shown for both division ratios in Figure 57 for divide by 16, -152.5 dBc/Hz at 679.75 MHz and Figure 58 for divide by 17, -154.5 dBc/Hz at 639.82 MHz.

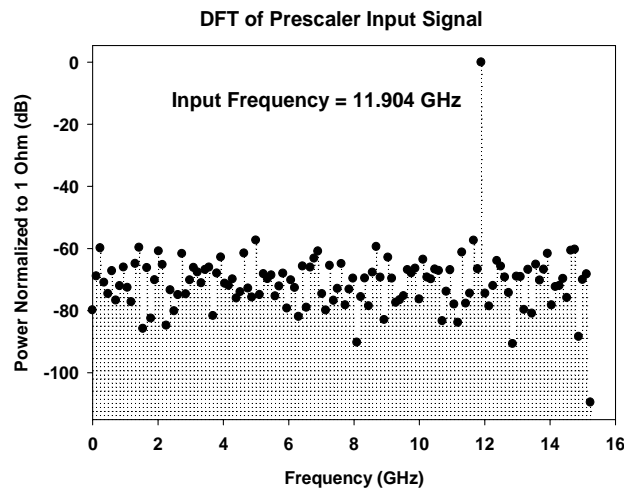


**Figure 57: Divide by 16 Simulated Phase Noise–Lower Frequency Limit**

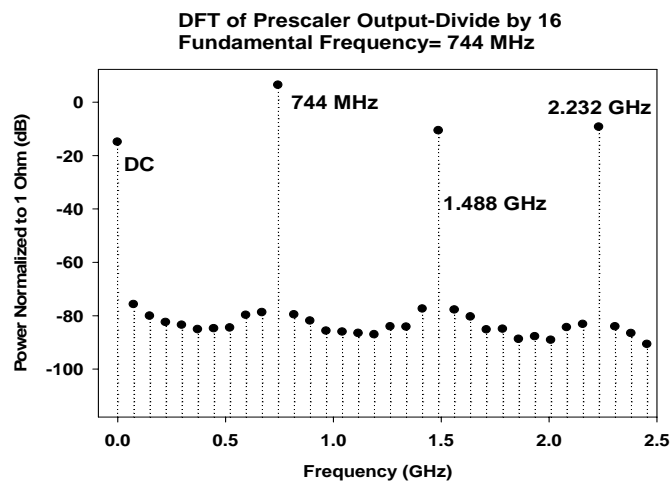


**Figure 58: Divide by 17 Simulated Phase Noise–Lower Frequency Limit**

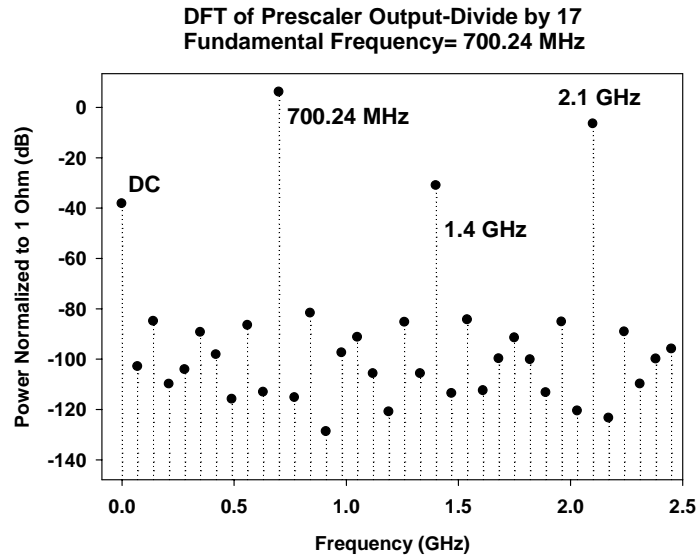
It is notable to mention that the level of phase noise is close in all six cases. The variation across the frequency band and also from mode to mode difference is small. As operating frequency decreases, a slight reduction in phase noise is visible. Indeed, the lower output frequency in divide by 17 mode shows less phase noise even though it has more switching transistors contributing noise compared to divide by 16 mode at the same frequency. The following plots are the simulated input and output spectrum of the prescaler. Figure 59 shows the spectrum of the input signal.



**Figure 59: Discrete Fourier Transform of the Input Signal**



**Figure 60: DFT of the Output Signal during Divide by 16**



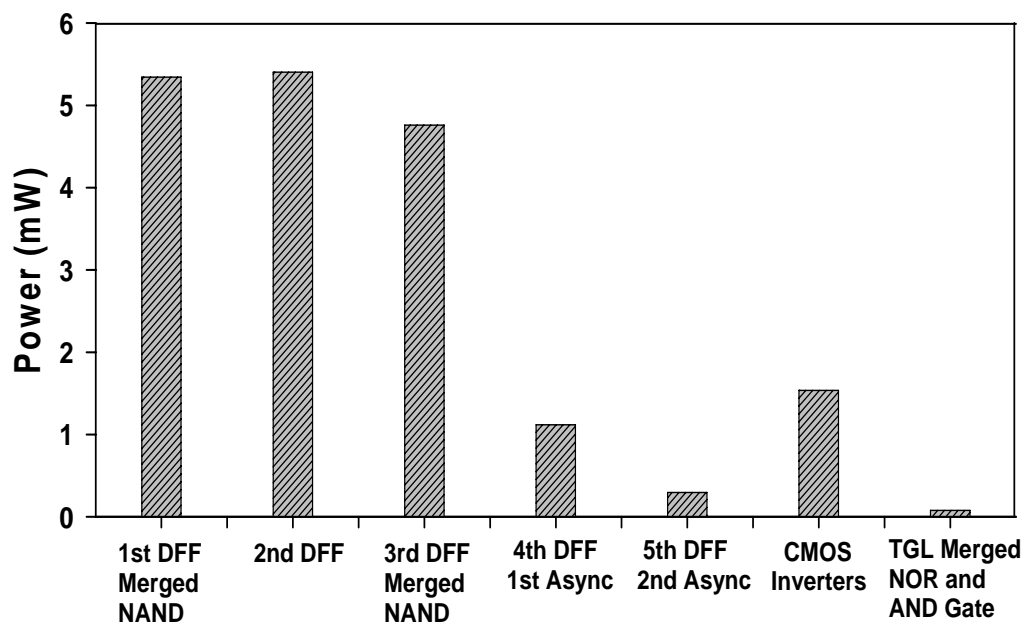
**Figure 61: DFT of Output Signal during Divide by 17**

In Figure 60 and Figure 61, the discrete fourier transform of the transient response of the prescaler is shown. The large 2<sup>nd</sup> and 3<sup>rd</sup> order harmonics are expected and desirable because the intended output is a digital square wave.

**Table 10: Post Layout Simulated Specifications for Prescaler**

Technology	.18 $\mu$ TSMC
Divide Ratio	16/17
Power Consumption	18.5 mW
Phase Noise @ 1 MHz Offset	-150 dBc/Hz
Size ( $\mu\text{m} \times \mu\text{m}$ )	~(160 x 125)
Area	.02 mm <sup>2</sup>
Input Signal (Center at 900mV)	2 V <sub>pp</sub> (7.63 dBm)
Output Amplitude (Center at 900mV)	3.2 V <sub>pp</sub> Rail to Rail
Input Frequency Range	11.11-12.98 GHz

In Table 10, a summary of the post layout simulation results are given. The signal is both amplified and divided at once. This combined with the low power consumption, small silicon footprint, and low phase noise make this prescaler example of a well-rounded and state of the art implementation.

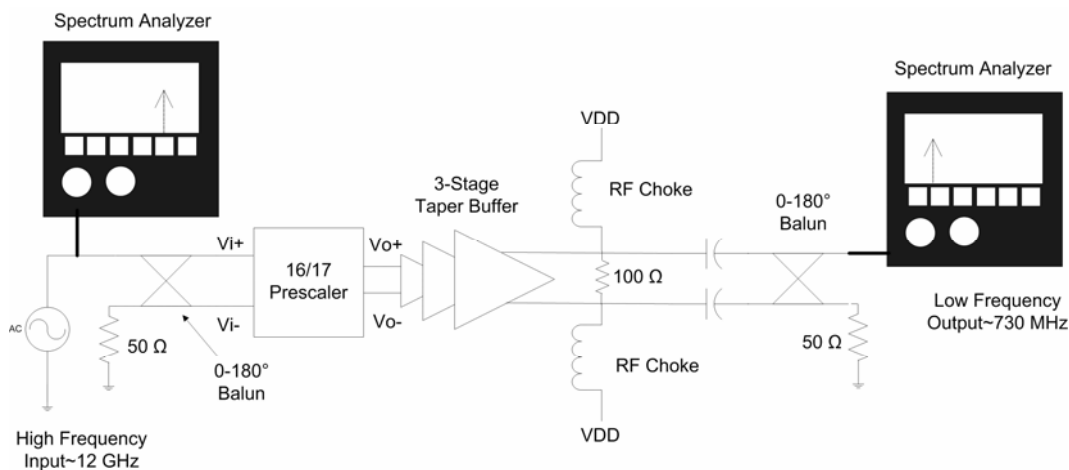


**Figure 62: Bar Graph of Power Consumption by Prescaler Sub-circuits**

In Figure 62, a breakdown of the simulated power distribution for each sub-circuit of the prescaler is shown. Clearly, the TGL gate uses very little power compared to other sections of the prescaler.

## 5. Measurement Results

### 5.1 Test Conditions and Setup

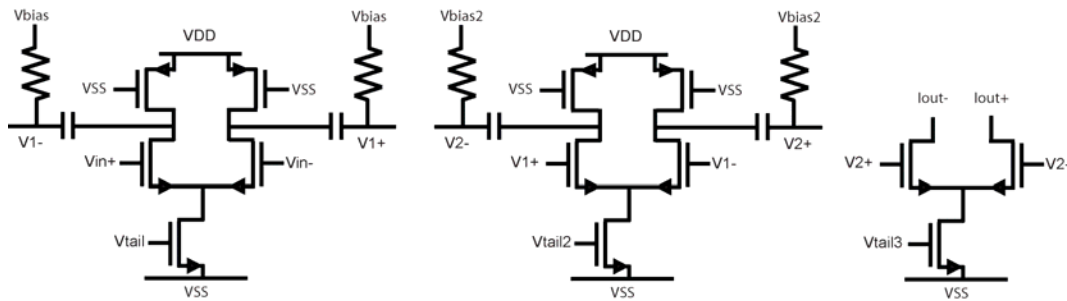


**Figure 63: Measurement Setup for the 16/17 Prescaler**

The measurement test setup is shown in Figure 63. A high frequency source (HP8673C from Agilent Technologies) generates a single ended sine wave within the 11-13 GHz range which then is converted into a differential signal by using a wideband (6-26 GHz) 0-180 degree hybrid coupler (from Krytar) with very small phase and amplitude imbalance before being applied to the prescaler. The output of the prescaler in an actual PLL would be high impedance however the output signal is measured by a spectrum analyzer (E4446A from Agilent Technologies) which has a low input impedance of 50 ohms. Therefore, a buffer must be placed at the output of the prescaler in order to attain the desired measurement. The last stage of the buffer is an open drain type and therefore must be biased with 1.8V DC source using a RF choke. The coupling capacitor transfers the AC signal into a low frequency 0-180° signal combiner (from



MiniCircuits. The signal is converted to a single-ended signal again at the output of this combiner and is ready to be measured by the spectrum analyzer.

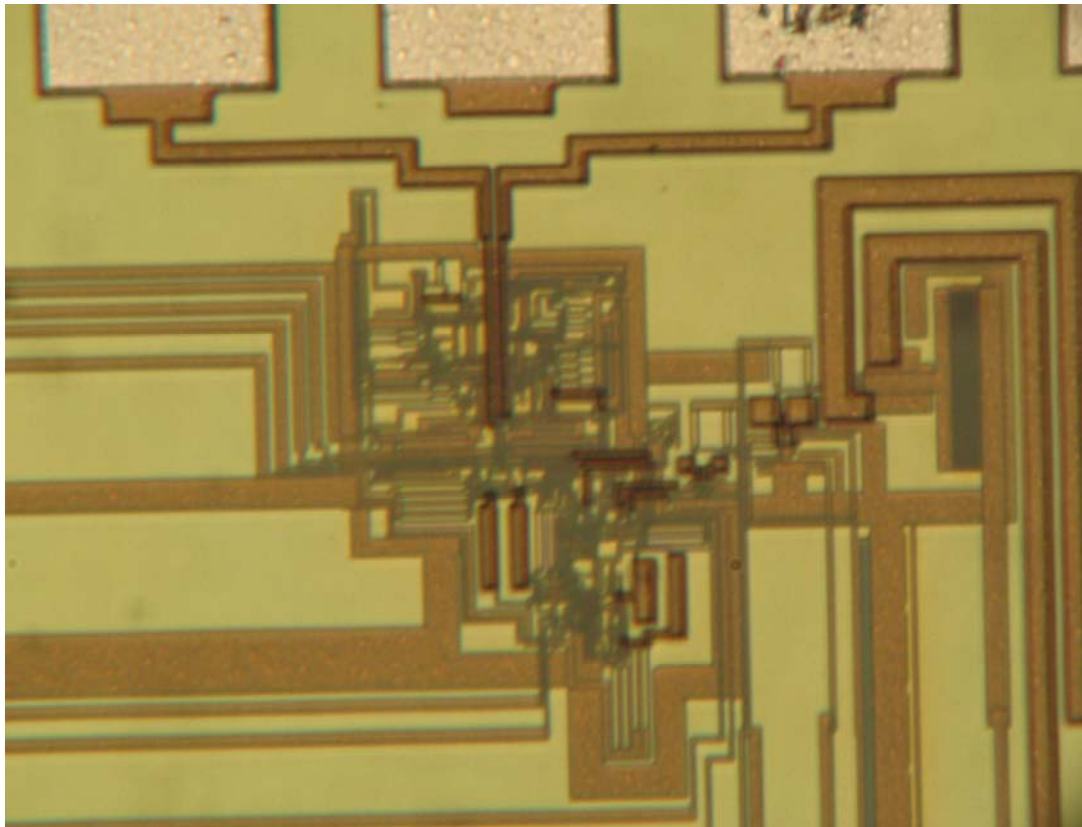


**Figure 64: 3-Stage CMOS Output Buffer for On-Wafer Measurement**

The three stage output buffer for the prescaler is shown in Figure 64. The function of this circuit is to gradually lower the output impedance from a high impedance seen at the output of the prescaler to a low impedance seen into the spectrum analyzer. Each stage uses AC-coupling to provide an adjustable input common-mode bias point. When this feature is combined with an adjustable tail current source for output common mode adjustment in each stage, the operating region of the signal processing transistors can be well controlled. This large amount of adjustability in the buffer vastly increases the probability of attaining an experimental measurement from the project due to buffer failure. Since the operating frequency range for this buffer is 653 MHz to 813 MHz, the corner frequency of the high pass AC-coupling filter must be significantly lower than this frequency range in order to provide good signal transfer from one stage to another. The PMOS load transistors are configured with their gates attached to the bottom supply rail to ensure their operation in the triode region. This provides a low resistance and a low contribution to the parasitic capacitances at the output node. This reduction of capacitance maximizes the voltage slew rate which lowers the measured phase noise at the output of the buffer.

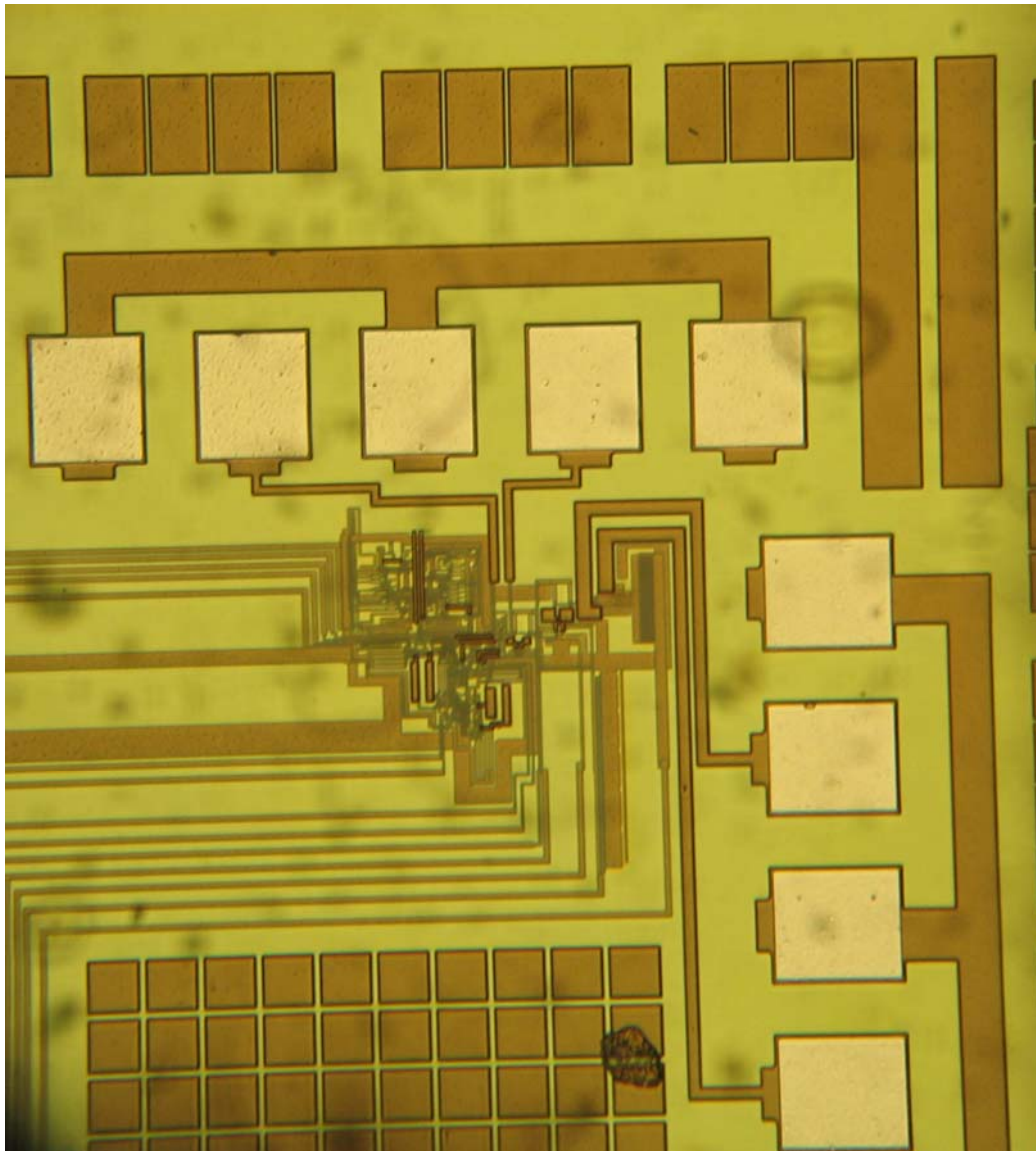
## 5.2 Chip Micrographs

This section presents two micrographs of the on-chip prescaler and buffer.



**Figure 65: Chip Micrograph #1**

In Figure 65, the chip micrograph of the prescaler is shown.



**Figure 66: Chip Micrograph #2**

In Figure 66, a micro graph of the prescaler with the input and output pads is shown. The top horizontal pad are the input pads which provide the input differential signal through a ground-signal-ground-signal-ground (GSGSG) differential probe. The vertical pads on the right are the output pads which provide the output signal through another GSGSG differential probe to the spectrum analyzer.

### 5.3 Measurement Information

The measurement procedure consists of a series of steps which provides the most relevant specifications about the prescaler. These specifications include the power consumption, the phase noise and the operating bandwidth. In order to correctly characterize the phase noise and power consumption of the prescaler, the effect of the output buffer must be separated from the prescaler. This is a simple task for power consumption as the buffer was placed on a separate power supply. However, separating the phase noise of the buffer from the prescaler is not trivial and the buffer could contribute significant noise and degrade the measurement performance. To deal with this issue, we will use information provide by simulation for the buffer to allow us to infer the underlying prescaler performance from the measurement data. It is important to note that the operating bandwidth of the prescaler should not be affected by the output buffer. In the following, we will describe the performance of the prescaler by first showing the raw measurements. This will be followed with some corrections which can be made because the cable losses are known as are the buffer simulation results.

The raw measurement of the combined prescaler and buffer with no corrections, such as phase noise or input power correction, is given in Table 11.

**Table 11: Raw Uncorrected Measurement Results**

Technology	.18 $\mu$ TSMC
Divide Ratio	16/17
Power Consumption	19.8 mW
Phase Noise @ 1 MHz Offset @ 12.5 GHz Input	-114.3 dBc/Hz
Phase Noise @ 1 MHz Offset @ 13 GHz Input	-113.2 dBc/Hz
Phase Noise @ 1 MHz Offset @ 11 GHz Input	-111.8 dBc/Hz
Input Power	10 dBm
Input Frequency Range	11-13 GHz

The first correction is to calculate the phase noise that will be added by the output buffer. The buffer serves as an impedance matching block. This is necessary because the prescaler must drive the 50 ohm load on the spectrum analyzer for measurement instead of a high impedance load it would normally drive in a real application.

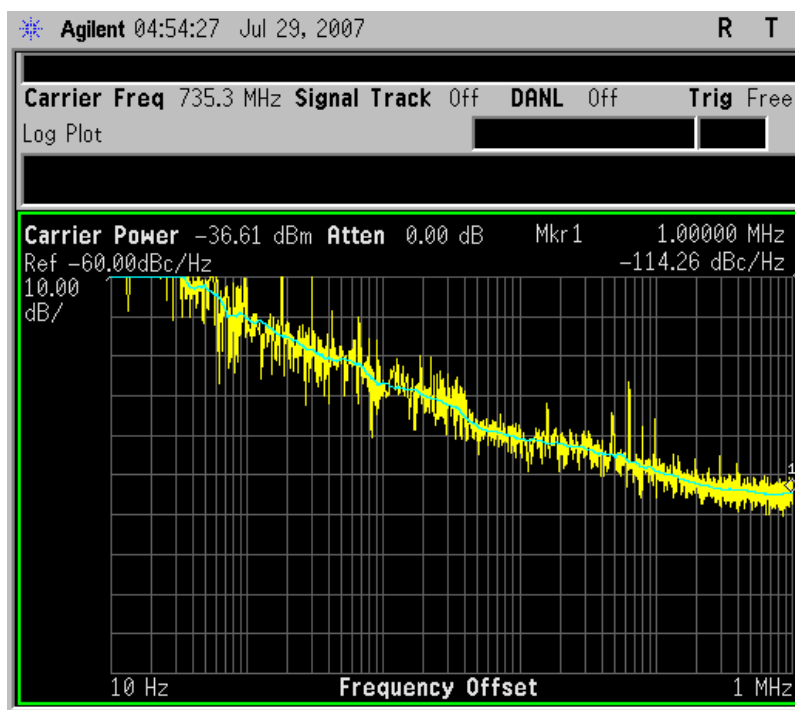
During simulation it was noted that the phase noise at the input and the output of the buffer differs by 15 dB at 1 MHz offset. This is similar to saying that the signal to noise ratio has degraded by 15 dB through the buffer. We will assume the measured buffer has a similar degradation to phase noise and at the same time note that this assumption probably is somehow optimistic and the buffer would most probably contribute a larger amount of noise. Also the cable loss at the input of the prescaler attenuates the input signal from 10 to 7.6 dBm. Corrected results after considering the effect of the buffer and input cable losses are shown in Table 12.

**Table 12: Buffer Corrected Measurement Results**

Technology	.18 $\mu$ TSMC
Divide Ratio	16/17
Power Consumption	19.8 mW
<b>Phase Noise @ 1 MHz@ 12.5 GHz Input</b>	<b>-129.5 dBc/Hz</b>
<b>Phase Noise @ 1 MHz @ 13 GHz Input</b>	<b>-128.4 dBc/Hz</b>
<b>Phase Noise @ 1 MHz @ 11 GHz Input</b>	<b>-127 dBc/Hz</b>
<b>Input Power</b>	<b>7.7 dBm</b>
Input Frequency Range	11-13 GHz

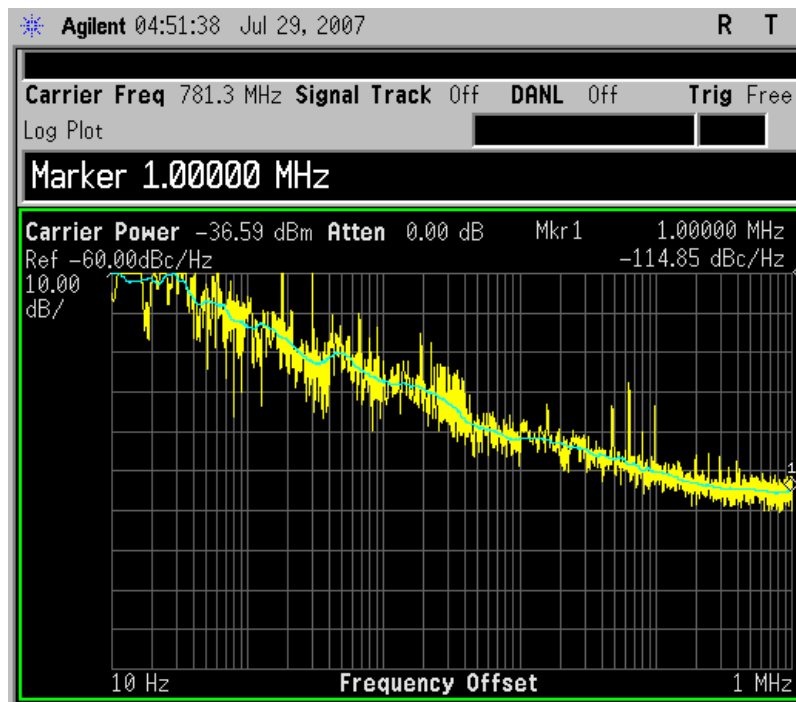
This table is closer to the simulated results, however, the simulation results show slightly lower power consumption but this can be justified. When the prescaler layout was extracted, inductive effects were not included and neither were the non-ideal effects of the power supplies. Therefore, a slight increase in power consumption would be necessary to overcome these negative effects. The other specification that still stands out

is the phase noise. The simulated prescaler employed noiseless frequency sources but that could never be the case in a real world experiment.



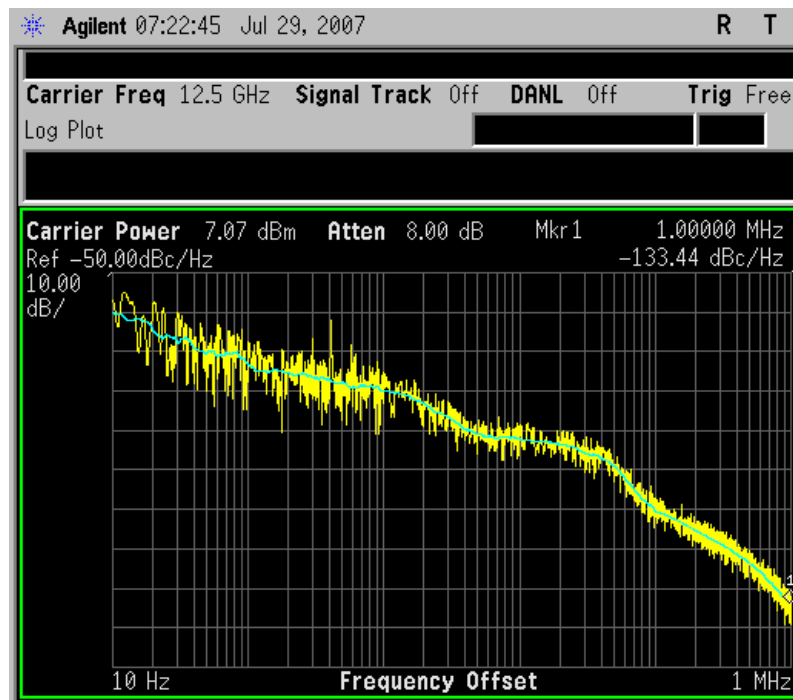
**Figure 67: Phase Noise in Divide by 17 fin=12.5 GHz**

The phase noise screenshot which was measured at the output of the buffer at a input frequency of 12.5 GHz and while in divide by 17 mode is shown in Figure 67. The phase noise at 1 MHz offset is shown to be -114.26 dBc/Hz. According to the simulation, the buffer contributed 15 dB to that number so the actual phase noise is -129.26 dBc/Hz.



**Figure 68: Phase Noise in Divide by 16 Fin=12.5 GHz**

The phase noise in divide by 16 mode is shown in Figure 68 for completeness. It is -114.85 dBc/Hz at a offset of 1 MHz.



**Figure 69: Phase Noise of Frequency Source at 12.5 GHz**

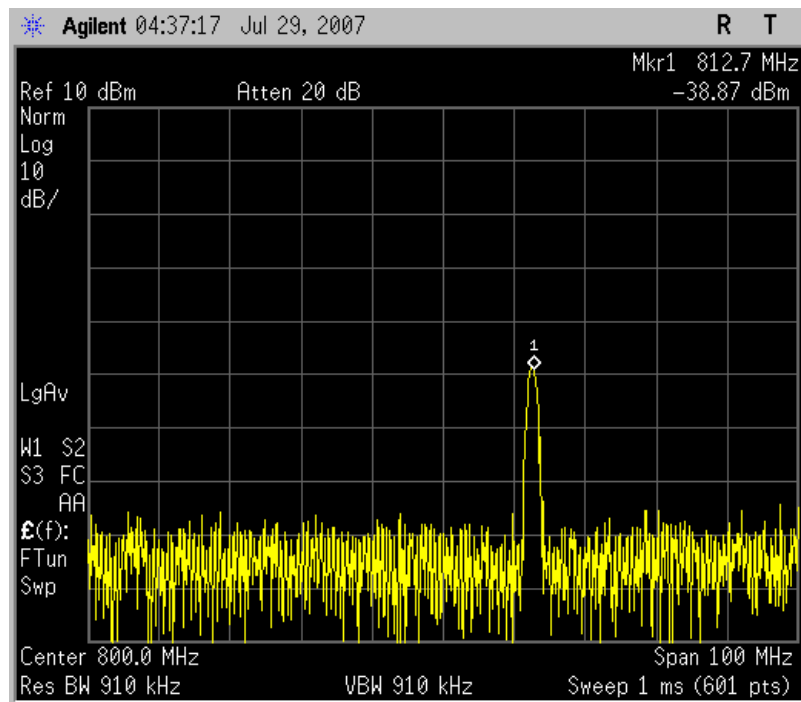
The phase noise plot of the source at 12.5 GHz is shown in Figure 69. The measured phase noise at 1 MHz offset is shown to be -133.44 dBc/Hz. If we maintain a constant frequency offset of 1 MHz and divide the frequency by two, the phase noise should decrease by 6 dB. We will call this effect the phase noise reduction from frequency division. Considering this effect and assuming the prescaler was noiseless with unity gain, we should expect the phase noise at the output of the prescaler to be -157.44 dBc/Hz. However, the prescaler gain is less than unity and this loss of prescaler should reduce both the signal and noise power equally. But this does not happen because the initial absolute noise power level at the output of the prescaler at a certain frequency offset is already near the thermal noise floor due to the phase noise reduction from



frequency division. Therefore, even a small prescaler loss is significant enough to push the absolute noise power level at the output of the prescaler to the thermal noise floor and resist further attenuation. On the other hand, the initial power of the signal is quite high compared to the thermal noise floor and attenuated the full amount of loss. In essence, the signal and noise power levels are attenuated by different amounts. Phase noise is a relative ratio between the signal power and the noise power and is usually specified at a certain frequency offset from the primary signal. It will certainly be degraded because the noise power reaches its minimum level while the signal does not and is further attenuated, reducing the ratio between the two numbers. In conclusion, unless the prescaler is initially very noisy at a certain frequency offset, the phase noise at that offset will always be equal to difference between the signal power and the thermal noise floor power at the output of the prescaler.

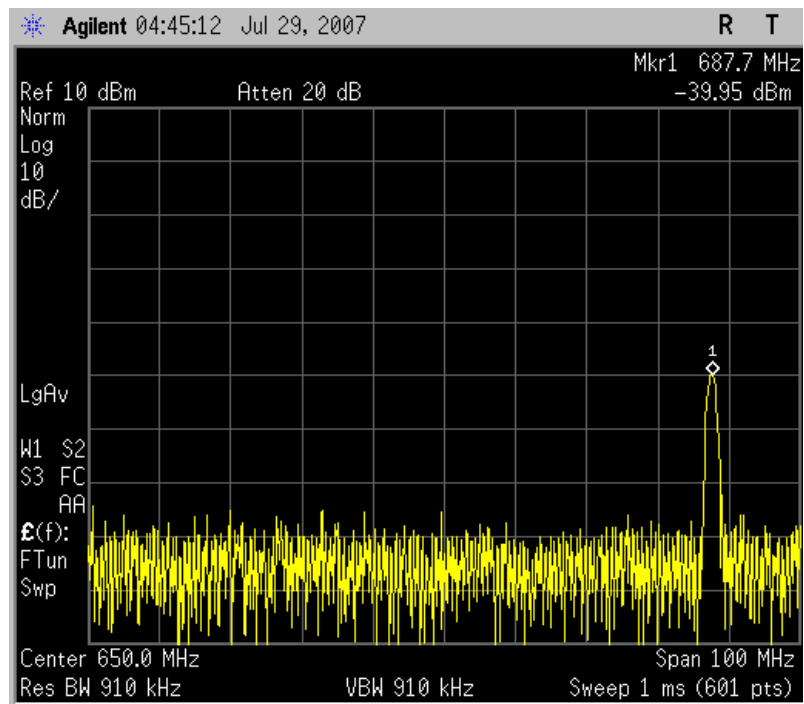
As mentioned before, the buffer-corrected phase noise at the output of the prescaler is -129.46 dBc/Hz. This is about 4 dB higher than the phase noise of the frequency source at the input. therefore we can say that all the combined effects on the signal while traveling through the prescaler cause an approximate 4 dB degradation in phase noise at a 1 MHz offset from the carrier.

Now, we look at the measured operational bandwidth of the prescaler.



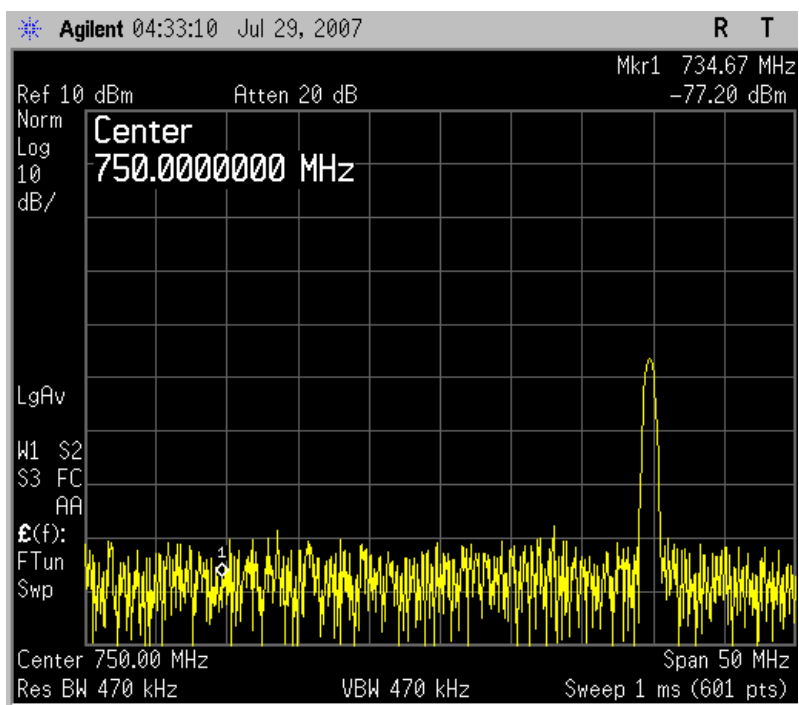
**Figure 70: Divide by 16, fin=13 GHz, fout=812.7 MHz**

In Figure 70, when the input frequency is 13 GHz, there is a signal at the output of the prescaler showing that the prescaler divides correctly up to the desired frequency in divide by 16 mode.



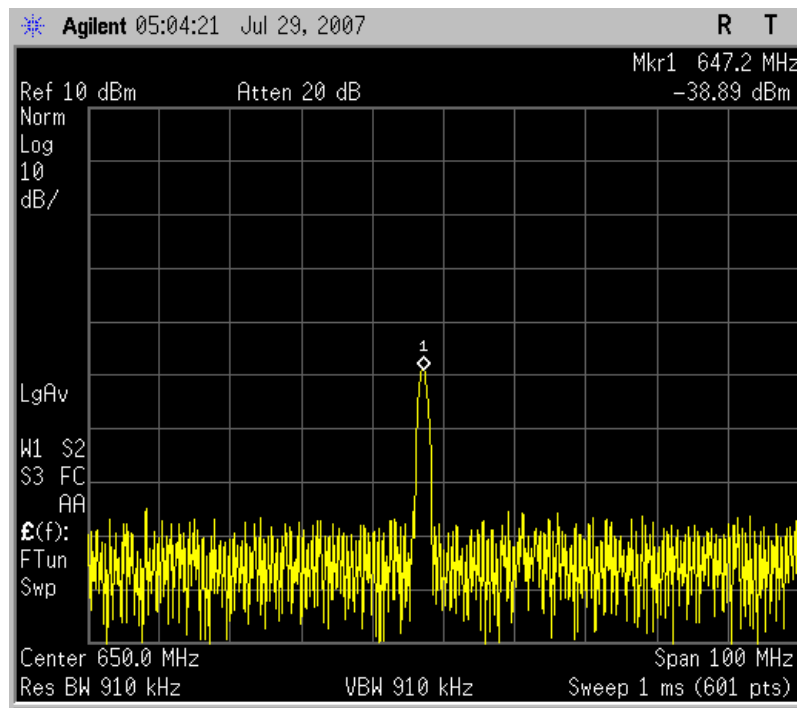
**Figure 71: Divide by 16, fin=11 GHz, fout= 687.7 MHz**

In Figure 71, when the input frequency is 11 GHz, there is a signal at the output of the prescaler showing that the prescaler divides correctly down to the desired frequency in divide by 16 mode.



**Figure 72: Divide by 17,  $f_{in}=13$  GHz,  $f_{out}=764.7$  MHz**

In Figure 72, when the input frequency is 13 GHz, there is a signal at the output of the prescaler showing that the prescaler divides correctly down to the desired frequency in divide by 17 mode.



**Figure 73: Divide by 17, Divide fin=11 GHz fout=647.2 MHz**

In Figure 73, when the input frequency is 11 GHz, there is a signal at the output of the prescaler showing that the prescaler divides correctly down to the desired frequency in divide by 17 mode. In Figure 70 through Figure 73, the measured bandwidth of the prescaler is demonstrated, which is equal to the expected bandwidth from post-layout simulation.

## 6. Comparison with Other High Frequency Prescalers

**Table 13: Comparison of Dual or Triple Modulus Prescalers**

	This Work	[19]	[3]	[28]
Year	2007	2004	2007	2005
Supply Voltage (V)	1.8	1.8	1.8	1.2
Process ( $\mu\text{m}$ )	.18 TSMC	.18	.18 TSMC	.09
Max Frequency (GHz)	13	14	16	24
Divide Ratio	16/17	256/257	6/7/8	4/5
Power (mW)	19.8	28.8	40	34
Phase Noise at 1 MHz Offset (dBc/Hz)	-129.5	N/A	N/A	N/A
Area ( $\text{mm}^2$ )	.02	N/A	.04	.23 <sup>†</sup>

Table 13 presents a comparison between this work and recent prescalers. The most remarkable advantage is the low power consumption and small area used in this work to provide high operating frequency. The circuit achieves a maximum operating frequency of 13 GHz while consuming only 19.5 mW of power. In [19], the maximum operating frequency is slightly higher at 14 GHz but power consumption is significantly higher at 28.8 mW. In [3], the maximum frequency is a few GHz higher at 16 GHz but the circuit consumes more than twice the power at 40 mW. The primary reason for the disparity in efficiency is the fact that the other works are designed for simultaneous performance in a variety of specifications while this work focuses on a reducing power for a single application. For instance, in [19], the large divide ratio (256/257) may be unnecessary as dividing 14 GHz by a lower ratio would still place the prescaler output frequency within range of very low power dynamic logic and save some power. In [3], the input bandwidth of the prescaler is very large but limitations in other blocks (i.e. VCO) of the PLL will prevent the PLL from taking full advantage of the large bandwidth in the prescaler, resulting in inefficient use of power. A prescaler with large input bandwidth is necessary to ensure wide acquisition range in a PLL. However, it should be optimized to the application (i.e. VCO tuning range for PLL design) in order to ensure power is consumed only to provide operation in the frequency band required. In [28], the maximum frequency is very high at 24 GHz but the division ratio of 4/5 results in the output frequency of the prescaler located at 6 GHz. This is very fast for dynamic logic and therefore the division ratio might need to be increased for a practical application or the following block (i.e. counter) will need to have enhanced performance. Either of these options will increase the total power consumption above 34 mW. Additionally, the prescaler in this work occupies the smallest chip area among recent prescaler designs. This small area means shorter interconnect pathways which directly translates into fewer parasitics, reduced delay and decreased power consumption for the overall system.

## V SUMMARY AND CONCLUSIONS

A 16/17 prescaler has been designed in .18 $\mu$  TSMC technology. The designed prescaler operates in a 2 GHz bandwidth to ensure large lock-in range for PLL applications. The design uses CML when necessary for high frequency operation and TGL for the lower frequency sections. The layout was optimized for equal capacitive loads at each DFF output, preventing a critical path which would severely degrade performance. The achieved power consumption is 19.8 mW which is notable for prescalers operating at high frequencies above 10 GHz.



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## VITA

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