DESIGN OF CLOCK DATA RECOVERY INTEGRATED CIRCUIT FOR HIGH SPEED DATA COMMUNICATION SYSTEMS

A Dissertation

by

JINGHHUA LI

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2008

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Edgar Sanchez-Sinencio
	Weiping Shi
	Hongbin Zhan
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ABSTRACT

Design of Clock Data Recovery Integrated Circuit for High Speed Data Communication Systems.

(December 2008)

Jinghua Li, B.S., Harbin Engineering University; M.S., Shanghai Jiaotong University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

Demand for low cost Serializer and De-serializer (SerDes) integrated circuits has increased due to the widespread use of Synchronous Optical Network (SONET)/Gigabit Ethernet network and chip-to-chip interfaces such as PCI-Express (PCIe), Serial ATA(SATA) and Fibre channel standard applications. Among all these applications, clock data recovery (CDR) is one of the key design components. With the increasing demand for higher bandwidth and high integration, Complementary metal-oxide-semiconductor (CMOS) implementation is now a design trend for the predominant products.

In this research work, a fully integrated 10Gb/s (OC-192) CDR architecture in standard 0.18μm CMOS is developed. The proposed architecture integrates the typically large off-chip filter capacitor by using two feed-forward paths configuration to generate the required zero and poles and satisfies SONET jitter requirements with a total power dissipation (including the buffers) of 290mW. The chip exceeds SONET OC-192 jitter tolerance mask, and high frequency jitter tolerance is over 0.31 UI_{pp} by applying PRBS

data with a pattern length of 2^{31}-1.The implementation is the first fully integrated 10Gb/s CDR IC which meets/exceeds the SONET standard in the literature.

The second proposed CDR architecture includes an adaptive bang-bang control algorithm. For 6MHz sinusoidal jitter modulation, the new architecture reduces the tracking error to 11.4ps peak-to-peak, versus that of 19.7ps of the conventional bang-bang CDR. The main contribution of the proposed architecture is that it optimizes the loop dynamics by adjusting the bang-bang bandwidth adaptively to minimize the steady state jitter of the CDR, which leads to an improved jitter tolerance performance. According to simulation, the jitter performance is improved by more than 0.04UI,which alleviates the stringent 0.1UI peak to peak jitter requirements in the PCIe/Fibre channel/Sonet Standard.

DEDICATION

To my wife Daxin Wang,

For her true love and support;

And to my new-born daughter Annie;

And in memory of my Father-in-Law

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I need to thank my late father-in-law, who was a professor of electrical engineering, and who was very interested in seeing my integrated inductor. He always encouraged me to be confident of myself; however, I never had a chance to show him one. I dedicate my

circular inductor especially to him. Thanks also go to my parents, my mother-in-law and younger brother; they never requested anything during my six years study in Texas and highly encouraged me to finish my work.

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I. INTRODUCTION

I.1. Background of Optical Communications

The volumes of data transported over the telecommunications network have increased at a compounded annual rate of 100% from 1995 to 2002 in the US, mainly due to the increased Internet traffic. The call for technologies, such as the interface that expands the capacity of fiber-based transport links to10Gb/s (and beyond) has risen recently [1]. The Synchronous Optical Network (SONET) protocol has long become the standard in optical communications used in wide area networks (WAN). SONET standard specifies a set of transmission speeds, all of which are multiples of "OC-1" rate, which is 51.84 Mb/s. Currently OC-192, running at approximately 9.95328 Gb/s, will be, or, are being deployed throughout North America, due to the rising response to the explosion in data traffic. As a result, there is a great demand for low cost and fully integrated transmitter (TX) and receiver (RX) chips to be deployed in the internet backbone router, which is the core element in the network infrastructure [1].

A typical OC-192 transceiver is shown in Fig 1.1.A network processor converts input data into the form of 16 parallel signals, each operating at 622Mb/s. These signals are sent to the parallel inputs of the transmitter where they are synchronized to a precise reference clock and then serialized so that the output of the transmitter is a single channel operating at 9.95328Gb/s.

This dissertation follows the style and format of *IEEE Journal of Solid-State Circuits.*

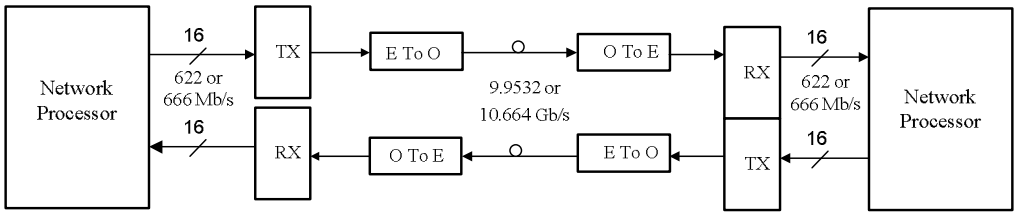


Figure 1.1 OC-192 Transceiver Architecture

The high speed serial transmitter output is used to modulate a laser driver, which generates the optical signal that is sent through the optical fiber. More details of the transmitter and receiver (transceiver) are shown in Figure 1.2. At the receiving side of the fiber, the light is applied to a photodiode connected to a trans-impedance amplifier (TIA) which then converts the signal back to electronic form. The transmitter and receiver (transceiver) is shown in Figure 1.2. The electronic signal is applied to a post-amplifier and then a limiting amplifier before it is passed to the clock data recovery (CDR), which extracts and recovers a clock synchronized to the incoming data stream at the input of the receiver. At the receiver side, a clock synchronized to the incoming data is generated using a clock data recovery (CDR) circuit. The recovered clock and re-timed data provided by the CDR are then applied to a de-multiplexer (DeMux) which outputs 16 parallel signals, each at 622Mb/s. These signals are applied to another network processor which performs the necessary overhead and framing operations. Among the transmitter and receiver blocks, CDR is the most critical and difficult block to design.

This research is focused on the design of the clock data recovery (CDR) IC for high speed data communications. As an example, Optical OC-192 CDR was designed to study the circuit implementation techniques.

As an initial phase, we designed a 2.5Gb/s OC-48 transceiver using TSMC 0.35um technology, such that some design experience was accumulated on the transceiver design. However, due to the limited cut-off frequency of the MOS transistors in TSMC 0.35um technology, it is not possible to design a 10Gb/s transceiver in TSMC 0.35um CMOS technology. Hence, the OC-192 CDR was finally designed in the TSMC 0.18um technology.

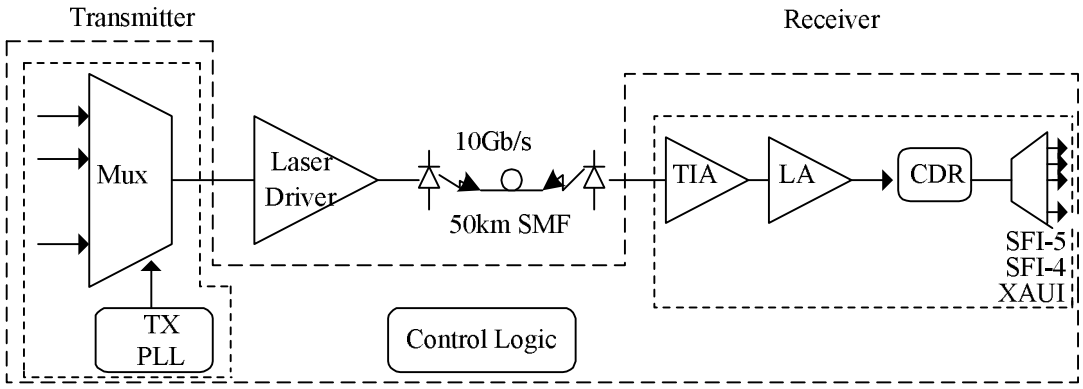


Figure 1.2 Optical Transceiver Block Diagram

The primary objective of this project is to design, layout and characterize an integrated clock data recovery circuit operating at a clock frequency of 10 Gb/s for OC-192 optical communications. The previously reported 10 Gb/s CDR ICs require off-chip

loop capacitors that increase the difficulties of system design; increasing the pin counts, making the system more sensitive to external noise sources, and increasing the difficulty for PCB layout. For PCB design, the loop filter capacitor has to connect to the chip, and the routing complexity increases especially when the IC is packaged in flip-chip Ball Grid Array (BGA) package. This research is focused on implementing a fully integrated CDR IC and demonstrates the feasibility of the proposed design approach by using a new configuration to efficiently generate the equivalent full on-chip solution.

Also, in the practical applications of data communications and telecommunications, due to the variety of the noise sources, the data from the Fiber and backplane is jittery, and the jitter frequency is in general not known in advance, thus the CDR device has to re-time the data with an unexpected in-band jitter ranging from 50KHz to 80MHz, which is also noted as jitter tolerance. In this research work, a CDR architecture is proposed to track the data jitter adaptively, which is different from the conventional CDR architecture which can only track specific small range of in-band jitter.

I.2. Jitter Requirements of the CDR Device for Optical Communications

I.2.1. Jitter Transfer Specification

For the typical applications in Telecommunications, a chain of repeaters, which constitute both transmitter, receiver, laser driver and photo diode devices, are used to regenerate data to long-distance, thus any jitter in one PLL can accumulate to a

significant level in a series of tandem PLLs [2]. The jitter transfer function of a CDR circuit represents the relationship between output jitter versus the input jitter, which is the same as the closed loop phase response of a PLL, i.e, the output phase response versus the input phase across different input frequencies.In Figure 1.3(a), a chain of repeaters are drawn to help define the jitter transfer. The data Vi transmitted at the head of the chain has a clock data recovery based on a PLL, and the data is re-timed as V1. After some distance of transmission, distortion and noise require that the signal to be regenerated. For long-distance telecommunications, repeated clock data recovery operation may occur as many as several hundred times [2]. At the end of the chain, the output is Vo, which is the regenerated data from Vi. Each CDR circuit in the transmission path adds its own jitter to the total jitter of the chain. The accumulation of the jitter is described in Figure 1.3(b). Assume that the input data jitter θ_i is zero, and the static phase error of each PLL is the same, and thus each PLL has the same effective phase θ_s which is due to static phase error and data pattern. The jitter transfer function (JTF) of a PLL, $H(j\omega)$, is typically a low pass function between phase of the PLL output and that of the reference clock. The response $H(j\omega)$ is applied not only to the jitter introduced in the same repeater, but also the jitter introduced in all repeaters upstream. Then the overall transfer function from θ_s to the last stage output phase θ_o at the output for N repeaters can be represented as:

$$H_{total}(j\omega) = \sum_{i=1}^{N} H^i(j\omega) = H(j\omega)\frac{1-H^N(j\omega)}{1-H(j\omega)} \tag{1.1}$$

For a given *H(jω)* and jitter power spectrum, this relation allows us to predict the total jitter as a function of the number of repeaters. To reduce the jitter accumulation effect in a chain of repeaters, the jitter transfer specification that is defined in the Telecordia GR-253-CORE [3] standard requires the jitter peaking to be less than 0.1dB, and the corner frequency (f_c) is defined in Figure 1.4. For the data rate of OC-192(10Gb/s), the corner frequency is 120KHz, which is difficult to meet even if using LC tank VCO. However, as pointed out in [4], the jitter transfer characteristic can be shaped by the transmitter, which typically uses a PLL with a low bandwidth of 120KHz.

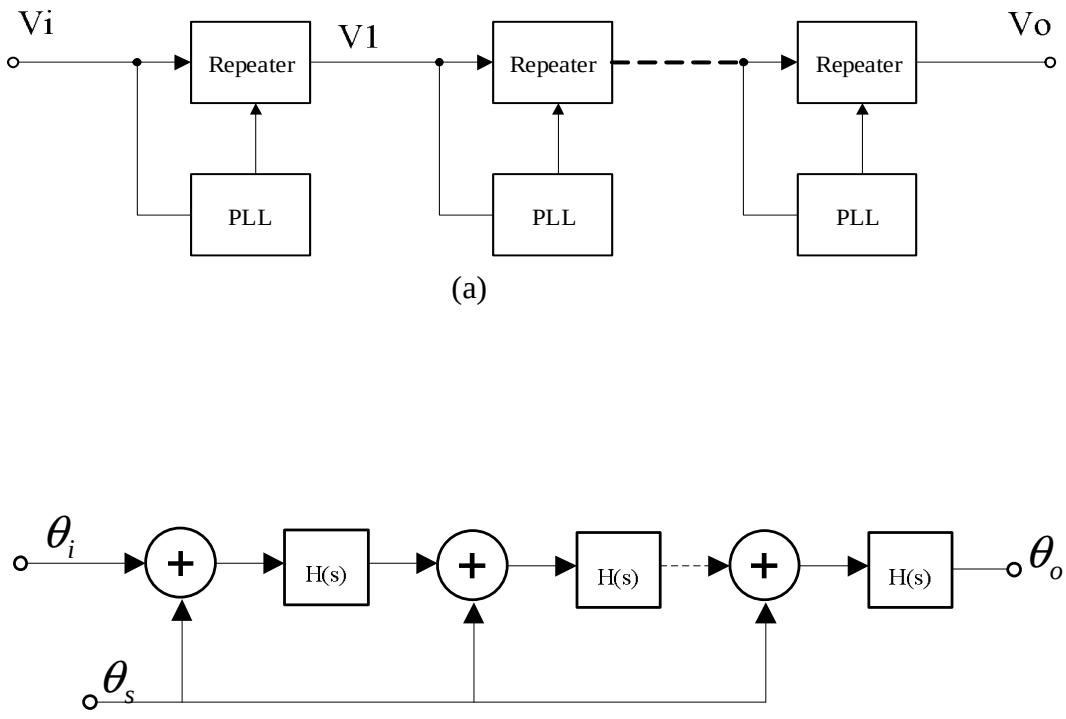
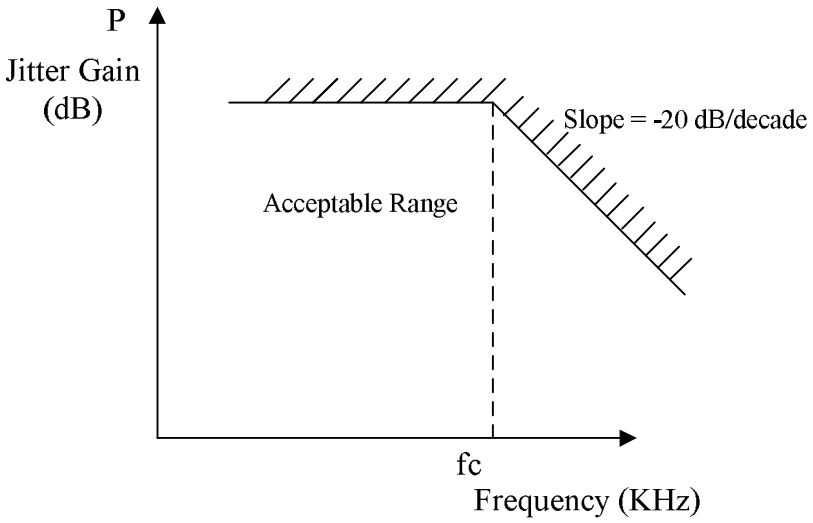


Figure 1.3 Jitter Accumulation: (a) Jitter Accumulation Diagram and (b) Jitter Accumulation in a Chain of N Repeaters



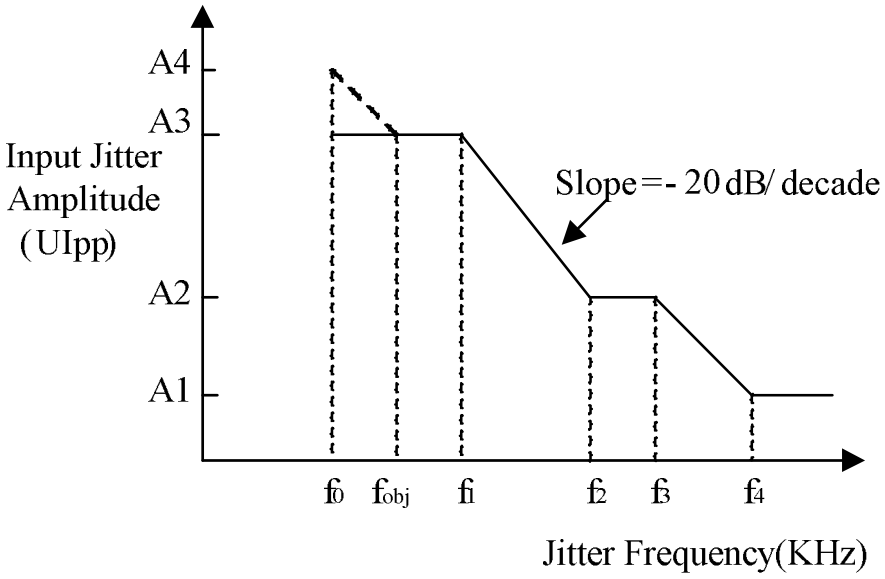
OC-N/STS-N Level	Fc (KHz)	P(dB)
1	40	0.1
3	130	0.1
12	500	0.1
48	2000	0.1
192	120	0.1

Figure 1.4 Jitter Transfer Mask of SONET OC-1 to OC-192

I.2.2. Jitter Tolerance Specification

Jitter tolerance is a measure of the capability of a regenerator to tolerate incoming jitter without causing the bit error rate less than 10^{-12}[3]. The measurement is done by

applying a sinusoidal jitter with peak to peak amplitude in peak-to peak Unit interval (denoted as UIpp, for OC-192, 1UIpp is 100ps). The jitter tolerance mask defined in the SONET standard is shown in Figure 1.5. For example, for OC-192 applications, the high frequency(>4MHz) jitter tolerance is required to be larger than 0.15UIpp.



OC-N/STS-N Level	f_0 (Hz)	f_{obj} (Hz)	F_1 (Hz)	f_2 (Hz)	f_3 (kHz)	f_4 (kHz)	A_4 (UIpp)	A_3 (UIpp)	A_2 (UIpp)	A_1 (UIpp)
1	10	NA	30	300	2	20	NA	15	1.5	0.15
3	10	NA	30	300	6.5	65	NA	15	1.5	0.15
12	10	18.5	30	300	25	250	27.8	15	1.5	0.15
48	10	70.9	600	6000	100	1000	106.4	15	1.5	0.15
192	10	206	2000	20000	400	4000	444.6	15	1.5	0.15

Figure 1.5 Jitter Tolerance Mask of SONET OC-1 to OC-192

I.2.3. Jitter Generation Specification

Jitter generation of a CDR specifies the jitter produced by the CDR circuit with no jitter or wander applied at the input. For a typical OC-192 CDR device, the jitter generation should be less than 0.1UIpp, or 0.01UIpp rms jitter [3].

I.3. Currently Reported CDRs

Currently, many existing 10Gb/s CDR ICs use expensive Bipolar or SiGe BiCMOS technology [5-9].The reported works in [10-13] adopt CMOS technology, however, all the implementations need off-chip loop filters to meet the jitter performance which is required by the SONET standard.

Savoj and Razavi [10] proposed a reference-less CDR which uses a double edged DFF based binary phase detector(BPD) and frequency detector(FD). The CDR architecture is shown in Figure 1.6. As can be seen in Figure 1.6, the whole CDR implementation is a dual-loop design which features both phase detection and frequency detection capability. The BPD shown in Figure 1.7 was first proposed by Anderson in his patent[14], and the frequency detector in Figure 1.8 uses two of the aforementioned DEFF BPDs. The frequency detector uses an 8 clock phase's clock. The architecture is basically the CMOS implementation of the previous work of Buchwald's GaAs HBT realization [15]. Although the implementation does not need a reference clock, it has limited frequency locking range when the data has long runs of 1's or 0's, and hence affect the jitter tolerance performance. As reported in [10], the IC realization based on

this approach is not able to pass jitter tolerance mask defined in SONET OC-192 standard.

Cao [11] proposed a full rate, dual loop CDR architecture with reference clock. The CDR uses a full rate linear phase detector whose output is proportional to the phase difference between the data and the VCO output. The pulse width is proportional to the phase difference, which is very difficult to control in 0.18μm CMOS technology with a unity gain frequency f_t of only 50GHz. For a robust design, the f_t has to be at least ten times of that of the data rate frequency.

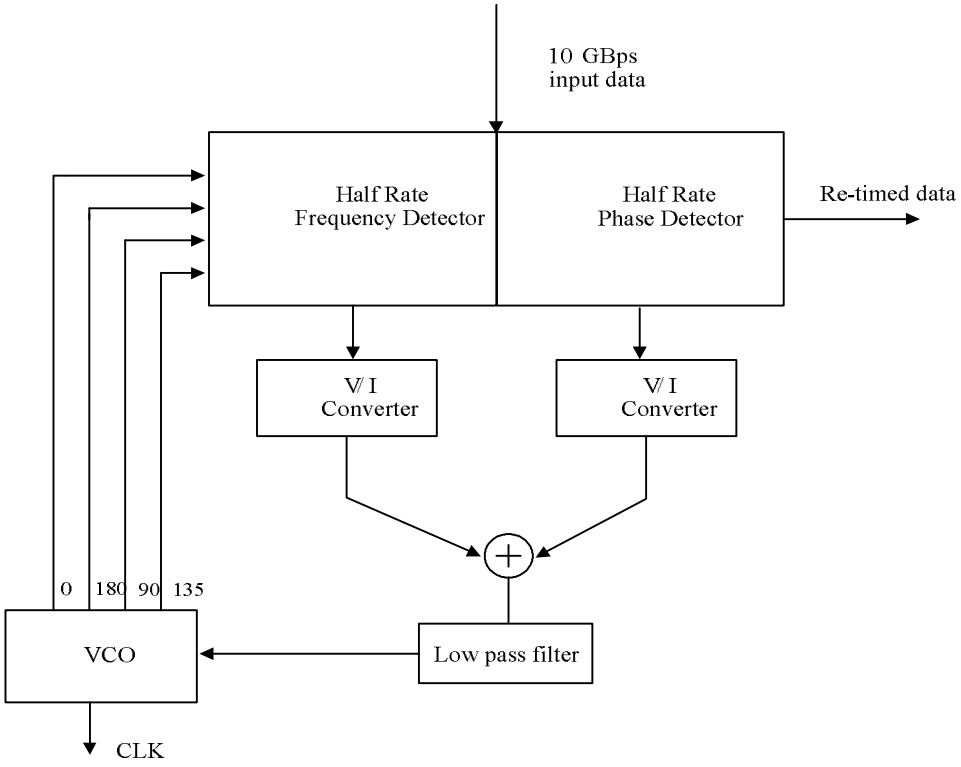


Figure 1.6 Reference-less CDR Architecture in [10]

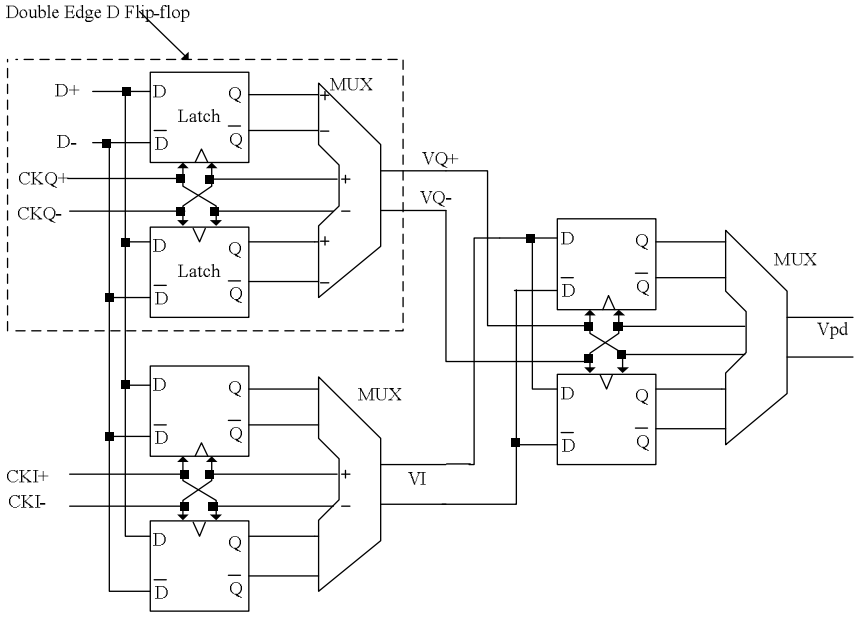


Figure 1.7 DEFF Phase Detector

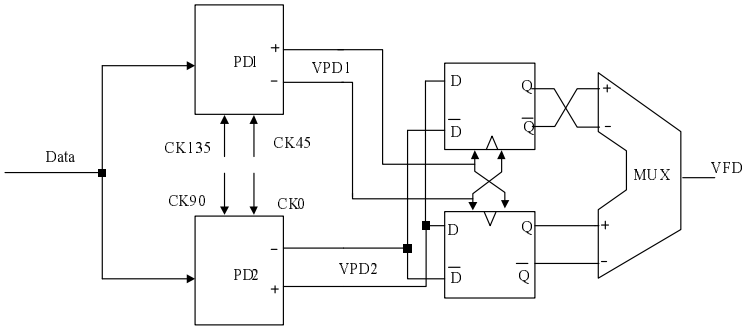


Figure 1.8 Frequency Detector Used in [10]

Rogers and Long [12] proposed a binary phase detector CDR architecture that does not include the frequency acquisition loop. The implementation features a LC delay cell based ring oscillator which is depicted in Figure 1.9, and slightly passed the jitter tolerance mask. This topology has very small pull-in range of only 0.21%.Adding a frequency detection loop will remedy this issue. However, the LC delay cell based oscillator is prone to process variations, which adds the difficulty in the oscillator modeling. Moreover, the LC delay cells consume large silicon area.

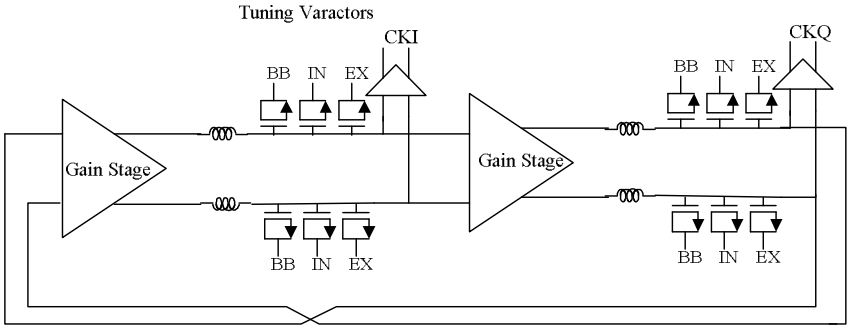


Figure 1.9 Ring Oscillator Using LC Delay Cell

In 2006, Sidiropoulos [13] used a DLL based CDR architecture. Since the DLL is a first order system, hence the resulting CDR has worse jitter tolerance and more jitter generation than PLL based CDR when asynchronous/Mesochronous operation is enabled.

I.4 Main Contribution of This Work

A major limitation of all previously reported topologies is that all of them use off-chip loop filters. So stringently they are not monolithic integrated designs. This research

work is focused on the integration of the whole CDR on a full on-chip solution, and by adopting a new loop filter configuration. The required zero and poles are generated by adding two feed-forward paths, and hence the use of expensive large capacitor integration is obviated.

In telecommunication and data communication systems, the noise and hence the jitter with the incoming data is not well known in advance, which increases the difficulty of the CDR to regenerate the original data. The second proposed CDR architecture utilizes an adaptive bang-bang control algorithm, which adjusts the CDR bandwidth under slope overload situation and steady state separately. The architecture is in essence an adaptive delta modulation (ADM) which predicts the actual CDR loop dynamics according to the past history. Comparing with the conventional Bang-bang CDR solution, the proposed architecture can adaptively adjust its bandwidth to tolerate the unknown jitter existing in the system and hence improve its jitter tolerance capability.

Besides, in this research, the study of the nonlinear properties of the bang-bang CDR is performed in detail. Due to the nonlinear nature of the phase detector used, a bang-bang CDR can not be simply analyzed using classical control theory as that in linear PLL/CDR system. In this dissertation work, for the first time, the describe function analysis method is used for the evaluation of the equivalent bandwidth of a bang-bang CDR.

This dissertation is organized as follows. Section II introduces the building blocks for the clock recovery applications. In Section III, a full on-chip CMOS Clock Data Recovery IC for OC-192 Applications is described in detail. A half rate binary phase

detector and the Quadrature VCO design contributed to the low power performance of the test chip. A dual charge pumps configuration and the on-chip loop filter realization lead the designed chip to a cheaper solution with higher jitter tolerance capability. Section IV describes a multi-Gigabit/s Clock data recovery architecture using an adaptive bang-bang control strategy. Finally the conclusions are drawn in Section V.

II. BUILDING BLOCKS FOR CLOCK DATA RECOVERY APPLICATIONS

Clock data recovery (CDR) is the key element of the telecommunication and data communication applications. A typical diagram of the conventional PLL based CDR is shown in Figure 2.1. The basic building blocks are input/output buffers, phase detector, charge pump, passive loop filter and VCO. Among the blocks, the input buffers amplify the input data amplitude for the phase detector to detect; the phase detector is used to generate the phase error between the input data and the VCO output; charge pump and loop filter are used to generate the control voltage for the VCO; the VCO is the clock generator.

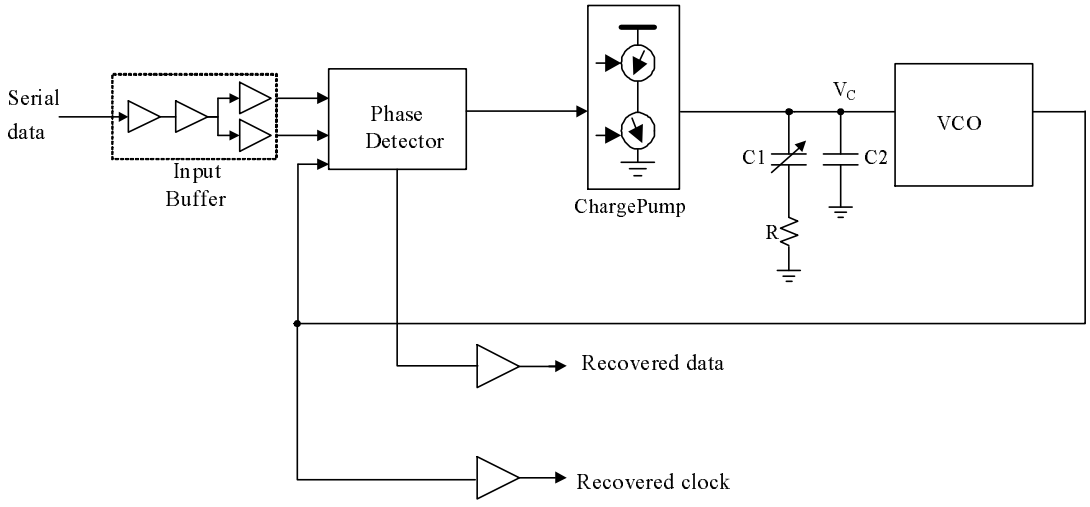


Figure 2.1 CDR Diagram

The Phase detector (PD) architectures for clock data recovery applications mainly include two categories: linear phase detector and binary phase detector. As shown in the following sections, the linear phase detector outputs the phase error which is proportional to the phase difference between the incoming data and the VCO output, while the binary phase detector outputs only the sign of the aforementioned phase difference. Thus the linear PD based CDR can be designed using linear analysis, while the binary PD based CDR can only be analyzed using nonlinear design procedure, which makes the design more complex. Secondly, when the data rate is in the range of 10Gb/s, the output of linear PD is the fractional potion of 100ps, which is very difficult for the prevalent CMOS technology, so quarter rate or even 1/8 rate phase detector with 4 or 8 slices of data path has to be used, which makes it very challenging to match several branches of high speed blocks. On the contrary, the binary phase detector only needs to output the sign of the incoming data and VCO output, so a full rate or a half rate implementation is possible. Thus the binary PD is preferred over the linear PD in the CDR design in recent publications of OC-192 ICs [13].

II.1. Linear Phase Detector

In the linear phase detectors that are used in the clock data recovery applications, Hogge Phase detector is used most frequently due to its inherently smaller jitter generation comparing with binary PD in low speed telecommunication products.

II.1.1. Hogge Phase Detector

A Hogge phase detector compares each data transition with the rising (or falling) edge of the retiming clock and generates pulses whose widths are proportional to the phase difference between the input data and clock[16]. Due to the random nature of the input data, it is not straightforward to compare the clock and data directly to extract the phase difference. However, by comparing with the input data and a delayed replica of the input data [16], the phase difference between the data and clock can be extracted indirectly. As illustrated in Figure 2.2, the random data is delayed by two D-FFs. One of the FFs samples its input on the rising edge of the clock and the other one samples it at the falling edge. The timing diagram is shown in Figure 2.3. Assume there is no clock-to-Q delay for the time being, if the clock is correctly aligned to the data, since the data at point B is a replicated version of the input data with a delay of exact half period of the clock. At the output of XOR_1, the pulse at Y is then a half period of the retimed clock. If the input data D_{in} has timing mismatch with the retimed clock, the pulse width will be smaller (or larger) than half a cycle of the retiming clock if the clock is early (or late) than the optimum. While the output at XOR2 is a constant half period of the retime clock. The difference between the pulse Y and X gives out the phase difference between the input data D_{in} and the retimed clock. Also, the pulses Y and X occur for every transition of the data. The pulse width at Y is directly proportional to the phase difference between the input data and retime clock, sometimes it is called proportional pulse. The pulse width at X is always half a cycle of the retime clock; it is often referred as reference.

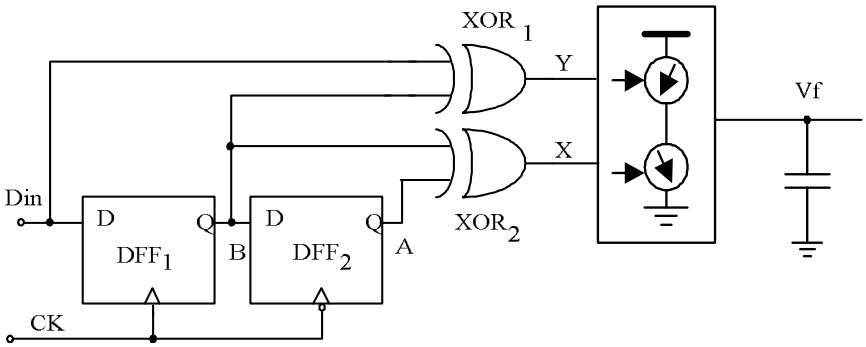


Figure 2.2 Hogge Phase Detector Implementation

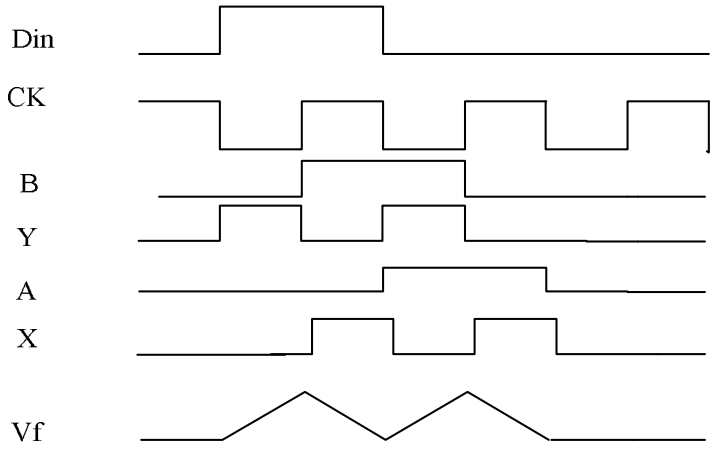


Figure 2.3 Timing Diagram of Hogge PD When Locked

One of the important features of Hogge phase detector is the automatic retiming of the incoming sequence. In the locked condition, the zero crossings of the clock signal appear in the middle of the data eye, which is the optimum point for data retiming.

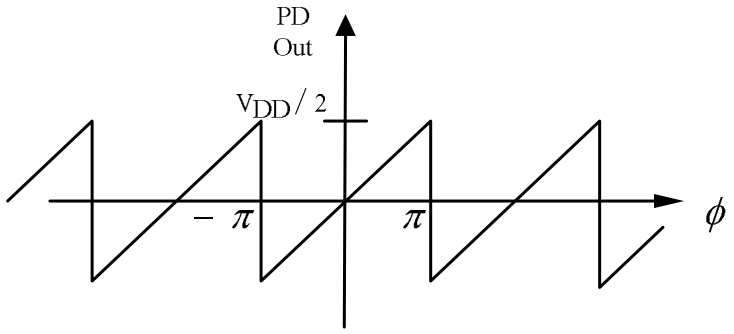


Figure 2.4 Characteristic of Hogge Phase Detector

However,as pointed out in [17], the Hogge phase detector has the retiming delay through DFF2, which leads to a half period skew between the pulses at XOR_1 output Y(error) and XOR_2 output X(reference). It can be concluded that, even in lock condition, a charge pump and loop filter driven by Error and reference produces a positive ramp when the reference is high, the control voltage of the VCO then experiences a triwave with a positive net area as in Figure 2.3. This positive net area will cause static phase offset in the retimed clock output even in the lock condition. The resultant control voltage versus phase difference transfer curve is illustrated in Figure 2.4, where the horizontal axis φ is the phase difference between the input data and recovered clock. It

can be seen that the relationship between the control voltage and phase difference is linear within [-π, π].

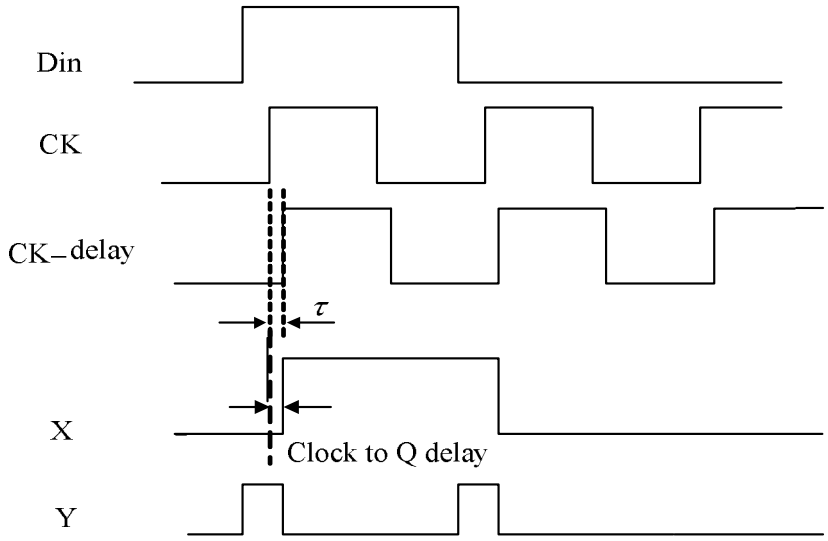


Figure 2.5 Clock-to-Q Delay Effect on the Hogge PD Output

As one remedy, Tom Lee and John Bulzacchellia modified the architecture which is so-called triwave phase detector to remove the static phase error [17],[18].By including two more registers, the “half period skew” limitation of the Hogge PD is solved. Though the triwave detector exhibits a much reduced sensitivity to data transition density, it is more sensitive to duty cycle distortion in the clock signal.

The above discussion does not consider the clock-to-Q delay of the DFFs used, which is sown in the timing diagram of Figure 2.5. And the clock-to-Q delay causes static phase offset when it is used in a CDR/PLL, thus it should be subtracted from the

pulse at Y. A potential solution to this issue is to add a delay cell to compensate for the Clock-to-Q delay in the Hogge PD as shown in Figure 2. 6.

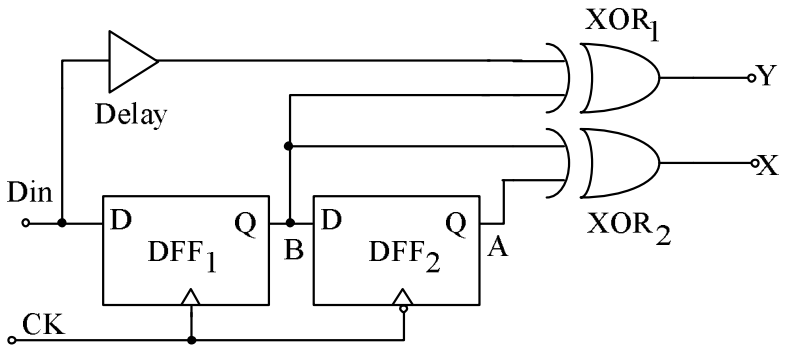


Figure 2.6 Delay Compensation for the Clock-to-Q Delay Effect

II.1.2. Limitations of the Hogge Phase Detector

Although the Hogge phase detector has inherently small jitter generation due to the PD itself compared with the binary PD, it still presents some limitations.

Firstly, the Hogge Phase detector gain is sensitive to incoming data transition density. Assume the incoming data pattern changes from “010101…” to “001100110011….”, the phase detector gain will be reduced by half. Secondly, the Hogge phase detector has inherently small jitter generation due to the PD itself compared with the binary PD such as Alexander PD.

The Hogge PD is limited by the bandwidth requirements; as stated before, it is difficult to design a Hogge PD for 10Gb/s applications. Most important, the mismatch between the DFFs in the circuits will cause static phase offset, and thus affects the jitter performance of the CDR circuit.

Due to the above limitations, Hogge phase detector is usually not adopted in 10Gb/s CDR design.

II.2. Binary Phase Detector

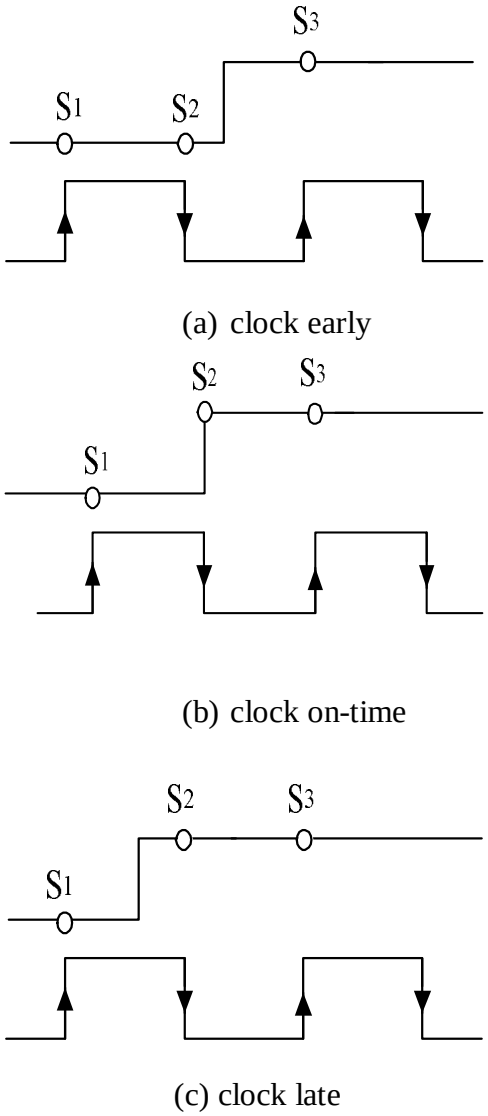
Several state of the art implementations for 10Gb/s and 40Gb/s CDR adopted the binary phase detector architecture due to the difficulty to generate the narrow pulses in currently available CMOS/BiCMOS technologies with a f_t in the range of 60GHz to 120GHz. These techniques are revisited in the following subsections. Among these binary phase detectors, Alexander phase detector is used most frequently.

II.2.1. Alexander Phase Detector

As shown in Figure 2.7, the Alexander PD samples the input data signal at three time instants[5-7],[19-21]. S_1 and S_3 sample two consecutive bits while S_2 samples the data transition, as indicated in Figure 2.7. By comparing whether the transition is close to S_1 or S_3, clock early or late can be determined. If the three samples S_1, S_2, and S_3 are the same, there is no transition during the decision process, thus there is no decision from the PD output. The summary of these operations are tabulated in Table II.1 for

clarity. Notice that, when the samples of S_1,S_2, and S_3 are the same, or have alternate pattern of '0' and '1', the PD output will not change, i.e., no decision will be made.

Figure 2.8 shows an implementation of the Alexander PD[21]. The S_1, S_2, and S_3 samples of input data in Figure 2.7 are generated by using three D-Flip-flops (DFF) and one latch; two Exclusive OR(EXOR) elements are used to generate the early and late signals. As a modified version of the PD, the DFF which generates S_1 can be changed to a latch, while the latch to generate S_2 is removed; the resultant overall function keeps the same as that in Figure 2.8. The ideal characteristic transfer function is shown in Figure 2.9. The control voltage versus the phase difference transfer curve is like a step function, just because the Alexander PD only outputs the sign of the phase difference instead of the magnitude. However, due to the limited speed of the DFFs that are used in the PD, the transfer curve flattens as shown in Figure 2.10 [22]. It can be seen that the PD linear range is 2δ, which is usually less than $\pi/6$ according to [22], thus the linear range is far smaller than that of the Hogge PD shown in Figure 2.7. As will be shown in the next sections, the Alexander PD based CDR is a nonlinear architecture, thus the conventional linear control theory can not be directly used for its analysis, which makes its design more difficult.



(a) clock early

(b) clock on-time

(c) clock late

Figure 2.7 Binary Phase Detector: (a) Clock Is Early, (b) Clock Is On-time and (c) Clock Is Late

TABLE II.1 ALEXANDER PHASE DETECTOR

S_1	S_2	S_3	Operation
0	0	0	No Decision
0	0	1	Clock is fast (early)
0	1	0	No Decision
0	1	1	Clock is slow (Late)
1	0	0	Clock is slow (Late)
1	0	1	No decision
1	1	0	Clock is fast (early)
1	1	1	No Decision

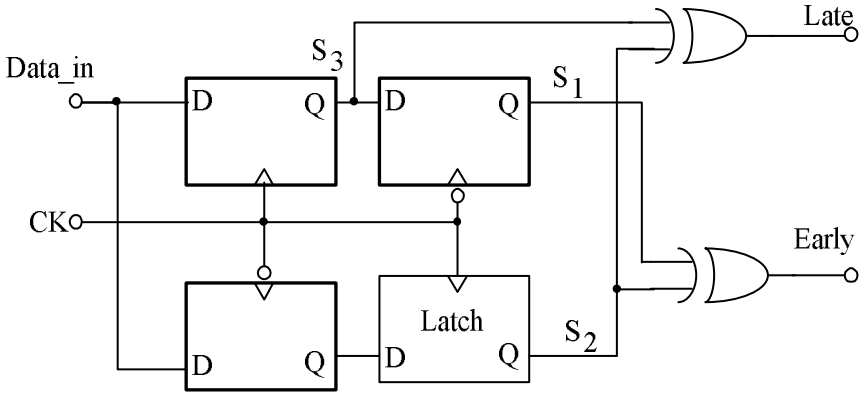


Figure 2.8 Alexander Phase Detector

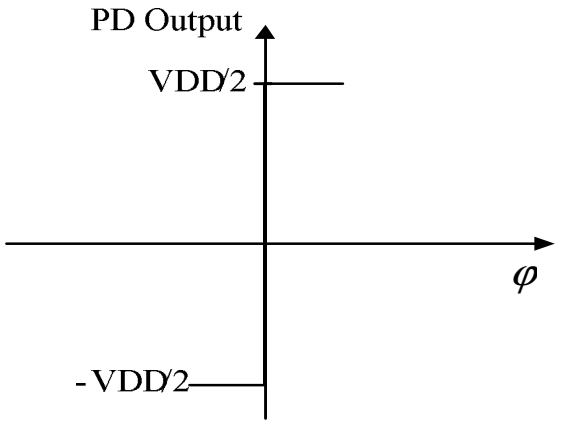


Figure 2.9 Ideal Transfer Function of Alexander PD

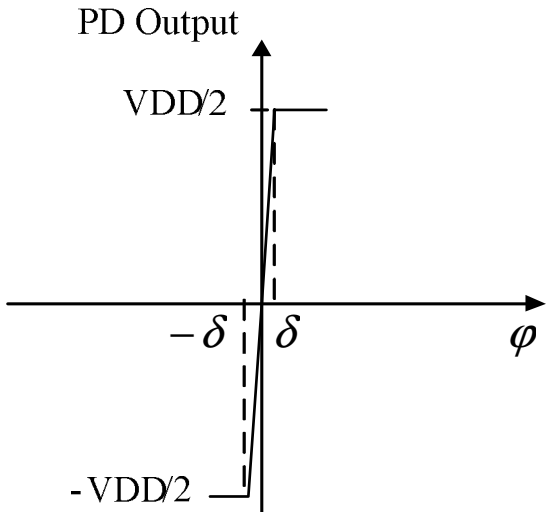


Figure 2.10 Non-ideal Transfer Function of Alexander PD

II.2.2. Limitations of the Alexander PD

Although the Alexander PD can detect whether the clock phase is ahead or later than the optimal sampling instant, it does not indicate the magnitude of the phase error as the linear PD does. In general, the jitter of the Alexander PD CDR is worse than that of linear PD CDR. However, for applications above 10Gb/s or 40Gb/s, the available technology such as 0.18 μm BiCMOS, achieves the unity gain frequency f_t up to 120GHz. The f_t is only 12 times and 4 times larger than the clock frequency of 10Gb/s and 40Gb/s systems. Under such situation, the linear phase detector needs to generate very narrow pulses proportional to the phase difference. On the other hand, the Alexander phase

detector only needs to detect the sign of the phase difference, thus it can achieve higher speed than Hogge PD. Thus Alexander PD can still be a trade-off between the performance and design challenge.

In summary, the Alexander PD is nonlinear in nature and generates higher jitter due to its nonlinear nature. Because it detects the sign of the phase error instead of the magnitude as linear PD does, it presents more jitter generation than a linear PD. The Alexander PD is a binary phase detector, thus the linear analysis can not be used to explain its behavior. However, as the Alexander PD can potentially run at higher speed than Hogge PD does, in this research, a binary phase detector is adopted.

II.3. Phase Frequency Detector

II.3.1. Pottbaker PFD

The Phase frequency detector proposed by A. Pottbacker and U. Langmann [23] is a digital implementation of the Quadricorrelator reported in [15]. The in-phase and quadrature mixers are replaced by the double edge triggered DFFs as shown in Figure 2.11. However, this circuit has limited tuning range. It was reported that at nominal frequency of 8GHz, frequencies errors on the order of 100MHz can be acquired. In this research work, a similar architecture is used for the phase detector.

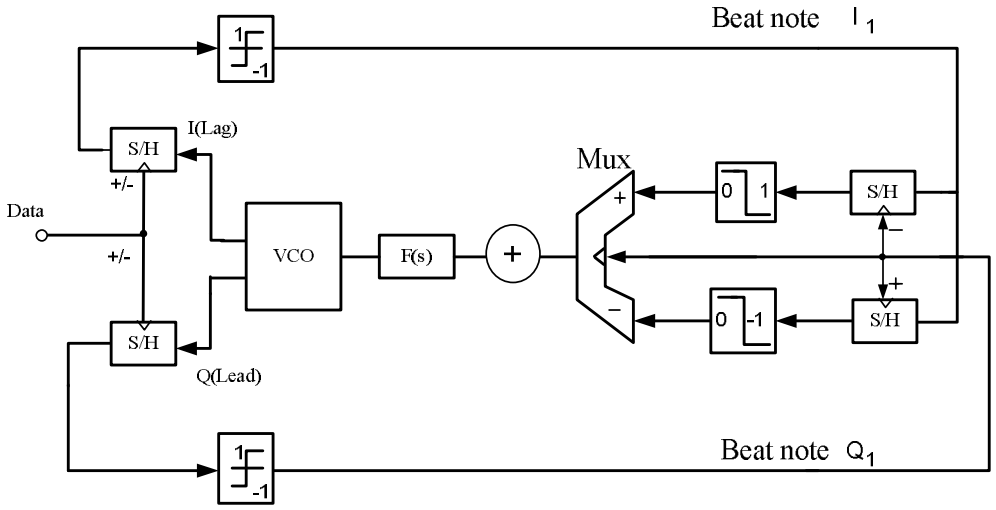


Figure 2.11 Block Diagram for Pottbacker PD Based CDR Implementation

II.3.4. Conclusion

In Linear phase detectors such as Hogge detector, the output pulse width is linearly proportional to the input phase difference, resulting in a constant loop gain during lock transient and minimal charge pump activity after phase lock is achieved. The difficulty is how to generate the pulse widths equal to a fraction of the clock period at speeds near the limit of the technology. While the Bang-bang PDs employ simple flips flops for maximum speed, they provide only two output states, creating significant ripple on the control line even in the locked condition and producing larger jitter at the VCO output. Thus there is a trade-off when selecting the linear or binary PD. In this research work, binary PD is adopted considering the speed requirements and technology available when this research work is performed.

II.4. Charge Pump

II.4.1. Single-ended Charge Pump

Single-ended charge pumps are used extensively since they only need one loop filter and thus consume less power in tri-state operation. In the standard frequency synthesizer, the output current of the charge pump can be as high as several mA [24] to provide better spur performance over the leakage current and to have high SNR at the charge pump for low noise contribution to the PLL. A typical configuration is shown in Figure 2.12 with switches at the drain of the transistors in the current mirror [24],[25].

II.4.1.1. Single-ended Charge Pump with Switches at the Drain of Current Mirrors

Figure 2.12 shows the charge pump with the switch at the drain of the MOS transistors in the current mirror. When the switch DN is turned off, the drain of M_1 is pulled to ground. After the switch DN is turned on, the voltage at the drain of M_1 increases from 0V to the voltage held by the loop filter. For proper operation, M1 has to be in the linear region till the voltage at the drain of M_1 is higher than the minimum saturation voltage, V_{dsat}.

During the transient time the drain current of M_1 and the switch M_{sw} are described by equations (2.1) through (2.3).

$$I_{D,M_{sw}} = u_n C_{ox}\left(\frac{W}{L}\right)_{M_{SW}}\left[\left(V_{DD} - V_{d,M_1} - V_{th,M_{sw}}\right)\left(V_{ctl} - V_{d,M_1}\right) - \frac{1}{2}\left(V_{ctl} - V_{d,M1}\right)^2\right] \quad (2.1)$$

$$I_{D,M1} = u_n C_{ox}\left(\frac{W}{L}\right)_{M1}\left[\left(V_{g,M_1} - V_{th,M_1}\right)\left(V_{d,M_1}\right) - \frac{1}{2}V_{d,M1}^2\right] \quad (2.2)$$

$$\Delta I_D = I_{D,Msw} - I_{D,M1} \quad (2.3)$$

where V_{DD} is the power supply voltage, $Vg_{,M1}$,$V_{d,M1}$ and $Vth_{,M1}$ are gate voltage, drain voltage and threshold voltage of M1; $V_{th,Msw}$ is the threshold voltage of the switch transistor M_{sw}; V_{ctl} is the control voltage at the charge pump output. From (2.1-2.13), even if the *W/L* sizes of M1 and *Msw* are the same, the currents of the two transistors change with the variations of the drain voltage of the M_1 and the threshold changes of *Msw* when the switch is turned on, until the M_1 is in saturation. Thus high peak current(spike) is generated. In other words, if solving the equation $\Delta I_D = 0$, the solution of the root does not necessarily always exist with the variation of $V_{d,M1}$. And the matching of the peak current in NMOS current mirror with that in PMOS mirror is difficult since the amount of the peak current varies with the charge pump output voltage [24]. When the switch at the drain of M_1 is turned off, there is charge injection into the output node of the charge pump, and the generated current spike also affects the performance of the charge pump.

Because of the limitation of generating high peak current when the switches is on from off or vice versa, other charge pump configurations have to be considered. In the following sections, more charge pumps will be discussed.

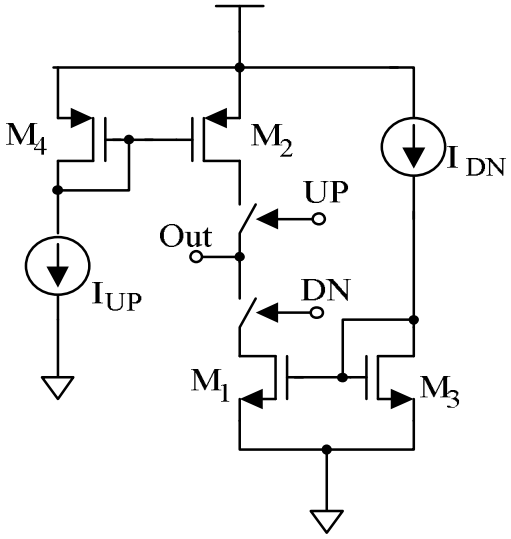


Figure 2.12 Single-ended Charge Pump: Switch at the Drain

II.4.2. Improved Charge Pump

In addition to the typical single-ended configuration discussed previously, some variations of the charge pumps can be adopted to improve the performance.

II.4.2.1. Charge Pump with Active Amplifier

To reduce the high peak current issue in Figure 2.12, one potential solution is by replicating the UP and DN switches with its gate controlled by the inversion signals of UP and DN, i.e., $\overline{UP}$ and $\overline{DN}$,respectively, thus the current source (M_1 or M_2 in Figure 2.12) is always on. The differential charge pump with an active amplifier [26-27] is shown in Figure 2.13(a), where the current sources I_{dn} and I_{up} are equivalent to M_1 and

M_2 in Figure 2.12, respectively. With the unity gain amplifier, the voltage at the drain of $M_1(I_{dn})$ or $M_2(I_{up})$ is set to the voltage at the output node when the switches are off. By doing this way, the voltage difference between the charge pump output and the drain of M_1 (or M_2) is reduced, and less peak current is generated comparing with the single-ended charge pump in Figure 2.12.

II.4.2.2. Charge Pump with Current Steering

The charge pump with the current steering switch is shown in Figure 2.13(b). The performance is similar to the one shown in Figure 2.13(a), but the switching time is reduced by using the current switch [24], where the turn-on time of the switch is smaller than the slewing of an amplifier which has smaller bandwidth to reduce power in Figure 2.13(a). This architecture can be easily converted into differential version as done in [18], [24].

II.4.2.3. Charge Pump with NMOS Switches Only

In Figure 2.13(c), the inherent mismatch of PMOS transistor and NMOS transistor is avoided by using NMOS switches only [19],[24],[28],[29].However, the pole which is caused by the diode connected transistor M_6 limits the speed of the charge pump. If large current is used, the transconductance of the M6 is increased, thus the limitation of M_6 can be greatly alleviated. In order to counteract this effect, a differential implementation

as [11] can be adopted in spite of the area increase of the differential loop filter.

II.4.3. Summary

In this work, the charge pump with active amplifier in Figure 2.13(a) is used for its better performance comparing with that in Figure 2.12.However, even though the peak current issue in Figure 2.12 is solved by using Figure 2.13(a), there is charge sharing issue when the UP or DN switch is turned on from the off state, or vice versa. These charge sharing can be easily reduced by adding dummy transistors operating in the complementary phases of the switches. For 2.13(c), a differential implementation will be further addressed in Section III.

II.5. Voltage Controlled Oscillators

Voltage controlled oscillator (VCO) is one of the most important blocks in high speed CDR design. To meet the jitter or phase noise specification of the CDR, the VCO has to meet the following criteria:

- Good spectral purity or low phase noise
- Reasonable power consumption
- Large tuning range

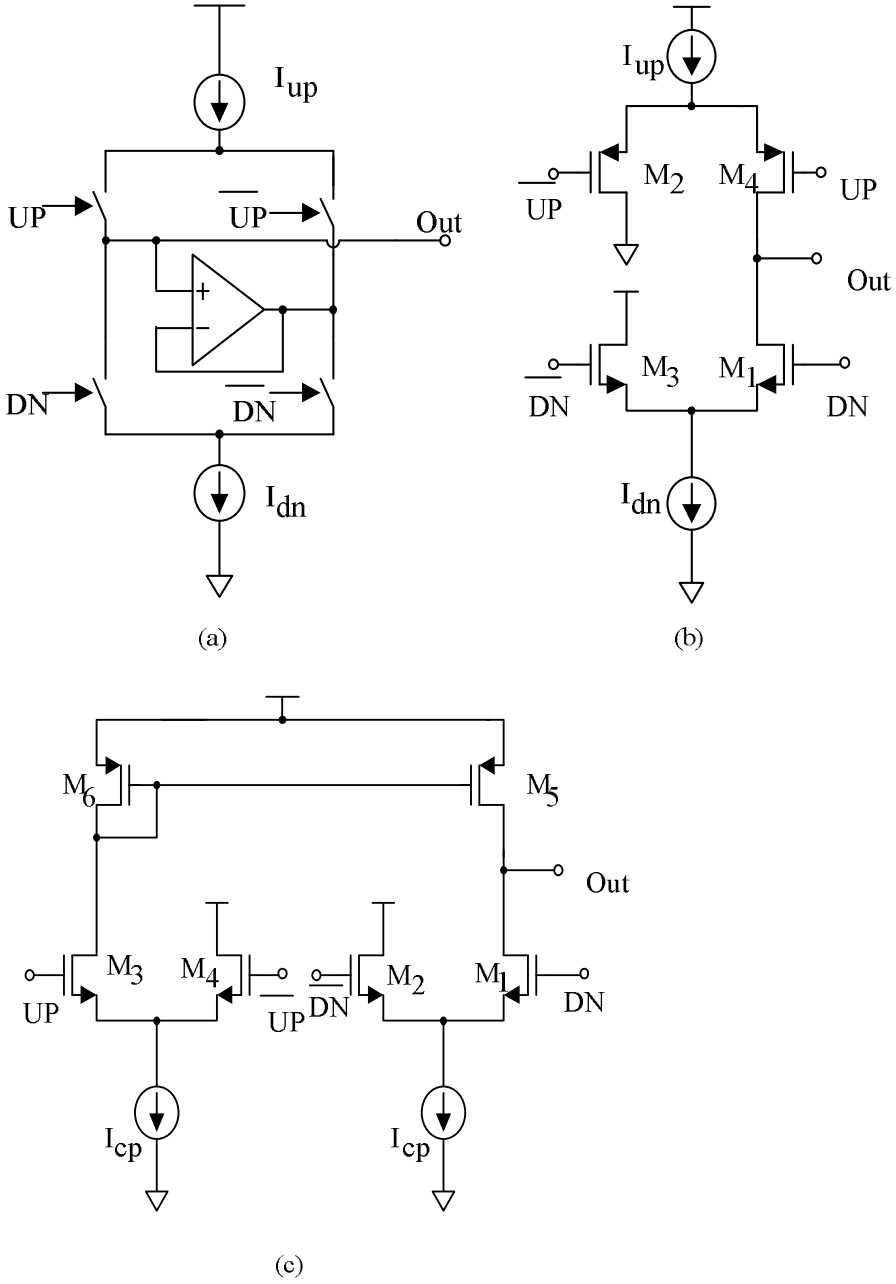


Figure 2.13 Improved Single-ended Charge Pump Architecture: (a) With Active Amplifier, (b) With Current Steering and (c) With NMOS Switches Only

- Relatively small sensitivity (VCO gain)

In recent designs, ring oscillator and LC tank oscillator are the most frequently used architectures in frequency synthesizer and CDR applications. Optical communication applications require using low phase noise VCO. Thus, in this research, only LC tank oscillator is adopted due to its lower phase noise performance compared to ring oscillators [30].

II.5.1. LC Tank VCO

II.5.1.1. Startup Behavior

LC tank VCO is used in wireless transceivers because of its low phase noise performance. According to the topology, the LC tank oscillator can be divided further into single cross-coupled pair and complementary cross-coupled pair topologies [21],[31], which are shown in Figure 2.14(a) and Figure 2.14(b).

In Figure 2.14(a), the cross-coupled differential pair constitutes a small signal negative differential resistance *-2/gm* across the LC tank to compensate for the series loss resistance of the inductors. When the bias current is large enough to start the oscillation, the oscillation amplitude is larger than the voltage required to switch the differential pair, i.e. $\sqrt{2}\left(V_{gs}-V_{th}\right)$, then the cross-coupled pair transistors conduct currents to the LC tank to sustain the oscillation by compensating for the loss of the tank.

Figure 2.15 shows the currents in the cross-coupled differential pair and the VCO output. It can be seen that the currents in the differential pair are close to square

waveform.

As depicted in Figure 2.16, once the VCO starts oscillation, the currents flowing in the cross-coupled MOS transistor pair can be described as two square waves with amplitude of I_{bias} and 0, alternating in a frequency of f_0, which is the VCO oscillation frequency.

For simplicity, a square wave *f(t)* with a frequency of f_0 ,and the amplitude of I_0, the Fouries representation as follows:

$$f[t] = \frac{4I_0}{\pi} \sum_{n=1,3,5...}^{\infty} \frac{1}{n} \sin(n\omega_0 t);\ \omega_0 = 2\pi f_0; \tag{2.4}$$

Thus the VCO amplitude can be written as

$$VCO_{Amplitude} = \frac{2}{\pi} I_{bias} R_p; \tag{2.5}$$

where R_p is the equivalent parallel resistance of the inductor, $R_p = \omega_0^2 L / R_s$, where R_s is the series resistance of the inductor.

In a limited range of increasing the I_{bias} current, the VCO amplitude is also increased, which is denoted as current limited region, however, when the bias current is further increased, the amplitude reaches a single-ended amplitude of VDD, the negative peaks momentarily force the tail current source transistor into triode region, thus the ouput amplitude is limited, which is denoted as voltage limited region [32],[33].

The startup behavior can be analyzed from Figure 2.17. In order to cancel the effect of the equivalent parallel resistor of the inductor, *Rp*, $G_m R_p$ must be greater than 1. G_m is the large signal transconductance if the tail current transistor works in saturation region,

computed as:

$$G_m = \mu_n C_{ox} \frac{W}{L}(V_{Gs} - V_{th}) \tag{2.6}$$

From Figure 2.17(a), assume the oscillator is operating in its steady state, thus the CKO+ and CKO- output equal amplitude with 180 degree phase difference. Then it can be simplified as Figure 2.17(b) using half circuit. Using one port view of the LC tank VCO, the impedance of the *RLC* tank together with negative G_m contributes to the VCO oscillation, which is shown in Figure 2.17(c). The impedance of the whole LC tank VCO is computed as in the equation (2.7).

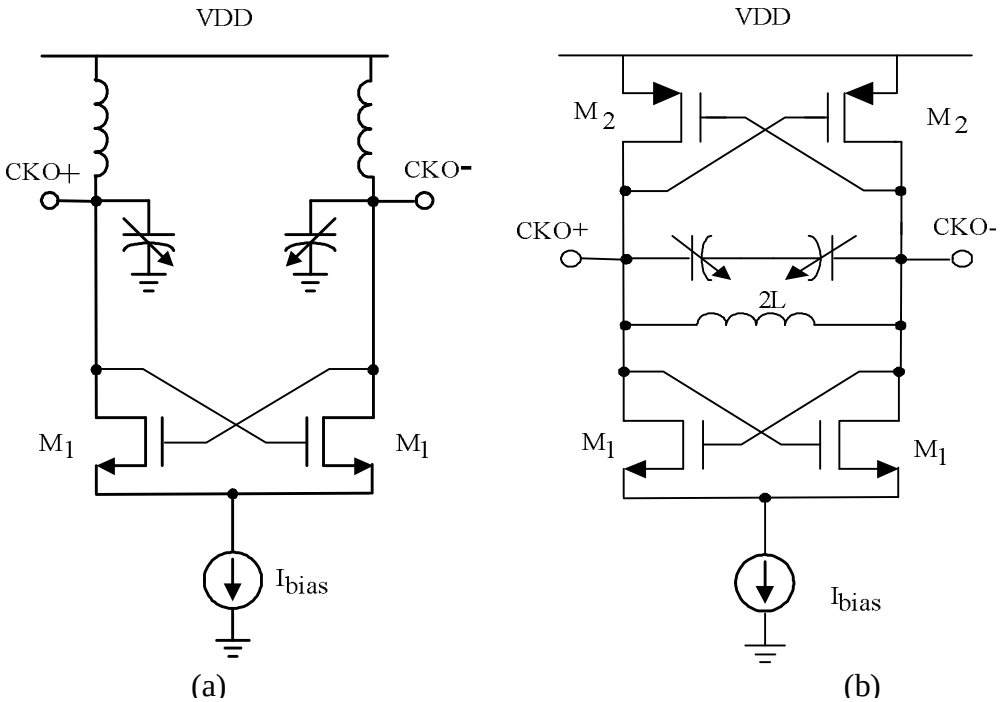


Figure 2.14 LC Tank VCO: (a) Standard LC Tank VCO, and (b) Complementary LC Tank VCO

$$Z(s)=\frac{1}{sC+(G_p-G_m)+(sL)^{-1}}=\frac{sL}{s^2LC+s(G_p-G_m)L+1} \tag{2.7}$$

If $G_p<G_m$, then we have two poles at the right plane of the Laplace S plane. Once perturbed by the power supply or other means, the VCO oscillates and continues to build up. Once the amplitude is large enough, the oscillator operates in a nonlinear mechanism. If $G_p=G_m$, which means $G_mR_p=1$, then the two poles lie on the imaginary axes of the S-plane, such that a stable oscillation is sustained. In real applications, $G_mR_p>2$ is designed to help startup the oscillation stably [21].

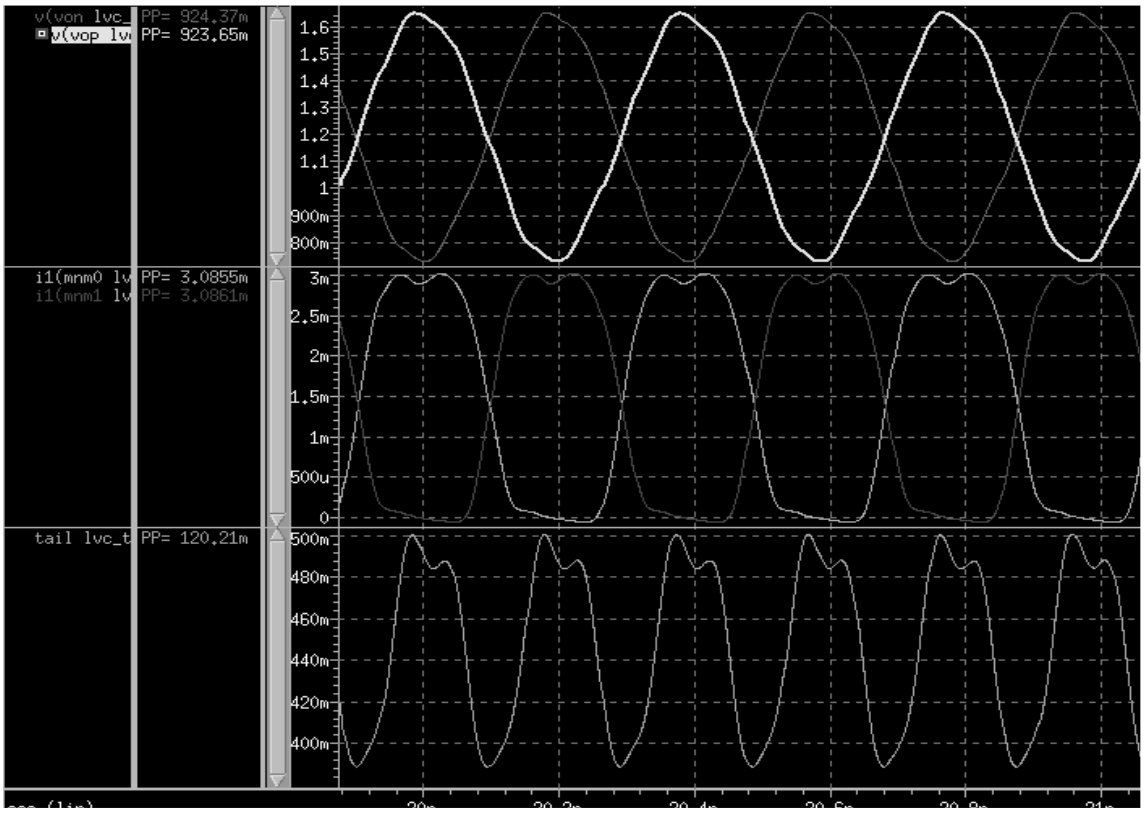


Figure 2.15 Transient Simulation of a Typical LC Tank VCO. Note: From the Top to the Bottom, the Signals Are: VCO Differential Outputs, Currents in the Cross Coupled Transistors and Tail Voltage

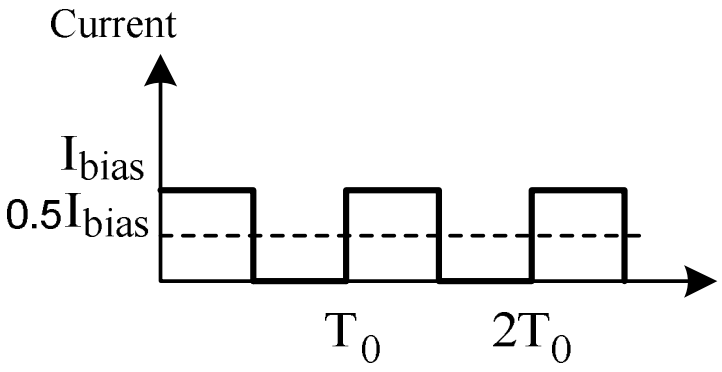


Figure 2.16 Current Flowing in One Transistor of the Cross-coupled Pair

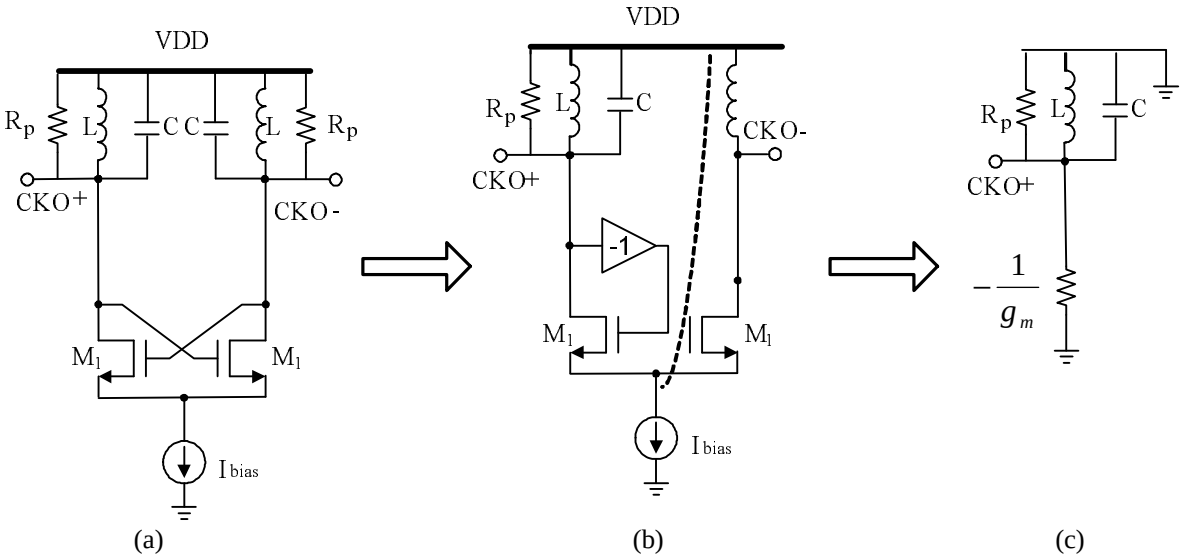


Figure 2.17 Derivation for LC Tank VCO Startup Requirements

II.5.1.2. Phase Noise Consideration

The oscillator output with small random excess phase can be represented as [28]:

$$x(t) = A\cos[\omega_0 t + \phi_n(t)]$$

where $\phi_n(t)$ is the excess phase.

By manipulating trigonometric operation, and notice that the excess phase is very small, by approximating $\cos(\phi_n(t)) \approx 1$, $\sin(\phi_n(t)) \approx \phi_n(t)$, the *x(t)* can be expanded as follows:

$$\begin{aligned} x(t) &= A[\cos(\omega_0 t)\cos(\phi_n(t)) - \sin(\omega_0 t)\sin(\phi_n(t))] \\ &= A[\cos(\omega_0 t) - \sin(\omega_0 t)\phi_n(t)] \end{aligned} \tag{2.8}$$

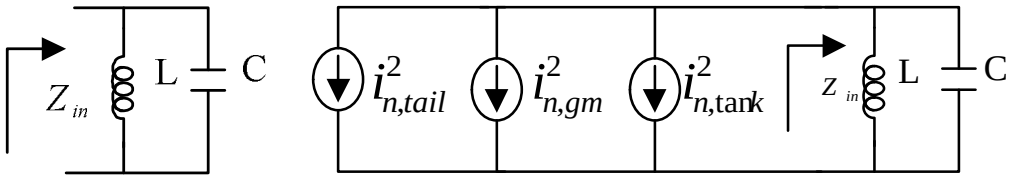
Represented in frequency domain, we have:

$$\begin{aligned} X(\omega) &= A\pi\{[\delta(\omega-\omega_0)+\delta(\omega-\omega_0)] - [\delta(\omega-\omega_0)+\delta(\omega-\omega_0)] \otimes \phi_n(\omega)\} \\ &= A\pi\{[\delta(\omega-\omega_0)+\delta(\omega-\omega_0)] - [\phi_n(\omega-\omega_0)+\phi_n(\omega+\omega_0)]\} \end{aligned} \tag{2.9}$$

which means that the excess phase is translated into frequency components centered around ω_0.

In general, denote carrier frequency as f_0, the spectral purity of an oscillator is generally measured by using phase noise which is defined as:

$$\ell(f) = \frac{noise\ \ power\ \ within\ 1\ Hz\ at\ an\ offset\ \ f\ \ with\ respect\ to\ \ f_0}{carrier\ \ power} \tag{2.10}$$



(a) LC tank diagram (b) Noise representation of LC tank

Figure 2.18 LC Tank and Its Noise Sources Which Contribute to Phase Noise

Now from the definition of phase noise, the analysis of LC VCO will be performed in the following paragraphs.

From Figure 2.18(a), the input impedance at $\omega_0+\Delta\omega$, ω_0 is the resonant frequency with the value of $1/\sqrt{LC}$ .In Figure 2.18(b), the noise sources in the LC tank VCO include, $i_{n,tail}^2$,which is attributed to the tail current source; $i_{n,gm}^2$, which is due to the differential pair, and $i_{n,\tan k}^2$ is attributed to the resistive element in the inductor.

$$\begin{aligned} Z(\omega)\big|_{\omega=\omega_0+\Delta\omega} &= \left(\frac{1}{j\omega C} \parallel j\omega L\right)\Bigg|_{\omega=\omega_0+\Delta\omega} \\ &= \frac{j(\omega_0+\Delta\omega)L}{1-(\omega_0+\Delta\omega)^2 LC} \\ &= \frac{j(\omega_0+\Delta\omega)L}{1-\omega_0^2 LC-2\omega_0\Delta\omega LC-\Delta\omega^2 LC} \end{aligned} \tag{2.11}$$

At low frequency offset,

$$\begin{aligned} Z(\omega_0+\Delta\omega) &\cong \frac{j(\omega_0+\Delta\omega)L}{-2\omega_0\Delta\omega LC} \\ &= -\frac{j}{2\omega_0 C}\frac{\omega_0}{\Delta\omega} = -\frac{j\omega_0}{2Q\Delta\omega} \end{aligned} \tag{2.12}$$

where *Q* is the quality factor of the LC tank, which is defined as in [18]. For a parallel *RLC* tank,

$$Q = \frac{R}{\left|Z_{L,C}\right|} = \frac{R}{\omega_0 L} = \omega_0 RC \tag{2.13}$$

The thermally induced phase noise density [18] due to resonator loss (mainly the equivalent parallel resistance Rp of the inductor L in Figure 2.18(a) is:

$$\begin{aligned} \ell(\Delta\omega) &= \frac{4KTR_p Z(\omega_0 + \Delta\omega)}{A^2/2} \\ &= \frac{8KTR_p}{A^2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \end{aligned} \tag{2.14}$$

where *A* and *Q* are the VCO output amplitude and quality factor, respectively. It can be easily concluded to increase the inductor quality of factor, and to increase the VCO amplitude, as well as reduce Rp can improve the phase noise performance.

The switching of the differential pair(cross-coupled negative Gm pair) samples the noise in the tail currents as a single-balanced mixer [34]. The noise is frequency modulated into the LC tank, mainly at the zero crossing point of the VCO output. Noise originating in the tail current at a frequency of $2\omega_0 \pm \Delta\omega$ is down-converted to $\omega_0 \pm \Delta\omega$.Notice that the conversion gain of a mixer is typically $2/\pi$, the noise at the VCO output due to the tail current source thus is:

$$V_{n,tail}^2 = n \times \frac{4KT}{g_{m,tail}}\left(\frac{2}{\pi} G_{m,diff} Z(\omega)\right)^2 \tag{2.15}$$

where n represents accumulated noise after aliasing, consider the cross-coupled pair as mixers, then $n = 2\left(1 + 1/3^2 + 1/5^2 + ...\right) = \pi^2/4$; where the first term is the thermal noise

mixed by the fundamental tone at ω_0; the second term is the noise around $3\omega_0$, which is downconverted by the third harmonic of the VCO, and the conversion gain is reduced to 1/3 of the main harmonic, etc.

The phase noise caused by the thermal noise at $2\omega_0$ is reported in [32], rewrite here:

$$\ell(\Delta\omega) = \frac{\pi^2}{4}\frac{4KT\gamma}{g_{m,tail}} \times \frac{4}{\pi^2}\frac{G_{m,diff}^2 R_p^2}{A^2/2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \tag{2.16}$$

where $g_{m,tail}$ is the transconductance of each transistor in the cross coupled differential pair, and γ is the noise factor in a single FET, normally it is 2/3 in long channel CMOS technology, and larger than 1 in short channel transistors. If the Vdsat of the differential pair and the tail current source are designed similar, using the fact of $G_m = \frac{2I_D}{V_{gs}-V_T} = \frac{2I_D}{V_{dsat}}$, and notice the current in the differential pair is half the tail current at the zero-corssing point of the VCO output, (2.15) can be simplified to

$$\ell(\Delta\omega) = 4KT\gamma\frac{G_{m,diff}R_p^2}{2A^2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 = \frac{4KT\gamma R_p^2}{A^2}\frac{I_{tail}}{V_{dsat}}\left(\frac{\omega_0}{2Q\Delta\omega}\right) \tag{2.17}$$

For the cross-coupled differential pair, the switching of the differential pair requires the amplitude of the VCO is larger than $\sqrt{2}(V_{gs}-V_t)$, which is the voltage required to switch the differential pair. The differential pair sustains the oscillation by injecting an energy-replenishing square wave into the LC resonator [33]. As depicted in [32] and redrawn in Figure 2.19, the noise in the differential pair is actually not sampled by impulses, but by time window of finite width. The window height is proportional to

transconductance, and the width is set by the tail current, and the slope of the oscillation waveform at zero crossing. The input referred noise spectral density of the differential pair is inversely proportional to transconductance. Thus the narrower the sampling window, the lower the noise spectral density. Using the fact that the transconductance of the differential pair is $G_m = 2I/\Delta V$, as shown in Figure 2.19. For sinusoidal signal with amplitude of A, the slew rate SR is $SR = 2A\omega_0$.Denote the pulse in Figure 2.19(c) as *p(t)*. The noise current of the cross-coupled differential pair is given in [34]:

$$i_{n,diff}^2 = \frac{2}{T_0}\int_0^T p^2(t)dt \cdot V_n^2 = \frac{2}{T_0}\left(\frac{2I_{tail}}{SR}\right)^2 \frac{1}{T_w}V_n^2 = \frac{I_{tail}4KT\gamma}{SR \cdot T_0} = 4kT\gamma\frac{I_{tail}}{\pi A} \qquad (2.18)$$

where T_0 is the period of the sinusoidal VCO output, and A is the amplitude.

The phase nose due to the differential pair (with a factor of 2 due to the two transistors in the pair) is [32]:

$$\ell(\Delta\omega) = \frac{2I_{tail}R_p}{\pi A}\frac{4KT\gamma R_p}{A^2/2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \qquad (2.19)$$

Connecting to the famous Leeson's model, which describes the phase noise using the following formula [18], [23]:

$$\begin{aligned}\ell(\Delta\omega) &= 10 \cdot \log\left[\frac{2FKT}{P_{sig}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]; \\ &= 10 \cdot \log\left[\frac{4FKTR_p}{A^2}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right]\end{aligned} \qquad (2.20)$$

where F is an unspecified noise factor; K is Boltzmann's constant which is $8.62\times10^{-5}eV$, and T is the temperature, P_{sig} is the power of the carrier at the fundamental frequency of ω_0, and Q is the quality factor of the LC tank, while the $\Delta\omega$ is

the offset frequency from the carrier frequency ω_0.The phase noise denotes the “decibels below the carrier per Hz or dBc/Hz”. Due to the facto of equal split the noise into AM and PM noise, from [34], the noise factor due to the thermal noise can be represented as:

$$F = 1 + \frac{2\gamma R_p I_{tail}}{\pi A} + \gamma \frac{1}{2} \frac{I_{tail}}{V_{dsat}} R_p \tag{2.21}$$

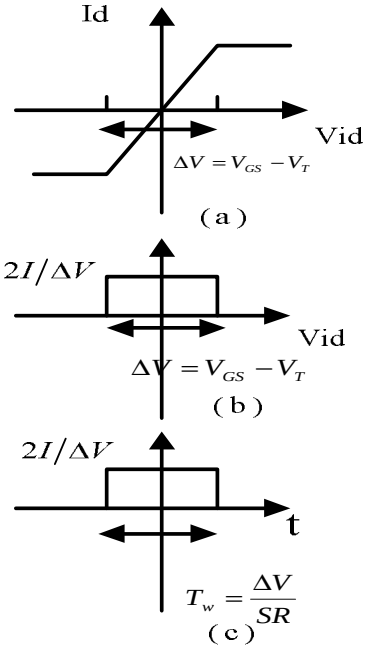


Figure 2.19 Properties of Cross-coupled Pair: (a) Switching Pair I-V Curve, (b) The Transconductance of the Switching Pair in Voltage Domain, and (c) Transconductance in Time Domain [34]

As described in [16], when the LC tank oscillator works in a current limited region, which means that increasing tail current, the oscillation amplitude also increases, thus

second term in (2.27) is constant, namely 2γ. However, when the tail current is increased beyond some point, the oscillation amplitude is limited by the supply, which is called "voltage limited mode". Thus increasing further the tail current will worsen the phase noise because the differential pair caused phase noise takes more effect.

Assume the VCO works in current limited region, thus the noise factor can be written as:

$$F = 1 + \frac{2\gamma}{\pi} + \gamma \frac{1}{2} \frac{I_{tail}}{V_{dsat}} R_p \tag{2.22}$$

For a LC tank oscillator in Figure 2.14(a), with a initial guess of inductor L=1.1nH, and quality of factor Q=7, and the resonant frequency is 5GHz, the equivalent parallel resistance Rp is

$$R_p = Q\omega_0 L = 7 \times 2\pi \times 5 \times 10^9 \times 1.1 \times 10^{-9} = 242 \tag{2.23}$$

The minimum tail current is

$$I_{tail} \geq \frac{0.6}{\frac{4}{\pi} R_p} = 2mA \tag{2.24}$$

As calculated in the Section III, the phase noise of the LC tank VCO should be less than -100dBc at 1MHz offset to meet the jitter requirements in optical communications.

$$\ell(\Delta\omega) = 10 \cdot \log\left[\frac{4FKTR_p}{A^2} \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right] \quad < \quad -100 \tag{2.25}$$

where $V_{dsat} > 63mV$ if $I_{tail} > 4mA$.

Then long channel length transistor with reasonable width tail current source should be used. Further phase noise simulation needs to be done to ensure the VCO meets the

noise requirements.

For completeness, there is also -30dB/decade region which is possibly attributed to the flicker noise(*1/f* noise), and Leeson gave out the modified version of phase noise equations, which is defined as [16], [23].

$$\ell(\Delta\omega) = 10 \cdot \log\left\{ \frac{2KT}{P_{sig}} \left[1 + \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right] \left(1 + \frac{\Delta\omega_{1/f^3}}{|\Delta\omega|} \right) \right\} \tag{2.26}$$

A typical LC tank oscillator working at 3.3GHz is shown in Figure 2.20. The phase noise finally flattens out for large frequency offsets, rather than continuing to drop at -20dB/decade as predicted in (2.19). That is due to the noise floor associated with any active elements (buffers) placed between the test fixture and test equipment, and the noise flloor limited by the measurement instrument itself.

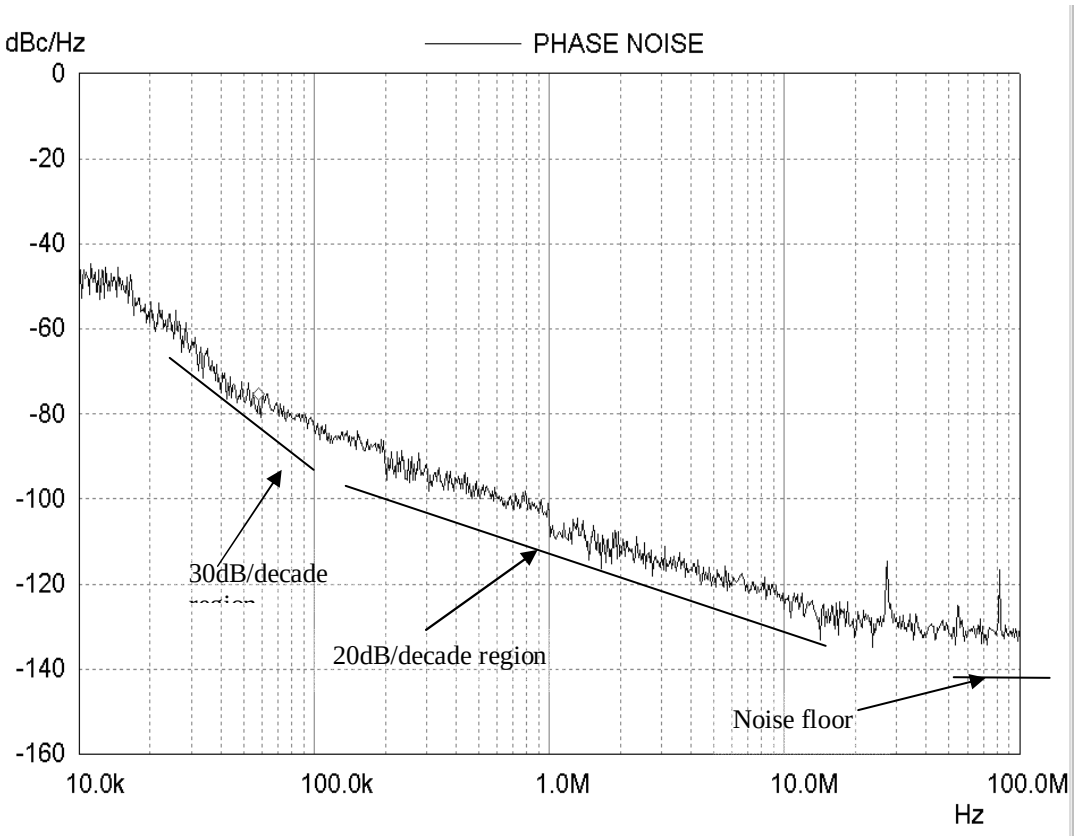


Figure 2.20 Phase Noise Measurement of a 3.3GHz LC Tank VCO

II.5.1.3. Tuning Range

For a LC tank VCO in Figure 2.14(a), the total capacitance is composed of fixed capacitance, C_{fix}, and varacotr, *Cvar*. Thus the minimum frequency is

$$f_{\min} = \frac{1}{2\pi\sqrt{L\left(C_{fix} + C_{\text{var},\max}\right)}} \tag{2.27}$$

$$f_{\max} = \frac{1}{2\pi\sqrt{L\left(C_{fix} + C_{\text{var},m\min}\right)}} \tag{2.28}$$

The frequency tuning range is calculated as $(f_{max}-f_{min})/((f_{max}+f_{min})*0.5)$.

For the varactor used in this research work, the $C_{var,max}/C_{var,min}=1.8$, the percentage of the frequency tuning is shown in Figure 2.21. The maximum tuning range is 21% when the fixed capacitance is 20% of the total capacitor tank; and 7% when the fixed capacitance takes 70% of the overall capacitance. So it is necessary to reduce the fixed capacitance over the varactor bank in order to achieve higher tuning range.

II.5.1.4. Summary

The LC tank VCO includes integrated inductor and varactor, thus it occupies larger area than a LC-less ring oscillator. However, due to the higher *Q* of the LC tank, the phase noise of a LC VCO(<-100dBc at 1MHz offset) is less than that of a ring oscillator, which presents a phase noise of <-90dBc at 1MHz offset.

The LC tank VCO has limited tuning range due to the relatively low ratio of the maximum and minimum capacitance that the varactor can achieve. Thus multiple banks of Capacitors have to be used to increase the tuning range.

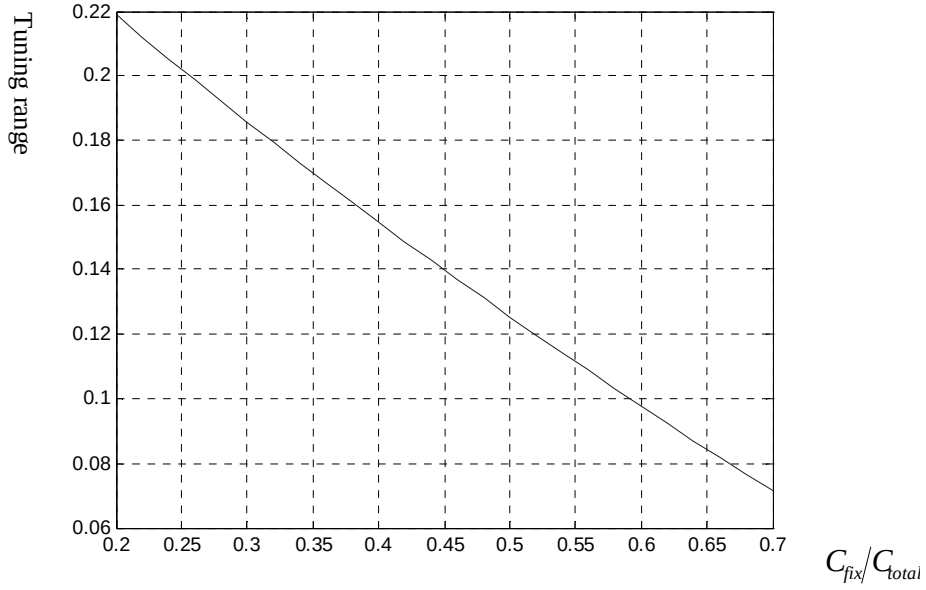


Figure 2.21 Tuning Range of a LC Tank VCO with L=1.25nH, C_{total}=1pF

II.5.2. Quadrature LC VCO

Quadrature VCOs, which generate I/Q phase clocks, are widely used in the RF front- end transceivers. Also, it finds extensive usage in SerDes(Serializer and De-serializer) devices which require half rate phase detection, phase interpolation and frequency detection. The methods for generating quadrature phase clocks include the following three ways:Divide-by-2 circuit, poly phase filter, and Quadrature phase VCO(QVCO). QVCO is not always the best solution for wireless applications, for example, a direct conversion receiver often uses divide-by-2 to avoid pulling problems. QVCO requires more on-chip inductors and often result in larger die

area.Moreover,QVCO is more prone to substrate coupling with more on-chip inductors. Nevertheless, QVCO is widely used in SerDes and CDR designs. The main reason is that, it is quite challenging to design full rate architecture if the design works at 10GHz or above under current popular CMOS technology; the half rate architecture which uses I/Q clocks leverage the device speed requirements.

A typical QVCO schematic is shown in Figure 2.22. Besides the LC tanks, the transistors M_1 and M_2 constitute the negative G_m and the coupling transconductance G_{mc}, respectively. With an equivalent circuit diagram in Figure 2.23, the coupling mechanism can be easily explained. The two LC tanks are coupled using G_{mcI} and G_{mcQ}, which is very similar to a two stages ring oscillator.

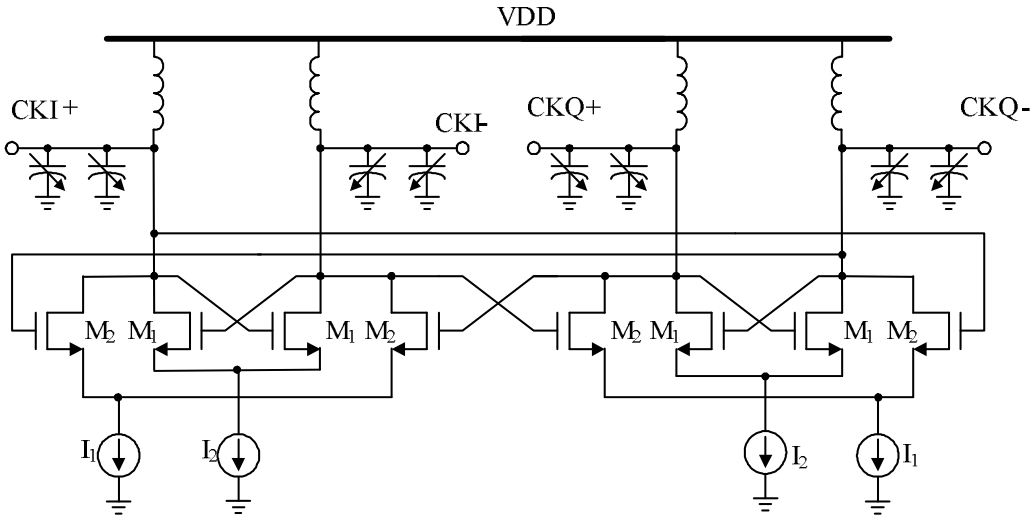


Figure 2.22 Quadrature LC Tank VCO [35]

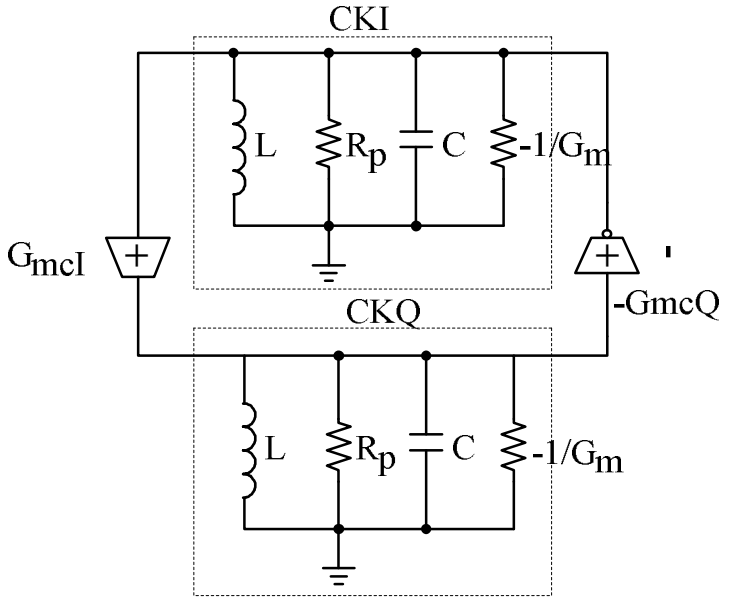


Figure 2.23 Diagram of Coupled Quadrature LC Tank VCO

Denote the coupling transconductance in Figure 2.23 as G_{mc}, $Z(j\omega)$ is the impedance of the RLC tank, we have:

$$CKI(j\omega) = -G_{mcQ} * Z(j\omega) * CKQ(j\omega) \tag{2.29}$$

$$CKQ(j\omega) = -G_{mcQ} * Z(j\omega) * CKI(j\omega) \tag{2.30}$$

Note that in Figure 2.23, G_{mcQ} has a inversion sign comparing with G_{mcI}. It can be concluded that $CKI^2(j\omega) + CKQ^2(j\omega) = 0$, which is equivalent to $CKI = \pm jCKQ$. Then CKI and CKQ have phase difference of $\pm 90^\circ$, however, the phase lead or lag relationship between them are ambiguous[35],[36], which means that two oscillation frequencies are possible if reflecting the phase relationship into the frequency response as will be discussed next.

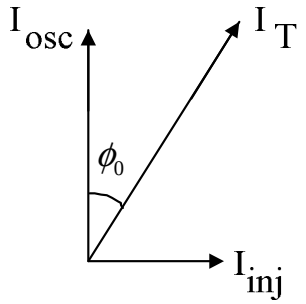


Figure 2.24 Explanation of QVCO Using Injection Lock Phenomenon

Basically, the coupled QVCO operates away from the resonant frequency and hence achieves worse phase noise than a stand-alone LC tank VCO, also it presents two stable modes of oscillation with different frequencies. By explanation using injection locking [21], as demonstrated in Figure 2.24, the injection locking shifts the frequency from resonance so that each tank produces a phase shift of [21]

$$\phi_0 = \tan^{-1}\left(\frac{I_{inj}}{I_{osc}}\right) \tag{2.31}$$

where I_{inj}/I_{osc} is also called coupling factor, and I_{inj} denotes the current injected by one oscillator into the other and *Iosc* is the current produced b the core of each oscillator. The required frequency shift is shown in Figure 2.25.

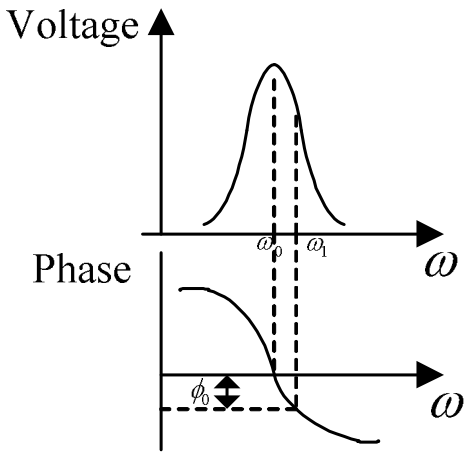
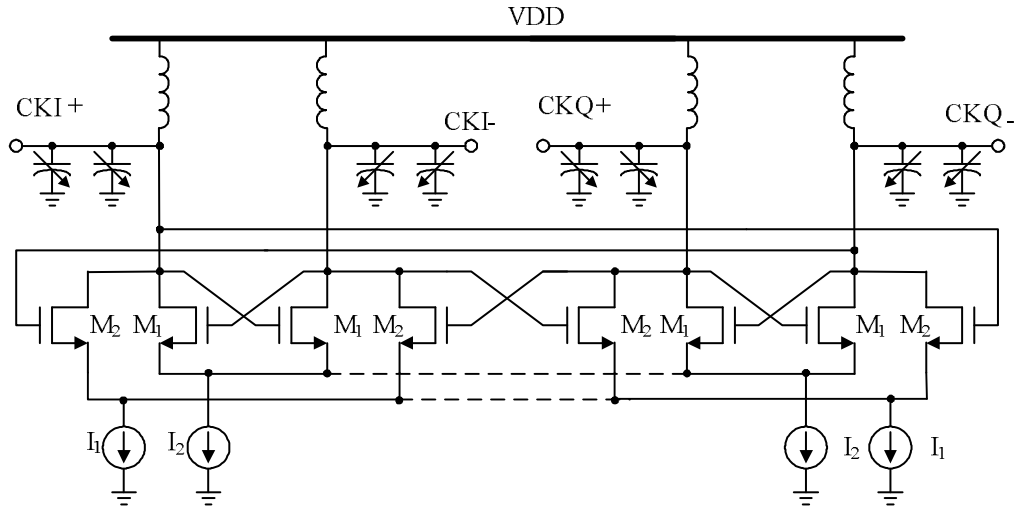


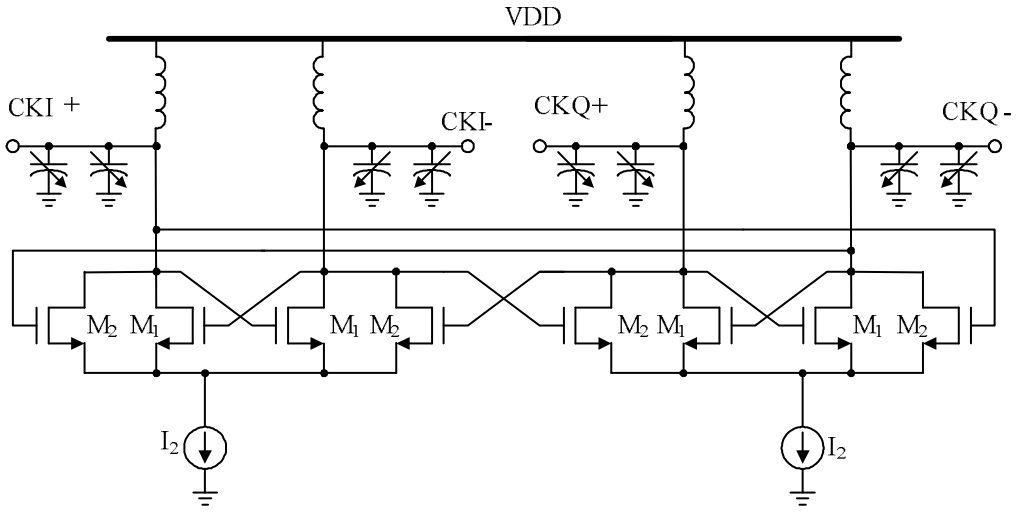
Figure 2.25 Frequency Shift due to Additional Phase Shift in Coupled QVCO

As a variant of the architecture in Figure 2.22, the QVCO in Figure 2.26 share the tail current sources for the coupling branch and oscillation LC tank respectively, i.e., the tail nodes of the two LC tanks are shorted together, while the tail nodes of the coupling pairs are shorted together [37]. The theory behind this is that, when one LC tank needs less current, say the tank with output of CKI, then the bias current can supply to the tank whose output is CKQ to sustain enough oscillation [33],[37]. In this research work, the configuration in Figure 2.27 is used to share the coupling transistors bias current with the LC tank, so as to supply extra current when the coupling transistors need larger bias currents [38].



(Tail nodes of each tank are shorted in dashed line together, coupling transistors tail node are shorted in dashed lines too)

Figure 2.26 Quadrature VCO Diagram Coupled through Tail Currents



(tail nodes of each LC tank and coupling pair are shorted together)

Figure 2.27 Modified Quadrature VCO Diagram Sharing Tail Currents

In summary, Quadrature VCO inherently generates quadrature clock phases, and with comparable phase noise performance as LC tank VCO, with more power consumption. However, the circuits connected to the quadrature VCO can be designed in half rate, which reduces the design complexity as well.

II.6. Experimental Results of a Prototype IC

With the system level function which is described in Appendix A, A linear phase detector based CDR prototype IC is designed in TSMC 0.35μm CMOS technology. The CDR Chip microphotograph is shown in Figure 2.28, which occupies an area of less than 2.5x2.5mm^2. The CDR mainly uses a Hogge Phase detector shown in Figure 2.2, a LC tank VCO as that in Figure 2.14(a), a charge pump as in Figure 2.13(a) and off-chip RC loop filter, which is the same as that in Figure 2.1.

The output spectrum of the clock is shown in Figure 2.29. The phase noise of the clock output is shown in Figure 2.30, when the CDR is locked to the 200MHz reference clock; at 1MHz offset, the phase noise is -107dBc/Hz. Figure 2.31 shows that the clock spectrum purity, with a 35MHz sinusoidal jitter modulation at the data input, the clock output has an 27.8dB attenuation of the harmonic tone at 35MHz offset to the fundamental tone.

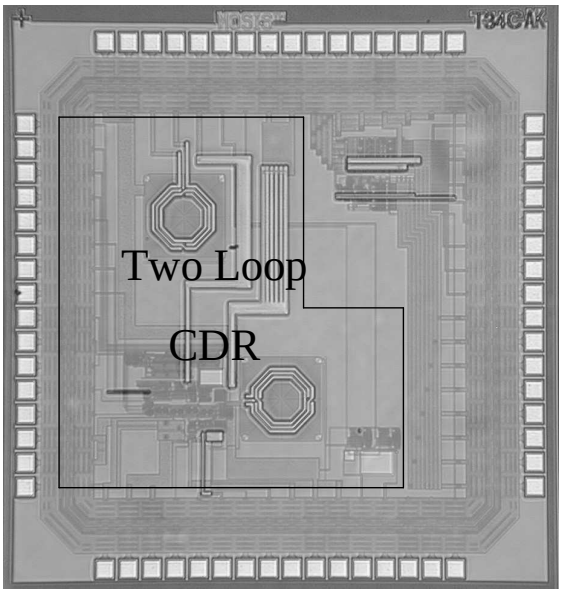


Figure 2.28 Prototype IC Micrograph in 0.35μm CMOS

However, when the input goes to 10Gb/s, the expected clock output phase noise will be -107dBc+9.5dB =-97.5dBc, which is marginal in implementing a 10Gb/s CDR. Also,the speed requirements of other blocks such as phase detector and frequency divider, necessitate a faster technology such as 0.18um CMOS to be used. In the next section, an implementation of 10Gb/s CDR will be addressed in more detail.

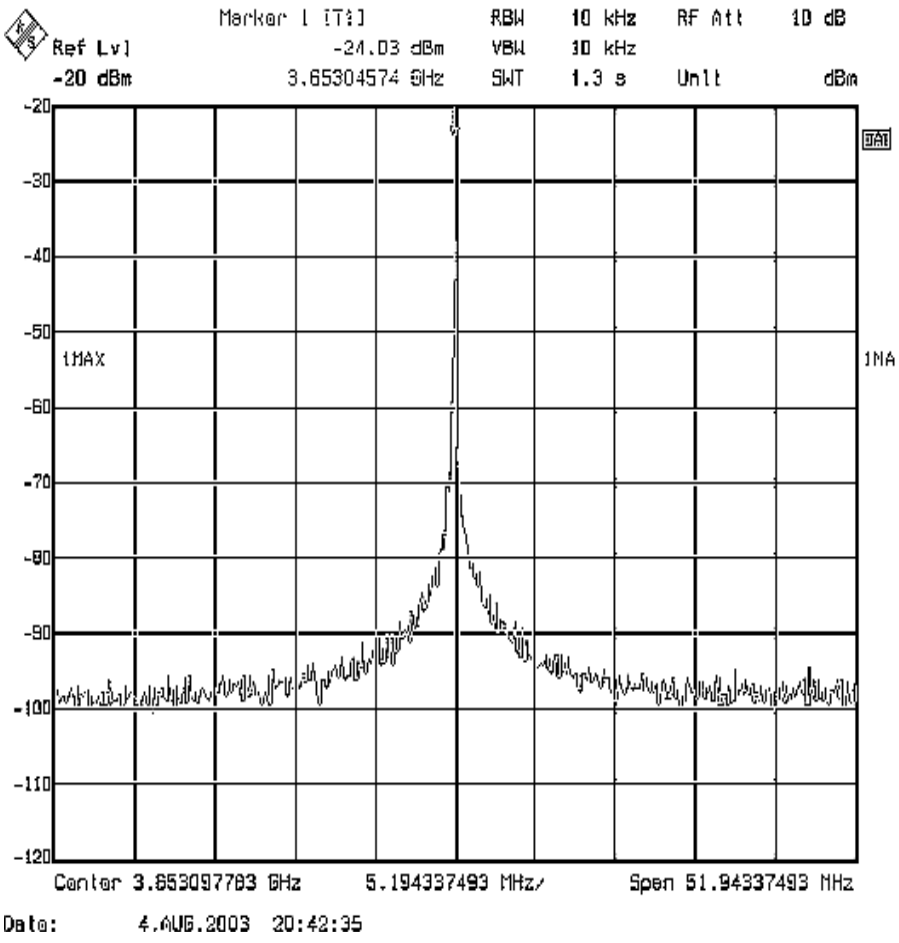


Figure 2.29 Measured Clock Spectrum of the Prototype IC

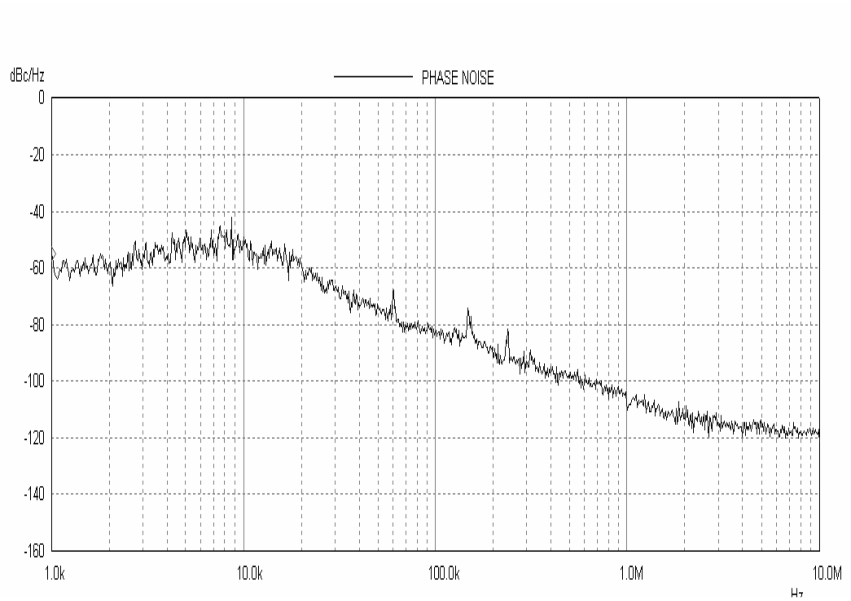


Figure 2.30 Measured Phase Noise of the Clock Output of the CDR IC

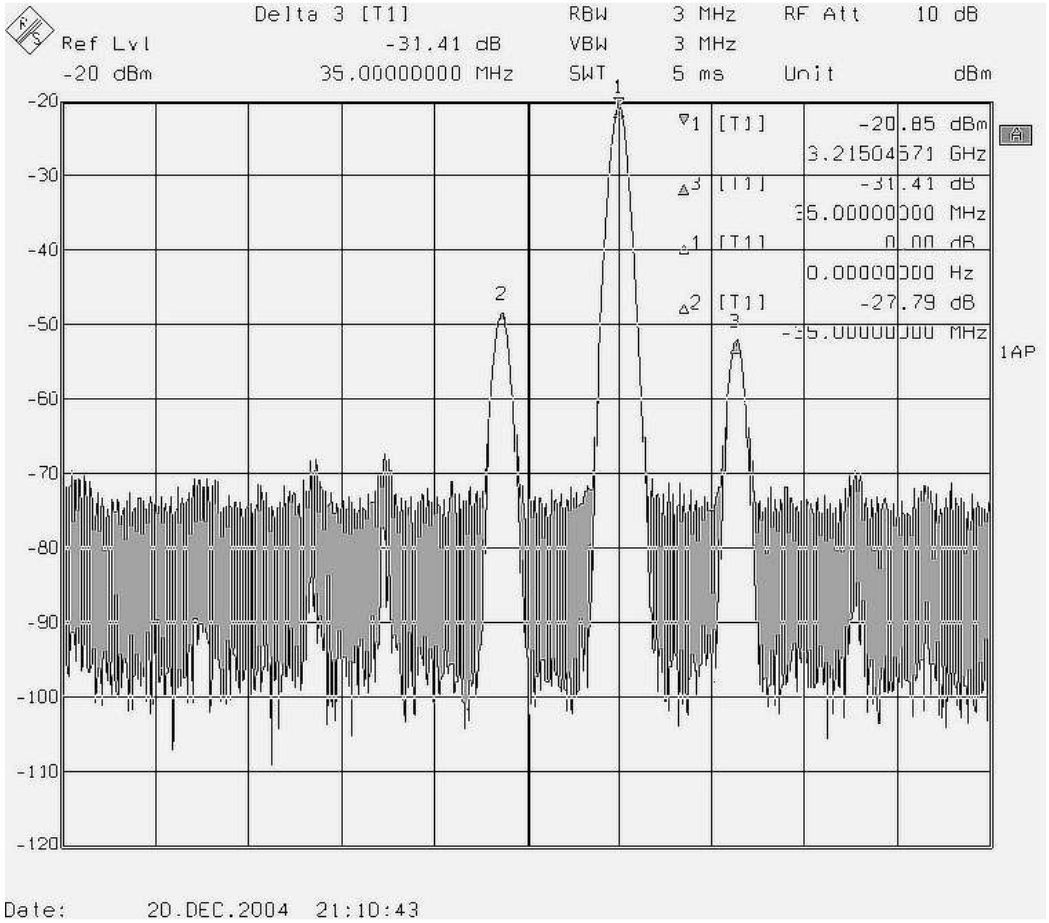


Figure 2.31 Clock Spectrum Purity When 35MHz Sinusoidal Jitter Is Added

III. A FULL ON-CHIP CMOS CLOCK DATA RECOVERY IC FOR OC-192 APPLICATIONS

III.1. Introduction

Demand for low cost transceiver IC has increased due to the convergence of Datacom and Telecom network applications [5]. A typical transceiver design includes both a transmitter and a receiver as shown in Figure 3.1. The transmitter (TX) includes a PLL and multiplexer (MUX), which serializes the 16 bits parallel data if SFI4 interface is used in the typical OC-192 applications. The synchronization clock is provided by a narrow bandwidth PLL. After serialization(or MUX), the data is sent to the photodiode through a laser driver(LD) as the interface of the single-mode Fiber or multi-mode Fiber for long distance data transmission. At the receiver side, the transimpedance amplifier (TIA) detects the photodiode current and converts it to voltage, and then the limiting amplifier (LA) amplifies and limits the voltage signal to a fixed level in order to increase the sensitivity of the clock data recovery (CDR) block. Finally, the recovered data is de-serialized into parallel data outputs for further framing or overhead processing[1].

Several 10 Gb/s transceiver ICs have been recently reported [5]-[13], many of them are fabricated in SiGe BiCMOS [5]-[8]. More recently, efforts have been reported to integrate the 10Gb/s CDR in CMOS technology for cost reduction and higher integration purposes [10]-[13]. However, these designs need a large off-chip integration capacitor to

[1] Overhead processing includes add-drop multiplexer.

meet the jitter peaking and jitter tolerance defined in the Telecordia OC-192 standard.The off-chip capacitor increases the number of external components and pin count; also it couples noise from off-chip to the control voltage of the VCO in the CDR block. Another issue is that the bondwire inductor increases drastically the high-frequency impedance of the loop filter making the CDR more sensitive to HF noise.

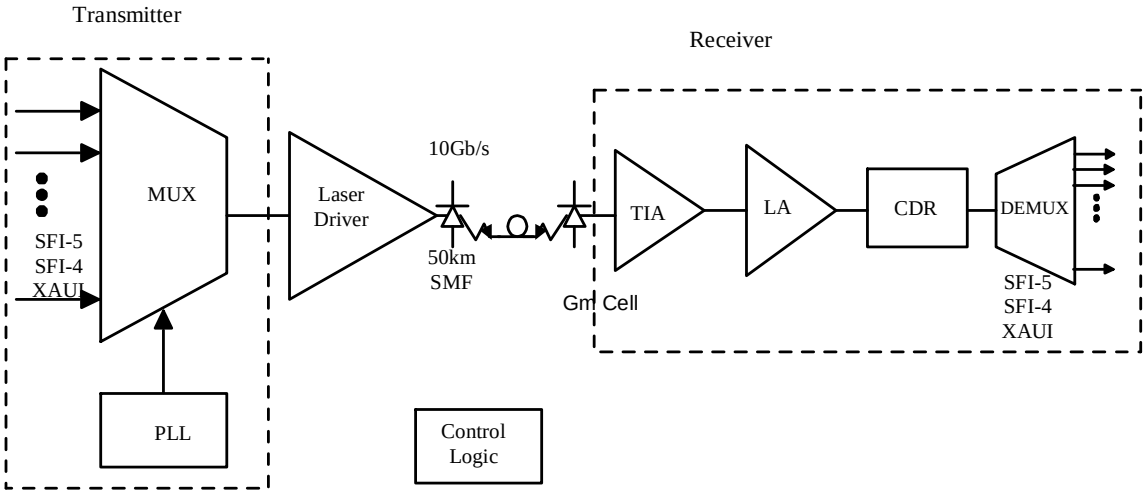


Figure 3.1 Optical Transceiver Block Diagram

As shown in [39], decreased area of on-chip capacitance can be realized by using active loop filters together with feedforward charge pumps. However, active loop filters increase the design complexity and jitter due to noise (mainly flicker) and offset contributions of active devices.

In [40], a sample-reset loop filter is proposed to create the stabilization zero. Theproportional path needs a narrow pulse to perform the reset function, but the narrow pulse generation is quite difficult in 10Gb/s CDR circuitry.

In this section, a fully integrated CDR architecture that obviates the need of the large off-chip integration capacitor by adding two feed-forward paths to generate the stabilization zero is proposed. The required capacitor in this architecture is of the order of hundred picofarads (pFs), which is far smaller than that required by conventional loop filter configurations. Besides, resistive source degeneration techniques used in the auxiliary path reduce the effective input capacitance and alleviate the loading of the phase detector. RC source degeneration techniques are adopted for zero peaking and hence bandwidth extension in double edge D-Flip-flops (DEFF) of the phase detector (PD) designs is obtained. The CDR can recover the PRBS data with pattern length of 2^{15}-1 and more than 0.5 unit interval peak to peak (UI_{pp}) total jitter (54.5ps eye closure by passing data through 9 inches FR4 PCB trace) and the total jitter of the recovered data is 22.7ps with a RMS jitter of 0.74ps.[2]

The high frequency jitter tolerance of this design is over $0.31UI_{pp}$ by applying a PRBS data with a pattern length of 2^{31}-1. The CDR was fabricated in a standard 0.18μm CMOS technology. In III 2 existing solutions and the proposed architecture are compared. In III.3, the building blocks are described in detail. The measurements results are discussed in III.4, and the conclusions are given in III.5.

[2] Only PRBS 2^{15}-1 data pattern is applied to test the CDR recovery capability to the ISI effect. For PRBS 2^{31}-1 data, the eye closure is much heavier than 0.55UI and BER is difficult to be maintained as low as 10^{-12} unless an extra limiting amplifier is inserted between the FR4 PCB trace and the data input on- chip.

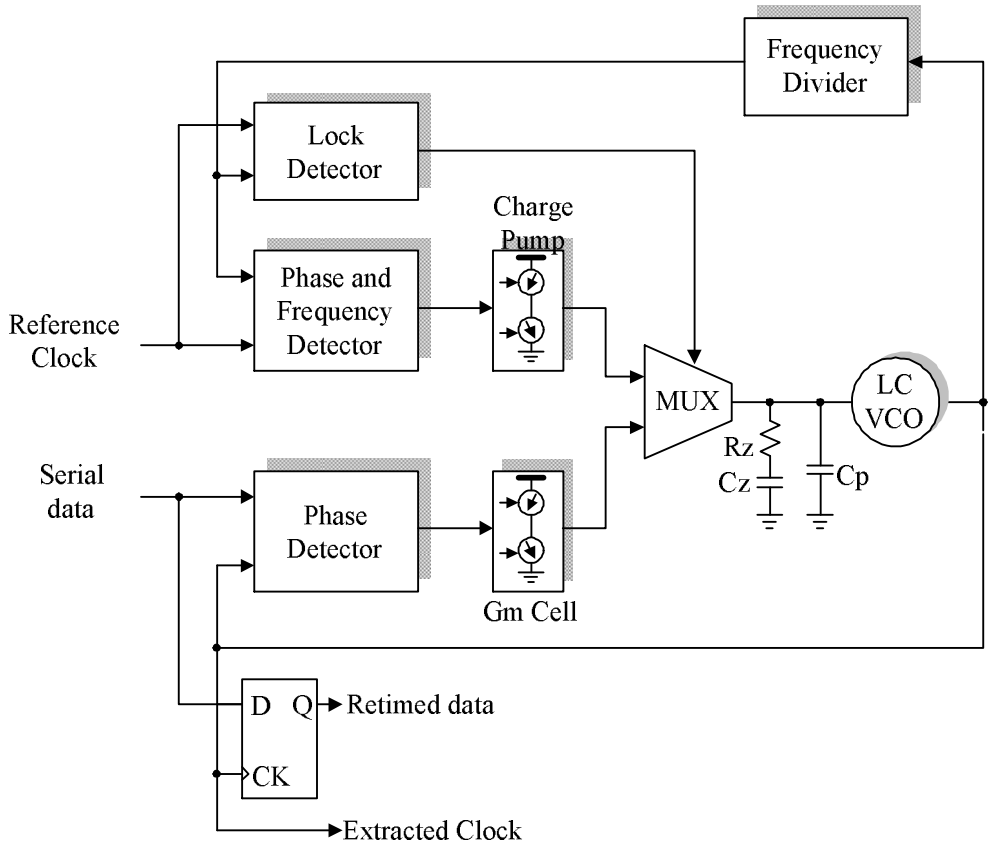


Figure 3.2 Conventional PLL Based CDR Architecture

III.2. Description of the Architecture

III.2.1. Existing CDR Architectures

In most OC-192 CDR ICs reported, PLL based CDR architecture is preferred over DLL based architecture because DLL is usually a first order system hence DLL based

CDR has worse jitter tolerance and more jitter generation. When designing multiple channel receivers, it is advantageous to use the DLL [41], but this is not the scope of this dissertation. The CDR architecture can be divided into linear and binary depending on the selection of the phase detector [21]. The conventional linear and binary CDRs use a Hogge Phase detector and Alexander phase detector, respectively. Typically, binary CDR is widely adopted in OC-192 receiver implementation for the following reasons: i) the D-flip-flop (DFF) in binary phase detector has inherently good match with the retiming DFF; ii) most linear phase detectors generate narrow pulses with widths proportional to the phase error between the timing alignment of the data and clock signals [6]. In a typical 0.18μm CMOS technology, the narrow pulses are difficult to generate and prone to process variations.

The diagram of a typical linear CDR is shown in Figure 3.2 [11]. The CDR includes two loops, a frequency acquisition loop (FAL) and a phase detection loop (PDL). The VCO's frequency is tuned through two control mechanisms: proportional control which directly modulates the VCO control port by the phase detector (PD) output directly and integration control which slowly tracks (integrates) the variations at the output of phase detector through an integration capacitor. The proportional and integration controls have basically the same effect as using a charge pump together with a filter made of a series resistor and a capacitor [8]-[9].Although this architecture is used frequently in the past, the dual loop linear CDR limits its performance due to two drawbacks. Firstly, the linear phase detector can not run at very high speed under current CMOS technology. Secondly, the CDR needs a large off-chip capacitor which is difficult to integrate on-chip. The

extra pin for the off-chip cap can potentially cause noise which affects the jitter performance of the CDR design.

III.2.2. Proposed CDR Architecture

The previously reported architectures need an off-chip loop filter or integration capacitor to meet the jitter specifications. The proposed CDR employs the conventional dual-loop architecture but the multiplexer is inserted before the charge pump CP1 and an auxiliary charge pump CPA is connected to the loop filter as shown in Figure 3.3. A similar technique has been reported in a patent which was recently released [42].

The frequency acquisition loop uses a conventional linear phase frequency detector, while the phase detection loop adopts a half rate, double-edge DFF (DEFF) based binary phase detector which is similar to that reported in [10]. Although the DEFF phase detector may allow to eliminate the frequency acquisition loop, the FAL was included to ensure enough frequency locking range. The switching between the FAL and PAL loops is controlled by a lock detector which works at the reference frequency of the FAL. Upon power-up, a successive-approximation register (SAR) type controller performs a coarse tuning for the VCO to within 1% frequency error of the target frequency by switching in or out a MIM capacitor bank and tuning a large coarse tuning varactor. Once the frequency difference between the internally divided clock and the reference clock is within 300ppm, the CDR will switch to the phase detection loop.

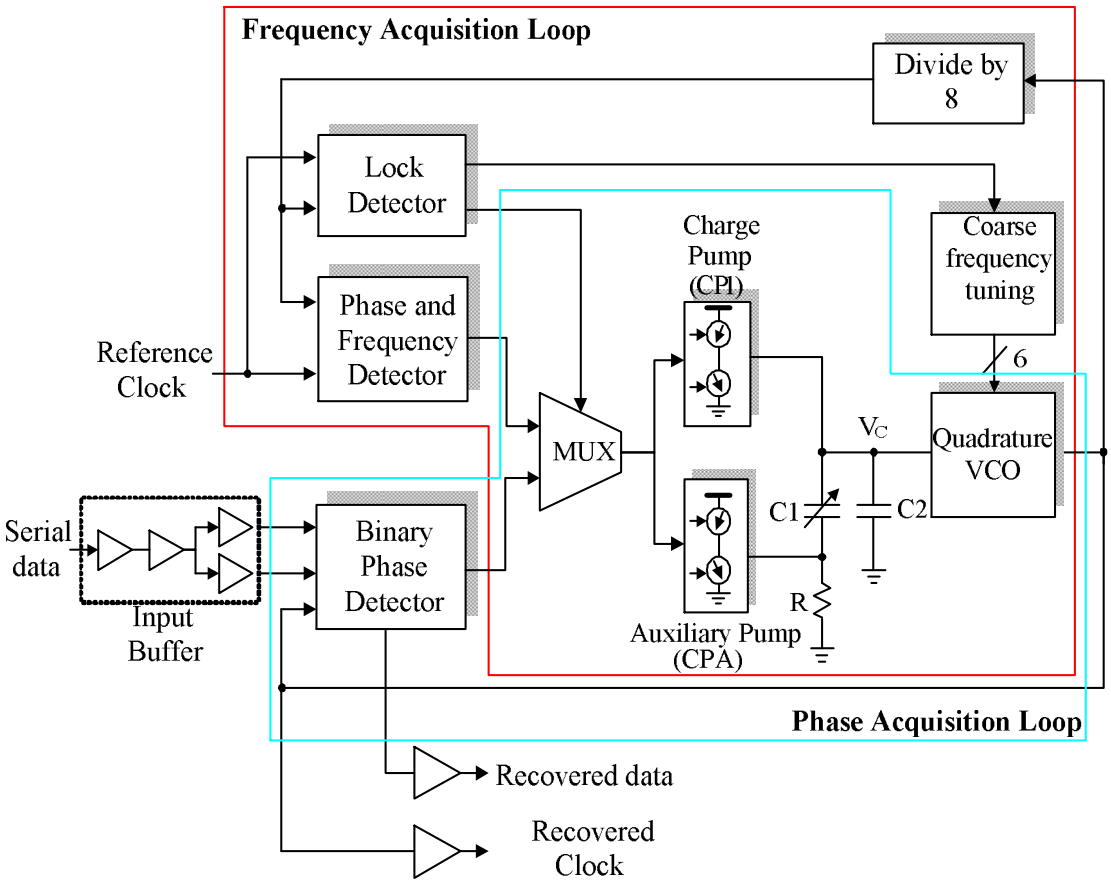


Figure 3.3 Proposed CDR Architecture

The phase detection loop uses a couple of charge pumps (CP1 and CPA). CP1 and loop filter enables the operation of a regular charge pump; the location of the zero-pole pair is determined by the time constants *R(C1+C2)* and *RC2*, respectively. In absence of the CPA, the spacing between the pole and zero frequency is entirely determined by the capacitive spread between C1 and C2. Low frequency noise signals injected into the loop filter are integrated by *C1+C2* while high frequency signals are absorbed by C2

only. Therefore, it is desirable to increase as much as possible C2 to make the loop filter more robust against medium and high frequency noise current injected at node Vc in Figure 3.3. Since C1 is often more than 15*C2 to ensure enough loop phase margin, often C1 values are in the range of nF, making very difficult to have full on-chip solutions.By adding the CPA more flexibility is introduced for the design of the loop filter and allows us to increase C2 for a given zero-pole location. As demonstrated in section III.C, another benefit is that the zero-pole location is still determined by C1/C2 but also by the ratio of the bias current used in CP1 and CPA, resulting in capacitance values that can be integrated into a single-chip. Also, high-frequency attenuation can be improved because C2 can be scaled up.

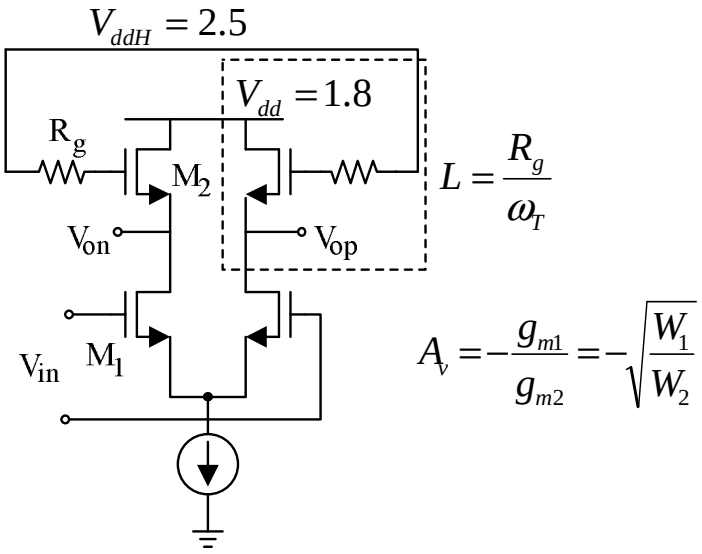


Figure 3.4 Active Inductor Peaking Amplifier

III.3. Description of the Building Blocks

In this section, the design of the main building blocks of the proposed architecture is discussed.

III.3.1. Input Buffer & Output Buffer

Both the input and output buffer shown in Figure 3.3 include five stages of CML amplifiers. Active inductor zero peaking is adopted every two buffer stages to avoid excessive equalization effect. To save chip area, active emulated inductors are employed [43].The schematic of the active inductor is shown in Figure 3.4. By using two power supply, i.e., VddH=2.5V, Vdd=1.8V, with the resistor Rg series connected to the gate of M2, the equivalent inductor $L = R_g / \omega_T$.

The gain of the amplifier is $A_v = -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{W_1}{W_2}}$; where ω_T is the cutoff gain frequency of the M_2, W_1 and W_2 are the widths of M_1 and M_2, respectively. Extensive simulations were done to ensure both enough bandwidth (> 7.5GHz) and small group delay variation (< 13ps). Lack of enough bandwidth, excessive equalization and large group delay reduces the eye opening and hence affect the signal integrity of the data.

III.3.2. Phase Detector Design Considerations

The architecture is similar to that reported in [10],[14], as shown in Figure 3.5. The double edged D flip-flop(DEFF) is constructed by using two current mode logic (CML)

latches which are clocked with opposite clock phases, followed by a multiplexer that is selected by the input clock level of the CML latch. Zero peaking is a good solution to extend the bandwidth to tolerate higher input data rate such as 10Gb/s; in fact, series feedback has been successfully used in wideband Cherry-Hopper amplifier design in 1960's[44]. In this design, a multiplexer with RC source degeneration is used to extend its 3 dB bandwidth; the schematic is shown in Figure 3.6. The effective small signal gain transfer function of the multiplexer is

$$Av(s) = \left(\frac{G_m R_L}{1 + G_m R_s / 2} \right) \left(\frac{1 + sR_s C_s}{\left(1 + \frac{sR_s C_s}{1 + G_m R_s / 2} \right)(1 + sR_L C_L)} \right) \tag{3.1}$$

where G_m is the transconductance of the input pair transistor; R_L and C_L are resistor and capacitor load, respectively. R_s and C_s are the degeneration resistor and capacitor, respectively, added to improve multiplexer performance. If the MUX is designed such that $R_s C_s \cong R_L C_L$, the zero cancels the output pole and the bandwidth increases without causing peaking in its frequency response. The *RC* source degeneration network decreases the input capacitance and thus eases the design of the preceding latch which sees smaller capacitance load. The expression for the multiplexer input capacitance yields

$$C_{in,effective} = \left(\frac{C_{in}}{1 + G_m R_s / 2} \right) \left(\frac{1 + sR_s C_s}{1 + \frac{sR_s (C_s + C_{in})}{1 + G_m R_s / 2}} \right) \tag{3.2}$$

where C_{in} is the gate-source capacitance of the input transistors. According to (3.2),the

input capacitance is reduced by a factor $(1+G_mR_s/2)$ at low and medium frequencies.

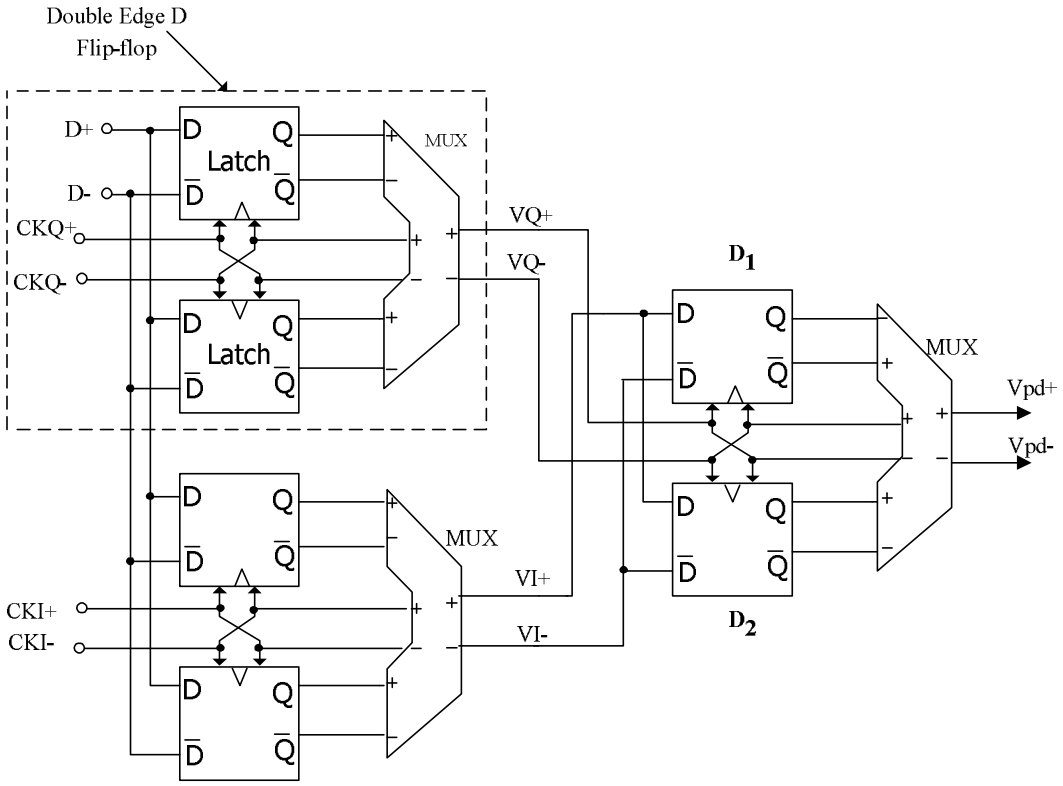


Figure 3.5 Half Rate Phase Detector

The DC gain of the circuit is $Av = \dfrac{G_m R_L}{1+G_m R_s/2}$ .The output noise and input referred noise can be written as follows:

$$\overline{V}_{n,out}^{2} = \left(\begin{array}{l} \left(2(4KT)R_L^{-1}\right) + 2(4KT\frac{2}{3})G_m^{-1}\left(\frac{G_m}{1+G_m R_s/2}\right)^2 \\ + 2(4KTR_s^{-1})(\frac{R_s}{G_m^{-1}+R_s})^2) \end{array} \right) R_L^2 \\ + 2(4KT\frac{2}{3})G_{m5,6}\left(\frac{R_s}{G_m^{-1}+R_s}\right)^2 R_L^2 \tag{3.3}$$

$$\overline{V}_{n,in}^{2} = 2(4KT)\left\{ \begin{array}{l} \frac{2}{3}G_m^{-1} + R_s + R_L^{-1}\left(\frac{1+G_m R_s}{G_m}\right)^2 + \\ \frac{2}{3}G_{m5,6}R_s^2 \end{array} \right\} \tag{3.4}$$

G_m and $G_{m5,6}$ are the transconductance of transistor M1 & M5,6 source, respectively. In order to improve the noise performance of the multiplexer, the R_s has to be designed small, while increasing G_m in the differential pair, and reducing $G_{m5,6}$ can help reduce the input referred noise.

The size of the transistors are tabulated in Table III.1.The design target is to put the zero at 2.5GHz, while the dominant pole is above 9GHz.

The simulated AC response is shown in Figure 3.7, where three conditions are compared, $RsCs=1.8R_LC_L$; $RsCs=R_LC_L$; No degeneration resistor and capacitor are used. It can be concluded that with RC source degeneration, the bandwidth is expanded about 1.65 times.

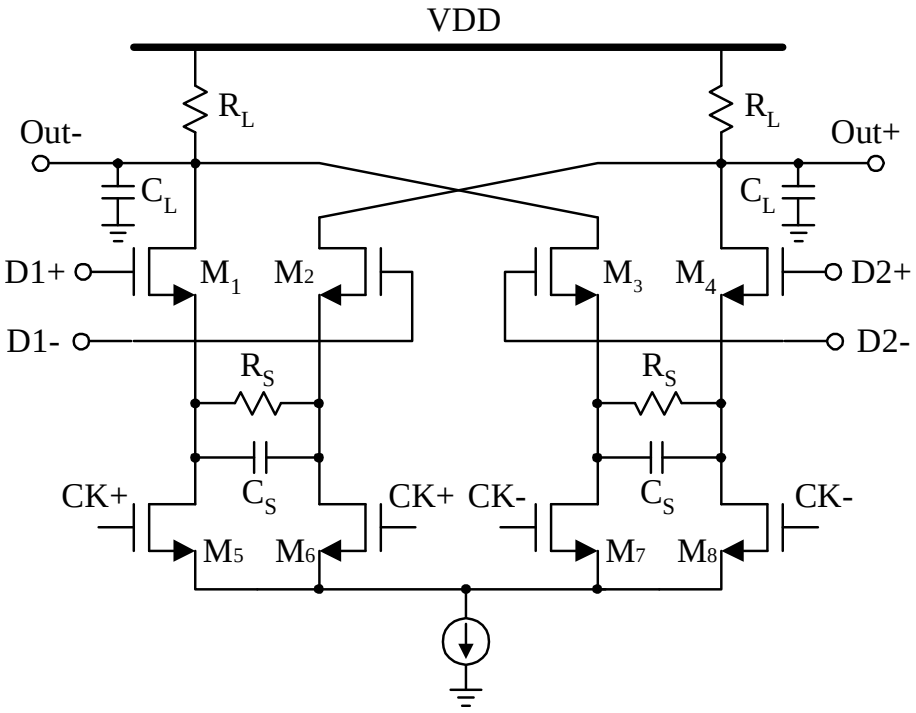


Figure 3.6 Multiplexer with RC Source Degeneration Used to Extend Bandwidth

III.3.3. Charge Pump and Loop Filter

The typical charge pump topology is shown in Figure 3.8(a). The resultant transimpedance transfer function of the configuration, when taking the I_C as the input and V_{ctl} as the output, is found as

$$V_{ctrl}(s) = \left(\frac{1}{s(C_P + C_Z)}\right)\left(\frac{1 + sR_Z C_Z}{1 + sR_Z \dfrac{C_P C_Z}{C_P + C_Z}}\right) I_C(s) \tag{3.5}$$

TABLE III.1 DESIGN PARAMETERS OF THE MULTIPLEXER

Component	Value	Component	Value	Component	Value
M1,M2 M3,M4	8u/0.18u	M5,M6 M7,M8	8u/0.18u	Mtail of the Current source	24u/0.36u
R_L	800	Rs	100	Cs	600f
Itail	800uA				

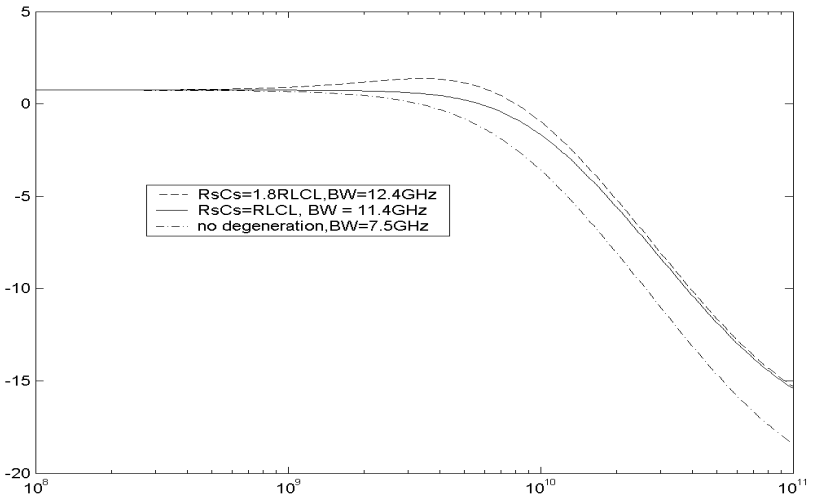
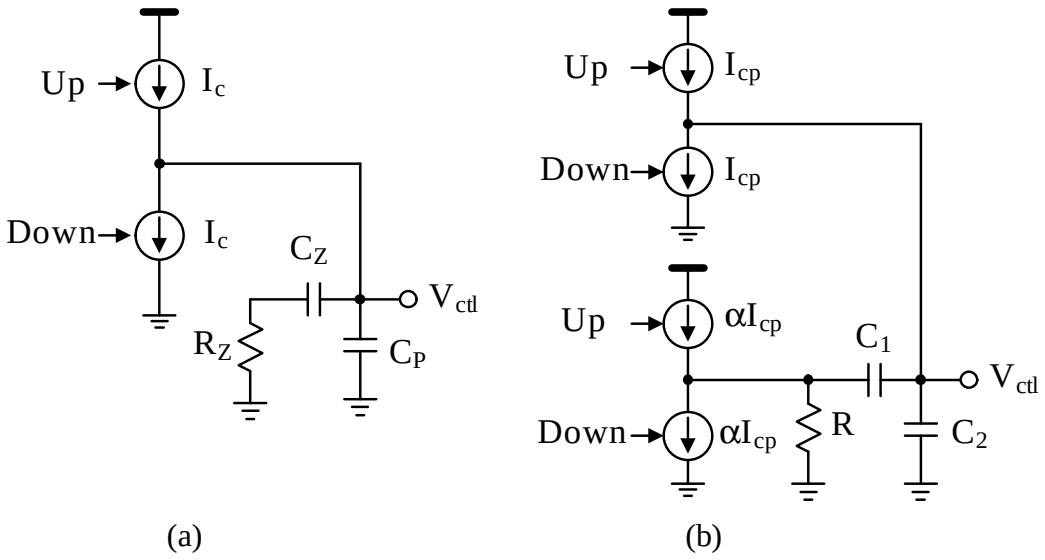


Figure 3.7 Bandwidth Expansion of the Multiplexer Using RC Degeneration

TABLE III.2 DESIGN PARAMETERS FOR THE FILTERS SHOWN IN FIGURE 3.8

Topology	Impedance @ V_{ctl} low-frequencies	Impedance @ V_{ctl} high-frequencies	Zero's Frequency	Pole's Frequency	Pole/zero Spacing
Figure 3.7(a)	$\frac{1}{s(C_Z + C_P)}$	$\frac{1}{sC_P}$	$\frac{1}{R_Z C_Z}$	$\cong \frac{1}{R_Z C_P}$	$\cong \frac{C_Z}{C_P}$
Figure 3.7(b)	$\frac{1}{s(C_1 + C_2)}$	$\frac{1}{sC_2}$	$\frac{1}{RC_1(1+\alpha)}$	$\frac{1}{RC_2}\left(1+\frac{C_2}{C_1}\right)$	$\left(\frac{C_1}{C_2}+1\right)(1+\alpha)$



(a) (b)

Figure 3.8 Charge Pump and Loop Filter Configurations: (a) Conventional Structure and (b) Proposed Configuration

In the proposed filter, the pole is placed at around 29.3Mhz, while the zero is at 270.2KHz, the pole and zero spacing is 108.5. In the classical filter design, the pole is at 26.79MHz, while the zero is at 265.2KHz, with a spacing of 100. In this design, two feed-forward paths are added to generate the required zero and poles. A simplified schematic of the single-ended configuration is shown in Figure 3.8(b).

The charge pump on top of Figure 3.8(b) generates the current I_{cp} that is mainly integrated through the capacitor C_2; the bottom cell injects αI_{cp} current into the R-C_1 node to generate a voltage proportional to the phase detector output. The resultant filter's output of the proposed configuration is found from the following expression

$$V_{ctrl}(s)=\left(\frac{1}{s(C_1+C_2)}\right)\left(\frac{1+sRC_1(1+\alpha)}{1+sR\left(\frac{C_1C_2}{C_1+C_2}\right)}\right)I_{CP}(s) \tag{3.6}$$

The location of the poles and zero are also given in Table III.2. To compare both topologies two cases are considered. Unless otherwise specified, I_C is the charge pump current of the typical loop filter with a single charge pump as shown in Figure 3.8(a). Next two cases on optimization of the filter configuration will be discussed separately.

III.3.3.1 Same Low-frequency Behavior ($C_P+C_Z=C_1+C_2$ and $I_C=I_{CP}$)

The conventional and proposed topology can be compared if its components are designed for the same loop transfer function; from Table III.2 it can be found that these components are related as follows:

$$C_1 = C_Z - \alpha C_P\left(1+\frac{(1+\alpha)C_P}{\alpha C_Z}\right) \cong C_Z - \alpha C_P$$
$$C_2 = (1+\alpha)\left(1+\frac{C_P}{C_Z}\right)C_P \cong (1+\alpha)C_P \tag{3.7}$$
$$R = \frac{R_Z}{\left(1-\frac{\alpha C_P}{C_Z}\left(1+\frac{(1+\alpha)C_P}{\alpha C_Z}\right)\right)(1+\alpha)} \cong \frac{R_Z}{\left(1-\frac{\alpha C_P}{C_Z}\right)(1+\alpha)}$$

It is assumed in these expressions that $C_Z >> C_P$ to ensure enough pole-zero spacing in the conventional charge pump. According to (3.7), reasonable values of α $(1<\alpha<C_Z/C_P)$ lead to $C_1<C_Z$ and $C_2>C_P$. Although to increase α is desirable because C_1 can be further reduced, its benefits are limited due to the large values required for R when α approaches C_Z/C_P. It can be shown that the smallest R is required when

$$\alpha = \frac{\frac{C_Z}{C_P}-1}{2} \tag{3.8}$$

In this case, $R=R_Z/(1+ C_Z/C_P)$. The most remarkable benefit of this approach is the larger capacitance C_2 $(=(1+\alpha)C_P)$ seen by the high-frequency noise current injected at the VCO's control node V_{ctl}, making the circuit less sensitive to high frequency noise; e.g. $\alpha = 9$ gives an additional 20 dB of attenuation for the high-frequency noise.

III.3.3.2 Minimization of Capacitors

The current used in the charge pump can also be scaled down and still be able to realize the required loop transfer function. If the bias current I_{CP} is scaled down, $I_C/I_{CP} = \beta > 1$, then the low-frequency filter's impedance, determined by C_1+C_2, can be scaled

down by a factor β as follows:

$$C_1 \cong \frac{C_Z - \alpha C_P}{\beta}$$
$$C_2 \cong \frac{(1+\alpha)C_P}{\beta} \qquad (3.9)$$
$$R \cong \frac{\beta R_Z}{\left(1-\frac{\alpha C_P}{C_Z}\right)(1+\alpha)}$$

It is clear that filter's dominant capacitance C_1 can be further reduced due to the effect of the auxiliary charge pump CPA and the current scaling factor β. The downside is that the effective low-frequency filter's impedance at the control node increases proportional to the current scaling factor. The low frequency impedance increase does not affect circuit's performance if the bias current of the charge pump is scaled accordingly. Fortunately, the medium and high frequency impedance (determined by C_2) can be made even larger than C_P if we select the scaling factors such that $1+\alpha>\beta$. The main advantage of this approach is that the overall filter's capacitance can be scaled down further while high frequency noise is filtered out by a larger capacitor.

For a typical 10G CDR with conventional series resistor and capacitor filter, the integration capacitor C_Z is around 10-30nF even if the jitter transfer bandwidth is in the range of 4M~6MHz, which is very expensive to integrate on-chip. In the proposed implementation, the integration capacitor is around 100pF which is a realizable value in CMOS 0.18μm technologies. The filter component values used for both topologies achieving the same filter output are given in table III.3.The silicon area saving of the proposed method is evident; the overall capacitance is reduced from 3 nF down to 140

pF.

TABLE III.3 COMPONENT VALUES FOR SAME CHARGE PUMP-FILTER RESPONSE

Conventional Loop Filter I_C=1.2mA	Proposed Loop Filter α=30, β=21, I_{CP}=60μA
C_Z=3 nF	C_1=100 pF
C_P=30 pF	C_2=40 pF
R_Z=200 Ω	R=190 Ω

In the real design, both charge pumps CP1 and CPA are differential architectures. The schematic of the charge pump CP1 is shown in Figure 3.9(a); the common mode feedback system (CMFB), not shown in the schematic, fix the common-mode level of V_{0+} and V_{0-}. The PMOS current sources are realized using a high swing cascode topology to increase the output resistance and reduce the current mismatches. This configuration achieves higher voltage swing (up to $1.1V_{pk\text{-}pk}$ in this design) than the classic cascode architecture.

The simplified schematic of the auxiliary charge pump is shown in Figure 3.9(b). The resistor loads are balanced; the maximum differential voltage swing across each load resistor is given as $(4\alpha I_{CP})R$. Although there is no need for large input linear range (the binary PD only outputs either high or low digital state), the source degeneration resistors are added to reduce the effective input capacitance of the CPA such that the phase detector deals with smaller capacitive loading. Because the use of resistive

terminations the need of a common mode feedback circuit is avoided. The transistors size are tabulated in Table III.4.

TABLE III.4 TRANSISTOR PARAMETER FOR BOTH CHARGE PUMPS

CP1		CPA	
M1	3u/0.18u	M1	12u/0.18u
M2	10u/0.18u	R	190
M3	20u/0.36u	Mtail	100u/0.3u
Mtail	10/0.3u		

The filter's components are found according to the following considerations. Although the binary phase detector shows nonlinear characteristic, it can still be analyzed at the benefit of its highly overdamped PLL design to meet SONET jitter peaking requirements. The stability factor as defined in [9] and [45] should be far larger than 1 to ensure the loop stability. For the proposed architecture, the stability factor ξ is defined as [9]

$$\xi = \frac{2\alpha RC_1}{T_{bit}} >> 1 \tag{3.10}$$

where T_{bit} is the bit period. Because of the overload limited (Slew limited) characteristic of the nonlinear phase tracking loop, the effective bandwidth of the CDR loop can be

computed as follows [46]:

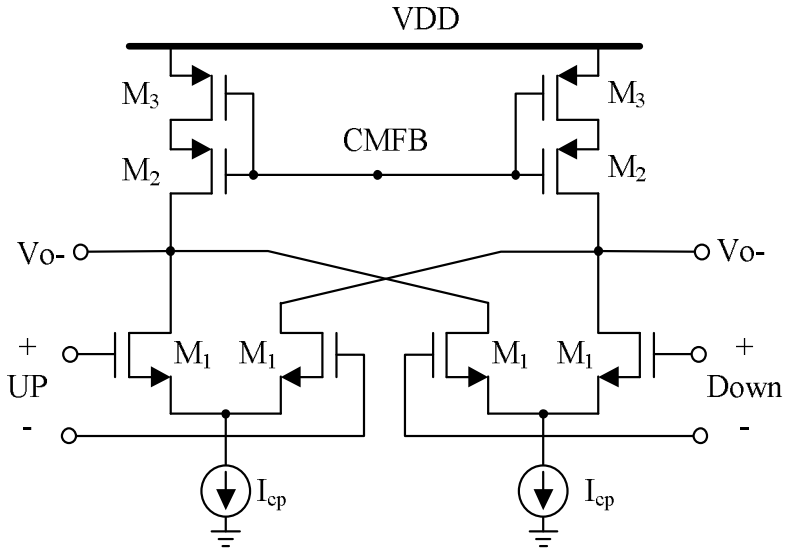
$$BW = \frac{K_p I_{cp} RK_{VCO}}{Jitter_{UI_{pk-pk}}} \tag{3.11}$$

where $Jitter_{UIpk\text{-}pk}$ is the peak to peak jitter amplitude in an unit interval ($UI_{pk\text{-}pk}$) at the frequency of interest; K_p is a fitting parameter that accounts for the delay of the phase detector, and I_{cp} is the charge pump current. The equation (3.11) is also derived in detail in the Appendix C.

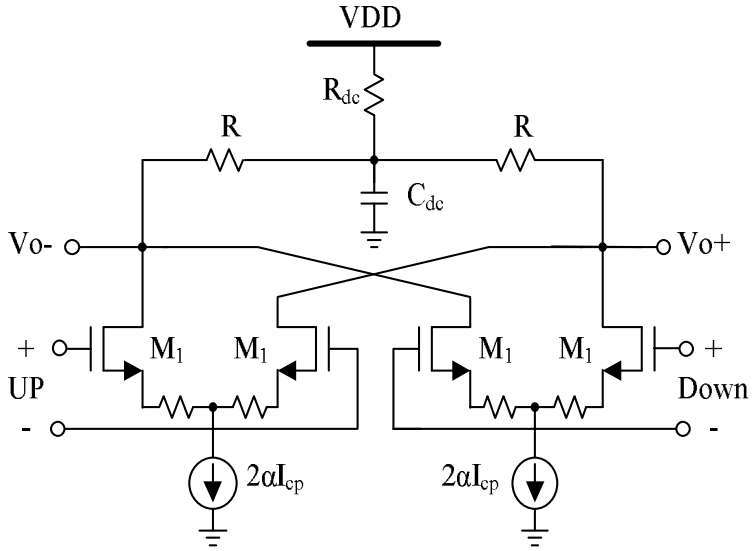
The SONET jitter tolerance specification requires that the phase detection loop should have as large effective bandwidth *BW* as possible to tolerate high frequency jitter, while the in-band noise of the PLL finally limits the bandwidth because of the low pass characteristic of the PLL. A high current in the charge pump reduces the mismatch between the up and down current, while large bias currents result in more thermal noise. The charge pump current used in this design I_{CP} is around 40μA, and the auxiliary cell uses a typical current of 500μA; $\alpha=12.5$, which can also be adjusted up to 32.

III.3.4. Quadrature LC VCO

The core of the Quadrature LC VCO is similar to that reported in [35],[37]. As shown in Figure 3.10, it is composed by 6 switch-able MIM capacitor banks for coarse frequency tuning, and a varactor for fine tuning. The varactor works in accumulation mode and is made of NMOS transistors fabricated into an N-well.



(a)



(b)

Figure 3.9 Charge Pump Schematic: (a) Simplified Charge Pump (CP1) and (b) The Auxiliary Charge Pump (CPA)

To satisfy the SONET jitter requirements, the maximum VCO phase noise must be computed. The relationship between phase noise $\ell(\Delta f_0)$ and VCO power spectrum $S\varphi(\Delta f_0)$ is derived in [31] by using the autocorrelation function of the timing jitter process and the Wiener-Khinchin algorithm. The RMS jitter of the VCO output signal is given as:

$$\sigma_j^2 = \frac{8}{\omega_0^2}\int_0^\infty S_\phi(f)\sin^2(\pi f\tau)df \tag{3.12}$$

where τ is the time duration during which the jitter is measured, and the power spectrum becomes $S\varphi(f) = 2\,\ell(f)$. Since the phase noise follows a -20dB/decade shape, it can be approximated as

$$\ell(f) = \frac{\ell_0}{(2\pi f)^2} \tag{3.13}$$

where ℓ_0 is an fitting parameter at high frequency offset in the measurement. Using the fact that

$$\int_0^\infty \frac{\sin^2(x)}{x^2}dx = \frac{\pi}{2} \tag{3.14}$$

It can be found that the RMS jitter is determined by $\sigma_j^2 = 2\ell_0\tau$; normalized by the VCO timing period yields $\sigma_j^2 = 2\ell_0\tau/(2\pi f_0)^2$ .Because the binary CDR is sensitive to the data transitions, τ can thus be approximated as the time span when consecutive runs of either "1" and "0" happen, the phase detector does not update in this case(either high or low), thus the VCO jitter accumulates as free-running case.[3] Assuming a maximum run length

[3] The charge pump can be tri-stated to alleviate the jitter accumulation, the worst case is considered here.

of 127 consecutive ‘1’s and ‘0’s data sequence, and making σ_j < 0.01UI (Unit interval, 100ps for 10Gb/s bit rate), the phase noise of the VCO should be less than -90dBc @ 1MHz offset, which is similar to that derived in [47]. The simulated phase noise curve is shown in Figure 3.11(a), with a comparison of the 2% mismatch in LC tanks. With a 2% mismatch in LC tank, the phase noise degrades about 5dB at low frequency offset up to 10KHz. Figure 3.11 (b) and Figure 3.11(c) show the phase difference between the I and Q clock is 89.8924 degree and 86.397, under normal case and 2% mismatch between the I and Q LC tanks. In Figure 3.11(d), the center frequency of 5GHz is covered by 6 bands of frequency tuning to overcome the limited tuning range of LC tank VCO.

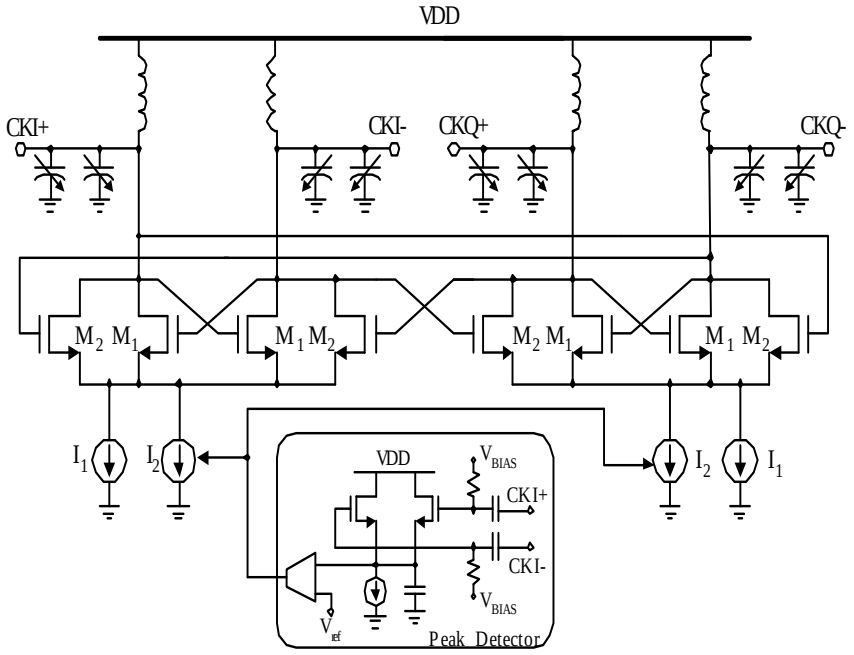
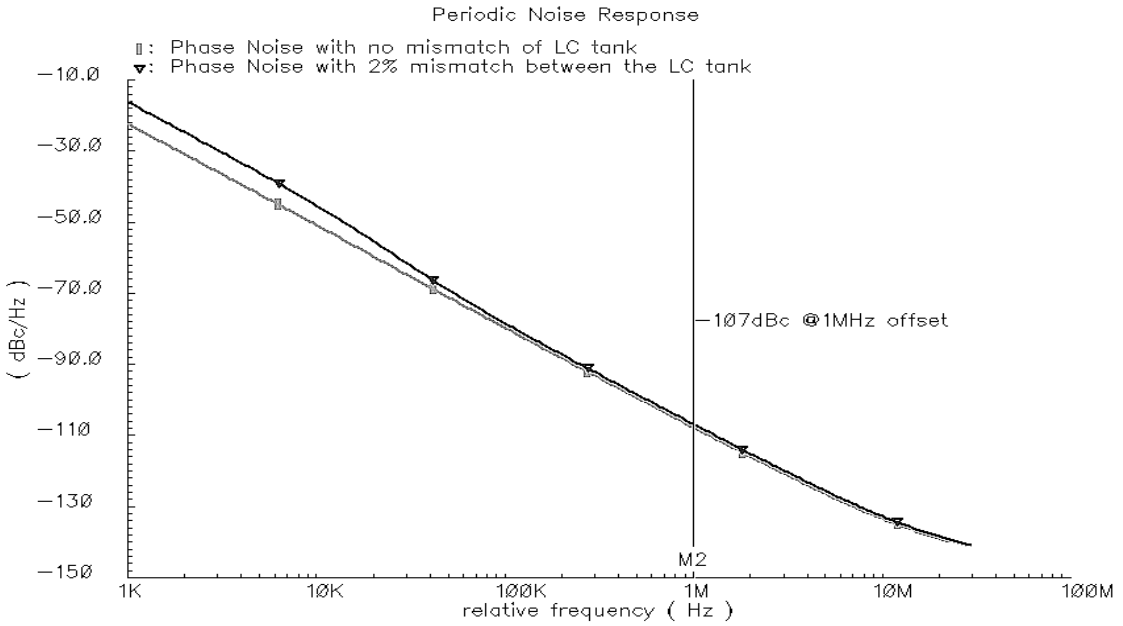
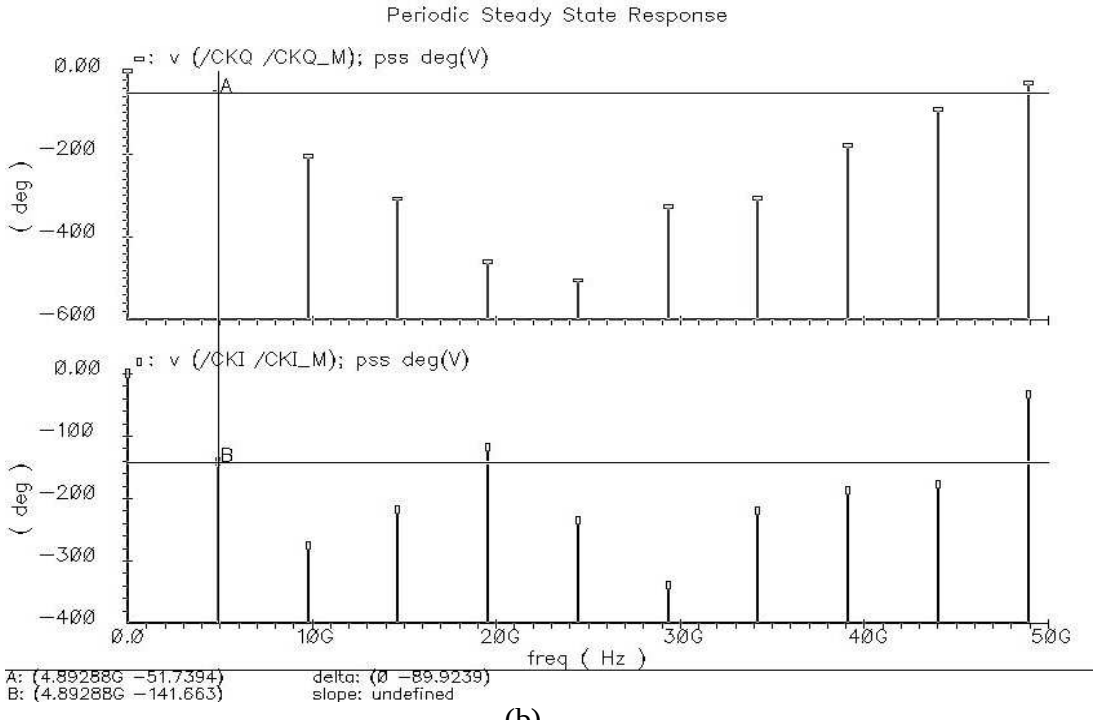


Figure 3.10 Quadrature VCO Iimplementation

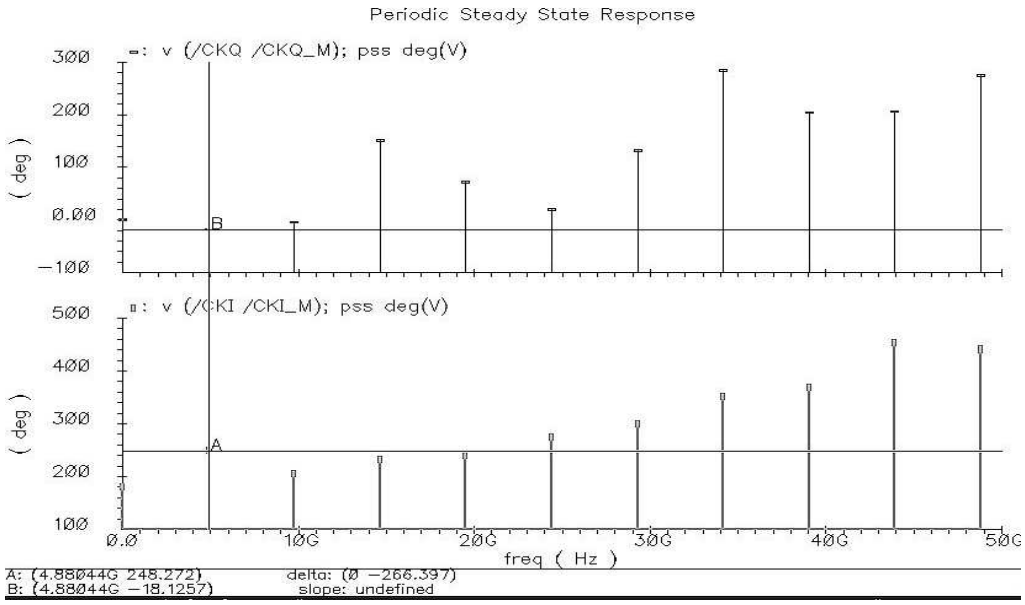


(a)

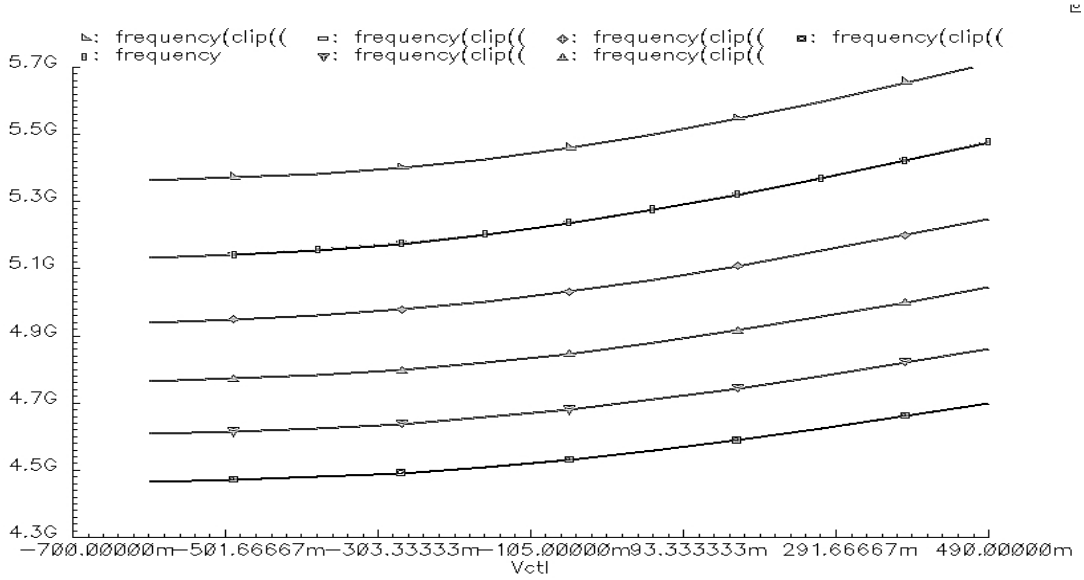


(b)

Figure 3.11 PSS Analysis of the VCO: (a) Phase Noise Simulation of the VCO, (b) Phase Mismatch between the I/Q Clocks of the VCO



(c)



(d)

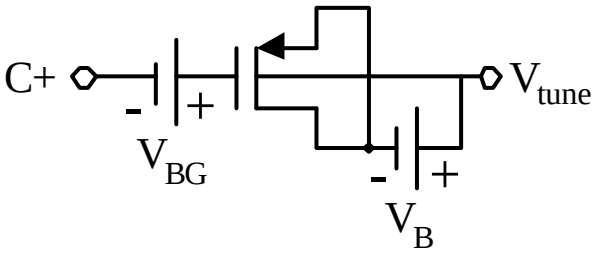
Figure 3.11 Continued: (c) Phase Mismatch between the I/Q Clock of the VCO(Assume 2% Mismatch between the LC tank), and (d) VCO Tuning Curve with 6 Frequency Bands

Due to process, voltage and temperature (PVT) variations the amplitude of the VCO output is not well controlled. To minimize this issue, an automatic amplitude control that uses a peak detector [48] and a single-stage differential pair amplifier which adjusts the tail current of the LC tank maintains constant VCO amplitude. The VCO's output amplitude can also be externally adjusted through an array of programmable current sources.

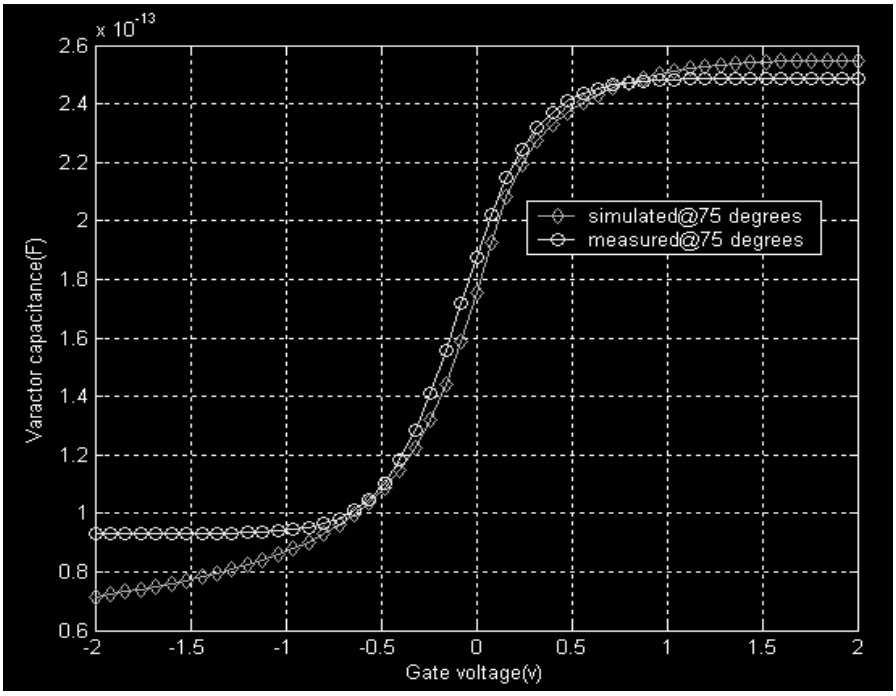
The switching in or out of the MIM capacitor bank is controlled by a successive approximation register (SAR) block. Since the accumulation varactor is designed by putting NMOS transistor into an N-well, it can not be simulated directly as the inversion mode varactor which can use the transistor model. The varactor simulation is made easy by a convenient model which is shown in Figure 3.12 (a). The model use a PMOS transistor which has the same size as the NMOS transistor in the varactor, and the V_{BG} is the bandgap voltage source (around 1.2V); the bulk of the PMOS transistor is considered as the tuning voltage input. The simulated varactor curve and the measured varactor curve are compared in Figure 3.12(b); deviations are less than 10% at 75°. The component values are summarized in Table III.5.

TABLE III.5 COMPONENT VALUES OF THE QVCO IN Figure 3.8(a)

M1	16u/0.18u	Mtail (I2)	250u/0.54
M2	8u/0.18u	Mtail (I1)	54/0.5u
Inductor	0.9nH	Varctor	0.8 to 1.5pF



(a)



(b)

Figure 3.12 Varactor Model and Simulation: (a) Varactor Model and (b) Varactor Capacitance versus Input Gate Voltage

III.3.5. BER Considerations for Input Data

The Bit error rate (BER) is a function of both deterministic jitter (DJ) and random jitter (RJ)[49]. The total jitter (TJ) which is a combination of DJ and RJ determines the eye opening of a data input. For RJ, with a standard deviation σ, the probability density function(pdf), pdf_{RJ} can be represented as

$$pdf_{RJ}(t,\sigma) = \frac{1}{\sqrt{2\pi\sigma}} e^{-\left(\frac{t^2}{2\sigma^2}\right)} \tag{3.15}$$

While the DJ can be written as

$$pdf_{DJ}(t,W,\sigma) = 0.5\left(\delta\left(t,-\frac{W}{2}\right) + \delta\left(t,\frac{W}{2}\right)\right) \tag{3.16}$$

where W is the magnitude of DJ, given as peak to peak.

The TJ *pdf* can thus be derived as convolution of the DJ and RJ *pdf*.

$$pdf_{TJ} = pdf_{RJ} \otimes pdf_{DJ} \tag{3.17}$$

By sweeping various sampling time ts, the BER can be estimated by calculating the cumulative density function using pdf_{TJ}.

$$BER(ts) = \int_{-\infty}^{ts} pdf_{TJ}(t)dt + \int_{ts}^{\infty} pdf_{TJ}(t)dt \tag{3.18}$$

The BER bath-tub curve is displayed in Figure 3.13.For robustness, it is desirable to have more than 0.5UI eye opening in the input data stream, such that the CDR can recover data with low BER. Figure 3.13 shows that the eye opening is 0.45UI when the input data with a RJ of 0.008UI and a DJ of 0.44UI. For this case, the sampling instant falls into the inner region of the bath tub curve, the data can be recovered when the eye

opening is over 0.44UI with a *BER* < 10^{-12}. For the combination of 0.02UI RJ and 0.6 UI DJ, the eye opening is only 0.16UI for a *BER* < 10^{-12}, which is very tough even for the CDR to recover data with BER < 10^{-12}.

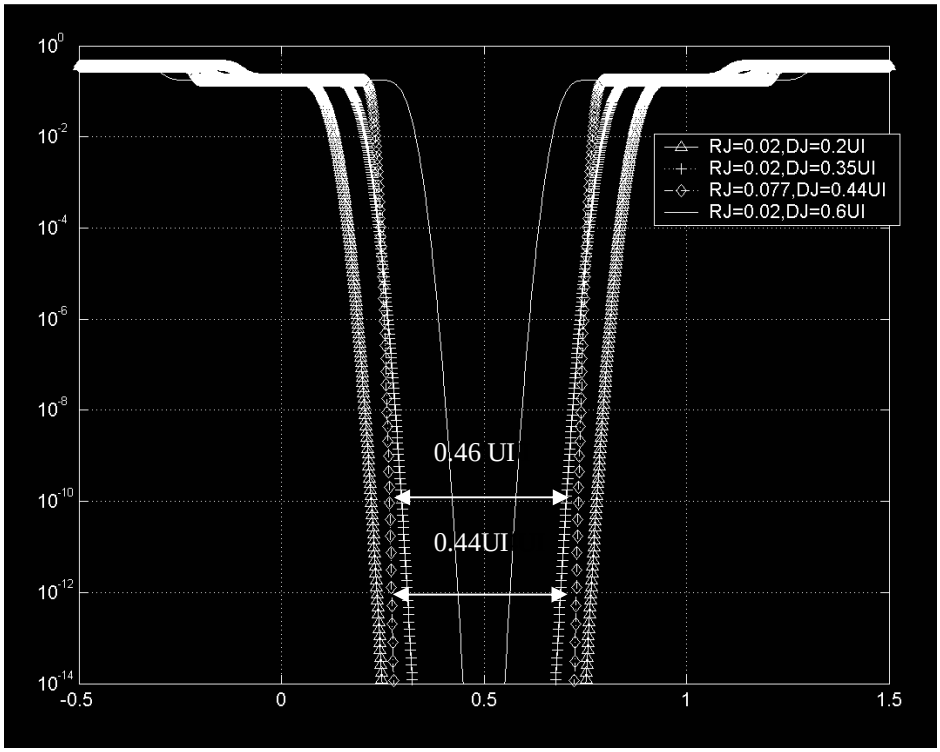
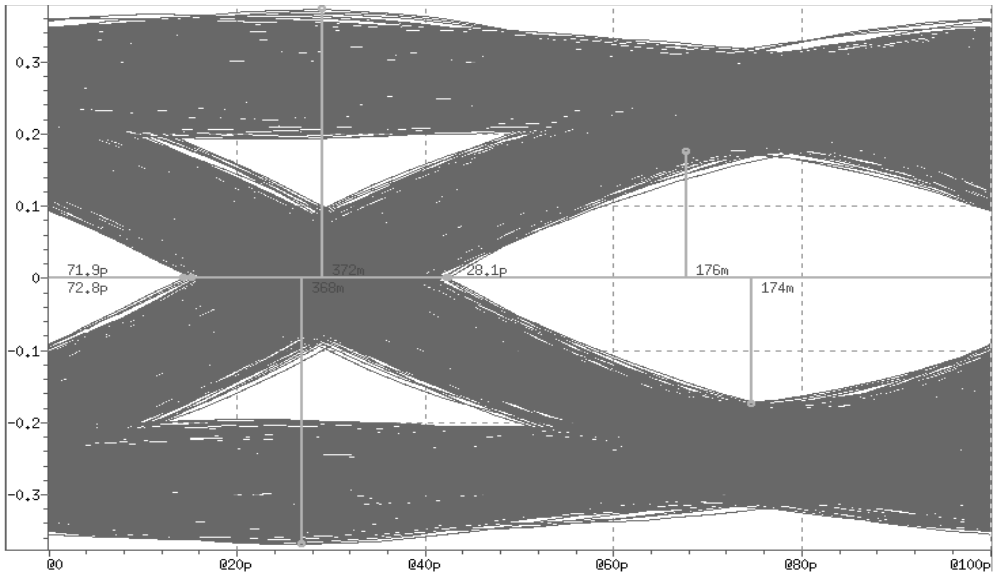


Figure 3.13 BER Bath-tub Curve as Function of Different DJ & RJ Combinations

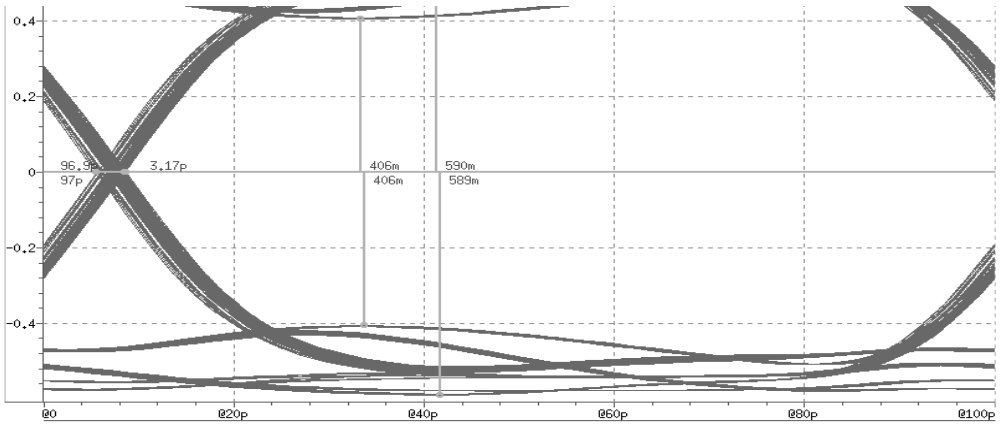
III.3.6. Some Simulation Results of the CDR Loop

To verify the function of the designed CDR circuit, the 10Gb/s PRBS data input are distorted by adding over 0.28UIpp ISI jitter. The CDR can regenerate the input data and the peak to peak jitter is less than 4ps, which is less than 0.05UIpp. The eye diagram of the input data and the recovered data of the CDR device is shown in Figure 3.14 (a) and

Figure 3.14(b); Figure 3.14(c) demonstrates the pull-in process of the CDR, the recovered clock of the CDR converges to the frequency of 5GHz, which is half rate of the input date rate, the rms jitter of the clock is 0.96ps. In the next section, experimental results are described in detail.



(a)



(b)

Figure 3.14 Top Level Simulation Results: (a) The Eye Diagram of the Input PRBS Data with a Total Jitter (TJ) of 28.1ps, (b) The Eye Diagram of the Recovered Data by the CDR,with a TJ of 3.17ps

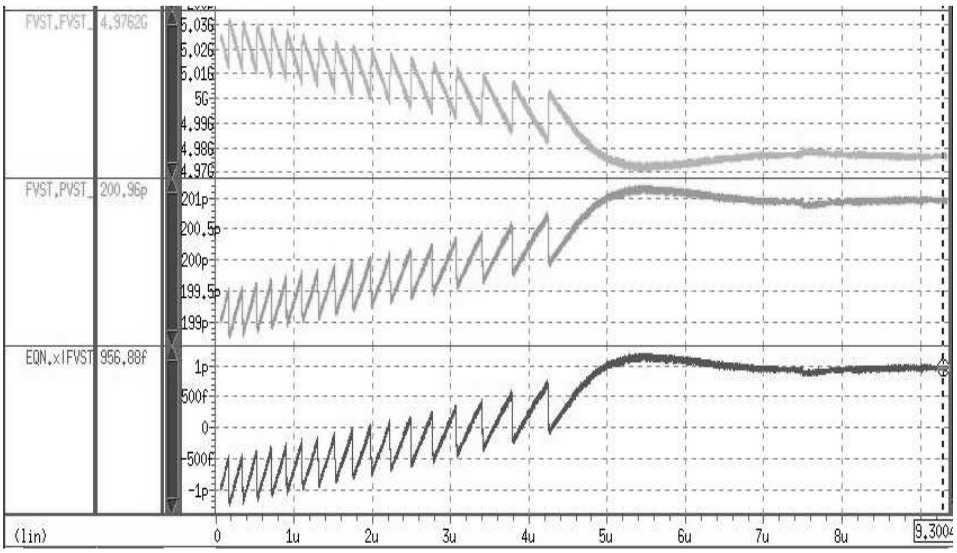


Figure 3.14 Continued: (c) The Pull-in Process of the CDR Circuit

III.4. Experimental Results

The chip was fabricated in a 0.18μm, 1P6M CMOS process through the MOSIS educational service; Figure 3.15 shows a micrograph of the CDR, which is pad-limited and occupies 2 x 2 mm^2 chip area with the on-chip loop filter included. The entire characterization test is performed at room temperature. BER and jitter tolerance were performed by using an Anritsu MP1763C 12.5GHz pattern generator, Anritsu 1764C 12.5GHz error detector, and Agilent 71501C jitter analysis test systems.

III.4.1. Printed Circuit Board (PCB) Design

A four layers PCB is designed and fabricated for the characterization of the prototype chip. A photo of the fabricated PCB is shown in Figure 3.16. The reference

clock differential inputs, data inputs, and recovered clock outputs, recovered data outputs are routed as co-planar waveguide (CPW) in order not to cause serious loss to high speed signals. All the high speed signal tracks are terminated using 50 ohms load. Several potentiometers (variable resistors) are used to adjust the bias of the CDR devices.

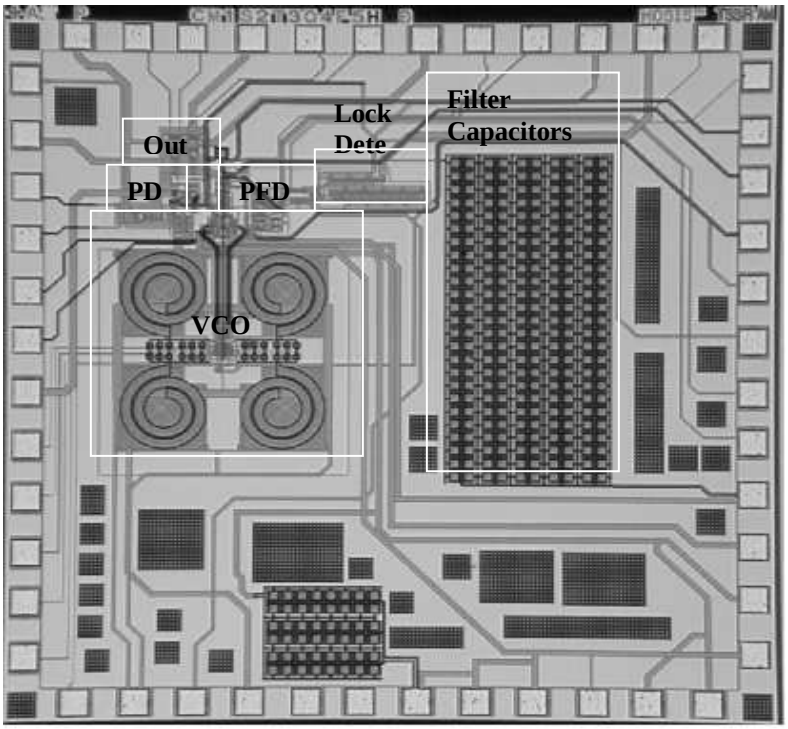


Figure 3.15 Chip Microphotograph

The analog and digital power supplies are separated in order to reduce the effect of digital switching noise coupled into the analog power supply. The VCO and VCO buffer are powered using a separate voltage regulator to reduce the power pulling of the VCO.

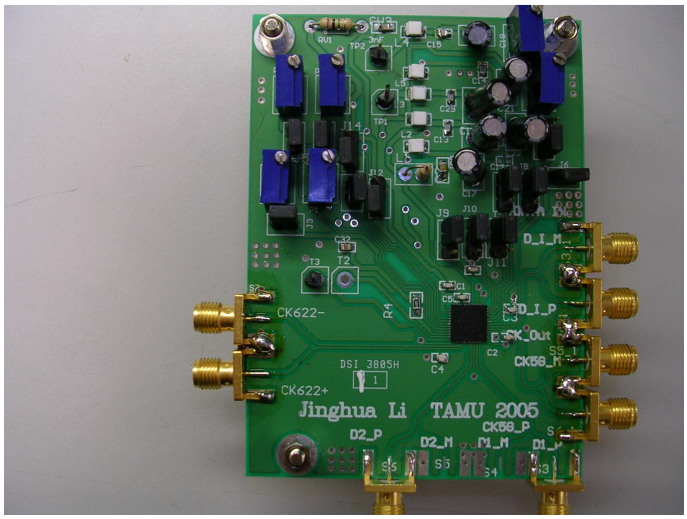


Figure 3.16 The PCB to Test the Prototype IC

Special attention is paid in designing the PCB by using Protel CAD software; to name a few:

1) The CPW traces are 10mil wide typically; the differential pair traces are 11mil wide separated.
2) Enough vias are placed for ground plane for good conduction.
3) Fill ground plane near the high speed traces as symmetrical geometry, such that the differential signals have the same environments and hence good matching.
4) Adding decoupling caps near the chip to reduce the ground bounce noise.
5) ESD power and ground are routed separately.

6) Power traces are made as wide as possible, in order to improve the thermal performance, tear-drop vias are placed on both power and ground.
7) All the transmission lines avoid the use of right angle to reduce the reflection effect. As shown in the photo of the fabricated PCB, the transmission lines bend smoothly instead of using right angles.
8) All the 0805 package chip capacitor are replaced using smaller SMT package such as 0402 and 0603 package to reduce parasitic capacitance.
9) When soldering SMA connector, the SMA pins are cut shorter to reduce the parasitic effect and improve the signal integrity.

III.4.2. Test Equipments Setup

Test equipments setup, the list of the test equipments used are listed below:

1) Agilent 71501D jitter analyzer
2) Agilent 70843C Error Detector
3) HP Signal generator 83752A for reference clock generation.
4) Agilent 86100C Oscilloscope(>40G/s)
5) Anritsu PRBS pattern generator MP1764C
6) HP Power supply

The test diagram is shown in Figure 3.17.

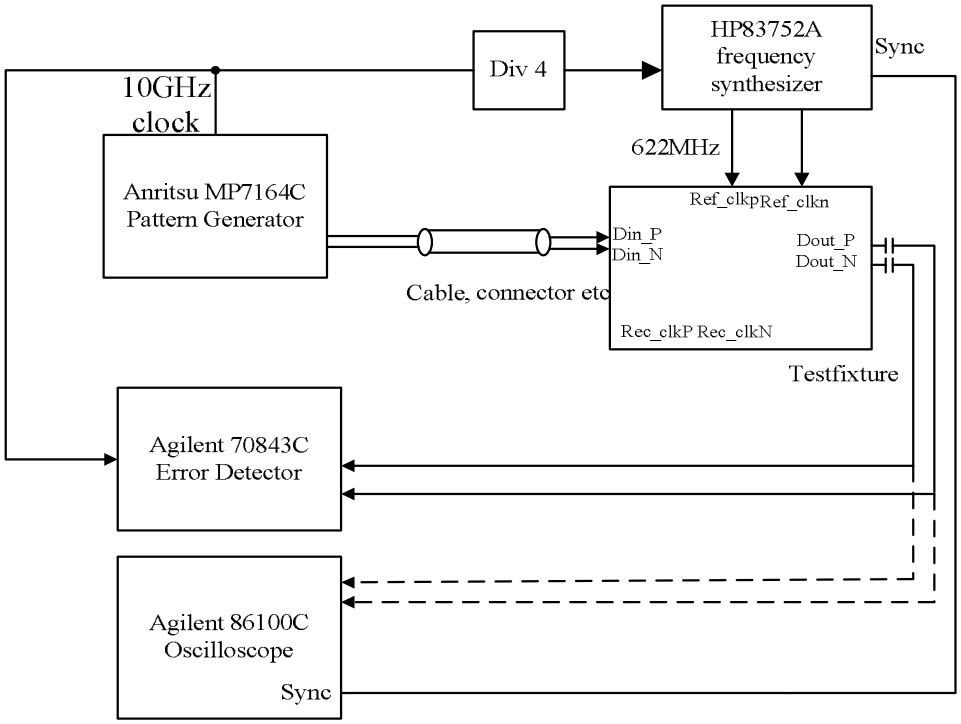


Figure 3.17 Measurements Setup Diagram

The test PCB board for the prototype chip is connected in the setup shown in Figure 3.18. The input data at 9.9532Gb/s is generated by the Anritsu MP7164C pattern generator; then the data is passed through the measurement cable and connectors to the data input SMAs of the PCB board. The recovered data is connected to the Agilent 70843C to perform Bit error rate(BER) analysis. Also the data can be passed to the high speed sampling oscilloscope for measuring the eye diagram. The jitter tolerance and jitter transfer measurement is similar; the only difference is that the Oscilloscope is replaced by the Agilent 71501D jitter analyzer.

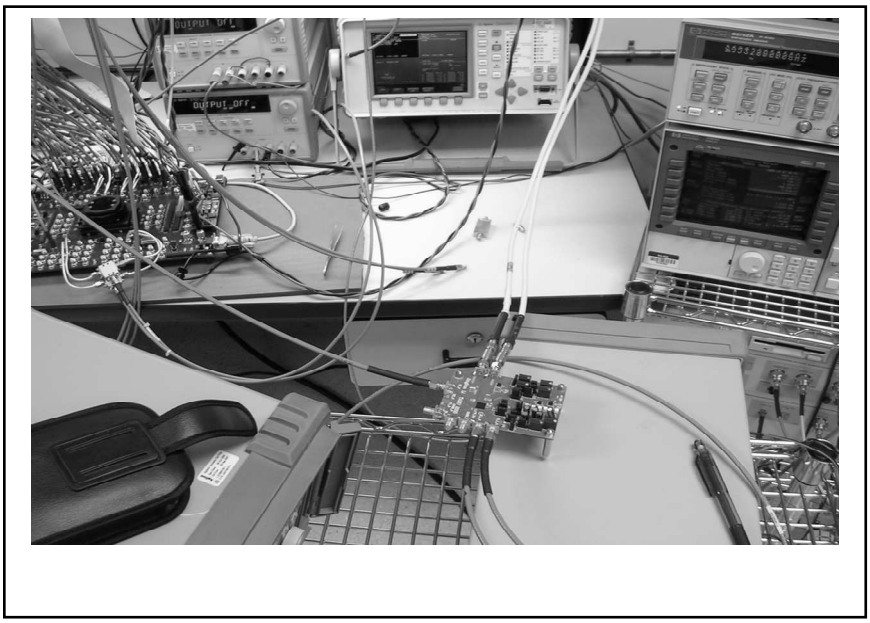


Figure 3.18 Photo of a Typical Equipment Setup to Test the Prototype IC

III.4.3. Measurements Results of the Prototype IC

III.4.3.1.Measurements by Adding ISI in the Input Data

In 10-Gigabit Ethernet (10GE) applications, the wideband jitter in the serial inputs typically adds the difficulty of the CDR device to recover the clock. A good way to measure the performance of the CDR device is to add inter-symbol interference (ISI) to the input data, the ISI induced jitter is a wideband jitter which can test roughly the jitter tolerance of the CDR.

By passing the input data to a 9 inches PCB traces, excess ISI is included in the data input, the horizontal eye closure is around 0.54UI. Figure 3.19 shows the eye diagram of a stressed 2^{15} –1 input PRBS data and the recovered data at 9.953Gbps. Even if the horizontal eye closure[4] is 0.54UI, the device can still recover the data with a BER < 10^{-12}. The RMS-jitter of the recovered data is less than 0.74ps with a 2^{15} –1 PRBS pattern for input data with 150mV_{pp} single-ended amplitude. Jitter statistics are shown in Figure 3.20. It can be shown that the ISI jitter in the input data pattern is around 54.5ps while in the recovered data the ISI jitter is only 13.3ps peak to peak, which shows that the CDR works properly with acceptable jitter tolerance for 10 Gigabit Ethernet applications. The active inductor peaking in the buffer chain contributes to help equalize the input data signal.

The waveform of the recovered clock is shown in Figure 3.21 with a peak to peak jitter of 8ps which is less than 0.08UI and conforms to the SONET jitter generation specification(< 0.1UIpp). Jitter tolerance is tested by passing the data pattern generated from the pattern generator to the device under test (DUT), the recovered data is sent to BERT tester for BER test. There is no loop back testing through the transmitter. As shown in Figure 3.20, for an input signal of 150mV_{pp} single-ended, a high frequency jitter tolerance greater than 0.3 UI_{pp} is achieved (at 80MHz of sinusoidal jitter frequency, the jitter tolerance is 0.31UI_{pp}), which confirms that, for 0.5UI eye closure at the input

[4] The stressed data is generated by passing the data out of pattern generator to 9 inches FR4 PCB trace.

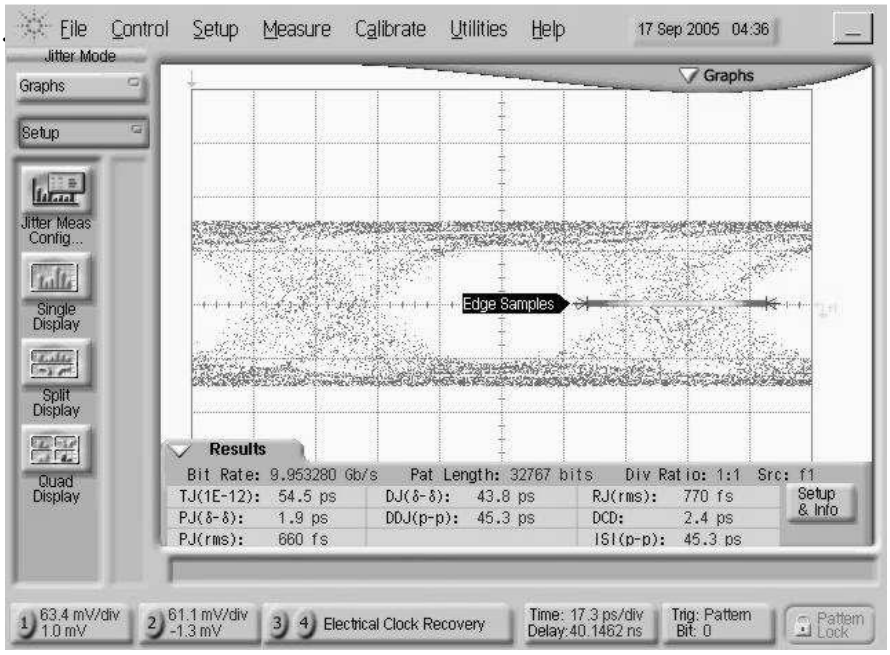


Figure 3.19 Eye Diagram for Input Data PRBS 2^15-1 with TJ of 54.5ps

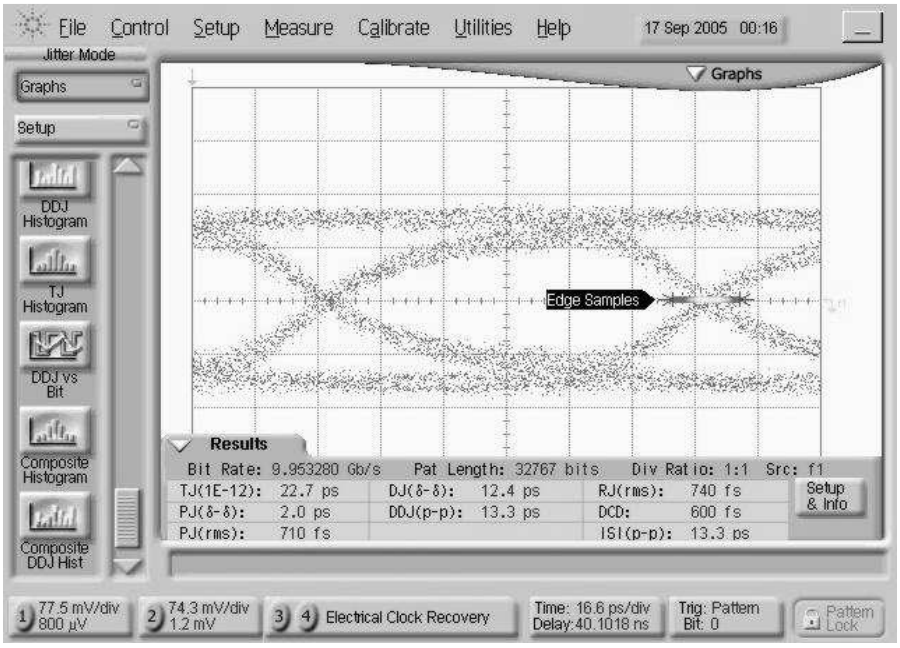


Figure 3.20 Eye Diagram of Recovered Data with Input Data Shown in Figure 3.19

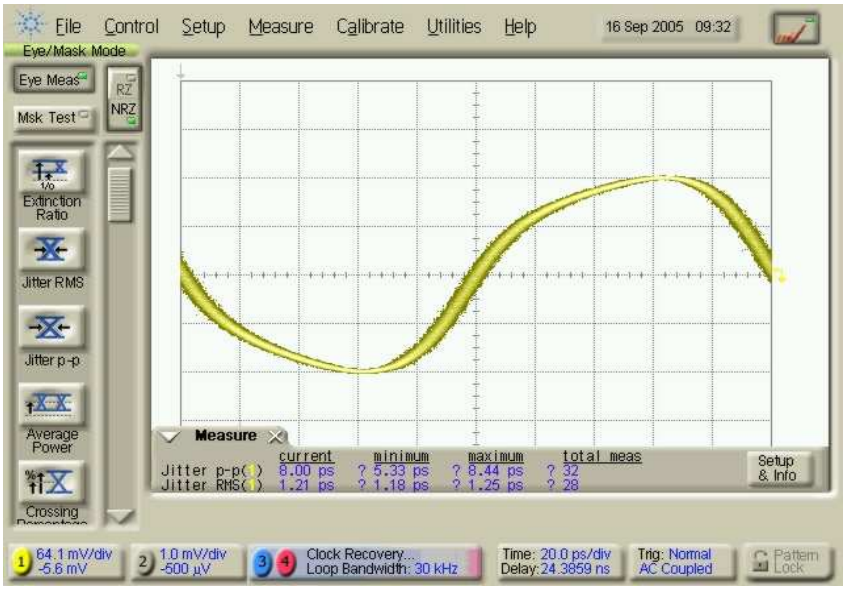


Figure 3.21 The Recovered Half Rate Clock with 8ps Peak-to-peak with PRBS with a Pattern Length of 2^{31}-1

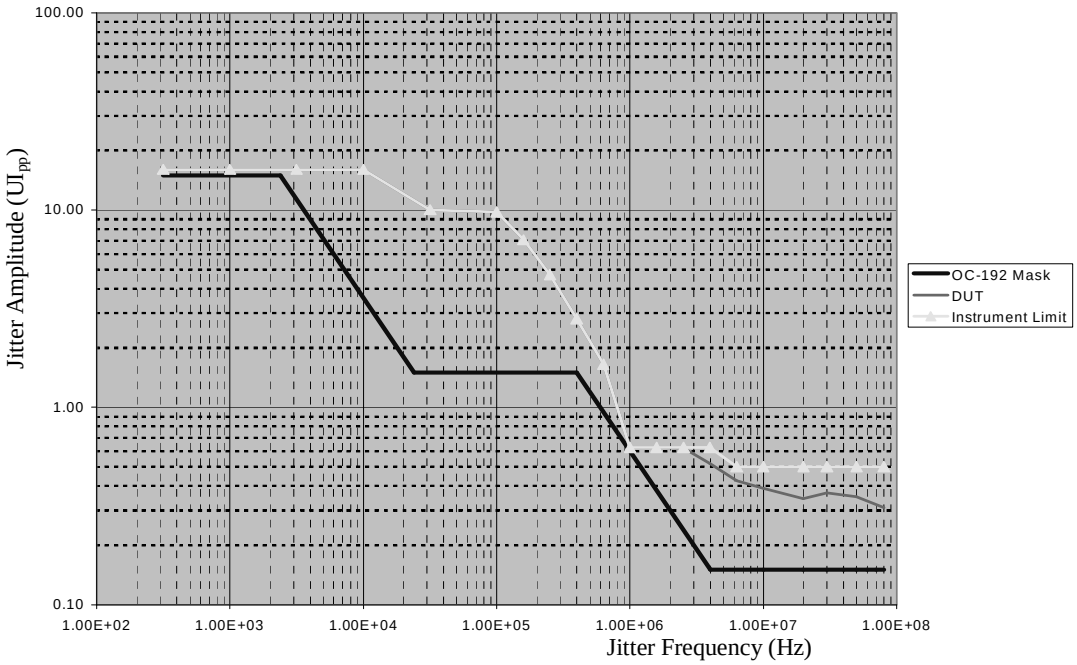


Figure 3.22 CDR Jitter Tolerance Measurements

data due to ISI distortion, the CDR can still recover the data correctly. The CDR exceeds the SONET OC-192 jitter tolerance mask with over 100% margin for jitter frequency higher than 10MHz; for jitter frequency lower than 2MHz, the CDR exceeds the jitter tolerance test limit of the equipment used, where the data input is a 2^{31}-1 PRBS pattern.

III.4.3.2.Jitter Tolerance Measurement

The jitter tolerance specification in SONET OC-192 standard defines the jitter criteria to measure the ability of the CDR device to recover the input data with an in-band jitter ranging from 50KHz to 80MHz. It is in general measured by adding sinusoidal jitter (<80MHz) to the input data until -1dB loss in the signal power is reached. In our measurement, only several measurements are based on BER of 10^{-12} because it is very time consuming. In many cases, a BER of 10^{-10} measurement can be performed to check the functionality of the prototype IC. Measurement result shown in Figure 3.22 shows that the device passes the jitter tolerance test , with a slightly passing at around 1MHz frequency; That is due to the measurement limit of the test equipment.

III.4.3.3.Jitter Transfer Measurement

As discussed in previous sections, SONET jitter transfer specification defines the jitter peaking performance of the CDR devices when used in a chain of repeaters in telecommunication products. A jitter peaking of less than 0.1dB is recommended in

SONET OC-192 specification. The jitter transfer measurement is done by phase modulating the input data and measuring the phase modulation in the recovered clock. The jitter transfer curve is similar to a single-pole low pass filter response, i.e., it shows a -20dB rolling off until the 3dB bandwidth frequency is reached. The measurement result is shown in Figure 3.23, which shows that the jitter transfer bandwidth (corner frequency) is 6.2MHz, and the jitter peaking is 0.07dB(less than 0.1dB defined in the SONET standard), thus it does not meet the SONET standard for the jitter transfer specification of 120KHz. However, as pointed out in [5], the jitter transfer characteristic can be shaped by a jitter attenuator PLL to shape the jitter transfer bandwidth of the clock recovered by the CDR.

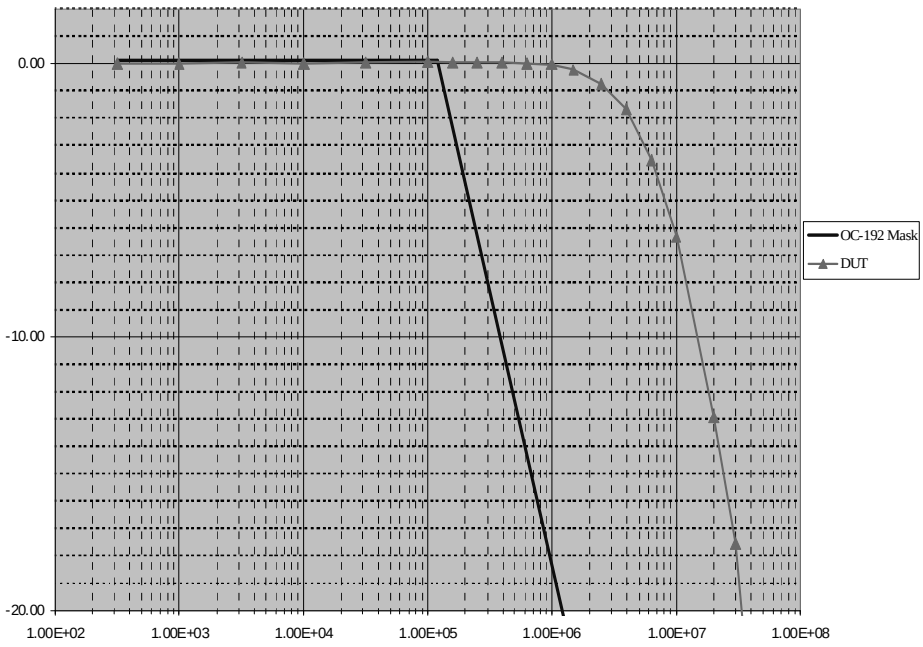


Figure 3.23 Jitter Transfer Measurement of the CDR Device

III.4.3.4.Jitter Generation Measurement

The jitter generation measurement is performed without adding external jitter at the input data, and measure the CDR device intrinsic jitter (or Phase noise). The limitation of the bang-bang CDR is that due its nonlinear nature. Even if the CDR loop is locked, the control voltage of the VCO fluctuates slightly, which is unlike a linear phase detector CDR, thus potentially bang-bang CDR has worse jitter generation performance than a linear phase detector CDR.

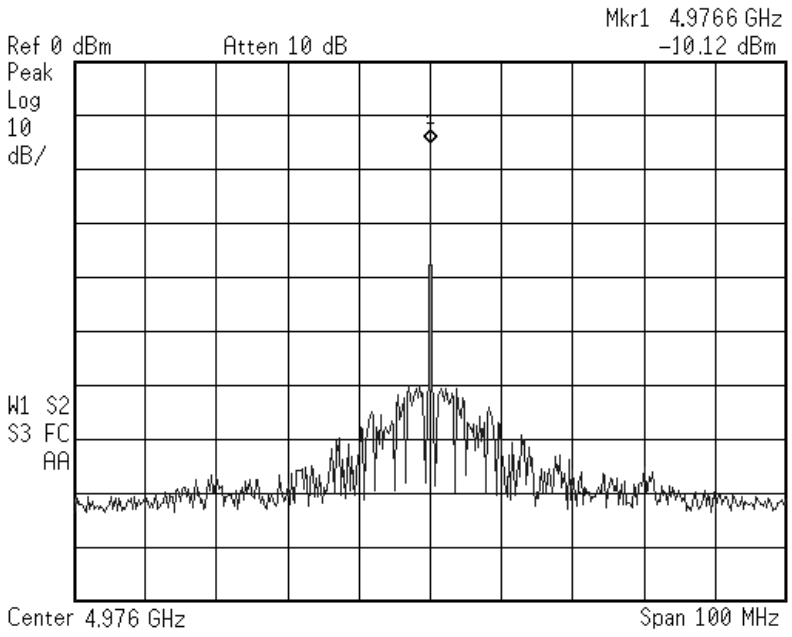


Figure 3.24 Frequency Spectrum of the Recovered Clock

The measurement of the spectrum and phase noise of the recovered clock when the CDR device is locked are shown in Figure 3.24 and Figure 3.25, respectively.Notice that, the measured phase noise is a little bit worse than the simulated VCO phase noise at 1MHz offset, the reason probably is the lack of the accuracy when modeling the inductor. Also long interconnection in the layout of the chip limits the performance of the whole chip.

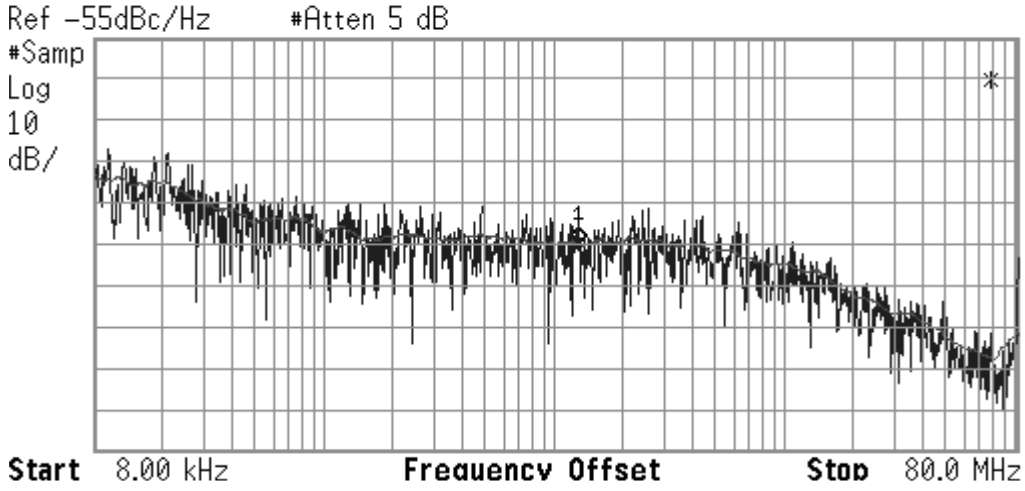


Figure 3.25 Phase Noise Plot of the Recovered Clock

To test the spectrum purity of the recovered clock, an 80MHz sinusoidal jitter with 0.32UIpp amplitude is applied to the data input by the pattern generator, the clock spectrum is shown in Figure 3.26. The attenuation of the 80MHz sinusoidal jitter is better than -42dB.

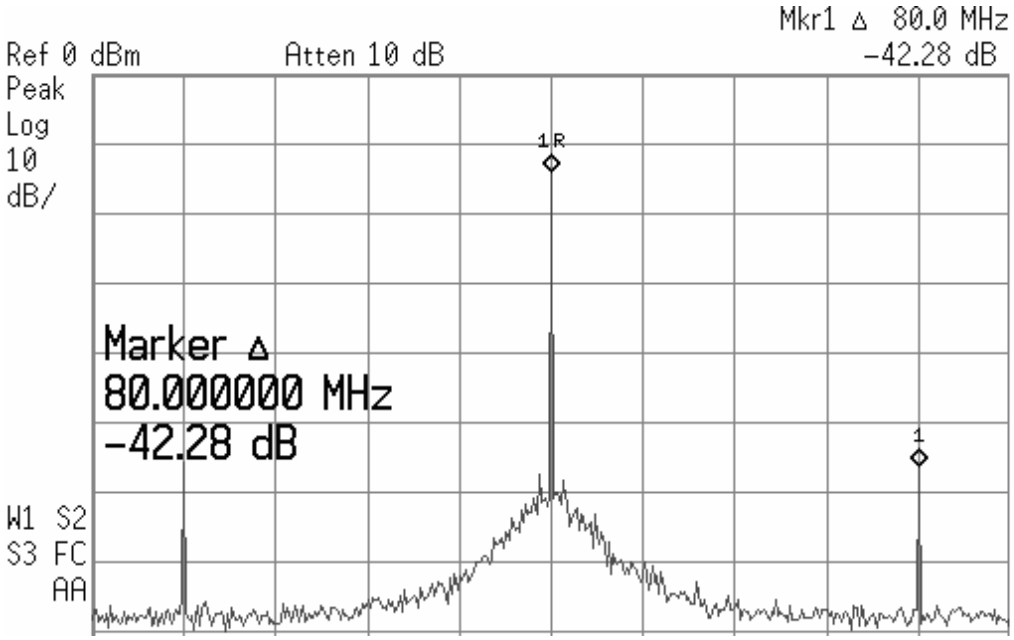


Figure 3.26 Measured Attenuation of 80MHz of Sinusoidal Jitter, 0.32UIpp

III.4.3.5.Return Loss Measurement

Return loss is the ratio, at the junction of a transmission line and a terminating impedance or other discontinuity, of the amplitude of the reflected wave to the amplitude of the incident wave [50]. The return loss value describes the reduction in the amplitude of the reflected energy, as compared to the forward energy. Typically in a transmission line, return loss is defined as

$$RL = 20\log_{10}\left|\frac{Z_{src} - Z_0}{Z_{src} + Z_0}\right| \tag{3.19}$$

where Z_{src} and Z_0 are the impedance toward the source and the load respectively. In our prototype, Z_0 is selected as 50 ohm to match the prevalent of the industry PCB vendor.Figure 3.27 shows the return loss of the input buffer, it is less than -13dB at 5GHz.

III.4.3.6.Pull-out Range Measurement

After the CDR locks to the input data at 9.953Gb/s rate, the phase detection loop can maintain lock even if the input data rate changes from 9.947Gb/s to 9.958Gb/s without going to frequency acquisition loop, which shows that the pull-out range of the phase detection loop is over 1100ppm.

III.4.3.7.Summary of the Measurements

Including the buffers, the chip consumes 290mW with a 1.8VPower supply. The chip is packaged in a 5 x 5 mm QFN package. Multiple pins are assigned to both power supply and ground to minimize the crosstalk effect. Performance of the chip is summarized in Table III.6, which shows that the proposed implementation consumes less power than previously reported solutions, except for the one reported in [10] which does not account the power consumption of the buffers. If the four on-chip inductors are

replaced with two symmetric inductors, the chip area can be reduced even further. The jitter tolerance performance of the chip is approaching or even better than reported implementation using better CMOS technologies such as 0.11um CMOS.

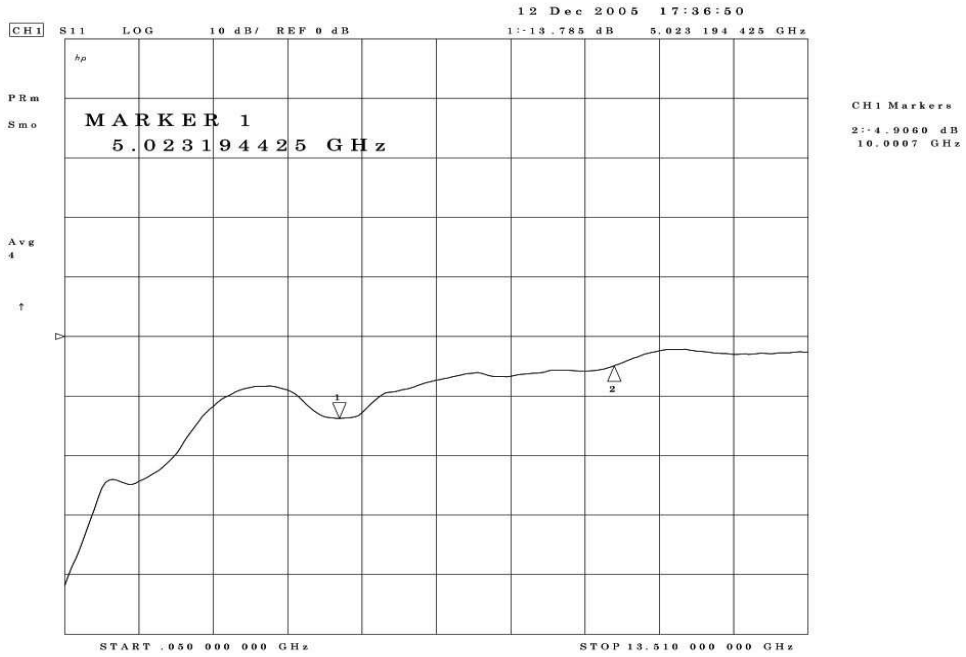


Figure 3.27 Measured Return Loss of the Input Buffer (< -13dB at 5GHz)

III.4.3.8.Summary of the Measurements

Including the buffers, the chip consumes 290mW with a 1.8VPower supply. The chip is packaged in a 5 x 5 mm QFN package. Multiple pins are assigned to both power supply and ground to minimize the crosstalk effect. Performance of the chip is

summarized in Table III.6, which shows that the proposed implementation consumes less power than previously reported solutions, except for the one reported in [10] which does not account the power consumption of the buffers. If the four on-chip inductors are replaced with two symmetric inductors, the chip area can be reduced even further. The jitter tolerance performance of the chip is approaching or even better than reported implementation using better CMOS technologies such as 0.11um CMOS.

III.5. Conclusions

A fully integrated 10-Gb/s CDR is implemented in a 0.18μm CMOS process. The design uses half rate architecture due to the relative low f_t (50GHz) of the CMOS process used. By using a new loop filter and charge pump configuration, the chip integrates all the components on-chip including the integration capacitor. Improved charge pump architecture with source degeneration, VCO with amplitude tuning and multiplexer scheme in double edged DFFs are the other techniques adopted to enhance the chip performance.

The CDR can recover data with a BER less than 10^{-12} when the input eye closure is slightly above $0.5UI_{pp}$(Horizontal eye closure) and the recovered clock with peak to peak jitter less than $0.1UI_{pp}$.The CDR also exceeds the OC-192 jitter tolerance mask with high frequency jitter tolerance over $0.31UI_{pp}$. To the best our knowledge, this reported implementation is the first fully integrated, PLL based 10Gb/s CDR in the literature.

TABLE III.6 SUMMARY OF THE MEASUREMENT RESULTS FOR 2^{15}-1

	[10]	[12]	[51]	[30]	This work[52]
Technology	0.18μm CMOS	0.18μm CMOS	0.11um CMOS	0.13um CMOS	0.18μm CMOS
Power dissipation	91mW+buffer power	400mW	311mW	980mW(including TX)	290mW(buffer included)
Chip size(mm^2)	1.75x1.55	1.95x1.5	2.9x1.6(for two channels sharing PLL)	3x5(the transceiver)	< 2x2
Input Bit rate(Gb/s)	9.9532	9.9532	9.9532	9.9532	9.9532
RMS/peak-to-peak clock Jitter when locked to input data	0.8ps/9.9ps pk-pk(locked to PRBS 2^{23}-1)	1.2ps/8ps pk-pk(locked to 2.5GHz sinusoidal)	NA	1.1ps/8.3ps pk-pk(locked to 2^{31}-1 PRBS)	1.2ps/8ps pk-pk(locked to 2^{31}-1 PRBS)
Frequency detection	Included	Not included	NA	Included	Included
Jitter tolerance	Not passing	~0.15UIpp at high frequency	~0.2UIpp at high frequency	0.35UIpp	> 0.31UIpp for high frequency JTOL
BER	10^{-9}	NA	$<10^{-14}$	$<10^{-12}$	$< 10^{-12}$
Pull-out range of the phase detection loop only	NA	NA	500ppm	NA	>1100ppm
Supply voltage	1.8V	1.8V	1.2V	1.2V	1.8V. ± 10%

IV. A MULTI-GIGABIT/S CLOCK DATA RECOVERY ARCHITECTURE USING AN ADAPTIVE BANG-BANG CONTROL STRATEGY

IV.1. Introduction

Demand for low cost SerDes ICs have been boosted due to the widespread use of SONET/Gigabit Ethernet network and chip-to-chip interface such as PCI-Express (PCIe), Serial ATA (SATA) and Fiber channel standard applications. Among all these applications, clock data recovery (CDR) is one of the key design components. With the increasing demand for higher bandwidth and large scale integration, CMOS implementation is now a design trend for predominant products. The higher bandwidth requirements (over 10GHz) and the relatively low transistor's f_t make the bang-bang phase detector based clock recovery products dominate the current market compared with the Hogge phase detector CDR products [51].

A linear phase detector usually outputs a pulse whose width is proportional to the phase error, and is a percentage of the data period; hence at a data rate greater than 10Gb/s, it is very difficult to process the phase error pulse even if state of the art deep submicron CMOS technologies are employed. The bang-bang phase detector is based on a digital processing of the phase information in a nonlinear way.

In spite of these compelling advantages of the bang-bang CDR loop, all of the reported PLL based CDR loops use a fixed bang-bang control setting to perform phase detection. Under such fixed configurations, when tracking high frequency sinusoidal jitter, the CDR experiences slew-rate limited tracking process and the jitter tolerance

performance is degraded due to the limited equivalent bandwidth of the bang-bang loop.

In this section, a new CDR architecture with slope-overload prediction and adaptive bang-bang control mechanism to maximize its jitter performance is proposed [46]. A digital predictor helps to optimize the loop bandwidth based on current and previous data. The main idea is that, by predicting the timing information of the CDR adaptively, the clock information can be more accurate than classical CDR architecture.

IV.2. Description of the Classic Bang-bang CDR Architecture

IV.2.1. Existing CDR Architecture

IV.2.1.1.1st Order Bang-bang CDR

The 1st order bang-bang CDR can be represented by the block diagram shown in Figure 4. 1. The incoming data has a nominal frequency f_{nom} and an offset frequency δf. As discussed in [53], the data phase ϕ_d (the sum of phase jitter and the phase shift caused by δf) and VCO phase ϕ_v generate the phase error ϕ_e; the error phase is digitized by the two-level phase comparator (detector) at the clock rate of the VCO output. The digitized phase error information is firstly attenuated by a factor α and then pulse modulates the VCO to track its phase with the input data phase. Evidently this phase tracking is a non-linear process due to the inherently non-linear phase detector. If the

gain of the VCO is denoted as K_{vco}, whenever a phase error is detected, a frequency step is generated, which is given by:

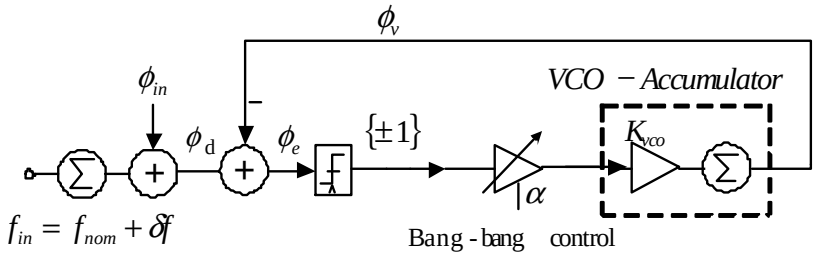


Figure 4.1 Diagram of First Order Bang-bang CDR Loop

$$f_{bb} = \alpha K_{VCO} \tag{4.1}$$

f_{bb} is the maximum frequency deviation between the VCO output and the input data nominal frequency. Assuming that the input data phase ϕ_{in} is small enough, the frequency variation is then determined as follows

$$-f_{bb} < \delta f < f_{bb} \tag{4.2}$$

Thus, the loop generates an excess hunting jitter with a peak-to-peak value of two bang-bang phase ramps, and the peak-to-peak jitter approximately computed as

$$J_{pp} = 4\pi f_{bb} / f_{nom} \tag{4.3}$$

It is worth mentioning that the loop delay in the bang-bang CDR can cause larger phase error or bit errors, which is due to the fact that, with large loop delay, the phase detector can not respond to the change of the input phase on time, thus a phase error occurs [54].If $N=log_2(f_{nom}/f_{bb})$ and denoting the maximum tolerable phase error as PE_{UIpp}, the

loop delay (LD) should satisfy:

$$LD \le \left(2^N - 1\right) PE_{UIpp} \tag{4.4}$$

Assuming a maximum jitter of 0.25 *UIpp*, and N=10 for reasonable bandwidth, the loop delay should be less than time required by 255 cycles. In this paper, the loop delay is selected to be less than the time required by 16 cycles for ease of implementation, stability, and jitter tolerance considerations.

Despite the straightforward implementation of the 1st order bang-bang loop, it has the limitation of limited frequency tracking range. In order to increase the locking range of the bang-bang loop, besides the bang-bang branch, an integral branch can be added to extend its frequency range, and hence the jitter performance of the CDR can be improved further.

IV.2.1.2. 2nd Order Bang-bang Loop

The block diagram of a 2nd order Bang-bang loop is shown in Figure 4. 2. The contribution to the phase control of both paths α and integrator of $(1/\tau)\Sigma$ in a time period equal to the bit period T_{bit} occurs when $\alpha = T_{bit}/2\tau$; therefore, the loop stability factor ξ is defined in [53].

$$\xi = \frac{2\alpha\tau}{T_{bit}} >> 1 \tag{4.5}$$

where T_{bit} is the bit period, and τ is the time constant of the integrator used in the loop filter. It is well known in control systems that to guarantee stability the loop must be designed such that $\xi >> 1$ [53].

Because of the overload limited (Slew limited) characteristic of the nonlinear phase tracking loop, the limit for the effective bandwidth of the CDR loop (*BW*) follows the following equation (4.6). It can be expressed in a simplified form as follows [22]

$$BW = \frac{K_p f_{bb}}{Jitter_{UIpk-pk}} \tag{4.6}$$

where $Jitter_{UIpk-pk}$ is the peak to peak jitter amplitude in a unit interval (UI_{pk-pk}) at the frequency of interest; K_p is the fitting parameter which accounts for the delay of the phase detector and is usually approximated as 1.2 when input sinusoidal jitter amplitude is around $0.06UI_{pk-pk}$, and f_{bb} is the bang-bang frequency step. According to (4.6), the bandwidth is inversely proportional to the input jitter amplitude, which is a result of the nonlinear nature of the binary PD. This statement can be confirmed by the describe function obtained in Appendix C.

An ideal comparator is described as $V_{out}=D*Sign(V_{in})$, and the describe function is found in the Appendix C as $DF=4*D/\pi A$, where A is the amplitude of the input sinusoidal signal V_{in} ;and D is the signal amplitude at the PD output. If the DF is combined with the linear part of the system, as expected, it is shown that the resultant loop bandwidth is inverse proportional to the input jitter amplitude; details of this derivation are given in Appendix C.

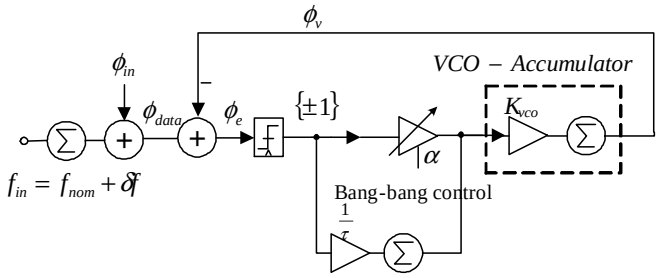


Figure 4.2 Diagram of a Typical 2nd Order Bang-bang CDR

IV.2.1.3. Slope Overload or Slew-rate Limited Process in Phase Tracking

For simplicity, let us assume that the frequency difference between the incoming data and the VCO is small, and that $\phi_d(t) = A_{UI}\sin(2\pi f_{\mathrm{mod}} t + \phi_0)$, where A_{UI} is the maximum jitter amplitude measured in peak-to-peak unit intervals, f_{mod} is the sinusoidal modulation frequency, and ϕ_0 is the initial phase for the sinusoidal jitter input. If the CDR tracking speed is not as fast as the input data phase changes, then jitter induced slope-overload or slew-rate limited process appears, as depicted in Figure 4.3. The slew rate limited process is very similar to the case of the over-damped unit response of a linear system.

The slew-rate (or slope-overload) occurs if the incoming phase variation is larger than the VCO phase variation; this condition is mathematically expressed as

$$\max\left\{\frac{d}{dt}(\phi_d(t))\right\} = 2\pi f_{\mathrm{mod}} A_{UI} > 2\pi f_{bb} \tag{4.7}$$

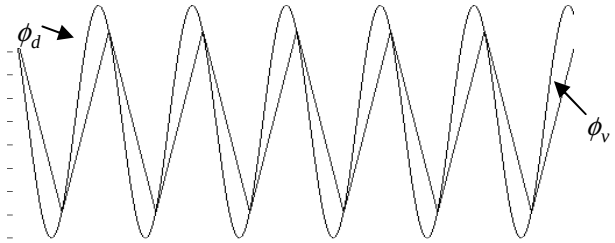


Figure 4.3 Slope-overload (or Slew-rate Limited) Phase Tracking Process

Under this condition, the peak-to-peak jitter of the hunting jitter given in (4.3) is larger compared with the case of non-slew-rate limited process. According to (4.7), the slew rate limiting also depends on the product of both the jitter frequency and the peak-to-peak jitter amplitude when considering a sinusoidal jitter, which is the toughest condition for a typical CDR device to track.

IV.3. Proposed CDR Architecture

The conventional bang-bang CDR is based on constant bang-bang frequency step to control its loop dynamics. Recently [54],[55] added some programmability to the bang-bang control to optimize the loop bandwidth; in those approaches, the charge pump current sources or the buffer amplifier gain are adjusted to change the loop dynamics. The 1st order bang-bang loop bandwidth can be varied in four steps, i.e., 2^{-13}, 2^{-14}, 2^{-15}, or 2^{-16} of the nominal data rate. The bang-bang control in a strict sense still belongs to a constant bang-bang control category and can not track the high frequency jitter because

the equivalent CDR loop bandwidth is inversely proportional to the peak to peak input jitter amplitude. For larger input data jitter, the effective bandwidth is reduced, and thus its jitter tracking capability decreases as well. In many cases, due to the presence of the unknown high frequency jitter, it is necessary to include a top level controller or CPU to configure the PLL bandwidth for the IC through a higher level protocol. However, by adopting an adaptive control of the bang-bang CDR can lead to a more robust performance across different high frequency jitter of interest.

If the CDR bandwidth is not large enough, then there is definitely the slew-rate limiting process and the corresponding peak-to-peak jitter is larger than that without severe slope-overloading case. Even if there is no slew-rate limiting process, the nonlinear nature of the bang-bang CDR loop shows hunting jitter at its steady state and the phase detector still outputs alternate high and low pulses, for the first order loop, that is equivalent to a clock pulse with close to 50% duty cycle. With a frequency change in data(Δf_d), and delta frequency variation in the VCO (Δf_V), a frequency step response can be derived similar to linear system response. Shown in Figure 4.4, the top graph is the case for a slope-overload (slew-rate limiting); and the bottom trace shows a slope-overshoot case where the CDR loop bandwidth is too small. Under both situations, the resultant tracking phase error is not optimized when the CDR loop operates in the steady state.

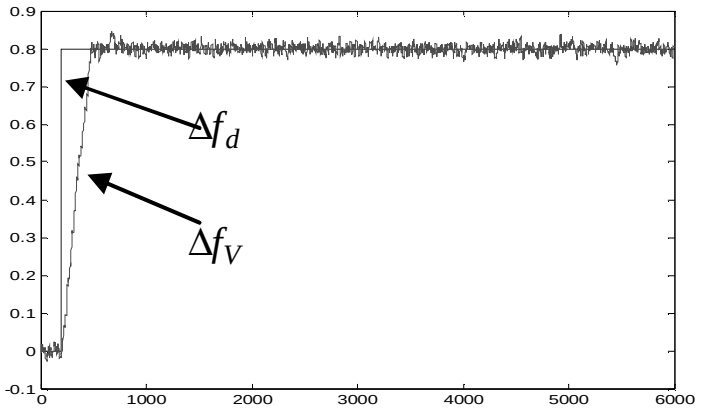
If the slope-overload or the slew-rate limiting process are detected or predicted in advance, then the loop dynamics can be varied according to the input jitter characteristic and hence the jitter tolerance performance can be greatly improved. In the following

sections, an architecture with adaptive bang-bang control is presented to tradeoff the design of slew-rate limiting and steady state jitter generation.

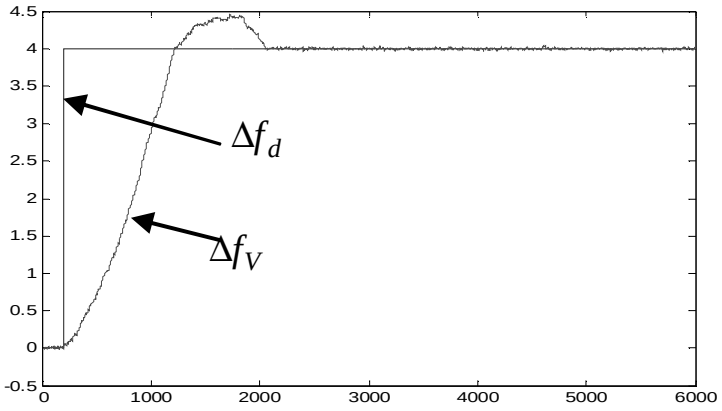
Referring back to the diagram in Figure 4.3, the digitized phase error output is plotted in Figure 4. 5. If the slope of the top trace(data phase) changes fast, there is constant high or low signal at the digitized phase error output, which means that there is slew-rate limiting occurrence. If looking more carefully at the digitized phase error output, it can be concluded that there is similarity between the architecture in Figure 4.3 with the conventional Sigma-delta modulator or delta modulator. That is the basic starting point why the adaptive modulation is adopted in the proposed bang-bang CDR design.

IV.3.1. CDR Architecture with Adaptive Bang-bang Control

A formal quantitative definition of slope overload in the CDR tracking process is difficult. A succession of more than two like bits is a reasonable criterion. Then the target is to find a method to detect or predict slope overload or slew rate limiting in the phase tracking process and then adaptively adjusts the bang-bang loop bandwidth when needed.



(a)



(b)

Figure 4.4 The Phase Tracking Slew Rate Limiting Process: (a) Slope Overload Caused by Limited Bandwidth; (b) Slope Overshoot Caused by Too Small Loop Bandwidth

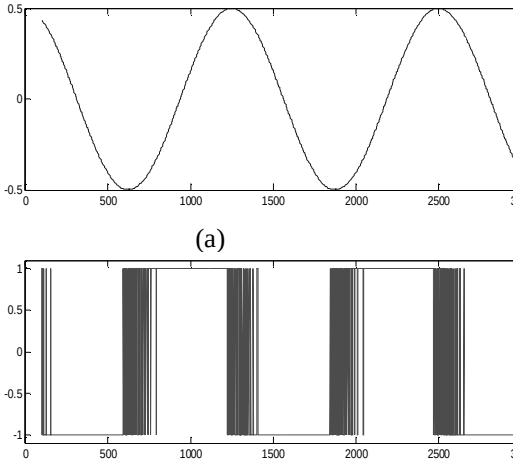
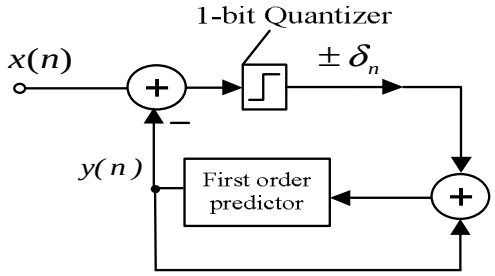
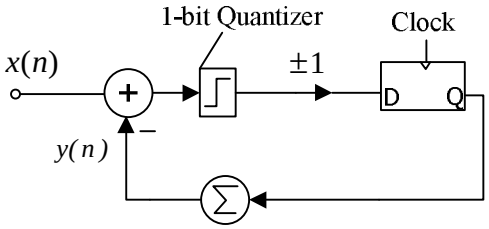


Figure 4.5 The Digitized Phase Error Output of Figure 4.3: (a) Input Data Phase and (b) Phase Comparator Output

As stated in [1], the bang-bang CDR can be treated as a special case of a sigma-delta modulator (ΣΔM); more strictly, it should be treated as a delta modulator (DM). In [55] it is shown that the bang-bang CDR loop is very similar to a classic speech delta modulation system. According to the schematic shown in Figure 4. 3, the phase error is quantized by two levels ($\pm\delta_n$) and the phase error is predicted through a backward feedback loop to keep track of the input jitter. In the topology shown in Figure 4.6 (a), the input signal is firstly quantized into two levels, and then sent back to the input through a signal predictor, which is an integrator in Figure 4.6(b). The feedback loop forces the predictor output y(n) to track the input x(n) closely.



(a)



(b)

Figure 4.6. Delta Modulator: (a) Standard Delta Modulation Diagram (Similar to DPCM) and (b) An Implementation of DM Encoder

The concept of first order predictor can be extended to higher order; in Figure 4.7 and 4.8 an adaptive bang-bang CDR diagram for 1st and 2nd order CDR, respectively, are presented. Actual and previous values of the quantized phase error are used to control the bang-bang attenuating factor α, such that the loop bandwidth can then be dynamically adjusted according to the phase variations of the input data.

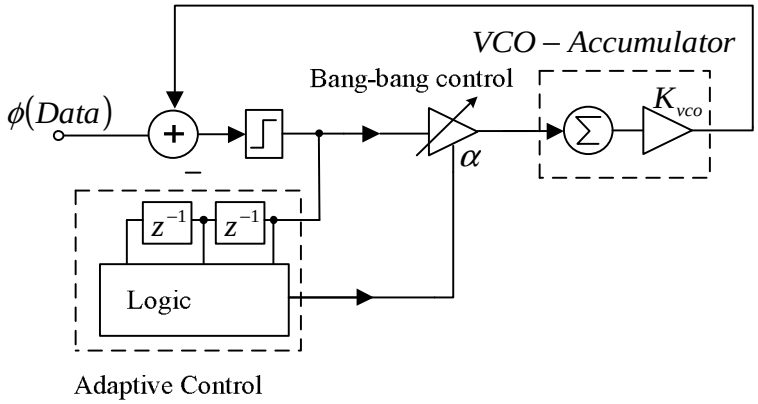


Figure 4.7 1st Order Binary CDR with Adaptive Control

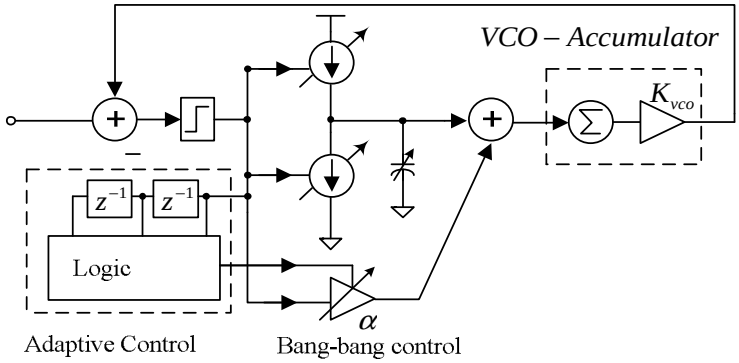


Figure 4.8 2nd Order Binary CDR with Adaptive Bang-bang Control

In order to use adaptive delta modulation (ADM) scheme in our CDR system, the architecture of ADM should be addressed first. In [54], a constant factor adaptive delta modulation with a one-bit memory is proposed. Denoting the quantizer output as *b(n)*, and its previous memory is *b(n-1)*, and defining the current quantization step size as $\delta(n)$, and its previous step size is $\delta(n-1)$ then

$$\delta(n)=\begin{cases} M_1\delta(n-1) & if \;\; b(n) = b(n-1) \\ M_2\delta(n-1) & if \;\; b(n) \neq b(n-1) \end{cases} \tag{4.8}$$

where M1 and M2 are the step sizes of the quantizer.

In the proposed implementation, two bits of memory of the phase error are adopted for robust slope overload prediction, which is similar to the approach suggested in [56]-[57]. The phase error output generates four different results: when successive three or more bits of the same level (high or low) are output from the phase detector, the condition is defined as slope overload; if two consecutive phase outputs have the same level, and differ from the foremost history, this is classified as a semi-overload condition; while both the previous output and the foremost memory differ from the current phase detector output, the condition is classified as sign reversal; when the current output and previous two output alternate polarity, we denote this condition as "alternate polarity". These conditions are mathematically described as follows:

$$\delta(n)=\begin{cases} M_1\delta(n-1) & if \;\; b(n) = b(n-1) = b(n-2); \\ M_2\delta(n-1) & if \;\; b(n) = b(n-1) \neq b(n-2); \\ M_3\delta(n-1) & if \;\; b(n) \neq b(n-1) = b(n-2); \\ M_4\delta(n-1) & if \;\; b(n) \neq b(n-1) \neq b(n-2); \end{cases} \tag{4.9}$$

For this implementation, M_1 is selected as 2.0, M_2 is 1.5, and M3 is 0.5, while M_4 is 0.75 for easy installation of the current source arrays. $M_1 = 2.0$ can be realized by using logic left-shift one bit (<< 1); M_3 thus can be right-shifted by 1 bit (>>1); and M_2 is the sum of left-shift 1 bit and right-shift 1 bit; M_4 is the sum of right-shift 1 bit and right shift 2bits of the operands.

IV.3.2. Circuit Implementation of the Adaptive Bang-bang Control

Table IV.1 shows the adaptive control of the frequency step size. *B(n)* is the actual phase detector output, and *B(n-1)* and *B(n-2)* are one and two cycle delays of the B(n). Figure 4.9a shows an implementation of the state machine of adaptive bang-bang control. The state is described as *S[1:0]*, which corresponds to the two bits of *B(n-1)* and *B(n-2)*; there are four possible states "00","01","10" and "11". The output of the Mealy state machine is separated with the incoming bit by a slash "/", for example, "0/11", the incoming bit is "0", the output is "11". The step size of the bang-bang control can be represented as:

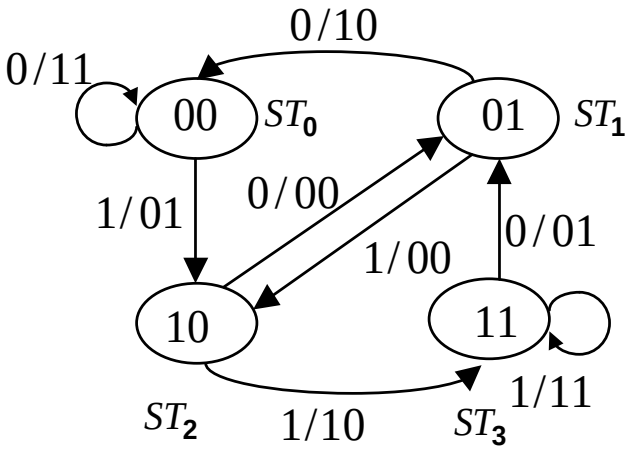
$$\left\{\begin{array}{l} Step\_size[1] = \overline{B(n) \oplus B(n-1)}; \\ Step\_size[0] = \overline{B(n-1) \oplus B(n-2)} \end{array}\right\} \tag{4.10}$$

where $\oplus$ denotes XOR logic function, and $\overline{output}$ denotes logic inversion. The adaptive logic diagram is depicted in Figure 4. 9b.

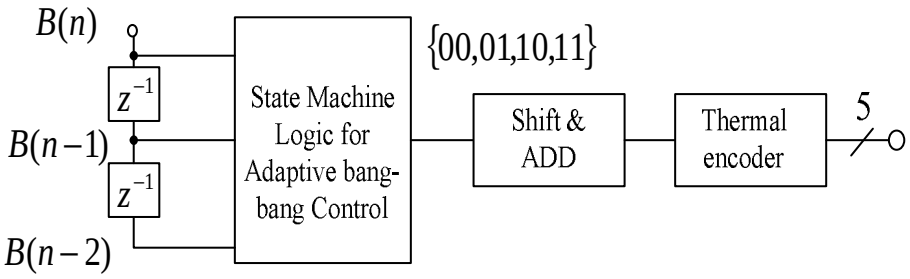
As a reference design, a variable gain amplifier design with source degeneration, shown in Figure 4.10, can be used as the bang-bang control block (denoted as α) in Figure 4.7 and Figure 4. 8.

TABLE IV.1.STEP SIZE ADJUSTMENT FOR THE PROPOSED CDR

B(n)	B(n-1)	B(n-2)	State	Step size
-1	1	-1	Alternate polarity	0.75
1	-1	1	Alternate polarity	0.75
-1	1	1	Sign reversal	0.5
1	-1	-1	Sign reversal	0.5
-1	-1	1	Semi-overload	1.5
1	1	-1	Semi-overload	1.5
-1	-1	-1	Overload	2
1	1	1	Overload	2



(a)



(b)

Figure 4.9 Bang-bang Control Implementation: (a) State Diagram of the Adaptive Bang-bang Control, (b) Adaptive Control Logic Diagram

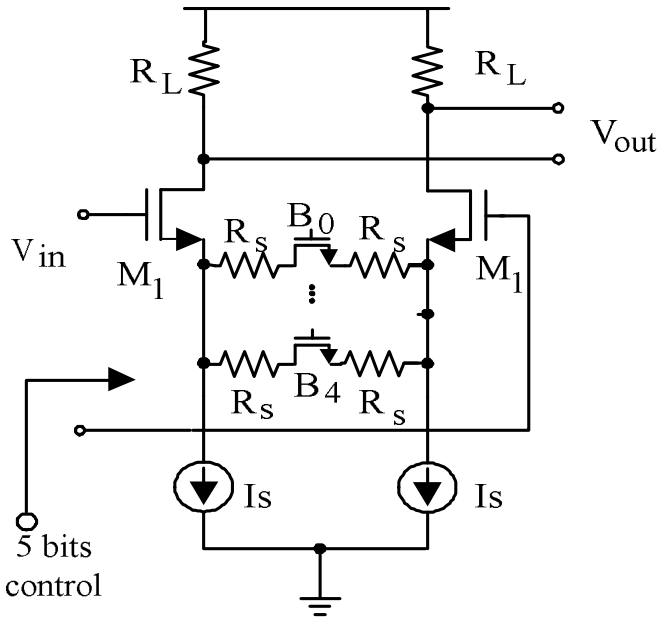


Figure 4.10 Variable Gain Amplifier Using Source Degeneration

IV.4. Performance Comparison: A Statistical Approach

In this section, we will derive the steady state probability of the adaptive CDR comparing with that of classical BB CDR using Markov chain modeling and statistical analysis.

The discussion of a Markov chain can be found in [58]. In general, a Markov chain is a sequence of random variables *X1,X2,X3*… with the Markov property, namely that, given the present state, the future and past states are independent[59]. Formally, the conditional probability is defined as the probability of some event, given the occurrence

of some other state such as X_n, written as. In Figure 4. 8, the bang-bang control is in essence a finite state machine. If the machine is in state *STn* at time n, then the probability that it moves to state *STn+1* at time *n+1* depends only on the current state. Thus the state machine can be explained using a Markov chain. Simply we have:

$$\Pr\left(ST_{n+1} = x \middle| ST_{n} = x_n, .., ST_1 = x_1\right) = \Pr\left(ST_{n+1} = x \middle| ST_n = x_n\right) \tag{4.11}$$

where x and x_n are the possible values of variable ST_n.

The possible values of ST_n from a countable set S called the state space of the chain. In our analysis, because for each state change in the state machine, the phase of the recovered clock changes accordingly, it is reasonable that the possible phases of the recovered clocks are modeled as a Markov chain, with a state space $\{\phi_n\}$, as shown in Figure 4. 11[60]. The transition between the states governed by the up and down decisions to hold, advance or retreat the current phase. Now let's assume that p_{ij} is the single step transition probability from state ϕ_i to ϕ_j, which is defined in (14):

$$p_{ij} = pr\left(\phi_{k+1} = \phi_j \middle| \phi_k = \phi_i\right) \tag{4.12}$$

Once we know all the transition probabilities for each of the phase states, a Markov transition matrix T can be formed and be used to calculate the steady-state phase probabilities by looking either at the eigenvalues of the transition matrix or solving for transitions iteratively [58].

$$\Pr_{n+1}^{\phi} = T \cdot \Pr_{n}^{\phi} \tag{4.13}$$

$$T = \begin{bmatrix} p_{0,00}\, p_{0,01} \cdots\cdots\cdots\cdots\cdots\cdots & 0 \\ p_{1,10}\ p_{1,00}\ p_{1,01} & 0 \\ 0 \quad p_{2,10}\ p_{2,00}\ p_{2,01} & 0 \\ \vdots \qquad\qquad p_{n,00}\ p_{n,01} & \\ 0 \qquad \cdots \quad \cdots\ P_{N,10}\ p_{N,00} & \end{bmatrix} \tag{4.14}$$

where $p_{n,00}$ means the probability of hold state, $p_{n,01}$ the probability of transition from ϕ_n to ϕ_{n+1}, $p_{n,10}$ the probability of transition from ϕ_n to ϕ_{n-1}. Using (4.15) and (4.16), the steady state of the possible recovered clock phases can be estimated in a statistical manner. The basic theory for the previous statement is that, the steady state distribution will converge to a state denoted as Π which is a row vector. Thus we have:

$$\Pi = \Pi P \tag{4.15}$$

In general, if the markov chain is irreducible and aperiodic, there is a unique stationary distribution of Π, namely,

$$\lim_{k\to\infty} P^k = E\Pi \tag{4.16}$$

where E is the column vector with all entries equal to 1. This means that as time goes by, the Markov chain converges to a steady state distribution in spite of its initial distribution [58].

With all these setups, the probabilities of up, down, and hold in the phase detector of the CDR can be calculated using behavior modeling tools such as Matlab.The transition probabilities of proposed adaptive CDR are shown in Figure 4.12, with the raw input probabilities (p-early, p-late, p-novalid) in the PD output of classical BB CDR. Notice in

these results that the proposed adaptive CDR has a higher probability of detection than that of the classic BB CDR.

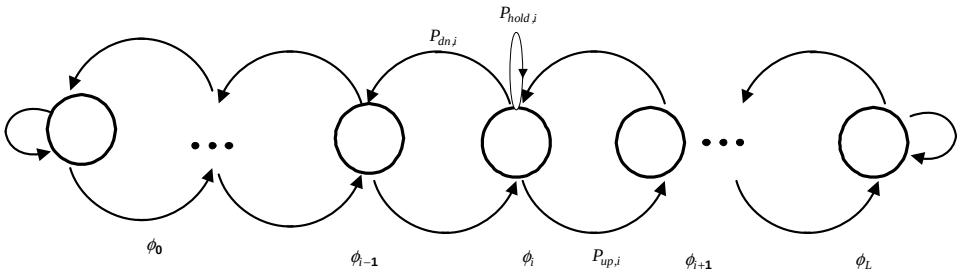


Figure 4.11 1st Order Markov Chain Phase-state Model

Since the proposed CDR presents an adaptive frequency (phase) update step, for some states and some transition probability values, it is necessary to jump a few states rather than just going to the neighboring state. However, it is practical to make the phase states in much smaller steps than the classical BB CDR, actually for adaptive CDR, the VCO frequency is varied in smaller steps than a BB-CDR to keep track of larger frequency deviation in the incoming data.

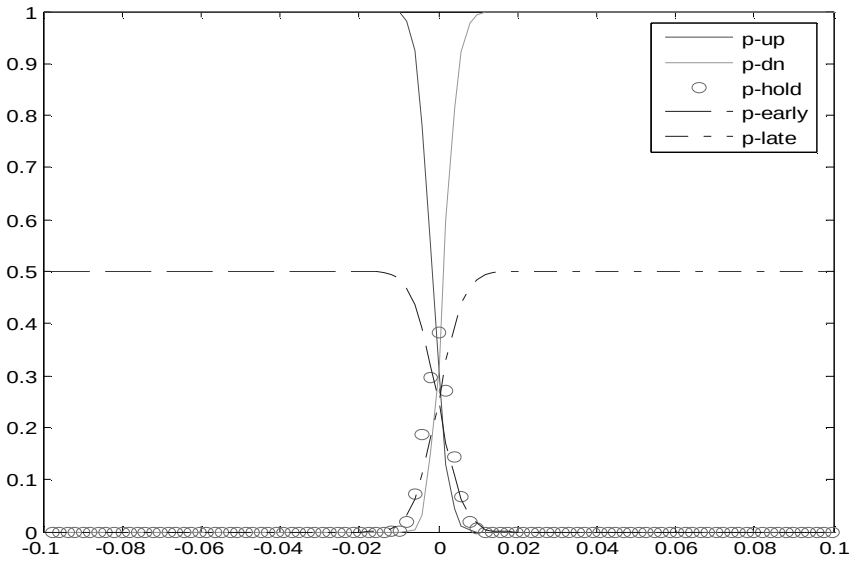


Figure 4.12 The Probabilities of Up, Down and Hold Signal in Proposed CDR

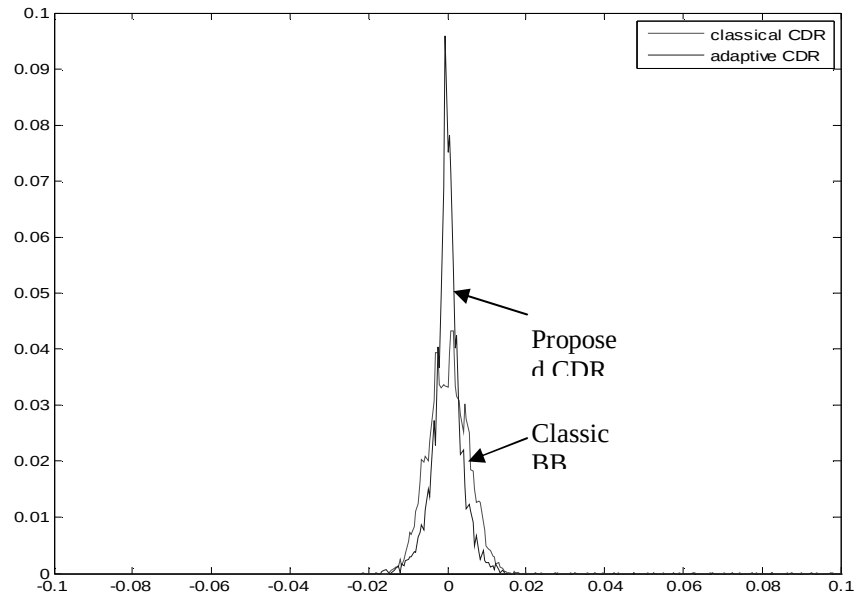


Figure 4.13. Comparison of the Steady State Phase Probabilities for the Transition Probabilities

The steady state probability of the possible phases of the recovered clock for proposed CDR and conventional CDR are shown in Figure 4.13 and Figure 4.14, where the X-axis is the possible CLK phase in UI.

The RMS jitter of the recovered clock can be estimated from the probability distribution of the phases of the recovered clock. Thus the statistical analysis of the steady state phase of the CDR will converge to the long-term jitter histogram of the recovered clock. Notice in these results that the proposed CDR has better statistical performance compared with the conventional BB-CDR architecture.

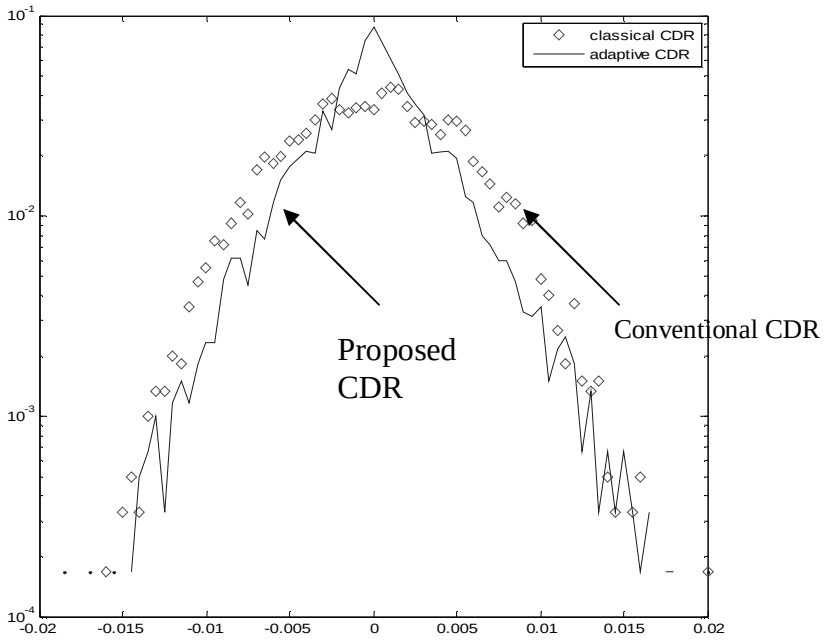


Figure 4.14 The Logarithmic Plot of the Steady State Probabilities of Proposed and Classic BB CDR

IV.5. Simulation Results

In the following experiment, a PRBS (pseudo-random bitstream) generator outputs data pattern and the data is passed to a 5Gb/s CDR block which extracts the clock from the incoming data. In this paper, only a bit error rate (BER) of 1e-4 is simulated for the tradeoff of computing time.

The jitter measurement through sinusoidal jitter modulation in the input data is the toughest in jitter tolerance test, and adopted in all of the Serial PHY standard such as Gigabit Ethernet, SONET, PCI Express (PCIe) , SATA and Fiber Channel. For a typical sinusoidal modulation jitter addition, we have:

$$\phi_{SJ} = A_{SJ} \sin\left(2\pi f_m t + \phi_0\right) \tag{4.17}$$

where f_m and ϕ_0 are sinusoidal modulation frequency and initial sinusoidal jitter phase, respectively; A_{SJ} is the sinusoidal phase modulation amplitude in rad/s, which can also be measured in Unit intervals (UI). Since one UI corresponds to 2π, in our simulation, the phase error jitter is measured in time units instead of rad/s, i.e, the recovered clock phase has peak to peak deviation

$$\phi_{pk\_pk,SJ} = 2\pi\, J_{pk\_pk,SJ} \,/\, T_{bit} \tag{4.18}$$

where $J_{pk\text{-}pk,SJ}$ is the phase error jitter of the recovered clock in time unit; and T_{bit} is the period of the input data pattern.

IV.5.1. Phase Tracking with 6MHz Sinusoidal Jitter Modulation (1st Order BB CDR)

All the experiments of 1st order BB CDR are performed with the data and clock frequency deviation of 150ppm. For the 1st order BB CDR, the phase error tracking of 6MHz sinusoidal jitter is shown in Figure 4.15. The conventional BB CDR has an equivalent bandwidth of 4.5MHz, while the adaptive has a steady state bandwidth of 2MHz. The phase error jitter[5] for the adaptive CDR is 13.3ps peak to peak versus that of 22.4ps pk-to-pk in the conventional BB CDR.

Notice that in Figure 4.15, δf , frequency difference between data and clock, is 150ppm. The waveform in (a) shows that the phase tracking of adaptive CDR is better than of that in the classical BB CDR in (c).

IV.5.2. Phase Tracking with 2MHz Sinusoidal Jitter Modulation

In Figure 4.16, an initial frequency difference between data and clock is set to 150ppm for simulation. The traces from the top to the bottom are: (a) phase tracking of conventional BB CDR; (b) phase tracking error of classical CDR; (c) phase tracking of adaptive BB CDR; (d) phase error of 2MHZ SJ in adaptive BB CDR;(e) phase tracking error comparison between adaptive BB CDR and conventional CDR. The conventional BB CDR has an equivalent bandwidth of 4.5MHz, while the adaptive has a steady state

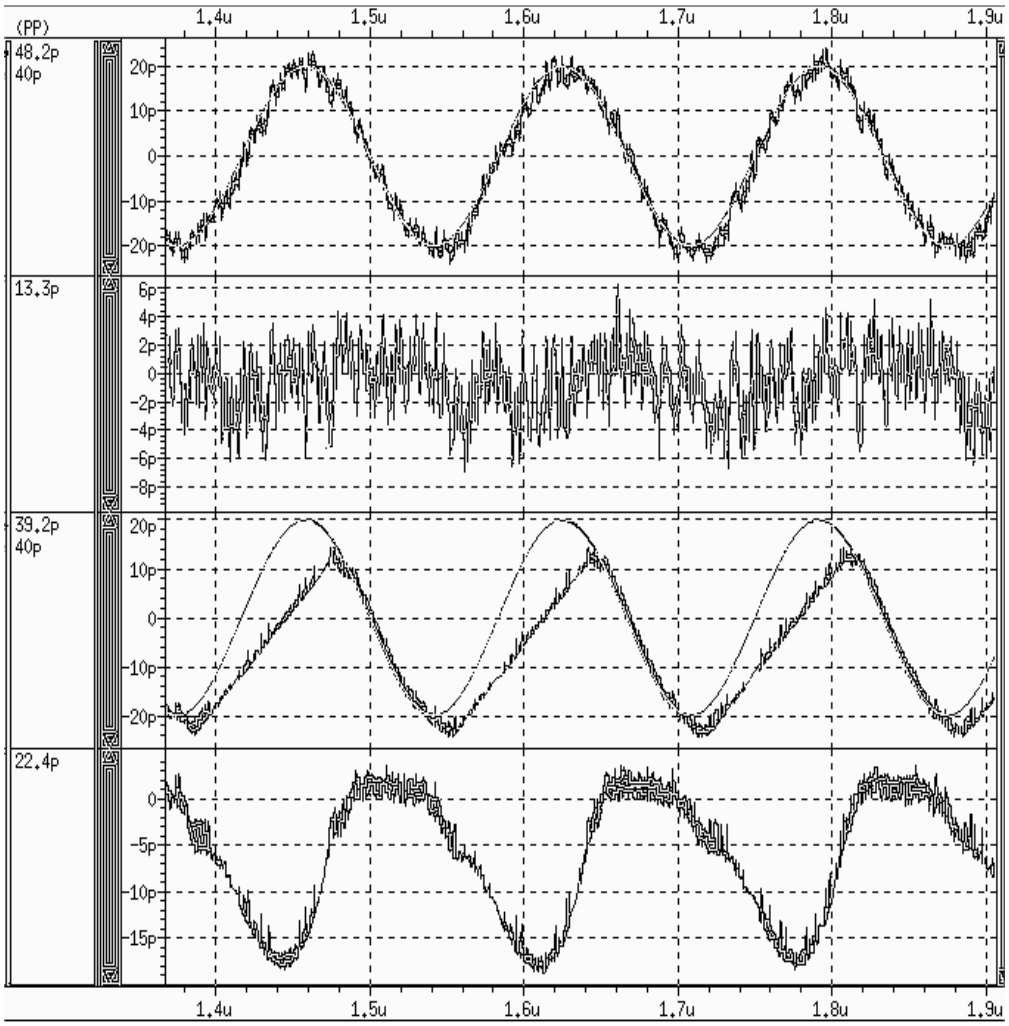
[5] The phase error jitter is defined not as the rad/s, but the orginal phase error divided by 2, which is in unit interval, then it is multiplied by clock period which is measured in seconds.

bandwidth of 2MHz. The phase error jitter[6] for the adaptive CDR is 11.7ps peak to peak versus that of 20.4ps pk-to-pk in the conventional BB CDR.

IV.5.3. Phase Tracking with 6MHz Sinusoidal Jitter Modulation for a 2nd Order CDR

The following experiments for a 2nd order CDR were done with the data and clock frequency deviation of 300ppm. Simulations for conventional second order BB-CDRs configured with a steady state loop bandwidth of factors one (x1) and three times(x3) the equivalent bandwidth of the adaptive CDR were carried out. Figure 4.17 shows the phase error tracking for a second order CDR which is configured x1 and x3 of equivalent bandwidth of an adaptive CDR. The phase error for the 1x conventional CDR is 19.8ps pk-pk versus 12ps pk-pk of the x3 bandwidth configuration, while the adaptive CDR presented a phase error of 11.3ps pk-pk. The adaptive CDR outperformed the x3 conventional CDR. Furthermore, as aforementioned, very large CDR bandwidth may cause large phase errors when tracking low speed frequency jitter, making very difficult the selection of the correct bandwidth unless the frequency of the sinusoidal jitter can be accurately predicted. The adaptive CDR can achieve significant jitter optimization and better jitter tolerance as tabulated in Table IV.2. For these results, 2^{15}-1 PRBS pattern with frequency variation of 300ppm, and 0.15UI ISI distortion were used.

[6] The phase error jitter is defined not as the rad/s, but the orginal phase error divided by 2, which is in unit interval, then it is multiplied by clock period which is measured in seconds.



(a)

(b)

(c)

(d)

Figure 4.15 Phase Tracking of 1st Order BB CDR with 6MHz Sinusoidal Jitter: (a) Phase Tracking of the Adaptive BB CDR, (b) Phase Tracking Error of the Adaptive BB CDR, (c) Phase Tracking of the Classical BB CDR, and (d) Phase Tracking Error of the Classical BB CDR

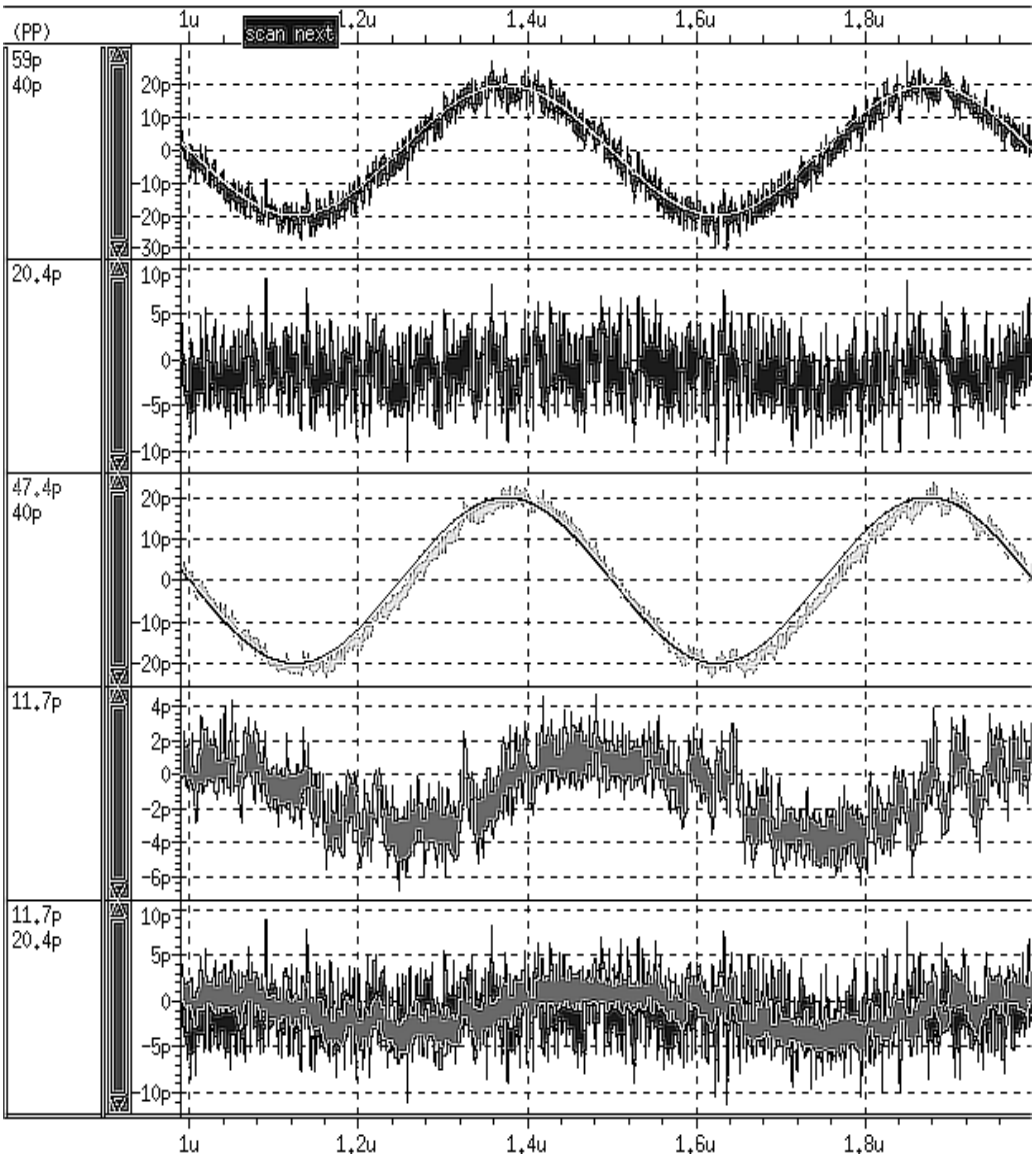


Figure 4.16 Comparison of Phase Tracking between 1st Order Conventional and Adaptive BB CDR: (a) Phase Tracking of Conventional BB CDR, (b) Phase Tracking Error of Classical CDR, (c) Phase Tracking of Adaptive BB CDR, (d) Phase Error of 2MHZ SJ in Adaptive BB CDR and (e) Phase Tracking Error Comparison between Adaptive BB CDR and Conventional CDR

TABLE IV.2: SUMMARY OF SIMULATION RESULTS

Technology	x1 BB CDR	x3 BB CDR	Adaptive CDR
Input data rate (Gb/s)	5	5	5
Equivalent BW	7MHz	9MHz	4MHz
Extracted sinusoidal pk-pk jitter(ps) to track 6MHz SJ with 0.32UIpp	49.4	45.4	44.4
pk-pk phase error (ps) to track 6MHz SJ with 0.32UIpp	19.2	12	12
pk-pk phase error (ps) to track 3MHz SJ with 0.32UIpp	10.8	10.8	10.4

Figure 4.18 shows the simulation of the phase tracking of the adaptive and conventional Bang-bang CDRs with input sinusoidal jitter amplitude of 0.34UIpp, at a frequency of 6MHz. The steady state bandwidth of the conventional CDR (6MHz) is 3x that of adaptive CDR (BW=2MHz). Theoretically, under steady state, the conventional BB-CDR with BW=6MHz should track the sinusoidal jitter much better due to its inherent larger bandwidth; however, simulation results show that the jitter tracking performance of the adaptive CDR is better mainly because the bandwidth adjusting mechanism. The adaptive CDR achieves a peak-to-peak phase error of 11.4ps while the conventional CDR achieves 19.2ps.

For lower frequency sinusoidal jitter input both CDRs can track the sinusoidal jitter since there is no slew rate limiting process in the tracing. Figure 4.18 confirms that both architectures achieve similar phase error when tracking 3MHz sinusoidal jitter. In spite of the advantage of the adaptive CDR, increasing the steady state equivalent bandwidth of the conventional CDR, both topologies achieve good phase tracking performance. In some cases it is unnecessary to perform the adaptive CDR but it is critical to consider the following issues: i) as aforementioned, very large CDR bandwidth will cause large phase error when tracking low speed frequency jitter; ii) it is not easy to predict which kind of jitter is present at the input of the system; iii) some standards such as the typical Gigabit Ethernet / SONET OC-192 require a 3dB bandwidth of only 120KHz, and a bandwidth of several MHz will have to be either shaped by a transmitter with a narrower bandwidth, or a digital FIFO and a bandwidth re-shaping PLL can be used to achieve such a stringent and narrow bandwidth [11]. The incoming jitter is often unexpected; hence it is difficult to define the optimal steady-state loop bandwidth. The beauty of the adaptive CDR architecture is that, based on phase estimation, it adapts the loop bandwidth for the best possible jitter tracking performance.

In Figure 4.18, the sinusoidal jitter (SJ) frequency is 6M Hz, the jitter amplitude is 0.32UIpk-pk; frequency difference between data and clock is 300ppm.From the simulation results, the adaptive CDR has better phase tracking performance comparing with the classical BB CDR design.

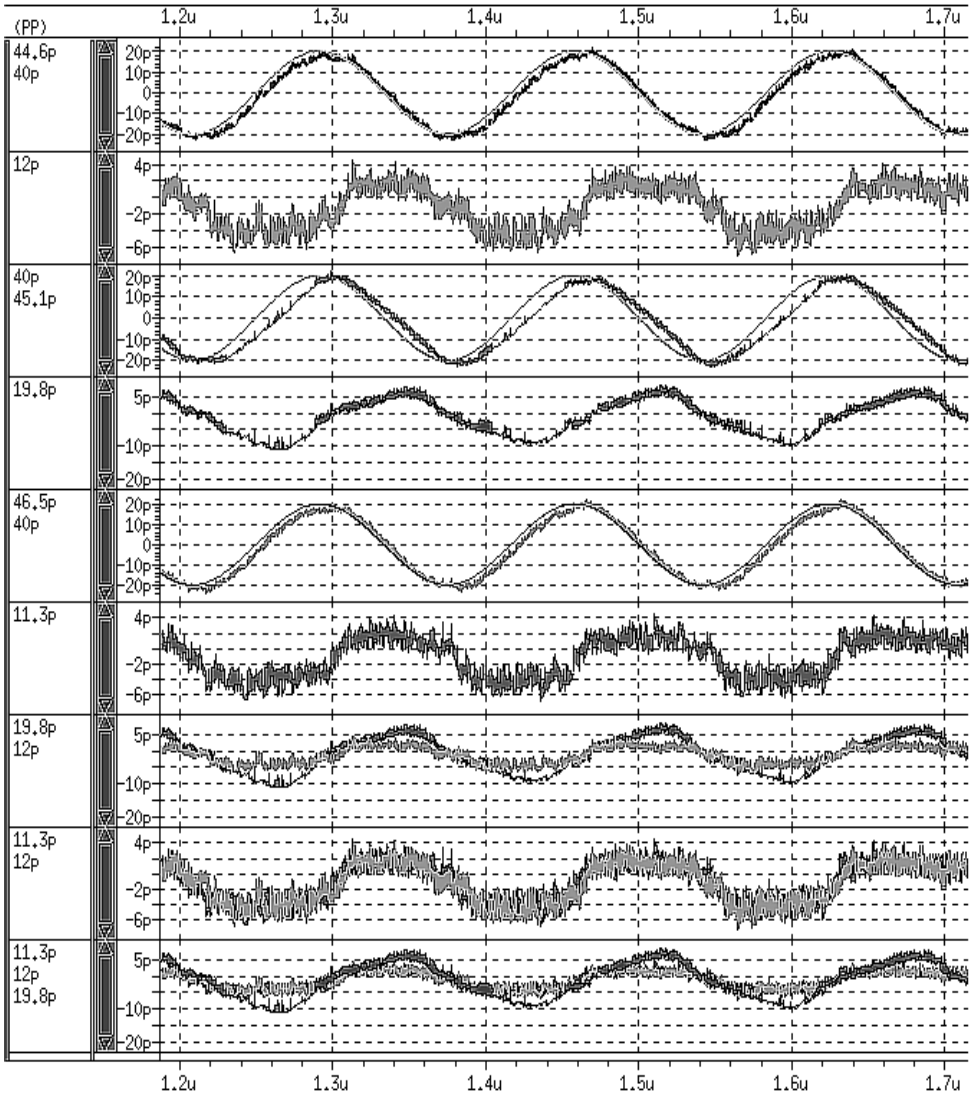


Figure 4.17 Phase Comparison of x1, x3 2nd Order , BB CDR and 2nd Order Adaptive BB CDR, Frequency Difference Is 300ppm: (a) Phase Tracking of Adaptive BB CDR, (b) Phase Tracking Error of Adaptive BB CDR, (c) Phase Tracking of Conventional BB CDR(x1 bandwidth), (d) Phase Tracking Error of Classical BB CDR(x1 BW), (e) Phase Tracking of Conventional BB CDR(x3 BW),(f) Phase Tracking Error of Conventional BB CDR(x3), (g) Comparison of CDR(x1BW) vs. BB CDR(x3), (h) Comparison of BBCDR(x3) vs. Adaptive BB CDR; and (i) The Comparison of CDR(x1),CDR(x3) and Adaptive CDR

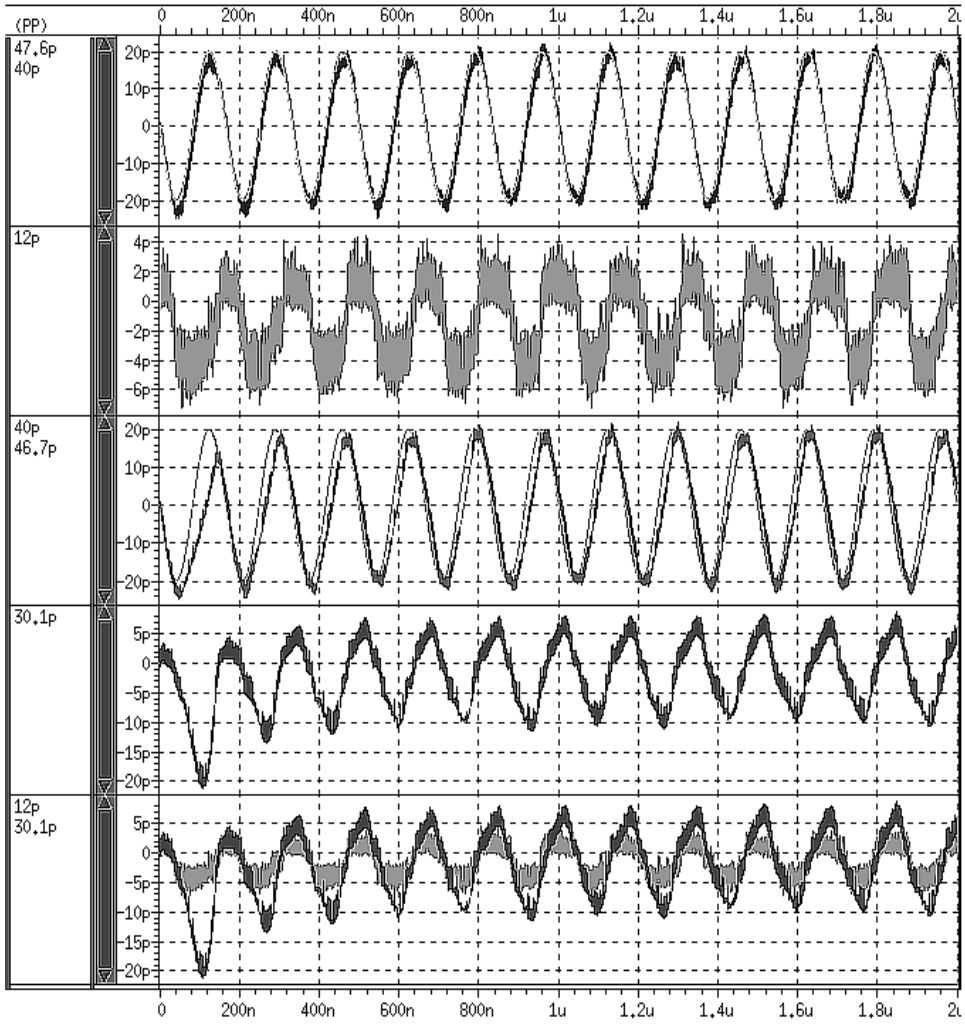


Figure 4.18 Comparison of Phase Error Tracking of Adaptive Bang-bang CDR and Classical Bang-bang CDR: (a) Adaptive Phase Error Tracking, (b) Phase Error in Adaptive Bang-bang CDR, (c) Classic Bang-bang Phase Error Tracking(Slew Rate Limiting), (d) Classic BB CDR Phase Error Tracking, and (e) Phase Error Comparison

IV.6. Conclusions

A CDR with adaptive bang-bang control and hence adaptive bandwidth control has been proposed. This architecture can be used in many applications such as PCIe, SATA and Fiber channel for the chip-to-chip interface where jitter peaking requirements are relaxed (3dB at a maximum). For stringent standards such as Gigabit Ethernet or SONET OC-192, the adaptive BB-CDR outperforms the conventional BB-CDR due to its phase dependent loop bandwidth, which leads to superior jitter tolerance performance. Theoretical analysis, in good agreement with extensive simulations, supports the foundations of the proposed architecture. This architecture can also be used in DLL/phase interpolator based digital CDRs by varying the digital loop filter.

V. CONCLUSIONS

In this dissertation, two clock data recovery integrated circuits architecture used for telecommunication or data communication systems have been discussed.

Firstly, a fully integrated 10-Gb/s CDR is implemented in a 0.18μm CMOS process. The design uses half rate architecture due to the relative low f_t (50GHz) of the CMOS process used. By using a new loop filter and charge pump configuration, the chip integrates all the components on-chip including the integration loop filter capacitor. Improved charge pump architecture with source degeneration, VCO with amplitude tuning and multiplexer scheme in double edged DFFs are the other techniques adopted to enhance the chip performance. The CDR device can recover data with a BER less than 10^{-12} when the input eye closure is slightly above $0.5UI_{pp}$(Horizontal eye closure) and the recovered clock with peak to peak jitter less than $0.1UI_{pp}$.The CDR also exceeds the OC-192 jitter tolerance mask with high frequency jitter tolerance over $0.31UI_{pp}$. To the best our knowledge, this reported implementation is the first fully integrated, PLL based 10Gb/s CDR in the literature.

Secondly, in a real world telecommunication or data communication application, the jitter frequency is not known in advance, a CDR with too large or too low bandwidth can not track the jitter in an optimal way, thus a CDR with adaptive bang-bang control and hence adaptive bandwidth control has been proposed. This architecture can be used in many applications such as PCIe, SATA and Fiber channel for the chip-to-chip interface where jitter peaking requirements are relaxed (3dB at a maximum). For

stringent standard such as Gigabit Ethernet or SONET OC-192, the adaptive BB-CDR outperforms the conventional BB-CDR due to its phase dependent loop bandwidth, which leads to a superior jitter tolerance performance. Theoretical analysis, in good agreement with extensive simulations, supports the foundations of the proposed architecture. This architecture can also be used in DLL/phase interpolator based digital CDRs by configuring the digital loop filter easily.

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APPENDIX A

LOOP DYNAMICS OF THE CDR LOOP

In this dissertation, the CDR is based on charge pump PLL configuration. The CDR diagram is represented in Figure A.1, the K_{pd} is the gain of the combined phase detector and charge pump in Figure 2.1. F(s) is the loop filter, and K_{vco}/S is the representation of the VCO used in the CDR loop.

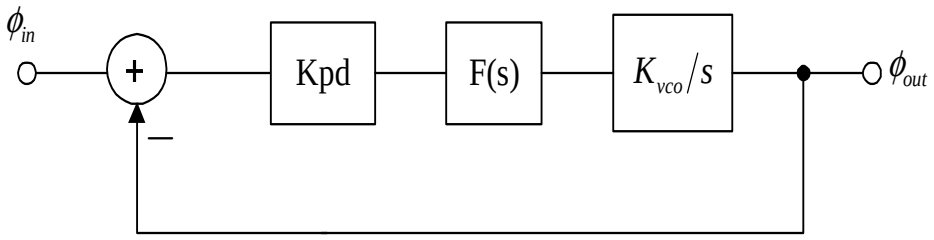

Figure A.1 Phase Diagram of a Typical CDR loop

Now neglect the parallel capacitor C_2 in Figure 2.1, the loop filter can be represented in the laplace s-domain as

$$F(s) = R_1 + \frac{1}{sC_1} = R_1 \frac{s + 1/(R_1C_1)}{s} \tag{A.1}$$

The phase(jitter) transfer function from φ_{in} to φ_{out} can be obtained as [2]

$$H(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = \frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \tag{A.2}$$

where $\xi = 0.5\sqrt{K/\omega_2}$, $\omega_n = \sqrt{K\omega_2}$, $K = K_{pd}K_{vco}R_1$, $\omega_2 = (R_1C_1)^{-1}$ .The jitter peaking can be derived by find the maximum of the magnitude of the *H(s=jω)*, namely,

by solving $\frac{d}{d\omega}\left(\left|H(j\omega)\right|^2\right)=0$, the peaking value is solved as

$$\begin{aligned} JP &= \left[1-2\alpha-2\alpha^2+2\alpha\left(2\alpha+\alpha^2\right)^{1/2}\right]^{-1/2} \quad \textit{where } \alpha=\omega_2/K \\ &\cong 1+\frac{\omega_2}{K} \quad \textit{when } \omega_2<0.1K \end{aligned} \tag{A.3}$$

The jitter tolerance describes how much input jitter a CDR must tolerate without increasing the bit error rate, and it is determined by [21]

$$\begin{aligned} JTOL(s) &= \frac{0.5}{1-H(s)}=\frac{1}{2}\frac{s^2+2\xi\omega_n s+\omega_n^2}{s^2} \\ &\cong \frac{1}{2}\frac{s+2\xi\omega_n}{s} \quad \textit{as } s\to\infty \end{aligned} \tag{A.4}$$

An example of jitter transfer curve is shown in Figure A.2, the peaking increases with the increase of ω_2/K. The jitter tolerance curve is shown in Figure A.3.

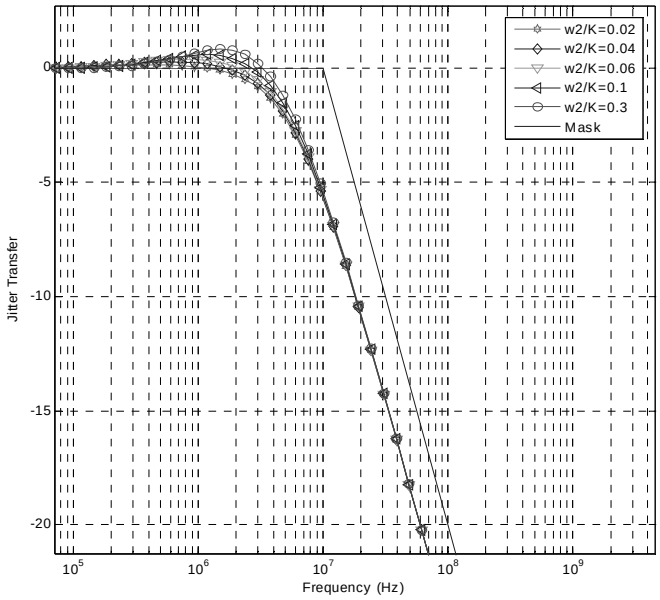

Figure A.2 Jitter Transfer curve for a CDR with a Bandwidth of 6MHz

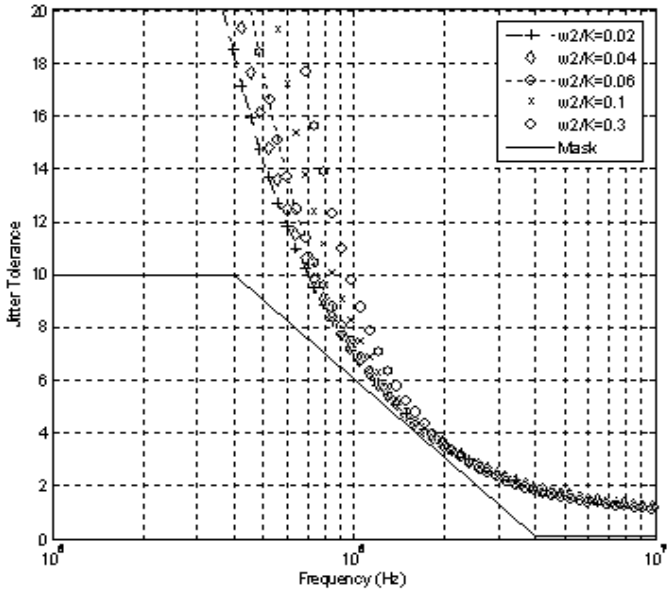

Figure A.3 Jitter Tolerance Curve for a CDR with a Jitter Transfer Curve of Figure A.2

APPENDIX B

COARSE FREQUENCY TUNING CIRCUIT IN THE CDR

The coarse frequency tuning circuit is composed of the output range detector of the loop filter output and SAR control logic, as shown in Figure B.1. In the output range detector of the loop filter, the VCO tuning voltage Vc is compared with two reference voltages, Vref+ and Vref-. The outputs of the two comparators cmp_H and cmp_L represent whether the loop filter voltage is out of range or not [21]. The operation principle is shown in Table B.1. Basically, when $V_c > V_{ref+}$, which means the VCO is not slow enough, thus more variable capacitance should be placed in the LC tank; when $V_c < V_{ref-}$, the VCO needs to speed up such that Vc doesn't reduce further.

The SAR control logic works as follows, after the start pulse is asserted low, the shift registers output the sequence of pulses, q<5:0>. Shown in Figure B.2, the SAR output q<5> first outputs a '1', and the capacitor array control bit C<5> is also '1'; when the range detector output cmp is '1'; then q<4> and q<3> output '1', and C<4> and C<3> are both set to '1's as the cmp still keeps high; then when the range detector outputs '0', thus C<2> is set to '0', etc. Besides the automatic SAR control, the capacitor bank can also be set manually by pull p<5:0> control bits to low to add more capacitor arrays.

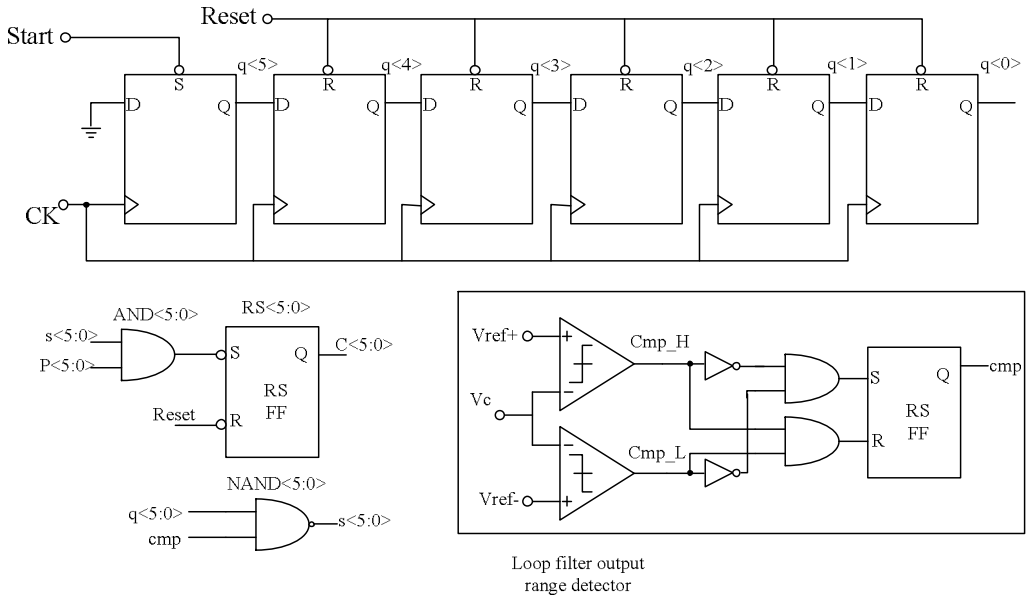

Figure B.1 Coarse Frequency Tuning Circuit

TABLE B.1 Principle of the voltage range detector of loop filter output

Cmp_H	Cmp_L	Operation
0	0	Vc> Vref+, Vc>Vref-; Increase capacitance
0	1	Vc>Vref+, Vc<Vref-; Reset the range detector
1	0	Vref-<Vc<Vref; No operation
1	1	Vc<Vref+, Vc<Vref-; Reduce the capacitance

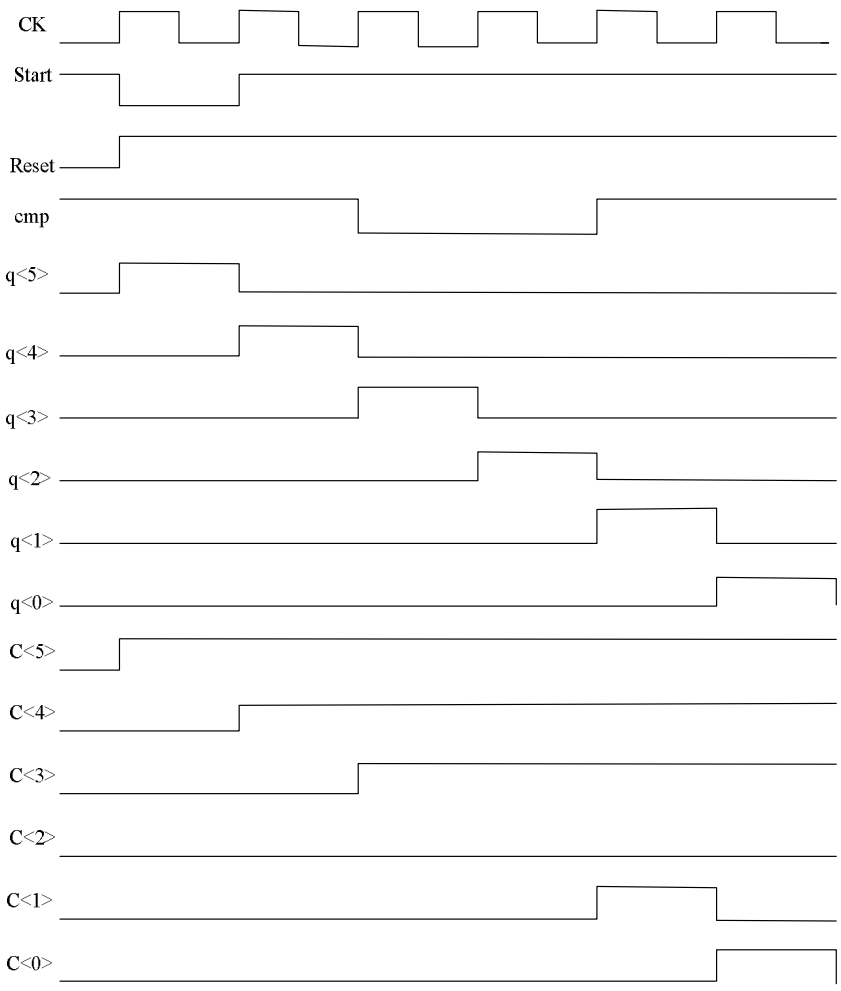

Figure B.2 Timing Diagram of the Coarse Frequency Tuning Circuit

APPENDIX C

DETERMINATION OF THE BANDWIDTH OF THE BB-CDR

Unlike the linear systems, which can be studied through classical Laplace/Fourier transform in frequency domain, the binary phase detector based clock recovery architecture is a nonlinear system and the frequency response functions of nonlinear elements cannot be defined directly [53],[61],[62]. The binary CDR phase error converges to a limit cycle in a phase plane instead of settling to a relatively constant value as in the case of linear CDRs. Thus, it is mandatory to perform complete transient simulations. However, it is not very appropriate in the first stage of the design of a nonlinear system because one must wonder whether enough initial condition and input combinations are covered in the resultant system response. Although not accurate, the Describe Function (DF) gives a quasi-linear approximation representation of the nonlinearities by minimizing the mean-squared approximation error with sinusoidal or random inputs applied to the nonlinear element [63]. A convenient way to derive the DF is exciting the nonlinear system with a sinusoidal signal; the output of the non-linear device generally consists of the harmonics of the input sinusoidal signal[63]. Discarding all other frequency components except the one with the same frequency as the input, the ratio transfer function between that output component and the input signal defines the DF. As an example, the ideal comparator has the form $V_{out}=D*sgn(V_{in})$; when excited by a sinusoidal signal $V_{in} = A\sin(\omega t)$,its frequency equivalent is given by

$V_{out} = \frac{4D}{\pi}\sum_{1}^{\infty}\frac{\sin(n\omega t)}{n}$, where n is an odd number. Keeping only the fundamental tone, and dividing the output component by the input signal, we get $DF = 4D/\pi A$, which is inverse proportional to the amplitude of the input tone A. Thus it is easy to understand why the jitter transfer of a binary PD based CDR is inverse proportional to the input jitter amplitude. Even though the *DF* method is only an approximation, it is a good tool to predict limit cycles in nonlinear systems. However, due to its nonlinear nature, it is not surprising that the results are somewhat not accurate and further system simulations are needed to verify system functionality.

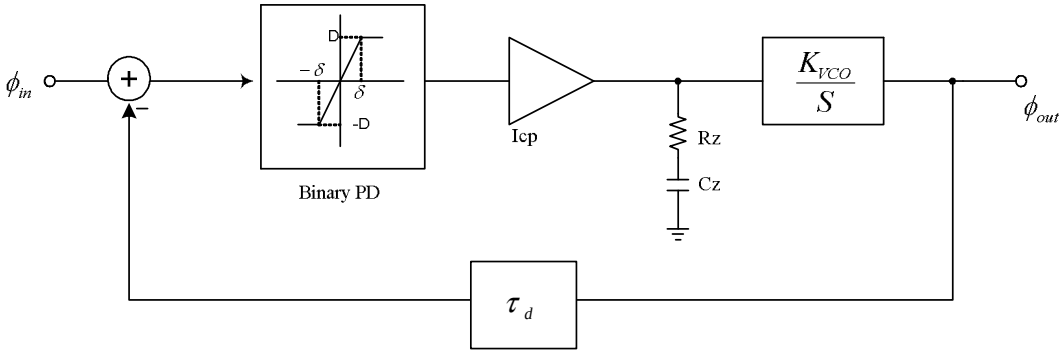

Figure C.1. Block Diagram of a Binary PD Based CDR

The limit cycle of the binary PD based clock recovery can be determined by analyzing its close-loop transfer function, namely the following equation:

$$1+N(A)L(j\omega)=0 \tag{C.1}$$

where *N(A)* is the describe function of the nonlinear binary phase detector whose characteristic is drawn in Figure C.1 ; *A* is the potential limit cycle amplitude and *L(jω)* is the Fourier transform of the linear part of the system; K_{VCO} is the gain of the VCO; I_{cp} is the charge pump current, and $\tau_z = R_Z C_Z$ is the time constant associated with the loop filter. T_d is the systematic loop delay. $L(\omega)$ can be derived from the linear part of the loop, see Figure C.1, as follows

$$L(s)=\frac{\tau_z s+1}{s^2 C_z} K_{VCO} I_{cp} e^{-s\tau_d} = \frac{K(\tau_z s+1)}{s^2} e^{-s\tau_d} \tag{C.2}$$

where $K = K_{VCO} I_{CP} / C_z$. The describing function for the non-linear phase detector can be mathematically model as

$$N(A)=\frac{D}{\delta} f\left(\frac{\delta}{A}\right) \tag{C.3}$$

where *A* is the amplitude of the input sinusoidal signal, $V_{in}(t) = A\sin(\omega t)$, and f is the following function [63]

$$f\left(\frac{\delta}{A}\right)=\frac{2}{\pi}\left[\sin^{-1}\left(\frac{\delta}{A}\right)+\frac{\delta}{A}\sqrt{1-\left(\frac{\delta}{A}\right)^2}\right] \tag{C.4}$$

The loop bandwidth limitation to guarantee loop stability can be obtained combining equations (C.1-C.3); the resulting expression is

$$\frac{K\left(j\omega_{LC}\tau_z+1\right)}{{\omega_{LC}}^2}e^{-j\omega_{LC}\tau_d}=\frac{\delta}{Df\left(\frac{\delta}{A}\right)} \tag{C.5}$$

In this expression ω_{LC} is the frequency at which (C.1) is satisfied. To satisfy (C.5), two conditions are required; for the magnitude we have

$$\frac{K}{{\omega_{LC}}^2}\sqrt{{\omega_{LC}}^2\tau_z^2+1}=\frac{\delta}{Df\left(\delta/A\right)} \tag{C.6}$$

Therefore, the potential limit cycle amplitude can be obtained as

$$A=\frac{\delta}{f^{-1}\left(\delta{\omega_{LC}}^2\Big/\left(DK\sqrt{{\omega_{LC}}^2\tau_z^2+1}\right)\right)} \tag{C.7}$$

where $f^{-1}(x)$ is the inverse function of $f(x)$; see expression (C.4). A second condition is associated with the phase of the left-hand side term of expression (C.5); thus, the following second condition arises

$$\tan^{-1}(\omega_{LC}\tau_z)-\omega_{LC}\tau_d = 2n\pi;\ \ n=0,\pm 1,\pm 2,... \tag{C.8}$$

From (C.8), and assuming that the $tan^{-1}(\omega_{LC}\tau_Z) \cong \omega_{LC}\tau_Z$ a simplified expression for the potential limit cycle frequency can be obtained

$$\omega_{LC} \cong \frac{2n\pi}{\tau_z - \tau_d} \tag{C.9}$$

It is worth mentioning that for a binary phase detector clock recovery system which uses first order loop filter, and assuming that $\tau_d=0$, the system will not show any limit cycle dynamics.

In a typical binary CDR system the systematic delay τ_d, due to phase detector delay and divider delay (if any), contributes to the limit cycle dynamics. Thus it is necessary to adopt the phase detector with less delay or delay immune phase detector to improve the system performance.

VITA

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He worked as an internship design engineer with Optical Transport Department, Agere Systems(now LSI Logic), Allentown, PA from June to December 2002. From June 1998 until June 2000, he was a Member of technical staff at Bell Labs(China), Lucent Technologies, working on single-chip HDTV design using 0.25um CMOS technology in Murray Hill, NJ, USA and Shanghai, China, respectively. His research interests include analog and mixed-signal circuit design for high speed serial link design. He can be reached at his email address of jinghuali@ieee.org, or through Dr. Jose Silva-Martinez, 318D, Wisenbaker Engineering Research Center, Analog and Mixed Signal Center, Department of Electrical Engineering, Texas A&M University, College Station, Texas 77843-3128, USA.