PASSIVE AND ACTIVE CIRCUITS IN CMOS TECHNOLOGY FOR RF,

MICROWAVE AND MILLIMETER WAVE APPLICATIONS

A Dissertation

by

MOHAN KRISHNA CHIRALA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2007

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Cam Nguyen
Committee Members,	Edgar Sánchez-Sinencio
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ABSTRACT

Passive and Active Circuits in CMOS Technology for RF, Microwave and Millimeter

Wave Applications. (December 2007)

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The permeation of CMOS technology to radio frequencies and beyond has fuelled an urgent need for a diverse array of passive and active circuits that address the challenges of rapidly emerging wireless applications. While traditional analog based design approaches satisfy some applications, the stringent requirements of newly emerging applications cannot necessarily be addressed by existing design ideas and compel designers to pursue alternatives. One such alternative, an amalgamation of microwave and analog design techniques, is pursued in this work.

A number of passive and active circuits have been designed using a combination of microwave and analog design techniques. For passives, the most crucial challenge to their CMOS implementation is identified as their large dimensions that are not compatible with CMOS technology. To address this issue, several design techniques – including multi-layered design and slow wave structures – are proposed and demonstrated through experimental results after being suitably tailored for CMOS technology. A number of novel passive structures - including a compact 10 GHz hairpin

resonator, a broadband, low loss 25-35 GHz Lange coupler, a 25-35 GHz thin film microstrip (TFMS) ring hybrid, an array of 0.8 nH and 0.4 nH multi-layered high self resonant frequency (SRF) inductors are proposed, designed and experimentally verified.

A number of active circuits are also designed and notable experimental results are presented. These include 3-10 GHz and DC-20 GHz distributed low noise amplifiers (LNA), a dual wideband Low noise amplifier and 15 GHz distributed voltage controlled oscillators (DVCO). Distributed amplifiers are identified as particularly effective in the development of wideband receiver front end sub-systems due to their gain flatness, excellent matching and high linearity. The most important challenge to the implementation of distributed amplifiers in CMOS RFICs is identified as the issue of their miniaturization. This problem is solved by using integrated multi-layered inductors instead of transmission lines to achieve over 90% size compression compared to earlier CMOS implementations. Finally, a dual wideband receiver front end sub-system is designed employing the miniaturized distributed amplifier with resonant loads and integrated with a double balanced Gilbert cell mixer to perform dual band operation. The receiver front end measured results show 15 dB conversion gain, and a 1-dB compression point of -4.1 dBm in the centre of band 1 (from 3.1 to 5.0 GHz) and -5.2 dBm in the centre of band 2 (from 5.8 to 8 GHz) with input return loss less than 10 dB throughout the two bands of operation.

To my mother, Indira Devi...

ACKNOWLEDGEMENTS

First and foremost, I would like to sincerely thank my advisor and committee chair, Dr. Cam Nguyen, who has taken the trouble of guiding me towards the end of my graduate studies at Texas A&M University and for having faith in my ability to perform research of high caliber in this intensely challenging field.

I would also like to thank my committee members, Dr. Edgar Sánchez-Sinencio, Dr. Chin B. Su and Dr. David A. Church, for their guidance and support, particularly during my preliminary examinations that led to a more definite shaping of my research work.

Thanks also go to my dear friends in Texas - my lab mates cum room mates Xin Guan and Rui Xu, not just for their technical discussions time and again but also for their friendship. My good friends - Alexandre Veniamin, Samuel Kokel, Marina Kovina and "Professor" Baski must be acknowledged for their friendship that has been tried and tested over the course of several years. My profound thanks are also due to Dr. Mahadevan Sridharan, president of Z~Communications, for giving me a full time employment opportunity in San Jose, CA. I also wish to thank the National Science Foundation that supported a part of my research work and the staff at the electrical engineering department of Texas A&M University, particularly Ms. Tammy Carda, for being extremely helpful on all departmental issues.

Finally, I would like to acknowledge my loving parents and my sister Yamini for their unwavering love and support.

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CHAPTER I

INTRODUCTION

Over the course of the past decade, wireless industry has grown to be a highly versatile and diversified industry turning over revenues worth billions of dollars, with applications spanning across a wide swath of civilian and military domains. Several applications are being continuously updated to supplant existing tethered communication systems with wireless technology. Whether it is an EZ-tag that allows a much swifter automobile passage at freeways or ground penetration radar that helps detect hidden landmines, wireless industry has revolutionized modern life and made its presence ubiquitous. The flexibility and hands-free capability facilitated by Wireless appliances and tools has fuelled an unprecedented demand for a wide array of wireless devices. A modest idea of what an explosive growth this industry has witnessed could be gauged from Figure 1.1. Currently, there are over 218 million subscribers of wireless products in USA alone which is a five fold increase since the trend towards inexpensive products started gaining momentum and the market has been growing by at least 24 million each year in the past 2 years [1]. A wireless product is sold every second and a wireless access point is installed every four seconds in the United States of America. A significant reason for this unprecedented growth is the competitive pricing of wireless products. Such cost effectiveness has primarily been fuelled by lower cost per chip area facilitated by CMOS and related monolithic silicon technologies, whose benefit trickles

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down to the consumer.

At the same time, cost effectiveness alone wouldn't be a compelling reason without reasonable product performance. It is here that the role of an RF designer becomes clearly defined – it lies in the ingenuity to extract maximum circuit performance while striving to conserve chip area. The goal of the current dissertation is to achieve the same moderation required from RF designers - in balancing optimum circuit performance with reasonable chip area consumption.
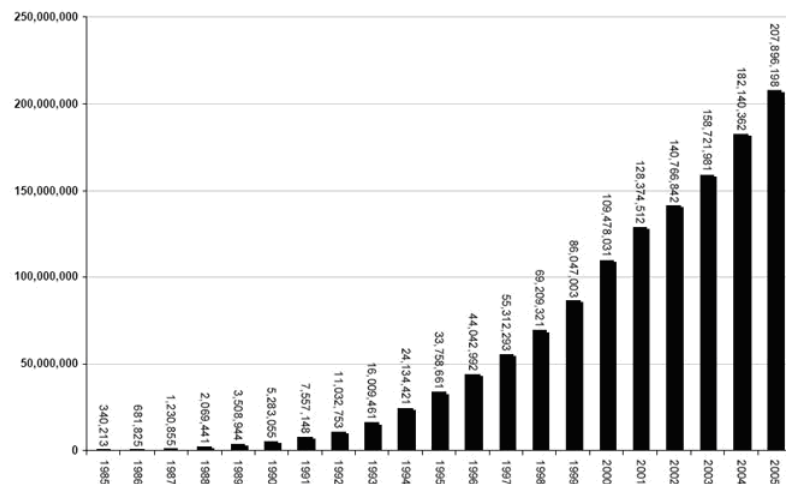
Figure 1.1 Estimated number of wireless subscribers in USA (source CTIA [1]).

1.1 Research motivation

Commensurate with the current trend of rapid wireless market expansion, the complications involved in the design of high frequency wireless circuits become more

difficult to specify with certainty. However, commercial applications that employ wireless products typically require a wide array of high performance, low cost and low power circuits though the design challenges vary from one application to another. Circuit specifications typically depend on their respective applications. Broadly, circuits catering to wireless communication related applications could be classified into two categories, depending on their frequencies of operation: (a) Front-end, the high frequency sub-system that performs signal amplification and down/up conversion (b) Back-end, the low frequency sub-system that performs signal extraction/generation. The front-end receiver sub-system is of particular interest owing to the challenges posed by the high frequency behavior of passives and active components of CMOS technology which tend to complicate optimal signal detection, extraction and regeneration. A receiver front-end usually consists of a low noise amplifier (LNA), down-conversion mixer, frequency synthesizer, image rejection filters, intermediate frequency filters and amplifiers. Regardless of the nature of wireless applications, the challenges posed in the design of these high frequency wireless circuits, viz., the front-end sub-system components are common and directly related to the needs of the wireless market.

There were two prime motivations in conducting the current course of research. One was to develop high performance and extremely compact novel RF passive structures and front end circuits for Ultra Wideband (UWB), WLAN and the unlicensed Ka-band (26.5 GHz to 40 GHz) for Industrial, Scientific and Medical (ISM) applications. A second motivation was to contribute to the development of new wireless applications by developing a novel sub-system capable of *possible* multi-functional operation. A dual-

wide band concurrent receiver front-end sub-system is demonstrated, whose concept could be extended either to Ultra Wideband (UWB) or to multi-functional architectures serving multiple applications on the same chip.

To gist, regardless of the nature of wireless application, the design challenges of any wireless circuit are market oriented and are commonly subject to technological constraints that need to be carefully addressed by the designer.

1.2 Dissertation overview

The current dissertation comprises of three broad segments – passive, active and sub-system. The following section on Passive structures includes novel topologies of 90º and 180º couplers, resonators and inductors. Chapter II discusses the design and development of CMOS-millimeter wave specific novel passive components. A variety of CMOS-specific miniaturization techniques were also developed and applied to these passive structures and are presented in detail. Chapter III details the design and development of wideband amplifiers, particularly distributed low noise amplifiers, which employ novel multi-layered inductor structures as well as integrated inductors and transmission lines. The LNAs including a DC-20 GHz broad band amplifier and an ultra-compact, low power UWB amplifier are both discussed elaborately in this chapter. A novel dual wide band amplifier with lumped element analog design principles is also demonstrated. A point worth mentioning here is that all the low noise amplifiers were designed considering their possible integration into a dual wideband sub-system. The subsequent chapter on VCOs discusses the general operational principles of multi-stage

distributed VCOs. Design issues related to the usage of artificial transmission lines in CMOS DVCOs are also discussed here and also the impact of multi-layered vertically coiled inductors on VCO performance. The fifth chapter discusses a novel dual-band UWB receiver sub-system. The circuit components, including a novel concurrent dual band distributed LNA, active baluns, dual balanced Gilbert cell mixer and output buffers are discussed along with system level issues in this section. The final chapter presents the recommended future work that could be carried out in each of these fields as well as a brief summary of the current work.

The dissertation has an extensive and ambitious scope aiming to cover a wide range of novel passive, active and front-end sub-system elements from DC till 40 GHz based applications. And because of such extensiveness, there could be a deliberation on the common factor binding such disparate circuits as a 90º Lange coupler and a dual wide-band low noise amplifier. It is here that it must be noted that the common binding factor lies in the similarity of the design premise in all implementations – of trying to develop high performance, miniaturized, low power consumption RF, microwave and millimeter-wave system and circuit blocks that are highly attractive to the wireless market. Another ambitious agenda was to successfully demonstrate the amalgamation of both analog and microwave design concepts – a useful trend that enables implementation of novel topologies for increasingly higher frequency related applications in CMOS.

CHAPTER II

DISTRIBUTED PASSIVE CIRCUITS

In this chapter, distributed passive circuits ranging from inductors to microwave couplers are discussed and several new design techniques are presented that improve their overall performance. Section 2.1 gives an overview of these passive components hitherto implemented in GaAs MMICs, need for miniaturization and a summary of all the important miniaturization techniques. Section 2.2 deals with the basics of CMOS microwave passive design while section 2.3 focuses on the theory and implementation of slow wave structures and the feasibility of its applicability to CMOS passive circuit miniaturization. A novel slow wave structure is also introduced here and its application to a hairpin resonator is also studied. Multi-layered design techniques form an important segment of discussion in section 2.4. A variety of microwave passive couplers miniaturized by multi-layer design techniques are presented and discussed in this section. The section also discusses the basic principles of multi-layered design and how the CMOS metal stack and the high resistive SiO_2 dielectric could be exploited for vertical design that facilitates substantial miniaturization. Finally, section 2.4 also presents a composite design technique that combines both slow wave and multi-layered design principles to achieve a novel 3-D complementary slow wave structure, which is shown to yield the benefits of both quality factor enhancement as well as circuit miniaturization, better than the 2-D planar slow wave. It can be noted that all the design techniques presented in this section, though implemented in CMOS, could be extrapolated to any monolithic IC technology where the size and performance of

passives is a major concern. The final section discusses some possible applications for the designed CMOS microwave passives.

2.1 Overview of existing miniaturization techniques in MMICs

Since the discovery of Gunn effect [2] in 1962, development of GaAs based Monolithic Microwave Integrated Circuit (MMIC) components began at an extremely rapid pace. The first MMIC passive components were designed by Mehal et al [3] and Mao et al [4] who developed a series of couplers, phase shifters, mixers and diodes for millimeter wave applications up to 94 GHz. Since then, GaAs has been the workhorse of novel passive circuitry catering to the microwave and millimeter wave integrated circuit domain. The invention of MESFETs and PHEMTs in 1970s and 90s respectively, further contributed to the development of passive circuitry to complement the availability of excellent transistors with low transit carrier times and high resistance substrates. As a consequence, a number of monolithic passive design techniques are available in GaAs and this section provides an overview of those existing techniques.

2.1.1   Couplers

Couplers are typically passive components that perform power division or combination bearing an appropriate phase difference between their output terminals. During power division an input signal is divided into one or more signals of lesser power, either of equal or unequal power, usually accompanied with loss. Four port couplers that split the power equally between their outputs are called hybrids and exhibit

either 90° or 180° phase difference between the outputs [5]. In MMIC design, couplers

are implemented in novel ways to conserve chip area and reduce their inherent losses. A

list of popular MMIC based couplers is shown in figure 2.1. The ring hybrid is one of the

most widely used 180° hybrid structures. It operates in either summation (in phase) or
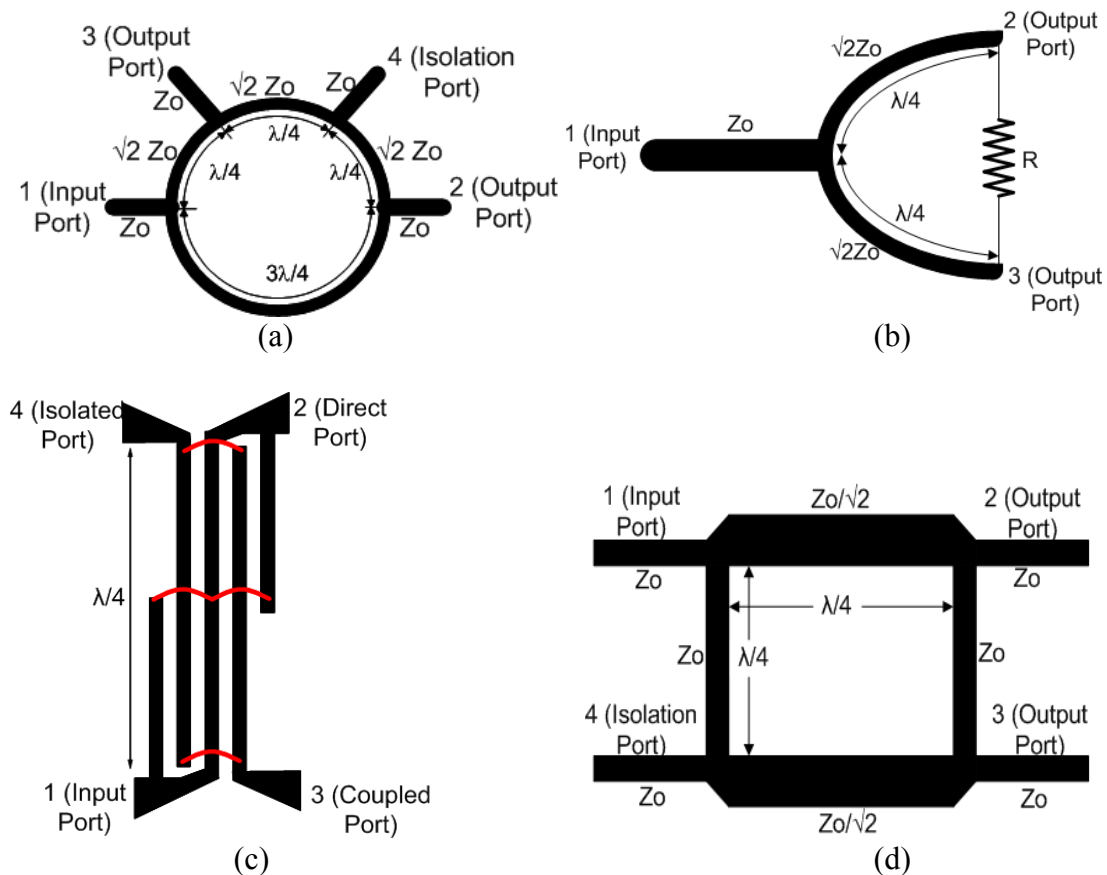
Figure 2.1 Layouts of popular MMIC couplers (a) Ring Hybrid (b) Wilkinson Coupler
(c) Lange Coupler and (d) Branchline Coupler.

difference (out of phase) modes. The layout shown in Figure 2.1(a) is of the difference

mode, which splits the input signal equally and causes a 180° phase shift between the

two outputs. For the summation mode, the signal is typically applied at port 4 (currently labeled as the isolation port) to gain two signal outputs of similar phase but equally split. The main advantages of the ring hybrid are its ease of design, uni-planar configuration that facilitates easier fabrication and flexibility of operation while the prime disadvantages are its exorbitant size that makes it impractical even for RF frequencies in monolithic technologies and narrow bandwidth. Several techniques have been proposed in MMIC technologies to enhance the bandwidth and reduce the prohibitively large circuit dimensions of this coupler which are discussed in more detail in the coming section on the TFMS ring hybrid. Nonetheless, this circuit finds enormous applications in MMIC design – from active mixers to phase shifters.

The Wilkinson coupler [6] shown in figure 2.1 (b) is a three port 90° coupler, i.e., which can split input power equally, with excellent matching at all three ports and good isolation of input and output ports. It can also be designed for unequal power transfer and arbitrary phase difference as well. Its main strength lies in the ease of design and relatively moderate dimensions. However, for usage in RF applications, there is a possibility of loss in the resistor that leads to amplitude reduction. Furthermore, tighter coupling with very small insertion loss becomes exceedingly difficult to achieve with this coupler as it has been conceived as a power splitter and or power combiner rather than a low insertion loss, tight coupler.

This problem is overcome in a Lange coupler [7] that allows very tight coupling ratios. The 4-fingered, edge-coupled, folded version of the Lange coupler is shown in figure 2.1(c). This structure has the immediate advantage of tighter coupling and

extremely wide bandwidth through a completely uni-planar structure. The coupler works by forcing the even and odd mode phase velocities to be close to each other, which is achieved by creating equi-potential surfaces through inter-connects on alternate metal strips on an edge coupled structure. The Lange coupler is highly attractive for a variety of broadband RF and microwave applications if its quarter-wavelength dimension problem is solved. This is the subject of further discussion in the broadside coupled Lange structure.

The Branchline coupler introduced in figure 2.1(d) is the final structure which owes its popularity for being the simplest coupler to design and fabricate. When perfectly matched, power entering port 1 is evenly divided between ports 2 and 3, with a 90° phase difference between them. It is also a perfectly symmetrical structure that allows any port to function as an input. Its prime disadvantages that make it difficult for MMIC design are its inherently large chip area consumption. The coupler also suffers from very narrow bandwidths compared to the Lange, while occupying significantly larger area than the latter.

Among these different types of couplers mentioned above, two couplers are of particular interest to CMOS designers owing to their significant advantages for providing silicon based solutions for various microwave and millimeter wave applications. They are - the Lange coupler, which is a 90° hybrid and the ring hybrid, a 180° rat race coupler. The Lange coupler removes the problem associated with narrow bandwidths of the Branchline at the same time while facilitating a monolithic fabrication. It is a very tight coupling circuit and less than 3 dB coupling is easily

possible. Insertion losses less than 0.2 dB have been achieved even at millimeter wave frequencies, while facilitating several octaves of bandwidth, independent of technology. All these qualities prove extremely attractive to CMOS millimeter wave designers, where applications constantly demand greater bandwidths and low loss power combining or dividing circuits. On the other hand, the Ring hybrid can perform the role of single to differential conversion through its 180° phase difference between both of its output ports. It finds immediate applicability in CMOS Microwave design, for instance, through the super-heterodyne receiver architecture to ease the transition from a single ended LNA output to a differential input double balanced Gilbert cell mixer. By functioning as a Balun, it can be utilized in a wide variety of CMOS receiver circuit applications as well. However, the greatest obstacle in exploiting the circuit level applications of these immensely useful topologies is their prohibitively large size.

The above discussion makes it apparent that miniaturization of microwave passives is the biggest challenge in their CMOS implementation. The concept of exploring miniaturization techniques for microwave passives was in vogue ever since the first implementation of couplers in a monolithic IC technology by Waterman et al [8] and Brehm et al [9]. The reported dimensions were in excess of 1 x 3 mm even at millimeter wave frequencies. Lange couplers were among the first 90° hybrids to be fabricated owing to their uni-planar structure that do not necessitate additional procedures on the fabrication technique. Early miniaturization techniques involved only meandering that folded the coupler along its length without affecting the internal coupling between different turns of the coupler [8]. Multi-layered design techniques began to be utilized

for further scaling down the dimensions and circuits measuring 1 x 0.8 mm were reported by Robertson et al [10] for 0.1-12 GHz applications. Novel miniaturization techniques appeared around 1990s and involved utilizing lumped elements to mimic transmission line properties [11] which significantly scaled down dimensions. Yet, they suffered from inherent bandwidth limitations and could not span multiple decades of operation like their distributed counterparts. Multi-layered design techniques were proposed by [12]-[15] and began to be extensively used to scale down the size significantly as well as to increase the coupling of inter-digitated lines. Other notable techniques include periodic stub loading that creates either an inductive or capacitive periodic attenuation of the wave velocity, thereby causing an artificial slow wave impact [16]-[18], incorporating slow wave structures [19]-[20] and aggressive meandering [21]. Both capacitive and inductive loading are typically accomplished by short and open circuited stubs at microwave and millimeter wave frequencies. A variety of slow-wave structures particularly tailored for monolithic technologies, notably the Uni-Planar Compact Photonic Band Gap (UC-PBG) structure developed by Prof. Itoh et al [22], have been applied in GaAs to reduce wave propagation velocity, increase the effective dielectric constant and thus reduce circuit dimensions. However, slow wave design has not yet caught up with CMOS owing to the non-compatibility of dimensional requirements. Design complications also abound as slow wave structures need to satisfy physical properties and cannot comply with arbitrary miniaturization procedures. Aggressive meandering, while being the easiest of all, is more of a layout principle than

a design technique and can be used in addition to any of the above techniques to gain further miniaturization.

2.1.2   Resonators

Traditionally, any structure that enables resonance or resonant behavior could be characterized as a resonator. A wide variety of resonators exist from 100 MHz to 100 GHz to satisfy a significant number of applications. In RF and millimeter wave circuit design, resonators perform several important functions like enabling oscillations inside local oscillators, diplexers and band pass filter components. Since the advent of monolithic circuit design, the basic resonator structures underwent a drastic change from bulk wave, surface acoustic wave (SAW), helical, dielectric and waveguide to coaxial and stripline resonators [23]. Bulk wave, SAW and helical resonators mostly operate below 1 GHz and handle diverse power requirements. Helical resonators are capable of handling larger powers than the other two. Dielectric resonators are mostly meant for RF and microwave applications and present exceptional characteristics – low loss and high quality factor. Yet, their reliance on exotic dielectric materials makes them unattractive for monolithic circuit implementation and also very expensive to realize in bulk. Waveguide resonators are among the oldest and most studied resonators and have proven valuable for applications more than 100 GHz. However, they too suffer from extremely large dimensions which makes them difficult to realize in monolithic technologies. Stripline and coaxial resonators, on the other hand, do not match either waveguide or dielectric resonators on the performance aspect. Yet, they are deemed very

useful by MMIC designers owing to their flexible, simple design procedures and relatively smaller dimensions. They are also technology independent, which makes them
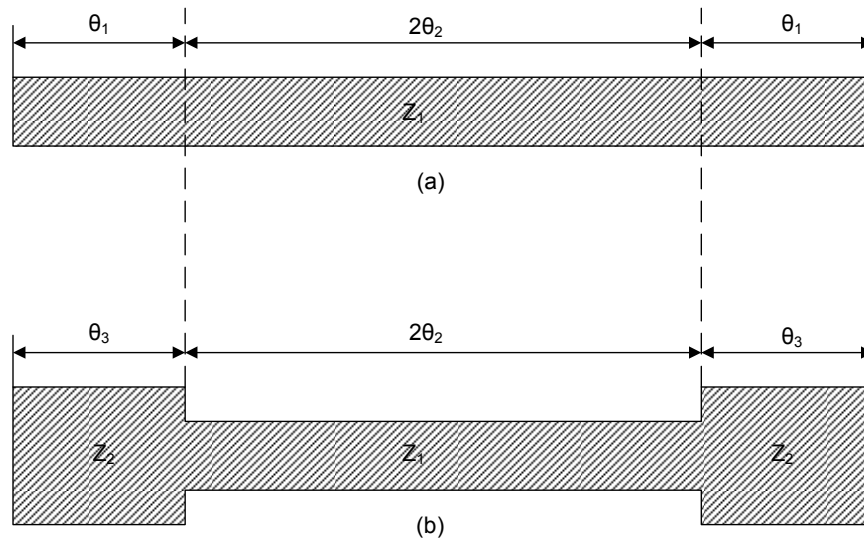
Figure 2.2 Types of Stripline resonators (a) Uniform Impedance (b) Stepped Impedance. [23]

less expensive to fabricate. Stripline resonators are more suited for monolithic design as they allow planar circuits.

Stripline resonators could be broadly classified into Uniform Impedance Resonators (UIR) and Stepped Impedance Resonators (SIR). They are depicted in figure 2.2. The electrical length of the stepped branches in the SIR is related to the electrical length of the extended uniform arms of the UIR by the relation [23]:

$$\tan \theta_3 = \frac{Z_2}{Z_1} \tan \theta_1 . \tag{2.1}$$

The uniform impedance resonator, while being very easy to design doesn't give designers many opportunities to introduce variations due to its limited design parameters. It also introduces spurious responses at integer multiples of fundamental resonant frequency. Stepped Impedance Resonators overcome these limitations by allowing greater design flexibility through its non-uniform impedance characteristics. Due to the availability of very powerful 2, 2.5 and 3 D Electro-magnetic simulators, the modeling and design of these resonators is very much simplified. Stepped impedance resonators have hitherto found several applications in filters, oscillators and mixers in MMIC design. Based on their electrical length, stepped impedance resonators are further classified into three classes - full, half and quarter wave length as shown in figure 2.3. The full wave length SIR is depicted as a circle in order to be area efficient. The half wavelength resonator could have both open and both short circuited ends. The quarter wavelength resonator is depicted with open ends in the figure, but it could also have short.

While full wavelength resonators are too large for monolithic IC implementation, quarter-wavelength SIRs inspite of having a significant size advantage over the half wavelength SIR, suffer from limited number of geometries and the convenience to tap the output in cross coupled structures that are used to generate negative resistance in CMOS design of voltage controlled oscillators, where such resonators could find potential application. Resonators like these are similar to distributed versions of typical RLC tank circuits. Their main practical disadvantage for CMOS design lies in the case of having an extremely low impedance terminal which is close to short at the resonant
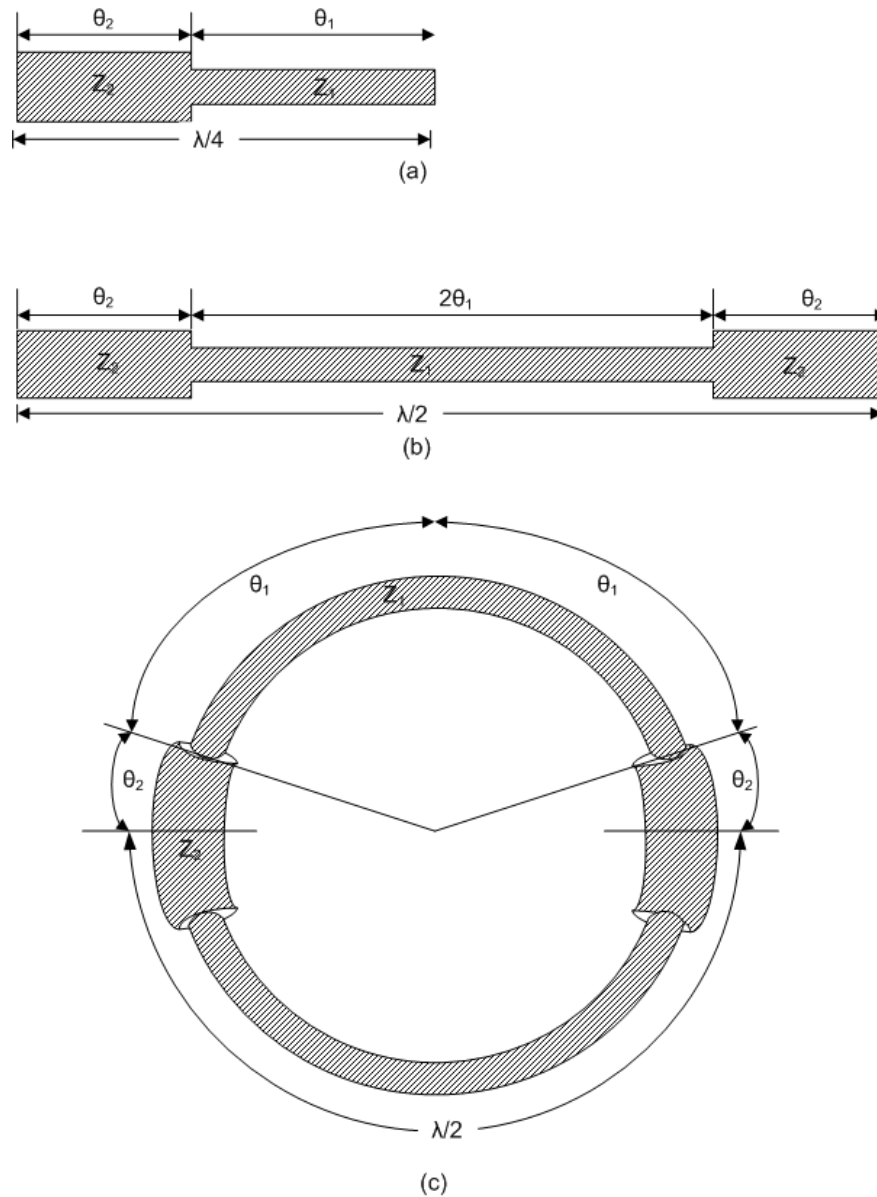
Figure 2.3 Stepped Impedance Resonators (a) quarter-wavelength ($\lambda_g/4$) (b) Half wavelength ($\lambda_g/2$) and (c) Full wavelength (λ_g). Each node is either open or short depending on the application.

frequency when the other terminal is a high impedance node. This could also causes problems in routing metal through the low impedance node. For microwave and
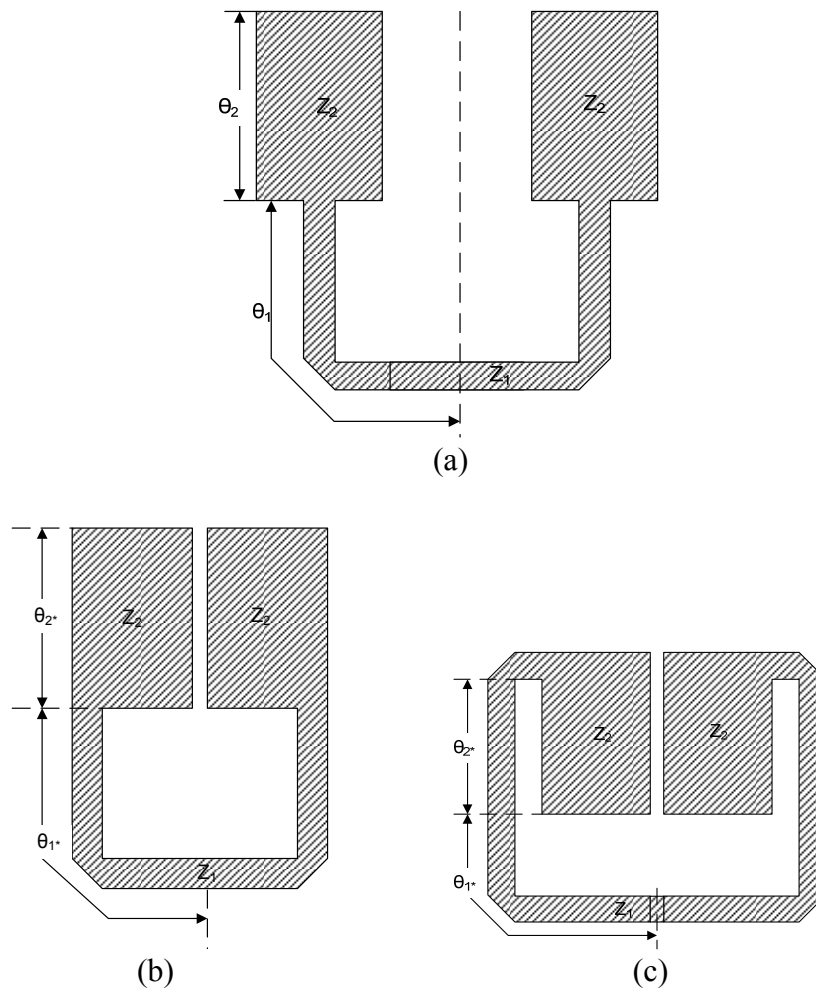
Figure 2.4 (a) Conventional hair pin resonator (b) internally coupled hairpin resonator (c) Ring type resonator with internal coupling. [23]

millimeter wave CMOS design, layout geometry flexibility is very important to enable high frequency routing between active devices and passive microwave structures. Half wavelength SIRs not only allow easier routing, a feature not available in quarter wavelength. The quarter wavelength resonator also tends to exhibit at least one low impedance node whenever the other end is left open. This becomes a practical problem at multi-GHz frequencies. Further, the half-wavelength resonators allow several different

geometries including hairpin, ring, etc, which gives the designer greater flexibility to tailor the functionality of the passives for specific circuit needs, depending on the application. Cristal et al [24] reported the first half wavelength resonators used a hairpin structure to implement a bandpass filter operating around 1.5 GHz. The structure had a uniform impedance and consisted of several mutually coupled hairpin structures. Stepped impedance resonators were first proposed by Makimoto et al [25] for designing bandpass filters at 900 MHz. The first attempt at miniaturization and practical high frequency application of half wavelength resonators was carried out by Sagawa et al [26] who developed an ultra compact hairpin split ring resonator which could be readily integrated in MMIC. Significant size reduction could be obtained by exploiting internal coupling between the resonator arms. Subsequently, miniaturized hairpin and other variants of half wavelength resonators have been widely used to design a variety of push-push oscillators [27], bandpass filters [26] and even as slow wave structures [28]. Currently, the sole miniaturization techniques applied to the traditional hairpin resonator has been to fold the structure internally. This internal coupled slow wave structure is depicted in figure 2.4 (c).

Structure (b) is explored in depth in section 2.2 as it could be of significant interest to CMOS designers at millimeter wave frequencies as a possible alternative to RLC tank circuits in NMOS-PMOS cross coupled voltage controlled oscillators (VCO). However, in its present form, the existing dimensions and inadequate miniaturization techniques donot make it compatible for CMOS implementation even at 30 GHz.

2.1.3 Inductors

Contrary to the previous two categories of interest mentioned earlier, inductors have been exclusively researched in both performance and size aspects in CMOS more than any other passive structure in any other technology. Popular Silicon based spiral inductors meant for analog applications were first patented by A. E. Hubbard [29] and their multi-GHz behavior was first studied by Nguyen et al [30]. Numerous models exist in literature that quantify and characterize the three important performance factors of an inductor – the inductance, quality factor and self-resonant frequency, specifically for Radio frequency and microwave/millimeter wave applications. Quality factor is characterized by the following expression derived from the single port Y-parameters of a spiral coil :

$$Q = \frac{-\text{Im}(Y_{11})}{\text{Re}(Y_{11})} \ . \tag{2.2}$$

(a)   (b)   (c)
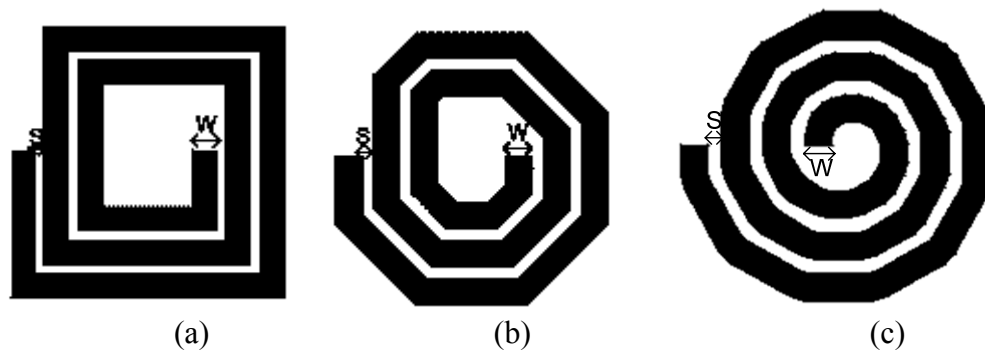
Figure 2.5 Planar spiral inductors in CMOS (a) Rectangular (b) Octagonal and (c) Circular.

An alternate expression is used to account for the finite Q values at the Self resonant frequency [31]:

$$Q = \frac{\omega_0}{\Delta\omega_{3dB}} \quad . \tag{2.3}$$

with $\Delta\omega_{3dB}$ being the 3-dB bandwidth measured around ω_0. The self-resonant frequency, another important parameter, is defined as the frequency above which the extracted impedance becomes capacitive. Most communication circuits require higher quality factor values and higher self-resonant frequencies owing to the increasingly higher frequencies of circuit operation. The most widely used CMOS inductor structure is the planar spiral, which relies on mutual coupling between each turns to store magnetic energy. While it suffers from limited quality factors, it provides the best means to achieve a wide variety of inductances for different communication circuit applications. Different forms of planar spirals are shown in figure 2.5. The coil width 'w' and the spacing between the turns 's' are depicted in all cases.

The loss mechanisms in planar silicon based inductors are due to silicon substrate conductivity, substrate eddy current losses and current constriction in the turns of a multi-turn spiral and the spiral underpass capacitance [32], [33]. Subsequently, when the inductor structure is subject to miniaturization, these loss mechanisms must be taken into consideration as some miniaturization techniques might prove detrimental to the overall performance metrics.

Miniaturization of inductors is even more challenging than those of couplers and resonators because of their critical impact on key communication circuit blocks. The size reduction techniques employed for inductors in silicon have followed their microwave passive counterparts by exploiting the presence of multiple metal stacks in monolithic

CMOS technology. Currently, vertically stacking, micro-machining and selective removal of lossy Si substrate and vertical solenoid are three prominent approaches to the design of miniaturized inductors. Vertically stacked inductors use a set of stacked planar inductors, implemented on different metal layers of a standard CMOS technology, to generate higher inductance without occupying much lateral chip area. A fractional increase in self resonant frequencies has also been reported [34]-[35]. Micro-machined inductors are typically fabricated using non-standard MEMS procedures on a standard silicon technology or on CMOS grade silicon wafers. They consume lower chip area and typically have extremely high quality factors, owing to the removal of lossy silicon substrate below the inductor [36]. However, this approach is the least preferred alternative owing to the extra cost incurred during the post-fabrication MEMS procedure. The vertical solenoid inductors are implemented in a helical form along the CMOS metal stack. The multiple turns of the inductor are each implemented on a different metal layer so as to build a vertical inductor structure that consumes little lateral chip area [37]. Higher quality factors and self-resonant frequencies have been reported using this design structure along with significant chip area consumption. Figure 2.6 shows the layouts of the two varieties of standard miniature inductors mentioned above.

Overall, existing miniaturization techniques for all the passive circuits mentioned in this section are still grappling with performance and cost optimization problems, while designers are constantly seeking new ideas to further reduce the chip area consumption and enhance their performance metrics. There is also a significant difficulty while trying
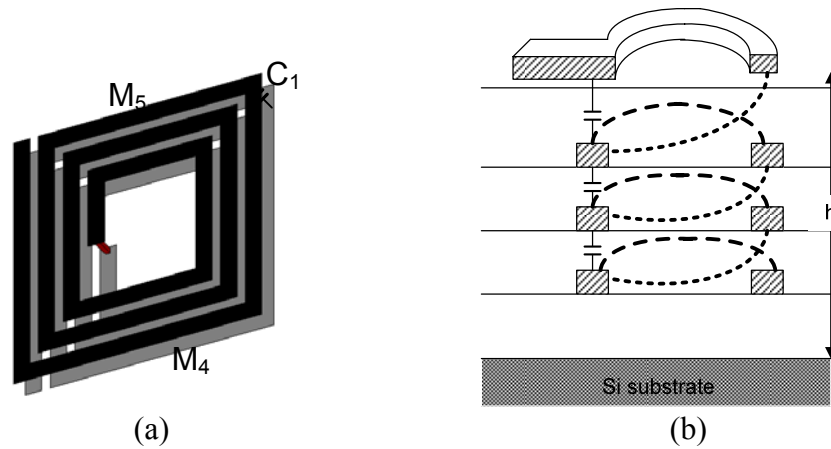
Figure 2.6 Miniaturized inductors in CMOS (a) Vertically stacked (b) Vertical Solenoid. M5 and M4 indicate metal layers 5 and 4.

to map the existing miniaturization techniques in well established MMIC technologies like GaAs into the newly developing CMOS technology due to the lossy nature of silicon substrate as well as the extremely small dimensions being required in CMOS technologies. These challenges along with some novel ideas that have been implemented for the first time in CMOS technologies are discussed in the subsequent sections of this chapter.

2.2 Design of microwave structures in CMOS

CMOS based technologies pose a critical challenge in the design of microwave passive structures since size limitations are a major challenge to circuit designers even at millimeter wave frequencies. In this section, properties of the silicon substrate as well as

design considerations of how CMOS technology tends to influence microwave passive design are studied.

2.2.1   Properties of silicon based substrates

The Silicon dioxide dielectric constant inside which all the metal layers of any standard CMOS technology are embedded is typically 3 times smaller than that of Duroid RT/6010 substrate laminate, a popular low loss substrate for developing microwave passives. Table 2.1 shows the comparison between a standard CMOS technology and a Duroid substrate. It shows the properties of the oxide and passivation layers, for the CMOS technology, as the metals are embedded inside the oxide layer. The structures of both the Duroid substrate and CMOS technologies are illustrated in figure 2.7. It should be noted that for quasi-TEM transmission lines like microstrip and CPW, which are extensively used in distributed topology based circuits; the role of silicon substrate is also crucial and as such its conductivity influences microwave passive circuit performance. The high conductivity of typical bulk silicon substrate which is about 12 S/m impacts inductor performance as well, leads to induction of large eddy currents in the substrate. The smaller dielectric constant within the oxide layer as well causes a significant reduction of metal width for microstrip transmission lines. The top metal thickness is only moderately thick which also poses additional problems of skin effect at millimeter wave and higher microwave frequencies.

Table 2.1 Comparison of CMOS and Duroid substrates

Substrate Properties	Typical CMOS technology	RT/Duroid
Type	Multi-layered	Single
Dielectric Constant	3.95-4.1	2.24-10.5
Thickness	Few tens of micron	At least 127 μm
Substrate Electrical Conductivity	Prominent	Negligible
Loss tangent	0.004-0.015	0.0009 to 0.002
Top metal thickness	Few Micron	At least 19 μm

The smaller dielectric constant of the oxide is also counterproductive as it causes the effective wavelength to be larger for transmission lines. In spite of these apparent flaws, CMOS technology still holds some useful properties that could be exploited by microwave passive circuit designers. Firstly, successive technologies at the sub-micron gate length level are using thicker top metals that are placed much higher above the bottom metal. This is fuelled by the need for denser and more efficient power routing in digital circuits, which are typically integrated with the analog/RF blocks. Secondly, the electrical conductivity of the SiO_2 layer itself is quite small and it is in this layer that the major chunk of electric field is concentrated. Finally, the presence of passivation layers

<center>(a)   (b)</center>
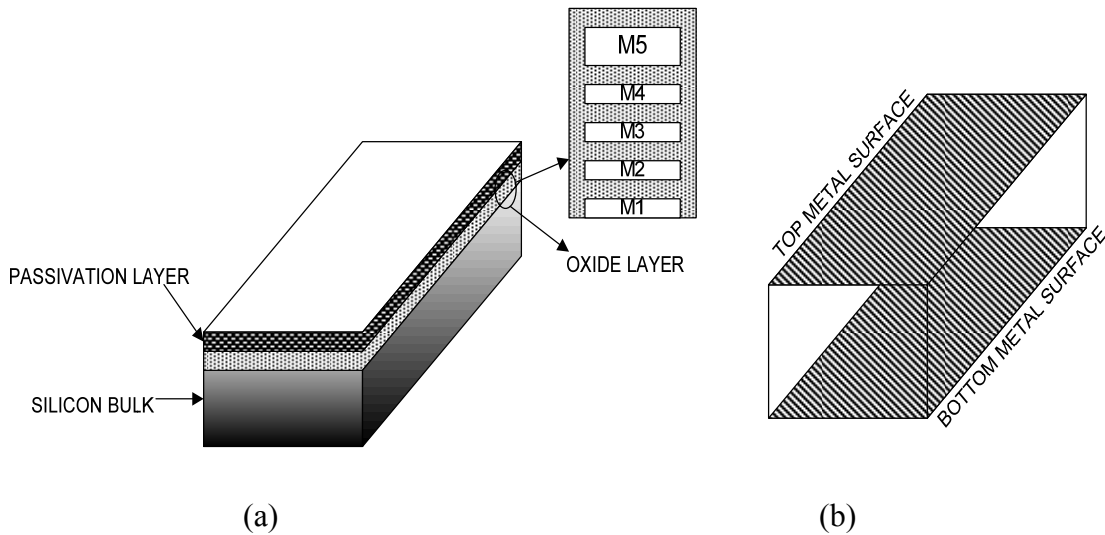
Figure 2.7 Graphical representation of (a) CMOS and (b) Duroid/RT substrates.

above the oxide layer, further cushions the electric field from interfering with the outer environment, a facility not available in traditional monolithic substrates without additional fabrication procedures. Further more, the problems associated with the lossy and conductive silicon substrate could be easily alleviated by the designer's understanding of the substrate properties in CMOS as well as some by some time tested design techniques.

2.2.2   Microstrip vs CPW

An important consideration in the design of microwave passive circuits lies in choosing which quasi-TEM transmission lines are to be preferred for implementing them. From the five metal CMOS technology shown in figure 2.7 (a), a microstrip line could be implemented using metals 5 (M5) and 1 (M1) while a (non-conductor backed)

CPW can be entirely implemented on M5. For microstrip lines, M1 could considered as the ground plane while M5 is used as the signal line, in order to extract the maximum substrate thickness from the technology. This is because having a larger substrate thickness allows usage of larger signal line widths to realize larger characteristic impedances, which is highly desirable since smaller metal widths usually face the problem of current crowding at high frequencies.

Microstrip transmission lines have the inherent advantage of easier routing and layout. However, their maximum impedances cannot go above 100 Ω for most sub-micron standard CMOS technologies as their widths become too narrow at higher impedances. CPW structures pose a difficulty in routing and tend to occupy greater chip area. But greater impedances are easily realizable through CPW than microstrip lines without risking narrower widths.

The clinching factor in favor of microstrip lines is that they tend to reduce the penetration of the electric field through the silicon substrate unlike the CPW which has significant field penetration. The electric field patterns of both these transmission lines are displayed in figure 2.8 for high characteristic impedance on a typical CMOS substrate. It is evident that the CPW segments risk greater silicon substrate penetration at higher impedances and as such might prove more lossy than microstrip lines at higher impedances which depend on having larger spacing between the signal and ground planes. The larger width advantage facilitated by CPW structures, therefore, could be replaced by a greater risk of silicon substrate field penetration. Thus, in this work, the microstrip transmission lines are the transmission lines of choice.

(a)

(b)
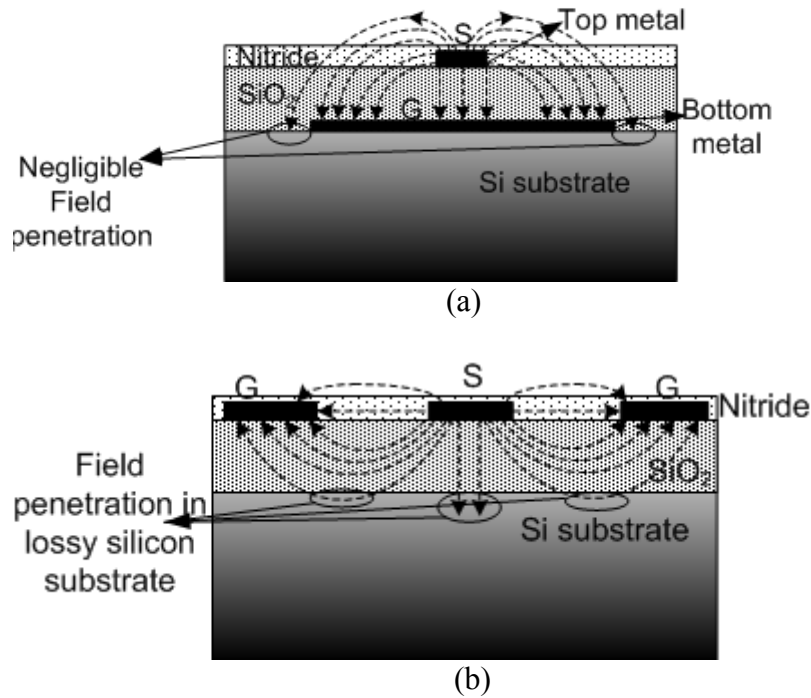
Figure 2.8 Electric field distribution in a high impedance (a) Microstrip and (b) CPW in CMOS.

2.3 The slow wave theory

Slow wave techniques have been extensively used in non monolithic, multi-dielectric substrates to achieve frequency selective behavior in microwave passive circuits. Though the idea of creating a periodic change in dielectric constant is not new in itself, much of the initial focus was concentrated on slow wave transmission lines, which consisted of Metal-Insulator-Semiconductor (MIS) which had the intrinsic disadvantages of higher ohmic losses and lower impedances [38]. Moreover, with increasing demand for high frequency applications, need for higher impedance, low loss structures became the primary concern. Initial interest in slow wave structures was generated from photonic

crystals with slow wave characteristics [39] and subsequently, development of periodic band gap structures that emulate a similar behavior in the microwave domain [40]. These structures have much higher impedances and do not require any non-standard, exotic substrates for implementation. This section presents the theory of slow wave propagation resulting from such slow wave structures and discusses their applicability to miniaturization and performance enhancement of RF, microwave and millimeter wave CMOS based distributed passive circuits. A novel slow wave structure is also presented and its impact on a hairpin resonator is evaluated as well.

2.3.1 Basic principles

Slow wave structures are 2 or 3-D periodic (and often, multi-layered) structures that prevent the propagation of Electro-magnetic waves within specific bands. This unique property of these structures offers designers an additional degree of freedom to control the EM behavior of a circuit. Mathematically, modeling an infinite periodic structure is much easier than a finite periodic structure owing to the occurrence of inhomogeneous modes in the latter. Since practical applications require only finite periodic structures, only they are of any significant interest to microwave engineers. In microwave circuits, finite periodic slow wave structures are designed in such a way that there would be an increase in the effective dielectric constant, which leads to reduction of group wave velocity. The periodicity of the slow wave pattern also leads to a complete attenuation of surface waves at some frequencies. A circuit operating subject to slow wave condition is bound by the stop band criterion [41]:

$$\beta.a = \pi \ . \tag{2.4}$$

wherein β is the phase constant at the center of the stop band and a is the lattice period of the periodically repeating slow wave structure. Several analytical approaches have been suggested to deal with the modeling challenges of finite periodic structures. One of the more feasible ways is to recursively extract the s-parameters of a finite periodic structure with $n+2m$ repetitions from the ABCD matrices of the same structure with $n+m$ and n repetitions as [43]:

$$\begin{bmatrix} A_{n+2m} & B_{n+2m} \\ C_{n+2m} & D_{n+2m} \end{bmatrix} = \begin{bmatrix} A_{n+m} & B_{n+m} \\ C_{n+m} & D_{n+m} \end{bmatrix} \begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix}^{-1} \begin{bmatrix} A_{n+m} & B_{n+m} \\ C_{n+m} & D_{n+m} \end{bmatrix}. \tag{2.5}$$

However, this still requires a prior knowledge of the ABCD parameters of the previous stages. A further thorough analytical treatment requires the extraction of the entire behavior of the complex propagation constant through dispersion diagrams of the EM modes supported by the periodic structure. A modified Brillouin zone diagram could also gives insight into the range of frequencies attenuated by the structure [42].

Even though analytical approaches give much needed insight, a much simpler mechanism to design and model slow wave based structures is to use a full wave EM analysis through EM simulation software. It should be noted that the attenuation in the stop band depends on the dimensions of the slow wave structure. The pass band characteristics are also affected by the lattice dimensions as increasing the size tends to increase the effective dielectric constant and also leads to a variation in characteristic impedance and hence, greater mismatch. Therefore, by carefully understanding the impact of each of these parameters, the modeling challenge can be translated directly

from an EM based analytical approach to a parameter based simulation approach
through a software tool.

2.3.2 Existing slow wave structures

Since the first demonstration of slow wave structures as a viable technique to
improve the performance and dimensions of microwave circuits in 1997, extensive
studies have been undertaken to apply them to planar microwave circuit design using
monolithic substrates. Figure 2.9 shows some traditional slow wave structures which
require exorbitant dimensions and lattice spacing, making them incompatible for
monolithic implementation.

      (a)   (b)   (c)
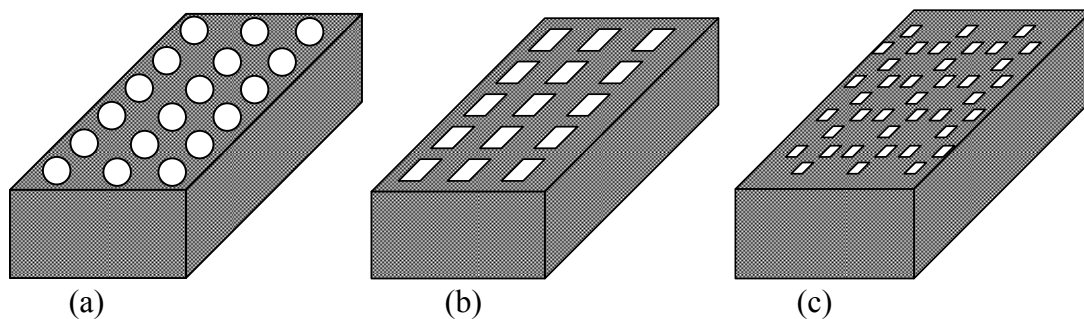
Figure 2.9 Traditional slow-wave lattices (a) circular (b) rectangular (c) rectangular
honey comb.

The biggest challenge in implementing slow wave structures on monolithic multi-dielectric substrates involves trade-offs with issues of miniaturization, matching, impedance and loss optimization. Some novel slow wave structures have been proposed that alleviate this problem for uni-planar substrates. The most prominent one is the Uni-planar photonic bandgap or UC-PBG structure [22], whose CPW implementation is shown in figure 2.10 that provides compact dimensions suitable for monolithic implementation. From the UC-PBG lattice unit cell lattice shown in fig. 2.10, it is evident that the UC-PBG structure provides slow wave properties by forming an RLC-
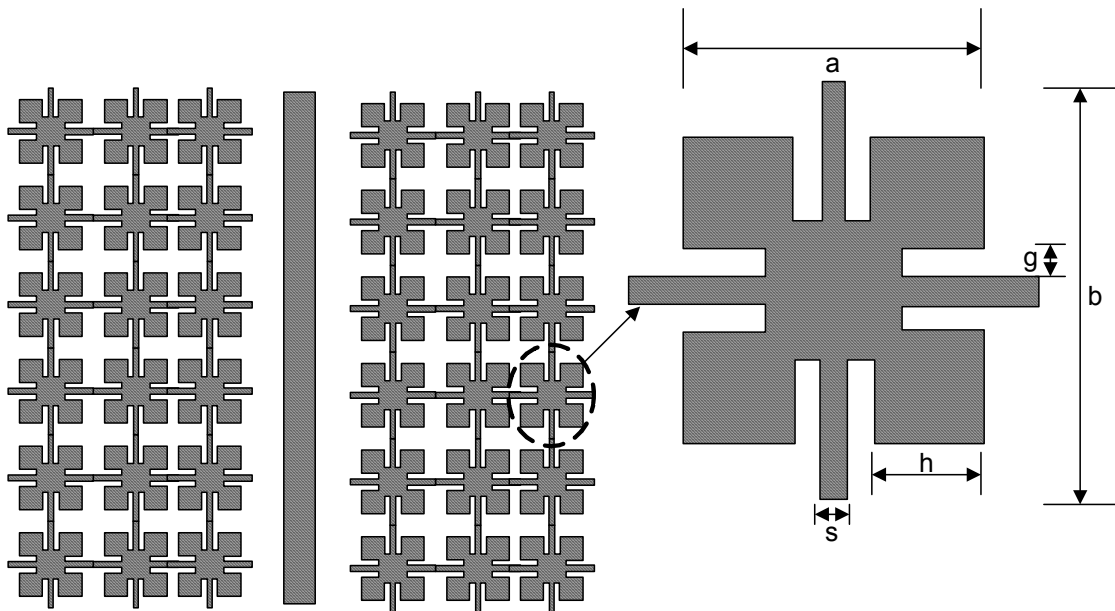
Figure 2.10 UC-PBG lattice as a CPW ground plane with the unit cell shown in the inset.

ladder network that depends on the series inductance introduced by the narrow strips and the shunt capacitance between the pads. Once the stop band condition in Equation (2.4)
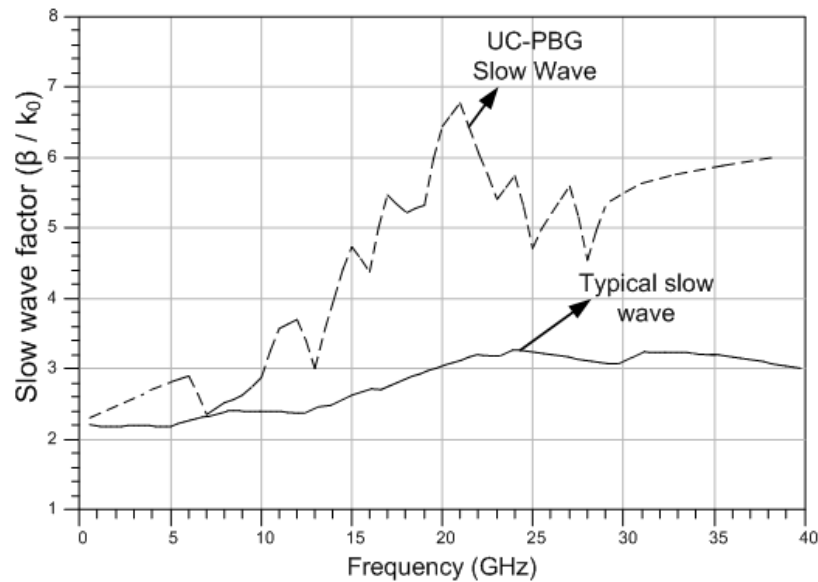
Figure 2.11 Simulated slow wave factors of Silicon substrate based UC-PBG structure and traditional slow wave structure shown in figure 2.9 (c).

is satisfied, the propagation of EM waves will be prohibited at certain frequencies along the transmission line. Both the inductance and capacitance are increased in the case of this structure compared to an ordinary transmission line with solid ground plane. This enhances the effective propagation constant which directly depends on both these parameters. This increase in propagation constant aids in miniaturizing any circuit implemented along the signal line either as a microstrip or CPW.

A lumped element model and characterization of the UC-PBG structure incorporated transmission line proves difficult as the characteristic impedance of the UC-PBG based transmission line is non-uniform over an incremental length. However, using a full wave EM simulator, IE3D [44], the performance of UC-PBG structure can be evaluated relative to the other slow wave structures. Figure 2.11 shows the slow wave factor of a

UC-PBG structure relative to a traditional slow wave structure shown in figure 2.9 (c). Both structures were designed using typical dimensions, involving quarter wavelength cell spacing and the dimensions of UC-PBG were similar to those used in [40]. On a 50 mil Rogers RT/Duroid 6010 substrate of relative dielectric constant 10.2, the filling factor (r/a) which indicates the ratio of rectangular cell length to the periodic spacing between two cells (refer to fig 2.9 (c)), of the traditional rectangular honeycomb PBG lattice is 0.2 and 'a' is 250 mil. On the other hand, for the UC-PBG structure [22], the filling factor is d/a, where d is the alignment offset between the centers of the microstrip and the UC-PBG ground plane while 'a' is indicated in figure 2.10. The ratio d/a is given by 0.2 while 'a' is 120 mil. It is apparent that the slow wave factor of the UC-PBG structure is much higher in spite of consuming a much smaller chip area. The structure is able to such high β/k_0 values by providing an LC ladder network through the narrow strips and gaps on the ground plane, which causes a low pass filter-like behavior. An interesting property of the UC-PBG structure is that the slow wave factor increases with frequency compared to existing slow wave structures [45]. This makes the structure very suitable for high frequency applications. The structure also results in a higher effective dielectric constant, which makes it possible to have larger strip widths for realizing similar characteristic impedance as on a solid ground plane. At high frequencies, this is a particularly attractive property; since the conductive loss associated with the signal line directly depends up on the width of the transmission line. Hence, having a larger width would result in a smaller conductive loss per wavelength. These two properties make the UC-PBG structure highly suitable candidates for silicon substrate based high

performance passive circuit implementation at microwave and millimeter wave frequencies.

2.3.3 Design of slow wave structures in CMOS

CMOS based technologies pose a critical challenge in the design of slow wave structure since size limitations are a major challenge to circuit designers even at millimeter wave frequencies. For the slow wave impact to be significant, lattice segments need to be spaced at least half wavelength apart. In a silicon dioxide dielectric, dimensions of the slow wave lattice arrays typically have millimeter long dimensions even in the lower millimeter wave frequency range. Further, implementing non-planar slow wave structures is very difficult and counter-productive to monolithic circuit design. The low substrate dielectric constant of silicon dioxide tends to adversely influence design with microstrip structures at higher frequencies as the width of the microstrip becomes smaller, leading to a large attenuation factor along the direction of signal propagation.

Being a planar structure, the UC-PBG structure, lends itself as an important slow wave structure that could be amenable for CMOS implementation. The design of the UC-PBG structure is application dependent. It has been earlier proved that the slow wave factor varies significantly with the inner dimensions of the structure. Figure 2.12 depicts the impact of the strip width s, the gap between pad length g and the strip length $(b-a)/2$ on the slow wave factor. Two UC-PBG lattices one non-optimized and another optimized are simulated in IE3D and their impact on the characteristics of a 50 Ohm line

is studied. The non-optimized UC-PBG lattice had 'a'=2.78 mm, 'b' = 3.05 mm, 's'= 'g'=0.254 mm and 'h'=0.7 mm, while the optimized UC-PBG has 'a'= 2.773 mm, 'b'=2.9 mm, 's'= 'g' =0.127 mm and 'h'=1.2 mm on a standard TSMC 0.25. μm CMOS substrate. The slow wave factor is significantly influenced, almost doubled when the lattice dimensions contributing to the inductance and capacitance, that is the strip width 's', the pad length 'g' and the strip length '(b-a)/2' are altered. The increase in both inductance and capacitance requires narrower strip widths and smaller gap, as indicated by parameters mentioned above.
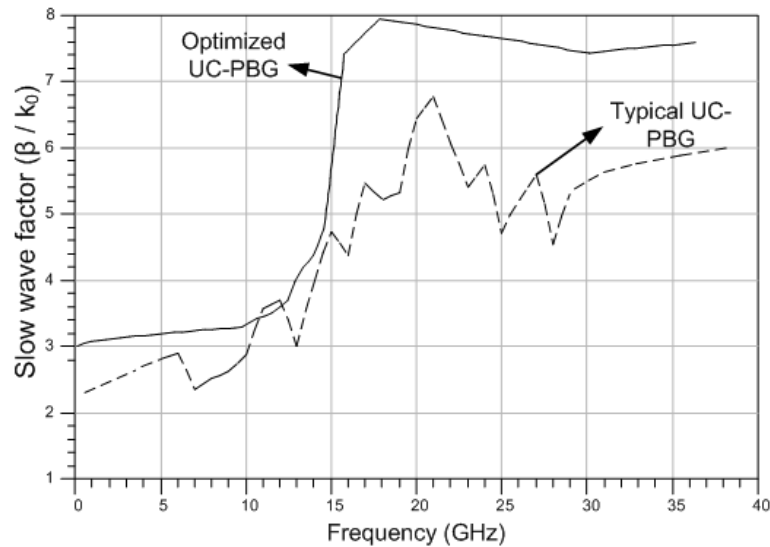
Figure 2.12 Fully optimized UC-PBG reflecting the impact of strip length, width and gap on the slow wave factor. Also shown is the un-optimized UC-PBG slow wave factor.

However, size restrictions in CMOS do not allow significant increase of inductance or capacitance. To further exacerbate the size problem, the silicon dioxide dielectric constant is small causing the electrical wavelength to be much longer. It must also be noted here that the stop band condition could be modified to make the lattice dimensions smaller by trading off the attenuation in the stop band. Hence, instead of following the stop band criterion in equation (2.4), we could use modified dimensions to achieve a similar impact, albeit with an acceptable mismatch and lower stop band attenuation. That is for CMOS design, equation (2.4) could not be implemented in its present form. For initial design, we hypothetically assumed an approximated expression:

$$\beta.a = \theta . \tag{2.6}$$

where in $\theta << \pi$.

To further illustrate this point, a miniaturized UC-PBG structure has been designed for TSMC 0.25 μm CMOS process and applied as a 1 x 10 lattice ground plane on a microstrip line which has 50 Ω characteristic impedance on a solid ground plane as shown in figure 2.13. At 16 GHz of stop band operation, the dimensions of the structure

Figure 2.13 Microstrip based UC-PBG structure. Metal 5 was used for the microstrip line and Metal 1 for the UC-PBG ground plane.

are: a=230 μm, b=250μm, s=g=10 μm and h=50 μm. This corresponds to θ of 5.56°, which is small enough to ignore serious mismatch. The UC-PBG structure exhibits the following properties when implemented at these dimensions, as in figure 2.14. If θ were equal to pi, the stop and pass bands would be more pronounced in the steepness of their slopes as well as attenuation. However, their dimensions would be impractical for any meaningful application.

It is apparent that there is some attenuation, but it is not significant enough to cause a deeper stop band as is the case when equation (2.4) was fully met. Instead of behaving like a low pass filter, the band-stop property seems predominant at lower values of θ. This property is further exploited in enhancing the band pass characteristics of the UC-PBG structure by creating an additional capacitive node through a defective UC-PBG structure, which is proposed in the next sub-section.
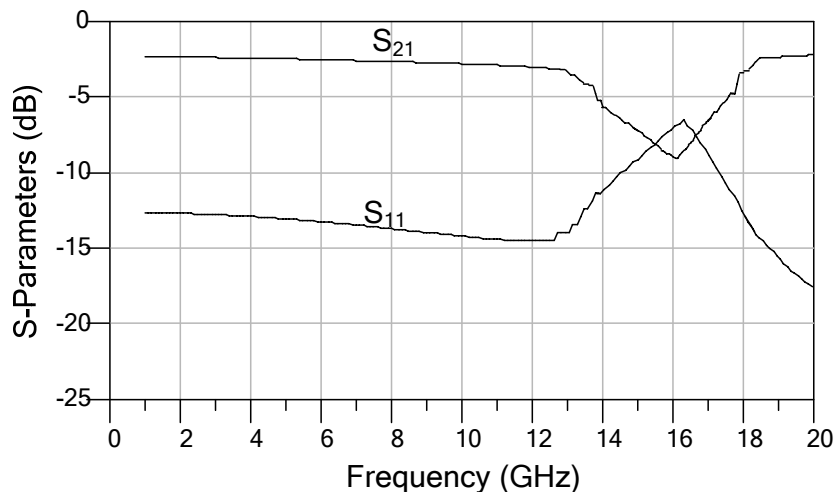
Figure 2.14 S-parameters of the UC-PBG incorporated 50 Ω microstrip line on a 5-metal layer CMOS technology.

2.3.4 Principles of defective UC-PBG

As mentioned in the previous sub-section, a defective UC-PBG (D-UCPBG) structure is based on the principle of exploiting the band stop characteristics of low electrical length UC-PBG in order to obtain high performance stop and pass band characteristics. The defective structure is confined within each cell of a UC-PBG lattice and tends to introduce a series capacitance factor along with the strip length inductance. This accentuates the band pass characteristics leading to more well defined stop and pass bands. The D-UCPBG structure is shown in figure 2.15.
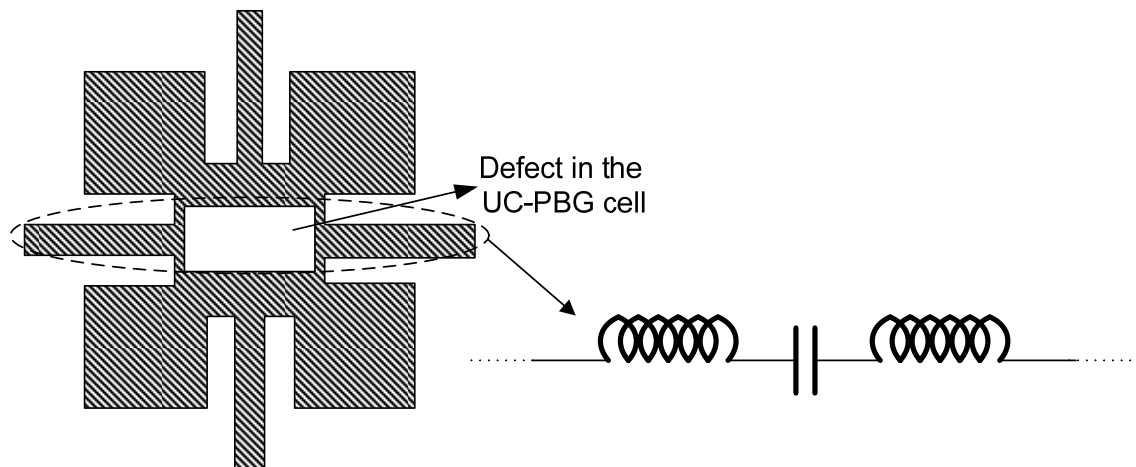
Figure 2.15 Defect in the UC-PBG cell.

An important advantage this structure presents compared to other alternatives - increasing series strip inductance and strip capacitance - is that it doesn't require additional chip area to enhance the net reactive impedance of the ground plane. This approach is therefore quite attractive for CMOS implementation. The D-UCPBG structure could be implemented easily on an M1 ground plane of any standard CMOS

technology while a microwave passive structure could be implemented on the topmost metal layer. The operational principles of a D-UCPBG are demonstrated on a half-wavelength resonator in the next sub-section. A minor drawback of this structure is that it could cause some leakage of electric field into the silicon bulk, but it is not significant enough to damage the circuit performance. In fact, higher quality factors and lower insertion losses are possible using this structure because of the reduction in eddy currents as the continuity of the ground plane is broken by the localized defect.

2.3.5 High-Q D-UCPBG hairpin resonator

The hairpin resonator, shown in figure 2.16 (a), is basically a λg/2 resonator with internal coupling between low characteristic impedance sections that enhances the coupling factor. The even and odd mode characteristic impedances of the shunt arm define the values of Z_p, the shunt arm characteristic impedance, along with the coupling between the two parallel shunt arms. Using the resonance condition for a $\lambda_g/2$ resonator [23]:

$$\theta_0 = \tan^{-1}(\frac{Z_p}{Z_s}).$$
(2.6)

where θ_0 is the optimum resonant electrical length (ideally $\theta_0 = \theta_p = \theta_s$), with Z_s being the series arm characteristic impedance, a set of resonant impedance values corresponding to the shunt and series arm characteristic impedances for a given frequency can be derived. The resonance condition can be derived through an elementary analysis on figure 2.15 (a).

Consider the basic stepped impedance $\lambda_g/2$ resonator structure shown in figure 2.17. The input admittance at any of the two ends when the other end is open is given by [23], [46]:

$$Y_i = jY_P \cdot \frac{2(R_Z \tan\theta_s + \tan\theta_p)(R_Z - \tan\theta_s \tan\theta_p)}{R_Z(1 - \tan^2\theta_s)(1 - \tan^2\theta_p) - 2(1 - R_Z^2)\tan\theta_s \tan\theta_p}. \qquad (2.7)$$

wherein R_Z is the shunt to series impedance ratio, Z_p/Z_s. If the electrical lengths of the shunt and series arms are equalized, then (2.7) can be rewritten as:

$$Y_i = jY_P \cdot \frac{2(1 + R_Z)(R_Z - \tan^2\theta)\tan\theta}{R_Z - 2(1 + R_Z + R_Z^2)\tan\theta}. \qquad (2.8)$$
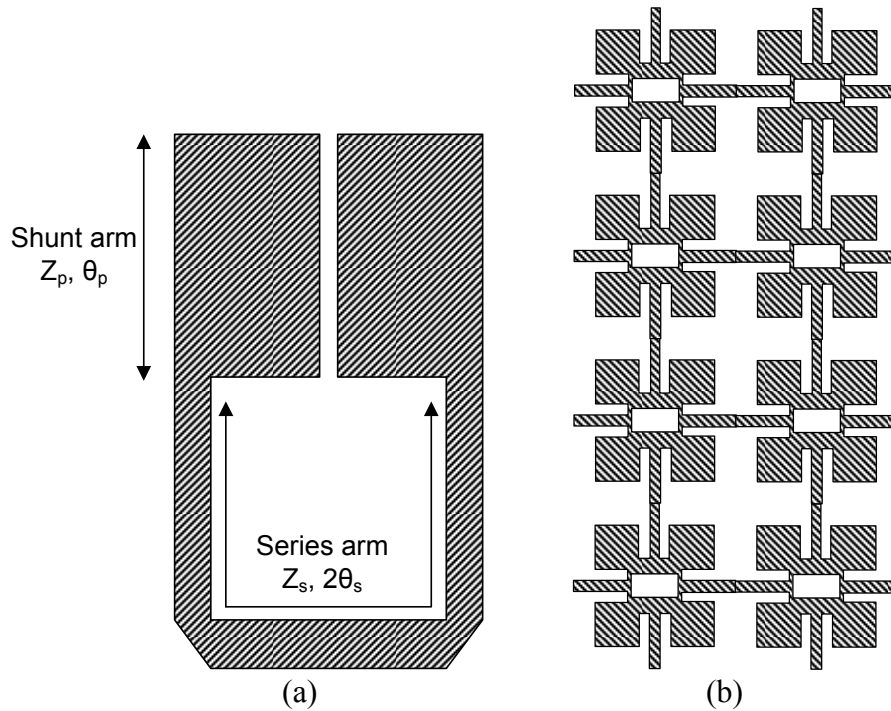
Figure 2.16 (a) Hairpin resonator on top metal and (b) 2 x 4 D-UCPBG lattice as ground plane.

From which the resonant condition is obtained by equating Y_i to zero as:

$$\theta_p = \theta_s = \theta_0 = \tan^{-1}\sqrt{R_Z} \qquad (2.9)$$

For the case of total electrical length of the resonator being exactly half-wavelength, the resonance condition becomes:

$$\theta_T = 2(\theta_s + \theta_p) = 4\tan^{-1}\sqrt{R_Z} = \pi$$
$$=> R_Z = 1 \qquad (2.10)$$

Equation (2.10) indicates that in the ideal case of total resonator length being exactly half wavelength, the impedance of series and shunt arms become equal or the resonator becomes a uniform impedance resonator.

The design of a hairpin resonator on CMOS involves some important considerations. Firstly, the shunt to series impedance ratio is fixed by the resonant frequency of the circuit. This implies that the maximum achievable impedance ratio allowed by CMOS would conflict with some miniaturization requirements. This is because it is highly desirable to seek as low an impedance ratio as possible in order to minimize the net electrical length of the structure. Secondly, the two shunt arms that behave as a pair of
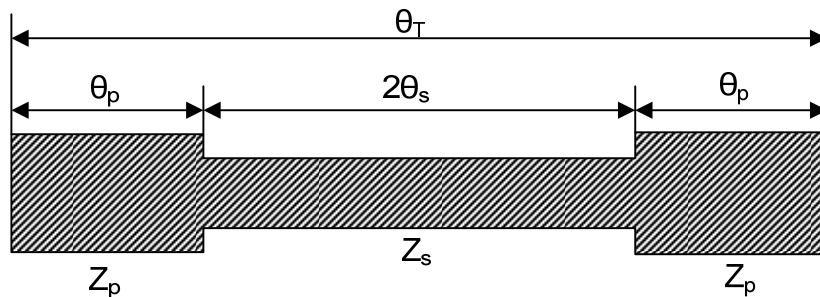
Figure 2.17 Basic Stepped impedance resonator [23].

parallel coupled lines experience even and odd mode characteristic impedances with

unequal phase velocities. Therefore, the characteristic impedance of the shunt arms would be characterized by even (Z_{pe}) and odd (Z_{po}) mode impedances that need to be calculated before hand. Finally, the most important design consideration is that the resonator itself should be first designed on a broad solid ground plane to allow effective confinement of the electric field and prevent field dispersion into the silicon substrate.

Based on these considerations, the impedance ratio was chosen as 0.4 after estimating the even and odd mode impedances as well as the coupling factor between the two shunt arms. The even and odd mode impedances were calculated after allowing the tightest coupling possible based on the TSMC 0.25 μm CMOS process [47] design kit rules for minimal top metal spacing. After adjusting for frequency of operation, IE3D simulations enabled the estimation of optimal parameter values: Z_s =50 Ω, Z_p =20 Ω, θ_s = 32° and θ_p = 78° [48]. These parameters were then incorporated into the EM simulator IE3D to perform a full wave EM analysis and fine tune the resonator dimensions. In all these simulations, the structure of the standard TSMC 0.25-μm CMOS was employed, using the bottom Metal-1 layer for the finite solid ground plane or D-UCPBG ground plane and the topmost Metal-5 layer for the hairpin structure.

A 1 x 20 lattice of a D-UCPBG structure, similar to the one described in sub-section 2.3.4 with a=230 μm, b=250μm, s=g=10 μm and h=50 μm, similar to the miniaturized UC-PBG described in sub-section 2.3.3 is also implemented. The structure is ensured to match the design kit rules of the TSMC technology and designed by consecutive FDTD optimization.

Based on the above design procedure, two resonators, one with a D-UCPBG ground

plane and another with a solid ground plane, were fabricated using the TSMC 0.25 RF-mixed signal process. The dimensions of each resonator are 4.96 x 0.55 mm. The CMOS D-UCPBG incorporated hairpin resonator employs multiple 230 x 230 μm D-UCPBG cells in the ground plane, each incorporating a 100 x 60 μm rectangular defect. Figure 2.18 shows the Cadence layouts for these resonators.

(a)

(b)
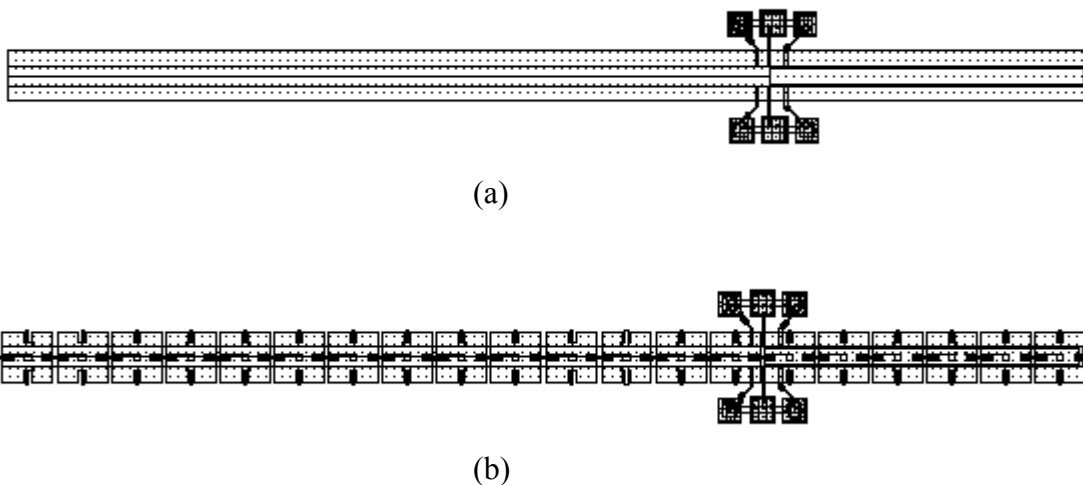
Figure 2.18 Cadence layouts of the CMOS (a) solid-ground and (b) D-UCPBG ground hairpin resonators including on-wafer probe pads. The hairpin structure is on the top (Metal-5) and the D-UCPBG or solid ground is on the bottom (Metal-1), both connected to the on-wafer pads with CPW segments [48].

It should be noted that though the size of the resonator is exorbitantly large from a CMOS perspective (e.g., with respect to a lumped-element resonator), it has been significantly scaled down compared to similar hairpin-resonator circuits implemented without the PBG slow-wave structure. This fact signifies the usefulness of incorporating PBG-based slow-wave structures into transmission-line-based CMOS RF ICs, particularly for large RF ICs such as on-chip transceivers and at millimeter-wave
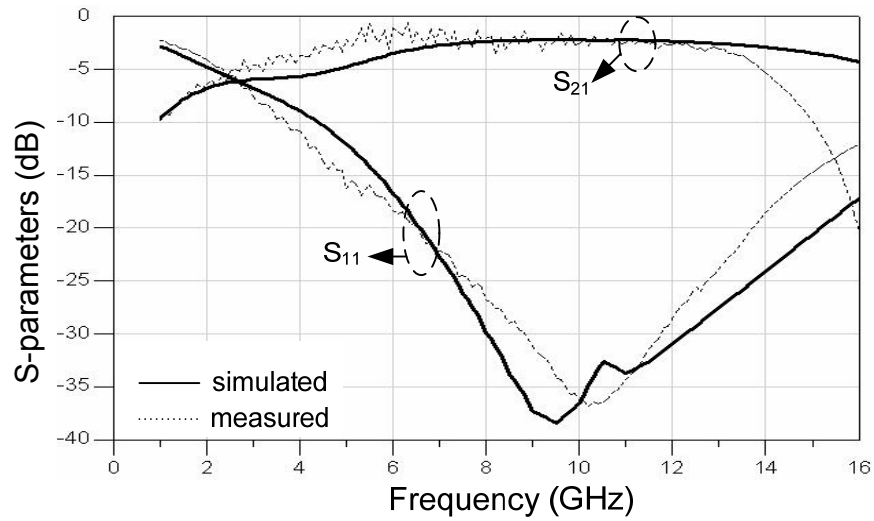
(a)
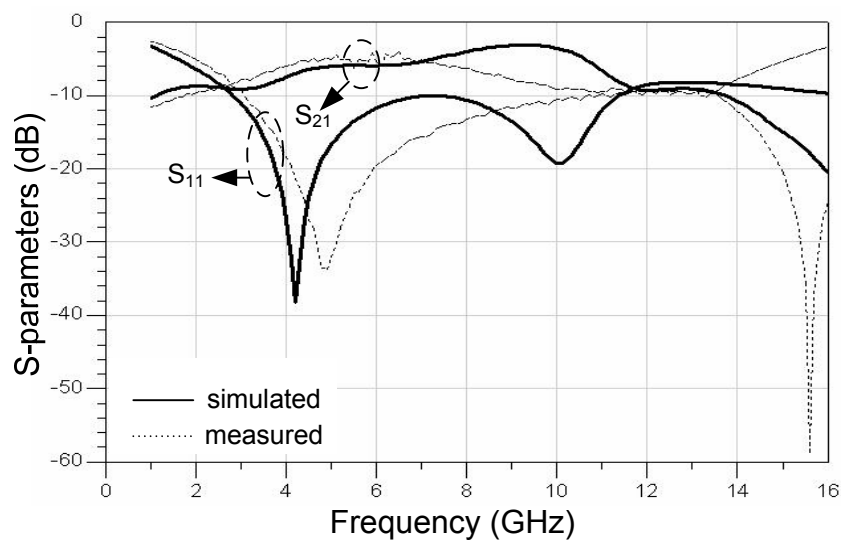
(b)

Figure 2.19 Simulated and measured S-parameters of (a) solid ground plane based hairpin resonator and (b) D-UCPBG ground plane based hairpin resonator [48].

frequencies.

Measurements were performed using a vector network analyzer and on-wafer probes.

Both the measured and calculated results are shown in figure 2.19. The measured results

in figure 2.19 (a) show a deep stop-band rejection of –36 dB at 10.2 GHz for the solid ground resonator. When the solid ground was replaced by the D-UCPBG slow wave structure, the resonant frequency shifted to 4.5 GHz, improving the Q while approximately retaining the stop-band rejection value. A reasonably good agreement between the calculated and measured results is also obtained. It should also be noted that, in figure 2.19(b), the measured result shows no resonance at the second harmonic in contrast with that calculated.

Simulated and measured results signify the advantage of slow wave in microwave passive circuit design. It is immediately observable that the resonant frequency drops by well over 50% due to the presence of the D-UCPBG ground plane. The stop band condition is now satisfied at a resonant frequency of 4.5 GHz, compared to 10.2 GHz for the hairpin resonator with a solid ground plane. Since, both the resonators were of similar dimension, it implies that a structure proportionally scaled down and incorporating a D-UCPBG structure would resonate at the same frequency as a solid ground plane based hairpin resonator. That is, the circuit size is effectively reduced by the presence of the D-UCPBG resonator.

Further more, the quality factor of the resonator was also found to be effected by the presence of the D-UCPBG ground plane. To estimate the loaded Q of the two resonators, the magnitude of the input impedance was calculated from the measured S-parameters and the Q value was obtained from the resonant frequency fr and the 3-dB bandwidth as:

$$Q = \frac{f_r}{\Delta f} \hspace{4cm} (2.11)$$

The resonator quality factor was found to increase from 5.8 to 13 as a consequence of the D-UCPBG structure. The D-UCPBG structure's Q-enhancement property could be explained by the reduction in eddy current losses caused by the rectangular cavity, which minimizes the formation of large ground plane currents.

Applications of D-UCPBG and other slow wave structures are still being investigated on CMOS substrates. However, as the above structures point out, the chip area consumed by this structure is exorbitant at the lower end of the microwave domain. Hairpin resonators, while being suitable for tank-circuit like behavior in oscillators, are yet to be explored thoroughly along with other microwave resonators. Currently, the author has not yet found any related publications other than his own, that relate to the development of CMOS hairpin resonator or slow wave structures.

2.4   Multi-layered design techniques

Typically, multi-layered design techniques involve implementing different segments of a microwave passive structure on different metal layers of a monolithic or non-monolithic substrate. As mentioned in an earlier section, multi-layered design techniques were originally pioneered by Robertson et al [10] to scale down the size of a 1.5- 10 GHz broadband coupler. They reported dimensions of at least 1.0 x .8 mm after incorporating aggressive meandering on a GaAs substrate. However, the coupler suffered from poor direct port insertion loss of about -7.5 dB and a very poor phase imbalance of over 10-15° over the entire bandwidth. Other multi-layered design

techniques focusing on size reduction [12]-[14] also faced insertion loss problems. On the other hand, multi-layered design techniques have not yet been exploited in the design of microwave passives in CMOS technology as very little work has been done in the field of implementing distributed couplers and filters in that technology.

In this section, multi-layered design techniques are exploited to the advantage of reducing the size without significant loss and performance deterioration of several couplers. Several passive structures employing multi-layered design technique have been fabricated in standard CMOS technologies and their performance is evaluated. Apart from their application in couplers, this technique is also used in designing a novel multi-layered inductor structure that provides an efficient integration mechanism for application in distributed amplifiers and VCOs.

2.4.1 TFMS broadside coupled Lange coupler

The design, fabrication and analysis of a CMOS novel broadside coupled Thin Film Microstrip (TFMS) Lange coupler is presented here. The Lange coupler, originally conceived by Julius Lange [7] in 1969, is a tight-coupling, low-loss, broad-band quadrature hybrid. In order to obtain tight coupling, inter-digitation was used with multiple strips on the same metal layer. The original structure was unfolded [49] in order to reduce the number of inter-connects and also for the ease of modeling. The two structures are shown in figure 2.20.

The Lange coupler operates on the principle of compensating even and odd mode phase velocities by equalizing the potential at alternate segments. Implementation of a

silicon substrate based Lange coupler can be performed by calculating the even and odd mode impedances for a set of values of the voltage coupling co-efficient. The coupler consists of an even number of inter-digitated edge-coupled lines, and is λ/4 long. The coupler can be characterized by [50]:
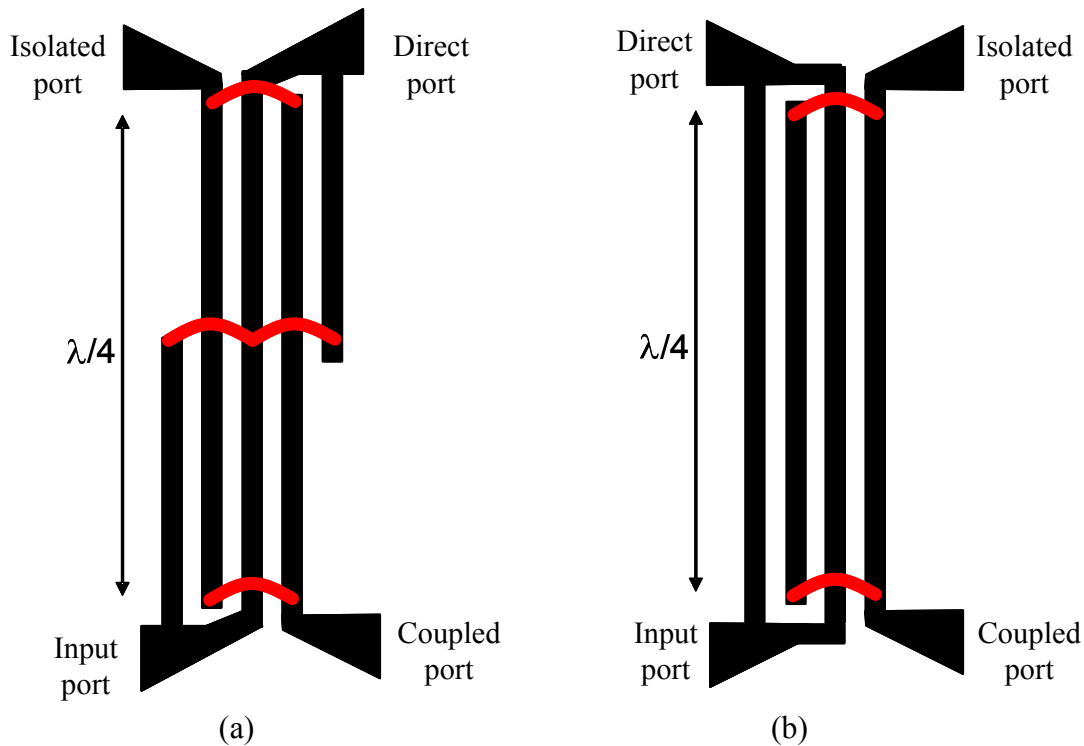
Figure 2.20 (a) Folded and (b) Un-folded Lange couplers with inter-connections shown in red.

$$Z_{0e} = \frac{4C - 3 + \sqrt{9 - 8C^2}}{2C\sqrt{(1-C)/(1+C)}} Z_0 , \quad\quad (2.12a)$$

$$Z_{0o} = \frac{4C + 3 - \sqrt{9 - 8C^2}}{2C\sqrt{(1+C)/(1-C)}} Z_0 . \quad\quad (2.12b)$$

where in C is the voltage coupling coefficient at center frequency, Z_0 is the characteristic impedance of each line and Z_{0e} and Z_{0o} are even and odd mode impedances of a coupled line pair. These equations show that for 3-dB coupling (c=0.7), Z_{0e} and Z_{0o} should be 180 and 50 Ω, respectively. A challenge for silicon substrate based Lange design is to achieve the high coupling ratio together with the high impedances, all-the-while satisfying the CMOS/BiCMOS technology design rules. An interesting problem here is that while the large coupling factors require a large even-to-odd mode impedance ratio, matching to 50 Ω roughly requires that the geometric mean of Z_{0e} and Z_{0o} of a 2-conductor coupled line be close to 100 Ω, since a 4-conductor Lange has two of these in
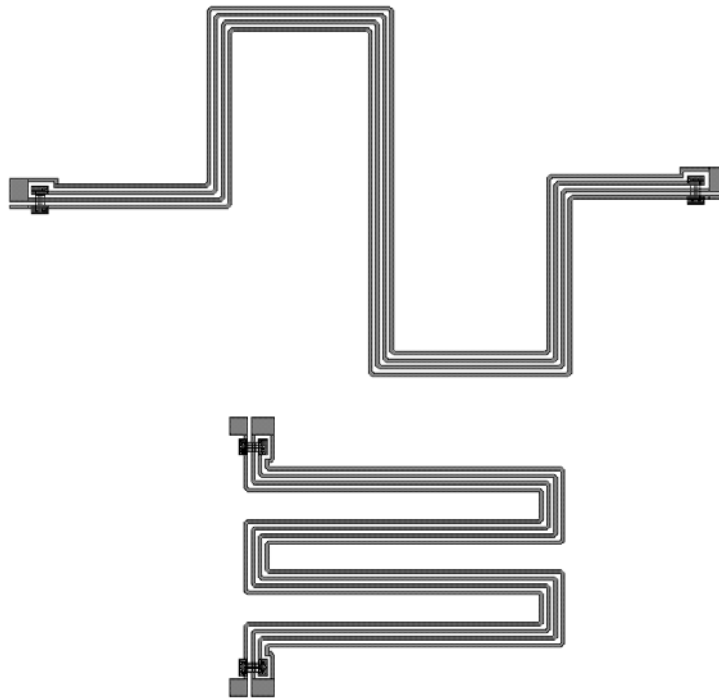
Figure 2.21   Two different versions of silicon based Lange couplers with different kinds of aggressive meandering [51].

parallel. The required impedance ratios were met by implementing the coupler in lower metal layers where the impedance ratio also approximately satisfied the matching conditions.

Using this procedure, CMOS based Lange couplers measuring 300 x 160 μm and 160 x 120 μm at 60 GHz and 140 x 120 μm at 77 GHz were implemented in IBM SiGe 0.13 μm BiCMOS technology [51]. Only aggressive meandering was used as the miniaturization technique. The couplers showed around -4 dB through, -5 dB coupling and less than 10 dB return loss and isolation. Typical layouts of the silicon substrate based Lange couplers are shown in figure 2.21.
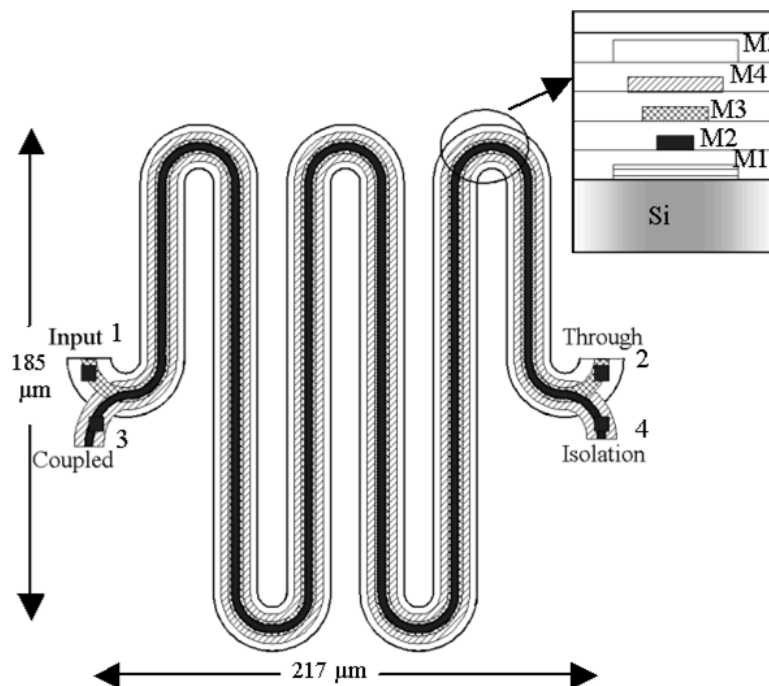
Figure 2.22 Layout of the proposed asymmetric broadside-coupled Lange coupler, with cross-section shown in the inset.   The four fingers are implemented on the top four metal layers (M2-M5).   The bottom metal layer (M1) is used as the ground plane [52].

In spite of the compact dimensions and reasonable performance, there is still a significant scope for further miniaturization and performance enhancement. For instance, the 2 dB loss in the coupling port beckons further improvement. The basic problem associated with this version of the Lange coupler is that it is edge coupled and aggressively meandered. Edge coupling topology doesn't facilitate tighter coupling. Further, using sharp rounded corners serves to only increase the chance of current crowding at higher frequencies.

All these factors serve as a major impetus for looking into novel topologies that could address the above problems. A novel asymmetric broadside coupled multi-layered Lange coupler, shown in figure 2.22, is proposed as a feasible alternative topology that could significantly solve this problem [52]. It implements the unfolded Lange coupler in a broadside-coupled structure to facilitate significant size reduction through simple meandering, while simultaneously enhancing the performance through tight broadside coupling. A major consideration in the design of the broadside-coupled Lange coupler is the treatment of the inhomogeneous and asymmetric nature of the structure, which prohibits the occurrence of even and odd modes [53]. Earlier Lange design procedures by Ou [54] and Paolino [55] cannot be used. Furthermore, in order to obtain similar characteristic impedance for each finger in the multilayer broadside-coupled structure, different widths need to be used, owing to their differences in distance to the ground plane and in the Oxide dielectric layers surrounding them. This further adds an asymmetric dimension along the broadside configuration.

The design was carried out by individually calculating the effect of the ground plane

(M1) on each finger. The coupling effect of the two adjacent fingers for the second (M4) and third (M3) fingers was also taken in account. It is evident from the cross-section of the structure that the top finger (M5) is not particularly affected by the bottom two fingers (M3 & M2), and the bottom finger (M2) is not strongly affected by the top two fingers (M5 & M4). This fact has been exploited to simplify the design by assuming the presence of only one finger (M4 or M3) adjacent to the top (M5) or bottom (M2) finger, respectively. A full wave EM analysis was then performed using IE3D [44], an FDTD tool, aiming for the basic impedance matching criteria for a set of adjacent parallel-coupled lines. Table 2.2 shows the possible widths for each finger obtained by this assumption.

The values in parenthesis for the widths in Table 2.2 are the optimized numbers

Table 2.2 Coupling and width estimation from EM analysis

Finger Layer	Coupling Layer	Width (μm)		Estimated coupling to adjacent layer (dB)
M5	M4	6-8	(7.8)	0.93
M4	M5, M3	4-7	(5.7)	0.6
M3	M4, M2	2-4	(3.4)	0.6
M2	M3	1-1.5	(1.0)	0.8

obtained after all four layers were incorporated together in EM simulation and after the widths were adjusted for impedance match and 90° phase difference conditions. Coupling (C) for each pair of adjacent fingers was calculated with another round of full wave EM analysis from S-parameters ($C = S_{ij}/S_{kj}$, where i, j and k are port numbers).

They indicate the tight coupling facilitated by the broadside topology. It must be noted that the coupling (as well as EM fields) for M4 and M3 is distributed unevenly between the two adjacent layers. The mathematical expressions for these coupling factors could be derived from the basic theory of broadside-coupled microstrip lines by assuming asymmetric lines, while solving the Green's functions for [L], [R], [C] and [G] matrices using a quasi-TEM analysis [56]. The Green's function could also be solved for the capacitance matrix in the method provided in [57] for multilayer transmission lines. The equalization of characteristic impedances of each line was necessary to obtain
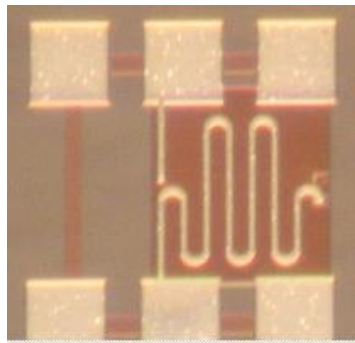
Figure 2.23 Die photograph of the fabricated Lange coupler (217 x 185 μm without RF pads).

impedance-match to the 50 Ω ports. This required that the widths be so optimized that they simultaneously provide 50 Ω in parallel. Estimated characteristic impedances were about 48 Ω at the input of each port, which satisfies the matching criteria.

The four-finger broadside-coupled Lange coupler, shown in figure 2.22, was fabricated on the TSMC 0.25-μm CMOS process [47]. The strip widths are indicated in Table 2.2, while the electrical length of each strip is estimated as 1238.5 μm based on
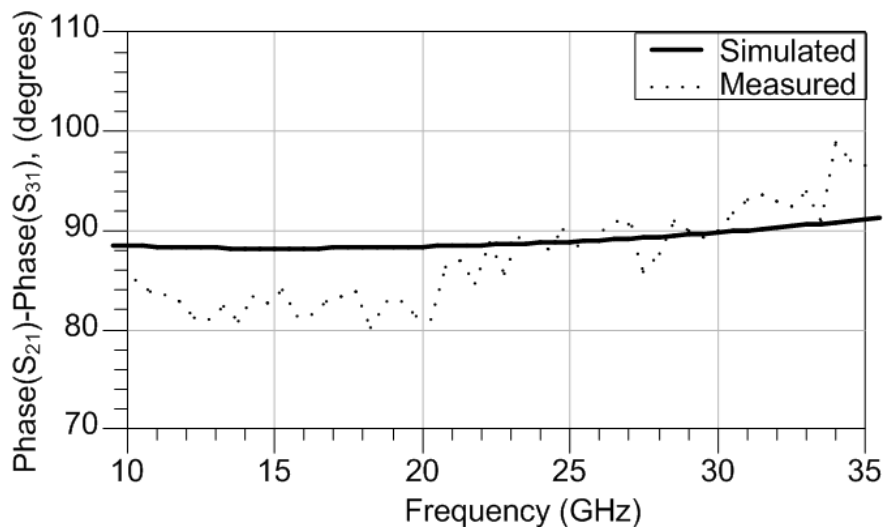
Figure 2.24 Phase imbalance of the through and coupled ports. 1: input,
2: through, 3: coupled, and 4: isolated port.

the λ/4 length requirement. The distances between adjacent metal layers, including the ground-plane metal, are the same and dictated by the CMOS fabrication process. The structure was meandered in order to make it more compact. Circular corners were used instead of rectangular corners in order to avoid field crowding effects at high frequencies. The vias were connected through a meandering arc between alternate multi-layers, that is, between M5-M3 and M4-M2, which could be easily de-embedded numerically as they introduce only a minor phase shift in the measured results. The fabricated structure is shown in figure 2.23.

For an easier 2-port calibration and measurement purposes, three different couplers were laid out for two-port through, coupling, and isolation configurations. The results are shown in figures 2.24-2.26. The measured results show a broadband performance
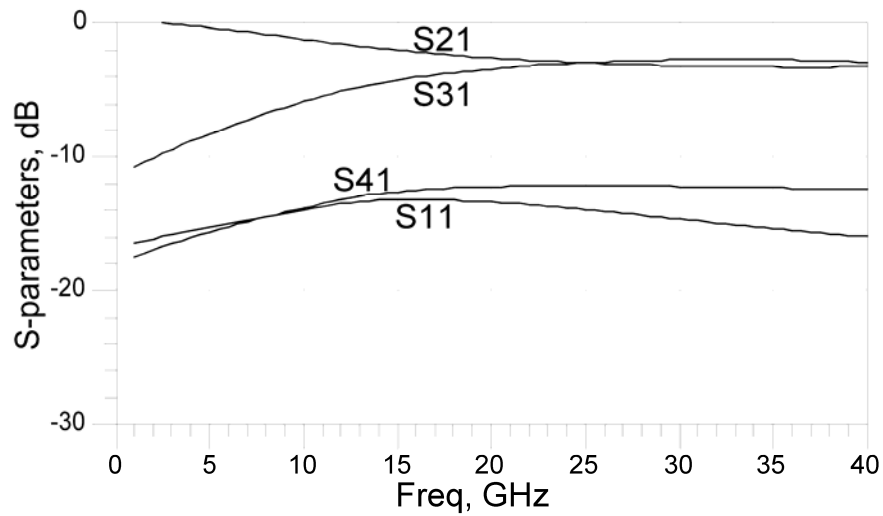
Figure 2.25 Simulated S-parameters of the TFMS multi-layered Lange coupler.
1: input, 2: through, 3: coupled, and 4: isolated port.
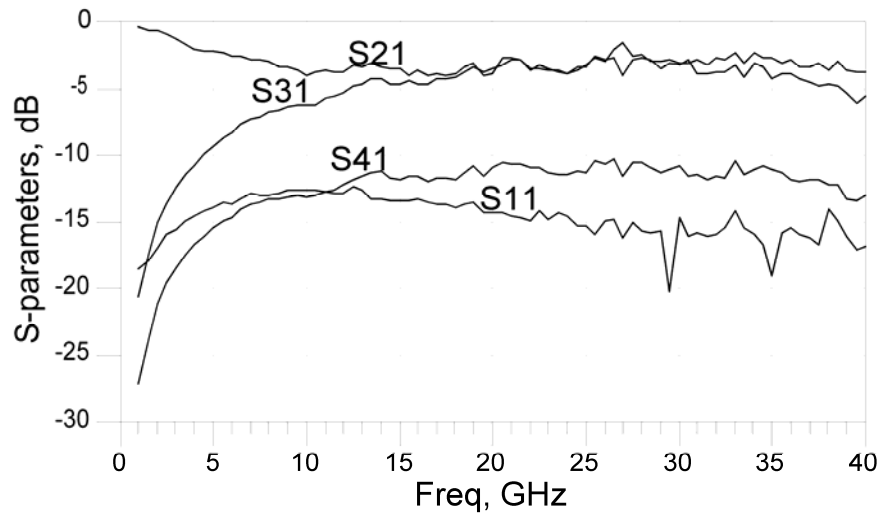
Figure 2.26 Measured S-parameters of the TFMS multi-layered Lange
coupler. 1: input, 2: through, 3: coupled, and 4: isolated port.

and close concurrence with the simulated results. The circuit measures just 217 x 185

µm (without RF pads) which is significantly smaller than any previously reported

implementations in Si CMOS and GaAs MMIC technologies, with respect to frequency, as seen in table 2.3 which compares the size and performance of the broadside-coupled Lange coupler with those recently reported. Measured performance exhibits - 3.3 to - 3.35 dB through, -3.3 to - 3.7 dB coupling, and more than 12 dB isolation and 15 dB return loss across 25-35 GHz. The measured amplitude imbalance is about ±0.35 dB while the measured phase imbalance is 90±4° over the 25-35 GHz range. The excess loss is not significant and attributed mainly to the conductor losses of the fingers, especially

Table 2.3 Comparison with recently published microwave Lange couplers

	Techno-logy	Freq-uency Range (GHz)	Dimen-sion (µm)	Throu gh (dB)	Cou pled (dB)	Isolati on (dB)	Ret urn Loss (dB)	Amplitu de Imbalan ce (dB)	Phase Imbalance (°)
This work	TSMC CMOS	25-35	217 x 185	-3.3 to -3.35	-3.3 to -3.7	<-12	<-15	±0.35	90°±4°
[51]	IBM SiGe BiCMOS	52.5-67.5	160 x 120	-4.3	-5	<-14	<-14	±0.7	90.6°±2°
		62.7-90	140 x 120	-3.9	-5.1	<-14	<-15	±1.2	90°±2°
[58]	MCM-D	10.8-14.9	3020 x 520	-3.35	-3.5	<-20	<-18	±0.2	90.2°±0.9°
		10.2-16.3	3020 x 454	-3.35	-3.4	<-17	<-15	±0.1	91.3°±1.6°
[59]	GaAs	25-39	900 x 260	-3.5	-5.5	-	<-16	± 2	90°±2.5°

those in the lower thin metal layers (M3 and M2), as well as to the non-ideal nature of vias. It is obvious that the current broadside coupled topology presents superior performance even on a lossy silicon substrate while occupying only a fraction of the area reported by other topologies.

2.4.2 TFMS ring hybrid coupler

The ring hybrid or rat-race coupler is a four-port structure which provides 180° phase shifts between its outputs when driven at its differential input port and 0° phase shift between its outputs when driven at its common-mode input port. The traditional ring-hybrid consists of three $\lambda/4$ segments and one $3\lambda/4$ segment, formed into a ring. Previous attempts to realize the ring hybrid on silicon based microwave substrates, by retaining the $3\lambda/4$ arm, have led to exorbitant dimensions [60].
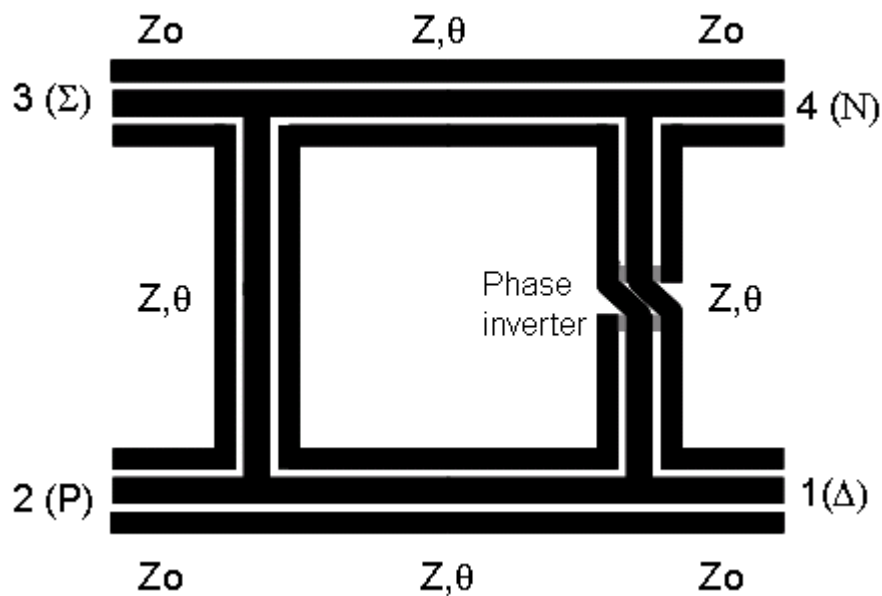
Figure 2.27 Ring Hybrid structure implemented in FG-CPW incorporating a phase inverter.1: Isolation, 2: Output, 3: Input, and 4: Output with 180° phase difference.

Multiple design techniques have been explored to reduce the size of the ring-hybrid. One promising technique employs a phase inverter in the $3\lambda/4$ arm [61], [62]. This is
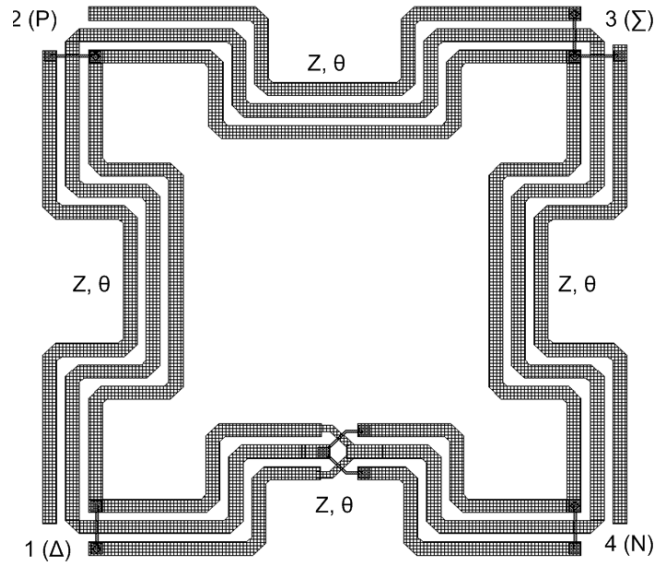
Figure 2.28 Layout of a compact Ring Hybrid structure implemented in FG-CPW incorporating a phase inverter [51]. Each side measures 340 x 340 μm. Interconnects in the phase inverter are implemented by vias.

depicted in figure 2.27, for a Finite Ground Coplanar Waveguide (FGCPW) implementation. A phase inverter simply exchanges the ground and signal traces in the transmission line, providing a 180-degree phase shift. The phase-inverter reduces the length of the 3λ/4 arm to λ/4. Generalizing this λ/4 by a phase shift, θ, the length of these arms can be further reduced by realizing that θ need not be 90 degrees when a phase inverter is used [61]. This leads to a smaller circumference at the expense of bandwidth. The matching criterion for an arbitrary θ is given by [61]:

$$Z = Z_0 \sqrt{2(1 - \cot^2 \theta)} \tag{2.13}$$

where in Z is the characteristic arm impedance and Z_0 is the port impedance. For θ=90$^{\text{o}}$, this reduces to the classic relation Z= $\sqrt{2}Z_0$. An earlier implementation on IBM 8HP
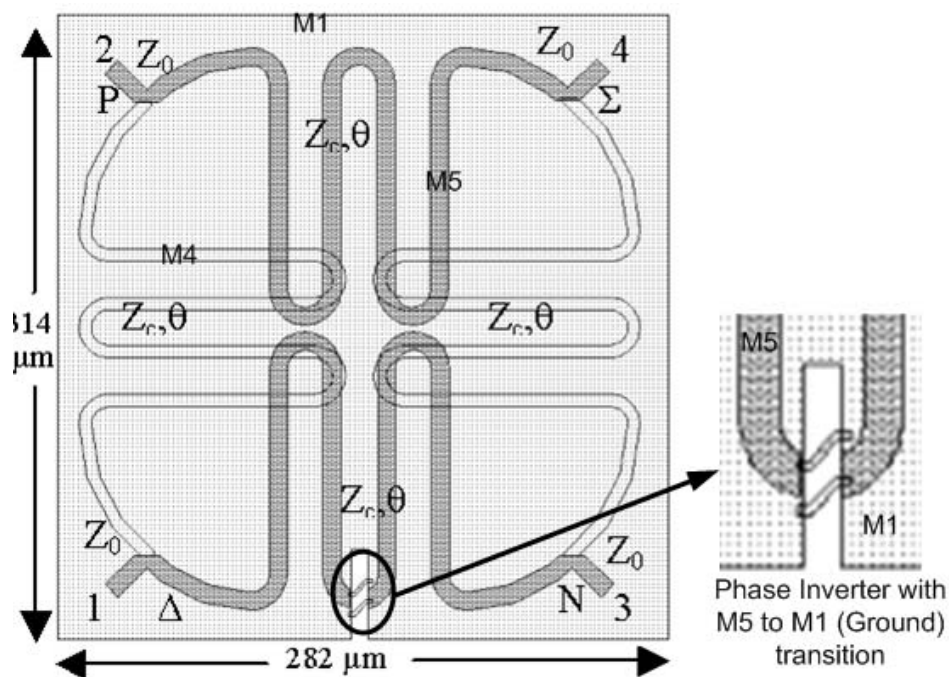
Figure 2.29 An extremely compact multi-layered Ring Hybrid structure using TFMS microstrip lines. [52].

SiGe BiCMOS Back End of Line (BEOL) process exploited this topology for compact dimensions of 334 x 334 μm at 60 GHz [51]. While a FG-CPW topology was used, the structure was meandered to further cut down the dimensions, as shown in figure 2.28.

Noting that even after the incorporation of the phase inverting arm and meandering, the dimensions of the ring hybrid are still large for CMOS, compatibility a novel TFMS ring hybrid has been developed [52]. This structure, shown in figure 2.29, takes the concepts of the natural compactness of TFMS lines compared to FG-CPW lines and the minimal impact of orthogonal EM fields on one another to accomplish an extremely compact ring hybrid structure.

As shown above, the phase inverter compensates for the typical $3\lambda/4$ arm through a $\lambda/4$ arm. The structure was implemented in a 5-metal layer TSMC 0.25 μm CMOS technology. Though each arm of the ring hybrid is $\lambda/4$ long, significant size reduction was obtained through simple meandering as the adjacent arms of the structure are implemented in different metal layers (Metal-5 and Metal-4). In order to maintain similar characteristic impedance in each arm, the width of the branch corresponding to the lower layer must be re-calculated corresponding to its decreased distance from the ground plane (Metal-1). The characteristic impedance of this structure is derived from the relation for a Chebyshev response rat race by numerically solving the admittance matrix in [62] Basically, the procedure involves the development of the even and odd mode equivalent circuits of the rat race structure. By inspection, the ABCD matrices can be deduced and expressed in the form of the admittance matrix parameters. Once we have the ABCD matrix, we can convert them into S-parameters and utilize the conditions for equi-ripple in the pass band. Thus, we have an expression for insertion loss, which involves S-parameters and by virtue of relation through the ABCD matrix – the Y parameters. This mathematical expression is then solved numerically to arrive at an optimum structure for generating a rat race coupler impedance values that exhibit a Chebyshev equi-ripple response in the pass band. This procedure has been mathematically treated in [62] to arrive at the relation shown in equation (2.13).

An interesting property this structure exploits here, which could prove quite useful in the development of novel future multi-layered circuits, is exploiting the fact that two orthogonal magnetic fields do not influence each other as magnetic coupling necessarily

requires a tangential current component. Figure 2.29 shows that each adjacent arm overlaps its neighbor. This overlap spans for 47 μm for each turn and represents 12% of the total length of each arm. However, the transverse layout of the M5 and M4 bends makes the magnetic field generated by currents flowing on each metal to be orthogonal to each other, which effectively minimizes the magnetic coupling between these two arms. The coupling caused by the electric field is also small because the cross sectional area of each line is not more than a few tens of microns, but its impact has not been analyzed through either simulation or experimentation.
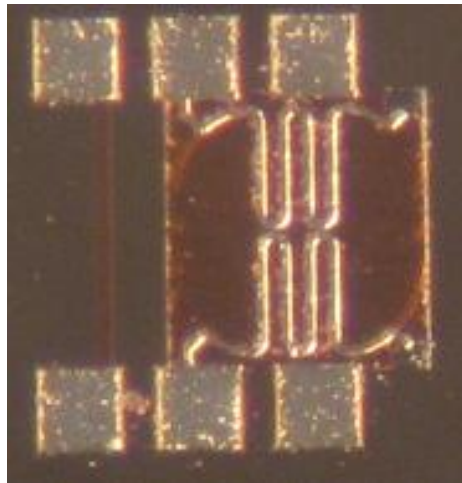
Figure 2.30 Die Photograph of the multi-layered ring hybrid coupler (314 x 282 μm without RF pads).

The design of this circuit was based on estimating the characteristic impedance and electrical lengths according to equation (2.13). For a characteristic impedance Z_c of 50 Ω, the electrical length θ was derived as 54.7° from that expression. However, after subsequent optimization through IE3D based EM simulations, the characteristic

impedance and electrical length were obtained as 48 Ω and 53°, respectively. The widths required to achieve these parameters were simulated from IE3D. The thicker M5 layer has a width of 10 μm while the M4 layer is 7.1 μm wide. Both of them have a similar electrical length of 781.6 μm. The phase inverter was realized with a 10-μm slit in the signal (M5) and ground (M1) planes with via holes connecting M5 and M1 layers through M3.
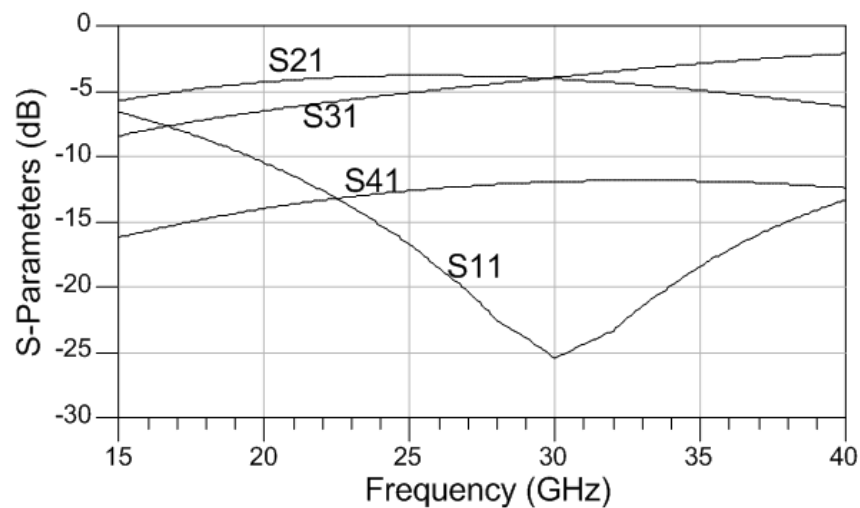
Figure 2.31 Simulated S-parameters of the TFMS Ring Hybrid Coupler.
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Three structures were fabricated in TSMC 0.25 μm CMOS technology order to measure the through, coupling, and isolation. A die photo of a typical ring hybrid is shown in figure 2.30. Since the structure is meandered and exploits the multilayer implementation, a very compact ring hybrid is achieved. The dimensions of this structure are 314 μm x 282 μm without RF pads. Earlier silicon-based ring hybrid had resulted in slightly larger dimensions even at twice the operating frequency [51]. The measured and simulated results are shown in figure 2.31-2.33. The through and coupled

ports exhibit measured amplitudes of –3.1 to -3.18 and –5.1 to -5.7 dB with more than

17 dB isolation between 25-35 GHz, respectively. The excess loss at the coupled port is
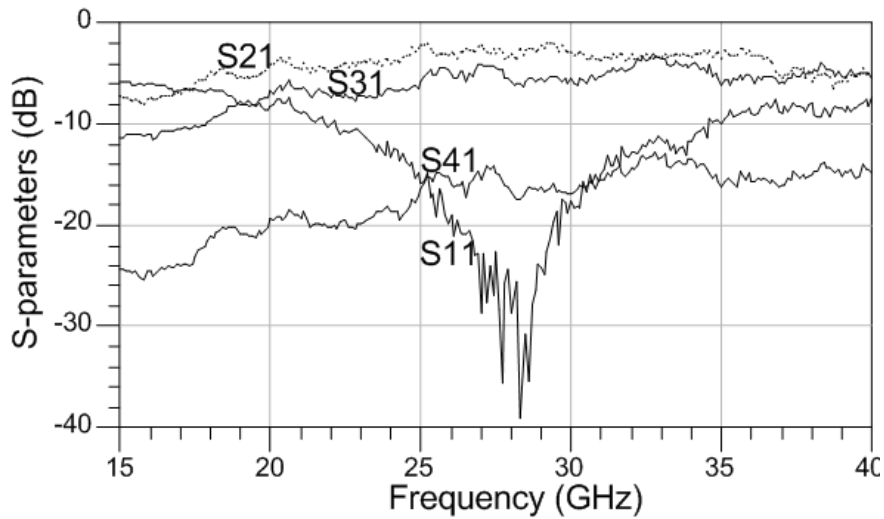
Figure 2.32 Measured S-parameters of the TFMS Ring Hybrid Coupler.
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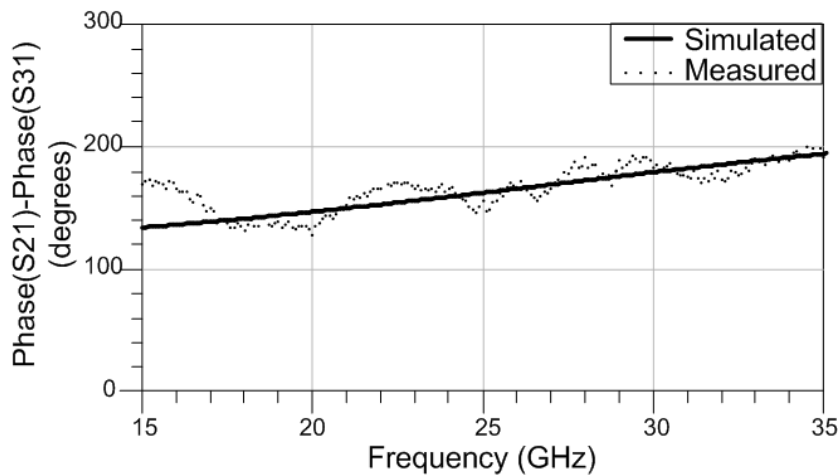
Figure 2.33 Simulated and measured phase difference between coupled and
inversion ports.

attributed mainly to the finite conductivity of the metal layers, the non-ideal nature of

vias, and the phase inverter. This excess loss is, however, a reasonable compromise for

obtaining such extremely compact structures, owing to the significant emphasis placed on chip area in silicon technologies. The structure is very well matched around 28 GHz with the measured return loss remains below 10 dB between 20-35 GHz. The measured phase difference between the through and coupled ports presents a 180° response at 30 GHz with a ±5° imbalance across 25-35 GHz.

It can be noted that previously reported MMIC implementations do not have such significant size compression, as is evident from Table 2.4 which shows some of the recent microwave and millimeter-wave integrated ring hybrid couplers. As mentioned earlier the structure enables over 50% size reduction compared to an already miniaturized ring hybrid structure with similar or superior performance than most

Table 2.4 Comparison with recently published microwave/millimeter wave ring hybrid couplers

	Technology	Frequency Range (GHz)	Dimensions (μm)	Through (dB)	Coupled (dB)	Isolation (dB)	Return Loss (dB)	Fractional Band width	Phase imbalance
This Work	TSMC CMOS	25-35	282 x 314	-3.1 to -3.18	-5.1 to -5.7	<-17	<-10	33%	180°±5°
[51]	IBM SiGe Bi CMOS	53.7-66.3	334 x 334	-4.1	-5.7	<-20	<-15	21%	184°±2°
		68.9-85.1	320 x 320	-4.2	-5.6	<-20	<-15	21%	186°±2°
[63]	GaAs	38-48	800 x 1600	-5.0	-5.0	<-25	<-20	23%	175°±5°
[60]	Silicon with poly mide	10.7-19.2	6000 x 6000	-4.65	-5.05	<-15	<-15	56%	180°±20°
[64]	GaAs	28.8-39.4	850 x 600	-4.1	-4.1	<-20	<-18	31%	180°±2°

published structures.

2.4.3 Vertically coiled inductors

As mentioned in an earlier section, multi-layered inductor design is one of the most extensively researched topic in CMOS based RF and microwave circuit design. Inductors occupy more chip area than every other passive component while playing a critical role in damaging a circuit's performance. Hence, their miniaturization would be inconsequential unless issues of lower quality factor and performance deterioration at higher frequencies are simultaneously addressed. It must be noted that inductor design in itself is a function of the applications they are intended to satisfy. This implies that some performance factors are more crucial than others, depending on the nature of the application. Some circuits like voltage controlled oscillators require high quality factor inductors to reduce the associated phase noise. The emphasis of the current work, on the other hand, is on the improvement of self-resonant frequency of inductors to enable the design of efficient and compact broad band amplifiers. Since we utilize smaller inductances in the design of broadband amplifiers, the quality factor is not significantly deteriorated.
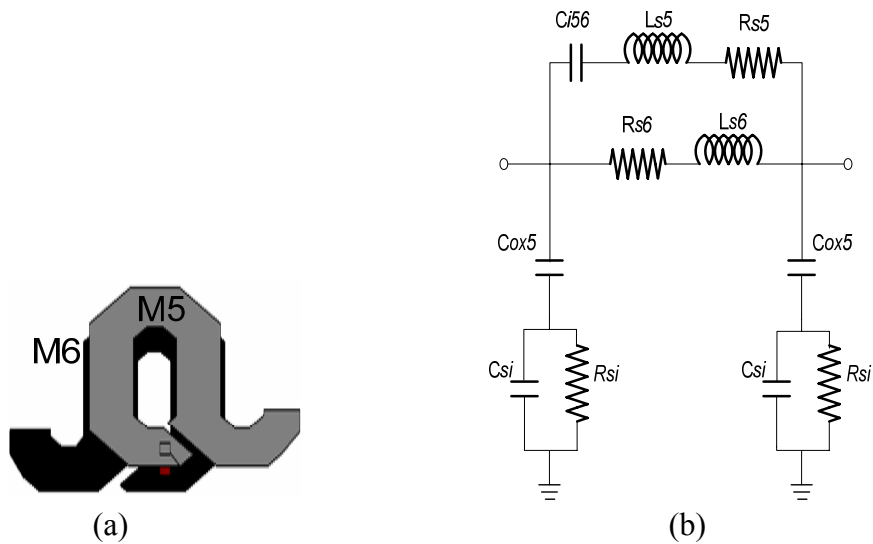
Figure 2.34   (a) Two-layered inductor structure and (b) equivalent circuit.
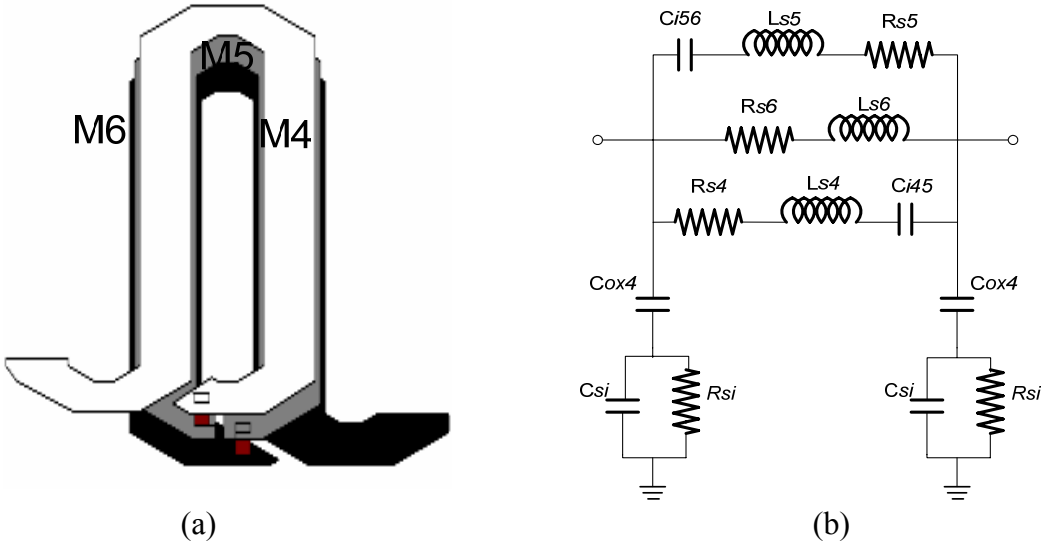
Figure 2.35 (a) Three-layered inductor structure and (b) equivalent circuit.

Figures 2.34 and 2.35 show two proposed multi-layered inductor structures and their lumped-element equivalents implemented on a six-metal Jazz 0.18 μm RF CMOS process [65]. The smaller inductor depicted in figure 2.34 (a) uses only the top two metal

layers – M6 and M5 – while the longer one shown in figure 2.35(a) uses M6, M5 and M4. Both the structures take advantage of the tightly spaced CMOS metal stack, which increases the mutual inductance between the coils without occupying significant area. Further, the thick top-most metal M6, has lower resistivity, which enables reducing the loss associated with each inductor.

The inductor shapes are so designed as to occupy minimum area during subsequent integration. The suggested shape may also ensure minimal impact of induced eddy currents on the segments, as they are implemented on different metal layers. That is because in a traditional spiral inductor, every segment is located on a similar plane which reinforces the overall induced current from them on the ones located directly opposite to them. On the other hand, in a multi-layered inductor, the segments that induce the eddy current are located below a passivating oxide shield, implying that the impact of the field may not be as significant as it would if they were located in a co-planar manner. The inherent nature of their topology with its stacked cells is best suited for realizing smaller inductances as there is a significant negative mutual inductance which prohibits realization of larger inductances. Using smaller inductors also has the intrinsic advantage of being able to realize larger quality factors owing to the lower values of the overall series resistance that is dependent up on the size of the inductors.

The high-frequency equivalent-circuit models suggested in figures 2.34(b) and 2.35 (b) are derived from a modification to the physical model of uni-planar spiral inductors given in [66] after taking the multi-layer effects into account. For simplicity of analysis the two layered structure is considered alone. The inductors L_{s6} and L_{s5} denote both the
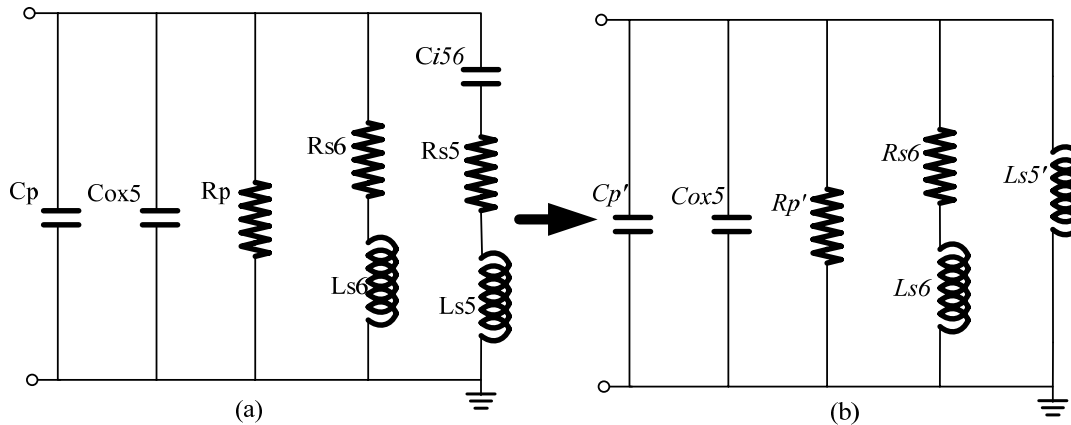
Figure 2.36 (a) One-port model of the multi-layer inductor and (b) simplified one-port model of the multi-layer inductor for analyzing the inductor's self resonant frequency. Cp' is the effective sum of non-oxide capacitances. Ls5' is the series to parallel transform of Ls5 and Rp' is the effective sum of resistances except the series resistance of the 6th layer.

self and mutual inductance manifested by each coil, located on metals 6 and 5, respectively. The respective series resistances are modeled by R_{s6} and R_{s5}. The inter-layer capacitance is denoted by C_{i56} which couples the input to the output through the series inductance and resistance. The oxide capacitance is represented by the capacitance from the bottom-most layer to the top edge of the silicon substrate. Substrate resistance and capacitive coupling are denoted by R_{si} and C_{si}.

To understand the impact of the multi-layer structure on inductor performance, a one-port model of the equivalent circuits can be used as shown in figure 2.36. By estimating the peak magnetic and electric energies and the energy loss in one cycle, the quality factor expression is obtained from figure 2.36 (b) as:

$$Q = \frac{\omega L_{s5}^{'} L_{s6}}{R_{s6}} \cdot \frac{R_p^{'}}{L_{s5}^{'}[R_p^{'} + \{1 + (\frac{\omega L_{s6}}{R_{s6}})^2\}R_{s6}]} \cdot [1 + \frac{(R_{s6}^2 + \omega^2 L_{s6}^2)}{L_{s5}^{'} L_{s6}}\{1 - L_{s5}^{'}(C_{ox5} + C_p^{'})\}]$$

(2.14)

where
$$L_{s5}^{'} = \frac{1}{\omega L_{s5}}\{R_{s5}^2 + (\omega L_{s5} - \frac{1}{\omega C_{s5}})^2\},$$

(2.14a)

$$C_p^{'} = \frac{1}{\omega^2 C_{i56}} \cdot \frac{1}{\{R_{s5}^2 + (\omega L_{s5} - \frac{1}{\omega C_{i56}})^2\}} + C_p$$

(2.14b)

and
$$R_p^{'} = [R_{s5} + \frac{1}{R_{s5}}(\omega L_{s5} - \frac{1}{\omega C_{s5}})^2\}] \| R_p$$

(2.14c)

are the equivalent-circuit elements of the series RLC branch absorbed into the simplified basic model of figure 2.36(a). C_p and R_p are the parallel transforms of the substrate capacitance and resistance similar to the ones derived in [66]. It is implicitly understood that the model presented here is meant for high frequencies in the range of several GHz at which the parasitic substrate as well as inter segment capacitances become prominent enough to influence the overall inductance. From (2.14), the self resonant frequency is determined to be:

$$\omega_0 = \sqrt{\frac{L_{s6}^{'}}{L_{s6}} \cdot \frac{1}{\{L_{s5}^{'}(C_{OX5} + C_p^{'}) - 1\}} \cdot [1 - \frac{R_{s5}^2}{L_{s5}^{'} L_{s6}}\{L_{s6}^{'}(C_{OX5} + C_p^{'}) - 1\}]}$$

(2.15)

which reduces to the expression for the self resonant frequency of uni-planar spiral inductors [115]:

$$\omega_0 = \sqrt{\frac{1}{L_{s6}(C_{OX5} + C_p')} \cdot \{1 - \frac{R_{s5}^2}{L_{s6}}(C_{OX5} + C_p')\}}$$ (2.16)

when $L_{s5}'(C_{OX5} + C_p) \gg 1$. A detailed proof of these equations is presented in appendix A. It is apparent from equation (2.15) that for smaller values of $L_{s5}'(C_{OX5} + C_p)$, ω_0 can attain much higher than in equation (2.16). The increase is substantiated by the frequency-dependent components, L_{s5}' and C_p', which show an inverse dependence on frequency in (2.15). The positive mutual inductance of the other coil located on another metal layer that contributes to L_{s5}' could be further minimized by reducing the coil dimensions to offset the overlapping capacitance that negatively affects the self-resonant frequency of the inductor.

The design procedure aims to increase the inductor's self resonant frequency by optimizing the dimensions of the segments. In order to proceed with the design, the parameters that contribute to multi-layer inductor behavior should be first studied. The most important parameters are the self and mutual inductance of each metal strip on each layer. The overall inductance of a segment could be characterized as:

$$L_{Sx(x=5,6)} = L_{slf} + \sum_p m_p - \sum_n m_n$$ (2.17)

where L_{slf} is the self inductance, while m_p and m_n are the positive and negative mutual inductances as shown in figure 2.37.
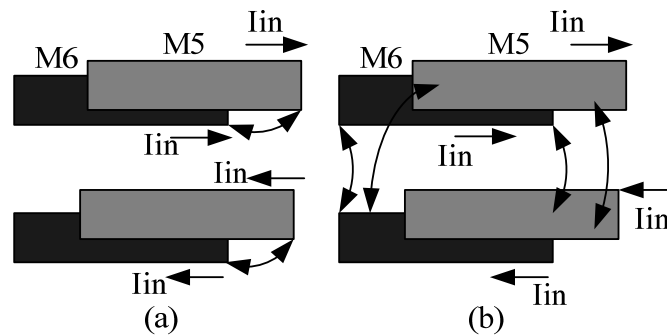
Figure 2.37 (a) Positive and (b) negative mutual coupling in two-layered inductors.

The inductance of the turn is overwhelmingly positive as it is symmetrically placed between both the parallel strips on each metal layer, which neutralizes negative mutual coupling from adjacent parallel strips. The overall inductance represented by each layer is governed by the distance between metal stacks, thickness of each metal layer, the pitch of the inductor turn, the length and widths of both parallel strip, and the number of

Table 2.5 Two layered inductor calculations

Metal layer	Parallel Strip Inductance, nH			Turn Inductance, nH		
	Self	Mutual		Self	Mutual	
		Positive	Negative		Positive	Negative
6	9.07e-3	2.059 e-2	4.84 e-3	1.6 e-2	2.689 e-2	Negligible
5	1.02 e-2	2.059 e-2	4.84 e-3	1.81 e-2	2.689 e-2	Negligible

turns.

The impact of these parameters can be computed analytically using the Greenhouse approach [67] and is tabulated in table 2.5 for the optimum structure dimensions arrived through IE3D iterations. The strong negative coupling associated with the parallel strips is a more important reason behind the reduced overall inductance. Since only three parameters – segment widths and lengths and the pitch of the turn – can be controlled by the designer, the design effect is more evident on the negative mutual inductance than on the positive mutual inductance or self inductance. After fixing the requisite inductance needed from circuit-level simulations, the inductor design challenge is reduced to exploiting the coil dimensions to achieve the desired self resonant frequency. A similar procedure is followed for designing the three layered inductor structure.

An interesting property of these inductors lies in their mutual coupling behavior during subsequent integration. This property is studied in the subsequent chapter on the distributed amplifier, since its integrated behavior proves fruitful in designing extremely broadband circuits with little or no gain ripple.

2.4.4 Complementary slow wave structures

In this section, the concept of complementary slow-wave structures is proposed and subsequently demonstrated on a hairpin resonator, whose Q exhibits a significant increase compared to the case when it only employs a single slow-wave structure while incurring substantial size reduction.

A complementary multi-layered slow-wave structure consists of different sets of slow wave segments that are implemented on different metal layers, such that any circuit implemented on the top metal layers remains completely isolated from the effects of the lossy silicon substrates. The multilayer slow-wave structure includes a complementary image of the bottom ground-plane slow wave structure on the metal layer immediately above it, so that the EM fields emanating from the microstrip circuits (on the top metal layer) are confined to the region between the circuits and the bottom ground plane rather than penetrating into the lossy silicon substrate. The concept is illustrated in figure 2.38. The complementary image pattern is not grounded and left free-floating. Since this
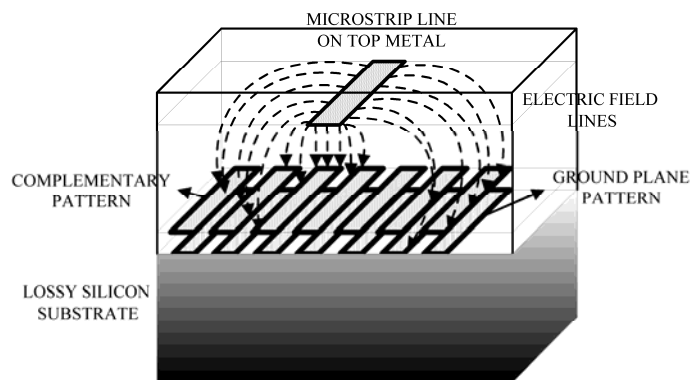
Figure 2.38 Illustration of multi-layer slow wave pattern shielding the top metal passive structure from a lossy silicon substrate. Periodic parallel-strip patterns, different from those used in actual resonators, are used here for the sake of clarity. H-lines are omitted for the sake of brevity.

pattern has a small surface area, any currents induced on it would not be significant. A periodic structure on the ground plane of a microstrip line contributes to an enhancement

of the effective dielectric constant, thereby reducing the phase velocity of the propagating wave. However, this structure leads to partial exposure of the top metal layer to the lossy silicon substrate, thus degrading the Q. In the multilayer slow wave structure the E-field lines are mostly shielded from the silicon substrate by the presence of a complementary image of the structure right above it.

The concept of multi-layered slow wave in silicon CMOS technology is demonstrated on a hairpin resonator with a UC-PBG pattern and its complementary image. The UC-PBG structure was selected because it is a very easily realizable 2-D slow-wave structure and particularly attractive for CMOS monolithic implementation, for reasons already discussed. The resonator is implemented on the topmost metal layer M5, while the complementary slow-wave structures are implemented on M1 and M2 layers. In order to observe the impact of multi-layered structure, three hairpin resonators of similar

(a)

(b)

(c)
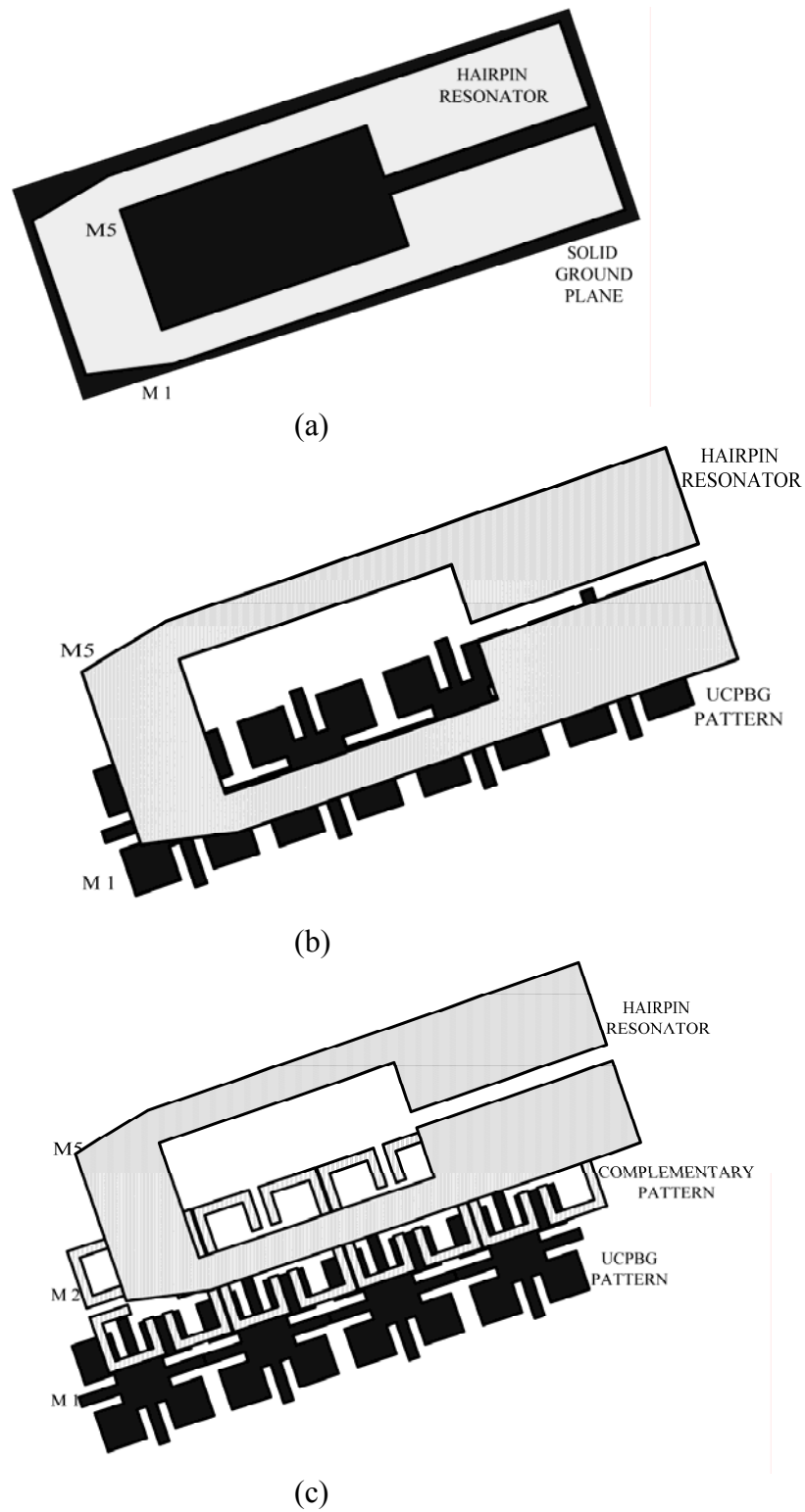
Figure 2.39 Hairpin resonators with (a) solid ground plane (b) UC-PBG ground plane and (c) UC-PBG patterned ground plane with a complementary pattern on top.

dimensions, one with a solid ground plane, other with a UC-PBG ground plane, and another with multi-layered slow-wave structure, were designed. The hairpin resonators were designed following a similar procedure as cited in section 2.3.5 with the values of the series and parallel electrical lengths and characteristic impedances being: Z_s =50 Ω, Z_p=20 Ω, Θ_s= 12°, and Θ_p= 48°. These parameters were then incorporated into the EM simulator, IE3D, to perform a full wave EM analysis and fine-tune the multi-layered UC-PBG resonator. The shunt- and series-arm lengths are 980 μm and 425 μm, respectively. Figures 2.39(a)-(c) depict the hairpin resonators with different ground planes, from solid to UC-PBG and multi layer complimentary UC-PBG. Each resonator is 1405 x 240 μm. While designing the UC-PBG structure, numerical simulations were performed to obtain accurate dimensions for each cell. The slow wave structure was duly miniaturized in accordance to equation (2.6) and the relevant theory discussed in that section. 2 2.

The miniaturized slow wave structure was implemented as a 1 x 6 lattice of 230 x 230 μm size, placed along the length of the resonator with each cell having the dimensions of a=230 μm, b=240 μm, s=g=10 μm, and h=70 μm. Based on these calculations, three hairpin resonators, each with different ground planes as indicated in figure 2.39, were fabricated in a standard TSMC 0.25-μm RF CMOS process. Figure 2.40 depicts the measured and simulated performance of these structures. The UC-PBG structure enhances the effective dielectric constant of the structure and serves as a size-reduction mechanism while the complementary UC-PBG structure further reduces the size and simultaneously provides an enhancement of the Q. The resonator with the solid ground
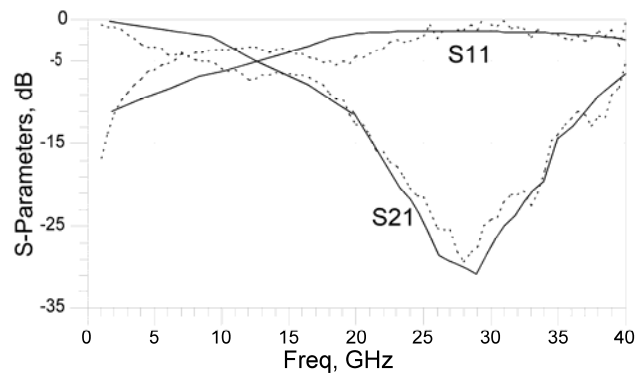
(a)
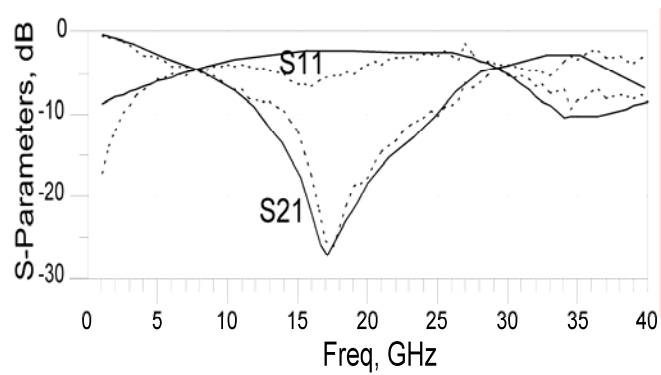
(b)
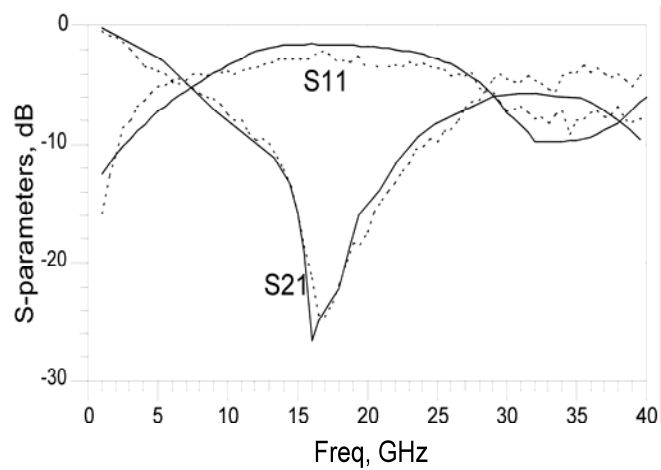
(c)

Figure 2.40 S-parameters of the hairpin resonators with (a) solid, (b) UC-PBG, and (c) multi-layered UC-PBG ground planes. Solid and dotted lines indicate calculated and measured results, respectively.

plane operates at 28 GHz while the UC-PBG incorporated resonator operates at 17.5

GHz. This indicates a drop of 37.5 % implying that a structure proportionally scaled down and incorporating a UC-PBG structure would resonate at the same frequency as a much larger-size resonator using a solid ground plane, thereby validating the size reduction concept. The multi-layered UC-PBG resonator, on the other hand, resonates at 16.5 GHz – lower than the UC-PBG resonator – and also provides a relatively higher Q improvement. The quality factors of the resonators with solid, UC-PBG, and multi-layer UC-PBG ground planes are 10, 11.13, and 14.5, respectively. The increase in Q while retaining miniaturization for the multi-layer resonator vindicates the concept of complementary UC-PBG.

2.5   Applications of microwave passives in CMOS design

Since transmission lines have the inherent advantage of broad bandwidths and excellent matching characteristics, they have immense potential to find applications in a variety of active circuitry. In this section some active circuits incorporating these microwave passives that could prove attractive in a variety of CMOS related design issues are described and issues relating to their CMOS implementation are discussed. Applications of miniaturized multi-layer inductors are presented in the next chapter during their incorporated as artificial transmission lines in a distributed amplifier.

2.5.1   Balanced amplifiers

One of the major applications of Lange couplers in CMOS high frequency design
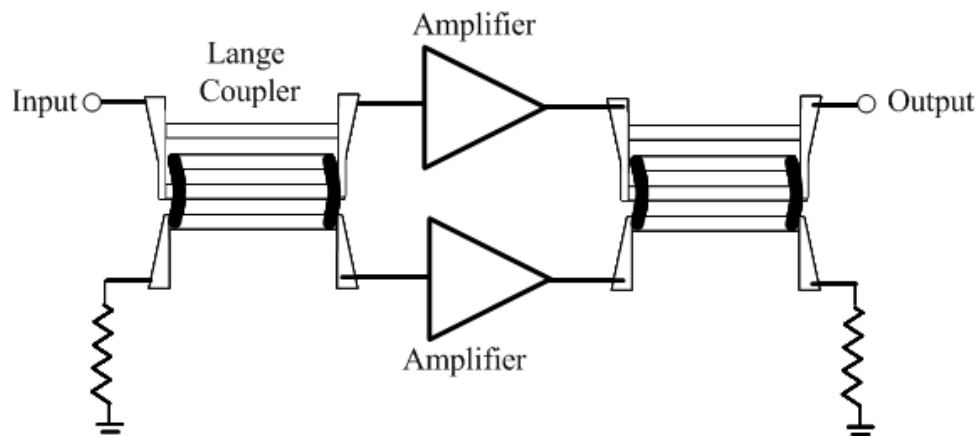
Figure 2.41 Balanced amplifier topology using Lange couplers.

would be in the implementation of high linearity, broadband and excellently matched amplifiers. Typically, in CMOS design, the challenge of obtaining broadband operation is satisfied by designing an amplifier for maximum gain transfer over a wide range of frequencies. However, it is highly difficult to obtain good input and output broadband matching as well as linearity. The balanced amplifier topology solves this problem by using 90° hybrids that cancel out input and output reflections from two identical amplifiers. This is shown in figure 2.41. The first Lange coupler splits the input signal into two equal amplitude components with 90° phase difference. The signals drive two amplifiers which are designed for simultaneous maximum gain and minimum noise, without concern for matching. Their outputs are re-combined by the second Lange coupler. Since the Lange coupler has excellent isolation and return loss at each node,

input matching could be easily accomplished [50]. It should be noted that the bandwidth of this type of amplifier depends on the bandwidth of the Lange coupler. The problems associated with this topology are the increased power consumption and increased chip area. And this is where the miniaturized multi-layered Lange couplers show a lot of potential for CMOS implementation. The miniaturized Lange couplers presented in the current work could be used to design UWB balanced amplifiers with excellent matching, stability, linearity and noise performance. Stability in balanced amplifiers is ensured by the inter-stage matching, as well as by input and output matching over a broad bandwidth because the input and output stages contain Lange couplers that have an excellent return loss property over a broad range of frequencies. Linearity enhancement of balanced amplifiers is also a intrinsic to the topology since the balanced configuration cancels out the two inter-modulation (IM3) products yield a higher input referred third order intercept point [68]. It can also be shown that the gain of a balanced amplifier is the same as each of the identical amplifiers while the noise figure is the average mean of that of its two amplifier constituents [50].

The only major disadvantage in CMOS design of balanced amplifiers, even after solving the chip area problem, would be in the power consumption. A balanced amplifier topology would typically consume twice as much power as a single broadband amplifier while retaining a similar gain-bandwidth product. Since this problem is an unavoidable constraint for this topology, it could be acknowledged as a reasonable trade-off for the considerable gains made in linearity, bandwidth, gain flatness and noise figure, using this topology.

2.5.2   Mixers and phase shifters

Two distinct applications of the ring hybrid coupler that could be useful in CMOS
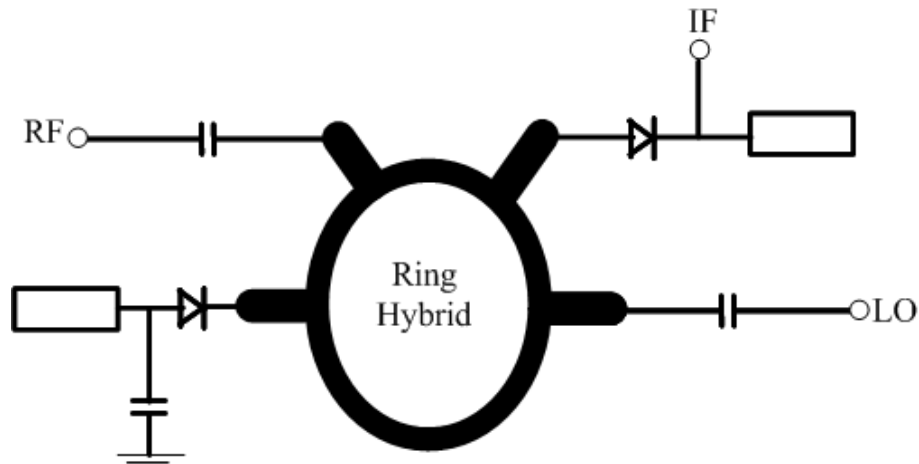
Figure 2.42 Mixer topology using Ring Hybrid coupler for millimeter wave.

design lie in millimeter wave mixers and phase shifters. A simple millimeter wave ring

hybrid based mixer is shown in figure 2.42. This topology has the immediate advantage

of excellent port matching due to the matching properties of the ring structure, which

translates to readily available 50 Ω port impedances for RF, LO and IF signals. RF and

LO ports are located two quarter-wavelengths from each other for better isolation and

prevent spurious LO components from being fed back into the RF input. A quarter wave

length transmission line at the IF port ensures that no RF and LO components are present

at the output over a narrow band of frequency.

Monolithic mixers using ring hybrid couplers have shown reasonable performance in

down converting RF signals up to 94 GHz even though the maximum transit frequency

available in that technology was just 50 GHz [69]. The two significant drawbacks of this topology include size and negative conversion gain. The problem related to the large dimensions could be overcome with the ultra-compact TFMS ring hybrid structure proposed earlier in this chapter.

Another important application of a ring hybrid lies in the development of CMOS size passive Baluns. Till date, the ultra-compact TFMS ring hybrid and its CPW counterpart are the only two distributed passive baluns that have dimensions suitable for CMOS based millimeter wave applications. However, they are not CMOS compatible due to the presence of the phase inverter, which connects the DC ground to the signal line in each of the two implementations. As a consequence any subsequent circuit connected to a
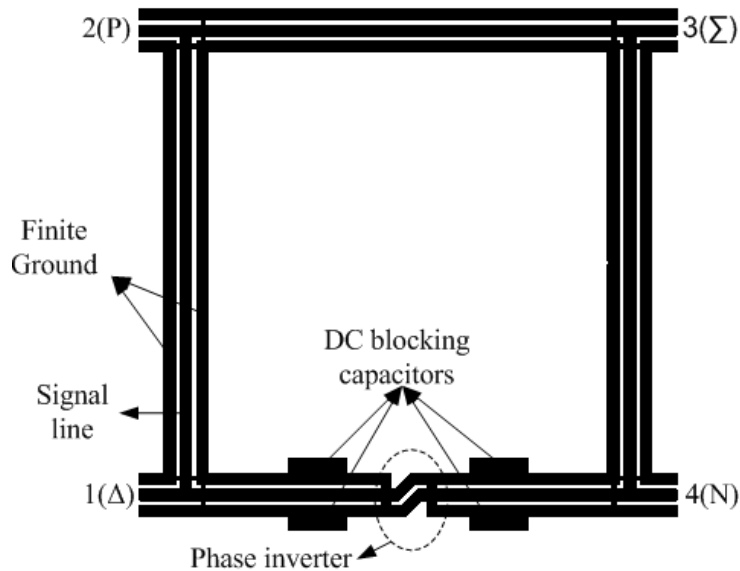
Figure 2.43 A CMOS compatible DC isolated phase inverter for millimeter wave applications [70].

ring hybrid incorporating this Ground-signal phase inverter would require additional DC blocking capacitors at all four ports of the ring hybrid, especially at the common-mode port. An interesting approach is to incorporate DC blocking capacitors within the ground traces of the CPW ring hybrid structure itself so that the signal trace would not be grounded. This minor alteration to the phase inverter incorporated ring hybrid topology makes it CMOS compatible. The CMOS compatible ring hybrid coupler is shown in figure 2.43.

2.5.3 Push-push voltage controlled oscillators

The stepped impedance hairpin resonator finds applicability in the design of microwave and millimeter wave push-push voltage controlled oscillators. A simple topology is illustrated in figure 2.44.

The push-push oscillators typically consist of two identical oscillators which are added 180° out of phase to each other. A parallel coupled hairpin resonator allows only
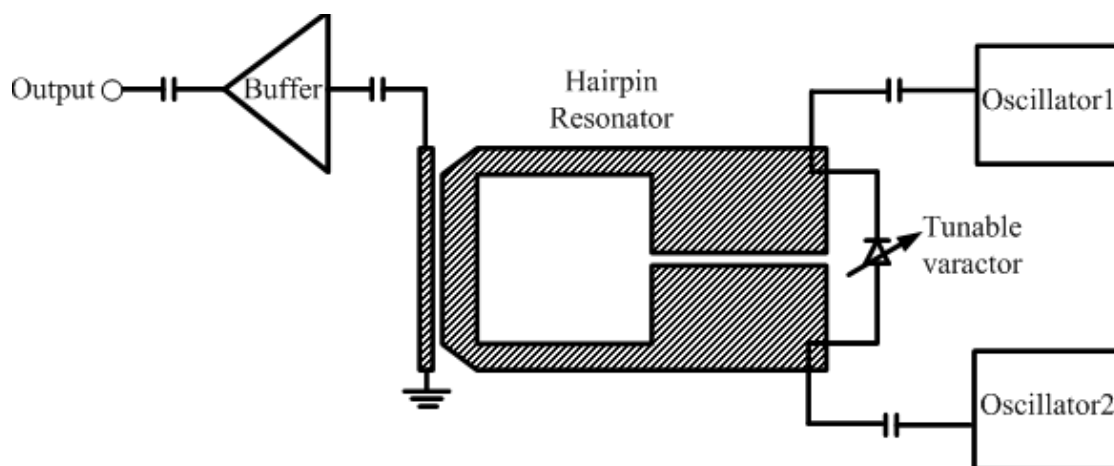
Figure 2.44 A Push-push VCO employing hairpin resonator [71].

one mode of propagation at resonance – either an even or odd mode – implying that if the fundamental resonates at an odd mode, the 1st harmonic resonates at even, so on and so forth. The push-push principle exploits this behavior and combines the first odd mode with the fundamental. This leads to a strong reduction of the phase noise while cancelling out the even mode harmonics.

While considering the design of the above topology in CMOS, the miniaturized versions of hairpin resonators could be accomplished by adding slow wave structures on their ground plane as demonstrated earlier in this chapter. Though the push-push principle leads to superior phase noise over conventional NMOS-PMOS cross coupled pair, it still suffers from a poor chip area and power consumption problems, since two oscillators are now involved and each consuming twice the input power as a single oscillator. However, as the trend towards miniaturization is making rapid strides in all monolithic technologies, the possibility of compact hairpin resonators with over 90% size reduction to the current ones emerging as strong competitors to traditional analog based NMOS-PMOS cross coupled Voltage controlled oscillators cannot be overruled.

CHAPTER III

BROADBAND LOW NOISE AMPLIFIERS

Typically at RF frequencies, wideband amplifiers in CMOS are implemented in one of two ways – shunt/series feedback topology or distributed amplifiers. Both have their own advantages and disadvantages. Distributed amplifiers offer excellent matching, linearity and bandwidth but poor power consumption, large die areas and smaller gain. Feedback topologies face matching problems and poor linearity but offer relatively higher broadband gains at low power consumption and occupy smaller die areas.

The present effort is directed towards implementing a broadband LNA that meets the specifications for a dual band UWB receiver front end. The application solicits broad band low noise amplification of the input RF signal from 3 to 8 GHz, thereby satisfying modes 1 and 3 of the MB-OFDM proposal that shall be discussed in detail in the penultimate chapter. Due to strong interference from existing wireless LAN applications in the mode 2, strong attenuation is required in that region. This also calls for high linearity in addition to broad band width as a defining characteristic of the amplifier.

To meet these requirements, a traditional analog based common source cascode source degenerated low noise amplifier with broad band input and output matching is first designed and its merits and demerits are debated. In the subsequent sections, two novel distributed amplifiers are designed to overcome the shortcomings of the analog based approach and also intend to solve the two major issues related to implementation of distributed topologies on CMOS- power consumption and size.

3.1 Concurrent dual wideband low noise amplifier

Low noise amplifiers are the first circuit blocks that encounter the signal and hence their operation over the RF range determines the performance metrics of the receiver front end sub-system. The current trend towards miniaturization is beckoning designers to seek novel ways in which more and more front end capabilities are integrated into the component level itself. To illustrate this consider a typical super-heterodyne receiver front-end in figure 3.1.
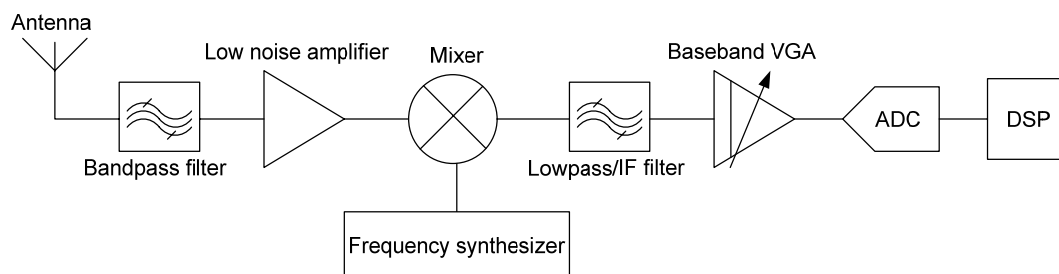
Figure 3.1 Super-heterodyne receiver front-end.

The input band pass filter controls which set of RF frequencies need to be amplified and down-converted to lower frequencies. Now if this topology is designed to operate over multiple set of frequency bands, different blocks of front-end need to be used. On the other hand, if the functionality of front-end components themselves are so tailored, that they operate in multiple bands, there wouldn't be any necessity of having different sets of additional circuits to operate over different frequency bands. A concurrent low noise amplifier exhibits such behavior by *intrinsically* operating over multiple bands of frequencies without the need of any external digital circuitry to control its operation. The
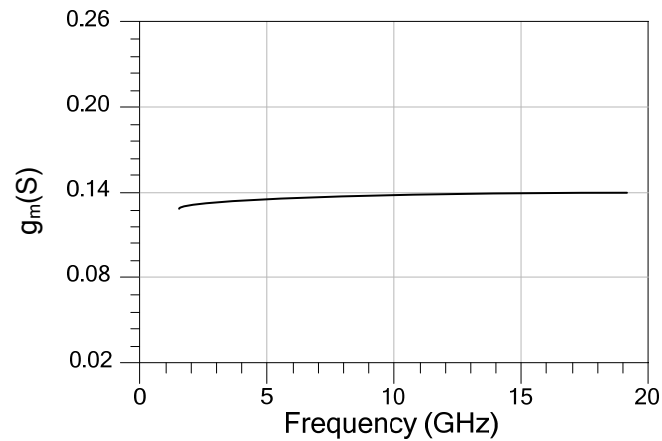
Figure 3.2 Transconductance of common-source NMOS device with 100/0.25 aspect ratio biased in the saturation region.

transfer function of the LNA itself is such that it causes deep stop bands in the frequency bands it doesn't operate and high gain in those that it operates. Typically, concurrent low noise amplifiers have been designed for operation at two different narrowband channels [72]. This section discusses the design of a novel concurrent low noise amplifier that extends this concept to wideband design.

3.1.1   Principles of concurrent dual wideband LNA

Based on the concept of concurrent narrow band LNAs, the concurrent dual wideband LNAs operates more or less on similar principles. The basic idea is dependent on realizing that the transistor's transconductance is inherently wideband and therefore, could be shaped by a filter or internal set of passive components to provide different functionalities. The transistor's transconductance at optimum bias level could be calculated as a function of frequency for a single common source transistor as in figure

3.2. Using some transfer function shaping elements, this wideband property could be exploited in a dual wideband LNA. Figure 3.3 gives the transfer function of a concurrent dual widebanband low noise amplifier. The signal spectra f_A and f_B indicate the incoming RF signal components which are the desired multi-channels that need to be simultaneously amplified. There is a problem associated with this kind of functionality relating to the formation of image of one band in the second one. This problem will be
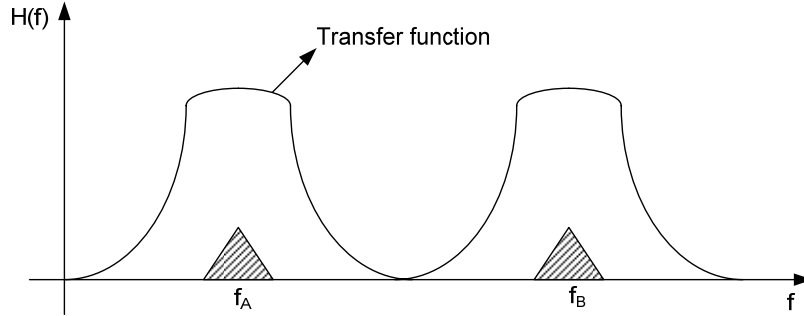
Figure 3.3 Dual wideband LNA transfer function.

discussed in chapter V.

In order to obtain the desired transfer function, a novel source tuning topology is proposed. Consider the common amplifier topology shown in figure 3.4 (a). We can derive an expression for the input impedance of this structure as [72], with Z_g being the gate impedance, Z_{gs} being the gate-source impedance, Z_s being the source impedance, Z_{gd} being the gate-drain impedance and ZL being the load impedance of a generic NMOS transistor in common-source configuration as depicted in figure 3.4(a):

$$Z_{in} = Z_g + Z_{gs} + g_m Z_s (1 + Z_{gs}).$$
(3.1)
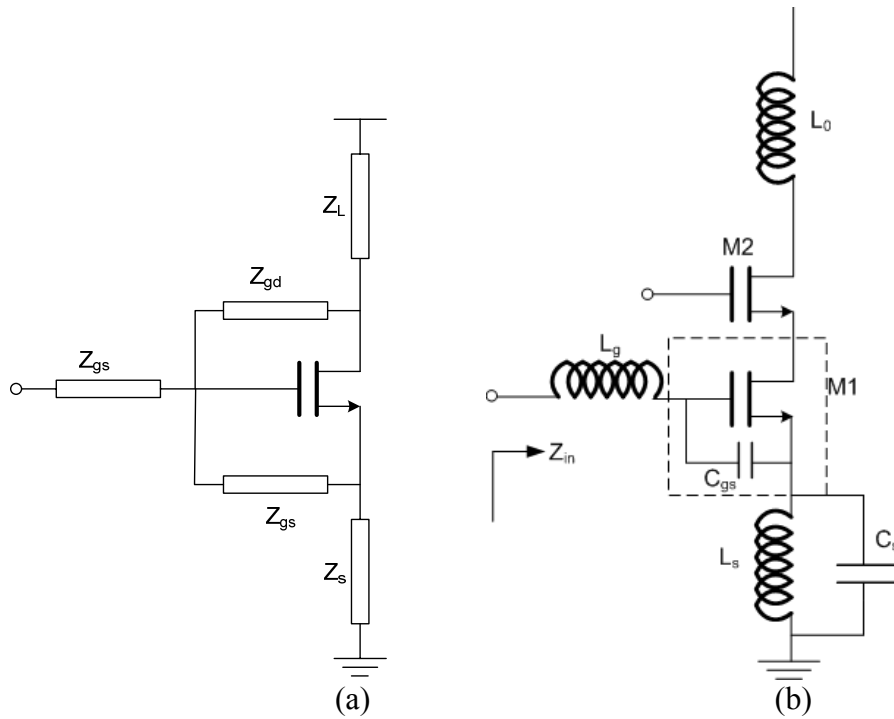
Figure 3.4 (a) General schematic of a common source degenerated LNA (b) A cascode source tuned LNA.

The voltage gain of the same structure is:

$$A_v = \left| \frac{g_m Z_{gs} Z_L}{Z_{in}} \right|.$$
(3.2)

where Z_L is an external load impedance shown in figure 3.4 (a).

Based on these equations, we can obtain the input impedance of the cascode source tuned LNA as:

$$Z_{in} = \frac{sL_s}{1 - w^2 L_s C_s} + sL_g + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}(1 - w^2 L_s C_s)}.$$
(3.3)

At resonance, the reactive part nullifies, while the real term becomes:

$$R_{in} = \frac{g_m L_s}{C_{gs}(1 - w^2 L_s C_s)}. \qquad (3.4)$$

On the outset, it appears that this frequency dependence of resistive part of input impedance might prevent broadband input matching. However, the impact of the frequency component term ($\omega^2 L_s C_s$) is negligible and roughly equal to 0.01 throughout the operational bandwidth and obtained by suitable choice of source inductance, Ls and capacitance, Cs.

The voltage gain expression of (3.2) can be used to derive the voltage gain expression for the cascode source tuned case as:

$$Av = \left| \frac{Z_L}{Z_s} \right|. \qquad (3.5)$$

where Z_L and Zs are the load and source impedances looking into the amplifier. For a typical narrowband concurrent LNA with a multi-resonant output load, the expression could be simplified as:

$$A_v = \left| \frac{Z_L}{Z_s} \right| = \frac{w(L_1 + C_1)}{L_s(1 + (L_1 + C_1)L_2')} \qquad (3.6)$$

where a series and a parallel LC tank are assumed to form a multi-resonant output load. Since the voltage transfer function of the LNA is primarily dependent up on load and source circuits, a multi resonant output load, with each tank circuit operating at the central frequency of a particular band would give the desired operation. However, the same approach fails in the case of a dual wideband low noise amplifier since having

multiple LC resonant tanks at the output would fail to provide dual wideband operation due to the narrow band resonance achieved by each of them.

The problem is solved by using source tuning circuit in an ultra wideband LNA in such a way that it creates a deep stop band in the center of the ultra-wideband LNA, thereby creating two wide frequency bands. As (3.6) indicates, the voltage gain is inversely dependent on the source impedance of the primary transistor of the first stage, therefore a resonant tank circuit at the source would create a stop band, thereby allowing the formation of two distinct UWB bands. The voltage gain of this dual wideband LNA could be obtained using (3.5) as:

$$Z_L = j\omega L_o \tag{3.7}$$

$$Z_S = \frac{j\omega L_s}{1 - \omega^2 L_s C_s} \tag{3.8}$$

Therefore, $\quad A_v = \frac{L_0(1 - w^2 L_s C_s)}{L_s}$ \hfill (3.9)

The source tuning circuit thus relieves the necessity of having multi-resonant output load circuits, which usually require multiple inductors that consume a lot of space and power. The output matching could now be made independent of the load inductor, and additional buffer stage could be used to obtain broadband output matching.

3.1.2   Amplifier design

The topology shown in figure 3.5 gives the schematic of the concurrent dual wideband LNA implemented in TSMC 0.18 μm RF CMOS process. It uses an input
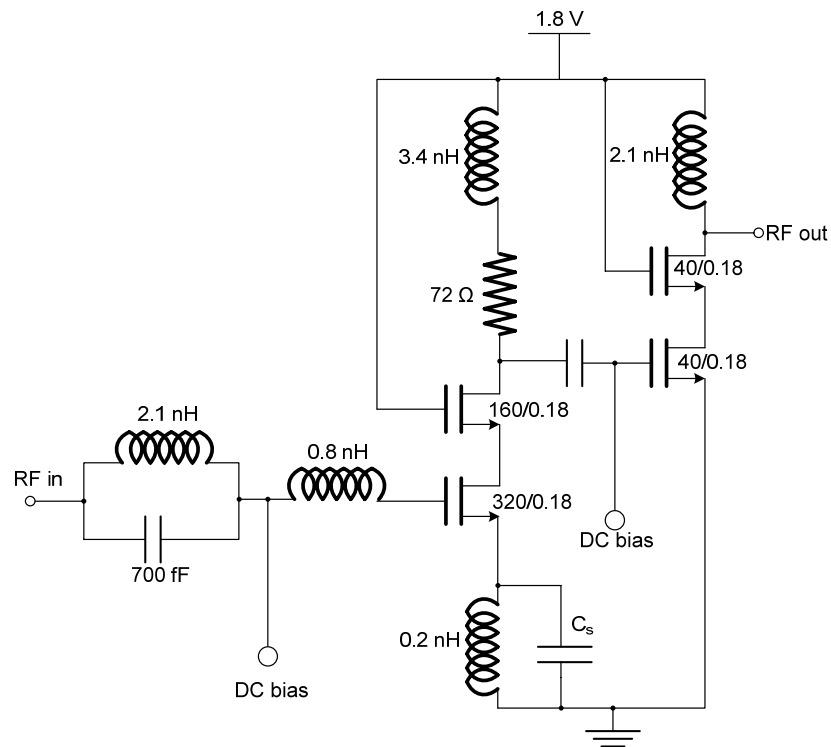
Figure 3.5 Schematic of the cascode source tuned LNA.

resonant tank for matching along with the source tuning network. The input resonant tank provides broad band input matching over the desired frequency range. The necessity of having additional resonant circuit at input arises because the source tank circuit has little impact on input matching as can be observed from (3.9). The cascode structure presents higher reverse isolation and also improves the voltage gain. In order to further enhance the gain a second stage is added. The noise figure is improved following

the same guidelines suggested for a concurrent LNA in [72]. Firstly, the transistor gates, implemented as multiple fingers, must be shorter in width in order to minimize the gate resistance. Their number could be increased in order to increase the width, which could also reduce the gate resistance. However, having a large width would increase the drain current consumption. If the drain current consumption increases, the noise figure worsens as it is inversely related to drain current. Thus, there must be an optimal value of transistor width which could be used to obtain a reasonable noise figure. Another aspect that was taken into account to obtain a minimal noise figure were the inductive losses. In order to minimize those, all the inductors of this circuit were designed and simulated from IE3D, an FDTD EM simulator, and their structures were fine tuned through repeated optimization. In order to further improve accuracy, the connecting metal layers from the inductors to circuit components were also included in the simulations so as to take their effect inductance into account.

3.1.3 Implementation and results

The layout of the cascode source tune LNA is shown in figure 3.6 and the measured results are shown in figure 3.7 (a)-(d). The performance indicates that there is dual wide 3 dB bandwidth of 500 MHz in first band (3.5-4 GHz), while it is nearly 1GHz in the second band (6-7 GHz). The gain in first band is about 7 dB while the gain in the second band varies between 7-9 dB over the 3 dB bandwidth. The circuit provides moderate input matching in both bands over the entire channel range. It can be observed that S_{11} follows the same staggered response as the voltage gain, due to the resonance effect of
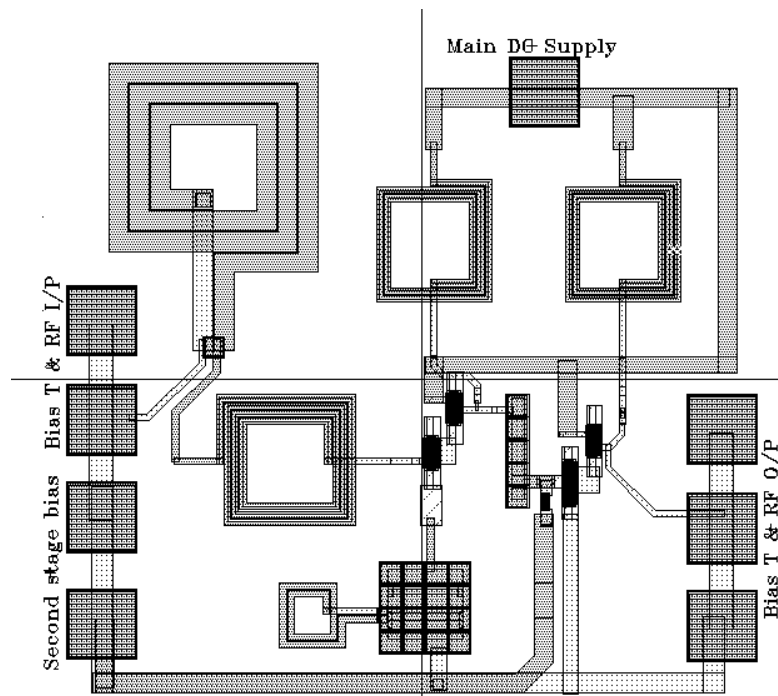
Figure 3.6 Layout of the cascode source tuned LNA.

the input tank as well as the source tank. The minimum noise figure values are 3.2 and 4.5 in the first and second band respectively while the input referred IP3 of the first band is shown in figure with a 100 MHz offset interferer is -12.5 dBm. The circuit consumes only 14 mW of DC power.

While the circuit is able to provide decent gain, matching at a low DC power consumption, the cascode source tuned structure has an important drawback. As the linearity simulations based on post layout simulations indicate, the LNA has insufficient linearity due to the inevitable dependence of small signal gain on the transconductance. This problem is typical of all analog based topologies. The advantage of source degeneration is offset by the usage of a tank circuit at the source, which makes the real part of input impedance dependent on frequency. Further, it has been earlier mentioned
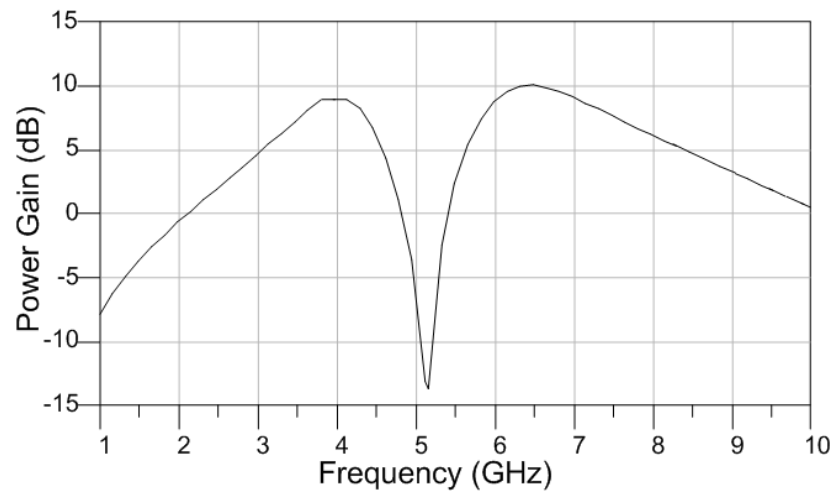
(a)
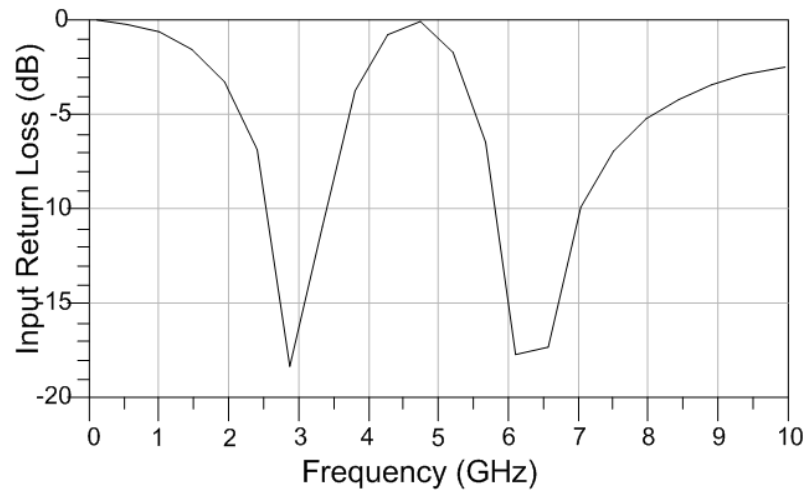
(b)
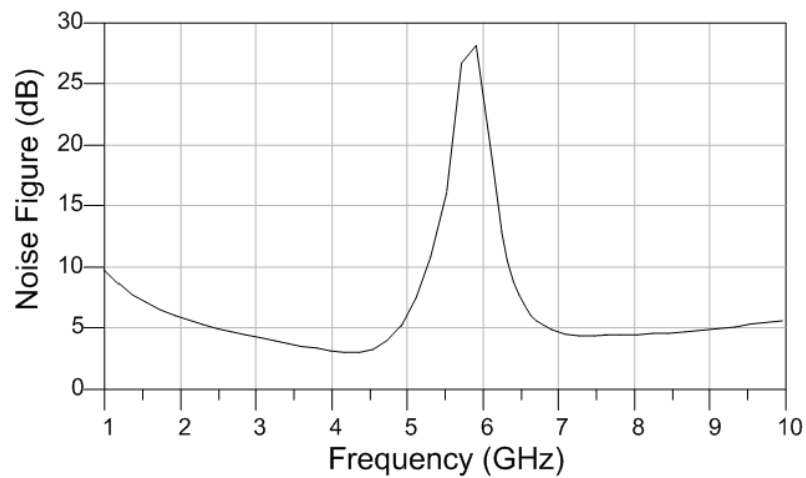
(c)

Figure 3.7 Simulated performance of the LNA (a) Power gain (b) Input return loss (c) Noise figure (d) simulated LNA response showing IIP3 in the first band.
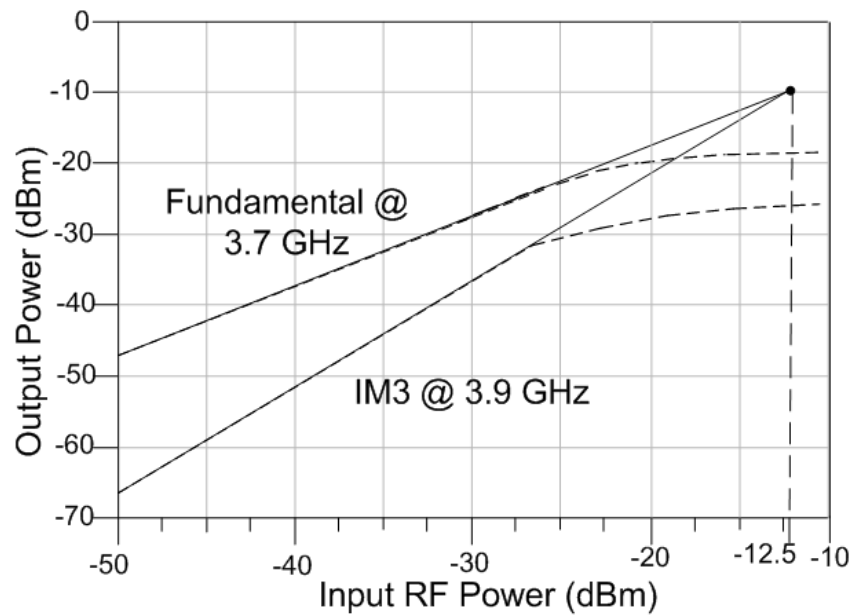
(d)

Figure 3.7, continued.

[72] that due to the possibility of a strong interferer in one band damaging the signal in the other, the IIP3 of a concurrent low noise amplifier necessarily has to be at least 3 dB higher than a normal low noise amplifier. Thus, the linearity requirements of this topology do not satisfy the requirements for front end integration and development of a dual band UWB receiver front end and alternative topologies are investigated based on the principles of distributed amplification, in order to particularly solve the problem of poor linearity arising from analog based approaches.

3.2   Theory of distributed amplification

Distributed amplifiers were first patented by Percival in 1937 [73]. Since then numerous studies have been conducted into their operation, design and analysis of important circuit parameters [74], [75]. Recently, with the emergence of Ultra wideband (UWB) technology, there has been a renewed interest in investigating novel topologies that could provide wide bandwidths over wide swaths of RF spectrum. However, the CMOS implementation of distributed low noise amplifiers is still an active research area facing numerous design challenges, particularly related to the size and power consumption of these circuits.

Distributed amplifiers implemented in monolithic form operate on the principle of traveling wave amplification. An input RF signal incident on the gate line is tapped at different phases and fed to gain stages, which promptly amplifies it and feeds them to the drain line. If the phase velocity of the signal at the gate line is equal to that at the drain line, the forward traveling waves add productively while the reverse traveling waves cancel each other out or get absorbed by the terminating impedance at the drain node.

In the example shown in figure 3.8, transistors form the gain blocks and hence its nodal drain to source and gate to source capacitances load the transmission line segments. The loaded gate and drain line characteristic impedances are given by [75]:

$$Z_g \cong \sqrt{\frac{L_g}{C_g + C_{gs}/l_g}} \tag{3.10}$$

$$Z_g \cong \sqrt{\frac{L_d}{C_d + C_{ds}/l_d}}$$

(3.11)
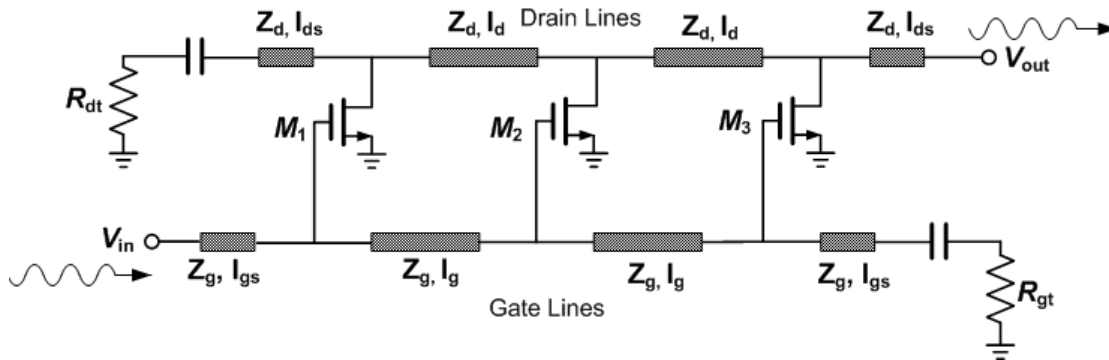
Figure 3.8 Representation of a distributed amplifier employing transmission line segments.

where l_g, l_d are the unit lengths of the gate and drain transmission lines, L_g, C_g, and L_d, C_d are the per- unit gate and drain transmission line inductances and capacitances, C_{gs} is the gate to source capacitance at the gate of the MOS transistor, while C_{ds} is the drain to source capacitance at the drain terminal of the MOS transistor.

Using a simple model for the MOS transistor as a transconductance and gate-source, drain-source capacitances, the general equation for small signal amplifier gain could be derived as [75]:

$$G = g_m^2 Z_d Z_g \left| \frac{\gamma_g l_g [\exp(-\gamma_g l_g n) - \exp(-\gamma_d l_d n)]}{\gamma_g^2 l_g^2 - \gamma_d^2 l_d^2} \right|^2$$

(3.12)

with l_g, l_d being the unit gate and drain lengths while γ_g and γ_d are the complex propagation constants of gate and drain lines. Assuming perfect phase synchronization

($\beta_g l_g = \beta_d l_d = \theta$) and perfect matching with lines terminated by their characteristic

impedances [75]:

$$G = g_m^2 Z_d Z_g \frac{[\exp(-\alpha_g l_g n) - \exp(-\alpha_d l_d n)]^2}{(\alpha_g l_g - \alpha_d l_d)^2} \tag{3.13}$$

Further, considering the low loss case with α_g and α_d are both negligible, expanding the

exponentials with $\alpha_g l_g n \ll 1$, (3.13) can be re-written as:

$$G = \frac{g_m^2 Z_d Z_g n^2}{4} \tag{3.14}$$

Equation (3.14) states that the gain of a distributed amplifier can be increased arbitrarily

with the number of stages. However, there is an upper bound for the optimum number of

stages for maximum gain possibility which can be obtained by subjecting (3.13) to the

maximum gain condition,

$$\frac{\partial G}{\partial n} = 0, \tag{3.15}$$

By solving that equation for n, we can arrive at n=N_{opt} such that:

$$N_{optim} = \frac{\ln(\alpha_d l_d) - \ln(\alpha_g l_g)}{\alpha_d l_d - \alpha_g l_g} \tag{3.16}$$

A very important property of the distributed amplifiers is their improved linearity

compared to conventional single or multi-staged analog amplifiers. It has been earlier

proved by Aitchison [76] that the carrier to inter-modulation voltage ratio, would be

drastically improved in the case of a distributed amplifier than a conventional amplifier

employing a cascaded stages. Mathematically, this could be expressed by employing the

Volterra series expansion on the I_d-V_{gs} non-linear dependency, which is the primary

source of non-linearity in most FET based amplifiers. The carrier to inter-modulation voltage ratio, C/IM3, for a distributed amplifier is given by [76]:

$$\frac{C}{IM3} = \left(\frac{g_{m1}^3}{3k^2 g_{m3}}\right)^2 . n^4 . e^{-2n\alpha_d} .$$

(3.17)

While that of a single staged analog amplifier could be denoted by:

$$\frac{C}{IM3} = \left(\frac{g_{m1}^3}{3k^2 g_{m3}}\right)^2 .$$

(3.18)

where g_{m1} and g_{m3} are the first and third order small signal transconductance coefficients of the non-linear I_d-V_{gs} dependent plot, k is the constant drain current seen by the primary transistor, n is the number of stages and α_d denotes the loss in the drain transmission line or inductor. (3.17) and (3.18) enable us to conclude that the linearity of a distributed amplifier will always be larger than a single or multi-stage analog amplifier as long as n>1 and α_d is. An interesting observation here is that the C/IM3 ratio of a multi-stage analog amplifier is even lower than that of a single staged amplifier. The derivation of the Volterra series expression for its analysis is beyond the scope of this work.

3.3   Overview of CMOS Distributed low noise amplifiers

The basic theory of distributed amplifiers covered in the earlier section needs to be enhanced to cover some specific design issues that are faced in CMOS design. Specifically, issues of lossy transmission lines, their exorbitant dimensions and power

consumption being the main ones. In this section, some of those design issues are considered in detail and several existing topologies are also discussed.

3.3.1 Design issues

In CMOS design, the main challenges facing the implementation of distributed amplifiers are their low gain, bulky size of the transmission line segments and the exorbitant power consumption of the circuit.

The gain of a distributed amplifier depends primarily on the characteristic impedances of transmission lines, the loss associated with each line as well as the number of stages. High characteristic impedance is desirable as they can then easily absorb the nodal parasitic capacitance of the transistor, but large impedances are not typically feasible in CMOS technologies. The maximum characteristic impedances of most 6-metal CMOS technologies do not exceed 100 Ω in microstrip. Though CPW structures might allow greater impedances, they do not meet the size requirements in modern RF and microwave circuits. As a result, there is a stringent technology dependent limiting factor on this parameter. At the same time, losses associated with transmission line implementation in CMOS also degrade the gain of the amplifier as seen from (3.15). The challenge of loss reduction could be mildly addressed by effectively shielding the lines from the silicon substrate. However, the problem of loss in transmission lines is   technology dependent and cannot be entirely controlled by the designer. Gain could always be improved by increasing the number of stages, but in

CMOS related technologies size and power consumption requirements might be disadvantaged by doing so.

Transmission line size is of significant concern to CMOS designers since it renders the circuits practically useless for potential integration with other circuits, as it increases the unit cost of implementation. Miniaturized versions of transmission lines as well as artificial transmission lines could be explored to solve this problem, but unless they prove that the dimensions of the distributed amplifier circuits are compatible with inductor based analog broad band circuits, they would not be preferred by the industry or the IC chip market. That implies size reduction to the tune of 90% or more from the existing dimensions.

Another final concern in implementing CMOS distributed amplifiers is their exorbitant power consumption. Since distributed amplifiers employ at least 3 or more cascaded gain stages, driving them would require a lot of DC power which once again offsets the design goals for their integrated application. A number of low power consuming distributed amplifier related novel gain stages are investigated to this regard. Another approach that could be wise to consider is to reduce resistive losses in the transmission line segments as they dissipate a significant amount of DC power as well.

3.3.2   Topologies

CMOS based distributed amplifiers (DA) typically try to address the size, power and gain concerns mentioned earlier. The most common trend in modern DA implementation has been the utilization of artificial transmission lines or inductors instead of regular

transmission lines, which serves to conserve chip area without any negative effects on the bandwidth and gain ripple. It must be noted that the most important parameter the designers use to effectively control the gain is transconductance and as such most of these approaches seek to improve only the gain cell of the amplifier. Several design techniques targeting the transistor's transconductance are reported, include cascode [77], current steering [78] and cascade common-source gain cells [79]. The latter two topologies simultaneously address the issue of power consumption. The issue of miniaturization is a bit more perplexing and only artificial transmission lines or inductors have been proposed as a viable solution. However, the chip area in most cases that employ spiral inductors is still in the range of a few mm^2 rendering the circuit too expensive for CMOS implementation. It must be explicitly understood that the chip area reduction is directly related to miniaturization of inductors or transmission lines. In the following sections two miniaturized distributed amplifier topologies are suggested that utilize miniaturized passive elements to obtain significant size compression.

3.4   A DC-20 GHz Low noise distributed amplifier

A novel DC-20 GHz distributed low noise amplifier incorporating both inductors and transmission lines as its impedance segments is proposed. The basic idea behind this topology is that since transmission lines and inductors have their own advantages in distributed amplifier design, a cumulative approach that incorporates both these elements will bring in the advantages related to best of both structures.

3.4.1   Basic principles

The idea behind incorporating both transmission line and inductors as impedance segments is discussed here. But before that, the functionality of the impedance segments in the basic traveling wave amplifier, on which the distributed amplifier is modeled up on needs to be understood.

Consider a unit cell of the distributed amplifier as shown in figure 3.9. L_{xs} is the inductance associated with a half section of the transmission line and C_{xs} is the
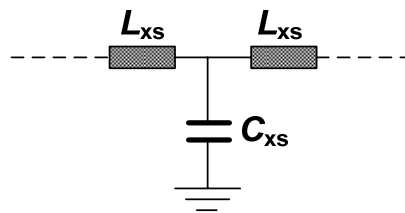
Figure 3.9 Unit cell of a distributed amplifier(x=d, g).

capacitance associated with the drain or gate nodes. The structure can be treated as a constant-k low pass T-section. Hence, using the image parameter method, the image impedance at the input of the section is determined as [50]:

$$Z_i = \sqrt{\frac{L_{xs}}{C_{xs}}}\sqrt{1 - \frac{\omega^2 L_{xs} C_{xs}}{4}} \tag{3.19}$$

and therefore, the cut off frequency is given as:

$$\omega_c = \frac{2}{\sqrt{L_{xs} C_{xs}}} \tag{3.20}$$

or in terms of characteristic impedance,Z_0:

$$f_c = \frac{1}{\pi.C_{xs}.Z_0} \tag{3.21}$$

with C_{xs} being the total nodal capacitance at the transistors drain or gate terminal. (3.21) gives some insight into the influence of impedance segment on the circuit operation. While the characteristic impedance is fixed for matching purposes, the capacitance per unit length as well as the nodal impedance of the transistor both influence the cut off frequency and hence the bandwidth of the amplifier. The impedance segment therefore controls the amplifier matching, gain flatness as well as playing an important role in determining the amplifier bandwidth.

Now, considering figure 3.8 once again, we can realize that the end segments l_{xs} (x=d,g) are the only segments that contribute to the matching while the inner segments do not contribute to the input or output matching. We also realize from (3.13) that the loss characteristics of the transmission line segments determine the gain ripple of the distributed amplifier. Losses in CMOS based passive structures are either due to conductivity of silicon substrate or due to ohmic resistances in the metals. In order to shield circuits from the silicon substrate, a pattern ground shield could be used which presents some modeling and layout challenges. On the other hand, a novel approach is presented here that does not require pattern ground shielding. In fact, the distributed amplifier itself is not implemented using typical inductors or transmission lines but using a structure that presents strong mutual coupling from within itself.

3.4.2 Integration of inductors and transmission lines

Figure 3.10 shows the layouts of the proposed multi-layered inductor and CPW structures. Both structures have a curvilinear "8" shaped pattern and the same structure is implemented both as an inductor as well as CPW transmission line by simply adding

Table 3.1 Transmission line parameters of the CPW structure for different spacing of the signal-ground lines

Spacing (μm)	Freq (GHz)	Re(Z) (Ohm)	Lambda (mm)	Alpha (dB/mm)
10	1	60.6	49.1	-0.15
	3	65.5	32.3	-0.17
	6	74.2	25.4	-0.18
	11	92.6	15.1	-0.22
	20	99.2	10.8	-0.25
Spacing (μm)	Freq (GHz)	Re(Z) (Ohm)	Lambda (mm)	Alpha (dB/mm)
16	1	81.1	31.4	-0.19
	3	90.4	18.8	-0.20
	6	102.3	10.4	-0.20
	11	115.3	8.5	-0.22
	20	124.8	4.4	-0.24
Spacing (μm)	Freq (GHz)	Re(Z) (Ohm)	Lambda (mm)	Alpha (dB/mm)
25	1	110.6	25.7	-0.20
	3	117.9	18.8	-0.23
	6	130.3	11.3	-0.23
	11	142.6	6.1	-0.26
	20	179.2	3.4	-0.27

two via-connected ground planes in each region of its operation. The primary advantage of this structure is that it generates very high characteristic impedance in its transmission line form while the loss is quite low. Because of the proximity of the ground planes to

the structure, the peripheral EM field does not pass through the silicon substrate and hence some loss is curtailed. Table 3.1 shows the properties of the transmission line based structure calculated from IE3D for a line shaped as in figure 3.10 (b) with line width of 12 μm, while the narrowest distance of the curvilinear signal strip of the transmission line to the ground plane is changed from 10 to 25 μm. The distance of 25 μm results in moderately large characteristic impedance, as is evident from table 3.1. Even greater characteristic impedance could've been obtained if the distance were increased even further but that would enormously increase the size of the structure. The ground plane strip is 15 μm wide.

Further the loss of the same structure when implemented as an inductor is also minimized possibly due to the strong negative coupling within the structure itself. The total inductance presented by the structure is given as:

$$L_{tot} = L_{slf1} + L_{slf2} + L_{slf3} + L_{slf4} - 2(m_{1,4} + m_{2,3}) \qquad (3.22)$$

where $L_{slfx(x=1-4)}$ denotes the self inductance of each segment while $m_{i, j}$ $(i \neq j, \ i, \ j \ = \ 1-4)$ denotes the mutual coupling between different segments. The presence of such strong negative coupling within the structure tends to lower the net inductance, which is acceptable and in fact mandated by the matching conditions for this particular circuit.

3.4.3 Design

The technology chosen to implement this design is TSMC 0.18-μm CMOS process [80]. For transmission lines, the ground planes are also implemented on both M6 and M5

(a)

(b)
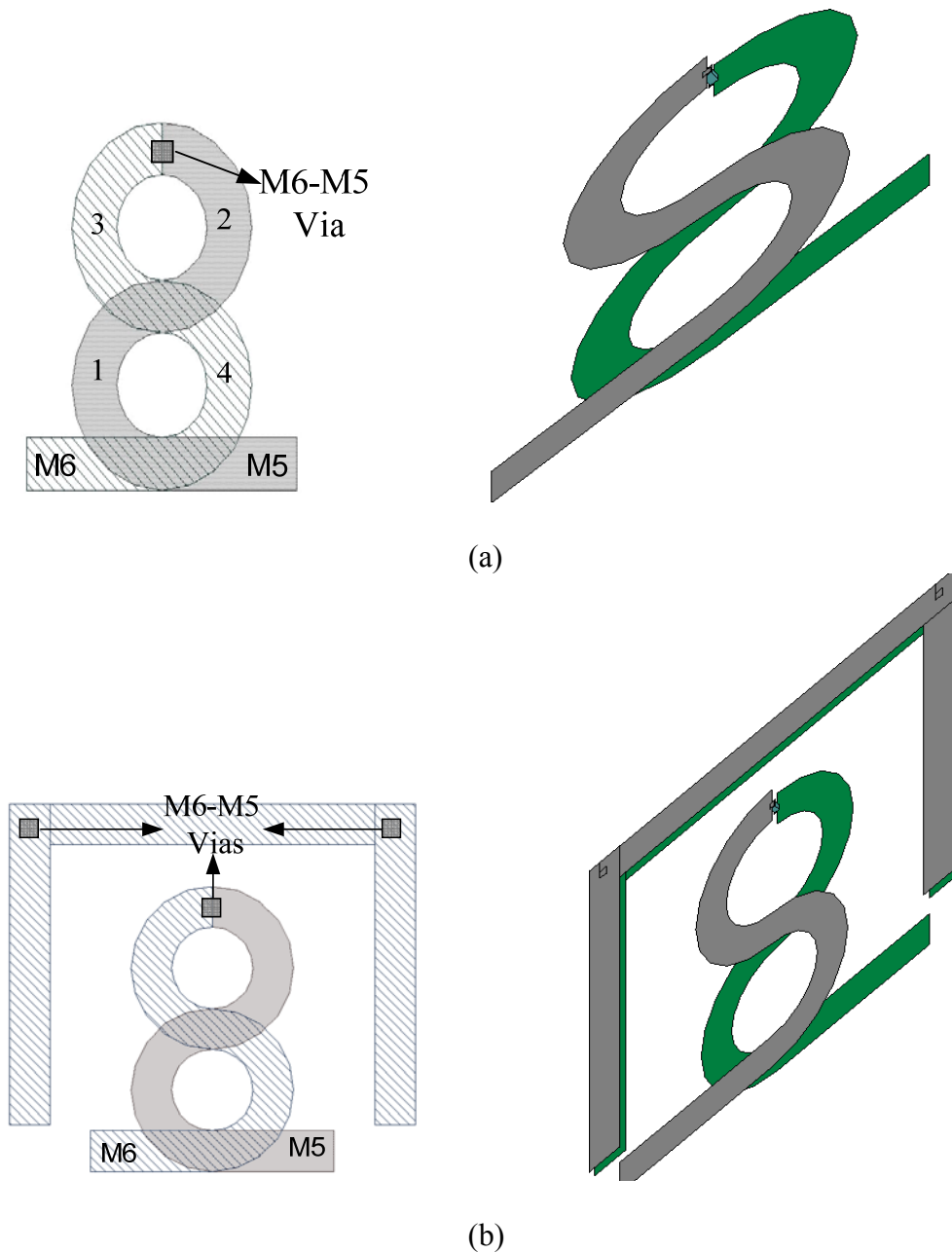
Figure 3.10 (a) Novel Octagonal multi-layered inductor and its 3-D view and (b) inductor modified as a CPW transmission line with its 3-D view.

metal layers and are spaced equidistant from each set of layers so that the overall symmetry of the structure is maintained. The design and optimization of the multi-
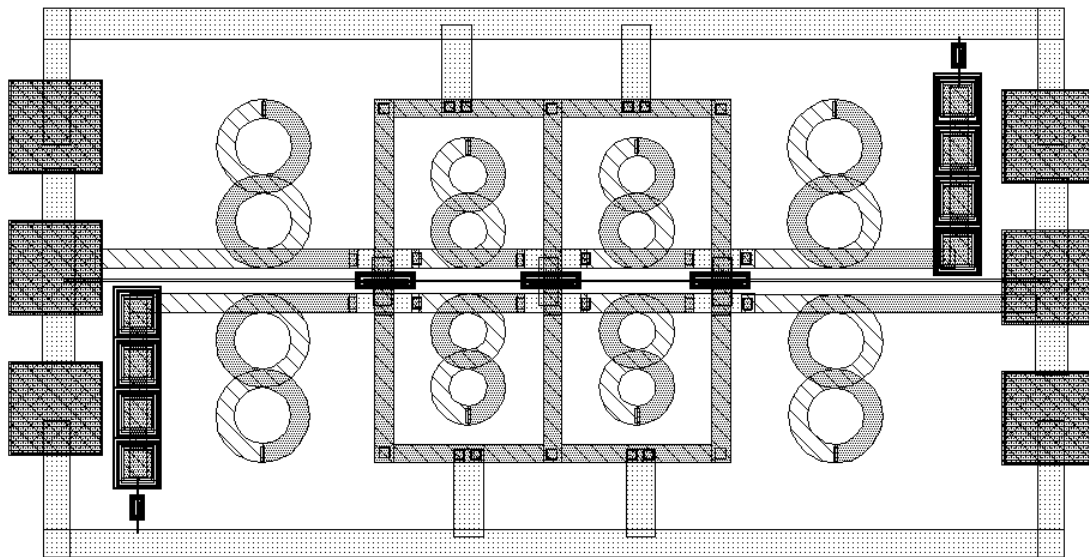
Figure 3.11 Layout of the 4-stage novel distributed amplifier employing transmission lines and inductors [81].

layered transmission line structure was performed in IE3D, which enable full-wave Electro-Magnetic (EM) simulations. Several iterations were performed to arrive at the best structure which yielded the required performance. It must be worth mentioning here, that when the structure is modeled as an inductor by removing its ground planes as in figure 3.10 (a), the segment length has to be increased in order to obtain half the inductance associated with the corresponding transmission line. The requirement for the (ground-less) inductors of 0.5-nH inductance was dictated by the input and output matching conditions for the designed distributed amplifier. When implemented as a transmission line figure. 3.10 (b), the characteristic impedance and loss of the structure are 180 Ohms and −0.1 dB/m, respectively, and when the ground plane is kept at a moderately large distance from the signal line of 25 µm and the structure is 200 x 180 µm in size. When implemented as an inductor, the size was similar to the transmission

line with ground planes but the inductance was drastically reduced. The low loss and high characteristic impedance associated with the transmission-line structure enables using only 3-stages for the distributed amplifier to achieve a decent gain across an extremely wide bandwidth. Further, only a single transistor element is utilized as the gain cell. If a cascode structure was employed, an even better gain, gain flatness and bandwidth could be achieved. The Cadence layout of the distributed amplifier designed with both the multi-layer transmission lines and inductors is shown in figure 3.10.

3.4.4   Results

Post layout simulations were performed on the layout shown in figure 3.11. Since the inductors and transmission line models were not readily available, Layout Versus Schematic (LVS) was performed by assuming wires for these structures in the schematic. The resulting S-parameters and noise figure of the amplifier was calculated by importing the touchstone files from IE3D into ADS. The results are shown in figure 3.12 The power gain is about 8 dB with 0.2 dB ripple in the entire frequency spectrum of DC- 20 GHz. The input and output return loss stay well below 10 db up to 17 GHz while the noise figure is less than 5 dB. The structure occupies just 1.05 x 0.37 mm2 of chip area making it one of the smallest distributed amplifiers ever reported till date. These results are based on post layout simulations and are compared to previously published results in table 3.2.
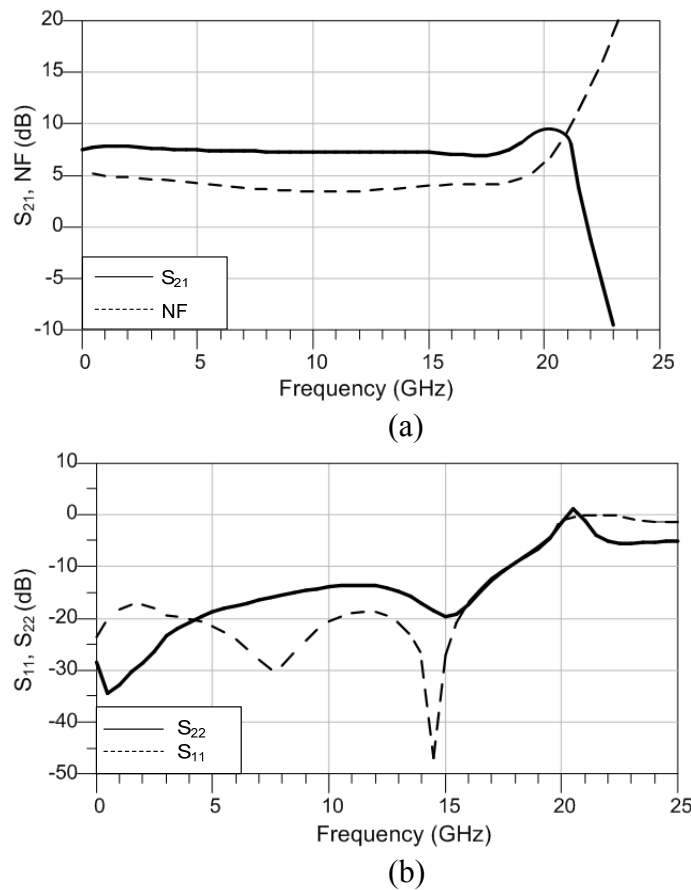
Figure 3.12 Post layout simulation results of the novel multi-layered wideband LNA showing (a) S_{21} and Noise Figure (b) Input and output return loss [81].

In spite of achieving compact dimensions compared to earlier distributed topologies, the circuit is still 1 mm long and hence unable to exploit the possible benefits of employing a distributed topology on CMOS. Because of this reason a more compact topology needs to be investigated for possibility of practical integration as a low noise amplifier in a receiver front end.

Table 3.2 Comparison with Transmission line based distributed amplifiers

Reference	Technology	S_{11} (dB)	S_{22} (dB)	Band Width (GHz)	NF (dB)	Die Area (mm^2)	Tx Line Type	Power Consumption (mW)
[82]	0.25µm CMOS	<-10	6	0-12	N/A	1×3	CPW	120
[83]	Silicon on Sapphire	<-7	5	0-10	N/A	N/A	CPW	N/A
[84]	0.18µm CMOS	<-10	4	39	N/A	1.1×3	Microstrip	140
This work	0.18µm CMOS	<-13 (to 17 GHz)	8	0-20	3.4-5	1.05×0.37	Multilayer Structure	34

3.5 An ultra-compact distributed LNA for UWB applications

The previous amplifier was designed to target two particular and crucial issues affecting distributed amplifiers – size and power consumption. However, as the layout indicates, the circuit is almost 1 mm long horizontally. This is a result of the larger size consumed by the CPW transmission lines. To avert this problem, new inductor structures need to be developed which are suitable specifically for the distributed amplifier topology. In this section, the design and implementation of an ultra-compact UWB amplifier is discussed.

3.5.1 Background and justification

The basic idea behind the design of this novel UWB amplifier lies in the realization that in order to achieve minimal chip area, the size of the impedance segments needs to

be miniaturized. Hence, the design challenge is to develop novel inductor topologies that could limit the chip area consumption while simultaneously providing high quality factor and self resonant frequency.

To simultaneously satisfy these implementations, a few observations need to be made. Firstly, obtaining a higher quality factor inductor is not a big challenge for smaller inductor values in most CMOS technologies. In fact, obtaining a higher self-resonant frequency is more crucial for broadband amplifier design applications. Secondly, the inductor design needs to be application specific as the inductors tailored to suit a voltage controlled oscillator may not satisfy all the requirements of a distributed amplifier, because distributed amplifier design may require very good matching at nodal ports, while a distributed oscillator requires equalization of group delays. Another issue one needs to bear in mind is the fact that miniature inductors themselves are not difficult to design but the key challenge lies in studying the impact of closely packed inductor structures.

The design of an ultra-compact distributed amplifier therefore involves two phases – study the means by which the structures could be integrated and study the impact of those integrated closely packed inductors on the overall circuit, so that efficient miniaturized structure could be possible. This is accomplished by treating all the drain and gate inductors as unique multi-port inductor structures and analyzing the impact of mutual coupling within that structure.

3.5.2   Integration issues in vertically coiled inductor structure

As mentioned earlier, while miniaturization of inductors can be accomplished by
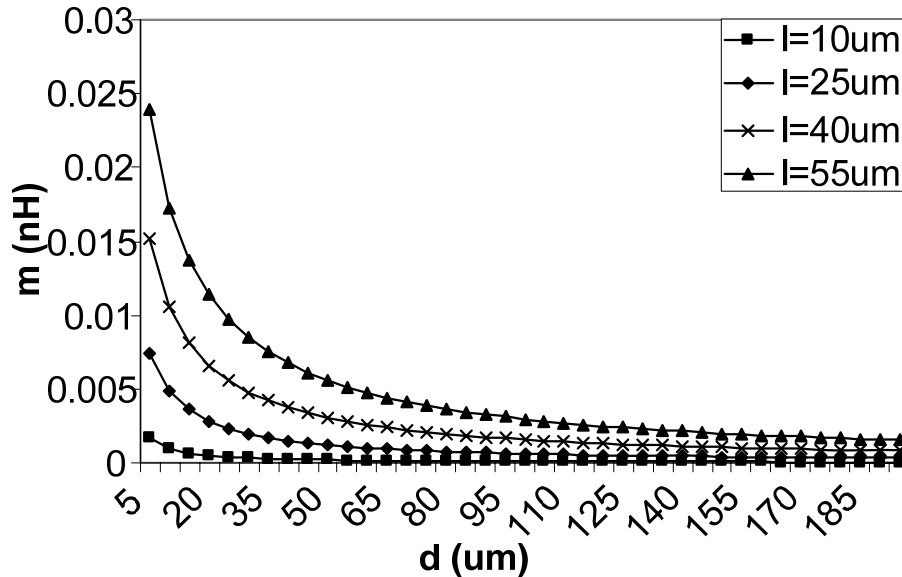
Figure 3.13 Variation of mutual inductance with pitch for different metal lengths [84].

using the techniques described in chapter II, the issues of integrating those inductors

efficiently to conserve chip area needs to be studied in much more detail.

Consider the vertically coiled multi-layered inductor structures in figures 2.33 and

2.34 in chapter 2. The integrated behavior of these inductors raises the obvious issue of

strong negative coupling between adjacent inductors when placed close to one another.

Coupling between any two wires or segments of metal strong depends on the distance

between them. Assuming that the pitch of an inductor's turn (d) is varied for different

inductor lengths (l), mutual inductance drops inversely with respect to the distance

separating the two metals as shown in figure 3.13. This makes a strong case for having a
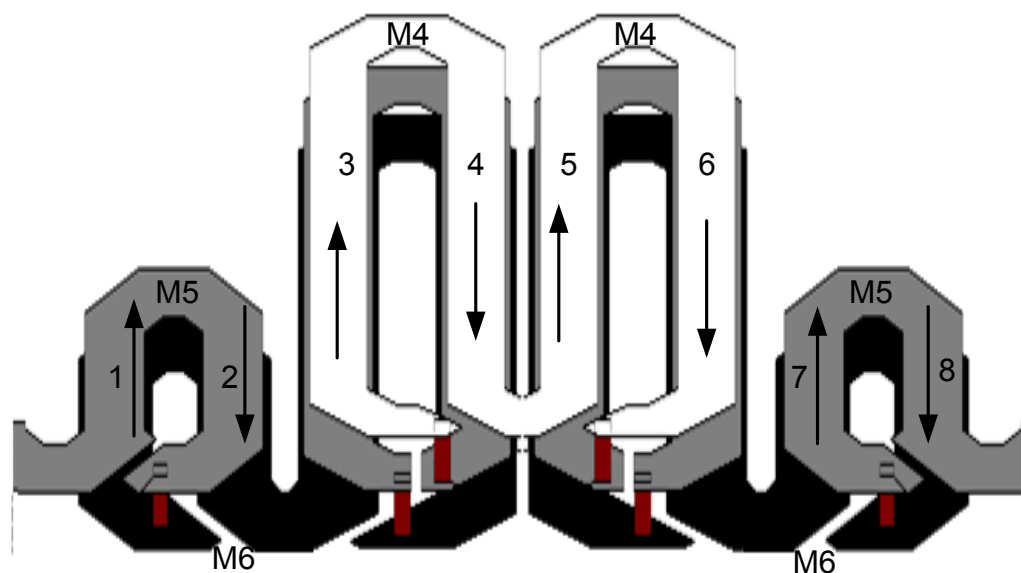
(a)
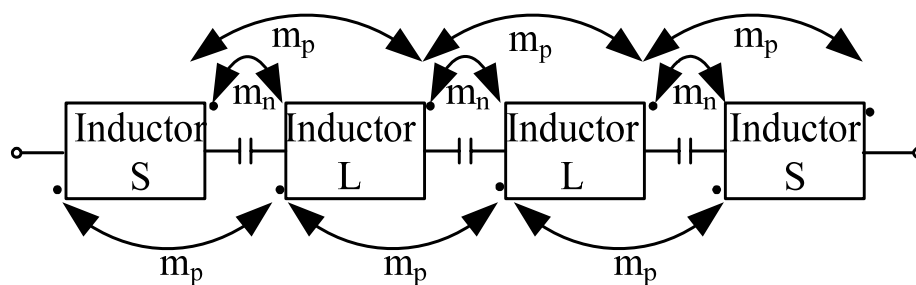
(b)

Figure 3.14 (a) Integrated multi-layered inductor structure and (b) schematic representation of the above structure [85]. Vias are shown in red in (a).

minimum pitch when strong positive coupling is desired and maximum values for avoiding negative coupling. In integrated inductor circuit design, however, a minimum pitch is chosen to integrate the inductors in order to arrive at an optimum dimension. The resultant structure is shown in figure 3.14 (a). It is apparent that the structure increases negative mutual coupling between successive inductors. However, increase in negative

mutual coupling is not necessarily negative for wideband circuit's overall performance. The impact of negative coupled inductors is suggested to be desirable, in one of the earliest studies conducted on distributed amplifiers by Ginzton et al [86] in 1948. It is claimed that negative coupled inductors tend to linearize the amplifier phase shift. In its simplified form, the phase shift associated with the gain transfer function is given by:

$$\phi = 2n \tan^{-1}\left(\frac{mf/f_0}{\sqrt{m^2 - (f/f_0)^2}}\right)$$

(3.23)

where m is the mutual coupling co-efficient, n is the number of cascading gain stages and f_0 is the resonant frequency at the drain (or gate) node of the nodal inductance and the capacitance associated with that node. Equation (3.23) shows that once mutual coupling coefficient is greater than 1 (as is the case for negative coupling), and resonant frequencies facilitated by smaller drain/gate segment inductances which are much higher than operating frequency, the phase shift will be a linear function of the frequency of operation. Having a linear phase shift results in very low distortion of the signal in time domain as the group delay is related to the phase through a derivative. This property is very attractive for UWB signals which are essentially time domain bursts of short pulses.

Another important observation is made by using equation 2.16 on the integrated inductor segment of figure 3.13 (a) to derive its total inductance. Therefore, using the Greenhouse approach [67]:

$$L_T = 2.(L_{sm} + L_{lo}) - 2.(m_{23} + m_{45} + m_{67}) + 4.(m_{13} + m_{35} + m_{57}) + (2.L_{6t} + L_{4t})$$

(3.24)

where L_{sm} and L_{lo} are the overall inductances of the small and large inductors indicated by blocks S and L in the schematic of Fig. 3.14 (b) respectively, including their internal mutual coupling parameters, m_{ij} denotes the coupling between the ith and j^{th} segments as shown in Fig. 3.14, and L_{kt} shows the turn inductance in the kth layer, owing to both self inductance and mutual inductance due to other inductor segments. The expression shows that, owing to the extremely compact dimensions, there is also a first-order positive mutual coupling between alternate segments, which significantly mitigates the impact of negative coupling. The impact of the first-order positive coupling between alternate segments can be estimated by:

$$m_{ij} = 2.l.[\ln(\frac{l}{d} + \sqrt{1+(\frac{l}{d})^2}) - \sqrt{1+(\frac{d}{l})^2} + \frac{d}{l}]. \tag{3.25}$$

wherein l and d represent the length of the metal strip and its pitch, respectively. (3.24) shows how the overall inductance is not adversely affected by the strong negative mutual coupling between adjacent inductors. It is estimated that the increase in the overall inductance is about 8% if the positive mutual inductance is 52% of the value of negative coupling. Negative mutual coupling is extremely strong owing to the smaller pitch as shown in figure 3.12. For shorter lengths, having a smaller pitch presents the best opportunity to increase mutual inductance, which explains why the multi-layer inductor structure offers a larger tight positive mutual inductance between the CMOS stacked layers.
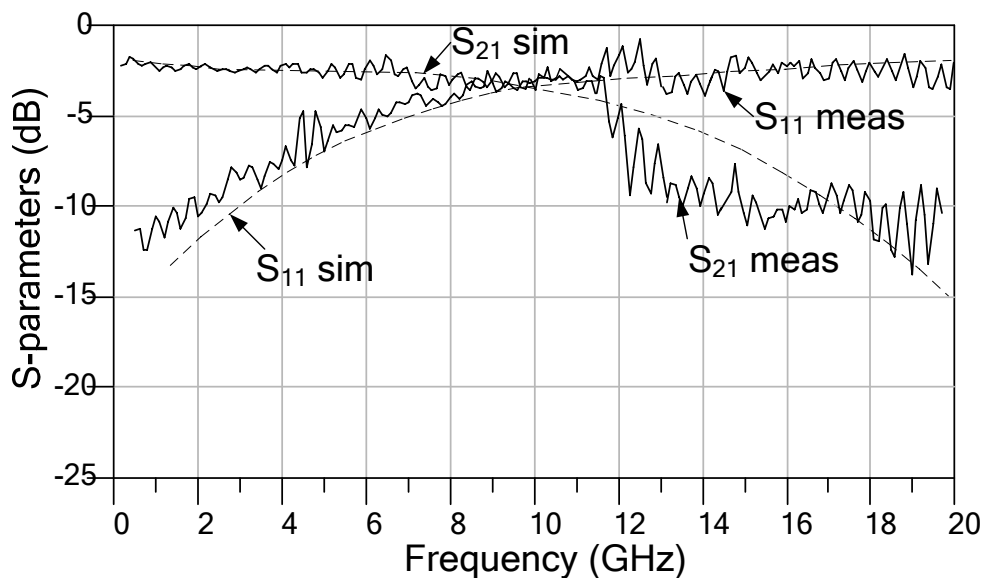
Figure 3.15 S-parameters of the integrated inductor segment [85].

To further study the properties of this integrated inductor segment, the structure was laid out and characterized in Jazz CA18HR 0.18 μm CMOS process. The cumulative properties of the multi-layered inductor segment are found from the measured and simulated S-parameters of the inductor segment shown in figure 3.15. It is apparent that the inductor segment exhibits the characteristics of a low-loss transmission line. This can be explained by the schematic model in figure 3.14 (b) which shows how the positive mutual inductance m_p and negative mutual inductance m_n, and the series capacitance from successive segments contribute to an enhancement of the bandwidth by increasing the overall self resonant frequency of the integrated segment. While the series capacitance serves to lower the individual capacitance of each inductance, the net inductance will be slightly increased by the mutual coupling.

Hence, it can be construed that the prime effects of extreme miniaturization on a

broad-band circuit performance are not necessarily negative and any of the impending losses could be reduced by utilizing multi-layered inductors in the top metal layers and careful optimization of their design parameters.

3.5.3 Amplifier design and layout

The design of distributed amplifiers requires optimization of transistors' width for maximum gain and lower power consumption requirements. The requirements were met for an aspect ratio of 136/0.18 (W/L). The gate inductance resonates with transistor's
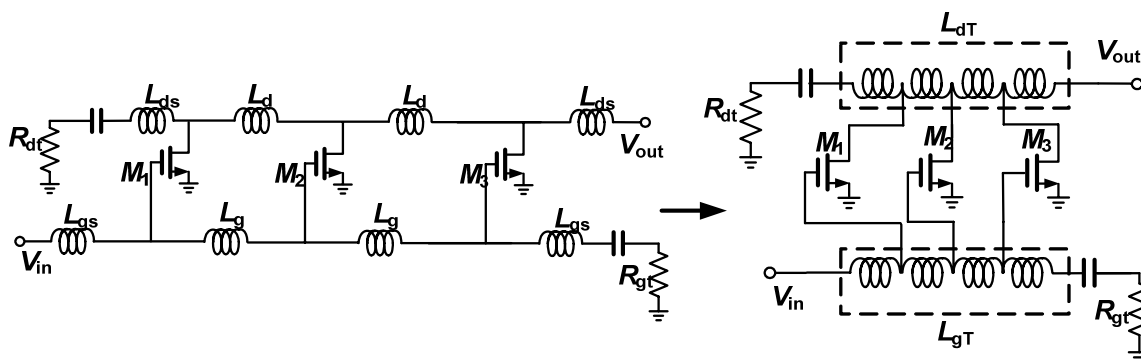
Figure 3.16 Schematic of the modified distributed amplifier with 5-port inductor segments [85].

input parasitic capacitance influencing the noise spectrum and, as such, small inductances of 0.85 nH and 0.4 nH are used to meet the bandwidth and noise requirements. The entire inductor segment was then jointly optimized as a 5-port network in IE3D to take into account both the negative and positive mutual coupling associated with adjacent multi-layer inductors. Figure 3.16 shows the schematic of the distributed amplifier treating the inductors as a single 5-port so that drain and gate

inductances could be jointly quantized. The amplifier was further tested for stability to check for unwanted oscillations, and calculations proved that it remains unconditionally stable up to 20 GHz.

3.5.4 Measurement results

Fig. 3.17 shows the fabricated die photograph of the distributed amplifier in JAZZ CA18HJazz CA18 HR 0.18-μm RF/Mixed signal process. The fabricated amplifier was
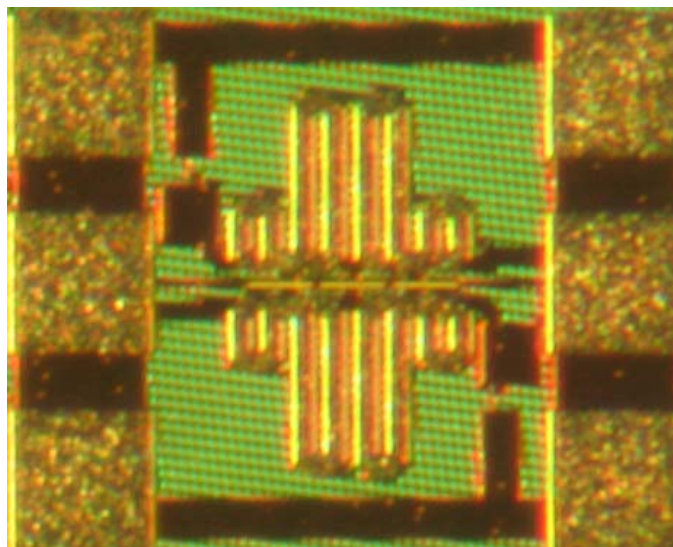
Figure 3.17 Die photograph of the fabricated DA.

measured using on-wafer probes and bias tees. In order to minimize reflection and enhance isolation, 50-Ω on-chip resistors were used along with 10 pF DC block capacitors at the isolation terminals. Figure 3.18 (a) shows the measured power gain of the amplifier. The amplifier exhibits around 6-dB flat gain throughout the entire 3.1-10.6
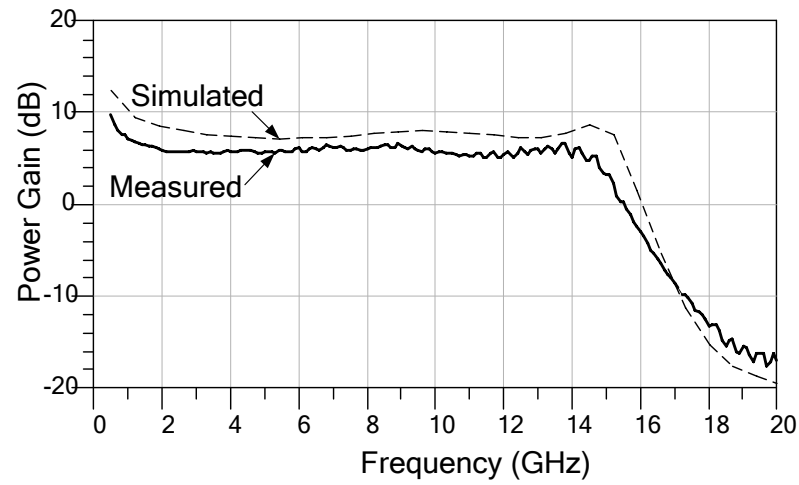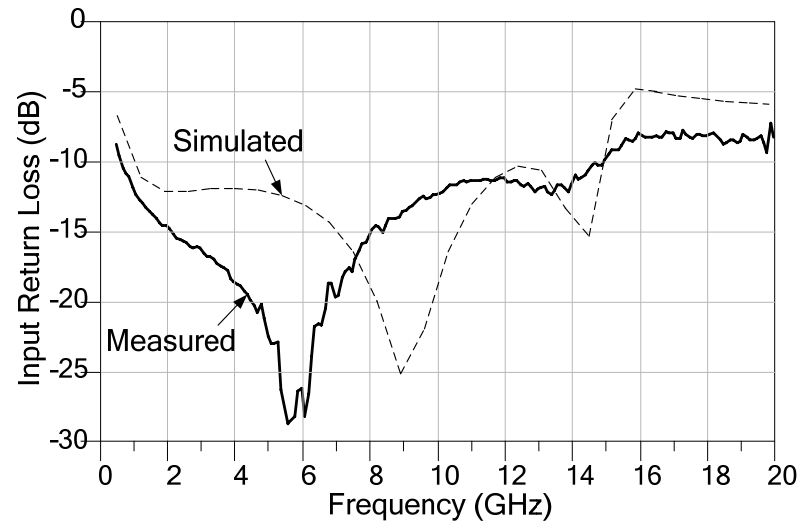
Figure 3.18 Simulated and measured S-parameters of (a) Power gain (S_{21}) and (b) Input return loss (S_{11}).

GHz UWB range, which follows very well the simulated results, albeit with 1.5-dB lower gain than expected. This difference is primarily attributed to the discrepancies in via-modeling as well as parasitics that couldn't be de-embedded. The input and output

(a)

(b)
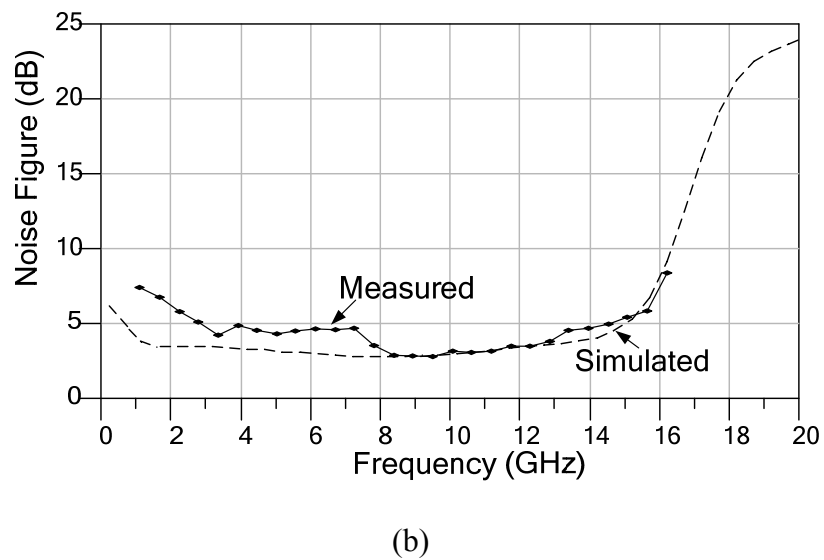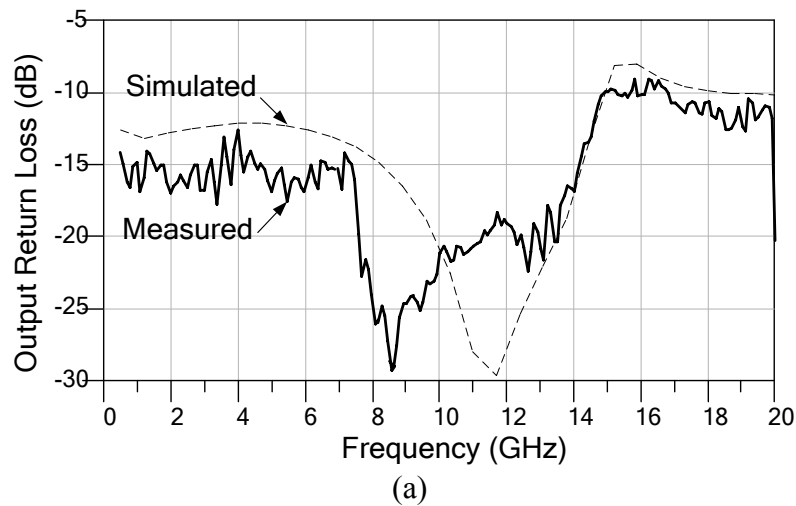
Figure 3.19 Simulated and measured (a) Output return loss and (S_{22}) and (b) Noise figure (NF).

return losses, shown in Figs. 3.18 (b) and 3.19 (a), remain well below 12 and 15 dB, respectively. Noise measurements shown in Figure 3.19 (b) results, with only 2.7 dB from 8 to 10 GHz. Simulations indicate that the amplifier shows a first-order IIP3 of

Table 3.3 Comparison with recently published CMOS distributed amplifiers.

	Technology	Topology (passives)	Band-width (GHz)	Size (mm^2)	% Size Compression	Average Gain ± ripple (dB)	Input Return Loss (dB)	Noise Figure (dB)	Power Consumption (mW)
[87]	0.6 µm CMOS	SD ** (spiral inductors)	5	0.79	90%	6.5 ± 1.5	<-10	>5.7	83.4
[79]†	0.18 µm CMOS	CSD* (spiral inductors)	11	1.44	95.5%	10 ±1	<-20	>3.3	19.6
[77]	0.18 µm CMOS	CSD (spiral inductors)	21	1.35	94.1%	7.3 ± 0.9	<-9	>4.3	52
[88]	0.18 µm CMOS	CSD (CPW)	26	1.62	95%	6 ± 1	<-10	>6	68.1
[84]	0.18 µm CMOS	SD (Microstrip)	39	3.3	97.5%	4 ± 0.5	<-15	NA	140
This work	0.18 µm CMOS	SD (multi-layered inductors)	13	0.08	-	6 ± 0.2	<-12	>2.7	22

† Only low power mode considered   *CSD=Cascode gain cell

 **SD=Single transistor gain cell

about +13.2 dBm at 14 GHz, indicating that the amplifier maintains an exceptional

linearity even at the end of the spectrum.

These results are compared to some of the most recent publications to date as shown

in table 3.3. The % size compression column shows how compressed the current

amplifier is - relative to the respective reference. It must be noted that in the current

work, the distributed amplifier is merely used to demonstrate the applicability of the

proposed integrated inductor structure to practical CMOS RFIC design and hence a

simple single transistor gain cell was used, which inevitably didn't show a larger gain as

some other publications employing cascode gain cells have. However, judging on the

overall aspects of size, matching, power consumption, linearity and noise figure, the circuit still compares favorably, especially noting that it merely occupies a maximum of 10% the chip area reported by the next smallest counterpart. This amplifier is therefore pursued as an integrable high-linearity, low noise, broad band amplifier that could be integrated in a realistic UWB receiver front end.

CHAPTER IV

DISTRIBUTED VOLTAGE CONTROLLED OSCILLATORS

Distributed Voltage controlled oscillators were first proposed by Skvor et al [89]. Numerous studies have been conducted into their operation, design and analysis of important circuit parameters notably Kleveland et al [90] and Hajimiri [91]. The distributed topology presents a good opportunity to realize oscillators above 10 GHz in CMOS where technology limitations seem to limit the performance of traditional LC-oscillators. Distributed VCOs have been also shown to exhibit very wide tuning ranges [91] that are highly attractive for broadband wireless applications. They however suffer from poor properties of size and power consumption.

In this chapter, distributed voltage controlled oscillators are discussed employing novel artificial transmission lines in order to significantly reduce their dimensions. Section 4.1 offers the basic theory of their operation and provides an insight into the working principles underlying the operation of distributed VCOs. The next section includes an overview of existing DVCOs and design issues specific to them. An ultra-compact distributed voltage controlled oscillator is designed and its operation is discussed towards the end of the chapter in the final section.

4.1   Theory of distributed voltage controlled oscillators (DVCO)

Distributed oscillators are formed by connecting the output of a distributed amplifier

to its input, so as to form a positive feedback loop which could sustain oscillations. The

oscillation frequency would then be dependent up on the round trip delay of the signal,

i.e., from the input of the gate through the transistors and the drain line and back to the

gate line. In order to mathematically analyze this behavior, consider just the amplifier

circuit in figure 4.1. As derived earlier, the equation for the voltage gain of this amplifier
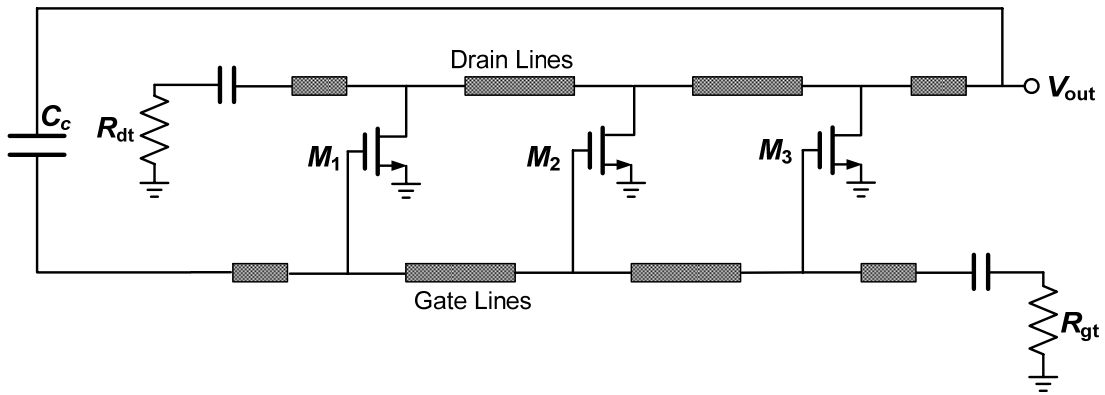
Figure 4.1 Generalized concept of a distributed oscillator.

is given by:

$$G = g_m^2 Z_d Z_g \left| \frac{\gamma_g l_g [\exp(-\gamma_g l_g n) - \exp(-\gamma_d l_d n)]}{\gamma_g^2 l_g^2 - \gamma_d^2 l_d^2} \right|^2 \tag{3.12}$$

which can be rewritten for a general case as [91]:

$$G = -g_m (Z_d \| Z_g).e^{-(\gamma_d l_d + \gamma_g l_g)/2} \cdot \frac{e^{-\gamma_d n l_d} - e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}}. \tag{4.1}$$

In the special case, where the gate and drain propagation constants are equal, i.e. when the structure allows equal phase velocities in both these lines,

$$\gamma.l = \gamma_d l_d = \gamma_g l_g \tag{4.2}$$

This simplifies (4.1) as:

$$G = -ng_m(Z_d \parallel Z_g).e^{-n\gamma.l}$$

$$= ng_m(Z_d \parallel Z_g).e^{-n\alpha.l}e^{-jn\beta.l}. \tag{4.3}$$

Now considering the feedback condition, the total open loop gain of the oscillator must be equal to -1, and therefore:

$$ng_m(Z_d \parallel Z_g).e^{-n\alpha.l}e^{-jn\beta.l} = -1 \tag{4.4}$$

In order to satisfy this condition, the imaginary component of LHS must equal 0. This implies that:

$$n\beta.l = \pi \tag{4.5}$$

Substituting for $\beta = \dfrac{2\pi f}{v_{phase}}$ in (4.5), we obtain an expression for frequency of oscillation

as:

$$f_{osc} = \frac{v_{phase}}{2n.l} \tag{4.6}$$

(4.6) implies that for maximum frequency of oscillation, the number of stages as well as segment length must be minimized. Another interpretation of the above equation could be obtained by considering the total capacitance and inductance associated with the drain and gate segments. That is:

$$f_{osc} = \frac{1}{\sqrt{L_{tot}.C_{tot}}} \qquad (4.7)$$

where $L_{tot}=2.n.l.L$ and $C_{tot}=2.n.l.C$.

Thus, using smaller transistors and greater number of stages tends to increase the resonant frequency of the oscillations.

In order to perform tuning operation on this oscillator, there are several viable options. It must be noted that using external varactors proves detrimental to the overall operation as they tend to degrade the resonant frequency by increasing the total capacitance. An efficient way to tune the oscillator is to tune its intrinsic parasitics at the drain-source and gate-source nodes. However, doing so might alter the operating point of the transistors. In order to prevent this, the transistors could be biased separately with current sources while DC voltages could be applied which could tune the transistor parasitics appropriately. Tuning ranges up to 14% have been obtained by just following this method [91].

A huge drawback of the distributed voltage controlled oscillator is once again the typical shortcoming of the distributed amplifier structure– large chip area and power consumption. In the next section, an ultra-compact distributed VCO is proposed and implemented by utilizing artificial transmission lines instead of bulky transmission lines that have been exclusively used hither to.

4.2   LC tank based VCOs Vs DVCOs

LC tank based VCOs are currently the most popular topology for VCO

(a)

(b)
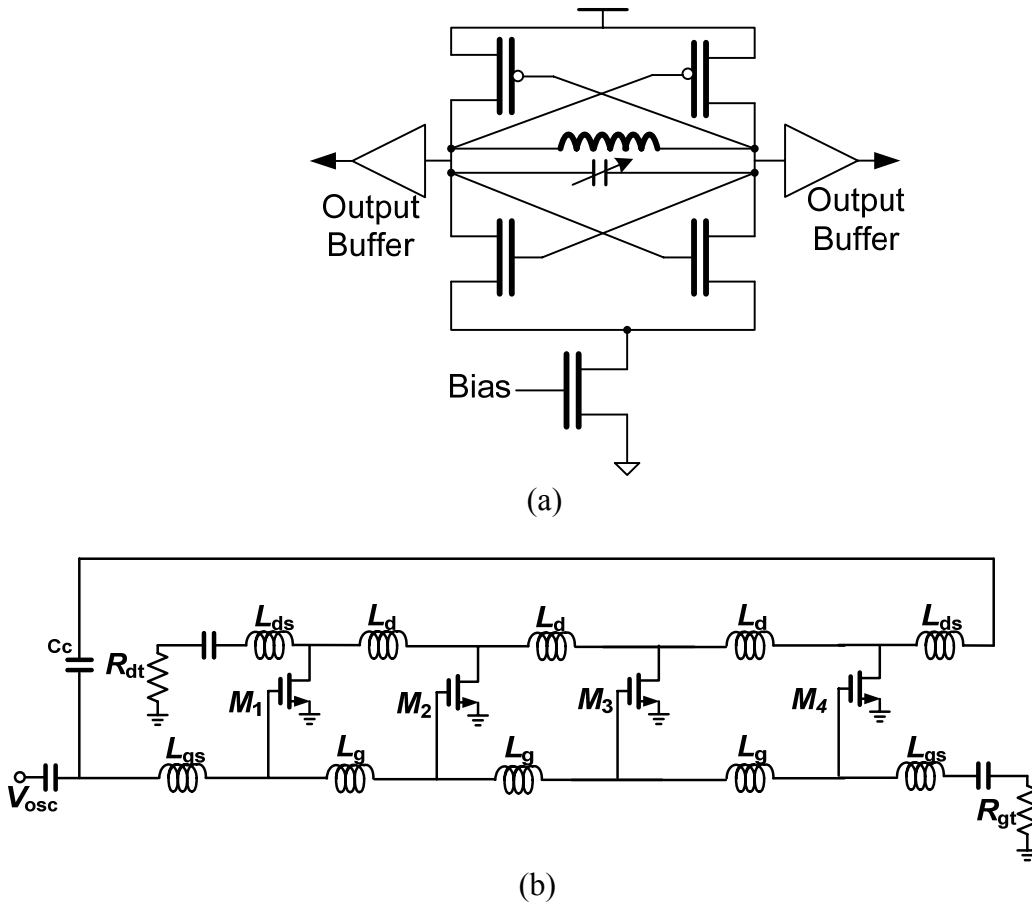
Figure 4.2 (a) LC-tank based VCO and (b) Distributed VCO.

implementation in CMOS technologies. A general schematic is shown in figure 4.2 (a).

LC tank based VCOs provide superior phase noise at lower power dissipation compared

to distributed VCOs. However, their main drawbacks are their limited tuning range and

excessive dependence on the transistor speed. Also, at multi-gigahertz applications, the smaller inductor values necessitated by the VCO that controls the frequency of operation, lead to higher power dissipation as the inductance operates in a parallel LC tank. On the contrary, distributed oscillators offer the possibility of wideband tuning range at a moderate level of power consumption. They also facilitate the possibility of multiple-phase signals using different stages that eliminate the need for power consuming divide-by-2 digital circuits or lossy poly phase filters. Also, the operational frequencies of the distributed oscillators depend on the round trip time delay of a signal, they do not depend on the speed of the transistor alone, and can be fine tuned by the additional degree of design freedom. However, their bulky size and power consumption are two main aspects that need to be addressed before making them compatible with LC-tank based VCOs.

4.3   Multi-stage DVCOs using inductors

Silicon distributed VCOs have been hitherto implemented employing only transmission lines in either CPW or microstrip form. However, practical results indicate that DVCOs do not implement favorably in comparison with LC-tank based VCOs, which typically occupy less than 0.1 mm^2 at higher frequencies. Table 4.1 shows some recently reported DVCOs. CMOS based DVCOs tend to occupy a significantly large chip area owing to their dependence on transmission lines. Utilizing inductors instead is a good alternative as they tend to provide greater inductance per unit area than

Table 4.1 Performance of some recently reported silicon based DVCOs

Reference	Technology	Oscillator frequency (GHz)	Tuning range (%)	Phase Noise (dBc/Hz@ 1MHz)	Die Area (mm^2)	Power Consumption (mW)
[90]	0.18 μm CMOS	16.6	-	-110	**>2**	52
[91]	0.35 μm SiGe BiCMOS	10.2	18	-114	**1.4**	35
[93]	0.18μm CMOS	10	14	-113.7	**0.91**	156

transmission lines conserving chip area. However, in most modern CMOS technologies, single layered inductors tend to occupy large chip areas since even most single-layer inductors also suffer from poor chip area consumption. Using an integrated multilayered inductor approach seems to be the most economical solution. Some important properties of these multi-layered inductors are studied as under.

The number of design stages of the distributed oscillator employing such inductors as L_d, L_g could be estimated by a simplified expression[1]:

$$n_{opt} = \text{mod} \, | \frac{2}{\gamma.l} + \frac{1}{G_m Z_{imp}} |$$ (4.8)

where $\gamma.l = \gamma_d l_d = \gamma_g l_g$ as in (4.2) and $Z_{imp} = Z_d \parallel Z_g$ where Z_d and Z_g are the impedances associated with inductors L_d and L_g, while G_m is the large signal transconductance of the transistor.

Employing multi-layered inductors, the impedances of drain and gate segments are replaced by the total inductance of each drain and gate segment. Since they are both equal:

$$Z_{imp} = \frac{Z_d}{2} = \frac{j.\omega.L_{tot}}{2} \qquad (4.9)$$

An expression for L_{tot} is obtained from the Greenhouse approach and (3.12) for the integrated inductor segment. Therefore, (4.8) can be re-written as:

$$n_{opt} = \mod | \frac{2}{\gamma.l} - j.\frac{2}{G_m.\omega.L_{tot}} | \qquad (4.10)$$

(4.10) implies that at least two stages are necessary in the design and implementation of distributed amplifiers.

Another important issue is the impact of number of stages of a DVCO on the output signal amplitude and phase noise. Both the output signal amplitude as well as the phase noise vary with the number of stages of a DVCO. A greater number of stages increase the inductive losses through the multi-layered structure as well as the cyclostationary noise associated with the MOS transistors. An expression for phase noise for distributed oscillators is given by [93] as:

$$\{\Delta\omega\} = 10\log\left(\frac{Z_0^2 \sum \Gamma_{eff,rms}^2 .i_n^2 / \Delta f}{V^2} . \frac{f_0^2}{2\Delta\omega^2} \right) \qquad (4.11)$$

with $\Gamma_{eff,rms}^2$ being determined by the transistor's cyclostationary properties, Z_0 being the

---

[1.] See Appendix B for derivation

characteristic impedance of a drain or gate segment, i_n being the input referred current component of noise of the transistor, Δf is the frequency offset, V is the voltage of the input signal and f_0 indicates the oscillation frequency For integrated multi-layered inductor sections, the transmission line characteristic impedance is replaced by the effective impedance of the drain or gate segments, i.e., $2.Z_{imp}$ as defined in (4.9).

4.4 A 15 GHz CMOS DVCO with wide tuning range

In this section, a 15 GHz distributed voltage controlled oscillator with a wide tuning range is designed and presented. The circuit employs the novel multi-layered inductors presented in an earlier section instead of transmission lines in order to significantly minimize the circuit dimensions. Before delving into the implementation details, a discussion on multi-stage distributed VCOs is presented.

4.4.1 Design principles

The inductor segment shown in figure 4.3 is analytically studied in order to find out the impact of negative mutual coupling on the overall performance. It is analytically calculated that the impact of first order positive mutual coupling overwhelms the net negative coupling, thereby causing a slight increase in overall inductance. Full wave EM simulations were then performed in IE3D to carefully optimize and design this structure. The inductance is intentionally kept low as it entails several advantages apart from the obvious size reduction. Firstly, lower inductance makes it easier to enhance the quality factor as well as self resonant frequency of the inductor, independent of the technology
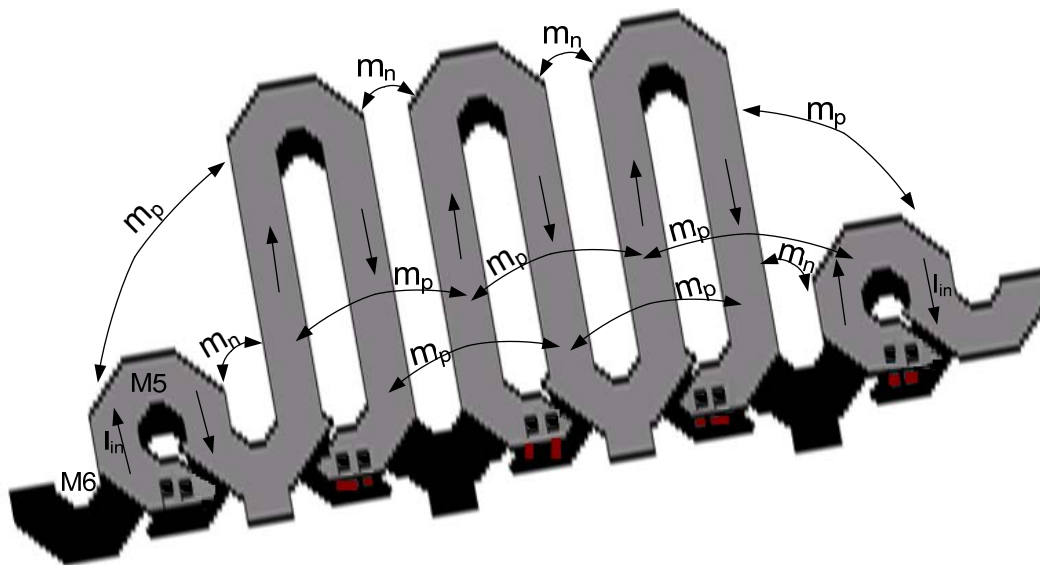
Figure 4.3 Integrated inductor segment using multi-layered inductors.

of implementation and without any further trade-off. Secondly, it makes it possible to use transistors of smaller aspect ratios which enable lower power consumption. The terminal inductors are kept at 0.3 times the value of the central inductors for matching purposes. The larger inductances are 0.75 nH while the smaller ones are just 0.25 nH. The oscillation frequency depends on the round trip delay time of the drain and gate inductor segments and is given by (4.6). The gate capacitances are controlled by an external bias which provides the tuning mechanism for this oscillator. A concern here is that any strong variation in the gate voltage to get additional tuning might displace the transistors from their DC operating points. This could be averted by fixing the drain current with constant current sources.

The VCO is primarily designed as a high gain, broad band, unstable amplifier. A four-stage implementation is implemented as the transistor aspect ratios are kept small for power consumption purposes. The W/L ratio of each transistor that satisfied the
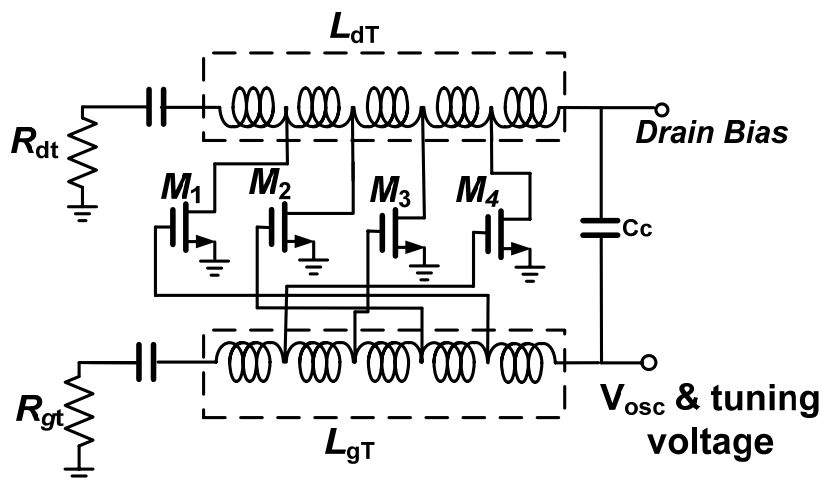
Figure 4.4 Schematic of the multi-layered inductor based DVCO.

power and matching requirements was 128μm/0.18μm. In order to further minimize the dimensions, the lengthy drain to gate feedback line is replaced by transistor gate to gate inductance segments, which are reverse connected as shown in the schematic of figure 4.4. Successive IE3D iterations of the multi-layer structure are imported into Agilent's ADS to optimize the transistor gain blocks of the circuit. A simple common-source transistor was used as the transistor gain block. The high-frequency transistor models were obtained from the design kit provided by JAZZ CA18HR 0.18 μm process.

4.4.2   Implementation and results

After the multi-layered inductor segment was laid out in Cadence, post layout simulations were carried out by re-performing simulations in IE3D and imported to ADS after their layout in Cadence. The total chip area is just about 0.08 mm^2, including the RF pads, while the core occupies only 0.06 mm^2 as evident in figure 4.5. The post layout simulated results for the VCO spectrum, tuning and phase noise are shown in figure 4.6. The VCO generates a 12% tuning range from 14.1 to 15.8 GHz centered around 14.9 GHz within reasonable limits of current consumption. The output spectrum shows a peak harmonic at 14.9 GHz while the phase noise at 1 MHz offset is -100.2 dBc/Hz. This performance is facilitated by a current consumption of 19 mA from a 1.8 V source.
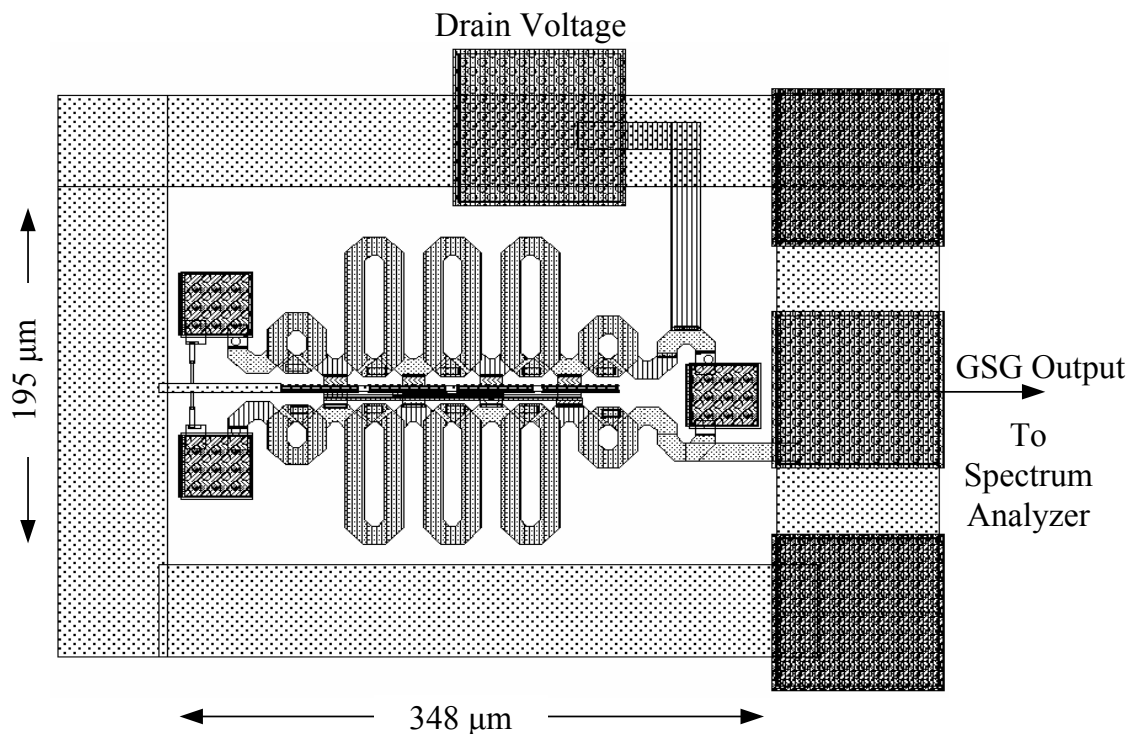
Figure 4.5 Layout of the multi-layered inductor based DVCO.
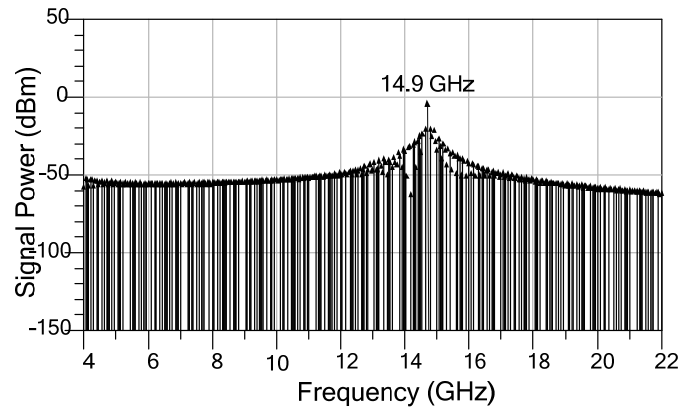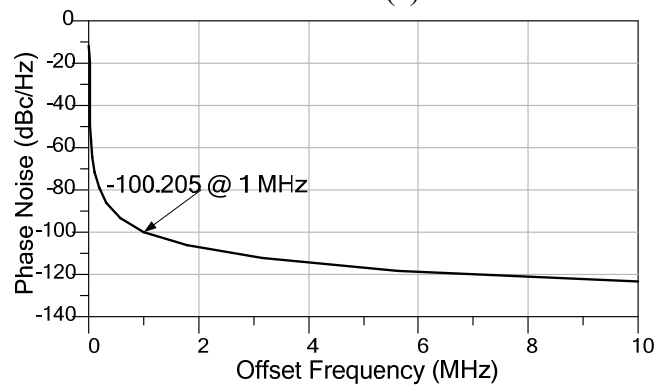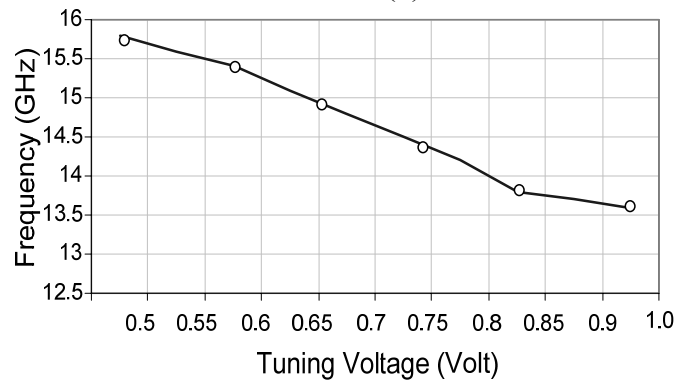
Figure 4.6 Simulation results of the multi-layered inductor based DVCO (a) Output spectrum (b) Phase Noise and (c) Tuning Range.

CHAPTER V

DUAL BAND UWB RECEIVER SUBSYSTEM

Traditionally, multi-band radios have been highly desired in RF wireless communications. The strong impetus for multi-band radios stems from requirements of miniaturization and low power consumption that make products attractive in the wireless market. Multi-band radio systems came into prominence to provide chip solution to different wireless standards catering to the same application but utilizing different frequency spectra. A single radio receiver could operate over different frequency spectra that could cover the world wide 3G standards for cellular applications [94]. This concept could be further extended to integrate chip solutions for different standards and applications on the same chip. A single chipset would be therefore utilized for different applications For instance, [95] discusses the integration of WLAN and WPAN (Bluetooth) standards on a single chipset that would enhance component integrability, lower the power consumption and chip area.

Till date, the concept of multi-band radio has been largely confined to narrowband applications. However, with the market driven need for greater data rates, wideband applications are steadily gaining prominence in wireless communication. One such protocol that targets the wideband market is Ultra wideband (UWB) that promises data rates up to several hundreds of Mbps. The FCC had earlier identified UWB signals as those having a -10 dB bandwidth of at least 500 MHz in the 3.1 to 10.6 GHz spectrum subject to some other power spectral density restrictions, which will be discussed shortly. While multi band orthogonal frequency division multiplexing (MB-OFDM)

technique has been approved as an ISO/IEC standard for UWB, the proposal emphasizes that only the lower band from 3.1-4.8 GHz as mandatory while the rest of the bands are deemed optional and could be implemented when the technology matures. This definition allows designers to solicit applications that could implement multi-band systems that do not contradict the FCC requirements for MB-OFDM by utilizing just two bands, the mandatory lower band (3.1-4.8 GHz) and one of the upper bands (6-8 GHz), for multi-functional applications.

The current chapter proposes a dual band UWB receiver sub-system that simultaneously operates in two different bands while preserving the MB-OFDM industrial standard requirements. System related issues as well as circuit components are discussed at length in this chapter along with implementation of the sub-system in JAZZ 0.18 μm technology [65] and the obtained results. But first, an overview of UWB communications and related theory is presented to better understand the concept of the proposed dual band UWB application.

5.1   UWB communications

History of UWB communications dates back to the 1960s, when Ross et al [96] conceived the concept of short-duration, carrier free pulses by characterizing the impulse response of multi-port microwave networks. The initial interest in UWB was confined largely to military due to the low signal imperceptibility and extraordinary resolution. Commercial interest in UWB began to surface in late 90s due to the increasing demands for high data rates beyond the capability of existing WPAN standards like Bluetooth.

FCC has regulated the Equivalent Isotropically Radiated Power (EIRP) emissions from UWB devices to be below the noise floor at -41.3 dBc/Hz to facilitate its co-existence with existing wireless PAN and LAN standards in the 3.1 to 10.6 GHz spectra [97] as shown in figure 5.1.

As figure 5.1 shows, UWB signals tend to occupy a large bandwidth at the expense of
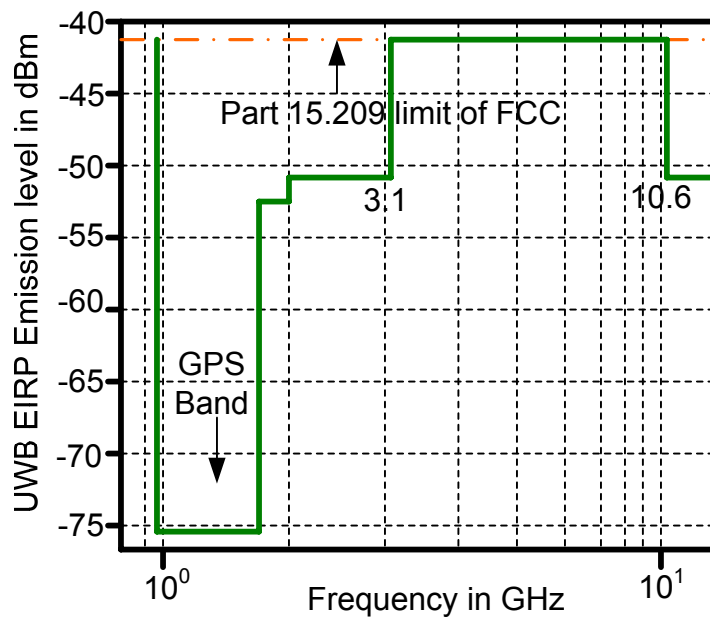
Figure 5.1 EIRP emission level for UWB devices.

small power spectral density. This large bandwidth translates to increased data rate transfer as observed from the Shannon-Hartley theorem [98]:

$$C = B \log_2 (1 + SNR_{sys}) \tag{5.1}$$

where C is the Channel capacity in bits per second, B is the system bandwidth in Hz and SNR_{sys} is the signal-to-noise ratio of the system within the bandwidth of interest. The

system's SNR could be enhanced to improve the channel capacity, but it would require increasing the signal transmission power. UWB provides a more direct solution by lowering the transmission power and utilizing greater bandwidth to increase the channel data transfer capacity. The low transmission power enables minimal interference with existing standards.

Since the definition of UWB by FCC in 2002, proposals catering to standardizing this technology were finalized by the end of 2003. They were grouped under two categories - one was Direct Sequence UWB and the other was Multi-band Orthogonal Frequency Division Multiplexing (OFDM) based UWB. The former, also known as impulse radio or "carrier-free" approach requires the transmission of small period pulses that spread the signal energy over a large bandwidth. The pulse repetition is obtained by a pseudo random noise code and the bit generation is applied by either Binary Pulse amplitude modulation (PAM) or Pulse position modulation (PPM).

On the other hand, the multi-band OFDM approach relies on dividing the 7500 MHz spectrum from 3.1 to 10.6 GHz into 14 smaller bands, each measuring 528 MHz and grouped into 5 band groups. Each band is further divided into 128 sub-channels each measuring 4.125 MHz. This approach is illustrated in figure 5.2. The reason for the presence of so many channels is to employ the concept of frequency hopping, i.e., information is interleaved across all the bands belonging to a particular group and the system switches between them, so that system robustness is improved and multi-path effects would be better handled. The switching speed is limited to 9.47 ns which poses some strong constraints on the frequency synthesizer. An important aspect of this
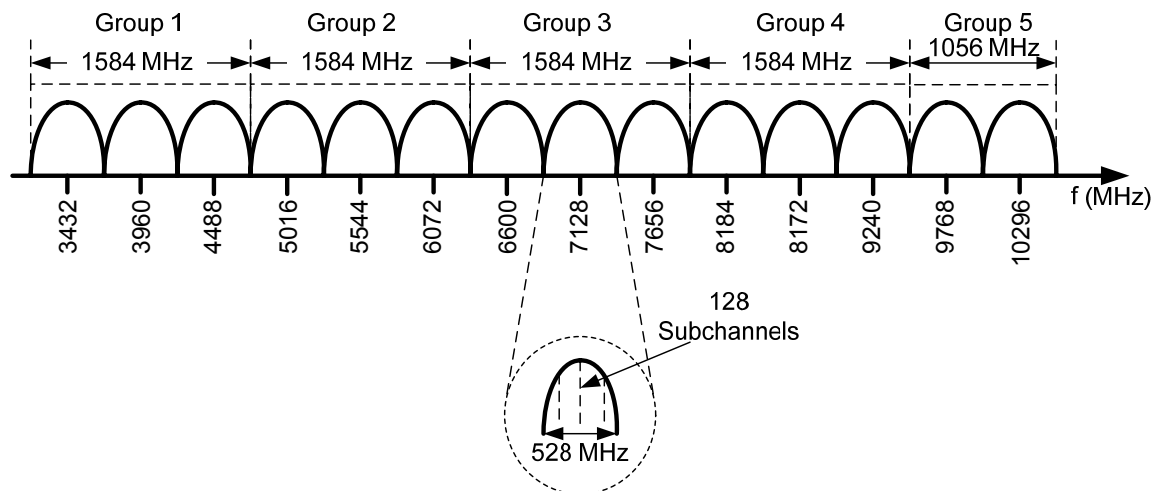
Figure 5.2 Band plan for the multi-band OFDM approach.

proposal is that only the first band group ranging from 3168 MHz to 4752 MHz is mandatory, while the rest of the band groups are deemed optional. The proposed approach also solicits employing Quadrature Phase Shift Keying (QPSK) modulation instead of pulse based modulation techniques like in the case of DS-UWB.

The MB-OFDM approach was able to garner strong support from both the industry and academia owing to its robustness to multi-path effects, improved spectral efficiency and minimal interference to existing narrowband standards. It was approved as an ECMA industrial standard in December 2005 [99] and as an ISO/IEC international standard in March 2007 [100].

5.2   Multi-band receiver systems

The need for multi-band receiver systems arose from realizing cost-efficient, miniaturized solutions to different standards while simultaneously improving the functionality of the over all system. It typically involves a trade off between the cost of processing the signal and the means by which the signal could be down converted into the baseband. The predominant approaches used in multi-band receiver system design are explored below.

5.2.1   Heterodyne architecture

Typically, narrow band heterodyne receivers down-convert an incoming RF signal in
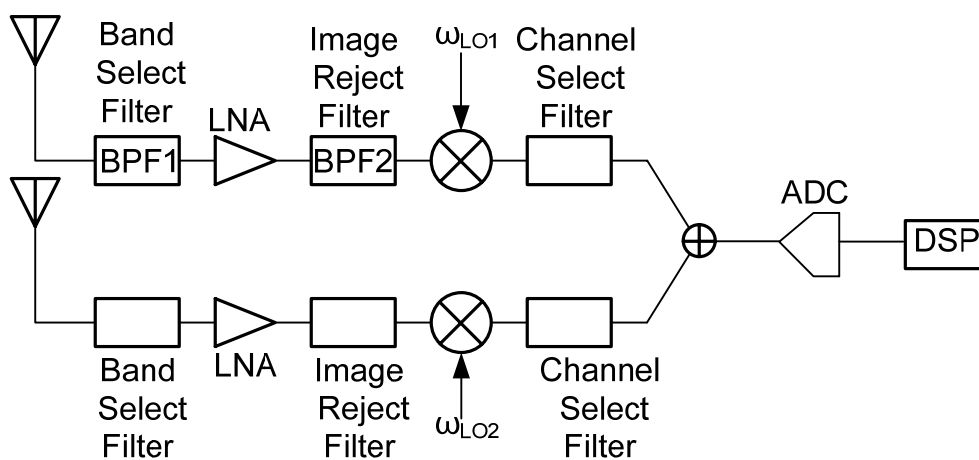
Figure 5.3 Typical multi-band heterodyne receiver architecture.

multiple steps by mixing and filtering, such that the quality factor requirements on the channel select filters, that select the band of frequencies containing the modulated signal, are significantly minimized. However, the quality factor requirements are still so high

that they cannot be easily realized with on-chip filters and hence, external filters are required. Filtering is a crucial aspect of the heterodyne architecture as they suffer from image frequency problem. Image frequency is that undesired input RF which is located at a distance of twice the intermediate frequency from the desired frequency band. Because of the cosine mixing properties, the image frequency also gets down converted along with the desired signal which leads to deterioration of system SNR. In multi-band heterodyne receiver sub-systems, the image problem is sorted out by a careful choice of LO signal between the two RF bands. And to further curb this problem, a large number of high-Q, external image reject filters are also utilized. Needless to say, this approach defeats the concept of multi-band radio as it adds to higher system cost and larger area. A typical multi-band receiver employing heterodyne architecture is shown in figure 5.3.

5.2.2   Homodyne architecture

Homodyne architecture allows the RF signal to be directly converted to the baseband thereby removing the image problem. Owing to the one-step conversion process, the dynamic range requirements of the mixers must be very high. Furthermore, since most modern modulation techniques employ either frequency or phase modulation, quadrature mixers are necessary so as to avoid loss of information while the RF input signal is being down converted to DC. By altogether removing the possibility of image interference, homodyne architecture removes the need of bulky external filters and requires only simple low pass filtering. However, it suffers from some serious issues relating to quadrature phase errors, quadrature phase and amplitude mismatch, 1/f noise, LO self
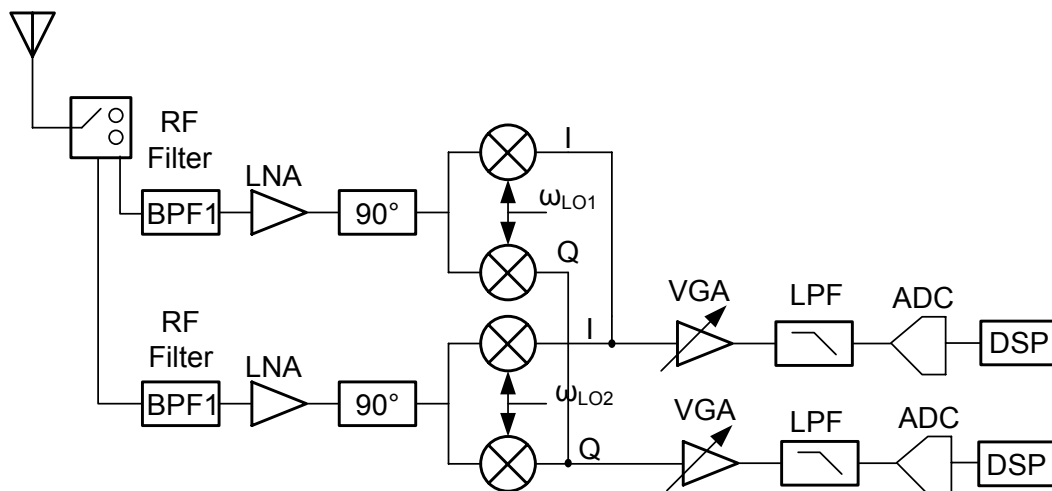
Figure 5.4 Dual-band homodyne receiver architecture for WLAN applications [101].

mixing and DC offset. The DC offset is a serious problem resulting from the extraneous voltages leaking into the receiver system that also get down converted to the DC output thereby presenting unwanted signal energy at the output. The elimination of this problem requires some correction circuitry at the baseband. The multi-band implementation utilizing the homodyne architecture is shown in figure 5.4 for the twin bands of IEEE 802.11 a/b/g WLAN [101].

5.2.3   Image rejection architectures

Both the homodyne and heterodyne architectures shown above require bulky additional external high Q filters that enhance the cost of system implementation. Image rejection architectures, on the other hand, facilitate the rejection of image through an orthogonal down conversion of the incoming RF signal. Most modern image rejection architectures are heavily drawn from the theory proposed by Hartley [102] and Weaver

[103]. A multi-band 900-MHz/1.8-GHz receiver architecture was proposed by Wu and

Razavi [104] that employs effective component sharing to minimize the die area as well
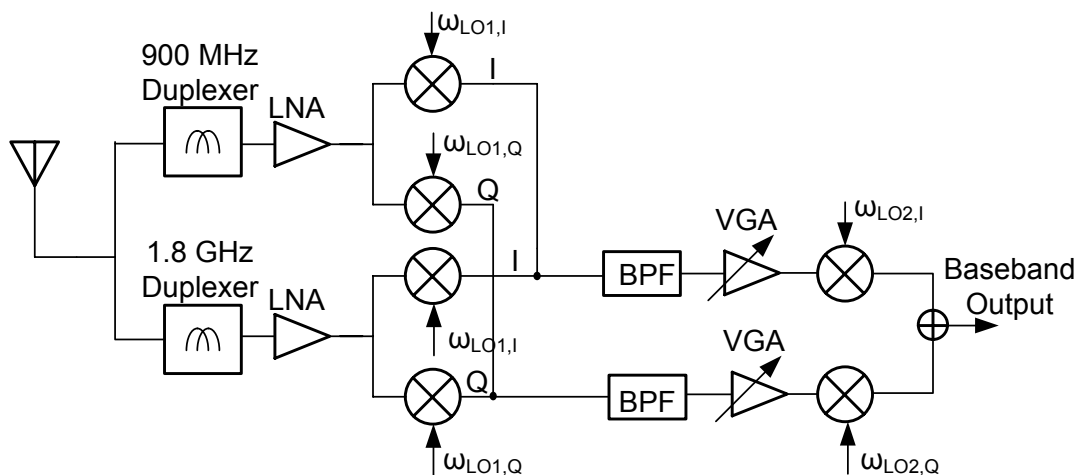
Figure 5.5 Dual-band Image rejection receiver architecture [104].

improve the receiver functionality is shown in figure 5.5. In spite of being cost efficient

and improved in functionality, image rejection architectures could suffer from potential

I-Q gain and phase mismatches resulting in insufficient rejection of image.

5.2.4   Concurrent narrowband architectures

The concept of concurrent receiver was first proposed by Hashemi et al [88] in order

to solve the problem associated with the excessive power consumption problem

associated with existing multi-band architectures based on switching and control

technology. The novelty of the approach lies in obtaining a multi-band response

intrinsically, from the system components itself, without the need for any additional
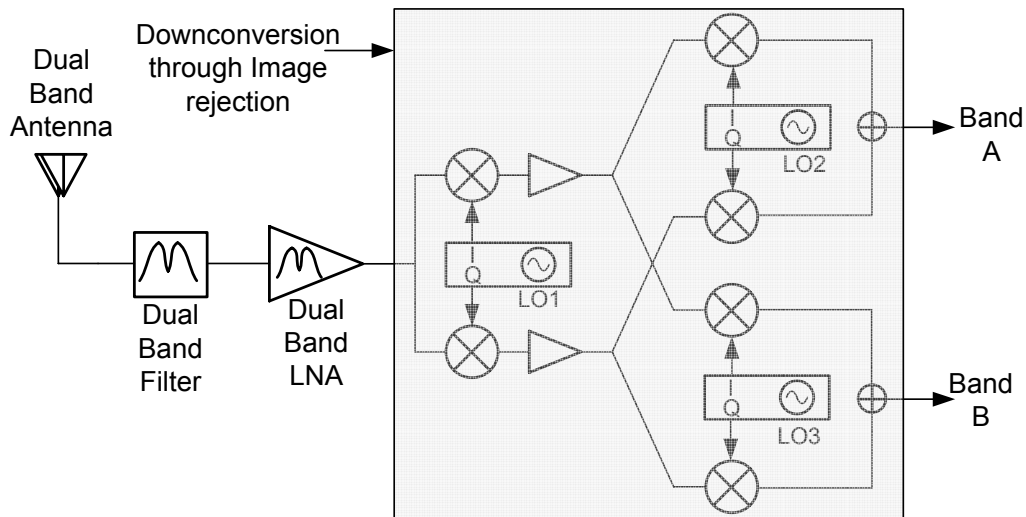
Figure 5.6 Concurrent dual-band receiver architecture for Bluetooth/WLAN applications [105].

control circuitry or parallel stages. The above mentioned receiver architectures could illustrate this point. In each of these architectures, a distinct LNA and input filter is required to operate at distinct frequency ranges. In a concurrent architecture, on the other hand, the circuit components operate simultaneously at different frequencies while ensuring maximum attenuation of out of band signals. A concurrent receiver architecture relying on image rejection down conversion is shown in figure 5.6. The architecture has three concurrent elements – including a dual band antenna, dual band RF filter and dual band LNA and some down conversion circuitry based on image rejection principle suggested by Weaver [103]. The receiver simultaneously operates in two bands by channeling two desired input RF signals simultaneously with the aid of the three concurrent elements, but from there onwards the signal is down converted separately through the dual-band image reject architecture shown in figure 5.5.

There are several issues to be addressed while analyzing the concurrent architecture. The most important ones are the choice of the LO frequencies and the linearity requirements of the concurrent elements, especially the low noise amplifier. The LO frequency selection needs special emphasis as there could be an accidental image signal if the LO is chosen mid way between the two bands of interest. In order to avoid this problem even in image reject architectures, it is recommended to offset the LO frequency from the mid point of the center frequencies of both bands. This allows the translation of the image to a much lower frequency and could be easily filtered out with internal channel select filters. The need for high linearity LNAs arises from the possibility of a strong channel in one band affecting the signal strength in the other. Any non-linearities in the system would lead to inter-modulation products resulting from the mixing of these frequencies to fall within one of the bands of interest. Thus, the system requirements mandate higher linearity components, specifically the low noise amplifier.

5.3 Dual band UWB receiver front end

Till date, implementation of RF front ends for UWB applications has necessitated the operation of the front end over the entire 14 band spectrum. However, the MB-OFDM proposal has mandated only the first band group's operation while leaving the others as optional [97]. This has given an opportunity to experiment with a concurrent architecture for potential application to MB-OFDM. That is, the concept of narrow band concurrency is reconciled to multi-band OFDM based wide band receivers in order to create a dual band UWB front end. The proposed receiver operates from 3.1 to 4.8 GHz in the first

band and 5.8 to 7.6 GHz in the second band there by satisfying band groups 1 and 2 of the MB-OFDM proposal. The implementation details as well as design issues are discussed in this section.

5.3.1   Principles of concurrent dual band UWB front end

The concept of concurrent dual band UWB relies on shaping the receiver front end transfer function such that two distinct wideband channels are formed which could be utilized for MB-OFDM applications. The typical approach of satisfying the MB-OFDM proposal relies on having constant wideband amplification through the entire UWB
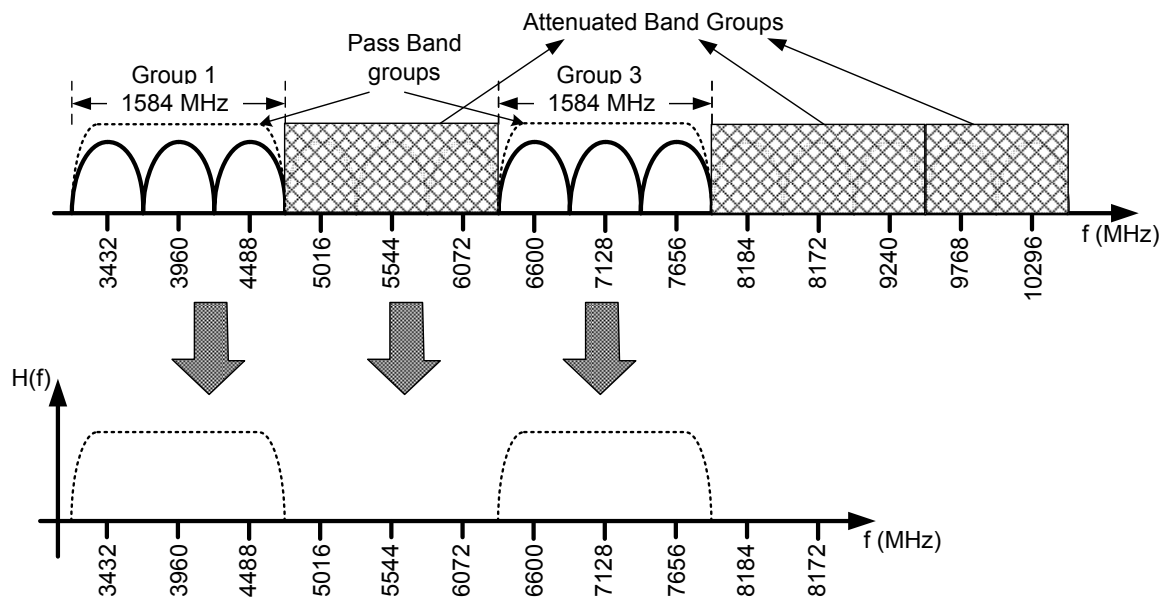
Figure 5.7 Dual band receiver frequency plan for MB-OFDM applications and proposed dual band receiver front end transfer function.

spectra. For satisfying two band groups of the MB-OFDM, the transfer function of the receiver front end could be so tailored that only the first and third groups are passed

while the second group is attenuated. The receiver front end transfer function is depicted in figure 5.7. The advantages of having a concurrent dual band approach rather than the wideband approach are greater flexibility of application, lower interference to existing WLAN applications in the 5.1 to 5.8 GHz band, possibility of greater circuit miniaturization and lower power consumption.

The realization of this transfer function could be achieved by a non-concurrent approach by controlling the frequency bands with external digital circuitry that can allow only one frequency band to operate at a time. However, the transfer function would then be dependent up on the non-idealities as well as the losses of the switch, further leading to deterioration of gain and increasing the gain ripple in the pass band. Concurrency removes the need of parallel architectures or switches by allowing for a tailored frequency response inherently from the low noise amplifier itself. Such a receiver front end has been demonstrated for narrow band applications in [88]. But for developing a wideband concurrent wideband receiver, the implementation could be sub-divided into two parts – achieving a wide band amplifier response and generating a wide stop band in the amplifier. This principle needs to be achieved only by the low noise amplifier because its transfer function is multiplied to the mixer transfer function, which therefore only needs to be broadband with a constant gain in both the frequency bands as well as the stop band.

For MB-OFDM, wideband concurrency could be accomplished by incorporating resonant loads at the input and output segments of a wideband distributed amplifier. This leads to better control over input and output matching. An important feature of the

proposed receiver is that there is significant attenuation of the signal in the stop bands. This attenuation is achieved by resonating the input and output loads at two points of the desired stop band. The input and output resonant loads also ensure sufficient optimization of the input and output reflection coefficients for matching purposes by causing a wide stop band in the contour of the power gain transfer function.

5.3.2 Receiver architecture

A complete receiver system architecture based on the direct conversion principle is shown in figure 5.8. The architecture separates the two band groups in order to avoid the problem of image frequency of one band interfering in the other. The implementation requires two series RF SAW filters as increasing bandwidths usually result in deteriorating quality factors and greater losses for the external filters. It must be noted that each SAW filter is expected to operate in a distinct band group. The low noise amplifier provides dual band UWB operation based on utilizing input and output resonant loads to generate a wide stop band in a wideband distributed amplifier as described in the subsequent sections. The signal is channelized based on each band group through careful LO mixing. Each wideband mixer aids in translating one particular band of RF signal to an IF. Both the LO signals required for each band group could be generated by a 9-band PLL based frequency synthesizer, which is widely regarded as the single most crucial block in the UWB receiver design.
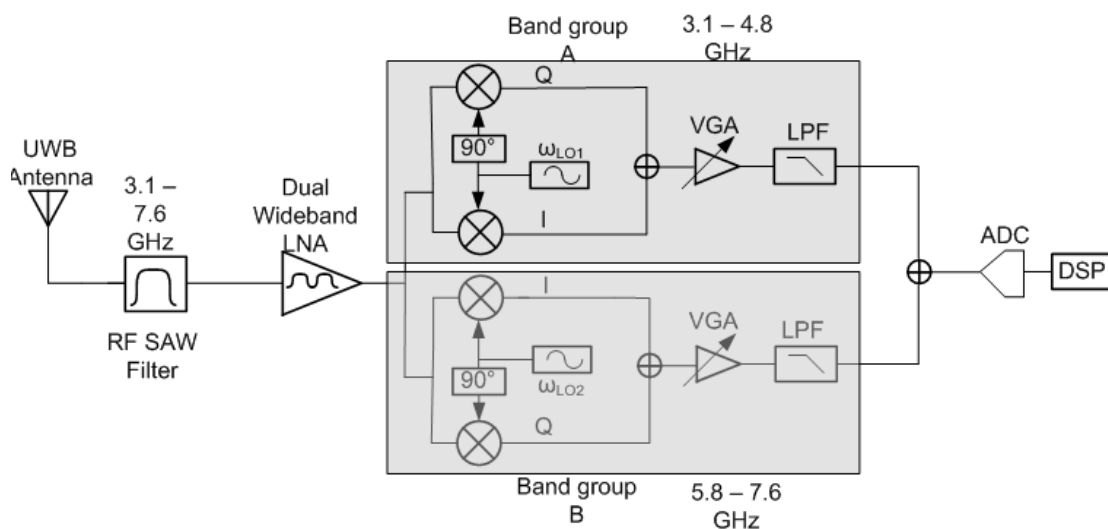
Figure 5.8 Dual band UWB concurrent receiver architecture based on the
homodyne principle.

In order to enhance the functionality of the receiver front-end, the current work

emphasizes more on the novelty of high linearity dual wideband RF front end that could

cater to not only UWB but any other future technology that could exploit wider

bandwidths through concurrency. Therefore, the implemented receiver front end is based

on the following architecture shown in figure 5.9 which is based on a simple heterodyne
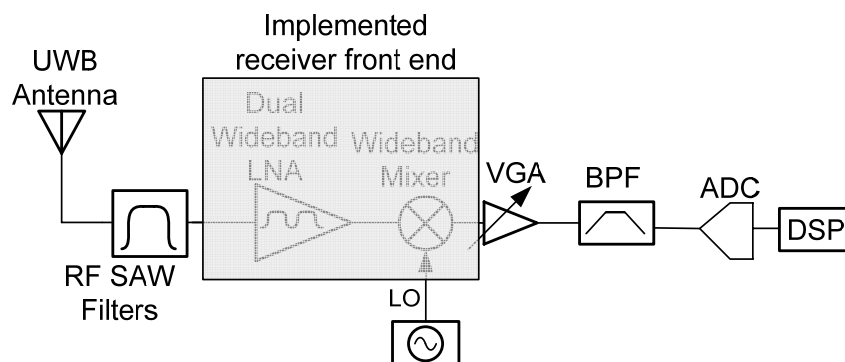
Figure 5.9 Implemented dual band concurrent receiver front end based on the
heterodyne principle.

principle. It must be noted that the designed receiver front end could be upgraded to a UWB- compatible architecture by incorporating a quadrature mixer.

5.3.3 Front end design issues and specifications

The block diagram of the implemented receiver front-end sub-system is shown in figure 5.10. The block diagram shows that several on-chip active baluns are necessary to transform the single ended to differential transition. Another necessity being that the high linearity low noise amplifier also suffers from moderate to poor gain and hence the active balun would not only facilitate single to differential conversion but also enhance the overall amplifier gain. The LO differential signal is also generated by an active balun
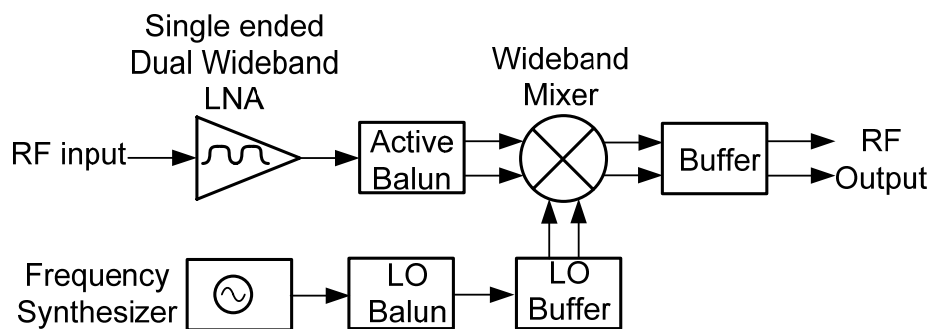
Figure 5.10 Block diagram of the implemented dual wide band concurrent receiver front end. All components except the frequency synthesizer are on-chip.

which generates precise anti-phase signals at the mixer's LO terminals. The LNA employs a novel ultra-compact distributed amplifier based topology that ensures very high linearity and excellent gain flatness in the frequency ranges of operation, as per the

specifications of the MB-OFDM. The need for high linearity in the LNA is explained by considering the original specifications for an ideal MB-OFDM system as shown below:

One of the important aspects of the MB-OFDM receiver is that it has to co-exist with existing narrow band channels in the 5-6 GHz region. This is particularly crucial because the most immediate application of MB-OFDM lies in wireless USB applications for personal computers and laptops where WiFi is already in existence in the 5.1-5.8 GHz

Table 5.1 MB-OFDM receiver specifications

Sensitivity	-73 dBm
Receiver NF	6-7 dB
Input 1-dB compression point	>-10 dBm
Data rate	480 Mbps
Channel Bandwidth	528 MHz
Gain	>70 dB
Switching time within band group	<9.47 ns

region. This imposes severe linearity requirements particularly on the receiver front end especially the low noise amplifier and it must therefore have a very high cross band IIP3 [105], a figure of merit that measures the effect of an interferer in an undesired band on the desired band, to prevent the interference of existing narrow band applications on these circuits. Furthermore, if the receiver front end were to be applied in a non-UWB multi-band application, the impact of a strong signal in the second band group would also adversely influence the signal in the first band group and vice versa. This once again emphasizes the need for having a high linearity low noise amplifier that ensures higher cross band IIP3 within both channels.

It must be noted that the specifications were derived based on simulations in system view [106] for a BER of 10^{-5} in each band group. The receiver sensitivity was required to be at least -70 dBm in deference to the MB-OFDM proposal. This places the receiver front end (which includes only the LNA and Mixer blocks) noise figure to be between 4-6 dB. The other specifications derived from system view closely follow the values presented in Table 5.1.

5.4 Front-end circuit blocks

5.4.1 Concurrent dual wideband distributed LNA

The concurrent dual wideband distributed LNA forms the most important block of the front end circuits owing to its strong influence on gain and linearity on subsequent sections of the receiver system. Several topologies were researched to arrive at the best possible candidate for implementing a high linearity, wideband amplifier. The existing topologies in wideband CMOS amplifiers could be broadly categorized into two – shunt/series feedback and distributed. Feedback amplifiers are implemented with lumped elements, on an average follow traditional analog design principles, consume low power and provide higher gain, but suffer from poor linearity while distributed amplifiers, provide much higher linearity, but occupy greater chip area and dissipate higher power [107]. For applications like MB-OFDM, with the upcoming wireless USB application, the issue of high linearity and signal integrity forces us to take a fresh look at the possibility of using the distributed amplifier as a possible contender for UWB design. The typical size of CMOS based distributed amplifiers is on average at least 1 x 1 mm^2
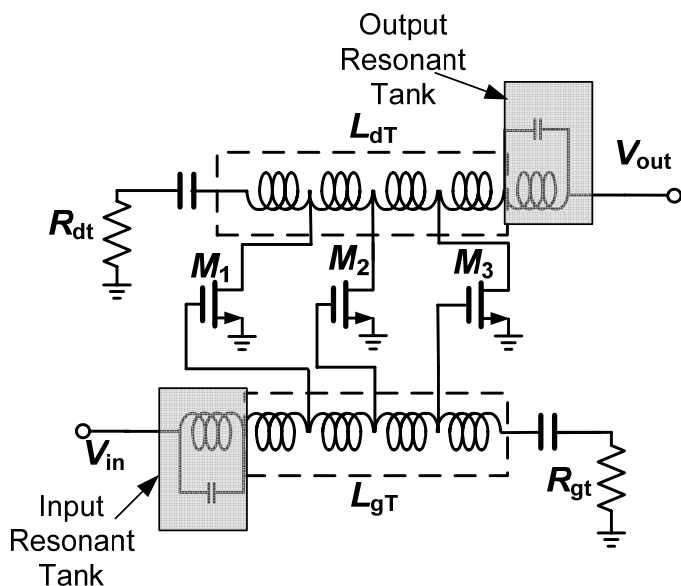
Figure 5.11 Three stage concurrent distributed amplifier with integrated multi-layered inductors and resonant input and Output tanks.

owing to the long transmission lines or traditional single layered spiral inductors that consume an exorbitant amount of chip area. In modern IC design, the entire RF and baseband segments of a receiver themselves do not consume that much chip area. Therefore, the linearity, lower gain ripple and larger bandwidth advantages of distributed amplifiers are easily offset by just this aspect itself.

To make the distributed amplifier a more viable contender in RFIC design, the concept of multi-layered inductors could be used and the impact of mutual coupling between adjacent inductors could be carefully analyzed so that extreme size miniaturization is possible. A distributed amplifier employing ultra-compact multi-layered inductors was successfully demonstrated in section 3.5. Its linearity was obtained

through post-layout simulations as +13.2 dBm at 10 GHz, indicating more than sufficient performance for MB-OFDM applications. In this section, the same distributed amplifier is employed as a wideband amplifier with input and output resonant loads to achieve the desired dual wideband operation, for MB-OFDM applications as well as any potential applications that involve high linearity, concurrent dual wideband amplifiers.

Figure 5.11 shows the schematic of the implemented concurrent dual wideband distributed LNA. The distributed amplifier described in an earlier section was utilized and loaded with input and output resonant tanks to create a wide stop band. The loading
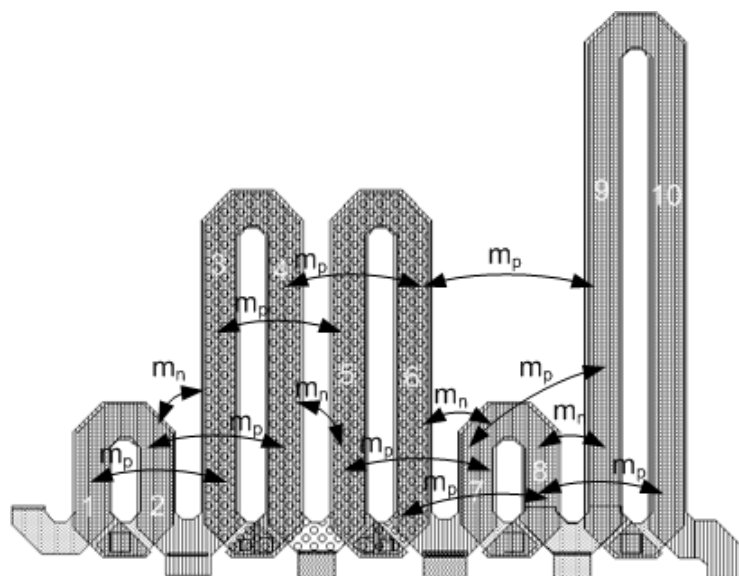
Figure 5.12 Layout of the integrated multi-layered inductors including tank Inductor and the positive (m_p) and negative (m_n) mutual coupling between segments.

inductor was integrated with the main inductor segment to so that the effect of its mutual coupling on adjacent inductors could be taken into account. The entire segment was then jointly simulated with a 2.5 D EM simulator, IE3D [44]. The integrated inductor
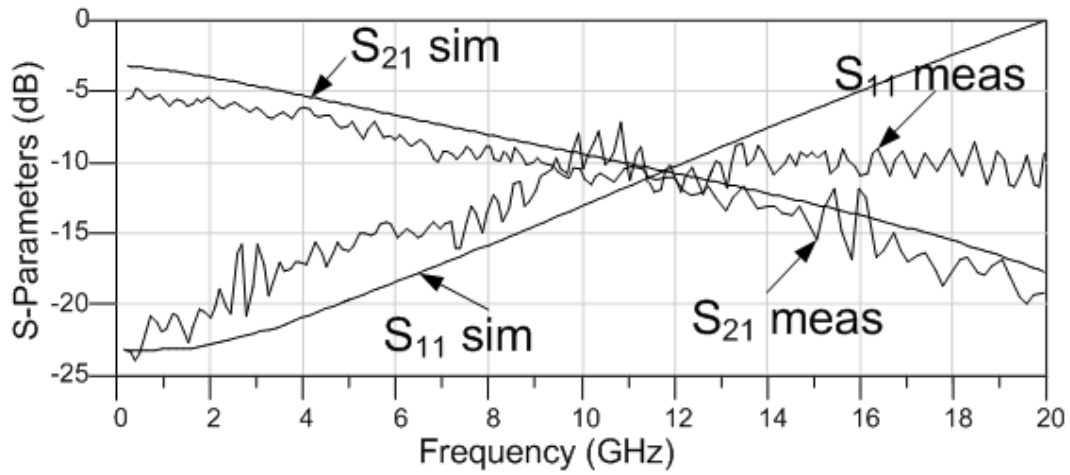
Figure 5.13 S-parameters of the integrated inductor segments of figure 5.12.

segment is shown in figure 5.11 with the resonant inductor shown by the segments 9 and 10.

Figure 5.12 shows the mutual coupling between different segments of the integrated inductors. Each segment is composed of different metal layers and multiple layers. The net inductance of the combined segments is given by:

$$L = \sum_{i=1}^{5} L_i + 2\sum_{j=1}^{8} m_{j,j+2} - 2\sum_{k=2}^{8} m_{k,k+1} \tag{5.2}$$

where L_i takes into account the composite inductance of each of the 5 inductors, $\sum m_j$ takes into account the positive mutual coupling between alternate inductor segments for all values of j and $\sum m_k$ takes the negative mutual coupling for all even values of k from 2 to 8.

The structure is then simulated in IE3D and jointly optimized as a 6-port network. This treats the inductor segments as transmission lines and also accounts for all the coupling effects of the 6-port network. The resulting s- parameters of the composite inductor segment are shown in figure 5.13.
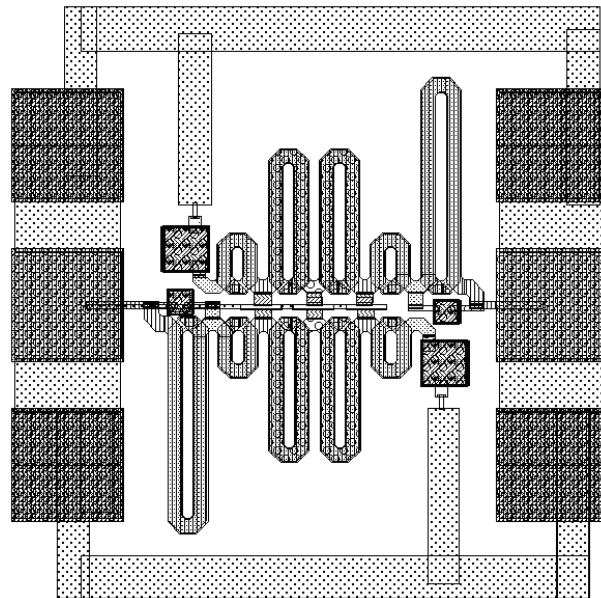
Figure 5.14 Distributed amplifier employing multi-layered inductors and input/output resonant loads .

After the inductor segment is designed the 3- stage distributed amplifier was redesigned to account for the changed impedance at each drain or gate node, due to the

altered coupling conditions arising from the presence of the resonant inductor. The
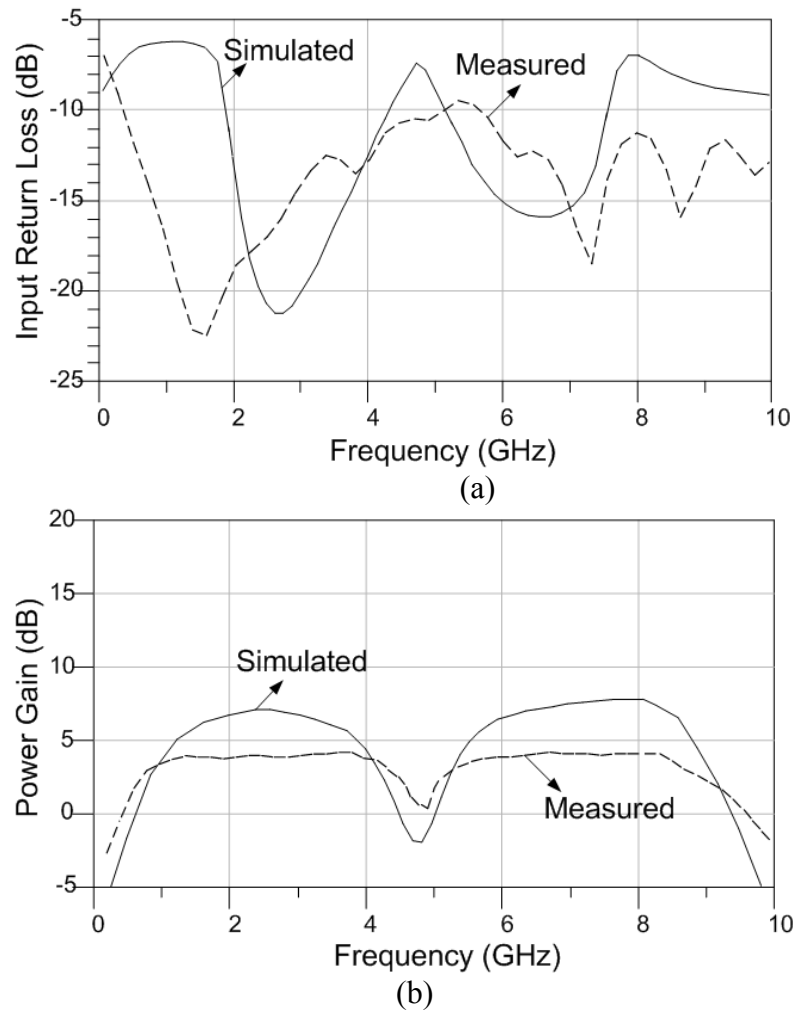
Figure 5.15 (a) Input return loss (b) Power gain of the distributed wideband
UWB amplifier and (c) Simulated LNA IIP3 in the second band (5.8-7.8 GHz).

resulting distributed amplifier now incorporates the same inductor segment at the gate

and drain portions whose properties can be completely and very accurately characterized

(c)
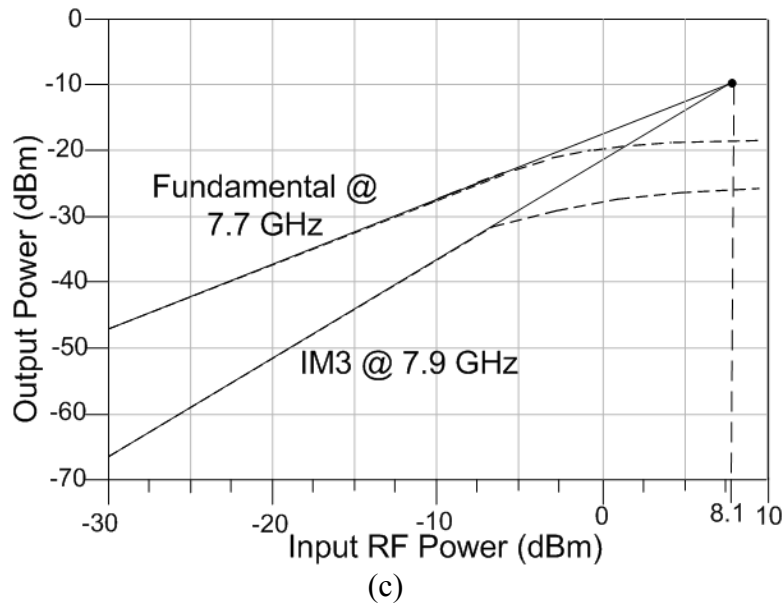
Figure 5.15, continued.

by EM simulators. In order to ensure that the circuit consumes a minimal chip area, inductor sizes are kept small. The smaller inductors are only 0.4 nH while the larger one measures 0.8 nH. The resonant tank inductors are 1.2 nH each and the chip capacitor in the resonant tank is 300 fF. The same resonant inductance with a small adjustment to the capacitance is used in the gate portion of the input. Figure 5.14 shows the layout of the distributed amplifier employing multi-layered inductors and resonant tanks. The DA was measured to have the s-parameters shown in figure 5.15. Figure 5.15(a) shows that the input return loss remains well below 10 dB easily covering both the bands of operation. The power gain, shown in figure 5.15 (b), has some deterioration in magnitude. However, it retains the dual wideband contour as the theoretical simulations. The discrepancy is found to be about 3-dB, the simulated average gain in each band at

this power level is 7.5 dB while the measured value is 4.3 dB. The reason for the discrepancy can be understood by characterizing the amount of loss associated with the input and output resonant tank circuits in the topology. The S-parameters of the integrated section were presented in figure 5.13. They indicate a higher insertion loss than expected and a slightly higher discrepancy between simulated and measured values of insertion loss. These values contradict the earlier result that indicated better correlation between the measured and simulated values for the distributed inductor segment in Fig. 3.15. This is attributed to the greater loss of RF power through the vias, which forms a spurious parasitic fringe capacitance, that hasn't been taken into account in the simulation. Figure 5.12 confirms the fact that the major source of loss is the passive segment of the amplifier and not any other source. And within the passive segment, the only parameters that haven't been effectively modeled are the vias. On further review it was found that the longer inductances at the end had a single via unlike the rest of the inductors compared to the rest of the components. This led to increased contact resistance at the via terminations. This problem did not exist for the distributed amplifier that was implemented earlier, as each multi-layer contact had numerous vias that lowered the contact resistance. Furthermore, the vias could not be modeled accurately with the EM simulation tool which otherwise takes every other non-ideality into account. It can be construed that the multi-layer inductor design presented in this chapter is more suitable for sub-nano Henry inductance values than larger inductors. The deviation is less prominent in the return loss measurement as can be observed from figure 5.14 (b) except for a slight shift in the frequencies. The measured values remain

well below -10 dB in both the bands of operation. As indicated in figure 5.14 (c), the LNA maintained a high linearity as shown by the simulated input IP3 of +8.1 dBm that was obtained with two single tone signals at 7.7 GHz and 7.8 GHz.. Further more, the LNA consumed 32 mW of DC power.

5.4.2   High gain active BALUN

Because of the poor power gain of the LNA, the subsequent stage involving the
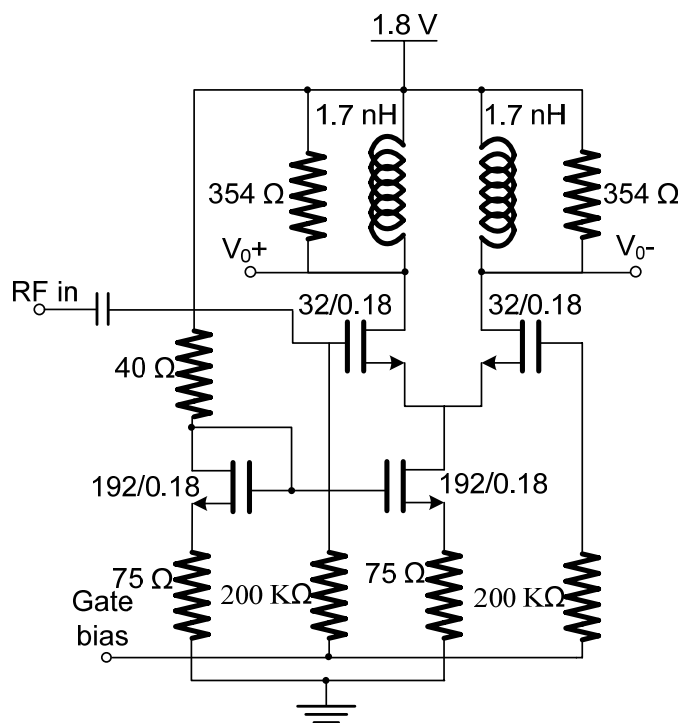
Figure 5.16 Active balun schematic with component values.

Balun not only needs to perform a perfect single-to-differential conversion, but also boost the gain of the low noise amplifier to beyond 15 dB while consuming as little power as possible. Several topologies were investigated and a simple differential pair

with resistive-inductive loads was found to be the best topology to split the input RF signal equally with a 180° phase shift. This is shown in figure 5.16. Since the distributed amplifier is designed to drive 50 Ω output load, the main RF transistors need smaller dimensions so that the gate-source capacitance at the input is low. The tradeoff involved here lies in obtaining a higher gain which requires larger transistors and at the same time allowing the DA to successfully drive the input of the balun. Another important concern is the minimization of noise figure. To take into account all these concerns, the balun RF transistors were maintained at an aspect ratio of 32/0.18. Further, in order to avoid any additional phase imbalance, the current source impedance is kept high by using very large transistors. Bias stabilization resistors are also used to accurately control the tail current at the common mode. The inductive-resistive loads serve to increase the output impedance at the drain nodes of the RF transistors thereby contributing to an increase in the overall gain. The devices are kept perfectly symmetrical and well matched during layout. Simulated performance of the balun indicates a gain of at least 8 dB with ±4° of phase imbalance up to 7 GHz while consuming a current of 10 mA from 1.8 V supply. The amplitude imbalance is ±0.95 dB. The higher gain facilitated by the balun would tend to augment the poor gain of the low noise amplifier. These results are vindicated by the boosted front end gain without significant deterioration of the linearity or noise figure. The differential power gain as well as the phase and amplitude response of the differential output of the balun are shown in figures 5.17-19.
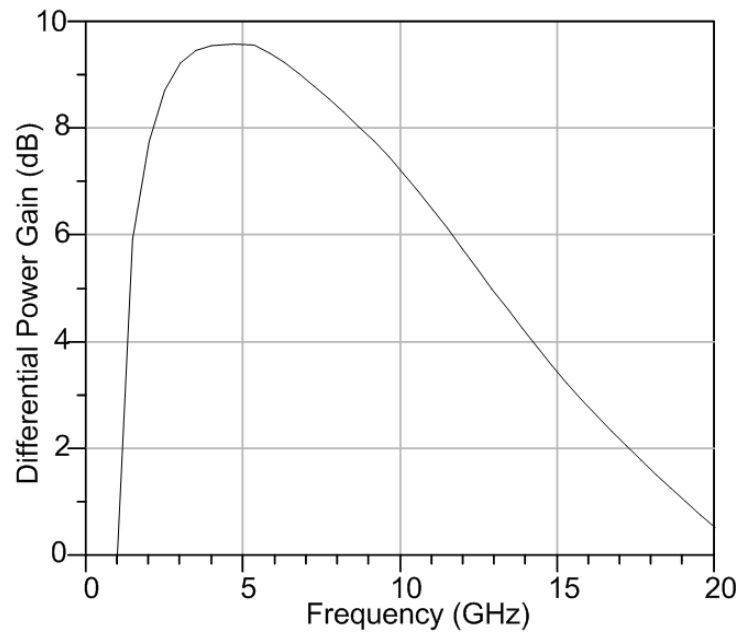
Figure 5.17 Simulated Differential power gain variation with frequency.
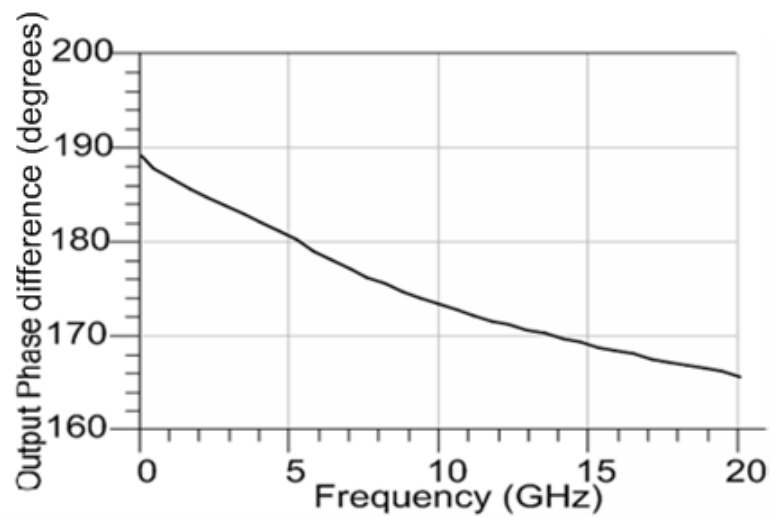
Figure 5.18 Simulated Phase difference between the two differential outputs.
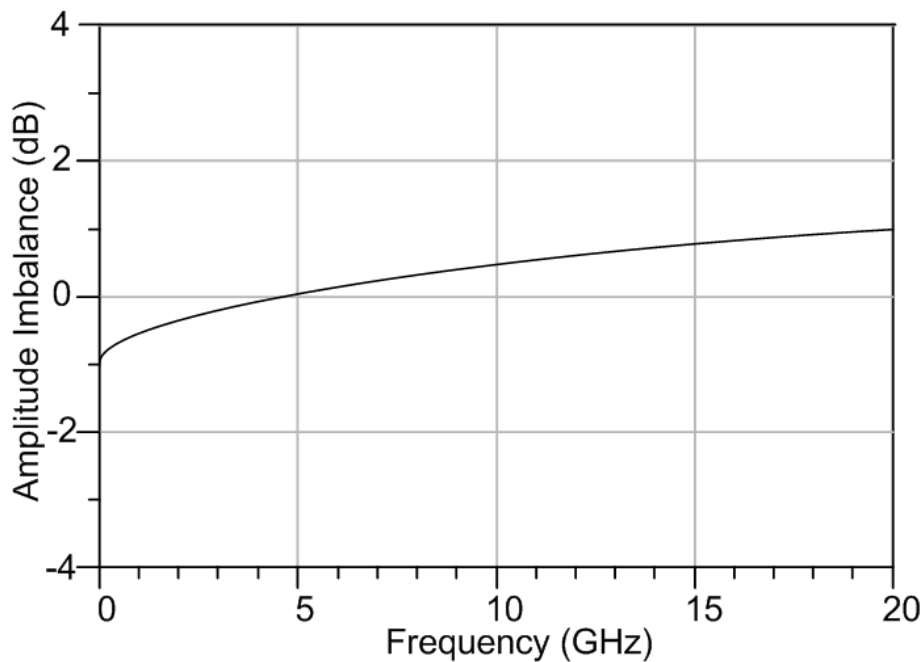
Figure 5.19 Simulated amplitude imbalance of the balun output.

5.4.3   Differential down conversion mixer

The receiver front end uses a fully differential down conversion mixer based on the Gilbert cell topology. The schematic is shown in figure 5.20. The transistors connected to the RF port act as voltage to current converters and allow the LO signal to modulate the tail current. This double balanced configuration eliminates even order distortion products and also prevents the LO signal leakage into the IF [108]. The topology is deemed suitable for a broadband operation due to the broadband frequency characteristics of the input RF transistor transconductance, which has been depicted in figure 3.2. A simple double balanced Gilbert cell topology with broadband RF matching has also been used to implement a 25-75 GHz Mixer in an earlier publication vindicating the intrinsic broad band nature of the Gilbert cell topology [109]. The linearity of the
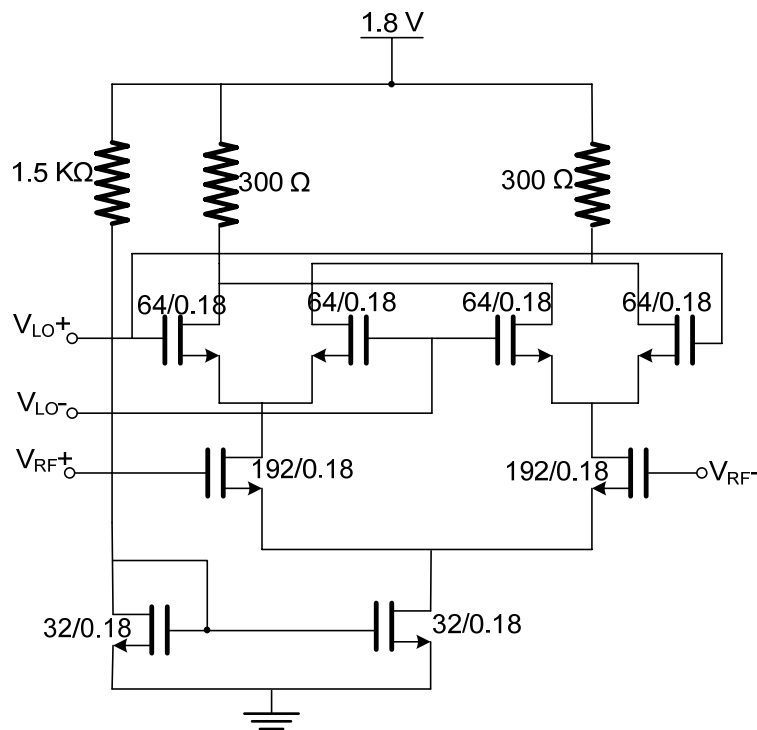
Figure 5.20 Schematic of a double balanced Gilbert cell mixer for broadband operation and component values.

traditional Gilbert cell topology could be further enhanced by resistively degenerating the source of the input RF transistors, but it further compromises the noise figure. Hence, that mechanism is not used in this design. Furthermore, to facilitate higher conversion gain, the load resistors of up to 300 Ω are used. The device component aspect ratios are fine tuned for noise and linearity requirements, as well optimized along with the load resistors for higher conversion gain. It must be noted that the designed mixer has been specifically tailored to complement the distributed low noise amplifier and balun. Therefore, it only needed to exhibit a sufficient conversion gain and moderate noise figure. As such, the simulation results indicate that the mixer shows at least 5 dB

conversion gain from 3 to 8 GHz with a noise figure of 7 dB while consuming 8 mA from 1.8 V supply. Figure 5.21 presents the simulated conversion gain and return loss of the RF port of this mixer. The mixer is difficult to measure as an individual block owing to the presence of three fully differential ports and therefore, only the integrated front end measurements are presented in the current work, that clearly confirm the logic behind opting for moderate noise figure and higher conversion gain through the mixer. Another point to be noted here is that the contour of the mixer conversion gain is perceived as flat throughout the two bands as well as the band that is supposed to be rejected. This imposes more stringent requirements on the resonant load tanks of the low noise amplifier, which are now the sole creators of the wideband rejection between 4.8-5.8 GHz.
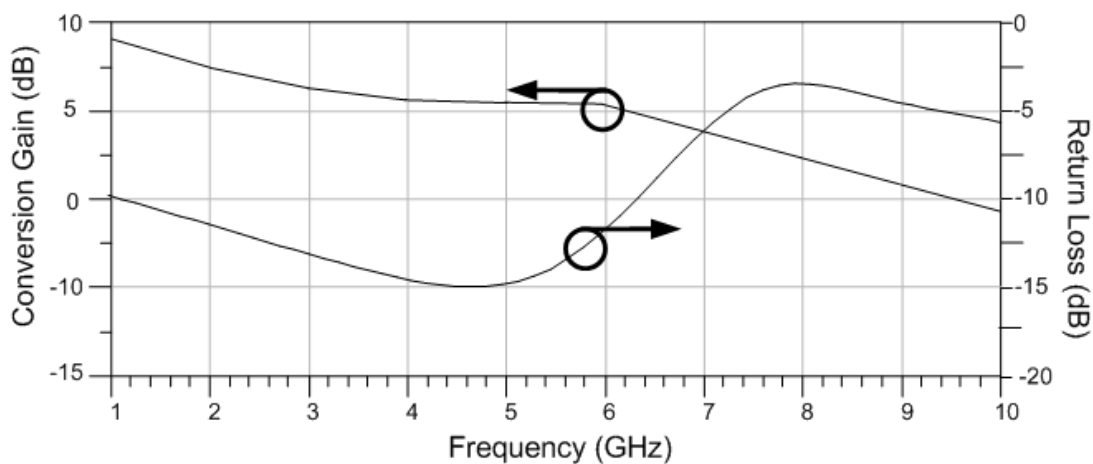
Figure 5.21 Simulated Conversion gain and return loss at the RF port of the double balanced Mixer.

5.4.4   Buffer amplifier

A buffer amplifier is another important circuit that was used to match the output impedance of the mixer to a 50 Ω load for measurement purpose. In the current case, we need the buffer to have a frequency independent and broadband response while consuming a minimal amount of power. To accomplish this, a buffer topology proposed in [110] was used, which consumed just 2 mA of current while simultaneously offering excellent broadband low impedance matching. The small difference between the current topology and the topology presented in [110] lies in the bias circuitry as shown in figure 5.22. The current source transistors are optimized to reduce their transconductance so that lower output impedance is possible. The larger RF common source transistors yield higher transconductance that control the maximum gain that could be extracted from the buffer. For matching purposes, the transistor widths are controlled such that they lead to 50 Ω output match over a broad range of frequencies. The buffer was not separately simulated for optimum performance but its parameters were jointly optimized along with the front-end and the LO port terminal of the mixer. As a result, no simulation data are available separately for the Buffer performance.

1.8 V

128/0.18 128/0.18

Rf$_{in}$ +   Rf$_{in}$ -

1.5 pF

Rf$_{out}$ +   Rf$_{out}$ -

250 Ω

1.5 pF

32/0.18   32/0.18

Gate   Gate
bias   bias

32/0.18   32/0.18

Figure 5.22 Schematic of the differential buffer with component values.

5.5 Integration issues

Several issues have to be accounted during integration, the main one being DC isolation from one stage to another. For this purpose large on-chip capacitors are used between every stage except for the output buffer which takes its bias from the previous mixer stage. The balun is multi-purpose and used both in the output of the LNA and also to convert the single ended frequency synthesizer to differential owing to the fact that the LO port of the mixer needs to be differential in operation. The buffer is also used both at the LO port of the mixer as well as for the IF port matching. The balun topology presented in section 5.4.4 was used here as it can handle broad band signals at low

impedance levels while being completely differential in operation. It is used at the LO port of the mixer as depicted earlier in the block diagram of figure 5.10. Another important issue to be considered during integration is the inductor optimization and sharing of bias points. As noted in earlier sections dealing with circuit implementation, only one set of transistors share bias from a previous stage that too in the case of the buffer amplifier. However, there are several other transistors that share common gate bias through the same voltage supply. These transistors belong to the mixer and balun blocks. An attempt was made to minimize as many different bias sources as possible through the use of resistive dividers and blocking capacitors that efficiently channel bias to the needed points. Inductor optimization was crucial during integration stage as the inductor spacing was kept at an optimal distance to avoid unwanted negative mutual coupling between two adjacent inductors. Biasing inductors were also incorporated on-chip to remove problems associated with multiple DC sources. During integration, it was also realized that the bond wire length , the length of the wire between the chip to the package pins, could severely deteriorate the performance of the LNA and in spite of repeated attempts to get those models from companies, we could not find an effective model for the package that we used for our chip. A novel way was used to solve this problem. We used an LQFP open cavity package (whose top outer casing is detachable) that allowed the RF portion to be measured with on-wafer probes on its Ground-signal-ground pads. On the other hand, the IF portion was bonded out to the package pin via bond wires and the pin was soldered to the SMA connectors through a PCB. It was
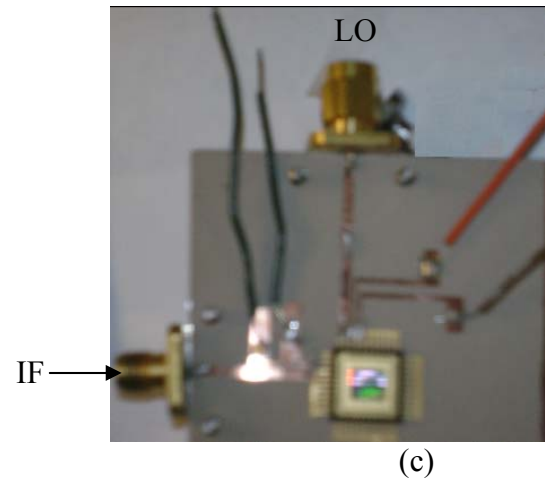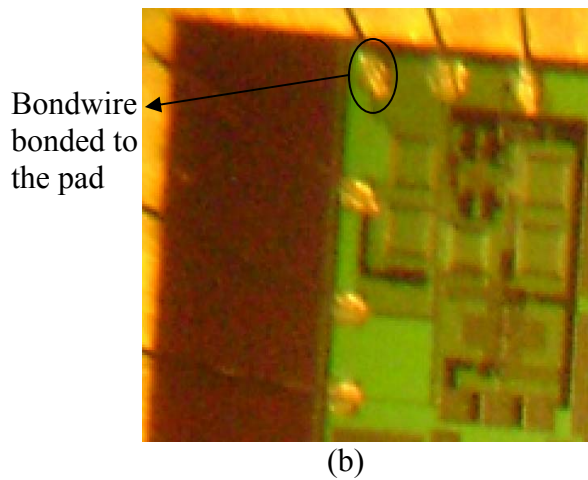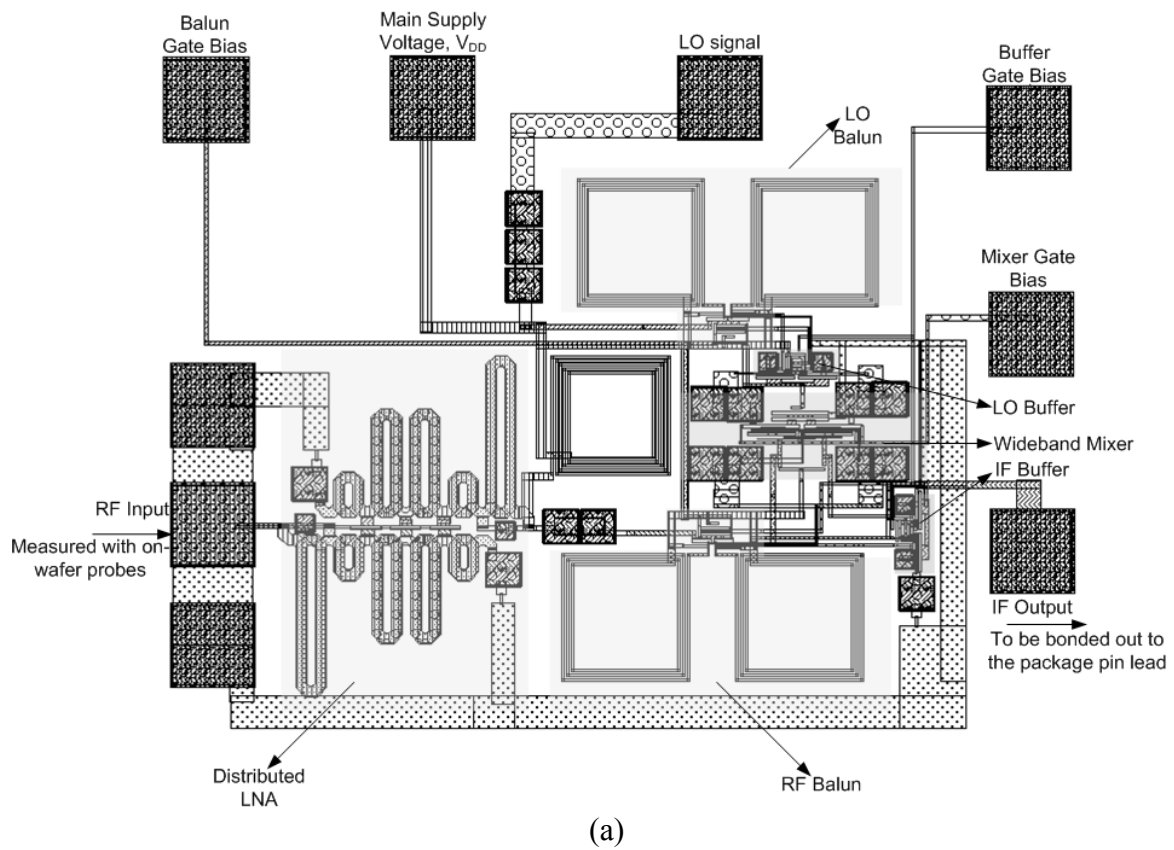
Figure 5.23 (a) Cadence Layout of the receiver front end showing different circuit blocks (b) Packaged IC showing the bond wires and (c) PCB designed for measurement of front-end.

assumed that since the IF port operates at a much lower frequency, the bond wire length

does not affect the output performance drastically.

5.6 Measurement results

The dual wideband front end was` fabricated in a standard Jazz CA18HR 0.18 μm process [65] and die attached, bonded and packaged in a 10 x 10 mm^2 LQFP open cavity plastic package. The size of the front end measured 1.18 x 0.87 mm^2 of which the dual wideband distributed amplifier occupied only 0.29 x 0.48 mm^2 or 0.13 mm^2 of chip area. Figure 5.23 shows the layout of the Duroid/RT based PCB packaged IC with the DC connections. The bond wires did not play a crucial role since care was taken such that only low frequency nodes were bonded out. The RF node was measured through on-wafer GSG probes.

The comparison between simulated and measured conversion gain is shown in figure 5.24, while the input RF matching in figure 5.25 and the noise figure is shown in figure 5.26. The conversion gain clearly shows a dual wideband output between 3-5 GHz and 6-8 GHz with at least 15 dB gain while maintaining a high return loss of up to -11.2 dB and -12.1 dB around the centers of the first and second bands respectively. The RF frequencies were chosen based on discussions in section 5.1 relating to the MB-OFDM UWB proposal. The conversion gain contour clearly shows the two bands but indicates that the stop band still has a finite gain with a 6 dB difference between stop and pass bands. However, it must be noted that the common procedure to use an active notch filter at these multi-GHz frequencies would have resulted in poor linearity due to the increased number of non-linearity causing MOS devices. Figures 5.27 and 5.28 show the
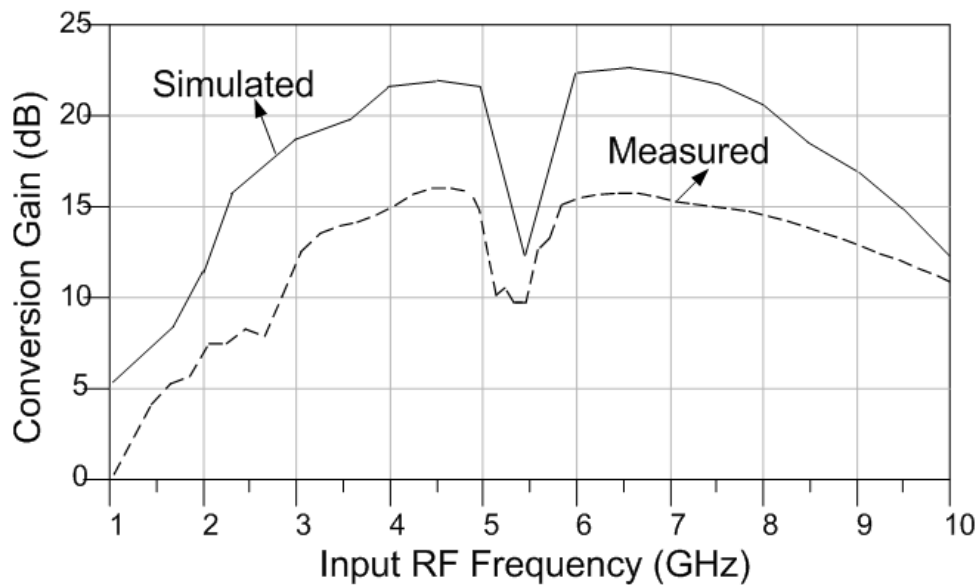
Figure 5.24 Conversion gain. LO Frequency is varied from 500 MHz to 9.5 GHz at a constant power of -10 dBm, IF = 500 MHz, RF signal power = -15 dBm.
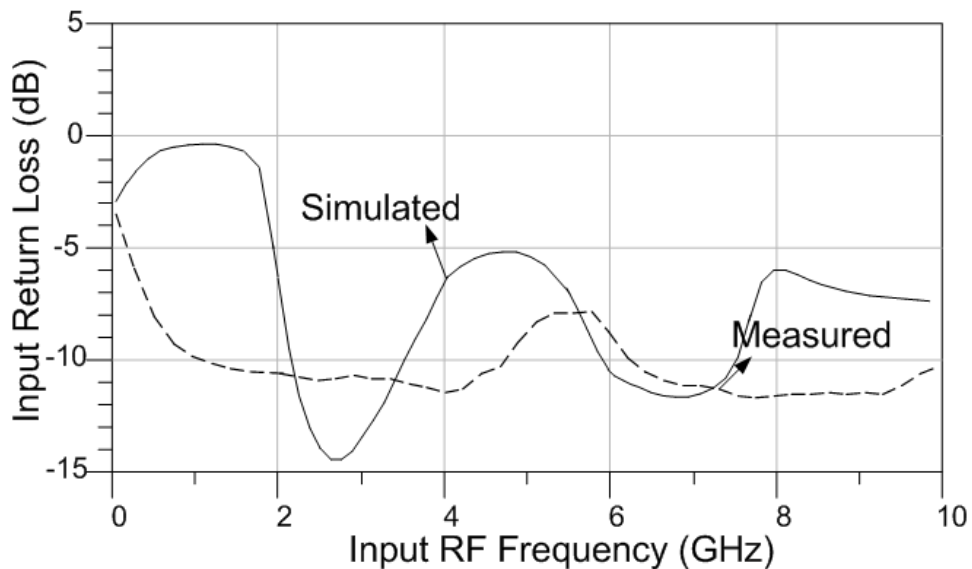
Figure 5.25 Input matching. LO frequency varied from 500 MHz to 9.5 GHz, IF =500 MHz, LO power = -10 dBm, RF power =-15 dBm.

measured 1-dB output power compression point of the front end. The values of 1-dB

compression point in the first and second band groups at 4 GHz and 6.5 GHz are -4.1
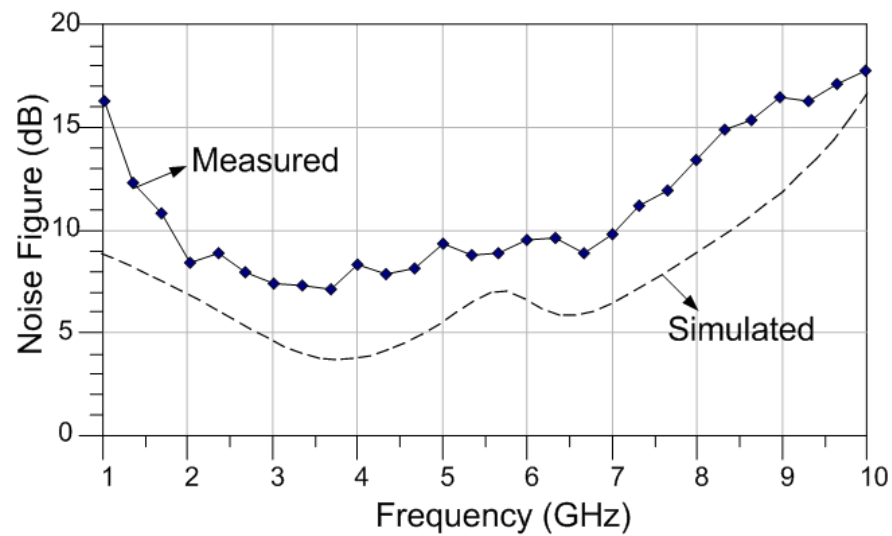
Figure 5.26 Noise Figure. LO frequency varies from 500 MHz to 9.5 GHz, LO power =-10 dBm, RF power =-15 dBm, IF = 500 MHz.
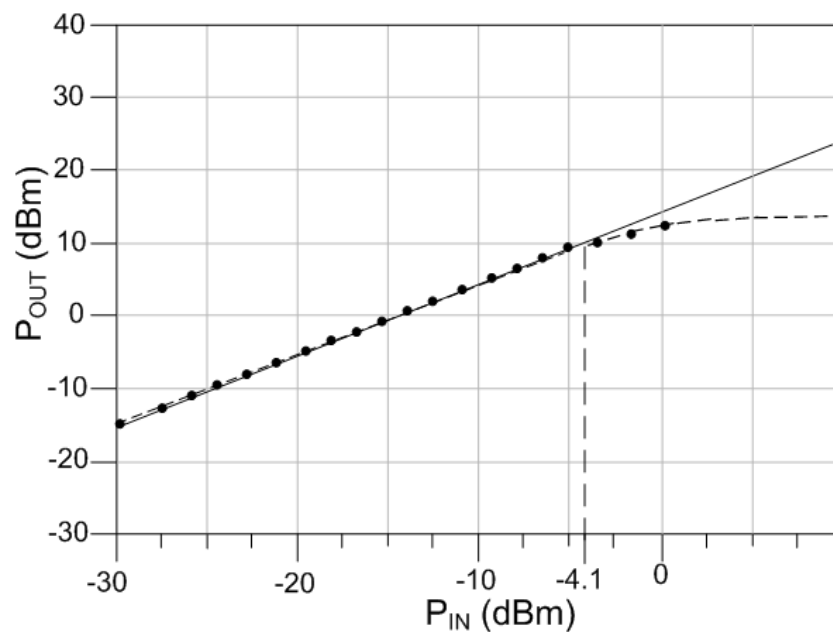
Figure 5.27 Maximum Input 1-dB compression point at 4 GHz in the first band (3.5 GHz – 5 GHz) .LO frequency is 3.5 GHz, while LO power is -10 dBm.

dBm and -5.2 dBm respectively. The LO frequencies used are from 2.5 GHz to 4.5 GHz

and 6.5 GHz to 8.5 GHz. By sweeping the LO frequency in such a manner, the IF is kept
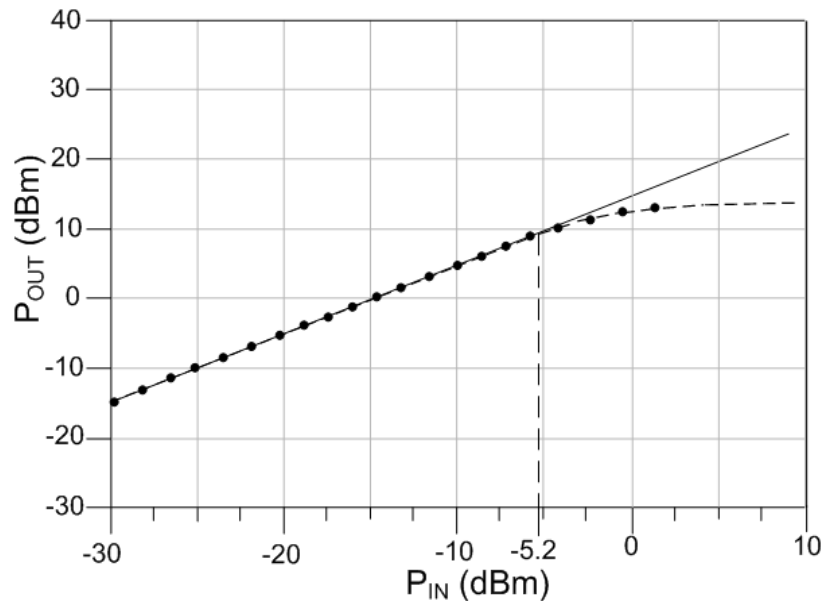
Figure 5.28 Maximum Input 1-dB compression point at 6.5 GHz in the second band (5.8 GHz to 7.8 GHz). LO frequency is 6 GHz and LO power is -10 dBm.

constant at 500 MHz. An advantage of doing such is that it results in most of the image frequencies at the edge of the bands to fall in the attenuated gap between 4 to 5 GHz. Table 5.2 shows a comparison of recently published values with the current work. Note that the conversion gain is still at least as good as the values published for a fully distributed front end in [112]. Yet, it is apparent that the conversion gain is lower than many published values based on traditional analog topologies. Furthermore the noise figure was less than 10 dB up to 7 GHz. Without the effect of the lossy IF port packages, the overall measured results of both conversion gain and noise figure could have been improved and correlated better to simulation results. The front end consumed about 42 mA of current from a 1.8 V power supply and 72% of this consumption was by the distributed LNA. It could be noted that to avoid any modeling problems with the

Table 5.2 Comparison of the receiver front end with recently published values

Reference	Technology	Frequency Range (GHz)	Conversion Gain (dB)	Noise Figure (dB)	1-dB Compression point (dBm)	Return Loss (dB)	Die Area (mm²)	Power Consumption (mW)	Type of Measurement
[111]	0.18 µm CMOS	0.925 – 0.960	12-39	2-12	-23 to -29	>12	3.5	22.5	Packaged
		2.11 – 2.17	6.5-33	4-15.9	-20 to -25	>18			
[112]	0.13 µm CMOS	3.1 – 10.6	13.8 – 15.5	5.2 – 5.4	-15.5	>10	1.5	15	On-wafer probed
[113]	0.18 µm SiGe BiCMOS	3.1 – 8.2	51-52 (entire receiver)	3.3 - 4.1	-9 to -10.2	>10	7	60	On-wafer probed
This Work	0.18 µm CMOS	3.1- 5.0	13.1 – 16.2	7.5 – 9.0	**-4.1**	> 10	**1.02**	75.6	Both on-wafer probed and packaged
		5.8 - 8	13.8 – 16.2	9.0 - 13	**-5.2**	> 10			

bond wire packages, the RF port was left unpackaged so that on-wafer probes could be used, while both the LO and IF ports were bonded out. If the RF port were also packaged, the effective performance would have been further seriously deteriorated owing to the unpredictability of the package model. In spite of the modest performance of the receiver front end, it cannot be denied that the most impressive achievement of this topology is the first complete integration of analog and microwave design concepts and the compatibility of otherwise exorbitantly bulky distributed amplifier to CMOS RFIC design.

CHAPTER VI

CONCLUSIONS

In this dissertation, an endeavor was made to implement various novel topologies of passive and active circuits for wireless applications.

6.1 Summary

At first a comprehensive literature survey of all historical implementations of IC based passive elements was provided and several existing topologies were discussed. Issues related to CMOS based passive microwave circuit design are fairly new and not much research has been done in this field till date. Hence a thorough understanding of similar issues faced by designers in GaAs might give an insight to the problems that lie ahead in the path to implementing passive elements in CMOS. Several crucial issues related to CMOS based design of passive components were identified and a wide range of passive couplers, resonators and inductors were implemented in traditional monolithic CMOS technologies that qualify as the smallest reported passive structures in any monolithic technology reported till date. Miniaturization techniques like multi-layered design and slow wave were explored to the fullest extent and a wide array of circuits were demonstrated for the first time in a standard CMOS technology. The next phase of the dissertation involving design of active circuits still stayed true to the overall theme of implementing novel circuits that were miniaturized and low power consuming. Different architectures were explored in the quest for implementing a dual wideband receiver front

end and a high-linearity distributed topology was found to be the most suitable for most of its specifications. Since size poses a critical problem in the practical utilization of distributed amplifiers, the distributed amplifier was first fully explored for possible miniaturization candidates and a multi-layered inductor based approach satisfied the size requirements of the front end. The implemented DA qualifies as the smallest distributed amplifier reported till date with over 90% size compression compared to any reported publication in GaAs or CMOS technologies. A distributed VCO was also explored for possible implementation, even though it was not part of the broader idea to implement a dual wideband front end. And finally, a receiver front end was implemented utilizing the miniaturized distributed amplifier and several other circuit components that showed excellent promise for being incorporated into multi-mode, MB-OFDM receiver systems.

6.2 Recommended future work

6.2.1 Passives

Till date, apart from the current work of the author, there have been very few publications or dissertation chapters dedicated to the design and implementation of microwave passive structures in CMOS. With the opening up of 60 GHz WLAN and 77 GHz automotive radar applications, it is expected that there would be tremendous commercial interest in seeking low cost solutions through CMOS and SiGe based technologies. At those millimeter wave frequencies, distributed design techniques need to be embraced along with traditional analog circuit design principles for efficient exploration of novel topologies. This implies that there would be a significant need for

high performance, low loss and extremely miniaturized passive circuits at those frequencies. Future work in the implementation of CMOS microwave passives should therefore be approached with an application oriented need and the requirement of extreme miniaturization. The miniaturization techniques explored in this chapter might be further explored to gain better size acceptance of microwave passives in CMOS. While multi-layered design tends to be readily amenable to any application, it could be used in conjunction with slow-wave techniques and their cumulative impact could be studied. Further more, the slow wave structures discussed in this work could be further explored for even greater miniaturization so that they could be applied to not just microwave passives but also to traditional lumped components like inductors. High self-resonant frequency (SRF) inductors could also be studied for generating higher inductances at RF frequencies since this work has only implemented high SRF in smaller inductors.

6.2.2 Distributed actives

Distributed amplifiers have been approached with a dimensional approach rather than gain approach in this work. From the beginning, the emphasis of the amplifier topologies mentioned in this work was on their potential application to meet the requirements of a dual wideband receiver sub-system. And through the course of this dissertation, extensive research work led to development of the most ultra-compact distributed amplifier ever reported. While this distributed amplifier presents itself as a viable candidate that promises high linearity, low power consumption, moderate noise figure,

excellent input and output matching, all the while occupying 90% smaller area than all previously reported structures, it suffers from poor reverse isolation and poor gain. Gain as well as reverse isolation could be enhanced by preferring a cascode structure and combining it with several other approaches mentioned by other authors. However, if the problem of poor reverse isolation still persists even with the cascode configuration, it could be attributed to the tighter mutual coupling that leaks the output signal back to the input due to the extremely small dimensions involved.

6.2.3   Dual wideband receiver sub-system

The dual wideband receiver sub-system is the first concurrent front-end reported in a 0.18 µm CMOS technology with a high linearity above 0 dBm in the RF frequencies. However, further investigations are necessary to complete their incorporation into practical MB-OFDM systems. Particularly the poor reverse isolation of the distributed LNA might prove detrimental to the suggested homodyne architecture, where LO leakage is a major concern. Additional investigation into non-distributed topologies that would yield significantly higher linearities is also an interesting challenge for front end designers.

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APPENDIX A

QUALITY FACTOR AND SELF-RESONANT FREQUENCY OF A 2-

METAL MULTILAYERED SPIRAL INDUCTOR

Quality factor of an inductor is defined in [110], [111]:

$$Q_{ind} = 2\pi . \frac{Energy\ stored}{Energy\ lost\ in\ one\ oscillation\ cycle} \qquad (A.1)$$

Or

$$Q_{ind} = 2\pi . \frac{Peak\ Magnetic\ Energy - Peak\ Electric\ Energy}{Energy\ lost\ in\ one\ cycle} \qquad (A.2)$$

There are two sources of magnetic energy from the simplified model of figure 2.35 (b). With V_0 being the peak voltage across the inductor terminals and Ip being the peak current through the inductor, an expression for Peak magnetic energy due to inductance L_{s6} and L_{s5}` (as shown in fig. 2.35 (b)) could be derived based on the expression $E_{m\_peak} = \frac{1}{2}.L.|I_P|^2$, as:

Peak magnetic energy due to inductance L_{s6} = $\frac{1}{2}.L_{s6.}\frac{V_0^2}{[R_{s6}^2 + \omega^2 L_{s6}^2]}$ $\qquad (A.3)$

Peak magnetic energy due to inductance L_{s5}` = $\frac{1}{2}.L_{s5}'\frac{V_0^2}{[\omega^2 L_{s5}'^2]} = \frac{V_0^2}{2\omega_0^2 L_{s5}'}$ $\qquad (A.4)$

where L_{s5}' is obtained by a simple series to parallel transformation of L_{s5} and is equal to

$$L_{s5}' = \frac{1}{\omega L_{s5}}\{R_{s5}^2 + (\omega L_{s5} - \frac{1}{\omega C_{s5}})^2\}.$$

The net peak magnetic energy is equal to:

$$E_{m\_peak} = \frac{V_0^2}{2} \cdot [\frac{1}{L_{s5}'} + \frac{L_{s6}}{R_{s6}^2 + \omega^2 L_{s6}^2}] \qquad (A.5)$$

Similarly, the net peak electrical energy is obtained as:

$$E_{e\_peak} = \frac{1}{2} \cdot C.V_0^2$$

=> $$E_{e\_peak} = \frac{V_0^2}{2} \cdot [C_P' + C_{ox5}] \qquad (A.6)$$

with C_P' being the series to parallel transformation of the effective non-oxide

capacitances, given by: $C_p' = \frac{1}{\omega^2 C_{i56}} \cdot \frac{1}{\{R_{s5}^2 + (\omega L_{s5} - \frac{1}{\omega C_{i56}})^2\}} + C_p$.

The energy loss per cycle of oscillation, within a period of time T, is determined by the

two resistive components, R_P' and R_s , such that:

$$E_{loss\_percycle} = \frac{1}{2} \cdot \frac{V_0^2}{R} \cdot T = \frac{1}{2} \cdot \frac{V_0^2}{R} \cdot \frac{2\pi}{\omega}$$

=> $$E_{loss\_percycle} = \frac{1}{2} \cdot V_0^2 \cdot [\frac{1}{R_P'} + \frac{R_{s6}}{R_{s6}^2 + \omega^2 L_{s6}^2}] \qquad (A.7)$$

with $R_p' = [R_{s5} + \frac{1}{R_{s5}}(\omega L_{s5} - \frac{1}{\omega C_{s5}})^2\}] \| R_p$ being a parallel transform of the series

component.

Substituting (A.5), (A.6) and (A.7) in the original definition of Q in (A.2):

$$Q = \omega \frac{\{(\frac{1}{L'_{s5}} + \frac{L_{s6}}{R_{s6}^2 + \omega^2 L_{s6}^2}) - (C'_P + C_{ox5})\}}{\frac{1}{R'_P} + \frac{R_{s6}}{R_{s6}^2 + \omega^2 L_{s6}^2}}$$

Factoring and dividing the numerator and denominator by $R_{s6}^2 + \omega^2 L_{s6}^2$,

$$Q = \frac{\omega.R'_P}{L_{s5}} \cdot [\frac{\{R_{s6}^2 + \omega^2 L_{s6}^2\}\{1 - (C_P + C_{ox5})L_{s5}\} + L_{s6}L'_{s5}}{R_{s6}^2 + \omega^2 L_{s6}^2 + R_{s6}R'_P}]$$

Further factoring and separating into meaningful terms yields:

$$Q = \frac{\omega L'_{s5}L_{s6}}{R_{s6}} \cdot \frac{R'_p}{L'_{s5}[R'_p + \{1 + (\frac{\omega L_{s6}}{R_{s6}})^2\}R_{s6}]} \cdot [1 + \frac{(R_{s6}^2 + \omega^2 L_{s6}^2)}{L'_{s5}L_{s6}}\{1 - L'_{s5}(C_{ox5} + C'_p)\}]$$

(A.8)

An expression for the inductor self-resonant frequency is derived from (A.8) by equating

Q to 0.

$$\Rightarrow [1 + \frac{(R_{s6}^2 + \omega_0^2 L_{s6}^2)}{L'_{s5}L_{s6}}\{1 - L'_{s5}(C_{ox5} + C'_p)\}] = 0$$

Solving for ω_0, we obtain the self resonant frequency expression as:

$$\omega_0 = \sqrt{\frac{L'_{s6}}{L_{s6}} \cdot \frac{1}{\{L'_{s5}(C_{OX5} + C'_p) - 1\}} \cdot [1 - \frac{R_{s5}^2}{L'_{s5}L_{s6}}\{L'_{s6}(C_{OX5} + C'_p) - 1\}]}$$

APPENDIX B

NUMBER OF STAGES IN DISTRIBUTED VCO

Consider the oscillation condition for a distributed VCO with equivalent impedance presented to the gate and drain segments as Z_{imp}, the large signal Transistor gain G_m, drain and gate propagation constants γ_d and γ_g, the number of stages n and unit gate length l_g, drain length l_d from [91] :

$$G_m.Z_{imp}.e^{-(\gamma_d l_d + \gamma_g l_g)/2.}\cdot\frac{e^{-\gamma_d n l_d} - e^{-\gamma_g n l_g}}{e^{-\gamma_d l_d} - e^{-\gamma_g l_g}} = -1 \qquad (B.1)$$

In the case of equal drain and gate segment lengths, (B.1) is rewritten as [91]:

$$G_m.Z_{imp}.n.e^{-(n.\gamma.l)} = -1 \qquad (B.2)$$

To solve for n, we can assume $G_m.Z_{imp}$ as X:

$$n.e^{-(n.\gamma.l)} = -\frac{1}{X} \qquad (B.3)$$

Approximating $e^{-\theta}$ as $(1- \theta/2)$ which is valid in the current case as θ is very small and ignoring higher order terms:

$$n.[1-\frac{n.\gamma.l}{2}] = -\frac{1}{X} \qquad (B.4)$$

Solving for n, by taking quadratic roots, we obtain:

$$n = \frac{1 + \mathrm{mod}(\sqrt{1 + 2\gamma.l.X})}{\gamma.l} \qquad (B.5)$$

Making a reasonable assumption that the negative solution is not practically relevant and

expanding the square root term and considering only the real values:

$$n = \mathrm{mod}[\frac{2}{\gamma.l} + \frac{1}{G_m.Z_{imp}}] \qquad (B.6)$$

VITA

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