

A FULLY INTEGRATED MULTI-BAND MULTI-OUTPUT SYNTHESIZER WITH
WIDE-LOCKING-RANGE 1/3 INJECTION LOCKED DIVIDER UTILIZING
SELF-INJECTION TECHNIQUE FOR MULTI-BAND MICROWAVE SYSTEMS

A Dissertation

by

SANG HUN LEE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2012

Major Subject: Electrical Engineering

A FULLY INTEGRATED MULTI-BAND MULTI-OUTPUT SYNTHESIZER WITH
WIDE-LOCKING-RANGE 1/3 INJECTION LOCKED DIVIDER UTILIZING
SELF-INJECTION TECHNIQUE FOR MULTI-BAND MICROWAVE SYSTEMS

A Dissertation

by

SANG HUN LEE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Approved by:

Chair of Committee,	Cam Nguyen
Committee Members,	Aydin Karsilayan
	Laszlo Kish
	Binayak Mohanty
Head of Department,	Costas N. Georghiadis

August 2012

Major Subject: Electrical Engineering

ABSTRACT

A Fully Integrated Multi-Band Multi-Output Synthesizer with Wide-Locking-Range 1/3 Injection Locked Divider Utilizing Self-Injection Technique for Multi-Band Microwave Systems. (August 2012)

Sang Hun Lee, B.S., Kwangwoon University, Korea;

M.S., Kwangwoon University

Chair of Advisory Committee: Dr. Cam Nguyen

This dissertation reports the development of a new multi-band multi-output synthesizer, 1/2 dual-injection locked divider, 1/3 injection-locked divider with phase-tuning, and 1/3 injection-locked divider with self-injection using 0.18- μm CMOS technology. The synthesizer is used for a multi-band multi-polarization radar system operating in the K- and Ka-band.

The synthesizer is a fully integrated concurrent tri-band, tri-output phase-locked loop (PLL) with divide-by-3 injection locked frequency divider (ILFD). A new locking mechanism for the ILFD based on the gain control of the feedback amplifier is utilized to enable tunable and enhanced locking range which facilitates the attainment of stable locking states. The PLL has three concurrent multiband outputs: 3.47-4.313 GHz, 6.94-8.626 GHz and 19.44-21.42-GHz. High second-order harmonic suppression of 62.2 dBc is achieved without using a filter through optimization of the balance between the differential outputs. The proposed technique enables the use of an integer-N architecture

for multi-band and microwave systems, while maintaining the benefit of the integer-N architecture; an optimal performance in area and power consumption.

The 1/2 dual-ILFD with wide locking range and low-power consumption is analyzed and designed together with a divide-by-2 current mode logic (CML) divider. The 1/2 dual-ILFD enhances the locking range with low-power consumption through optimized load quality factor (Q_L) and output current amplitude (i_{osc}) simultaneously. The 1/2 dual-ILFD achieves a locking range of 692 MHz between 7.512 and 8.204 GHz. The new 1/2 dual-ILFD is especially attractive for microwave phase-locked loops and frequency synthesizers requiring low power and wide locking range.

The 3.5-GHz divide-by-3 (1/3) ILFD consists of an internal 10.5-GHz Voltage Controlled Oscillator (VCO) functioning as an injection source, 1/3 ILFD core, and output inverter buffer. A phase tuner implemented on an asymmetric inductor is proposed to increase the locking range.

The other divide-by-3 ILFD utilizes self-injection technique. The self-injection technique substantially enhances the locking range and phase noise, and reduces the minimum power of the injection signal needed for the 1/3 ILFD. The locking range is increased by 47.8 % and the phase noise is reduced by 14.77 dBc/Hz at 1-MHz offset.

DEDICATION

To my aunt, my brothers and sisters, and my lovely wife and son

ACKNOWLEDGEMENTS

I would like to express my sincere gratitude to my doctoral advisor, Prof. Cam Nguyen, for his guidance, support, and encouragement throughout my research at Texas A&M University. His instructions are very valuable to my effort of developing the RF Synthesizer using injection locking for multiband microwave and millimeter-wave communication and radar systems. He believed in me from the beginning of the effort, and has been a constant source of encouragement throughout its duration. I thank to my committee members, Dr. Karsilayan, Dr. Kish, Dr. Mohanty, for their time and valuable suggestions. I also gained much from their course on broadband RF systems and low noise circuitry. The work presented in this dissertation could not have happened without helps and supports from many people.

I would like to thank my parents and my elder brother for their love, support and encouragement during these many years in the graduate school. Finally, I would like to express my love and gratitude to my beloved wife, Hyoeun Kim, son, Daniel Danhee Lee for the endless care and happiness brought throughout my degree studies.

This work was supported in part by the U.S Air Force Office of Science Research and in part by the U.S. National Institute of Justice.

TABLE OF CONTENTS

	Page
ABSTRACT	iii
DEDICATION	v
ACKNOWLEDGEMENTS	vi
TABLE OF CONTENTS	vii
LIST OF FIGURES	x
LIST OF TABLES	xvi
CHAPTER	
I INTRODUCTION	1
II BACKGROUND	6
1. Principles of Phase-Locked Loop	6
A. Phase/Frequency Detector	7
B. Charge Pump and Loop Filter	10
C. Voltage Controlled Oscillator	12
D. Linear Model of PLL	12
E. Frequency Divider	16
2. Conclusions	20
III LOW POWER WIDE-LOCKING-RANGE DUAL-INJECTION	
LOCKED 1/2 DIVIDER	21
1. Introduction	21
2. Divide-by-2 Divider using Single-Injection	26
3. Proposed Divide-by-2 using Dual-Injection	29
A. The Proposed Concept of Dual-Injection	29
B. Design of Proposed Divide-by-2 Dual-ILFD	35
4. Measured Results	40
5. Conclusion	49

CHAPTER	Page	
IV	A FULLY INTEGRATED 0.18- μm BiCMOS DIVIDE-BY-3 INJECTION-LOCKED FREQUENCY DIVIDER IMPLEMENTING PHASE TUNING TECHNIQUE	50
	1. Introduction	50
	2. Circuit Design and Analysis.....	52
	3. Measurement Results	58
	4. Conclusion	64
V	NEW DIVIDE-BY-3 INJECTION LOCKED FREQUENCY DIVIDER UTILIZING SELF-INJECTION TECHNIQUE	65
	1. Introduction	65
	2. Circuit Design and Analysis.....	67
	3. Phase Noise Analysis of ILFD	70
	4. Measurement Results	71
	5. Conclusion	80
VI	A FULLY INTEGRATED MULTI-OUTPUT SYNTHESIZER FOR MULTI-BAND MICROWAVE SYSTEMS	81
	1. Introduction	81
	2. Limitations of Conventional Calibration Techniques for Super-Harmonic-ILFD PLL	84
	3. Proposed Architecture and Calibration Mechanism for Super-Harmonic-ILFD PLL.....	87
	4. Sub-Blocks of Triple-Band PLL	90
	A. 10.5/21 GHz VCO and 21 GHz Buffer	93
	B. 1/3 ILFD	96
	C. The Proposed Mode-Converter and Minimized Mismatch Gain/Phase for Differential Outputs.....	99
	D. 1/2 CML Divider, 1/16 Prescaler, PFD, CP, and LF.....	101
	E. Latched 8-bit Decoder for Digital Control	102
	5. Results	103
	6. Conclusion	111

CHAPTER	Page
VII SUMMARY AND CONCLUSIONS	112
REFERENCES	115
VITA	121

LIST OF FIGURES

FIGURE	Page
Fig. 1.1 Block diagram of a PLL	2
Fig. 2.1 PLL as a negative feedback system	6
Fig. 2.2 Transfer function of PFD	8
Fig. 2.3 Block diagram of PFD using sequential method of 3 states: (a) schematic, (b) state machine	8
Fig. 2.4 The output signal of PFD using 3-state sequential method	9
Fig. 2.5 The transfer function of PFD in dead zone	9
Fig. 2.6 Block diagram of PFD with gate delayed using inverters	10
Fig. 2.7 Schematic of the charge pump (CP) with loop filter (LF)	11
Fig. 2.8 Linear model of the PLL in Fig. 2.1	13
Fig. 2.9 Modified loop filter (LF) for stabilization with R_p	14
Fig. 2.10 Transfer function and phase margin of a linear PLL model (a) without R_p and (b) with R_p	15
Fig. 2.11 CML frequency divider for 1/2 division: (a) block diagram using flip-flop, (b) schematic of each latch	17
Fig. 2.12 Schematic of ILFD [24], [31]	19
Fig. 2.13 Operation of ILFD: (a) phasor interpretation between ω_o and ω_i . Z_{11} is the input impedance of the resonator, (b) phasor diagram between i_{OSC} and i_{INJ}	19
Fig. 3.1 A conventional DILFD with single injection at NMOS: (a) schematic, (b) equivalent model using mixer, BPF, multiplier N, and (c) phasor diagram between i_{OSC} and i_{INJ}	23

FIGURE	Page
Fig. 3.2 Conventional 1/2 super-harmonic DILFD using single-injection: (a) circuit schematic, (b) output of divider (upper) with injection, V_{INJ} (lower), and (c) phasor interpretation between ω_0 and ω_i . Z_{11} is the input impedance of the resonator	26
Fig. 3.3 Behavioral model of the proposed 1/2 dual-ILFD	27
Fig. 3.4 Schematic of the proposed 1/2 dual-ILFD. A 1/2 CML frequency divider is integrated with the dual-ILFD and used to compensate for the output voltage variation. The injection signal is via either a balun or divider.....	28
Fig. 3.5 Equivalent circuit of resonator with external load R_L	30
Fig. 3.6 Phasor diagram for (a) single-injection vs. single-injection with reduced i_{OSC} and hence reduced Q_L , (b) single-injection vs. dual-injection, (c) dual-injection with and without reducing i_{OSC} (equivalent to with and without optimized Q_L), and (d) proposed dual injection vs. other dual injection.....	33
Fig. 3.7 Simulation results of 1/2 dual ILFD: current and g_m of M_1	37
Fig. 3.8 Output amplitude of 1/2 dual-ILFD versus VDD	37
Fig. 3.9 Locking range characteristics of the proposed 1/2 dual-ILFD versus injection voltage for different settings	39
Fig. 3.10 Die photograph of the 1/2 dual-ILFD. Size: 0.8mm^2 (with pads), 0.156mm^2 (without pads). $V_{INJ,1}$ is connected to either a balun or a divider	40
Fig. 3.11 Microphotograph of the designed 1/2 dual-ILFD (a) packaged chip mounted on FR-4 PCB (b).	41
Fig. 3.12 Measured kVCO and output power without injection	42
Fig. 3.13 Measured output spectrum of (a) the free-running 1/2 dual-ILFD and (b) the locked 1/2 dual-ILFD.....	43
Fig. 3.14 Measured phase noise of the locked 1/2 dual-ILFD	44

FIGURE	Page
Fig. 3.15 Measured phase noise of the unlocked 1/2 dual-ILFD	45
Fig. 3.16 Measured phase noise of the locked 1/2 dual-ILFD	45
Fig. 3.17 Measured phase noise of the locked 1/2 dual-ILFD	46
Fig. 3.18 Measured phase noise of 7 GHz external source	46
Fig. 3.19 Measured locking range with single-injection and dual-injection for 1/2 function.....	47
Fig. 4.1 (a) Block diagram model and (b) circuit schematic of the integrated divide-by-3 ILFD	51
Fig. 4.2 (a) Phase tuner and (b) its equivalent model.....	54
Fig. 4.3 Phase diagram between currents in the integrated ILFD	57
Fig. 4.4 Phase of the 2 nd and 4 th harmonic	57
Fig. 4.5 Integrated ILFD with constituent components	59
Fig. 4.6 Die photograph of the integrated 1/3 ILFD. Size: 2mm ² (with pads), 0.42mm ² (without pads) for 1/3 ILFD chain, 0.25mm ² (without pads) for 1/3 ILFD core.....	59
Fig. 4.7 Measured free-running frequency tuning range of the integrated 1/3 ILFD with 5-bit digital control.....	61
Fig. 4.8 Measured output spectrum in locked and unlocked states.....	61
Fig. 4.9 Measured locking range for different phase tuning.....	62
Fig. 4.10 Microphotograph of the designed 1/3 ILFD (a) packaged chip mounted on FR-4 PCB (b).	63
Fig. 5.1 Block diagram of the proposed divide-by-3 ILFD	66
Fig. 5.2 The schematic of the proposed divide-by-3 ILFD.....	67
Fig. 5.3 Die photograph of the proposed 1/3 ILFD chain with gain-boosted amplifier.....	72

FIGURE	Page
Fig. 5.4 Measured frequency tuning range vs. varactor control voltage for different capacitor arrays as noted in the digital codes.....	73
Fig. 5.5 Measured locking range vs. control voltage VDD of feedback amplifier under fixed capacitor array at 00110	73
Fig. 5.6 Measured locking range for fixed capacitor array at setting 00110.....	74
Fig. 5.7 Measured phase noise under fixed capacitor array at 00110	74
Fig. 5.8 Measured phase noise with feedback amplifier ON at 1.8-V control voltage for fixed capacitor array at 00110.	75
Fig. 5.9 Measured phase noise with feedback amplifier OFF at 1.8-V control voltage for fixed capacitor array at 00110	76
Fig. 5.10 Measured phase noise with feedback amplifier ON at 1.8-V control voltage for fixed capacitor array at 00110	77
Fig. 5.11 Measured phase noise with feedback amplifier OFF at 1.8-V control voltage for fixed capacitor array at 00110	77
Fig. 5.12 Measured phase noise of the external 12.247 GHz injection source	78
Fig. 5.13 Microphotograph of the designed 1/3 ILFD (a) packaged chip mounted on FR-4 PCB (b).	79
Fig. 6.1 Block diagram of PLL with conventional super-harmonic ILFD and calibration scheme for VCO frequency at coarse-locking.....	84
Fig. 6.2 Timing diagram of the frequency comparison techniques in ILFD PLL.....	86
Fig. 6.3 Block diagram of the proposed ILFD PLL and calibration scheme for VCO frequency at coarse-locking	88
Fig. 6.4 Block diagram of the multi-output PLL integrating all, except the reference clock, on a single chip	89
Fig. 6.5 Schematic of the 10.5/21-GHz push-push VCO and 21-GHz buffer...	91

FIGURE	Page
Fig. 6.6 Simulated output spectrum of the VCO at 10.5-GHz output (a) and 21-GHz output (b) ports	92
Fig. 6.7 Simulated phase noise of the VCO at 10.5-GHz output (a) and 21-GHz output (b) ports	94
Fig. 6.8 Schematic of the 1/3 ILFD.....	95
Fig. 6.9 Capacitance and quality factor of the 2nd harmonic at node P	96
Fig. 6.10 Simulated output power at node P	96
Fig. 6.11 Simulated output spectrum of the 1/3 ILFD at 3.5-GHz (a) and 7-GHz (b) output port.....	97
Fig. 6.12 The equivalent model of asymmetric inductor	99
Fig. 6.13 PFD, CP and 3rd-order LF	101
Fig. 6.14 Block diagram of the 8-bit decoder for digital control pins.....	102
Fig. 6.15 Die photograph of the fully integrated PLL. Size: 1.786mm ² with pads	105
Fig. 6.16 Measured frequency tuning range of the PLL at the 3.5-GHz output port with 5-bit digital control	105
Fig. 6.17 Measured frequency tuning range of the PLL around the 10.5-GHz signal with 5-bit digital control	106
Fig. 6.18 Measured output spectrum of the PLL at the 3.5 GHz output port. RBW: 100 kHz, VBW: 30 kHz, SPAN: 0.4 GHz, REF: -10 dBm, and ATT: 0, 45.55 dBc at 109.375 MHz, 65.95 dBc at 87 MHz, and 48.9 dBc at 150 MHz.....	106
Fig. 6.19 Measured output spectrum of the PLL at the 3.5 GHz output port. RBW: 100 kHz, VBW: 30 kHz, SPAN: 9 GHz, REF: -10 dBm, and ATT: 0, 2nd harmonic rejection: 62.2 dBc, reference signal rejection: -45.55 dBc.....	107
Fig. 6.20 Measured phase noise under fixed capacitor array at 00110	107

FIGURE	Page
Fig. 6.21 Measured phase noise of the PLL	108
Fig. 6.22 Measured output spectrum of the PLL at the 7- GHz port. RBW: 100 kHz, VBW: 30 kHz, SPAN: 10 MHz, REF: -10 dBm, and ATT: 0	108
Fig. 6.23 Measured output spectrum of the PLL at the 21-GHz port. RBW: 3 MHz, VBW: 1 MHz, SPAN: 19.25 GHz, REF: 0 dBm, and ATT: 0	109
Fig. 6.24 Microphotograph of the designed ILFD PLL (a) packaged chip mounted on FR-4 PCB (b).	110

LIST OF TABLES

TABLE	Page
2.1 Comparison between divider types	16
3.1 Comparison of measurement results between proposed ILFD and others	48
6.1 Simulated results of harmonic suppression of the proposed ILFD	98
6.2 Comparison of measurement results between proposed ILFD PLL and others	109

CHAPTER I

INTRODUCTION

Phase-locked loops (PLLs) have been introduced for synchronization of horizontal and vertical scans of television in early 1940s. It has become one of the most essential components in many electronic systems including televisions, radios, computers and communication systems, etc. PLL uses a control mechanism to reduce the phase error between the reference signal and the oscillator output while the loop is in a locked state. In early days, PLL was used in control systems such as motor speed control and so on and numerous research works have been conducted to improve the performance of PLL for the systems under high-noise environment. With the rapid development of radio communication systems since 1970s, PLLs have served important roles such as FM demodulation, synchronization, and frequency synthesis in the communication systems. Unlike the control systems, the communication systems are very susceptible to any noise sources since they determine the system fidelity and hence the quality of communications. Therefore, the spectral purity of the desired signal is one of the main concerns in building communication systems.

In communication systems, clean and stable periodic signal sources should be available for various functions such as signal transmission, generating a clock signal, calibrating a sampling clock, providing local oscillator (LO) signals, etc. PLL as a

frequency synthesizer can perform these functions inside systems. With the advances in semiconductor technology and IC fabrication process over the past few decades, people have been striving to integrate a frequency synthesizer together with whole transceiver subsystem on a single chip for cost-effectiveness and size reduction of the system. However, a major problem of an integrated PLL is the noise from the power supply, which is directly converted to phase noise at PLL. The noise from a power supply can enter a PLL directly via physical connections which can be reduced significantly by different design techniques like differential circuit implementation. The noise from a power supply and other nearby circuits can also arrive at the PLL through substrates, particularly the conductive Si substrate; this noise is difficult to reduce [1]-[4]. In order to improve power supply noise and common-mode noise rejection characteristics, the differential structure is commonly utilized for on-chip frequency synthesizer design [5]-[8].

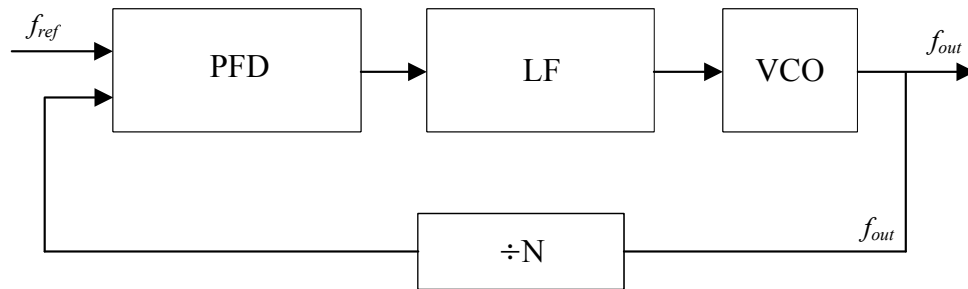


Fig. 1.1. Block diagram of a PLL

Figure 1.1 shows a conventional PLL structure working as a frequency synthesizer. The voltage-controlled oscillator (VCO) output signal is divided and its frequency f_{out} and phase are compared with those of a clean reference signal (at f_{ref}) in a phase-frequency detector (PFD). Any misalignment in the frequency and phase between the two signals will be converted to voltage at the output of the PFD, which is filtered by the loop filter (LF). The output voltage of the LF tunes the VCO's free-running frequency until a perfect alignment of frequency and phase between the two signals occurs.

For proper phase and frequency locking, which is the main objective of PLL, a frequency divider denoted by $\div N$ in Fig.1.1 must be able to provide the same frequency as the reference frequency to the PFD. Frequency division can be performed in either analog or digital domains. Analog frequency dividers are usually used at high frequencies while digital frequency dividers are at relatively low frequencies for reduced power consumption.

Therefore, in microwave and, especially, millimeter-wave applications, analog type is preferred as an initial stage of the frequency division and then digital type of the frequency division follows. Among different types of frequency dividers, injection-locked frequency divider (ILFD) is getting more attention for its low power and high frequency operation [9]-[12]. However, ILFD typically suffers from narrow locking range over which a frequency division can be supported. In fully integrated PLL system, an internal VCO is used to supply the injection signal with limited output power, which

directly leads to the limited locking range. Therefore, a new ILFD design is necessary to overcome the limitation on locking range under relatively small injection power.

Conventional PLL is usually designed to produce a single frequency output at VCO, which is used as the LO signal for up/down conversion in carrier-based communication systems. However, there may be a need for systems supporting multiple frequency bands such as multi-band sensing applications. In that case, more than a single-frequency output should be available and hence PLL must be able to synthesize all frequencies required for multi-band systems. Typically, multiple VCOs are used to create multiple frequency outputs. However, it is challenging or may not be feasible to complete such systems at high frequencies under small DC power constraints. In order to overcome the difficulty, a push-push VCO structure, formed by combining two balanced outputs, is very attractive for generating multiple frequency outputs without consuming additional DC power. It can simultaneously generate both low and high frequencies with low speed (f_{max}) transistors [13]-[16].

As introduced above, multi-band communication systems working “concurrently” over multiple bands provide significant advantages and have more capabilities compared to their single-band counterparts. Concurrent multiband systems allow communication and/or sensing to be performed at multiple frequencies simultaneously. To support these systems, concurrent multiband multi-output PLLs are needed, particularly, fully integrated CMOS/BiCMOS PLL’s for complete systems on chips. The challenges for obtaining concurrent multiband multi-output in microwave CMOS PLLs using ILFD are the primary motivation of this research.

A new CMOS multiband multi-output PLL and three new ILFDs for microwave applications are proposed. Particularly, the multi-band PLL is based on the ILFD with feedback amplifier to enhance the locking range. It demonstrates an improvement in the locking range with low power and good phase noise characteristics.

The dissertation is organized into six chapters. Chapter II presents the background of PLL. Chapter III presents a rigorous analysis on the locking range of a dual-ILFD under the influence of dc-bias as well as injection signal. Chapter IV presents a wide locking range $1/3$ ILFD design based on a new phase-tuning technique to improve the locking range. Chapter V presents a $1/3$ ILFD design based on the self-injection technique. Chapter VI presents the concurrent multiband multi-output PLL utilizing the self-injection technique discussed in chapter V. Chapter VII draws the conclusions and provides the final remarks.

CHAPTER II
BACKGROUND

1. Principles of Phase-Locked Loop

Conventional PLL is composed of the reference clock (f_{ref}), phase frequency detector (PFD), charge pump (CP), loop filter (LF), and frequency divider (FD) as shown in Fig. 2.1. PFD determines the phase and frequency difference between the reference signal (f_{ref}) and feedback signal (f_{fb}) which is a divided-by-N version of f_{out} , and generates an error signal representing the phase/frequency difference. The output signal of the PFD is converted into current by the CP, which is low-pass filtered and converted into a control voltage (V_{cont}) by the LF. Then, the output frequency of the

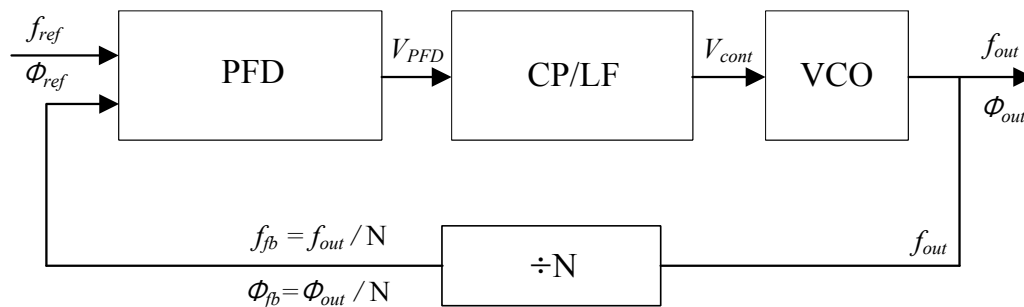


Fig. 2.1. PLL as a negative feedback system.

VCO (f_{out}) is tuned by V_{cont} and divided by a factor of N to be compared with f_{ref} at the PFD. This procedure continues in a closed loop fashion until $f_{out} = N \cdot f_{ref}$. This is done in two steps. In the first step, the frequency difference between f_{ref} and f_{fb} is compared and adjusted until it becomes very small. In the second step, the phase error between the signals at f_{ref} and f_{fb} (i.e., $\Phi_{ref} - \Phi_{out}/N$) is compared and adjusted until it is a constant, and hence the derivative of the phase error is zero, meaning that f_{out} is equal to $N \cdot f_{ref}$.

A. Phase/Frequency Detector

PFD produces an output signal having voltage proportional to the phase difference and frequency difference between the reference signal (f_{ref}) and the output signal of the frequency divider (f_{fb}). The transfer function of the PFD is shown in Fig. 2.2, where $\Delta\Phi$ is the phase difference between the signals at f_{ref} and f_{fb} , which shows the phase dependence. Similar dependence is obtained for the frequency difference. The response manifests that the PFD has a (periodic) linear phase range within $\pm 2\pi$. When the PLL is in locked state (i.e., the output frequency f_{out} is (ideally) equal to the desired frequency), the phase difference between f_{ref} and f_{fb} is normally very small and hence well within the PFD's linear operating region. Therefore, in the locked mode, the PFD is considered as a linear device. A PFD usually employs a memory device [17]-[18] such as flip flop and latch as shown in Fig. 2.3(a). The PFD state transitions and the events that cause these state transitions can be described using the state machine as shown in Fig. 2.3(b), where $V\uparrow$ is a rising edge event of f_{fb} and $R\uparrow$ is a rising edge event of f_{ref} . Each state of the PFD (state1, state2, and state2) yields a corresponding PFD output

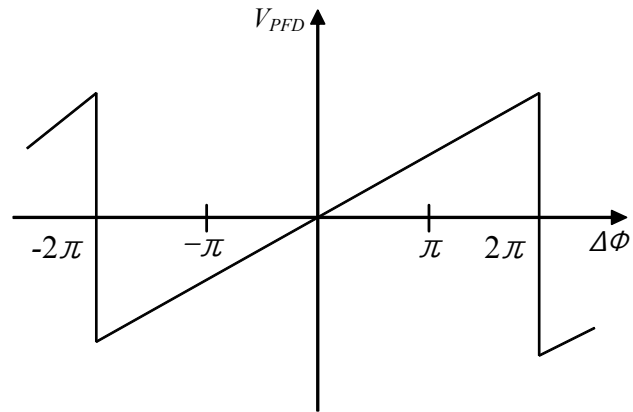
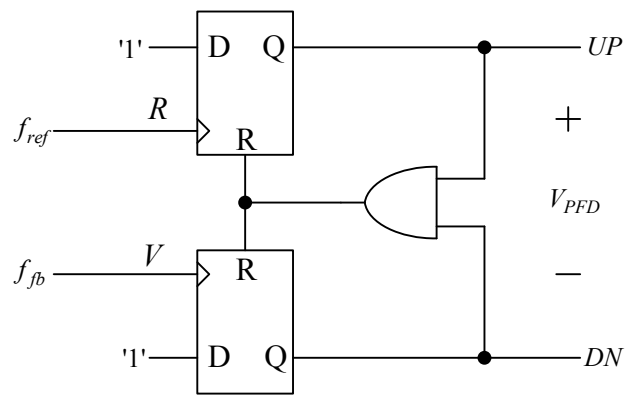
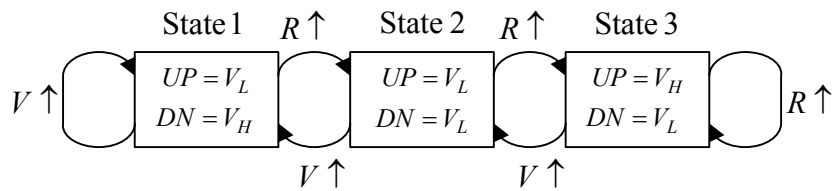


Fig. 2.2 Transfer function of PFD.



(a)



(b)

Fig. 2.3. Block diagram of PFD using sequential method of 3 states: (a) schematic,

(b) state machine.

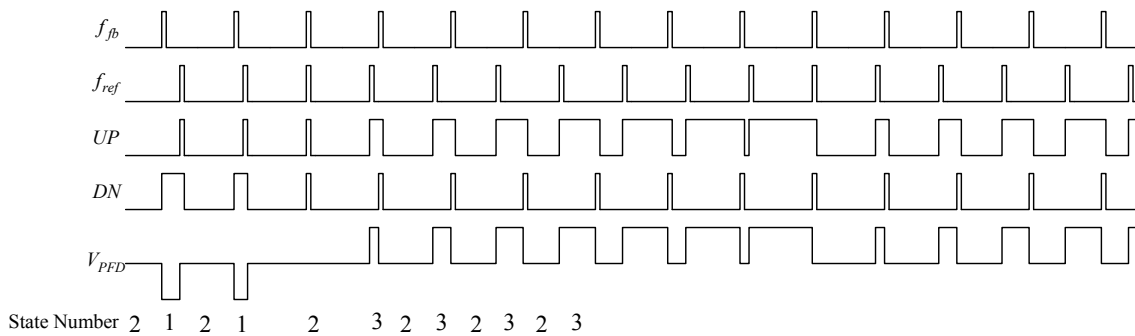


Fig. 2.4. The output signal of PFD using 3-state sequential method.

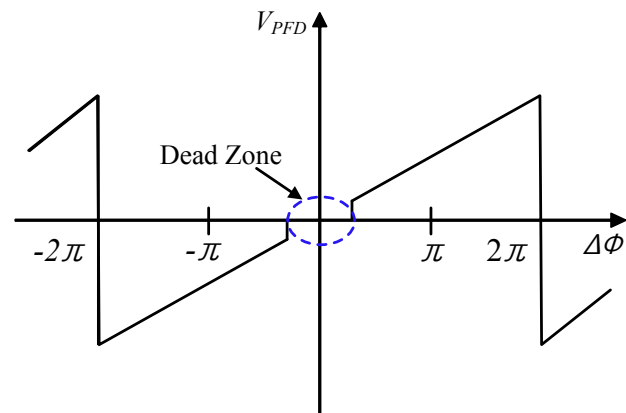


Fig. 2.5. The transfer function of PFD in dead zone.

voltage. The output signal of PFD is according to the events of state machine as shown in Fig. 2.4. The most important factor to consider is a dead-zone effect in which the phase/frequency difference is not detected as shown in Fig. 2.5. Even though the input signal of PFD has a different phase and frequency compared to the reference signal, the system does not change the gain of the PFD (defined as the ratio between the output

voltage and the phase difference) and then the PLL loses the locking. To overcome this problem (due to finite gate delay), time delay is required to reset the time when UP/DOWN is 1 (high) in PFD. As seen in Fig. 2.6, there are delay components like an Inverter.

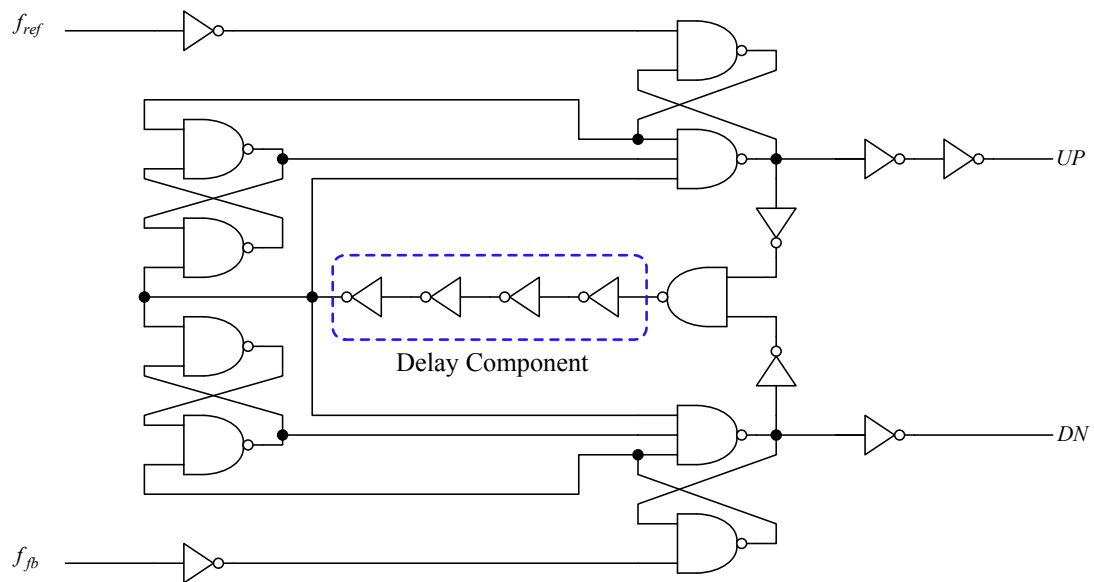


Fig. 2.6. Block diagram of PFD with gate delayed using inverters.

B. Charge Pump and Loop Filter

CP takes the UP and DN outputs of the PFD as input signals and gives a single current output (I_{PD}) [19]-[20]. Fig. 2.7 shows a simplified schematic of the CP and LF.

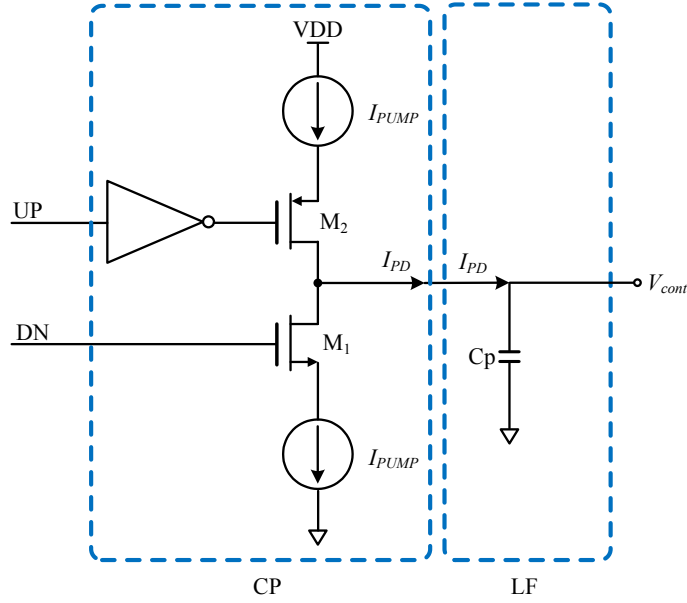


Fig. 2.7. Schematic of the charge pump (CP) with loop filter (LF).

When UP signal is in the “high” state, transistor M_2 turns ON while transistor M_1 is OFF, and the output current (I_{PD}) has a positivity polarity. On the other hand, when the DN signal becomes high, M_1 turns ON while M_2 is OFF, and I_{PD} has a negative polarity. With the switching operations by M_1 and M_2 according to UP and DN signals, the charge pump output current can be expressed as [21]

$$\begin{aligned}
 I_{PD} &= \frac{I_{PUMP} - (-I_{PUMP})}{4\pi} \times \Delta\Phi \\
 &= \frac{2I_{PUMP}}{4\pi} \times \Delta\Phi \\
 &= \frac{I_{PUMP}}{2\pi} \times \Delta\Phi \\
 &= K_{PD} \times \Delta\Phi
 \end{aligned} \tag{2.1}$$

where $K_{PD} = I_{PUMP}/2\pi$ (amps/radian).

As seen in Fig. 2.7, the output current IPD of the CP is fed into the LF, which is a simple low-pass filter made by a shunt capacitor C_p , whose transfer function is simply given by

$$\frac{V_{cont}}{I_{PUMP}}(s) = \frac{1}{sC_p} \quad (2.2)$$

where $s=j\omega$ is Laplace transform.

C. Voltage Controlled Oscillator.

VCO (after the LF) generates a periodic output signal whose frequency depends on the applied control voltage (V_{cont}) coming from the LF. Considering the VCO as a voltage-to-frequency converter for simplicity, its transfer characteristic can be written as

$$f_{out}(t) = K_{VCO}V_{cont} \quad (2.3)$$

where $f_{out}(t)$ is the VCO output frequency and K_{VCO} is the gain of VCO in the unit of Hz/V. Integrating both sides of (2.3) versus time yields

$$\Phi_{out}(t) = K_{VCO} \int_0^t V_{cont} \quad \text{or} \quad \frac{\Phi_{out}}{V_{cont}}(s) = \frac{K_{VCO}}{s} \quad (2.4)$$

where V_{cont} is assumed as a constant, which has a DC value under ideal condition.

D. Linear Model of PLL.

The PLL in Fig. 2.1 can be redrawn, considering each sub-block as a linear system, as a linear model shown in Fig. 2.8. The open-loop transfer function can be derived from Fig. 2.8 as

$$H(s)|_{open} = \frac{\Phi_{out}}{\Phi_{ref}}(s) = \frac{I_{PUMP}}{2\pi} \frac{K_{VCO}}{s^2} \quad (2.5)$$

The linear model in Fig. 2.8 also gives a closed-loop transfer function of

$$H(s)|_{closed} = \frac{\Phi_{out}(s)}{\Phi_{ref}} = N \cdot \frac{\frac{I_{PUMP} K'_{VCO}}{2\pi C_P}}{s^2 + \frac{I_{PUMP} K'_{VCO}}{2\pi C_P}} \quad (2.6)$$

where $K'_{VCO} = \frac{K_{VCO}}{N}$. The poles of the closed-loop transfer function are obtained from

(2.6) as

$$s = \pm j \sqrt{\frac{I_{PUMP} K'_{VCO}}{2\pi C_P}} \quad (2.7)$$

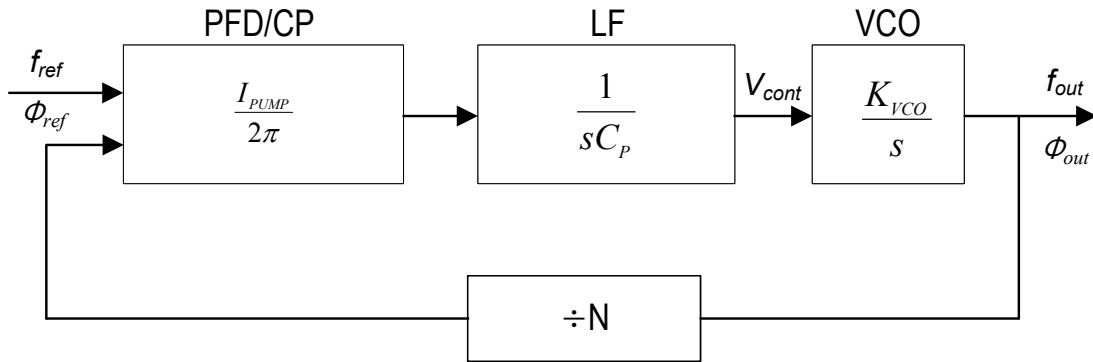


Fig. 2.8. Linear model of the PLL in Fig. 2.1.

As described by (2.7), the closed-loop transfer function contains two imaginary poles, which suggests that the PLL system is unstable. In order to stabilize the system, an additional zero needs to be included in (2.6), which can be achieved by inserting

resistor R_p in series with C_p as shown in Fig. 2.9. With the added resistance (R_p), the transfer function of the LF becomes

$$\frac{V_{cont}}{I_{PUMP}}(s) = \frac{1 + sR_pC_p}{sC_p} \quad (2.8)$$

where $s=j\omega$.

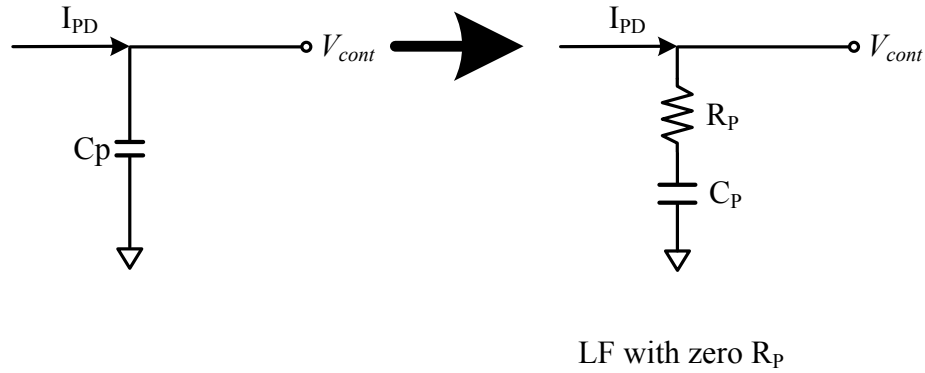


Fig. 2.9. Modified loop filter (LF) for stabilization with R_p .

The closed-loop transfer characteristic of the PLL with modified LF can be written as

$$\begin{aligned} H(s)|_{closed} &= N \cdot \frac{(1 + R_pC_p s) \frac{I_{PUMP} K'_{VCO}}{2\pi C_p}}{s^2 + s \frac{I_{PUMP} K'_{VCO}}{2\pi} R_p + \frac{I_{PUMP} K'_{VCO}}{2\pi C_p}} \\ &= N \cdot \frac{(1 + R_pC_p s) \omega_n^2}{s^2 + 2s\zeta\omega_n + \omega_n^2} \end{aligned} \quad (2.9)$$

where $\omega_n = \sqrt{\frac{I_{PUMP} K'_{VCO}}{2\pi C_P}}$ and $\zeta = \frac{R_P}{2} \sqrt{\frac{I_{PUMP} C_P K'_{VCO}}{2\pi}}$ with ω_n being the natural frequency and ζ being the damping factor. Fig. 2.10 shows the open-loop transfer function of the linear PLL model shown in Fig. 2.8 without and with R_P . As shown in Fig. 2.10(a), the phase margin is zero and hence the PLL is unstable. On the other hand, as shown in Fig. 2.10(b), the addition of R_P creates a zero and produces a 90-deg phase margin, which stabilizes the system. However, it causes ripples (periodic fluctuations) on V_{cont} , which generates sideband spurious tones. To reduce sideband spurs as well as to provide the stability for PLL, therefore, it is common to insert additional poles and zeros at proper locations in PLL design [22].

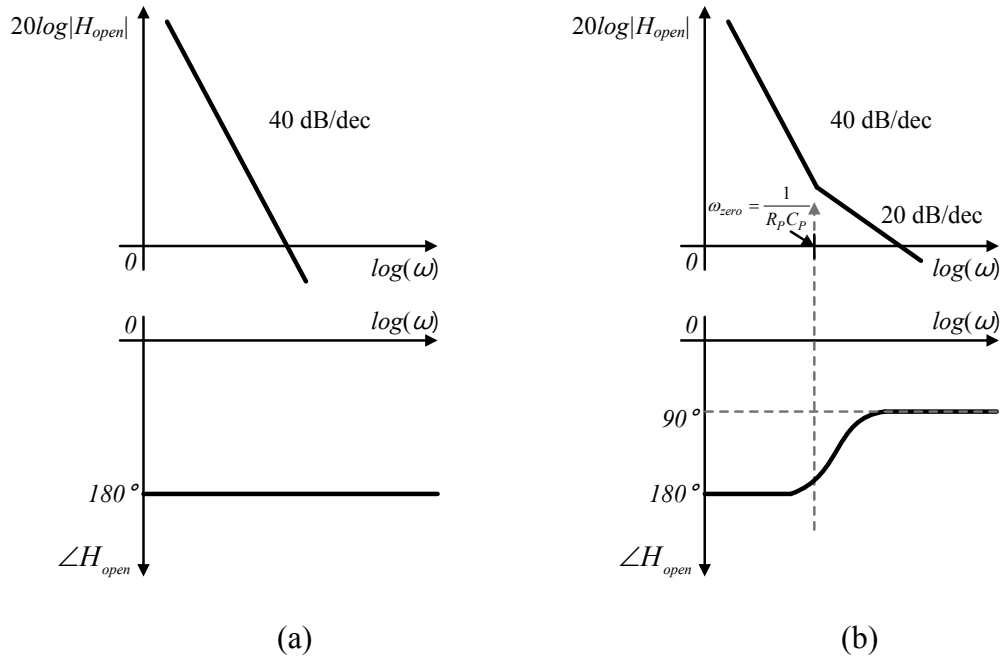


Fig. 2.10. Transfer function and phase margin of a linear PLL model (a) without R_P and (b) with R_P .

E. Frequency Divider

An external crystal oscillator is typically used as a reference source which has limited low frequency operation (up to a few hundreds of MHz) due to its physical property. On the other hand, the VCO typically has high frequency and hence the VCO output frequency needs to be divided until it is comparable to the reference frequency. Frequency division can be performed all in analog or digital domains, or combination of the two. Analog type frequency divider is normally used at the output of the VCO due to its high operation frequency with relatively low power consumption. There are different types of analog type frequency dividers such as current-mode logic (CML), true single-phase clock (TSPC), Miller type, and injection-locked (IL) type. The characteristics of each divider type are summarized in Table 2.1.

TABLE 2.1
Comparison between divider types

Divider structure	Advantage	Disadvantage
CML	High operating frequency Good phase noise	High power
TSPC	Low power	Limited operating frequency Rail-to-rail swing
Miller	High operating frequency	High power Poor phase noise
IL	High operating frequency Low power	Narrow locking bandwidth

The CML divider is simply built with a D-flip-flop, where the output (Q) is feedback into the input (D) as shown in Fig. 2.11(a). The master-slave D-flip-flop is composed of differential circuit for each latch as shown in Fig. 2.11(b). It samples the input while M_1 and M_2 pair is activated, and holds the data by means of the cross-coupled M_3 and M_4 . At low frequencies, the latches locked the sampled data and wait until the next clock phase comes in. The loop gain of the positive feedback ($M_3 - M_4$ pair and R_D) must exceed unity, and the output looks like a square wave under such a condition.

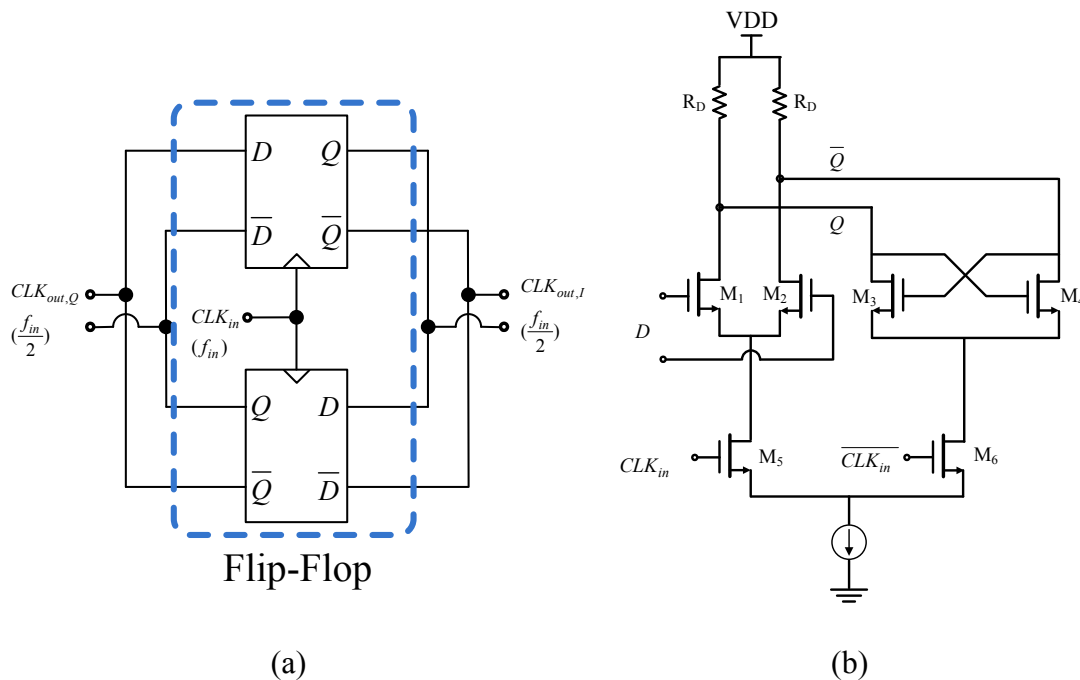


Fig. 2.11. CML frequency divider for 1/2 division: (a) block diagram using flip-flop, (b) schematic of each latch.

The injection-locked frequency divider can be implemented using tuned VCO (both LC VCO and ring VCO) resonating at a free-running frequency f_o [23]. Both LC VCO and ring VCO can be used to be a tuned VCO. A ring VCO has advantages of wide tuning range and small layout area compared to an LC VCO. However, an LC VCO typically exhibits superior performance in terms of phase noise, power consumption, and high frequency operating over a ring VCO. Fig. 2.12 shows the conceptual operation of injection locking in an oscillator. Assume that the required phase condition for oscillation is maintained and the total phase shift in the loop is zero at steady state. When the injection signal (i_{INJ}) with the frequency of (ω_i) is applied, it causes a deviation in the free running frequency (ω_o) by $\omega_i - \omega_o$. Consequently a phase shift of $\Phi_0/2\pi$ occurs in the resonator as shown in Fig. 2.13 and it forces the oscillation frequency to be ω_i rather than ω_o , where Φ_0 is the relative phase between the voltage and current in the resonator. The detailed explanation including a locking range is introduced in chapter III.

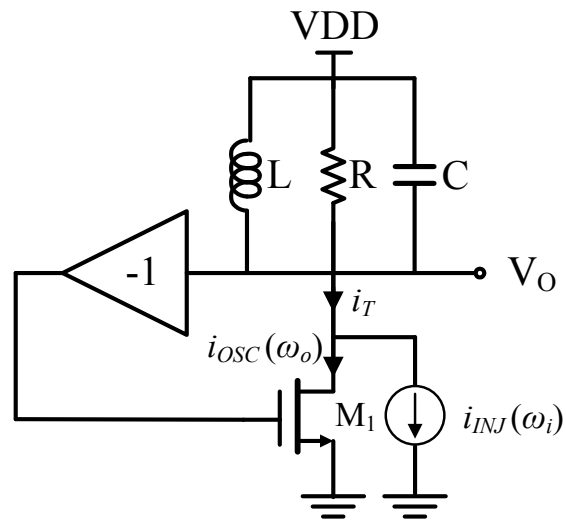


Fig. 2.12. Schematic of ILFD [24], [31].

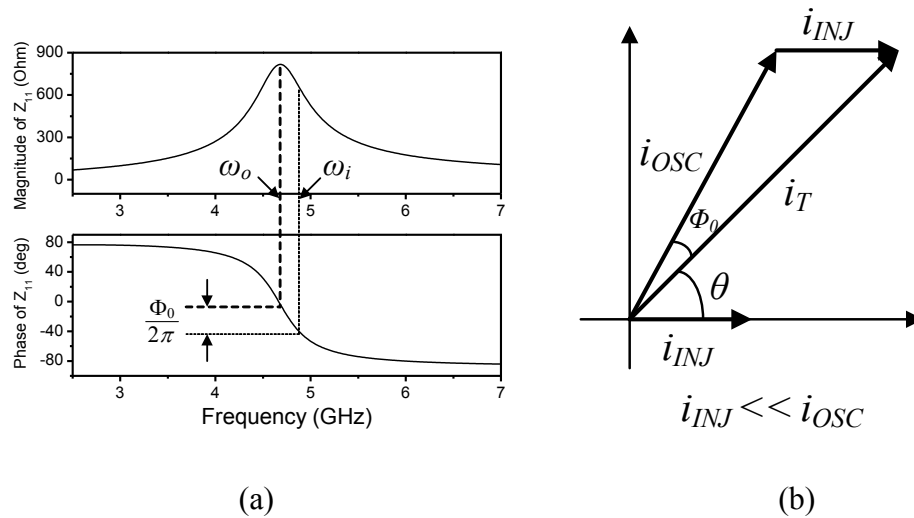


Fig. 2.13. Operation of ILFD: (a) phasor interpretation between ω_o and ω_i . Z_{11} is the input impedance of the resonator, (b) phasor diagram between i_{OSC} and i_{INJ} .

2. Conclusions

In this chapter, we have reviewed the principle of PLL design including PFD, CP, LF, frequency divider and VCO. It's transfer function and the linear model are briefly studied for the PLL itself. In the end, we have reviewed the ILFD and CML divider, for high frequency part and low frequency part in our design, respectively. This chapter presents as a basic knowledge for the design and analysis in later chapters. Circuit design and detailed analysis for each building block of the multi-band multi-output PLL will be discussed in the following chapters.

CHAPTER III
LOW POWER WIDE-LOCKING-RANGE DUAL-INJECTION LOCKED 1/2
DIVIDER

1. Introduction

Frequency divider is one of the most crucial building blocks in frequency synthesizer. Frequency divider is used for the frequency division of LO signals. Once divided, the phase and frequency of the divided signal is then compared with a reference signal. The reference signal is generally supplied by a crystal oscillator, whose maximum frequency is typically limited to only a few hundreds of MHz due to increased error at higher frequencies and limitation on physical material. To compare the low-frequency reference signal and high-frequency LO signal for tracking the phase and frequency, the LO signal needs to be divided until it has the same frequency with the reference signal.

Frequency divider can be categorized into 3 types: current-mode logic (CML), true single-phase clock (TSPC) type, and injection-locked (IL) type. The CML frequency divider is widely used in the PLL, accredited to its good input sensitivity. However, it generally requires high power and even higher power as the operating frequency increased [25], [26]. The TSPC frequency divider is limited to relatively low frequencies while having low-power characteristics [27]. Among the different divider types, the injection-locked frequency divider (ILFD) is popular since it can be designed to operate at high frequencies with low power consumption.

The frequency divider is based on Injection-Locked Oscillator. Injection-Locked Oscillator can be categorized into first-harmonic injection locked oscillator (FHILO), sub-harmonic injection locked oscillator (SBILO) and super-harmonic injection locked oscillator (SPILO) according to the injection frequency in (3.1) to (3.3). Especially, SPILO can be used as part of super-harmonic injection locked frequency divider (SPILD).

$$f_i = f_o, \quad \text{for FHILO}, \quad (3.1)$$

$$f_i = \frac{1}{N} f_o, \quad \text{for SBILO}, \quad (3.2)$$

$$f_i = N \times f_o, \quad \text{for SPILO}, \quad (3.3)$$

where f_i is the injection frequency, f_o is the output frequency of injection-locked oscillator and N is the integer value for divide ratio.

Fig. 3.1(a) shows a simple circuit schematic of a conventional direct injection-locked frequency divider (DILFD). The injection signal of frequency ω_i is applied to the gate of the transistor M_3 . Due to the nonlinearities of an active device (M_3), many intermodulation products are generated between the injection signal at (ω_i) and output signal at (ω_o). For 1/2 frequency division, only the desired signal at (ω_o) = $\omega_i/2$ is extracted through the LC-resonator at the output.

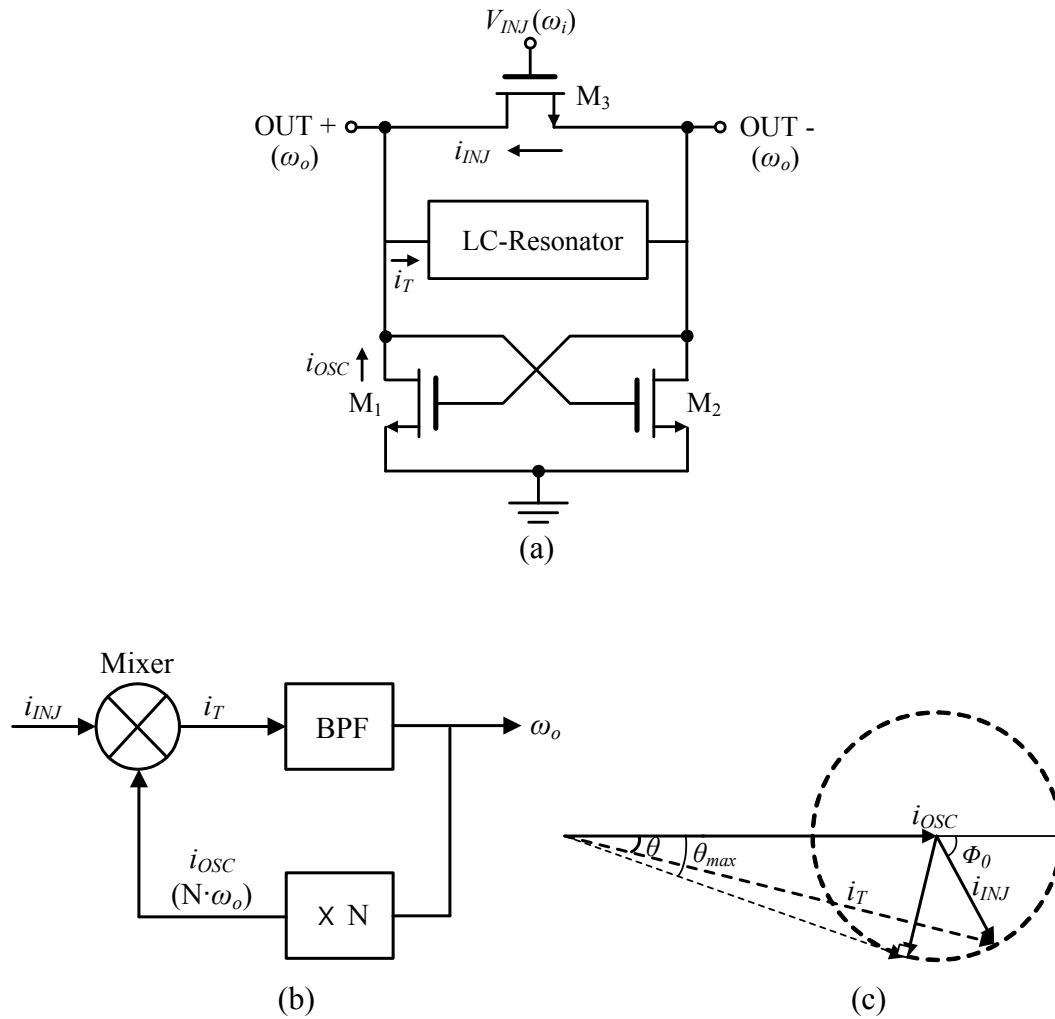


Fig. 3.1 A conventional DILFD with single injection at NMOS: (a) schematic, (b) equivalent model using mixer, BPF, multiplier N , and (c) phasor diagram between i_{OSC} and i_{INJ} .

Fig. 3.1(b) shows an equivalent model of the DILFD shown in Fig. 3.1(a), which includes a band-pass filter (BPF) formed by the LC resonator, an N^{th} order multiplier ($\times N$), and a mixer.

Fig. 3.1(c) shows a phasor diagram between the current of the cross-coupled pair i_{OSC} and injection current i_{INJ} , where Φ_0 is the relative phase between them. The locking range is enhanced as the angle θ is increased, and the maximum locking range is achieved when θ reaches θ_{max} which happens when the angle between i_T and i_{INJ} is 90° .

Conventional DILFD generally has limited locking range. The locking range of DILFD can be increased to some extent by employing techniques such as shunt-peaking [28], [29], impedance matching at the injection device, frequency tuning using varactor and/or capacitor bank. etc. In super-harmonic dividers, the locking range is even narrower in case of higher-order division since the coefficients of the N^{th} order harmonic of the injection signal (ω_i), which is contained in the series expansion of the injection signal, are smaller for higher order harmonics [30], [31].

In order to overcome the shortcomings of super-harmonic dividers, various works have been conducted to achieve a wider locking range while keeping the power consumption as low as possible [32]-[36]. Among them, dual-injection method was proposed to enhance the locking range using two injection signals having the same amplitude and phase [32]. The locking range is increased due to the increase of the amplitude of the injected signal resulting from the addition of the two injection signal amplitudes, as can be inferred from Fig. 3.1(c). In [33], the two injection signals are applied with 90° phase difference to obtain an increased locking range. However, the locking range cannot be maximized since the phase angle of the two injected signals is not optimal (i.e., not close to 90 degrees). The performance of the dual-ILFD's is fairly good in terms of locking range and power consumption. However, these papers do not

explain about the optimum phase angle between the injection signals, which maximizes the locking range. Also, the supply voltage (VDD) effect on the locking range is not presented.

A new dual-injection method is proposed to increase the locking range. The new dual-injection method can enhance the locking range by optimizing the quality factor (Q) of the combined transistors M_1 , M_2 and M_3 , the amplitude of the output cross-coupled current (i_{OSC}), and the phase angle between the injected signals. This chapter also analyzes the effects of the bias VDD on the Q and i_{OSC} , as well as the optimized phase angle between two injection signals, which ultimately affect the locking range. This chapter is organized as follows. Section 3.2 presents the operation of 1/2 DILFD using single-injection. Section 3.3 discusses the proposed dual-injection method for improving the locking range. Section 3.4 shows the simulation and measurement results, and Section 3.5 gives the conclusion.

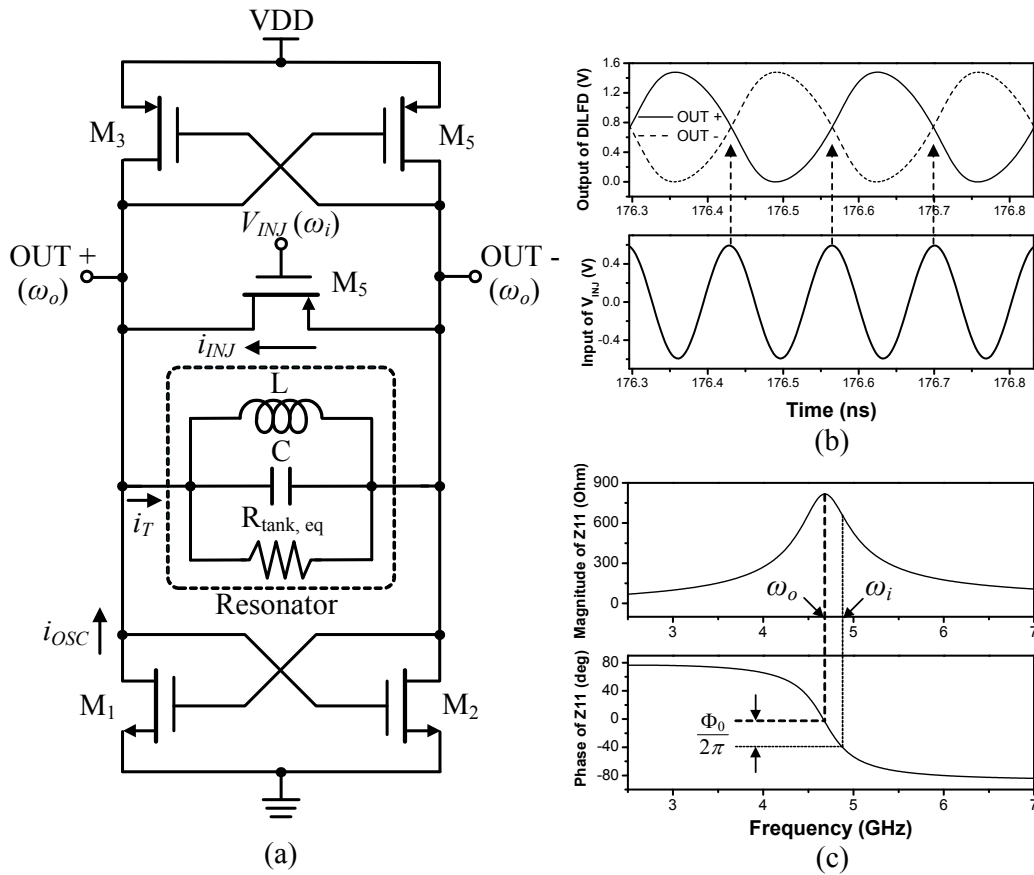


Fig. 3.2 Conventional 1/2 super-harmonic DILFD using single-injection: (a) circuit schematic, (b) output of divider (upper) with injection, V_{INJ} (lower), and (c) phasor interpretation between ω_o and ω_i . Z_{11} is the input impedance of the resonator.

2. Divide-by-2 Divider using Single-Injection

DILFD is a frequency divider that can lock its frequency to the frequency of an externally applied signal or its harmonics. DILFD can be categorized into 3 different types by the division ratio: first-harmonic DILFD, sub-harmonic DILFD, and super-harmonic DILFD. Fig. 3.2(a) shows the schematic of a conventional super-harmonic

DILFD for divided-by 2. Since the injection signal is periodic, the output of the divider is periodically “short” and “open” as M_5 turns ON and OFF by the injection signal (ω_i), respectively. Fig. 3.2(b) plots the transient results of the DILFD, which shows that the output frequency is divided by 2 ($\omega_i/2$) through the switching operation of M_5 . The resultant total output current (i_T at ω_o) flows into the resonator.

In order to examine the locking range of the super-harmonic DILFD, we assume there exists the necessary for oscillation phase condition. For instance, the phase shift in the loop is zero in steady state. When an injection current (i_{INJ}) is applied, a deviation from the free running frequency (ω_o) by $\omega_i - \omega_o$ results and, consequently, a phase shift of $\Phi_0/2\pi$ occurs in the resonator as shown in Fig. 3.2(c) which results in frequency change, where Φ_0 is the relative phase between the voltage and current in the resonator. The resultant current (i_T) at the output varies according to i_{INJ} and the locking range $\omega_i - \omega_o$ can be estimated as [37]

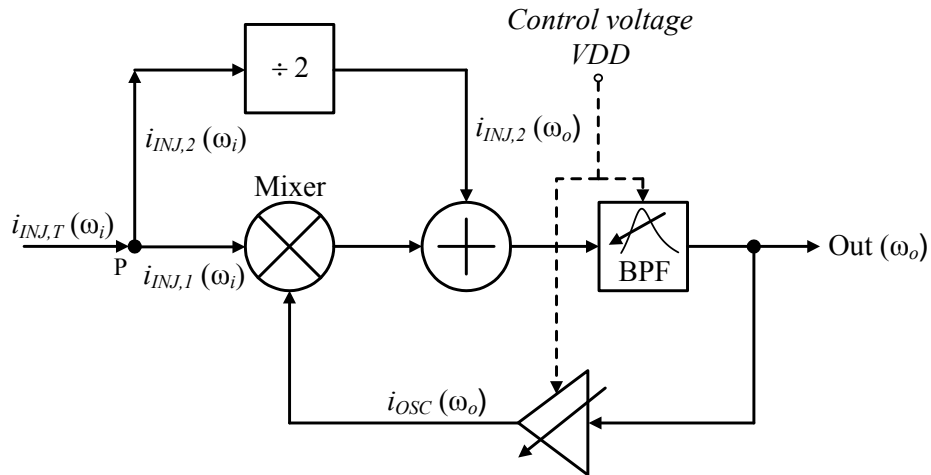


Fig. 3.3 Behavioral model of the proposed 1/2 dual-ILFD.

$$\omega_i - \omega_o = \frac{\omega_o}{2Q_L} \cdot \frac{i_{INJ}}{\sqrt{i_{OSC}^2 - i_{INJ}^2}} \quad (3.4)$$

where Q_L is the loaded quality factor of the LC tank with external elements such as transistors.

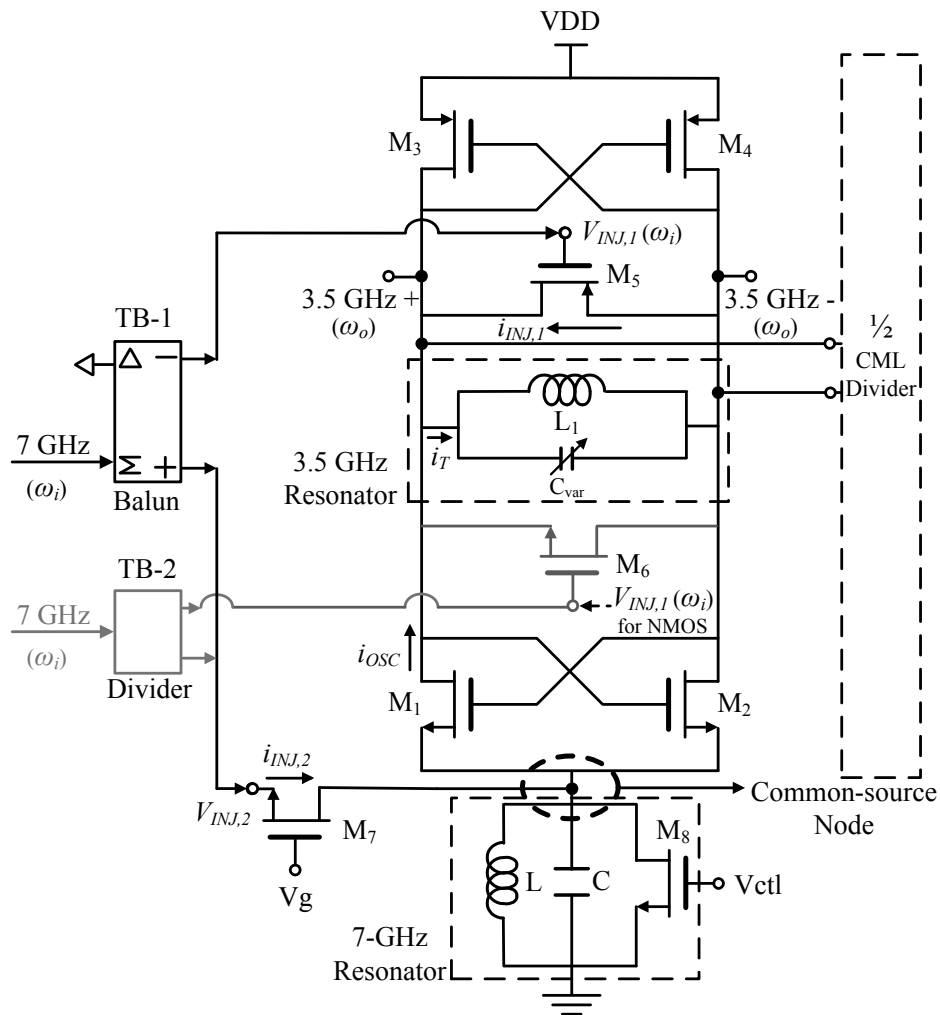


Fig. 3.4 Schematic of the proposed 1/2 dual-ILFD. A 1/2 CML frequency divider is integrated with the dual-ILFD and used to compensate for the output voltage variation. The injection signal is via either a balun or divider.

As can be seen in (3.4), the locking range can be increased by adjusting i_{INJ} , reducing Q , and/or decreasing i_{OSC} . Eq. (3.4) also indicates that i_{INJ} cannot be greater than i_{OSC} . i_{INJ} can be increased by using either the current reuse technique in [38] or dual-injection method in [32], [33] without consuming additional power. Reduced Q can be achieved by employing a resonator with lower Q . The relationship between reduced i_{OSC} and locking range is explained in section 3.

3. Proposed Divide-by-2 using Dual-Injection

A. The Proposed Concept of Dual-Injection

In the previous section, a 1/2 DILFD using single-injection method is discussed and its locking range is estimated as in (3.4). In order to increase the locking range, Dual-injection method is proposed. Fig. 3.3 shows an equivalent model for the proposed 1/2 dual-ILFD as shown in Fig. 3.4, which does not consume additional power as compared to a single-injection counterpart.

The new 1/2 dual-ILFD has two injection signals ($i_{INJ,1}$, $i_{INJ,2}$) and a control voltage (VDD) for optimizing Q_L and the amplitude of i_{OSC} needed for enhancing the locking range. The amplitude of i_{OSC} is controllable and it is modeled as a variable gain amplifier. The loaded Q_L is tunable and its resonant characteristic, and hence quality factor, can be modeled as a band-pass filter (BPF) response. An injection signal (i_{INJ}) at ω_i splits into $i_{INJ,1}$ and $i_{INJ,2}$ at node P through a balun or (equal-phase) divider depending on the device type used for injection in Fig. 3.3 and Fig. 3.4. $i_{INJ,1}$ is injected into a mixer, which represents a MOSFET used for direct injection (such as M_5 in Fig. 3.4), and it is

added to i_{OSC} . $i_{INJ,2}$ is injected at the common-source node of a cross-coupled pair, and then added to the output current ($i_{INJ,1} + i_{OSC}$). At the output, only a desired output component (ω_o) is obtained by filtering.

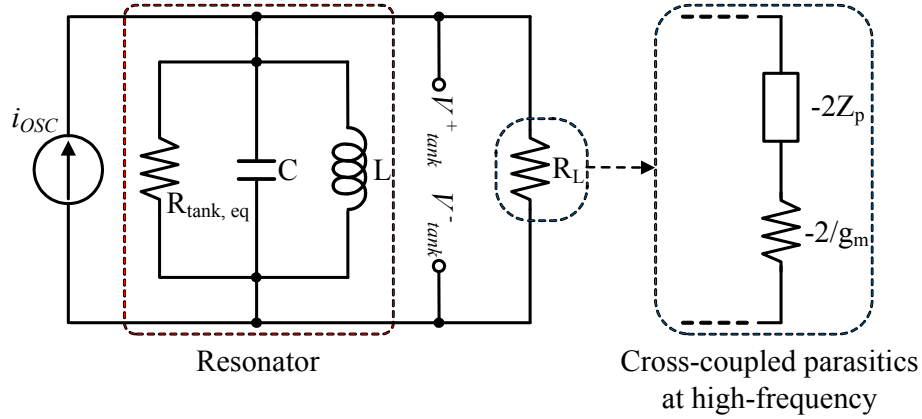


Fig. 3.5 Equivalent circuit of resonator with external load R_L .

Similar to the single-injection case, the locking range under the dual-injection can be approximately estimated by

$$\omega_i - \omega_o = \frac{\omega_o}{2Q_L} \cdot \frac{i_{INJ}}{\sqrt{i_{OSC}^2 - i_{INJ}^2}} \quad (3.5)$$

where $i_{INJ} = i_{INJ,1} + i_{INJ,2}$. Note that summation between $i_{INJ,1}$ and $i_{INJ,2}$ is vector. From (3.5), the locking range can be enhanced by reducing Q_L and i_{OSC} as well as adjusting i_{INJ} .

When the resonator is connected to an external load, the loaded quality factor (Q_L) can be expressed as

$$\frac{1}{Q_L} = \frac{1}{Q_E} + \frac{1}{Q} \quad (3.6)$$

where Q and Q_E represent the quality factor and external quality factor of the resonator, respectively.

Fig. 3.5 shows an equivalent circuit of the resonator circuit with an external load R_L , where $R_{tank,eq}$ is the effective resistance of the LC tank. The external load can be modeled as a series connection of the negative transconductance of the cross-coupled pair ($-2/g_m$), where g_m is the transconductance for one pair, and the impedance due to parasitic capacitors at high frequency ($-2Z_p$), where $Z_p = 1/(j2\omega_o C_p)$ with C_p being the parasitic capacitance at the common source node as seen in Fig. 3.4.

The external quality factor (Q_E) due to the cross-coupled pair can be expressed using its transconductance (g_m) and parasitic capacitance (C_p) as [39].

$$Q_E = \frac{g_m^2}{4 C_p^2 \omega_o^2} \quad (3.7)$$

An optimization mechanism of Q_E can be deduced from (3.7). If the supply voltage (V_{DD}) is decreased, I_{osc} (dc current) and i_{OSC} reduce accordingly. This will result in lower g_m , thus leading to reduced Q_E . Also, the voltage V_{tank} , across $R_{tank,eq}$ decrease in a linear manner as i_{OSC} lowers according to:

$$i_{OSC} = \frac{V_{tank}}{R_{tank,eq}} \quad (3.8)$$

where the maximum amplitude of V_{tank} is V_{DD} . Consequently, reducing V_{DD} to an optimum point gives an optimum value for Q_E and thus Q_L .

To verify how and how much Q_E is changed by varying I_{osc} , we use the

fundamental current equations of MOSFET, neglecting the channel-length modulation effect, in the saturation region:

$$g_m = 2\sqrt{\beta \cdot I_{osc}} \quad (3.9)$$

$$I_{osc} \approx \beta \cdot [V_{GS} - V_T]^2 \quad (3.10)$$

where V_T is the threshold voltage and β is $0.5\mu_n C_{ox}(W/L)$, with μ_n being the mobility of the carriers in the channel, C_{ox} being the oxide capacitance, and W and L being the transistor width and length, respectively. The gate-source voltage (V_{GS}) of the cross-coupled pair is equal to $VDD/2$, which is the output common mode level of the designed 1/2 dual-ILFD. Equating I_{osc} obtained from (3.9) and (3.10) with $V_{GS} = VDD/2$ give

$$I_{osc} = \frac{g_m^2}{4\beta} \approx \beta \cdot \left[\frac{VDD}{2} - V_T \right]^2 \quad (3.11)$$

The amplitude of I_{osc} in the designed 1/2 DILFD is minimum and maximum at the minimum (VDD_{min}) and maximum (VDD_{max}) value of VDD , respectively, according to (3.11). This leads to

$$\beta \cdot \left[\frac{VDD_{min}}{2} - V_T \right]^2 < I_{osc} \leq \beta \cdot \left[\frac{VDD_{max}}{2} - V_T \right]^2 \quad (3.12)$$

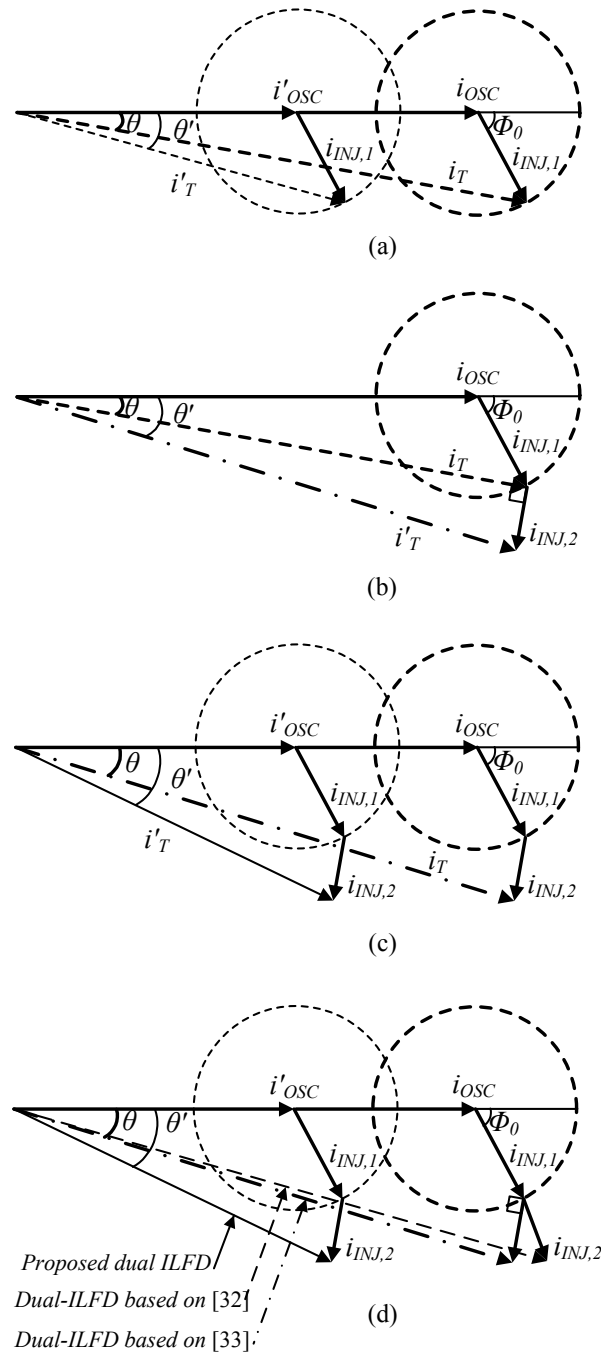


Fig. 3.6 Phasor diagrams for (a) single-injection vs. single-injection with reduced i_{OSC} and hence reduced Q_L , (b) single-injection vs. dual-injection, (c) dual-injection with and without reducing i_{OSC} (equivalent to with and without optimized Q_L), and (d) proposed dual injection vs. other dual injection.

In order to estimate the range of I_{osc} , we let V_T be 0.5 V and VDD_{max} be 1.8 V. We let VDD_{min} be 1.5 V, which is a reasonable value for guaranteeing oscillation. Substituting these values into (3.12) gives

$$0.0625 \cdot \beta < I_{osc} \leq 0.16 \cdot \beta \quad (3.13)$$

which shows a possible tuning range for I_{osc} .

We can see from (3.13) that I_{osc} can be reduced by about 60 % from the maximum. Correspondingly, g_m^2 can be reduced by the same amount, leading to a reduction in Q_E as can be seen from (3.7). Therefore, according to (3.8) and (3.12), by reducing VDD to a certain minimum value, i_{OSC} , and hence Q_E , can be optimized to produce an enhanced locking range.

Fig. 3.6 shows the conceptual phase diagrams under different conditions. Fig. 3.6(a) illustrates the effect of increasing the deviation angle (θ) with respect to the locking range by decreasing i_{OSC} , which correspondingly results in reduced Q_L as we discussed earlier, for single injection. For reduced i_{OSC} (expressed as i'_{OSC}) corresponding to reduced Q_L , the locking range can be increased by $\theta' - \theta$ while the total resultant current, i'_T , is lowered as compared to the original one, i_T . Fig. 3.6(b) compares the dual-injection with single-injection. The second injection signal ($i_{INJ,2}$) is added to the resultant current (i_T) after the first injection. When they bear a 90° phase difference, the effect of the second injection on the locking range is maximized. The effect of the dual-injection with the amplitude of i_{OSC} optimized, and hence Q_L , is shown in Fig. 3.6(c).

Fig. 3.6(d) shows that the locking range of the proposed 1/2 dual-ILFD can be extended further as compared to the other dual-injection methods [32], [33]. It is

manifested that a dual- injection with Q and i_{osc} optimized will maximize the locking range of ILFD. This approach, however, has a disadvantage in that the output amplitude of the 1/2 dual-ILFD varies as VDD and thus i_{osc} is changed. In order to compensate for the output voltage variation, a CML divider is connected to the output of the 1/2 dual-ILFD to produce a constant output amplitude with respect to VDD adjustment. The detailed design of the dual-ILFD will be presented in the following section.

B. Design of Proposed Divide-by-2 Dual- ILFD

Fig. 3.4 shows the schematic of the proposed 1/2 dual-ILFD. The VCO is operated at 3.5 GHz and consists of two complementary cross-coupled pairs and a 3.5-GHz LC resonator. The source and drain terminals of the N/PMOS are connected across the output terminals for direct injection. The 1/2 CML divider is connected at the output of the VCO. A 7-GHz signal is injected through the balun. The shunt-peaking resonator at 7 GHz is connected at the common source node of NMOS cross-coupled pair to create a high-impedance point at 7 GHz, forcing the 7-GHz injected signal to flow toward M_1 and M_2 . M_8 is connected in parallel with the resonator in order to control the impedance of the resonator by adjusting its gate bias voltage.

The operation of the proposed 1/2 dual-ILFD is as follows. Two injection signals ($V_{INJ,1}$ and $V_{INJ,2}$) at 7 GHz (ω_i) generated from a single external source through a balun are fed to M_5 and M_7 . Since these signals are 180° out of phase, M_5 (PMOS) and M_7 (NMOS) are turned on at the same time, thereby the resultant injection currents are constructively added at the output, effectively simulating the dual-injection. The injection current ($i_{INJ,1}$) at M_5 due to $V_{INJ,1}$ flows between the output terminals of the

VCO.

The second injection $V_{INJ,2}$ is applied to M_7 according to common gate which is selected for broadband characteristics. When the 7 GHz signal is injected into the common source node through the common-gate device (M_7), it mixes with one of the odd-harmonic products (10.5 GHz) generated by the switching differential pair M_1/M_2 to produce a 3.5 GHz signal. This 3.5-GHz intermodulation product further increases the output signal at 3.5-GHz (ω_o). The corresponding drain current of M_7 at 3.5 GHz splits into two branches at the common source node, which constitutes $i_{INJ,2}$ at the output.

Fig. 3.7 plots g_m and the current of the cross-coupled pair (M_1) for different values of the control voltage VDD . As the control voltage is reduced, g_m and the current decrease which, as can be seen from (3.7), leads to reduced Q_E . This, in turn, results in reduced Q_L when VDD is decreased, and hence an increase in the locking range can be expected. The output amplitude, however, also decreases as VDD is lowered.

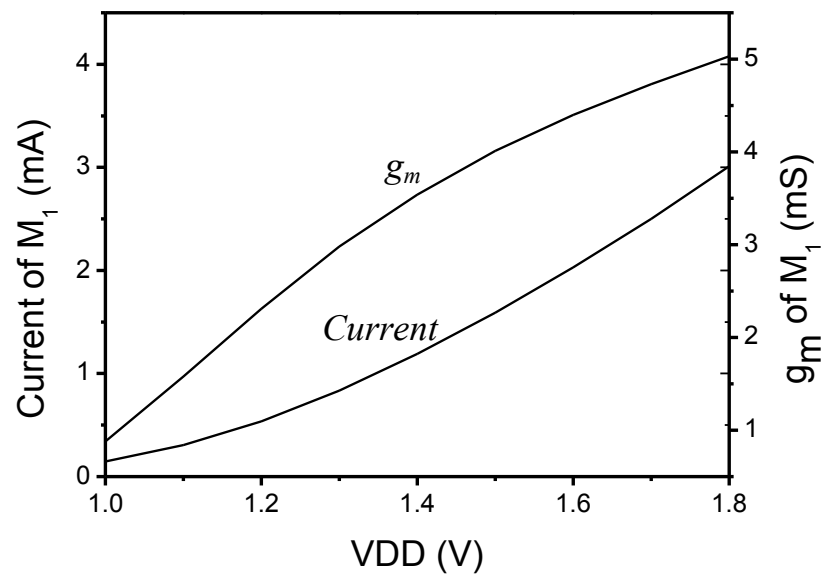


Fig. 3.7 Simulation results of 1/2 dual ILFD: current and g_m of M_1 .

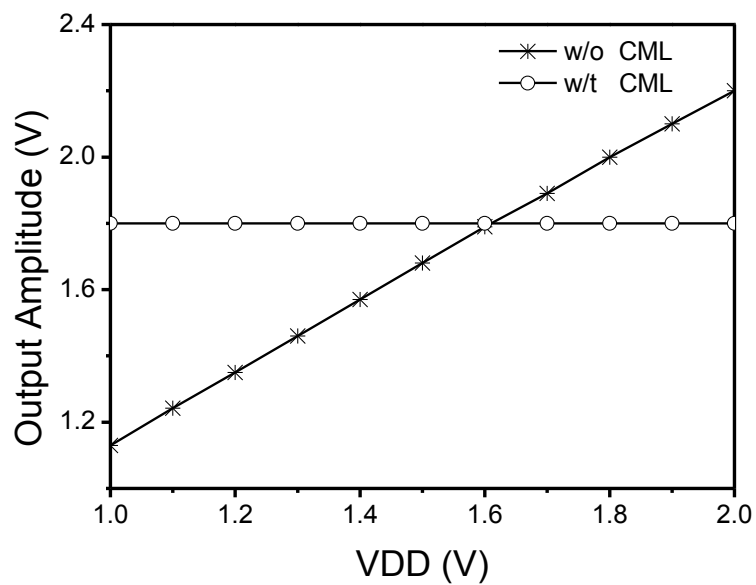


Fig. 3.8 Output amplitude of 1/2 dual-ILFD versus V_{DD} .

This can be problematic if the 1/2 dual-ILFD is cascaded with other blocks such as prescaler or other divider, which is normal configuration in phase-locked loops. Suppose that a digital divider for obtaining a desired division ratio is connected in cascade with the proposed 1/2 dual-ILFD. In standard 0.18- μm CMOS or BiCMOS process, the supply voltage is 1.8 V and the common mode DC voltage of the digital divider is normally set to be 0.9 V. It means that the (peak-to-peak) output voltage amplitude of the 1/2 dual-ILFD should be fixed at 1.8 V so that the output common level is 0.9 V. Since the output amplitude is different from 1.8V due to reduction as V_{DD} is reduced, the common-mode output level of the 1/2 dual-ILFD becomes lower than 0.9 V, which affects the common- mode level of the next stage.

A 1/2 CML divider, instead of a simple DC level shifter, is then connected at the output of the dual-ILFD in order to provide constant output amplitude, regardless of the V_{DD} variation. A 1/2 CML divider also provides an additional 1/2 division, hence relaxing additional division possibly needed in the next stage. Fig. 3.8 compares the output voltages of the proposed 1/2 dual-ILFD and without 1/2 CML divider versus V_{DD} , which shows that a constant output for the proposed 1/2 dual-ILFD.

Fig. 3.9 plots the locking ranges versus injection voltage from a single external source at 7 GHz. Four cases are considered: single-ILFD and dual-ILFD without optimizing V_{DD} , and optimized single-ILFD and dual-ILFD by changing V_{DD} .

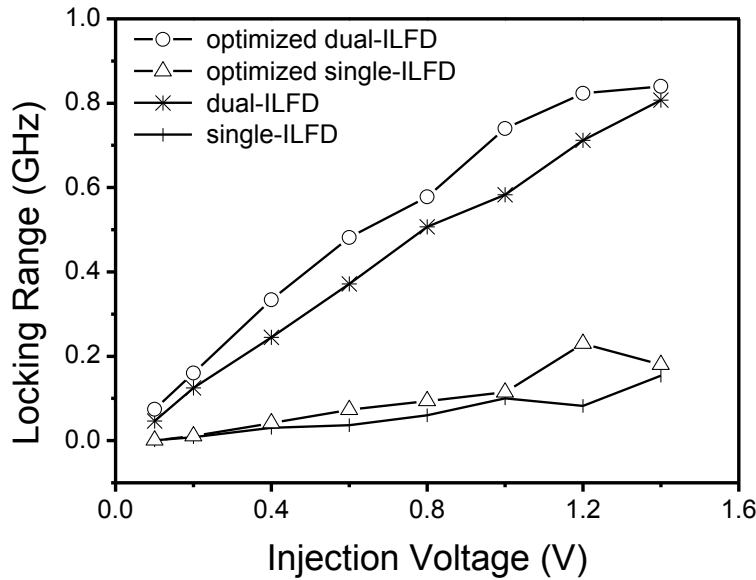


Fig. 3.9 Locking range characteristics of the proposed 1/2 dual-ILFD versus injection voltage for different settings.

The optimized locking range is obtained with lower V_{DD} and, as we note earlier, this corresponds to lower Q_L . Therefore, we can see and verify the positive effects of optimizing $e Q_L$ on the locking range of both dual-ILFD and single-ILFD. It can also be clearly seen that dual-injection method increases the locking range over the single-injection technique. The effect is more significant as the injection voltage level is increased. For example, the enhancement in the locking range is over 500-MHz at the injection voltage of 1 V while it is about 100 MHz at 0.2 V.

4. Measured Results

The designed 1/2 dual-ILFD was fabricated on a 0.18- μm CMOS in BiCMOS process [40] and its die photograph is shown in Fig. 3.10.

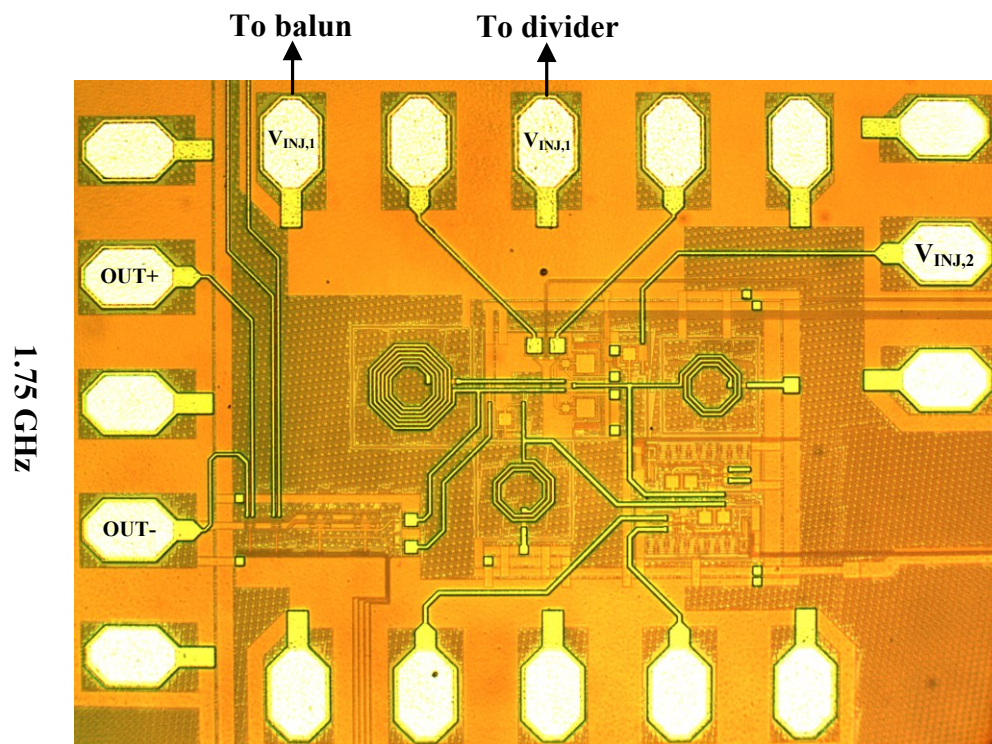
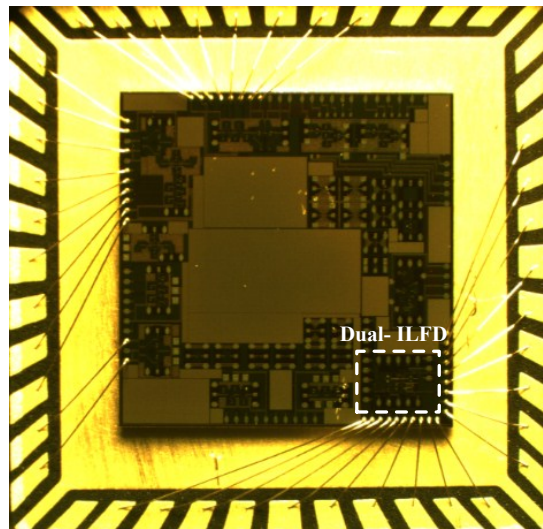
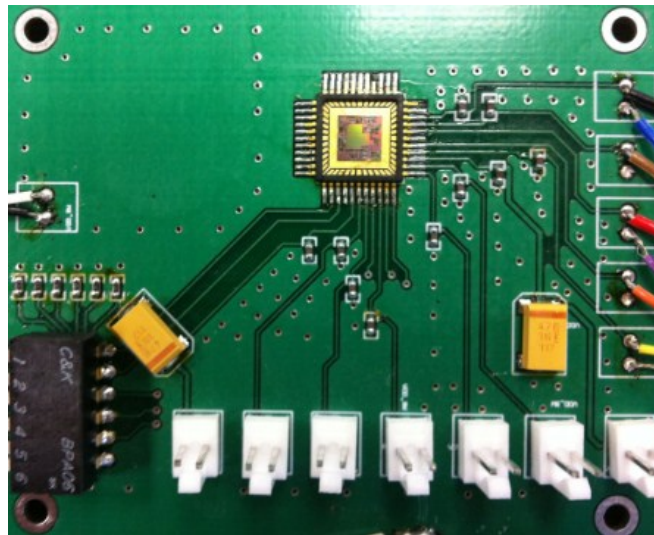


Fig. 3.10 Die photograph of the 1/2 dual-ILFD. Size: 0.8mm^2 (with pads), 0.156mm^2 (without pads). $V_{\text{INJ},1}$ is connected to either a balun or a divider.



(a)



(b)

Fig. 3.11 Microphotograph of the designed 1/2 dual-ILFD (a) packaged chip mounted on FR-4 PCB (b).

The entire chip size is 0.8mm^2 while the core size of the 1/2 dual-ILFD (without the 1/2CML and pads) is 0.156mm^2 . The package of the design chip uses the 44-pin quad flat package (QFP) type and all bias are connected to the chip through wire-bonding on the package mounted on FR-4 PCB as shown in Fig. 3.11.

To reduce the RF leakage through the bias line, the off-chip RF by-pass capacitor on the PCB is located as close as possible to the designed chip. The results of output spectrum are measured using HP 8692L Spectrum Analyzer. The result of phase noise is measured from Agilent E4446 Spectrum Analyzer. The current consumption of the designed 1/2 dual-ILFD with CML divider is 4.8 mA and that of the core 1/2 dual-ILFD is 2.93 mA with the supply voltage of 1.5 V.

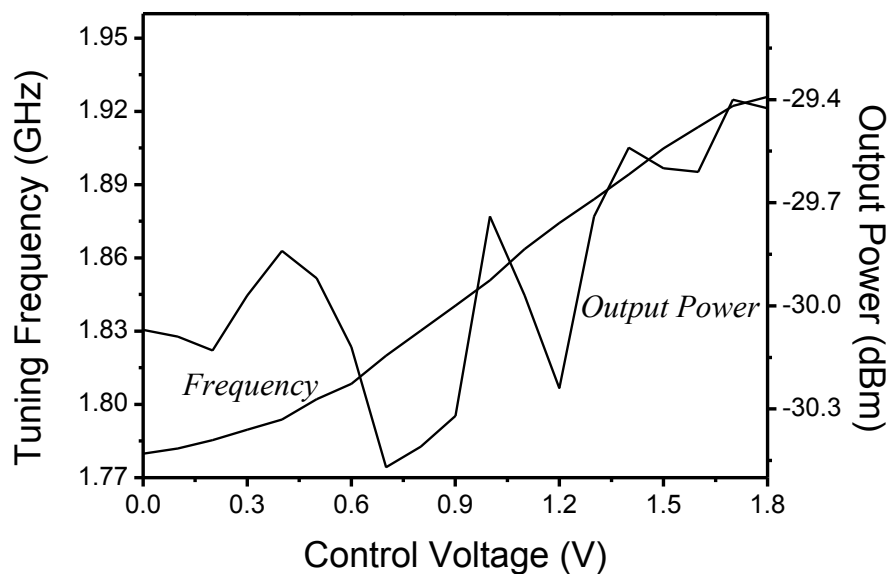
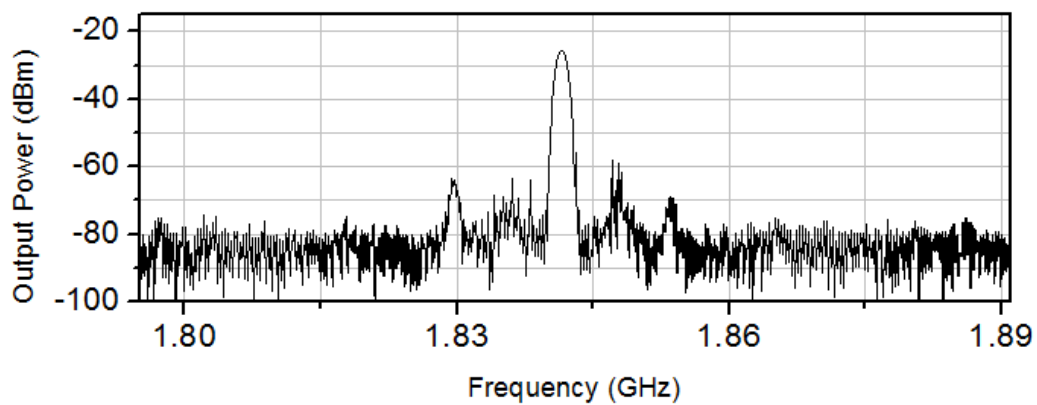
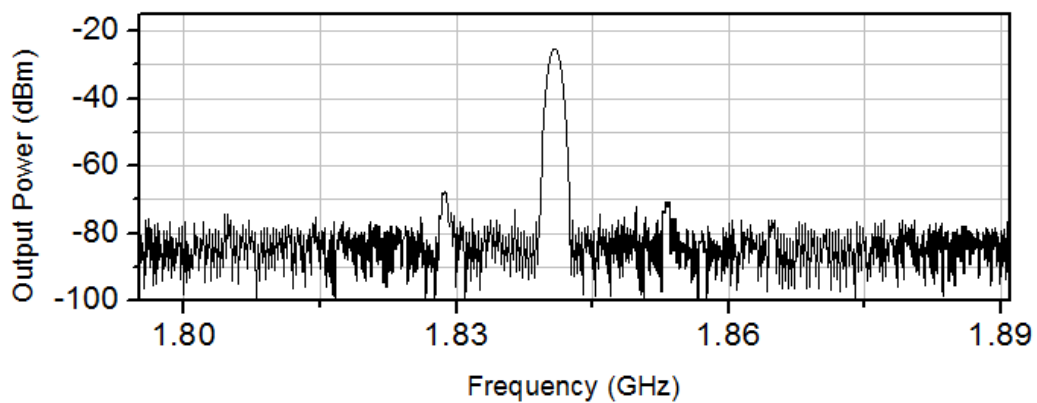


Fig. 3.12 Measured kVCO and output power without injection.

Fig. 3.12 shows the measured frequency range and output power without signal injection (free running) of the designed 1/2 dual-ILFD at the 1/2 CML output as a function of the control voltage of NMOS varactor. As can be seen, the output power varies little over the entire tuning range.



(a)



(b)

Fig. 3.13 Measured output spectrum of (a) the free-running 1/2 dual-ILFD and (b) the locked 1/2 dual-ILFD.

The free-running frequency without injection signal is 1.84 GHz at 0.9 V control voltage as shown in Fig. 3.12. The frequency changes from 1.78 to 1.9 GHz when the voltage of the NMOS varactor is tuned from 0 to 1.8. Fig. 3.13 shows the measured output spectrum of the free-running and locked 1/2 ILFD. As can be seen, the spurious signals are removed after the output signal is locked with the injected signal. Fig. 3.14 displays the measured phase noise of the designed 1/2 dual-ILFD, showing -122.19 dBc/Hz at 1MHz offset. As a comparison, the phase noise -115 dBc/Hz at 1 MHz offset without injection signal is shown in Fig. 3.15. The phase noise -96.36 dBc/Hz at 10 kHz offset with dual-injection is shown in Fig. 3.16 and -120.82 dBc/Hz at 100 kHz offset with dual-injection is shown in Fig. 3.17. The external injection source has -129.92 dBc/Hz at 1 MHz offset as shown in Fig. 3.18. All outputs are measured at output of 1/2

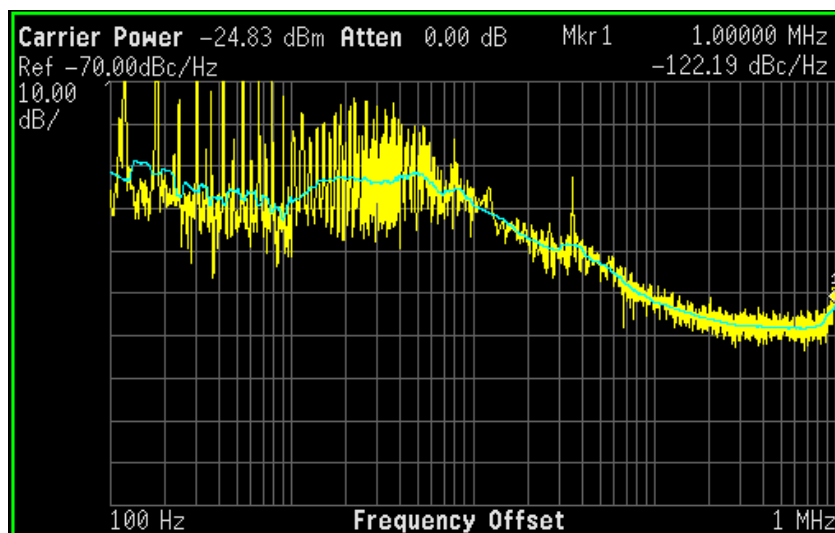


Fig. 3.14 Measured phase noise of the locked 1/2 dual-ILFD.

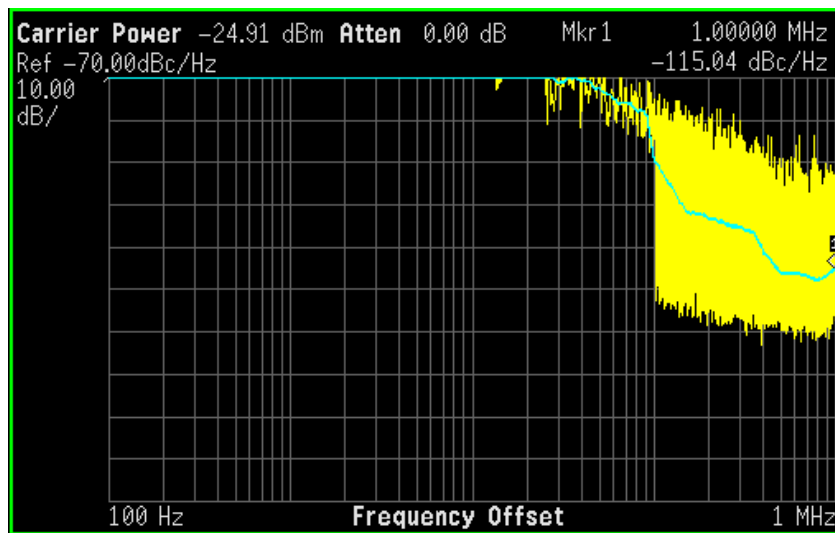


Fig. 3.15 Measured phase noise of the unlocked 1/2 dual-ILFD.

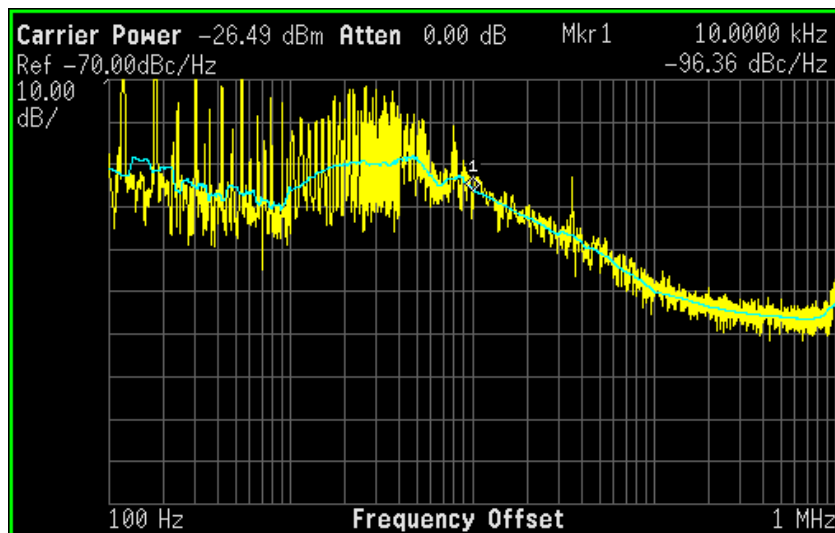


Fig. 3.16 Measured phase noise of the locked 1/2 dual-ILFD.

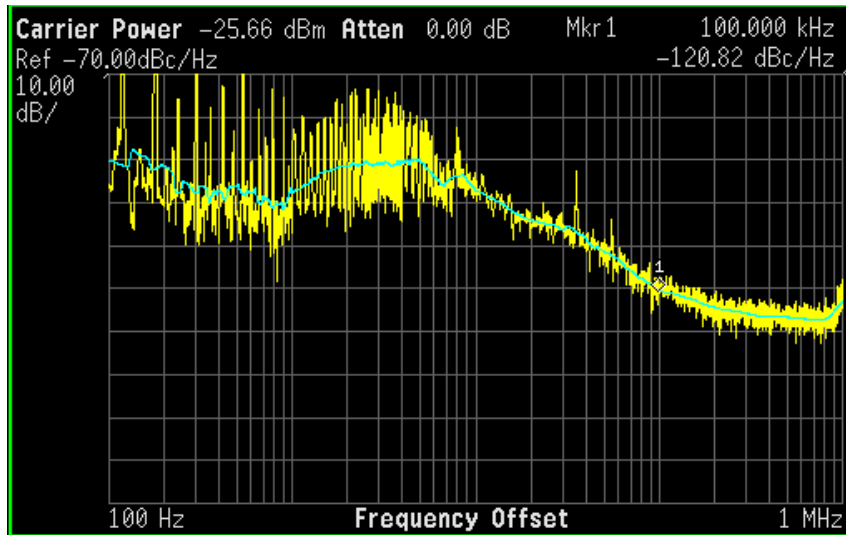


Fig. 3.17 Measured phase noise of the locked 1/2 dual-ILFD.

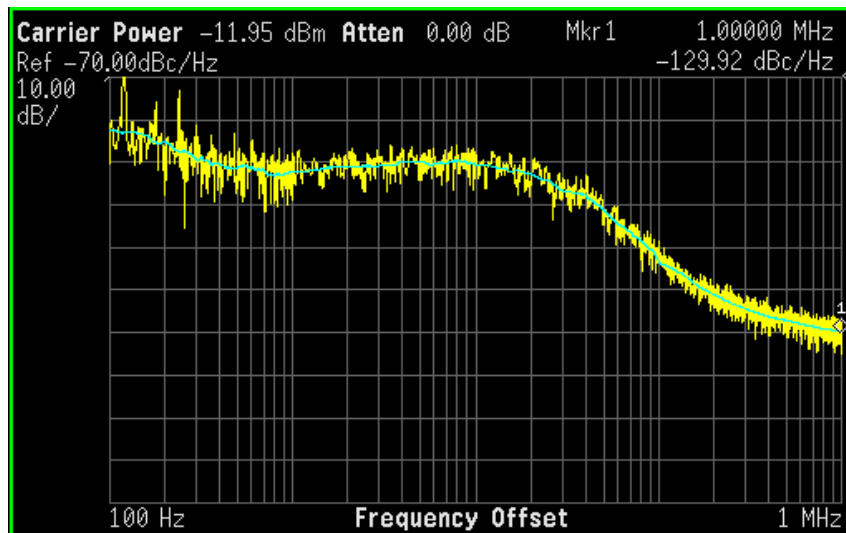


Fig. 3.18 Measured phase noise of 7 GHz external source.

CML divider. In addition, the phase noise of ILFD may provide higher than 122.19 dBc/Hz if measured with a signal generator (injection signal) having better phase noise capability. The locking ranges with single-injection, and dual-injection without and with i_{OSC} and Q_L optimized are about 70 MHz, 502 MHz, and 692 MHz, respectively, and the flatness of the output spectrum is within 1 dB as shown in Fig. 3.19. The locking range of the proposed 1/2 dual-ILFD with optimized Q_L and i_{OSC} is extended almost 10 times better than that for the single-injection and about 27% more than the dual-injection without Q_L and i_{OSC} optimized.

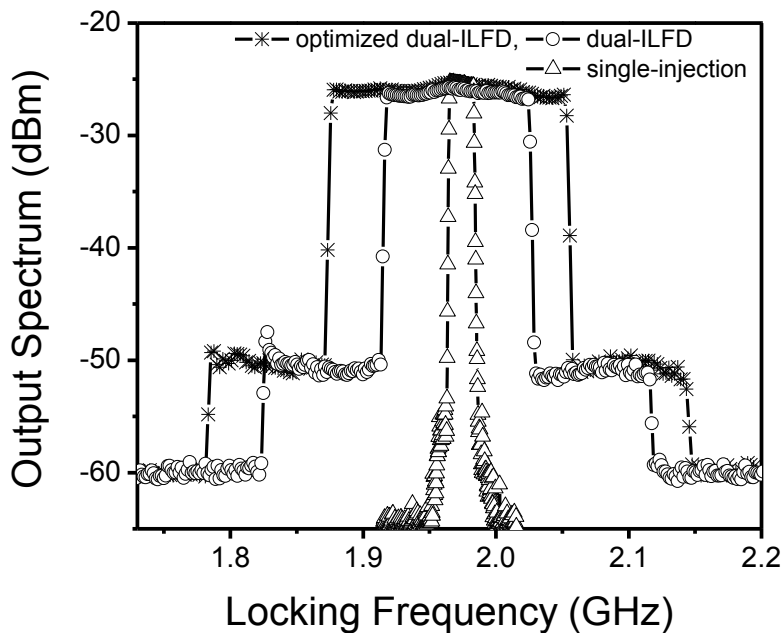


Fig. 3.19 Measured locking range with single-injection and dual-injection for 1/2 function.

TABLE 3.1
Comparison of measurement results between proposed ILFD and others

		This work		[32]	[33]	[41]	
Technology		0.18- μ m CMOS in BiCMOS		0.18- μ m RF CMOS	90-nm digital CMOS	0.13- μ m CMOS	
VDD [V]		Injected via Balun PMOS for $V_{INJ,1}$	Injected via Divider NMOS for $V_{INJ,1}$	1.4	0.8	1.5	
		1.5	1.25				
Power [mW]		4.4	1.5	2.8	0.8	23	
Area [mm ²]		0.156		0.3773	0.385	0.2303	
Division Ratio		$\div 2$		$\div 2$	$\div 2$	$\div 2, \div 3$	
Input Frequency (locking range) [GHz]		Via Balun	Via Divider	53.1-58	35.7 -54.9	PMOS	NMOS
		7.512- 8.204	7.184- 7.654			14.2- 14.8	15.1- 16.1
Input Power [dBm]		10		3	5	7	
Locking Range [%]		Via Balun	Via Divider	8.45	34.9	PMOS	NMOS
		8.8	6.3			4.14	6.41
Phase Noise [dBc/Hz]	@ 10kHz	-96.36		N/A	N/A	N/A	
	@ 100kHz	-120.82		N/A	N/A	N/A	
	@ 1MHz	-122.19		-124.9	-118.44	-126.91	
	External Source @ 1MHz	-129.92 @ 7.05-GHz		N/A	N/A	N/A	
Injection Method		Dual-injection with optimized Q_L and i_{osc}		Dual-injection	Dual-injection	Differential injection	
Divider Architecture		LC-P/NMOS complementary		LC-P/NMOS complementary	LC-P/NMOS complementary	LC-P/NMOS complementary	

The phase noise at low-frequency offsets are not addressed in [32], [33] and [41], while our 1/2 ILFD also includes the phase noise at 10 KHz and 100 KHz. It is noted that the phase noise of an ILFD at high-frequency offsets (e.g., 1 MHz) follows the phase noise of the injection source, while the phase noise at low frequency offsets (e.g., 100 KHz) depends on both the phase noises of the injected source and the free-running oscillator in the ILFD. Therefore, the phase noise of an ILFD at both low and high frequency offsets is very important to evaluate the phase noise performance of an ILFD. Table 3.1 compares the measured performance of the proposed 1/2 dual-ILFD and other

works. Results for injecting signals via a balun and divider are also listed in Table 1. The power consumption of the proposed 1/2 dual-ILFD is lower than those in [32] and [41]. The proposed 1/2 dual-ILFD (via the balun) achieves 8.8 % locking range as compared to 8.45 % and 6.41 % in [31] and [39], respectively. The locking range enhancement in [32] is obtained with the reduced V_{DD} of 1.4 V; however, its effect is not analyzed. In [33], V_{DD} is reduced from 1 V to 0.8 V to increase the locking range in a 90-nm process without analytic explanation. Also, the output power over the locking range varies substantially from -25 dBm to -14.7 dBm in [33], which is not a desirable feature for ILFD, while the proposed 1/2 ILFD output power variation is within 1 dBm.

5. Conclusion

A new 1/2 dual-ILFD that increases the locking range through optimizing the loaded Q and current while minimizing the output amplitude variation as well as providing additional dividing function using a 1/2 CML divider, is proposed. The proposed 1/2 dual-ILFD was fabricated using a 0.18- μm CMOS in BiCMOS process. The measured locking range of the designed 1/2 dual-ILFD is 692 MHz while that of the single-injection ILFD is 70 MHz, which demonstrates a significant improvement by a factor of almost 10. The designed core 1/2 dual-ILFD only consumes 2.93 mA 1.5 V supply voltage. With low power consumption and wide locking range, the proposed 1/2 dual-ILFD is attractive for various RF systems such as broadband PLL's requiring stringent power budget.

CHAPTER IV

A FULLY INTEGRATED 0.18- μm BiCMOS DIVIDE-BY-3 INJECTION-LOCKED FREQUENCY DIVIDER IMPLEMENTING PHASE TUNING TECHNIQUE

1. Introduction

Frequency divider is used in phased-lock loops (PLL) and frequency synthesizers to compare LO signal with a reference signal. Generally, the frequency of the LO signal is much higher than that of the reference signal and therefore needs to be divided until it is the same as the reference signal's frequency. Among the different types of frequency divider, the injection-locked frequency divider (ILFD) is becoming more popular due to its low power and high frequency characteristics.

One of the most important metrics of the ILFD is the 'locking range', which basically defines a range over which a frequency-division operation is supported. Various attempts have been made to increase the locking range such as increasing the injection signal level [31], lowering the output amplitude [42], reducing the quality factor of the LC resonator [43], using an additional injection signal [32, 33], etc. These approaches provide the injection signals using external sources with large power. In fully integrated ILFD's for PLL's, an internal VCO is used to supply the injection signal. This VCO typically has limited output power and hence enhancing the locking range with large injection signal power poses difficulty.

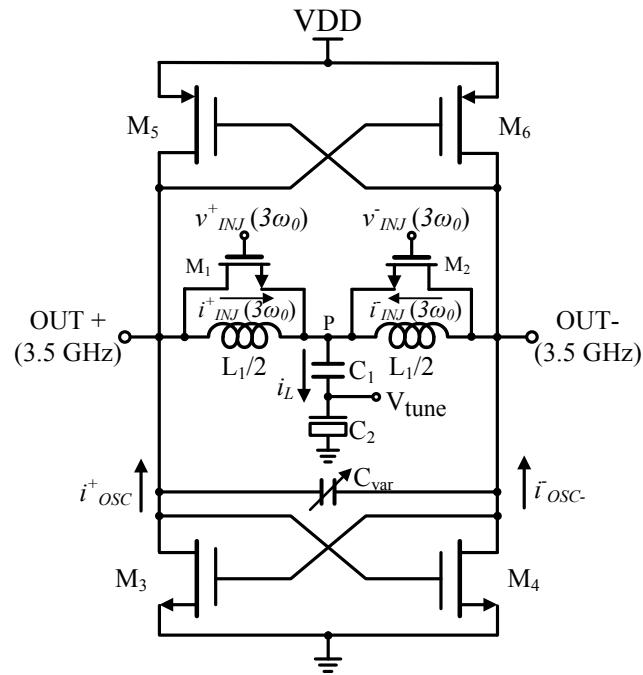
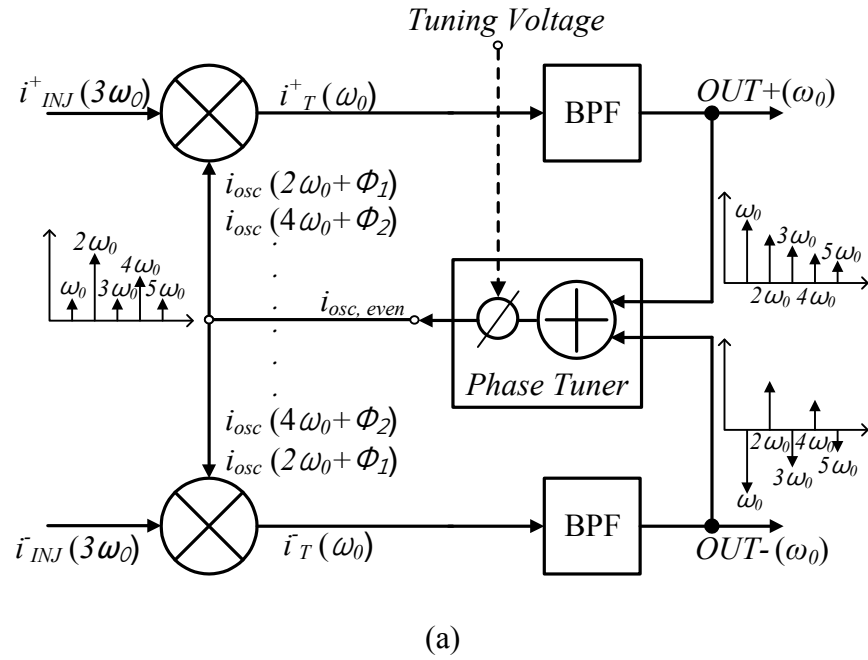


Fig. 4.1(a) Block diagram model and (b) circuit schematic of the integrated divide-by-3 ILFD.

In this chapter, we report the development of a fully integrated 0.18- μm BiCMOS 3.5-GHz divide-by-3 ILFD with enhanced locking range using a small-power injection source. The locking range is enhanced by implementing a phase-tuning concept. The injection source is provided by an internal 10.5-GHz VCO having only -18 dBm output power. This power level is significantly lower than that used in [31-33] and [42, 43], presenting a more realistic and practical solution to complete on-chip implementations.

2. Circuit Design and Analysis

Fig. 4.1(a) shows the block diagram that models the proposed divide-by-3 ILFD. The differential injection signals (i_{INJ}^+ and i_{INJ}^-) having frequency of $3\omega_o$ are applied to the mixers. After passing through the band-pass filter (BPF), which models an LC resonator, the differential signals at oscillating frequency ω_o and its harmonic components are generated at the output. Since the even harmonics are in-phase and odd harmonics are 180° out-of-phase in the differential signals, the differential outputs are summed to generate even-order harmonics (mainly $2\omega_o$) for the divide-by-3 operation.

Fig. 4.1(b) shows the circuit schematic of the proposed 1/3 ILFD. The transistor pairs M_3/M_4 and M_5/M_6 form a complementary cross-coupled oscillator. The transistors M_1 and M_2 are connected in parallel with each section of the asymmetric inductor ($L/2$) for mixing operation and, along with the MOSFET varactor C_2 , provide the phase tuning needed for enhanced locking range as described later. The variable capacitor (C_{var})

across the outputs is formed using a varactor and capacitor bank for frequency-tuning purpose.

The differential output currents of the ILFD across the asymmetric inductor can be expressed as

$$\begin{aligned} i^+_{osc} &= f(+V) = aV + bV^2 + cV^3 + dV^4 + eV^5 + \dots \\ i^-_{osc} &= f(-V) = -aV + bV^2 - cV^3 + dV^4 - eV^5 - \dots \end{aligned} \quad (4.1)$$

where a, b, c, d, and e are real constant coefficients and $V = \text{VOUT}^+ = -\text{VOUT}^-$ at the OUT+ and OUT- ports, respectively. Since the differential currents in (4.1) are added at node P, the total current at node P is obtained as

$$i_L = 2bV^2 + 2dV^4 + \dots \quad (4.2)$$

which shows that only even-order harmonics exist at node P. These signals mix with the injection signal to provide the divide-by-3 function; hence not only the frequency, but also the locking range, of the 1/3 ILFD depend on the even harmonics.

We now introduce a concept of phase tuner, through which the phase of the even-harmonic components is adjusted to enhance the locking range. Fig. 4.2(a) shows the phase tuner used in the 1/3 ILFD seen in Fig. 4.1(b). It is connected in parallel with the varactor (C_{var}) as seen in Fig. 4.1(b) to form an equivalent LC resonator across the differential outputs. M_1 and M_2 together with C_2 are used for tuning the phase of the resonator. The fixed MIM capacitor (C_1) is used for DC block when C_2 is controlled using a bias voltage.

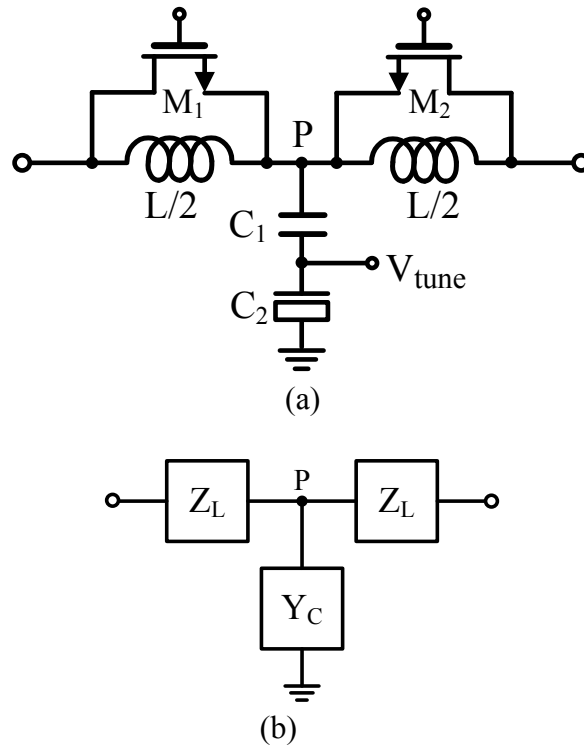


Fig. 4.2(a) Phase tuner and (b) its equivalent model.

Fig. 4.2(b) shows an equivalent model of the phase tuner where Z_L represents the impedance of the combined $L/2$ and parasitic capacitance of M_1 (or M_2) and Y_C represents the total admittance of C_1 and C_2 . Assume perfect match ($S_{11}=S_{22}=0$), the [ABCD] matrix of the equivalent model can be derived as

$$\begin{aligned} \begin{bmatrix} A & B \\ C & D \end{bmatrix} &= \begin{bmatrix} 1 & Z_L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/Z_C & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_L \\ 0 & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1+Z_L Y_C & Z_L(2+Z_L Y_C) \\ Y_C & 1+Z_L Y_C \end{bmatrix} \end{aligned} \quad (4.3)$$

where $Z_L = j\omega L/Z_0 = jX_L$ and $Y_C = j\omega C Z_0 = jB_C$ with Z_0 assumed to be the characteristic impedance of the terminating transmission line, X_L being the inductive reactance, B_C

being the capacitive susceptance, and L and C representing the equivalent inductance and capacitance, respectively. Eqn. (4.3) is calculated from cascaded ABCD-parameters.

We have from the conversion table:

$$\begin{aligned}
 A &= \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} \\
 B &= Z_0 \frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \\
 C &= \frac{1}{Z_0} \frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} \\
 D &= \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}}
 \end{aligned} \tag{4.4}$$

With an assumption that $S_{11}=S_{22}=0$ (perfect matching case), $A=D$ and $B \neq C$ as seen in (4.4). From Equation (4.4), when $S_{11}=S_{22}=0$, $B=CZ_0^2$, which upon substituting into (4.3) gives $Z_L(2+Z_L Y_C)=Y_C Z_0^2$, which can be re-written as

$$B_C = \frac{2X_L}{Z_0^2 + X_L^2} \tag{4.5}$$

From ABCD-parameter, we can derive

$$\begin{aligned}
 S_{21} &= \left[\frac{2}{A + B/Z_0 + CZ_0 + D} \right] \\
 &= \left[\frac{2}{A + CZ_0 + CZ_0 + D} \right] \\
 &= \left[\frac{2}{2(1 + Z_L Y_C + Y_C Z_0)} \right] \\
 &= \left[\frac{1}{1 - X_L B_C + jB_C Z_0} \right]
 \end{aligned} \tag{4.6}$$

from which the phase of S_{21} can be obtained as

$$\varphi = \angle S_{21} = \tan^{-1} \left[\frac{-B_C Z_0}{1 - X_L B_C} \right] = \tan^{-1} \left[\frac{-2X_L Z_0}{Z_0^2 - X_L^2} \right] \quad (4.7)$$

making use of (4.5). Using $\tan(2\varphi) = 2\tan(\varphi)/(1 - \tan^2 \varphi)$, we can obtain from (4.7):

$$X_L = -Z_0 \tan\left(\frac{\varphi}{2}\right) \quad (4.8)$$

L can then be derived from (4.8) as

$$L = -\frac{Z_0^2}{\omega} \tan\left(\frac{\varphi}{2}\right) \quad (4.9)$$

Substituting (4.8) into (4.5) and utilizing $B_C = \omega C Z_0$, we get

$$C = -\frac{1}{Z_0^2 \omega} \sin(\varphi) \quad (4.10)$$

making use of $1 + \tan^2(\varphi/2) = \sec^2(\varphi/2)$. Finally, substituting (4.9) and (4.10) into (4.7) yields

$$\varphi = \tan^{-1} \left(\frac{\omega C Z_0^2}{\omega^2 L C - 1} \right) = \tan^{-1} \left(\frac{2\omega L Z_0^2}{\omega^2 L^2 - Z_0^4} \right) \quad (4.11)$$

Eqn. (4.11) shows that the phase of the phase tuner, and hence the LC tank, can be changed by varying the capacitance (through the MOSFET varactor C_2) and/or the inductance (by adjusting the gate bias of transistors M_1 and M_2). Inductance tuning using a fixed inductor in parallel with an NMOS transistor was used for VCO [36]. The phase-tuning of the phase tuner can be exploited to enhance the locking range of the ILFD.

The enhancement in locking range can be visualized using a phase diagram between i_{OSC} and i_{INJ} as shown in Fig. 4.3. Maximum locking range can be achieved

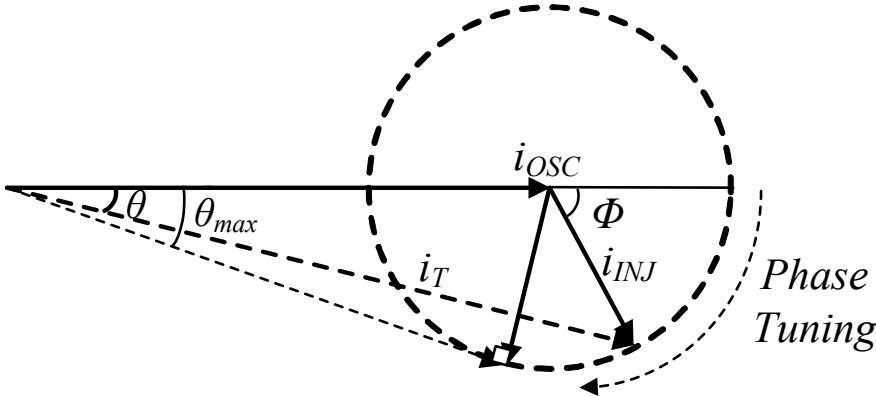


Fig. 4.3 Phase diagram between currents in the integrated ILFD.

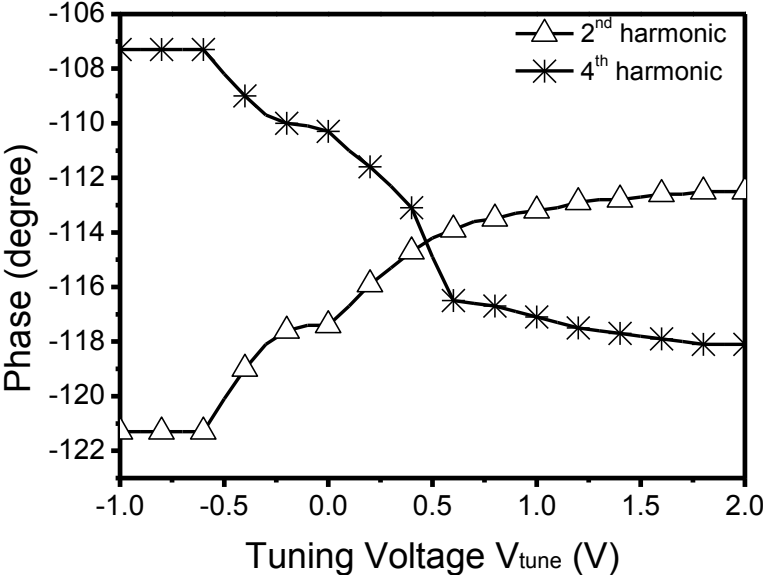


Fig. 4.4 Phase of the 2nd and 4th harmonic.

when the angle between the total current (i_T) and injection current i_{INJ} is 90° corresponding to $\theta_{max} = \arcsin(i_{INJ}/i_{OSC})$ [31]. The phase diagram suggests that the locking range under a fixed injection power can be increased by adjusting the angle Φ such that the angle θ between i_T and i_{INJ} moves toward 90° . This implies that i_{INJ} must be comparable to i_{OSC} , or large power must be injected, in order to increase the locking range. When i_{INJ} is smaller than i_{OSC} , or the injection power is small, θ is much smaller than θ_{max} and hence the resultant locking range is very narrow. In practice, the injection power is typically small, thereby posing difficulty in enhancing the locking range by simply relying on changing the angle Φ according to Fig. 4.3.

To overcome the above-mentioned problem of narrow locking range with a small injection power, the phase tuning of the even-order harmonics is implemented using the phase tuner to enhance the locking range. Fig. 4.4 plots the phase variation of the 2nd and 4th harmonic occurring at node P in Fig. 4.1(b) when V_{tune} is tuned from -1 V to 2 V. Over the tuning range of -1 to 2 V, about 10° of phase tuning for the 2nd and 4th harmonic can be achieved. This phase tuning capability can enhance the locking range as evidenced in the measurement results.

3. Measurement Results

Fig. 4.5 shows the block diagram of the integrated divider consisting of a 10.5-GHz VCO, divide-by-3 ILFD core, and output buffer. The internal 10.5-GHz VCO is used to provide the injection source. The output of the divide-by-3 ILFD core is

connected to the inverter buffer, which reduces the loading effect on the output impedance of the ILFD and improves the isolation between the ILFD and output pads.

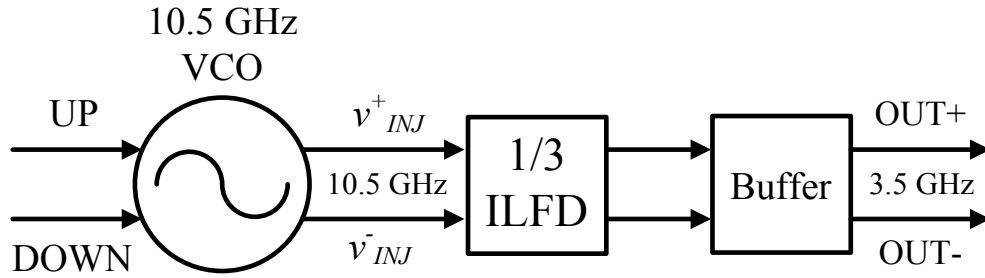


Fig. 4.5 Integrated ILFD with constituent components.

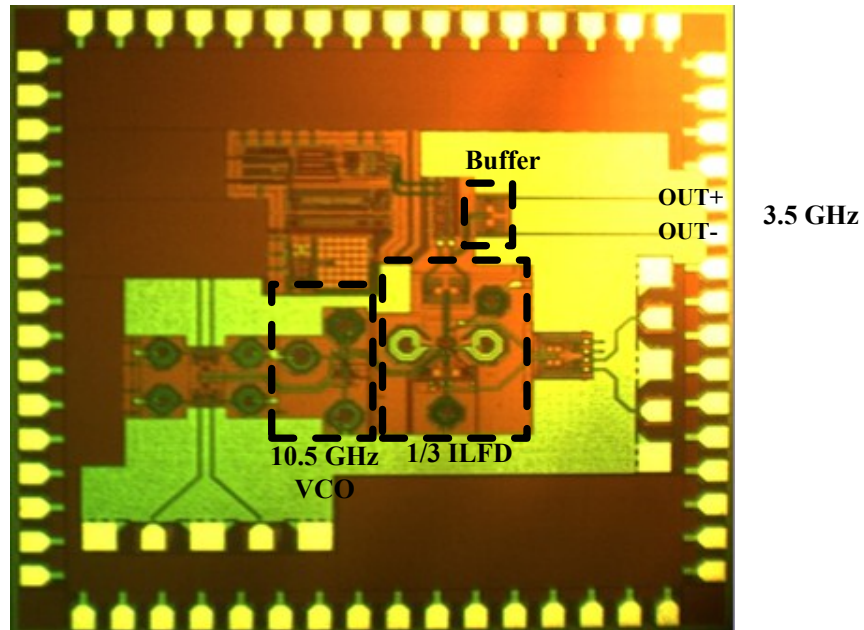


Fig. 4.6 Die photograph of the integrated 1/3 ILFD. Size: 2mm^2 (with pads), 0.42mm^2 (without pads) for 1/3 ILFD chain, 0.25mm^2 (without pads) for 1/3 ILFD core.

The integrated 1/3 ILFD was fabricated in Jazz 0.18- μm BiCMOS process [40] and a die photograph is shown in Fig. 4.6. The entire integrated 1/3 ILFD measures 0.42 mm^2 while the 1/3 ILFD core occupies 0.25 mm^2 . The power consumption of the integrated 1/3 ILFD including the VCO is 19.1 mW, while the ILFD core alone consumes 11.18 mW with a supply voltage of 1.8 V. The measurement was done on-wafer at the output of the inverter buffer using a spectrum analyzer.

Fig. 4.7 shows the frequency tuning characteristics of the integrated 1/3 ILFD as a function of the control voltage of the MOSFET varactor C_{var} . The frequency changes from 3.21 to 4.18 GHz as the control voltage is tuned from 0 to 1.8 V. Fig. 4.8 shows the locking characteristics of the integrated 1/3 ILFD as the frequency of the injection signal is varied. As one-third of the frequency of the injection source ($\omega_i/3$) approaches the desired output frequency (ω_o), the output of the integrated 1/3 ILFD moves from an unlocked state to a weakly locked state and then finally a locked state, verifying the divide-by-3 operation and frequency locking. Fig. 4.9 plots the locking range for different tuning voltage V_{tune} . The locking range is 12 MHz without phase tuning ($V_{\text{tune}} = -1.6$ V) and reaches 15 MHz when the phase is tuned ($V_{\text{tune}} = -0.6$ V), representing an increase of 25%. The package of design chip uses the 64-pin QFP type and all bias are connected to the chip through wire-bonding on the package mounted on FR-4 PCB as shown in Fig. 4.10.

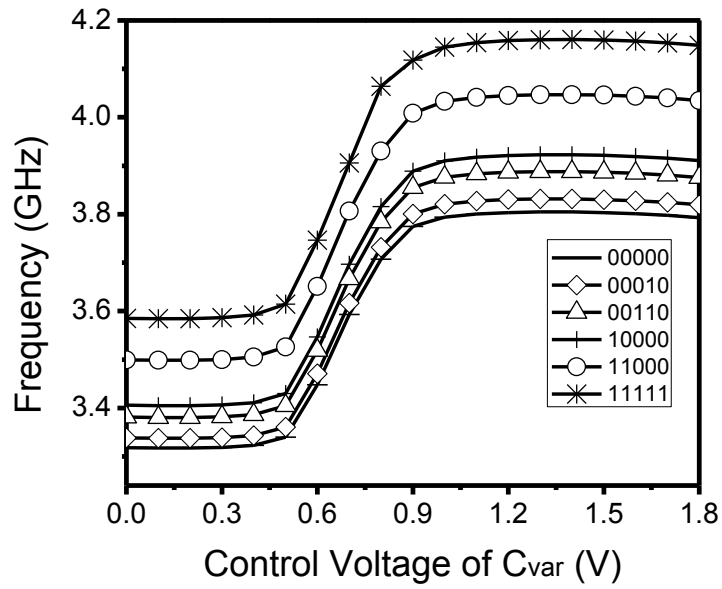


Fig. 4.7 Measured free-running frequency tuning range of the integrated 1/3 ILFD with 5-bit digital control.

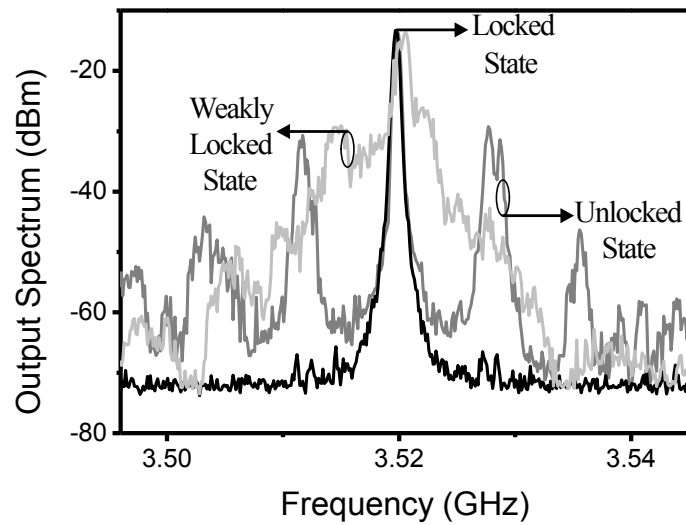


Fig. 4.8 Measured output spectrum in locked and unlocked states.

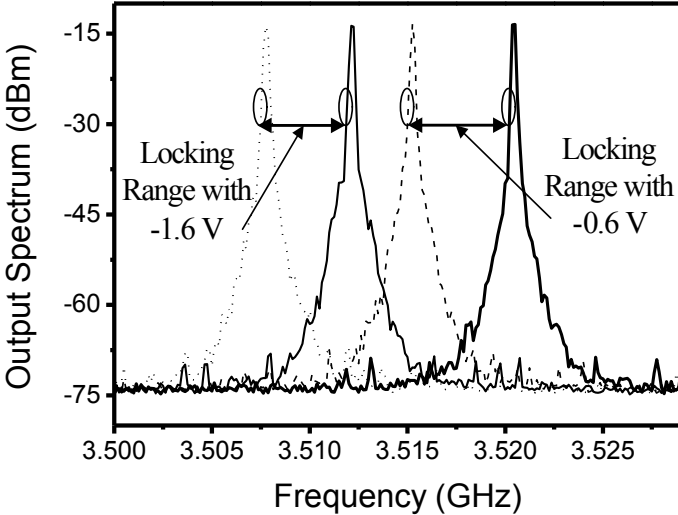
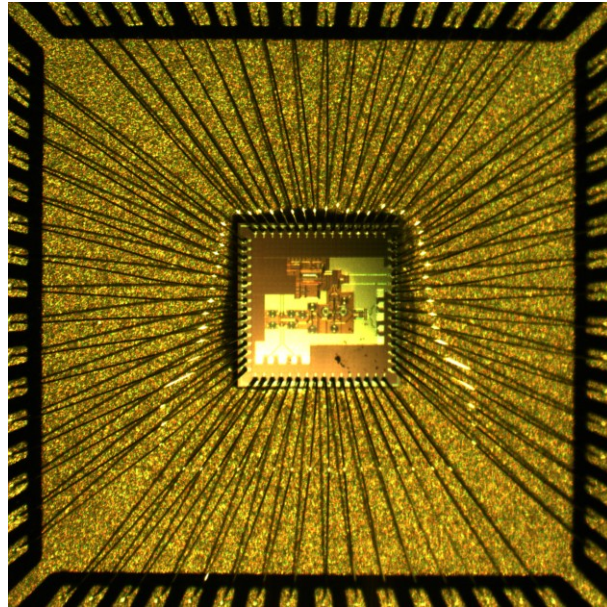
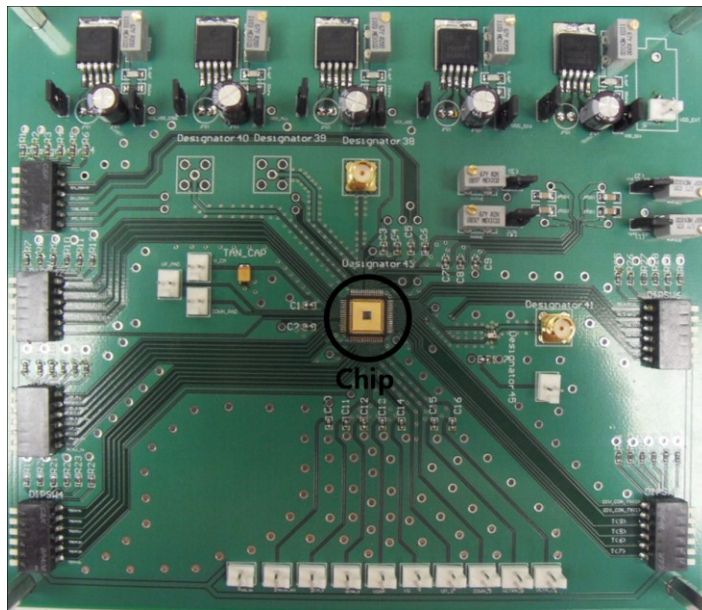


Fig. 4.9 Measured locking range for different phase tuning.



(a)



(b)

Fig. 4.10 Microphotograph of the designed 1/3 ILFD (a) packaged chip mounted on FR-4 PCB (b).

4. Conclusion

A fully integrated 3.5-GHz divide-by-3 ILFD having enhanced locking range with a very small injection power has been designed and fabricated in Jazz 0.18- μm BiCMOS process. A phase tuner implemented with an asymmetric inductor was proposed to achieve the divide-by-3 function and increased locking range. With an injection power of only -18 dBm, the integrated ILFD shows a 25-percent improvement in locking range without consuming additional power. Achieving enhanced locking ranges with a relatively small power injection source provided by an internal on-chip VCO is attractive for fully integrated PLL and synthesizers.

CHAPTER V
NEW DIVIDE-BY-3 INJECTION LOCKED FREQUENCY DIVIDER UTILIZING
SELF-INJECTION TECHNIQUE

1. Introduction

Injection-locked frequency divider (ILFD) receives significant interests for frequency dividing functional in PLL's and frequency synthesizer since it can operate at high frequencies while consuming low power. Specifically, differential structure based on LC resonator is widely used for its good phase noise. The differential structure has inherent even-order harmonic rejection and hence is advantageous for even-number division. However, this also implies that the differential structure is ill-suited for efficient odd-number division since the even-order harmonic power is inherently very small, thus resulting in a significant reduction in the injection efficiency and locking range. Therefore, a new technique should be employed to enhance the efficiency of the odd-number division and the locking range for the differential ILFD.

Several differential divide-by-3 ILFDs have been developed to increase the locking range [45]-[48]. In [45], a single-ended injection signal with four series inductors across the differential outputs is utilized to enable a high load-impedance for the 3rd harmonic. The work in [46] applies the differential injection signal through the bulk terminal of two PMOS constituting a negative- g_m cell. The linear mixer technique is proposed in [47] that results in a linear relationship between the injection signal and the output signal with increased locking range. In [48], a series injection is used and the

injection device is operated as a nonlinear mixer. All of these approaches, however, increase the locking range with large injection power and, therefore, are not very suitable when an ILFD is integrated within the same chip of PLL's or frequency synthesizer. For more integration suitability, an ILFD needs to provide a wide locking range with minimal injection signal power.

In this chapter, a divide-by-3 ILFD using self-injection, implemented by an odd-to-even mode converter, feedback amplifier (FB-AMP) and mixer, to enhance the locking range, phase noise and input sensitivity is presented. The 1/3 ILFD was designed

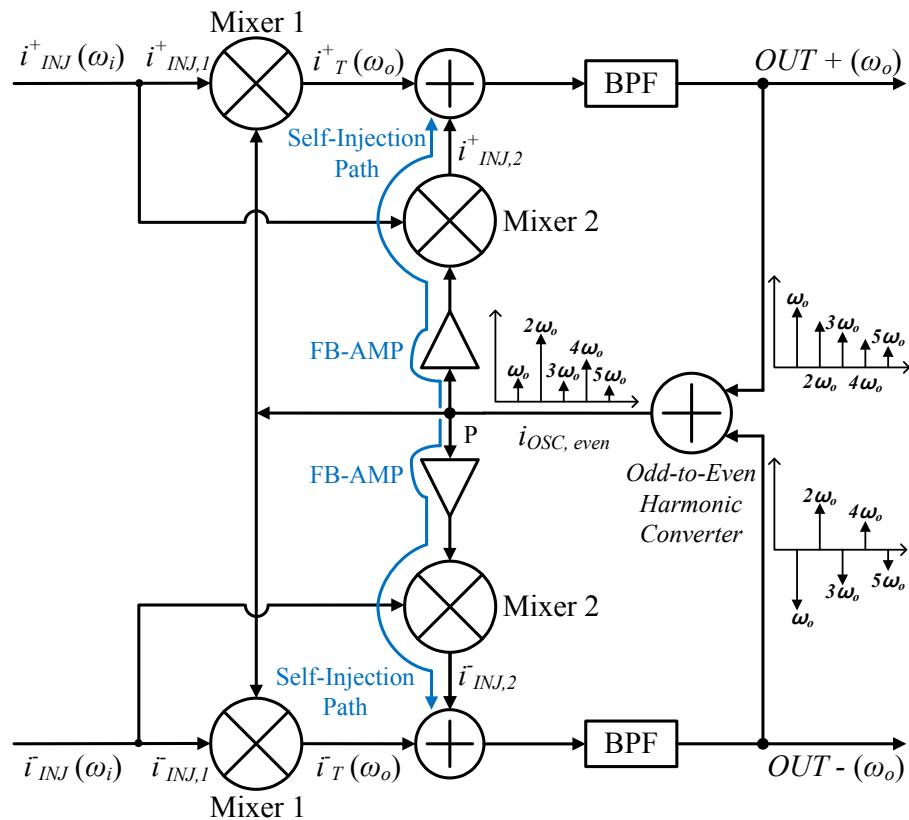


Fig. 5.1 Block diagram of the proposed divide-by-3 ILFD.

using a 0.18- μm BiCMOS process and achieves significant performance improvement as compared to that without self-injection.

2. Circuit Design and Analysis

Fig. 5.1 shows the conceptual block diagram of the new divide-by-3 ILFD. A differential injection signal at $3\omega_0$ is applied as input to both mixer 1 and mixer 2. To facilitate an efficient divide-by-3 operation, an odd-to-even harmonic converter is used

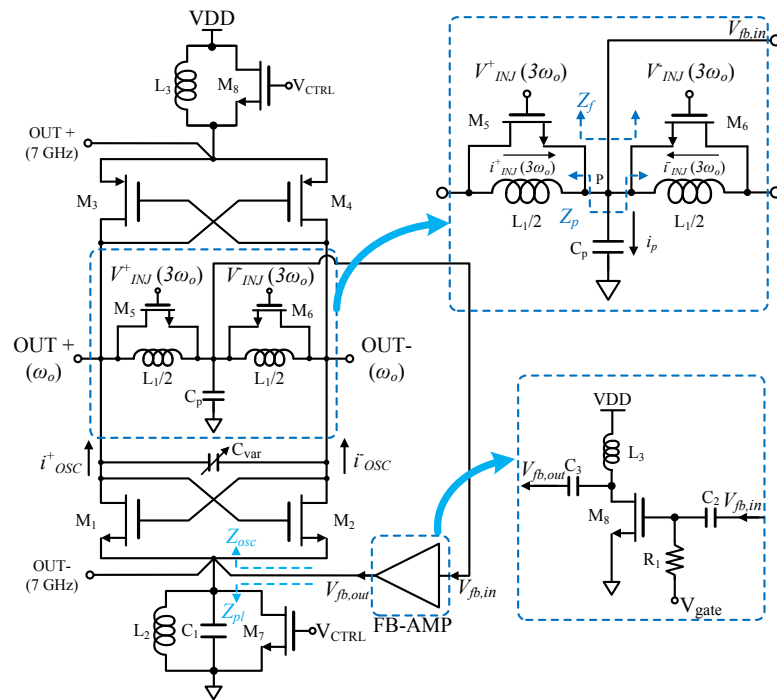


Fig. 5.2 The schematic of the proposed divide-by-3 ILFD.

to provide even-order harmonics (mainly $2\omega_0$) from differential signals at ω_0 . To increase the locking range of the ILFD and enhance the minimum sensitivity, a feedback path is created through the feedback amplifier followed by mixer 2. The amplified self-injection signal at $2\omega_0$ through the auxiliary feedback path mixes with the main injection signal at $\omega_i=3\omega_0$ in mixer 2 to produce an amplified signal at ω_0 . The resultant signal is then added to the output of mixer 1 and band-pass filtered through the LC resonator tuned at ω_0 to obtain the desired fundamental signal.

The circuit schematic of the proposed 1/3 ILFD with an auxiliary self-injection technique is shown in Fig. 5.2. The output LC tank is composed of a T-network with two series inductors tapped at the center by a shunt capacitor (C_p), and a varactor capacitor (C_{var}) in parallel with the output. The T-network combines two differential signals and produces only even harmonics, hence effectively functioning as an odd-to-even harmonic converter to convert the odd-order harmonics available at the differential output to the even-order harmonics at node P. Transistors M_5 and M_6 are connected in parallel with the two series inductors for main differential injection.

The feedback amplifier is utilized for the auxiliary self-injection and placed between node P and the common-source node of the NMOS cross-coupled pair (M_1 and M_2) to increase the locking range and improve the minimum input sensitivity. The locking range of an ILFD was derived analytically as [31]

$$\omega_i - \omega_o = \frac{\omega_o}{2Q_L} \cdot \frac{i_{INJ}}{\sqrt{i_{OSC}^2 - i_{INJ}^2}} \quad (5.1)$$

where i_{INJ} and i_{OSC} are the injection and oscillation currents, respectively. As can be seen, the locking range can be increased by adjusting i_{INJ} as well as i_{OSC} . Under a fixed i_{OSC} , the injection current (i_{INJ}) can be adjusted up to i_{OSC} to enhance the locking range. However, the injection signal level is limited when it is supplied by an on-chip VCO integrated within the ILFD, thus hindering the locking-range enlargement. Using the auxiliary self-injection technique, significantly lower injection signal level can be used due to the boosted second-harmonic signal, making possible an enhancement of the locking range even with a small injection signal.

The total injection signal can be defined as $i_{INJ} = i_{INJ,1} + i_{INJ,2}$, where $i_{INJ,1}$ is the injection signal from an external source, $i_{INJ,2}$ is the auxiliary self-injection signal, $i_{INJ} = i_{INJ}^+ + \bar{i}_{INJ}$, $i_{INJ,1} = i_{INJ,1}^+ + \bar{i}_{INJ,1}$, and $i_{INJ,2} = i_{INJ,2}^+ + \bar{i}_{INJ,2}$. The AC signal at node P consists of mostly even-harmonic components and can be expressed as

$$V_{fb,in} = \frac{Z_p \cdot Z_f}{Z_p + Z_f} \cdot i_p \quad (5.2)$$

where Z_p is the impedance of T-network, Z_f is the input impedance of the feedback amplifier, and i_p is the total AC current flowing into the node P. $V_{fb,in}$ is the feedback amplifier and injected into the common-source node of M_1 and M_2 .

Assuming the impedance of the resonator connected at the common-source node is finite, the output voltage of the feedback amplifier ($V_{fb,out}$), resultant self-injection current ($i_{INJ,2}$) and total injection current (i_{INJ}) can be derived as

$$V_{fb,out} = V_{fb,in} \cdot g_{m8} \cdot \frac{sL_3 \cdot Z_{pl}}{Z_{pl} \cdot Z_{osc} + sL_3(Z_{pl} + Z_{osc})} \quad (5.3)$$

$$i_{INJ,2} = \frac{2}{\pi} \cdot V_{fb,out} \quad (5.4)$$

$$i_{INJ} = i_{INJ,1} + \frac{2}{\pi} \cdot V_{fb,in} \cdot g_{m8} \cdot \frac{sL_3 \cdot Z_{pl}}{Z_{pl} \cdot Z_{osc} + sL_3(Z_{pl} + Z_{osc})} \quad (5.5)$$

where Z_{pl} is the impedance of the resonator at the virtual ground, Z_{osc} is the impedance looking into the cross-coupled pair, and g_{m8} is the transconductance of M_8 . Note that the constant $2/\pi$ in (5.4) is the effective conversion gain from $V_{fb,out}$ to $i_{INJ,2}$ [33]. It is noted from (5.5) that the total injection current is increased with the gain of the feedback amplifier (g_{m8}) and, therefore, the auxiliary self-injection technique enhances the locking range with the injection signal ($i_{INJ,1}$) fixed.

3. Phase Noise Analysis of ILFD

The phase noise of the self-injection ILFD is given by [49]-[53]:

$$\left| \delta\theta_{osc} \right|^2 = \frac{\left(\frac{\omega}{\omega_{3dB}} \right)^2 \left| \delta\theta_0 \right|^2}{\left(\frac{\omega}{\omega_{3dB}} \right)^2 + \rho^2 \text{COS}^2(\hat{\theta} - \hat{\theta}_{inj})} + \frac{\rho^2 \text{COS}^2(\hat{\theta} - \hat{\theta}_{inj}) \left| \delta\theta_{inj} \right|^2}{\left(\frac{\omega}{\omega_{3dB}} \right)^2 + \rho^2 \text{COS}^2(\hat{\theta} - \hat{\theta}_{inj})} \quad (5.6)$$

where the tilde ($\hat{\cdot}$) denotes a transformed or spectral variable, $\delta\theta_{osc}$ is the output phase fluctuation, ω is the frequency offset from the carrier, $\omega_{3dB} = \omega_0/(2Q)$ is the 3-dB bandwidth of the free-running oscillator's embedding circuit, ω_0 is the free-running frequency of the slaved oscillator, $\rho = A_{inj}/A$ is the injection signal amplitude (A_{inj}) normalized to the free-running signal amplitude (A), θ is the steady-state value of the output phase, θ_{inj} is the injection signal phase, $\left| \delta\theta_0 \right|^2$ represents the power spectral

density of the phase noise of the free-running oscillator, and $|\delta\theta_{inj}|^2$ is the phase noise of the injection signal into the oscillator. According to (5.6), the phase noise of an ILFD is that of the injection source near carrier frequency, and returns to its free-running noise for the noise offset frequency far from the carrier frequency [49].

As can be seen in (5.6), the phase noise of the ILFD is improved as ρ becomes larger, which implies that higher injection power results in better phase noise. However, the amplitude of an injection signal is limited when it is provided by an integrated source from a frequency synthesizer which typically has low power. In order to increase the injection power, the 1/3 ILFD using self-injection signal is used without an additional external source. By increasing the gain of the internal feedback amplifier, the total injection current to the ILFD is increased and hence the phase noise of designed 1/3 ILFD can be enhanced.

4. Measurement Results

The new 1/3 ILFD was fabricated in Jazz 0.18- μm BiCMOS process [40] and its die photograph is shown in Fig. 5.3. The total chip area is 2.2mm^2 while the 1/3 ILFD core occupies only 0.048mm^2 . Using different capacitor arrays and control voltages, the designed 1/3 ILFD can achieve (output) frequency tuning from 3.47-4.313 GHz as shown in Fig. 5.4. Correspondingly, the locking frequencies with respect to the input signal are from 10.41 to 12.94 GHz, representing a 21.7 % locking range. The measured (input) locking range as a function of the control voltage VDD of the feedback amplifier for a fixed capacitor array is shown in Fig. 5.5.

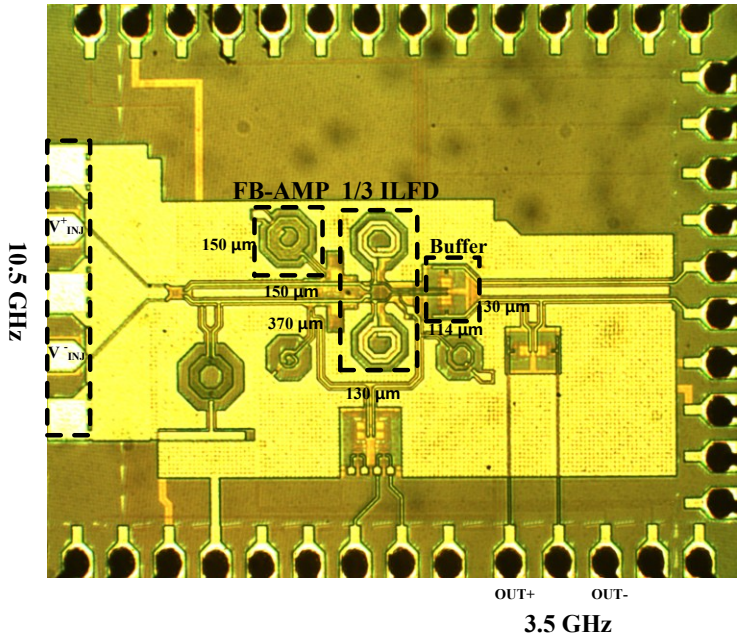


Fig. 5.3 Die photograph of the proposed 1/3 ILFD chain with gain-boosted amplifier.

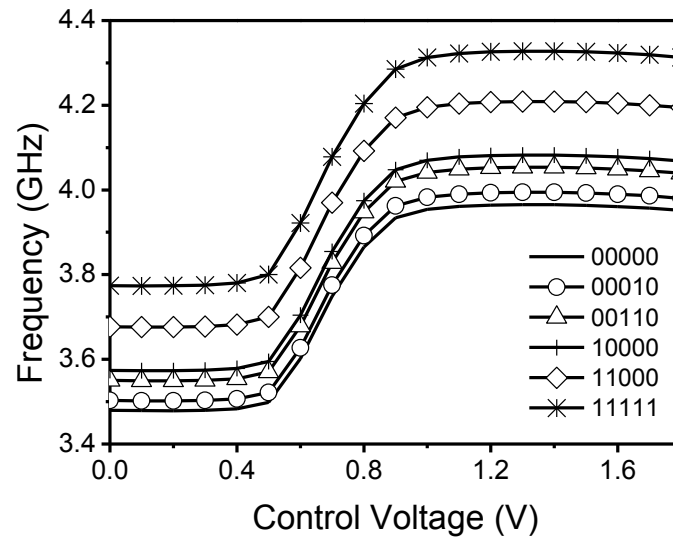


Fig. 5.4 Measured frequency tuning range vs. varactor control voltage for different capacitor arrays as noted in the digital codes.

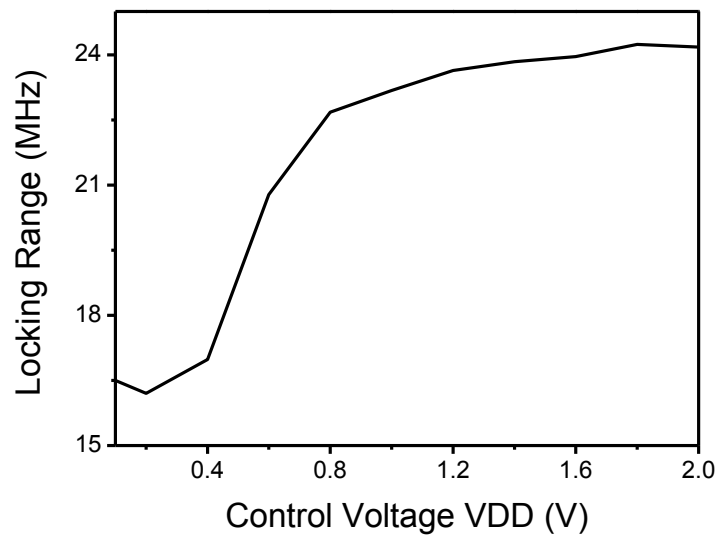


Fig. 5.5 Measured locking range vs. control voltage VDD of feedback amplifier under fixed capacitor array at 00110.

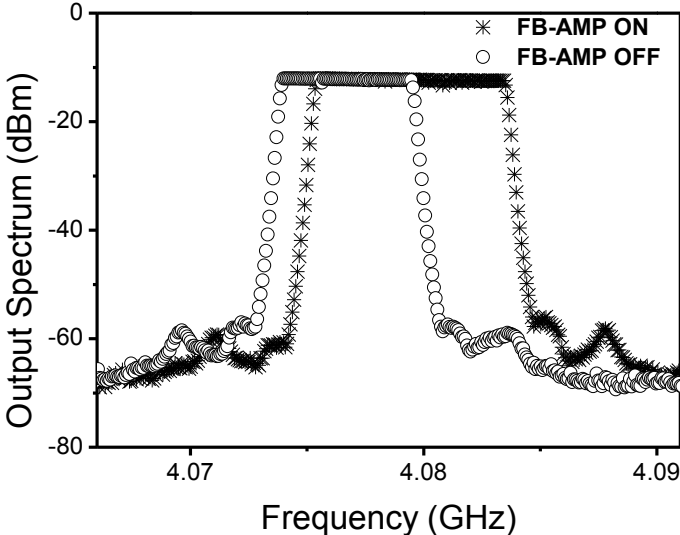


Fig. 5.6 Measured locking range for fixed capacitor array at setting 00110.

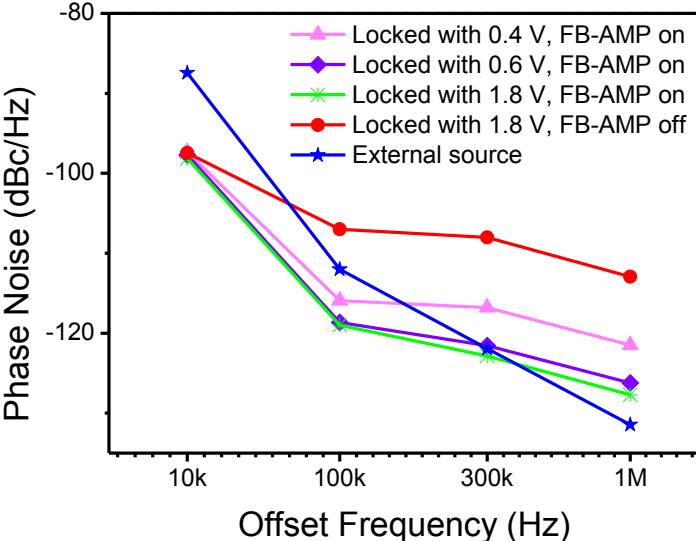


Fig. 5.7 Measured phase noise under fixed capacitor array at 00110.

Fig. 5.6 shows the measured output spectrum with an injection power of only -12 dBm and the feedback amplifier being turned on and off, showing that the (input) locking range extends as much as 47.8 % from 16.4 MHz under the amplifier's off-state (no self-injection) to 24.24MHz under the amplifier's on-state (with self-injection). The phase noise is enhanced as well for reasonable values of the control voltage V_{DD} (0.4~1.8 V), where the transistor M_8 of the feedback amplifier is operated in the saturation region. Fig. 5.7 shows the measured phase noise for different control voltages in comparison with the phase noise of the external source used for the injection signal.

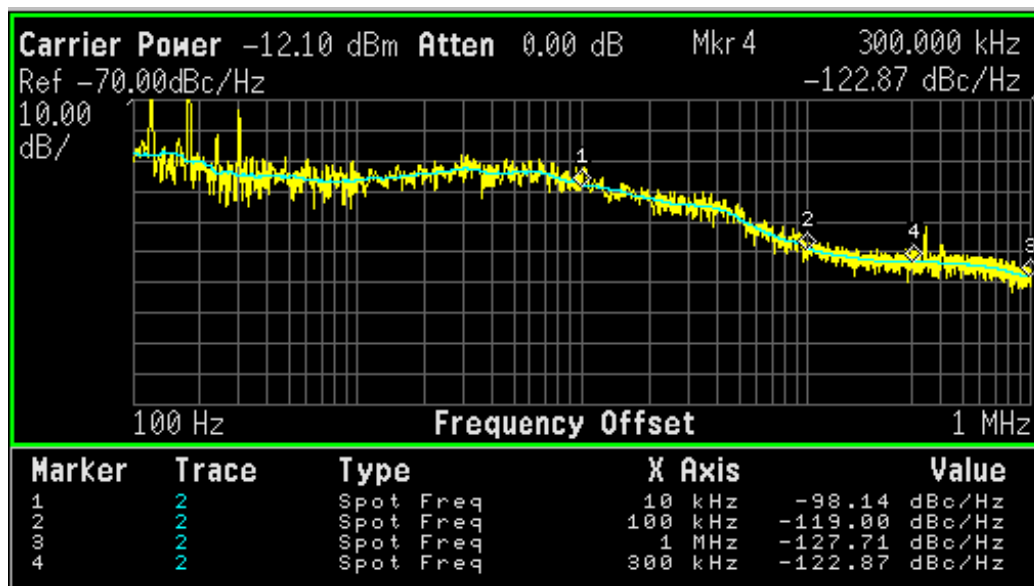


Fig. 5.8 Measured phase noise with feedback amplifier ON at 1.8-V control voltage for fixed capacitor array at 00110.

The measured phase noise for 1.8-V control voltage with the feedback on is depicted in Fig. 5.8. The phase noise at 1MHz offset is -127.71dBc/Hz and its enhancement is 14.77 dB compared to that of the 1/3-ILFD with the feedback amplifier off as shown in Fig 5.9. The designed 1/3 ILFD attains a minimum input sensitivity below -30 dBm for the injection signal which is significantly lower than those previously reported in [4-6] and [30]. The power consumption is 18.2mW from 1.8V supply.

The free-running phase noise of -105.53 dBc/Hz at 1 MHz offset with FB_AMP on is shown in Fig. 5.10 and -103.99 dBc/Hz at 1 MHz offset with FB_AMP off is shown in Fig. 5.11. The external injection source has -131.46 dBc/Hz at 1 MHz offset as shown in Fig. 5.12.

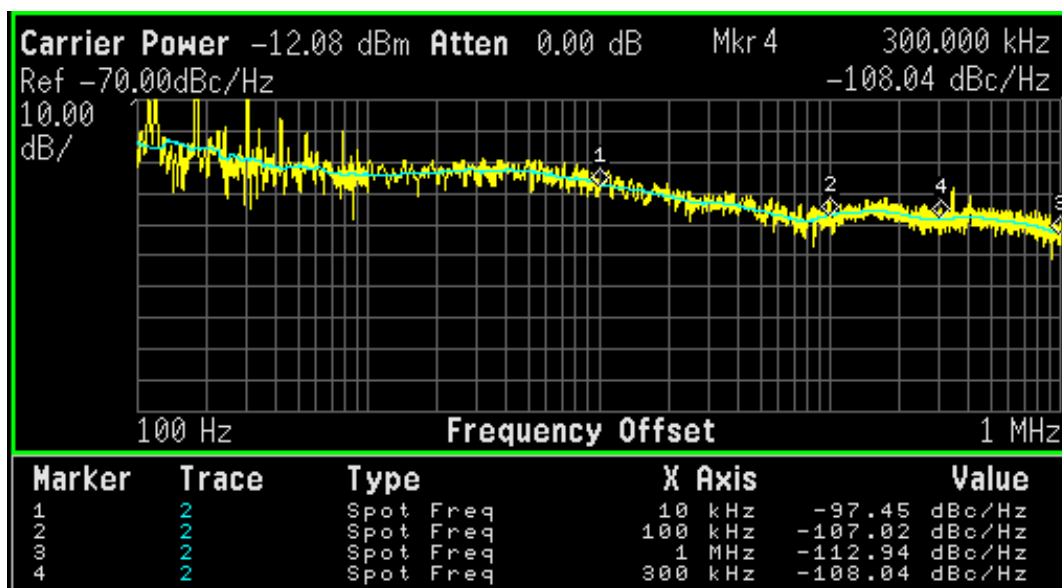


Fig. 5.9 Measured phase noise with feedback amplifier OFF at 1.8-V control voltage for fixed capacitor array at 00110.

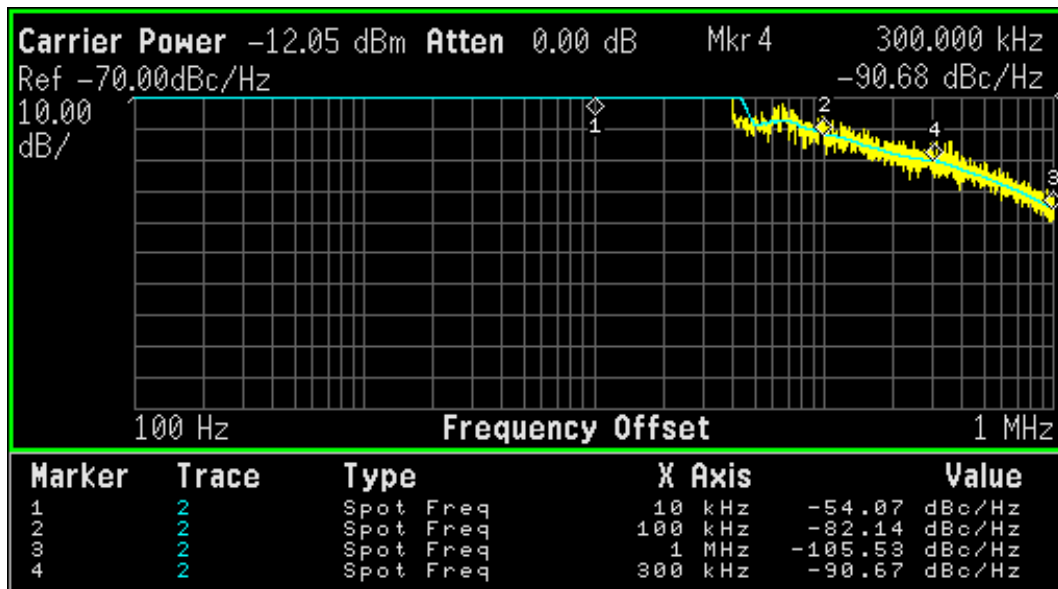


Fig. 5.10 Measured phase noise with feedback amplifier ON at 1.8-V control voltage for fixed capacitor array at 00110.

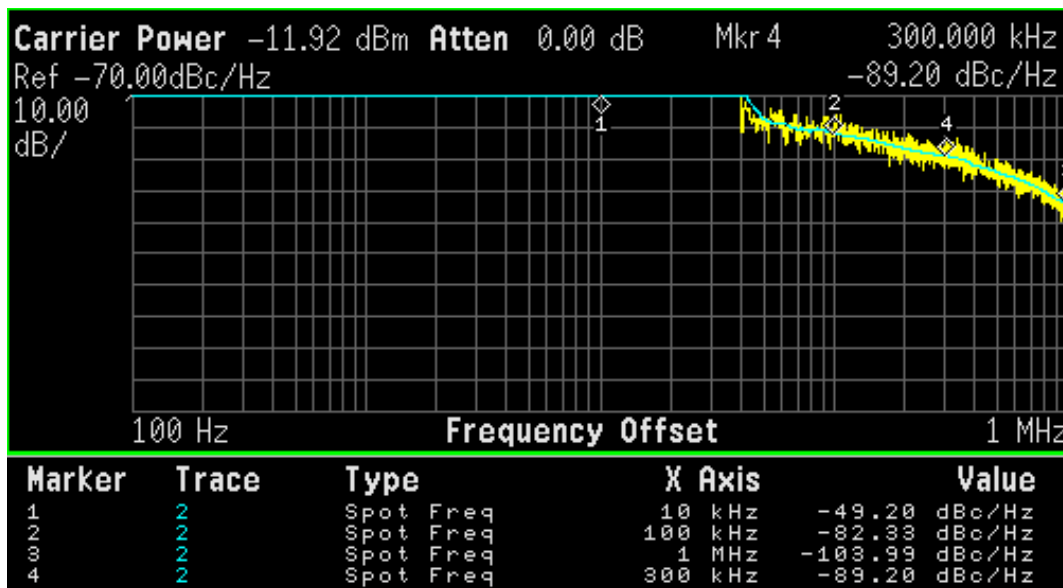


Fig. 5.11 Measured phase noise with feedback amplifier OFF at 1.8-V control voltage for fixed capacitor array at 00110.

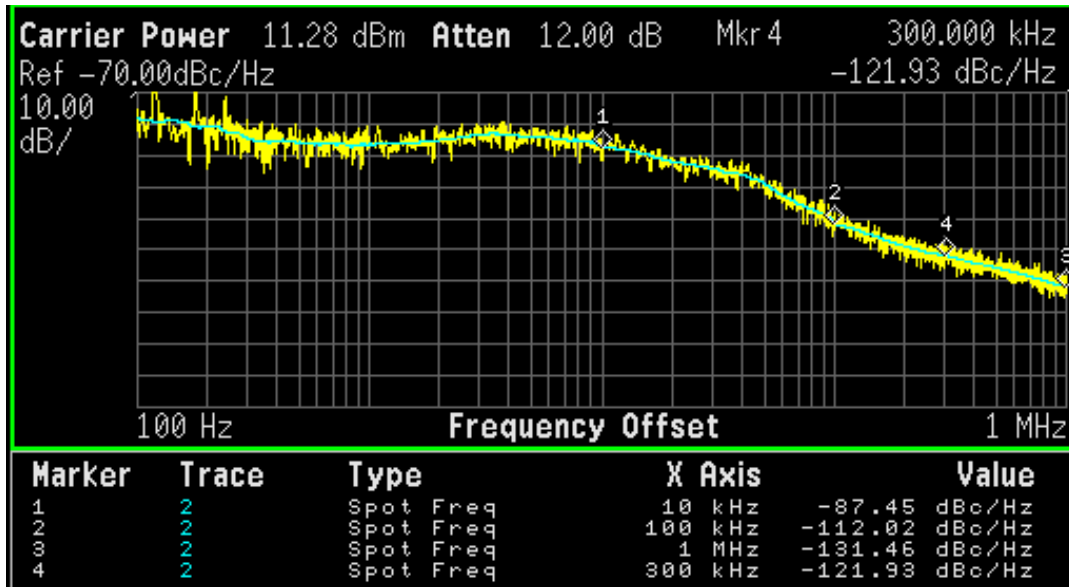
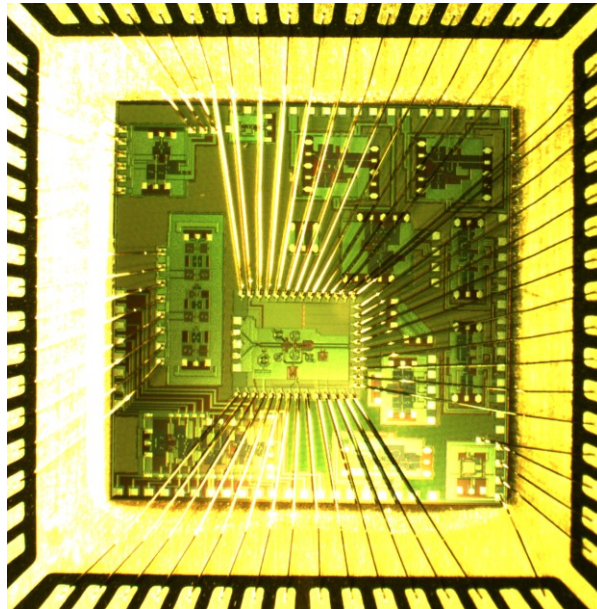
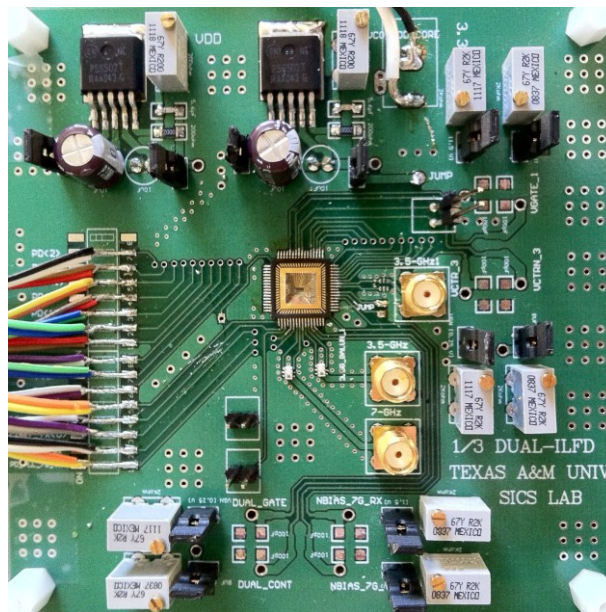


Fig. 5.12 Measured phase noise of the external 12.247 GHz injection source.



(a)



(b)

Fig. 5.13 Microphotograph of the designed 1/3 ILFD (a) packaged chip mounted on FR-4 PCB (b).

The package of design chip uses the 64-pin QFP type and all bias are connected to the chip through wire-bonding on the package mounted on FR-4 PCB as shown in Fig. 5.13.

5. Conclusion

A new divide-by-3 ILFD using self-injection technique is proposed and designed using CMOS in Jazz 0.18- μm BiCMOS process. The designed ILFD with self-injection helps enhance the locking range, phase noise and minimum injection sensitivity significantly as compared with no self-injection. With an injection power of only -12dBm, it achieves a locking-range enhancement of 47.8 %. The phase noise improvement is 14.77 dBc/Hz at 1 MHz offset, and the minimum input sensitivity attained is only -30 dBm. These characteristics make the developed ILFD well suited for PLL's and frequency synthesizers with low-power operation.

CHAPTER VI
A FULLY INTEGRATED MULTI-OUTPUT SYNTHESIZER FOR MULTI-BAND
MICROWAVE SYSTEMS

1. Introduction

Microwave systems working “concurrently” over multiple bands provide significant advantages and have more capabilities as compared to their single-band counterparts. Concurrent multiband systems allow communication and/or sensing to be performed at multiple frequencies simultaneously. To support these systems, concurrent multiband multi-output PLL’s are needed, particularly, fully integrated CMOS/Bi-CMOS PLL’s for complete systems on chips. Despite of their importance for systems, there were only few works reported on concurrent multiband PLL’s [54]-[56]. The PLL in [54] is implemented in a 0.25- μm SiGe BiCMOS process and uses two VCOs and a complex frequency divider chain consisting of many dividers to produce concurrent bands via the multiple dividers. The PLL in [55], an injection locked frequency divider (ILFD) and two VCOs are utilized to cover non-concurrent dual-band at 24 GHz and 77 GHz with a 0.18 μm BiCMOS process. The PLL in [56] use three VCOs and a multi-band ILFD in a 90-nm CMOS process to cover concurrent triple bands. These PLL’s employ multiple VCOs and frequency dividers to produce multiband concurrently. Use of multiple VCOs and frequency dividers results in challenging design for PLL’s and frequency dividers at high frequencies, especially under strict dc power constraints for single-chip systems.

ILFD is perhaps the most difficult component to design in PLL's, especially with wide locking ranges, and plays a crucial role in the PLL's performance. Several divide-by-3 (1/3) ILFDs for enhanced locking ranges have been developed [45]-[48]. In [45], a single-ended injection signal with four series inductors across the differential outputs is utilized to enable a high load-impedance for the 3rd harmonic. The work in [46] applies a differential injection signal through bulk terminal of two PMOS devices constituting a negative- g_m cell. A linear mixer technique is proposed in [47] that results in a linear relationship between the injection signal and the output signal with increased locking range. In [48], a series injection is used and the injection device is operated as a nonlinear mixer. All of these approaches increase the locking range using large injection power and, therefore, are not very convenient and/or easy to implement when the ILFD is integrated within the same chip of PLL's. Moreover, conventional ILFDs have fundamental problem in the locking process due to their fixed locking range. Lacking of tune-ability in the locking range makes these ILFDs not locked properly when the frequency of the input injected signal is outside the locking range of the ILFDs. Also, due to the narrow locking range of these ILFDs, the output of the frequency divider (prescaler) cannot easily determine the frequency of the injection source since the ILFD's are not locked with stability at the coarse-locking procedure. This results in increased locking time and poor phase noise with frequency mismatch between the reference frequency and the frequency of the divider. In the worst case, the ILFDs can lose the locking; either the coarse-locking or fine-locking cannot be achieved.

This chapter reports a fully integrated PLL capable of producing three simultaneous RF sources around 3.5, 7 and 21 GHz using 0.18- μm CMOS, except one buffer. The concurrent multiband multi-output PLL utilizes the self-injection technique proposed in chapter V for 1/3 ILFD to achieve enhancement as well as tune-ability for the locking range. A T-network resonator is employed to enable optimized differential outputs, leading to high 2nd order harmonic suppression. The developed PLL employs only one VCO, instead of multiple VCOs, to generate multiband, hence reducing possible unwanted cross-coupling between different VCOs, as well as chip size and power consumption. The tunable locking range provides better guaranty of locking states from coarse-locking to fine-locking as compared to a fixed locking range normally existed in PLL's. To the best of our knowledge, this is the first fully integrated CMOS PLL that provides concurrent tri-band tri-output using a single VCO and a single frequency divider with enhanced and tunable locking range, and enhanced 2nd harmonic suppression.

The chapter is organized as follows. Section 2 presents the limitations of conventional PLL using super-harmonic ILFD. Section 3 discusses the proposed locking mechanism for the super-harmonic ILFD. Section 4 shows the details of the circuit design in the proposed PLL. Section 5 shows the measurement results and section 6 gives the conclusions.

for coarse-locking. An injection signal (i_{INJ}) at frequency of $3\omega_o$ is applied to the mixer. Due to the nonlinearities of the mixer, inter-modulation products are generated between the injection signal ($3\omega_o$) and output signal (ω_o). After passing through the band-pass filter (BPF), only the desired signal (ω_o) can be acquired at the output. Switch 1 is disconnected and switch 3 is connected to the ILFD in order to adjust the frequency using a capacitor bank in the VCO at coarse-locking state (open-loop). Switch 2 is connected to the VCO to provide a fixed dc reference voltage of $0.5V_{DD}$ to the varactor in the VCO to set a certain $KVCO$. All the operations for switches 2 and 3 are determined in an open-loop state corresponding to the off-switch 1. To obtain a desired free-running frequency for the VCO, the output frequency of the VCO is calculated by counting the number of bits (f_{DIV}) at the output of switch 3 using the corresponding counter in the calibration block. $f_{DIV}=f_{VCO}/M(N+1)$ is under a coarse-locked state, where f_{VCO} is the VCO frequency and M and N are integers. The subsequent comparator then compares f_{DIV} with the reference signal's frequency f_{REF} and decides which one is faster.

Fig. 6.2 shows the timing diagram of the frequency comparison technique. It illustrates that f_{DIV} is counted during a time period of kt_{REF} , where $t_{REF}=1/f_{REF}$ and k is the number of the duration t_{REF} executed to achieve $f_{DIV}=f_{REF}$ which implies that a coarse-locked state has been reached. During kt_{REF} , the counter estimates whether f_{DIV} or f_{REF} is faster and controls the capacitor bank of the VCO to adjust f_{DIV} until a coarse-locked state is reached for the PLL. If this method is applied to the ILFD PLL, the VCO loses its coarse-locking. During the coarse-locking, the output frequency of the VCO may be set far away from a desired frequency. The locking range of a conventional ILFD is

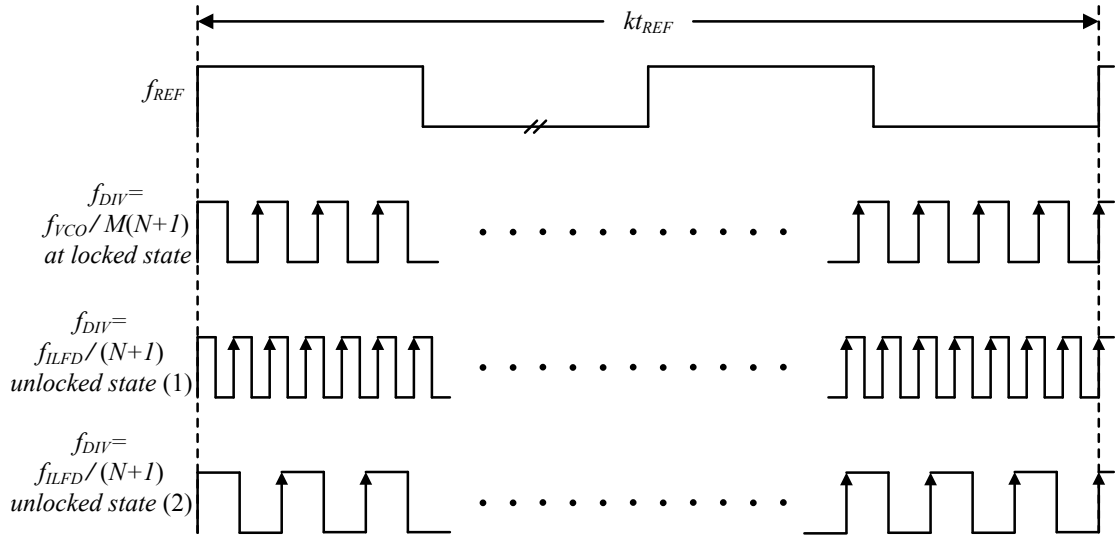


Fig. 6.2. Timing diagram of the frequency comparison technique in ILFD PLL.

typically very narrow with small injection power. The output of the ILFD hence does not follow the injection signal under an unlocked state. Possible frequency of the divider (f_{DIV}) that the counter provides during the time duration of kt_{REF} is given by

$$f_{DIV} = \frac{f_{VCO}}{kM(N+1)}, \quad \text{locked state} \quad (6.1)$$

$$f_{DIV} \neq \frac{f_{VCO}}{kM(N+1)}, \quad \text{unlocked state} \quad (6.2)$$

which shows that, under the locked state, f_{DIV} follows, and can be used to find, f_{VCO} in coarse-locking state. Under the unlocked state, f_{DIV} does not follow f_{VCO} since the ILFD is not locked with the injection source. Under the unlocked state, f_{DIV} is given by

$$f_{DIV} = \frac{f_{ILFD}}{k \cdot M} \quad (6.3)$$

where f_{ILFD} is the free-running frequency of ILFD, and f_{DIV} can be higher or lower than $f_{VCO}/M(N+1)$ as shown in Fig. 6.2.

Under the unlocked state, f_{VCO} cannot be recognized when it is out of the boundary of the ILFD's locking range. However, the output counter recognizes the frequency f_{DIV} given in (6.2), and it simply changes the capacitor bank in the VCO to vary f_{VCO} accordingly. The resultant f_{VCO} , however, may not be the desired frequency within the locking range due to the fact that it cannot be determined from f_{DIV} according to (6.2). This problem is more serious as the division ratio $(N+1)$ increases for high-order super-harmonic ILFD's due to low harmonic coefficients. Furthermore, if the output power of the VCO (injection signal power) is reduced, the narrow locking range problem becomes severe [31]. The proposed calibration technique and PLL described in Section 3 achieves enhanced and tunable locking range which helps minimize the problems of the conventional calibration technique.

3. Proposed Architecture and Calibration Mechanism for Super-Harmonic-ILFD PLL

Fig. 6.3 shows the block diagram of the proposed PLL with self-injection signal along with the calibration scheme. To increase the locking range, a self-injection technique is applied with additional power depending on the locking-range control. At the coarse-locking state, switch 1 is off and switches 2, 3 and 4 are on. The injection signal $i_{IN,2}$ from Mixer 2 is increased per the conversion gain of the mixer, hence helping extend the locking range.

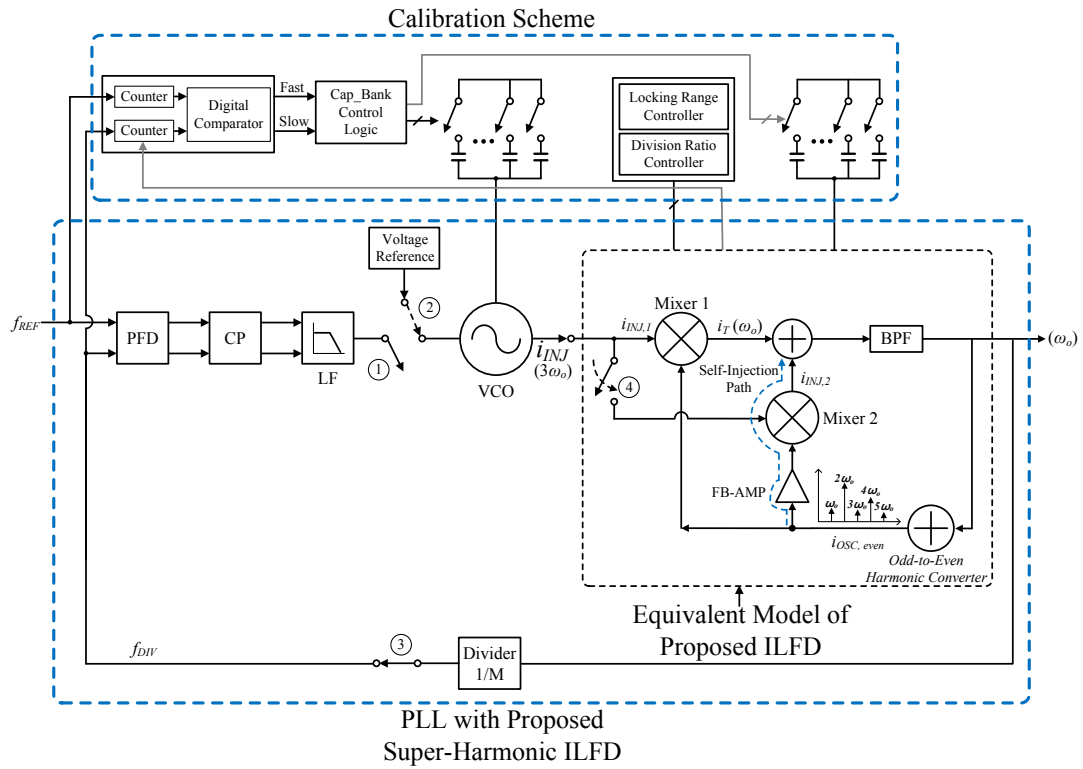


Fig. 6.3. Block diagram of the proposed ILFD PLL and calibration scheme for VCO frequency at coarse-locking.

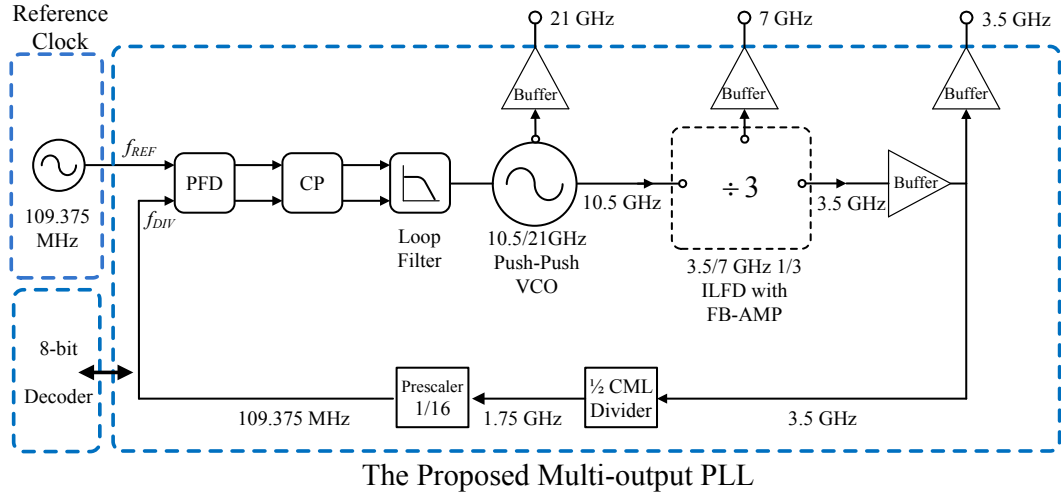


Fig. 6.4. Block diagram of the multi-output PLL integrating all, except the reference clock, on a single chip.

The locking range of an ILFD was derived analytically as [31]

$$\omega_{inj} - \omega_0 = \frac{\omega_0}{2Q_L} \cdot \frac{i_{INJ}}{\sqrt{i_{OSC}^2 - i_{INJ}^2}} \quad (6.4)$$

where i_{INJ} and i_{OSC} are the injection and oscillation current, respectively. Under a fixed i_{OSC} , the injection current can be adjusted to enhance the locking range until i_{INJ} is less than i_{OSC} and the constructive summation is ensured. However, the injection signal level is limited when it is supplied by an integrated VCO.

With the implemented auxiliary injection technique, the injection signal level can be significantly lower for super-harmonic ILFD due to the boosted injection signal. The injection signal can be defined as

$$i_{INJ} = i_{INJ,1} + i_{INJ,2} \quad (6.5)$$

where $i_{INJ,1}$ is the injection signal by the VCO and $i_{INJ,2}$ is the auxiliary injected signal. In (6.4), the injection signal $i_{INJ,1}$ is dependent on the division N of the super-harmonic ILFD. The effective signal strength of the wanted harmonic resulted from the application of $i_{INJ,1}$ is reduced by $1/N$ in view of the locking range, where N is the division number of the divider. $i_{INJ,2}$ is generated by the auxiliary self-injection with feedback amplifier. The feedback amplifier increases the $i_{INJ,2}$ strength and hence the locking range.

4. Sub-Blocks of Triple-Band PLL

Fig. 6.4 shows the proposed concurrent multi-band multi-output PLL. It consists of a feedback loop, comprised of VCO, $1/3$ ILFD, buffer, $1/2$ CML divider, $1/16$ prescaler (PS), phase-frequency detector (PFD), charge pump (CP), and loop filter (LF), 8-bit decoder, and output buffers – all integrated in a single chip – and an off-chip reference clock. The PLL provides three differential outputs at 21, 7 and 3.5 GHz concurrently utilizing only a single ILFD and VCO. The 21-GHz signal is provided directly by the push-push VCO, whereas those at 7 and 3.5 GHz are obtained via the $1/3$ ILFD. The ILFD also provides the 3.5-GHz signal to the feedback loop for close-loop function of the PLL.

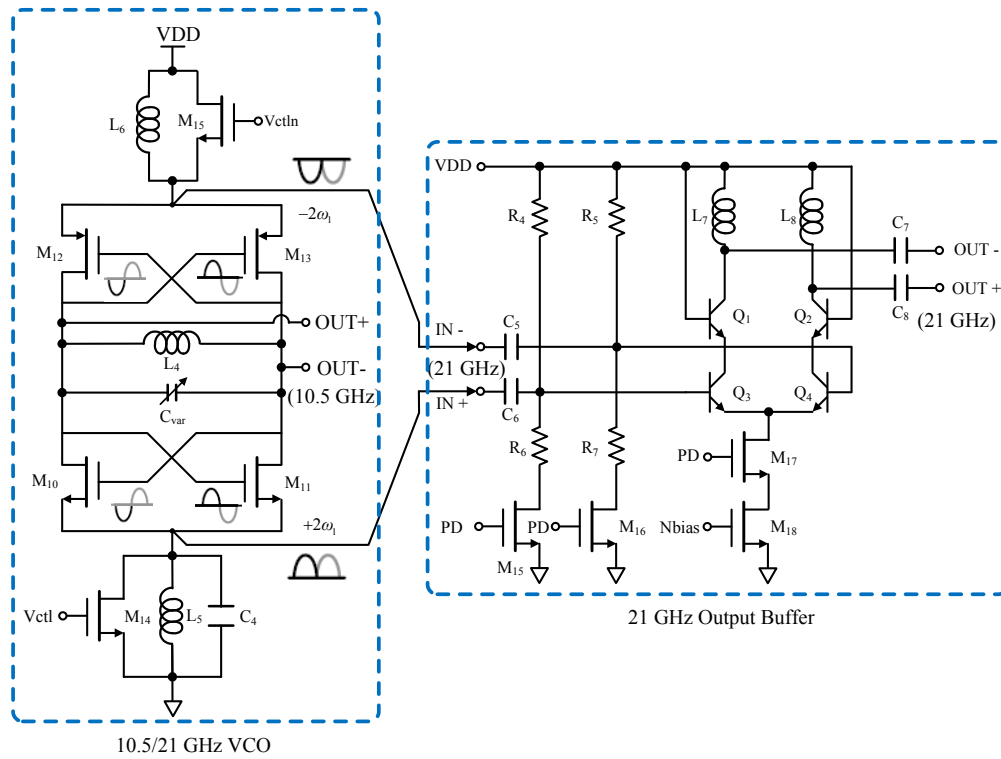
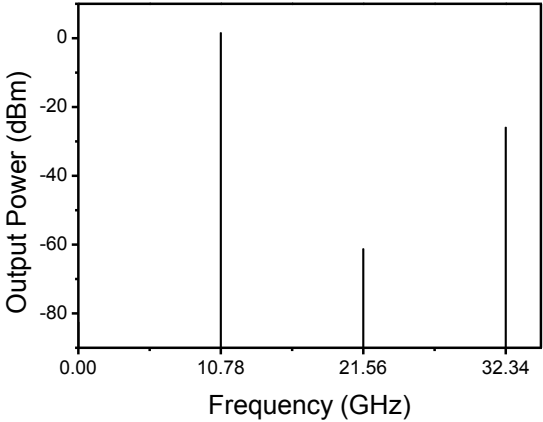
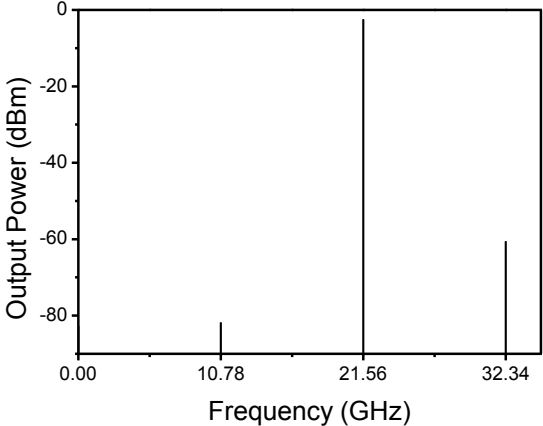


Fig. 6.5. Schematic of the 10.5/21-GHz push-push VCO and 21-GHz buffer.



(a)



(b)

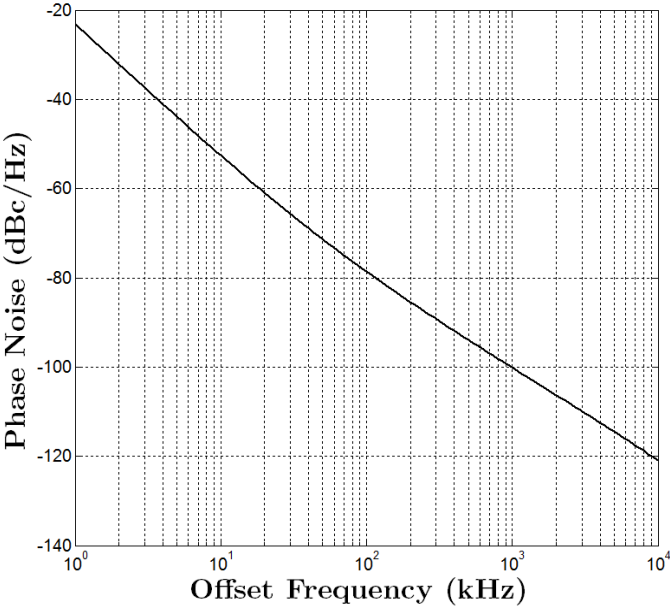
Fig. 6.6. Simulated output spectrum of the VCO at 10.5-GHz output (a) and 21-GHz output (b) ports.

A. 10.5/21GHz VCO and 21GHz Buffer

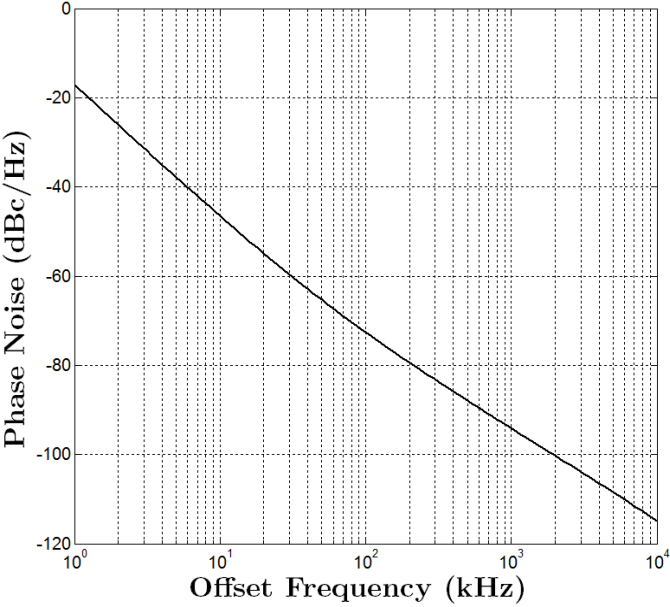
Fig. 6.5 shows the schematic of the 10.5/21GHz VCO along with the 21-GHz output buffer. The VCO is realized using a push-push oscillator architecture based on PMOS and NMOS cross-coupled pairs. The VCO produces two concurrent differential output signals: one at the fundamental frequency of 10.5 GHz and another at the second harmonic of 21 GHz (via the common sources of the cross-coupled pairs). The push-push topology enables both low frequency ($f_0=10.5$ GHz) and high frequency ($2f_0=21$ GHz) to be produced concurrently using transistors having low f_{max} suitable for the low frequency. Generation of signals at high frequencies using transistors with low f_{max} would not be possible if the signals are generated directly using a non-push-push configuration. Potentially higher quality factor Q is also possible since the VCO is designed at the low frequency of $f_0/2$. The 21-GHz buffer is a cascoded amplifier employing BJT (Q₁-Q₄) instead of MOSFETs as in the other components of the PLL due to the limited f_T of about 40 GHz for the 0.18- μ m CMOS.

Fig. 6.6 shows the simulated results of the spectrums at the 10.5- and 21-GHz output ports. The output powers at 10.5 and 21 GHz are 1.67 and -2.4 dBm, respectively. The harmonic rejections are 59.5 and 25.8 dBc for the 2nd and 3rd harmonic at the 10.5-GHz output port, respectively. At the 21-GHz output port, the harmonics rejections are 79.37 and 58.1 dBc for the fundamental signal and 3rd harmonic, respectively. In all simulations, the differential ports are connected to a balun and the powers are obtained at the balun's output port.

The simulated phase noise is shown in Fig. 6.7. The phase noises of the 10.5-



(a)



(b)

Fig. 6.7. Simulated phase noise of the VCO at 10.5-GHz output (a) and 21-GHz output (b) ports.

GHz signal is -102.05 dBc/Hz at 1-MHz offset, and that of the 21-GHz signal is 3 dB higher. At the common sources of the cross-coupled pairs, the 10.5-GHz fundamental signals are anti-phase, whereas the 21-GHz second-order harmonic signals are in-phase, making it a convenient point to extract the 21-GHz output signal to form a concurrent dual-band along with the 10.5-GHz signal using a single VCO.

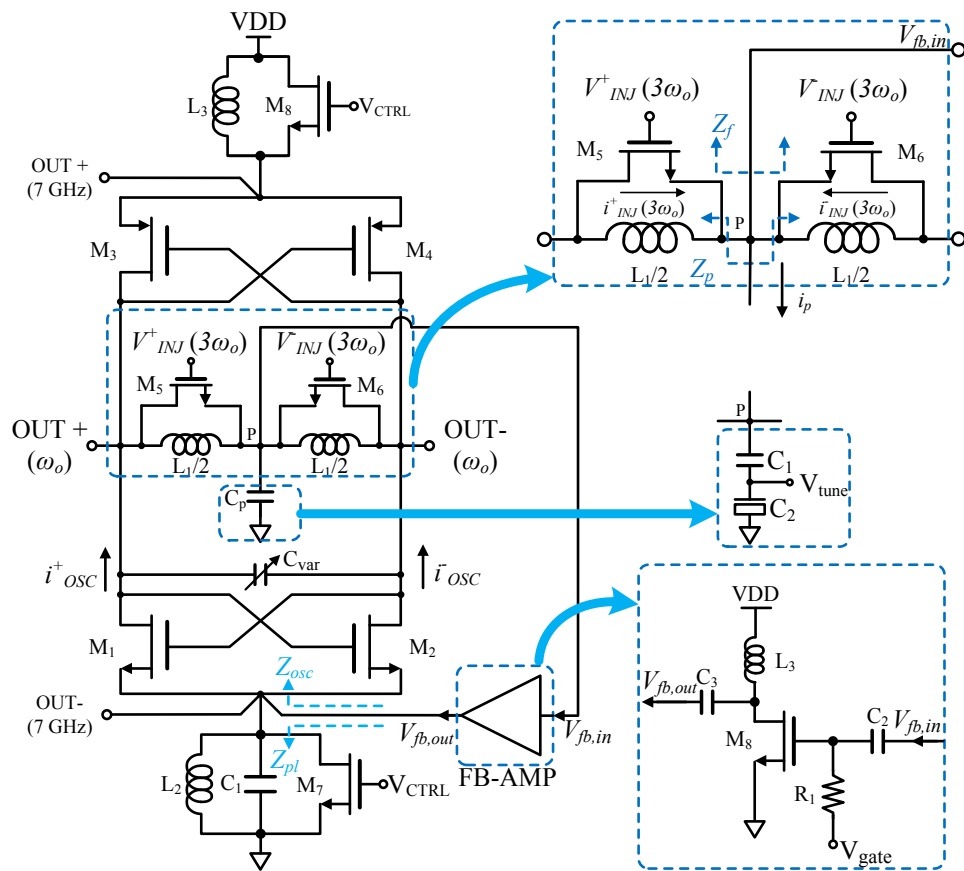


Fig. 6.8. Schematic of the 1/3 ILFD.

B. 1/3 ILFD

Fig. 6.8 shows the schematic of the 1/3 ILFD with an auxiliary self-injection technique that has two concurrent outputs at 3.5 and 7 GHz in chapter V. Fig. 6.9 shows the capacitance and quality factor Q of C_p at node P (noted in Fig. 8) implemented using an NMOS active device (C_2) as a function of the tuning voltage V_{tune} . C_p can be tuned from 0.88-0.2-pF while Q can be changed from 12-24.

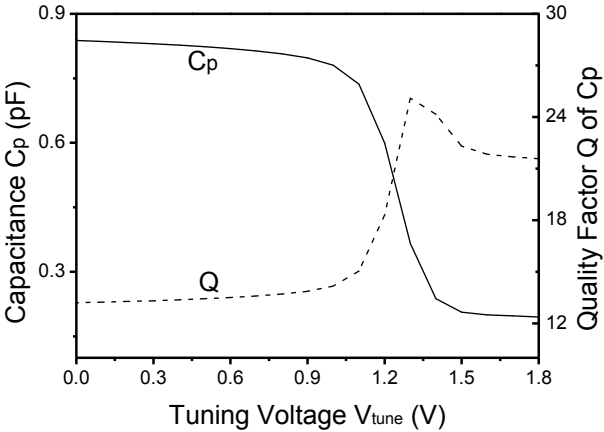


Fig. 6.9. Capacitance and quality factor of the 2nd harmonic at node P.

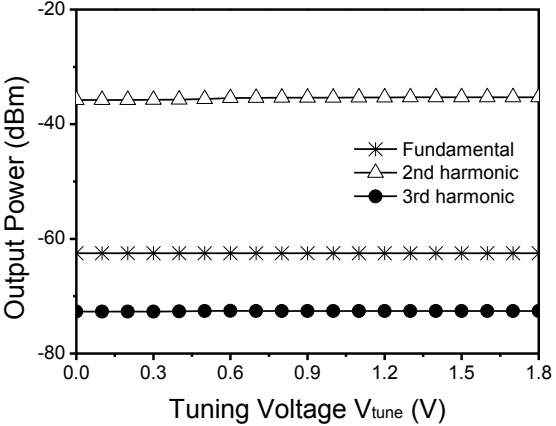
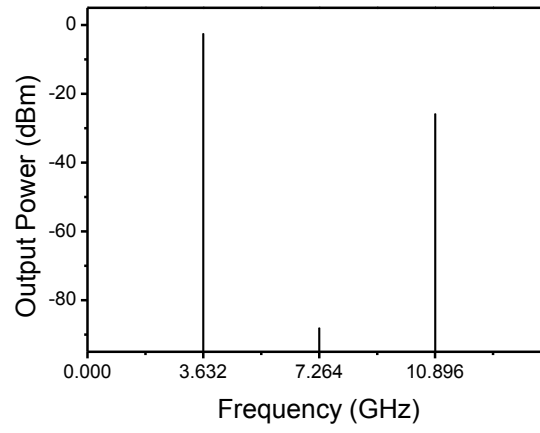
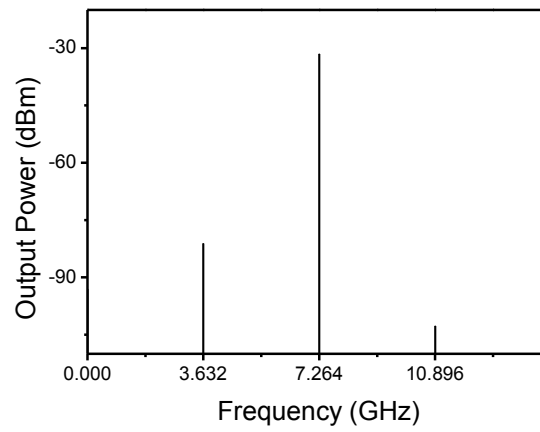


Fig. 6.10. Simulated output power at node P.



(a)



(b)

Fig. 6.11. Simulated output spectrum of the 1/3 ILFD at 3.5-GHz (a) and 7-GHz (b) output port.

TABLE 6.1
Simulated results of harmonic suppression of the proposed ILFD

Output Port		3.5GHz	7GHz	10GHz	21GHz	Node P
Output Power [dBm]		-2.5	-30	1.67	-2.4	-25
Spurs rejection [dBc]	1st		49.6		79.37	51.5
	2nd	85.6		59.5		
	3rd	23.3	100	25.8	58.1	85.6

Fig. 6.10 shows the simulated powers for the fundamental and the 2nd and 3rd harmonics at node P. The fundamental and 3rd harmonic signals are rejected by about 51.5 and 85.6 dBc with respect to the 2nd harmonic, respectively. Fig. 6.11 displays the simulated spectrums at the 3.5 and 7 GHz output ports of the 1/3 ILFD. The output powers at 3.5 and 7 GHz are -2.5 and -30 dBm, respectively. At the 3.5-GHz output port, the 2nd and 3rd harmonic rejections are 85.6 and 23.3 dBc, respectively. At the 7-GHz output port, the fundamental signal and 3rd harmonic rejections are 49.6 and 100 dBc, respectively. In all simulations, the differential ports are connected to a balun and the powers are obtained at the balun's output port. The summary of the powers and the harmonic suppressions at the output ports is shown in Table 6.1.

C. *The Proposed Mode-Converter and Minimized Mismatch Gain/Phase for Differential Outputs*

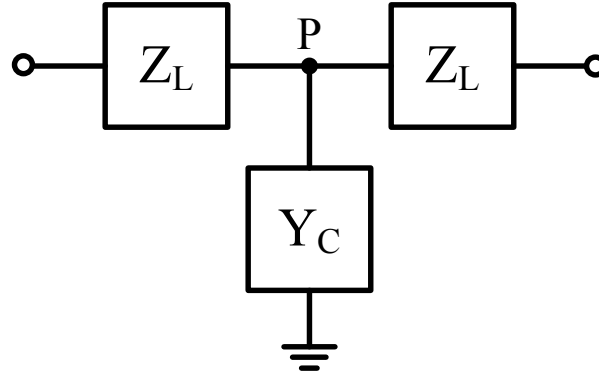


Fig. 6.12. The equivalent model of asymmetric inductor.

We now consider the T-network at node P shown in Fig. 6.12 that consists of $L_1/2$ in parallel with M_5 , $L_1/2$ in parallel with M_6 , and C_p , and let L represent the equivalent inductance of the combined $L_1/2$ and the parasitic capacitance of M_5 (or M_6), and C represent C_p .

The [ABCD] matrix of the equivalent model can be derived as

$$\begin{aligned} \begin{bmatrix} A & B \\ C & D \end{bmatrix} &= \begin{bmatrix} 1 & Z_L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/Z_C & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_L \\ 0 & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1+Z_L Y_C & Z_L(2+Z_L Y_C) \\ Y_C & 1+Z_L Y_C \end{bmatrix} \end{aligned} \quad (6.6)$$

where $Z_L = j\omega L/Z_0$ and $Y_C = j\omega CZ_0$ with Z_0 assumed to be the characteristic impedance of the terminating transmission line, and L and C representing the equivalent inductance and capacitance, respectively. We have from the conversion table:

$$\begin{aligned} A &= \frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{2S_{21}} \\ B &= Z_0 \frac{(1+S_{11})(1+S_{22})-S_{12}S_{21}}{2S_{21}} \\ C &= \frac{1}{Z_0} \frac{(1-S_{11})(1-S_{22})-S_{12}S_{21}}{2S_{21}} \\ D &= \frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{2S_{21}} \end{aligned} \quad (6.7)$$

The asymmetric inductor as shown in Fig. 6.12 is symmetric and hence $A=D$.

Under $S_{11}=S_{22}=0$ (perfect match), the symmetric network becomes reciprocal and

$$AD-BC=1 \quad (6.8)$$

Using $S_{11}=S_{22}=0$, we can obtain from (6.7)

$$B=CZ_0^2 \quad (6.9)$$

which upon substituting into (6.8) gives $AD-C^2Z_0^2=1$, which can be re-written using the parameters in (6.6) as

$$(1+Z_L Y_C)^2 - Y_C^2 Z_0^2 = 1 \quad (6.10)$$

Substituting $Z_L = j\omega L/Z_0$ and $Y_C = j\omega CZ_0$ into (6.10), we get

$$\omega^4 L^2 C^2 + \omega^2 (C^2 Z_0^4 - 2LC) = 0 \quad (6.11)$$

There are two possible solutions from (6.11), one of which is dc ($\omega=0$) which is discarded. The other is

$$\omega_0 = \sqrt{\frac{2LC - C^2 Z_0^4}{L^2 C^2}} \quad (6.12)$$

This is the oscillation frequency corresponding to the symmetric inductor in Fig. 6.12 under perfect match condition.

Since a perfect symmetry for the T-network implies that the outputs OUT+ and OUT- at ω_0 are equal in amplitudes and 180-deg out of phase, we can see from (6.10) that proper values for L and C can be chosen corresponding to an oscillation at ω_0 that results in differential outputs. In other words, we can optimize the T-network to produce well-behaved differential outputs, which is an interesting and important design information for the 1/3 ILFD.

D. 1/2 CML Divider, 1/16 Prescaler, PFD, CP, and LF

The 1/2 CML divider, 1/16 prescaler, PFD, CP and LF are based on conventional circuit topologies. As an example, Fig. 6.13 shows the PFD, CP and LF. The PFD

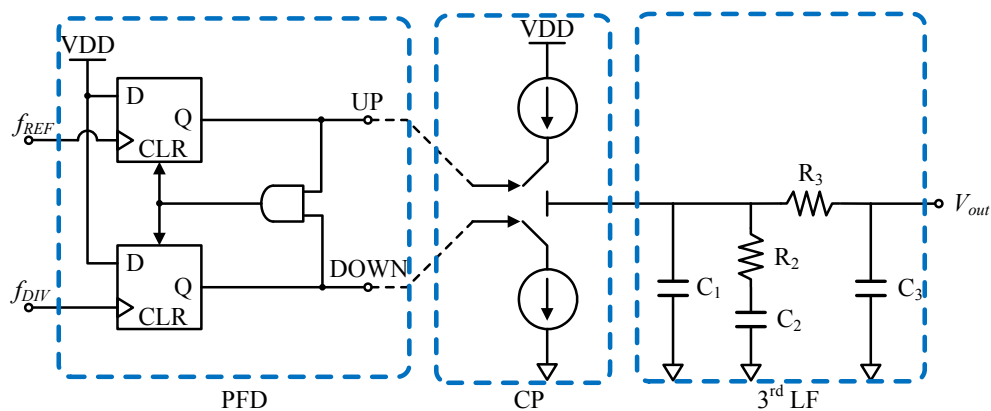


Fig. 6.13. PFD, CP and 3rd-order LF.

utilizes a three-state phase detection scheme and it operates as a linear system in the locking range. The reference clock is at 109.375 MHz. The CP is the main source for undesired reference spurs due to current and timing mismatch. The reference spurs can be reduced by controlling the loop bandwidth and loop phase error of the LF. The current of CP is controllable from 100 to 200 μA . The LF is a third-order filter and consists of three capacitors and two poly resistors. The LF's loop bandwidth can be tuned to have either 1 or 2 MHz. The phase margin of the LF is around 56.6 degrees.

E. Latched 8-bit Decoder for Digital Control

Fig. 6.14 shows the block diagram of the latched 8-bit decoder unit, that has 4-bit address, 8-bit data, 4-bit reset and single clock which provide input signals to the

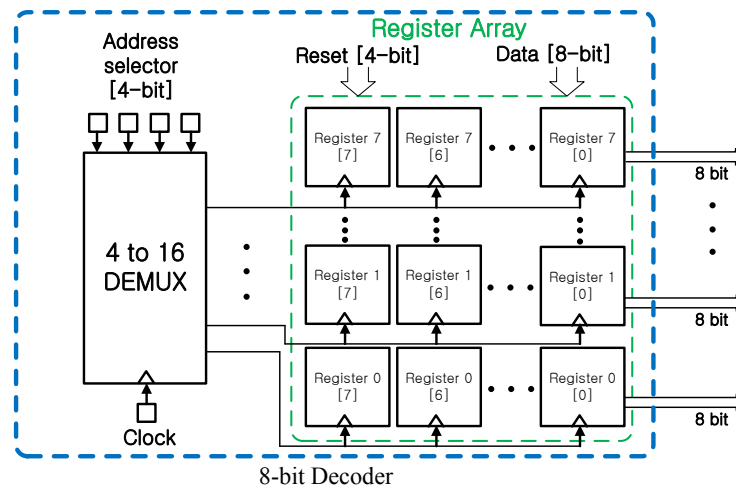


Fig. 6.14. Block diagram of the 8-bit decoder for digital control pins.

decoder. Each address can be selected from the 4-bit address. Once a path is selected by an address bit, the data is written and stored in the 8-bit registers. The data stored in the registers can be cleared by the 4-bit reset control. The clock signal is used to write the data while the clock is “high” and to remember the data while the clock is “low”.

5. Results

The entire PLL was fabricated using 0.18- μm CMOS, except the 21-GHz buffer, on Jazz 0.18- μm BiCMOS process [40]. Its die photograph is shown in Fig. 6.15. The chip size is 1.786 mm².

The measured frequency tuning range of the PLL at the 3.5-GHz output port is 3.47-4.313 GHz as shown in Fig. 6.16. Measured results show that the frequency of the PLL at the 7-GHz and 21-GHz output ports can be tuned from 6.94-8.626 GHz and 19.44-21.42-GHz, respectively. The measured frequency tuning range of the PLL around the 10.5-GHz signal is 9.72-10.71-GHz as shown in Fig. 6.17. Fig. 6.18 shows the measured output spectrum at the 3.5-GHz output port. The suppression of the 109.375-MHz reference spurs is greater than 45.55 dBc. Other spurs come from the buffer of the external clock that is shared between the reference signal and digital control clocking signal. Fig. 6.19 shows that the measured 2nd harmonic suppression is 62.2 dBc. This suppression level is achieved without filter and significantly higher than those reported to date.

It is noted, as reported in chapter V, that the locking range of the constituent 1/3 ILFD with the auxiliary self-injection is extended as much as 47.8 %, from 16.4 MHz

without the feedback amplifier (FB-AMP) to 24.24 MHz with the FB-AMP using a fixed capacitor bank. The 1/3 ILFD can achieve an (input) locking range about 2.529 GHz with the FB-AMP using a 5-bit capacitor bank and fine-tuning varactor voltage. The (input) 2.529-GHz locking range of this ILFD is more than 2.5 times of the free-running frequency range of 1 GHz (around 10.5 GHz) of the 10.5/21GHz VCO shown in Fig. 6.17, thus guarantying the finding of the VCO frequency at coarse-locking which, in turn, always results in a locked signal for the PLL. The measured phase noise of the 1/3 ILFD and PLL for different control voltages of the FB-AMP is shown in Fig. 6.20 and Fig. 6.21, respectively. As can be seen, the phase noise at 1-MHz offset corresponding to 1.8V control voltage for the FB-AMP is -80.9dBc/Hz at 50-kHz offset, that is 4.4 dB better than that of the PLL with the FB-AMP off. The measured spectrums of the signals at the 7- and 21-GHz output ports of the PLL are shown in Figs. 6.22 and 6.23, respectively. Table 6.2 compares the performance of the designed PLL with those of other concurrent multiband PLL's. The package of design chip uses the 80-pin QFN type and all bias are connected to the chip through wire-bonding on the package mounted on FR-4 PCB as shown in Fig. 6.24.

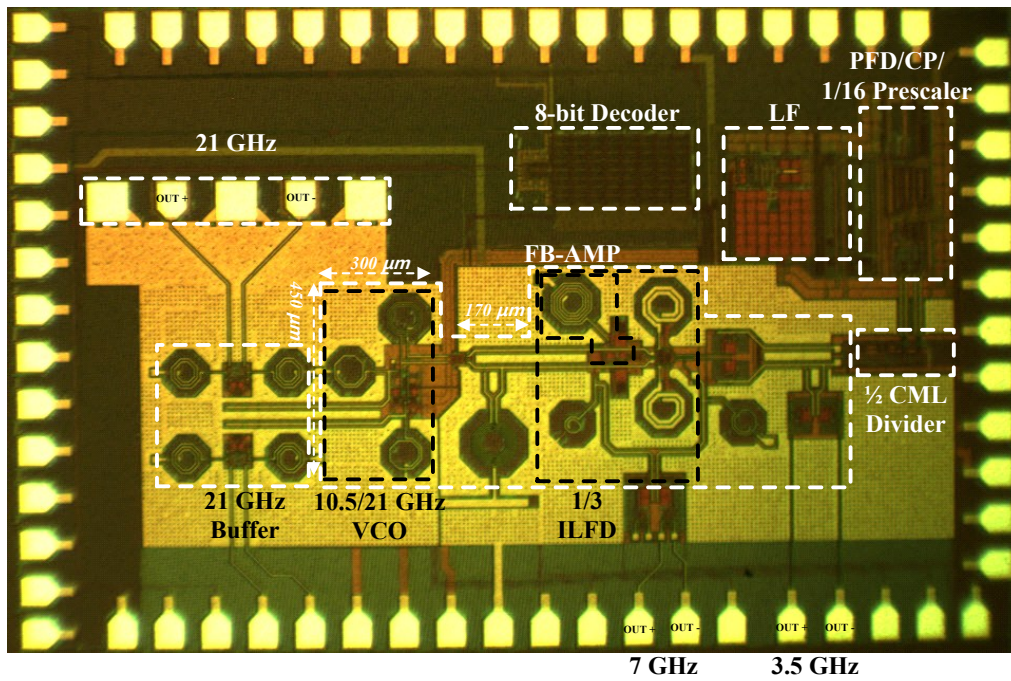


Fig. 6.15. Die photograph of the fully integrated PLL. Size: 1.786mm^2 with pads.

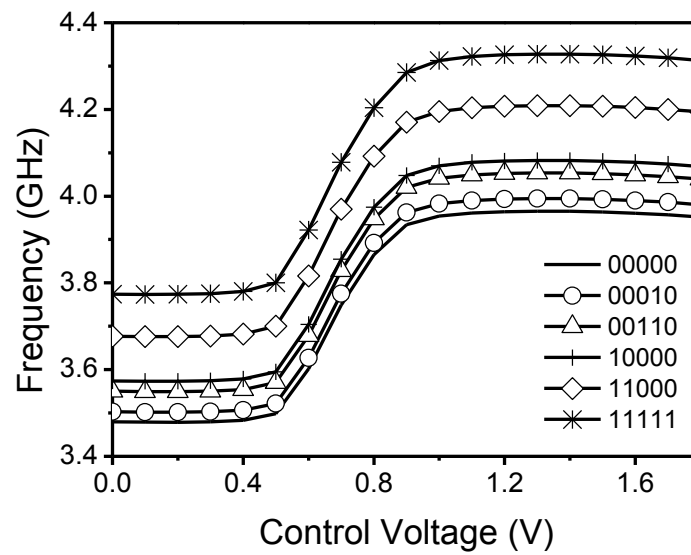


Fig. 6.16. Measured frequency tuning range of the PLL at the 3.5-GHz output port with 5-bit digital control.

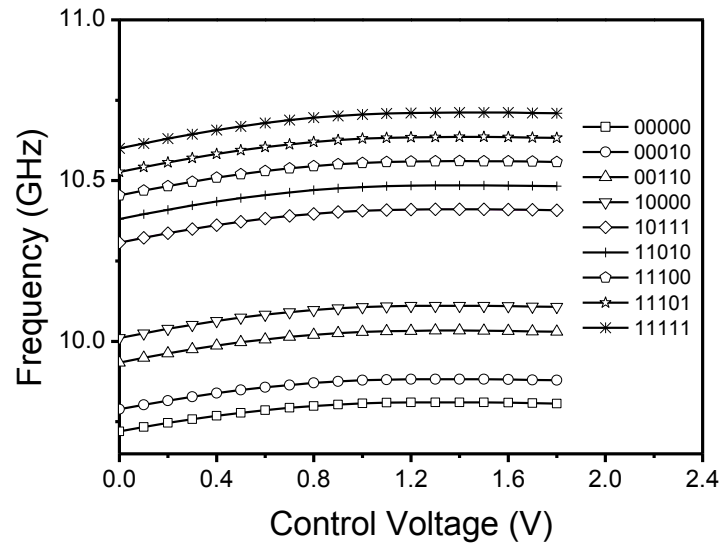


Fig. 6.17. Measured frequency tuning range of the PLL around the 10.5-GHz signal with 5-bit digital control.

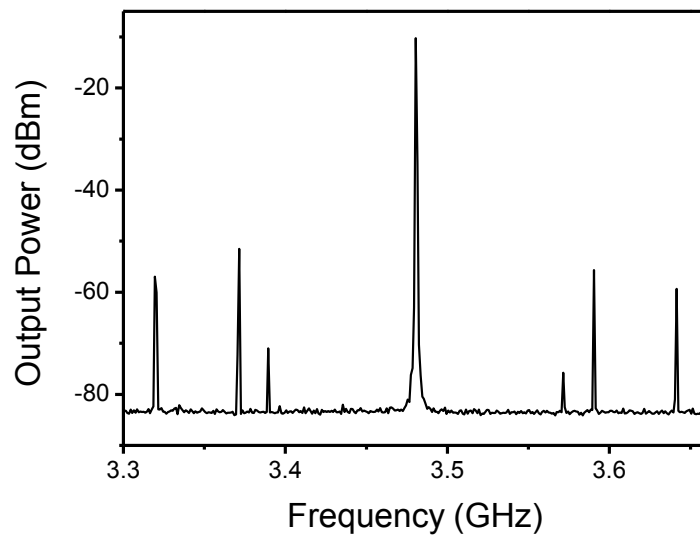


Fig. 6.18. Measured output spectrum of the PLL at the 3.5 GHz output port. RBW: 100 kHz, VBW: 30 kHz, SPAN: 0.4 GHz, REF: -10 dBm, and ATT: 0, 45.55 dBc at 109.375 MHz, 65.95 dBc at 87 MHz, and 48.9 dBc at 150 MHz.

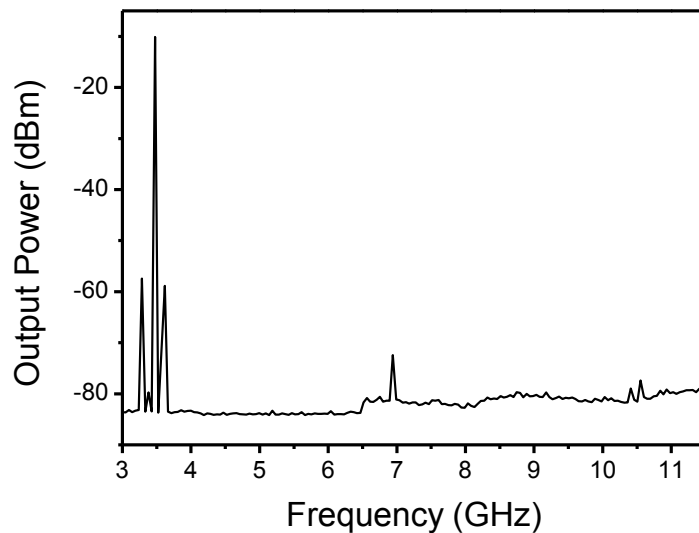


Fig. 6.19. Measured output spectrum of the PLL at the 3.5 GHz output port. RBW: 100 kHz, VBW: 30 kHz, SPAN: 9 GHz, REF: -10 dBm, and ATT: 0, 2nd harmonic rejection: 62.2 dBc, reference signal rejection: -45.55 dBc.

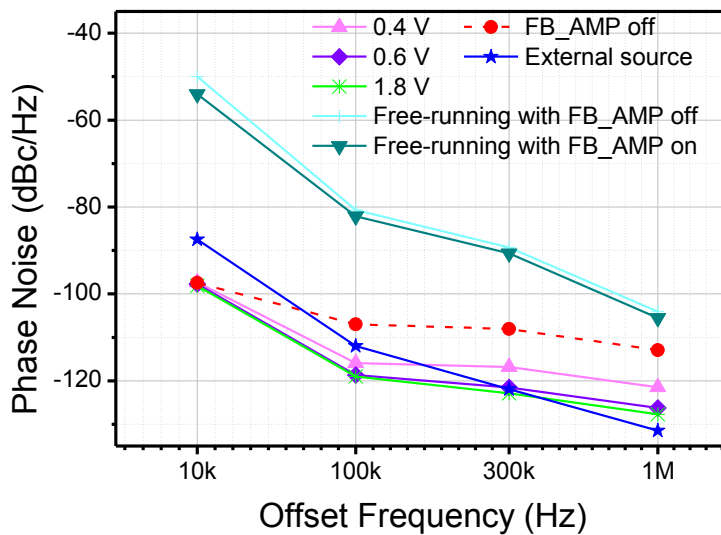


Fig. 6.20. Measured phase noise under fixed capacitor array at 00110.

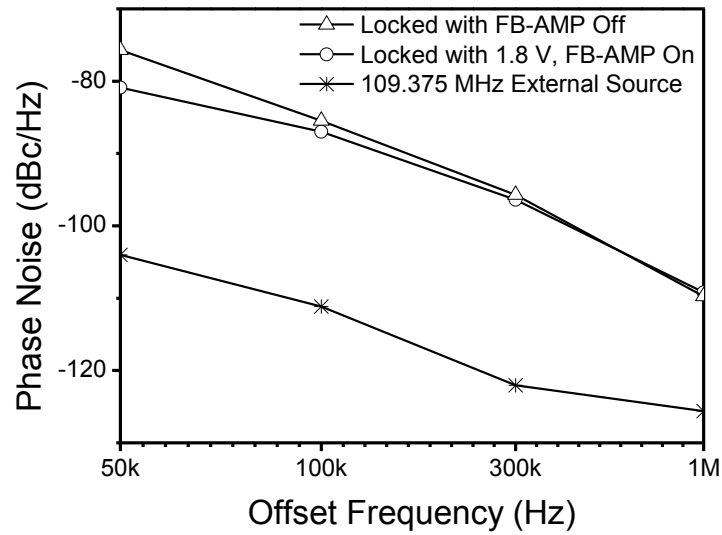


Fig. 6.21. Measured phase noise of the PLL.

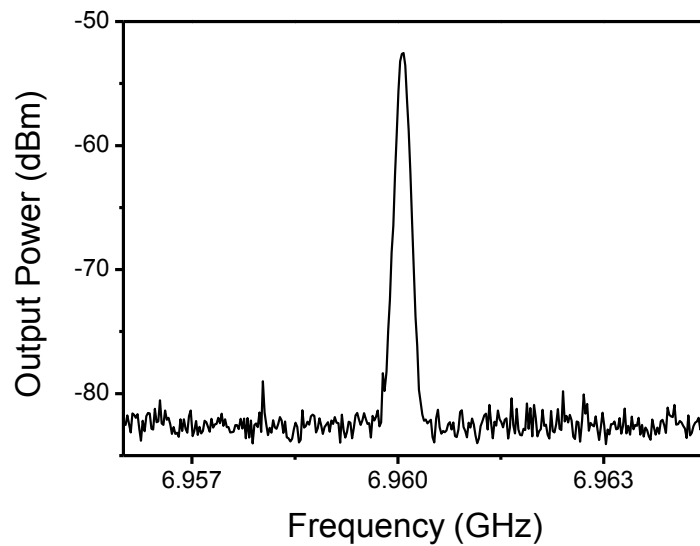


Fig. 6.22. Measured output spectrum of the PLL at the 7-GHz port. RBW: 100 kHz, VBW: 30 kHz, SPAN: 10 MHz, REF: -10 dBm, and ATT: 0.

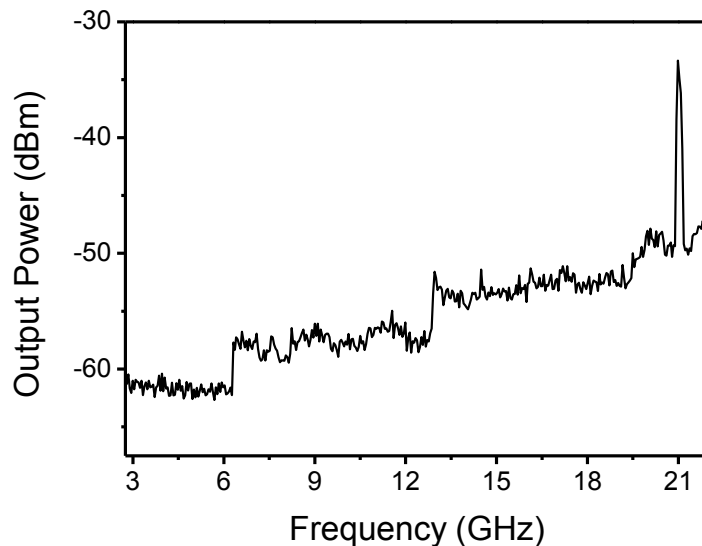
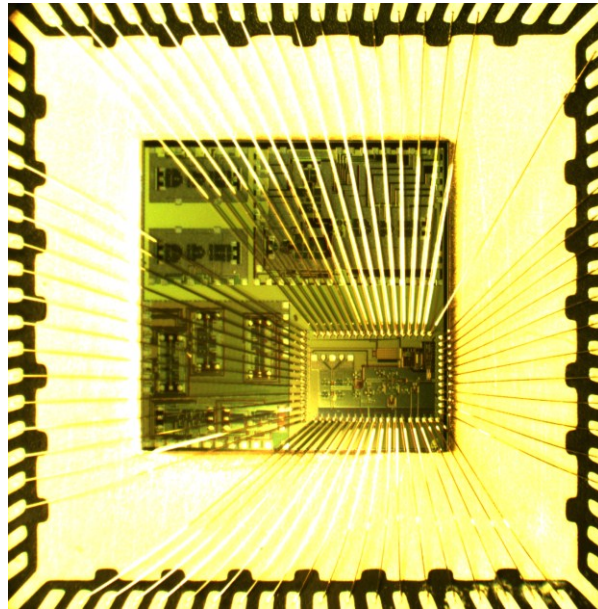


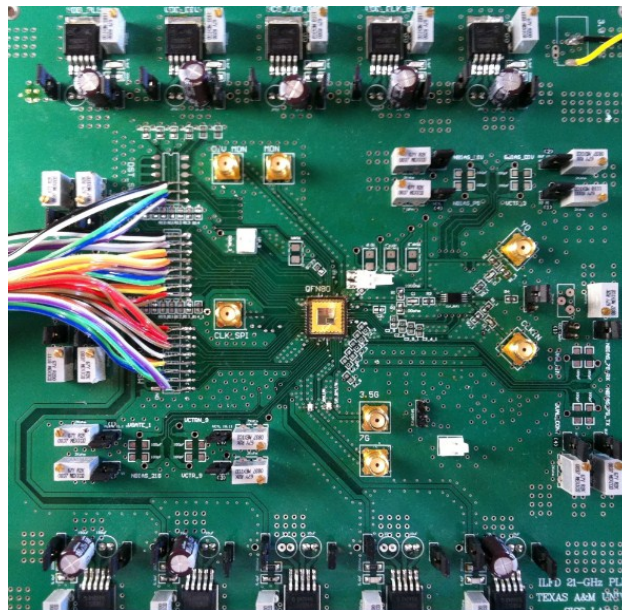
Fig. 6.23. Measured output spectrum of the PLL at the 21-GHz port. RBW: 3 MHz, VBW: 1 MHz, SPAN: 19.25 GHz, REF: 0 dBm, and ATT: 0.

TABLE 6.2
Comparison of measurement results between proposed ILFD PLL and others

		This work			[54]	[55]	[56]	
Technology [μm]		0.18- μm CMOS in BiCMOS (except the 21GHz buffer)			0.25- μm SiGe BiCMOS	0.18- μm SiGe BiCMOS	90-nm CMOS	
Core active device		CMOS (ILFD)	CMOS (PLL)		BJT	BJT	CMOS	
VDD [V]		1.8	1.8			2.5	1.5	
Power [mW]		19.1	81		680	50	113/106/109	
Area [mm^2]		0.048	1.786		4.8	0.8	1.125	
Outputs Frequency Range [GHz]		3.47-4.313 6.94-8.626 19.44-21.42			0.6-4.6 5-7 10-14 20-28	23.8-26.95 75.67-78.5	39.7-41.2 60.2-62.4 81.3-83.3	
Number of VCO		1			2	2	3	
Outputs generation method		Concurrent			Switch	Switch	Concurrent	
Phase Noise [dBc/Hz]		3.5GHz	unlock	lock	lock	4GHz	24G	40G
		@ 50k	-54.05	-108	-80.9	N/A		
		@ 100k	-82.14	-119	-86.98	N/A		
		@ 300k	-90.67	-123	-96.38	N/A		
		@ 1M	-105.3	-128	-109.2	-121	-114	-71.02
Division Ratio		3		96		256/768	512/768/1024	
Locking range		2.529G		300M		1.8-2.7G		
Spurs rejection		f_{REF}	-45.55			-70	-49.5	-36
		2 nd	-62.2			N/A	N/A	
		others	-48.9			N/A	N/A	
Architecture		Integer-N, 1/3 ILFD			Integer-N	Integer-N, 1/3 ILFD	Integer-N, 1/3 ILFD	
Order of LF		3rd for LF 4th type II			3rd for LF 4th type II	2nd for LF	2nd for LF	



(a)



(b)

Fig. 6.24. Microphotograph of the designed ILFD PLL (a) packaged chip mounted on FR-4 PCB (b).

6. Conclusion

A fully integrated PLL with 1/3 ILFD having concurrent tri-output and tri-band at 3.47-4.313 GHz, 6.94-8.626 GHz and 19.44-21.42-GHz is presented. The PLL is completely realized using 0.18- μm CMOS, except the 21-GHz buffer, and possesses features that are attractive for single-chip concurrent multiband microwave synthesizers and systems including wide and tunable locking range, high 2nd harmonic suppression, more stable locking, and use of single VCO and ILFD.

CHAPTER VII

SUMMARY AND CONCLUSIONS

A fully integrated multi-band multi-output synthesizer using 0.18- μm CMOS for multi-band microwave and millimeter-wave systems has been developed. Various injection-locked frequency dividers have also been designed.

A new 1/2 dual-injection locked frequency divider (dual-ILFD) with wide locking range and low-power consumption is proposed, analyzed, and developed together with a divide-by-2 current mode logic (CML) divider. The chip was fabricated using a 0.18- μm BiCMOS process. The 1/2 dual-ILFD enhances the locking range with low-power consumption through optimized load quality factor (Q_L) and output current amplitude (i_{OSC}) simultaneously. The relationship between i_{OSC} and Q_L , and hence the locking range, is explained analytically. The designed 1/2 dual-ILFD also works as a free-running oscillator between 3.592 GHz and 4.102 GHz without injection signals. The 1/2 dual-ILFD achieves a locking range of 692 MHz between 7.512 and 8.204 GHz. The current consumption of the designed core 1/2 dual-ILFD is 2.93 mA with 1.5 V supply. The designed 1/2 dual-ILFD increases the locking range by 9.9 times over a single-injection counterpart. The new 1/2 dual-ILFD is especially attractive for microwave phase-locked loops and frequency synthesizers requiring low power and wide locking range.

A fully integrated 3.5-GHz divide-by-3 (1/3) injection-locked frequency divider (ILFD) is developed. It consists of an internal 10.5-GHz Voltage Controlled Oscillator

(VCO) functioning as an injection source, 1/3 ILFD core, and output inverter buffer. A phase tuner implemented on an asymmetric inductor is proposed to increase the locking range. With an internal injection signal power of only -18 dBm, a 25% enhancement in the locking range from 12 to 15 MHz is achieved with the proposed phase tuning. The integrated 1/3 ILFD has a frequency tuning range of 3.3 – 4.2 GHz. It is realized using a 0.18- μm BiCMOS process, occupies $0.6 \times 0.7 \text{ mm}^2$, and consumes 19.1 mW.

A new divide-by-3 injection-locked frequency divider (ILFD) utilizing self-injection technique is developed. The self-injection is realized with an odd-to-even harmonic converter through a feedback-amplifier that increases the injection efficiency of the 1/3 ILFD with boosted self-injection signal. The self-injection technique substantially enhances the locking range and phase noise, and reduces the minimum power of the injection signal needed for the 1/3 ILFD. The locking range is increased by 47.8 % and the phase noise is reduced by 14.77 dBc/Hz at 1-MHz offset. The required minimum injection signal power is only -30 dBm. The 1/3 ILFD is realized in CMOS technology with Jazz 0.18- μm BiCMOS process. The core 1/3 ILFD occupies 0.048 mm^2 with power consumption of 18.2 mW from a 1.8 V power supply.

A fully integrated concurrent tri-band, tri-output phase-locked loop (PLL) with divide-by-3 injection locked frequency divider (ILFD) is presented. The PLL is completely realized using 0.18- μm CMOS, except one buffer, and employs only one VCO and one frequency divider, resulting in small chip size, low power consumption and less unwanted coupling. A new locking mechanism for the ILFD based on the gain control of the feedback amplifier is utilized to enable tunable and enhanced locking

range which facilitates the attainment of stable locking states. The PLL has three concurrent multiband outputs: 3.47-4.313 GHz, 6.94-8.626 GHz and 19.44-21.42-GHz. High second-order harmonic suppression of 62.2 dBc is achieved without using a filter through optimization of the balance between the differential outputs. The PLL consumes 81 mW with supply voltage of 1.8 V and occupies $1.9 \text{ mm} \times 0.94 \text{ mm}$.

REFERENCES

- [1] G. A. Katopis, "Delta-I noise specification for a high-performance computing machine," *Proc. IEEE*, vol. 73, pp. 1405-1415, Sept. 1985.
- [2] R. Senthinathan, J. L. Prince, "Simultaneous switch ground noise calculation for packaged CMOS devices," *IEEE J. Solid-State Circuits*, vol. 26, no. 11, pp. 1724-1728, Nov. 1991.
- [3] P. Larsson, "di/dt noise in CMOS integrated circuits," *Analog Integrated Circuits and Signal Processing*, no. 1.2, pp. 113-130, Sept. 1997.
- [4] S. R. Vemuru, "Effects of simultaneous switching noise on the tapered buffer design," *IEEE Trans. VLSI Systems*, vol. 5, no. 3, pp. 290-300, Sept. 1997.
- [5] M. R. M. Hashemi and T. Itoh, "Coupled composite right/left-handed leaky-wave transmission lines based on common/differential-mode analysis," *IEEE Trans. Microw. Theory and Tech.*, vol. 58, no. 12, pp. 3645-3656, Dec. 2010.
- [6] C. H. Wu, C. H. Wang, and C. H. Chen, "Novel balanced coupled-line bandpass filters with common-mode noise suppression," *IEEE Trans. Microw. Theory and Tech.*, vol. 55, no. 2, pp. 287-295, Feb. 2007.
- [7] D. E. Bockelman and W. R. Eisenstadt, "Direct measurement of crosstalk between integrated differential circuits," *IEEE Trans. Microw. Theory and Tech.*, vol. 48, no. 8, pp. 1410-1413, Aug. 2000.
- [8] M. Hyunwon, K. Sungweon, K. Youn Tae, and L. Kwiro, "A fully differential LC-VCO using a new varactor control structure," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 9, pp. 410-412, Sept. 2004.
- [9] K. W. Kobayashi, A. K. Oki, L. T. Tran, J. C. Cowles, A. Gutierrez-Aitken, F. Yamada, T. R. Block, and D. C. Streit, "A 108-GHz InP-HBT monolithic push-push VCO with low phase noise and wide tuning bandwidth," *IEEE J. Solid-State Circuits*, vol. 34, no. 9, pp. 1225-1232, Sept. 1999.

- [10] A. Yazdi and M. M. Green, "A 40 GHz differential push-push VCO in 0.18 μm CMOS for serial communication," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 11, pp. 725-727, Nov. 2009.
- [11] C. Hsien-Chin and K. Chih-Pin, "A wide tuning range 69 GHz push-push VCO using 0.18 μm CMOS technology," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 2, pp. 97-99, Feb. 2010.
- [12] J. Sheng-Lyang, S. Chih-Chieh, L. Cheng-Chen, and J. Miin-Horng, "A 0.18 μm CMOS quadrature VCO using the quadruple push-push technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 6, pp. 343-345, Jun. 2010.
- [13] K. Yen-Hung, T. Jeng-Han, C. Hong-Yeh, and H. Tian-Wei, "Design and analysis of a 77.3% locking-range divide-by-4 frequency divider," *IEEE Trans. Microw. Theory and Tech.*, vol. 59, no. 10, pp. 2477-2485, Oct. 2011.
- [14] H. Hsieh-Hung, C. Huan-Sheng, and L. Liang-Hung, "A V-Band divide-by-4 direct injection-locked frequency divider in 0.18- μm CMOS," *IEEE Trans. Microw. Theory and Tech.*, vol. 59, no. 2, pp. 393-405, Feb. 2011.
- [15] Y. Xiang, B. Chirn Chye, D. Manh Anh, Y. Kiat Seng, and L. Wei Meng, "Design of ring-oscillator-based injection-locked frequency dividers with single-phase inputs," *IEEE Microw. Wireless Compon. Lett.*, vol. 21, no. 10, pp. 559-561, Oct. 2011.
- [16] L. Ming-Wei, W. Po-Chi, H. Tzuen-Hsi, and C. Huey-Ru, "Low-voltage, wide-locking-range, millimeter-wave divide-by-5 injection-locked frequency dividers," *IEEE Trans. Microw. Theory and Tech.*, vol. 60, no. 3, pp. 679-685, Mar. 2012.
- [17] Leenaerts, D., J. V. D. Tang, and C. S. Vaucher, *Circuit Design for RF transceivers*, pp. 243-258, Kluwer Academic Publishers, Boston, 2001.
- [18] Best, R. E., *Phase-Locked Loop Design, Simulation, and Application*, 2nd edition, pp. 13-18, McGraw-Hill, New York, 1993.
- [19] Dan H. Wolaver, *Phase-Locked Loop Circuit Design*, pp. 9-22, Prentice Hall Publication, New Jersey, 1991.

- [20] B. Razavi, *Design of Analog CMOS Integrated Circuits*, pp. 532-567, McGraw-Hill, New York, 2002.
- [21] R. J. Baker, H. W. Li, and D. E. Boyce, *CMOS Circuit Design, Layout, and Simulation*, pp. 375-417, Wiley-IEEE Press, New York, 2010.
- [22] Dean Benerjee, *PLL Performance, Simulation, and Design*, Fourth Edition, pp. 45-47, Dog Ear Publishing, Indianapolis, IN, 2006.
- [23] J. Dixon, E. Bradley, and Z. B. Popovic, "Nonlinear time-domain analysis of injection-locked microwave MESFET oscillators," *IEEE Trans. Microw. Theory and Tech.*, vol. 45, no. 7, pp. 1050-1057, Jul. 1997.
- [24] R. Adler, "A study of locking phenomena in oscillators," *Proc. IRE*, vol. 34, pp. 351-357, June 1946.
- [25] C. Shanfeng, T. Haitao, J. Silva-Martinez, and A. I. Karsilayan, "A fully differential low-power divide-by-8 injection-locked frequency divider up to 18 GHz," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 583-591, Mar. 2007.
- [26] S. Pellerano, S. Levantino, C. Samori, and A. L. Lacaita, "A 13.5-mW 5-GHz frequency synthesizer with dynamic-logic frequency divider," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 378-383, Feb. 2004.
- [27] J. Lee and B. Razavi, "A 40-GHz frequency divider in 0.18- μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 39, no. 4, pp. 594-601, Apr. 2004.
- [28] T. Haitao, C. Shanfeng, A. I. Karsilayan, and J. S. Martinez, "An injection-locked frequency divider with multiple highly nonlinear injection stages and large division ratios," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 4, pp. 313-317, Apr. 2007.
- [29] W. Hui and A. Hajimiri, "A 19 GHz 0.5 mW 0.35 μm CMOS frequency divider with shunt-peaking locking-range enhancement," in *IEEE ISSCC Tech. Dig.*, Feb. 2001, pp. 412-413, 471.
- [30] Y. N. Miao, C. C. Boon, M. A. Do, K. S. Yeo, and Y. X. Zhang, "High-frequency

- low-power LC divide-by-2/3 injection-locked frequency divider," *IEEE Microw. Optical Tech. Lett.*, vol. 53, no. 2, pp. 337-340, Feb. 2011.
- [31] B. Razavi, "A study of injection locking and pulling in oscillators," *IEEE J. Solid-State Circuits*, vol. 39, no. 9, pp. 1415-1424, Sep. 2004.
- [32] L. Tang-Nian, Y. J. E. Chen, and H. Deukhyoun, "A V-band wide locking range CMOS frequency divider," in *IEEE MTT-S Symp. Dig.*, Jun. 2008, pp. 563-566.
- [33] L. Tang-Nian and Y. J. E. Chen, "A 0.8-mW 55-GHz dual-injection-locked CMOS frequency divider," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 3, pp. 620-625, Mar. 2008.
- [34] Z. Hui and H. C. Luong, "Ultra-low-voltage 20-GHz frequency dividers using transformer feedback in 0.18- μ m CMOS process," *IEEE J. Solid-State Circuits*, vol. 43, no. 10, pp. 2293-2302, Oct. 2008.
- [35] S. Hara, K. Okada, and A. Matsuzawa, "10MHz to 7GHz quadrature signal generation using a divide-by-4/3, -3/2, -5/3, -2, -5/2, -3, -4, and -5 injection-locked frequency divider," in *IEEE VLSI Circuits Symp.*, Jun. 2010, pp. 51-52.
- [36] K. Yen-Hung, T. Jeng-Han, and H. Tian-Wei, "A 1.5-mW, 23.6% frequency locking range, 24-GHz injection-locked frequency divider," in *Proc. European Microwave Conf. (EuMC)*, Sep. 2010, pp. 73-76.
- [37] L. J. Paciorek, "Injection locking of oscillators," *Proc. IEEE*, vol. 53, no. 11, Nov. 1965, pp. 1723-1727.
- [38] R. Sujiang, A. W. L. Ng, and H. C. Luong, "0.9mW 7GHz and 1.6mW 60GHz frequency dividers with locking-range enhancement in 0.13 μ m CMOS," in *IEEE ISSCC Tech. Dig.*, Feb. 2009, pp. 96-97.
- [39] W. Ting, M. Un-Ku, and K. Mayaram, "Dependence of LC VCO oscillation frequency on bias current," in *Pro., IEEE Int. Symp. Circuits Syst.* May 2006, vol. pp. 5039-5042.
- [40] Jazz Semiconductor, Newport Beach, CA.

- [41] M. Tiebout, "A CMOS direct injection-locked oscillator topology as high-frequency low-power frequency divider," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1170-1174, Jul. 2004.
- [42] W. Chung-Yu and Y. Chi-Yao, "Design and analysis of a millimeter-wave direct injection-locked frequency divider with large frequency locking range," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 8, pp. 1649-1658, Aug. 2007.
- [43] S. Shekhar, G. Balamurugan, D. J. Allstot, M. Mansuri, J. E. Jaussi, R. Mooney, J. Kennedy, B. Casper, and F. O'Mahony, "Strong injection locking in low-Q LC oscillators: modeling and application in a forwarded-clock I/O receiver," *IEEE Trans. Circuits Syst. I*, vol. 56, no. 8, pp. 1818-1829, Aug. 2009.
- [44] Y. Seong-Mo and K. O. Kenneth, "Demonstration of a switched resonator concept in a dual-band monolithic CMOS LC-tuned VCO," in *Proc. Custom Integr. Circuits Conf.*, May 2001, pp. 205-208.
- [45] J. Sheng-Lyang, L. Chien-Feng, and Y. Wei-Hsung, "A divide-by-3 injection locked frequency divider with single-ended input," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 2, pp. 142-144, Feb. 2008.
- [46] J. Sheng-Lyang, L. Chih-Yeh, and L. Chien-Feng, "A low voltage 0.35 μm CMOS frequency divider with the body injection technique," *IEEE Microw. Wireless Compon. Lett.*, vol. 18, no. 5, pp. 470-472, July 2008.
- [47] J. Sheng-Lyang, C. Yu-Sheng, C. Chia-Wei, and L. Cheng-Chen, "A wide-locking range $\div 3$ injection-locked frequency divider using linear mixer," *IEEE Microw. Wireless Compon. Lett.*, vol. 20, no. 7, pp. 390-392, Jul. 2010.
- [48] W. Hui and Z. Lin, "A 16-to-18GHz 0.18- μm Epi-CMOS divide-by-3 injection-locked frequency divider," in *IEEE ISSCC Tech. Dig.*, Feb. 2006, pp. 27-29.
- [49] C. Heng-Chia, A. Borgioli, P. Yeh, and R. A. York, "Analysis of oscillators with external feedback loop for improved locking range and noise reduction," *IEEE Trans. Microw. Theory Tech.*, vol. 47, no. 8, pp. 1535-1543, 1999.

- [50] C. Heng-Chia, C. Xudong, U. K. Mishra, and R. A. York, "Phase noise in coupled oscillators: theory and experiment," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 5, pp. 604-615, May 1997.
- [51] C. Heng-Chia, C. Xudong, M. J. Vaughan, U. K. Mishra, and R. A. York, "Phase noise in externally injection-locked oscillator arrays," *IEEE Trans. Microw. Theory Tech.*, vol. 45, no. 11, pp. 2035-2042, Nov. 1997.
- [52] C. Heng-Chia, X. Cao, U. K. Mishra, and R. A. York, "Phase noise in coupled oscillator arrays," in *IEEE MTT-S Symp. Dig.*, Jun. 1997, pp. 1061-1064.
- [53] C. Heng-Chia, "Noise and stability analysis of coupled oscillators," Ph.D. dissertation, Dept. Elect. Comput. Eng., Univ. California at Santa Barbara, Santa Barbara, CA, pp. 47-85, 1998.
- [54] S. A. Osmany, F. Herzel, and J. C. Scheytt, "An integrated 0.6-4.6 GHz, 5-7 GHz, 10-14 GHz, and 20-28 GHz frequency synthesizer for software-defined radio applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1657-1668, Sep. 2010.
- [55] V. Jain, B. Javid, and P. Heydari, "A BiCMOS dual-Band millimeter-wave frequency synthesizer for automotive radars," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2100-2113, Aug. 2009.
- [56] C. Hsien-Ku, W. Tao, and L. Shey-Shi, "A millimeter-wave CMOS triple-band phase-locked loop with a multimode LC-based ILFD," *IEEE Trans. Microw. Theory Tech*, vol. 59, no. 5, pp. 1327-1338, May 2011.

VITA

Sang Hun Lee received his B.S. degree in 2002 from Kwangwoon University, Seoul, Korea, and M.S. degree in 2004 from Kwangwoon University, Seoul, Korea, in Electrical Engineering. Before his Ph.D. study with Dr. Cam Nguyen, he worked as a helicopter maintenance engineer in Korea Army from 1993 to 1998. During that time, he developed subsystems and systems for Helicopter Maintenance, Seoul, Korea. He was also a RFIC design engineer at Mission Inc., Seoul, Korea, for 5 years working on RFID Tag and RF Interference Cancellation Systems, and a RFIC design engineer at Mewtel Inc., Seoul, Korea, for 3 years working on Bluetooth EDR Transceiver.

His research interests are high frequency radio frequency integrated circuits design.

Mr. Lee can be reached through the Department of Electrical and Computer Engineering at Texas A&M University, College Station, TX 77843-3126. His email is platune@gmail.com.