A LOW TOTAL HARMONIC DISTORTION SINUSOIDAL OSCILLATOR BASED ON DIGITAL HARMONIC CANCELLATION TECHNIQUE

A Thesis

by

JUN YAN

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2012

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sánchez-Sinencio
Committee Members,	Kamran Entesari
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ABSTRACT

A Low Total Harmonic Distortion Sinusoidal Oscillator based on Digital Harmonic Cancellation Technique.

(May 2012)

Jun Yan, B.S., Huazhong University of Science and Technology

Chair of Advisory Committee: Dr. Edgar Sánchez-Sinencio

Sinusoidal oscillator with low total harmonic distortion (THD) is widely used in many applications, such as built-in-self-testing and ADC characterization. An innovative medical application for skin cancer detection, which employed a technology named bio-impedance spectroscopy, also requires highly linear sinusoidal-wave as the reference clock. Moreover, the generated sinusoidal signals should be tunable within the frequency range from 10kHz to 10MHz, and quadrature outputs are demanded for coherent demodulation within the system.

A design methodology of sinusoidal oscillator named digital-harmonic-cancellation (DHC) technique is presented. DHC technique is realized by summing up a set of square-wave signals with different phase shifts and different summing coefficient to cancel unwanted harmonics. With a general survey of literature, some sinusoidal oscillators based on DHC technique are reviewed and categorized. Also, the mathematical algorithm behind the technique is explained, and non-ideality effect is analyzed based on mathematical calculation.

The prototype is fabricated in OnSemi 0.5um CMOS technology. The experimental results of this work show that it can achieve HD2 is -59.74dB and HD3 is -60dB at 0.9MHz, and the frequency is tunable over 0.1MHz to 0.9MHz. The chip consumes area of 0.76mm^2, and power consumption at 0.9MHz is 2.98mW. Another design in IBM 0.18um technology is still in the phase of design. The preliminary simulation results show that the 0.18um design can realize total harmonic distortion of -72dB at 10MHz with the power consumption of 0.4mW. The new design is very competitive with state-of-art, which will be done with layout, submitted for fabrication and measured later.

DEDICATION

To my family

ACKNOWLEDGEMENTS

First and foremost, I would like to express my deep appreciation to my advisor Dr. Edgar Sánchez-Sinencio for having accepted me into his group, his invaluable guidance, insightful thinking, kindness and support throughout my graduate study. Without his patient support and encouragement, this work would not have been completed. I would also like to express my gratitude to other committee members, Dr. Kamran Entesari, Dr. Rainer J. Fink and Dr. Sunil Khatri, Dr. Hu Jiang for their time and effort in guiding and supporting me throughout the course of this research.

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TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

Page

Page

Page

LIST OF TABLES

Page

1. INTRODUCTION

Sinusoidal oscillator with high linearity and wide frequency range plays an important role in many applications. It is well known that sinusoidal signals can be conventionally used as test waveform or references by certain electronic circuits and systems, such as frequency response characterization and THD measurement. On the other hand, due to the low power, small area attributes of integrated circuit, on-chip characterization system, such on-chip spectrum analyzer [1]-[3], distortion characterization of ADC [4] and IP noise tolerance testing [5], has increasingly gain popularity in the academia area. And on-chip sinusoidal oscillator is the key factor to achieve the high accuracy of the measurement system.

In addition, as is reported by [6], the medical applications have made great impact on electronics industry. Better utilization of health-care technology benefits people with a great chance to reduce costs and improve service. And the global market for medical electronics is expanding rapidly. Among them, electrical bio-impedance spectroscopy is one of the advanced electrical technologies which can help improve the early detection of some critical diseases.

1.1 Electrical bio-impedance spectroscopy technique for skin cancer detection

As is reported, more than 2 million cases of skin cancer are diagnosed in 2011 of United States, causing almost more than 10,000 estimated deaths [7]. Though it is advised for people to develop a good life style and keep away from unhealthy habits that

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will cause skin cancers, regular examinations by a health care professional can help with the early protection and removal of precancerous growth, which is crucial for timely and effective treatment. For the conventional clinical detection, visual inspection helps preliminarily diagnose the potential of skin cancer, and then biopsy and appropriate treatment can be followed. Even if visual inspection is carried by a health care professional, error is often caused. As for biopsy, though being an accurate method to detect cancer, the patient will suffer from physical uncomfortable feeling, and high cost. Consequently, seeking for a new skin cancer detection method instead which is with high accuracy, low cost and being convenient is a very promising topic in the medical area. Electrical impedance detection, which diagnoses electrical properties of the biological tissue, starts to become attractive for these reasons. As a non-invasive diagnosis approach, it can largely alleviate the pain of patients. Also, considering the high integration feature of IC product, this low cost solution can be widely distributed to medical care provider.

1.1.1 Dispersion of skin tissue

The bio-electrical impedance spectroscopy for skin cancer detection is basically based on the dispersion attributes of skin tissues. Electrical impedance spectrum of skin tissue contains frequency regions where the impedance decreases as frequency increases, and the phenomena is named dispersion. There are different dipole interactions between dielectric materials. When posing to electromagnetic field surrounding, these dielectric materials within the molecular structures, will experience dispersion in frequency domain. In the lower (<1MHz) frequency range, the electrolytic dominates the immittance of the tissues. At higher frequencies range, the dielectric properties of tissue start to dominate.

And the tissue properties become almost equal to pure water which has the relaxation frequency of around 18GHz [8].

Schwan was the first to correctly identify three main dispersions of bio-impedance spectrum due to three different dielectric relaxation mechanisms, and termed them as α-, β- and γ-dispersions [9]. And Fig. 1.1 shows the three dispersion phenomena in frequency response.

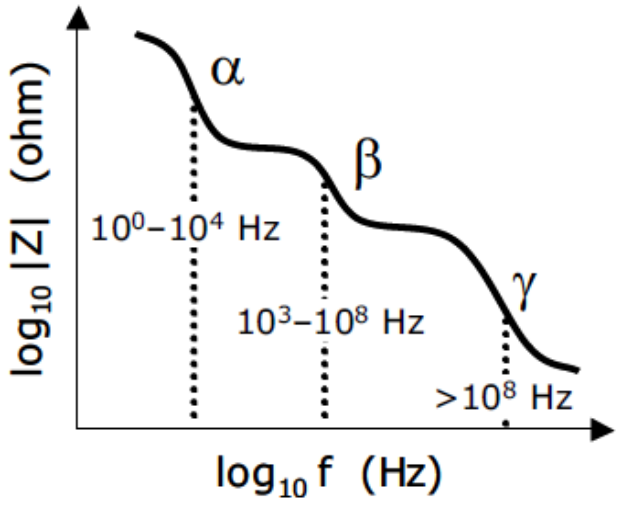


Fig. 1.1. Three dispersion phenomena in frequency response [9]

The α-dispersion (Hz to tens of kHz) reflects mainly polarization of ionic clouds around the cells. Structural membrane changes, oedema, and polarization of cell membranes affect the β-dispersion (kHz to hundreds MHz). The γ-dispersions (over hundreds MHz) reflects relaxation of water and other small molecules. Hence, the β-dispersion often contains most of the clinically relevant information, that why most of bio-medical testing method is based on the frequency range from kHz to MHz [10]. Consequently, the electrical impedance skin cancer detection system should target at the

frequency range from 100kHz to 10MHz, which also sets the specification for the sinusoidal oscillator designed in this work.

1.1.2 Electrical impedance spectrometer system

A general impedance spectrometer system scheme used for skin cancer detection is demonstrated in Fig. 1.2. And the whole system mainly consists of five parts: probe, signal conditioning circuit, amplitude/phase extractor, digital signal processing circuit and quadrature sinusoidal oscillators. Probe has the direct contact with skin tissue under test (TUT), and injects and gathers the electrical signals which pass through the skin tissue. Signal conditioning is to provide a good interface between probe and information processing module in good accuracy. As is mentioned that the skin cancer can be detected by a variation from a benign skin based on the amplitude and phase information over a certain frequency range change, the amplitude/phase extractor applied coherent demodulation to obtain the required information. A highly linear quadrature sinusoidal oscillator provides the reference signals for amplitude/phase extractor and signal conditioning circuit. DSP in the back-end will justify the condition of the skin tissue under test based on a certain programmed algorithm. In the following, each of the main modules is discussed in details to help the readers gain more understanding of this system.

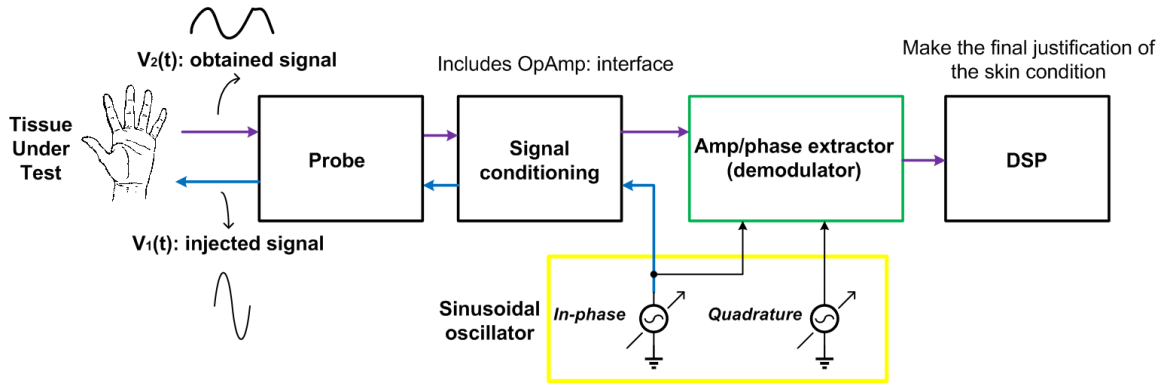


Fig. 1.2. A general impedance spectrometer system

a. Electrode probe

As visualized in Fig. 1.3, a hand-held probe with circular concentric electrodes is used in the testing experiments of impedance spectrometer [11]-[13]. There are four electrodes for this probe as A, B, C and D. The outmost two electrodes, C and D, are source electrodes. By distributing sourcing current of C and D electrodes, a "virtual" electrode is formed in between. An electrode is a current sink, which senses the electrical information which results from the virtual source electrode and passes through the tissue-under-test (TUT). B electrode is a guard electrode, which is used to reduce the surface current. By changing the distance between the virtual source electrode and the sink

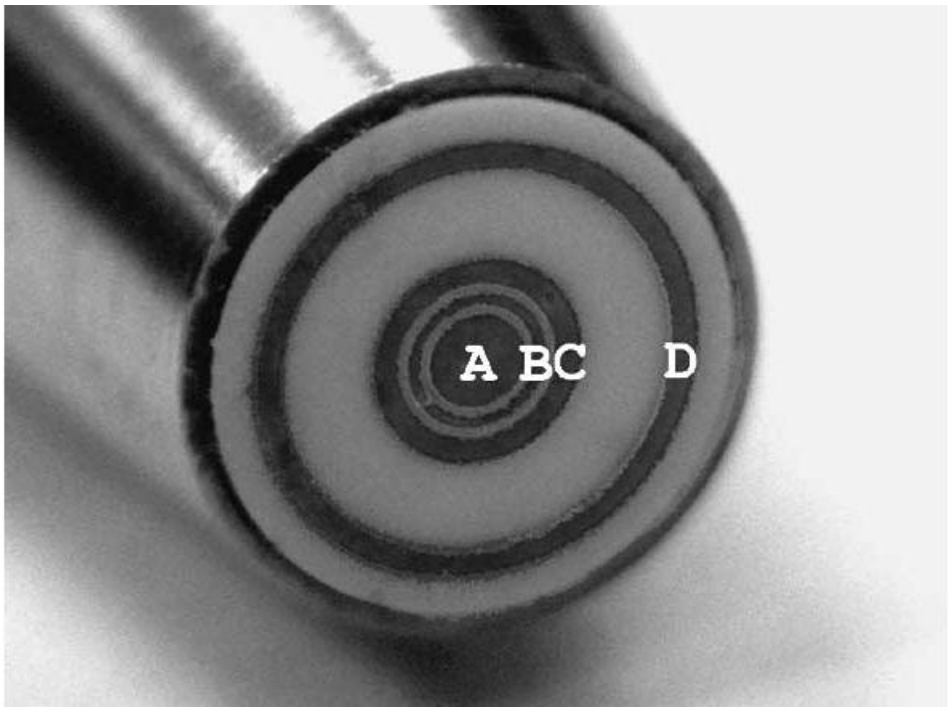


Fig. 1.3. Probe tip with impedance spectrometer [12]

electrode, the depth of skin which testing current can transmitted also varies. In this way, electrical information of skin tissue within some depth is connected by the impedance spectrometer probe. The rest is for the integrated circuit to process.

b. Signal conditioning circuit

The probe is the front end to inject the testing electrical signal and senses the signal modified by passing through TUT directly. The interface task between probe and signal processing module is carried by an analog signal conditioning circuit. In this circuit, a very pure sinusoidal signal, which can be in either voltage or current form is generated from the sinusoidal oscillator module, and then be injected into source electrode of the probe. Also, the system helps sink electrode of the probe collect new signal, which can

also be either voltage or current form. With all the transmitted and received information available, the coherent demodulator can extract the amplitude and phase information, and then passes it to DSP to obtain the clinical information for the final justification of skin condition.

For the impedance spectrometer system, four-terminal sensing, also known as Kelvin sensing, has better testing accuracy over the conventional two-terminal sensing as electrical impedance measuring technique. One auto balancing bridge skin cancer detection system is proposed in [10], as shown in Fig. 1.4, which helps understand how a signal conditioning circuit works.

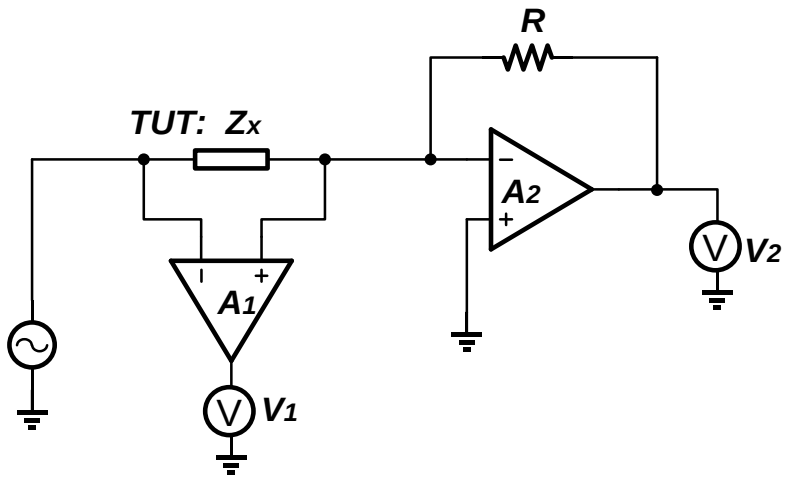


Fig. 1.4. Auto balancing bridge skin cancer detection system

The tissue-under-test (TUT) sample has impedance to be Z_x, which is targeted to be measured in this circuit. The AC current source injects a high linearity sinusoidal current into Z_x. A high gain instrumentation amplifier A_1 is used to buffer the two terminals across Z_x, and also conduct a differential to single ended conversion to generate a output voltage which be collected at voltage meter V_1. Another Opamp A_2 is used to do

I-V conversion, and translate the current flowing through Z_x to voltage information which can be measured in another voltage meter V_2. In this way, the impedance Z_x can be calculated from voltage across the sample and the output of Opamp A_2 which is proportional to the current flowing through the sample.

c. Coherent demodulation

By comparing injected sinusoidal signal $V_1(t)$ and the new signal $V_2(t)$ which is modified by the tissue, the amplitude and phase difference can be extracted and the bio-impedance of skin tissue is reflected. An intuitive idea to obtain the amplitude and phase information of signals is to employ a peak detector and phase detector in the measurement [14], [15]. However, considering the noisy environment for skin cancer detection, the approach is not suitable to tolerate the non-ideal condition. Instead, coherent demodulation is able to reject the noise and interference out of frequency of interest. In this scheme, the bio-impedance measurement is centered at some specific frequency within the bandwidth of some Hz every time. Because of this feature, coherent demodulation is employed in most situations [10]. The diagram of coherent demodulation is illustrated in Fig. 1.5, and the mathematical theory is explained as below.

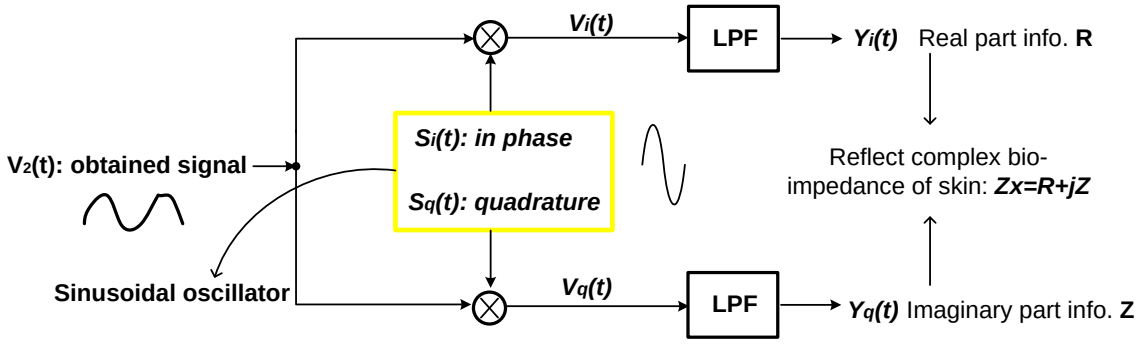


Fig. 1.5. Coherent demodulation scheme

First of all, suppose the measurement is based on some specific frequency as f_0. $V_2(t)$ is obtained from the voltage across the impedance Z_x by the injection of sinusoidal current $I(t) = I_{const}\cos(2\pi f_0 t)$. Impedance Z_x based on a certain frequency is a constant, which can be represented as:

$$Z_x = |Z_x|\cos(\theta) + j \cdot |Z_x|\sin(\theta) = R + jX$$

Where R and X are resistance and reactance of complex impedance Z_x respectively. And $V(t)$ can be expressed as:

$$V_2(t) = I(t) \cdot Z_x = |Z_x| I_{const} \cos(2\pi f_0 t + \theta)$$

$S_i(t)$ and $S_q(t)$ are in-phase and quadrature sinusoidal signals generated from sinusoidal oscillators, and can be represented as:

$$S_i(t) = A_{const} \cos(2\pi f_0 t)$$

$$S_q(t) = A_{const} \sin(2\pi f_0 t)$$

Through the demodulation from upper branch, it is obtained:

$$V_i(t) = V(t) \cdot S_i(t) = |Z_x| A_{const} I_{const} \cos(2\pi f_0 t)\cos(2\pi f_0 t + \theta)$$

$$= |Z_x| A_{const} I_{const} \frac{\cos(4\pi f_0 t + \theta) + \cos(\theta)}{2}$$

The low pass filter (LPF) has corner frequency which is far below f_0, so only the DC information is left as:

$$Y_i = |Z_x| A_{const} I_{const} \frac{\cos(\theta)}{2}$$

As a result, the resistance R of complex impedance Z_x can be expressed as:

$$R = |Z_x|\cos(\theta) = \frac{2Y_i}{A_{const} I_{const}}$$

Similarly, the reactance X of complex impedance Z_x can be calculated as:

$$X = |Z_x| \sin(\theta) = \frac{2Y_q}{A_{const} I_{const}}$$

Consequently, the real and imaginary part of bio-impedance is obtained, and phase and amplitude information can be derived.

d. Digital signal processing (DSP) module

First of all, a predefined mathematical model of skin is obtained and is used to deduce some critical skin parameters using a programmed algorithm. As the impedance spectrometer scans the patient's skin, the associated information is stored in DSP and a detailed image of scanned skin's properties is provided to health care professionals for diagnosis.

e. Sinusoidal oscillator

Sinusoidal oscillator is required to provide very linear sinusoidal signals with quadrature form. Considering this the work of design in the thesis, a detailed explanation will be illustrated as separate session as below.

1.2 Sinusoidal oscillator in impedance spectrometer system

From electrical bio-impedance measurement fundamental theories and the impedance spectrometer system introduction, some features are critically required for the sinusoidal oscillator. To cover the β-dispersion of skin tissue which has most useful information for clinical inspection, frequency range from 10kHz to 10MHz is desired. To provide the reference for coherent modulation scheme, the sinusoidal oscillator should generate quadrature outputs. Another critical specification is high spectral purity, or low

total harmonic distortion (THD) for the sinusoidal waveform. The importance of the purity performance is explained as below in the spectrum domain analysis:

Ideally, the spectrum of a pure sinusoidal waveform only includes one desired tone located as a certain frequency. After injecting this signal $V_1(t)$ through skin tissue, a new modified signal $V_2(t)$ is reshaped and obtained. Any amplitude and phase change for the new signal is used as the electrical information for the detection of skin cancer. The spectrum response of the two signals is indicated in Fig. 1.6.

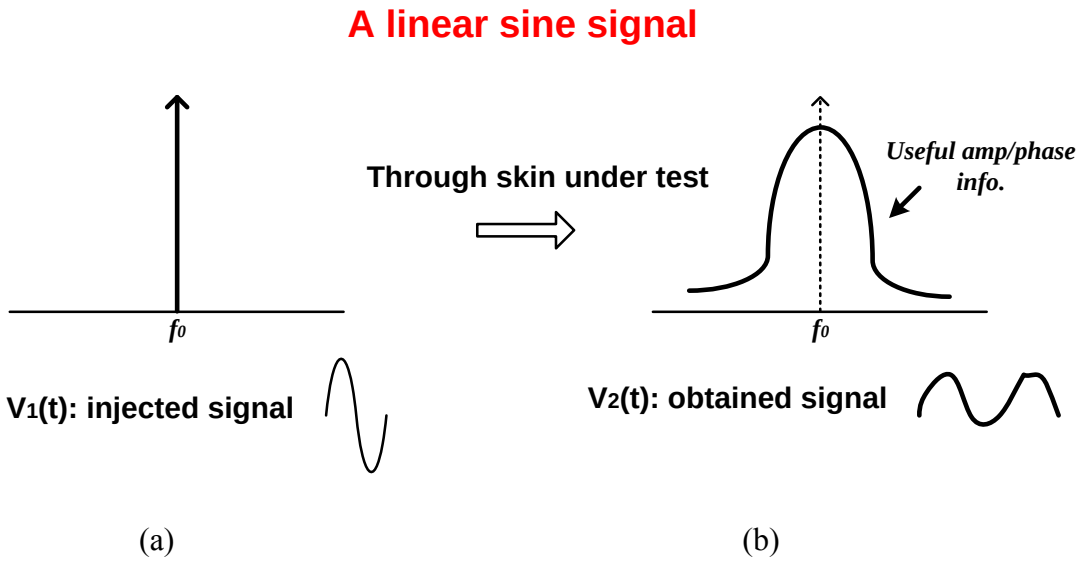
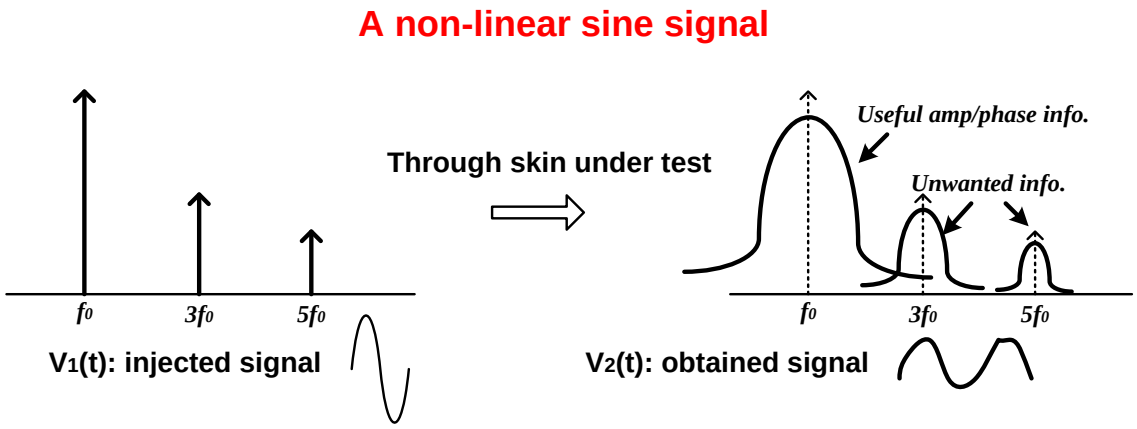


Fig. 1.6. Spectrum of injected and modified signal through tissue (ideal case)

In practical situation, the odd harmonics of the fundamental frequency, which are among the important non-ideality, will seriously harm the effectiveness and accuracy of skin cancer detection in impedance spectrometer. As is shown in Fig. 1.7(a), the sinusoidal oscillator output spectrum has main tone at f_0, and unwanted odd harmonics at $3f_0$, $5f_0$, etc. Each frequency tone is modulated by tissue sample separately and all of the

information is mixed together and folded to low frequency, which is named intermodulation effect. In this way, the demodulation system cannot extract the accurate amplitude and phase information from the mixed-up signal. And the credibility of the measurement is largely degraded. As a result, regarding purity of sine signal is demanded in the design, the THD specification is set to be less than -70dB.



(a) (b)

Fig. 1.7. Spectrum of injected and modified signal through tissue (practical case)

1.3 Thesis organization

This thesis is composed of five sections and organized as follows.

Section 1 provides a general background for sinusoidal oscillators. The proposed sinusoidal oscillator in this work targets at application in bio-impedance spectroscopy system. And main specifications of the design are discussed based on the requirement of the application.

Section 2 introduces the concept of a core design theory for sinusoidal oscillators named digital-harmonic-cancellation (DHC) technique. Several related works in literature as well as the design in this thesis are reviewed and summarized into two categories, feedback-based DHC technique and open-loop-based DHC technique.

Section 3 explains the mathematical algorithm behind the general DHC technique, and discusses how different design parameters affect the performance of sinusoidal oscillator. In addition, mismatch analysis is introduced to show how the non-ideality impacts on the accuracy of harmonic cancellation.

Section 4 presents the circuit level implementation of the work. In addition, some potential alternatives for each modules of the sinusoidal oscillator system are also introduced and analyzed.

Section 5 shows experimental results for design in OnSemi 0.5um technology and the simulation results for design in IBM 0.18um technology. A comparison of start-of-art is also listed in this section.

Section 6 concludes this work.

2. SINUSOIDAL OSCILLATOR DESIGN BACKGROUND

2.1 Background of conventional sinusoidal oscillator

Oscillators are used in many electronic systems to provide reference clock for sequential operation of the entire system. Based on the specific requirement for the test equipment, oscillators are designed to produce either sinusoidal signals, square, sawtooth or triangular shaped waveforms. In this thesis, sinusoidal oscillators which can generate a pure sinusoidal waveform with constant amplitude and frequency are discussed.

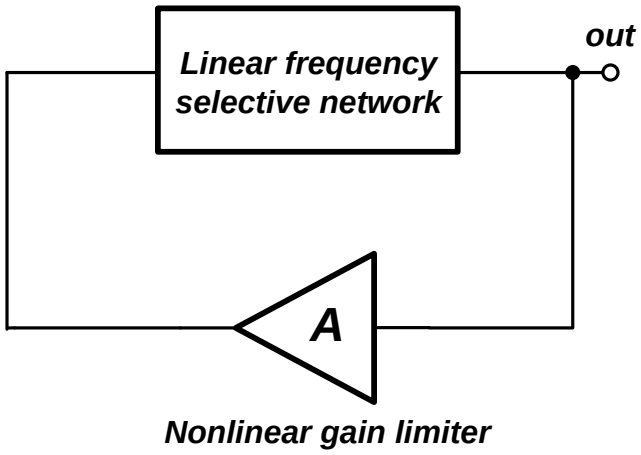


Fig. 2.1. Conventional sine wave generator block diagram

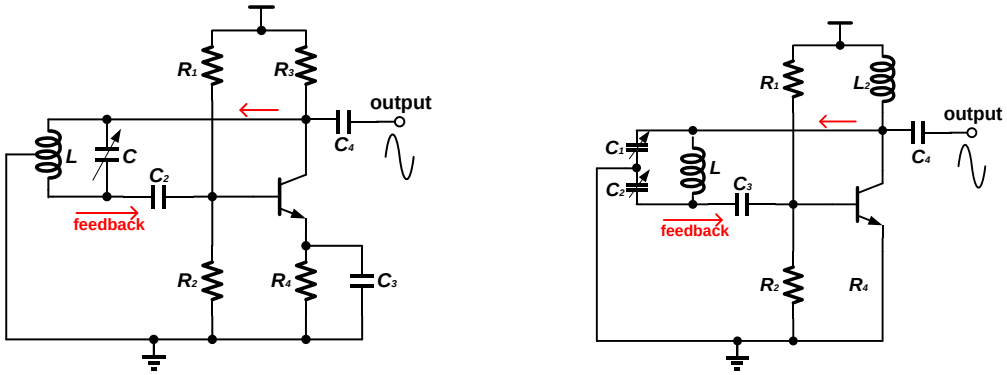
Fig. 2.1 shows the block diagram of a conventional sine wave generator, which consists of a linear frequency selective network and a nonlinear gain limiter. As for LC oscillator as an example, LC tank and a voltage amplifier made of Opamp, FET or bipolar devices corresponds to frequency selective network and nonlinear gain limiter

respectively. The output frequency is determined by the value of L and C within the LC tank as:

$$f = \frac{1}{2\pi\sqrt{LC}}$$

However, there is energy loss because of the non-ideality of L and C during each cycle of oscillation. To sustain the oscillation going in LC tank, the voltage amplifier, which is made of active devices, is used to replace the energy lost in each oscillation. To produce a constant oscillation of sinusoidal waveform, there must be automatic gain control for make sure the overall feedback loop gain is unity. Otherwise, the sinusoidal oscillation will die away to zero, or become clipped by the supply rails.

There are also some different ways to construct LC filter network and amplifier, with the most common to be Hartley LC oscillator and Colpitts LC oscillator, which are showed in Fig. 2.2. For these two types of sinusoidal oscillators, a technique named



(a) (b)

Fig. 2.2. (a) Hartley oscillator (b) Colpitts oscillator

automatic base bias, which can control the amplitude of oscillation, is involved. The technique works in such a way that if the oscillation increases, the biasing conditions change and the gain of amplifier decreases, and vice versa. As for the parallel LC resonator tank circuit, Hartley oscillator has the feedback to be achieved with an inductive divider, while Colpitts oscillator employs a capacitive divider.

Moreover, there are some other sinusoidal oscillator which uses a number of resistors and capacitors for the linear frequency selective network, such as Wien Bridge oscillator, which is showed in Fig. 2.3.

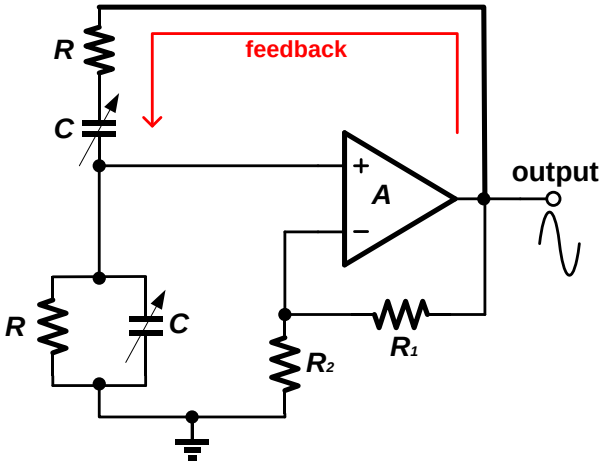


Fig. 2.3. Wien Bridge oscillator

For these conventional oscillators, the output purity of spectrum mainly relies on the filtering effect of the frequency selective network. Thus, the linearity of these sinusoidal oscillators is insufficient for many applications.

2.2 Background of sinusoidal oscillator with DHC technique

Nowadays, thanks to the fast scaling speed for the integrated-circuit (IC) technology, the performance of algorithm realized with digital circuits is tremendously improved. For instance, the digital nature makes the circuits unsusceptible to noise, as well as be faster, consume less power and silicon area with technology scaling. On the contrary, because of design complexity brought by reduced supply voltage and increased nonlinearity of transistors, analog circuits are deprived of many benefits from the trend of technology scaling. As a result, realizing some traditional analog circuits with digital approach has become an increasingly popularized topic recently. For example, all-digital PLL and DLL are already investigated and implemented. In this thesis, digital harmonic cancellation (DHC) technique, as an effective design methodology for sinusoidal oscillator design methodology is introduced. The fundamental algorithm of DHC technique and several important related works in literature are presented.

A typical sinusoidal oscillator implemented with DHC technique consists of two building blocks, DHC module and filter module. With DHC module, a set of different time-shifted square-wave signals is summed up, and some harmonics of fundamental tone are cancelled out for the spectrum response. A filter module is used to suppress the other harmonic tones which are unable to be compensated by DHC module. Finally, a sinusoidal signal which is free from harmonics is produced in this way.

The DHC technique, though briefly introduced above, can derive a number of variations for a specific sinusoidal oscillator design. And the different approaches can be categorized in the three aspects as follows. First of all, it can be either feedback-based architecture or open-loop-based architecture. Second, how the different phase-shifted

square-wave signals are chosen and how to sum them up can also derive different designs. For example, for the ratios of all summing phase-shifted signals, some are identical while the others are programmable. Thirdly, though it is intuitive to maintain the fundamental tone and suppress the harmonics, the work in [16] provides an innovative idea to emphasize on high order harmonic boosting, like 5^{th} and 7^{th}, to achieve large frequency span.

By "playing" with variable design factors with mathematical tools based on the harmonic cancellation idea, some novel changes can be explored for the system-level implementation of DHC technique. In the next, a conventional sinusoidal oscillator and three other works based on DHC technique are demonstrated. Also, the proposed design is also included with brief introduction for a general review and comparison with other works.

2.3 Basic examples of digital harmonic cancellation

2.3.1 Spectrum of different periodic signals

Digital harmonic cancellation technique can be based on different types of periodic signals, such as square wave, triangular wave and sawtooth. Thus, Fourier expansion analysis is applied to these different types of waveform to explore how the spectrum response does look like.

For any periodic function $f(t)$ with period of T, it can be expressed as:

$$f(t) = \frac{a_0}{2} + \sum_{n=1}^{\infty} a_n \cos(n\omega_0 t) + \sum_{n=1}^{\infty} b_n \sin(n\omega_0 t)$$

Where the Fourier parameters are:

$$a_0 = \frac{2}{T}\int_0^T f(t)dt \quad a_n = \frac{2}{T}\int_0^T f(t)\cos(n\omega_0 t)dt \quad b_n = \frac{2}{T}\int_0^T f(t)\sin(n\omega_0 t)dt$$

If $f(t)$ is an odd function, all a_n equals to 0, so the Fourier expansion only contains sine terms, and there is no phase shift for different harmonics.

a. Square wave signal

Square wave signal is the most common signal which is very convenient to be obtained from electronic circuit. The Fourier expansion can be expressed as:

$$f(t) = \frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}\sin(n\omega_0 t)$$

From the spectrum response shown in Fig. 2.4, only odd harmonics for sine terms are included. Because of the simplicity of the spectrum response, square wave signal is a conventional raw material used for harmonic cancellation.

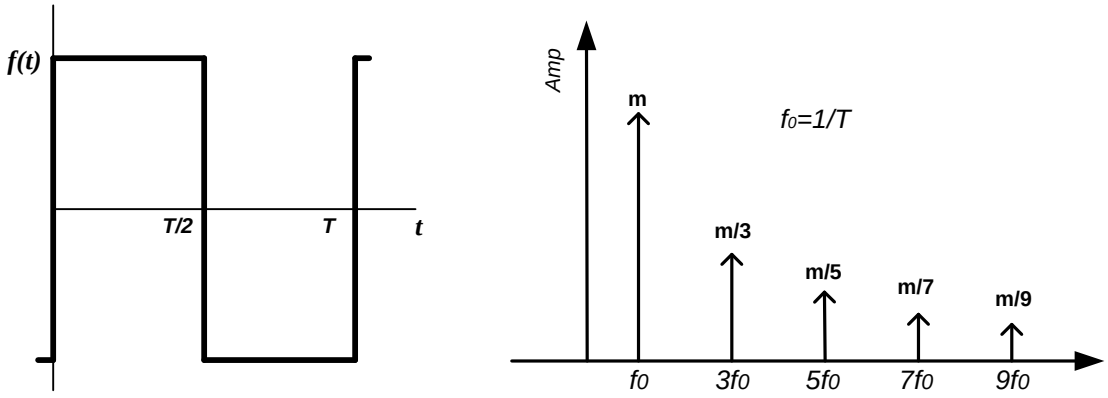


Fig. 2.4. Waveform and spectrum of square wave signal

b. Triangular wave signal

Triangular wave signal is another type of popular signals. The Fourier expansion can be expressed as:

$$f(t) = \frac{8}{\pi^2} \sum_{n=1,3,5...}^{\infty} \frac{(-1)^{(n-1)/2}}{n^2} \sin(n\omega_0 t)$$

From the spectrum response shown in Fig. 2.5, similar as square wave signal, only odd harmonics for sine terms are included. In addition, it has better intrinsic harmonic suppression for the harmonics, and the coefficients for harmonics are inversely proportional to square of harmonic sequences.

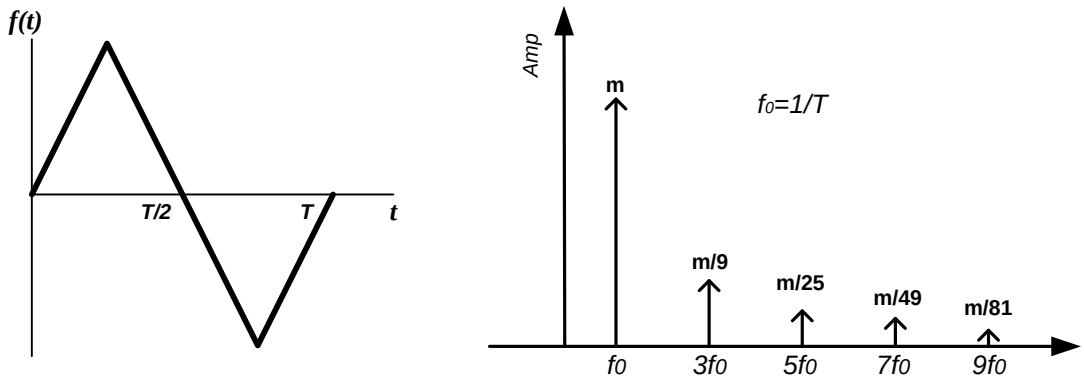


Fig. 2.5. Waveform and spectrum of triangular wave signal

c. Sawtooth signal

Sawtooth has the Fourier expansion to be expressed as:

$$f(t) = -\frac{1}{\pi} \sum_{n=1}^{\infty} \frac{1}{n} \sin(n\omega_0 t)$$

From the spectrum response shown in Fig. 2.6, as an odd function, only sine terms are included. However, even harmonics are still maintained along with odd harmonics. This type of signals is not preferred for digital harmonic cancellation technique.

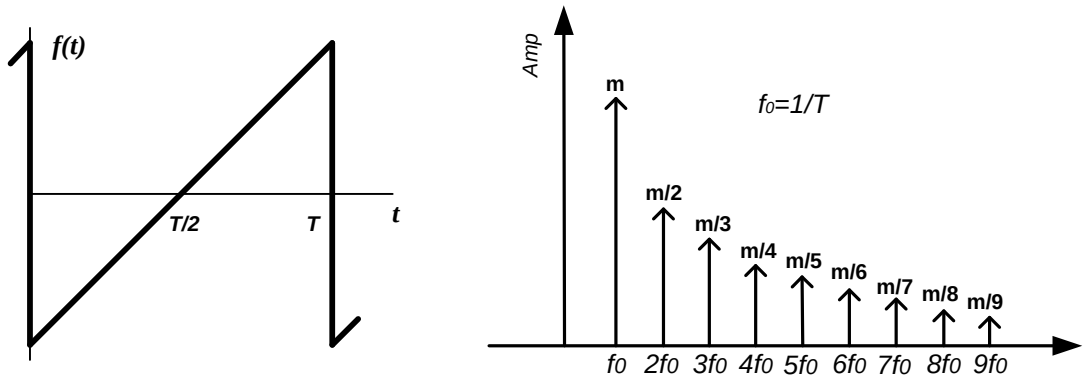


Fig. 2.6. Waveform and spectrum of sawtooth signal

d. Pulse train signal

As shown in Fig. 2.7, for pulse train signal with period of T, high level time of A and low level time of B, the Fourier expansion can be expressed as:

$$f(t)=\frac{1}{2}\frac{A-B}{A+B}+\frac{1}{\pi}\sum_{n=1}^{\infty}\left\{\frac{1}{n}\left[\sin(n\omega_0 A)\right]\cos(n\omega_0 t)+\frac{1}{n}\left[1-\cos(n\omega_0 A)\right]\sin(n\omega_0 t)\right\}$$

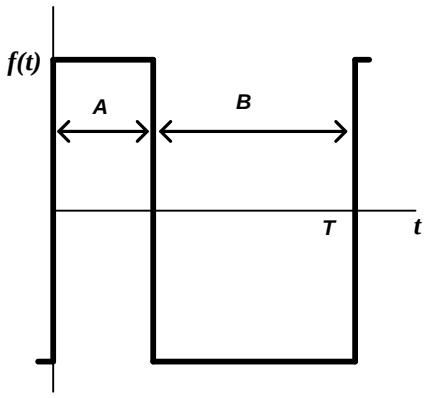


Fig. 2.7. Waveform of pulse train signal

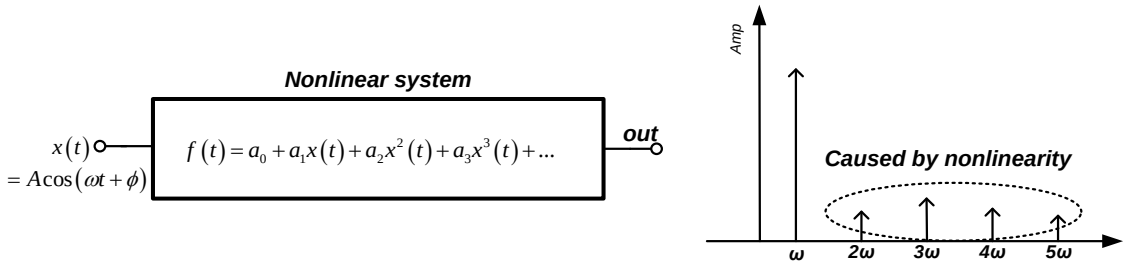
If the duty cycle is 50%, the signal is equivalent to a square wave signal. Otherwise, the signal is not an odd function and contains both sine terms and cosine terms for the Fourier expansion. In this case, this type of signals is not suitable for phase shifted summing to achieve harmonic cancellation effect.

For example, when duty cycle is 25%, the Fourier expansion can be expressed as:

$$f(t) = -\frac{1}{4} + \frac{1}{\pi}\sum_{n=1}^{\infty}\left\{\frac{1}{n}\left[\sin\left(n\cdot\frac{\pi}{2}\right)\right]\cos(n\omega_0 t) + \frac{1}{n}\left[1-\cos\left(n\cdot\frac{\pi}{2}\right)\right]\sin(n\omega_0 t)\right\}$$
$$= -\frac{1}{4} + \frac{1}{\pi}\left\{\left[\cos(\omega_0 t)+\sin(\omega_0 t)\right] + \frac{1}{2}\left[2\sin(2\omega_0 t)\right] + \frac{1}{3}\left[-\cos(3\omega_0 t)+\sin(3\omega_0 t)\right] + \ldots\right\}$$

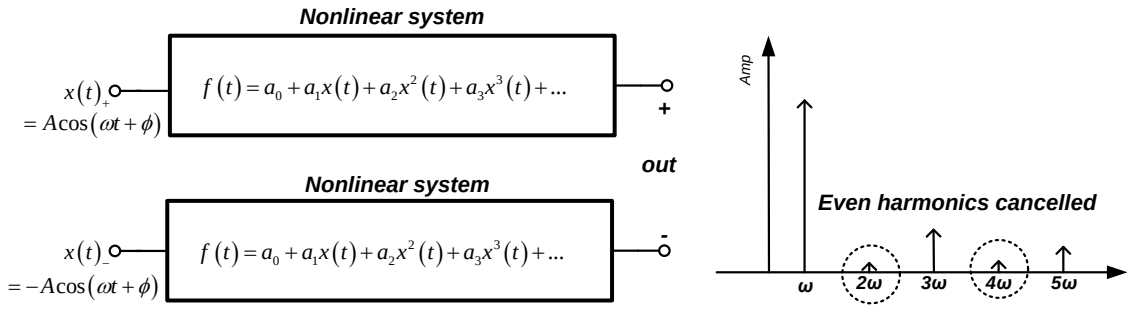
2.3.2 Differential mode cancels even harmonic

Differential periodic signals have the intrinsic function of even harmonics cancellation [28]. The diagram of comparison between a single ended nonlinear system and a differential mode nonlinear system is shown in Fig. 2.8.



(a)

Fig. 2.8. Diagram of (a) single ended and (b) differential mode nonlinear system



(b)

Fig. 2.8. Continued

Suppose a circuit is weakly nonlinear and its behavior can be described by a Taylor approximation as:

$$f(t)=a_0+a_1x(t)+a_2x^2(t)+a_3x^3(t)+...$$

Where $x(t)$ and $f(t)$ are the input and output of the nonlinear circuit respectively. And a_i are constants. If $x(t)=Acos(\omega t+\phi)$, and the ideal output signal is $a_1Acos(\omega t+\phi)$. However, due to the nonlinear terms, high order harmonics are obtained.

$a_2x^2(t)$ will give:

$$a_2x^2(t)=a_2\left(A\cos(\omega t+\phi)\right)^2=\frac{1}{2}a_2A^2\left(1+\cos\left(2\omega t+2\phi\right)\right)$$

$a_3x^3(t)$ will give:

$$a_3x^3(t)=a_3\left(A\cos(\omega t+\phi)\right)^3=\frac{1}{4}a_3A^3\left(3\cos\left(\omega t+\phi\right)+\cos\left(3\omega t+3\phi\right)\right)$$

For a differential signal pair, the input signals are $x(t)_+=A_0cos(\omega t+\phi)$ and $x(t)_-=-A_0cos(\omega t+\phi)$. By putting them into $a_2x^2(t)$ and $a_3x^3(t)$ expression, and use a subtraction operation between the differential terms as follows:

$$a_2\left[x(t)_+\right]^2 - a_2\left[x(t)_-\right]^2 = a_2\left(A\cos(\omega t+\phi)\right)^2 - a_2\left(-A\cos(\omega t+\phi)\right)^2 = 0$$

$$\begin{aligned} a_3\left[x(t)_+\right]^3 - a_3\left[x(t)_-\right]^3 &= a_3\left(A\cos(\omega t+\phi)\right)^3 - a_3\left(-A\cos(\omega t+\phi)\right)^3 \\ &= 2a_3\left(A\cos(\omega t+\phi)\right)^3 \end{aligned}$$

Finally it is obtained that the second harmonic term is cancelled out, and the third harmonic is remained. This operation is also valid for higher order harmonics. Consequently, all even harmonics can be removed with differential form of any periodic signals.

2.3.3 Phase-shifted periodic signal cancels out odd harmonics

The summing of phase shifted square wave signals and triangular wave signals can lead to useful cancellation of harmonics. And the comparison is made between the two types of summing signals in the spectrum response. Moreover, other types of signals, such as sawtooth signal and pulse train signal are also explored for digital cancellation technique.

a. Square wave signals

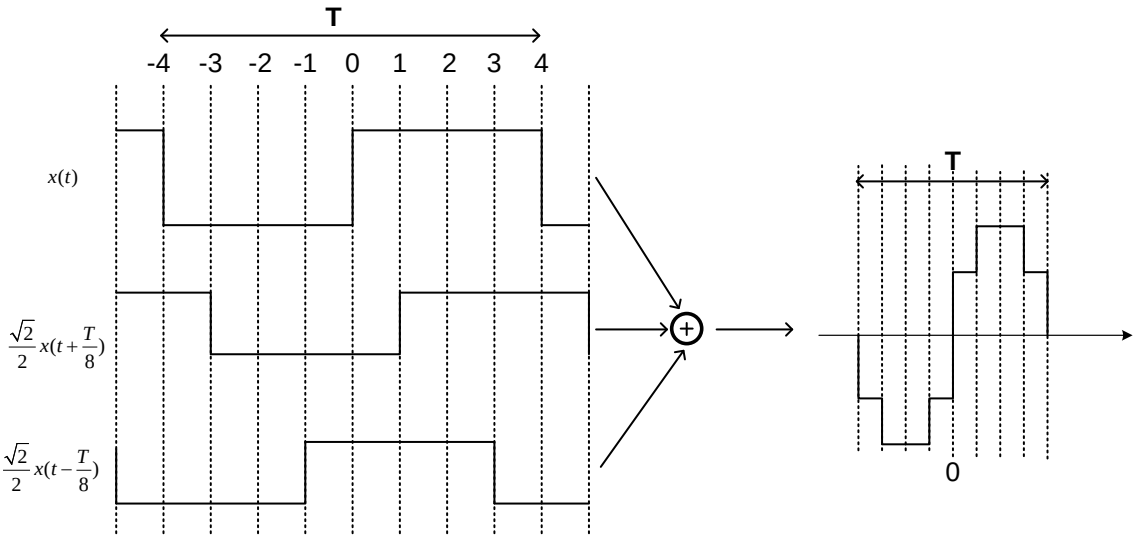


Fig. 2.9. Block diagram for odd harmonic cancellation (square wave)

Fig. 2.9 shows the summing of square-wave signals of same frequency but different phase shifts can cancel odd harmonic tones. $x(t)$ is the square-wave signal with no phase shift, $x(t+T/8)$ and $x(t-T/8)$ are square-wave signals with 45° and -45° phase shift. By summing them up with the coefficient of 1, $\sqrt{2}/2$ and $\sqrt{2}/2$ respectively, a new stair-case like signal is obtained as:

$$f(t) = x(t) + \frac{\sqrt{2}}{2}x(t+\frac{T}{8}) + \frac{\sqrt{2}}{2}x(t-\frac{T}{8})$$

The Fourier expansion of a square wave can be expressed as:

$$x(t) = \frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}\sin(n\omega_0 t)$$

As a result, the Fourier expansion of the summed stair-case signal can be expressed as:

$$\begin{aligned} f(t) &= \frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}\left[\sin(n\omega_0 t) + \frac{\sqrt{2}}{2}\sin\left(n\omega_0\left(t+\frac{T}{8}\right)\right) + \frac{\sqrt{2}}{2}\sin\left(n\omega_0\left(t-\frac{T}{8}\right)\right)\right] \\ &= \frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}\left[1+2\cdot\frac{\sqrt{2}}{2}\cos\left(n\omega_0\cdot\frac{T}{8}\right)\right]\sin(n\omega_0 t) \\ &= \frac{4}{\pi}\sum_{n=1,3,5...}^{\infty}\frac{1}{n}\left[1+\sqrt{2}\cos\left(n\cdot\frac{\pi}{4}\right)\right]\sin(n\omega_0 t) \end{aligned}$$

So the coefficient the n times harmonics can be expressed as:

$$C_n = \frac{4}{\pi}\cdot\frac{1}{n}\left[1+\sqrt{2}\cos\left(n\cdot\frac{\pi}{4}\right)\right]$$

Thus, when $n = 1$, the fundamental tone coefficient can be expressed as:

$$C_1 = \frac{4}{\pi}\left[1+\sqrt{2}\cdot\cos(\frac{\pi}{4})\right] = \frac{4}{\pi}\left[1+\sqrt{2}\cdot\left(\frac{\sqrt{2}}{2}\right)\right] = \frac{8}{\pi}$$

And the 3rd and 5th harmonic tone coefficients can be calculated for $n = 3$ and $n = 5$ as:

$$C_3 = \frac{4}{\pi}\cdot\frac{1}{3}\left[1+\sqrt{2}\cdot\cos(\frac{3\pi}{4})\right] = \frac{4}{\pi}\cdot\frac{1}{3}\left[1+\sqrt{2}\cdot\left(-\frac{\sqrt{2}}{2}\right)\right] = 0$$

$$C_5 = \frac{4}{\pi}\cdot\frac{1}{5}\left[1+\sqrt{2}\cdot\cos(\frac{5\pi}{4})\right] = \frac{4}{\pi}\cdot\frac{1}{5}\left[1+\sqrt{2}\cdot\left(-\frac{\sqrt{2}}{2}\right)\right] = 0$$

As a result, the 3rd and 5th harmonics can be fully cancelled out.

b. Triangular wave signals

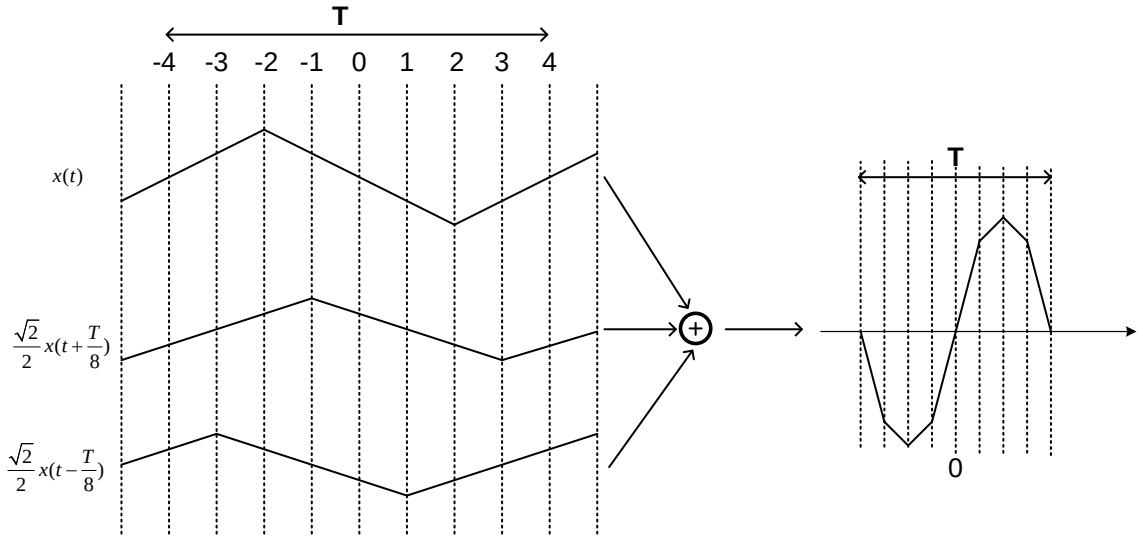


Fig. 2.10. Block diagram for odd harmonic cancellation (triangular wave)

Fig. 2.10 shows the summing of square-wave signals of same frequency but different phase shifts can cancel odd harmonic tones. For digital harmonic cancellation technique with triangular wave signal, it is obtained that:

$$x(t) = \frac{8}{\pi^2}\sum_{n=1,3,5...}^{\infty}\frac{(-1)^{(n-1)/2}}{n^2}\sin(n\omega_0 t)$$

The summation of three different phase-shifted triangular wave patterns can be obtained as:

$$f(t) = x(t) + \frac{\sqrt{2}}{2}x(t+\frac{T}{8}) + \frac{\sqrt{2}}{2}x(t-\frac{T}{8})$$
$$= \frac{8}{\pi^2}\sum_{n=1,3,5...}^{\infty}\frac{(-1)^{(n-1)/2}}{n^2}\left(1+\sqrt{2}\cdot\cos\left(n\cdot\frac{\pi}{4}\right)\right)\sin(n\omega_0 t)$$

So the coefficient the n times harmonics can be expressed as:

$$C_n = \frac{4}{\pi}\cdot\frac{(-1)^{(n-1)/2}}{n^2}\left[1+\sqrt{2}\cos\left(n\cdot\frac{\pi}{4}\right)\right]$$

The fundamental tone coefficient can be expressed as:

$$C_1 = \frac{4}{\pi}\frac{(-1)^{(1-1)/2}}{1^2}\left[1+\sqrt{2}\cdot\cos(\frac{\pi}{4})\right] = \frac{4}{\pi}\left[1+\sqrt{2}\cdot\left(\frac{\sqrt{2}}{2}\right)\right] = \frac{8}{\pi}$$

And the 3rd and 5th harmonic tone coefficients can be calculated as:

$$C_3 = \frac{4}{\pi}\cdot\frac{(-1)^{(3-1)/2}}{3^2}\left[1+\sqrt{2}\cdot\cos(\frac{3\pi}{4})\right] = \frac{4}{\pi}\cdot\left(-\frac{1}{9}\right)\left[1+\sqrt{2}\cdot\left(-\frac{\sqrt{2}}{2}\right)\right] = 0$$

$$C_5 = \frac{4}{\pi}\cdot\frac{(-1)^{(5-1)/2}}{5^2}\left[1+\sqrt{2}\cdot\cos(\frac{5\pi}{4})\right] = \frac{4}{\pi}\cdot\frac{1}{25}\left[1+\sqrt{2}\cdot\left(-\frac{\sqrt{2}}{2}\right)\right] = 0$$

As a result, the 3rd and 5th harmonics can be fully cancelled out.

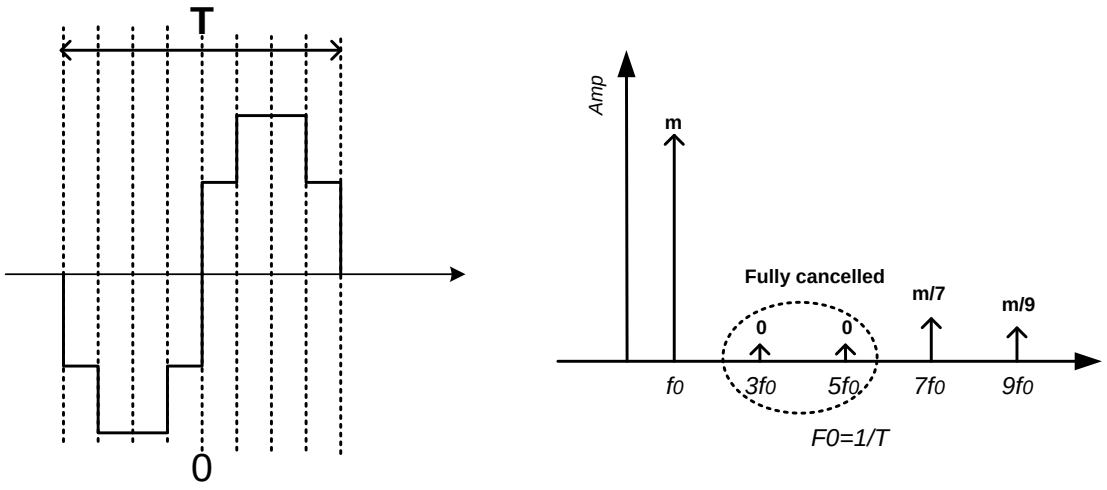
c. Conclusion

Both square wave signal and triangular signal can be expressed as:

$$x(t) = \sum_{n=1,3,5...}^{\infty} A_n \sin(n\omega_0 t)$$

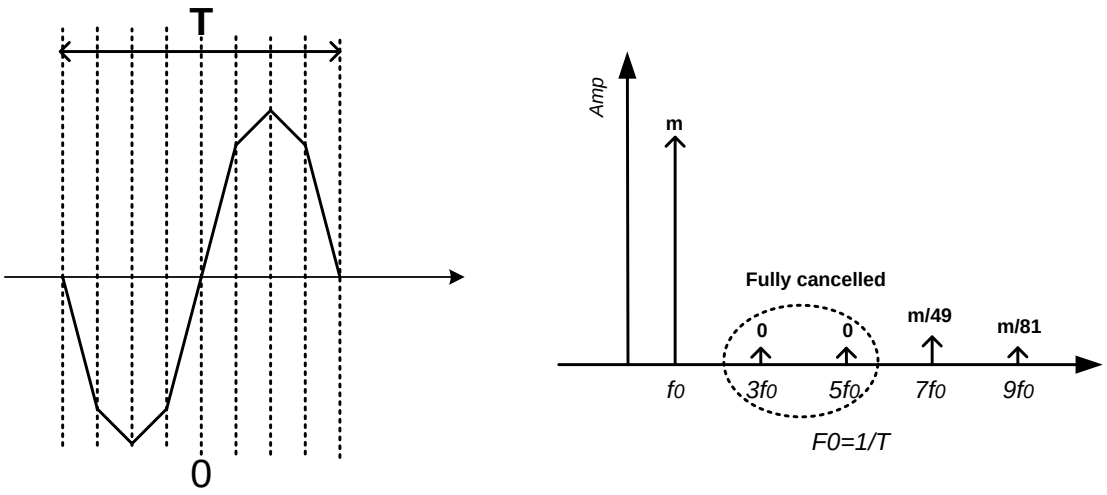
Where only odd time harmonics are included and the coefficient A_n can be any value. And the phase-shifted combination waveform $f(t) = x(t) + \frac{\sqrt{2}}{2}x(t+\frac{T}{8}) + \frac{\sqrt{2}}{2}x(t-\frac{T}{8})$ is

able to be eliminated from 3rd and 5th harmonics. However, for sawtooth signal with the Fourier expansion as $f(t) = -\frac{1}{\pi}\sum_{n=1}^{\infty}\frac{1}{n}\sin(n\omega_0 t)$, though 3rd and 5th harmonics can also be cancelled, the even harmonics still remain. As a result, sawtooth signal is not a suitable choice to fulfill digital harmonic cancellation. The waveform and spectrum response of the staircase like signal made of summing square waves and piecewise signal made of summing triangular waves are illustrated in Fig. 2.11. From the comparison of 7th and 9th harmonic coefficients, piecewise signal has better intrinsic suppression of harmonics than staircase like signal. From the mathematical algorithm, piecewise signal made of triangular wave signals are preferred. However, square wave signals are easy to obtain from circuit implementation.



(a)

Fig. 2.11. Waveform and spectrum of (a) staircase like signal and (b) piecewise signal



(b)

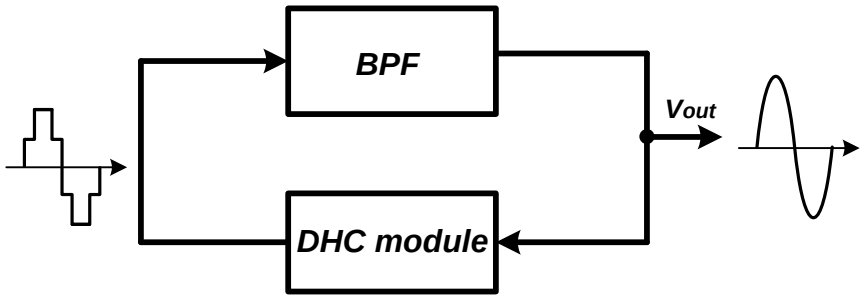
Fig. 2.11. Continued

By choosing more different phase shifts and proper summing coefficient, more harmonic tones can be removed. This algorithm will be studied in this thesis to show how to employ the digital harmonic cancellation technique to suppress the unwanted harmonics.

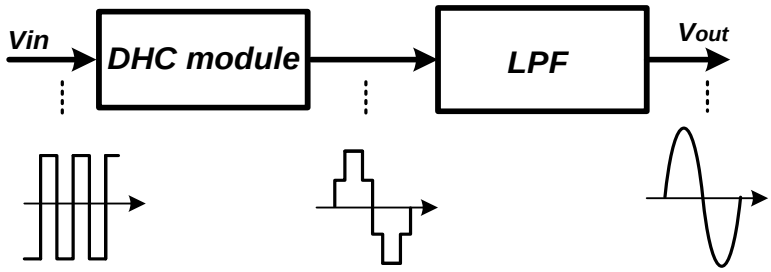
2.4 Two categories of sinusoidal oscillator

As is mentioned above, the sinusoidal oscillator designs can be divide into two categories, feedback-based architecture and open-loop-based architecture. Feedback-based architecture is very straightforward, and a popular theory named Barkhausen criterion provides insight into how a general oscillator can be obtained from a positive feedback system. In contrast, open-loop-based architecture processed a square-wave clock signal from input to produce a sinusoidal waveform at output.

The diagrams of sinusoidal oscillator of the two architectures and signal waveforms are illustrated in Fig. 2.12. As is observed, both of them include a DHC module and a filter module, but they are connected in a different style.



(a)



(b)

Fig. 2.12. Block diagram of sinusoidal oscillator with (a) feedback-based architecture (b) open-loop-based architecture

2.5 Sinusoidal oscillator with feedback-based architecture

Barkhausen stability criterion is a mathematical condition which determines whether a system will oscillate or not. It is widely used in the prevention of unwanted ringing or oscillation in the design of general negative feedback systems, such as OpAmp. In addition, it also helps in the design of oscillators by amplifying random

electrical elements, such as noise in a positive feedback system. The criterion is stated as follows:

From the diagram of feedback system in Fig. 2.13, the transfer function of the feedback system is:

$$T(s) = \frac{Vout(s)}{Vin(s)} = \frac{H(s)}{1 - H(s)\beta(s)}$$

A steady-state oscillation will be sustained if the following conditions are satisfied:

- The total loop gain is: $|H(s)\beta(s)| = 1$.
- The total loop phase shift is: $\angle H(s)\beta(s) = n \times 360° \ (n = 1,2 \ldots)$.

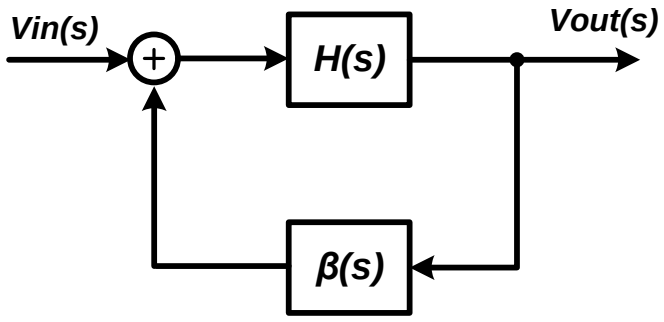


Fig. 2.13. Block diagram of a feedback system

Generally, almost all kinds of oscillators, including LC oscillators and ring oscillators are designed to satisfy the two Barkhausen criterion conditions. However, the "oscillation" only indicates a constant periodic signal without defining the shape of the waveform. In most situations, the output from these oscillators is buffered to result in a square-wave signal, which can be used as a clock reference for many electronic systems.

And obviously, for a sinusoidal oscillator, the harmonics which accompany the fundamental frequency tone are undesired and should be removed as much as possible.

A feedback-based oscillator with comparator and BPF is one effective solution to realize a "genuine" sinusoidal oscillator. According to the type of comparator employed in the system, two feedback-based sinusoidal oscillators are discussed.

2.5.1 Feedback-based sinusoidal oscillator with two-level-comparator

This feedback-based sinusoidal oscillator, as illustrated in Fig. 2.14, consists of a high Q-factor BPF and a basic two-level voltage comparator [17]. This implementation is not included in the category of DHC design, because there is no reshaping effect for the square-wave signal at comparator output to cancel harmonics. But it provides insight into how the feedback-based sinusoidal oscillator is formed and sets the basis for a similar work based on DHC technique which will be explained later.

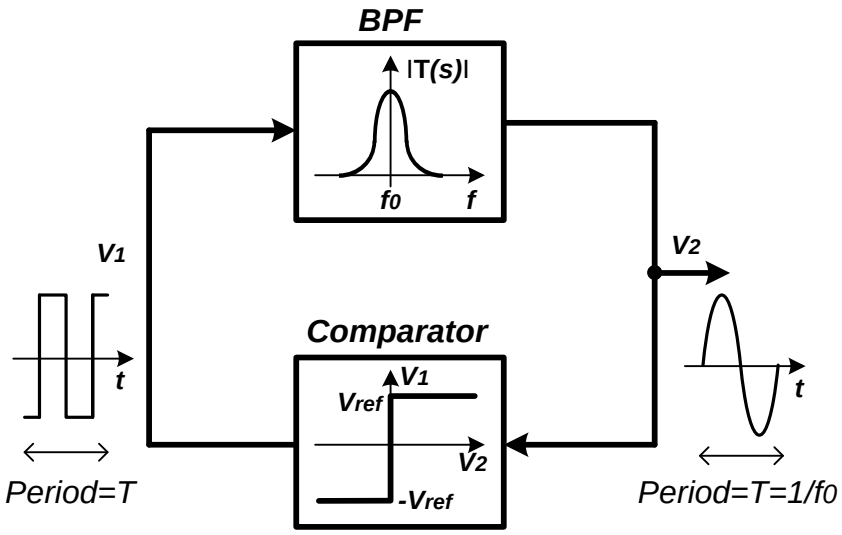


Fig. 2.14. Feedback-based sinusoidal oscillator with two-level-comparator

For the sinusoidal oscillator, it is assumed that there is a start-up mechanism which sets up the initial oscillation. Small signal analysis can be applied at the initial oscillation phase. Assume the transfer function of BPF and comparator can be expressed as:

$$\text{BPF: } T(s) = -\frac{ks}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}; \quad \text{Comparator: } \beta$$

Considering comparator is a nonlinear block, the correlated voltage gain β is amplitude dependent, which is assumed to be a constant for a specific amplitude input for small signal analysis. As a result, the close loop transfer function can be expressed as:

$$F_{cl}(s) = \frac{T(s)}{1+T(s)\beta} = \frac{-\frac{ks}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}}{1-\frac{ks}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}\beta} = -\frac{ks}{s^2 + (\frac{\omega_0}{Q} - k\beta)s + \omega_0^2}$$

To sustain continuous oscillation, the close loop transfer function must have RHP poles, so it is obtained that:

$$\frac{\omega_0}{Q} - k\beta < 0 \Rightarrow \beta > \frac{\omega_0}{kQ}$$

As is shown in Fig. 2.15, when the amplitude of oscillation signal increases, the comparator gain β decreases, and thus the complex poles move to imaginary axis finally.

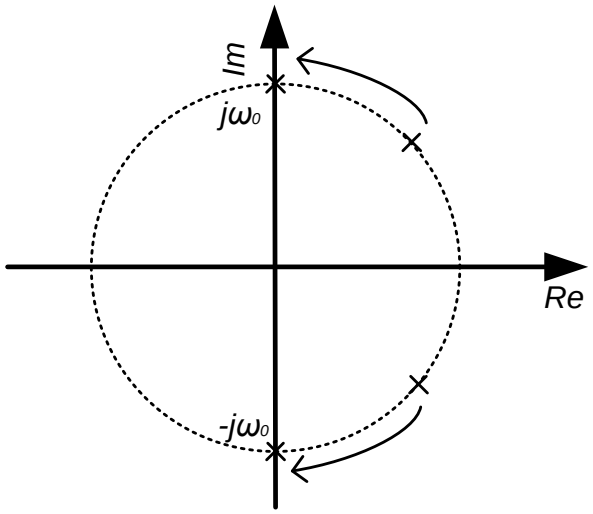


Fig. 2.15. Root locus when oscillation amplitude increases

When the oscillation signal increases to some extent, large signal analysis is applied. During every feedback cycle when square-wave signal V_1 , which is the output of the comparator, is filter by the high Q-factor BPF to generate V_2, the frequency elements close to f_0 are maintained while the rests are suppressed in the frequency domain. Next, when the filtered signal V_2 goes into the two-level-comparator as input, a square-wave signal V_1 is produced. And V_1 contains a number of new spectrum elements for the BPF for selection. Thus, no matter whatever V_1 and V_2 spectrum is initially, for every cycle of the circulation, the f_0 tone is enforced and other frequency tones are suppressed. After a period of time, a pure and sustained sinusoidal waveform with frequency of f_0 is formed at. V_2, while V_1 is a 50% duty cycle square wave, which also has frequency of f_0.

The high Q-factor is a design difficulty for the feedback-based sinusoidal oscillator. It not only sets the oscillation frequency f_0, but also the linearity of the

sinusoidal signal is heavily dependent on the Q-factor of BPF Switched-capacitor (SC) filter is preferred for BPF design due to its accuracy and reduced sensitivity to process variation.

The view of spectrum of V_1 and V_2 as BPF input and output, which appears in Fig. 2.16, can help understand how the linearity of the generated sinusoidal signal is concerned for this design.

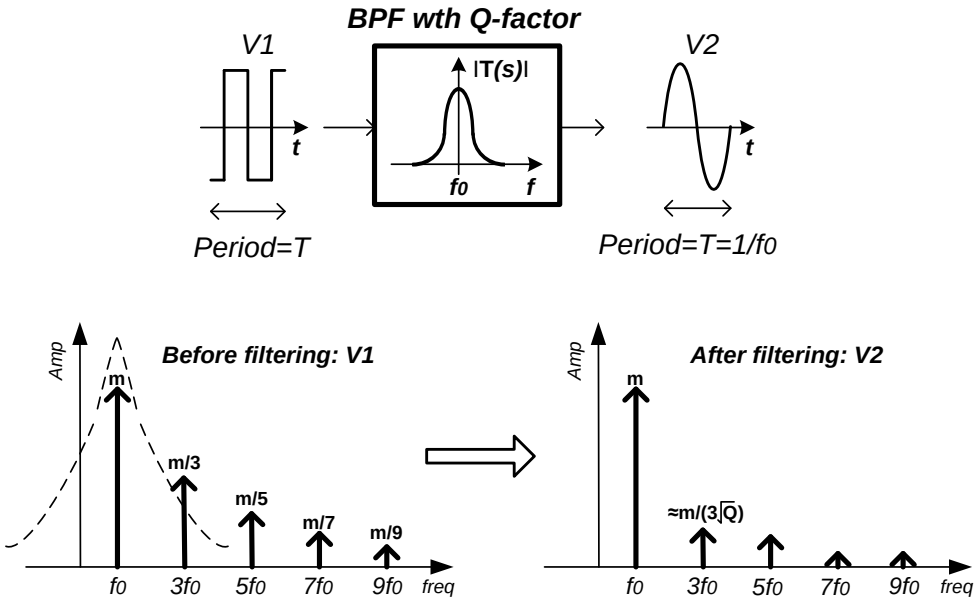


Fig. 2.16. Spectrum response of BPF input and output signals

It is observed that a high Q-factor BPF, which has a narrow frequency shaping function, means much suppression for the harmonics. For a BPF with a certain Q-factor, the harmonic distortion (HD) specification of n times harmonic tone can be expressed as:

$$HD_n \approx \frac{1}{n^2 Q}$$

Where $1/n^2$ is contributed by intrinsic harmonic suppression of the square-wave, which is constant, while $1/Q$ is contributed by BPF, which is designable based on the overall HD requirement. Fig. 2.17 shows the HD3 of the oscillator versus the quality factor of the BPF.

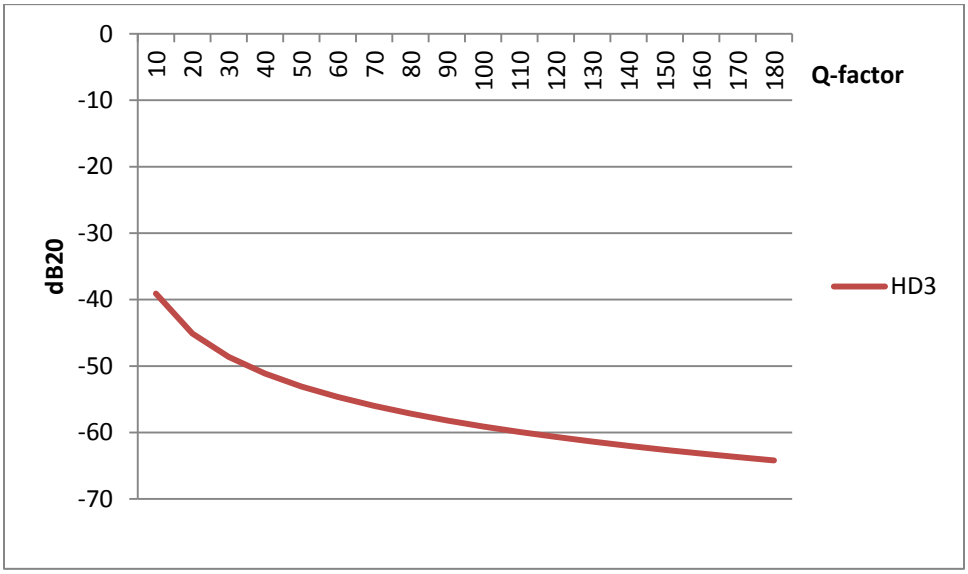


Fig. 2.17. HD3 versus Q-factor

For example, to realize HD3 = -50dB, Q-factor is required to be 35. However, a BPF with a larger Q-factor implies more complicated design, more power consumption and chip area occupation. For practical circuit implementation, Q-factor is fairly difficult to exceed 10. Consequently, the feedback-based sinusoidal oscillator with two-level-comparator has limited applications due to the restraint of linearity.

2.5.2 Feedback-based sinusoidal oscillator with multi-level-comparator

Fig. 2.18 shows an improved feedback-based sinusoidal oscillator which employs a multi-level comparator. Multi-level-comparator acts as a DHC module, which is able to

cancel out some harmonics, and thus relieving the design pressure of the BPF with high Q-factor.

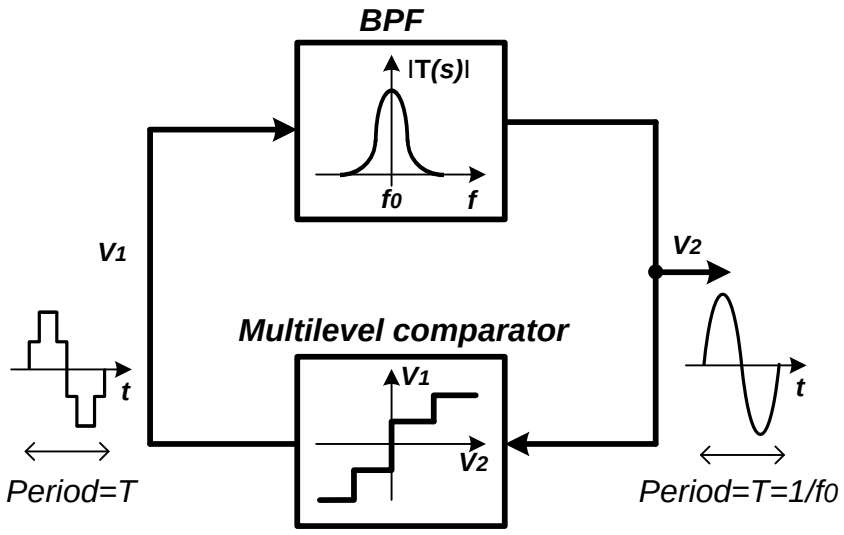


Fig. 2.18. Feedback-based sinusoidal oscillator with multi-level comparator

As for the multi-level-comparator, several clamping levels for different threshold voltages are included. With the modulation effect of this comparator, V_1 is no longer a square wave but a staircase-like waveform. With investigation of the spectrum of V_1, it is observed that some of the unwanted harmonics for V_1 can be largely suppressed by choosing the proper clamping levels and threshold voltages for comparator. Fig. 2.19 shows spectrum response of the work in [18] which employs a four-level comparator, and 3rd and 5th harmonics can be fully cancelled out. The higher harmonics, though left uncompensated from DHC module, are comparatively far away from the fundamental tone. Thus they are be suppressed with the BPF, which demands a smaller Q-factor than the counterpart with two-level-comparator. The experimental results show that for both

oscillators with equal Q-factor of 10, there is 20dB improvement on HD3 for multi-level-comparator-based oscillator over the conventional one.

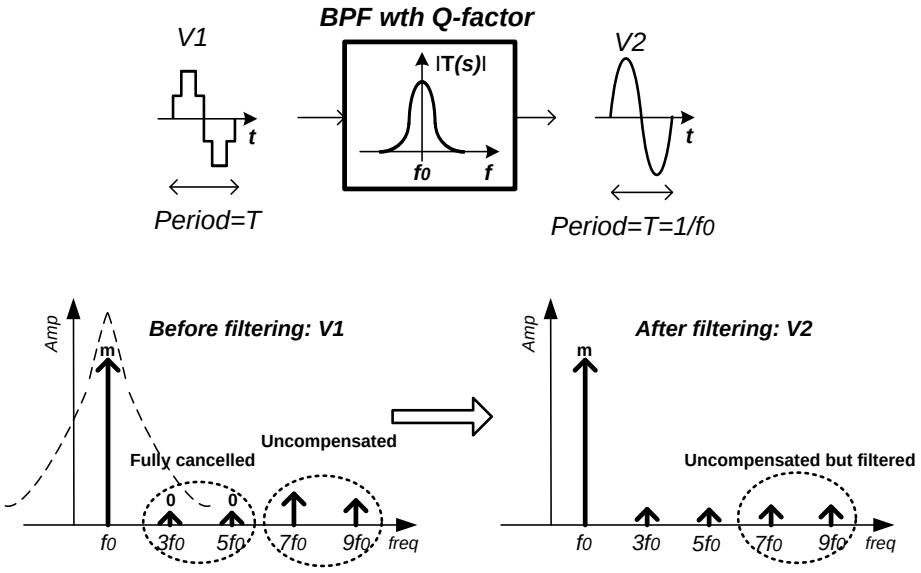


Fig. 2.19. Spectrum response of BPF input and output with multi-level comparator

Ideally, it is feasible to design a multi-level comparator with more clamping levels and improved harmonic cancellation for higher order tones. However, not only increased design complexity is involved, but also there is a limitation of matching accuracy for circuit implementation. For example, the four-level comparator has the clamping level ratios to be $1:\sqrt{2}$, which can only be realized with the approximation of some integer ratios. Moreover, SC BPF design of large Q also suffers from linearity, output swing and power consumption problems.

2.6 Sinusoidal oscillator with open-loop-based architecture

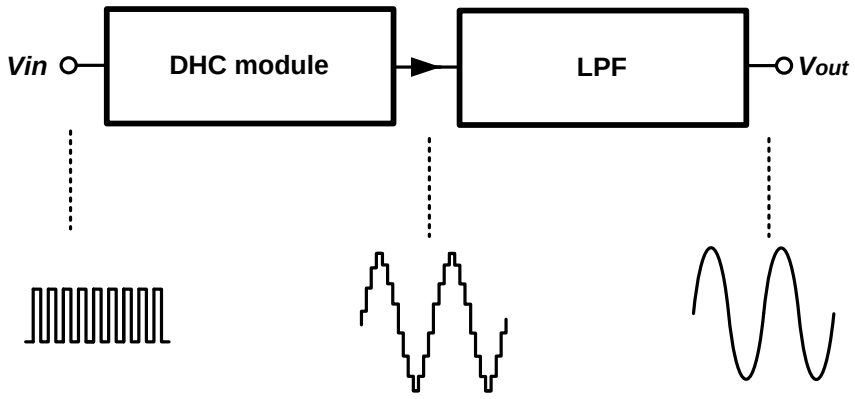


Fig. 2.20. Sinusoidal oscillator with direct-loop-based-architecture

As is shown in Fig. 2.20, sinusoidal oscillator with open-loop architecture processes a square-wave signal provided by a frequency synthesizer with a DHC module and a filter module, and a sinusoidal signal is obtained at output. The design difficulty of DHC module in open-loop-based architecture can be largely relaxed compared to multi-level comparator in the feedback-based oscillator. And a better harmonic cancellation performance can be demonstrated. Moreover, the filter module requirement for the open-loop-based architecture can be also lessened, and a basic passive filter is sufficient for the design. Due to the digital nature of the design, in more advanced technology, the oscillator can be easily redesigned and will outperform in power consumption, area size, etc.

Two works based on open-loop-based architecture from published papers [4] and [16] are presented, and also the work of this thesis is discussed.

2.6.1 Time-mode-based sinusoidal oscillator

A novel time-mode-based sinusoidal oscillator is proposed in [4], which can obtain sinusoidal output with frequency range up to 10MHz and THD of -72dB. The block diagram of the design is visualized in Fig. 2.21. The input of the system is a very high frequency square-wave signal with cycle period of T_{clk}. Four pairs of complementary square-wave signals are generated from the input clock with cycle period of $T_{cycle} = N \cdot T_{clk}$ and time shift sequence defined as $[\pm m_0, \pm m_1, \pm m_2, \pm m_3]$. The next, these different time-shifted square-wave signals are summed up to form the staircase–like signal. The highlight of this technique is that the summing coefficient for each time shift signal is identical, and time shift sequence is the only design parameter.

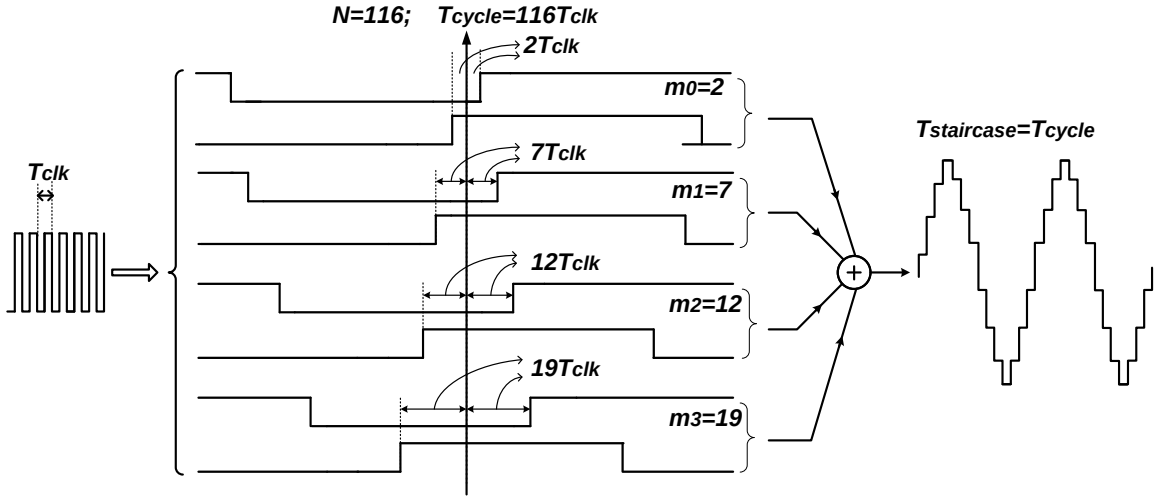


Fig. 2.21. Block diagram of time-mode-based sinusoidal oscillator

A search algorithm of finding an appropriate set of time shifts is executed in a mathematical program. Finally, $N = 116$ and $[\pm m_0, \pm m_1, \pm m_2, \pm m_3] = [\pm 2, \pm 7, \pm 12,$

± 19] are selected to generate a low THD sinusoidal output signal. And the corresponding phase shift mode can be represented as $[\pm 6.2°, \pm 21.7°, \pm 37.2°, \pm 59.0°]$.

From the spectrum view of the input and output of DHC module shown in Fig. 2.22, the target specification is THD can be expressed as:

$$THD = \frac{\sqrt{A_3^2 + A_5^2 + A_7^2 + A_9^2 + \ldots}}{A_1}$$

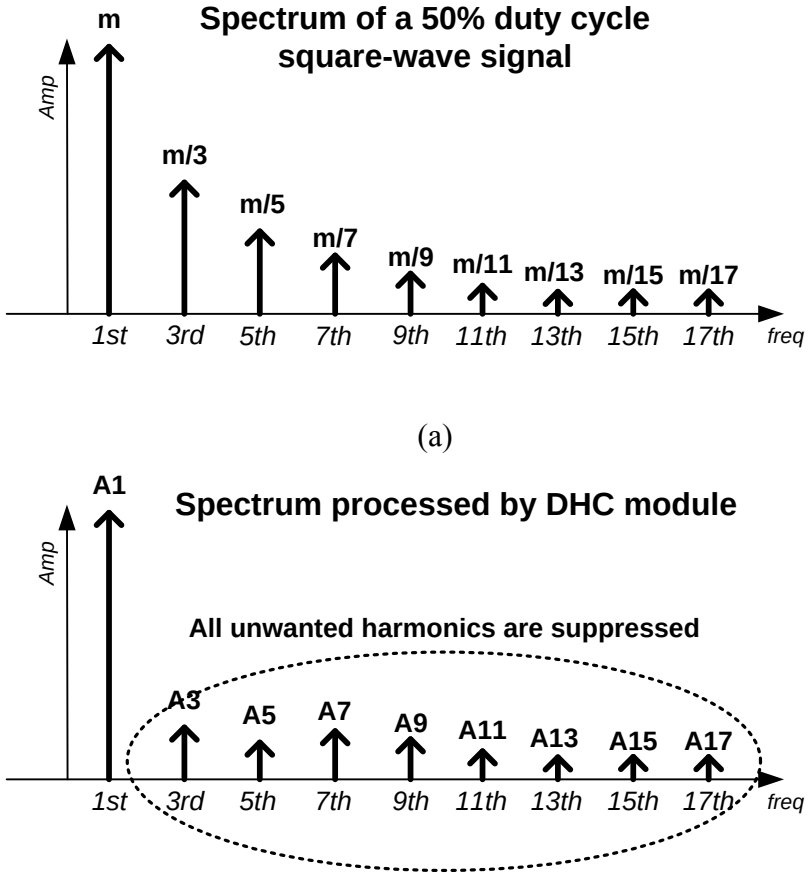


Fig. 2.22. Spectrum of (a) input and (b) output of DHC module

The accurate harmonic cancellation spectrum is plotted in Fig. 2.23. The low order harmonics, such as 3rd and 5th are largely suppressed. The high order harmonics, though not greatly eliminated, can be further reduced with the help of LPF.

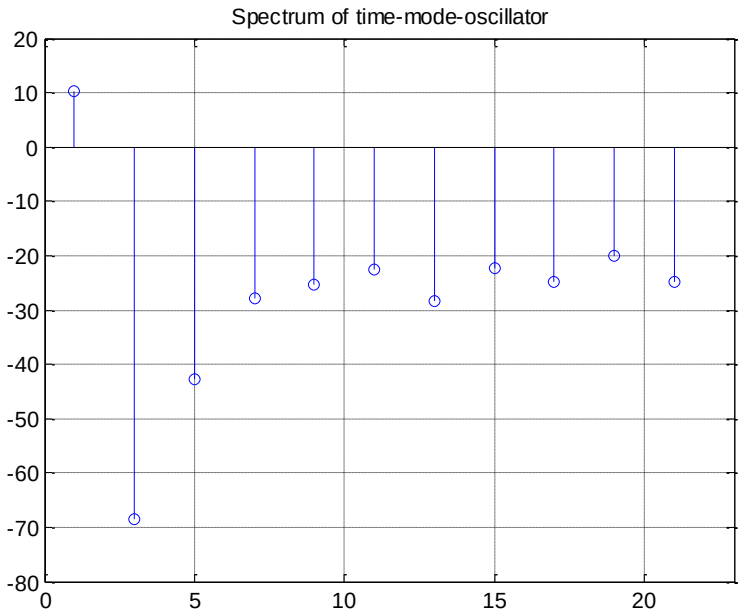


Fig. 2.23. Spectrum of signal after DHC with Matlab

For the circuit implementation, the high frequency clock input is used to trigger a counter that divides the clock frequency by N, and then generate the required time shift sequence square-wave patterns with some other static logic circuitry. So with the speed limitation of a certain CMOS technology, N cannot be very large. Otherwise, the high frequency input clock is unable to be normally processed.

Moreover, $n = 4$ pairs of complementary phase shift signals are summed up. Ideally, more phase shift signals can be selected and a better harmonic suppression can be achieved. However, more phase shift signals indicate more flip-flops and summing

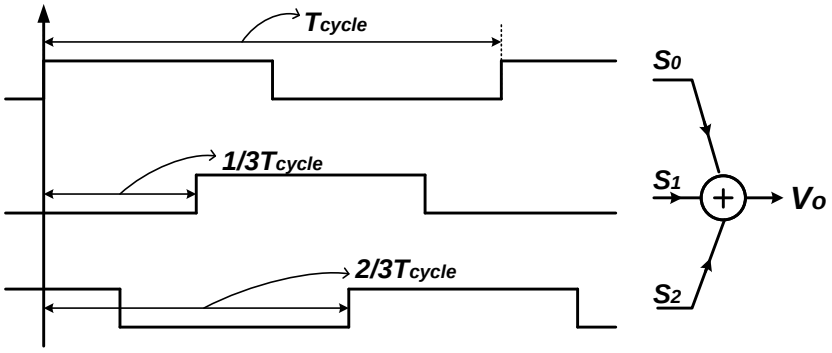
resistors are required. And at the same time, the mismatch issue will degrade and the better harmonic suppression effect will be overshadowed by the nonlinearity in this way.

The time-mode-based sinusoidal oscillator has the purity of the output sinusoidal signal which solely relies on the time accuracy of CMOS circuit. However, it is also noticed that the design parameter $N = 116$ means a 1.16GHz square-wave reference clock is required to produce a 10MHz sinusoidal output, which is inefficient for a sinusoidal oscillator. So this is not a practical implementation for harmonic cancellation technique.

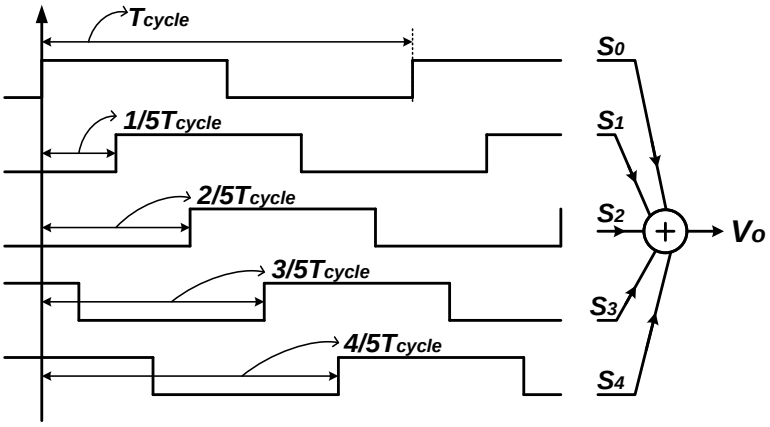
2.6.2 High-order-harmonic-boosting sinusoidal oscillator

Another innovative DHC technique named high-order-harmonic-boosting selects one of a high order harmonic, such as 3rd, 5th or 7th harmonic as the target output frequency tone, while suppressing the other harmonics as well as the fundamental tone.

As a general open-loop-based DHC technique, the harmonic cancellation operation is processed by summing up different time-shifted square-wave signals. Fig. 2.24(a) and Fig. 2.24(b) show the block diagram for 3rd harmonic boosting and 5th harmonic boosting respectively. And Fig. 2.25 demonstrates the corresponding phase diagram. Suppose the input clock period is T_{clk}. For the 3rd harmonic boosting case, three square-wave patterns with time shift sequence $[0, \frac{1}{3}T_{clk}, \frac{2}{3}T_{clk}]$ are generated and summed up. As is observed from the corresponding frequency response shown in Fig. 2.26(d), 3rd harmonic and its odd harmonics, such as 9th, 15th harmonics are maintained while the rest are cancelled. After the DHC module, a filter is employed to keep the 3rd harmonic tone while eliminating the others. As for 5th harmonic boosting, a similar operation is carried while 5th harmonic is selected to be maintained.

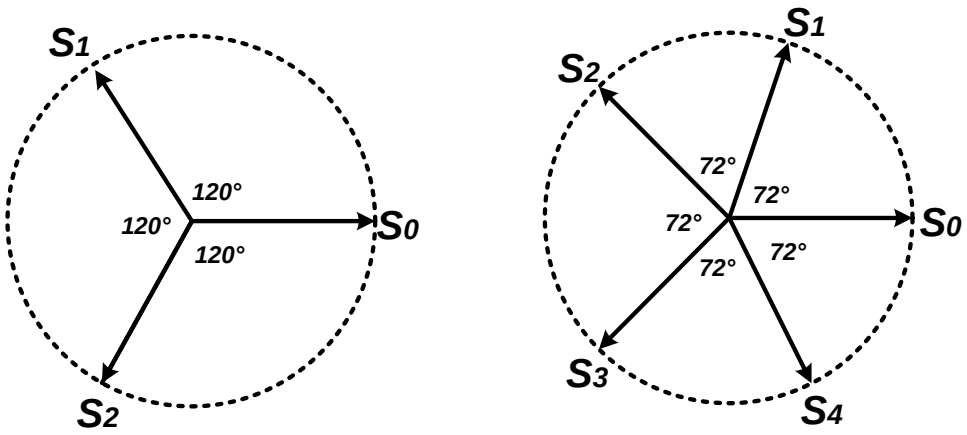


(a)



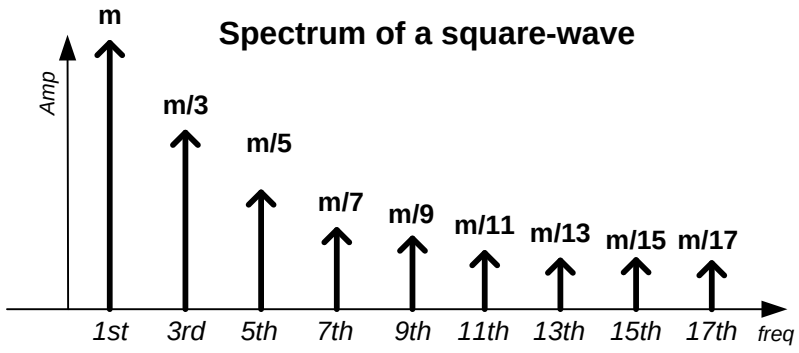
(b)

Fig. 2.24. Phase shifted waveform summing operation for (a) 3rd harmonic boosting (b) 5th harmonic boosting

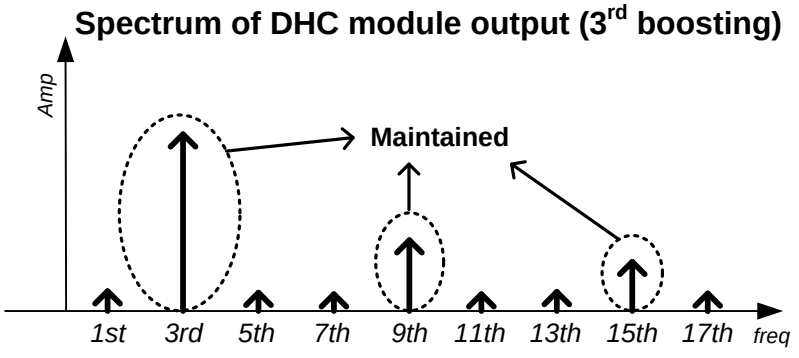


(a) (b)

Fig. 2.25. Phase diagram for (a) 3rd harmonic boosting (b) 5th harmonic boosting

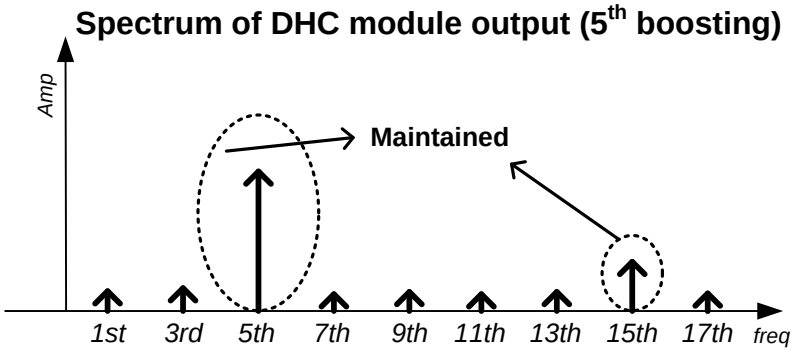


(a)



(b)

Fig. 2.26. High order harmonic selection technique spectrum (a) input spectrum and spectrum after DHC module with (b) 3rd harmonic boosting (c) 5th harmonic boosting



(c)

Fig. 2.26. Continued

For a work in the paper [16], 5th and 7th harmonics are selected for boosting according to output frequency planning. With this operation, an input signal from PLL with the frequency 1-1.43GHz can result in an output frequency from 5-10GHz. And some other frequency boosting techniques are employed to generate a 5-40GHz sinusoidal signal eventually.

For the 5th and 7th harmonic boosting mode, the corresponding the time shift sequence $[0, \frac{1}{5}T_{clk}, \frac{2}{5}T_{clk}, \frac{3}{5}T_{clk}, \frac{4}{5}T_{clk}]$ and $[0, \frac{1}{7}T_{clk}, \frac{2}{7}T_{clk}, \frac{3}{7}T_{clk}, \frac{4}{7}T_{clk}, \frac{5}{7}T_{clk}, \frac{6}{7}T_{clk}]$ can be expressed in phase shift sequence $[0, \pm 72°, \pm 144°]$ and $[0, \pm 51.4°, \pm 102.8°, \pm 154.3°]$ respectively. Considering the two harmonic boosting mechanisms should be fulfilled in the same circuitry, a modified operation is to use 6 summing signals with the phase shifts that can be obtained from a same DLL configuration. Finally, based on a DLL which can provides the interval phase shifts of $10°$, $[0, \pm 70°, \pm 140°]$ and $[0, \pm 50°, \pm 100°]$ are chosen for 5th and 7th harmonic boosting respectively, and the phasor diagram is visualized in Fig. 2.27.

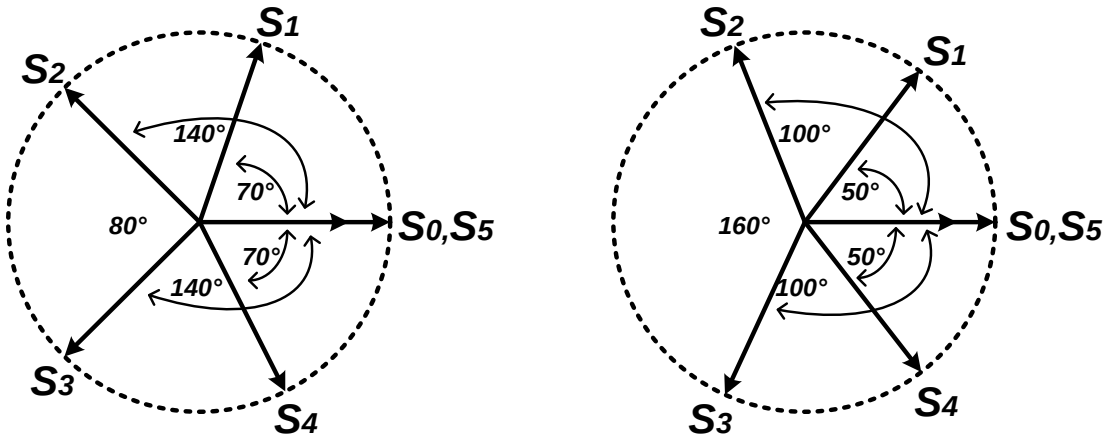


Fig. 2.27. Phase diagram for (a) 5th harmonic boosting (b) 7th harmonic boosting for practical implementation in [16]

2.6.3 Proposed time-and-voltage-mode-based sinusoidal oscillator

This thesis brings up a new DHC technique which includes both time-mode-based and voltage-mode-based techniques to achieve a low THD sinusoidal output. Thus, not only the time shift sequence of square-wave signals can be designed, but also the corresponding summing coefficients can be devised. In this way, compared to previously introduced time-mode-based oscillator, the frequency of the input reference clock is greatly reduced without the degradation of spectrum purity of output sinusoidal waveform.

The block diagram of the design is illustrated in Fig. 2.28. The input a square-wave clock with cycle period of T_{clk}. Four pairs of complementary square-wave signals with cycle period of $T_{cycle} = N \cdot T_{clk}$ are generated, and the corresponding time shift sequence is denoted as $[\pm m_0, \pm m_1, \pm m_2, \pm m_3]$. And then, these square-wave signals are summed

up with different summing coefficient sequence $[\alpha_0, \alpha_1, \alpha_2, \alpha_3]$. And thus, a staircase–like signal is obtained. Fig. 2.29(a) and Fig. 2.29(b) demonstrate the spectrum of input and output signals of DHC module. It is seen that through the processing of the DHC module, the odd harmonics from 3rd to 13th are almost fully cancelled out. Though 15th and 17th harmonics are left uncompensated, they can be easily suppressed with a 3rd order passive RC filter.

Through the mathematical calculation of the DHC theory, $N = 16$, $[\pm m_0, \pm m_1, \pm m_2, \pm m_3] = [\pm 0, \pm 1, \pm 2, \pm 3]$ and $[\alpha_0, \alpha_1, \alpha_2, \alpha_3] = [17,32,24,13]$ are selected for the design. The time shift sequence can be also represented as phase shift sequence as $[\pm 0°, \pm 22.5°, \pm 45°, \pm 67.5°]$.

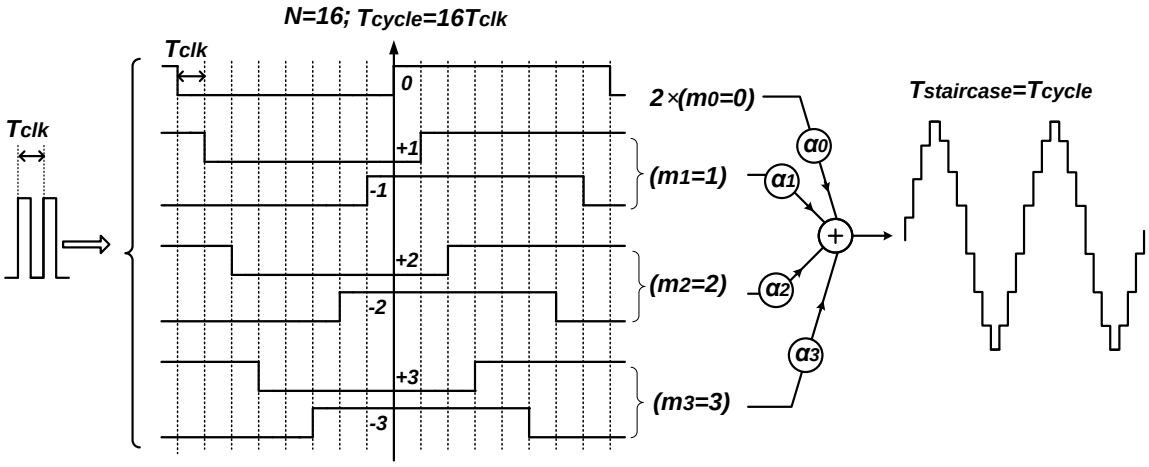


Fig. 2.28. DHC theory in time-voltage-mode-based sinusoidal oscillator

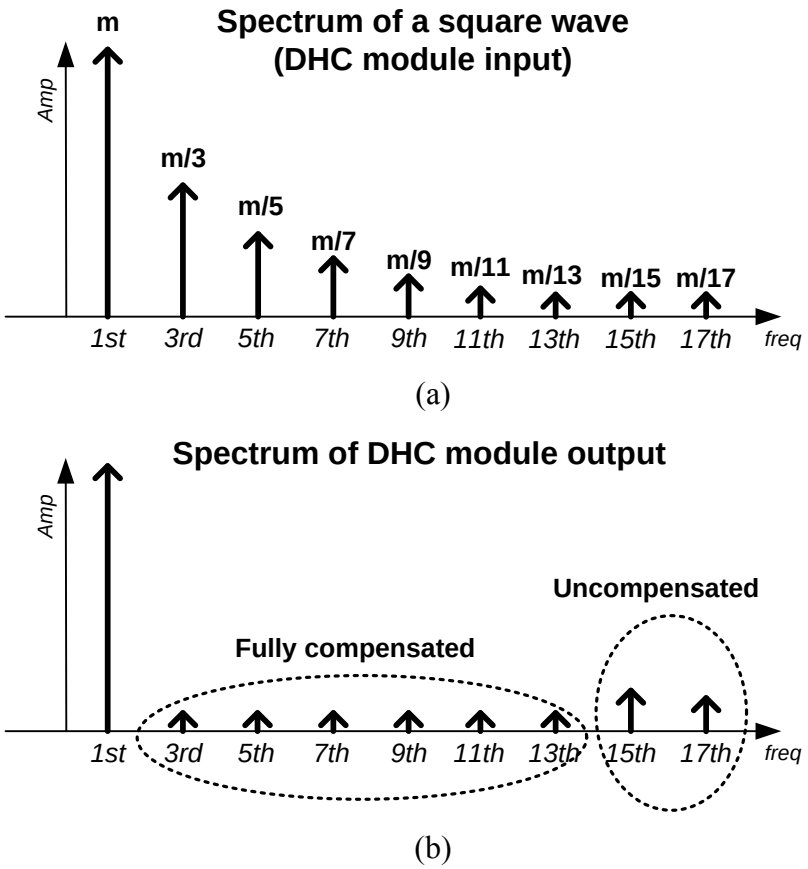


Fig. 2.29. Spectrum of DHC module (a) input (b) output

2.7 Comparison of sinusoidal oscillator based on DHC technique

As is already mentioned, feedback-based sinusoidal oscillators have great linearity limitation due to complexity of circuit implementation. Though it seems that it can avoid employing a high frequency clock reference at the input, an 80MHz clock is required to control the switched-capacitor (SC) BPF. Furthermore, two highly linear Opamps are used in the SC BPF, which will result in large power consumption compared to pure digital implementation of the open-loop-based oscillator.

As for open-loop-based sinusoidal oscillator, the design complexity is largely reduced because the whole oscillator only consists of digital circuitry and passive

components. The work [4] only consumes 4.04mW and can achieve -72dB THD performance for the differential mode implementation in CMOS 0.13um technology, which shows overwhelming advantages over its counterparts in literature. However, one limitation for this design is that a 1.16GHz is required to generate a 10MHz sinusoidal output, which is very inefficient. The design proposed in this thesis only employs 160MHz to generate 10MHz sinusoidal outputs. In addition, quadrature outputs are be generated is, and other performances, such as linearity, power consumption and design complexity are still competitive.

3. MATHEMATICAL ALGORITHM OF DHC TECHNIQUE

Some conventional integrated circuits are capable of producing square-wave signal with 50% duty cycle and tunable frequency range, which is shown in Fig. 3.1. The input V_{in} is from a crystal oscillator with fixed frequency usually at kHz and MHz range. Frequency synthesizer generates periodic signal V_1 with the desired programmable frequency. Digital buffer can increase the pulling up and down effort of the periodic signal to make it to be a square-wave V_2. A digital ÷2 dividing operation is employed to generate a new square-wave V_3 with duty cycle of 50% at the cost of reduced frequency.

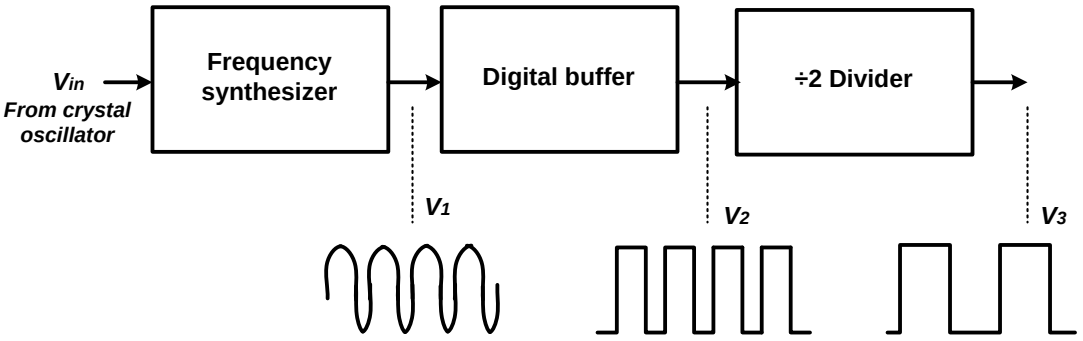


Fig. 3.1. Conventional circuits to generate square-wave with 50% duty cycle

Periodic square-wave signals are usually employed as the clock reference for an electronic system. In most cases, V_2 without 50% duty cycle is sufficient, because only rising or falling edge of the square-wave signal is employed to track the operation of sub-circuits in the system. However, to design a sinusoidal oscillator which can generate a sinusoidal output, 50% duty cycle square-wave is used as the input signal.

3.1 Introduction of DHC technique

A square-wave signal with 50% duty cycle can be expressed with Fourier expansion form in (1), and the spectrum response is shown in Fig. 3.2.

$$x(t) = \frac{4}{\pi} \sum_{k=1,3,5\ldots}^{\infty} \left[\frac{1}{k} sin(k\omega_0 t) \right] \quad (1)$$

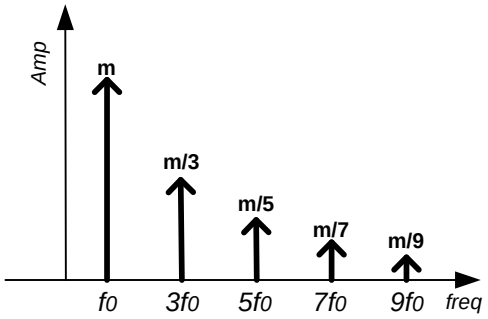


Fig. 3.2. Spectrum of a square wave with 50% duty cycle

It's observed that aside from fundamental tone locating at f_0, there are other odd harmonics with the amplitude which is reversely proportional to the order times. Thus, sinusoidal oscillator based on harmonic cancellation technique is required to maintain the fundamental tone while suppressing the harmonics.

As is shown in Fig. 3.3, the sinusoidal oscillator with DHC technique presented in this thesis consists of two major sub-systems: a DHC module and a LPF. DHC module target at suppressing low order harmonics, while a simple passive LPF is used mainly remove high order harmonics. The two steps are explained in detail as below.

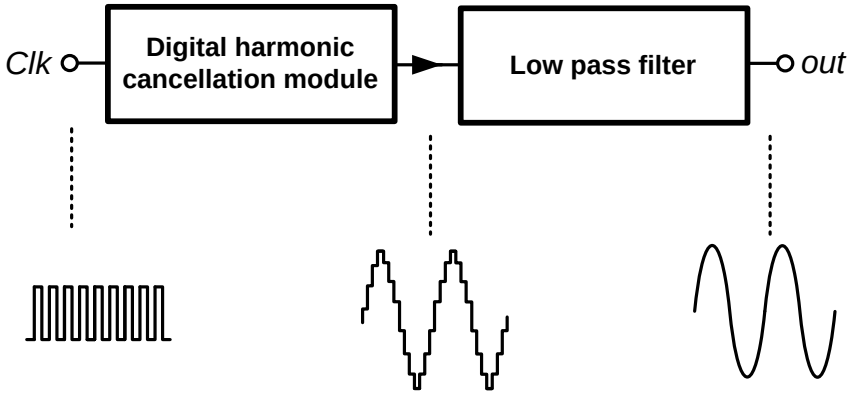


Fig. 3.3. Two steps of sinusoidal oscillator

In the first step, the output of DHC module is generated by adding several square-waves with different time shifts and different amplitude coefficients. Phase shifts and corresponding summing coefficients are two sets of design parameters. Changing these parameters will result in different harmonic cancellation effect in frequency spectrum. In this work, the output of DHC module and the spectrum response are shown in Fig. 3.4.

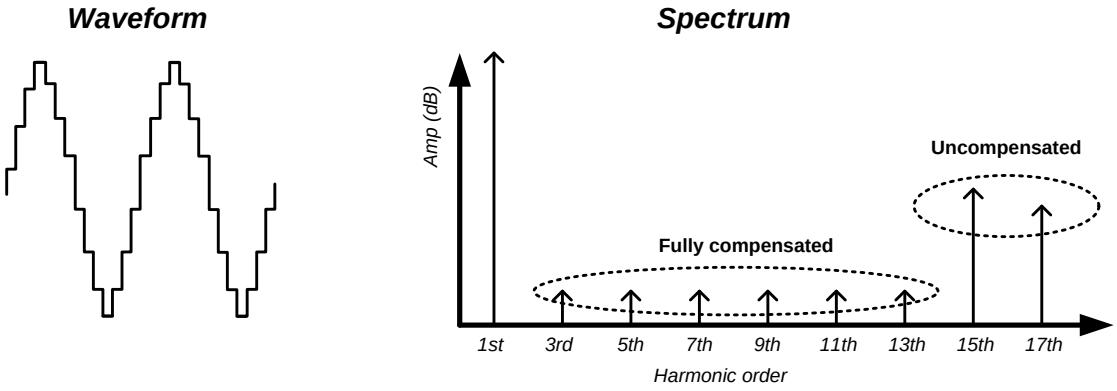


Fig. 3.4. Waveform and spectrum of DHC module output signal

As is observed, the staircase-like signal for DHC module output has sharp edges and corners, but it emulates the outline shape of sinusoidal wave. From the spectrum response, it is showed that the low order odd harmonics, such as 3^{rd}, 5^{th}, 7^{th}, 9^{th}, 11^{th} and 13^{th} harmonics are fully cancelled out, while 15^{th} and 17^{th} harmonics remain with comparatively larger amplitude. Actually, these uncompensated high order harmonics are the representation of edges and corners in the frequency domain.

In the second step, LPF module is used to remove the uncompensated high order harmonics. The output waveform of LPF and the spectrum response is shown in Fig. 3.5. As the 15^{th}, 17^{th} and other higher order harmonics are far away from fundamental tone in the frequency domain, so the requirement for LPF is greatly relaxed. As a result, a passive 3^{rd} order LPF is employed in this work.

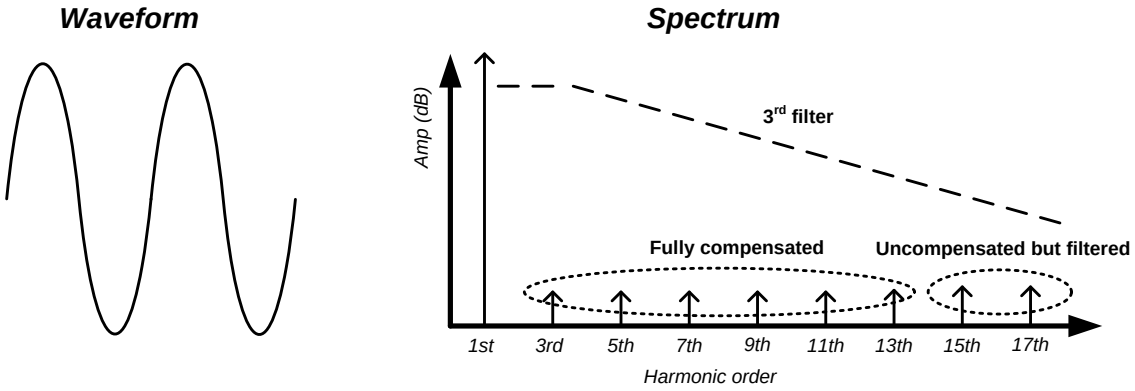


Fig. 3.5. Waveform and spectrum of 3^{rd} LPF output signal

3.2 Mathematical algorithm of DHC technique

As is mentioned above, the square-wave signal with 50% duty cycle consists of an infinite sequence of odd harmonics with amplitudes obtained as follows.

$$x(t) = \frac{4}{\pi} \sum_{k=1,3,5\ldots}^{\infty} \left[\frac{1}{k} sin(k\omega_0 t) \right]$$

Where k is the harmonic index, ω_0 is the fundamental frequency.

Suppose time shift of Δt is imposed to the original square wave, the functions can be expressed as shown below:

$$\begin{aligned} x(t+\Delta t) &= \frac{4}{\pi} \sum_{k=1,3,5\ldots}^{\infty} \frac{1}{k} sin\left[k\omega_0 (t+\Delta t)\right] \\ &= \sum_{k=1,3,5\ldots}^{\infty} \left[\frac{4}{\pi} \cdot \frac{1}{k} sin\left(k\omega_0 \Delta t\right) \right] cos\left(k\omega_0 t\right) \\ &+ \sum_{k=1,3,5\ldots}^{\infty} \left[\frac{4}{\pi} \cdot \frac{1}{k} cos\left(k\omega_0 \Delta t\right) \right] sin\left(k\omega_0 t\right) \end{aligned}$$

At the same time, suppose time shift of $-\Delta t$ is imposed to the original square wave, the functions can be expressed as shown below:

$$\begin{aligned} x(t-\Delta t) &= \frac{4}{\pi} \sum_{k=1,3,5\ldots}^{\infty} \frac{1}{k} sin\left[k\omega_0 (t-\Delta t)\right] \\ &= -\sum_{k=1,3,5\ldots}^{\infty} \left[\frac{4}{\pi} \cdot \frac{1}{k} sin\left(k\omega_0 \Delta t\right) \right] cos\left(k\omega_0 t\right) \\ &+ \sum_{k=1,3,5\ldots}^{\infty} \left[\frac{4}{\pi} \cdot \frac{1}{k} cos\left(k\omega_0 \Delta t\right) \right] sin\left(k\omega_0 t\right) \end{aligned}$$

By adding the pair of complementary time-shifted square-wave signals, the $\cos(k\omega_0 t)$ terms are cancelled, and only the $\sin(k\omega_0 t)$ terms are left.

$$x(t+\Delta t) + x(t-\Delta t) = 2 \sum_{k=1,3,5\ldots}^{\infty} \left[\frac{4}{\pi} \cdot \frac{1}{k} cos\left(k\omega_0 \Delta t\right) \right] sin\left(k\omega_0 t\right)$$

$$= 2 \sum_{k=1,3,5...}^{\infty} \left[\frac{4}{\pi} \cdot \frac{1}{k} cos(k\phi) \right] sin(k\omega_0 t)$$

Where, time shift Δt is changed to phase shift angle $\emptyset$ through the relationship $\emptyset = \omega_0 \Delta t$. Assume there are n pairs of complementary square-wave signal with different phase shifts $\emptyset_i$ $(i = 0,1 \ldots n-1)$, and they are summed up with different coefficients A_i $(i = 0,1 \ldots n-1)$, the overall Fourier expansion is obtained as :

$$x|_{overall} = \frac{8}{\pi} \cdot \sum_{k=1,3,5...}^{\infty} \left[\frac{1}{k} \sum_{i=0}^{n-1} A_i cos(k\phi_i) \right] sin(k\omega_0 t)$$

As a result, the total harmonic distortion (THD) can be reduced by:

- Maintain fundamental tone: $C_1 = \frac{8}{\pi} \cdot \sum_{i=0}^{n-1} A_i cos(\phi_i),\ (k = 1)$
- Minimize harmonics: $C_k = \frac{8}{\pi} \cdot \frac{1}{k} \sum_{i=0}^{n-1} A_i cos(k\phi_i),\ (k \neq 1)$

For practical circuit design consideration, $\emptyset_i$ $(i = 0,1 \ldots n-1)$ variables cannot be randomly chosen. With the help of digital circuits, such as Johnson counter, or analog circuits, such as PLL and DLL, phase-shifted square-wave signals can be generated in the waveform shown in Fig. 3.6. These phase shifts are equally distributed based on the phase step of $\frac{2\pi}{N}$, and total phase shift number of N.

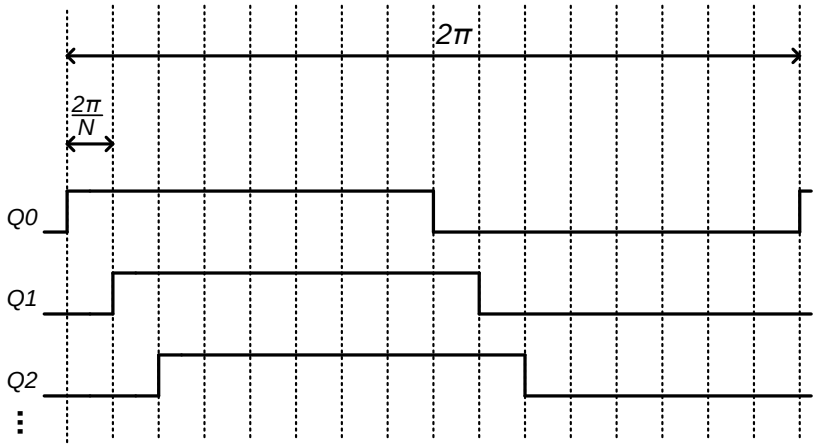


Fig. 3.6. Multi-phase square-wave signal waveforms

N different square-wave $Q_0, Q_1, Q_2 \dots Q_{N-1}$ are denoted to the phase shifts of $\emptyset_i = m_i \cdot \frac{2\pi}{N}$ $(i = 0,1 \dots n-1)$ respectively. Among them, n sets of complementary signals are chosen for the summation. Assume the complementary phase shift sequence is represented as $[\pm m_0, \pm m_1, \dots \pm m_{n-1}]$.

In the design of this thesis, as illustrated in Fig. 3.7, it is selected with $N = 16$, $n = 4$ and $[\pm m_0, \pm m_1, \pm m_2, \pm m_3] = [\pm 0, \pm 1, \pm 2, \pm 3]$. And the corresponding summing coefficients $[A_0, A_1, A_2, A_3]$ for phase-shifted square-wave signals $[\pm m_0, \pm m_1, \pm m_2, \pm m_3]$ are calculated by harmonic cancellation algorithm. The next sub-section will explain how to choose each design parameter for practical consideration.

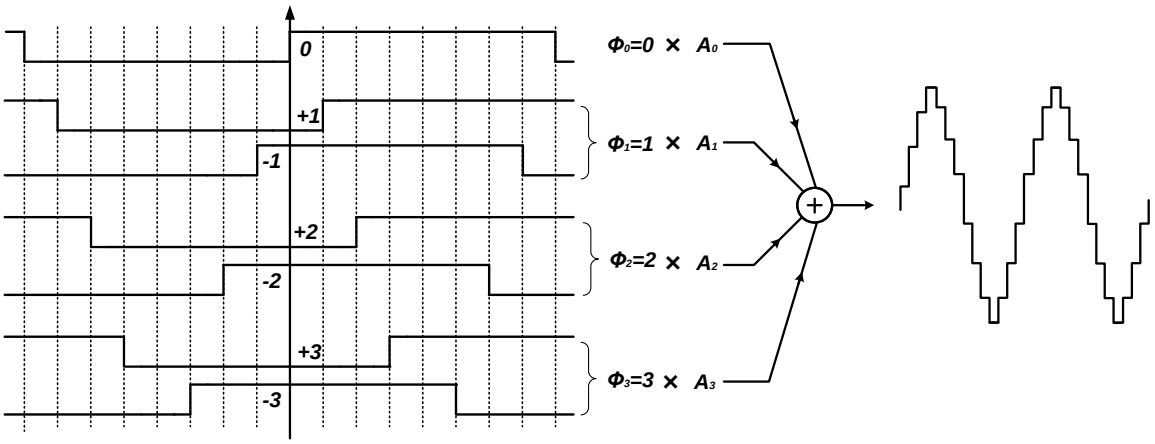


Fig. 3.7. Summing operation of different phase shifts

3.3 Selection of the design parameters

It is already discussed that the main design parameters for DHC technique in this work include:

- N: the total number of phase shifts
- n: number of phase-shifted complementary signal pairs for summing
- $[\pm m_0, \pm m_1 \dots \pm m_{n-1}]$: complementary phase shift sequence
- $[A_0, A_1 \dots A_{n-1}]$ and $[\alpha_0, \alpha_1 \dots \alpha_{n-1}]$: the ideal adding coefficient sequence and the practical one with a certain resolution

A review of the paper [4] will help enhance the understanding of the parameters trade-offs. Implemented in TSMC 0.18um technology, the design includes the parameters as: $\mathrm{N} = 116$, $\mathrm{n} = 4$, $[\pm \mathrm{m}_0, \pm \mathrm{m}_1, \pm \mathrm{m}_2, \pm \mathrm{m}_3] = [\pm 2, \pm 7, \pm 12, \pm 19]$ and $[\mathrm{A}_0, \mathrm{A}_1, \mathrm{A}_2, \mathrm{A}_3] = [1,1,1,1]$. The highlight is the summing coefficients for each time-shifted square-wave path are identical. According to the explanation in the thesis, summing coefficient matching problem is largely relieved in this way. However, this is not a critical issue in

integrated circuit design. Some layout techniques, such as common centroid, interdigitization and randomization of the unit circuit components, can greatly reduce mismatches. On the other hand, the large division ratio N is costly for his work, which requires 1.16GHz signal to generate 10MHz output. And the processing of high frequency input, up to 1.16GHz in his work is impossible to fulfill for long channel technology like OnSemi 0.5um. In view of the speed limitations, by making the summing coefficients to be designable, the total time shift number N is much relaxed and sinusoidal signal can be achieved with competitive THD specification in OnSemi 0.5um technology. A discussion of how to choose all the design parameters based on the work of this thesis is presented in the next.

3.3.1 How to select total phase shifts (N)

In this work, $N = 16$ is selected with several considerations as follows:

First of all, it is observed that with a larger N, more phase-shifted square-wave signals are available for harmonic cancellation operation, and thus more unwanted harmonics can be cancelled out. For example, if $N = 12$, 3^{rd}-9^{th} odd harmonics can be ideally fully cancelled; if $N = 14$, 3^{rd}-11^{th} odd harmonics can be ideally fully cancelled; while if $N = 16$, 3^{rd}-13^{th} odd harmonics can be ideally fully cancelled.

On the other hand, the larger N implies the increased design complexity, and degradation in harmonic cancellation is involved due to the mismatch issue. This is especially significant for the situation where N phase-shifted square-wave signals are produced by a multi-stage ring oscillator or delay locked loop. On the contrary, if the digital Johnson counter is employed to generate the N phase-shifted square-wave signals, an input clock of N times higher frequency of output signal is demanded. A large N will

suffer from the technology speed limitation. For example, OnSemi 0.5um technology which is used for the design of the thesis has a limit of processing speed for static logic as 200MHz, and an output sinusoidal signal of 10MHz is required. If $N = 16$, input clock signal is 160MHz, and the design is feasible. However, if N is larger than 20, the required input clock signal will exceed the technology speed limit and the whole design is unachievable.

Moreover, both in-phase and quadrature sinusoidal signals are required at the same time for this application, so N should be the multiples of 4, such as 8, 12, 16 or 20. Because quadrature signals require phase shift of 90° which corresponds to the phase shift number of $N/4$. Thus only with $N/4$ to be an integer can the quadrature sinusoidal outputs be realized. The details of quadrature output signals design are discussed at circuit implementation section.

3.3.2 How to select complementary phase shift pairs for summing

n is the number of total phase shifts to be chosen from N available phase shifts, and $[\pm m_0, \pm m_1 \ldots \pm m_{n-1}]$ is denoted as the phase shift sequence.

As is designed with $N = 16$, four complementary pairs of square waves ($n = 4$) with time shift sequence $[\pm 0, \pm 1, \pm 2, \pm 3]$ are used to summed up to produce the sinusoidal signal. Though there are 16 different phases for summing, 8 phases are the inversion form of the other 8 phases. For example, the 1st phase is $22.5°$ and the 9th phase is $202.5°$, and $\cos(22.5°) = -\cos(202.5°)$. For the summing of different phase shifts to cancel these harmonics, either 1st or 9th phase can be chosen according to the polarity of summing coefficient.

Considering differential and quadrature sinusoidal outputs are desired, all these 16 different phases are demanded.

3.3.3 How to calculate summing coefficients (magnitude) for the phase shift signals

Based on the total time shifts of $N = 16$, and $n = 4$ pairs of complementary phase-shifted signals are selected, the amplitude of fundamental tone which is designed to be maintained is:

$$C_1 = \frac{8}{\pi}\left(1 + A_1 cos\left(22.5^\circ\right) + A_2 cos\left(45^\circ\right) + A_3 cos\left(67.5^\circ\right)\right)$$

While the amplitude of odd harmonics which are designed to be suppressed is:

$$C_k = \frac{8}{\pi}\cdot\frac{1}{k}\left(1 + A_1 cos\left(k\cdot 22.5^\circ\right) + A_2 cos\left(k\cdot 45^\circ\right) + A_3 cos\left(k\cdot 67.5^\circ\right)\right)\ \left(k = 3,5,7...\right)$$

As A_0 is normalized to unity, there are three design variables A_1, A_2, A_3, which can lead to fully cancellation of 3rd, 5th and 7th harmonics as:

$$\begin{cases} C_3 = \frac{8}{\pi}\cdot\frac{1}{3}\left(1 + A_1 cos\left(3\cdot 22.5^\circ\right) + A_2 cos\left(3\cdot 45^\circ\right) + A_3 cos\left(3\cdot 67.5^\circ\right)\right) = 0 \\ C_5 = \frac{8}{\pi}\cdot\frac{1}{5}\left(1 + A_1 cos\left(5\cdot 22.5^\circ\right) + A_2 cos\left(5\cdot 45^\circ\right) + A_3 cos\left(5\cdot 67.5^\circ\right)\right) = 0 \\ C_7 = \frac{8}{\pi}\cdot\frac{1}{7}\left(1 + A_1 cos\left(7\cdot 22.5^\circ\right) + A_2 cos\left(7\cdot 45^\circ\right) + A_3 cos\left(7\cdot 67.5^\circ\right)\right) = 0 \end{cases}$$

It is solved that $[A_0, A_1, A_2, A_3] = [1, 1.8478, 1.4142, 0.7654]$. A further observation shows that not only 3rd, 5th and 7th harmonics as targeted are fully cancelled, 9th, 11th and 13th harmonics are also fully removed.

$$\begin{cases} C_9 = \frac{8}{\pi}\cdot\frac{1}{9}\left(1 + A_1 cos\left(9\cdot 22.5^\circ\right) + A_2 cos\left(9\cdot 45^\circ\right) + A_3 cos\left(9\cdot 67.5^\circ\right)\right) = 0 \\ C_{11} = \frac{8}{\pi}\cdot\frac{1}{11}\left(1 + A_1 cos\left(11\cdot 22.5^\circ\right) + A_2 cos\left(11\cdot 45^\circ\right) + A_3 cos\left(11\cdot 67.5^\circ\right)\right) = 0 \\ C_{13} = \frac{8}{\pi}\cdot\frac{1}{13}\left(1 + A_1 cos\left(13\cdot 22.5^\circ\right) + A_2 cos\left(13\cdot 45^\circ\right) + A_3 cos\left(13\cdot 67.5^\circ\right)\right) = 0 \end{cases}$$

Is this a coincidence? By comparison between the summing coefficient of C_3, C_5, C_7 and C_9, C_{11}, C_{13}, it obtained that:

$$cos\left(m\cdot 22.5^\circ\right) = \cos\left((16-m)\cdot 22.5^\circ\right)$$
$$cos\left(m\cdot 45^\circ\right) = \cos\left((16-m)\cdot 45^\circ\right)$$
$$cos\left(m\cdot 67.5^\circ\right) = \cos\left((16-m)\cdot 67.5^\circ\right)$$

When $m = 3,5,7$, it is found that $C_3 = C_{13}, C_5 = C_{11}, C_7 = C_9$ are always satisfied. Consequently, when C_3, C_5, C_7 are cancelled out, C_9, C_{11}, C_{13} are surely to be suppressed at the same time.

In conclusion, summing coefficient $[A_0, A_1, A_2, A_3] = [1, 1.8478, 1.4142, 0.7654]$ are selected to realize fully cancellation of 3rd to 13th harmonics.

3.3.4 How to select summing coefficient resolution

As is obtained that precise summing coefficient for time shift sequence $[\pm 0, \pm 1, \pm 2, \pm 3]$ is $[1, 1.8478, 1.4142, 0.7654]$ respectively. In such condition, the 3rd to 13th harmonics can be fully cancelled.

However, in CMOS circuit implementation, the precise summing coefficient is impossible to achieve. The summing of signals with different ratios is realized by putting an array of identical unit cells side by side, and injecting each signal into a certain number of unit cells and combining all signals together. The identical unit components can be either passive components, such as resistors and capacitors, or active components,

such as current steering cell. Based on this idea of signal addition, the resolution of summing coefficient is determined by how many unit cells can be used for addition. To implement adding coefficients of $[1, 1.8478, 1.4142, 0.7654]$ with H-bit resolution, the unit cell number array $[\alpha_0, \alpha_1, \alpha_2, \alpha_3]$ can be derived with the equation:

$$[\alpha_0, \alpha_1, \alpha_2, \alpha_3] = round\left\{\frac{[1,\ 1.8478,\ 1.4142,\ 0.7654]}{1.8478 \times 2^H}\right\}$$

As a result, the unit cell number array for different resolution is shown in Table I. With a higher resolution, a larger number of unit cells are required, and the equivalent summing coefficient is closer to the precise value.

Table I

UNIT COMPONENT NUMBER FOR EACH SUMMING PHASE

	α_0	α_1	α_2	α_3
Bit=3	4	8	6	3
Bit=4	9	16	12	7
Bit=5	17	32	24	13
Bit=6	35	64	49	27
Bit=7	69	128	98	52

Also, the corresponding spectrum response for the summing coefficient resolution is illustrated in Table II-VI and Fig. 3.8-3.12.

Table II

HARMONIC DISTORTION OF DHC TECHNIQUE (RESOLUTION=3BIT)

Spectrum order	1st	3rd	5th	7th	9th	11th	13th	*15th*	*17th*
Amp (dB)	26.6	-34	-17.4	-25.4	-27.5	-24.2	-46.7	*3.07*	*1.99*
Harmonic distortion		HD3	HD5	HD7	HD9	HD11	HD13	*HD15*	*HD17*
(dB)		-60.6	**-44**	-52	-54.1	-50.8	-73.3	*-23.5*	*-24.6*

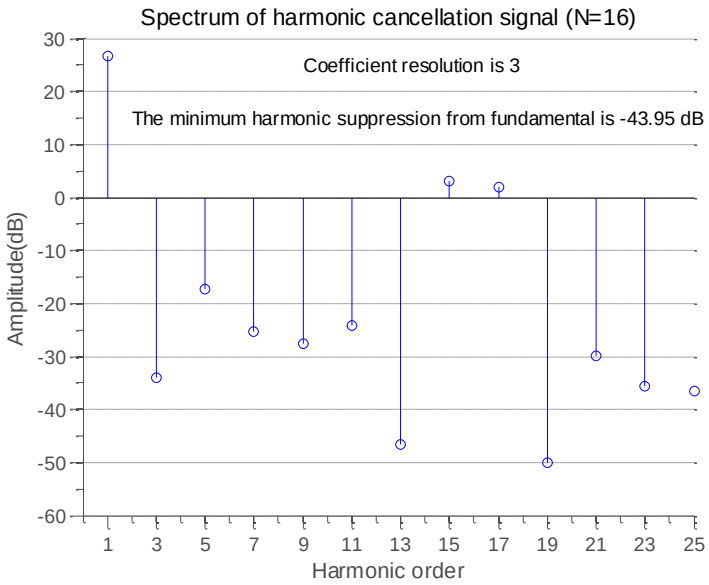


Fig. 3.8: Spectrum of digital harmonic cancellation signal: resolution=3bit

Table III

HARMONIC DISTORTION OF DHC TECHNIQUE (RESOLUTION=4BIT)

Spectrum order	1st	3rd	5th	7th	9th	11th	13th	*15th*	*17th*
Amp (dB)	33	-22.8	-13.2	-47	-49.2	-20.1	-35.5	*9.44*	*8.36*
Harmonic distortion		HD3	HD5	HD7	HD9	HD11	HD13	*HD15*	*HD17*
(dB)		-55.8	**-46.2**	-80	-82.2	-53.1	-68.5	*-23.6*	*-24.6*

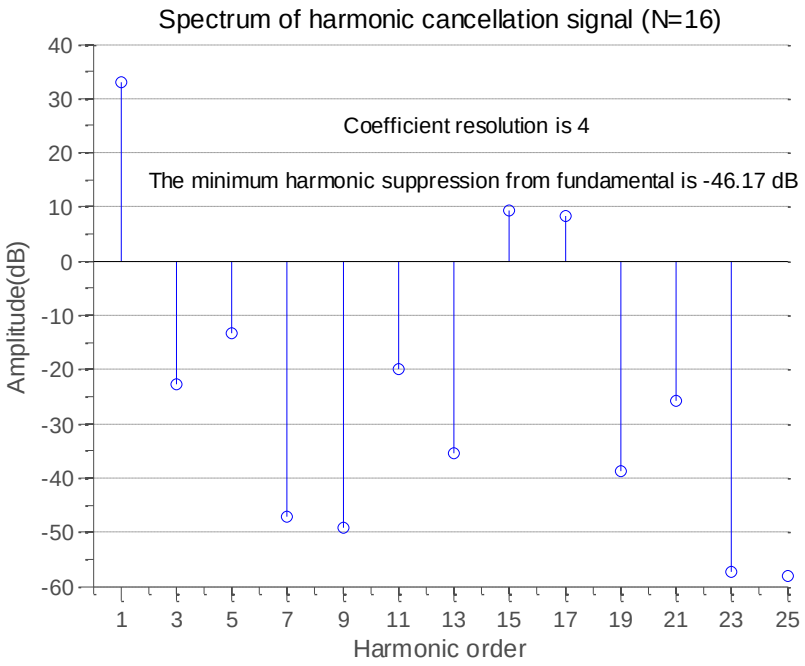


Fig. 3.9: Spectrum of digital harmonic cancellation signal: resolution=4bit

Table IV

HARMONIC DISTORTION OF DHC TECHNIQUE (RESOLUTION=5BIT)

Spectrum order	1st	3rd	5th	7th	9th	11th	13th	*15th*	*17th*
Amp (dB)	38.8	-19	-25.6	-19.7	-21.9	-32.5	-31.7	*15.3*	*14.2*
Harmonic distortion		HD3	HD5	HD7	HD9	HD11	HD13	*HD15*	*HD17*
(dB)		**-57.8**	-64.4	-58.5	-60.7	-71.3	-70.5	*-23.5*	*-24.6*

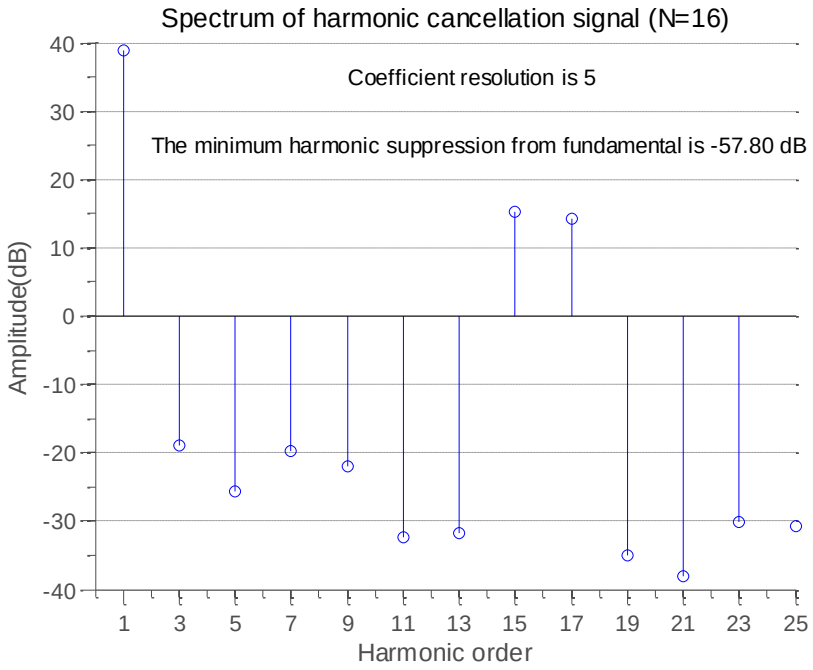


Fig. 3.10: Spectrum of digital harmonic cancellation signal: resolution=5bit

Table V

HARMONIC DISTORTION OF DHC TECHNIQUE (RESOLUTION=6BIT)

Spectrum order	1st	3rd	5th	7th	9th	11th	13th	*15th*	*17th*
Amp (dB)	45	-27.3	-13.8	-29.3	-31.5	-20.6	-40.1	*21.4*	*20.4*
Harmonic distortion		HD3	HD5	HD7	HD9	HD11	HD13	*HD15*	*HD17*
(dB)		-72.3	**-58.7**	-74.3	-76.5	-65.6	-85.1	*-23.6*	*-24.6*

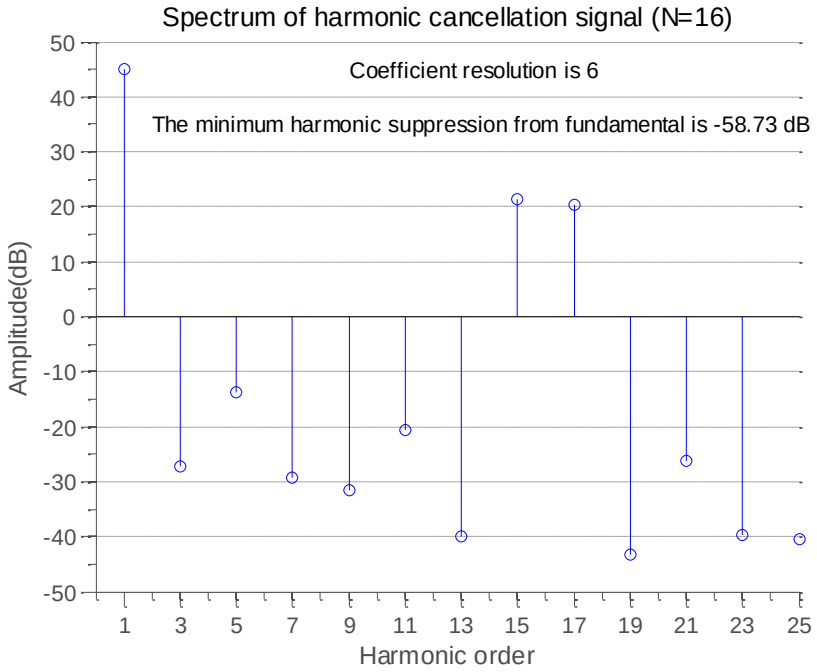


Fig. 3.11: Spectrum of digital harmonic cancellation signal: resolution=6bit

Table VI

HARMONIC DISTORTION OF DHC TECHNIQUE (RESOLUTION=7BIT)

Spectrum order	1st	3rd	5th	7th	9th	11th	13th	*15th*	*17th*
Amp (dB)	50.9	-18.5	-21.9	-27.1	-29.3	-28.8	-31.3	*27.4*	*26.3*
Harmonic distortion		HD3	HD5	HD7	HD9	HD11	HD13	*HD15*	*HD17*
(dB)		**-69.5**	-72.8	-78	-80.2	-79.7	-82.2	*-23.5*	*-24.6*

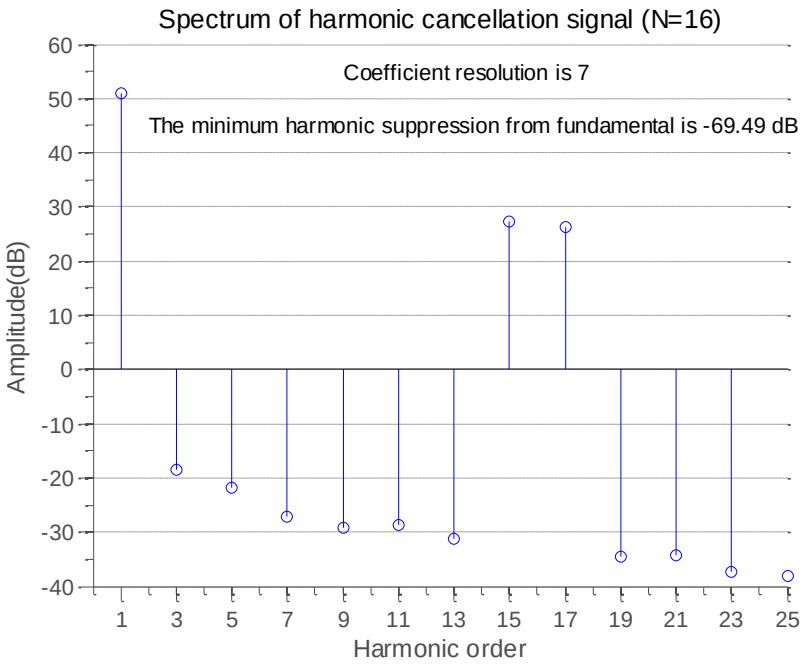


Fig. 3.12: Spectrum of digital harmonic cancellation signal: resolution=7bit

The total harmonic distortions of 3rd to 13th odd harmonics are listed in Table VII. Higher resolution results in better harmonic distortion effect, but at the cost of larger volume of unit cells to be employed. Moreover, even good THD performance can be achieved with high resolution, but it will be overshadowed by the mismatches, which is caused by PVT variation on silicon.

Table VII

HARMONIC DISTORTION FOR DIFFERENT RESOLUTION

Resolution	3-bit	4-bit	5-bit	6-bit	7-bit
THD	-43.9dB	-46.2dB	-57.8dB	-58.7dB	-69.5dB

Finally, 5-bit resolution is selected for the trade-off considerations.

3.4 Time shift mismatch and summing coefficient mismatch analysis

Either systematic error brought by the design or random error brought by process variation will always accompany with any CMOS circuit design. So it is inevitable to consider how these non-idealities affect the performance of the circuit. In this work, the harmonic distortion performance is analyzed based on two factors of mismatch:

- The time/phase shift mismatches
- The summing coefficient mismatches

It is assumed that these two types of mismatches are in the Gaussian distribution. Time shift mismatches are based on time shift sequence as $[\pm m_0, \pm m_1, \pm m_2, \pm m_3] = [\pm 0, \pm 1, \pm 2, \pm 3]$, while summing coefficient mismatches are also based on 5-bit resolution summing coefficient $[\alpha_0, \alpha_1, \alpha_2, \alpha_3] = [17, 32, 24, 13]$. As mismatch usually has most significant influence on 3rd harmonic tone, HD3 is chosen as the indicator for harmonic purity performance. Other order of harmonic distortions are analyzed but not discussed here.

In the spectrum of DHC module output signal, the absolute amplitude of the fundamental tone is large and therefore insensitive to mismatch, which can be expressed as:

$$\text{fundamental\_tone} = \frac{8}{\pi}\sum_{i=0}^{3}\left[\alpha_i Cos\left(m_i \cdot \frac{2\pi}{N}\right)\right]$$

3rd harmonic tone is cancelled out with DHC technique, so the absolute amplitude is weak and therefore very sensitive to mismatch. So the amplitude of 3rd harmonics without and with mismatch can be expressed as:

$$\text{3rd\_harmonic\_w/o\_mismatch} = \frac{8}{\pi}\sum_{i=0}^{3}\frac{1}{3}\left[\alpha_i Cos\left(3m_i \cdot \frac{2\pi}{N}\right)\right]$$

$$\text{3rd\_harmonic\_w\_mismatch} = \frac{8}{\pi}\sum_{i=0}^{3}\frac{1}{3}\left[\alpha_i\left(1+\Delta\alpha_i\right)Cos\left(3m_i\cdot\frac{2\pi}{N}+\Delta m_i\cdot 2\pi\right)\right]$$

HD3 with mismatch can be expressed as:

$$\text{HD3\_w\_mismatch} = \frac{\text{3rd\_harmonic\_w\_mismatch}}{\text{fundamental\_tone}}$$

Where $\Delta\alpha_i$ and Δm_i are summing coefficient mismatch and time shift mismatch respectively. Both of the two mismatches are assumed in Matlab with the mean of zero and a certain variance in Gaussian distribution. With 5-bit summing coefficient resolution, the HD3 is -57.8dB ideally. However, if mismatch is added, HD3 specification will be degraded.

Time shift mismatch is chosen with variance of 0.5%, 1% and 2% with regard to a cycle period, and summing coefficient mismatch is chosen with variance of 1%, 2% and 4% with regard to its actual value. A large amount (2000) of independent simulations is executed and HD3 performance is illustrated in histogram from Fig. 3.13 to Fig. 3.21.

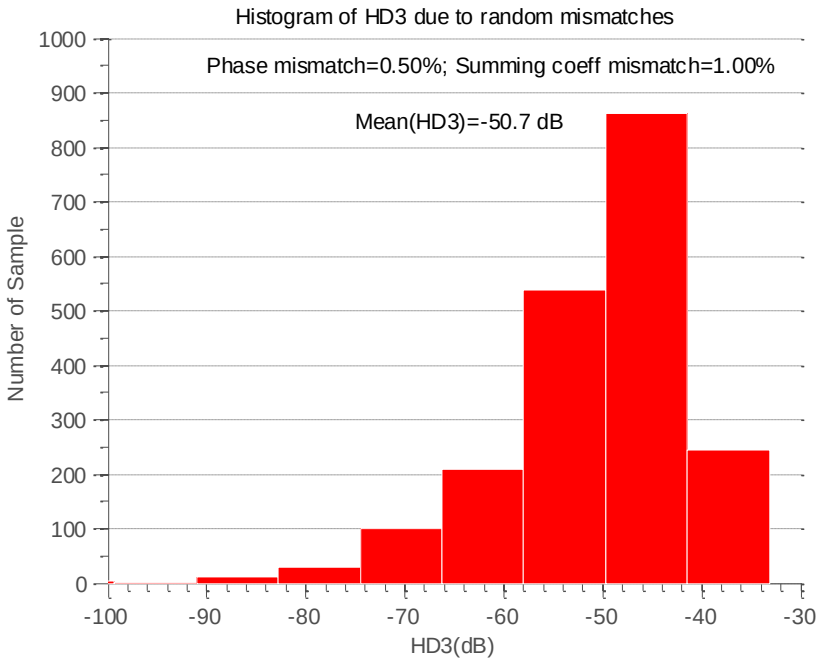


Fig. 3.13. HD3: Time shift mismatch=0.5%; summing coefficient mismatch=1%

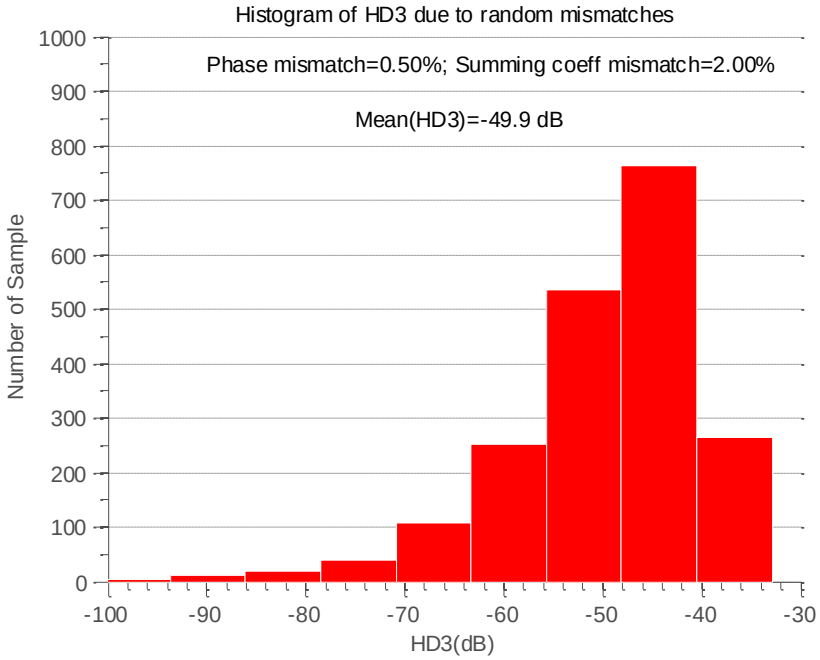


Fig. 3.14. HD3: Time shift mismatch=0.5%; summing coefficient mismatch=2%

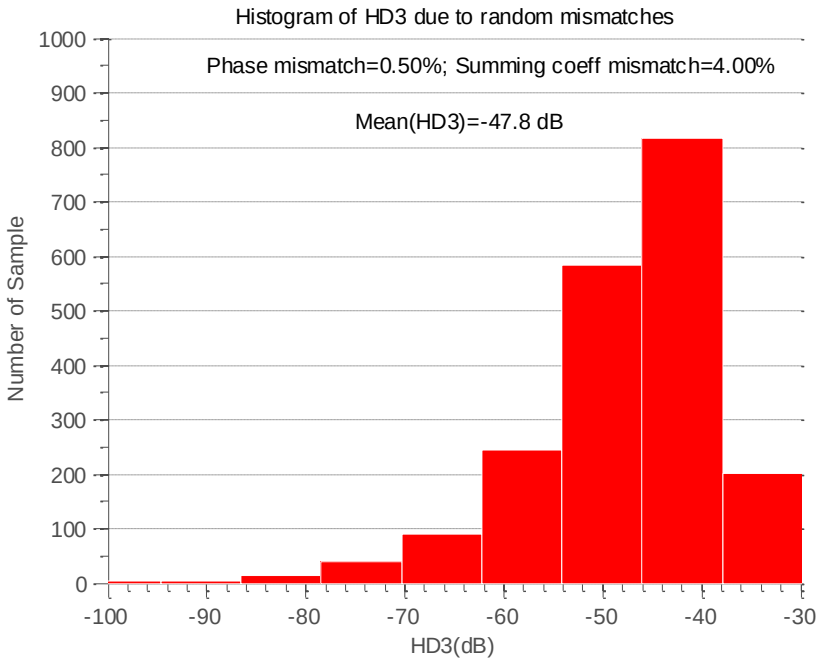


Fig. 3.15. HD3: Time shift mismatch=0.5%; summing coefficient mismatch=4%

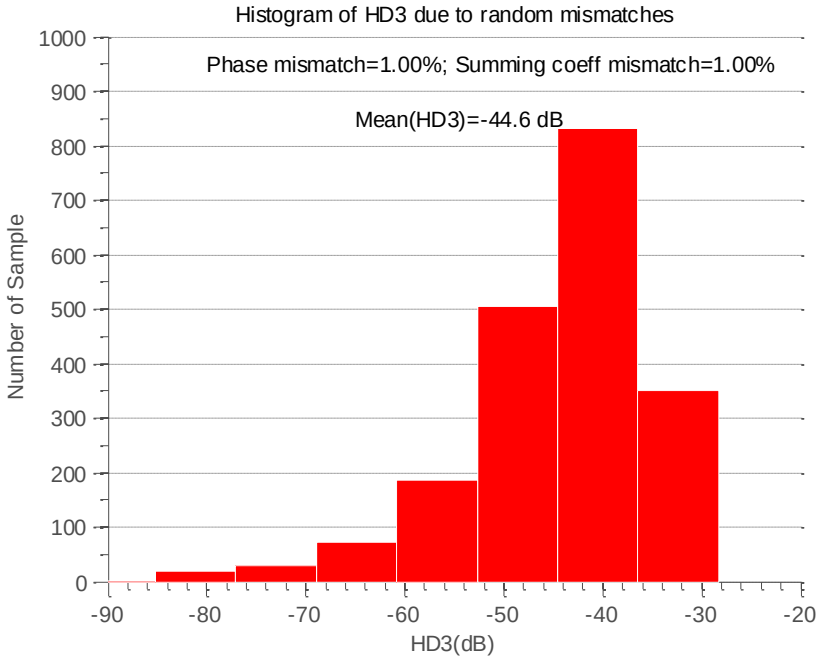


Fig. 3.16. HD3: Time shift mismatch=1%; summing coefficient mismatch=1%

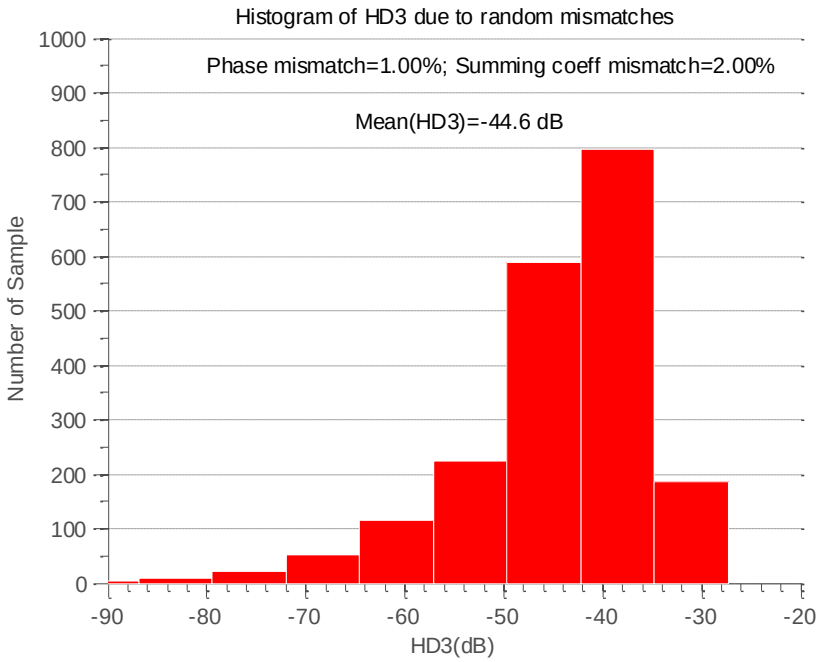


Fig. 3.17. HD3: Time shift mismatch=1%; summing coefficient mismatch=2%

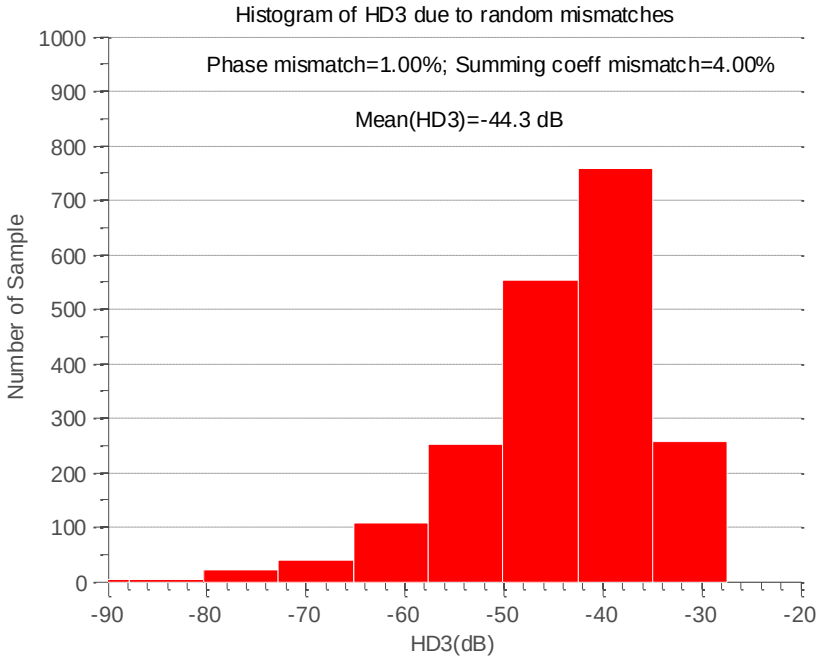


Fig. 3.18. HD3: Time shift mismatch=1%; summing coefficient mismatch=4%

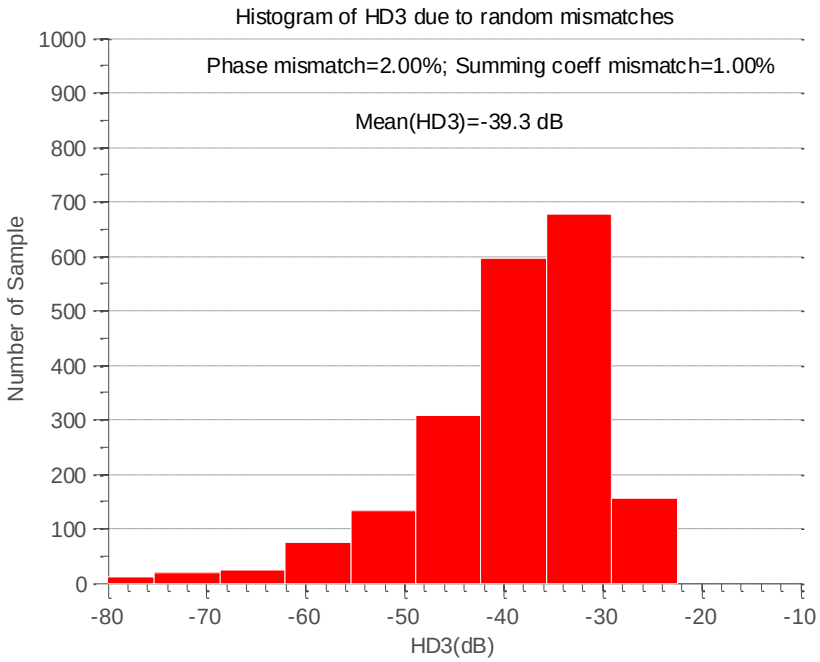


Fig. 3.19. HD3: Time shift mismatch=2%; summing coefficient mismatch=1%

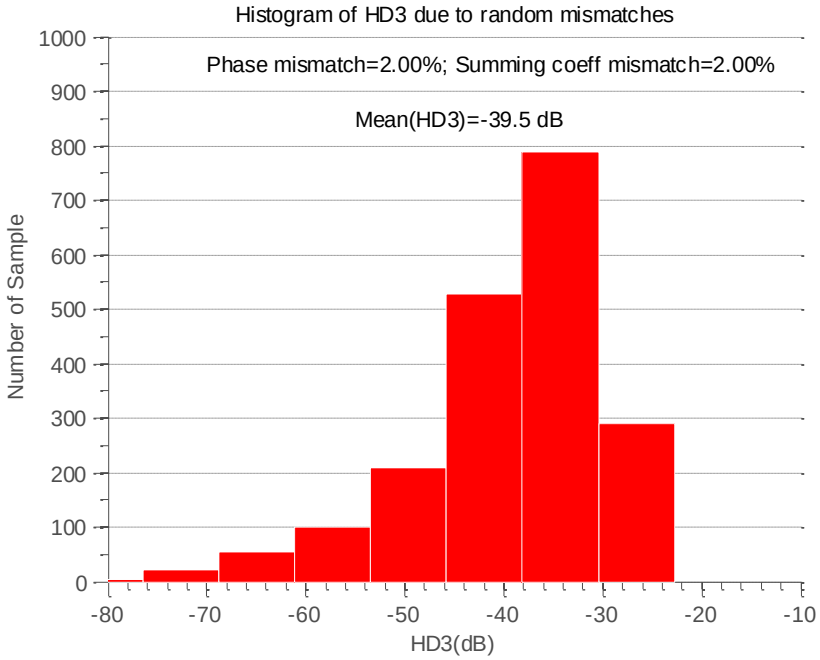


Fig. 3.20. HD3: Time shift mismatch=2%; summing coefficient mismatch=2%

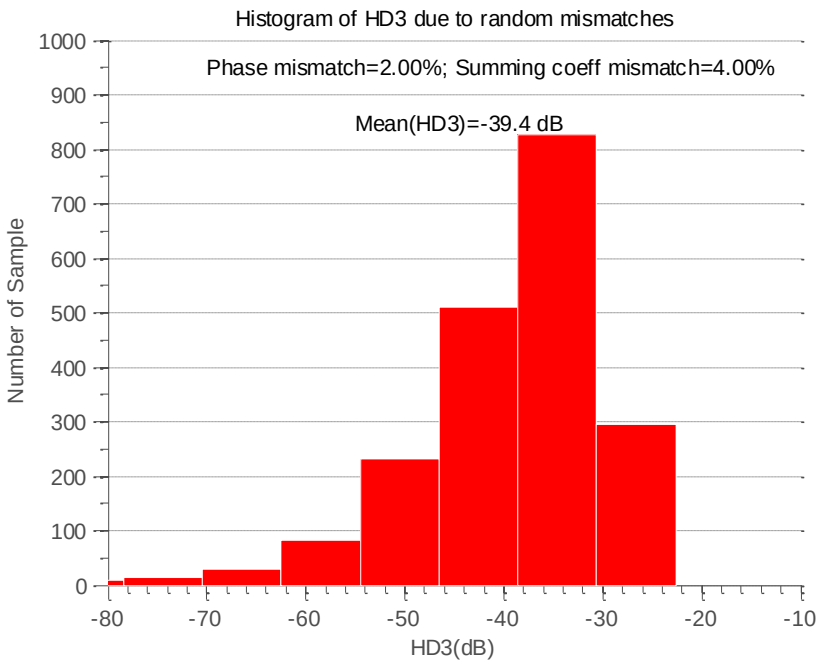


Fig. 3.21. HD3: Time shift mismatch=2%; summing coefficient mismatch=4%

Table VIII

HD3 PERFORMANCE BASED ON DIFFERENT MISMATCHES

HD3(mean value)	**Time shift 0.5%**	**Time shift 1%**	**Time shift 2%**
Summing coeff 1%	-50.7dB	-44.6dB	-39.3dB
Summing coeff 2%	-49.9dB	-44.6dB	-39.5dB
Summing coeff 4%	-47.8dB	-44.7dB	-39.4dB

From Table VIII, it is observed that time shift mismatch will have much more influence than summing coefficient mismatch on HD3 performance. If the output frequency of the whole system is 10MHz, the period is 100ns, 0.5% phase mismatch is 0.5ns, which is possible to be realized with digital circuit. In addition, utilizing interdigitized layout techniques for the summing cells (summing string resistors for the

proposed work), 4% summing coefficient mismatch is also an attainable value. Consequently, -50dB is a reasonable specification for HD3 with the DHC technique.

4. PROPOSED SINUSOIDAL OSCILLATOR SYSTEM

4.1 Overall diagram of sinusoidal oscillator system

The block diagram for proposed sinusoidal oscillator system and corresponding waveform illustration are shown in Fig. 4.1.

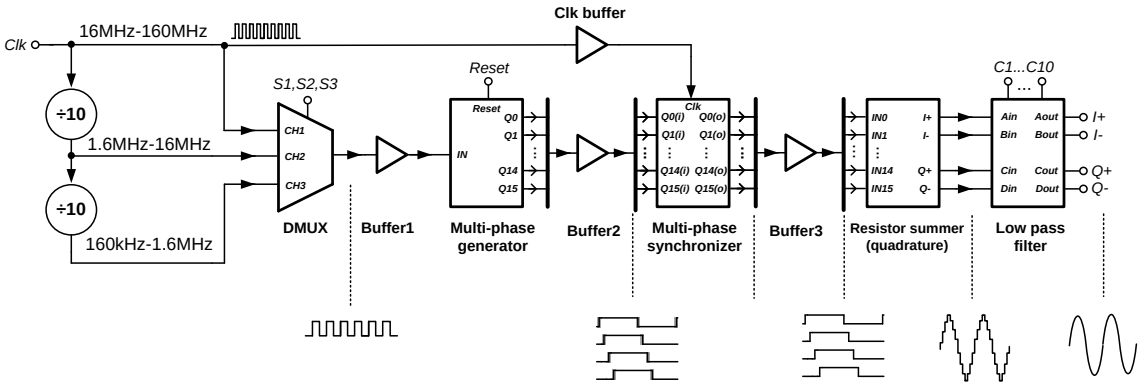


Fig. 4.1. Function diagram of proposed sinusoidal oscillator system

A frequency synthesizer is used to generate the master clock running at a one decade frequency, from 16MHz to 160MHz. The master clock is fed into two ÷10 dividers in serial connection to span the frequency range of the oscillator. The frequency synthesizer combined with the frequency dividers provides three signal paths, which is 16MHz-160MHz, 1.6MHz-16MHz, 160kHz-1.6MHz. A digital multiplier (DMUX) is employed to select one of the three signal paths. Next, a digital multi-phase generator is used to generate 16 square-wave signals with different phase shifts at a 16 times lower frequency, which is 1MHz-10MHz, or 100kHz-1MHz, or 10kHz-100kHz. In order to

eliminate the non-uniform time delay, a multi-phase synchronizer is used to align all the signals to the falling edge of reference clock. Resistor string summer adds up the multi-phase square-wave signals by with different coefficient to cancel out some of the unwanted low order harmonics. Finally, LPF is used to suppress the uncompensated high order harmonics. Besides, several digitals buffers are inserted between the adjacent building blocks to increase the drivability and overcome the parasitic problem.

The design considerations for each module are expanded in the discussion as below.

4.2 Frequency divider

Frequency divider module consists of two frequency dividers with dividing ratio of ten, and each ÷10 divider stage is made of ÷5 divider and ÷2 divider connected in series, as shown in Fig. 4.2. The basic elements for the dividers are D flip-flops. Based on the choices of the D flip-flops, the dividers are involved with different design complexity and behavior performance. Typically, static logic and dynamic logic are two design methodologies.

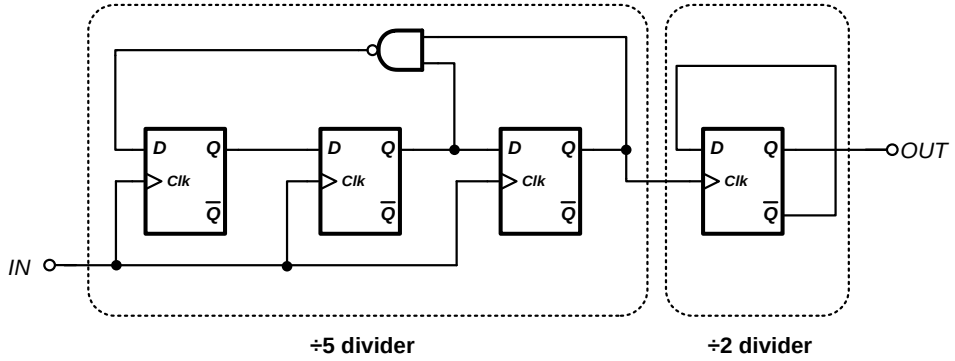


Fig. 4.2. ÷10 divider implemented with DFF.

Static logic D flip-flops are widely employed in digital CMOS integrated circuits. The principle of static logic can be phrased as there is always low-impedance path between the output and either the supply voltage or the ground. So it can operate at very low frequency. Fig. 4.3 shows a positive edge triggered D flip-flop made of NAND gates. Moreover, D flip-flops can also be implemented with NOR gates. Considering NOR gates have several PMOS transistors in series, which make it slower due to poor mobility of PMOS, NAND gates are usually preferred over NOR gates for the implementation of digital circuits.

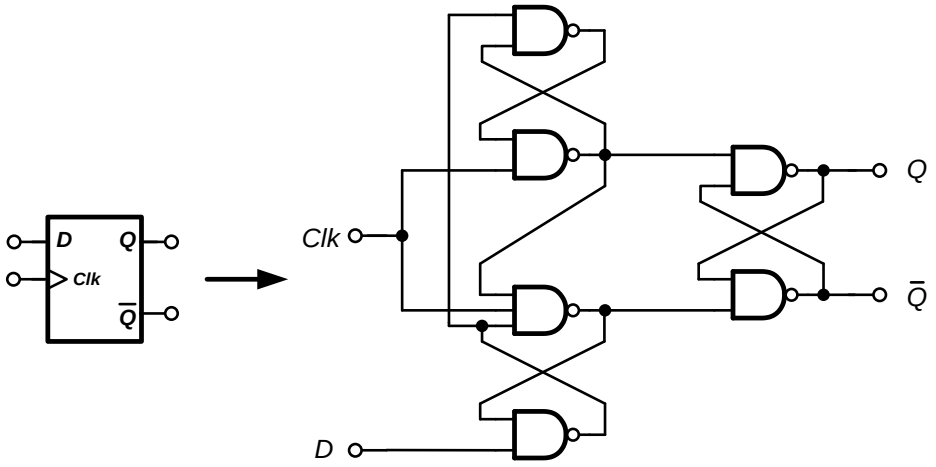


Fig. 4.3. D flip-flop with NAND gates (static logic)

Dynamic logic is distinguished from static logic by exploiting temporary storage of information in stray and gate capacitance. Thus, dynamic logic circuits are usually faster than static counterparts, and need less silicon area, but involve in more complicated design and more power consumption. Another feature or disadvantage for dynamic logic circuits is that they cannot operate at very low frequency which is unable to sustain dynamic transition of signals in the circuits.

Dynamic logic methodology mainly includes true single phase clock (TSPC) and current mode logic (CML). The illustration of TSPC is depicted in Fig. 4.4. However, frequency dividers are followed by digital buffers and multiplier, which apply static logic and are the bottleneck for the speed consideration. So it is unfeasible to use dynamic logic divider in this work.

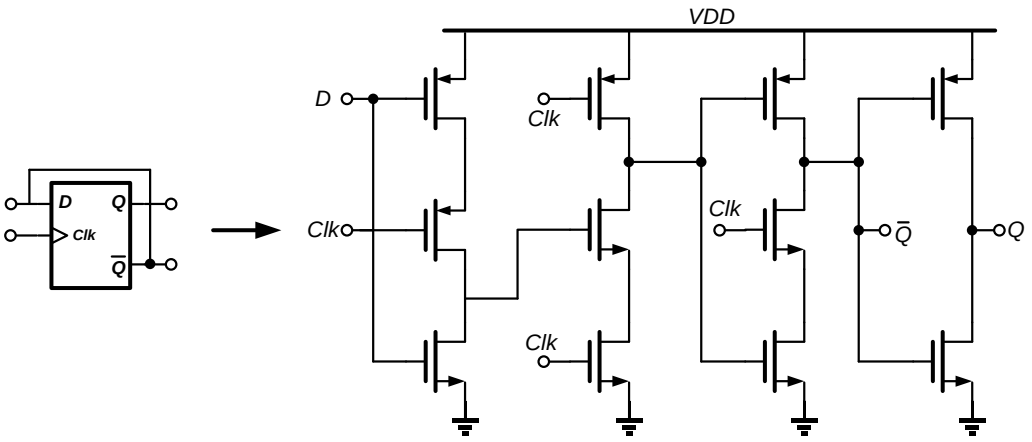
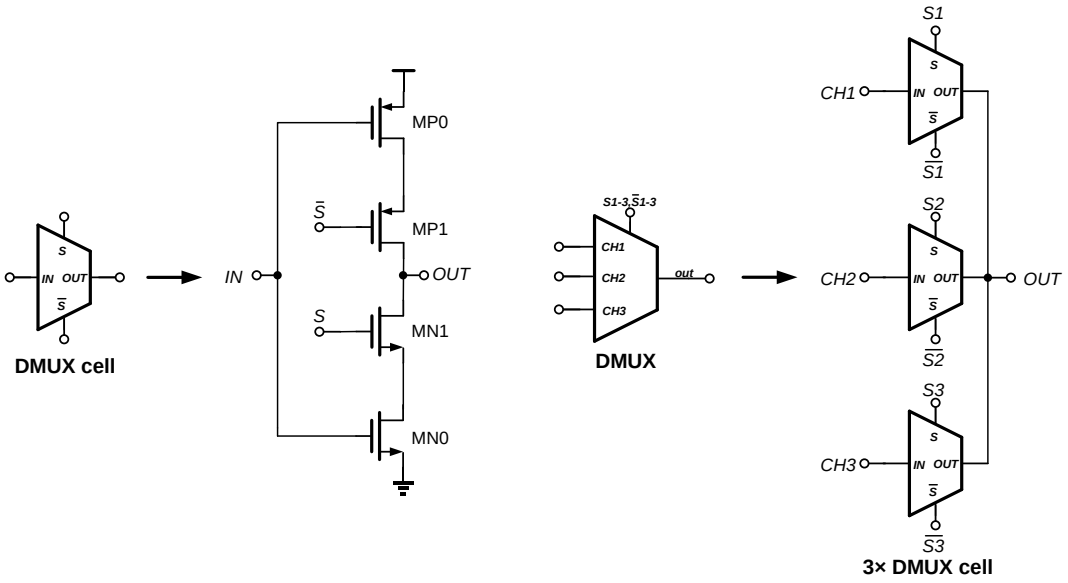


Fig. 4.4. TSPC ÷2 divider

4.3 Digital multiplexer (DMUX)

Three master clock paths, which cover three frequency decades, are available to feed into the next stages. Thus, digital Multiplexer (DMUX) is used to select one master clock path as required in the measurement. As is shown in Fig. 4.5, the DMUX module consists of three identical DMUX cells. For one DMUX cell, MN1 and MP1 operate as complementary switches to turn on and off the first signal path. To be specific, when S and $\overline{S}$ are connected to VDD and GND respectively, MN1 and MP1 are turned on, and this DMUX cell is able to conduct the corresponding master clock to output, and vice versa. Each time, only one DMUX cell is turned on, and the other two are turned off.



(a) (b)

Fig. 4.5. Digital MUX (a) DMUX cell (b) DMUX

4.4 Multi-phase generator

After a certain master clock is selected, digital multi-phase generator is used to generate 16 different phase-shifted square-wave signals at a 16 times lower frequency.

Some alternatives are available to generate square-wave signals of multiple phase shifts on silicon, such as multi-stage ring oscillator based frequency synthesizer and DLL. Frequency synthesizer can realize accurate frequency control, and multi-stage ring oscillator can generate output square-wave signals with required time shifts. [19]-[21] provides the design examples for the multi-stage ring oscillator. N-stage ring oscillator and each stage implementation are illustrated in Fig. 4.6.

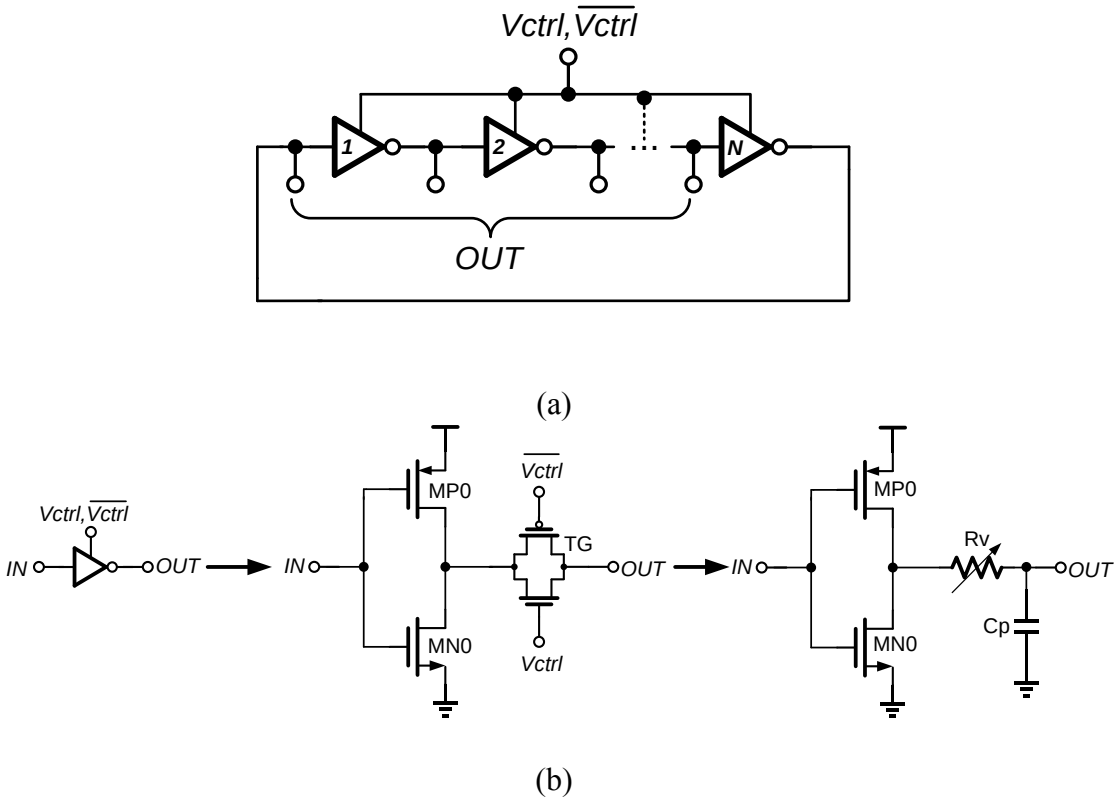


Fig. 4.6. (a) N stage ring oscillator (b) Each cell implementation

Here, Rv is a variable resistor implemented with a complementary transmission gate (TG). By changing the complementary control signal of TG ($Vctrl$ and $\overline{Vctrl}$), the correlated resistance Rv will be changed. Cp is the parasitic capacitance of next stage, and Gm is the transconductance of $MP0$ and $MN0$. As a result, the delay τ of each stage can be calculated as:

$$\tau = \frac{Cp \cdot (1 + Gm \cdot Rv)}{Gm}$$

And the corresponding oscillation frequency is:

$$f_{osc} = \frac{1}{2N\tau} = \frac{1}{2N} \cdot \frac{Gm}{Cp \cdot (1 + Gm \cdot Rv)}$$

Consequently, the N stage ring oscillator has frequency tuning mechanism by changing $Vctrl$ and $\overline{Vctrl}$.

Compared to the digital alternative approach which will be discussed later, multi-stage ring oscillator can reach much higher frequency. The reason is that there is no frequency dividing down from master clock to output. However, due to the process variation of each stage of ring oscillator, phase shift mismatch is comparatively large and intolerable, which degrades the sinusoidal signal purity greatly. Although self-calibration approach in [22], [23] is introduced to minimize the phase mismatch issue of multi-phase oscillator, the increased complexity of the design, area and power consumption is involved. In comparison, the digital multi-phase generator is sufficient to satisfy the speed requirement for the system, but can achieve better accuracy, less area and power consumption. DLL implementation is a similar approach as multi-stage ring oscillator based frequency synthesizer, it uses delay line instead of ring oscillator to generate multiple phases and thus also suffers from similar problems.

Digital multi-phase generator, which is employed in the design of the thesis, is shown in Fig. 4.7. The digital multi-phase generator consists of 16 identical positive-edge-triggered D flip-flips with $reset$. Suppose Clk input of the multi-phase is a square-wave of 160MHz, 10MHz identical square wave signals with 16 consecutive phases $m \times \frac{360^{\circ}}{16} (m = 0,1,2 \dots 15)$ are obtained from outputs $\mathrm{Q0}, \mathrm{Q1} \dots \mathrm{Q15}$.

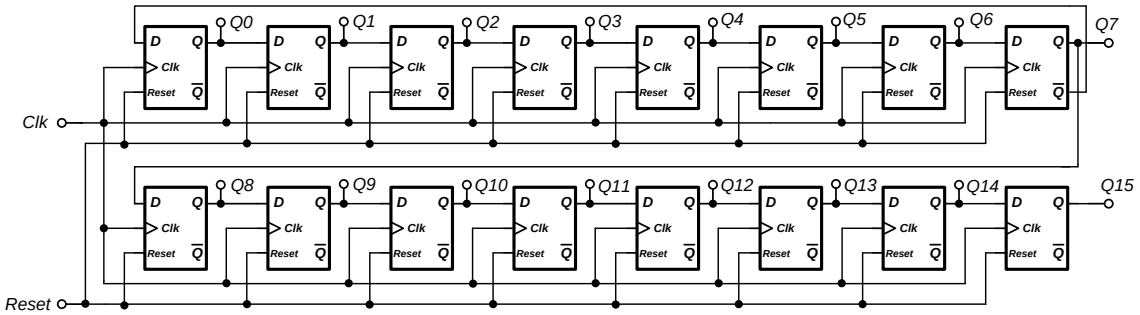


Fig. 4.7. Digital multi-phase generator

The 8 D flip-flops in the first row form a Johnson counter, which has the function of register shifting. Fig. 4.8 illustrates how the Johnson counter works in this work.

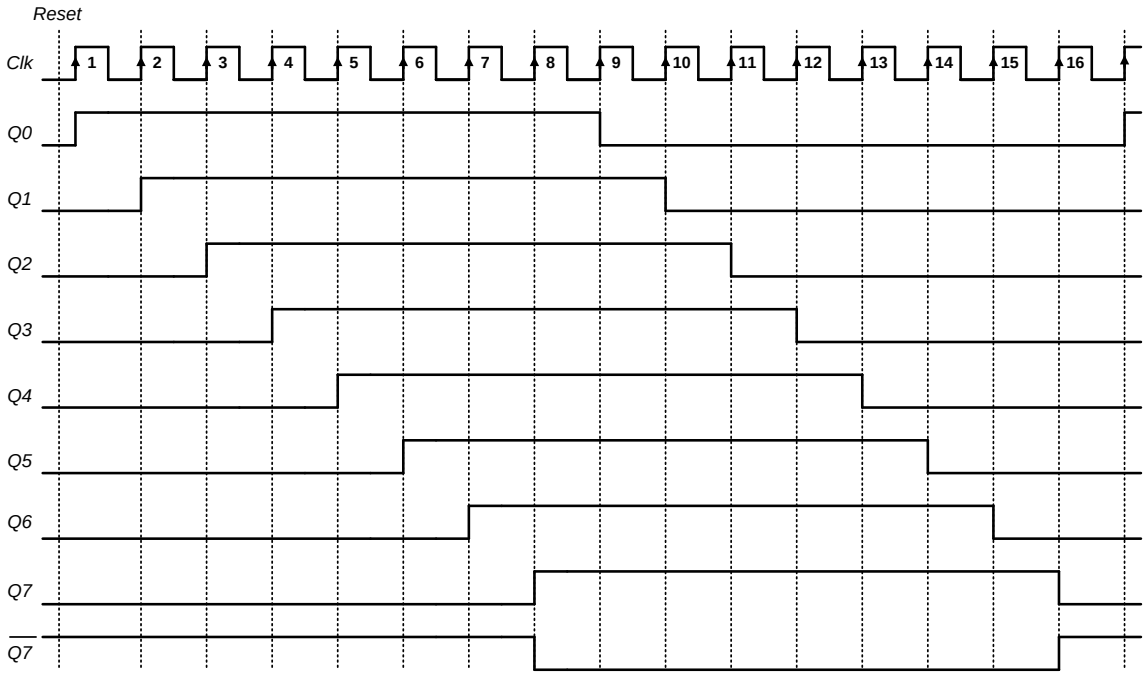


Fig. 4.8. Johnson counter operation waveform

At the beginning, all $Q0, Q1 \ldots Q7$ are reset to low voltage. For the first D flip-flop, $\overline{Q7}$ and Q0 are the data input and output respectively. The operation of Q0 follow $\overline{Q7}$ is

triggered on the rising edge of the first clock cycle and Q0 flips up. In the next, Q1 follows Q0 on the second rising edge of clock cycle and flips up, Q2 follows Q1 on the third rising edge of clock cycle and flips up, and so forth. On the 8th rising edge of clock cycle, the first D flip-flop detects low voltage of $\overline{Q7}$ as the data input, and makes Q0 flip down. As a result, the first 8 phase-shifted square-wave signals are generated.

The other 8 phase-shifted square-wave signals are actually the inversion pattern of $Q0, Q1 \dots Q7$. The $\overline{Q}$ outputs of first 8 D flip-flops are supposed to these patterns of signals. However, considering there is intrinsic time delay for Q and $\overline{Q}$ outputs of the same D flip-flop based on static logic implementation, the harmonic cancellation effect will be affected. To solve this issue, another 8 D flip-flops in the second row are connected in series with input from $Q7$, and outputs to be $Q8, Q9 \dots Q15$. Eventually, $Q0, Q1 \dots Q15$ are the 16 phase-shifted square-wave signals to feed to the next stage for summation.

4.5 Multi-phase synchronizer

In the digital multi-phase generator module, optimized design and layout techniques are employed to reduce the phase shift mismatch from different signal paths $Q0, Q1 \dots Q15$. Multi-phase synchronizer, though unnecessary, but strongly recommended to implement, can improve the phase matching on top of other techniques. And it can be also regarded as digital calibration for these signals.

Fig. 4.9 shows the multi-phase synchronizer circuit implementation. Clk is the master clock of the system, and $\overline{Clk}$ is the inverted pattern of the clock. Both Clk and $\overline{Clk}$ are buffered and used as the control signal for the transmission gates on the path of each phase-shifted signal.

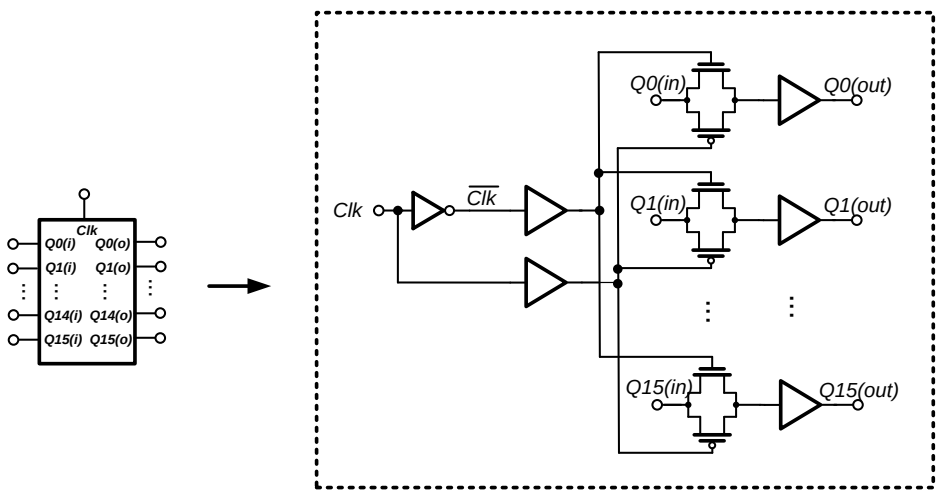


Fig. 4.9. Multi-phase synchronizer circuit

The waveform of multi-phase synchronizer inputs and outputs are visualized in Fig. 4.10, where only signals in $Q0$ and $Q1$ paths are illustrated as example.

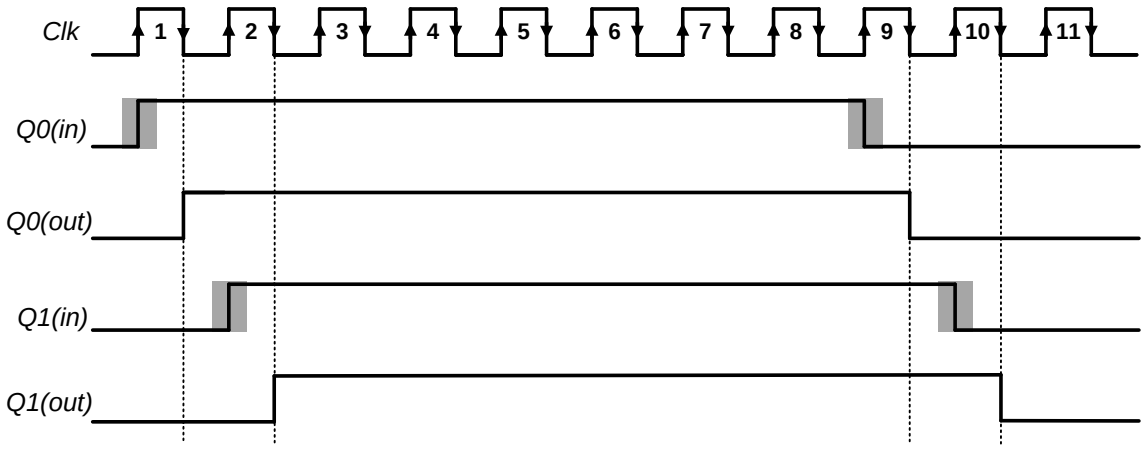


Fig. 4.10. Multi-phase synchronizer waveform

The grey area along with rising and falling edge of the synchronizer inputs are undeterministic timing variation. With the help of transmission gate, $Q(out)$ in each

signal path is able to synchronize with the falling edge of Clk, and the phase shift sequence for all signal paths are maintained. Consequently, the timing accuracy of the 16 different phase-shifted square-wave signal can be improved in this way.

4.6 Resistor string summer

Resistor string summer is used to sum up the phase-shifted square-wave signals with given coefficients calculated from mathematical tools. Aside from resistor string summer, there are also other alternatives to realize the same function. For active circuit implementation, current steering summer is widely used especially for digital-to-analog convertor (DAC) applications. For passive circuit implementation, either resistors or capacitors can be used as the elements of the summer.

Current steering summer is a very prominent approach for summer due to its high speed operation and small area occupied. And [24], [25] give some example of current steering summer design based on different systems. Fig. 4.11 illustrates the circuit implementation of current steering summer in differential mode.

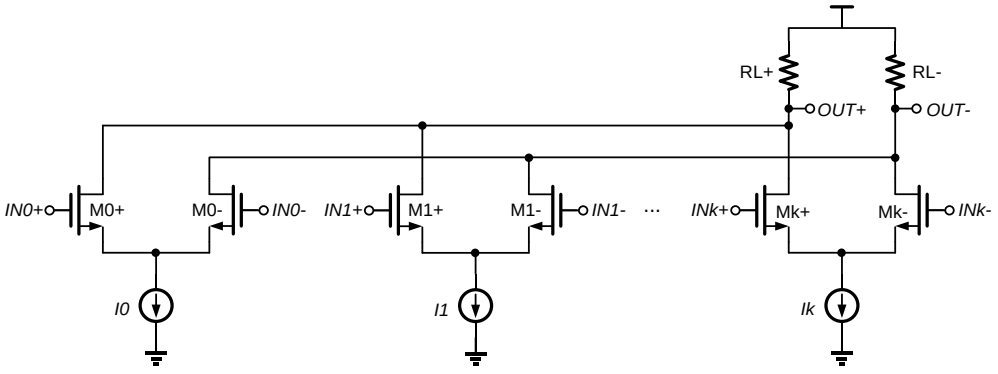


Fig. 4.11. Current steering summer

The square-wave signals of different phase shifts are injected to the gates of differential transistor pairs $M0, M1, \ldots Mk$. The summer coefficient of each input signal is implemented by giving bottom current sources different values as $I0, I1, \ldots Ik$. Finally, all the currents are summed up at the load resistor R_L, and differential output voltage is obtained at OUT^+ and OUT^-.

The limitation of current steering summer is the active circuit intrinsic nature, which suffers more or less from linearity problem. Especially when large output swing is desired and low supply voltage is employed in advanced CMOS technology, the issue becomes more severe. In addition, In addition, the low output impedance of current steering summer is difficult to drive passive LPF, and simple digital buffers cannot be inserted. Instead, although resistor string summer is slower than current steering summer, it can overcome other limitations of current steering summer. And to process a MHz range signal summation, resistor string summer is sufficient with good matching accuracy.

As is discussed that from mathematical calculation, the accurate summing coefficient for time shift sequence $[\pm m_0, \pm m_1, \pm m_2, \pm m_3] = [\pm 0, \pm 1, \pm 2, \pm 3]$ is $[A_0, A_1, A_2, A_3] = [1, 1.8478, 1.4142, 0.7654]$. With approximation of 5-bit resolution, the new summing coefficient which can be realized in circuit is $[\alpha_0, \alpha_1, \alpha_2, \alpha_3] = [17, 32, 24, 13]$. For the resistor string summer, if all unit resistors are connected in parallel to do the summing operation, $[\alpha_0, \alpha_1, \alpha_2, \alpha_3]$ is the number of unit resistors for each signal path. The architecture for resistor string summer connected in parallel is showed in Fig. 4.12.

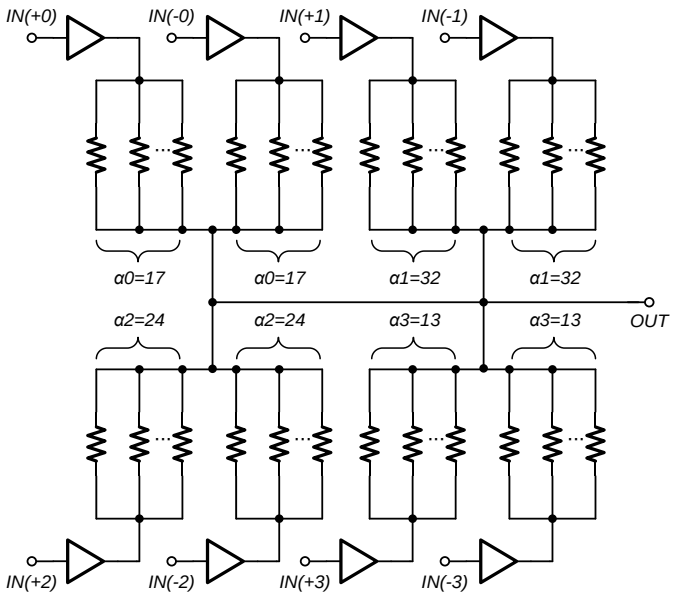


Fig. 4.12. Resistor string summer with parallel architecture

However, as is shown in Fig. 4.13, the parallel resistors will result in a very small equivalent resistance, which will bring up significant matching issue with the consideration of the output resistance of buffers which drive each signal path of the summer.

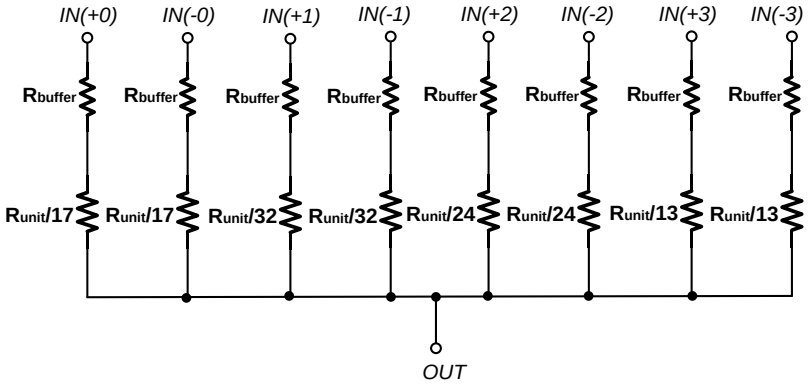


Fig. 4.13. Equivalent resistor string summer in parallel

Another way to implement resistor string summer is to put all the unit resistors for each signal path in series, as shown in Fig. 4.14. As the larger number of unit resistors for a certain signal path is, the less current is injected from the corresponding input, so the summing coefficient should be inversely proportional to $[\alpha_0, \alpha_1, \alpha_2, \alpha_3]$. After calculation, the new summing coefficient for time shift sequence $[\pm 0, \pm 1, \pm 2, \pm 3]$ is $[\beta_0, \beta_1, \beta_2, \beta_3] = [24,13,17,32]$.

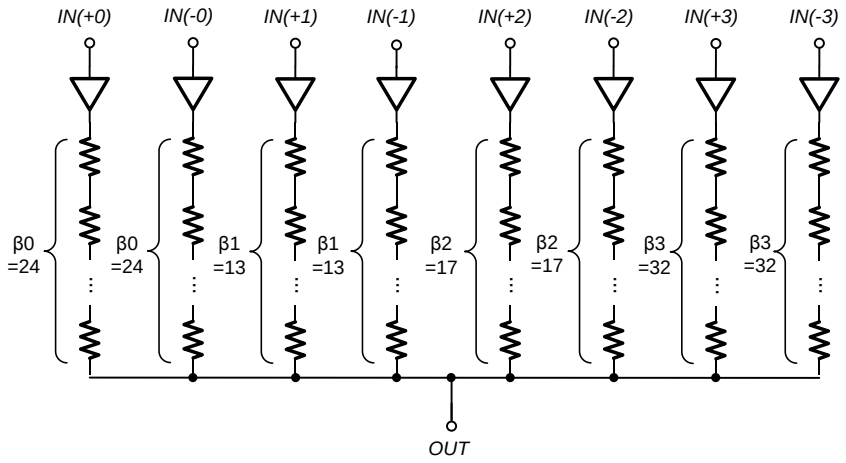


Fig. 4.14. Resistor string summer in series

The equivalent resistor string summer for the architecture in series is showed in Fig. 4.15. The unit resistor is $6k\Omega$, and the buffer output resistance is less than $1k\Omega$. The accuracy of the summer is not affected by considering the buffer output resistance.

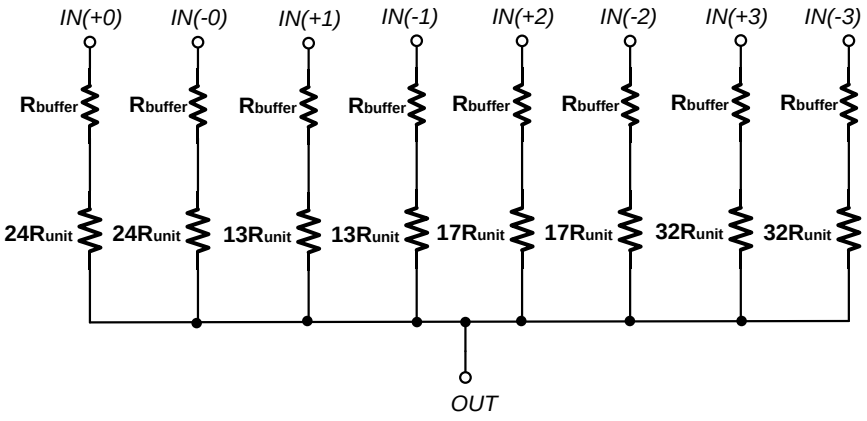


Fig. 4.15. Equivalent resistor string summer in series

The quadrature output sinusoidal signals with differential mode are required in this design. Differential operation has a higher immunity to environment noise and also even harmonics can be suppressed [26]. And quadrature outputs are used to realize the demodulation operation for the bio-impedance spectroscopy application.

Based on the total phase shifts N=16, time shift sequence $[\pm 0, \pm 1, \pm 2, \pm 3]$ is a fundamental pattern to lead to one version of sinusoidal output. As is already learned, there are 16 time-shifted signals named $Q_0, Q_1, Q_2, \ldots Q_{15}$ provided from multi-phase signal generator. As is shown in Table IX, phase of a whole cycle is 360°, which corresponds to 16 time shifts. Considering there is 180° phase shift between the differential signals, which corresponds to 8 time shifts. While there is 90° phase shift between the quadrature signals, indicating 4 time shifts. Fig. 4.16 provides a more intuitive view of comparing the differential pattern and the quadrature pattern compared with the main pattern version in time domain.

Table IX

PHASE SHIFT AND TIME SHIFT CONVERSION FOR N=16

	One cycle	Differential	Quadrature
Phase shift	360°	180°	90°
Time shift	16	8	4

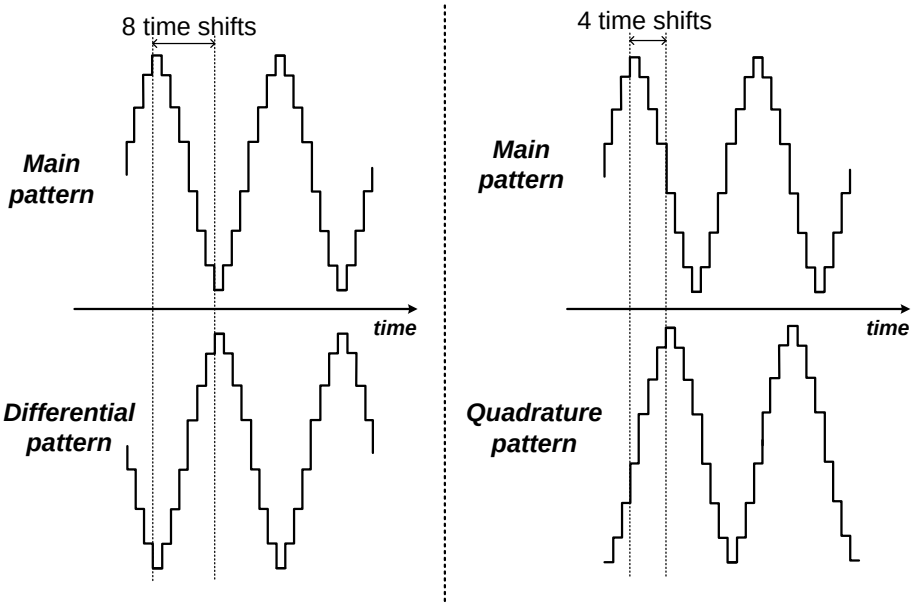


Fig. 4.16. Quadrature output waveform in differential mode

To obtain the quadrature output waveform, the total time shifts N is required to be integer times of 4, such as 12, 16, 20 and 24. The Table X takes N=18 as an example to explain the reason. In this case, the time shift for quadrature signals is 4.5, which is unattainable in the circuit implementation. That's why it fails for our purpose of the design.

Table X

PHASE SHIFT AND TIME SHIFT CONVERSION FOR N=18

	One cycle	Differential	Quadrature
Phase shift	360°	180°	90°
Time shift	18	9	**4.5**

Consequently, with 16 phase-shifted square-wave signals $Q_0, Q_1, Q_2, \ldots Q_{15}$ available, the required signal paths for each sinusoidal signal version are listed in Table XI. And I+, I-, Q+, Q- are the four branches of differential and quadrature output signals.

Table XI

REQUIRED SIGNAL PATHS FOR EACH SINE SIGNAL VERSION

	IN(+0)	IN(-0)	IN(+1)	IN(-1)	IN(+2)	IN(-2)	IN(+3)	IN(-3)
I+	Q0	Q0	Q1	Q15	Q2	Q14	Q3	Q13
I-	Q8	Q8	Q9	Q7	Q10	Q6	Q11	Q5
Q+	Q4	Q4	Q5	Q3	Q6	Q2	Q7	Q1
Q-	Q12	Q12	Q13	Q11	Q14	Q10	Q15	Q9

As is shown in Fig. 4.17, to reduce the summing coefficient mismatches brought by process variation, interdigitized technique should be applied to the layout of resistor string summer. Moreover, the unit resistor sequence for each path is fully randomized, which is listed in Table XII. And the number 1, 2, 3 and 4 denote the unit resistor from the four signal paths $IN(0), IN(1), IN(2), IN(3)$ respectively..

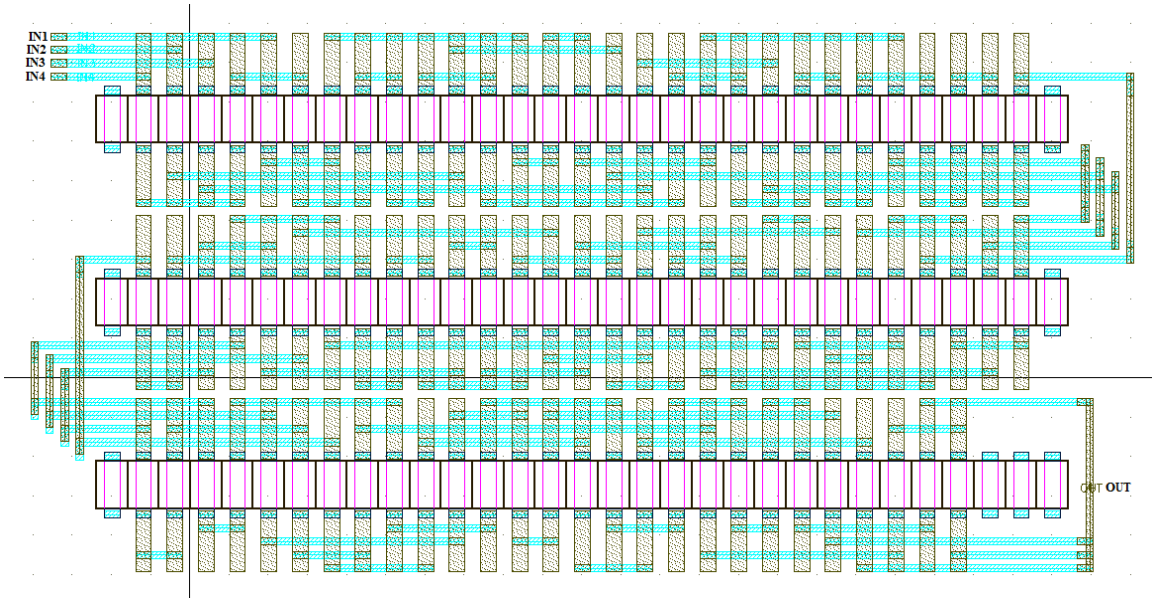


Fig. 4.17: Layout of resistor string adder

Table XII

RESISTOR STRING ADDER SEQUENCE

Row	Resistor string finger sequence														
1st	4	2	3	4	1	4	1	4	4	4	2	4	1	1	1
	2	3	4	1	4	3	4	4	4	1	4	4	4	4	
2nd	4	4	3	1	3	2	1	4	4	4	3	3	4	2	3
	4	2	4	3	4	1	1	2	2	1	4	1	3	1	
3rd	3	3	1	1	2	3	4	3	1	4	2	1	2	2	4
	1	4	1	3	1	1	1	2	4	3	1	3			

4.7 Passive RC LPF

All circuits discussed above make up the DHC module, which cancels out the low order harmonics. A LPF as the last stage is used to eliminate the uncompensated high order harmonics to obtain a highly linear sinusoidal wave eventually.

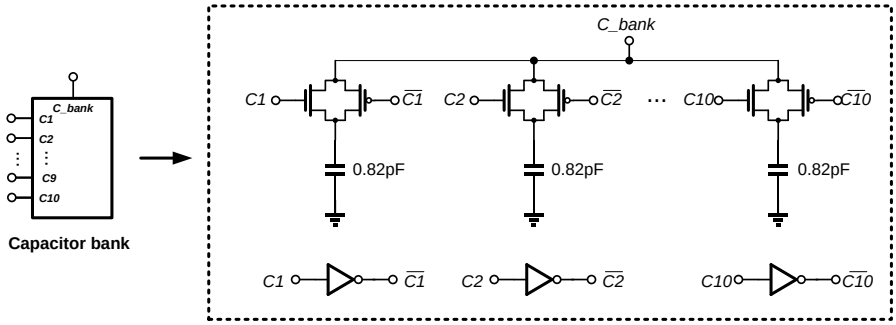
Though passive RC LPF is selected as the final architecture for the filter, some other active alternatives are already considered. Active RC filter and Gm-C filter, though can achieve accurate tuning of bandwidth, voltage gain higher than unity and high Q-factor, suffer from the inherent linearity restriction and large power consumption. Switched capacitor (SC) filter has aliasing issue, and also non-overlapping clocks with very high frequency are required. As for passive RC filter, it occupies large silicon area, has low frequency range behavior and has DC gain less than unity. But the benefit of high linearity feature makes it a suitable option for this system. The 3^{rd} order is chosen for the passive RC filter, and it is sufficient to suppress the uncompensated 15^{th} and 17^{th} harmonics.

For the passive RC LPF design, there is also concern of how to tune the bandwidth of the filter. If both resistors and capacitors can be programmable in certain scale, the silicon area occupied by LPF can be largely minimized. However, CMOS switches, which control the tuning operation, introduce both parasitic capacitance and resistance. For the case of resistor tuning, if there is large voltage swing for the signal passing through LPF, the equivalent on-resistance of CMOS switches vary with the voltage level. As a result, the linearity of the whole filter is degraded. Instead, the switches which are used to tune the capacitor bank can avoid this issue when placing them at the bottom plates of the capacitors. Eventually, the LPF in this work is programmable based on tuning capacitor bank.

The other problem for the LPF design is the very wide bandwidth tuning range which covers three frequency decades. Based on the author's knowledge from literature works and industrial products, all designs which involve in wide bandwidth tuning range

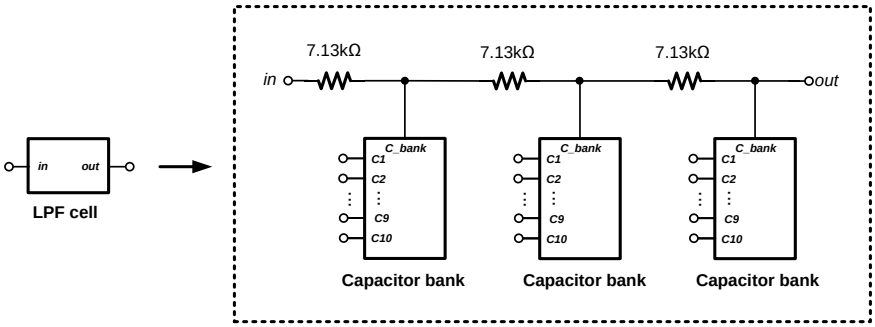
for passive filters are implemented with discrete components on PCB. As required for the design of this thesis, three frequency decades indicates the capacitance value of the capacitor bank should be tunable in 1000 times range. For double-poly capacitor which is used in LPF design, the bottom plate to substrate parasitic capacitor is as much as 10% of main capacitance. So it is unpractical to make the minimum capacitor tunable step as large as the parasitic capacitance of some larger tunable capacitors in the capacitor bank. In addition, to realize the very low bandwidth for the LPF, very large resistors or capacitors are required which surpass silicon area quota. Consequently, this chip only tests the frequency range from around 0.1MHz to 1MHz.

The LPF hierarchy design is illustrated in Fig. 4.18. Fig. 4.18(a) is the capacitor bank implementation which uses 10 control signals C1, C2,…C10 to enable and disable 10 identical unit capacitor of 0.82pF for each. Fig. 4.18(b) is a LPF cell to process a certain signal path coming from resistor string summer. And Fig. 4.18(c) shows four LPF cells with a whole LPF module to process all four signal paths, which are I^+, I^-, Q^+ and Q^- respectively.

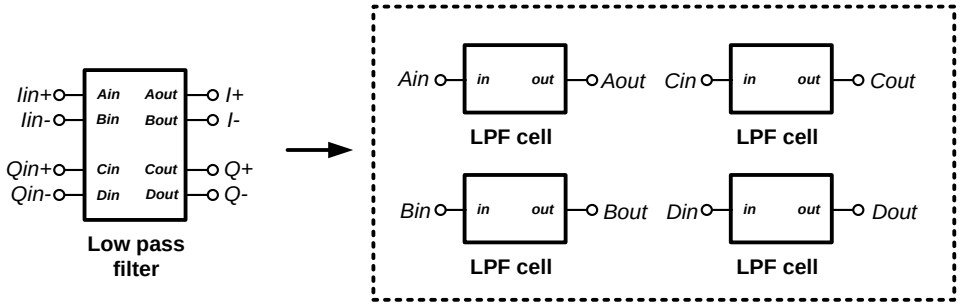


(a)

Fig. 4.18: LPF hierarchy design (a) capacitor bank (b) LPF cell (c) LPF module



(b)



(c)

Fig. 4.18: Continued

The simulation finds out the bandwidth for LPF by enabling different number of capacitors with capacitor bank in Table XIII.

Table XIII

PROGRAMMABLE BANDWIDTH OF LPF

Number of capacitors	Bandwidth
1	1.45MHz
2	0.91MHz
3	0.67MHz
4	0.52MHz
5	0.42MHz
6	0.37MHz
7	0.32MHz
8	0.28MHz
9	0.25MHz
10	0.23MHz

5. EXPERIMENTAL/SIMULATION RESULTS (0.5um/0.18um)

The proposed architecture is designed with OnSemi 0.5um technology and IBM 0.18um technology respectively. For the 0.5um technology design, the chip is already taped out and measured. The experimental results are presented in this section. As for the 0.18um technology design, it is still in the phase of schematic design and layout, and the chip is scheduled to be submitted for fabrication and tested later. Thus, the schematic simulation is shown in this section.

5.1 Experimental results for 0.5um technology design

The proposed sinusoidal oscillator was fabricated in OnSemi 0.5um technology. The chip has area of 0.76mm^2 and packaged with DIP40. The chip micrograph is shown in Fig. 5.1.

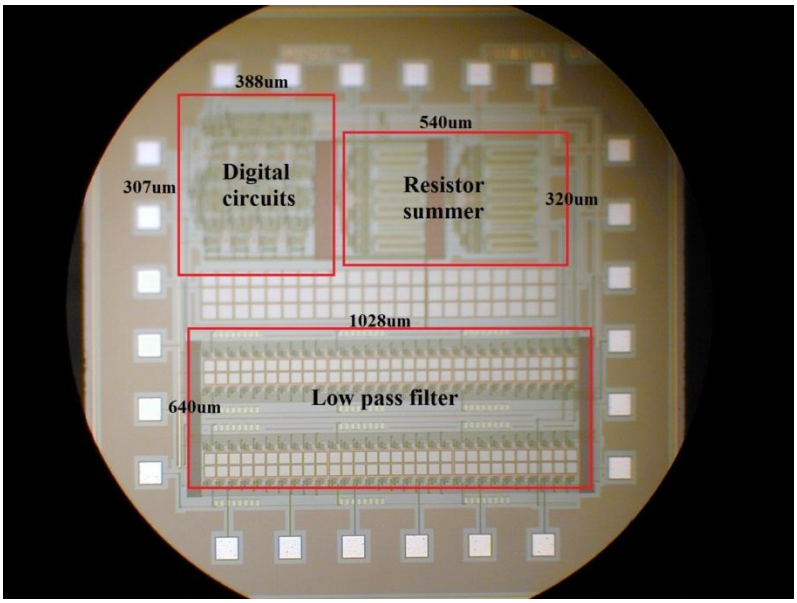


Fig. 5.1. Chip micrograph

5.1.1 Test bench setup

The PCB for testing the sinusoidal oscillator is fabricated using two-layer copper plate. Test setup for PCB is illustrated briefly in Fig. 5.2. DIP switch on the top is used to select the required frequency range, and DIP switch at the bottom is used to tune the LPF bandwidth. Tactile switch is employed to reset the D flip-flops of multi-phase generator when the whole test board circuits are powered on. Switch debouncer is used to suppress the voltage ringing by pushing the button of tactile switch. Moreover, the power supply of the chip is provided from a LDO. The oscilloscope is with the model of Tektronix TDS 3054, which has the sampling rate of 5Gs/s.

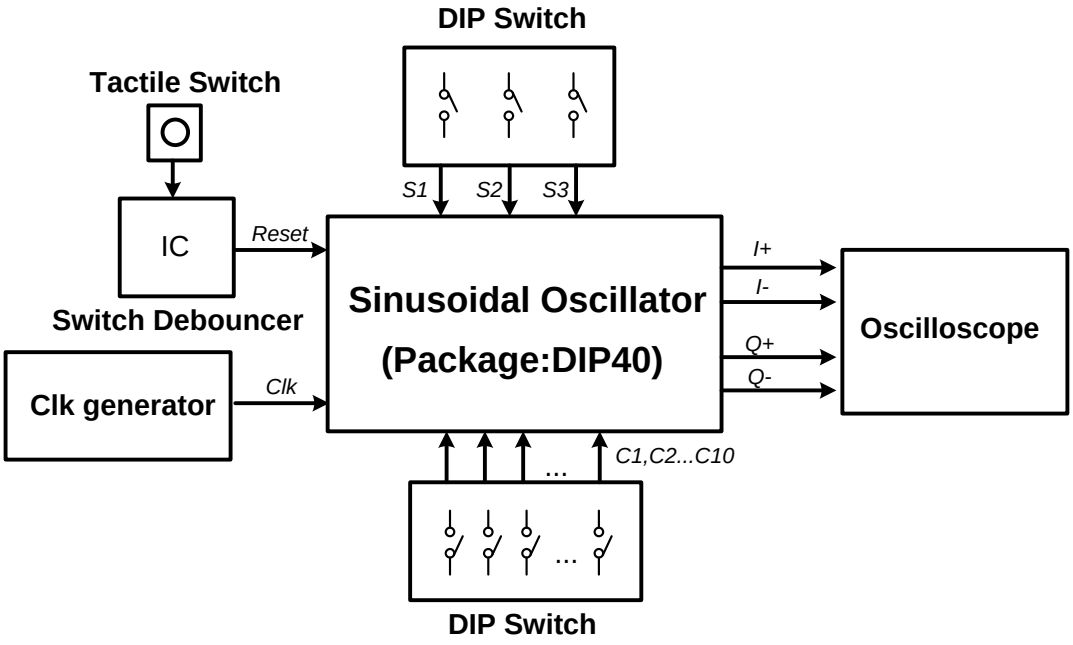


Fig. 5.2. Test setup

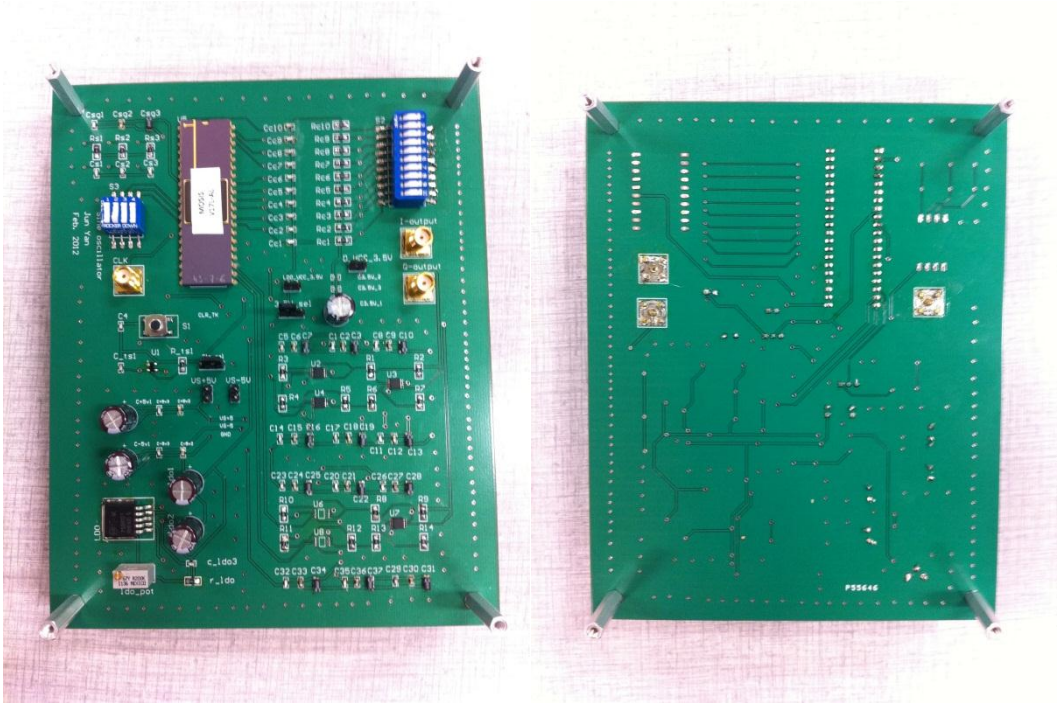


Fig. 5.3. PCB photo

The photos of the PCB for testing are shown in Fig. 5.3. And the photos of oscilloscope when showing the differential sinusoidal signals and quadrature sinusoidal signals are demonstrated in Fig. 5.4 and Fig. 5.5.

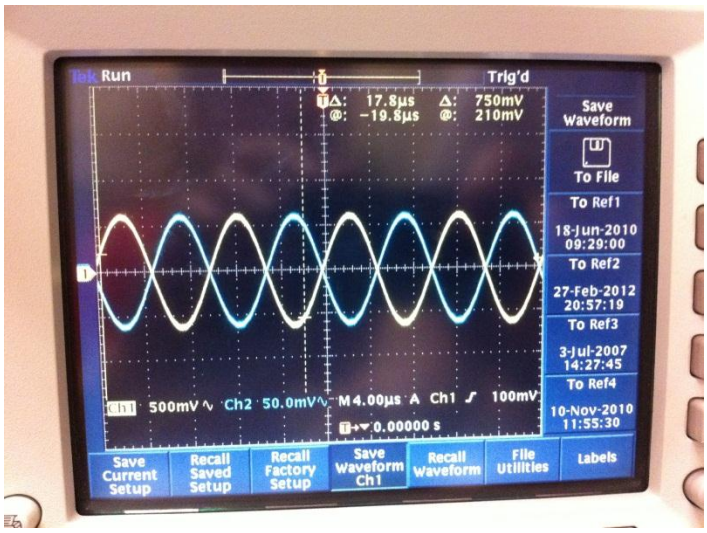


Fig. 5.4. Differential sinusoidal signals from oscilloscope

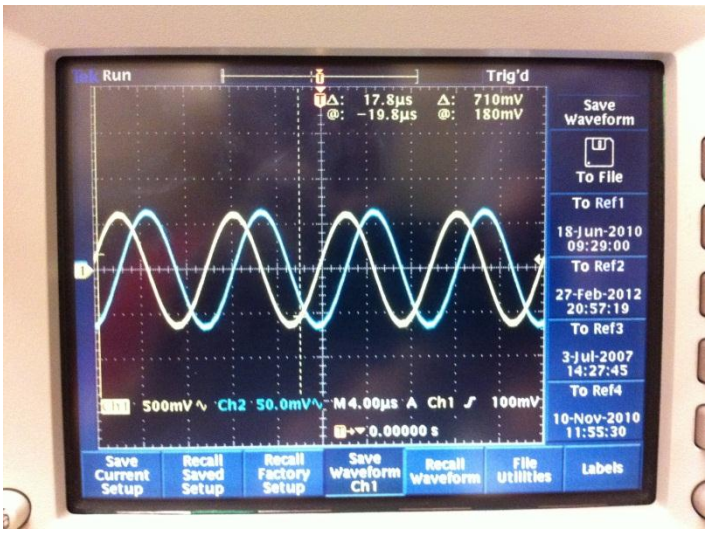


Fig. 5.5. Quadrature sinusoidal signals from oscilloscope

5.1.2 Experimental results

The waveform data of sinusoidal oscillator output is observed and recorded from the oscilloscope, and it is imported into the computer to do the post-processing with Matlab. The time domain waveform is showed in Fig. 5.6. As is seen, the waveform

demonstrates very good sinusoidal shape, but with high frequency noise accompanied with the signal. The high frequency noise results mainly from the design of this sinusoidal chip. The isolation for the power supply to provide high frequency master clock signal and the power supply of buffers to drive the low frequency phase-shifted square wave signals is neglected. Thus, there will cause the interference of signals through power supply, and purity of the sinusoidal signals is degraded. This deficiency can be solved in the design of next run.

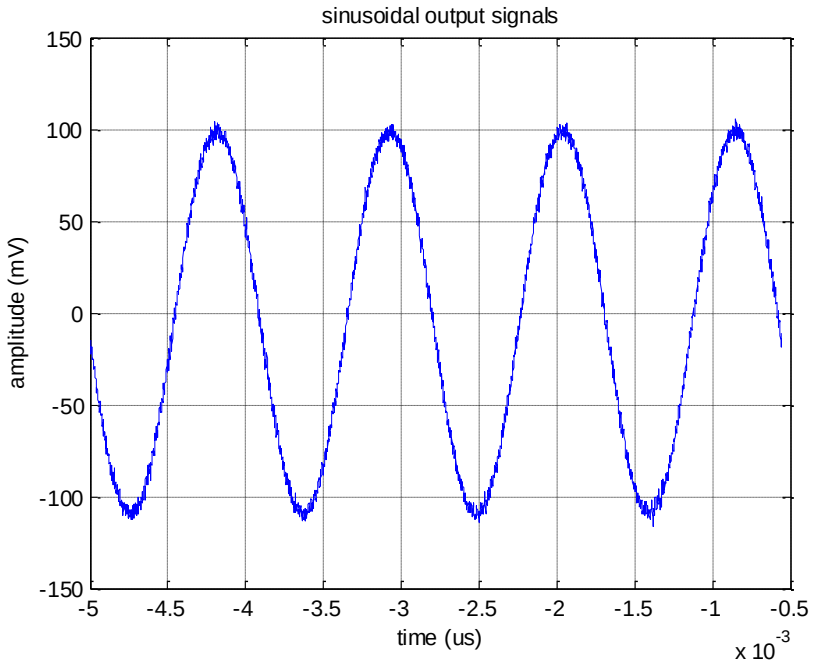


Fig. 5.6. Sinusoidal output waveform

Fig. 5.7 shows the spectrum of a sinusoidal output waveform when the LPF module is shut off. As it clearly demonstrates that the low order harmonic signals are cancelled out through the DHC module, while the 15^{th} and 17^{th} are left uncompensated.

However, when LPF module is introduced, these uncompensated high order harmonics will be largely suppressed.

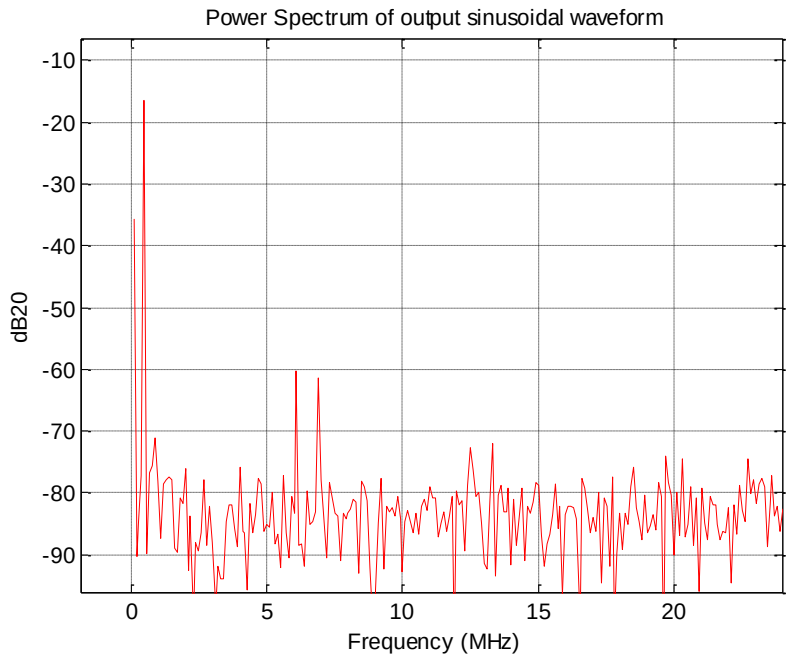


Fig. 5.7. Spectrum of sinusoidal output without LPF

The spectrum analysis is carried for the output sinusoidal signals with frequency range from 0.1MHz to 0.9MHz with 0.1MHz interval. One spectrum graph showed in Fig. 5.8 is for 0.9MHz output signal. As it is observed, the HD2 is -59.74dB and HD3 is -60dB. Also, there is another obvious tone at the high frequency which is around 16 times of the output frequency. The harmonic is not the uncompensated harmonics, instead this is the interference from the master clock, which is conveyed and injected to output signal through power supply line. Other HD2 and HD3 data for different frequency is showed in Fig. 5.9. The reason for the harmonic distortion degradation at lower frequency is

because the LPF design for lower frequency includes a very large tunable capacitor. With the limitation of chip area, this required total tunable capacitance value is reduced for the practical consideration.

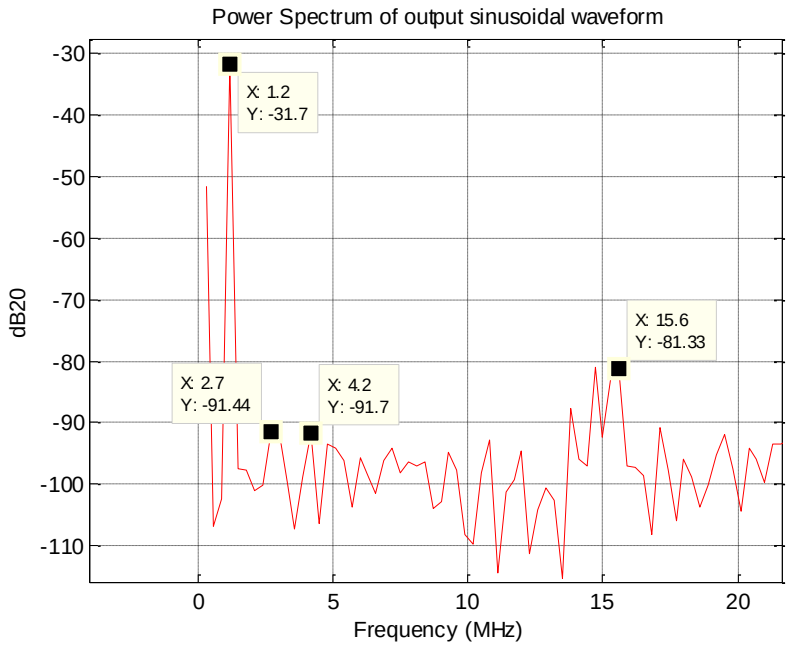


Fig. 5.8. Spectrum of sinusoidal signal at 0.9MHz

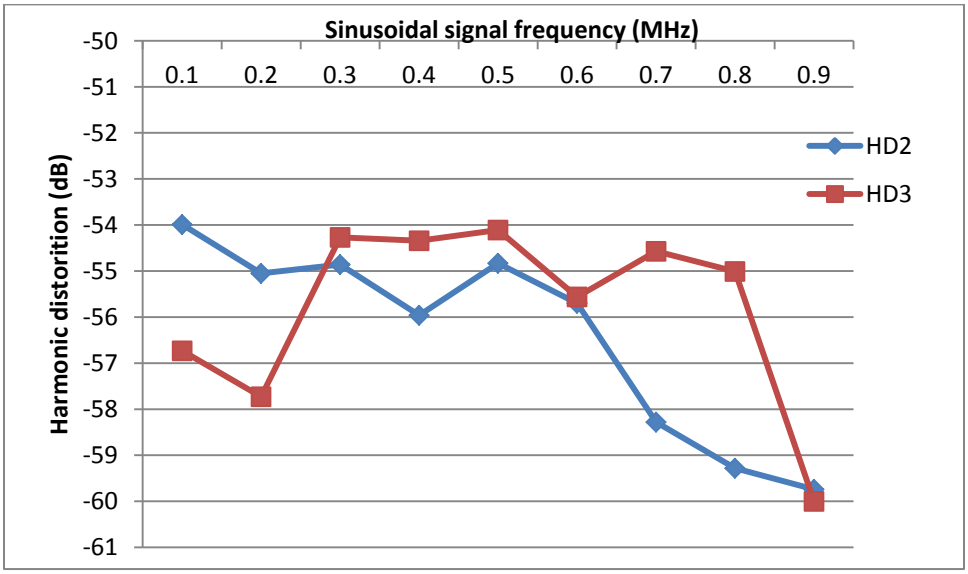


Fig. 5.9. HD2 and HD3 vs. output frequency

5.2 Simulation results for 0.18um technology

The proposed architecture is also implemented in IBM 0.18um technology. And there are two aspects of improvement to implement the circuit in this advanced technology.

Firstly, there is technology performance improvement. Design in 0.18um is faster, consume less power and area. Moreover, MIM capacitor is available, and less parasitic capacitance is involved, which is good news for the precision of LPF design. In addition, QFN package is employed for the package, and less parasitic capacitance and bondwire inductance is involved.

Secondly, there is some design modification and improvement. As a faster technology is used, the new work will focus on the frequency range of 10-40MHz with quadrature output. Moreover, better clock distribution for the multi-phase synchronizer module is used to reduce phase mismatches. In addition, separate power supply and ground is provided for the sensitive circuit modules to reduce noise level and cross-talk phenomenon. Also, the design variables for the system are optimized.

The preliminary simulation results are obtained as following. Fig. 5.10 shows the differential output waveform of sinusoidal oscillator, and Fig. 5.11 shows the corresponding spectrum response with 10MHz output. As if observed that HD2=-83.13dB, HD3=-72.19dB, HD5=-72.24dB, HD15=-75.9dB and HD17=-80.43dB. This harmonic distortion performance reflects that:

1. Even harmonics are suppressed with differential mode.
2. Odd harmonics are cancelled out with digital harmonic distortion technique.
3. 15^{th} and 17^{th} harmonics are fully suppressed with low pass filter.

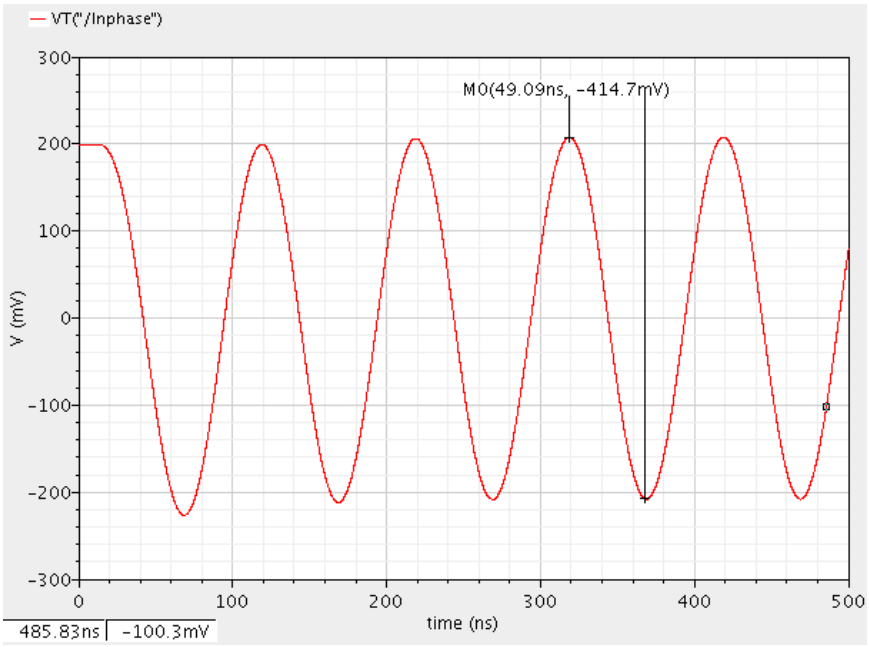


Fig. 5.10. Differential output waveform of sinusoidal oscillator

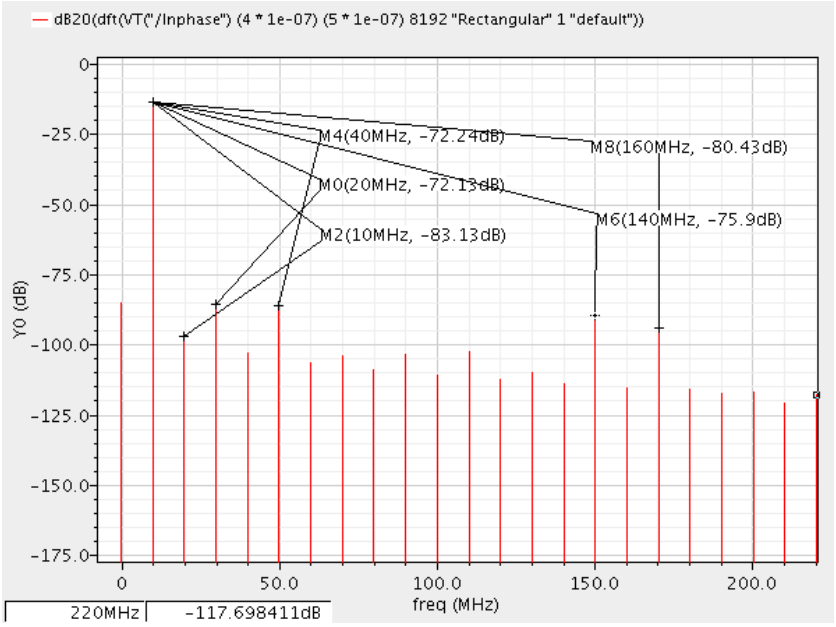


Fig. 5.11. Spectrum response for 10MHz output sinusoidal signal

In addition, the sinusoidal oscillator is with power supply of 1V and consumes 0.44mW for 10MHz output.

5.3 Comparison of state-of-art

Table XIV

SINUSOIDAL OSCILLATOR COMPARISON

	JSSC' 2010 [4]	**JSSC' 2007 [18]**	**JET' 2011 [27]***	**This work (0.5um)**	**This work (0.18um)****
Frequency	10MHz	10MHz	40.7MHz	0.9MHz	10MHz
Power	4.04mW	20.1mW	Not reported	2.98mW	0.4mW
Area	$0.186mm^2$	$0.2mm^2$	$0.1mm^2$	$0.76mm^2$	----------
Technology	0.13um	0.35um	0.35um	0.5um	0.18um
Supply	1.2V	3.3V	Not reported	2.5V	1V
THD	-72dB	-54.8dB	-72dB	-60dB	-72dB
Quadrature	No	No	No	Yes	Yes

* This work only has post-layout simulation results.

** The design only includes schematic simulation results for the moment.

6. CONCLUSION

A novel architecture has been proposed for the sinusoidal oscillator which employs digital harmonic cancellation technique to remove low order harmonic tones. This architecture delivers quadrature sinusoidal signals with frequency tunable over a certain frequency range. Due to the digital nature of this technique, this architecture consumes less power, more insusceptible to noise and it is easy to be redesigned in a different CMOS technology. A 3rd order low pass filter is used to as an auxiliary module to remove high order harmonics.

There are other works in literature, which also employ digital harmonic cancellation techniques. Some are based on feedback architecture [18], and some are based on open-loop architecture [4] [16]. The feedback architecture requires analog circuits and it is more power consuming and difficult in design, while open-loop architecture contains pure digital circuits and passive components. Thus, open-loop architecture is preferred for sinusoidal oscillator design from the literature review of recent years, and the proposed work also employs this architecture. However, the other open-loop-based sinusoidal oscillators use the summing ratio of different phase shift signals to be identical, while the proposed architecture has the summing ratio to be designable. As a result, the proposed architecture requires a slow master clock to produce the sinusoidal signal of same frequency. And also quadrature sinusoidal outputs are attainable based on the architecture.

OnSemi 0.5um CMOS technology through MOSIS educational service has been used to design and fabricate the proposed sinusoidal oscillator. The experimental results of this work show that it can achieve HD2 is -59.74dB and HD3 is -60dB at 0.9MHz, and

the frequency is tunable over 0.1MHz to 0.9MHz. The chip consumes area of 0.76mm^2. Low pass filter takes majority of area, and resistor string summer is in the second place. The power consumption at 0.9MHz is 2.98mW.

Considering the performance of the design in OnSemi 0.5um CMOS technology is not competitive with the state-of-art, the proposed architecture is also implemented in IBM 0.18um technology. The digital nature of the design makes the performance benefit from the scaling of technology tremendously in the aspect of power and area consumption. Also MIM capacitor with much less parasitic capacitance is available in this process, indicating a better performance of LPF design. QFN package will be used for the new chip, which will also improve the experimental results. Moreover, there are also some additional solutions to overcome the design deficiencies of the 0.5um chip, and the performance will be optimized. The preliminary simulation results show that the 0.18um design can realize total harmonic distortion of -72dB at 10MHz with the power consumption of 0.4mW. Though the performance will be degraded for post-layout simulation and final experimental results, the new design is still competitive with the state-of-art.

REFERENCES

[1] J. Wibbenmeyer, C.H. Chen, "Built-in self-test for low-voltage high-speed analog-to-digital converters," *IEEE Trans. Instrum. Meas.*, vol. 56, no. 6, pp. 2748-2756, Dec. 2007.

[2] M. A. Dominguez, J. L. Ausin, J. F. Duque-Carillo, and G. Torelli, "A high quality sine-wave oscillator for analog built-in self-testing," in *IEEE ISCAS Dig. Tech. Papers*, May 2006, pp.3454-3457.

[3] Méndez-Rivera, A. Valdes-Garcia, J. Silva-Martinez, and E. Sánchez-Sinencio, "An on-chip spectrum analyzer for analog built-in testing," *J. Electronic Testing: Theory and Applications*, vol. 21, no.3, pp. 205–219, June 2005.

[4] M. M. Elsayed, E. Sánchez-Sinencio, "A low THD, low power, high output-swing time-mode-based tunable oscillator via digital harmonic-cancellation technique," *IEEE J. Solid-State Circuits*, vol. 45, no. 5, pp. 1061-1071, May 2010.

[5] M. Soda, Y. Bando, S. Takaya, T. Ohkawa, T. Takaramoto, T. Yamada, S. Kumashiro, T. Mogami, and M. Nagata, "On-chip sine-wave noise generator for analog IP noise tolerance measurements," in *Proc. IEEE ASSCC*, Nov. 2010, pp. 1-4.

[6] C. Wade, and J. Wade, *The impact of medical applications on the electronics industry*, Technology Forecaster Inc., Santa Clara, 2010.

[7] American Cancer Society, "Cancer facts and figures 2011", American Cancer Society, Atlanta, GA, 2011.

[8] S. Grimnes, O. G. Martinsen, *Bioimpedance and bioelectricity basics*, Academic Press, New York, 2000.

[9] H. P. Schwan, "Electrical properties of tissue and cell suspension," *Adv. Biol. Med. Phys*, pp. 147-209, 1957.

[10] A. I. Cano, "Contributions to the measurement of electrical impedance for living tissue ischemia injury monitoring," Ph.D. Thesis, Barcelona, Feb. 2005.

[11] D. G. Beetner, S. Kapoor, S. M. Manjunath, X. Zhou, and W. V. Stoecker, "Differentiation among basal cell carcinoma, benign lesions, and normal skin using electrical impedance," *IEEE Transaction on Biomedical Engineering*, vol. 50, no. 8, pp. 1020-1025, Aug. 2003.

[12] R. Dua, D. G. Beetner, W. V. Stoecker, and D. C. Wunsch, II, "Detection of basal cell carcinoma using electrical impedance and neutral networks," *IEEE Transaction on Biomedical Engineering*, vol. 51, no. 1, pp. 66-71, Jan. 2004.

[13] P. Åberg, I. Nicander, J. Hansson, P. Geladi, U. Holmgren, and S. Ollmar, "Skin cancer identification using multifrequency electrical impedance - a potential screening tool," *IEEE Transaction on Biomedical Engineering*, vol. 51, no. 12, pp. 2097-2102, Dec. 2004.

[14] J. Schröder, S. Doerner, T. Schneider, and P. Hauptmann, "Analogue and digital sensor interfaces for impedance spectroscopy", *Measurement Science and Technology*, vol. 15, pp. 1271-1278, 2004.

[15] D. Tsunami, J. McNames, A. Colbert, S. Pearson, and R. Hammerschlag, "Variable frequency bioimpedance instrumentation," in *Proc. 26th Ann. Inter. Conf. IEEE Eng. Med. Biol. Soc.*, Sep. 2004, pp. 2386-2389.

[16] M. M. Abdul-Latif, M. M. Elsayed, and E. Sánchez-Sinencio, "A wideband millimeter-wave frequency synthesis architecture using multi-order harmonic-

synthesis and variable N-push frequency multiplication," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1265-1283, June 2011.

[17] K. Martin, and D. Johns, *Analog integrated circuit design*, New York: Wiley, 1997.

[18] S. W. Park, J. L. Ausín, F. Bahmani, and E. Sánchez-Sinencio, "Nonlinear shaping SC oscillator with enhanced linearity," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2421-2431, Nov. 2007.

[19] R. Chebli, X. Zhao, and M. Sawan, "A wide tuning range voltage-controlled ring oscillator dedicated to ultrasound transmitter," in *Proc. Int. Conf. Microelectron.*, Dec. 2004, pp. 313-316.

[20] N. Retdian, S. Takagi, and N. Fujii, "Voltage controlled ring oscillator with wide tuning range and fast voltage swing," in *Proc. IEEE Asia-Pacific Conf. ASIC*, Aug. 2002, pp. 201–204.

[21] M. Sheu, T. Lin, W. Hsu, "Wide frequency range voltage controlled ring oscillators based on transmission gates", in *Proc. ISCAS IEEE Int. Circuits Syst. Symp.,* May 2005, pp. 2731- 2734.

[22] H. Chang, J. Chang, C. Kuo, and S. Liu, "A 0.7-2-GHz self-calibrated multiphase delay-locked loop", *IEEE J. Solid-State Circuits*, vol. 41, no. 5, May 2006, pp. 1051-1061.

[23] L. Chuang, M. Chang, P. Huang, C. Kan, and W. Hwang, "A 5.2mW all-digital fast-lock self-calibrated multiphase delay-locked loop", *IEEE Int. Symp. on Circuits and Systems*, pp. 3342-3345, May 2008.

[24] D. A. Mercer, "Low-power approaches to high-speed current-steering digital-to-analog converters in 0.18um CMOS", *IEEE J. Solid-State Circuits*, vol. 42, no. 8, pp. 1688-1698, Aug. 2007.

[25] T. Chen, G. E. Gielen, "A 14-bit 200-MHz current-steering DAC with switching-sequence post-adjustment calibration", *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2386-2394, Nov. 2007.

[26] A. Sedra, and K. C. Smith, *Microelectronic Circuits*, 5th ed. New York: Oxford Univ. Press, 2004.

[27] M. Barragan, D. Vazquez, and A. Rueda, "Analog sinewave signal generator for mixed-signal built-in test application", *J. Electron Test*, pp. 305-320, 2011.

[28] E. Mensink, E. Klumperink, and B. Nauta, "Distortion cancellation by polyphase multipath circuits", *IEEE Transactions on Circuits and Systems*, vol. 52, no. 9, pp. 1785-1794, Sept. 2005.

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