

TUNABLE SUBSTRATE INTEGRATED WAVEGUIDE FILTERS IMPLEMENTED  
WITH PIN DIODES AND RF MEMS SWITCHES

A Thesis

by

MARCELINO ARMENDARIZ

Submitted to the Office of Graduate Studies of  
Texas A&M University  
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2010

Major Subject: Electrical Engineering

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and RF MEMS Switches

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## ABSTRACT

Tunable Substrate Integrated Waveguide Filters Implemented with PIN Diodes  
and RF MEMS Switches. (December 2010)

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Chair of Advisory Committee: Dr. Kamran Entesari

This thesis presents the first fully tunable substrate integrated waveguide (SIW) filter implemented with PIN diodes and RF MEMS switches. The methodology for tuning SIW filters is explained in detail and is used to create three separate designs. Each SIW cavity is tuned by perturbing via posts connecting or disconnecting to/from the cavity's top metal layer. In order to separate the biasing network from the SIW filter, a three-layer PCB is fabricated using Rogers RT/duroid substrates. The first tunable design utilizes the Philips BAP55L PIN diode. This two-pole filter provides six frequency states ranging from 1.55 GHz to 2.0 GHz. Fractional bandwidth ranges from 2.3% – 3.0% with insertion loss and return loss better than 5.4 dB and 14 dB respectively for all frequency tuning states. The second tunable design utilizes the Radant RMSW-100 MEMS switch, providing six states ranging from 1.65 GHz to 2.1 GHz. Fractional bandwidth for this filter varies from 2.5% - 3.0% with insertion loss and return loss better than 12.4 dB and 16 dB respectively for all states. The third design utilizes the OMRON 2SMES-01 RF MEMS relay, providing fourteen states ranging from 1.19 GHz to 1.58 GHz. Fractional bandwidth ranges from 3.6% - 4.4% with

insertion loss and return loss better than 4.1 dB and 15 dB respectively for all frequency states. Two of the three designs (Philips PIN diode and OMRON MEMS) produced good results validating the new SIW filter tuning methodology.

Finally, to illustrate the advantage of microstrip planar structures integrated with SIW structures, low pass filters (LPFs) are implemented along the input and output microstrip-to-SIW transition regions of the tunable SIW filter. With minimal change to the overall filter size, this provides spurious suppression for the additional resonant modes inherently present in waveguide structures. The implemented design utilizes the same OMRON MEMS tunable SIW filter specifications. This two-pole tunable filter provides the same performance as the previous OMRON MEMS design with exception to an added 0.7 dB insertion loss and spurious suppression of -28 dB up to 4.0 GHz for all frequency tuning states.

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## CHAPTER I

### INTRODUCTION

#### A. Substrate Integrated Waveguide Filter Applications

Radio Frequency (RF) filters possess the properties of frequency-selective transmission allowing energy to transmit desirable bandwidths (passbands) and attenuate undesirable bandwidths (stopbands). These microwave filters are essential components for the front-end of today's communication systems. The current progression of wireless communication technologies demand RF front-end designs to have better performance, lower power, and a more compact size. Conventional non-planar structures such as the rectangular waveguide possess the advantage of producing higher performing filters compared to planar configurations due to their lower loss characteristics. However, advantages of planar structures such as microstrip and coplanar waveguide (CPW) filters relate to a more compact size and lower manufacturing cost. Fig. 1 illustrates the two conventional planar and non-planar structures [1].

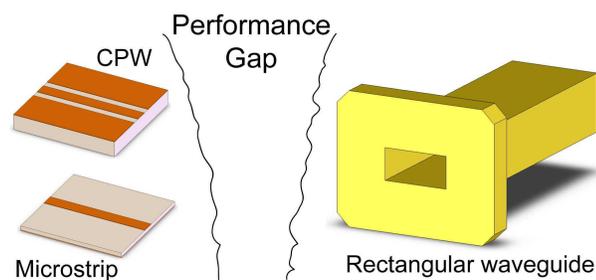


Fig. 1. Performance gap between planar structures (microstrip and CPW) and non-planar structures (rectangular waveguide).

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This thesis follows the style of *IEEE Microwave and Wireless Components Letters*.

The substrate integrated waveguide (SIW) has recently been developed to fill this performance gap by possessing the advantages of both types of structures [1]. The basic concept of the SIW merges waveguide cavities with planar structures on a single dielectric high frequency material. This is accomplished through rows of vias in a substrate dielectric acting as the walls of a waveguide cavity. The top and bottom metal layers of the high frequency PCB material next form the upper and lower cavity walls, while planar transmission lines provide RF input/output [2]. Tapered transition regions are then placed between the planar transmission lines and the top metal layer of each cavity, completing the SIW structure [3]. Fig. 2(a-b) depicts a basic SIW structure and a simple fabricated SIW filter utilizing microstrip transmission lines [4].

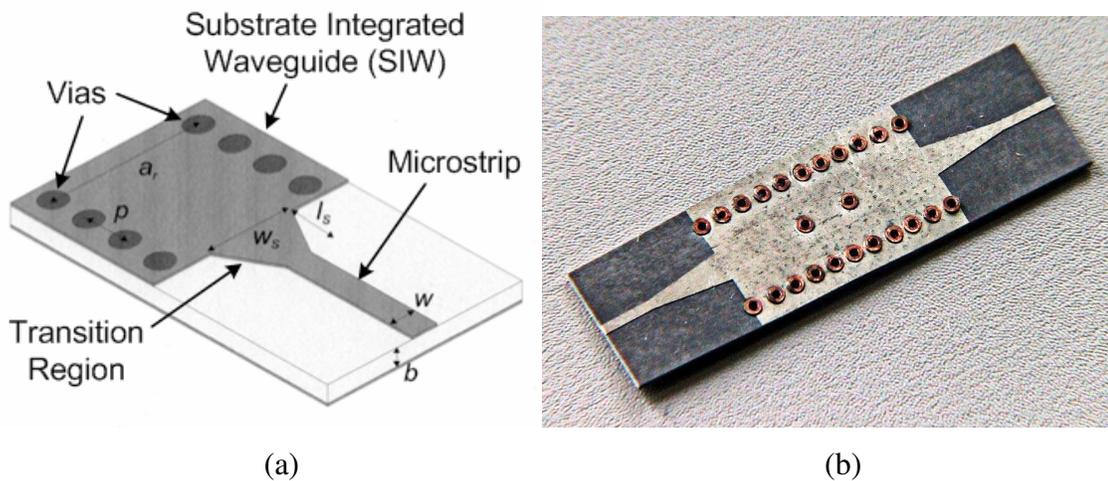


Fig. 2. (a) Basic substrate integrated waveguide (SIW) and (b) simple fabricated SIW filter.

Many applications are attributed to the use of SIW structures. Depending on the configuration, the SIW has been utilized for antenna arrays [5]-[8] and slot antennas [9]-

[11]. For RF circuit applications, proper adjustment to the dimensions of SIW transmission waveguides enable the development of various linear phase shifters [12]-[13]. Additionally, directional couplers [14]-[16], power divider/combiners [17]-[19], and mixers/oscillators [20]-[22], all have been realized through the use of different configurations of multiple SIW cavities.

The most researched application of the SIW involves filter design. Various designs have been implemented to help reduce the size of SIW filters even further including folded substrate integrated waveguide (FSIW) [23]-[24], half-mode substrate integrated waveguide (HSIW) [25], and evanescent-mode SIW filters [26]-[27]. In addition, SIW cavities have been employed to produce higher quality filters compared to planar configurations such as dual-mode SIW filters [29]-[30], compact super-wide bandpass filters [31], and multilayered substrate integrated waveguide (MSIW) filters [32]. Lastly, complete front-end systems regarded as system-in/on-package (SiP/SoP) designs have recently been developed with SIW structures such as an X-band receiver with embedded MSIW filters [33] or a 60 GHz multi-chip module receiver having both an SIW antenna and an SIW filter all on one substrate [34].

## B. Tunable Filter Integration

Tunable microwave filters are critical to RF front-end design through the capability for single systems to select multiple frequencies. For instance, such frequency agile filters provide military radars to scan a wide spectrum along a particular frequency band for electronic counter measure (ECM) applications [35]. Additionally, secure

military communication systems such as frequency hopping transceivers also require the implementation of RF tunable filters [35].

The microwave filter tuning mechanism is classified into three major types: mechanical, magnetic, and electronic [36]. Mechanically tunable filters are realized using co-axial or waveguide resonators and have large power-handling and low insertion loss. However, these tuned filters have slow tuning speed and often are large and more bulky for application in modern integrated systems [37]. Magnetically tunable filters have been used extensively in microwave communication systems and have single-crystal Yttrium-Iron-Garnet (YIG) spheres in their resonators that are tuned by changing the biasing current. Advantages of these filters are very high tuning range, spurious free response, low insertion loss, and high quality factor (Q-factor). Disadvantages include size, power consumption, tuning speed, and incompatibility in integrated systems [38]-[39]. Electronically tunable filters typically employ variable capacitors, semiconductor diodes, or RF MEMS switches that are controlled by applying a bias voltage. This provides the required variance to the capacitive or inductive loading in a resonator thereby electrically shifting the center frequency of the filter. Advantages include high tuning range, compact size, fast tuning, and compatibility to integrate with other front-end systems. However, disadvantages involve lower filter performance parameters compared to magnetic or mechanically tuned filters [40]-[41].

Tuning conventional rectangular waveguides typically involve mechanical or magnetic types of tuning mechanisms, since the resonant-mode is determined by the internal physical dimensions of the waveguide cavity instead of lumped circuit

elements [42]. Consequently, tuning waveguide filters electrically can be the more non-trivial option. However, mechanically or magnetically tuning an SIW filter is also not practical, since the advantages of utilizing standard PCB fabrication techniques for the SIW would be negated due to the complex nature and non-standard materials needed to manufacture such a tunable filter. As a result, current research is limited for tunable SIW filters [43]-[44], only providing possible theories and simulations with no physical evidence of a fully tunable multi-cavity SIW filter on a planar substrate. Currently, no effective methodology has been presented to electrically tune resonant-mode SIW bandpass filters. A novel tuning methodology is therefore presented, providing the first fully tunable SIW filter based on perturbing via posts located inside the cavities. Appropriate positioning of these via posts provides both proper tuning and matching for various states. Multiple states are achieved through connecting/disconnecting the perturbing via posts to/from the SIW cavity top metal layer.

### C. Thesis Overview

Three different tunable SIW filters are designed, fabricated, and characterized through the use of a multi-layer RT/duroid design using PIN diodes and RF MEMS devices as the switching elements. Chapter II covers basic SIW theory with the introduction of the SIW filter tuning methodology. Chapter III discusses the implementation of the tuning methodology on three separate designs utilizing the PIN diode, Radant MEMS, and OMRON MEMS RF switches. Chapter IV illustrates a simple integration of microstrip planar filters with the tunable SIW filter design, creating

an overall high quality, compact size tunable RF filter with spurious suppression.

Chapter V concludes the thesis and discusses possible future work.

## CHAPTER II

### DESIGN OF SUBSTRATE INTEGRATED WAVEGUIDE TUNABLE FILTERS

#### A. Substrate Integrated Waveguide Basic Theory

Substrate Integrated Waveguide (SIW) cavities follow the same basic principles compared to conventional air-cavity rectangular waveguides. Some key differences relate to the dissimilar dielectrics of air versus a substrate material. More care must be taken in order to design SIW cavities for microwave applications. This is due to higher frequencies being more sensitive to substrate losses versus a very low loss air dielectric. Additionally, compared to conventional 3-D rectangular waveguides, thinner substrate dielectrics prevent Transverse Magnetic (TM) modes to resonate. Therefore, only Transverse Electric (TE) modes can effectively propagate through SIW cavities [45].

Given the above distinctions, two primary design rules for SIW cavities are next presented in order to exploit the same modeling and design procedures for conventional waveguides. These rules pertain to the diameter ( $d$ ) of the metal via posts emulating the waveguide side walls and the via post spacing ( $b$ ) [45-46]:

$$d < \lambda_g / 5 \quad (2.1)$$

$$b \leq 4d \quad (2.2)$$

Disregarding these expressions creates too much leakage loss for the via post SIW cavity side walls to perform as conventional rectangular waveguide side walls. Fig. 3 depicts a single SIW cavity resonator with appropriately labeled dimensions.

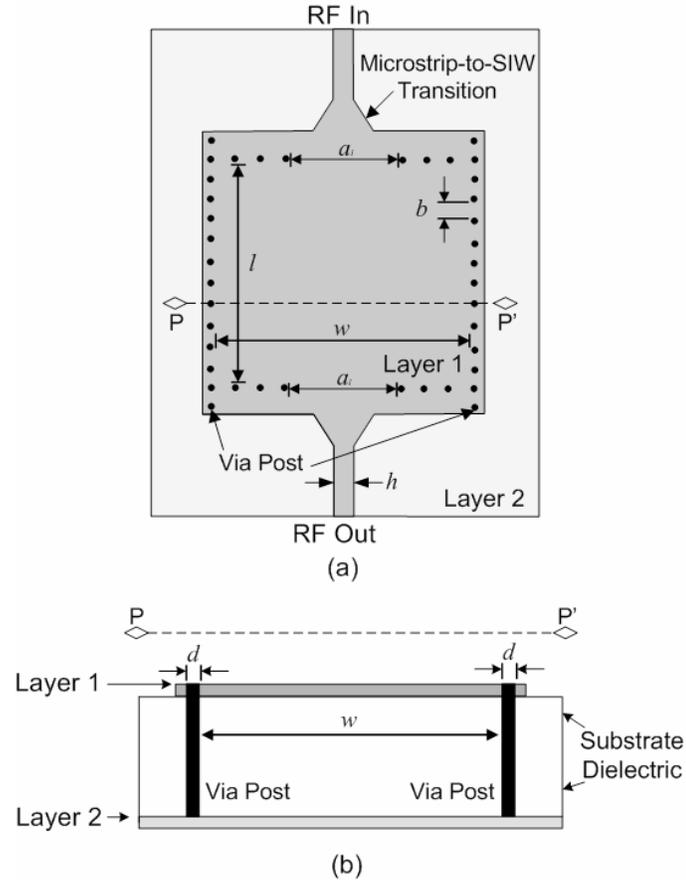


Fig. 3. SIW single cavity resonator, (a) top view and (b) side view.

Metal layers 1 and 2 create the top and bottom terminations of the waveguide with via posts generating the side wall terminations of the waveguide. The  $50\Omega$  microstrip transmission lines (having width  $h$ ) include tapered transition regions that connect to the top metal layer of the SIW cavity resonator. The following expressions provide the first resonant frequency mode for the SIW cavity [47]:

$$f_{101} = \frac{c}{2\pi\sqrt{\mu_r\epsilon_r}} \sqrt{\left(\frac{\pi}{w_{eff}}\right)^2 + \left(\frac{\pi}{l_{eff}}\right)^2} \quad (2.3)$$

$$l_{eff} = l - \frac{d^2}{0.95 \cdot b}, \quad w_{eff} = w - \frac{d^2}{0.95 \cdot b} \quad (2.4)$$

where  $f_{101}$  is the first resonant mode of the cavity,  $w$  and  $l$  are the width and length of a single SIW cavity,  $d$  is the diameter of the vias, and  $b$  is the via spacing (depicted in Fig. 3). The expressions are only valid when equations 2.1 and 2.2 are upheld, enabling the via posts to function as conventional rectangular waveguide side walls. Additionally, the outer coupling windows  $a_i$  in Fig. 1 relates to the external quality factor ( $Q_{ext}$ ) where adjusting the dimensions of this outer coupling window effects the resonator's  $Q_{ext}$ . This topology provides the flexibility of having both planar microstrip structures integrated with waveguide structures all on one substrate material.

#### B. Fixed Filter Implementation

To accomplish bandpass SIW filter design, once a single SIW cavity resonator is created for a specific resonant mode, the design methodology closely resembles conventional simulation-based microstrip filter design [48] – [49]. Coupling coefficients and external quality factors are calculated from derived expressions based on lowpass prototype parameters [49]. These values are then compared to the simulated extracted coupling coefficients and external quality factors for a particular cavity geometry. Iterations and adjustments to the dimensions of the coupling areas of the filter are performed until the calculated values match the extracted values from full-wave simulation, providing the desired filter. Utilizing this method, the following requirements in Table I provide the SIW bandpass filter implemented for subsequent analysis.

Table I. SIW Bandpass Filter Characteristics

2.1 GHz Center Frequency	Two-pole, Chebyshev
1.0% Fractional Bandwidth (FBW)	0.1 dB Passband Ripple

The substrate material chosen is a Rogers RT/Duroid 6010LM with dielectric constant ( $\epsilon_r$ ) of 10.2, loss tangent ( $\tan \delta$ ) of 0.0023, thickness of 2.54 mm, and 2 oz rolled copper foil. Given the desired resonant frequency of 2.1 GHz and considering equations 2.1 and 2.2, via post diameter ( $d$ ) is chosen to be 0.6 mm with via spacing ( $b$ ) of 2.1 mm. Utilizing equations 2.3 and 2.4, the approximate length ( $l$ ) and width ( $w$ ) for a single SIW square cavity is calculated as following:

$$f_{101} = 2.1 \text{ GHz} = \frac{c}{2\pi\sqrt{10.2}} \sqrt{\left(\frac{\pi}{w_{\text{eff}}}\right)^2 + \left(\frac{\pi}{l_{\text{eff}}}\right)^2} \quad (2.5)$$

$$l_{\text{eff}} = w_{\text{eff}} = 31.5 \text{ mm (square cavity)} \quad (2.6)$$

$$l_{\text{eff}} = 31.5 \text{ mm} = l - \frac{(0.6 \text{ mm})^2}{0.95 \cdot (2.1 \text{ mm})} \quad (2.7)$$

$$l = w = 31.2 \text{ mm} \quad (2.8)$$

Conforming to the design rules of equations 2.1 and 2.2 results in similar values of  $l_{\text{eff}}$  and  $w_{\text{eff}}$  compared to  $l$  and  $w$ , respectively. These single SIW cavity resonator dimensions are the basis for the two-pole fixed filter design. Two single cavity resonators are coupled together through apertures along the RF input and output microstrip-to-SIW transition areas and an aperture located in-between two SIW cavities.

These apertures provide the inductive loading needed to couple the resonators in the same way as a planar microstrip multi-resonator filter. Adjusting the dimensions of these coupling window openings in the SIW cavities provides the tuning needed to match coupling coefficients and external quality factors extracted from full-wave simulation to the calculated parameters. Fig. 4 depicts a two-pole SIW bandpass filter topology with  $a_1$  representing the outer coupling windows and  $a_2$  representing the inter-stage coupling window.

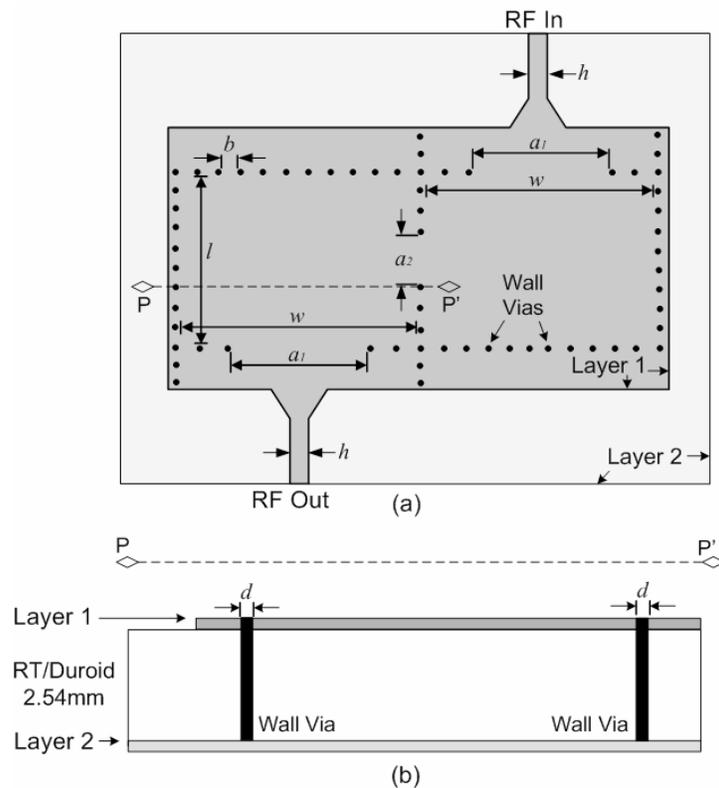


Fig. 4. SIW two-pole bandpass filter, (a) top view and (b) side view.

To find the appropriate dimensions for  $a_1$  and  $a_2$ , the coupling coefficient ( $M_{1,2}$ ) and external quality factors ( $Q_{e1}$ ,  $Q_{e2}$ ) are first calculated [50]:

$$M_{1,2} = \frac{FBW}{\sqrt{g_1 g_2}} \quad , \quad Q_{e1} = \frac{g_0 g_1}{FBW} \quad , \quad Q_{e2} = \frac{g_2 g_3}{FBW} \quad (2.9)$$

where  $g_0, g_1, g_2,$  and  $g_3$  are the lowpass filter prototype parameters and  $FBW$  is the filter fractional bandwidth. Given the filter requirements from Table I, lowpass prototype parameters are found from the methodology presented in [49]. The coupling coefficient ( $M_{1,2}$ ) and external quality factors ( $Q_{e1}, Q_{e2}$ ) are then calculated as following:

$$M_{1,2} = \frac{FBW}{\sqrt{g_1 g_2}} = \frac{0.01}{\sqrt{0.8431 \cdot 0.6220}} = 0.0175 \quad (2.10)$$

$$Q_{e1} = \frac{g_0 g_1}{FBW} = \frac{1 \cdot 0.8431}{0.01} = 84.3 \quad (2.11)$$

$$Q_{e2} = \frac{g_2 g_3}{FBW} = \frac{0.622 \cdot 1.3554}{0.01} = 84.3 \quad (2.12)$$

These calculated values are next compared to their corresponding values extracted from full-wave simulation. To extract the external quality factor, the previously designed single SIW cavity resonator from Fig. 3 with dimensions from equations 2.5-2.8 is simulated using Sonnet software [51]. The extracted external quality factor  $Q_{ext}$  is defined as [25]:

$$Q_{ext} = \frac{f_o}{\Delta f_{-3dB}} \quad (2.13)$$

where  $f_o$  is the center resonant frequency and  $\Delta f_{-3dB}$  is the 3 dB bandwidth. Varying the outer coupling window spacing ( $a_1$ ) provides different  $Q_{ext}$  values. Fig. 5 depicts  $S_{21}$

parameters for  $a_1 = 12$  mm providing a resonant frequency of 2.11 GHz and 3 dB bandwidth of 50 MHz.

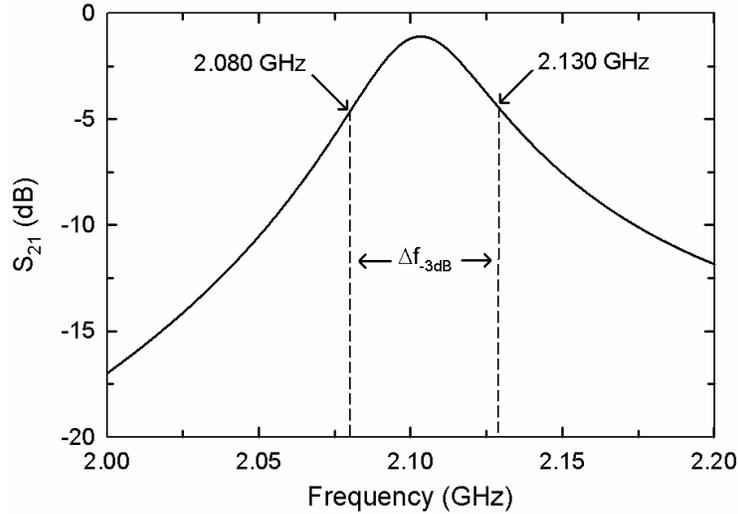


Fig. 5. Simulated  $S_{21}$  parameters for single cavity resonator of  $a_1 = 12$  mm.

External quality factor for this condition is extracted using equation 2.13:

$$Q_{ext} = \frac{f_o}{\Delta f_{-3dB}} = \frac{2.11 \text{ GHz}}{(2.130 - 2.080) \text{ GHz}} = 84.4 \quad (2.14)$$

For output coupling window spacing of 12 mm, the extracted external quality factor ( $Q_{ext} = 84.4$ ) closely matches the calculated external quality factors ( $Q_{e1} = Q_{e2} = 84.3$ ). This is achieved through multiple iterations of various outer coupling window dimensions ( $a_1$ ), extracting the associated external quality factor ( $Q_{ext}$ ), and generating the following design fitting curve (Fig. 6).

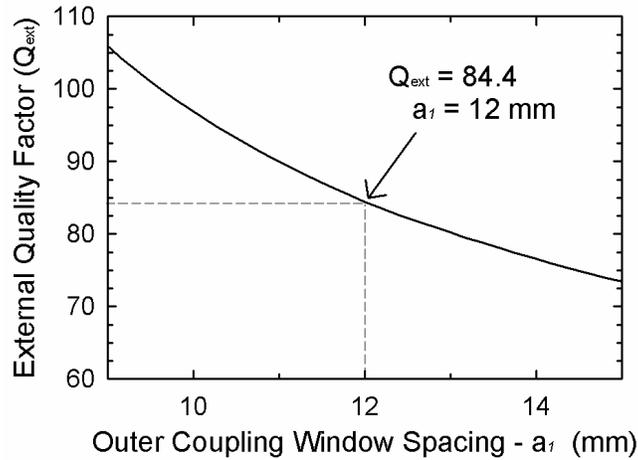


Fig. 6. Extracted  $Q_{ext}$  with respect to  $a_1$  depicting the desired outer coupling window spacing of 12 mm.

To obtain the desired inter-stage coupling window spacing ( $a_2$ ), the extracted coupling coefficient ( $k$ ) is next matched to the calculated coupling coefficient ( $M_{1,2}$ ). This task is done through weakly coupling two previously designed SIW cavity resonators ( $a_1$  fixed at 12 mm) with a shared aperture  $a_2$  [50]. Fig. 7 depicts the SIW structure utilized to extract the coupling coefficient.

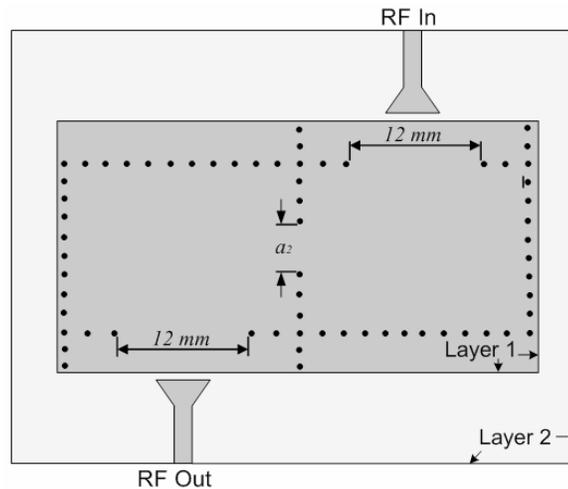


Fig. 7. Two SIW cavity resonators weakly coupled (microstrip-to-SIW transition region disconnected from the SIW cavities) with shared aperture  $a_2$ .

The extracted coupling coefficient ( $k$ ) is defined [25]:

$$k = \frac{f_{p2}^2 - f_{p1}^2}{f_{p2}^2 + f_{p1}^2} \quad (2.15)$$

where  $f_{p2}$  and  $f_{p1}$  are the resonant characteristic frequencies simulated from the structure depicted in Fig. 7. Fig. 8 shows the  $S_{21}$  parameters for the weakly coupled SIW structure with  $a_2 = 6.6$  mm,  $f_{p2} = 2.116$  GHz, and  $f_{p1} = 2.080$  GHz.

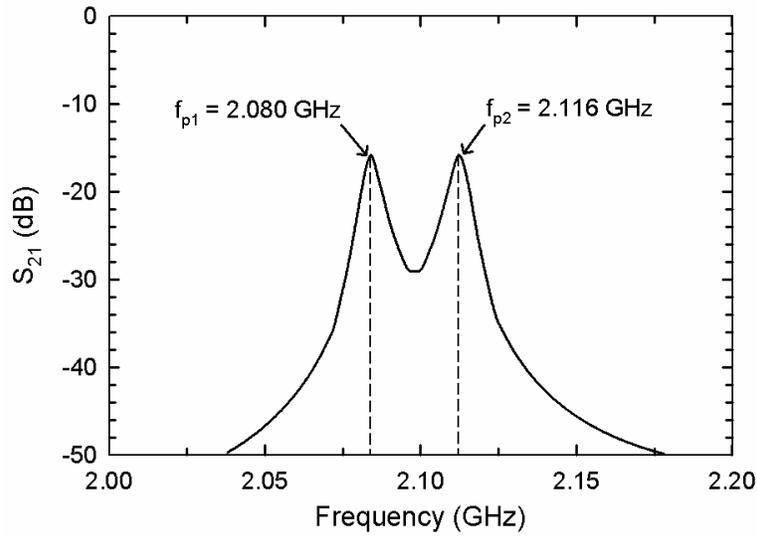


Fig. 8. Simulated  $S_{21}$  parameters for weakly coupled SIW structure with  $a_2 = 6.6$  mm.

The coupling coefficient ( $k$ ) for this condition is extracted from equation 2.15:

$$k = \frac{f_{p2}^2 - f_{p1}^2}{f_{p2}^2 + f_{p1}^2} = \frac{2.116^2 - 2.080^2}{2.116^2 + 2.080^2} = 0.0172 \quad (2.16)$$

For inter-stage window spacing of 6.6 mm, the extracted coupling coefficient ( $k = 0.0172$ ) closely matches the calculated coupling coefficient ( $M_{1,2} = 0.0175$ ). This is achieved through multiple iterations of various inter-stage coupling window dimensions ( $a_2$ ), extracting the associated coupling coefficient ( $k$ ), and generating the following design fitting curve (Fig. 9).

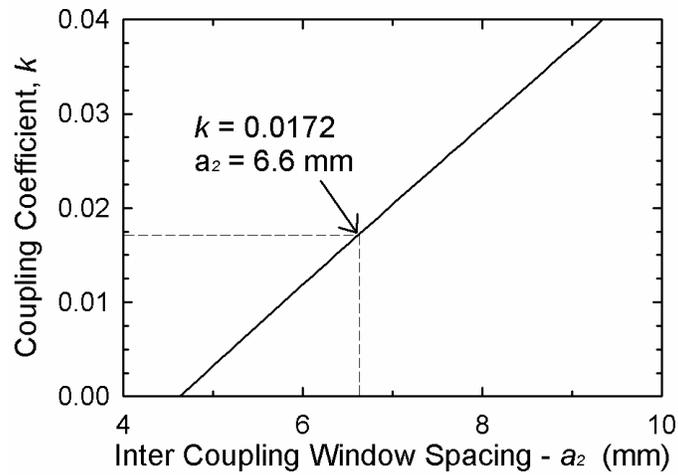


Fig. 9. Extracted  $M_{1,2}$  with respect to  $a_2$ .

Considering  $a_1 = 12$  mm and  $a_2 = 6.6$  mm the required quality factor and coupling coefficient for the filter is achieved, and the desired fixed filter described in Fig. 4 is realized with the response shown in Fig. 10 using Sonnet full-wave simulation.

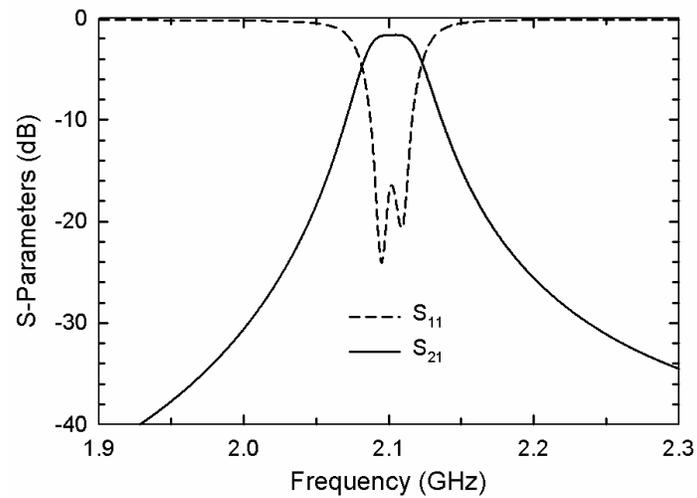


Fig. 10. Two-pole SIW bandpass fixed filter simulated response.

An insertion loss investigation is next performed to the newly designed SIW bandpass filter simulating various via spacing emulating the SIW cavity wall. Fig. 11 depicts insertion loss for different via spacing values ( $b$ ) of 0.0 mm, 2.1 mm, 4.2 mm, 5.1 mm, and 6.6 mm.

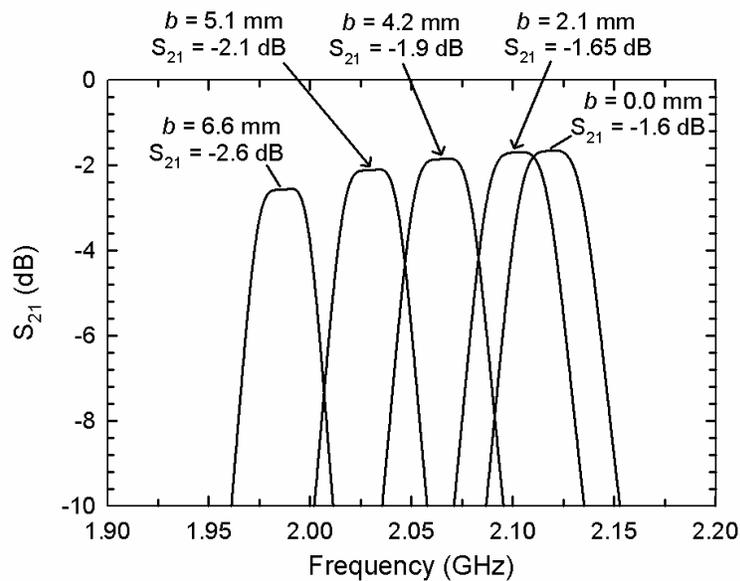


Fig. 11. Simulated insertion loss for different via spacing values ( $b$ ) of 0.0 mm, 2.1 mm, 4.2 mm, 5.1 mm, and 6.6 mm.

Fig. 11 validates the design rules given in equations 2.1 and 2.2 with no significant insertion loss difference between via spacing values of  $b = 0.0$  mm and  $b = 2.1$  mm. For increasing values of  $b$ , up to a 1 dB decrease to insertion loss performance is observed for  $b = 6.6$  mm. Additionally, increasing the via spacing also increases the effective length and width of the cavity, thereby shifting the resonant frequency down by nearly 7% for  $b = 6.6$  mm. This also proves resonant frequency design equations 2.3 and 2.4 are invalid for via spacing values greater than four times the diameter of the vias described in equation 2.2. Therefore, when conforming to the given design rules, insertion loss for SIW fixed filters is primarily attributed to standard parameters (e.g. substrate material, metal material, fractional bandwidth).

### C. Empirical Analysis of Tuning Mechanism

The proposed tuning mechanism involves perturbing via posts located inside the SIW cavities. Tuning is achieved through connecting/disconnecting the top of the perturbing via posts to/from the top metal layer of the SIW cavities. Via islands on top of the via posts serve as the contact areas to/from the top metal layer. The perturbing via posts with via islands are located at the same location with respect to each cavity's outer coupling window. Fig. 12 illustrates the same previously designed fixed filter with the added via post perturbations. Table II depicts the corresponding physical dimensions. Via island dimensions  $m = 1.5$  mm and  $n = 0.3$  mm are chosen based on the dimensions of the packaged RF switches presented in the next section and standard PCB fabrication tolerances for through-hole vias.

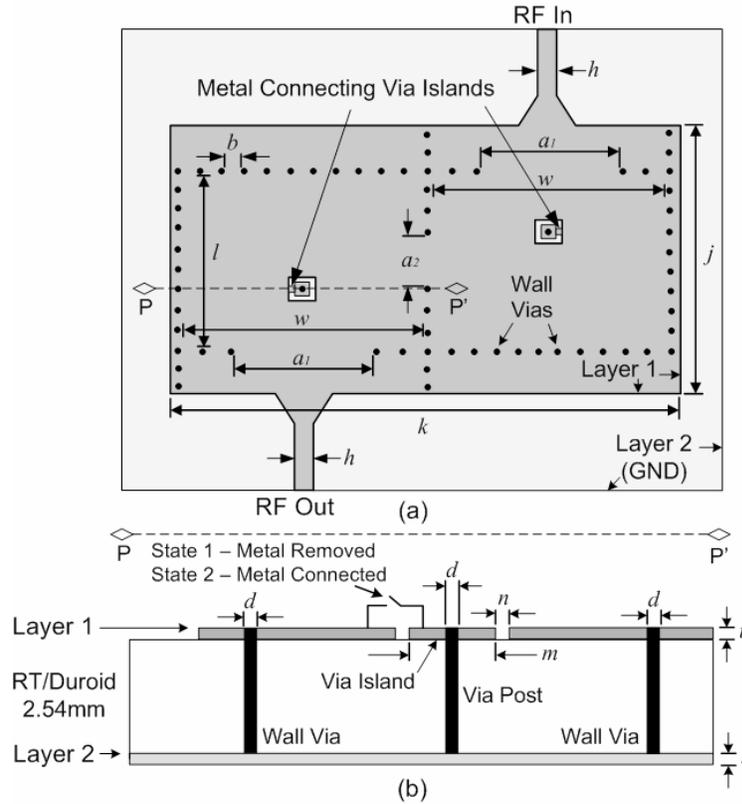


Fig. 12. SIW filter with single perturbing via post and island per cavity, (a) top view and (b) side view.

Table II. SIW Perturbing Filter Physical Dimensions

$d$	0.6 mm	$h$	2.4 mm	$w$	31.2 mm
$b$	2.1 mm	$j$	34.5 mm	$m$	1.5 mm
$a_1$	12.0 mm	$k$	64.2 mm	$n$	0.3 mm
$a_2$	6.6 mm	$l$	31.2 mm	$t$	35 $\mu$ m

If the via island is not connected to the top metal layer (state 1 in Fig. 12(b)), the filter response shows a small variation compared to the unperturbed filter in Fig. 13.

Conversely, when a single metal strip connects the via island to the top metal layer (state 2 in Fig. 12(b)), the filter response shifts to 2.45 GHz. This demonstrates merely isolating the via island is similar to having no perturbing vias present in the cavities, and shorting the via island to the top of the SIW cavity provides considerable tuning to the filter.

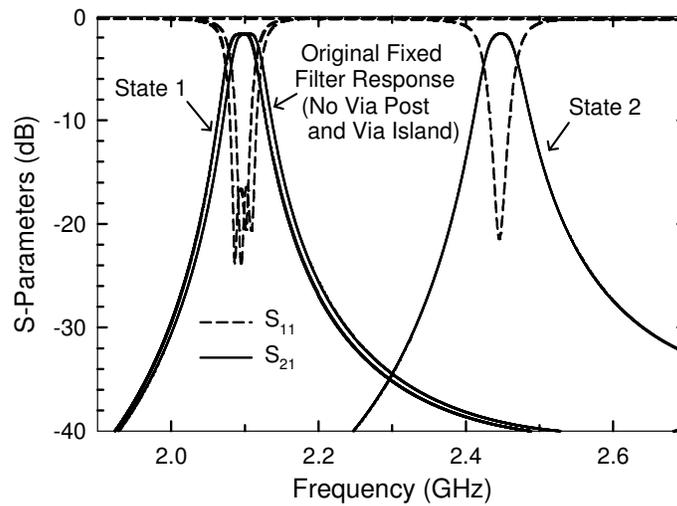


Fig. 13. Original fixed filter SIW response compared to the filter response with perturbing vias (state 1 and state 2).

Fig. 14 depicts the top view and current distribution for each case described in Fig. 13. Despite the physical difference between the original fixed filter and the perturbing filter, current distribution is relatively unaffected when compared to the “state 1” filter (via island disconnected from the top metal cavity). When the via island is connected to the top metal layer, the perturbing via post resonates at 2.45 GHz shifting the maximum current density to the middle of the cavity.

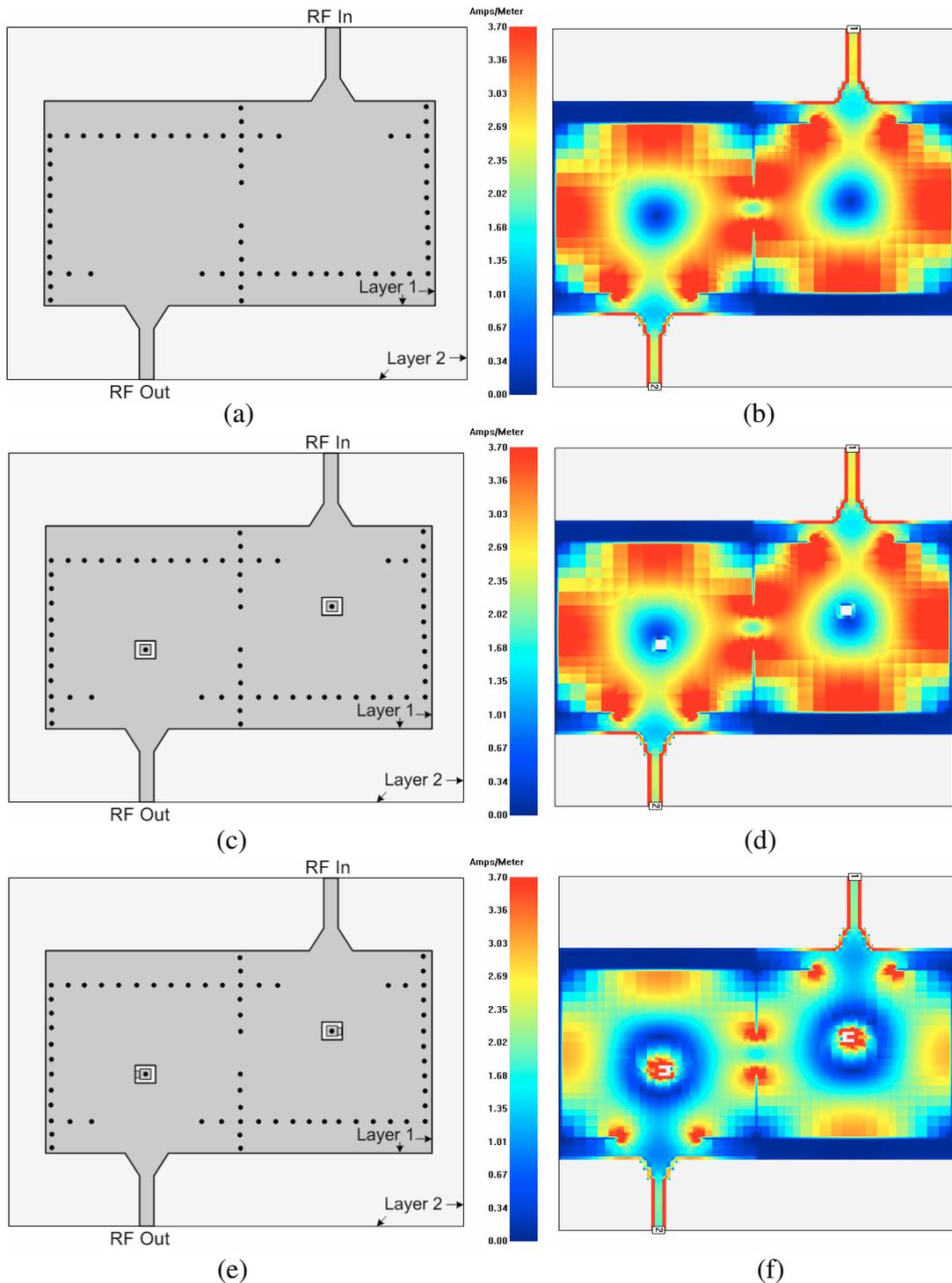


Fig. 14. Comparison of (a) original fixed filter top view, (b) original fixed filter current distribution, (c) perturbing vias state 1 top view, (d) perturbing vias state 1 current distribution, (e) perturbing vias state 2 top view, and (f) perturbing vias state 2 current distribution.

The following methodology shows how a single perturbing via post is optimally located inside an SIW cavity, creating the second state of Fig. 13. First, via posts with their corresponding islands are connected to the top of the SIW cavity and located in the middle of the input/output coupling windows (point A in Fig. 15(a)). The perturbing vias are then swept from point A to point B towards the center of the cavities. Fig. 15(b) illustrates the simulated return loss while the via moves from point A to point B. An optimal location  $L$  is observed within the line AB at 2.45 GHz, providing the highest tuning range and best matching simultaneously. Performance below and above this location reveals less tuning and poor return loss.

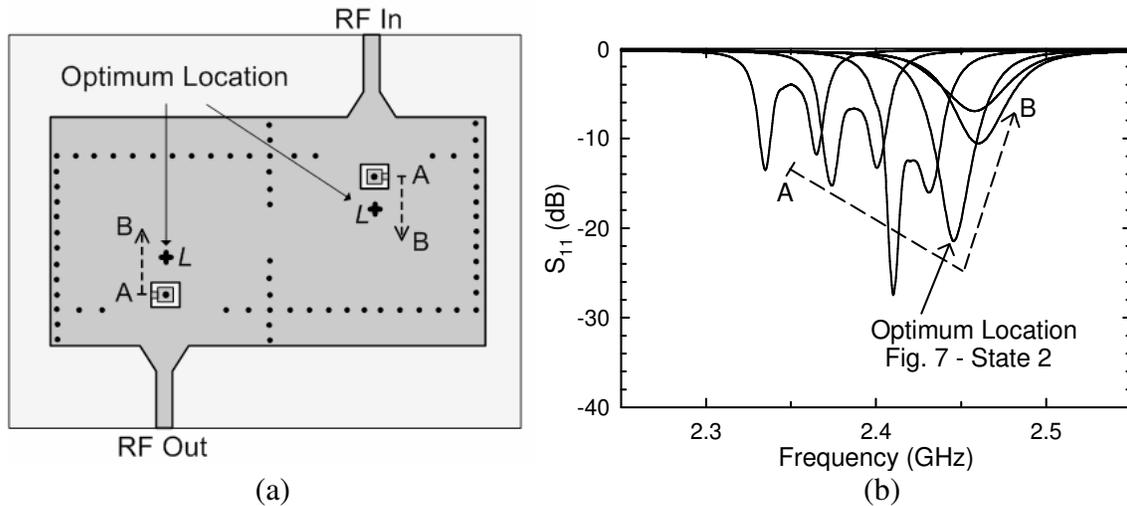


Fig. 15. Via post/island sweep towards SIW cavity center, (a) AB sweep top view and (b) AB sweep response.

The next step utilizes the optimal position along the AB line but sweeps this location along the horizontal axis from point C to point D depicted in Fig. 16. Simulated

return loss of the CD line in Fig. 17 illustrates the same principle of increased tuning towards the center of the cavities. However, locations closer to the edge of the cavity via walls (point C) reveal lower frequency tuning states with acceptable matching. Consequently, the CD tuning line must be employed to obtain fine tuning closer to the original fixed filter response. The intersection of the AB and CD tuning lines reveals the optimum location ( $L$ ) providing the highest tuning state with best return loss, represented as state 2 in Fig. 13.

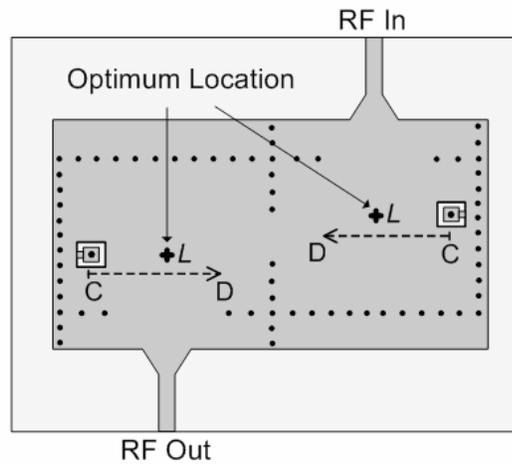


Fig. 16. Via post/island CD sweep towards SIW cavity center.

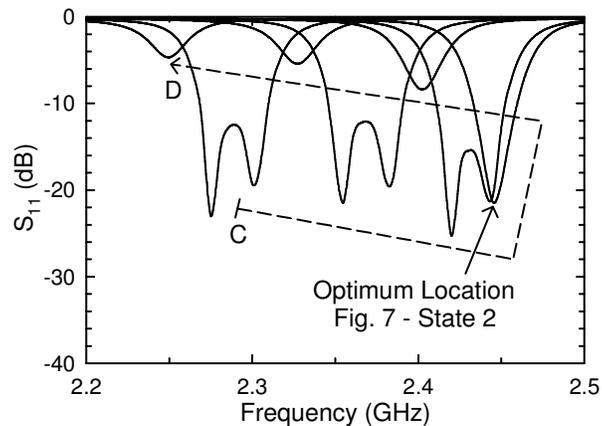


Fig. 17. Via post/island CD sweep response.

Frequency tuning from the original fixed filter response 2.1 GHz up to 2.45 GHz can be obtained through the CD tuning line, providing a 15% tuning capability. To obtain states beyond 2.45 GHz, via posts/islands are placed vertically along the AB tuning line surrounding optimum location  $L$  as depicted in Fig. 18(a), (c), (e). Multiple states are achieved through different combinations of connected via islands (i.e. on-state via posts), provided the perturbing vias are symmetrically activated around position  $L$ . This preserves good matching for all tuning states while keeping the optimum location at the center of various on-state via posts. Using this method, higher number of on-state via posts correlates to higher frequency tuning states where “0” designates an off-state via post and “1” designates an on-state via post. Fig. 18(a-f) depicts top views of three separate cases each representing a different resonant frequency along with the corresponding current distribution. A direct correlation is observed between larger areas of high current density along the AB tuning line and higher frequencies states. Fig 19 depicts the simulated frequency response for each case.

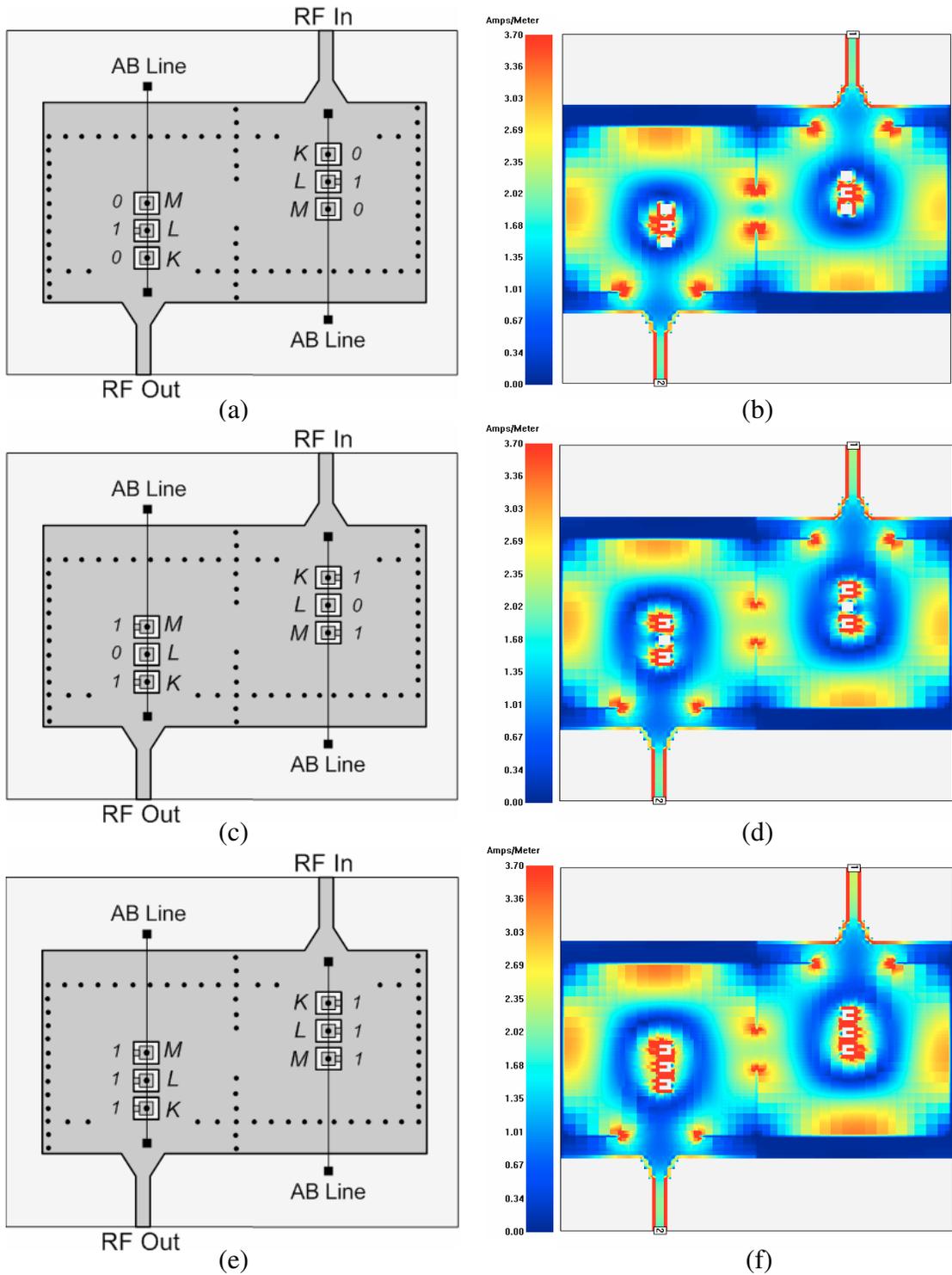


Fig. 18. Higher frequency states utilizing AB tuning line with on/off (“1” / “0”) via post configurations  $KLM$  of (a) 010 top view, (b) 010 current distribution, (c) 101 top view, (d) 101 current distribution, (e) 111 top view, and (f) 111 current distribution .

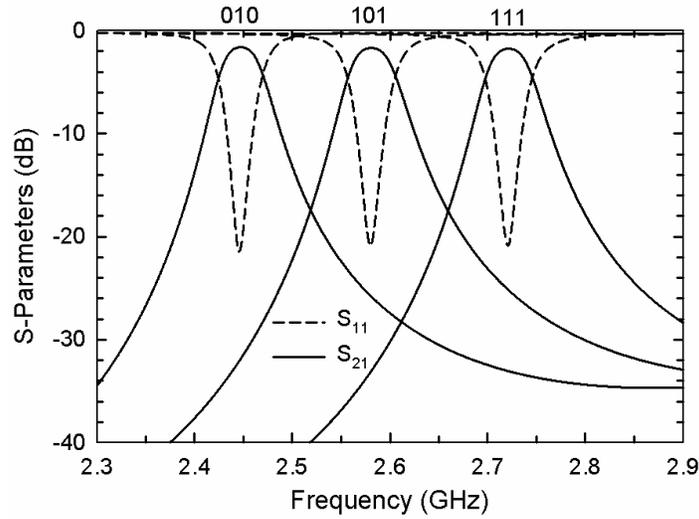


Fig. 19. Simulated response for frequency states along the AB tuning line with  $KLM$  values of 010, 101, and 111 (from Fig. 18(a-f)).

The simulated response shown in Fig. 19 illustrates frequency states beyond 2.45 GHz when utilizing the AB tuning line. Via posts are symmetrically activated around the central tuning location  $L$ , where each additional on-state via post creates equally spaced frequency states. In this instance, three via posts contribute to an extra 11% tuning capability (2.45 GHz – 2.72 GHz). With respect to the original fixed filter frequency state ( $KLM = 000$ , 2.1 GHz), overall tuning capability for this configuration is 26% (2.1 GHz – 2.72 GHz). In order to expand the tuning capability even further, more perturbing via posts are needed. The next section validates this ideal tuning mechanism through fabrication and measurement while investigating the limits of tuning capability along the AB tuning line.

#### D. Verification of SIW Filter Tuning Mechanism

Three filters representing three separate states are fabricated to perform frequency tuning along the vertical AB line. Rogers RT/Duroid 6010 laminate substrate ( $\epsilon_r = 10.2$ , thickness = 2.54 mm,  $\tan \delta = 0.0023$ ) is utilized on a standard PCB manufacturing process. This particular filter is designed for fractional bandwidth of 2% and resonant frequency of 1.9 GHz. Two more perturbing via posts are added to each SIW cavity to expand the tuning capability. Fig. 20 illustrates one fabricated filter representing the first ideal state where no via islands are connected to the top cavity metal layer. Via posts/islands are labeled as *J*, *K*, *L*, *M*, and *N* per cavity where *L* is the same optimal location described from the previous section. The remaining two ideal states are achieved by fabricating two filters exactly the same as the one in Fig. 20 with different combinations of on-state via posts.

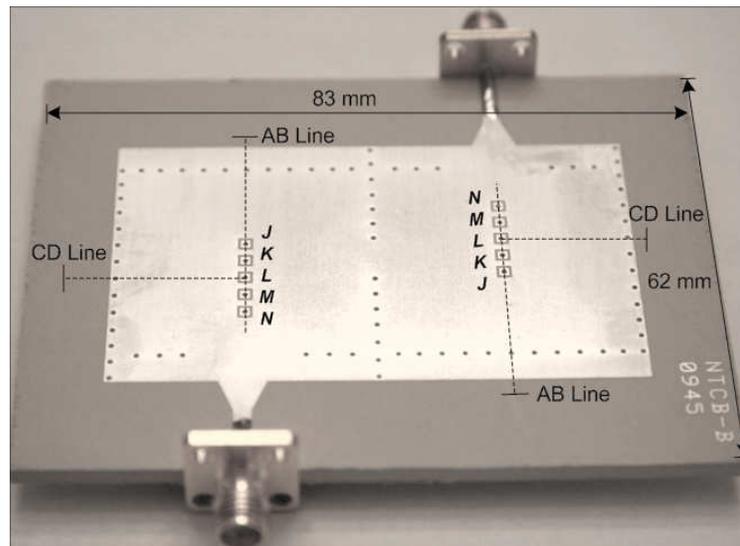


Fig. 20. Fabricated SIW filter with five via posts/islands per cavity – all via islands disconnected from cavity's top metal layer (first state).

Fig. 21 shows the simulated and measured s-parameters for all three filters.

Table III presents a summary of each state's measured performance parameters.

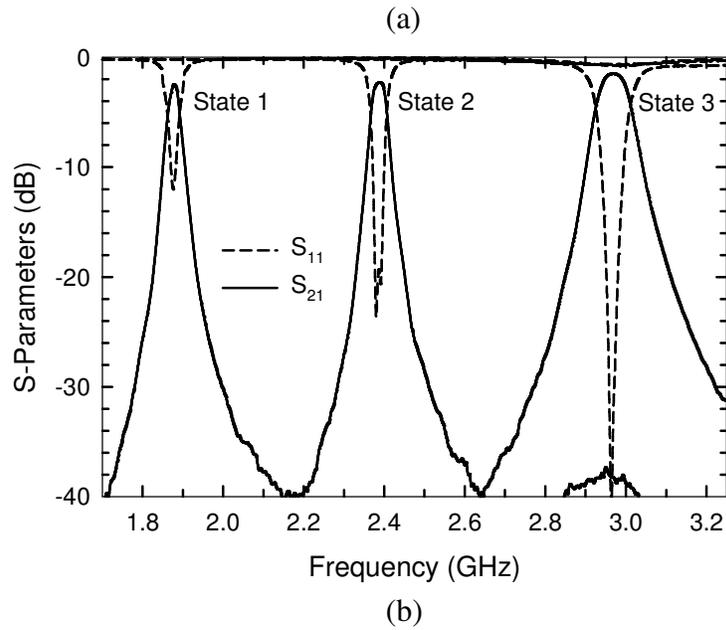
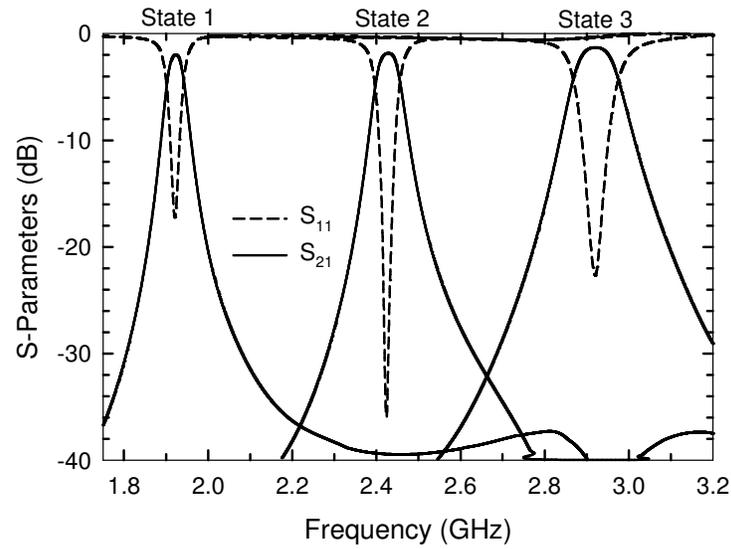


Fig. 21. S-paramaters for three fabricated SIW filters each tuned at different frequencies, (a) simulation and (b) measurement.

Table III. Ideal Tuning SIW Filter Performance Parameters

State	<b>0 – Via Island Disconnected (Off -State Via Post) 1 – Via Island Connected (On-State Via Post)</b>				
	<i>JKLMN</i>	<b>f<sub>o</sub></b>	<b>S<sub>21</sub></b>	<b>FBW</b>	<b>Q<sub>U</sub></b>
1	0 0 0 0 0	1.9 GHz	-2.5 dB	1.8%	221
2	0 1 0 1 0	2.4 GHz	-2.3 dB	1.7%	255
3	1 1 1 1 1	3.0 GHz	-1.5 dB	2.9%	223

Filter loaded and unloaded quality factors  $Q_L$  and  $Q_U$  are calculated from [44].

$$Q_L = \frac{f_o}{\Delta f_{-3dB}} \quad (2.15)$$

$$Q_U = \frac{Q_L}{1 - S_{21}(f_o)} \quad (2.16)$$

The parameter  $f_o$  is the center frequency for each state, and  $\Delta f_{-3dB}$  is the 3 dB bandwidth for each state. Unloaded quality factor for this filter configuration is twice compared to the highest quality planar microstrip filters [49]. Tuning achieved from this method is from 1.9 GHz to 3.0 GHz (45% tuning) with return loss better than 12 dB over the entire tuning range. A direct correlation is observed between higher frequency states and the higher number of on-state via posts. Other examples of acceptable states (not fabricated) are  $JKLMN = 00100$  ( $f_o = 2.2$  GHz),  $01110$  ( $f_o = 2.6$  GHz), and  $11011$  ( $f_o = 2.8$  GHz).

Simulated resonant frequencies for each state closely match measurements. The insertion loss discrepancy between simulation and measurement is 0.8 dB due to the manufacturing loss tangent tolerances of the material. Despite return loss discrepancies caused by fabrication tolerances from the PCB company, measurements still provide better than 12 dB matching. Additionally, five perturbing via posts per cavity have increased the fractional bandwidth from 1.8% in the lowest frequency state to 2.9% in the highest frequency state. This 62% increase to the fractional bandwidth is not as prevalent with the original three perturbing via posts per SIW cavity primarily due to the outer and inter-stage coupling windows designed for the lowest frequency state. Since the coupling windows are originally designed for the first state, significantly altering the original structure of the SIW filter (e.g. higher frequency tuning states) also alters the filter response parameters. In this case, the primary effect to higher tuning relates to an increase to fractional bandwidth. If a significant increase to the fractional bandwidth is not desirable, tuning capability for this topology is limited to 30%. However, if there are no design restrictions to the increase of fractional bandwidth, tuning capability for this topology is proven to be at least 45% (depicted in Fig. 21). In the next chapter, both AB lines (higher frequency coarse tuning) and CD lines (lower frequency fine tuning) are utilized for a fully tunable SIW filter employing two types of packaged RF tuning elements: PIN diodes and RF MEMS switches.

## CHAPTER III

TUNABLE FILTER IMPLEMENTATION WITH  
PIN DIODES AND RF MEMS SWITCHESA. PIN Diode – Philips BAP55L1. Modeling and Design

The PIN diode is a semiconductor device which functions as a variable resistor at microwave frequencies [52]. The resistance value depends on the biasing of the diode. Forward biasing provides lower resistance values while reverse biasing provides high resistance, producing the needed RF switch operation. A simple PN junction provides this same basic function, however in order to provide higher quality isolation and reduce signal distortion, an intrinsic layer is sandwiched between the p-type and n-type regions [53]. To fabricate such a device, an intrinsically pure silicon wafer is diffused with p-type material on one side and n-type material on the other side. The resulting intrinsic region in-between the two diffused regions is thus a function of the original wafer's thickness. A wafer with higher thickness directly correlates to a higher thickness intrinsic region ( $W$ ). Fig. 22 depicts a typical PIN diode structure.

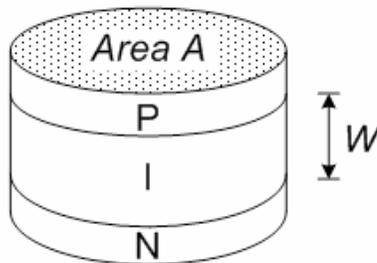


Fig. 22. PIN diode fundamental structure.

Trade-offs associated with the thickness ( $W$ ) of the intrinsic region and the area ( $A$ ) of the PIN diode junctions are distortion, isolation (off-state performance), and series resistance (on-state performance). Thicker intrinsic regions and smaller areas of the PIN diode junctions correlate to higher isolation and lower distortion but with a trade-off correlating to higher on-state series resistance. Fig. 23 illustrates the circuit model of a packaged PIN diode in the reverse bias configuration [54].

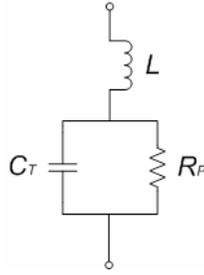


Fig. 23. Packaged PIN diode in reverse bias condition.

The parameter  $L$  is the series inductance due to packaging,  $R_P$  is the PIN diode parallel resistance, and  $C_T$  is the total capacitance expressed as the following [54]:

$$C_T = \frac{\epsilon A}{W} \quad (2.17)$$

where  $\epsilon$  is the silicon dielectric constant, and the values  $A$  and  $W$  are depicted in Fig. 22. When the PIN diode is at zero or reverse bias there is no stored charge in the intrinsic region, resulting in the diode performing as a parallel plate capacitor ( $C_T$ ) shunted by a parallel resistance ( $R_P$ ). As a result, lower values of capacitance due to increased  $W$  correlate to higher reactance and overall impedance, resulting in higher isolation and

lower distortion (increased off-state performance). Fig. 24 depicts a packaged PIN diode in the forward biased condition.



Fig. 24. Packaged PIN diode in forward bias condition.

The parameter  $L$  is the series inductance due to packaging, and  $R_s$  is the series resistance predominately affected by the width of the intrinsic region. The expression for  $R_s$  is as following [54].

$$R_s = \frac{W^2}{(\mu_N + \mu_P) Q} \quad (2.18)$$

where  $W$  is the intrinsic width depicted in Fig. 22,  $\mu_N$  and  $\mu_P$  are the electron and hole mobility of the material respectively, and  $Q$  is the stored charge in the intrinsic region. When the PIN diode is forward biased, electrons and holes are injected into the intrinsic regions creating a conductive path thereby lowering the series resistance of the diode [53]. In this case, an increase to the thickness of the intrinsic region ( $W$ ) correlate to higher series resistance, thereby decreasing on-state performance. Therefore, an optimum intrinsic region thickness ( $W$ ) and PIN diode junction area ( $A$ ) must be derived from the requirements of a particular switching application.

For the tunable SIW filter switching application, both on and off state performance have equal emphasis in order to maximize the quality of each frequency state. The best overall performing PIN diode is chosen (Philips BAP55L) with the following parameters depicted in Table IV.

Table IV. Philips BAP55L PIN Diode Parameters

Forward Biased 10 mA	Reverse Biased -5 V
$R_s = 0.8 \Omega$	$C_T = 0.20 \text{ pF}$
	$R_P = 10 \text{ k}\Omega$
$L = 0.6 \text{ nH}$	$L = 0.6 \text{ nH}$

Inserting these parameters into the circuit models of Fig. 23-24 reveals the following s-parameters simulated on Agilent Advanced Design System [55] (Fig. 25(a-b)).

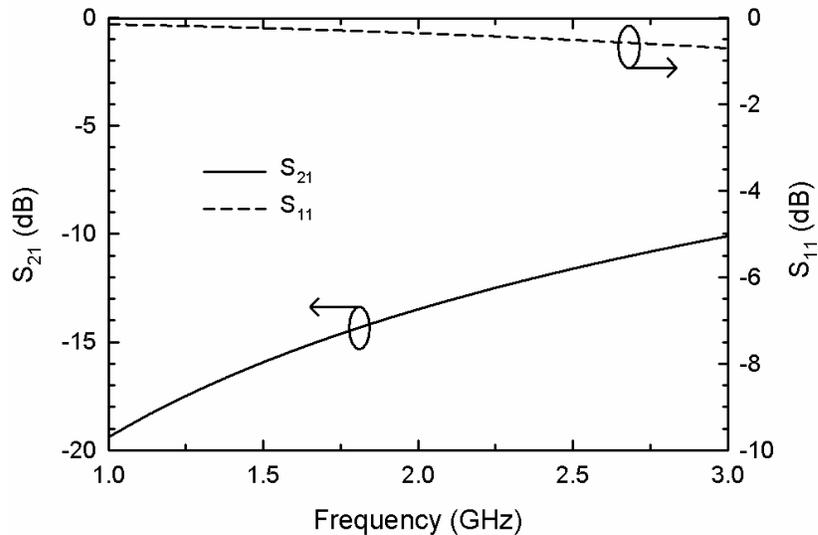


Fig. 25(a). S-parameters for Philips BAP55L PIN diode with reverse bias of -5 V.

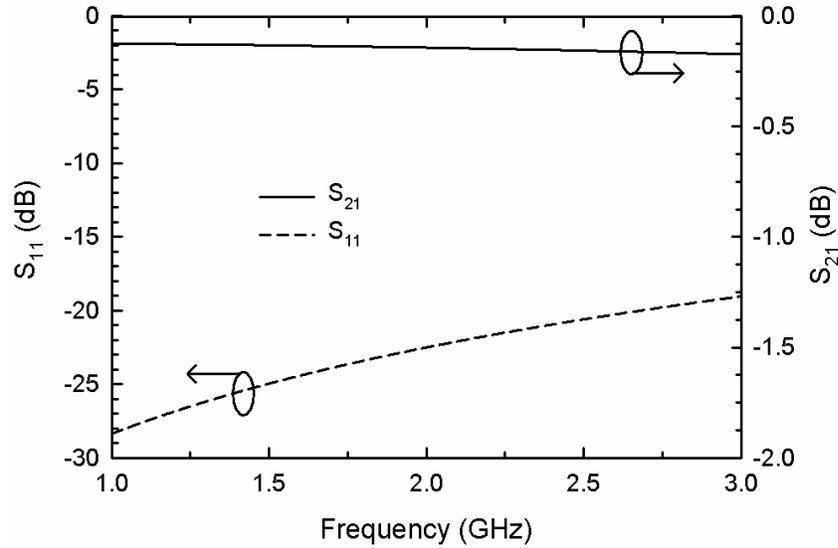


Fig. 25(b). S-parameters for Philips BAP55L PIN diode with forward bias of 10 mA.

The results of the simulated off-state and on-state parameters depicted in Fig. 25(a-b) provide the models utilized for the design of the tunable SIW filter. The parasitics depicted in this non-ideal switch model provide more insertion loss to the overall filter response. As a result, the unloaded quality factor of the filter decreases compared to the performance of the filters fabricated in the previous chapter. Additionally, the parasitics of the PIN diode also contribute to the limited tuning range. However, the resulted quality factor for the proposed SIW tunable filter is still higher compared to standard tunable planar microstrip filters [56] – [60] and is further discussed in the subsequent section.

Incorporating PIN diodes as switching elements involves a three-layer PCB implementation in order to separate the switching device biasing network from the SIW

filter. This provides better isolation and minimizes undesirable coupling between DC biasing components from the RF filter structure. The biasing network is laid out on a separate duroid substrate ( $\epsilon_r = 10.2 \pm 0.25$ , thickness = 0.635 mm) and bonded to the top of the SIW filter as depicted in Fig. 26.

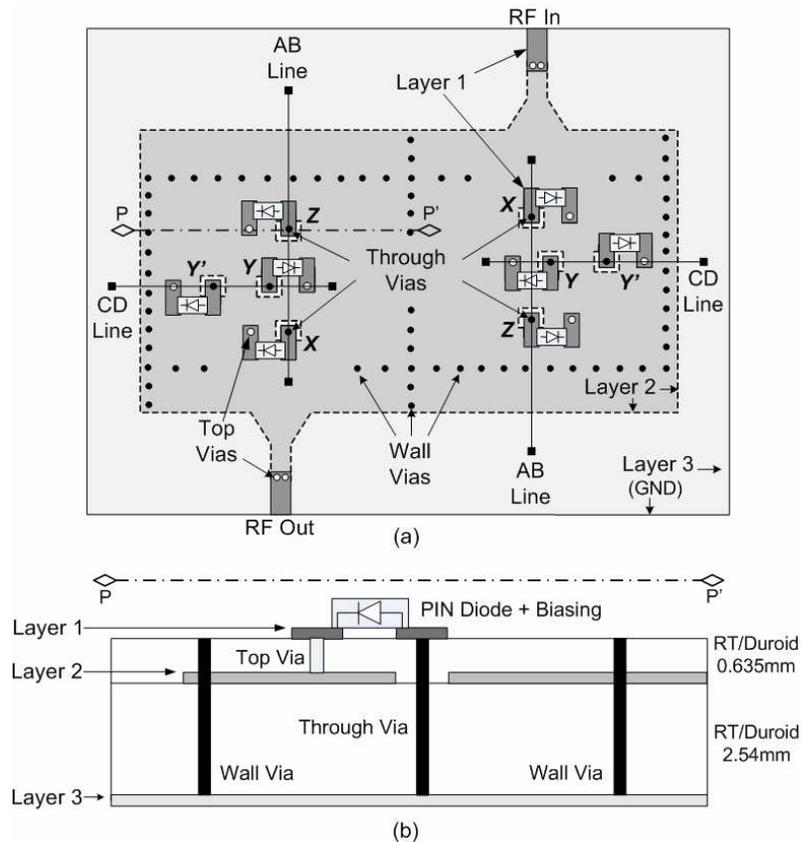


Fig. 26. Tunable SIW filter layout with PIN diodes: a three-layer design, (a) top view and (b) side view.

In this topology, metal strips connecting/disconnecting via posts/islands described in the previous chapter are replaced with PIN diodes. Top vias connect layers 1 and 2 and through vias connect layers 1 and 3. As a result, turning the PIN diode on

and off produces the same type of switching operation. Utilizing the AB/CD tuning line methodology obtained from the previous chapter, locations  $Y$  and  $Y'$  provide lower frequency tuning through positions along the CD line. Locations  $X$  and  $Z$  provide higher tuning states through positions along the AB line. Both AB and CD lines are employed to provide course and fine tuning for different frequency states. Fig. 27-32 depicts current distributions of the three layer design depicted in Fig. 26 where various combinations of  $X Y Y' Z$  represent different frequency states (“1” – on state, “0” – off state).

Investigating the filter current distribution from the lowest frequency state to the highest frequency state reveals a minor shift to the location of maximum current density. For example, the difference between  $X Y Y' Z = 0000$  and  $X Y Y' Z = 0010$  is observed along the horizontal CD tuning line. With all switches off (Fig. 27(a)), the lower frequency state displays higher current density at the very outer edge of the CD tuning line along the via cavity wall (Fig. 27(b)). The next frequency state of  $X Y Y' Z = 0010$  (Fig. 28(a)) displays a minor shift of higher current density away from the via walls towards the center of the CD tuning line (Fig. 28(b)), resulting in a resonant frequency slightly higher than the previous state. Utilizing the tuning methodology described in the previous chapter, these minor shifts to the current distribution are consequently applied to both the CD and AB tuning lines. The result is the desired overall symmetrical tuning response (Fig. 35) ranging from the lowest frequency state (Fig. 27) to the highest frequency state (Fig. 32).

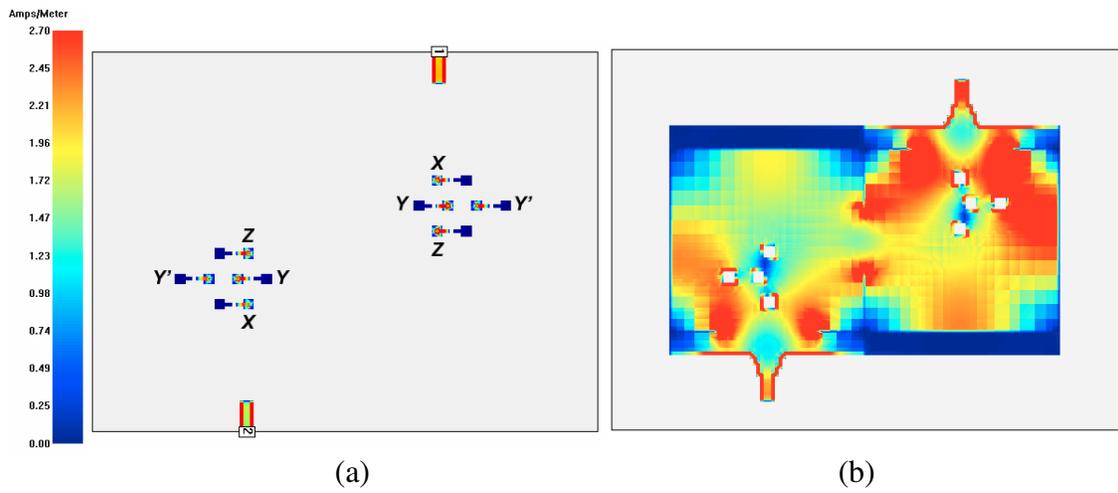


Fig. 27. Current distribution for three-layer PCB tunable SIW filter from Fig. 26 with  $XY'YZ = 0000$ , (a) layer one and (b) layer two.

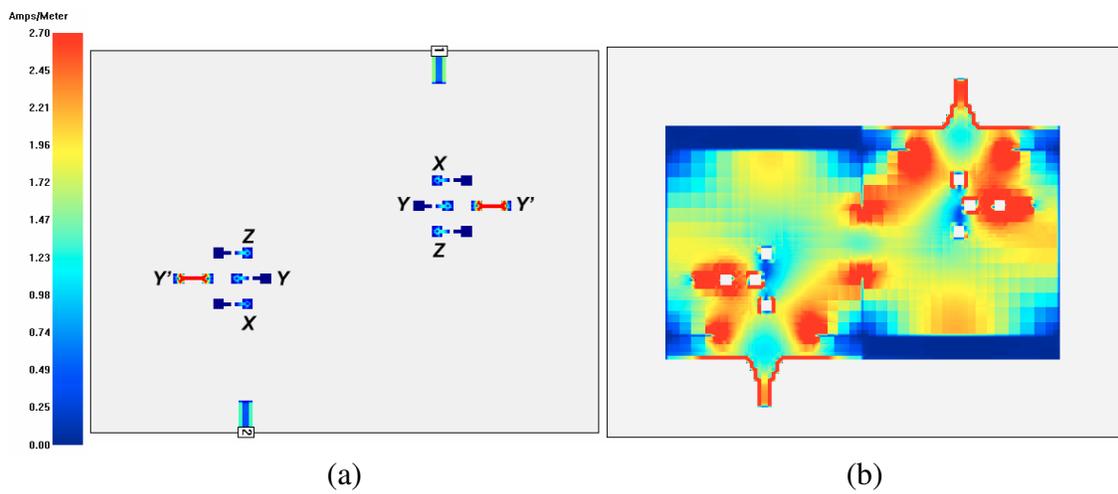


Fig. 28. Current distribution for three-layer PCB tunable SIW filter from Fig. 26 with  $XY'YZ = 0010$ , (a) layer one and (b) layer two.

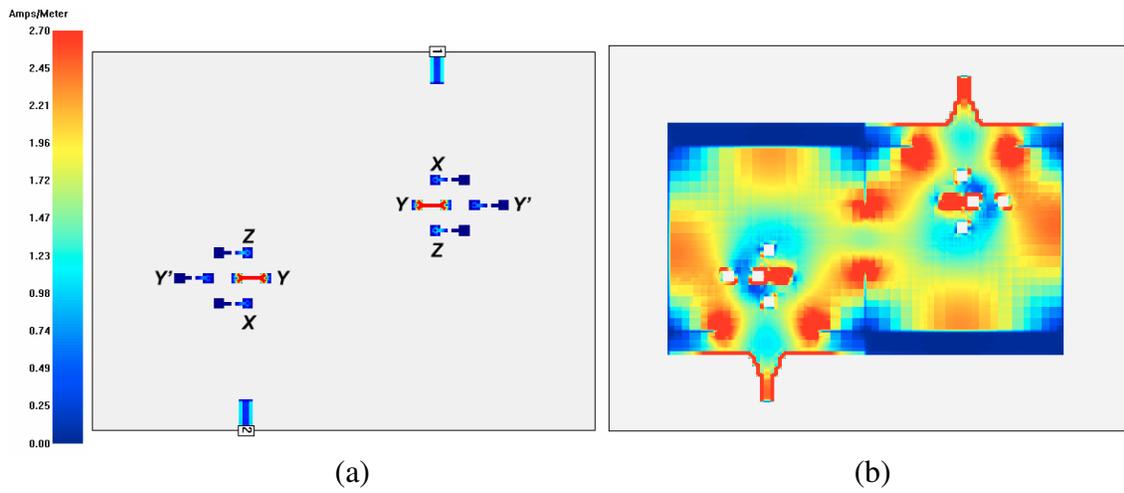


Fig. 29. Current distribution for three-layer PCB tunable SIW filter from Fig. 26 with  $XY'Y'Z = 0100$ , (a) layer one and (b) layer two.

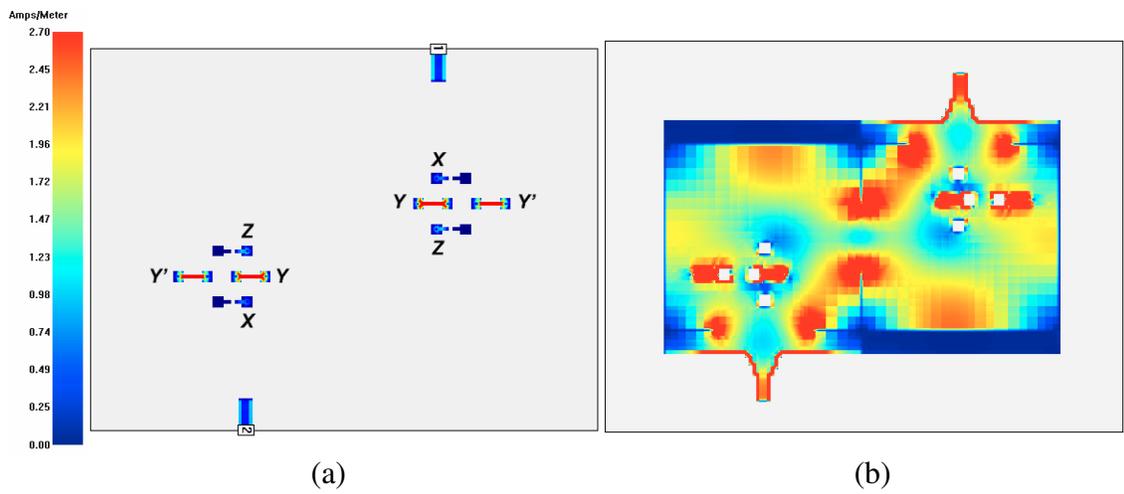


Fig. 30. Current distribution for three-layer PCB tunable SIW filter from Fig. 26 with  $XY'Y'Z = 0110$ , (a) layer one and (b) layer two.

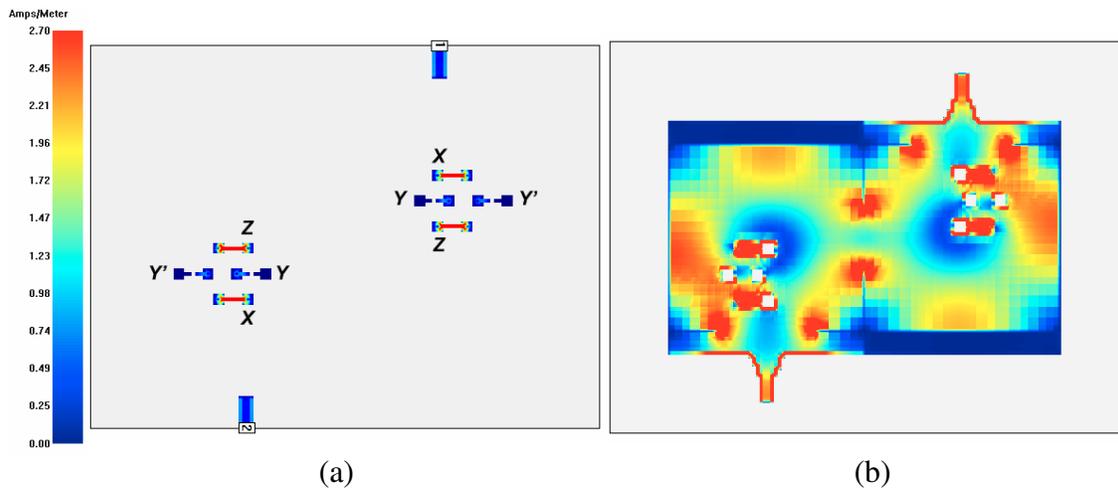


Fig. 31. Current distribution for three-layer PCB tunable SIW filter from Fig. 26 with  $XYY'Z = 1001$ , (a) layer one and (b) layer two.

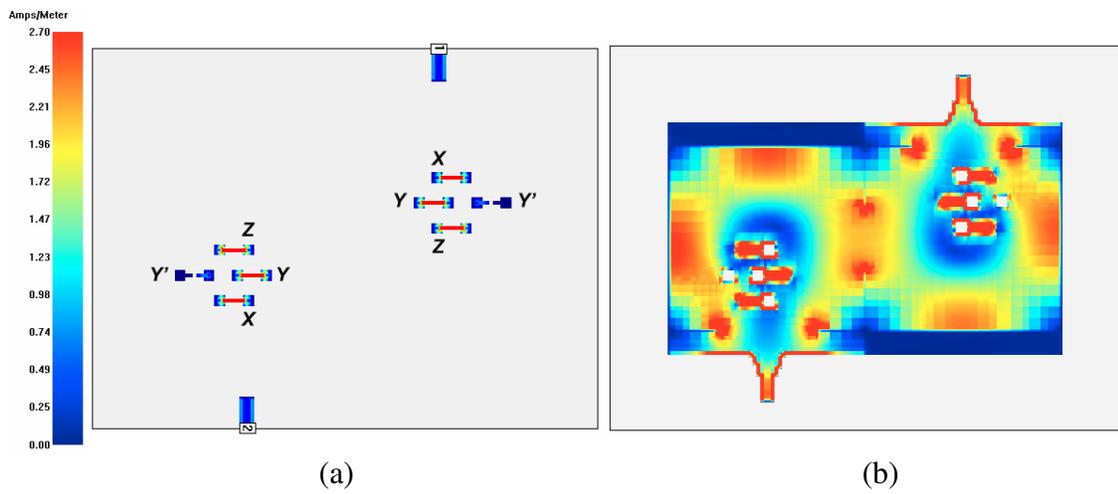


Fig. 32. Current distribution for three-layer PCB tunable SIW filter from Fig. 26 with  $XYY'Z = 1101$ , (a) layer one and (b) layer two.

To properly employ a PIN Diode as an RF switch, a biasing network similar to one shown in Fig. 33 is necessary [52], where C1 is the DC blocking capacitor and L2 is the RF choke. This ensures maximum isolation between the DC biasing circuit and the SIW RF filter at the operating frequencies of interest.

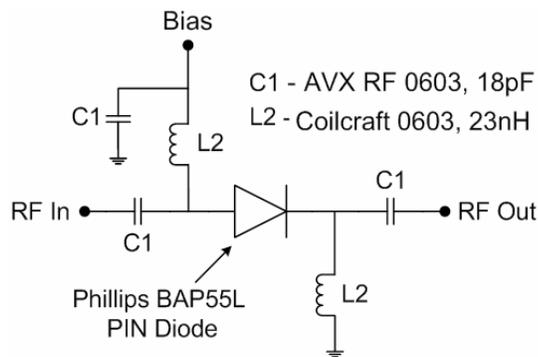
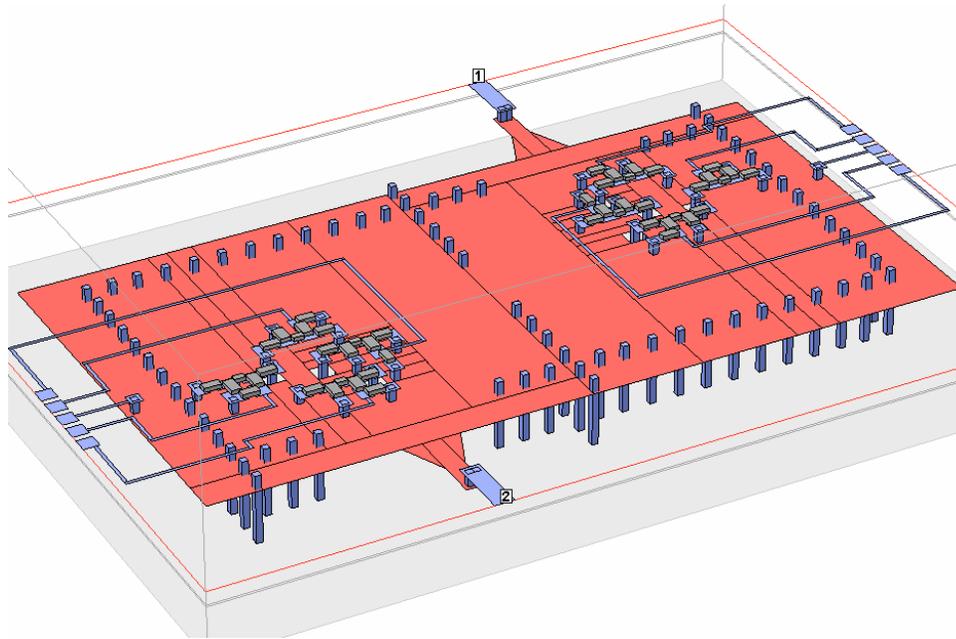


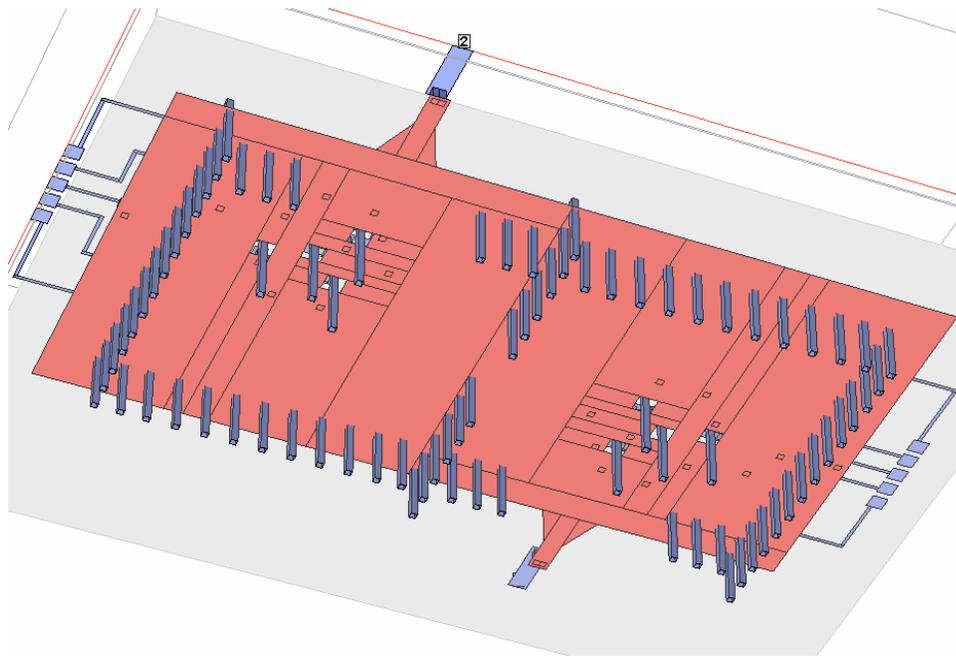
Fig. 33. PIN diode biasing network.

The value for C1 is chosen to provide the lowest reactance (highest possible capacitance) while still ensuring that the self resonant frequency of the component is greater than the operating frequency of the filter. This provides lowest possible resistance for the RF signal while blocking the DC biasing. The value for L2 is chosen to provide the highest reactance (highest possible inductance) while still ensuring that the self resonant frequency of the component is greater than the operating frequency. This provides highest possible resistance for the RF signal while passing through the DC biasing [52].

With all parameters known, the PIN diode biasing circuit is next laid out on top of the SIW tunable filter structure with full-wave simulation performed utilizing Sonnet. Fig. 34 depicts the three-dimensional top and bottom view of the implemented filter.



(a)



(b)

Fig. 34. PIN diode tunable SIW filter Sonnet layout, (a) top view and (b) bottom view.

Due to parasitics of the switching elements, SIW filter dimensions for the PIN diode design are re-adjusted for 3% bandwidth and lower frequency states ranging from 1.7 GHz to 2.2 GHz. This leads to re-establishing a new optimum tuning location and corresponding AB/CD tuning lines through the methodologies presented in the previous chapter. Fig. 35 depicts full-wave simulation of the PIN diode SIW filter design layout with Table V presenting the simulation performance summary.

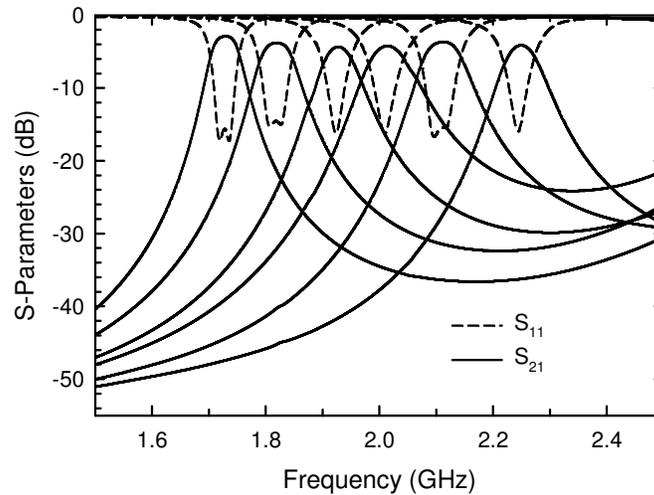


Fig. 35. Full-wave simulated response for tunable SIW filter with PIN diodes.

Table V. Tunable SIW Filter with PIN Diodes Simulated Performance Summary

State	0 – PIN Diode Off 1 – PIN Diode On				
	$f_0$	$X Y Y' Z$	$S_{21}$	FBW	$Q_U$
1	1.75 GHz	0 0 0 0	-2.8 dB	2.8%	135
2	1.82 GHz	0 0 1 0	-3.3 dB	2.9%	125
3	1.92 GHz	0 1 0 0	-4.3 dB	2.7%	117
4	2.00 GHz	0 1 1 0	-4.4 dB	3.4%	105
5	2.09 GHz	1 0 0 1	-3.4 dB	3.3%	115
6	2.22 GHz	1 1 0 1	-3.3 dB	3.0%	120

## 2. Tunable Filter Fabrication and Measurement

The top vias depicted in Fig. 26 and the first two layers (metal layer 1 – biasing network, metal layer 2 – SIW top cavity layer) are fabricated using both sides of the 0.635 mm duroid substrate. Metal layer 3 is provided from the bottom side of the 2.54 mm duroid substrate. Standard glass fiber (GF) pre-preg material is used to bond the two duroid materials followed by drilling holes for the wall and through vias shown in Fig. 26. Fig. 36 shows the fabricated board. Since the SIW cavity's top metal layer is sandwiched between the two substrates, only the biasing circuit is exposed.

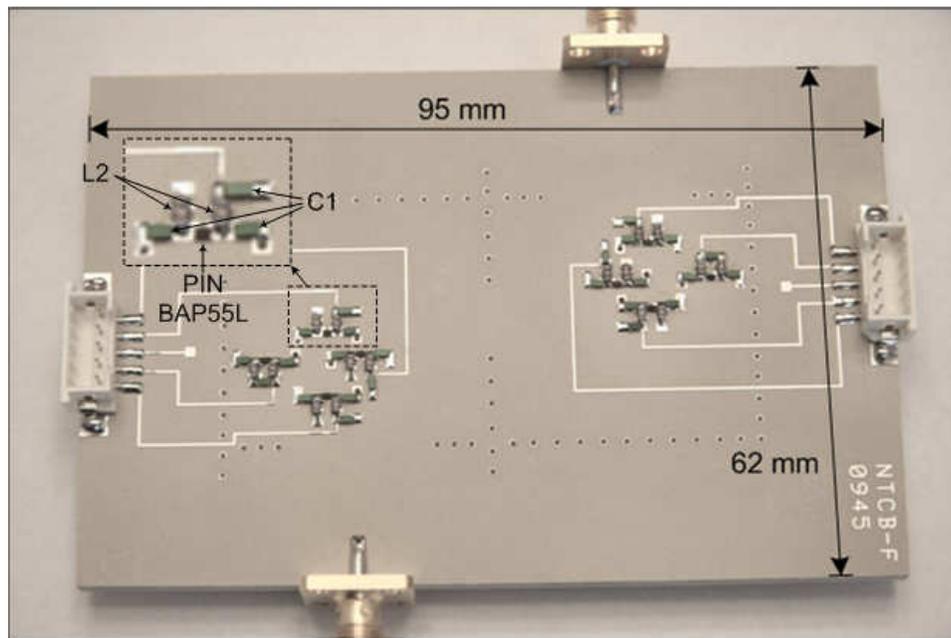


Fig. 36. Fabricated tunable SIW filter with PIN diodes including zoom-in of a single biasing circuit ( $C1 = 18 \text{ pF}$ ,  $L2 = 23 \text{ nH}$ ).

Fig. 37 shows the measured s-parameters for the PIN diode tunable SIW filter. Four PIN diodes per SIW cavity provide six states with 25% tuning range. Table VI presents measured performance for each state.

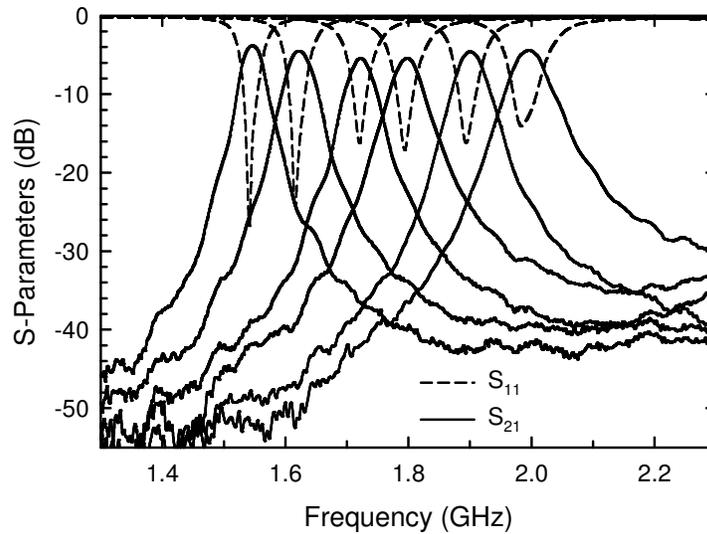


Fig. 37. Measured response for tunable SIW filter with PIN diodes.

Table VI. Tunable SIW Filter with PIN Diodes Measured Performance Summary

State	0 – PIN Diode Off 1 – PIN Diode On				
	$f_0$	$X Y Y' Z$	$S_{21}$	FBW	$Q_U$
1	1.55 GHz	0 0 0 0	-3.8 dB	2.4%	120
2	1.62 GHz	0 0 1 0	-4.4 dB	2.5%	115
3	1.72 GHz	0 1 0 0	-5.4 dB	2.3%	114
4	1.80 GHz	0 1 1 0	-5.4 dB	2.5%	105
5	1.89 GHz	1 0 0 1	-4.5 dB	2.8%	104
6	2.00 GHz	1 1 0 1	-4.4 dB	3.0%	101

The measured performance has a shift of 180 MHz for all tuning states compared to simulations due to permittivity tolerances of the substrate dielectric. The difference

between measured and simulated insertion loss is now around 1 dB primarily due to the added loss tangent manufacturing tolerances of a second duroid substrate in the multi-layer design. In addition, PIN diode performance provides a lower unloaded quality factor compared to the one obtained from the ideal tunable filter. This lower value is primarily attributed to the parasitics of the PIN diode. Maximum current consumption is 60 mA due to six forward biased PIN diodes for the highest tuning state (state 6).

## B. RF MEMS Switch – Radant MEMS RMSW-100

### 1. Modeling and Design

An RF MEMS switch chosen for this design is a product from Radant MEMS Incorporated [61]. The RMSW-100 Radant device is a series in-line metal contact switch with a MEMS cantilever construction fabricated on high-resistivity silicon. The cantilever beam performing the RF switching operation is sealed and protected inside a wafer cap. This type of construction provides simpler integration with other RF systems as well as increasing performance reliability. Fig. 38 illustrates the packaged three terminal device with the source, drain, and gate depicted.

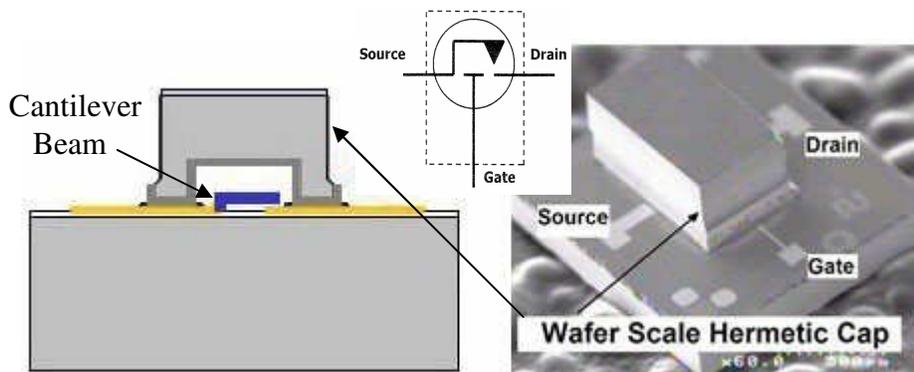


Fig. 38. Radant MEMS RMSW-100 RF switch with terminal arrangement.

Performance characteristics for the RMSW-100 include no quiescent power distribution, near zero harmonic distortion, low insertion loss (0.16 dB at 2.4 GHz), and high isolation (23 dB at 2.4 GHz). Fig. 39 shows how the single-pole single-throw (SPST) RF switch is activated through the gate terminal. Biasing the gate with a drive voltage of 90 V provides the electro-static force necessary to close the cantilever beam down onto the drain terminal (on-state/down position). With the appropriate protection circuits in place to isolate DC and RF signals, removing the drive voltage at the gate restores the cantilever to the up position providing the desired off-state condition.

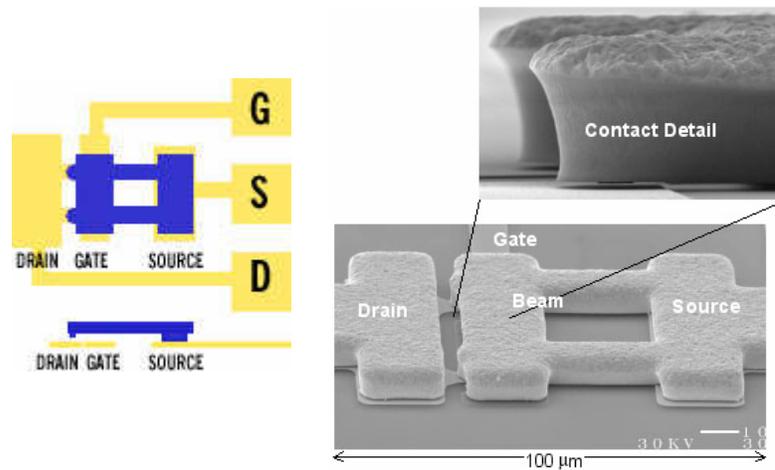


Fig. 39. Radant MEMS RMSW-100 single-pole single-throw switch illustration.

On-state and off-state s-parameter models have been provided by the company [61] for this device and are depicted in Fig. 40.

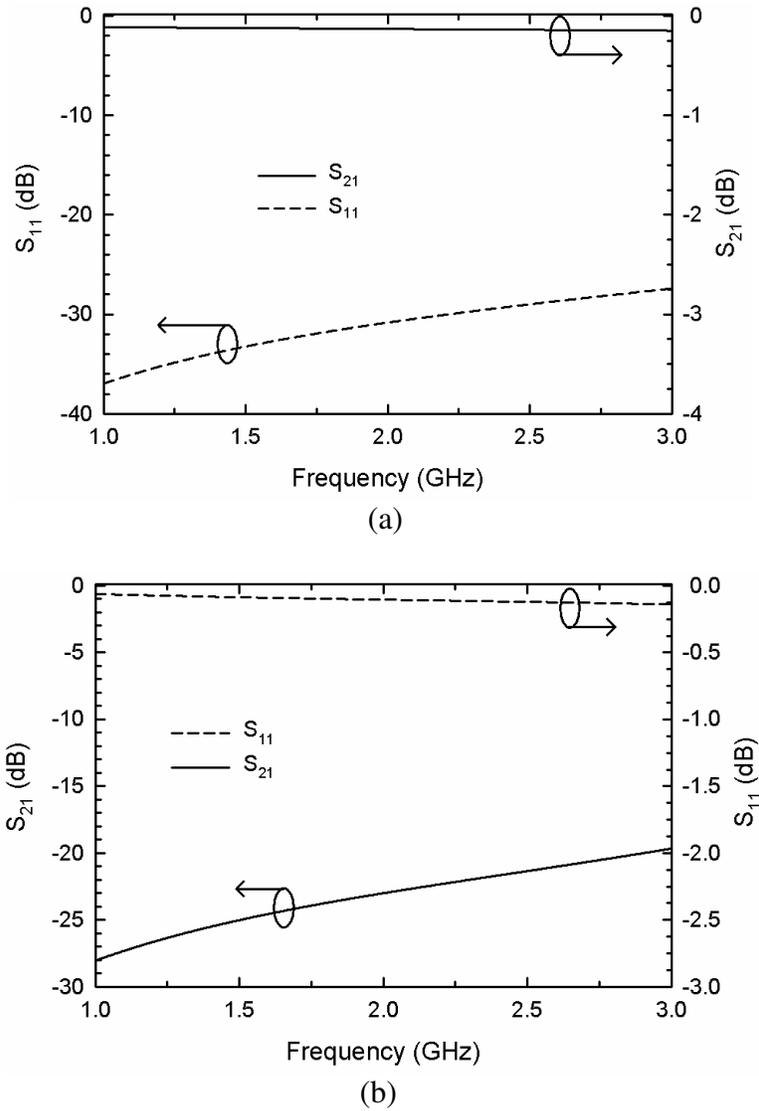


Fig. 40. Radant MEMS RMSW-100 switch s-parameters of (a) down-state position and (b) up-state position.

Utilizing the Radant MEMS switch s-parameter data, a new tunable SIW filter is designed employing the dimensions and characteristics of this device. Four RMSW-100 switches per SIW cavity are positioned appropriately along the CD and AB tuning lines derived from the methodology presented in the previous chapter. Due to the three

terminal arrangement, the source and drain pads on the packaged wafer are wire-bonded to the corresponding perturbing vias of the SIW tunable vias. The gate drain pad is next wire bonded to the appropriate biasing drive circuit. This provides the same tuning mechanism of on-state/off-state perturbing via posts utilized with the previous PIN diode design. Fig. 41 depicts the Radant MEMS layout and Fig. 42(a-b) shows the 3D layout in Sonnet.

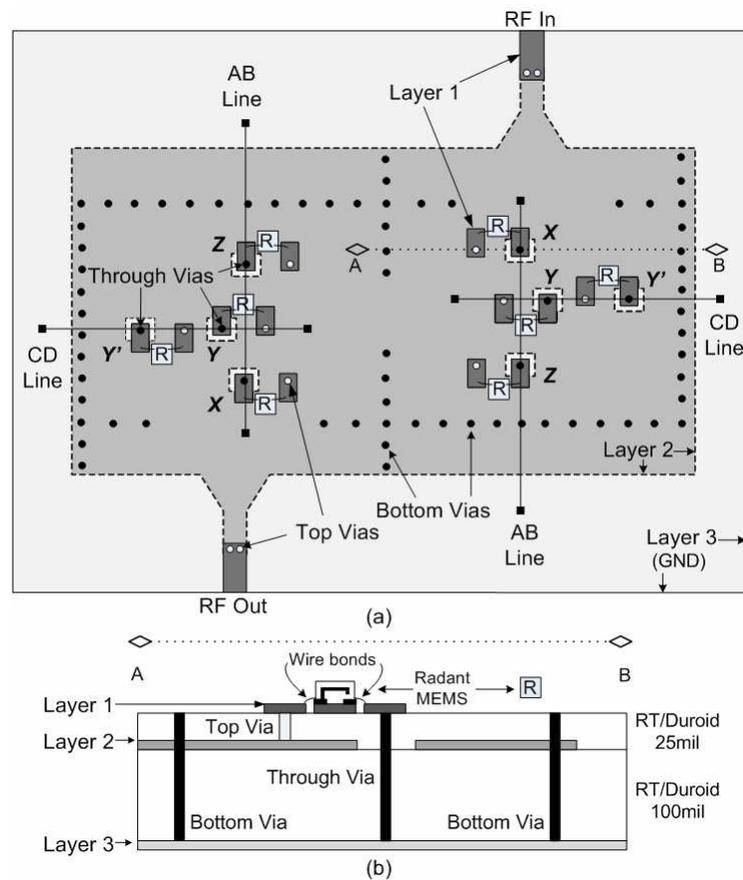


Fig. 41. Tunable SIW filter layout with Radant MEMS: a three-layer design, (a) top view and (b) side view.

By employing the filter design methods from the previous chapter, the first frequency state and fractional bandwidth for this layout are set to be 1.8 GHz and 3%,

respectively. Six frequency tuning states ranging from 1.8 GHz to 2.2 GHz are implemented with four Radant MEMS switches per cavity. Fig. 43 shows the full-wave simulated response. Table VII provides the simulation performance summary.

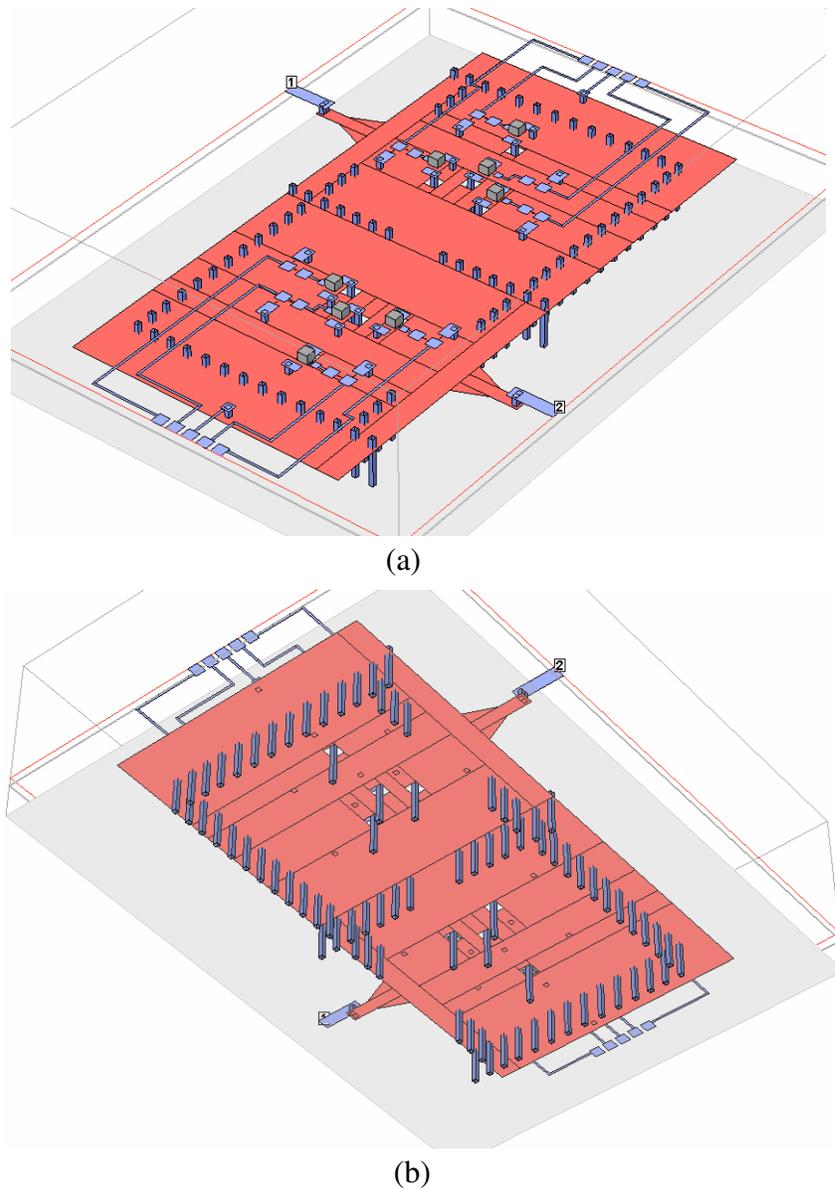


Fig. 42. Tunable SIW filter Sonnet layout with Radant MEMS switches, (a) top view and (b) bottom view.

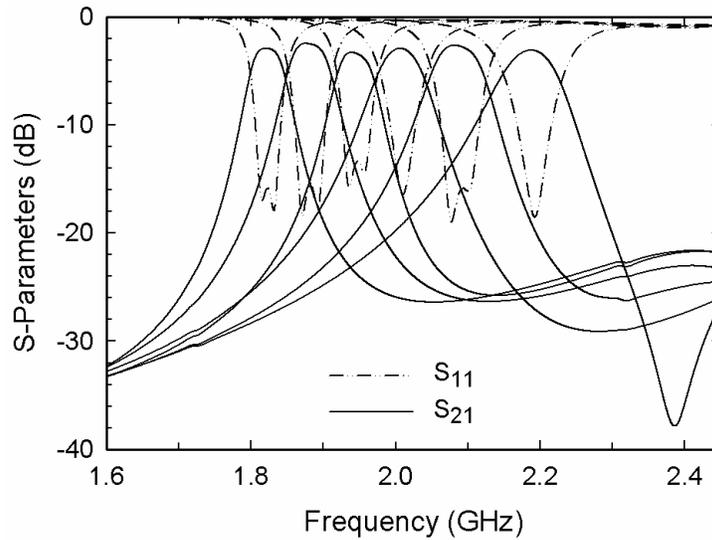


Fig. 43. Tunable SIW filter with Radant MEMS switches simulated response.

Table VII. Tunable Radant MEMS SIW Filter Performance Summary

State	0 – Radant MEMS Upstate 1 – Radant MEMS Downstate				
	$f_0$	$X Y Y' Z$	$S_{21}$	FBW	$Q_U$
1	1.82 GHz	0 0 0 0	-2.5 dB	3.0%	141
2	1.90 GHz	0 0 1 0	-2.1 dB	3.3%	136
3	1.97 GHz	0 1 0 0	-2.8 dB	2.9%	123
4	2.04 GHz	0 1 1 0	-2.6 dB	3.1%	121
5	2.12 GHz	1 0 0 1	-2.2 dB	3.3%	118
6	2.19 GHz	1 1 0 1	-2.8 dB	3.5%	110

Utilizing four Radant MEMS switches per SIW cavity, six states are simulated ranging from 1.82 GHz to 2.19 GHz (22% tuning). With fractional bandwidth ranging from 3.0% to 3.5%, insertion loss is better than 2.8 dB. Return loss is also better than 15 dB. Main differences between PIN diode filter and Radant MEMS filter performance include the higher simulated unloaded quality factors and lower power consumption for

the Radant MEMS filter. PIN Diode tuning requires 60 mA of current for the highest tuning state, whereas the Radant MEMS tuning supplies no current through the filter during the switch operation. This could be a considerable advantage for systems requiring low power consumption. Overall, simulations show Radant MEMS having better performance for tuning SIW filters.

## 2. Tunable Filter Fabrication and Measurement

The same multi-layer fabrication procedure as for the PIN diode filter is utilized to implement the Radant MEMS tunable SIW filter. Each switch has an R-C filter ( $R1 = 10\text{ k}\Omega$ ,  $C2 = 10\text{ pF}$ ) at the gate terminal to ensure isolation between DC and RF signals. Electrostatic protection from the drain and source terminals are not necessary, since these nodes are already connected to DC ground from the SIW cavity's top and bottom metal layers. Fig. 44 depicts the fabricated Radant MEMS tunable SIW filter.

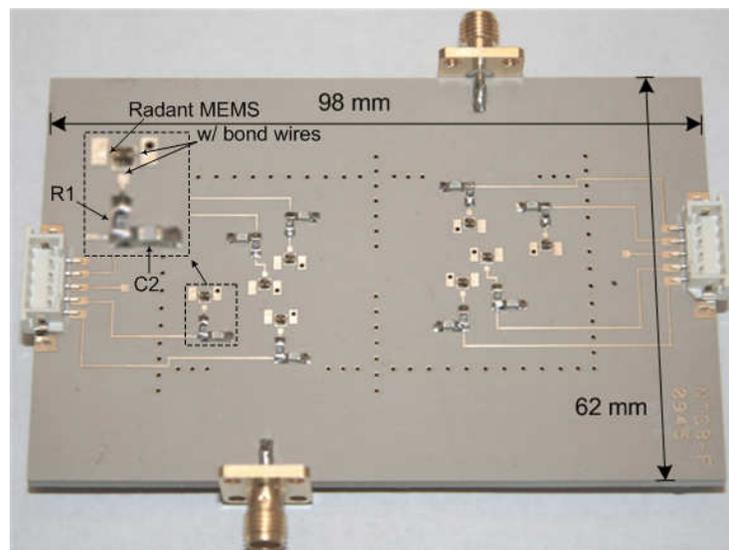


Fig. 44. Fabricated tunable SIW filter with Radant MEMS including zoom-in of a single biasing circuit ( $R1 = 10\text{ k}\Omega$ ,  $C2 = 10\text{ pF}$ ).

Fig. 45 shows the measured s-parameters for the Radant MEMS tunable SIW filter. Four Radant MEMS switches per SIW cavity provide six states with 24% tuning range. Table VIII presents the measured performance for each state.

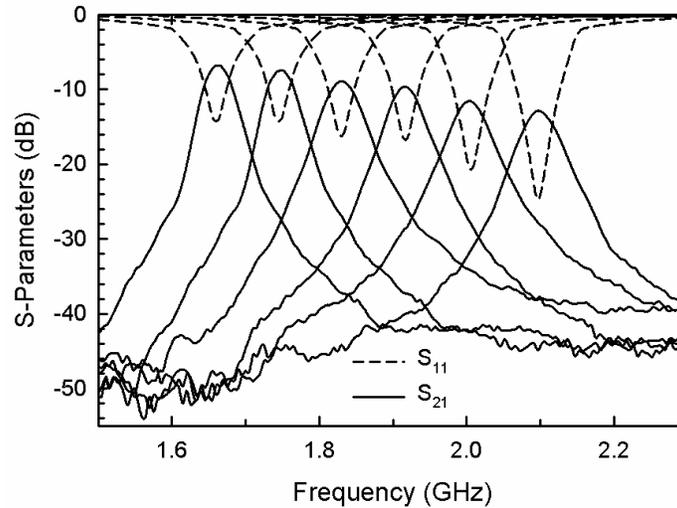


Fig. 45. Measured response for tunable SIW filter with Radant MEMS.

Table VIII. Tunable SIW Filter with Radant MEMS Measured Performance Summary

State	0 – Radant MEMS Upstate 1 – Radant MEMS Downstate				
	$f_0$	$X Y Y' Z$	$S_{21}$	FBW	$Q_U$
1	1.65 GHz	0 0 0 0	-6.9 dB	2.5%	72
2	1.74 GHz	0 0 1 0	-7.5 dB	2.8%	62
3	1.83 GHz	0 1 0 0	-9.3 dB	2.4%	63
4	1.92 GHz	0 1 1 0	-9.8 dB	2.6%	57
5	2.01 GHz	1 0 0 1	-11.2 dB	2.8%	49
6	2.10 GHz	1 1 0 1	-12.4 dB	3.0%	44

A considerable difference is observed between simulated and measured insertion loss results. As the frequency tuning states increase, insertion loss performance degrades. With all switches in the upstate position (state 1) the insertion loss is 6.9 dB. With six switches in the down-state position (state 6) the insertion loss increases to 12.4 dB. Each Radant MEMS switch in the downstate position seems to contribute an average of 1 dB insertion loss. Additionally, the measured isolation performance of the Radant MEMS switch did not appear as expected. Simulated and measured insertion loss with all switches in the up-state position (state 1) are 2.8 dB and 6.9 dB respectively. An investigation is continuing to more accurately predict Radant MEMS application to this design in addition to researching more ways to improve the loss. Subsequently, a second RF MEMS switch is chosen to examine different packaged MEMS technologies applied to this tunable SIW filter design.

### C. RF MEMS Switch – OMRON 2SMES-01

#### 1. Modeling and Design

The next RF MEMS switch chosen for this design is a new product from OMRON Corporation [62]. Newly developed OMRON 2SMES-01 is a single-pole dual-throw (SPDT) RF MEMS switch with operating frequencies up to 10 GHz. Some high performance characteristics attributed to this MEMS switch include high isolation (45 dB at 2 GHz), low power consumption (10  $\mu$ W), miniature size (5.2 x 3.0 x 1.8 mm), and a more robust fully enclosed solderable package. Additionally, two independent

MEMS switches can be utilized per packaged device for the SPDT switch. Fig. 46 shows the OMRON 2SMES-01 packaging and terminal arrangement.

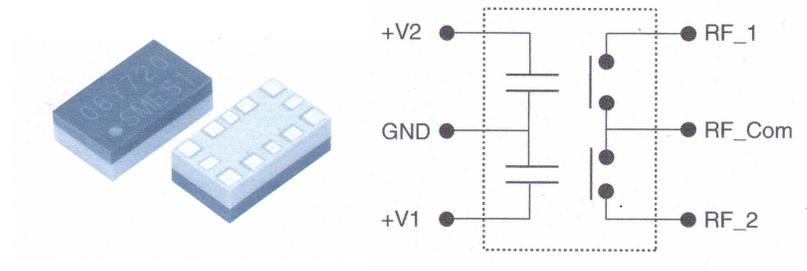


Fig. 46. OMRON 2SMES-01 MEMS relay with terminal arrangement.

Fig. 47 describes the basic operation of the OMRON MEMS switch. There is an electro-static actuator inside the packaged device with release springs connecting the RF MEMS shunt switch. A driving voltage of 34 V (V1 or V2 in Fig. 46) is required to charge the actuator, creating the electrostatic force necessary to move the electrodes into the contact position (on-state/down position). To turn off the switch (off-state/up position), the discharge resistor shown in Fig. 47 is required to effectively dissipate the charge accumulated in the electrodes once the drive voltage is removed, thereby enabling the restoring force of the springs to return the switch into the up position. Without this discharge mechanism, the MEMS shunt switch would be permanently in the down-state position following an initial turn-on drive voltage.

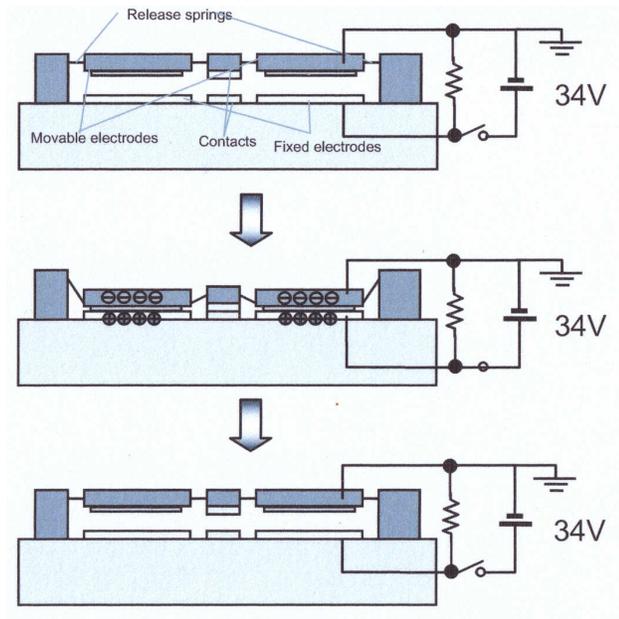


Fig. 47. Basic operation of OMRON 2SMES-01 RF MEMS switch.

On-state and off-state s-parameter models have been provided by the company [62] for this device and are depicted in Fig. 48(a-b).

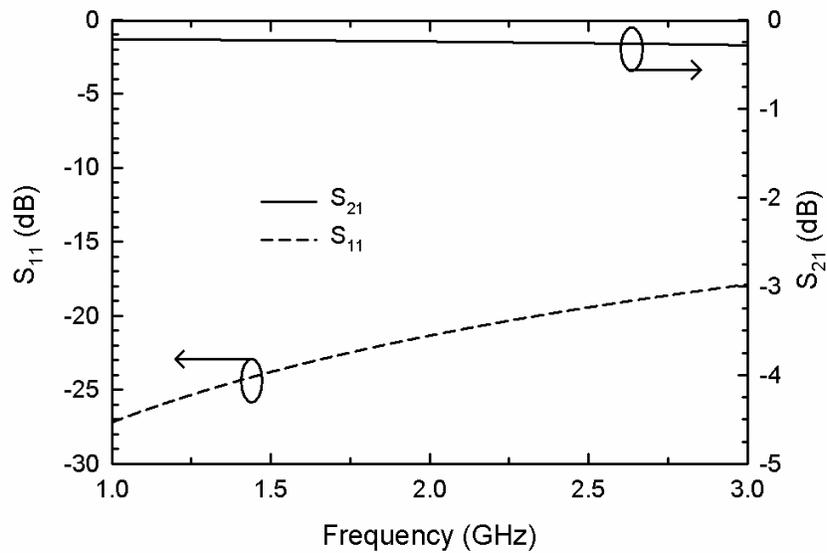


Fig. 48(a). OMRON MEMS switch s-parameters for down-state position.

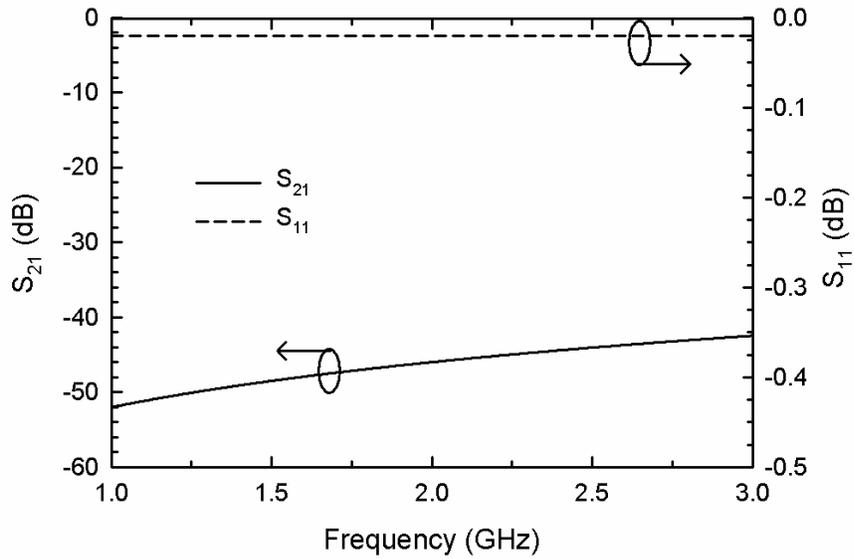


Fig. 48(b). OMRON MEMS switch s-parameters for up-state position.

Utilizing the OMRON MEMS switch s-parameter data, a new tunable SIW filter is designed exploiting the unique characteristics of this device. Three OMRON MEMS packaged relays per SIW cavity are positioned appropriately along the CD and AB tuning lines derived from the methodology presented in the previous chapter. Due to the device's single-pole double-throw attribute, two perturbing via posts can be implemented using one 2SMES-01 MEMS relay. This provides more tuning capability compared to both the PIN diode and Radant MEMS designs. Additionally, unloaded quality factors for this tunable filter should still have good performance despite more switches implemented due to a very high isolation attributed to this device (-50 dB at 1.5 GHz). Fig. 49 depicts the new layout.

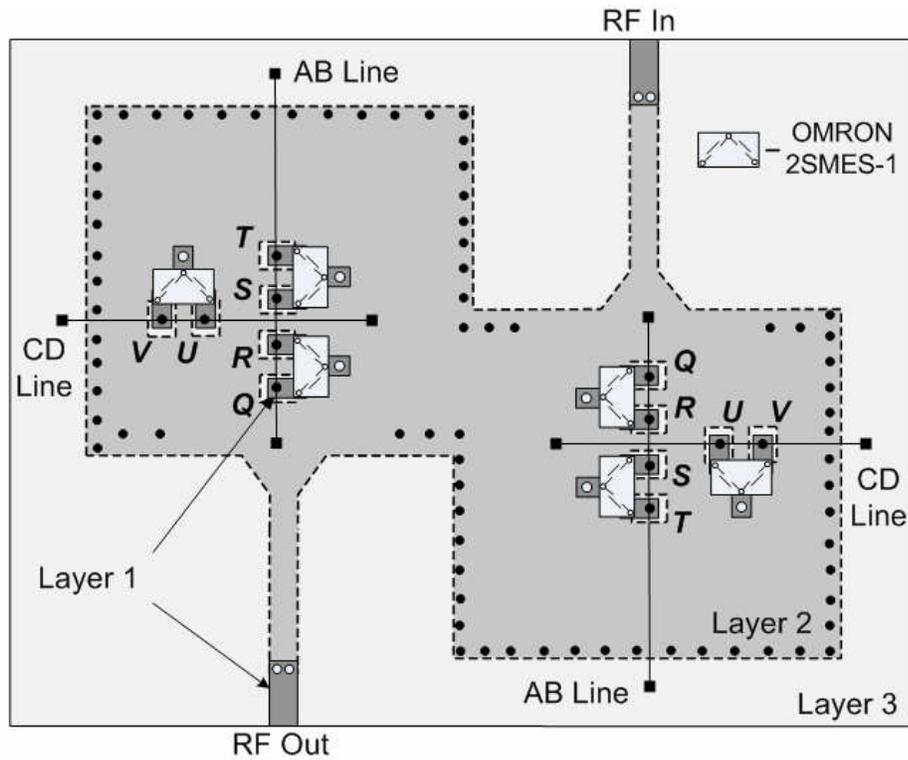
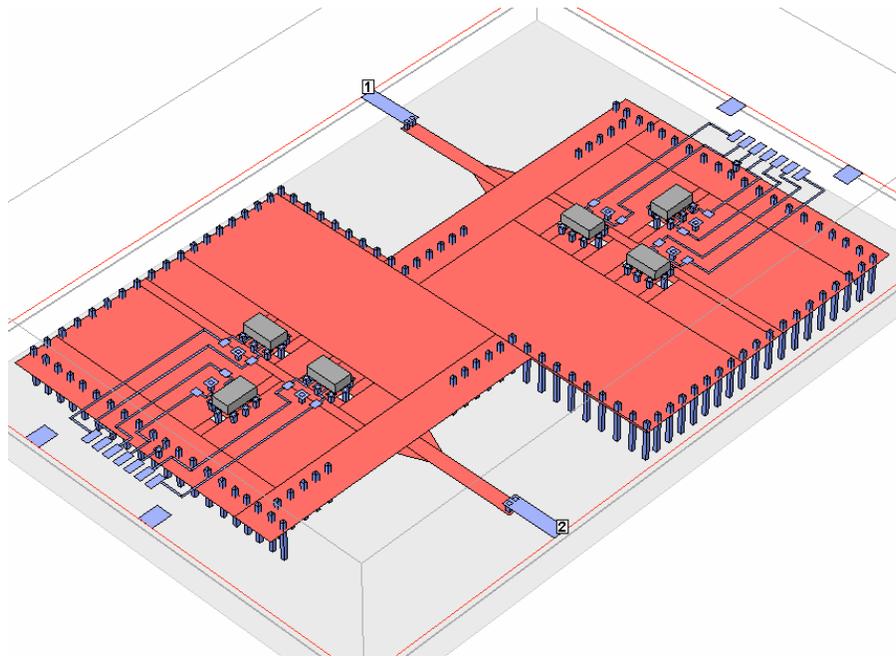
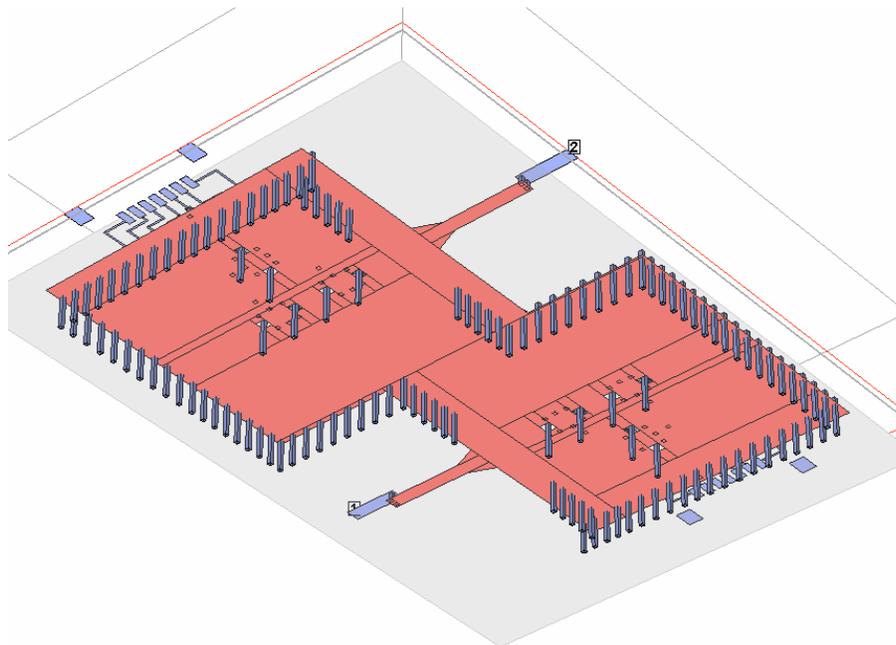


Fig. 49. Tunable SIW filter layout with OMRON MEMS switches.

Employing the filter design method from the previous chapter, the first frequency state and fractional bandwidth for this layout are 1.5 GHz and 4% respectively. This new design incorporates more skew to the two SIW cavities. Since higher bandwidths correlate to poor stop band performance, the skewed structure creates a transmission zero outside the pass band in order to help suppress the second spurious frequency mode [63]. Further suppression techniques are discussed and utilized in the following chapter. Fig. 50 shows the filter layout in Sonnet with three SPDT switches per cavity (six via posts per cavity) while Fig. 51 depicts the full-wave simulated response. Table IX provides the simulation performance summary.

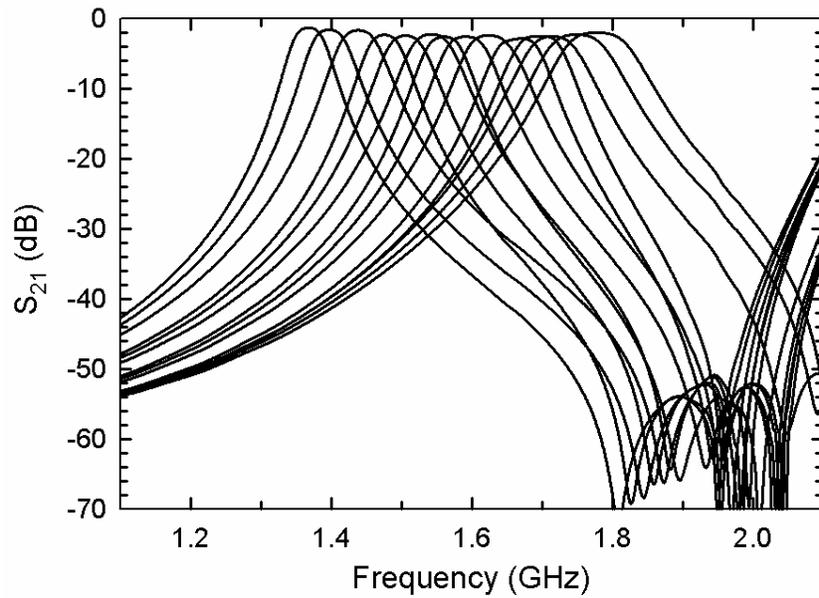


(a)

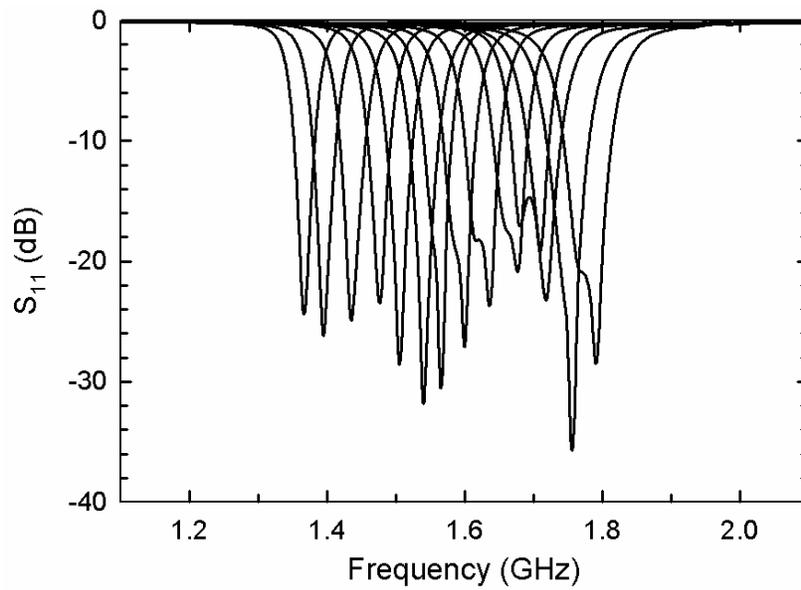


(b)

Fig. 50. Tunable SIW filter Sonnet layout with OMRON MEMS switches, (a) top view and (b) bottom view.



(a)



(b)

Fig. 51. Tunable SIW filter with OMRON MEMS switches simulated response, (a)  $S_{21}$  and (b)  $S_{11}$ .

Table IX. Tunable OMRON MEMS SIW Filter Performance Summary

State	0 – OMRON MEMS Up-State 1 – OMRON MEMS Down-State				
	$f_0$	$QRSTUV$	$S_{21}$	FBW	$Q_U$
1	1.37 GHz	000000	-1.3 dB	4.0%	178
2	1.40 GHz	000001	-1.6 dB	4.1%	155
3	1.44 GHz	000010	-1.7 dB	4.2%	140
4	1.47 GHz	010000	-2.3 dB	3.9%	129
5	1.50 GHz	010001	-2.4 dB	3.9%	121
6	1.54 GHz	010010	-2.5 dB	4.0%	115
7	1.57 GHz	101000	-2.6 dB	4.1%	117
8	1.60 GHz	101001	-2.5 dB	4.2%	113
9	1.63 GHz	101010	-2.4 dB	4.4%	110
10	1.66 GHz	111001	-2.8 dB	4.2%	109
11	1.69 GHz	111010	-2.5 dB	4.1%	115
12	1.72 GHz	111100	-2.5 dB	4.3%	111
13	1.75 GHz	111101	-2.2 dB	4.9%	108
14	1.78 GHz	111110	-2.0 dB	5.1%	106

Utilizing three OMRON MEMS relays per SIW cavity, fourteen states are simulated ranging from 1.37 GHz to 1.78 GHz (26% tuning). With fractional bandwidth ranging from 3.9% to 5.1%, insertion loss is better than 2.8 dB. Return loss is also better than 15 dB. The main difference for the OMRON MEMS filter performance is in the slight increase to the tuning range compared to the PIN Diode and Radant MEMS design. This is due to more perturbing via posts present for this design. From the previous chapter, more perturbing via posts correspond to an increase to the tuning capability of the filter. Additionally, despite similar unloaded quality factors, the

OMRON MEMS response provides over two times more frequency states compared to both previous designs. This reveals an overall better insertion loss performance per OMRON MEMS switch.

## 2. Tunable Filter Fabrication and Measurement

The same multi-layer fabrication procedure as the other two filters is utilized for the OMRON MEMS tunable SIW filter. Each OMRON MEMS device has a discharge resistor ( $R1 = 1\text{ M}\Omega$  - resistor depicted in Fig. 47) connected to the V1 and V2 biasing terminals. Fig. 52 depicts the fabricated OMRON MEMS tunable SIW filter.

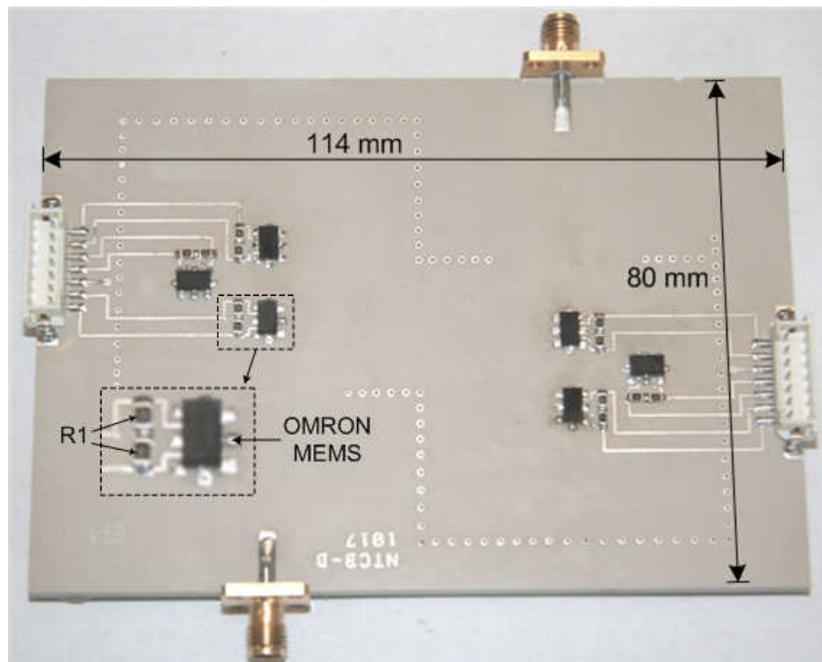


Fig. 52. Fabricated tunable SIW filter with OMRON MEMS relays including zoom-in of a single biasing circuit ( $R1 = 1\text{ M}\Omega$ ).

Fig. 53 shows the measured s-parameters for the OMRON MEMS tunable SIW filter. Three OMRON MEMS relays per SIW cavity provide 14 states with 30% tuning range. Table X presents the measured performance for each state.

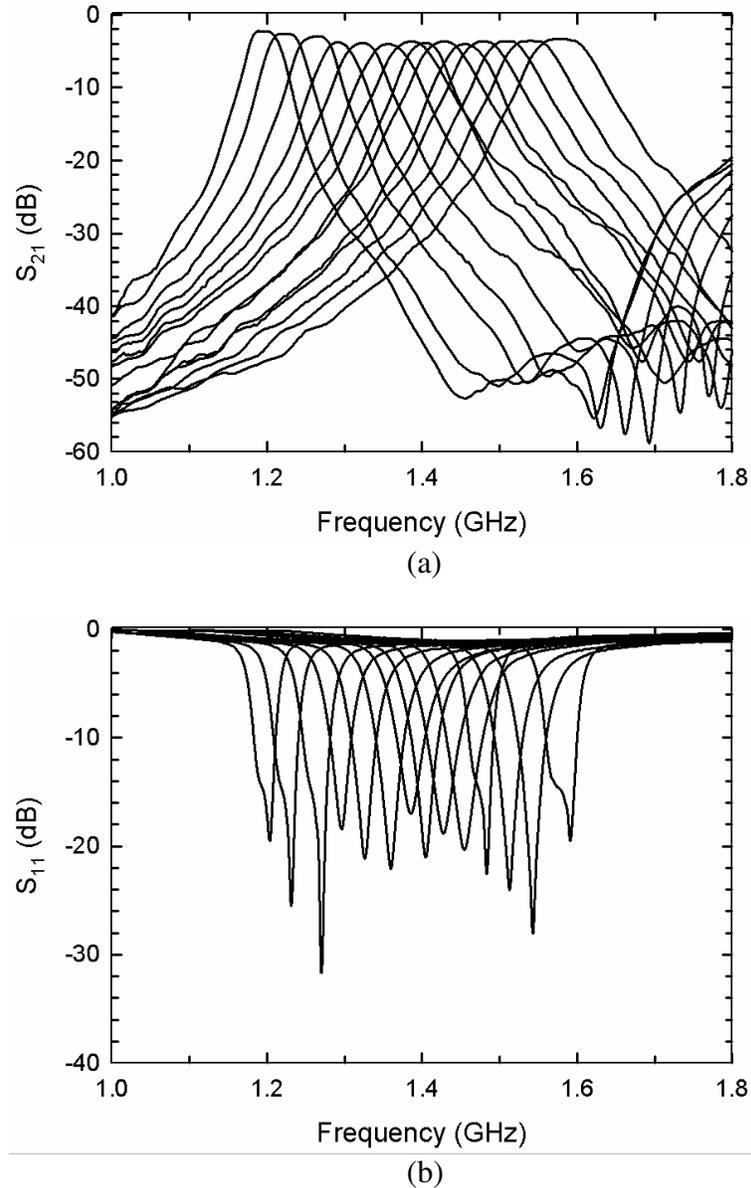


Fig. 53. Measured response for tunable SIW filter with OMRON MEMS, (a)  $S_{21}$  and (b)  $S_{11}$ .

Table X. Tunable OMRON MEMS SIW Filter Measured Performance Summary

State	0 – OMRON MEMS Up-State 1 – OMRON MEMS Down-State				
	$f_0$	$QRSTUV$	$S_{21}$	FBW	$Q_U$
1	1.19 GHz	000000	-2.2 dB	3.6%	132
2	1.22 GHz	000001	-2.6 dB	3.8%	120
3	1.26 GHz	000010	-2.9 dB	3.7%	117
4	1.29 GHz	001000	-3.6 dB	3.1%	112
5	1.32 GHz	001001	-3.8 dB	3.5%	110
6	1.36 GHz	001010	-4.1 dB	3.8%	95
7	1.38 GHz	001110	-3.6 dB	4.0%	101
8	1.40 GHz	101001	-3.9 dB	3.9%	96
9	1.42 GHz	101010	-3.7 dB	3.7%	100
10	1.45 GHz	111001	-4.0 dB	3.9%	94
11	1.48 GHz	111010	-3.6 dB	3.8%	108
12	1.51 GHz	111100	-3.7 dB	3.9%	97
13	1.54 GHz	111101	-3.6 dB	4.2%	93
14	1.58 GHz	111110	-3.2 dB	4.4%	95

Fourteen frequency tuning states are measured ranging from 1.19 GHz to 1.58 GHz (30% tuning). With fractional bandwidth ranging from 3.6% to 4.4%, insertion loss is better than 4.1 dB. Return loss is also better than 15 dB. OMRON MEMS tunable SIW filter measurements more closely match simulations compared to the Radant MEMS tunable SIW filter. However, insertion loss still measures around 1.0 dB higher compared to simulations resulting in a slightly lower unloaded quality factor. This is again due to the added manufacturing tolerances of the loss tangent for a second duroid substrate in the multi-layer design. In addition, the slight frequency shift is also

attributed to the permittivity tolerances of the manufactured substrate. Overall, both the PIN diode and OMRON MEMS RF switches provide very promising results for tuning SIW two-pole bandpass filters.

## CHAPTER IV

## SPURIOUS SUPPRESSION FOR TUNABLE SIW FILTERS

A. Spurious Suppression – Basic Idea and Implementation

As described in the previous chapter, creating a skewed two-cavity SIW filter provides a transmission zero located at the second spurious mode. To suppress higher order modes, a simple technique is utilized enabling planar filter structures to be integrated with the SIW filter. Due to the nature of SIW cavities, planar low pass filters can be placed at both the input and output ends of the microstrip-to-SIW transition regions [64]. This provides the required spurious suppression for higher order modes. Fig. 54 depicts the simulated insertion loss response of the OMRON MEMS SIW tunable filter design carried out to 4.0 GHz.

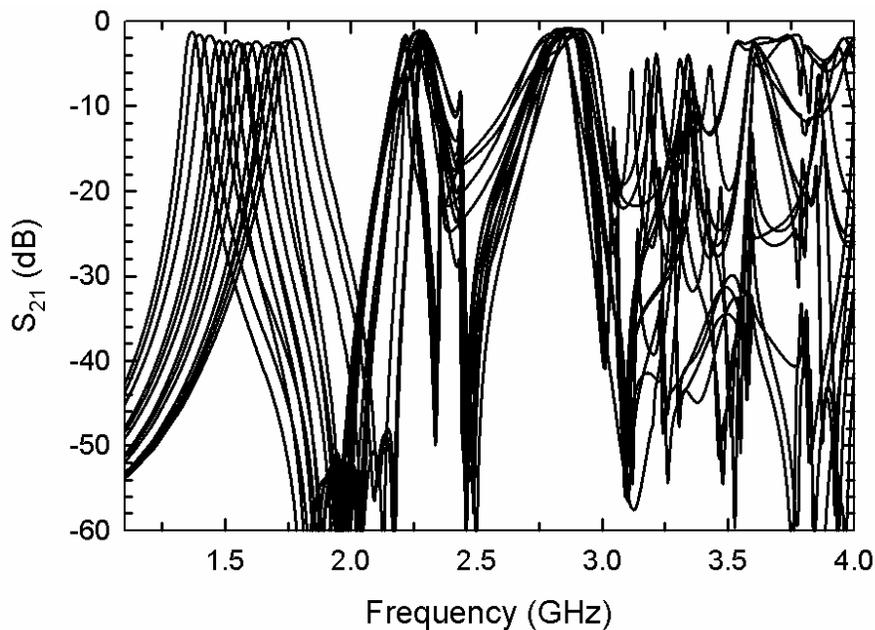


Fig. 54. SIW tunable filter with OMRON MEMS switches simulated response (spurious modes up to 4.0 GHz).

With the second order spurious mode suppressed by the skewed SIW cavities, third and fourth order spurious modes are still observed at 2.25 GHz and 2.8 GHz respectively. Consequently, a lowpass filter (LPF) is designed with greatest stopband performance near 2.25 GHz. However, the passband characteristics for the LPF must also provide minimal loss from the lowest to highest frequency tuning states for the OMRON MEMS SIW tunable filter. Such a LPF is realized according to [49] utilizing the same substrate materials from previous designs. A fifth-order elliptic LPF filter with passband ripple of 0.1 dB and cutoff frequency of 1.9 GHz is developed and simulated in Sonnet. For added isolation from the biasing network located on the top layer, the LPF is implemented on the same metal layer as the top of the SIW cavity. Fig. 55 illustrates the layout of the LPF with Fig. 56 depicting the simulated response.

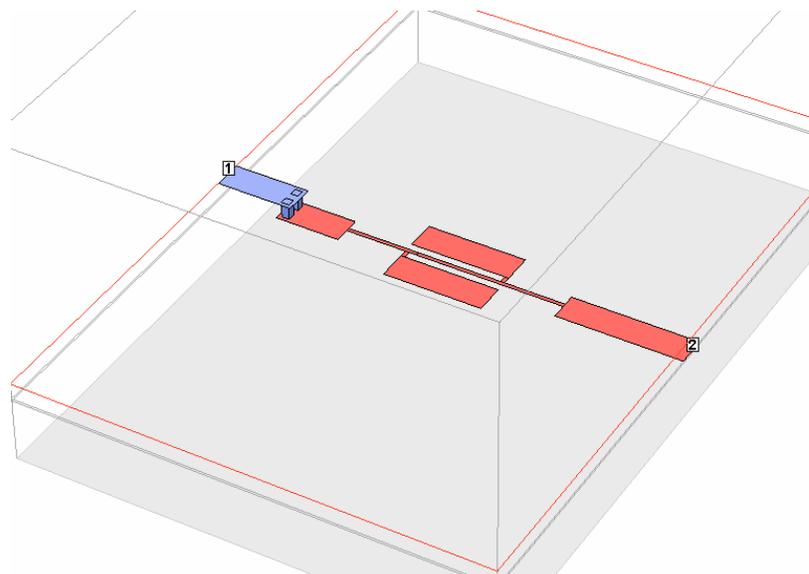


Fig. 55. Spurious suppression LPF Sonnet layout for OMRON MEMS SIW tunable filter.

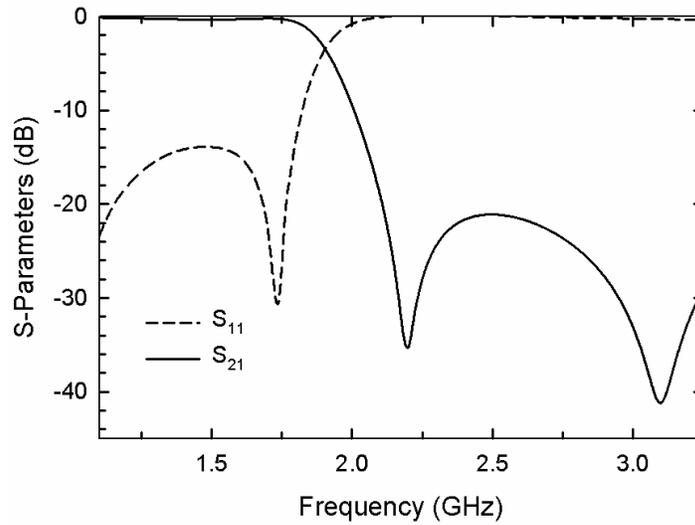


Fig. 56. Fifth-order elliptic LPF simulated response with  $f_o = 1.9$  GHz.

This LPF filter has the desired maximum stopband performance at approximately 2.25 GHz. Additionally, Fig. 57 illustrates how the passband provides minimal loss from the lowest to highest frequency tuning states of the OMRON MEMS tunable SIW filter.

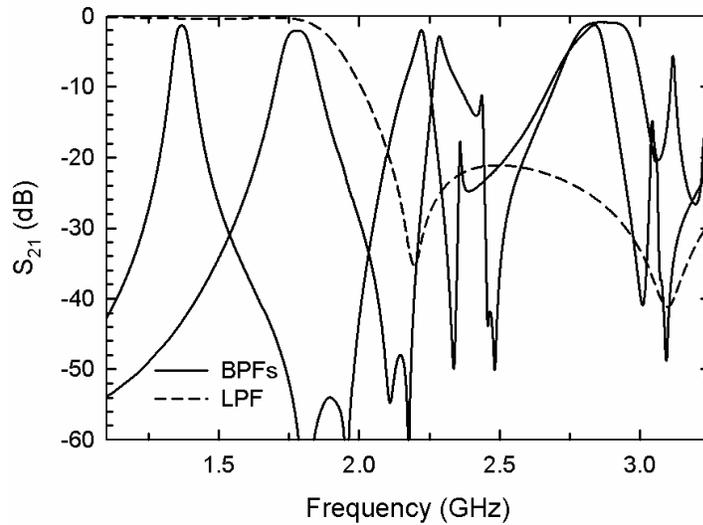


Fig. 57. Overlay of lowest and highest frequency tuning states (BPFs) with fifth-order elliptic LPF, simulated response.

Fig. 58 shows the simple integration of the fifth-order LPF connecting to both ends of the OMRON MEMS SIW tunable filter. Fig. 59 illustrates the lowest frequency tuning state performance. Since all tuning states have the same third and fourth order spurious modes at 2.25 and 2.8 GHz respectively, only one frequency state is depicted to simplify analysis and compare to subsequent LPFs.

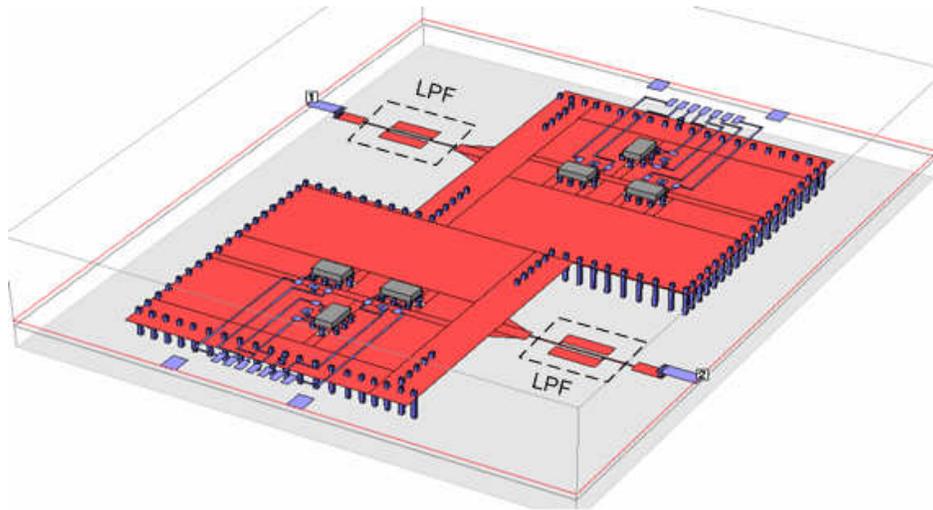


Fig. 58. Fifth-order elliptic LPF layout integrated with OMRON MEMS SIW tunable filter.

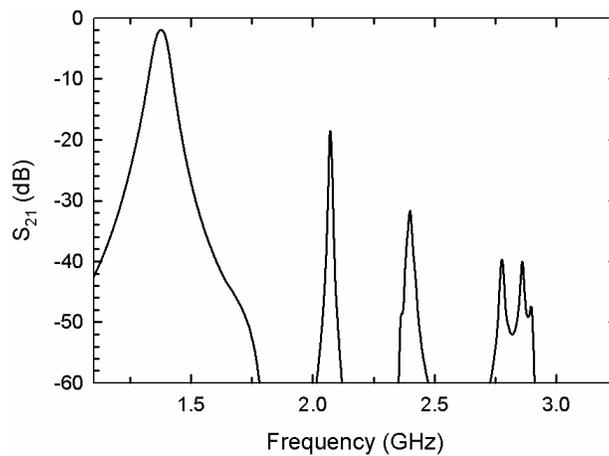


Fig. 59. Simulated insertion loss of lowest frequency tuning state for the fifth-order elliptic LPF integrated with OMRON MEMS SIW tunable filter.

Fig. 59 shows good suppression beyond 2.25 GHz, though there is still a spur present at approximately 2.0 GHz. Shifting the cutoff frequency lower would remove this notch. However, since the highest frequency state for the OMRON MEMS SIW tunable filter is 1.8 GHz, the cutoff frequency for the LPF must not deviate from the previously designed 1.9 GHz. A higher order LPF filter ( $n = 10$ ) is therefore implemented with a sharper roll-off while still maintaining the same specifications of the previous LPF ( $f_0 = 1.9$  GHz, passband ripple = 0.1). Fig. 60 illustrates the Sonnet layout for the tenth-order elliptic filter. The simulated response is shown in Fig. 61.

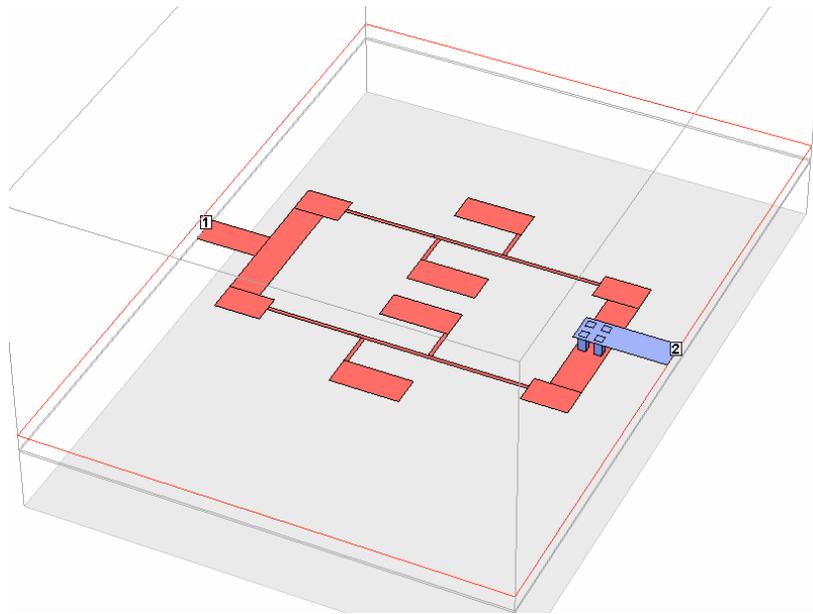


Fig. 60. Tenth-order spurious suppression LPF Sonnet layout for OMRON MEMS SIW tunable filter.

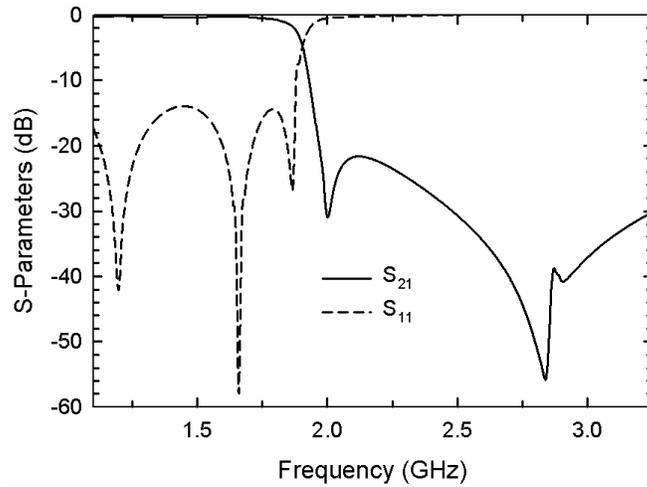


Fig. 61. Tenth-order spurious suppression LPF for OMRON MEMS SIW tunable filter, simulated response.

The overlay of this LPF with the lowest and highest frequency tuning states reveals the same cutoff frequency of 1.9 GHz but with a steeper stopband (Fig. 62). This configuration removes the spur at 2.0 GHz. However, it can only provide around 22 dB suppression at the spurious frequency of 2.25 GHz due to an  $S_{21}$  of -22 dB for the LPF at 2.25 GHz.

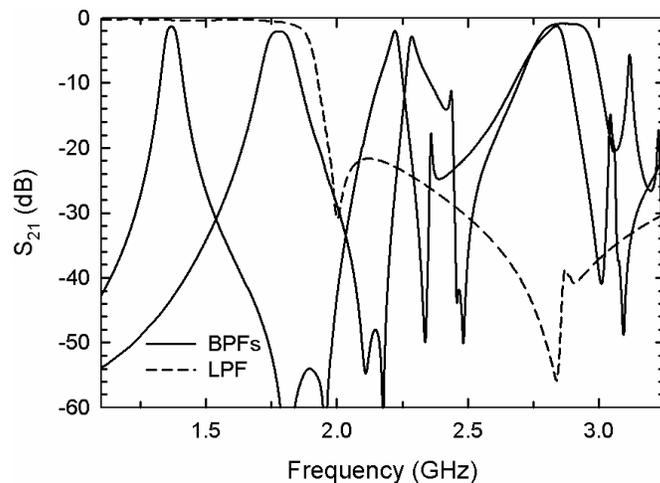


Fig. 62. Overlay of lowest and highest frequency tuning states (BPFs) with tenth-order spurious suppression LPF, simulated response.

Inserting the higher order LPF filter in Fig. 61 onto both sides of the OMRON MEMS SIW tunable filter reveals the following lowest frequency state simulated response illustrated in Fig. 63, confirming -22 dB suppression at 2.25 GHz.

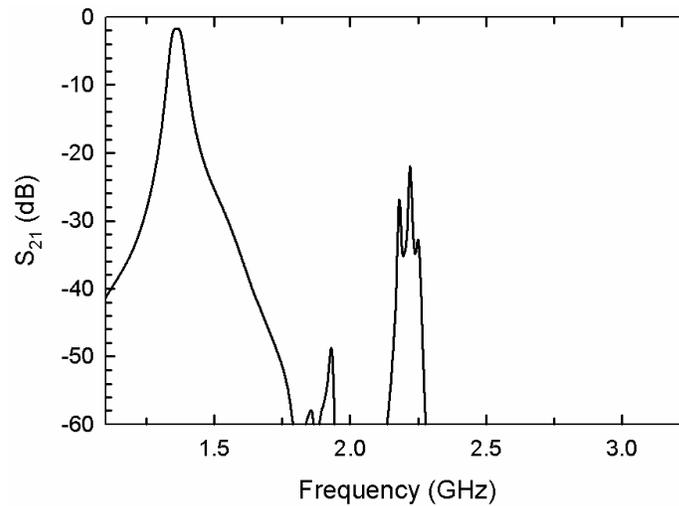


Fig. 63. Tenth-order spurious suppression LPF integrated with OMRON MEMS SIW tunable filter, simulated insertion loss of lowest frequency tuning state.

In order to fully suppress the entire region through 3.0 GHz, both types of LPFs (Fig. 55-56 and Fig. 60-61) are employed. The first LPF (fifth-order elliptic) provides better than -30 dB suppression at the spurious band of 2.25 GHz. However, a spur at 2.0 GHz is still present for this filter. The second LPF (tenth-order elliptic) removes the spur but only provides -22 dB suppression at the spurious band of 2.25 GHz. To better optimize the spurious rejection outside the SIW filter tuning range, both LPFs are employed as shown in Fig. 64. The first LPF is located at the input port, and the second LPF is located at the output port of the tunable filter.

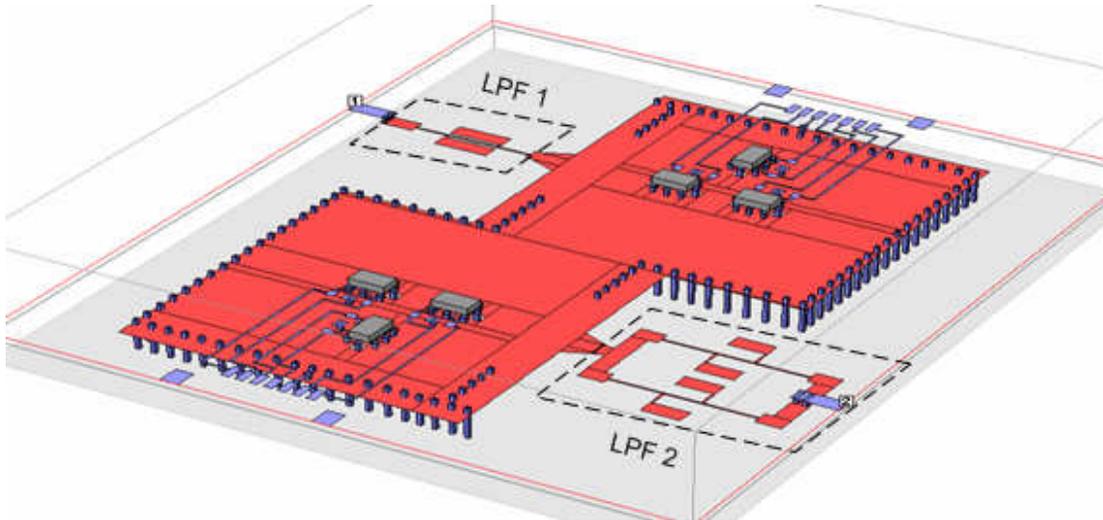


Fig. 64. Both types of spurious suppression LPFs integrated with OMRON MEMS SIW tunable filter.

Fig. 65 shows the overlay response for both types of LPFs with the lowest and highest frequency states from the OMRON MEMS SIW tunable filter. Both LPFs provide the same cutoff frequency of 1.9 GHz with different stop bands to improve the out-of-band spurious rejection performance.

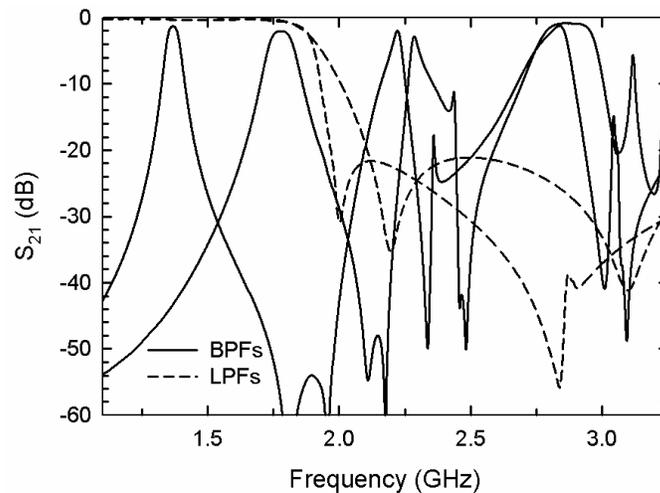


Fig. 65. Overlay of lowest and highest frequency tuning states (BPFs) with both types of spurious suppression LPFs, simulated response.

The lowest frequency state simulated response for this fully integrated configuration is illustrated in Fig. 66. This results in spurious suppression of -42 dB through 3.0 GHz.

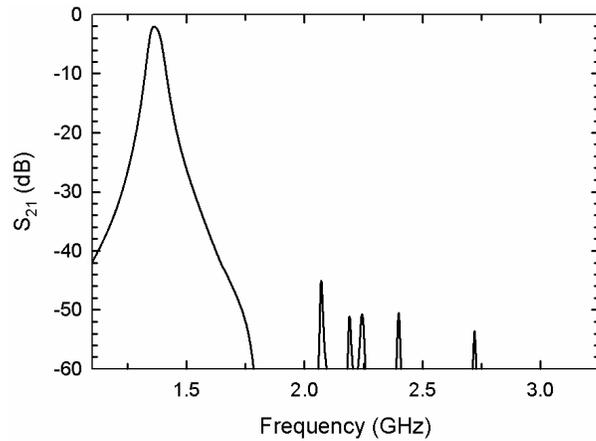


Fig. 66. Fully integrated spurious suppression LPFs with OMRON MEMS SIW tunable filter, simulated insertion loss of lowest frequency tuning state.

Fig. 67 shows the simulated response of the final configuration implemented on all frequency tuning states for the OMRON MEMS SIW tunable filter.

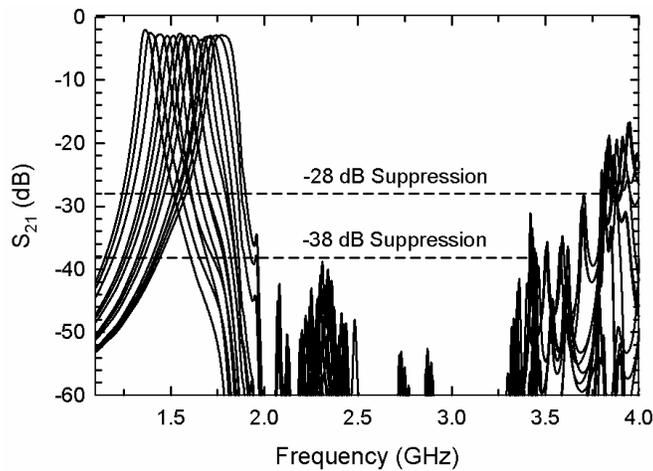


Fig. 67. Simulated  $S_{21}$  response of the OMRON MEMS SIW filter with spurious suppression LPFs for all tuning states.

This final configuration provides better than -28 dB spurious suppression up to 3.8 GHz for all frequency states. In addition, every tuning state's second (1.9 GHz), third (2.25 GHz), and fourth (2.8 GHz) spurious modes have better than -38 dB suppression. All frequency states have the same passband tuning characteristics compared to the OMRON MEMS SIW tunable filter without LPF spurious suppression presented in the previous section. Primary differences only involve a higher insertion loss due to the low pass filters which is less than 0.4 dB.

#### B. Spurious Suppression Measurement for SIW Tunable Filters

The same multi-layer fabrication procedure as previous SIW tunable filters is utilized for the OMRON MEMS tunable SIW filter with spurious suppression. With minimal increase to the overall size of the tunable filter, LPFs are placed at the RF input and output microstrip transmission line locations. Additionally, since the LPFs are fabricated into the inner-metal layer of the design, there is no difference to the outer appearance compared to filters without spurious suppression. Fig. 68 depicts the fabricated OMRON MEMS tunable SIW filter with spurious suppression LPFs located at the input and output ports of the filter.

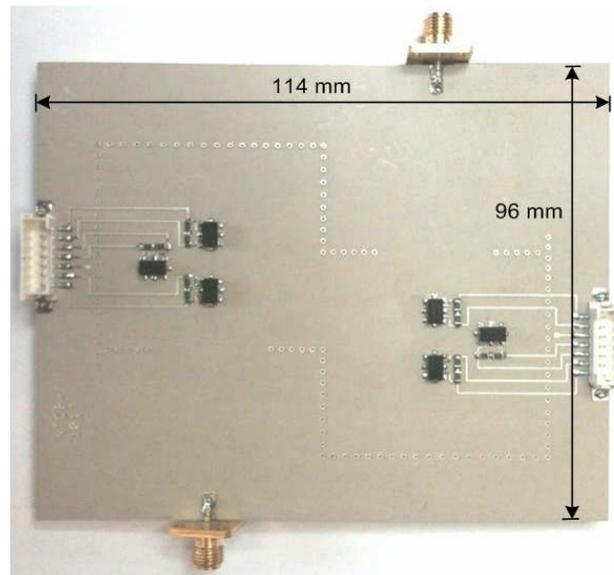


Fig. 68. Fabricated tunable SIW filter with ORMON MEMS relays and spurious suppression.

Fig. 69 shows the measured insertion loss for the OMRON MEMS tunable SIW filter with spurious suppression. Table XI presents measured performance for each state.

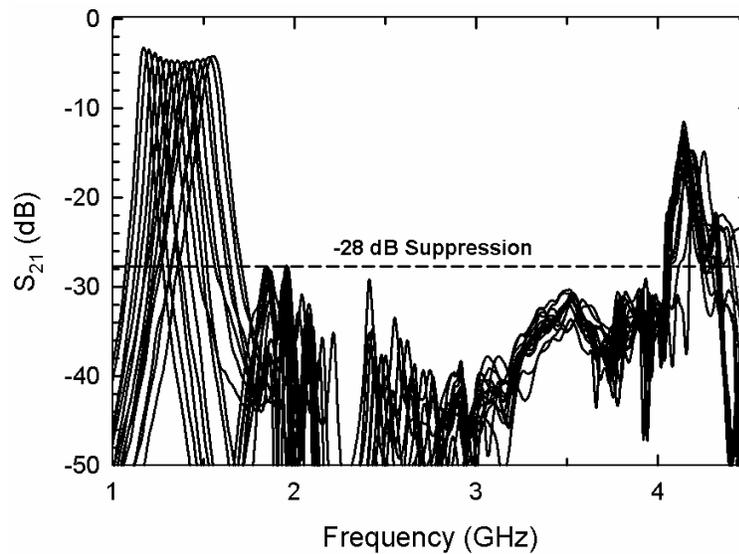


Fig. 69. Measured response for the OMRON MEMS tunable SIW filter with spurious suppression.

Table XI. Tunable OMRON MEMS SIW Filter with Spurious  
Suppression Measured Performance Summary

State	<b>0 – OMRON MEMS Up-State</b> <b>1 – OMRON MEMS Down-State</b>						
	$f_0$	$QRSTUV$	$S_{21}$	$S_{11}$	FBW	$Q_U$	Spurious Suppression to 4.0 GHz
1	1.18 GHz	000000	-3.2 dB	-18 dB	3.8%	116	-28 dB
2	1.20 GHz	000001	-3.4 dB	-17 dB	3.9%	111	-28 dB
3	1.24 GHz	000010	-3.7 dB	-18 dB	3.8%	103	-28 dB
4	1.27 GHz	010000	-4.3 dB	-22 dB	3.6%	100	-28 dB
5	1.30 GHz	010001	-4.5 dB	-21 dB	3.7%	96	-29 dB
6	1.32 GHz	010010	-4.7 dB	-23 dB	3.8%	93	-30 dB
7	1.35 GHz	101000	-4.6 dB	-16 dB	3.6%	97	-32 dB
8	1.38 GHz	101001	-4.7 dB	-17 dB	3.9%	92	-29 dB
9	1.40 GHz	101010	-4.8 dB	-18 dB	4.3%	88	-32 dB
10	1.44 GHz	111001	-4.7 dB	-25 dB	4.1%	90	-32 dB
11	1.47 GHz	111010	-4.6 dB	-26 dB	4.0%	92	-31 dB
12	1.50 GHz	111100	-4.4 dB	-25 dB	4.2%	91	-33 dB
13	1.53 GHz	111101	-4.2 dB	-19 dB	4.6%	88	-31 dB
14	1.56 GHz	111110	-4.1 dB	-18 dB	4.7%	86	-32 dB

Better than -28 dB spurious suppression is observed up to 4.0 GHz for all frequency states. This includes second (1.9 GHz), third (2.25 GHz), and fourth (2.8 GHz) spurious mode rejection for all frequency tuning states. Measured passband characteristics are very similar to the previous design without spurious suppression with exception to a slight increase to the insertion loss of each state (approximately 0.7 dB).

## CHAPTER V

### CONCLUSIONS AND FUTURE WORK

#### A. Summary

The main purpose of this thesis is to present the first fully tunable resonant-mode SIW bandpass filter on a planar substrate using PIN diodes and RF MEMS switches. The first part of the thesis deals with the basic theory of SIW in comparison to conventional rectangular waveguides. From this section, a two-pole SIW bandpass fixed filter has been designed and simulated with the following specifications: 2.1 GHz center frequency, 1% fractional bandwidth, and 0.1 dB passband ripple. The dimensions of this filter are then subsequently utilized for the analysis of perturbing vias inside the SIW cavities.

Perturbing via posts with via islands are next placed inside each SIW cavity at the same location with respect to the outer coupling window. A tuning mechanism is realized when connecting/disconnecting the top of the perturbing via posts to/from the top metal layer of the SIW cavities. A disconnected via post/island from the top metal layer of the SIW filter shows little difference in the center frequency (2.1 GHz) compared to the previously designed SIW fixed filter with no perturbing vias present. Moreover, connecting the via island to the top metal layer of the SIW cavity reveals considerable tuning (2.45 GHz). Finding the optimum location of the perturbing via posts/islands inside the SIW cavities to produce the 2.45 GHz tuning state is presented through an empirical analysis of sweeping the via posts along the cavity vertical and

horizontal axes. Proper positioning of additional perturbing vias around the optimum location provides additional frequency states through activating via posts along the *AB* line and *CD* line for course and fine tuning, respectively. Three fabricated SIW filters are presented and characterized to validate the tuning mechanism, yielding three ideal states with a tuning range of 1.9 GHz to 3.0 GHz (45% tuning). Insertion loss and return loss for the fabricated filters measured better than 2.5 dB and 12 dB, respectively with fractional bandwidth ranging from 1.8% to 2.9%. Measured unloaded quality factors for the three states have a range of 221 to 255.

The next part of the thesis implements the tuning methodology to three fully tunable SIW filters utilizing three packaged switches: Philips BAP55L PIN diode, Radant RMSW-100 RF MEMS switch, and OMRON 2SMES-01 MEMS relay. In order to isolate the biasing of the RF switches from the SIW filter, a multi-layer duroid design is implemented utilizing the bottom substrate for the SIW filter and the top substrate for the biasing circuitry. Philips PIN diode SIW tunable filter measured performance yielded six separate frequency tuning states ranging from 1.75 GHz to 2.22 GHz. Insertion loss and return loss for the PIN diode design measured better than 4.4 dB and 15 dB respectively with fractional bandwidth ranging from 2.8% to 3.4%. Measured unloaded quality factors for the PIN diode SIW tunable filter have a range of 105 to 135. Radant MEMS SIW tunable filter measured performance yielded six separate frequency tuning states ranging from 1.65 GHz to 2.10 GHz. Insertion loss and return loss for the Radant MEMS design measured better than 12.4 dB and 15 dB respectively with fractional bandwidth ranging from 2.5% to 3.0%. Measured unloaded quality factors for

the Radant MEMS SIW tunable filter have a range of 44 to 72. Due to high insertion loss, this filter is not suitable for practical applications. Instead, OMRON MEMS SIW tunable filter measured performance yielded fourteen separate frequency tuning states ranging from 1.19 GHz to 1.58 GHz. Insertion loss and return loss for the OMRON MEMS measured better than 4.1 dB and 15 dB respectively with fractional bandwidth ranging from 3.6% to 4.4%. Measured unloaded quality factors for the OMRON MEMS SIW tunable filter tunable filter have a range of 93 to 132. Overall, both the PIN diode and OMRON MEMS RF switches provide very promising results for tuning SIW two-pole bandpass filters.

The last part of the thesis utilizes a simple technique to validate the straightforward integration of planar structures with SIW structures. For enhanced spurious suppression, microstrip low pass filters are designed and placed at both the input and output ends of the microstrip-to-SIW transition regions to the previously designed OMRON MEMS SIW tunable filter. Measured results show a -28 dB rejection of the 2nd, 3rd, and 4th order spurious modes for all fourteen frequency tuning states. With exception to an added 0.7 dB insertion loss, measured frequency state parameters are the same as the previous OMRON MEMS SIW tunable filter with no spurious suppression.

### B. Miniaturized Tunable SIW Filter

A new technique to help reducing the size of SIW filters involve inserting ridge vias inside SIW cavities. Fig. 70 shows a ridge via placed inside the SIW with only one side of the via connected to the top metal layer of the cavity. Whereas the original proposed tunable SIW filter with perturbing vias utilizes inductive loading to increase the center frequency, the SIW cavity with ridge vias creates capacitive loading thereby decreasing the center frequency [26]. This enables for a tunable SIW filter cavity to be originally designed to the dimensions of the highest frequency tuning state instead of the lowest tuning state. Subsequent lower frequency tuning states are then realized with “on-state” ridge vias inside the SIW cavity, thus providing a smaller cavity size compared to standard SIW filters with no ridge vias operating at the same center frequencies [4].

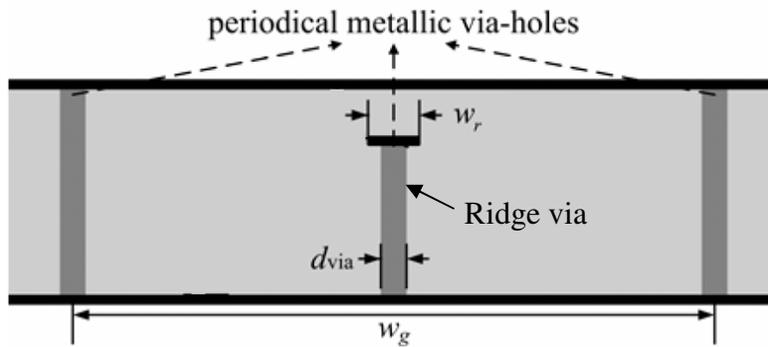


Fig. 70. Simple SIW with perturbing ridge via.

Applying the new ridge via SIW topology to this thesis is achieved through replacing the perturbing via posts of the OMRON SIW tunable filter with ridge vias

along the same  $AB$  and  $CD$  frequency tuning lines. Due to fabrication limitations, a third duroid substrate is required to create the ridge via inside the SIW cavity. All other layout techniques are identical to the previous OMRON tunable SIW filter with the upper wall of the SIW cavity sandwiched between the top DC biasing metal layer and the bottom wall SIW cavity metal layer. Fig. 71 illustrates the layout of the ridge via perturbed OMRON tunable SIW filter.

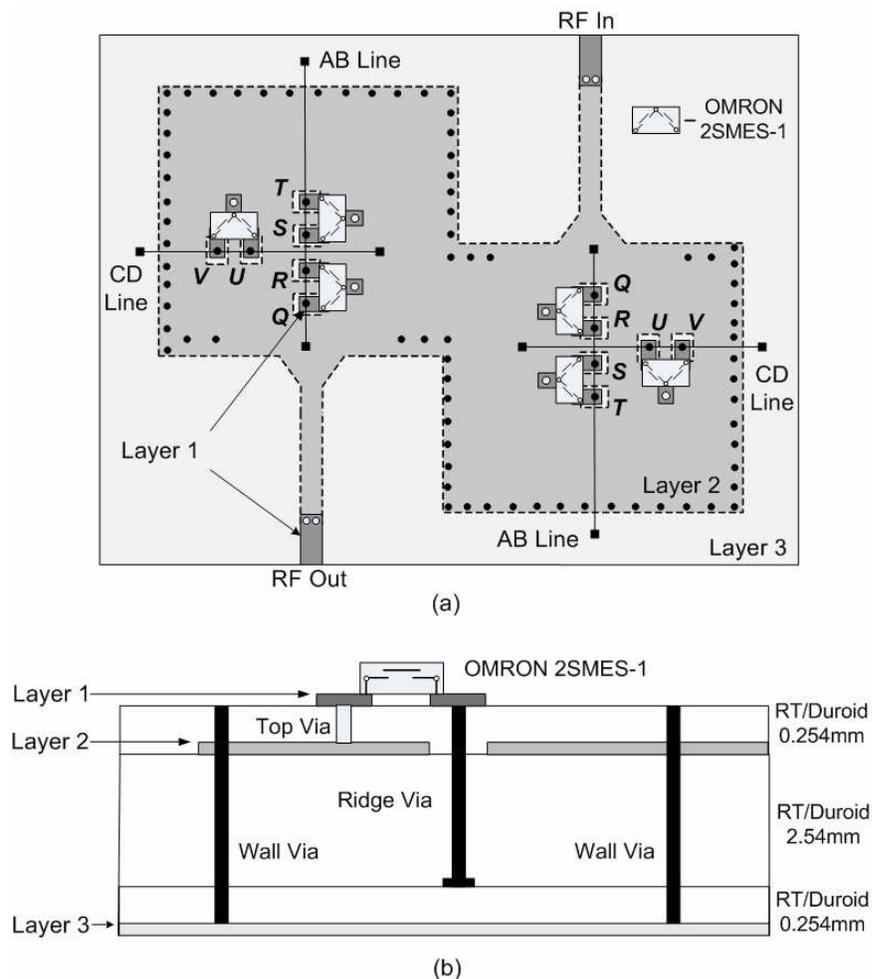


Fig. 71. OMRON MEMS tunable SIW filter layout with perturbing ridge vias.

Dimensions for this tunable filter are re-adjusted to match the lowest frequency tuning state of the previous OMRON MEMS SIW tunable filter (1.37 GHz) in order to compare filter size and tuning capabilities. Fig. 72(a-b) shows the full-wave simulated results with a tuning range of 1.37 GHz to 1.61 GHz.

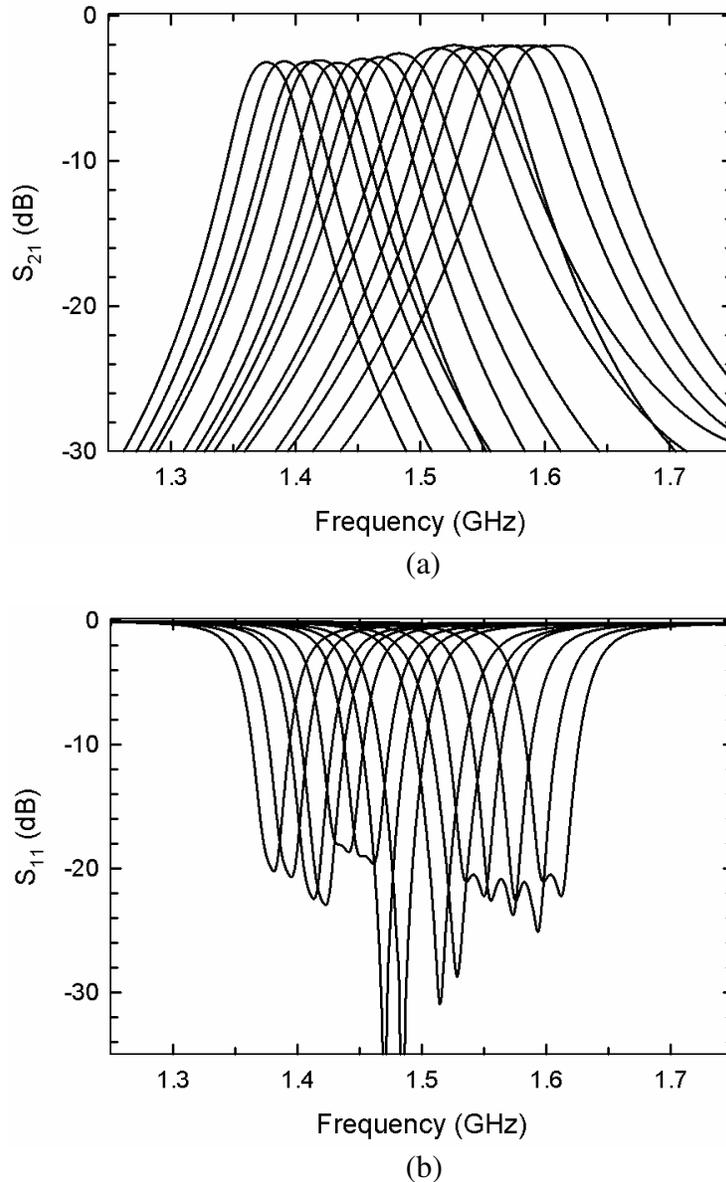


Fig. 72. OMRON MEMS tunable SIW filter with perturbing ridge vias simulated response, (a)  $S_{21}$  and (b)  $S_{11}$ .

Similar to the previous OMRON MEMS design, fourteen states are simulated. The same tuning methodology along the *AB* and *CD* lines is utilized to obtain multiple frequency states. However, in this instance the highest frequency tuning state (1.61 GHz) is achieved from all of the MEMS switches in the up-state position and the lowest frequency tuning state (1.37 GHz) is achieved from all of the MEMS switches in the down-state position. Table XII depicts the full-wave simulation comparison between the ridge via tunable filter and the previous perturbing via tunable filter.

Table XII. OMRON Tunable SIW Filter Comparison of Previous Inductive Loading with Perturbing Via Posts and New Capacitive Loading with Ridge Vias

	<b>Inductive loading w/ perturbing via posts</b>	<b>Capacitive loading w/ ridge vias</b>
<b>OMRON switches per cavity</b>	6	6
<b>Frequency tuning states</b>	14	14
<b>Frequency tuning range</b>	1.37 GHz – 1.78 GHz	1.37 GHz – 1.61 GHz
<b>Unloaded Q factor</b>	106 – 178	90 – 138
<b>FBW</b>	3.9% – 5.0%	4.0% – 4.9%
<b>Insertion loss</b>	2.8 dB	3.7 dB
<b>Filter size</b>	114 mm x 80 mm	88 mm x 62 mm

Given similar fractional bandwidths, insertion loss from the previous OMRON MEMS tunable SIW filter is still around 1 dB better than the new ridge via tunable filter. This is due to the original SIW filter topology utilizing inductive aperture windows for filter coupling. Complimenting inductive perturbing vias with this topology maintains continuity and better loss performance compared to capacitive loading ridge vias [26]. As a result, simulated unloaded quality factors are lower ranging from 90 to 138. Additionally, the tuning range for the ridge via tunable filter is lower. However, overall filter size for the ridge via design is 88 mm x 62 mm versus the original 114 mm x 80 mm (40% size reduction). Depending on design criteria, this new topology may be useful for future projects accepting the trade-off between size and very high performance.

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## Education

- B.S., Electrical Engineering, United States Air Force Academy, 2000
- M.S., Electrical Engineering, Texas A&M University, 2010

## Engineering Profile (2007-2010)

- Microwave passive circuit design including microstrip filters, coplanar waveguides, and substrate integrated waveguide filters
- Spurious suppression and tunable filter research exploiting different RF switch applications with various topologies
- Microelectronics fabrication – Class 100/ISO 5 clean room
  - Texas A&M integrated circuit manufacturing lab instructor
  - Silicon CMOS 10 $\mu$ m technology, contact photolithography, ion-implantation, isotropic etching

## Professional Profile (2000-2007)

- USAF Air Combat Command Electronic Warfare Pilot
  - E-8C JSTARS Aircraft Commander
  - 12<sup>th</sup> Airborne Command and Control Squadron Fight Safety Officer
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