POWER SUPPLY REJECTION IMPROVEMENT TECHNIQUES IN LOW DROP-OUT VOLTAGE REGULATORS

A Thesis

by

SAIKRISHNA GANTA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2010

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
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ABSTRACT

Power Supply Rejection Improvement Techniques in Low Drop-Out Voltage Regulators.

(August 2010)

Saikrishna Ganta, B.E., Osmania University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

Low drop out (LDO) voltage regulators are widely used for post regulating the switching ripples generated by the switched mode power supplies (SMPS). Due to demand for portable applications, industry is pushing for complete system on chip power management solutions. Hence, the switching frequencies of the SMPS are increasing to allow higher level of integration. Therefore, the subsequent post-regulator LDO must have good power supply rejection (PSR) up to switching frequencies of SMPS. Unfortunately, the conventional LDOs have poor PSR at high frequencies. The objective of this research is to develop novel LDO regulators that can achieve good high frequency PSR performance.

In this thesis, two PSR improvement methods are presented. The first method proposes a novel power supply noise-cancelling scheme to improve the PSR of an external-capacitor LDO. The proposed power supply noise-cancelling scheme is designed using adaptive power consumption, thereby not degrading the power efficiency of the LDO. The second method proposes a feed forward ripple cancellation technique to improve the PSR of capacitor-less LDO; also a dynamically powered transient improvement scheme has been proposed. The feed forward ripple cancellation is

designed by reusing the load transient improvement block, thus achieving the improvement in PSR with no additional power consumption.

Both the projects have been designed in TSMC 0.18 μm technology. The first method achieves a PSR of 66 dB up to 1 MHz where as the second method achieves a 55 dB PSR up to 1 MHz.

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I would also like to thank my friends Joon, Mohan, Aravind, Seenu, Karthik, Jusung, Raghavendra, Joselyn, Marvin, Richard, Jason, Mohammed, and Felix for their valuable suggestions and discussions regarding the project.

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CHAPTER I

INTRODUCTION

Extended battery life has become one of the most important design aspects for System on Chip (SoC) designs in portable, battery-powered applications, while power consumption is a concern in high-performance desktop and server applications because of packaging and cooling requirements [1,2]. These aspects lead to breakthrough of power management IC design whose basic functionality is improving the systems power efficiency.

A full on-chip power management unit (PMU) is highly desirable because this saves the valuable pin count, packing costs and bill of material (BOM). With commercial chips overall costs reaching just a few cents, pin count which can increase the packing costs is indeed a valuable commodity. The number of external components such as inductors and capacitors has to be reduced in order to reduce (BOM).

There are two important blocks in a PMU namely DC-DC switched mode power supplies (SMPS) and Low Drop Out (LDO) voltage regulators. Both of these provide the basic functionality of regulating the battery voltage to a constant voltage in-spite of load-line variations. Selecting one among these two regulators is a system dependent choice which includes various considerations such as efficiency, BOM, system complexity, pin count etc [2].

Fig. 1 shows a simple LDO regulator; its main component is its pass device

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This thesis follows the format of *IEEE Journal of Solid State Circuits*.

(MP), which acts like a voltage controlled current source, that is its gate voltage is adjusted according to load variations in order to provide the desired load current at a constant designed output voltage. In order to sense the output voltage a simple negative feedback mechanism is used comprising of the feedback resistors (R_{fb1} and R_{fb2} in Fig. 1) and an error amplifier (EA). The LDO has an output capacitor (C_{out}) which may be just the driven circuit's load capacitance or may have been an added external capacitor to enhance its transient and stability response, adding an external capacitor has the disadvantage of increased pin out.

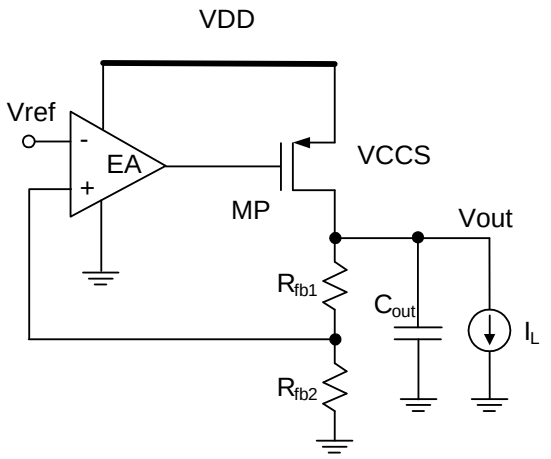

Fig. 1 A simple low drop out regulator

There is an inherent power loss of $(VDD - V_{out}) \times I_L$ in LDOs, where VDD is the input to the LDO i.e. battery voltage, V_{out} is the regulated output voltage and I_L is the load current. This power loss does not account the ground current consumption of LDO. Thus LDOs are power inefficient for large differences in input and output voltages.

Fig. 2 shows a simple model for buck converter, a buck converter is the most commonly used DC-DC switched mode power supply. A buck converter steps down the battery voltage to a lower regulated DC voltage. Controlled switching of the switch S1 results in regulated DC output voltage. A loss-less filter compromising of inductor and capacitor is required, thus SMPS necessitates additional pins and external components which increases BOM and overall cost of the chip. Theoretically a switching regulator is 100% power efficient making it an ideal choice in case of systems requiring very high efficiencies. They unfortunately suffer from the switching noise at their outputs.

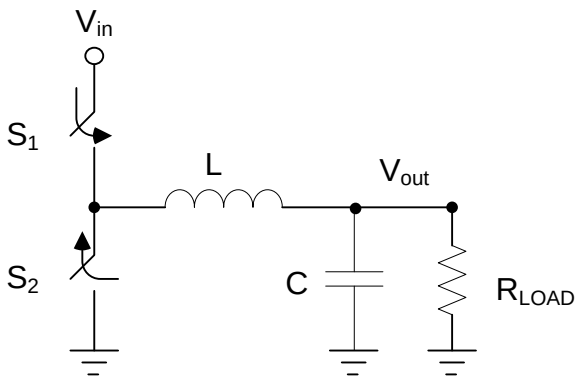

Fig. 2 A simple buck converter model

The advantages and disadvantages of LDOs and SMPS are summarized in Table 1.

Table 1 Comparison of LDOs and SMPS

Parameter	LDO	SMPS
Simplicity	Simple	Complex
External components	Not required *	Required
BOM	Low	High
Pin count	Low	High
Cost	Cheaper	Expensive
Output voltage	Clean	Noisy
Efficiency	Only efficient when VDD is close to V_{OUT}	Very efficient

* Conventionally a LDO was stabilized using an external capacitor; present SoC solutions are external capacitor-less.

After the brief knowledge of the main building blocks of PMU let us take a look in to an integrated PMU for GSM (Global System for Mobile communications) cell phone application which is shown in Fig. 3, it consists of battery charging control unit whose main job is to monitor the battery voltage and take action in case of over voltage. Generally lithium ion batteries are used which provides a voltage in between 3.1 to 4.6V depending on its charging condition.

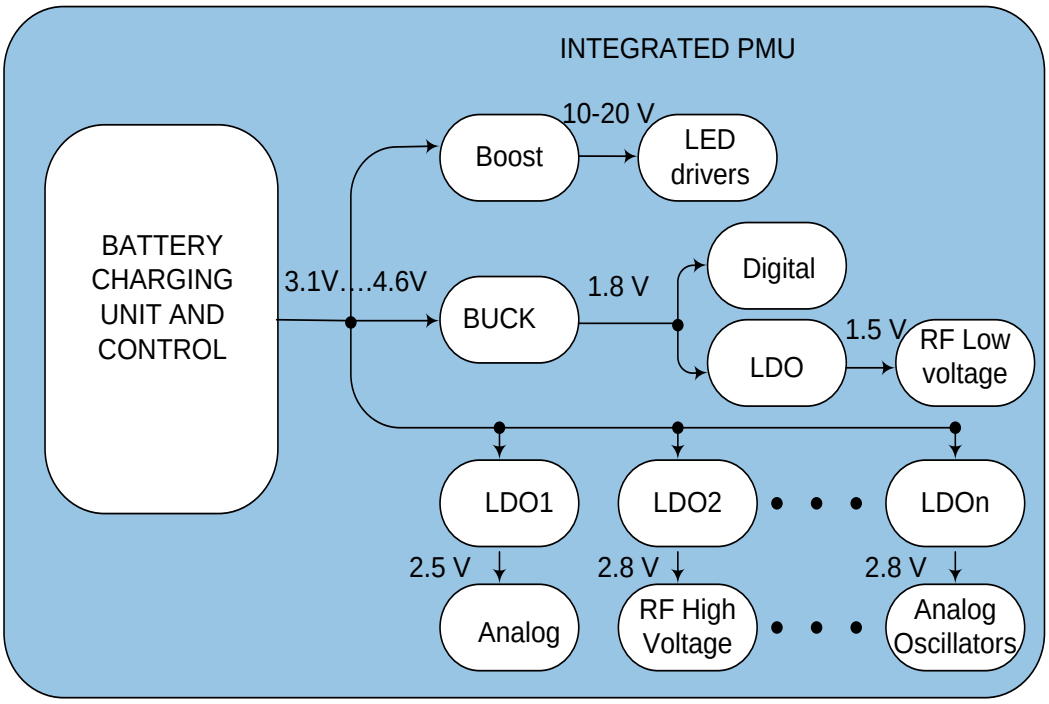

Fig. 3 An integrated power management unit for GSM phones

As shown in Fig. 3 the PMU has multiple tailored made LDOs [2] for different applications. Usually when there is no much difference between Input and output voltages the LDO is directly used after the battery to supply clean regulated voltages. Number of LDOs are being used in a PMU, one of the reason is to avoid cross talk between different systems and also due to different voltage supply requirements. As shown in figure the oscillator uses a separate LDO to avoid its kick-back noise affect other sensitive analog system performances.

As shown in Fig. 3 a buck converter is being used to supply the digital supplies which have relatively larger noise margins. A buck converter efficiently steps down the battery voltage to 1.8V which is used as supply by the digital block. As shown in the

same figure a LDO post regulates the buck converters noisy output to provide a clean 1.5V for the low voltage analog devices, note that directly using a LDO would have been very power inefficient due to the large difference in input and output voltages. A boost converter is also needed in order to drive the LED displays.

It is evident from the above example of PMU that for submicron technologies whose supply voltages are less than 2V the most power efficient method of generating the supply voltages is to step down the battery voltage using a buck converter, this buck converters output has to be cleaned using a LDO voltage regulator. This post regulation achieved by the LDO is credited by its quality called power supply rejection(PSR), this thesis proposes two different architectures for PSR improvement, before going further in to details, understanding of LDOs general specifications is required, some of the relevant LDO characteristics are mentioned in the next section.

I.1 LDO regulator characterization

This section provides with understanding of main LDO characteristics which are dropout voltage, line and load regulation, power supply rejection, current and power efficiencies.

a. Dropout Voltage

Dropout voltage is the minimum voltage difference between input voltage and LDOs output voltage before the pass transistor goes out of saturation. The dropout voltage design also depends on the maximum load current specification, when the load current exceeds the maximum level the pass transistor goes in triode region of operation. For example a LDO with a output voltage of 2.8V and dropout of 200mV with a maximum load current capability of 100mA means that for proper regulation, the input voltage for the LDO should not drop below 3V and the maximum load current cannot exceed 100mAs.

Dropout voltage is inversely proportional to the efficiency of LDO; hence designers strive to reduce the dropout voltage. Dropout voltages in range of 150mV to 500mV are common in CMOS designs, Dropout voltages below 150mVs severely affect the system transient response and hence are rarely designed so.

b. Line regulation

Line regulation is a steady state specification, which is defined as ratio of steady state change in the LDOs output voltage and the steady state change in its input voltage.

$$LNR = \frac{\Delta V_{OUT}}{\Delta V_{DD}} \alpha \frac{1}{A_{LOOP}} \tag{1.1}$$

The line regulation is inversely proportional to its loop gain (A_{LOOP}), thus larger loop gain assures a better line regulation.

c. Load regulation

Load regulation is defined as ratio of steady state change in output voltage with steady state change in load current.

$$LDR = \frac{\Delta V_{OUT}}{\Delta I_L} \approx \frac{r_{ds}}{A_{LOOP}} \tag{1.2}$$

Both line and load regulation can be improved by increasing open loop DC gain of the LDO.

d. Power supply rejection

It is defined as the ability of LDO to reject the variations in its supply voltage. This is similar to line regulation with the difference that this even includes the ac variations in its supply. In fact LNR is equivalent to DC value of PSR.

$$PSR \approx \frac{1}{A_{LOOP}(s)} \tag{1.3}$$

e. Power efficiency

The efficiency of the LDO is determined by its quiescent current consumption and the difference between its input and output voltages. Power efficiency is given by

$$P_{Efficency} = \frac{I_{Load} V_{out}}{(I_{Load} + I_q) V_{DD}} \tag{1.4}$$

Typically the quiescent current of LDO is designed to be less than hundred micro amperes, while the maximum load current can be few hundreds of milliamperes, thus at maximum loading conditions power efficiency is given by

$$P_{Efficency} \approx \frac{V_{out}}{V_{DD}} \tag{1.5}$$

Thus for maximum loading conditions power efficiency is mainly determined by the dropout voltage of LDO.

The fraction given by the following equation is termed as current efficiency

$$C_{Efficency} = \frac{I_{Load}}{I_{Load} + I_q} \tag{1.6}$$

At low or no loading conditions the power efficiency is mainly determined by current efficiency and is particularly important to have a good current efficiency if the device stays in standby mode for a majority of time.

I.2 Thesis organization

The main objective of this thesis is to develop power supply rejection improvement techniques for LDOs. The proposed PSR technique should have the following desirable qualities:

1. It should not affect other system dynamics like transients, stability.
2. It should not affect the system current efficiency, especially at low loading conditions.
3. It should be effective for a large range of load currents.

Chapter II deals with the detailed analysis of PSR in LDOs, which is followed by a proposal of novel power supply noise cancelling technique. Next the proposed solution's implementation details are discussed. Finally extensive post layout simulations are performed to prove the concept. The proposed solution however makes use of an external capacitor for satisfying its stability and transient response requirements. External capacitor requires an additional pin which is a luxury in a PMU, thus the acquired intimate knowledge regarding PSR is utilized in developing a full-on chip LDO which is presented in Chapter III. Due to the absence of external capacitor a novel transient enhancement scheme is proposed, finally simulation results are presented. In the fourth chapter the concluding remarks with scope for future work has been presented.

CHAPTER II

POWER SUPPLY REJECTION IMPROVEMENT IN EXTERNALLY COMPENSATED LDO VOLTAGE REGULATORS

PSR is an important design parameter for LDOs used as post regulators or when used for generating supply for noise sensitive analog blocks. When LDO is used as a post regulator it is expected to clean the switching noise introduced by the DC-DC switching converters, but unfortunately the PSR bandwidth of conventional LDOs is not large enough to reject switching noise introduced by DC-DC switching converters, due to increase in the latter's operating frequencies for higher level of integration [3]. In this chapter the analysis and discussion of the PSR in conventional LDOs is done followed by discussion of state of art PSR implementations, next the proposed solution and its implementation are presented, finally other system design issues such as stability and transient response are discussed.

II.1 PSR analysis

The various paths that affect the PSR are shown in Fig. 4. The error amplifier's (EA) finite PSR (path 1) and channel resistance of pass transistor (r_{ds}, path 2) together with the low-frequency loop gain mainly define the low-frequency PSR. While the low frequency PSR contribution of path (1) can be minimized by designing the error

amplifier [4-6] properly, the effects of the r_{ds} path can only be minimized by increasing the loop gain.

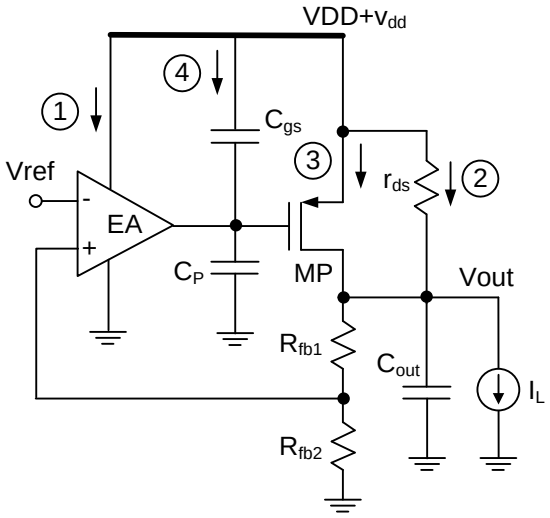

Fig. 4 Input to output ripple paths in conventional LDO

The EA's contribution to high frequency PSR is negligible [7] due to the large value of the parasitic capacitor present at the gate of the pass transistor .The transfer function of supply ripple due to path 1 to output of LDO can be found as following:

$$\frac{V_{out}}{v_{dd\ path1}} = \frac{g_m Z_{out} \dfrac{A_e}{1+\dfrac{s}{\omega_e}}}{1+\dfrac{g_m Z_{out} A_e R_{fb2}}{(R_{fb1}+R_{fb2})(1+\dfrac{s}{\omega_e})}} (PSRR_{EA}) \tag{2.1}$$

where g_m is the transconductance of the pass transistor, Z_{out} is the output impedance of the LDO, A_e and ω_e are the DC gain and the dominant pole of the EA respectively.R_{fb1}

and R_{fb2} are the feedback resistances, $PSRR_{EA}$ is the power supply rejection ratio of the EA and v_{dd} is the power supply ripple.

According to the equation (2.1) the power supply noise due to path (1) at higher frequencies is being filtered by the large parasitic capacitor at the gate of pass transistor and does not appear at the output of LDO. The effect of path (1) on the overall PSR of LDO is shown in Fig. 5.

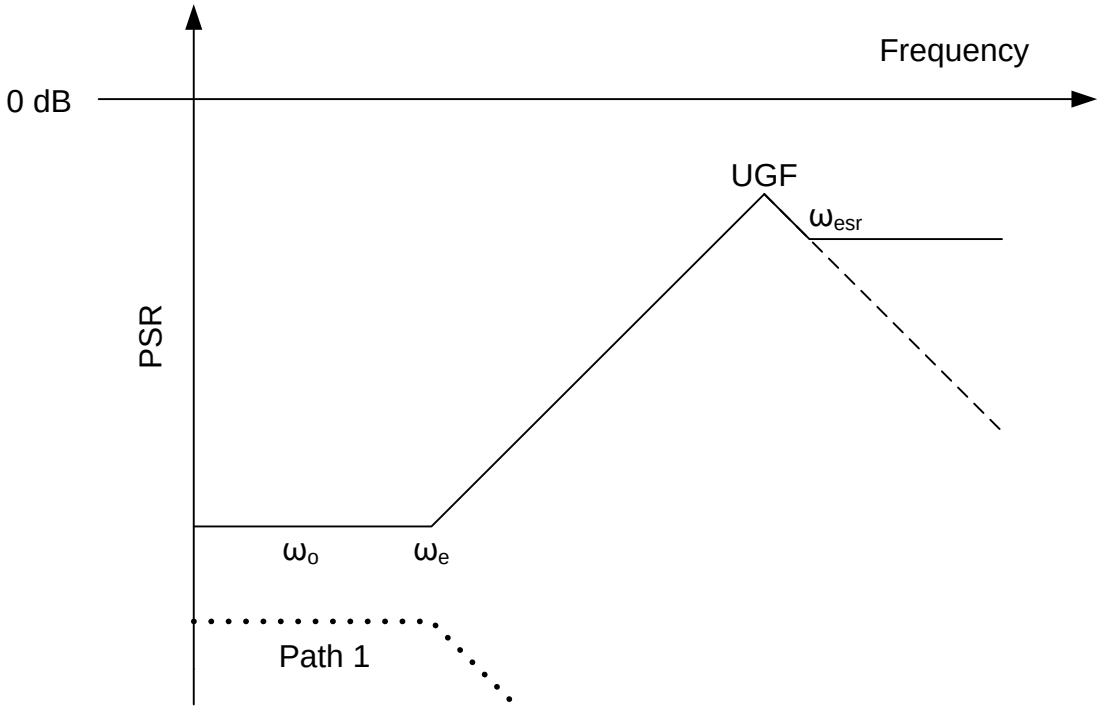

Fig. 5 PSR response across frequency

On the other hand, the PSR contribution due to r_{ds} (path 2) starts to increase beyond the frequency of the pole at the gate of pass transistor (ω_e) due to the loop-gain reduction at high frequencies. The high frequency PSR is severely affected due to the

coupling of supply noise through the gate-source capacitance of the pass transistor (path 4). Considering the circuit operation in open-loop, the high-frequency supply noise at the gate of the pass transistor due to C_{gs} is given by $\left(\frac{C_{gs}}{C_{gs}+C_P}\right)v_{dd}=\alpha v_{dd}$; where v_{dd} is the noise present on the power supply, C_{gs} is the gate-source capacitance of the MP, and C_p is overall parasitic capacitance present at the gate of the pass transistor excluding C_{gs}. As a result, the noise drain current delivered to the load in open loop is given by $(1-\alpha)g_m v_{dd}$, leading to limited rejection to high-frequency noise (g_m is the transconductance of MP).The overall PSR of LDO can be found as

$$\frac{V_{out}}{v_{dd}}=\frac{1+g_m r_{ds}\left[1-\alpha\right]}{1+\frac{r_{ds}}{R_{fb1}+R_{fb2}}+\frac{r_{ds}}{Z_L}+g_m r_{ds}\frac{R_{fb2}}{R_{fb1}+R_{fb2}}\frac{A_e}{1+\frac{s}{\omega_e}}} \tag{2.2}$$

where Z_L is the load impedance without considering the feedback resistances R_{fb1} and R_{fb2}.

Fig. 5 shows the PSR response across frequency of the conventional LDO, the PSR starts degrading at the frequency of the dominant pole of the EA, due to the reduction in loop gain, this degradation continues until the UGF, after the UGF the LDOs output impedance is dominated by the output capacitor, we can consider two possible scenarios:

Case 1.) There is no ESR, ESL associated with the output capacitor

In this case beyond UGF the output impedance is mainly capacitive and this capacitance is going to filter any supply noise present at the output, thus PSR keeps improving with frequency. This scenario is shown by dashed lines in Fig. 5.

Case 2.) The loop is stabilized using R_{ESR} or there is ESR, ESL associated with the output capacitor

In this case the final value of PSR settles to a value given by the equation below

$$\frac{V_{out}}{v_{dd}} = \frac{R_{ESR}}{R_{ESR} + r_{ds}}[1 + (1-\alpha) g_m r_{ds}] \tag{2.3}$$

Thus according to equation (2.3) the parasitic components such as ESR and ESL impede the improvement in PSR at higher frequencies.

In synopsis a wideband EA, along with high loop gain are desired for a wideband PSR response. It is interesting to see that the PSR is unaffected on the occurrence of dominant external pole (ω_o), this is due to the fact that even though the loop gain decreases at 20dB per decade after the occurrence of the dominant output pole, the output capacitor starts filtering the output supply correlated ripple at the same rate and these two effects cancel each other [7].

II.2 Previous academic work

Only a few previous works are available regarding improving PSR in LDO regulators [8-11].

Most of the techniques available in literature try to provide additional isolation between supply and output of LDO as depicted in Fig. 6. For getting additional isolation numerous techniques have been approached, a short description followed by their disadvantages is discussed in following paragraphs.

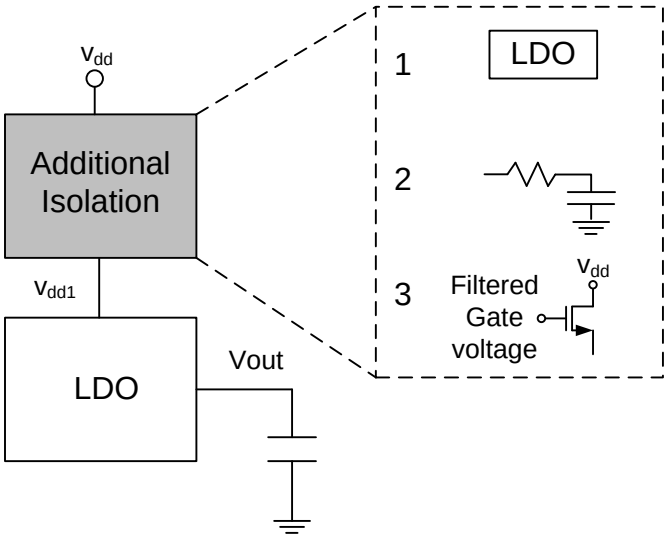

Fig. 6 Previous approaches to get high PSR by having additional isolation

When a LDO is used to get the additional isolation it is costly in terms of power because the total voltage headroom and quiescent current are doubled, added to this it will require twice the expensive silicon real estate.

When an RC filter is used the major disadvantage is the huge voltage drop across the resistor, this voltage drop across the resistor adds with the dropout voltage of the LDO to determine the overall dropout voltage. Thus, this technique increases the total drop out voltage thereby compromising the system efficiency for improved PSR.

Also few techniques employ a NMOS cascode transistor with a clean gate voltage to provide the additional isolation [9, 10]. In order to reduce the dropout voltage a charge pump is required. Also a RC filter is required for cleaning the gate voltage of the cascode transistor; more over this technique provides limited improvement for large load currents due to subsequent decrease of channel resistance of the cascode transistor.

A different approach for obtaining better PSR has been adopted in [8] which is shown in Fig. 7, The main idea is to reproduce the supply ripples on to the gate of pass transistor using a fast Feed-Forward-Amplifier [FFA], thus eliminating any supply noise due to transconductance of pass transistor, also the ripple on the gate is made larger to cancel the additional noise current due to finite channel resistance of pass transistor. Nevertheless due to r_{ds} variation with loading conditions this cancellation technique may not warrant good PSR for a large range of load currents (few 100s of mAs). Also a very large capacitor is used for compensating a relatively low load current in a superior technology, according to previous analysis large output capacitors help in improving high frequency PSR; hence the improvement offered by this technique alone is not very clear.

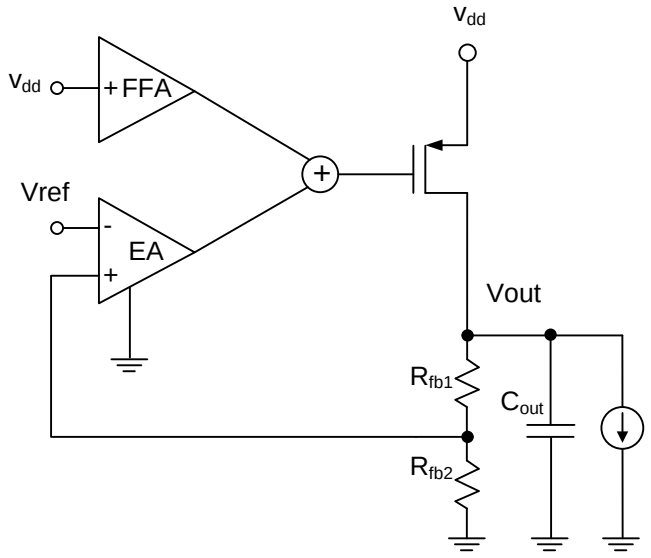

Fig. 7 Feed forward ripple cancellation technique

II.3 Proposed solution

The brief discussion done on the prior state of art techniques to improve PSR enlightened that these techniques suffer from major limitations which may be reduced efficiency, increased complexity or significant increase in silicon area, also these techniques may not warrant good PSR at very large load currents (few 100s of mA's), this large load handling capability is especially required when the LDO is used as post regulator for DC-DC switching converters which have the capability to provide load currents in range of 100's of mA's. In this chapter a LDO with a power supply noise cancelling technique is proposed which enjoys the benefits of being current efficient and maintains the same dropout voltage as a conventional LDO, without significant increase

in silicon area. The LDO has a maximum load handling capability of 200mAs, which confirms its robustness for a large range of load currents.

a. Main idea and block level implementation

If an additional auxiliary branch were added to the output of LDO which can generate a v_{dd} correlated current equal in magnitude and opposite in phase with that in the main branch, the sum of these currents would result in a much smaller v_{dd} correlated current at the output, i.e. superior PSR.

From the previous discussions it is clear that high frequency PSR degradation is due to parameters C_{gs}, C_{gd}, r_{ds} and g_m of the pass transistor hence in order for the auxiliary circuit to get an measure of v_{dd} correlated current we have to make a scaled replica of the pass transistor with the same DC operating conditions (scaling is required in order to maintain power efficiency). This task is accomplished as shown in Fig. 8. A large resistance developed using active circuit and a amplifier in negative feedback are used to maintain the same DC operating conditions for the replica transistor without disturbing the stability of the system. The replica transistor should be well matched with the pass transistor; good matching techniques have to be followed during the layout stage. Theoretically a 10% of mismatch in current sensing still yields a 20 dB PSR improvement over the uncompensated case.

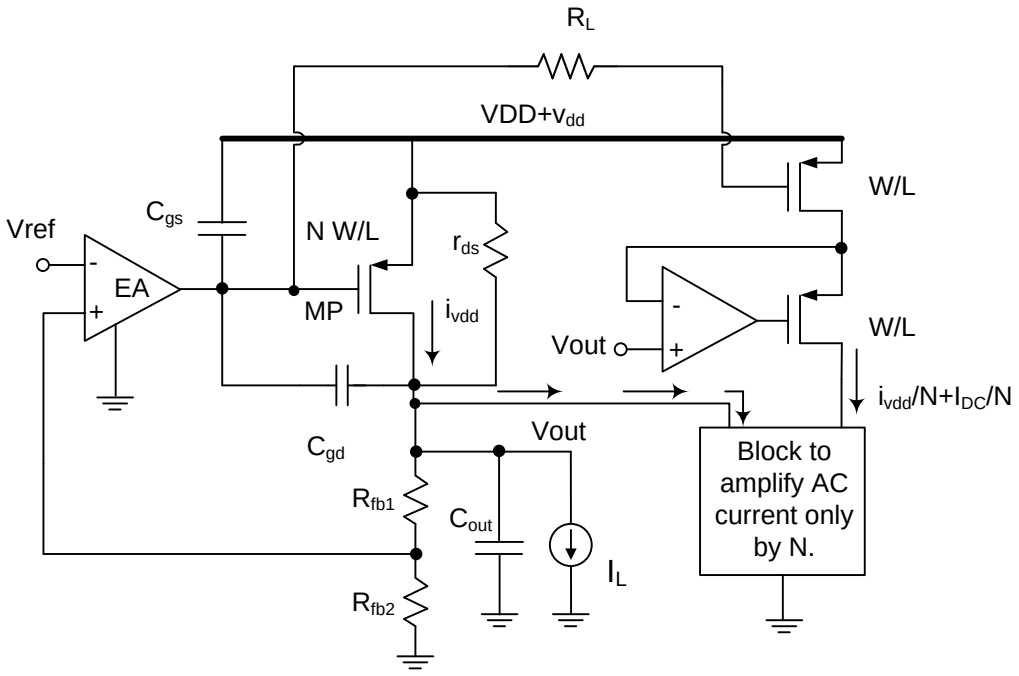

Fig. 8 LDO with the proposed auxiliary PSR enhancer

The power supply noise current being generated by the replica transistor is being scaled according to the scaling factor, hence a block is needed which can accomplish the task of amplifying the noise current by the scaling factor as well as invert its phase. Care must be taken that current amplifying block must be much faster than the intended frequency of improvement.

It should be noted that magnitude of v_{dd} noise current increases with increase in load current, the main reasons being decrease in r_{ds} and increase in the transconductance of the pass transistor; Hence for larger load currents, larger power is required in auxiliary block. Maintaining the same power for all loading conditions would drastically reduce the current efficiency of the system in low loading conditions, hence an adaptive biasing

scheme has been approached where the current consumed by the auxiliary block is a small fraction of its loading conditions. A much more detailed implementation is shown in Fig. 9.

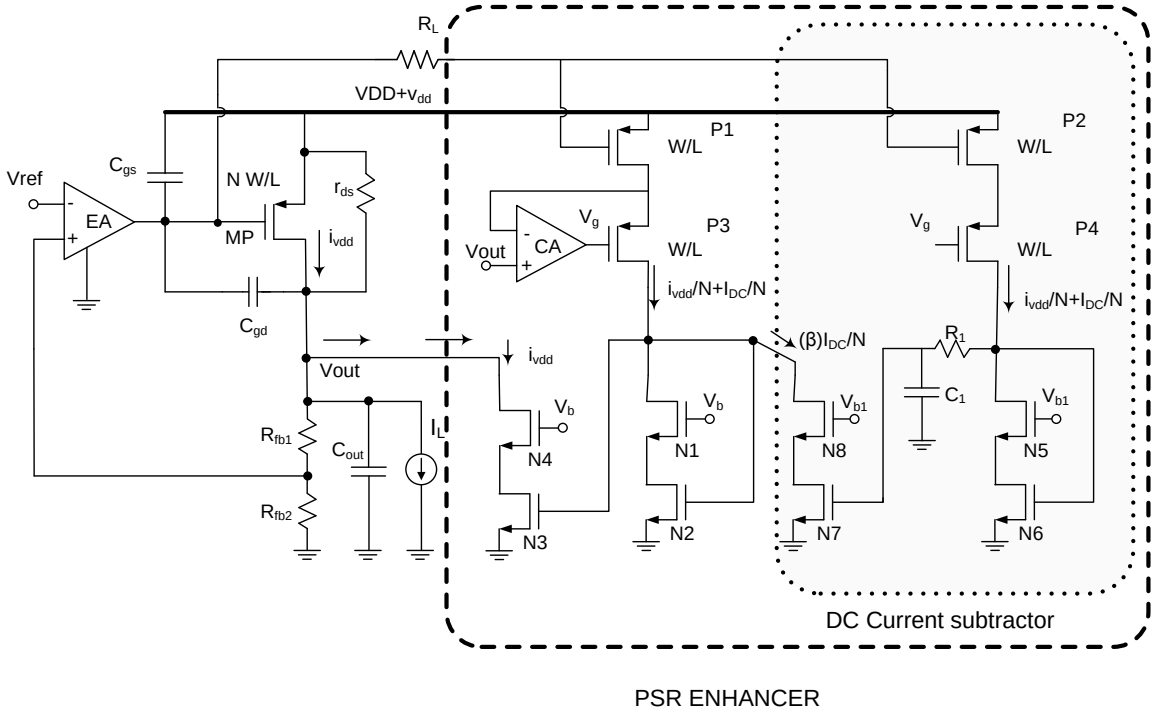

Fig. 9 Circuit level implementation of PSR enhancer for an external capacitor LDO

b. Circuit level implementation

The amplifier copy amplifier (CA) along with transistor P3 forms a negative feedback loop thereby forcing the drain voltages of P1 and P2 equivalent to Vout. CA is a simple two stage amplifier which consumes 10µA of quiescent current; a simple single

stage amplifier cannot be used due to the difficulty in maintaining the transistors in CA and transistor P3 in saturation. The transistor P1 and P2 are now true replicas of the pass transistor, they produce a supply noise current of i_{vdd}/N (in this design N is chosen as 100) where i_{vdd} is the power supply noise current in the pass transistor; also they produce a scaled version of DC current of pass transistor i.e. I_{DC}/N, where I_{DC} is the DC current in pass transistor. After having a good supply noise current sensor the main challenge left is the design of current amplifier which can amplify and invert the AC noise current without amplifying the DC current. The supply noise current amplification with a inverted phase can be achieved by using a simple current mirror with a mirroring ratio of N and the task of amplifying only the AC current is being achieved by using the DC current subtractor block which is depicted in the shaded region in Fig. 9.

The main task of DC current subtractor circuit is to extract most of the DC current from the drain current of transistor P3 so that the DC current in transistors N1, N2 is attenuated, subsequently this attenuated DC current when amplified by the mirroring ratio of N is small enough to have good current efficiency for the system. The DC current subtractor circuit consists of transistors P2, P4, N5-N8 and a low pass filter formed by R1 and C1. P2 along with P4 and CA forms a replica transistor similar to P1, as a result the drain current of P2 consists of scaled AC power supply noise current and scaled DC current of the pass transistor. R1, C1 filters the gate voltage of N6 so as to contain only DC information i.e. DC bias at the gate of N7, there by the drain currents of N7, N8 are DC and does not contain any AC information. The mirroring ratio of N7, N8 with respect to N5, N6 is chosen to be fraction β which is less than one(19/20 in this

design) , and thus $\frac{\beta I_{DC}}{N}$ amount of DC current is extracted from drain current of P3, subsequently the DC current of N1 and N2 is $\frac{(1-\beta)I_{DC}}{N}$,but the AC current remains intact as i_{vdd}/N. The mirroring ratio between N3, N4 with respect to N1, N2 is 100; Hence the drain current of N4 has a DC current of $(1-\beta)I_{DC}$, and has an AC current of i_{vdd}, this AC current cancels the power supply noise current in main branch thereby giving improved PSR.

Note that the location of filters pole in the subtractor circuit is very important; the subtractor circuit starts to stop subtracting the current at the frequency of filters pole. Since the PSR of the main loop start degrading at the frequency of the dominant pole of EA, we would like to stop subtracting current from drain of P3 around the frequency of EA's dominant pole.

The total DC current in the N3, N4 is given by $(1-\beta)I_{DC}$, which in this design is 5% of the total load current; thus the factor β determines the amount of DC current in N3, N4. The factor β is being selected based on peak magnitude of i_{vdd} current(the peak i_{vdd} current varies with magnitude of AC ripple present on the supply, a 50mV peak to peak ripple has be taken in to design consideration), the DC quiescent current has to be larger than this peak to peak AC current. Also if the magnitude of AC ripple present on the supply is smaller; the peak magnitude of i_{vdd} current is lesser, thereby lesser amount of DC current can be used in N3,N4 subsequently increasing the efficiency of the LDO.

c. Bias generation for the cascode transistors

The current amplifiers used in the PSR enhancer block need to have accurate current gains, hence cascode current mirrors are used, careful gate bias generation for the cascode transistors is needed due to varying load current conditions. Varying load currents require varying gate bias voltages for the cascode transistors in order to maintain the transistors in saturation for all loading conditions.

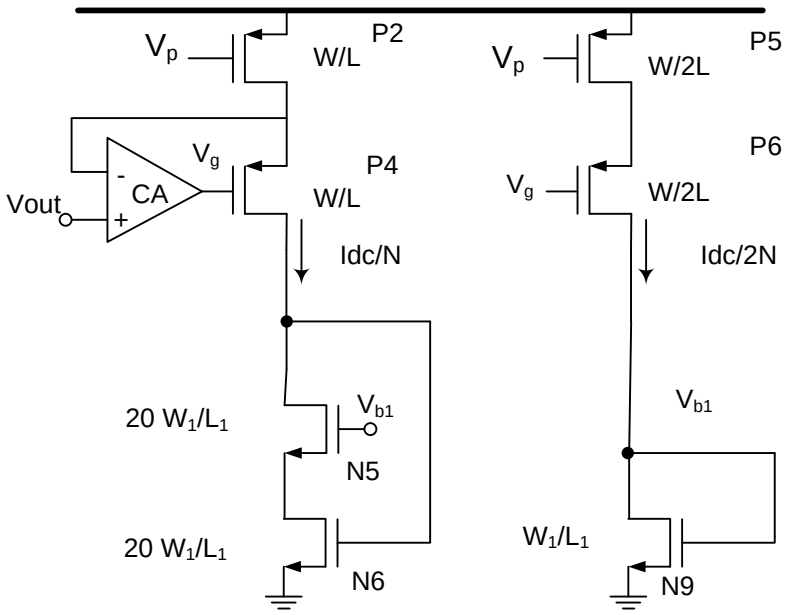

Fig. 10 Bias generation for the cascode transistors in PSR enhancer block

An adaptive biasing as shown in Fig. 10 has been employed, in which an additional replica transistor P5 is used and its drain current is forced in to a diode connected transistor N9.

N9 is scaled down 20 times as compared to N5 and N6, and replicas P5, P6 are 2 times scaled down as compared to the replica transistors P2 and P4, thus P5, P6 has half the DC current compared to P2, P4.

For the case $V_{DS6} = V_{DSAT6}$

V_{b1} must be greater than $V_{GS5}+V_{DSAT6} = V_{t5}+V_{DSAT5}+V_{DSAT6.}$

and $V_{GS9}= V_{b1}= V_{t9} + \sqrt{\frac{2}{\mu_n C_{ox}} \frac{L_1}{W_1} \frac{I_{dc}}{2N}}$

where V_{DS6} and V_{DSAT6} are the drain-source and overdrive voltage of N6 respectively, V_{GS5} ,V_{DSAT5} , V_{t5} are the gate-source, overdrive and threshold voltages of N5 respectively, and V_{GS9} and V_{t9} are the gate-source and threshold voltages of N9 respectively. Due to the scaling of the current and aspect ratio the V_{DSAT} of N9 is $\sqrt{10}$ times V_{DSAT} of N5, N6; which is 3.1 times ($V_{DSAT5, 6}$). The additional $1.1V_{DSAT5, 6}$ takes care of the increased threshold voltage of N5 due to body effect. A similar technique is used to generate V_b.

d. Error amplifier design

The error amplifier has to be designed to yield the desired minimum loop gain while considering other important system requirements like stability, PSR and transient response [12].

The design requirements for an error amplifier are:

1. High DC gain to ensure sufficient DC gain for all loading conditions, having high DC gain for the error amplifier is especially important because for large current loading conditions the pass transistor contributes negligible gain.
2. Low output impedance for pushing the pole at the gate of pass transistor to higher frequencies.
3. The internal poles of the error amplifier must be located at much higher frequencies that the UGF.
4. Error amplifier should not degrade the DC PSR.

The requirement of high DC gain together with low output impedance prohibits the error amplifier implementation using single stage cascode structures. Hence a two stage error amplifier has been chosen to ensure a minimum open loop gain of 65dB. The error amplifier gain is decided to be greater than 60dB. The two stage error amplifier used in this project is shown in Fig. 11. The first stage burns 10μA quiescent current, while the second stage burns a quiescent current of 20μA. Larger quiescent current is chosen in the second stage due to the slewing considerations at the gate of the pass transistor. The pole at the output of EAs first stage is placed at a frequency of 20MHz, while the maximum unity gain frequency of the LDO is 6.8 MHz, thus the EAs non dominant poles does not significantly affect the stability of the overall LDO.

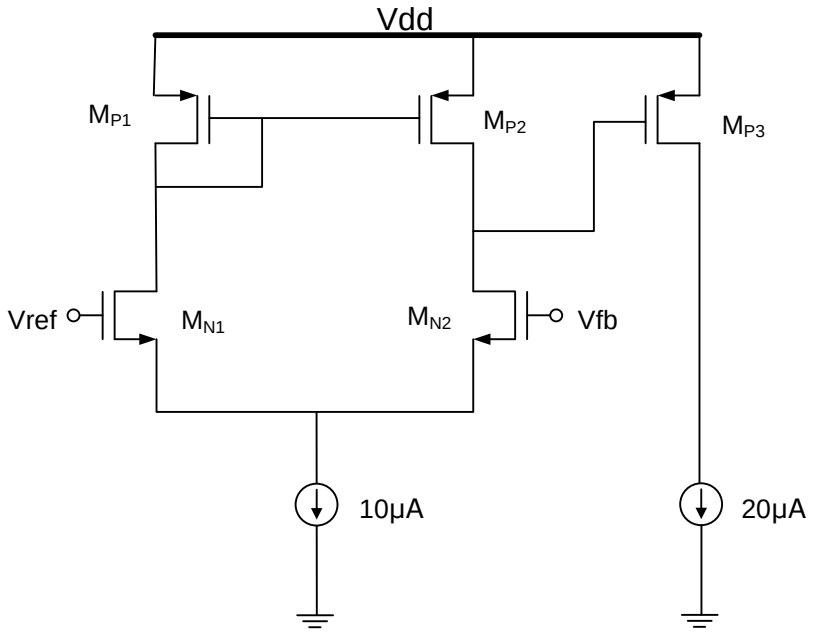

Fig. 11 Schematic of the error amplifier

Table 2 Error amplifier circuit parameters

Transistor	Width(μm)	Length(μm)	Current(μA)
M_{N1}	4	0.72	5
M_{N2}	4	0.72	5
M_{P1}	3	0.18	5
M_{P2}	3	0.18	5
M_{P3}	12	0.18	20

e. The design of error amplifier for high DC PSR

The LDO regulators essentially make use of PMOS transistors in order to satisfy the low drop out requirements. The gain from the source (i.e. supply) to the output of LDO is $g_m r_{ds}$ (where g_m and r_{ds} are the transconductance and channel resistance of the

pass transistor respectively) this causes additional supply noise, the same amount of gain but in opposite phase is obtained from the gate of the pass transistor to its output; hence if we design an error amplifier such that it can reproduce a supply correlated ripple at the gate of pass transistor, there will be no noise conduction through the transconductance of the pass transistor [4-6]. The error amplifier is thereby designed so as to reproduce a supply correlated ripple at the gate of the pass transistor in open loop. The error amplifiers circuit parameters are shown in Table 2. Fig. 12 shows the small signal model for PSR of EA's first stage which has been obtained by grounding the two inputs of the amplifier and applying a small signal ripple on the supply, this analysis has been adopted from [4].

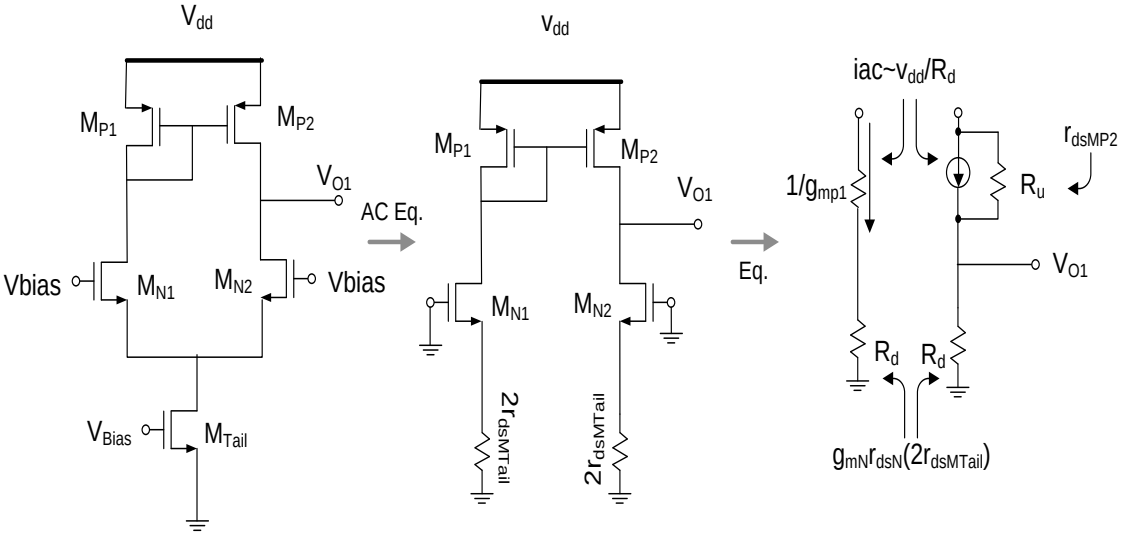

Fig. 12 PSR small signal model of error amplifier's first stage

Because both the transistors MN1 and MN2 are at same gate voltage they are broken in to their common mode half circuit as shown in Fig. 12.

Also the degenerated transistors can be replaced by their degenerated equivalent resistance of R_d which is $g_{mN}r_{dsN}(2r_{dsMTail})$, where g_{mN} and r_{dsN} is the transconductance and channel resistance of the input transistors, $r_{dsMTail}$ is the channel resistance of the current mirror. R_u is the channel resistance of M_{P2}. The supply correlated current produced in the left hand side branch is given by

$$iac = \frac{v_{dd}}{\frac{1}{g_{mp1}} + R_d} \approx \frac{v_{dd}}{R_d} \tag{2.4}$$

This current is being mirrored in to right hand side branch due to the current mirror pair M_{P1}, M_{P2} the total supply ripple at the output of first stage of error amplifier is given by

$$v_{o1} = iac\left(R_u \,||\, R_d\right) + v_{dd}\left(\frac{R_d}{R_d + R_u}\right) \approx v_{dd}\left(\frac{R_u}{R_d + R_u}\right) + v_{dd}\left(\frac{R_d}{R_d + R_u}\right) = v_{dd} \tag{2.5}$$

Now we proceed to the second stage of error amplifier which is shown in Fig. 13.

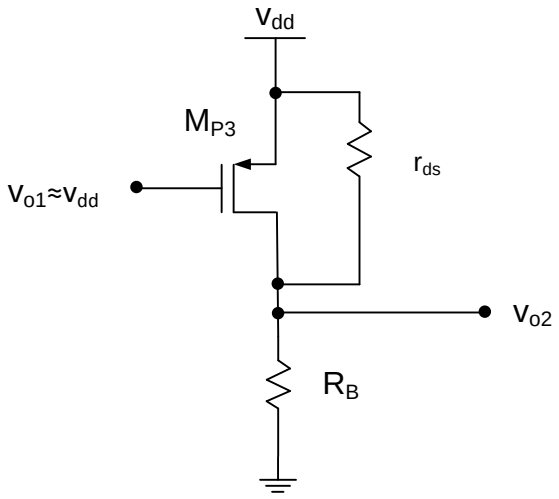

Fig. 13 PSR small signal model for the second stage of error amplifier

The output of the EAs first stage v_{01} has same ripple as that of supply at low frequencies according to equation (2.5), hence there is no current due to transconductance of transistor M_{P3}, and hence the supply noise at the second stage of error amplifier is given by

$$v_{o2} = v_{dd}\left(\frac{R_B}{R_B + r_{ds}}\right) \tag{2.6}$$

The transistor MP3 is designed with minimum channel length of .18µm where as the current source has a channel length of 1.2µm, hence $R_B >> r_{ds}$

Therefore equation (2.6) modifies as follows

$$v_{o2} = v_{dd}\left(\frac{R_B}{R_B + r_{ds}}\right) \approx v_{dd} \tag{2.7}$$

Thus as discussed the error amplifier is designed to reproduce supply correlated ripple at the gate of pass transistor, and thereby resulting in larger DC PSR.

f. Limitations and advantages of this scheme

Speed of current amplifier: The noise cancellation scheme is limited by the speed of the current amplifier used; the current amplifier has a parasitic pole at 2MHz for a loading condition of 1mA. In order to push this pole to much higher frequencies we have to burn more current which will reduce the current efficiency of the overall LDO; a point worth mentioning is this pole is adaptive to loading conditions and moves to higher frequencies for larger loading conditions.

Adaptive power consumption: The design of the auxiliary block is such that it does not significantly degrade the current efficiency of the overall LDO, this is because the auxiliary block consumes power adaptively, i.e. for no load conditions the auxiliary block consumes almost zero amperes of quiescent current, and in fact the auxiliary block consumes 7.5% of the load current.

The power efficiency of the LDO is given by

$$Efficency = \frac{V_{out}.I_{LOAD}}{V_{in}.(I_{GND} + I_{LOAD})} \tag{2.8}$$

Hence for the uncompensated case which has an V_{in} of 1.8V and gives a regulated output of 1.6V and has a quiescent current consumption of 30μAs, the power efficiency for a load of 200mAs is given by

$$Efficency \approx \frac{V_{out}}{V_{in}} = 88.88\% \tag{2.9}$$

In the same conditions the power efficiency for the PSR compensated LDO is

$$Efficency \approx \frac{V_{out}.I_{LOAD}}{V_{in}.(I_{LOAD}+I_{AUXILIARY})} = 82.68\% \quad (2.10)$$

Hence the system does not degrade the power efficiency considerably.

Also since the replicas are $\frac{1}{100}$ fraction of the main pass transistor, they don't occupy significant silicon area, although there is an additional requirement of 550KΩ resistor and 4pF capacitance.

The main advantage of this noise cancelling scheme is the ability to cancel the noise current for a wide range of current starting from 0mA to 200mA, this attribute is required to minimize the total number of LDOs following a DC-DC switching converter.

II.4 Stability in LDOs

Conventionally linear regulators have been high dropout devices, where dropout refers to minimum voltage difference between the unregulated supply and regulated output voltage. The pass transistor in a HDO is usually a NMOS or NPN transistor, they have reduced output impedance due to the source follower or emitter follower configuration, and hence HDOs are stable for all loading conditions [12]. HDOs do not require a large output capacitance to ensure a stable frequency response. For battery operated (portable applications) HDOs are not preferred due to their poor efficiencies. Minimum power lost by a regulator depends on product of dropout voltage and sum of load and quiescent currents. Hence the present design trend is towards LDOs.

LDOs have higher power efficiency at the expense of potential instability [12]. The reasons for instability are due to the following reasons:

1. The pass transistor used for a LDO is a PMOS transistor and its drain impedance is inversely proportional to the load current, and is particularly high for low load currents, this impedance with the large external capacitance causes a load dependent low frequency pole.
2. In order to achieve a low drop out voltage while keeping the pass transistor in saturation the pass transistor size is made very large, this increases the gate capacitance of the pass transistor, this capacitance along with the huge output impedance of the error amplifier is responsible for another low frequency pole. Due to the gate-drain capacitance [$C_{gd]}$ which forms a miller capacitor with the pass transistors, the pole at the gate of the pass transistor is load dependent but is less sensitive than the output pole.
3. Also the error amplifier is responsible for at least two more high frequency poles, the input capacitance of the error amplifier along with feedback resistors are responsible for an additional high frequency pole. These parasitic poles have to be designed such that they are far away from the unity gain frequency of the LDO.
4. A right hand zero is also present due to the large C_{gd} of the pass transistor. This has to be placed above the unity gain frequency for all loading conditions.

Due to the presence of two dominant low frequency poles the system may be potentially unstable; hence a zero must be introduced to compensate the phase

contribution of one pole [4]. A resistor in series with the large output capacitor gives the required left hand side zero, the zero must be placed optimally, assuring the stability for all loading conditions. The worst case phase margin occurs for two conditions:

1. For small load currents (very low frequency output pole), if the zero is located at very high frequencies.
2. For large load currents the open loop unity gain frequency increases and the parasitic poles start playing a more important role.

Keeping all these conditions in mind the zero is placed just beyond the UGF for the no load condition so as to ensure a minimum of 50 degrees phase margin for all loading conditions, placing the zero at a lower frequency would have improved the phase margin for this loading condition but would have increased the UGF for the full load condition and consequently degrading its phase margin due to the role played by the non-dominant poles. The expected gain vs frequency plot is shown in Fig. 14.

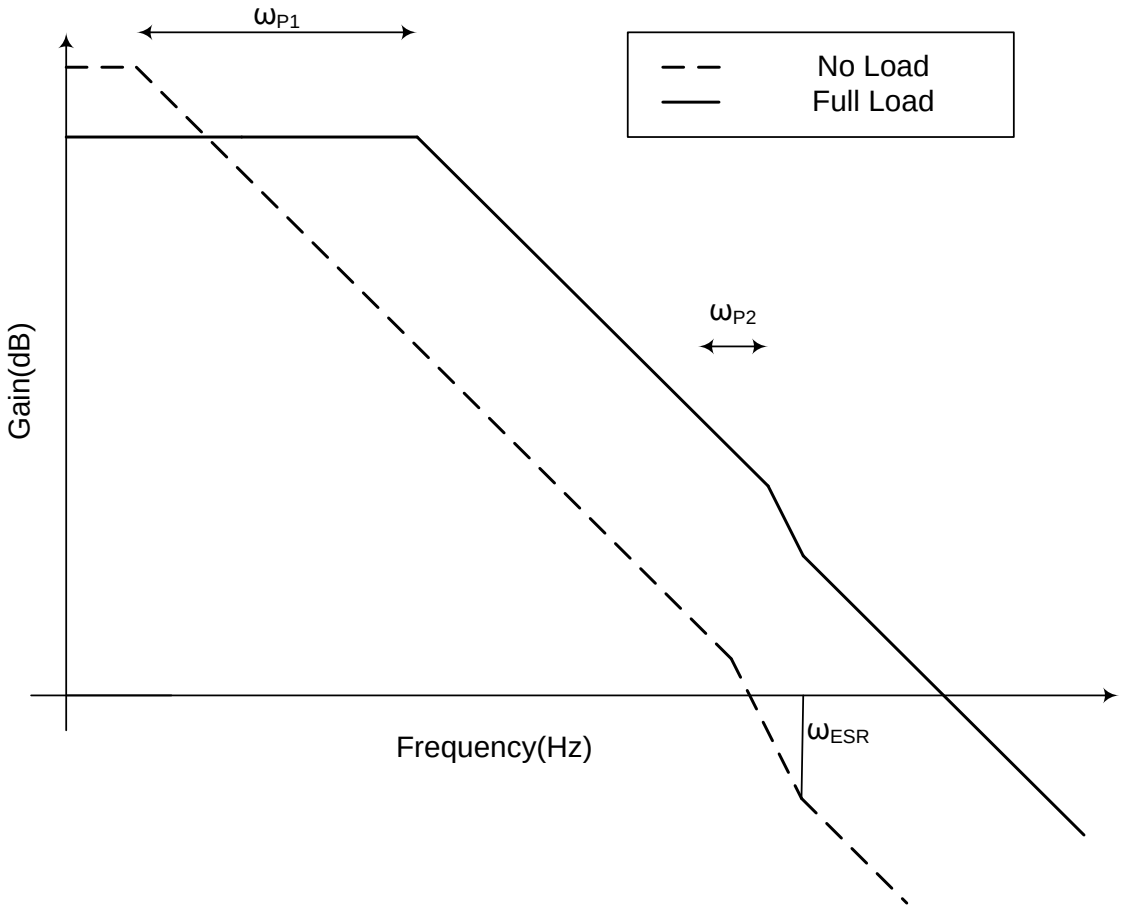

Fig. 14 Expected gain vs. frequency plot

The major disadvantages in stabilizing the LDO using an ESR generated zero, is an additional transient voltage droop due to the introduction of ESR. But it will be shown later in this chapter that the transient droop is less than 35mV, thanks to large output capacitor (2.2uF) and good technology (TSMC 0.18uM).

II.5 Stability of proposed LDO

The stability of the LDO is uncompromised by addition of the auxiliary block if some precautions are taken. The gate of the pass transistor has the main loops AC feedback information, if we tap the gate voltage directly without filtering it, the auxiliary block will cancel the high frequency feedback information, this is due to the fact that the auxiliary block at high frequencies has equal magnitude and opposite phase transconductance as compared to the pass transistor, subsequently the system may run in to instability. To avoid this from occurring we have to tap only DC gate voltage of the pass transistor to the gate of the replica, i.e. low pass filter the pass transistors gate voltage before we use it as gate voltage for the replica circuits, precaution must be taken that the low pass filter added should not contain any added shunt capacitance, i.e. the low pass filters shunt capacitance should only be the parasitic gate capacitance of the replica circuits, this is essential for the replica to have a correct measure of the supply noise due to path 4 (in Fig. 4). The second condition is that the this filter pole has to placed at much lower frequencies than the DC current subtractors filter pole, because the auxiliary block starts to amplify AC current after the subtractors filter pole, the main loop's feedback information tapped from the gate of pass transistor to replicas gate must be well attenuated before the AC amplification starts in order to avoid any high frequency AC feedback information cancellation. The subtractors filter pole is located at a frequency of 75KHz, hence the gate filters pole has to be as low as 1KHz to 10KHz range, the parasitic capacitance of the replica circuits is 2pFs, thus the resistance to be

used should be above 7.5 MΩs. The resistance is being generated using the active circuit shown in Fig. 15.

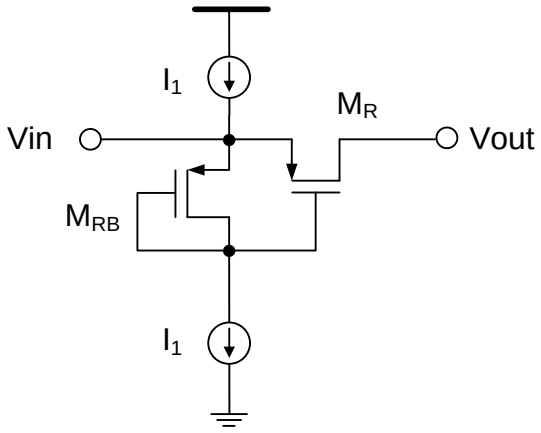

Fig. 15 Active resistance

It consists of the transistor M_R in triode region, with its gate source voltage being well controlled by the V_{GS} of diode connected transistor M_{RB}. A direct triode transistor cannot be used because of variation of the resistance with the large gate voltage variations of pass transistor. If the transistor M_{RB} is forced in to sub-threshold region of operation by biasing it with currents less than 0.5μA, the configuration can achieve very large resistances, the resistance obtained in this project is 70 MΩs, thereby the filter pole is located around 1KHz.

II.6 Post layout simulation results and discussion

a. Open loop AC response

Simulation results for the gain and phase response vs. frequency for the worst cases i.e. for a load current of 100uA and 200mA are shown in Fig. 16 and Fig. 17, the gain plots shows the variation of gain and UGF with load currents. The gain varies from 79dB to 90dB while the UGF varies from 500 KHz to 6.8 MHz, the LDO is stabilized using a zero generated by the R_{ESR} of the capacitor, and the zero was placed at a frequency of 720 KHz.

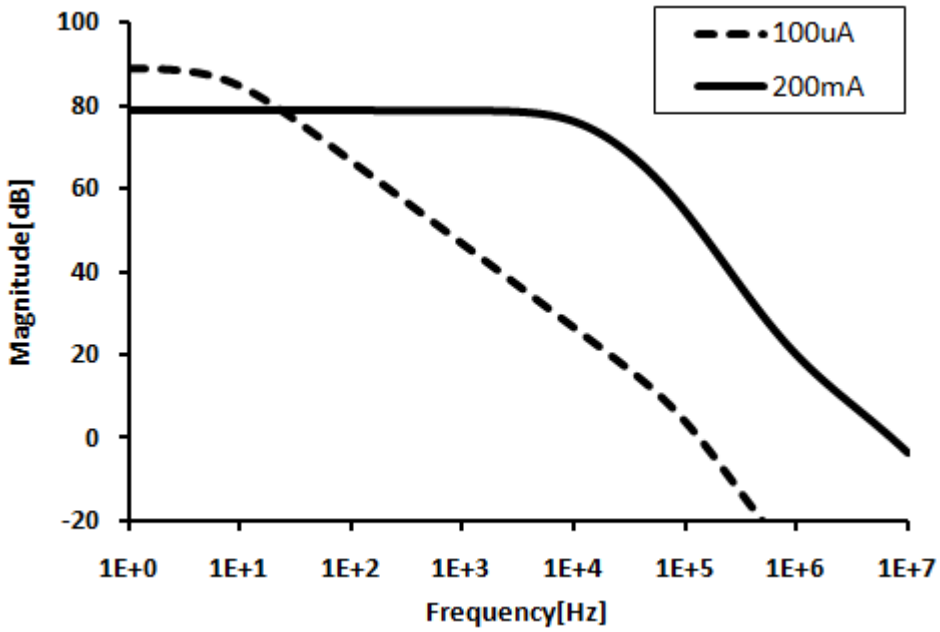

Fig. 16 Magnitude response vs. frequency for the proposed LDO

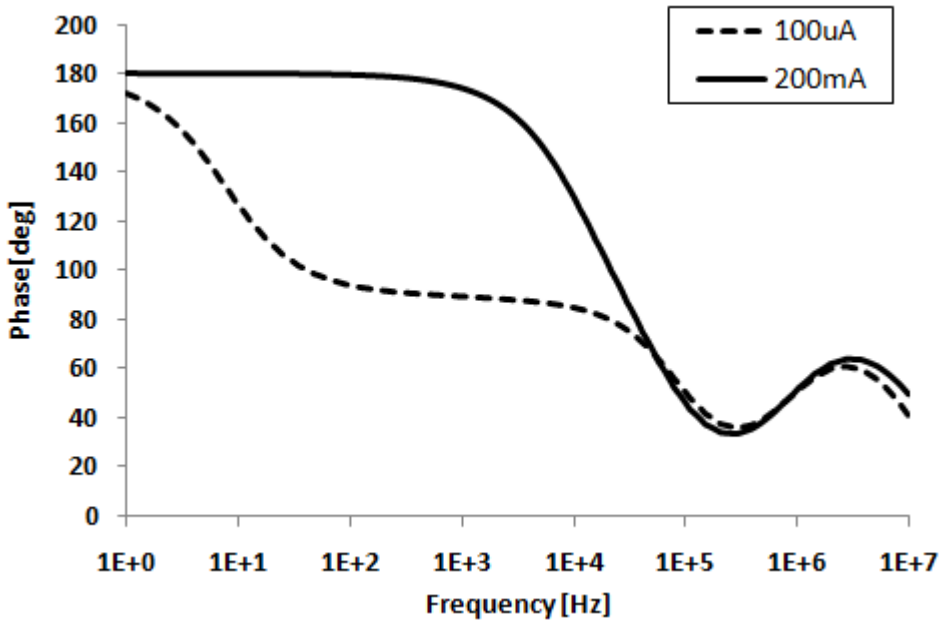

Fig. 17 Phase response vs. frequency for the proposed LDO

The phase margin of the LDO with variation of the load currents is shown in Fig. 18, the minimum phase margin occurs for load currents of 100uA and 200mA. In the case of 100uAs as the zero is located outside its UGF thereby not able to completely compensate for the negative phase of the dominant poles and for 200mA case the zero is located well within the UGF thereby increasing its UGF further and the parasitic of the EA start playing a major role. Nevertheless the phase margin is better than 55 degrees for all loading conditions.

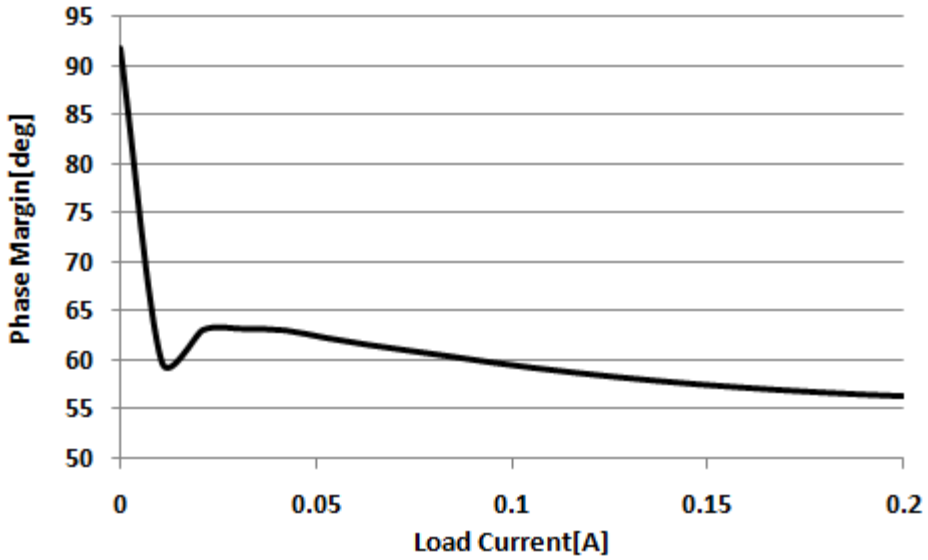

Fig. 18 Phase margin for different load currents

The effect of the auxiliary block on the stability, gain and phase can be analyzed from Fig. 19 and Fig. 20, it can be seen that the auxiliary block reduces the DC gain by 1dB while not affecting the stability.

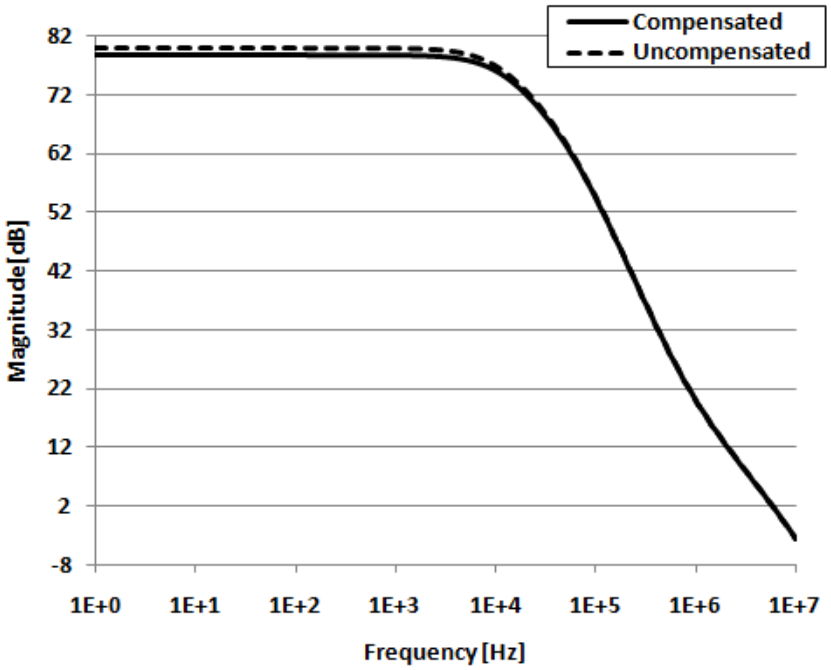

Fig. 19 Comparison of magnitude vs. frequency with and without the auxiliary block

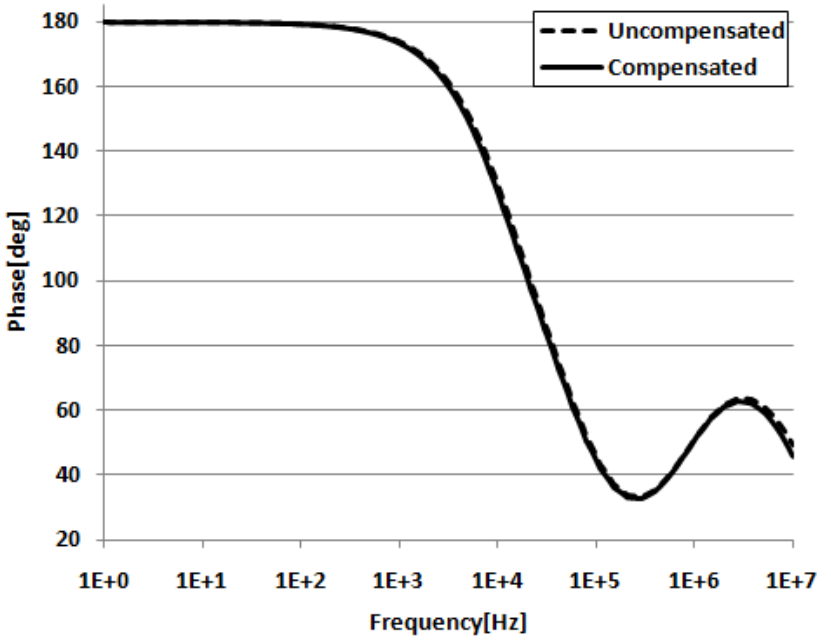

Fig. 20 Comparison of phase vs. frequency with and without the auxiliary block

b. Load transient response

An important specification in LDO regulators is the maximum allowable output voltage variation for a full range transient load current step, also known as transient voltage droop [4]. The specification of transient voltage droop is very stringent for LDOs serving sensitive analog blocks, large voltage drops may cause catastrophic functioning of the analog blocks and in extreme cases may even cause the analog blocks to switch off. The transient voltage droops are much more intense in "external capacitor-less" architecture, than the LDO's which have a huge external capacitor at its output, because the instance load current (I_{LOAD}) is being demanded, the output capacitor (C_o) has to serve this demanded current before the loop has a chance to compensate it due to its finite bandwidth [4]

$$\Delta V_t = \frac{I_{LOAD}}{C_O}\Delta t1 + \Delta V_{ESR} \tag{2.11}$$

where ΔV_t is the transient voltage droop, $\Delta t1$ is the time taken by the loop to respond and ΔV_{ESR} is the voltage droop caused by the ESR (R_{ESR}) associated with the output capacitor. From the equation (2.11) it is clear that larger capacitor at the output of the LDO helps in obtaining lesser transient voltage droops. The proposed LDO's transient response to a positive load current transition from 0-200mA with a rise time of 10nS is shown in Fig. 21.

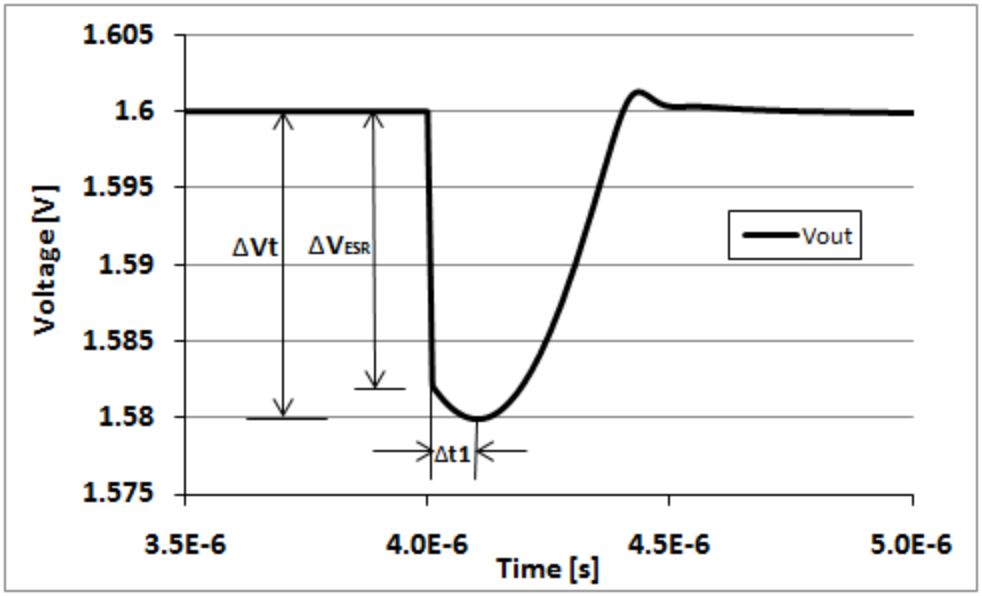

Fig. 21 Transient response of the LDO when current pulses from 0 to 200mA at 10nS rise time

As seen in Fig. 21 when there is a sudden load current demand, there is an instantaneous output voltage droop due to the ESR resistance associated with the capacitor; this is due to the fact that at very high frequencies the impedance of the capacitor is dominated by its ESR resistance, the ESR associated with the output capacitor is 100mΩ hence we expect a voltage droop of

$$\Delta V_{ESR} = I_{Load} * R_{ESR} = (200mA)*(100m\Omega) = 20mV \quad (2.12)$$

After the voltage droop due to R_{ESR} there is additional droop due to the finite bandwidth of the LDO, the delay Δt1 in equation (2.11) is given as

$$\Delta t1 = \frac{1}{B.W} + t_{S.R} \quad (2.13)$$

where B.W is the closed loop bandwidth of the LDO and $t_{S.R}$ is the additional loop delay caused due to the slew rate at the gate of the pass transistor.

Usually due to the presence of pass transistor's large gate parasitic capacitance the time delay in reaction of loop (Δt1) is limited by the slew rate at the gate of the pass transistor which is given by

$$t_{S.R} = C_{GATE} \frac{\Delta V_g}{I_b} \tag{2.14}$$

where C_{GATE} is the total parasitic capacitance present at the gate of the pass transistor, ΔV_g is the required voltage variation at the gate of pass transistor and I_b is the bias current in the second stage of the pass transistor. In the proposed LDO the second stage of the EA burns two-thirds of the total quiescent current of the EA to alleviate the limitation of slew rate at pass transistors gate.

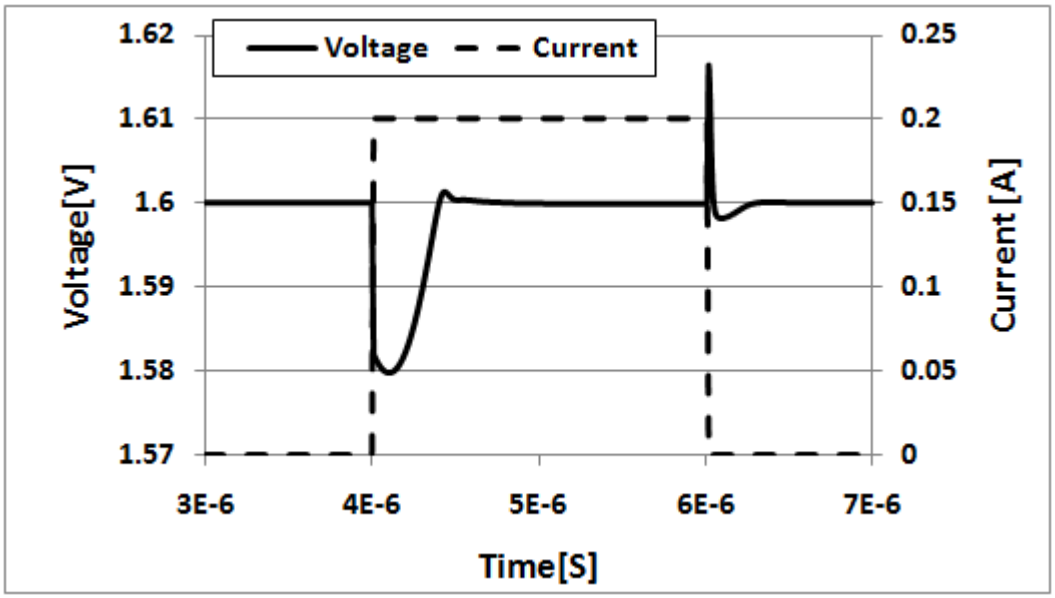

Fig. 22 Transient response to a load step of 200mA with rise and fall times of 10ns

Fig. 22 shows the complete load transient response of the LDO to positive and negative load dumps of 200mA per 10nS rise and fall times. It can be observed that the positive voltage droop is lesser than the negative voltage droop because of the unidirectional slew rate limitation of the system, i.e. the transistor M_{P3} (in Fig. 11) being a class A amplifier can provide large currents in one direction, and limited DC current in another direction [4].From Fig. 22 it can be seen that the total transient voltage droop is less than 35mVs and the worst case settling time is around 0.6μS.

c. PSR results

To compare the effectiveness of the compensation scheme over the conventional LDO, PSR post-layout simulation results for a load of 200mA's with and without the auxiliary block are compared in Fig. 23. The PSR enhancer block is able to improve the PSR by 30dB at 1MHz over the uncompensated block, the effectiveness of the PSR enhancer starts to degrade after 1MHz due to the parasitic poles in it.

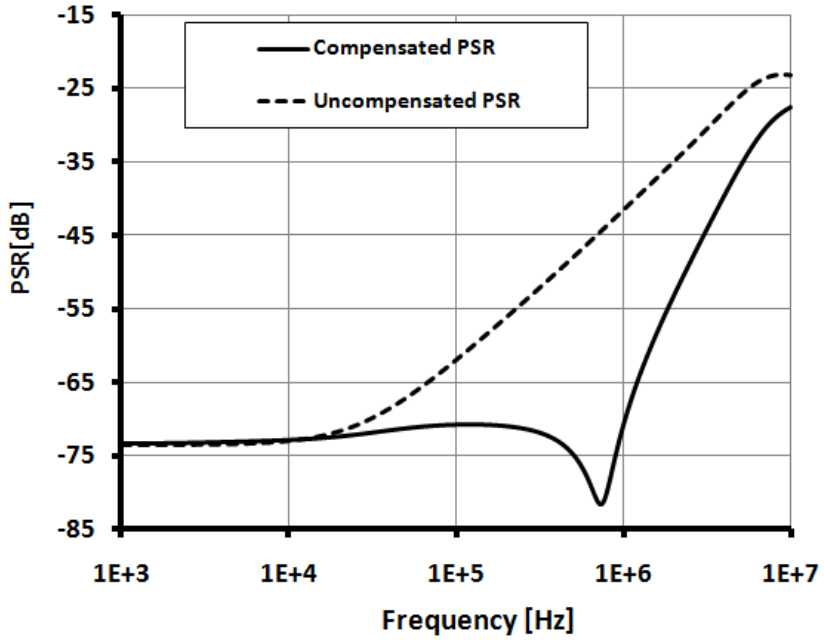

Fig. 23 PSR vs. frequency with and without compensation for a load of 200mA

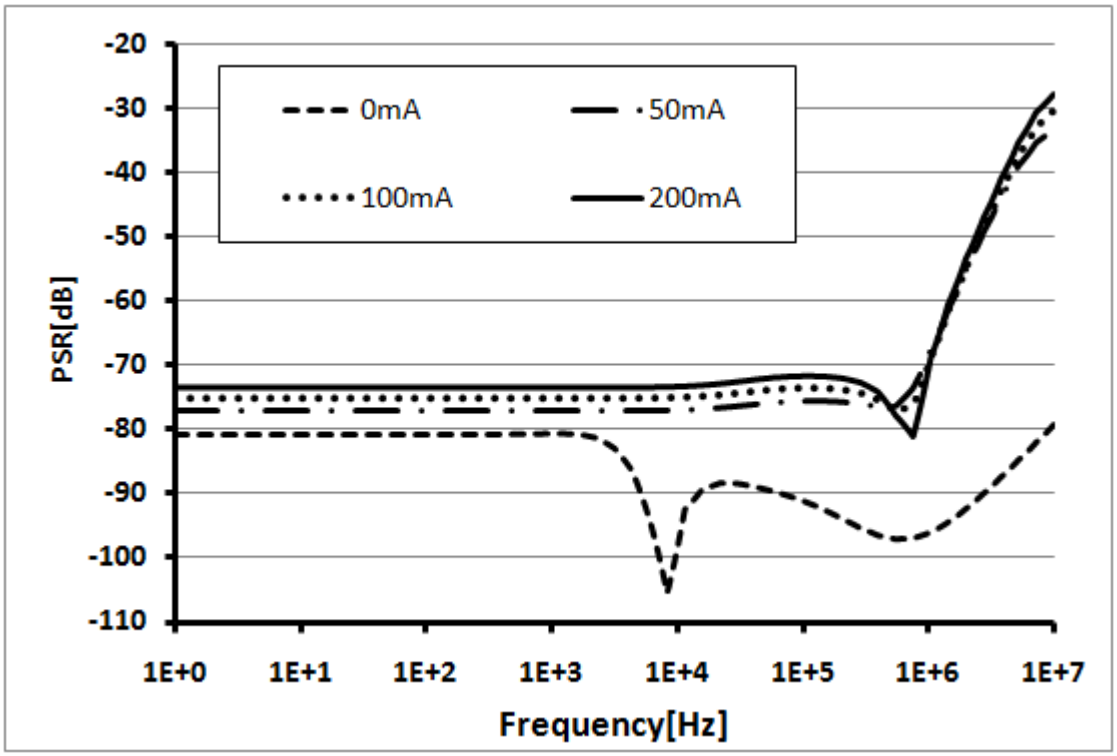

Fig. 24 PSR vs. frequency with compensation for different loading conditions

Fig. 24 shows the PSR for the proposed LDO vs. frequency with varying load currents, these curves confirm the robustness of the system for a large range of load currents, the system can achieve a PSR of 66 dB till 1MHz in the worst case.

II.7 Synopsis

A comprehensive analysis of PSR in conventional LDOs is being presented, followed by the discussions on present state of art implementations to improve PSR and their drawbacks. An intuitive idea to improve the PSR of the LDO by adding an additional auxiliary block which can attenuate the supply noise of the main block has been proposed, this is followed by the implementation details of the auxiliary block. The stability issues in LDOs are being discussed and the implication of adding auxiliary block on stability is presented, finally the transient analysis of the LDO followed by the transient and PSR simulation results have been presented, the simulation results agree with the anticipated results.

The merit of this architecture is compared with the state of art LDOs which aim at improving PSR, the comparison is summarized in Table 3.

Table 3 Comparison of the proposed topology against the state of the art

Performance Parameter	**[9]**	**[8]**	**Proposed Architecture**
Technology	0.6µm CMOS	0.13µm CMOS	0.18µm CMOS
Min. Input voltage	1.8V	1.15V	1.8V
Max. Load Current	5mA	25mA	200mA
Dropout Voltage	450mV	150mV	200mV
Output Capacitance	On-Chip	4µF	2.2µF
Load regulation	1.57mV/mA	0.048mV/mA	0.002mV/mA
IQ	70µA	50µA	50µA@no Load 15mA@Full Load
Worst case PSR @ 1MHz	40dB	66dB	66dB
ΔVout(full load transient)	937mV @ 5mA step	26mV @ 25mA step	35mV @ 200mA step

As seen from Table 3 the cascoding technique in [9] helps improving PSR but has the disadvantage of large dropout, and bad transient response. The feed forward ripple cancellation technique in [8] ,obtains the improvement of PSR by cancelling the power supply noise due to transconductance and channel resistance of pass transistor by

replicating supply ripple at the gate of pass transistor, this technique does not warrant PSR improvement for large range of load currents due to variation of channel resistance.

Finally it can be concluded that a robust PSR improvement technique for LDOs which can overcome the drawbacks in the previous state of art implementations is being presented, also the presented LDO has large load current capability without affecting the regular loop dynamics.

CHAPTER III

TRANSIENT AND POWER SUPPLY REJECTION IMPROVEMENT IN CAPACITOR-LESS LDOS

The devices like “smart phones”, “PDA’s” and other multifunctional battery operated devices demand “tailored” power supplies for each of the different blocks, “digital”, “baseband”, “RF” and “audio” [13]. For the digital circuits power supply rejection (PSR) and output noise are not “critical” however they demand power supply designs with sub-micro amperes of quiescent current because they are always in “ON” mode. Whereas power is traded to reduce output noise for the power supplies serving RF devices, the feedback resisters are made small enough to reduce the thermal noise at expense of extra current flowing through them. The battery voltage variations caused by GSM bursts creates noise on the battery, thus the audio devices require high PSR to avoid serious clicking noise. Thus multiple tailored made local on-chip regulators are required to power up each sub block; multiple on-chip regulators don’t have the luxury of extra pin for an external capacitor at their outputs, also the elimination of the external capacitor saves valuable PCB space and cost form.

Since the internal pole is made dominant in external capacitor-less LDO’s due to the lack of large (>1nF) load capacitors, these regulators are termed as “ internally compensated LDOS”. The absence of the external capacitor and large load impedance variations demand designs with conservative loop phase margins that usually require higher quiescent power. During the load transients according to the equation (2.11) from

Chapter II the change in output voltage is inversely proportional to output capacitance, in addition the time required for the loop to react to an load-current demand depends on the slew rate at the gate of the pass transistor, the capacitor-less LDOs typically has the dominant pole at its gate thereby reducing its slew rate, these two effects worsen the transient response of the capacitor-less LDOs. The use of transient compensation techniques employing fast feedback loops have shown to be an effective solution [14]. This approach reduces the LDO's output ripple due to fast loading variations, however the auxiliary feedback loop uses a class A amplifier and hence requires large quiescent currents to charge and discharge the bulky parasitic gate capacitance (C_{gate}) of the pass transistor (MP).

The conventional LDO voltage regulator, are stabilized using a large external output capacitor , but external-capacitor-less LDOs are devoid of this extravagance, few solutions are proposed in literature to stabilize the external-capacitor-less LDOs which are unfortunately unstable for low load currents [15, 16]. A successful AC compensation scheme which is stable for all loading conditions has been proposed in [14], In this project similar AC compensation scheme has been adopted.

Also the capacitor-less LDO's suffer from a inferior PSR response as compared to an externally compensated LDO's, the following analysis gives a comprehensive view of the PSR in external-capacitor-less LDO's.

III.1 PSR analysis in internally compensated LDOs

Fig. 25 shows the PSR analysis of externally and internally compensated LDOs, maximum loading condition has been taken in to consideration in both cases, the following practical conditions has been considered:

1. Both externally and internally compensated LDOs dominant pole is located at the same frequency.
2. Due to the smaller on-chip output capacitance of internally compensated LDOs the zero due to ESR associated with output capacitor is located at much higher frequency, as compared to ESR zero of the externally compensated LDO.
3. Usually pole splitting techniques are used to stabilize the internally compensated LDOs, in the case of maximum load current the output pole is placed outside the UGF.

In Fig. 25, ω_{DE} and ω_{DI} are the dominant poles of externally compensated and internally compensated LDO respectively, ω_{2E} and ω_{2I} are the second dominant poles of the externally compensated and internally compensated LDO respectively, UGF_E and UGF_I are the unity gain frequencies of the externally compensated and internally compensated LDO respectively ω_{esrE} and ω_{esrI} are the ESR associated zeros of the externally compensated and internally compensated LDO respectively.

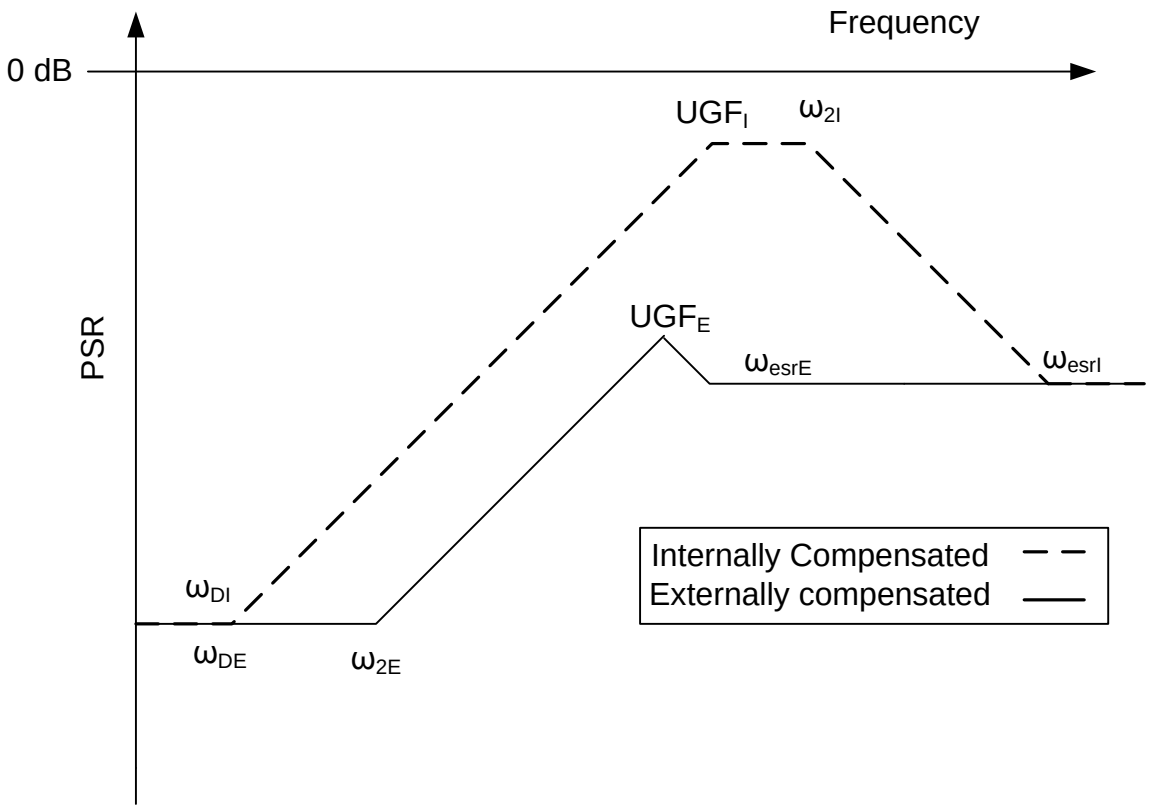

Fig. 25 PSR analysis of internally and externally compensated LDOs using a comprehensive analysis for a realistic case

The internally compensated LDOs PSR starts to roll off at the frequency of its dominant pole which is located at the gate of the pass transistor, this is due to the reduction in its loop gain, where as this is not the case with the externally compensated LDO, due to the fact that even though the loop gain decreases at 20dB per decade after the occurrence of the dominant output pole, the output capacitor starts filtering the output supply correlated ripple at the same rate and these two effects cancel each other[7].

In case of internally compensated LDOs after the UGF the PSR roll off stops until the occurrence of the output pole, after which the output capacitor starts filtering the supply noise at the output of LDO, this filtering keeps improving the PSR until the occurrence of the zero due to ESR associated with output capacitor, the final value of PSR can be found as

$$\frac{V_{out}}{v_{dd}} = \frac{R_{ESR}}{R_{ESR} + r_{ds}}[1 + (1-\alpha) g_m r_{ds}] \tag{3.1}$$

where R_{ESR} is the ESR of the output capacitance, r_{ds} and g_m are the channel resistance and transconductance of pass transistor and α is given by $\left(\frac{C_{gs}}{C_{gs} + C_P}\right) v_{dd} = \alpha v_{dd}$, where v_{dd} is the noise present on the power supply, C_{gs} is the gate-source capacitance of the MP, and C_p is overall parasitic capacitance present at the gate of the pass transistor excluding C_{gs}. The PSR analysis for the externally compensated LDOS has been briefly done in Chapter II, and the analyzed PSR curve in Fig. 5 has been adopted in Fig. 25. As seen from the analysis and as depicted in Fig. 25 the issue of PSR in internally compensated LDOs is much more severe.

The previous academic works and their disadvantages have been briefly discussed in Chapter II Section 2, this project presents an external-capacitor-less LDO architecture equipped with a couple of low-power complementary compensating blocks that improve transient performance, small signal stability, and PSR bandwidth. The compensation blocks employ a combination of few micro-amps quiescent current and dynamic biasing which help to reduce the overall static power. PSR bandwidth

improvement is achieved by employing a differentiating block embedded in a fast feedback loop.

III.2 Improving PSR in external-capacitor-less LDOs

Better high-frequency PSR figures can be achieved by replicating the supply ripples on to the gate of MP such that its gate-source voltage does not present any v_{dd} noise [8]. This can be done by using a feed forward path determined by C_{vdd} and the current amplifier as shown in Fig. 26. In order to account for the noise in paths 2 and 4, the amplitude of v_{dd} noise at the gate of the pass transistor should be made greater than the amplitude of v_{dd} noise at its source.

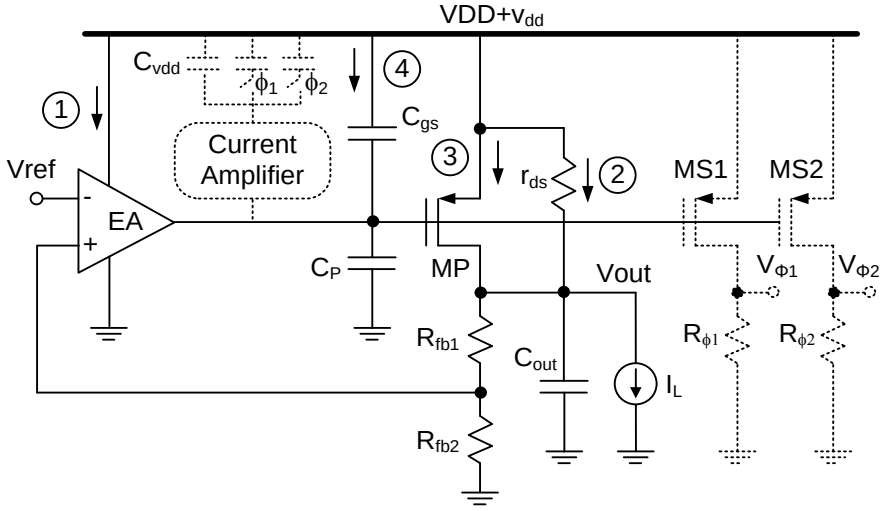

Fig. 26 The conventional LDO with proposed PSR enhancing block

The v_{dd} gain of this topology including the feed-forward path at frequencies much greater than the pole frequency at the gate of the pass transistor can be found as

$$\frac{v_{out}}{v_{dd}} = \frac{1 + g_m r_{ds}[1 - \alpha - \frac{C_{vdd}}{C_{gs} + C_P} A_i]}{1 + \frac{r_{ds}}{R_{fb1} + R_{fb2}} + \frac{r_{ds}}{Z_L} + g_m r_{ds} \frac{R_{fb2}}{R_{fb1} + R_{fb2}} A_{e(s)}} \tag{3.2}$$

where C_{vdd} is the PSR compensation capacitor in Fig. 26; A_i is the current amplification factor of the current amplifier; and Z_L is the total load impedance at the LDO output without the feedback resistances R_{fb1} and R_{fb2}. $A_e(s)$ is the frequency-dependent gain of the error amplifier. According to (3.2), the value of compensation capacitance (C_{vdd}) multiplied with current gain (A_i) required to realize a zero gain transfer function (so that there is no supply-related noise at the output of the LDO) is given by

$$A_i C_{vdd} = \left(C_{gs} + C_P\right)\left(1 - \alpha + \frac{1}{g_m r_{ds}}\right) \tag{3.3}$$

It is evident from (3.3) that the amount of required compensation capacitance varies with the loading conditions since C_{gs}, C_P, α, g_m, and r_{ds} are sensitive to the bias conditions of MP. Usually, high-current load conditions require large compensation capacitors, one of the major reasons being increase in supply noise current due to reduction of channel resistance (r_{ds}) with increase in load current. According to simulations, the optimal value for C_{vdd} is around 500fF for 0mA load, while the required capacitance is 900fF for maximum loading condition. To accommodate this varying requirement for C_{vdd} the effective capacitance is gradually adjusted using a simple control mechanism. It consists of two scaled versions of pass transistor MS1 and MS2

(scaled by a factor of 4000) whose gates are attached to the gate of MP, these transistors detect a fraction of load current. The current flowing through these transistors is forced trough resistors $R_{\Phi 1}$ (80KΩ) and $R_{\Phi 2}$ (185KΩ) and the generated voltages $V_{\Phi 1}$, $V_{\Phi 2}$ are used to control similar NMOS triode switches Φ_1 and Φ_2. Since both the transistors (MS1 and MS2) detect equal amounts of currents and MS2 forces the current in to a larger resistor $R_{\Phi 2;}$ switch Φ_2 switches at lower loads (approximately 15mA load current) compared to switch Φ_1 which switches at 35mA load current, hence the control voltages adjust the capacitance according to the loading conditions; the effective C_{vdd} for load range 0-15mA is 500fF, for load current in the range 15mA to 35mA is 700fF and for load range 35mA to 50mA is 900fF. MS1 and MS2 must detect same amount of currents, thus they have to be matched in layout using proper matching techniques. The load ranges need not be very precise, because even 10% mismatch in cancellation can still yield 20dB PSR improvement, and if needed more granularity can be easily added. This whole control mechanism consumes an additional static current of 30μA for a load of 50mA, while consuming less than a micro ampere for no loading condition, thus the current efficiency of the overall system is unaffected.

The block level implementation of the PSR enhancer is shown in Fig. 27, the proposed block consists of an integrator and an additional transconductance stage ($-Gm_{f2}$). In Fig. 27 C_{vdd} , C_{vdd1}, C_{vdd2} are the bank of capacitors which forms the required variable compensation capacitance controlled by the switches Φ_1 and Φ_2 , while R_{p1} and R_{p2} are the resistance associated with the switches, C_2,R_2 are the output resistance and capacitance of the first stage.

Ignoring the parasitic poles the transfer function would be

$$\frac{i_g}{v_{dd}} = sC_{vddt}(R_1 Gm_{f2}) \tag{3.4}$$

where C_{vddt} is the total compensation capacitance and i_g is the small signal current injected in the gate of the pass transistor.

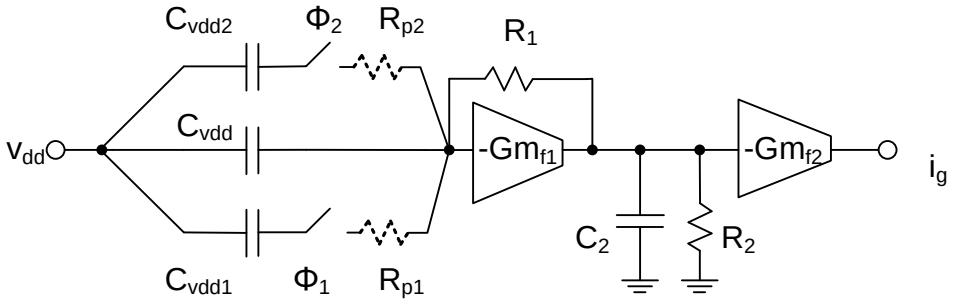

Fig. 27 Block level implementation of proposed PSR enhancer block

The amplification A_i which is given by the R_1Gm_{f2} is decided based on the transient response of the LDO and is described in the later part of the chapter. The differentiator has some parasitic poles and zeros and these has to be placed farther than the intended frequency of PSR improvement, the two dominant poles of the differentiator in Fig. 27 are

$$\omega_{PD1}{}^{*} \approx \frac{Gm_{f1}R_2}{C_{vddt}\left(R_1 + R_2\right)} \tag{3.5}$$

* For maximum load current.

$$\omega_{PD2} \approx \frac{1}{C_2\left(R_1 \| R_2\right)} \tag{3.6}$$

The switch sizes need not be large, the size selected in this design is as small as 4μ/180n, it has an worst case on resistance always less than 5K Ohms. The parasitic switch resistance R_{p1}, R_{p2} introduces a pair of parasitic poles and zeros which are located at several ten's of megahertz thereby not effecting our design.

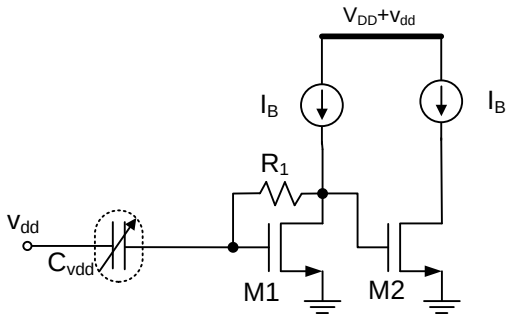

Fig. 28 Circuit level implementation of the PSR enhancer

The circuit level implementation of the PSR enhancer is shown in Fig. 28, in fact the current amplifier is implemented by reusing the differentiator in the undershoot canceler, which will be discussed in the later part of this chapter. The current amplifier together with variable C_{vdd} serves as the PSR enhancer block. Thus the PSR enhancement comes at virtually no additional power, the only additional requirement is additional capacitance and the control mechanism to vary the capacitance.

It should be noted that this method improves PSR only for high frequencies, DC PSR can be increased by increasing loop gain and designing EA using the techniques described in Chapter II section 3.e.

The EA is a simple two stage amplifier similar to Fig. 11, it has a gain of 55dB and consumes a quiescent current of 6μA.

PSR simulation results for 50mA load current with and without the proposed compensation scheme are shown in Fig. 29. The compensated LDO achieves an improvement of 20dB at 1MHz frequency over the uncompensated case. Fig. 30 shows the robustness of the cancellation scheme over a wide range of load currents achieved with the help of a bank of capacitors controlled by the output current level sensors. From Fig. 30 it is evident that the compensation scheme can yield a worst case PSR of 55dB till 1MHz.

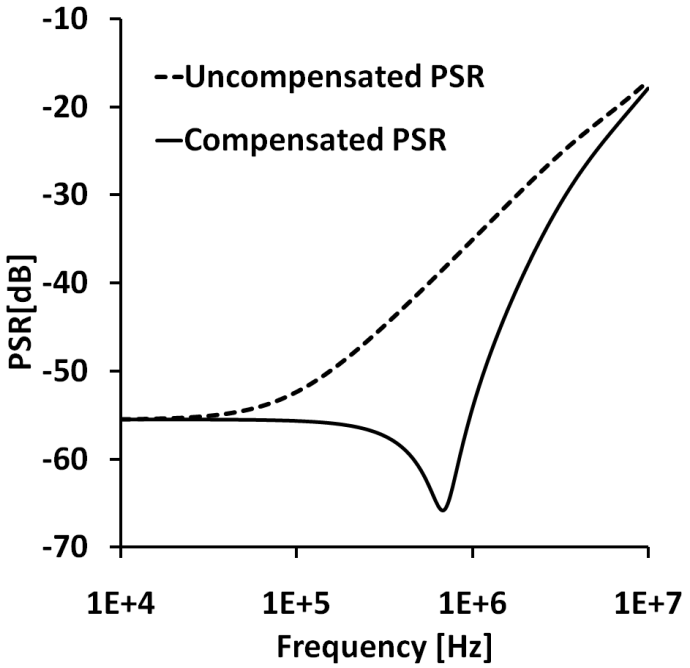

Fig. 29 PSR vs. frequency with and without compensation for a load of 50mA

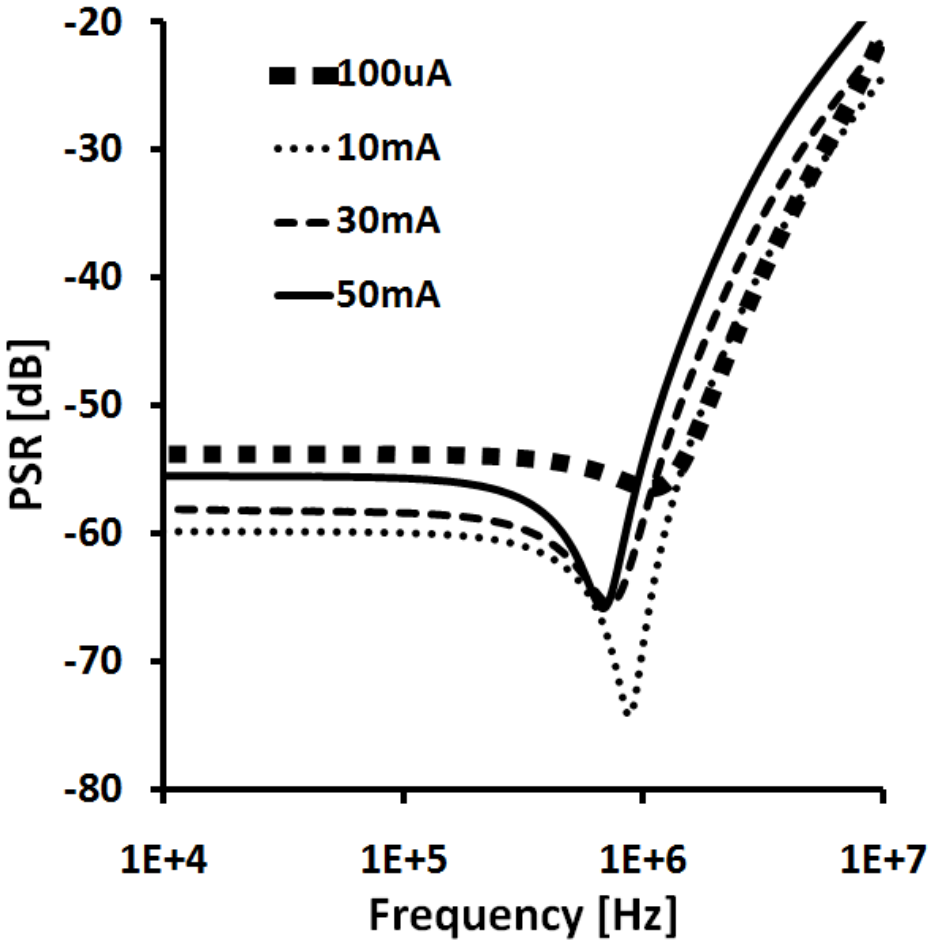

Fig. 30 PSR vs. frequency with compensation for different loading conditions

III.3 Transient response

The amplitude of the output voltage spikes (voltage droop) depends on various factors such as speed of the load variations, load capacitance present at the output of LDO, loop bandwidth, loop phase margin, but is mainly determined by the slew rate at the gate of the pass transistor [14, 17- 20].

A comprehensive equation for the voltage droop can be easily derived from the capacitor current equation and can be found as

$$\Delta V_t = \frac{I_{LOAD}}{C_O}\left(\frac{1}{B.W} + t_{S.R}\right) \tag{3.7}$$

where ΔV_t is the transient voltage droop, I_{LOAD} is the load current step, C_O is the output load capacitance, B.W is the bandwidth of the LDO, $t_{S.R}$ is the delay caused due to slew rate limitation. Further $t_{S.R}$ can be derived as

$$t_{S.R} = C_{GATE}\frac{\Delta V_g}{I_b} \tag{3.8}$$

where C_{GATE} is the total effective capacitance present at the gate of the pass transistor, ΔV_g is the voltage change at the gate of the pass transistor and I_b is the bias current in the second stage of the error amplifier.

A realistic situation is considered to compare the voltage droop due to delay caused by the finite bandwidth (B.W) and finite slew rate ($t_{S.R}$) , let us consider that the B.W is 1MHz, C_O is 100pF, C_{GATE} is 100pF (including miller effect caused due to C_{gd}), ΔV_g is 500mV and I_b is 2.5μA.

The delay caused due to slew rate limitation according to (3.8) is 20μS, while due to bandwidth limitation (B.W) limitation is just 1μS. Thus the major contributor of the output voltage spike is slew rate at the gate of the pass transistor.

A few attempts have been made previously to solve the issue of finite slew rate in LDOs [16-20], the quiescent current consumption of these previous solutions during load transients have been summarized in Fig. 31.

To overcome the slew rate limitations due to the excessive capacitance at the gate of MP, large amounts of current have to be used to charge and discharge C_{GATE} [16-20]. Hazucha et al. [18] solved this issue by using a huge bias current of 6mA. This approach of using large bias currents would drastically reduce the current efficiency in low loading conditions.

A smarter approach has been implemented by Rincon Mora et al. by using a buffer which has an adaptive bias current i.e. it increases its bias current with increase in its load current, thus the buffer can drive the large gate capacitance easily with the increased bias current, the bias current for this scheme is shown in Fig. 31. Large quiescent current is required only during the transient operation; once the output voltage reaches its steady state value no more current compensation is required. This means that the increased current in the buffer is not of use during steady state implying that there is more than necessary power consumption. Also this approach doesn't solve the issue of limited bandwidth of the LDO; there will still be a considerable voltage droop due to finite bandwidth of the LDO.

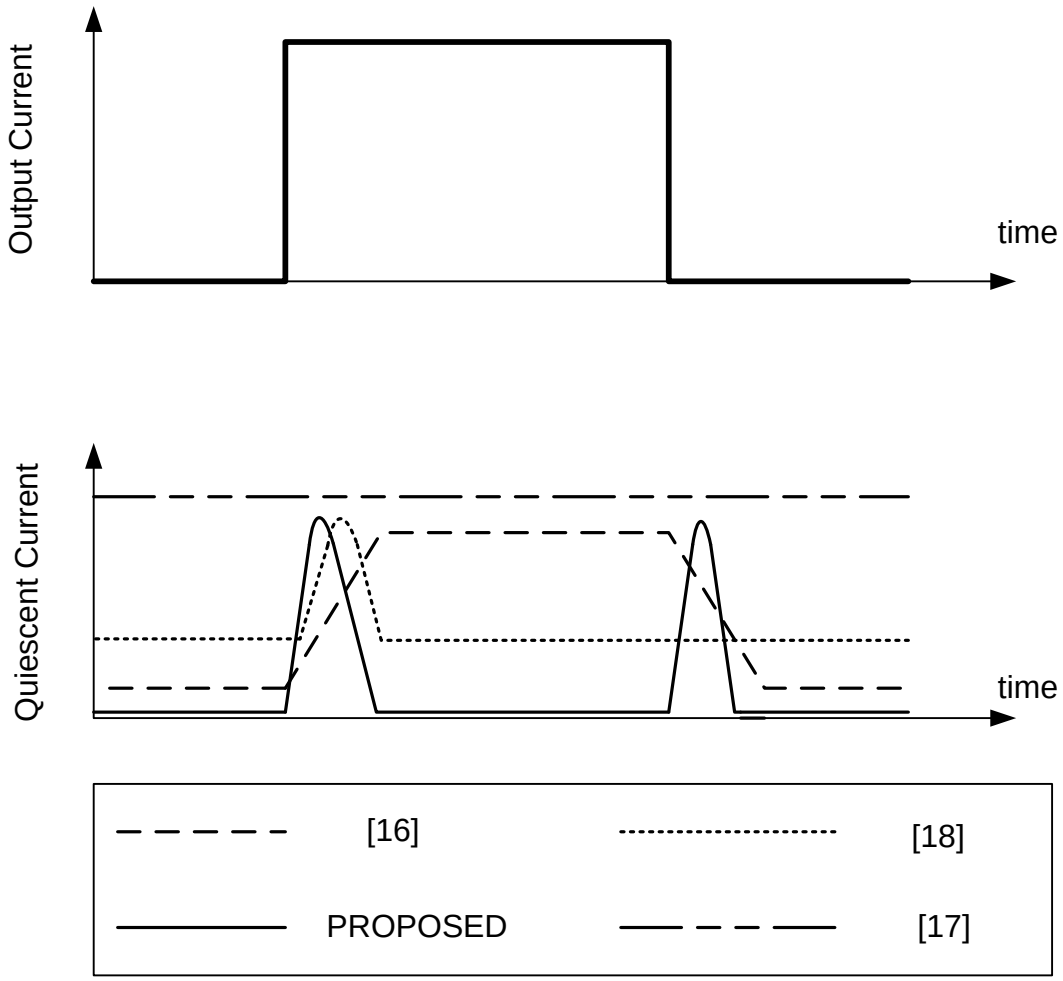

Fig. 31 The quiescent current consumption in various previous publications

The solution proposed by Milliken et al. uses a fast auxiliary transient path and thereby reduces the voltage droop due to the bandwidth limitations, but the used fast auxiliary block being a class A amplifier requires large quiescent currents to charge and discharge the gate capacitance of the pass transistor. It can be seen in Fig. 31 that the auxiliary block due to its “class A” nature can yield high currents in one direction but limited current in other direction. This solution can discharge the parasitic gate

capacitance at a faster rate than the solution in [16], because the feedback information from the output of the LDO to the gate of the pass transistor is via the fast auxiliary path compared to slow error amplifier path in [16].

After this brief review it is clear that the desired solution should only need extra bias during transients unlike the solution in [17,18], also to solve the issue of voltage droop due to finite band width of LDO , the transient feedback path must be a auxiliary fast loop [14] and should avoid the slow error amplifier path. Finally class AB or class-B solution would be more power efficient than the classic class A compensation scheme. The desired LDOs quiescent current during load transients is shown in Fig. 31.

A class AB system with dynamic current boosting solution is envisioned in this project which is shown in Fig. 31.

To improve the LDO transient response and to minimize the output ripple, a glitch detector based on a differentiator circuit is employed. A complementary operation for both positive and negative glitches enables true class AB operation and further minimizes the LDOs output ripple, the proposed circuit is shown in Fig. 32.

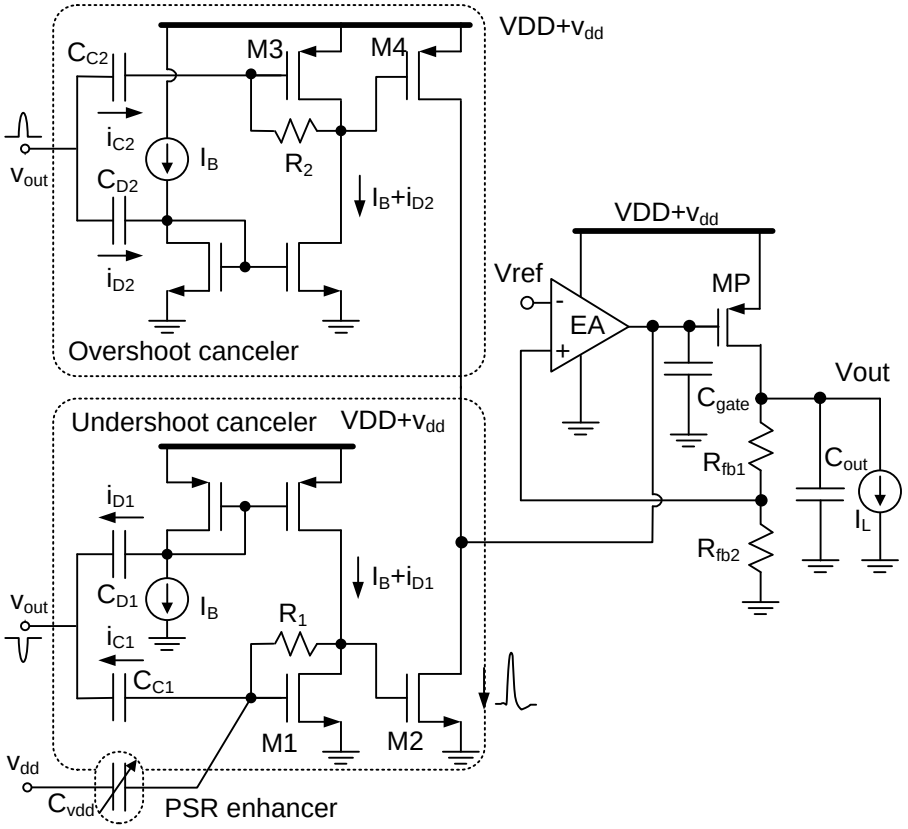

Fig. 32 Schematic of the proposed LDO with transient and PSR enhancing blocks

Let us consider first the operation of the undershoot canceller block which is redrawn in Fig. 33, For output voltage undershoots, C_{C1} senses the changes in the output voltage in the form of current (i_{C1}) assuming that the variations at the gate of M1 are small.

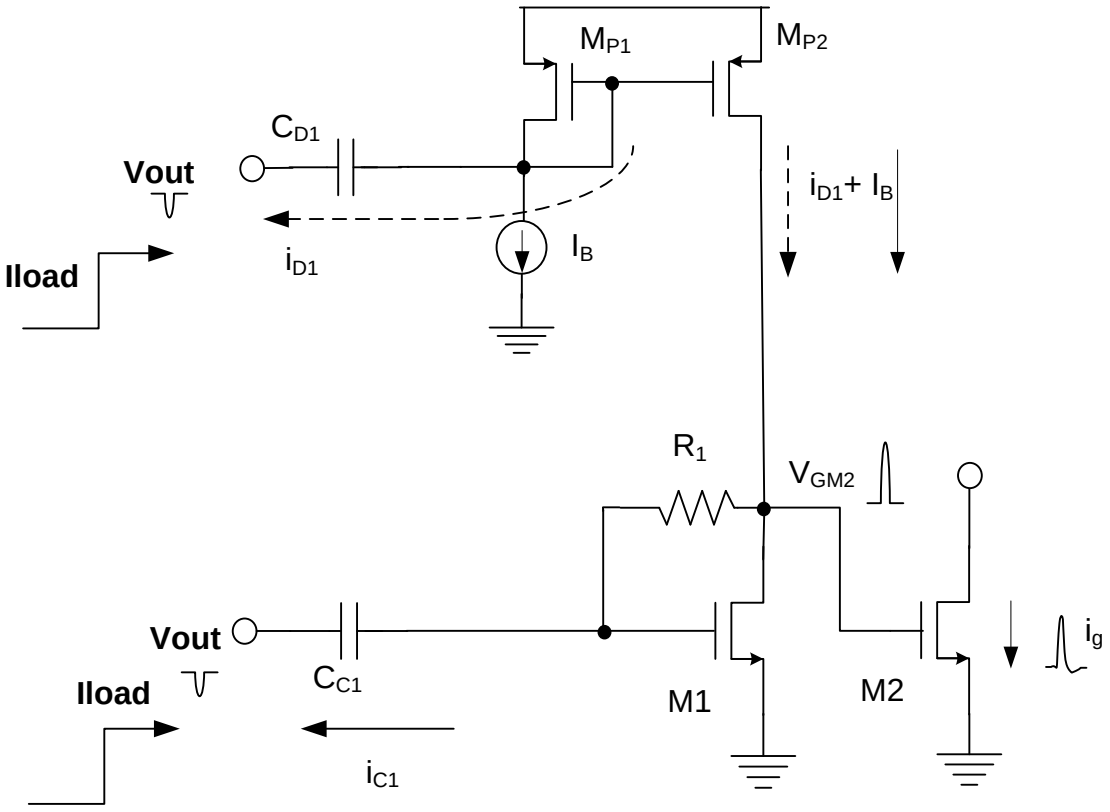

Fig. 33 Operation of undershoot canceller block

This current is proportional to the speed of the output voltage variation and is given by

$$i_{C1} = C_{C1}\left(\frac{dV_{out}}{dt}\right) \tag{3.9}$$

it is converted into voltage by R1 which is given by

$$V_{GM2} = C_{C1}R_1\left(\frac{dV_{out}}{dt}\right) \tag{3.10}$$

and this large voltage is converted back to current by M2

$$i_g = g_{m2} R_1 C_{C1} \left(\frac{dV_{out}}{dt} \right) \tag{3.11}$$

this large current is extracted from C_{GATE}. R1, M1 and M2 operate as a current amplifier while C_{C1} extracts the voltage variations of V_{out}. As demonstrated in [14], the amount of current injected into the gate of MP is effectively equivalent to the one provided by a capacitor of value $g_{m2}R_1C_{C1}$. The design strategy followed here is to employ this current mainly for undershoots, so that the bias current in both M1 and M2 is minimized. For class A operation, the bias current of M2 must be greater than the transient currents, since large transient currents are generated the current efficiency of the LDO degrades especially under light loading conditions.

An efficient undershoot compensation scheme require to pull down the gate of MP and this operation can be efficiently done by M2 even if its quiescent current is small. An issue here is that to pull up the gate of M2, it is necessary to inject significant amount of current onto the M1 drain terminal. This current is efficiently generated during transients only (current on demand) by C_{D1} and the P-type current mirror as shown in Fig. 33. During undershoots, C_{D1} senses the output voltage variations via current i_{D1} and sums it with I_B. The system sensitivity increases since both i_{C1} and i_{D1} add up, thereby absorbing the large current value generated by C_{c1}. To save power, the bias current of M1 and M2 is less than few micro amperes; hence M2 cannot efficiently pull-up the gate of MP. To overcome this drawback a dual scheme as depicted inside of the dashed boxes in Fig. 32 is employed which includes a complementary overshoot

canceller; similar bias conditions are used for both overshoot and undershoot cancelation circuits.

Simulation results shown in Fig. 34 shows the LDOs response to a load step of 0-50mA with 1µs rise and fall times for a 100pF load capacitance. The sum of peak overshoots and undershoots is under 75mV.

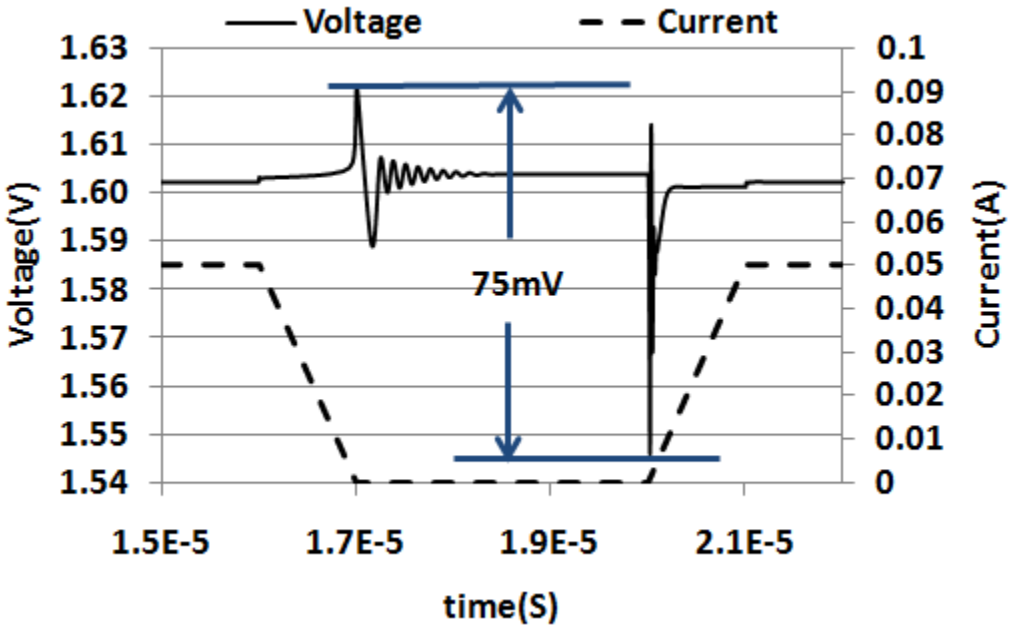

Fig. 34 Transient response to a load step of 50mA with rise and fall times of 1µs

III.4 Synopsis

Due to the absence of large external capacitance the external-capacitor-less LDOs have an substandard PSR and transient response, to overcome these issues a dynamically biased compensation block has been proposed, this block is capable of improving both the transient and PSR, the simulation results of the proposed LDO are being compared with state of art LDOs in Table 4.

As the comparison Table 4 shows the merit of proposed LDO compared to both the references [9, 20]. Reference [9] proposes a technique to improve PSR but it has poor load transients, the technique proposed in this chapter has better PSR with superior transients. The solution proposed in reference [20] improves the transient response, but is unstable for low load currents, while the solution proposed in this chapter is stable even for no load currents.

Table 4 Comparison of the proposed capacitor-less LDO topology against the state of the art

Performance Parameter	**[9]**	**[20]**	**Proposed Architecture**
Technology	0.6µm CMOS	0.35µm CMOS	0.18µm CMOS
Min. Input voltage	1.8V	1V	1.8V
Max. Load Current	5mA	66.7mA	50mA
Dropout Voltage	450mV	200mV	200mV
Output Capacitance	10pF	100pF	100pF
Load regulation	1.57mV/mA	----	0.03mV/mA
IQ	70µA	19µA	18µA@no Load 48µA@Full Load
Worst case PSR @ 1MHz	40dB	------	55dB
ΔVout(full load transient)	937mV	140mv @ 0.67mA-66.7mA	75mV

CHAPTER IV

CONCLUSIONS

Two novel power supply rejection improvement techniques have been presented in this thesis, in addition, in the second project a slew enhancement circuit was presented which consumes power only during transient instants and thereby enhances the transient response with minimum static power consumption.

Because of the absence of the external capacitor, the second project enjoys the benefit of having lesser pin-count and is a true SoC solution. Although capacitor-less solutions are very attractive, the external compensated LDOs are still useful to supply fast switching current loads such as analog oscillators which require currents having a rise and fall times in range of few pico-seconds or less. The external compensated LDO's huge output capacitor helps the regulator in suppressing output voltage variations in case of fast and high power load currents. In case of capacitor-less LDOs due to the small output capacitance the voltage spikes are very large which in effect switches off the circuits the LDO is supplying.

When we are limited in BOM , output pins and have fast switching oscillators on the chip, we replace the PMOS pass transistor in the regulator with an NMOS transistor . Whenever there is an output voltage glitch the gate-source voltage of the NMOS pass transistor changes and it automatically supplies the required load current instantaneously. However, the NMOS transistor due to its large dropout voltage has the disadvantage of lesser power efficiency. Summarizing this discussion, we have a

tradeoff between cost, power-efficiency and ability to supply fast switching loads. As a recommendation for future research in LDO's we can say that a capacitor-less LDO capable of supplying ultra fast switching loads is highly desirable.

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