REDUCED AREA DISCRETE-TIME DOWN-SAMPLING FILTER EMBEDDED WITH WINDOWED INTEGRATION SAMPLERS

A Thesis

by

KARTHIK RAVIPRAKASH

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2010

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Sebastian Hoyos
Committee Members,	Jose Silva-Martinez
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ABSTRACT

Reduced Area Discrete-Time Down-Sampling Filter Embedded With Windowed Integration Samplers. (August 2010)

Karthik Raviprakash, B.E., College of Engineering Guindy, Anna University, Chennai

Chair of Advisory Committee: Dr. Sebastian Hoyos

Developing a flexible receiver, which can be reconfigured to multiple standards, is the key to solving the problem of embedding numerous and ever-changing functionalities in mobile handsets. Difficulty in efficiently reconfiguring analog blocks of a receiver chain to multiple standards calls for moving the ADC as close to the antenna as possible so that most of the processing is done in DSP. Different standards are sampled at different frequencies and a programmable anti-aliasing filtering is needed here. Windowed integration samplers have an inherent *sinc* filtering which creates nulls at multiples of *fs*. The attenuation provided by *sinc* filtering for a bandwidth *B* is directly proportional to the sampling frequency *fs* and, in order to meet the anti-aliasing specifications, a high sampling rate is needed. ADCs operating at such a high oversampling rate dissipate power for no good use. Hence, there is a need to develop a programmable discrete-time down-sampling circuit with high inherent anti-aliasing capabilities. Currently existing topologies use large numbers of switches and capacitors which occupy a lot of area.

A novel technique in reducing die area on a discrete-time $sinc^2$ $\downarrow 2$ filter for charge sampling is proposed. An SNR comparison of the conventional and the proposed topology reveals that the new technique saves 25% die area occupied by the sampling capacitors of the filter. The proposed idea is also extended to implement higher down-sampling factors and a greater percentage of area is saved as the down-sampling factor is increased. The proposed filter also has the topological advantage over previously reported works of allowing the designers to use active integration to charge the capacitance, which is critical in obtaining high linearity.

A novel technique to implement a discrete-time $sinc^3$ $\downarrow 2$ filter for windowed integration samplers is also proposed. The topology reduces the idle time of the integration capacitors at the expense of a small complexity overhead in the clock generation, thereby saving 33% of the die area on the capacitors compared to the currently existing topology.

Circuit Level simulations in 45 nm CMOS technlogy show a good agreement with the predicted behaviour obtained from the analaysis.

DEDICATION

To my parents

ACKNOWLEDGEMENTS

First of all, I would like to thank my advisor, Dr. Sebastian Hoyos, for the support that he has provided me throughout my master's degree work. This thesis would not have been possible without his continuous motivation and encouragement in every stage of the project. Apart from his guidance in research, he always takes care of the welfare of his students. He is very kind, and I have enjoyed every minute of my interaction and work with him.

I would like to thank Dr. Styblinski, senior lecturer, for offering me a teaching assistantship for the course "Principles of Electrical Engineering." I felt extremely comfortable with her and enjoyed working for her. I am very happy that I met her and proud that I was able to earn her friendship. The position has given me the opportunity of interacting with undergraduate students. I thoroughly enjoyed every minute I worked as a teaching assistant for the course.

Special thanks to Dr. Sanchez for the motivation that he offers students through his courses. He is a role model for anyone who wants to pursue a career in the field. I admire his energy and his contributions to the field of analog circuit design.

Thanks to Dr. Jose Silva-Martinez, Dr. Peng Li and Dr. Javier Jo for serving as my committee members.

I would like to thank all my friends in College Station for the support that they have given me. My graduate life would not have been complete without them. The

discussions with my fellow mates in Analog and Mixed Signal Center (AMSC) have had a tremendous impact on my learning process.

My parents have always been there for me whether I succeed or fail in my attempts. My master's degree would not have been possible without their love and support.

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CHAPTER I

INTRODUCTION

The use of a mobile phone in today's world is more than that for voice communication. With the miniaturization of electronic devices, it has now become feasible to add multiple functionalities into hand-held devices at an affordable price for common man. With a new application and hence a new standard coming into the picture every now and then, there is a strong need for an efficient approach to design one radio and reconfigure for multiple standards. A platform which can be programmed to receive any single channel, with any modulation, located anywhere in a broad but finite predefined band is defined in [1] as software defined radio (SDR).

A. Challenges in SDR

The requirements of wireless applications differ on the basis of Data rate, range, mobility and quality of service (QOS) [1]. Most important of these requirements are channel bandwidth, image/blocker rejection at various stages in the receiver chain, frequency of sampling by the ADC and Noise Figure. It is extremely difficult to reconfigure various analog blocks in a receiver chain to meet the specifications of various standards.

This thesis follows the style of *IEEE Journal of Solid-State Circuits*.

B. Background

In 1995, Mitola [2] came up with the idea of a receiver in which the entire signal from the antenna is digitized immediately and the signal processing which has been conventionally done with analog blocks will now be done with a digital signal processor. Analog to digital convertor (ADC) is the only analog block in the receiver chain. With the wireless standards extending until 6 GHz and the dynamic range requirements being too high, even with today's technology (CMOS 45nm process), it is extremely challenging to build such an ADC and use it for hand-held devices. Although very idealistic in principle, Mitola's SDR concept has led to numerous advances in CMOS transceiver design. From then on, various attempts [3], [4] have been done in the lines of making a SDR true with the available technologies during the period.

In 2006, significant findings in this field were presented by Prof. Azad Abidi's team in UCLA [5]. Some of them are: 1) Direct conversion is the best choice for covering multiple bands. 2) Due to the clock-programmable anti-aliasing, the *windowed integration samplers* (Chapter II) can be considered to replace pre-select filters. 3) The RF front end should be wideband.

In [5], the channel of interest is down-converted to DC with a wide-band LNA and a mixer. Now, an anti-aliasing filter is required before baseband voltage sampling in order to isolate the wanted channel from a multitude of unwanted channels. Taking into consideration the bandwidths and blocker profiles of different standards, it is difficult to reconfigure an analog anti-aliasing filter to meet the wide range of requirements. The

inherent *sinc* anti-aliasing filtering provided by the windowed integration operation in charge sampling takes advantage of the frequency response nulls to eliminate unwanted interference.

The initial sampling rate for the windowed integration sampler is determined by the stop-band attenuation required for anti-aliasing and it can be much higher than the Nyquist rate for the input signal. To reduce the sampling rate to the Nyquist rate or the oversampled rate depending on the ADC architecture, down-sampling operation has to be performed. After down-sampling, the spectrum folds back again with the new sampling frequency equaling the sampling rate divided by the down-sampling factor. The anti-aliasing specification now needs to be met at the multiples of this new sampling frequency. A simple approach is to create a *sinc* down-sampling filter, which can be achieved by just summing up previous samples on capacitors and reading them out simultaneously. However, the attenuation provided by *sinc* down-sampling might not be sufficient and better filtering is necessary. By weighting previous samples with appropriate factors prior to summing up operation, $sinc^2$ and $sinc^3$ down-sampling filters can be created. These filters provide much deeper and wider nulls at the sampling frequency but require a large number of switches and capacitors. Ref [6] adopts the implementation in [5] and explains similar application of these down-sampling filters.

In multi-standard applications, many filters may be needed to select the channels of interest. Optimizing the filters' area becomes critical in lowering the production cost. In this thesis, a novel topology for the implementation of a $sinc^2$ filter with a down-sampling factor of two is proposed and compared to the conventional topology adopted

in [5], [6]. The proposed topology requires less number of switches and capacitors and this has been achieved by reducing the time for which the sampling capacitors are idle. To get the same SNR performance, the proposed topology requires 25% less die area for the sampling capacitors. The proposed topology also allows for the implementation of the filter using an active-integrator based sampler, which is difficult in previously proposed topologies. This has the advantage of improved overall linearity and insensitivity to output impedance of the Gm-stage.

Ref [5] explains the need for $sinc^2$ filter with higher down-sampling factor. The thesis also deals with the extension of the proposed topology to implement $sinc^2 \downarrow N$ filter. As the down-sampling factor N increases, area savings on the sampling capacitors increases reaching a maximum of 50% for large value of N.

For some applications [6], higher order *sinc* filters are needed and the thesis addresses the issue of reducing the die area of $sinc^3 \downarrow 2$ filters. It has been shown that the proposed filter saves 33% of the die area in sampling capacitors when compared with the conventional implementations. The simulation results shown in this thesis are done with CMOS 45nm technology.

C. Organization of Thesis

The theory of windowed integration samplers and discrete-time down-sampling filters is explained in Chapter II. In chapter III, the conventional and proposed implementations of $sinc^2 \downarrow 2$ has been explained. Benefits of the proposed topology with detailed mathematical analysis have been provided. Simulation results with CMOS

45nm technology have been included to support the claims. In Chapter IV, the extension of the proposed filter to get higher down-sampling factor is explained. Mathematical and simulation results are provided. In Chapter V, the implementation of $sinc^3 \downarrow 2$ with proposed technique has been explained and compared with the conventional implementation. Chapter VI summarizes the work done for the thesis along with the conclusion.

CHAPTER II

DISCRETE-TIME DOWN-SAMPLING FILTERS*

In this chapter, the theory behind windowed integration samplers providing reconfigurable anti-aliasing capabilities has been discussed. The practical difficulty in using windowed integration for multi-standard receivers with present technology and how it is overcome by using discrete-time down-sampling has been explained.

A. Windowed Integration Samplers

Consider Fig. 2.1 where the signal current *Gmvi(t)* is integrated on the sampling capacitor *Cs* for a duration Δt. At the instance when the capacitor is disconnected from the trans-conductor for readout, the signal is integrated on another sampling capacitor of the same value *Cs*. Here the sampling period *Ts* is equal to the integration duration Δt. At least two sampling capacitors are need to meet the condition $\Delta t = Ts$.

In essence, the signal is integrated for a period *Ts* and the integrated value is readout. Immediately after one integration, the next integration starts. This is depicted in Fig. 2.2.

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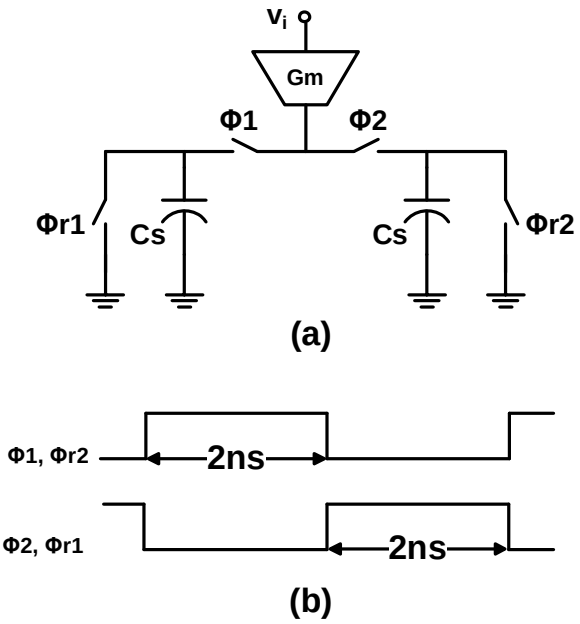

Fig. 2.1. Windowed integration samplers.

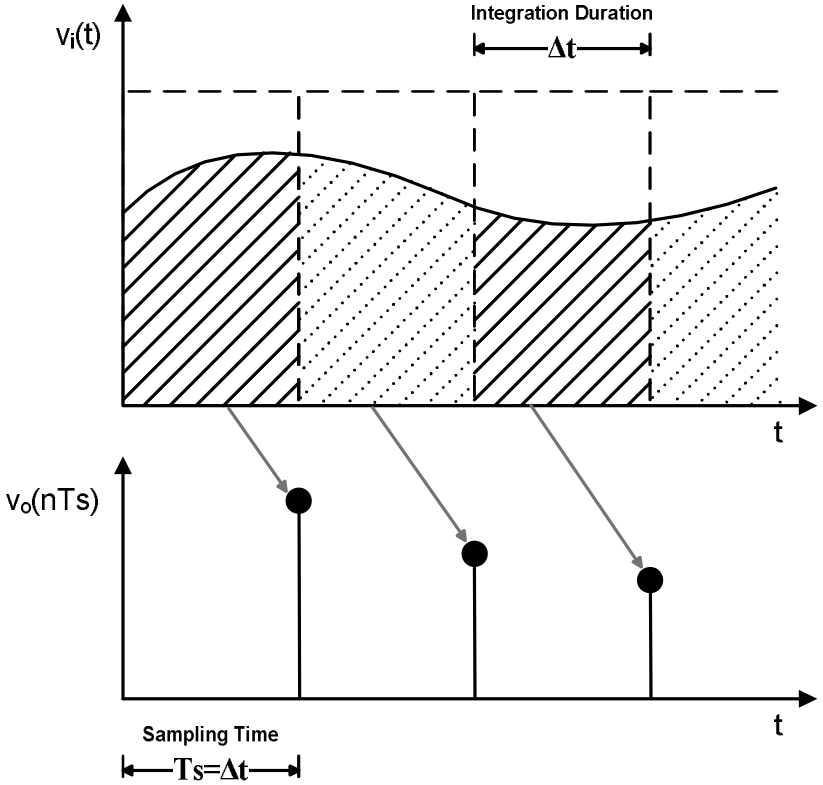

Fig. 2.2. Windowed integration where integration duration Δt = sampling period *Ts*.

The entire operation can be summarized as passing the signal *vi(t)* through a continuous time moving integration window of length Δt and then sampling the output at *Ts*. The mathematical modeling of the above operation is shown in (2.1).

$$vo(nTs) = \left\{ \frac{Gm}{Cs} \int_{\infty}^{-\infty} vi(\tau) h(t-\tau) d\tau \right\}_{sampled\ at\ t=Ts} \tag{2.1}$$

Here *h(t)* is defined in Fig. 2.3. Equation (2.1) is the convolution of *vi(t)* with *h(t)*. In other words, windowed integration sampling is nothing but passing the signal *vi(t)* through a continuous time filter of impulse response *h(t)* and then sampling the output at *Ts*. Fourier transform of *h(t)* is *sinc* with nulls at multiples of $1/\Delta t$. These nulls take care of attenuating the signals in the input spectrum at multiples of *fs (=Ts)*, which aliases back into the frequency of interest (around DC) as a result of sampling at *Ts*. This is shown in Fig. 2.4.

These nulls however offer limited attenuation as the interference bandwidth increases. The attenuation α due to *sinc* filtering, for a bandwidth *B* at N^{th} null is given by [5] (Fig. 2.5),

$$\alpha = \frac{2Nfs}{B} \tag{2.2}$$

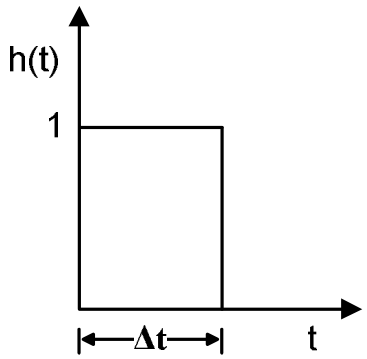

Fig. 2.3. Impulse response of windowed integration.

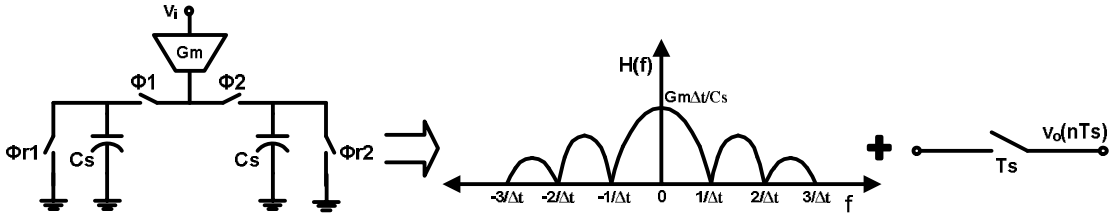

Fig. 2.4. Windowed integration sampling is equivalent to *sinc* filtering followed by sampling.

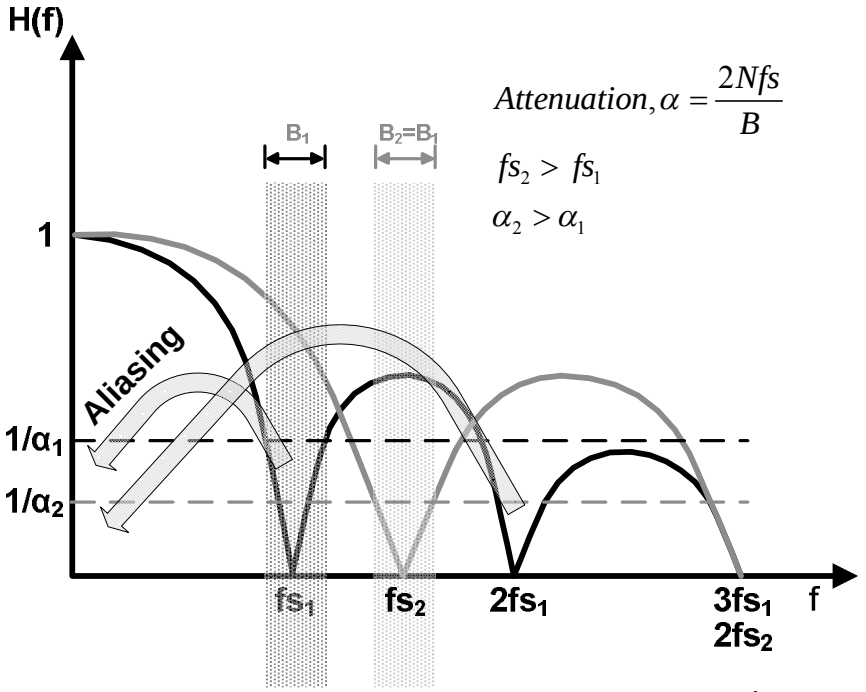

Fig. 2.5. For a given bandwidth *B*, attenuation *α* of the aliases due to the N^{th} null of *sinc* filter increases as the sampling frequency *fs* increases.

B. Discrete-Time Down-Sampling Filters

In order to meet the attenuation specification for a particular standard, the sampling frequency needs to be very high. Since the design of the ADC would pose extremely challenging specifications at such a high frequency, the sampled signal need to be down-sampled before digitization. This is done by discrete-time down-sampling filters.

(i) Rectangular Windowing

The sampled signals which are now stored as charges on capacitors can be down-sampled by adding the current charge-sample with *(N-1)* previous samples (Fig. 2.6(a)). This operation gives rise to a moving sum FIR filter, *H(z)* followed by $\downarrow N$ operation (Fig. 2.6(b)). Equation (2.3) and (2.4) shows the z-domain transfer function and the magnitude response of the filter, respectively. The FIR filter *H(z)* has nulls at multiples of *fs/N* and these are the frequencies which aliases back to the signal of interest after down-sampling. Depending upon the sampling frequency of the ADC (fs_{ADC}), the factor *N* is chosen.

$$Transfer\ function\ of\ the\ filter, H(z) = \sum_{i=0}^{N-1} z^{-i} = \frac{1 - z^{-N}}{1 - z^{-1}} \tag{2.3}$$

$$Magnitude\ response, H(f) = \frac{\sin\left(\frac{N\pi f}{fs}\right)}{\sin\left(\frac{\pi f}{fs}\right)} \tag{2.4}$$

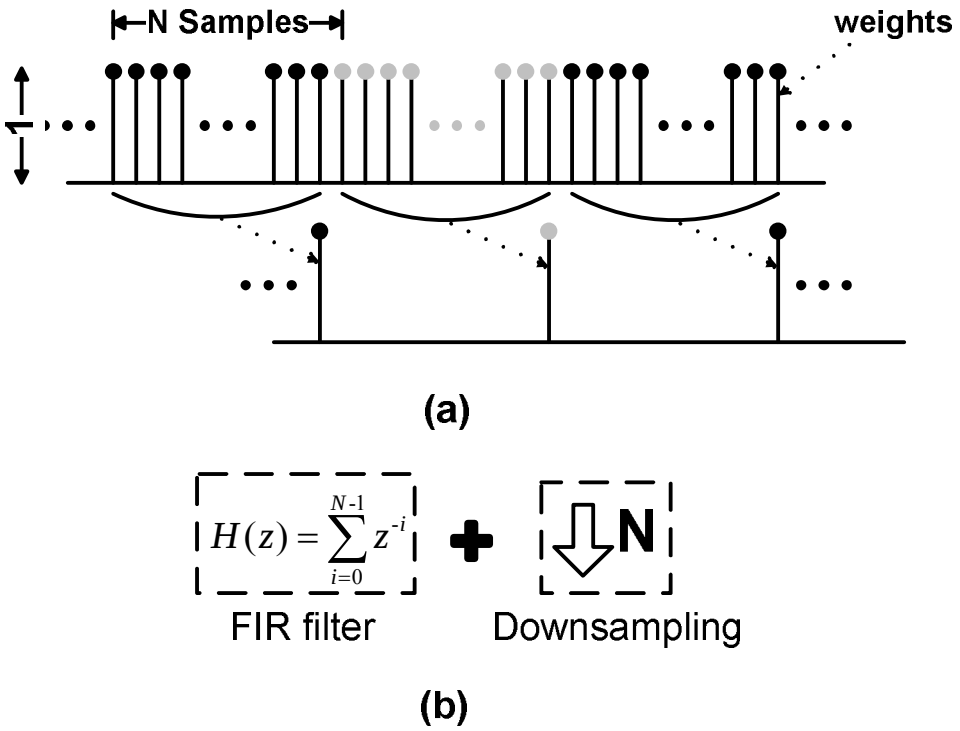

Fig. 2.6. (a) Down-sampling (↓*N*) using rectangular windowing (b) Equivalent representation, *H(z)*+↓*N*.

The attenuation provided by such a filter may not be sufficient for many applications and there is a need for a better filter.

Note on Frequency Response:

In literatures [5], [6], discrete time rectangular windowing is mentioned as *sinc* filtering. This is often misleading as the response (with DC magnitude normalized to 1) is $\frac{1}{N}\left(\frac{sin\left(\frac{N\pi f}{fs}\right)}{sin\left(\frac{\pi f}{fs}\right)}\right)$ and not $\left(\frac{sin\left(\frac{N\pi f}{fs}\right)}{\left(\frac{\pi f}{fs}\right)}\right)$. For $N=2$, it is $\frac{1}{2}\left(\frac{\sin\left(\frac{2\pi f}{fs}\right)}{\sin\left(\frac{\pi f}{fs}\right)}\right)=\cos\left(\frac{\pi f}{fs}\right)$

and not $sinc(\frac{2\pi f}{fs})$. It is more appropriate to call the filter *cos* than *sinc*. For *f/fs<<1*,

$$\frac{1}{N}\left(\frac{sin\left(\frac{N\pi f}{fs}\right)}{sin\left(\frac{\pi f}{fs}\right)}\right)\approx\left(\frac{sin\left(\frac{N\pi f}{fs}\right)}{\left(\frac{\pi f}{fs}\right)}\right)$$ and such filters can be called as *sinc* filters.

(ii) Higher Order *sinc* Filtering

A straight forward method of implementing n^{th} order *sinc* filter is to cascade *n* rectangular windows. The transfer function of n^{th} order *sinc* filter is shown in (2.5).

$$T(z)=\{H(z)\}^n=\left(\sum_{i=0}^{N-1}z^{-i}\right)^n \tag{2.5}$$

Equation (2.6) and (2.7) shows the transfer function and frequency response for *n=2*. It can be noticed that *n=2* corresponds to triangular windowing. Triangular windowing for ↓*4* is explained in Fig. 2.7(a).

$$\begin{aligned} &Transfer\ function\ of\ the\ filter,\\ H(z)&=1+2z^{-1}+\ldots+Nz^{-(N-1)}+\ldots+2z^{-(2N-3)}+z^{-(2N-2)}\\ &=\left(\frac{1-z^{-N}}{1-z^{-1}}\right)^2 \end{aligned} \tag{2.6}$$

$$Frequency\ Response, H(f)=\left(\frac{\sin\left(\frac{N\pi f}{fs}\right)}{\sin\left(\frac{\pi f}{fs}\right)}\right)^2 \tag{2.7}$$

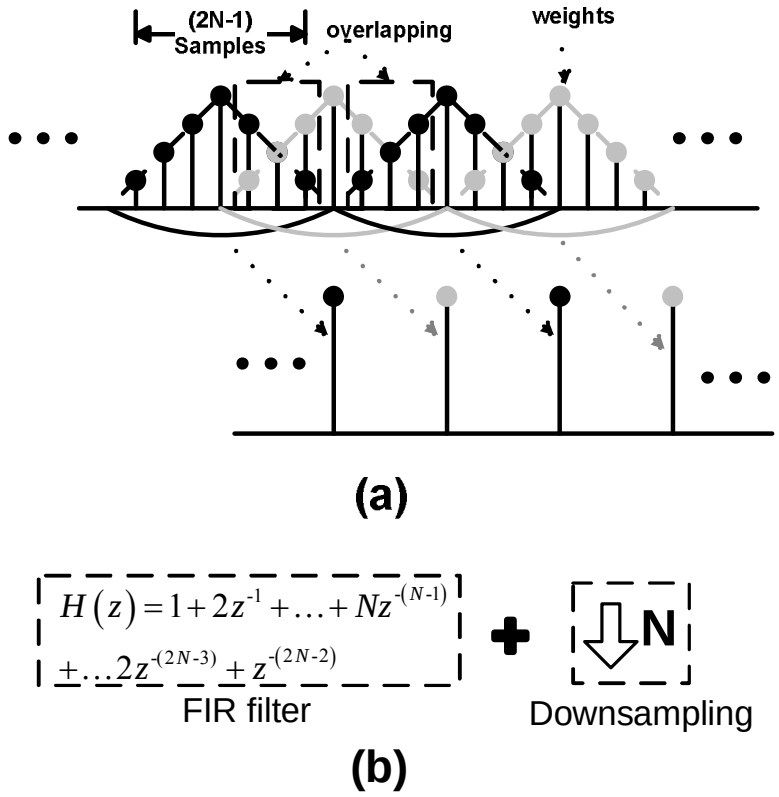

Fig. 2.7. (a) Down-sampling (↓4) filter using triangular windowing (b) Equivalent representation.

The magnitude response is the square of that obtained for moving sum. This gives rise to a better null attenuation compared to rectangular windowing. The disadvantage is that *(2N-1)* samples are needed to obtain ↓*N*. Unlike rectangular windows, triangular windows have to overlap in order to give the required performance, making the implementation complex.

For a sampling frequency of 500MHz, Fig. 2.8 compares the frequency responses of discrete time rectangular windowing, discrete time triangular windowing and $sinc^2$ for ↓2 and ↓4 up to *fs/2*. It should be noted that triangular windowing has better null

attenuation compared to rectangular windowing. Triangular windowing approximately follows $sinc^2$ for $f < fs/2$ and these filters are called $sinc^2$ filters in literature [5], [6].

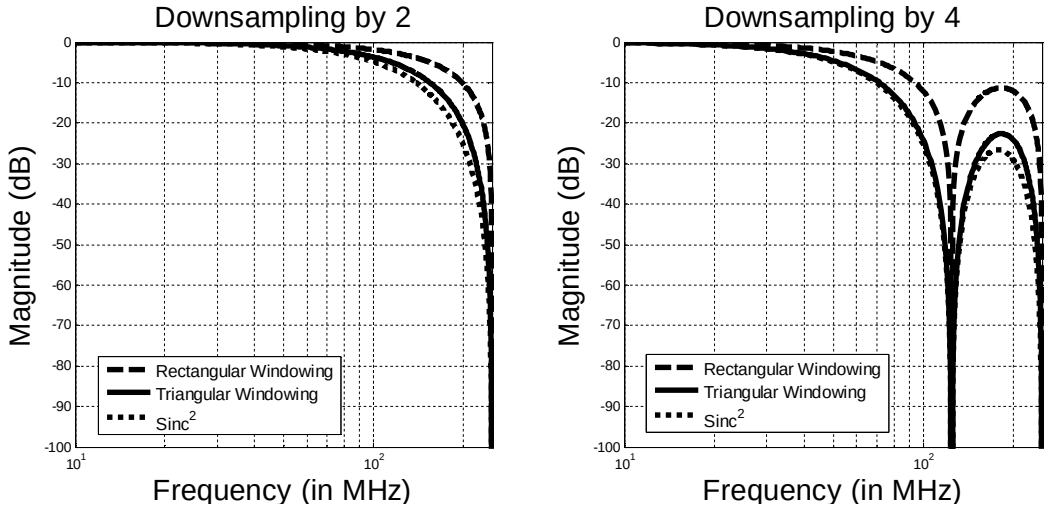

Fig. 2.8. Comparison of frequency response of discrete time rectangular windowing, discrete time triangular windowing and $sinc^2$ for $\downarrow 2$ and $\downarrow 4$

(iii) Summary

Table 2.1 summarizes the theory that has been discussed in discrete-time down-sampling filters.

Table 2.1. Transfer function of discrete-time filters

	Down-sampling by 2	Down-sampling by N
Rectangular Windowing (*sinc*)	$1+z^{-1}$	$\sum_{i=0}^{N-1} z^{-i} = \frac{1-z^{-N}}{1-z^{-1}}$
n^{th} Order *sinc* filtering	$\left(1+z^{-1}\right)^n$	$\left(\sum_{i=0}^{N-1} z^{-i}\right)^n = \left(\frac{1-z^{-N}}{1-z^{-1}}\right)^n$

Literatures discuss both higher order down-sampling (higher *N*) and higher order *sinc* filtering (higher *n*) in order to meet the specifications for various standards. Fig. 2.9(a) compares the frequency responses for the case where order *n* varies for a fixed down-sampling factor (*N=2*) and Fig. 2.9(b) compares the case where down-sampling factor *N* varies for a fixed order (*n=1*). The thesis explains the conventional implementations of both the cases and proposes solution to optimize the area on sampling capacitors in each case.

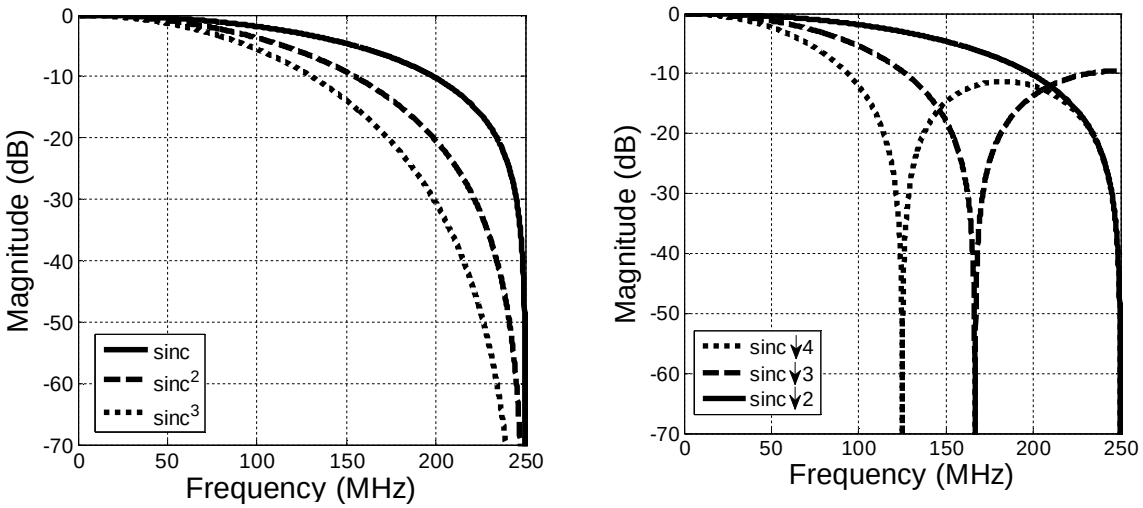

Fig. 2.9. Comparison of frequency responses when (a) For a fixed down-sampling factor (*N=2*), the order *n* varies (b) For a fixed order (*n=1*), the down-sampling factor *N* varies.

CHAPTER III

Sinc^2 ↓2 FILTER*

The implementation of sinc^2 ↓2 filter using conventional and proposed topology has been discussed in the chapter. The benefits of proposed topology over the conventional topology have been dealt in detail. Simulation results have been included at the end of the chapter.

A. *Sinc*^{2} ↓*2* Down-Sampling Filter - Conventional Topology

The conventional topology of *sinc*^{2} ↓*2* down-sampling filter [5], [6] is shown in Fig. 3.1(a). Fig. 3.1(b) shows its clock time diagram. The capacitor discharge switches are not shown for simplification. The sampling rate at the input is chosen to be 500MHz.

The signal current is integrated for a time window of 2ns on each capacitor pair. The signal charge, integrated in phase *p1* and *p3* on a single unit capacitor *Cs*, and on two unit capacitors during *p2* is read out during phase *p4*. Similarly, the charge during *p3*, *p4* and *p1* is read out during *p2*. A total of four capacitors are connected together and readout simultaneously during each sampling phase.

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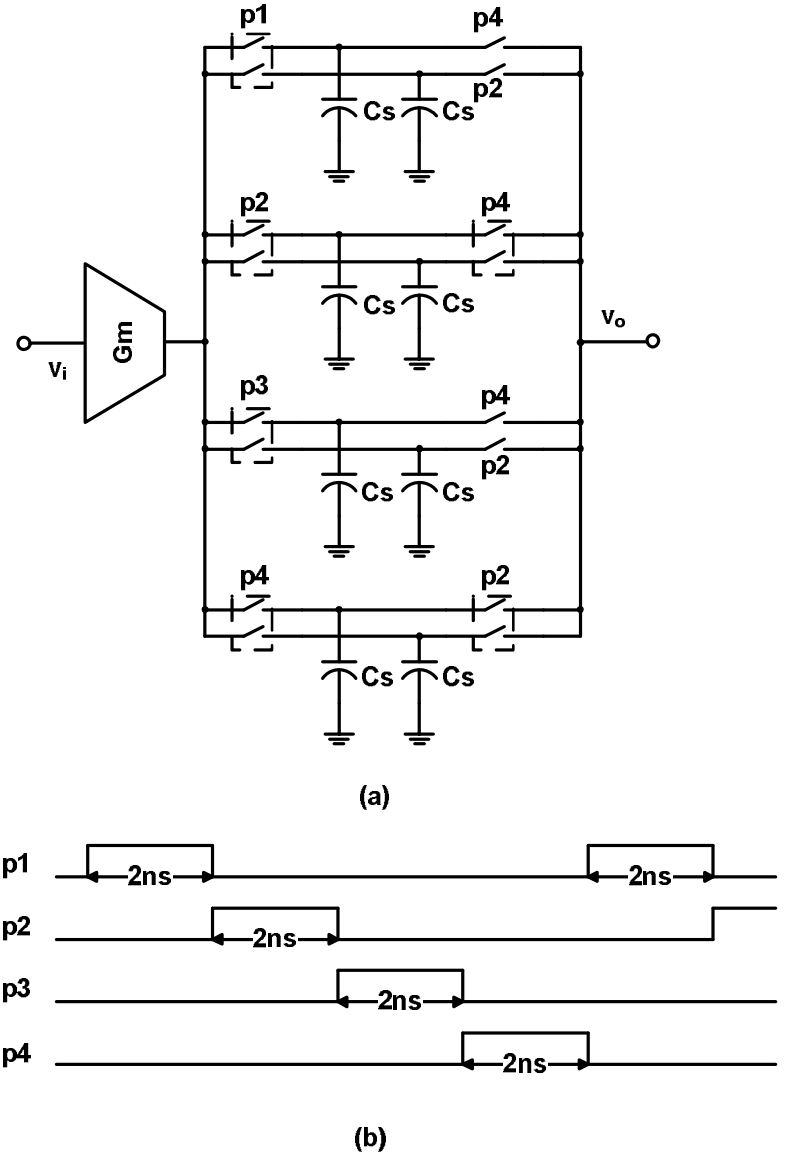

Fig. 3.1. (a) Conventional topology for *sinc*^{2} ↓2 filter [5], [6] (b) Clock time diagram.

The filter transfer function can be written in Z-domain as,

$$H(z) = \frac{1}{4}\left(1 + 2z^{-1} + z^{-2}\right) \tag{3.1}$$

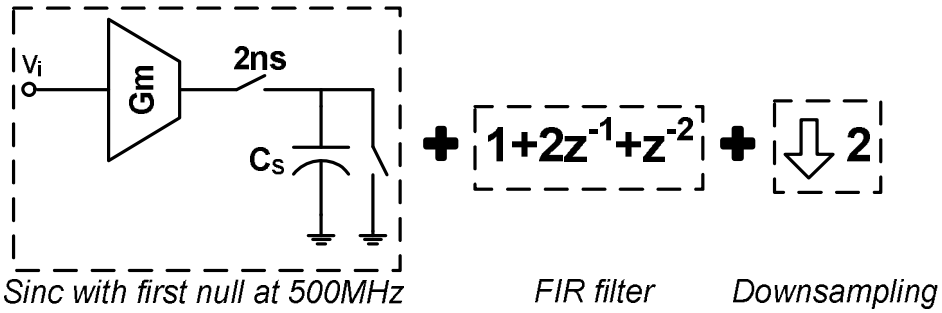

Fig. 3.2. Step by step explanation for conventional *sinc*^{2} ↓2 filters.

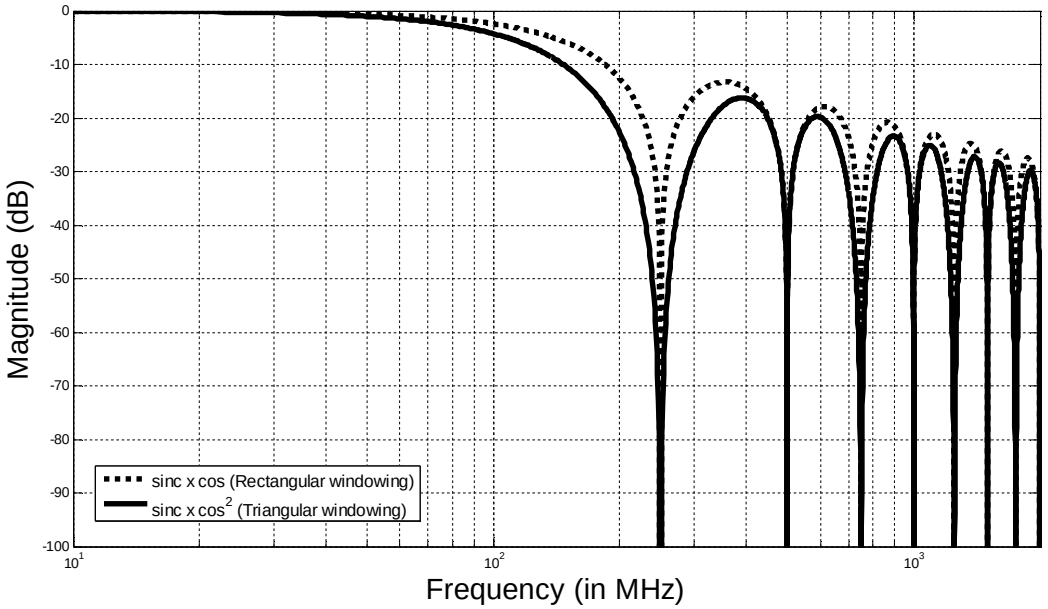

Fig. 3.3. Comparison of magnitude response of rectangular and triangular windowing. When decimated by 2, the components at 250MHz, 750MHz aliases to DC.

The factor 1/4 comes from the fact that four unit capacitors are connected together during readout. The windowed integration for 2ns will create a *sinc* filter with first null at 500MHz. The filter magnitude response for $H(z)$ is $cos^2(\pi f \Delta t)$ where Δt=2ns which will have two zeros at $fs/2$.

The operation of the filter is explained in Fig. 3.2. The overall filter response will be a cascade of the two filter responses mentioned before and is plotted in Fig. 3.3. The

wider nulls at 250MHz, 750MHz and so on, are due to the cos^2 filter magnitude response as explained in Chapter II.

B. $Sinc^2 \downarrow 2$ Down-Sampling Filter - Proposed Topology

The proposed topology for the down-sampling filter is shown in Fig. 3.4 along with the clock diagram. An extra overlap capacitor, *Cov* is added along with the sampling capacitors *Cs*. The size of the overlap capacitor is equal to that of the sampling capacitor. The operation of the filter is as follows. During first 2ns, the current is integrated on *Cs* and *Cov*. For the next 2ns, the overlap capacitor is disconnected while the sampling capacitor continues to integrate the charge. As the capacitance seen by the transconductor is now half the value compared to first 2ns, the voltage gain is now doubled. In the meantime, *Cov* is connected to the other sampling capacitor for readout and discharge. The same process is carried out on the other sampling capacitor and the overlap capacitor reconnects to the first sampling capacitor for readout. Switches *d1* and *d2* discharge the sampling capacitors after readout through switches *s1* and *s2*.

Effectively, the integration window in steady state looks like a stepwise approximation of a triangular window as shown in Fig. 3.5. The filter response of such a window can be easily plotted and it matches with the response of the conventional filter shown in Fig. 3.3.

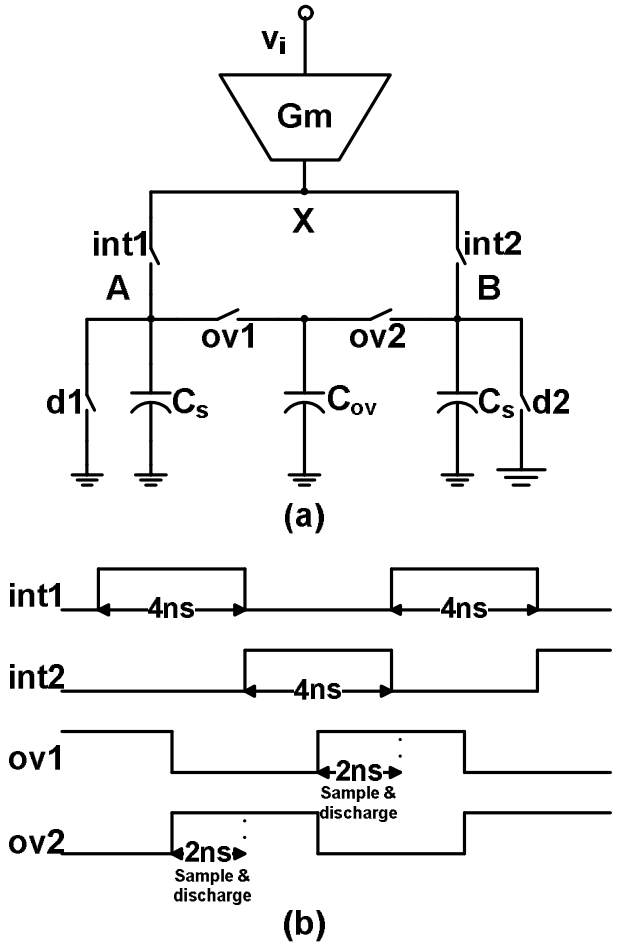

Fig. 3.4. Novel topology for the implementation of overlap (b) Clock scheme for the topology.

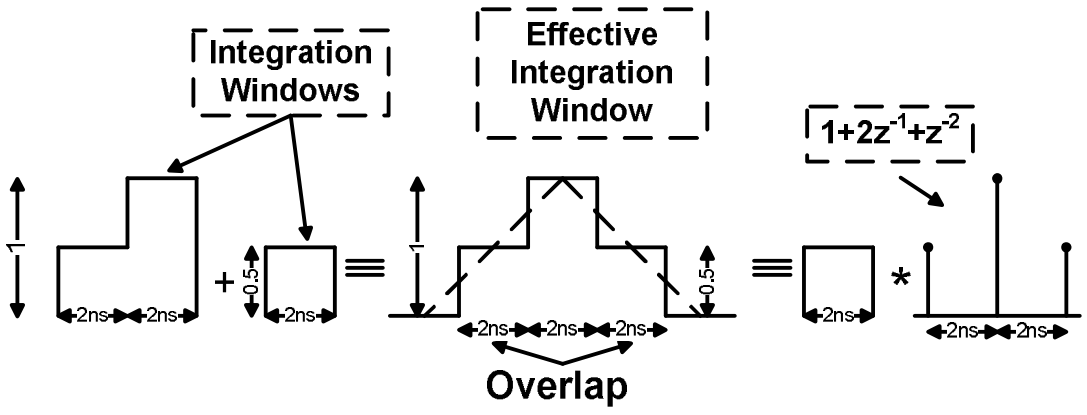

Fig. 3.5. Effective integration window for the proposed filter and its correspondence to the required function.

C. Comparison of Performance of the Two Filters

(i) Area Savings

For both filter topologies, the size of the unit sampling capacitor is determined by the noise requirements at the output. For the same peak to peak voltage range and the same SNR specification, the relation between the sampling capacitor size and transconductance value of the topologies can be determined.

The total integrated noise of the windowed integration sampling circuit is given by [7],

$$N = \frac{KT * 2Gm\Delta t}{Cs^2} \tag{3.2}$$

where K is the Boltzman constant, T is the absolute temperature, Gm is the transconductance of the amplifier, Cs is the value of sampling capacitor, Δt is the integration window duration. This expression holds under the condition that $\Delta t << Csrout$, where $rout$ is the output impedance of the transconductor. In the expression for channel noise of MOS device $\overline{i_n}^2 = 4KT\gamma gm$ adopted in (3.2), γ is assumed to be 1 for simplicity. Derivation of (3.2) is included in Appendix A. The gain of the sampling circuit is given by (3.3).

$$G = \frac{Gm\Delta t}{Cs} \tag{3.3}$$

Gm_{conv} and Cs_{conv} denote the transconductance and sampling capacitor values of the conventional topology and Gm_{prop} and Cs_{prop} for the proposed topology, respectively.

To get the same SNR, the signal gain and overall noise of both the samplers should be the same. If the noise is reduced by increasing the capacitance, then *Gm* needs to be increased proportionally to keep the gain and hence the output peak to peak range constant. From the noise expression, it can be seen that, integrated output noise is inversely proportional to square of the sampling capacitor and proportional to *Gm*. Therefore, the total noise reduces and overall SNR increases.

In the conventional topology, three windows of 2ns are added together with a scaling factor of 1/4 due to charge sharing. It can be seen that only half of the current is integrated on each sampling capacitor. This means that the effective transconductance for each capacitor will be half of the actual value, i.e., $Gm_{conv}/2$.

$$G_{conv} = \frac{1}{4}\left(\frac{Gm_{conv}\Delta t}{2Cs_{conv}} + \frac{2Gm_{conv}\Delta t}{2Cs_{conv}} + \frac{Gm_{conv}\Delta t}{2Cs_{conv}} \right) = \frac{1}{2}\left(\frac{Gm_{conv}\Delta t}{Cs_{conv}} \right) \tag{3.4}$$

In case of our proposed topology, the signal integrates on $2Cs_{prop}$ for the first 2ns, then integrates on Cs_{prop} for the next 2ns and finally again integrates on $2Cs_{prop}$ for the last 2ns. A factor of 1/2 is introduced during the readout operation. Therefore,

$$G_{prop} = \frac{1}{2}\left(\frac{Gm_{prop}\Delta t}{2Cs_{prop}} + \frac{Gm_{prop}\Delta t}{Cs_{prop}} + \frac{Gm_{prop}\Delta t}{2Cs_{prop}} \right) = \left(\frac{Gm_{prop}\Delta t}{Cs_{prop}} \right) \tag{3.5}$$

Equating (3.4) and (3.5) yields,

$$\frac{1}{2}\left(\frac{Gm_{conv}}{Cs_{conv}} \right) = \left(\frac{Gm_{prop}}{Cs_{prop}} \right) \tag{3.6}$$

Similarly the noise for each topology can be calculated as,

$$N_{conv} = \frac{2KT}{16}\left(\frac{Gm_{conv}\Delta t}{4Cs_{conv}^2} + \frac{Gm_{conv}\Delta t}{Cs_{conv}^2} + \frac{Gm_{conv}\Delta t}{4Cs_{conv}^2} \right) = \frac{3KT}{16}\left(\frac{Gm_{conv}\Delta t}{Cs_{conv}^2} \right) \tag{3.7}$$

The factor of 16 here is the square of the gain 1/4.

$$N_{prop} = \frac{2KT}{4}\left(\frac{Gm_{prop}\Delta t}{4Cs_{prop}^2} + \frac{Gm_{prop}\Delta t}{Cs_{prop}^2} + \frac{Gm_{prop}\Delta t}{4Cs_{prop}^2}\right) = \frac{3KT}{4}\left(\frac{Gm_{prop}\Delta t}{Cs_{prop}^2}\right) \tag{3.8}$$

The factor of 4 here is the square of the gain 1/2. Equating (3.7) and (3.8),

$$\frac{1}{4}\left(\frac{Gm_{conv}}{Cs_{conv}^2}\right) = \left(\frac{Gm_{prop}}{Cs_{prop}^2}\right) \tag{3.9}$$

Substituting (3.6) in (3.9),

$$Cs_{prop} = 2Cs_{conv} \tag{3.10}$$

$$Gm_{prop} = Gm_{conv} \tag{3.11}$$

The total area in the conventional filter is $8Cs_{conv}$ (Fig. 3.1(a)), whereas it is only $3Cs_{prop}$ (Fig. 3.4(a)) for the proposed filter. Therefore, 25% of the area from the dominant area consuming factor, the sampling capacitors, can be saved in the proposed filter when compared to the conventional filter.

(ii) Benefit of Linearity in Proposed Topology

The basic passive integrator consisting of just an integrator driving a capacitor has some certain disadvantages. In addition to sampling capacitor *Cs*, it has parasitic capacitance C_{par} (Fig. 3.6), which is the result of parasitic diodes, overlaps, crossings, strays and fringing effects [8]. The voltage dependence of the parasitic capacitance makes the response sensitive to power supply variations and degrades the distortion performance [8], [9]. Also, the finite output impedance of the Gm stage gets modulated by the swing of the voltage signal at its output. This creates non-linearity in the overall performance.

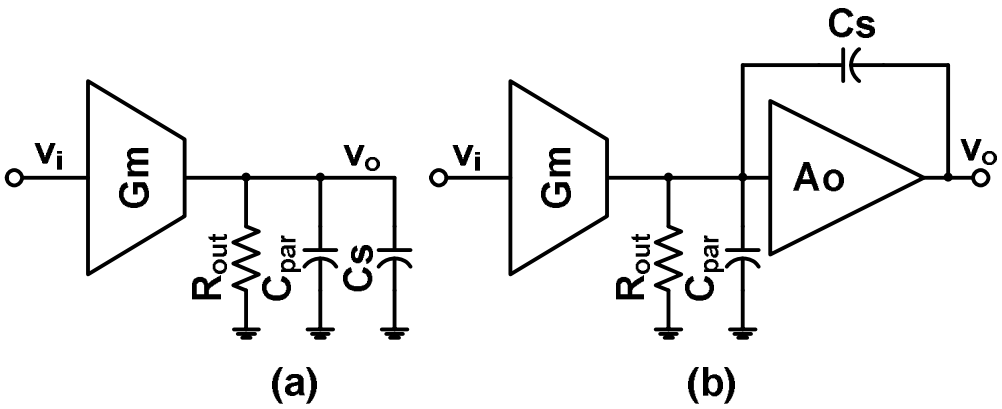

Fig. 3.6. (a) Basic passive integrator (b) Active integrator.

The above mentioned problem can be dealt with by using an active integrator based sampler as shown in Fig. 3.6 at the cost of power consumption and complexity.

For $A_o \rightarrow \infty$, the effect of C_{par} and R_{out} is neglected. The use of an active integrator can be well justified for the application discussed in this thesis. Here the signal is at baseband where the above benefits can be obtained without spending much power. In charge sampling circuits, usually a buffer is required before the ADC to drive low impedance. Here the OTA provides driving capability and hence the output can be read out directly at the sampling capacitor. Fig. 3.7 shows the block diagram of $sinc^2 \downarrow 2$ filter implemented with active integrator and Fig. 3.4(b) shows its clock scheme. In fig. 3.7, V_{cmi} and V_{cmo} denote the input and output common voltages of the OTA used for active integration respectively.

The benefits of active integration are obtained in the proposed topology only because the current is integrated at and read out from only two nodes. This is applicable for any order of decimation filter in the proposed topology. In the conventional topology, current is integrated and read out from multiple capacitors and depending on the order of

down-sampling, it varies. This complicates the active integration implementation and increases power consumption.

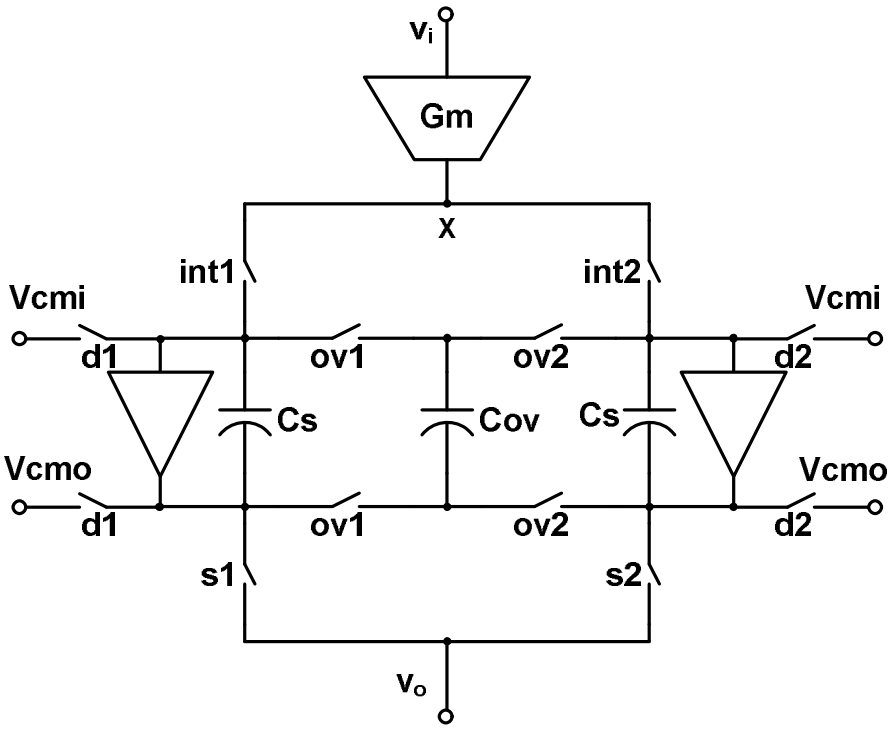

Fig. 3.7. *Sinc*^{2} ↓2 filter implemented with active integrator.

D. Simulation Results

Prototype filters of the conventional and proposed technique are simulated in 45nm technology and the results are compared. A differential version of the filter is shown in Fig. 3.8. A PMOS input fully differential folded cascode structure with active common mode feedback is used as Gm-stage (Fig. 3.9). For a fair comparison, the same Gm-stage is used for both the topologies. The specification of the transconductor is given in Table 3.1.

Table 3.1. Specification of the transconductor

Specification	Value
Gm	665.65 μA/V
r_{out}	818 KΩ
Integrated Input Referred Noise (0-20MHz)	18.36 nV^2
Maximum Differential Input Signal (THD = 5% @ 20MHz)	83.2094 mV
Excess Phase @ 20MHz	2^o
Supply Voltage	1.2 V
Current Consumption	282 μA

Ideally a transconductor with infinite output impedance is needed. Finite output impedance might limit either the null depth or null bandwidth [5]. If the signal is at DC with a bandwidth of Δf, depending on the requirement of attenuation of the aliasing signal, the value of r_{out} is chosen.

The Gain, Linearity and NF of the filter are mainly determined by the transconductor. In order to arrive at the required value of these parameters for the filter, various factors need to be considered. Some of them are:

1) SNR requirement of the receiver for each standard under consideration
2) Linearity Requirement of the receiver
3) Gain, Noise Figure and Linearity Allocation to LNA and Mixer
4) Blocker's profile

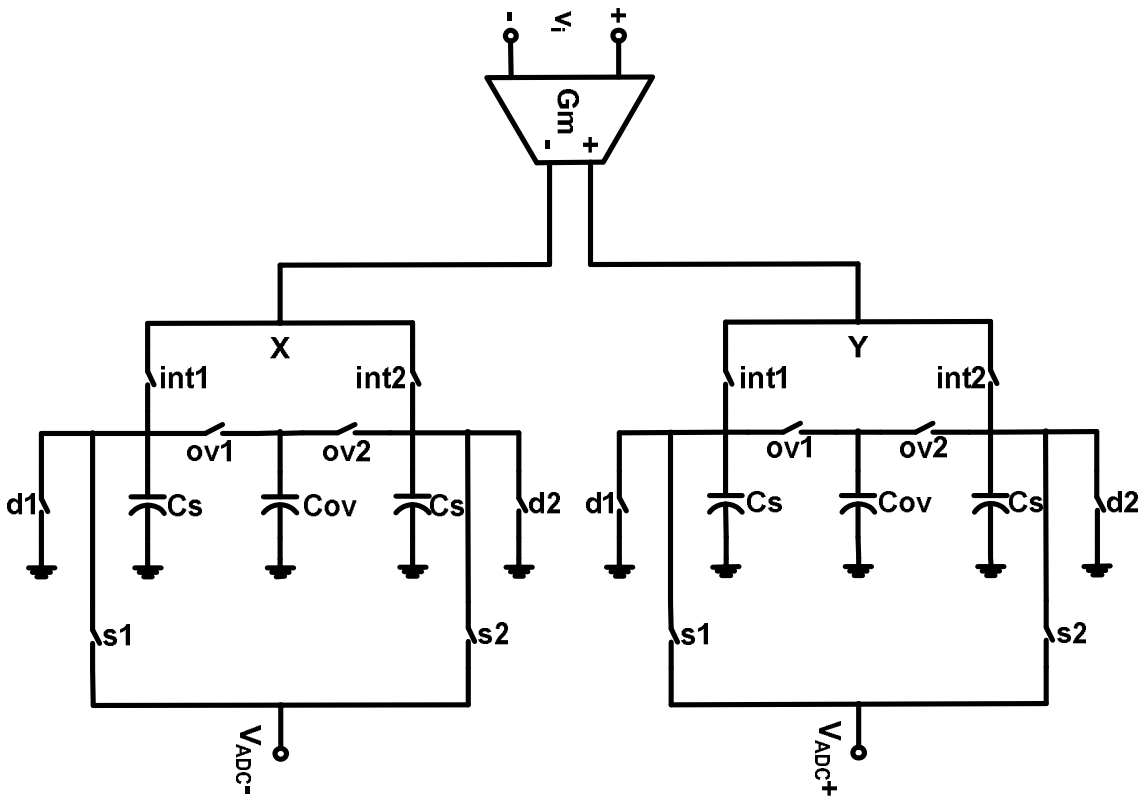

Fig. 3.8. Differential implementation of the filter.

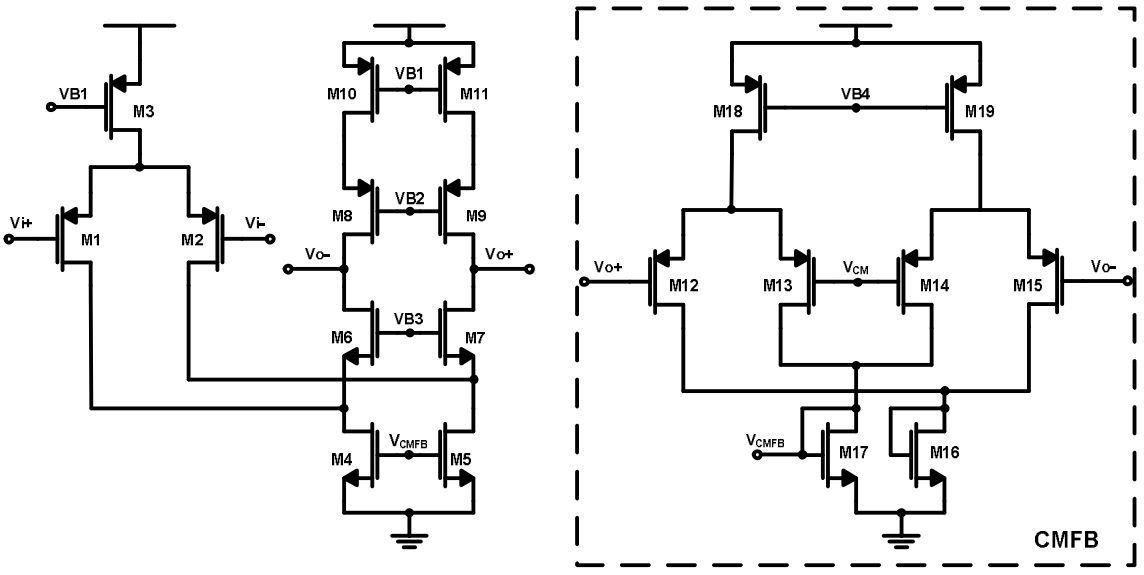

Fig. 3.9. Gm-stage: Folded-cascode topology.

The aim is to show that the proposed filter occupies less area on sampling capacitors when compared to the conventional filter. For a fair comparison in simulations, active integration is not used for proposed topology.

Channel Bandwidth and Blocker's profile determines the clock frequency. For example, in the analysis carried out in Chapter III of [1], the initial sampling rates of the two extreme cases of bandwidths, GSM (200KHz) and 802.11g (20MHz) are taken to be 72MHz and 480MHz respectively. Here, a sampling frequency of 500MHz is assumed for comparison of the two topologies.

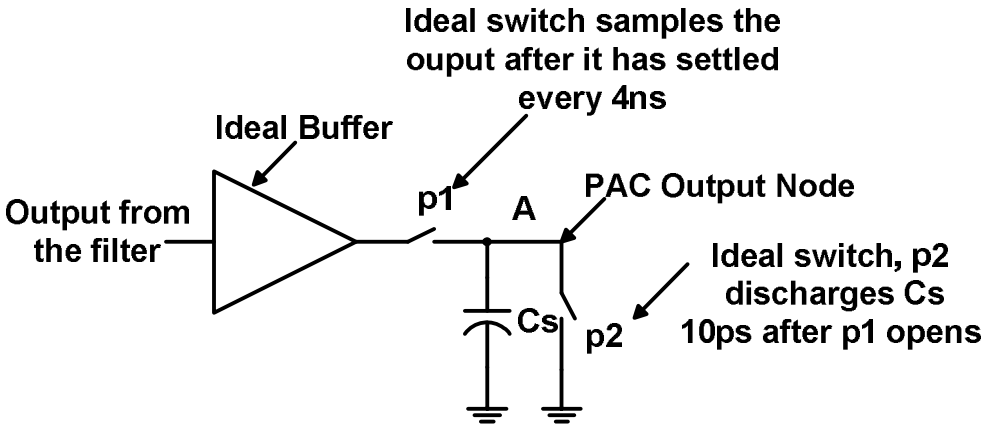

Fig. 3.10. Setup for finding the transfer function of the filter using PAC analysis.

PAC analysis of Spectre is used to find the transfer function of the discrete-time filters. In discrete-time filters, the output is valid only at one instant of time every *Ts* (here 4ns). For the remaining duration, the output is some random value. If PAC analysis is used directly at the output node to find the transfer function, the response obtained would not be accurate [10]. Ref [10] suggests sampling the output at the required instant and holding it for *Ts=4ns* using ideal analog blocks in Spectre. This is a useful

simulation technique for switched capacitor circuits where the frequency of interest, *f<<1/Ts*. In charge sampling circuits, in order to find the null performance, the frequency of interest also includes *f=1/Ts, 2/Ts* and so on. As suggested in [10], if the output is sampled and held for 4ns, then it is equivalent to multiplying the response of the filter with a *sinc* filter having null at 250MHz, which is the frequency where null of the discrete time filter also occur. The two nulls get mixed up and cannot be differentiated. The solution is to sample the output at the required instant every 4ns using ideal switches, discharge the output immediately (say, after 10ps) and find PAC at this node. This is equivalent to multiplying the output with a *sinc* having null at 100GHz (=1/10ps) and the response of the *sinc* is almost a straight line in the frequency of interest (0-250MHz). The simulation setup is shown in Fig. 3.10.

The Magnitude Responses of the proposed and conventional filter are shown in Fig. 3.11 and their phase responses are shown in Fig. 3.12.

Table 3.2 shows the summary of results. The filter responses are very nearly identical, with some small degradation in the null attenuation at 20MHz.

Table 3.2. Summary of simulation results

Specification	**Conventional Filter**	**Proposed Filter**
Null attenuation for 20 MHz	41.55 dB	38.26 dB
Integrated Output Noise (0-20MHz)	25.02 nV^2	25.66 nV^2
THD (1mV sine, 20MHz)	0.972%	0.972%
Overall Capacitor for sampling	8pF	6pF

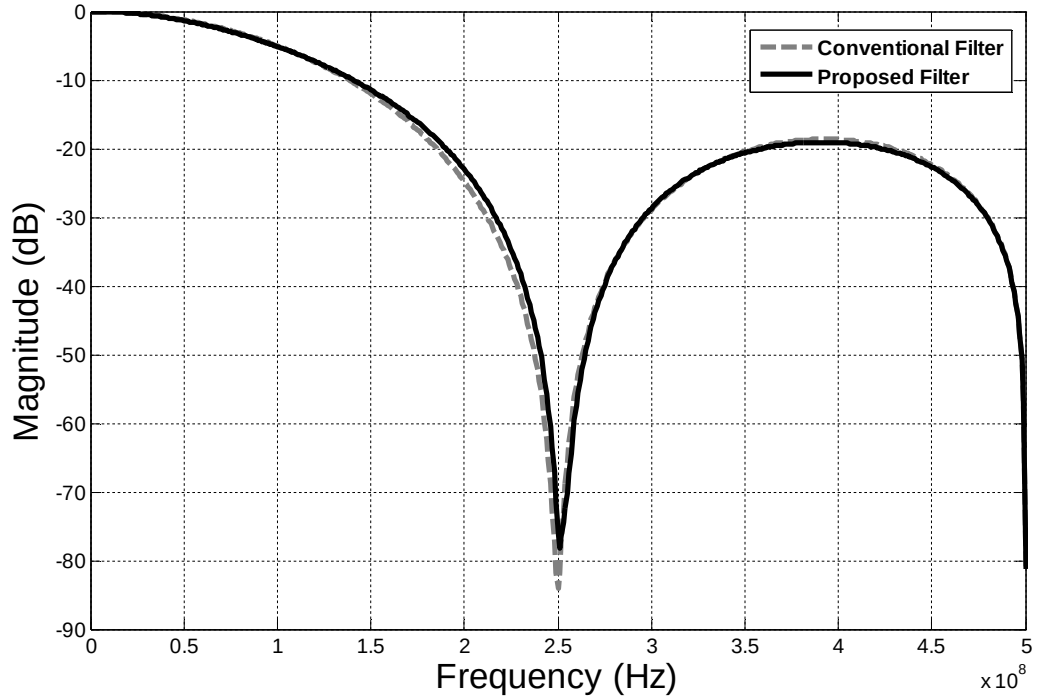

Fig. 3.11. Magnitude response of conventional and proposed filter using PAC analysis in Spectre.

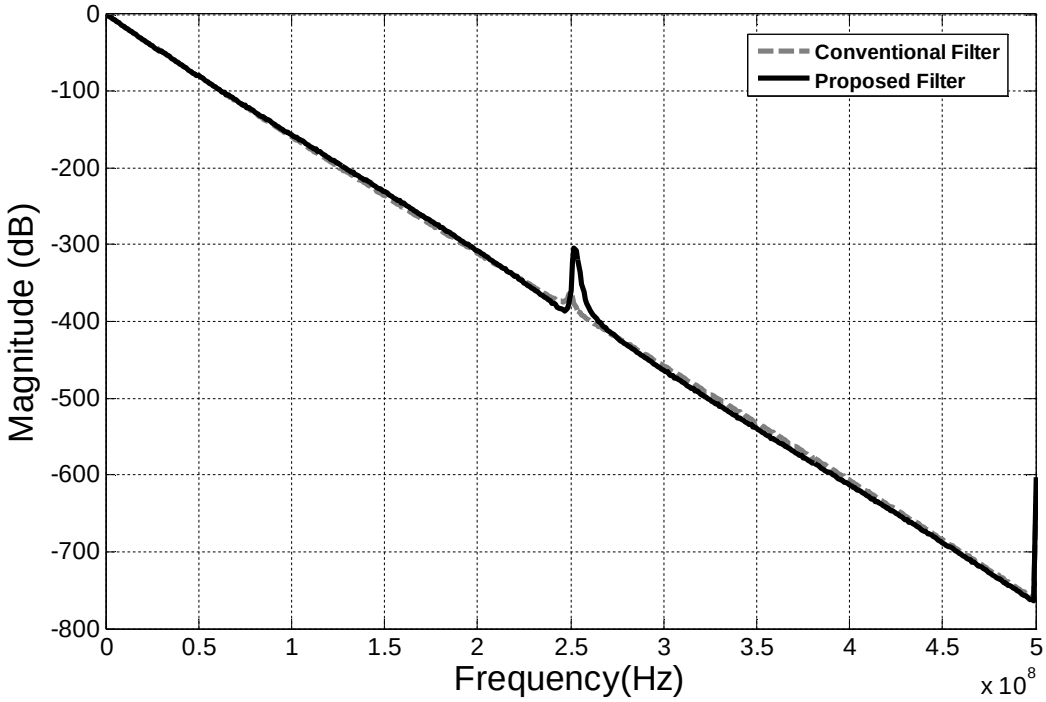

Fig. 3.12. Comparison of phases responses using PAC analysis in Spectre.

CHAPTER IV

EXTENSION OF THE PROPOSED TOPOLOGY TO ACHIEVE HIGHER DOWN-SAMPLING FACTOR*

There are cases where it is needed to integrate and sample the signal at a very high frequency to achieve the required null attenuation. In such a case, it is necessary to down-sample by a higher factor. In this chapter, the implementation of $sinc^2 \downarrow N$ filter using the proposed topology is discussed and compared with the conventional topology.

A. Comparison of the Topologies for $sinc^2 \downarrow 4$

The conventional topology for the implementation of $sinc^2 \downarrow N$ is just a straight forward extension of $sinc^2 \downarrow 2$ (Fig. 3.1(a)). Fig. 4.1 shows $sinc^2 \downarrow 4$ using the conventional topology [5]. The readout switches *s1* & *s2* and discharge switches *d1* & *d2* are not shown in the figure.

Fig. 4.2(a) shows the implementation with proposed topology and Fig. 4.2(b) shows the clock time diagram. It is assumed that input sampling frequency is 500MHz.

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*Part of this chapter is reprinted with permission from "A Discrete-Time Downsampling FIR Filter for Windowed Integration Samplers," by Karthik Raviprakash, Mandar Kulkarni, Xi Chen, Sebastian Hoyos, and Brian M. Sadler, 2009, International Journal of Microwave Science and Technology, vol. 2009, Article ID 758783.

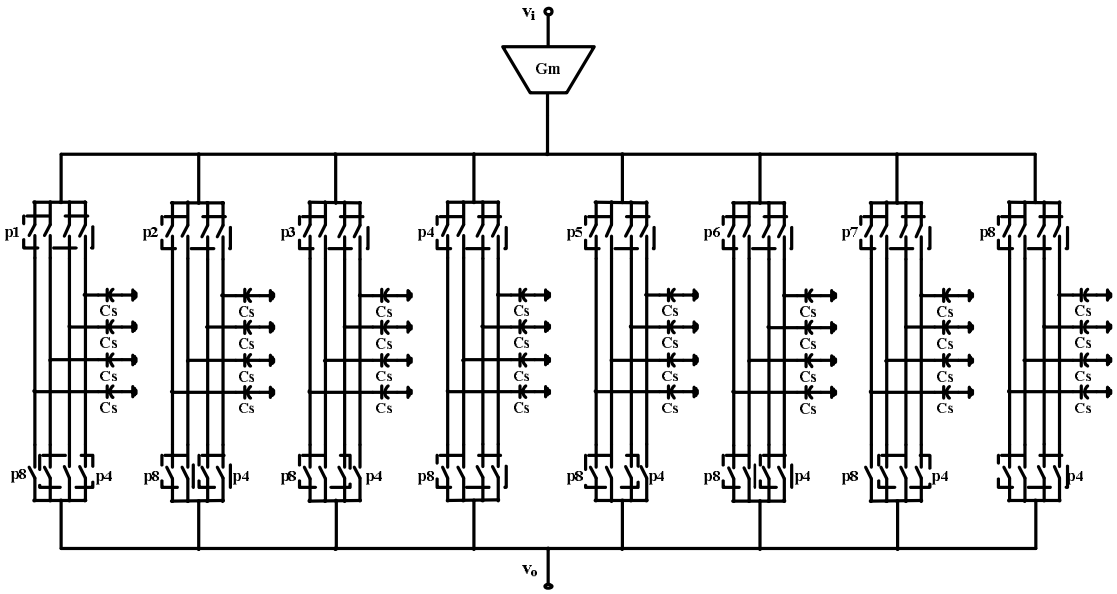


Fig. 4.1. *sinc*^{2} ↓4 filter – conventional topology.

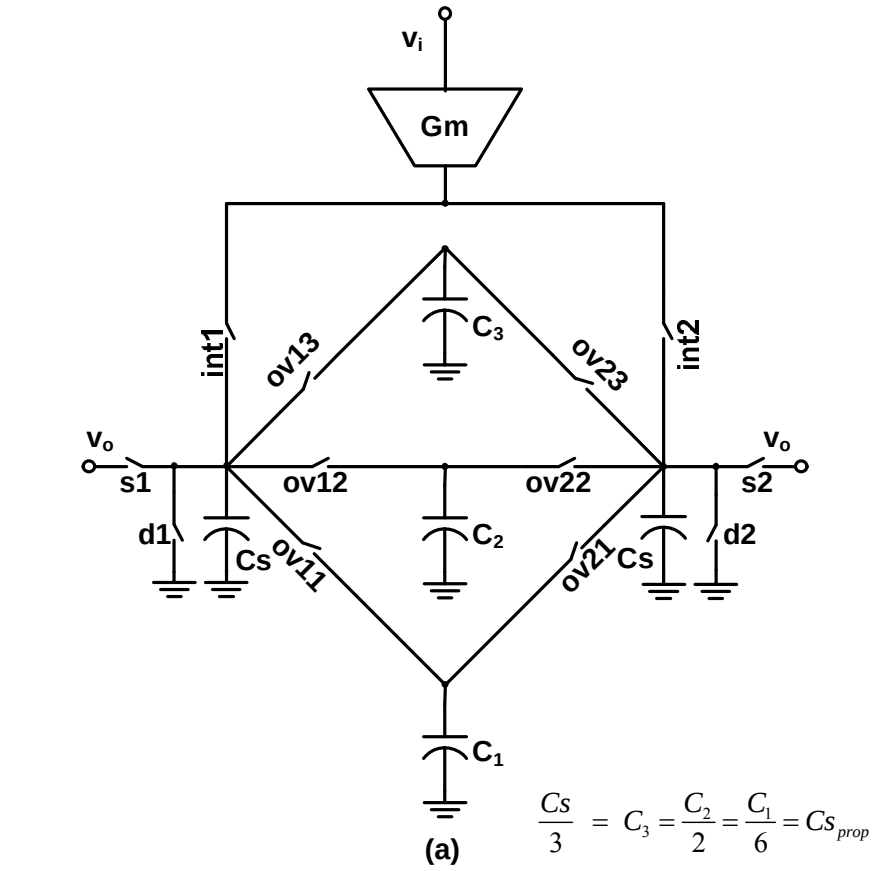
For Conventional Topology,

$$G_{conv} = \frac{1}{16}\left(2\frac{Gm_{conv}\Delta t}{4Cs_{conv}} + 2\frac{2Gm_{conv}\Delta t}{4Cs_{conv}} + 2\frac{3Gm_{conv}\Delta t}{4Cs_{conv}} + \frac{4Gm_{conv}\Delta t}{4Cs_{conv}}\right) = \frac{1}{4}\left(\frac{Gm_{conv}\Delta t}{Cs_{conv}}\right) \tag{4.1}$$

For Proposed Topology,

$$G_{prop} = \frac{1}{12Cs_{prop}}\left(Q_A + Q_{C1} + Q_{C2} + Q_{C3}\right) \tag{4.2}$$

where $Q_A, Q_{C1}, Q_{C2}, Q_{C3}$ are the charge stored in capacitors Cs, C1, C2, C3 respectively



$$\frac{Cs}{3} = C_3 = \frac{C_2}{2} = \frac{C_1}{6} = Cs_{prop}$$

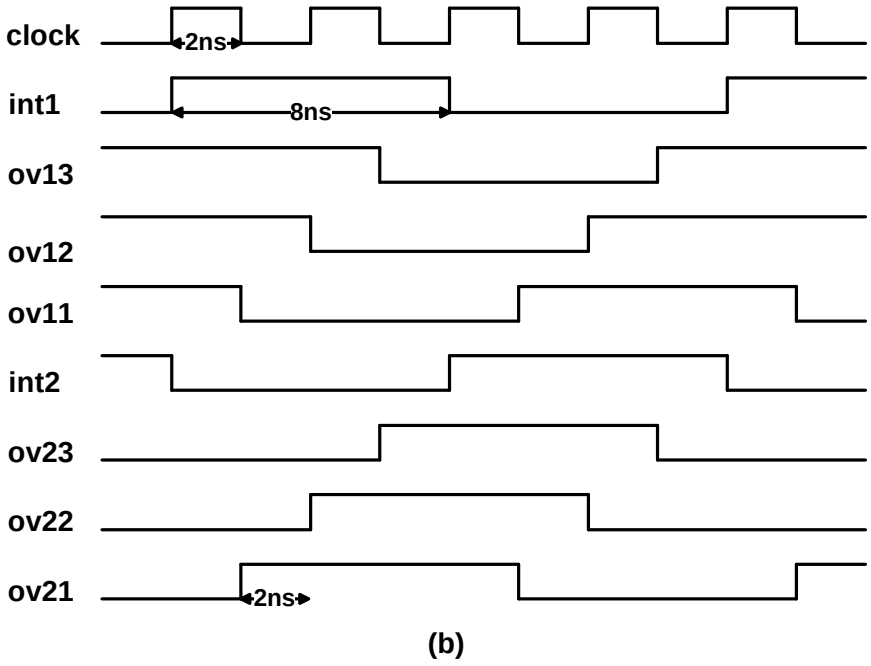


Fig. 4.2. (a) *sinc*^{2} ↓4 filter – proposed topology (b) Clock time diagram.

$$G_{prop} = \frac{1}{12Cs_{prop}} \left[\begin{array}{l} \left\{ 3Cs_{prop} \left(\frac{Gm_{prop}\Delta t}{12Cs_{prop}} + \frac{Gm_{prop}\Delta t}{6Cs_{prop}} + \frac{Gm_{prop}\Delta t}{4Cs_{prop}} + \frac{Gm_{prop}\Delta t}{3Cs_{prop}} \right) \right\} + \\ \left\{ 6Cs_{prop} \left(\frac{Gm_{prop}\Delta t}{12Cs_{prop}} \right) \right\} + \\ \left\{ 2Cs_{prop} \left(\frac{Gm_{prop}\Delta t}{12Cs_{prop}} + \frac{Gm_{prop}\Delta t}{6Cs_{prop}} \right) \right\} + \\ \left\{ Cs_{prop} \left(\frac{Gm_{prop}\Delta t}{12Cs_{prop}} + \frac{Gm_{prop}\Delta t}{6Cs_{prop}} + \frac{Gm_{prop}\Delta t}{4Cs_{prop}} \right) \right\} \end{array} \right] \quad (4.3)$$

$$= \frac{1}{3} \left(\frac{Gm_{prop}\Delta t}{Cs_{prop}} \right)$$

Equating (4.1) and (4.3),

$$\left(\frac{Gm_{conv}}{Cs_{conv}} \right) = \frac{4}{3} \left(\frac{Gm_{prop}}{Cs_{prop}} \right) \quad (4.4)$$

Noise of the two topologies can be derived as shown below,

$$\begin{aligned} N_{conv} &= \left(\frac{2KT}{256} \right) \left[2\frac{Gm_{conv}\Delta t}{16Cs_{conv}^2} + 2\frac{4Gm_{conv}\Delta t}{16Cs_{conv}^2} + 2\frac{9Gm_{conv}\Delta t}{16Cs_{conv}^2} + \frac{16Gm_{conv}\Delta t}{16Cs_{conv}^2} \right] \\ &= \left(\frac{2KT}{256} \right) \left(\frac{44Gm_{conv}\Delta t}{16Cs_{conv}^2} \right) \end{aligned} \quad (4.5)$$

Proceeding in the same way, the noise of the proposed filter is found to be,

$$N_{prop} = \left(\frac{2KT}{144} \right) \left(\frac{396Gm_{prop}\Delta t}{144Cs_{prop}^2} \right) \quad (4.6)$$

Equating (4.5) and (4.6),

$$\left(\frac{1}{256} \right) \left(\frac{44Gm_{conv}}{16Cs_{conv}^2} \right) = \left(\frac{1}{144} \right) \left(\frac{396Gm_{prop}}{144Cs_{prop}^2} \right) \quad (4.7)$$

$$\left(\frac{Gm_{conv}}{Cs_{conv}^2} \right) = \left(\frac{4}{3} \right)^2 \left(\frac{Gm_{prop}}{Cs_{prop}^2} \right) \quad (4.8)$$

Using (4.4) and (4.8),

$$Gm_{prop} = Gm_{conv} \tag{4.9}$$

$$Cs_{prop} = \frac{4}{3} Cs_{conv} \tag{4.10}$$

Referring to Fig. 4.1, Fig. 4.2(a) and (4.10),

$$\frac{Total\ Area\ of\ Proposed\ Filter}{Total\ Area\ of\ Conventional\ Filter} = \frac{15Cs_{prop}}{32Cs_{conv}} = \frac{20}{32} \tag{4.11}$$

$$Percentage\ of\ area\ savings = 37.5\% \tag{4.12}$$

B. Comparison of the Topologies for $sinc^2 \downarrow N$

The $sinc^2 \downarrow N$ filter using the proposed topology is shown in Fig. 4.3. Here the capacitors have to satisfy (4.13).

$$\begin{aligned}
C_{N-1} &= Cs_{prop} \\
Cs &= (N-1)Cs_{prop} \\
C_{N-2} &= \frac{N(N-1)}{(N-1)(N-2)} Cs_{prop} \\
C_{N-3} &= \frac{N(N-1)}{(N-2)(N-3)} Cs_{prop} \\
&\vdots \\
C_2 &= \frac{N(N-1)}{(2)(3)} Cs_{prop} \\
C_1 &= \frac{N(N-1)}{(1)(2)} Cs_{prop}
\end{aligned} \tag{4.13}$$

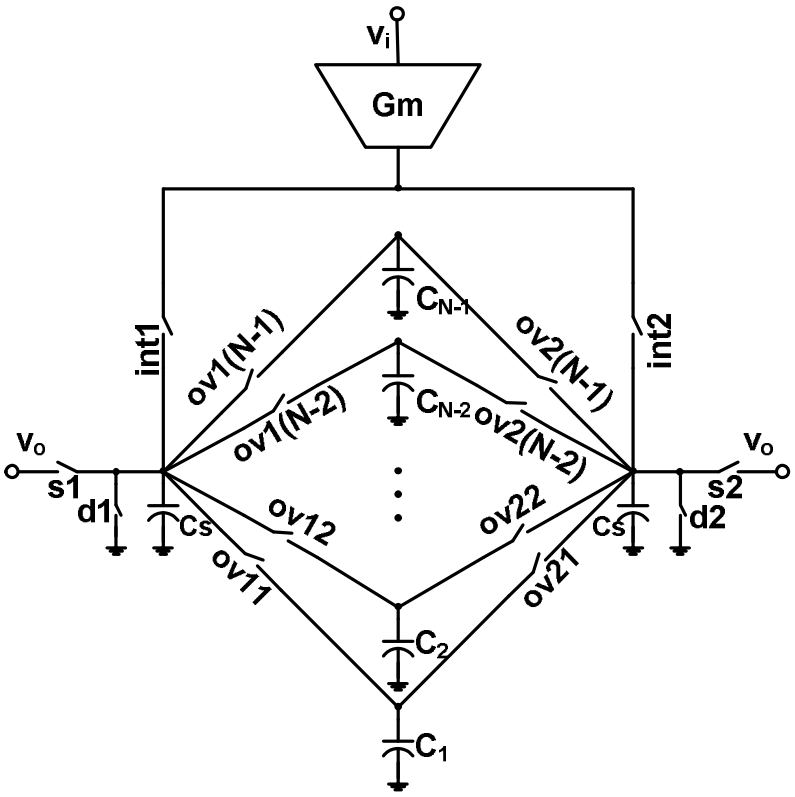


Fig. 4.3. *sinc*^{2} $\downarrow N$ filter – proposed topology.

The proposed and the conventional topologies can be compared as in section A.

$$G_{conv} = \frac{1}{N}\left(\frac{Gm_{conv}\Delta t}{Cs_{conv}}\right) \tag{4.14}$$

$$G_{prop} = \frac{1}{(N-1)}\left(\frac{Gm_{prop}\Delta t}{Cs_{prop}}\right) \tag{4.15}$$

Using (4.14) and (4.15),

$$\left(\frac{Gm_{conv}}{Cs_{conv}}\right) = \frac{N}{(N-1)}\left(\frac{Gm_{prop}}{Cs_{prop}}\right) \tag{4.16}$$

From noise calculations, it can be shown that,

$$\left(\frac{Gm_{conv}}{Cs_{conv}^2}\right) = \left(\frac{N}{N-1}\right)^2\left(\frac{Gm_{prop}}{Cs_{prop}^2}\right) \tag{4.17}$$

Using (4.16) and (4.17),

$$\frac{Cs_{prop}}{Cs_{conv}} = \frac{N}{N-1} \tag{4.18}$$

The total area required by the two filters is,

$$A_{conv} = 2N^2 Cs_{conv} \tag{4.19}$$

$$A_{prop} = \left(N^2 - 1\right) Cs_{prop} \tag{4.20}$$

Using (4.18), (4.19) and (4.20),

$$\begin{aligned} \%\ of\ \ area\ savings &= \frac{(A_{conv} - A_{prop})}{A_{conv}} x100\% \\ &= \frac{N-1}{2N} x100\% \end{aligned} \tag{4.21}$$

From (4.21), it can be noted that as the decimation factor is increased, the percentage of area saved compared to the conventional topology also increases. For large values of N, the area savings rapidly approaches 50%.

CHAPTER V

HIGHER ORDER SINC FILTERING*

In previous chapters, it was discussed that the attenuation provided by *sinc* filtering may not be sufficient for some applications and hence, the need for $sinc^2$ filtering. Literatures also discuss the need for higher order *sinc* attenuation [6]. A topology has been proposed to implement $sinc^3 \downarrow 2$ filter which saves 33% of the area on sampling capacitors when compared to the conventional topology.

The z-domain transfer function of $sinc^3$ FIR Filter can be described by (5.1). Fig 5.1 shows the weights applied on the sampled signals in a $sinc^3 \downarrow 2$ filter.

$$H(z) = (1 + z^{-1})^3 = 1 + 3z^{-1} + 3z^{-2} + z^{-3} \tag{5.1}$$

A. Conventional Implementation of $sinc^3 \downarrow 2$ Filter

The conventional implementation of $sinc^3 \downarrow 2$ filter [6] is shown in Fig. 5.2(a) and the clock time diagram is shown in Fig. 5.2(b). For illustration, the sampling frequency was set to be 500MHz. The discharge and read-out are not shown for simplification.

*Part of this chapter is reprinted with permission from "Reduced area discrete-time down-sampling filter embedded with windowed integration samplers," by K. Raviprakash, R. Saad, and S. Hoyos, 2010, Electronic Letters, vol. 46, Issue 12, p.828-830

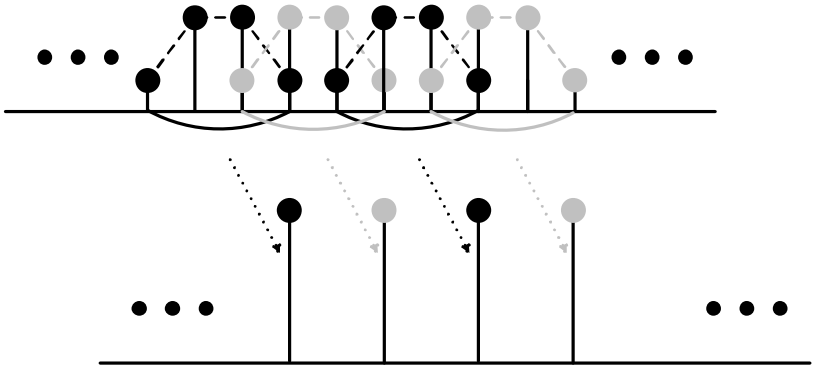


Fig. 5.1. *sinc*^{3} ↓2 filter operation.

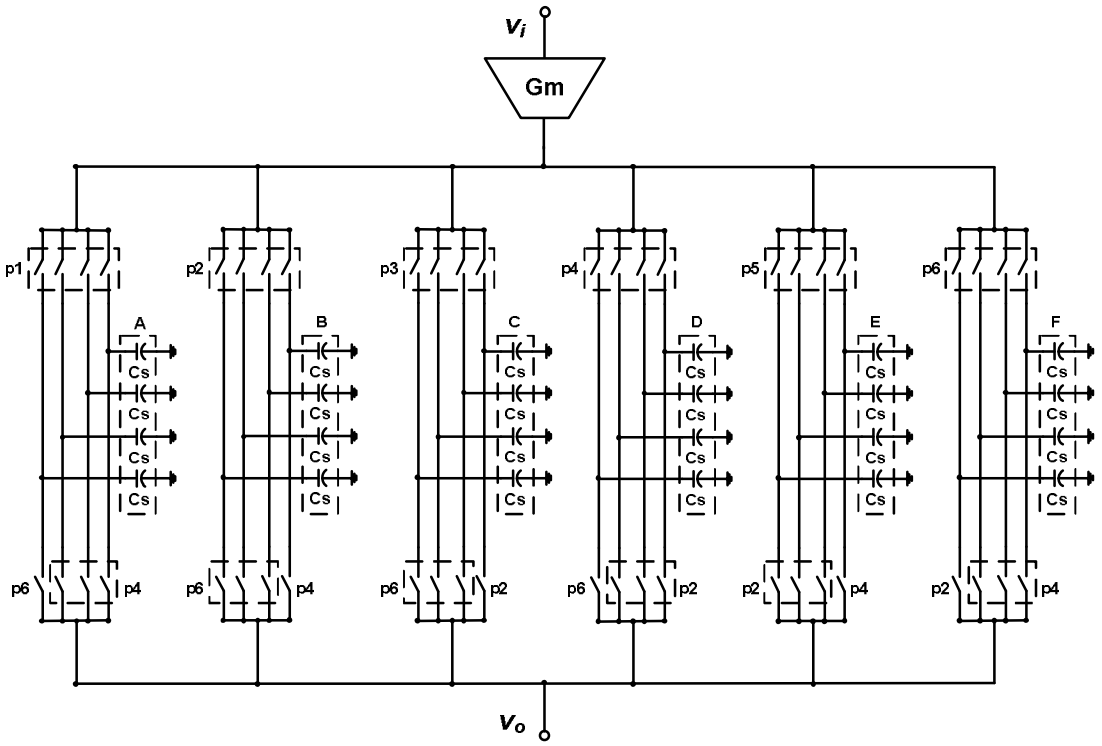
The sampling capacitors are all of the same value *Cs*. At *t=0ns*, the switches *p1* are closed and the signal current *Gmvi(t)* is integrated on the capacitor set *A*. At *t=2ns*, let *v1* be the voltage across the capacitors. At every *2ns*, the cycle is repeated in order for all the other capacitor sets. At *t=8ns*, let *v2, v3, v4* be the voltage across capacitor sets *B, C, D* respectively. one capacitor from the set *A*, three from set *B*, three from set *C* and one from set *D* are connected in parallel for read out (*t=10ns* to *t=12ns*) through switches *p6*. The output voltage sampled at *t=12ns* is given by (5.2),

$$vo\left(t=12ns\right)=\frac{v1+3v2+3v3+v4}{8} \tag{5.2}$$

v1, v2, v3 and *v4* can be viewed as the samples (*Ts = 2ns*) of windowed integration of *Gmvi(t)/2Cs* with a window duration of *Δt = 2ns*.

At *t=16ns*, capacitors from the sets *C, D, E,* and *F* are connected in the ratio 1:3:3:1 through switches *p2* and the output voltage sampled is given by (5.3),

$$vo\left(t=16ns\right)=\frac{v3+3v4+3v5+v6}{8} \tag{5.3}$$



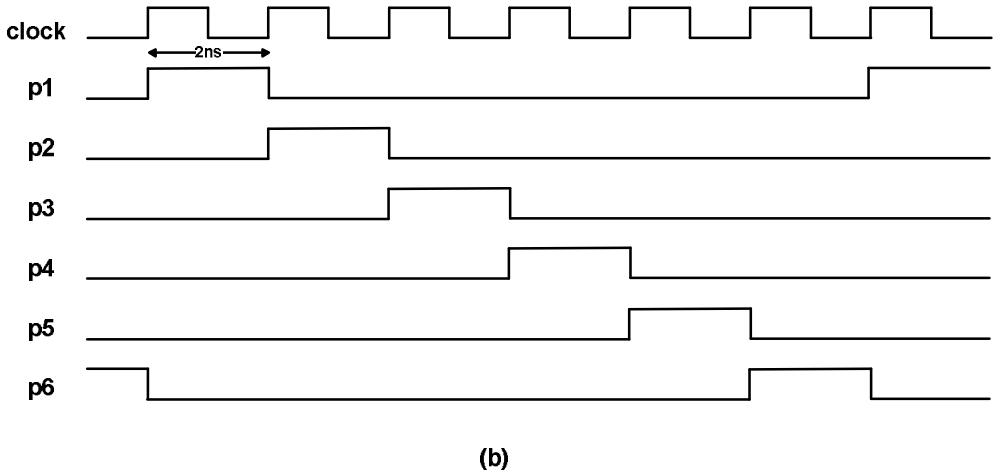


Fig. 5.2. (a) Conventional topology for $sinc^3 \downarrow 2$ (b) Clock time diagram for the topology.

Similarly, at *t=20ns*, the output voltage sample is,

$$vo(t = 20ns) = \frac{v5 + 3v6 + 3v7 + v8}{8} \tag{5.4}$$

From (5.2), (5.3) and (5.4), it is observed that the input signal *vi(t)* is sampled at every 2ns and the output is read at every 4ns. The signal transfer function can be defined by *H(z)* + ↓*2*, where *H(z)* is given by,

$$H(z) = \frac{1 + 3z^{-1} + 3z^{-2} + z^{-3}}{8} \tag{5.5}$$

The overall transfer function from *vi(t)* to *vo(2nTs)* is shown in Fig. 5.3.

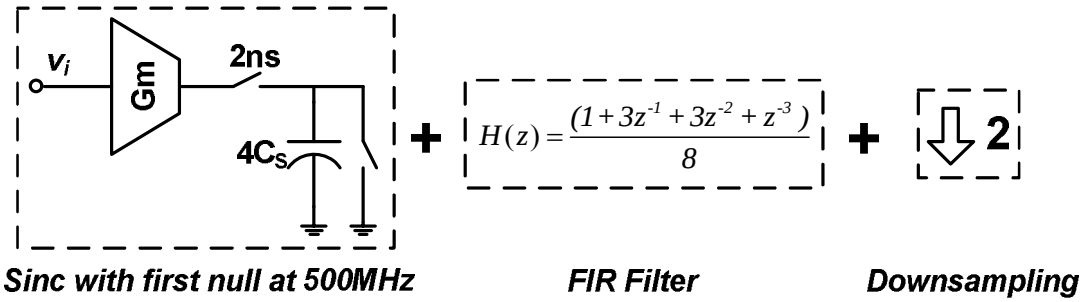


Fig. 5.3. The overall transfer function from input to output of the conventional topology.

B. Proposed Topology

Fig. 5.4 shows the proposed discrete-time filter topology and its clock time diagram. The sampling capacitors (C_{A1} through C_{D2}) are all of the same value *Cs*. At *t=2ns*, when switches s_A are closed, let *v1* be the voltage across the capacitor set *A* (C_{A1} *and* C_{A2}). Let *v2* be the voltage across capacitor set *B* (C_{B1} *and* C_{B2}) at *t=4ns*, when switches s_B are closed. Later, when s_X is ON, the charge across C_{A2} and C_{B1} redistributes so that the voltage across C_{A2} and C_{B1} is equal to *(v1+v2)/2*. Voltage across C_{B2} remains

as *v2*. The same set of operations are repeated for capacitor sets *C* (C_{C1} *and* C_{C2}) and *D* (C_{D1} *and* C_{D2}) and the voltage across C_{C1} is equal to *v3* and that across C_{C2} and C_{D1} is equal to *(v3+v4)/2*. When capacitor sets *B* and *C* are connected in parallel (switch s_{BC}) for read out, the output voltage sampled at *t=10ns* is defined by,

$$vo\left(t=10ns\right)=\frac{v1+3v2+3v3+v4}{8} \tag{5.6}$$

The set of operations are repeated for every 4ns and now when the capacitor set *D* and *A* are connected (switch s_{AD}) for readout, the output voltage sampled at *t=14ns* is given by,

$$vo\left(t=14ns\right)=\frac{v3+3v4+3v5+v6}{8} \tag{5.7}$$

If the signal transfer function is defined by *H(z)* + ↓*2*, then *H(z)* is given by,

$$H\left(z\right)=\frac{1+3z^{-1}+3z^{-2}+z^{-3}}{8} \tag{5.8}$$

The overall transfer function from input to output of the proposed topology is shown in Fig. 5.5.

C. Area Savings

Let's define Gm_{conv} and Cs_{conv} as the transconductance and sampling capacitor values of the conventional topology and Gm_{prop} and Cs_{prop} for the proposed topology respectively. Referring to Fig. 5.2, Gain G_{conv} of the conventional topology is given by,

$$G_{conv}=\frac{Gm_{conv}\Delta t}{4Cs_{conv}} \tag{5.9}$$

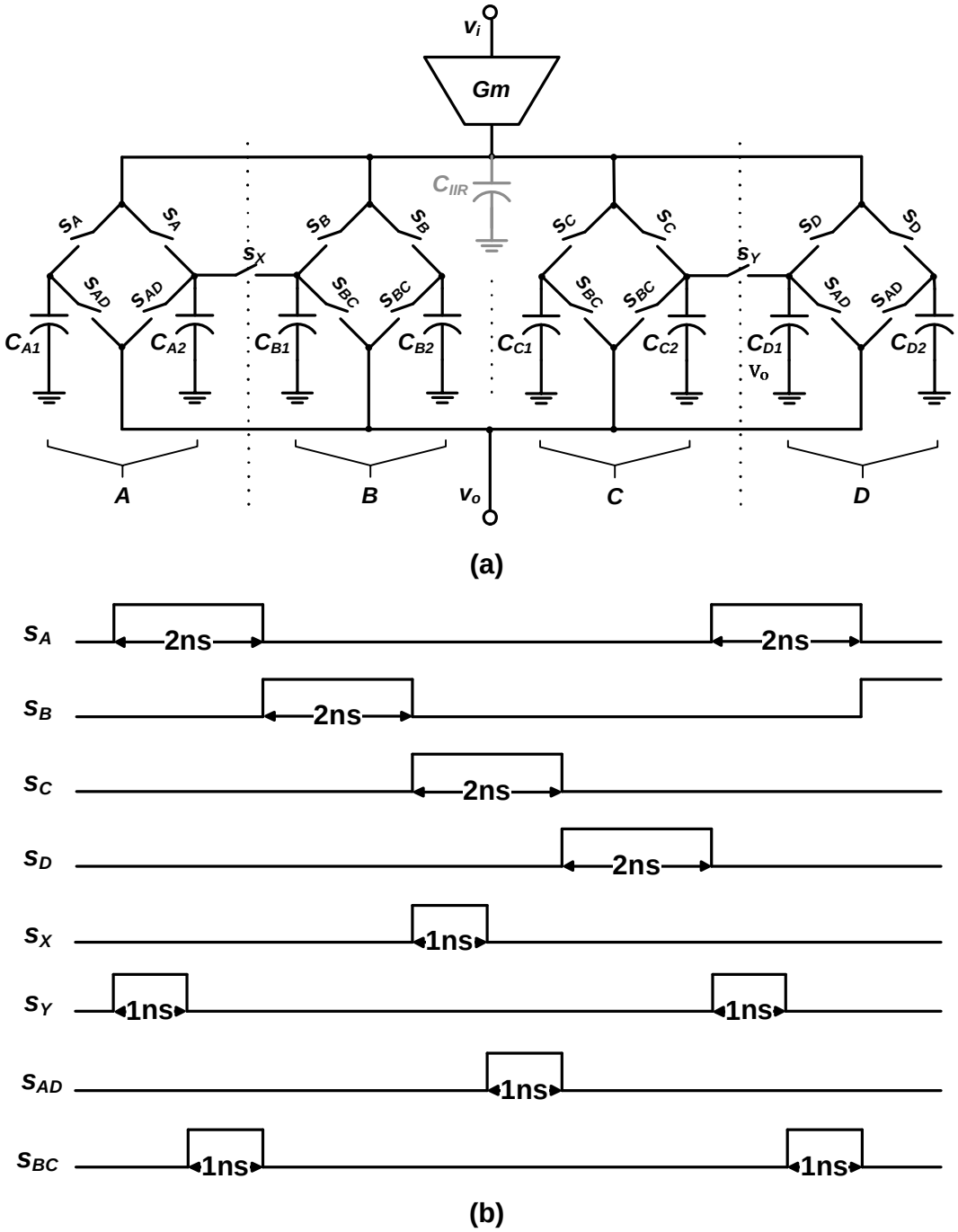


Fig. 5.4. (a) Proposed topology of $sinc^3 \downarrow 2$ filter (b) Clock time diagram.

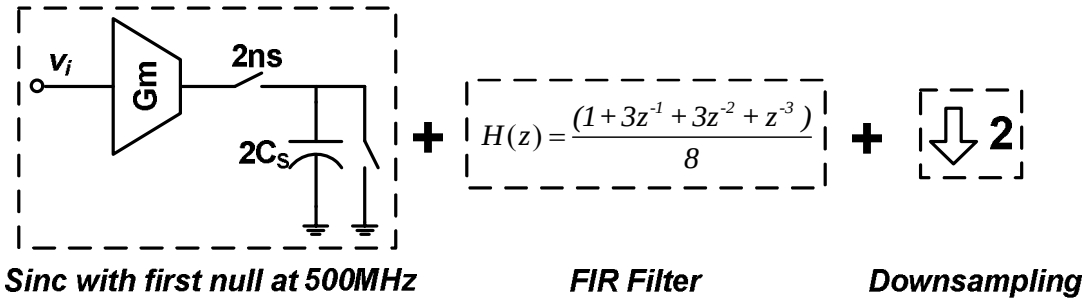


Fig. 5.5. The overall transfer function from input to output of the proposed topology.

From Fig. 5.4, Gain G_{prop} of the proposed topology is given by,

$$G_{prop} = \frac{Gm_{prop}\Delta t}{2Cs_{prop}} \tag{5.10}$$

Equating (5.9) and (5.10),

$$\frac{Gm_{conv}}{Cs_{conv}} = 2\left(\frac{Gm_{prop}}{Cs_{prop}}\right) \tag{5.11}$$

Similarly, the noise of the two topologies can be calculated as follows,

$$\begin{aligned} N_{conv} &= \frac{2KT}{64}\left(\frac{Gm_{conv}\Delta t}{16Cs_{conv}^2} + 9\frac{Gm_{conv}\Delta t}{16Cs_{conv}^2} + 9\frac{Gm_{conv}\Delta t}{16Cs_{conv}^2} + \frac{Gm_{conv}\Delta t}{16Cs_{conv}^2}\right) \\ &= \frac{2KT}{64}\left(20\frac{Gm_{conv}\Delta t}{16Cs_{conv}^2}\right) \end{aligned} \tag{5.12}$$

The factor 1/64 comes in the expression because of charge sharing.

$$N_{prop} = \frac{2KT}{16}\left(\begin{aligned} &\frac{Gm_{prop}\Delta t}{16Cs_{prop}^2} + \\ &\left\{\frac{Gm_{prop}\Delta t}{16Cs_{prop}^2} + \frac{Gm_{prop}\Delta t}{4Cs_{prop}^2} + 2\frac{Gm_{prop}\Delta t}{4\times 2\times Cs_{prop}^2}\right\} + \\ &\left\{\frac{Gm_{prop}\Delta t}{16Cs_{prop}^2} + \frac{Gm_{prop}\Delta t}{4Cs_{prop}^2} + 2\frac{Gm_{prop}\Delta t}{4\times 2\times Cs_{prop}^2}\right\} + \\ &\frac{Gm_{prop}\Delta t}{16Cs_{prop}^2} \end{aligned}\right) \tag{5.13}$$

$$= \frac{2KT}{16}\left(20\frac{Gm_{prop}\Delta t}{16Cs_{prop}^2}\right) \tag{5.14}$$

Equating (5.12) and (5.14),

$$\frac{Gm_{conv}\Delta t}{Cs_{conv}^2} = 4\left(\frac{Gm_{prop}\Delta t}{Cs_{prop}^2}\right) \tag{5.15}$$

From (5.11) and (5.15),

$$Gm_{conv} = Gm_{prop}; Cs_{prop} = 2Cs_{conv} \tag{5.16}$$

In the conventional topology, there are 24 capacitors used which amounts to a total capacitance of $24Cs_{conv}$. For the proposed topology, there are only 8 capacitors used which amounts to a capacitance of $8Cs_{prop}$ *or* $16Cs_{conv}$. This translates to 33% area savings in the proposed topology when compared to the conventional one. The reduced area in the proposed topology is obtained at the expense of small complexity overhead in clock generation.

D. DT-IIR Filtering

A capacitor C_{IIR} at the output of the trans-conductance amplifier creates a discrete time IIR (DT-IIR) filtering with a pole at z_p [5].

$$z_p = \frac{C_{IIR}}{C_{IIR} + 2Cs} \tag{5.17}$$

The capacitor C_{IIR} improves null attenuation apart from preventing large overshoots.

E. Simulation Results

The proposed filter is simulated in 45nm CMOS technology. Fig. 5.6 compares the simulated responses with ideal response The value of sampling capacitor *Cs* is chosen to be 2pF. Non-idealities of the switch, glitches during switching and finite output impedance of the transconductor are the main reason why null attenuation is slightly lesser in circuit level simulations compared to ideal transfer characteristic. It is also observed that the null bandwidth widens as C_{IIR} =5pF is added at the output of the tranconductance amplifier.

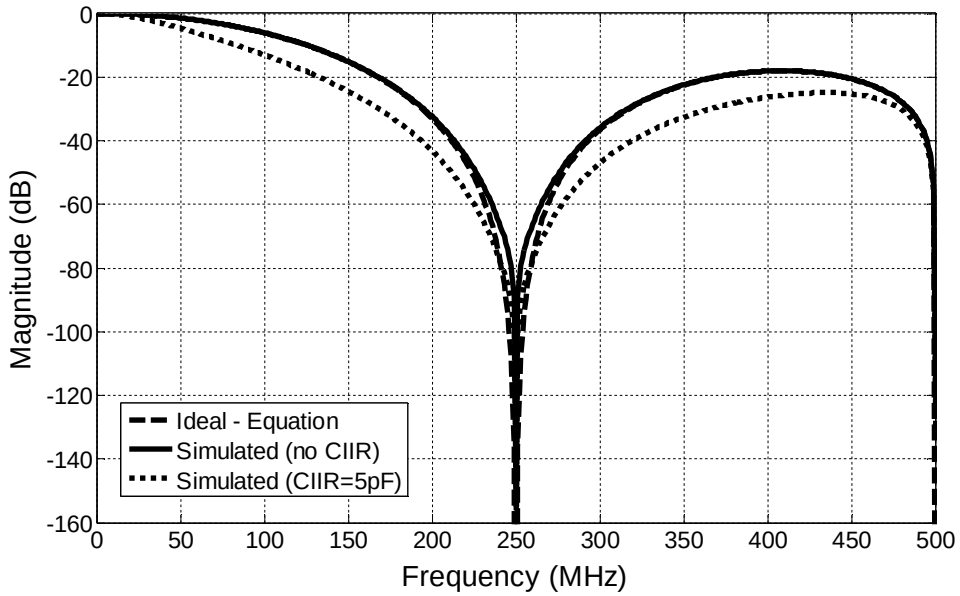


Fig. 5.6. Comparison of Simulated filter response, filter response with CIIR = 5pF and ideal response (Equation).

CHAPTER VI

CONCLUSION

A novel technique to implement a $sinc^2$ ↓2 filter has been proposed. Both the conventional and proposed filters have been simulated in 45nm technology and the results are compared. The results show that the proposed filter gives the same performance as the conventional topology with 25% area savings on sampling capacitors, which dominates the area occupied by the filter. The proposed topology can also be extended to achieve $sinc^2$ function with higher down-sampling factor. The higher the down-sampling factor, the greater is the area savings compared to conventional filter. The proposed filter topology has an additional benefit; it allows charging and reading the sampling capacitor in closed loop with an OTA. In a software defined radio, when linearity and area are of main concern, the usefulness of the proposed filter is evident.

A technique to implement a $sinc^3$ ↓2 filter has also been proposed. Area savings of 33% can be achieved at the cost of small additional complexity in the clock generation. The implementation is simple and it is observed that the simulated transfer characteristic matches well the ideal transfer function.

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APPENDIX A

NOISE ANALYSIS OF CHARGE SAMPLING CIRCUITS

In charge sampling circuits, switches contribute very less to the total output noise. Noise from the transconductor is the dominant factor in deciding the overall noise performance of the circuit. Fig. A.1(a) shows the simplified model for noise analysis, where $\overline{i_n}^2 = 4KT\gamma gm$ is the noise from the transconductor, r_o is the output impedance of the transconductor and C is the sampling capacitance. Fig. A.1(b) shows the equivalent representation with transfer functions.

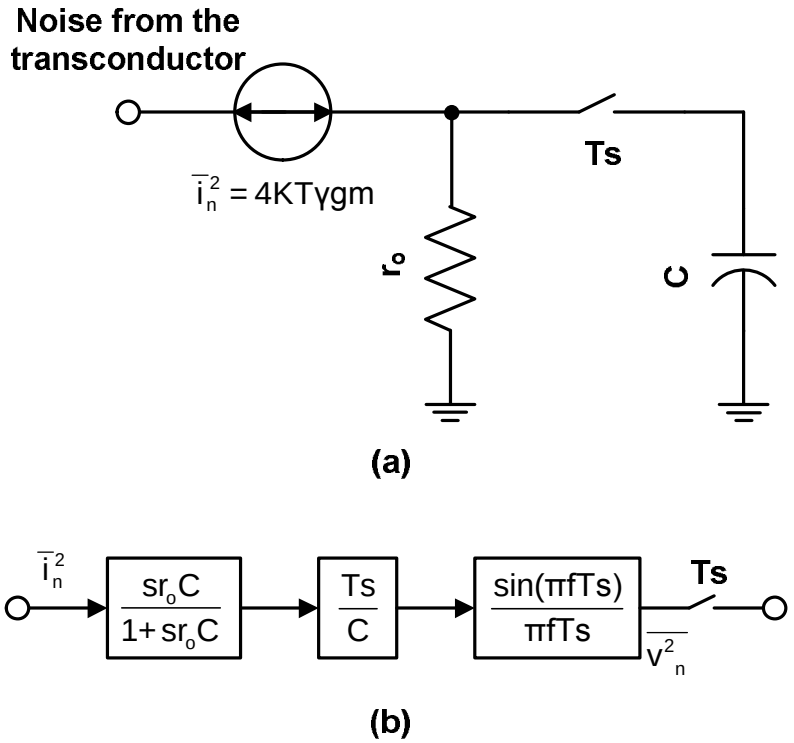

Fig. A.1 (a) Model of charge sampling assumed for noise analysis (b) Equivalent representation with transfer functions.

$$N_{Total} = \int_0^\infty \overline{v_n^2}(f)df = \int_0^\infty \left(\frac{Ts}{C} \frac{\sin(\pi fTs)}{\pi fTs} \frac{2\pi fr_oC}{\sqrt{1+(2\pi fr_oC)^2}} \right)^2 \overline{i_n^2}(f)df$$

$$= \left(\frac{Ts}{C}\right)^2 \left(\frac{1}{\pi Ts}\right)^2 \overline{i_n^2}(f) \int_0^\infty \frac{\sin^2(\pi fTs)}{f^2 + \frac{1}{4\pi^2C^2r_o^2}} df$$

$$= \frac{\overline{i_n^2}(f)}{2C^2\pi^2} \left[\int_0^\infty \frac{1}{f^2 + \frac{1}{4\pi^2C^2r_o^2}} df - \int_0^\infty \frac{\cos(2\pi fTs)}{f^2 + \frac{1}{4\pi^2C^2r_o^2}} df \right]$$

$$= \frac{\overline{i_n^2}(f)}{2C^2\pi^2} \left[\pi^2Cr_o - \pi^2Cr_oe^{-\frac{Ts}{Cr_o}} \right]$$

$$N_{Total} = \frac{\overline{i_n^2}(f)r_o}{2C} \left(1 - e^{-\frac{Ts}{Cr_o}}\right) \tag{A.1}$$

The above expression is obtained without any approximation.

$$\text{If } \frac{Ts}{Cr_o} << 1 \text{ (or) } Ts << Cr_o, \text{ then,}$$

$$N_{Total} = \frac{\overline{i_n^2}(f)r_o}{2C} \left(\frac{Ts}{Cr_o}\right) = \frac{\overline{i_n^2}(f)Ts}{2C^2} \tag{A.2}$$

$$\text{If } i_n^2 = 4KT\gamma gm \text{ (Noise of MOS Transistor)}$$

$$N_{Total} = \frac{2KT(\gamma gm)Ts}{C^2} \tag{A.3}$$

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