# CALIBRATED CONTINUOUS-TIME SIGMA-DELTA MODULATORS

A Dissertation

by

CHO-YING LU

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

May 2010

Major Subject: Electrical Engineering

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Approved by:

| | |
|---|---|
| Chair of Committee, | Jose Silva-Martinez |
| Committee Members, | Aydin Karsilayan |
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**ABSTRACT**

Calibrated Continuous-Time Sigma-Delta Modulators. (May 2010)

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Chair of Advisory Committee: Dr. Jose Silva-Martinez

To provide more information mobility, many wireless communication systems such as WCDMA and EDGE in phone systems, bluetooth and WIMAX in communication networks have been recently developed. Recent efforts have been made to build the all-in-one next generation device which integrates a large number of wireless services into a single receiving path in order to raise the competitiveness of the device. Among all the receiver architectures, the high-IF receiver presents several unique properties for the next generation receiver by digitalizing the signal at the intermediate frequency around a few hundred MHz. In this architecture, the modulation/demodulation schemes, protocols, equalization, etc., are all determined in a software platform that runs in the digital signal processor (DSP) or FPGA. The specifications for most of front-end building blocks are relaxed, except the analog-to-digital converter (ADC). The requirements of large bandwidth, high operational frequency and high resolution make the design of the ADC very challenging.

Solving the bottleneck associated with the high-IF receiver architecture is a major focus of many ongoing research efforts. In this work, a $6^{th}$-order bandpass continuous-

time sigma-delta ADC with measured 68.4dB SNDR at 10MHz bandwidth to accommodate video applications is proposed. Tuned at 200 MHz, the fs/4 architecture employs an 800 MHz clock frequency. By making use of a unique software-based calibration scheme together with the tuning properties of the bandpass filters developed under the umbrella of this project, the ADC performance is optimized automatically to fulfill all requirements for the high-IF architecture.

In a separate project, other critical design issues for continuous-time sigma-delta ADCs are addressed, especially the issues related to unit current source mismatches in multi-level DACs as well as excess loop delays that may cause loop instability. The reported solutions are revisited to find more efficient architectures. The aforementioned techniques are used for the design of a 25MHz bandwidth lowpass continuous-time sigma-delta modulator with time-domain two-step 3-bit quantizer and DAC for WiMAX applications. The prototype is designed by employing a level-to-pulse-width modulation (PWM) converter followed by a single-level DAC in the feedback path to translate the typical digital codes into PWM signals with the proposed pulse arrangement. Therefore, the non-linearity issue from current source mismatch in multi-level DACs is prevented. The jitter behavior and timing mismatch issue of the proposed time-based methods are fully analyzed. The measurement results of a chip prototype achieving 67.7dB peak SNDR and 78dB SFDR in 25MHz bandwidth properly demonstrate the design concepts and effectiveness of time-based quantization and feedback.

Both continuous-time sigma-delta ADCs were fabricated in mainstream CMOS 0.18um technologies, which are the most popular in today's consumer electronics industry.

# DEDICATION

To my parents

To my dearest wife, Jihying Chang, and daughter, Ariel Lu

# ACKNOWLEDGEMENTS

In coming to the final stage of my graduate studies, all my successful work reflects the relationships with many inspiring and gracious people I met during these years. I would like to contribute my thanks to all your priceless support.

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I want to thank Dr. Aydin Karsilayan, Dr. Kai Chang, and Dr. Alexander Parlos for serving as my committee members and for their invaluable comments and suggestions to my research and my dissertation. The guidance and encouragement from Dr. Kai Chang assisted me a lot in planning my future career.

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**CHAPTER I**

**INTRODUCTION**

1.1 Motivation

With the recent developments on wireless communications, different wireless services are proposed year by year. With different definitions of signal power, signal bandwidth, signal frequency and coding methods in the standards, the required performance of the hardware for each one of these services is unique. For example, the receiver in GSM system has to have fast settling time due to the adoption of frequency hopped time-division multiple-access (TDMA) system. Nevertheless, by employing code-division multiple-access (CDMA) system, the timing requirement in WCDMA receiver is irrelevant. The noise and linearity performance in WCDMA is more important because of the higher required bit error rate (BER.) As a result, the conventional scheme building a multi-standard wireless device is to design different receiver modules for different wireless services. The solution is simple but the efficiency on power and area is low. Integrating as many wireless services as possible into a single chip-set is recently a trend for the semiconductor sector in order to cut down the cost of the products and raise the device competitiveness [1].

The software-defined radio receiver architecture (High-IF architecture) is a potential candidate to realize the multi-standard receiver [2]. With no DC offset and the relaxed image problem, this architecture eases the front-end circuit specifications. However, the requirements of large bandwidth ($\geq$ 10MHz for video communication), high operational

_____
This dissertation follows the style and format of *IEEE Journal of Solid-State Circuits*.

frequency (> 100MHz for high-IF receiver) and high resolution (≥ 11bits for video communication) make the design of the ADC very challenging. None of the reported ADCs can match these three specifications perfectly in the architecture at this moment. In this research, therefore, the design of a continuous-time sigma-delta (ΣΔ) ADC to overcome the bottleneck of the software-defined radio receiver is addressed.

Unlike a discrete-time ΣΔ ADC with immunity to the process, voltage, temperature (PVT) variations by using capacitor ratios to determine the system coefficients, one of the critical issues of a continuous-time ΣΔ ADC is its high sensitivity to the variations due to the demands on RC time constants. These variations drastically degrade the performance of the ADCs or even break the stability conditions. Therefore, either manual or automatic calibration is definitely needed after fabrication. In this dissertation, an efficient software-based automatic calibration technique is proposed to recover the system performances from the PVT variations.

In order to maintain the resolution of continuous-time ΣΔ ADCs, increasing sampling frequency and employing multi-bit quantizer and DACs are now essential due to the growth of the signal bandwidth in wireless services. The device mismatch issue in multi-level DACs threatens the system's linearity and degrades the ADC's resolution. Although there are different reported solutions to either pseudo-randomize or shape the mismatch, the reduced delay margin in the digital feedback path due to the increase of sampling frequency makes the solutions inadequate to improve the linearity of broadband ADCs. Hence, to implement continuous-time ΣΔ ADCs with wide bandwidth and high resolution, a new technique to alleviate the non-linearity issue with minimal delay requirements and power consumption has to be proposed.

1.2 Research Contribution

To overcome the limitations on current software-radio defined receiver architectures by employing a wide-band, high-speed, high-resolution continuous-time $\Sigma\Delta$ ADC are some of the objectives in this research. A 6th-order bandpass continuous-time $\Sigma\Delta$ ADC is implemented in TSMC 0.18um CMOS technology to acquire 10MHz bandwidth for video applications. The distortion issues due to the input stage filter are cautiously analyzed and a two-integrator type active-RC filter is designed with remarkable linearity performance. Since the sensitivity of continuous-time $\Sigma\Delta$ ADCs to PVT variations is a critical issue, a robust unique software-based calibration technique is proposed to efficiently calibrate the system. By injecting two test tones at the input of the quantizer to measure the noise transfer function, the output noise level of the ADC is detected by software and minimized by tuning the system coefficients. The measured bandpass continuous-time $\Sigma\Delta$ ADC achieves 68.4dB SNDR at 10MHz bandwidth with 160mW power consumption. The resulted figure-of-merit (FoM) of 3.72pJ/bit out perform all the currently reported bandpass continuous-time $\Sigma\Delta$ ADCs.

To alleviate the non-linearity issues from device mismatches of the conventional multi-level DACs is also one of the core objectives of this research. The techniques are employed for the design of a 25MHz bandwidth 5th-order lowpass continuous-time $\Sigma\Delta$ ADC. With oversampling ratio equal to eight, instead of using a 3-bit conventional quantizer and DAC, the 3-bit time-domain quantizer and DAC are proposed to achieve the required resolution at a 25MHz bandwidth.

By using a pulse-width modulation (PWM) scheme with appropriate pulse shape arrangement in digital feedback path, an inherently linear single-level DAC is employed and hence the current source mismatch problem is relaxed. Although the use of pulse-width modulation in continuous-time $\Sigma\Delta$ ADCs is not a novel concept introduced in this dissertation, the detail analysis on jitter behavior of the time-domain DAC and non-linearity issue because of timing mismatch are for the first time addressed. The jitter noise sensitivity of the ADC is eased with the implementation of complementary injection-locked frequency divider, which can achieve the required reference clocks with improved jitter noise performance. Fabricated in Jazz 0.18um CMOS technology, the measurement of the proposed lowpass continuous-time $\Sigma\Delta$ ADC results in 67.7dB peak SNDR and 78dB SFDR at the ADC output. By using only the cheapest technology, the 444fJ/bit FoM is comparable to the state-of-arts, which are implemented in more advanced technologies.

1.3 Dissertation Organization

In order to fully understand the design issues of a continuous-time $\Sigma\Delta$ ADC for wireless communication applications, the advantages and limitations of different receiver architectures are analyzed and compared in Chapter II. In addition, the comparison between Nyquist ADCs and oversampling ADCs are addressed in Chapter II. An overview of the continuous-time $\Sigma\Delta$ ADCs is given in Chapter III, where the design issues and design strategies are explained. The survey of currently reported works identifies the implementation trends of $\Sigma\Delta$ ADCs.

Chapter IV presents a 10MHz bandwidth $6^{th}$-order bandpass continuous-time $\Sigma\Delta$ ADC with 200MHz operational frequency and 800MHz sampling frequency for software-defined radio receiver architectures. A proposed unique calibration scheme to overcome the lack of accuracy of continuous-time $\Sigma\Delta$ ADCs is well explained in this chapter. The design of a 25MHz bandwidth $5^{th}$-order lowpass continuous-time $\Sigma\Delta$ ADC with a time-domain two-step 3-bit quantizer and feedback DAC for zero-IF architecture is described in Chapter V. The advantages of the pulse-width modulation are specified and the limitations of the scheme are fully discussed. The design flow, circuit implementation, and measurement results of both aforementioned continuous-time $\Sigma\Delta$ ADCs are presented in their own chapters. Finally, Chapter VI depicts the conclusions of this dissertation.

**CHAPTER II**

**THE BOTTLENECK OF THE NEXT GENERATION RECEIVERS: ANALOG-**

**TO-DIGITAL CONVERTER**

2.1 Next Generation Receivers

Due to the demand for high-performance radio frequency (RF) integrated circuit design in the past decades, a system-on-chip that enables integration of analog and digital parts on the same die has becoming the trend of the microelectronics industry. Also, many different standards have been developed for different wireless applications. The cell phones segment includes standards like GSM, CDMA, UMTS, GPRS, TDMA, DECT, EDGE, IS-95 etc. The wireless local area network for laptops, desktops and PDA's include standards like Bluetooth, for the Personal Area Network (PAN); WiFi for the Local Area Network (LAN); 802.16 for the Metropolitan Area Network (MAN) and IEEE 802.20 for the Wide Area Network (WAN). As a result, a major requirement of the next generation wireless devices is to support multiple standards in the same chip-set, as shown in Fig. 2.1. This would enable a single device to support multiple applications and services and also improve the total power consumption, form factor and device competitiveness.
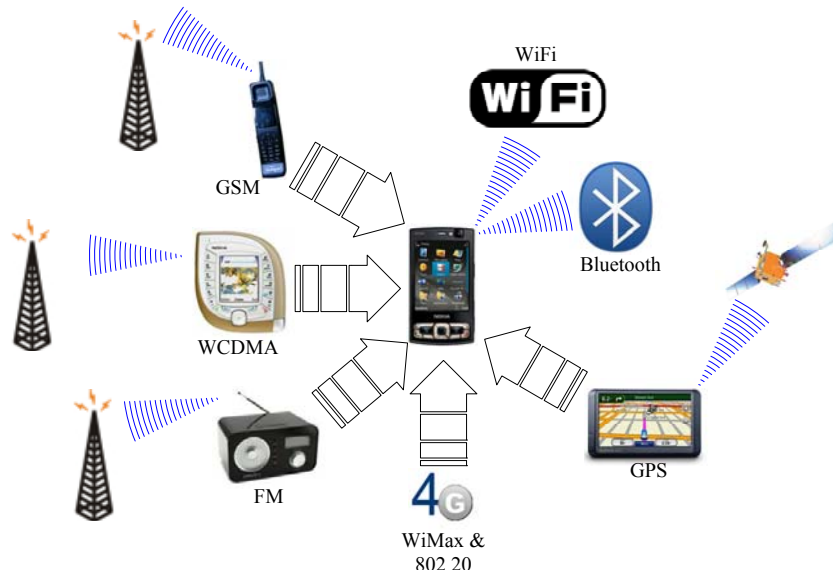
Fig. 2.1. A next generation wireless device supporting multiple services.

As the frequency spectrum in Fig. 2.2 shows, different services employ different radio frequency bands to build the communication between stations and mobile devices. In order to support multiple standards, the receiver within the next generation wireless device has to be able to select the preferred channel and process them accurately.
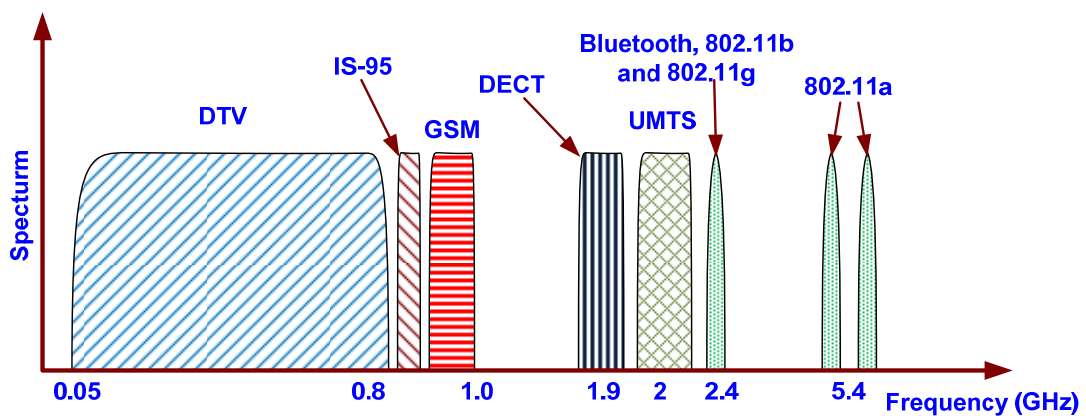


Fig. 2.2. The band distribution of different services.

The first design step is to determine the receiver architecture. Since there are several receiver architectures available, the detailed and thorough research on these architecture solutions, including all the advantages and drawbacks, is necessary to find the most potential candidate for the realization of next generation receivers. Section 2.2 discuss the operational concepts and the characteristics of each one of different receiver architectures and identify the best choice for the next generation receiver.

The Analog-to-Digital Converter (ADC) is the last block in the front-end of the wireless architectures. The main function of ADCs is to digitalize analog signals such that the following digital-signal-processing (DSP) circuits can process the signal and demodulate the wanted information through robust, flexible, and reliable software. In section 2.3, we will compare the different ADC architectures and point out the performance limitations. In section 2.4 we will make a conclusion on the observations on the receiver architectures and ADCs and determine the best choices for the realization of wideband receivers.

2.2 Common Receiver Architectures for Wireless Communication

2.2.1    Superheterodyne architecture

This is the most traditional system architecture of a receiver in wireless communication. The main concept was introduced by Edwin Armstrong in 1918. As depicted in Fig. 2.3, when antenna captures the signal, the unwanted blockers and interferences are filtered out by the band selection filter and the signal is amplified by a low-noise amplifier (LNA.) This band selection filter is an external component with a very high Q.   In order to reduce the difficulty in processsing the signal, the desired channels are down-converted to the intermediate frequency (IF) from the original radio frequency (RF) usually in a range of 800MHz to 8GHz depending on the services. The channel select filter will select the required channel of the system and reject the adjacent channels and the un-desired high frequency spectral components produced by the mixer. The second mixer down-converts the cleaned signal to the baseband with I-Q paths, which have 90 degree phase difference between each other. The variable-gain amplifier (VGA) reduces the signal power range based on its flexible gain. At the last, the ADC converts the analog signal to the digital domain such that the digital signal processor (DSP) circuits can operate the signal and demodulate the information.

In this architecture, because there are many blocks needed to process the signal into the acceptable signal power level and frequency, the total power consumption is much higher than other solutions. Besides, when wanting to integrate multiple standards into single device, the only solution of this architecture is to duplicate the whole receiving path.   Therefore,  the  power  dissipation  increases  drastically.  Nevertheless,  this

architecture has been popular for many years since this is the easiest solution comparing with other architectures.
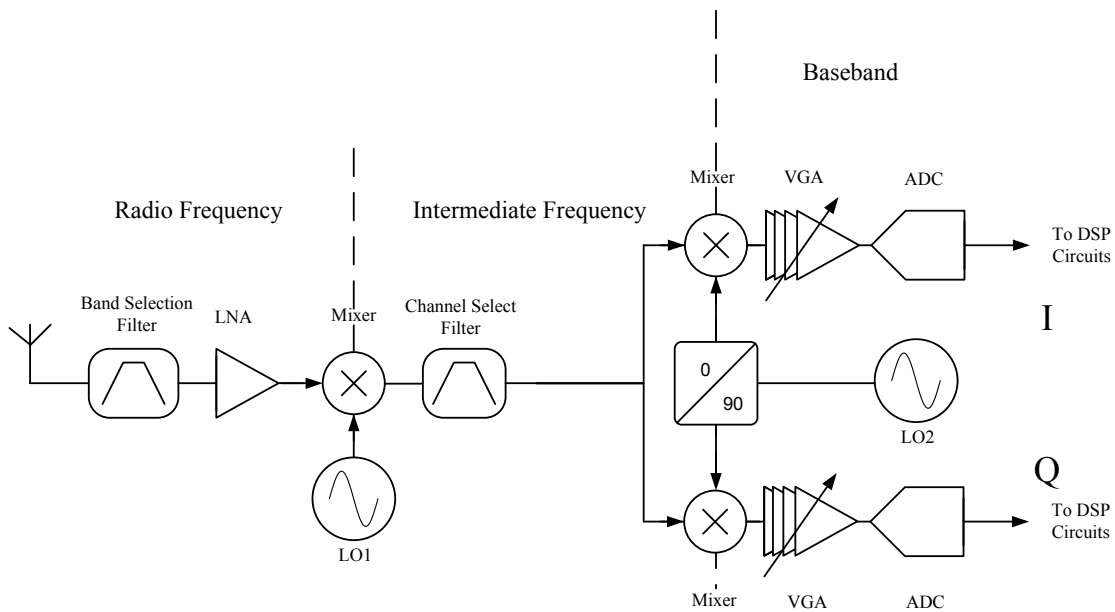


Fig. 2.3. The superheterodyne architecture of a receiver.

### 2.2.2 Low-IF architecture

Instead of employing two down-conversions, the low-IF architecture down-converts the signal only once to decrease the number of blocks and thus reduce the overall power dissipation of the receiver as depicted in Fig. 2.4. In addition, by lowering the IF frequency, the power consumption of each IF block can be reduced.

The image effect in this architecture is a critical issue since the IF is lowered. Based on the concept of mixing, when there are a signal at frequency of $f_{sig}$ and a reference clock at frequency $f_{LO}$ from LO, the output of mixer will generate a tone at $f_{IF}=f_{sig}-f_{LO}$ and hence complete the down-conversion of the signal. However, if there is an interference locating at $2f_{LO}-f_{sig}$, (= $f_{sig}-2f_{IF}$) it can be demonstrated that this interference will also fall into the frequency of $f_{sig}-f_{LO}$ after mixing. The interference overlapping

with signals is very difficult to be rejected. The best way to prevent this effect is to attenuate the interference at $f_{sig}$-2$f_{IF}$ before mixer. However, since the IF frequency is only few MHz in low-IF architecture, this image interference may be the adjacent channel signal of the wireless system, which might has higher power than the desired channel. The purpose to eliminate this strong image interference results in a very power-hungry external bandpass RF filter. This is not a wanted solution in system-on-chip (SoC) applications. Other solutions, such as Hartley architecture [3] and Weaver architecture [4], were proposed in order to eliminate the image problem after mixer by taking the advantage of phase difference between IQ signals. However, the solutions are more expensive and the gain and phase mismatch limit the rejection of the image.
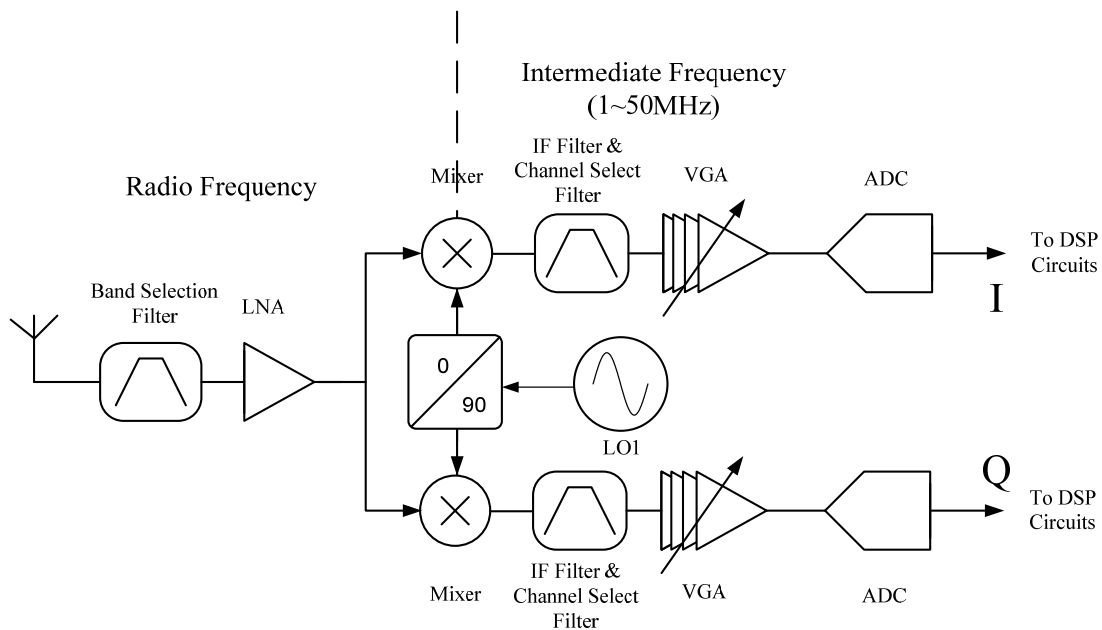


Fig. 2.4. The low-IF architecture of a receiver.

2.2.3    Direct conversion architecture

The direct conversion or zero-IF architecture, plotted in Fig. 2.5, down-converts the RF signal to baseband directly. By choosing the LO frequency equal to the desired signal frequency, there is no image issues in this architecture. The power of the receiver is now further reduced since the desired channel is centered at DC after mixer.

Although the image problem is thoroughly solved, the extra issues from flicker noise, DC offset and IIP2 constraint the performance of the architecture. Since the circuits after mixer work at baseband, the flicker noise dominates the noise performance and threatens the system. An additional emphasis on this flicker noise has to be done when designing baseband circuits. DC offset issues are the results of the self-mixing where the reference signal from LO leaks to antenna and is received with signals. Since the frequency of reference signal and the desired signal are the same, it is impossible to distinguish them. To enhance the isolation of the mixer from LO port to RF port is normally the solution to alleviate the problem. In addition, if there are two blockers close to each other in frequency, the second-order intermodulation of Mixer and LNA will produce an undesired tone at baseband and affect the quality of the baseband signal. As a consequence, the even-order intermodulation performance of the LNA and Mixer are critical parameters in direct conversion architectures. The Mixer's isolation between RF and output ports is critical as well.
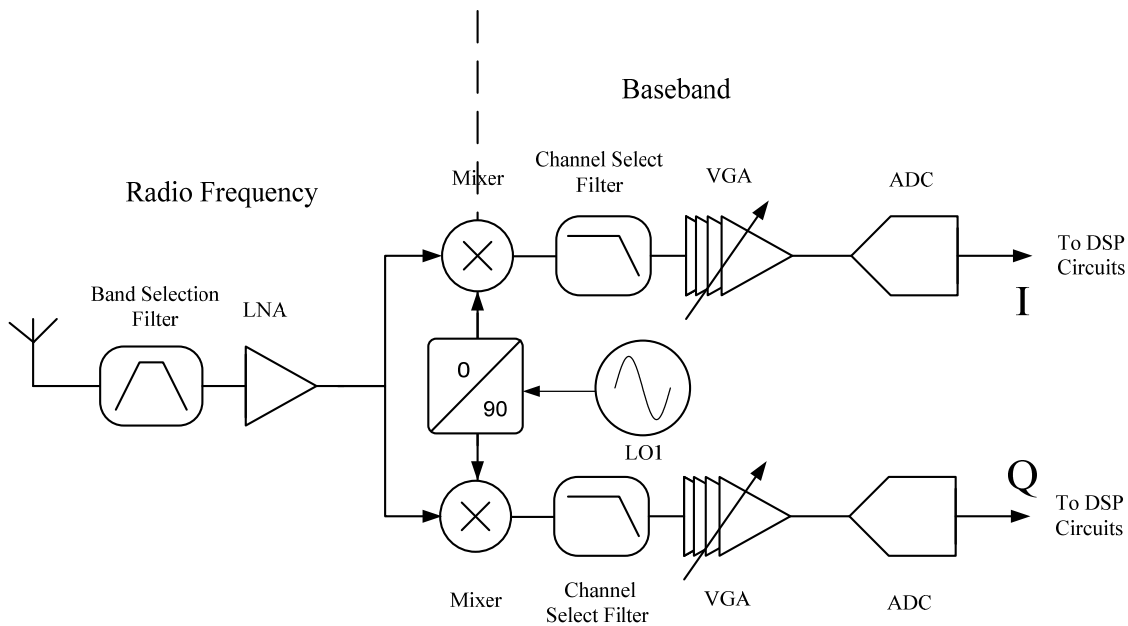
Fig. 2.5. The direct conversion of a receiver.

## 2.2.4 High-IF architecture (software-defined radio architecture)

Fig. 2.6 shows the architecture of a High-IF receiver. Similar to the low-IF architecture, the high-IF architecture down-converts the signal to the intermediate frequency and then digitalizes it. The high-IF radio presents several unique properties by digitalizing the signal at few hundred MHz. The baseband operations, such as baseband conversion and channel filtering, are more robust and power efficient in digital domain and fewer analog blocks would require to be replicated for each standard. Neither the image effect presenting in Low-IF architecture nor the DC offset issues in direct conversion will degrade the performance of the system. This architecture relaxes the specifications for most of the front-end building blocks but not for the ADC. The demands of wide bandwidth, high signal frequency and high resolution make this ADC a bottleneck when developing this architecture. Although there have been many reported papers for these specifications, none of them can fulfill the requirements perfectly.

Intermediate Frequency
(>100MHz)

IF Filter &
Channel Select
Filter

Radio Frequency

Mixer

VGA

ADC

To DSP
Circuits

I

Band Selection
Filter

LNA

0

90

LO1

Q

To DSP
Circuits

Mixer

IF Filter &
Channel Select
Filter

VGA

ADC
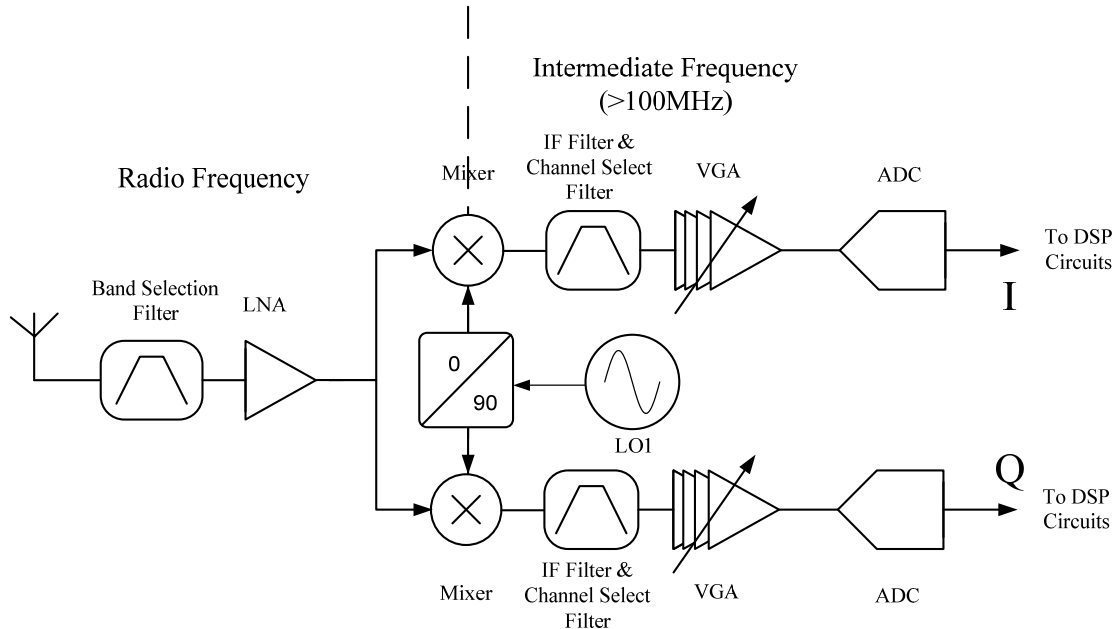
Fig. 2.6. The high-IF architecture of a receiver.

## 2.2.5 Software radio architecture

Regarding the software radio, it is a concept proposed in 1991 to minimize the use of analog blocks due to the uncertainty of the analog circuits by digitalizing the signal at RF. As illustrated in Fig. 2.7, the signal is digitalized directly after a programmable LNA. This architecture is not only robust due to the entire signal processing in the digital domain but also suitable for multiple standard applications since all the signals from different standards can be processed by the same receiving path by running different software. In order to cover all the signal power ranges from sensitivity to maximum possible power in different applications, the LNA has to be programmable and the ADC has to achieve enough dynamic range at GHz range of signal frequency. Due to the huge barrier on the LNA and ADC requirements it is not economical to implement it. The

power consumption of the solution may be huge even with the most advanced
technologies.

Radio Frequency
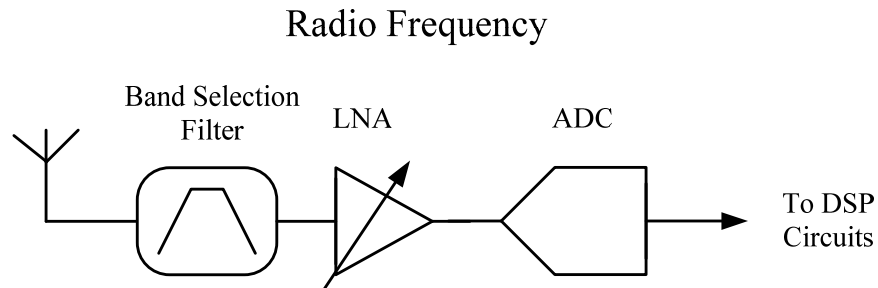
Fig. 2.7. The software radio architecture of a receiver.

2.2.6   The comparison of the architectures

Table 2.1 compares the characteristics of all the receiver architectures. Based on the
considerations on design issues, multi-standard compatibility and design difficulty, it is
obvious that direct conversion and high-IF architectures are the most appropriate
candidates to be employed in the next generation receiver. Indeed, the direction
conversion architecture is the most popular architecture in many different applications
nowadays. Many solutions are proposed to solve the issues from DC offset and flicker
noise. The IIP2 of LNAs and Mixers in the architecture also keep being improved with
the advances of circuit design techniques. Regarding the high-IF architecture, the
development is constrained solely by the ADC where the operational speed of the circuit
is a bottleneck. Fortunately, with the evolvement of the CMOS technologies, the $f_T$
frequency of the devices achieves about 200GHz; this will definitely assist overcoming

the bottleneck of ADCs and thus relax the limitation of the High-IF architecture development.

Table 2.1 The comparison of the receiver architectures

| | Multiple standard compatibility | Power Consumption | DC-offset | Image effect | IQ mismatch | Complexity |
|---|---|---|---|---|---|---|
| Superhete-rodyne | - | ++ | - | + | + | - |
| Low-IF | + | + | - | ++ | + | + |
| Direct Conversion | ++ | - | ++ | - | + | + |
| High-IF | ++ | + | - | + | - | ++ |
| Software Radio | ++ | ++ | - | - | - | +++ |

2.3 Analog-to-Digital Converter (ADC)

2.3.1   The basic concept of an ADC

The natural signal is analog but the digital signal is robust and efficient. When the analog signal travels through the air and is detected by a receiver, ADCs are required in order to digitalize the analog signal and take the advantages of the digital processing. The basic concept of an ADC, shown in Fig. 2.8, is to sample the analog signal with sampling frequency $F_s$ and then quantize this sampled discrete-time signal into digital bits. Since there are always errors between the original signal and the quantized signal due to the limited number of bits in the quantizer, the average of the error is named quantization noise. A general signal-to-quantization noise (SQNR) equation in (2.1) can predict the resolution performance of an ADC [5].

$$SQNR = 6.02n + 1.76 \tag{2.1}$$

where n means the number of bits of a quantizer.
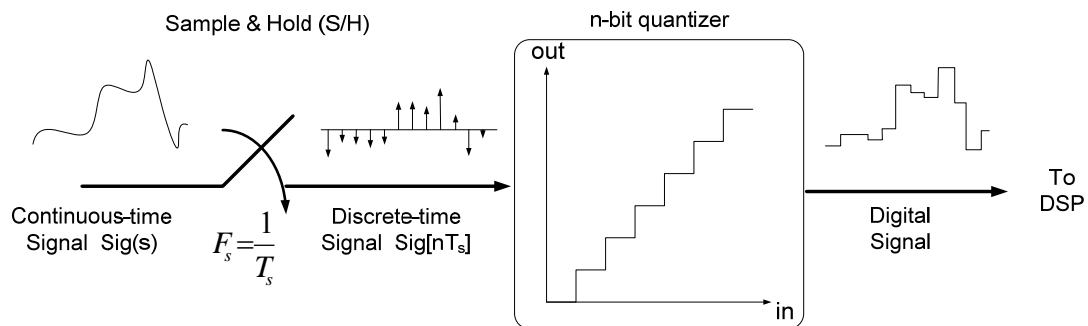


Fig. 2.8. The basic concept of an ADC.

2.3.2   Nyquist ADC and oversampling ADC

There are several ADC architectures that could be used for broadband communications. Overall, there are two main categories to classify these ADCs according to the ratio between the sampling frequency and signal bandwidth: Nyquist ADCs and Oversampling ADCs.

As described by equation (2.2) and (2.3), in Nyquist ADCs the sampling frequency [6] can be as low as twice the signal bandwidth to avoid series aliasing effect. Oversampling ADCs employ a sampling frequency larger than twice of signal bandwidth.

$$\frac{f_{sNyquist}}{f_{BW}} = 2 \qquad\qquad (2.2)$$

$$\frac{f_{soversampling}}{f_{BW}} > 2 \qquad\qquad (2.3)$$

There are many different types of Nyquist ADCs. Fig. 2.9 illustrates the performance distribution on the resolution and sampling frequency of currently relevant Nyquist ADCs. The pipeline ADCs have the highest resolution but the slowest operational speed because of the employment of the cascaded quantizer stages. The flash ADCs have the fastest operational speed since the architectures are composed by a single quantizer stage. However, the resolutions of the flash ADCs are limited because the circuit complexities are proportional to $2^{bit}$. The requirements of the ADC in a high-IF receiver architecture demand on both high resolution (> 12bits) and high operational speed ($\geq$ 800MHz sampling frequency). Therefore, there is no potential candidate of Nyquist ADCs that can fulfill the requirements of the ADC in high-IF architecture. In addition, since all the Nyquist ADCs are lowpass ADCs, the bandwidth of the ADC has to cover the bandwidth from DC to the desired high-IF frequency. However, the desired signal

bandwidth is usually in the range of 1MHz to 25MHz depending on the standard used. This will waste all other bandwidth as well as the power of the ADCs.
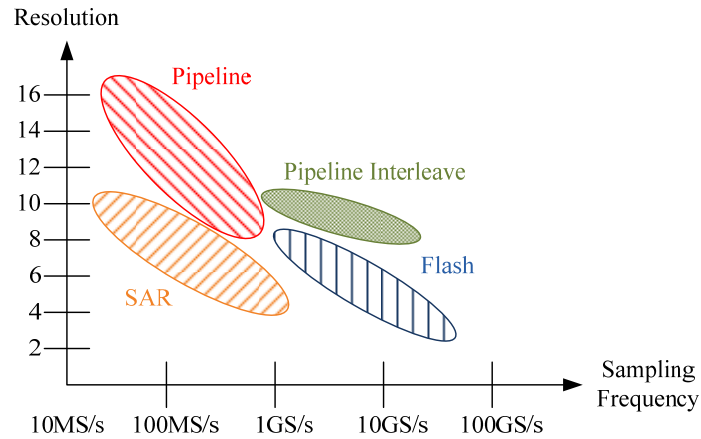


Fig. 2.9. The performance distribution of the Nyquist ADCs.

Unlike Nyquist ADCs, oversampling ADC has many inherent advantages especially for the high-IF application. As shown in Fig. 2.10 (a), when using a quantizer with sampling frequency equal to twice of the signal bandwidth BW, the rms quantization noise is $\frac{1}{12}LSB^2$ where LSB is least significant bit of the quantizer. In oversampling ADCs with the same quantizer, by doubling the sampling frequency from $F_s$ to $F_{s2}$ ($F_{s2}=2F_s$), the rms quantization noise is the same but is spread into more frequency range. If the quantization noise is considered as the only noise source to the ADC, the integrated in-band noise power becomes $v_n(rms) = \sqrt{e^2 \cdot BW}$ . A 3dB resolution is improved when doubling the sampling frequency [7]. Therefore, in general, oversampling ADCs perform better resolution due to this characteristic. However, due to the employment of close loop system, the operational speed of an oversampling ADC is not as fast as that of a flash ADC. Fortunately, the speed of ΣΔ ADCs nowadays keeps

increasing thanks to the higher frequencies achievable with advanced technologies. Despite the resolution performance, [8] has already achieved 1GHz bandwidth and 40GHz sampling frequency by using SiGe BiCMOS technology. As a result, the ΣΔ ADC is the best candidate in the application with high-IF receiver architecture. The design strategies of the high-IF ΣΔ ADC will be depicted in Chapter III.
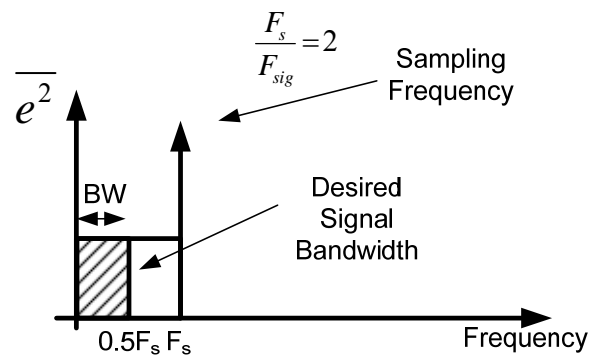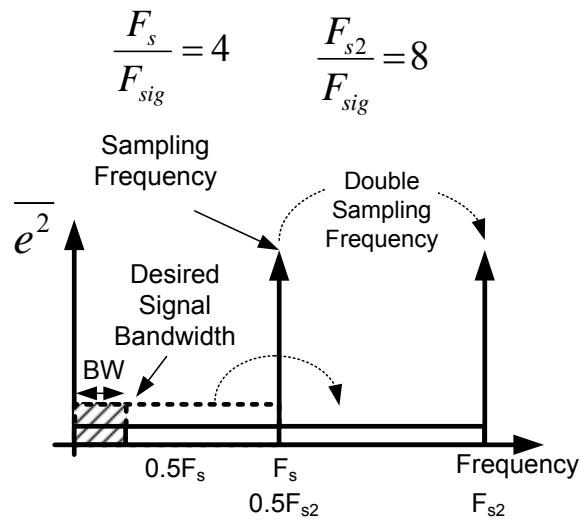


Fig. 2.10. The quantization error distribution in frequency spectra
(a)Nyquist ADC (b) Oversamping ADC.

2.3.3   ADC performance

To judge the performance of an ADC, SQNR, SNR, IM3, peak SNDR, SFDR and DR are the most critical indicators. Fig. 2.11 (a) illustrates the general output power spectrum of an ADC. By injecting an input signal, the output of the ADC is composed by the signal, noise, and harmonic distortions. Thermal noise from transistors or resistors, quantization noise from a quantizer and jitter noise from the sampling clock all contribute to the overall noise performance. The harmonic distortions are generated due to the non-linear behavior of the circuits. The relation between power of those components and input signal power is depicted in Fig. 2.11 (b). Basically, the integrated in-band noise power is fixed and the total in-band harmonic distortion (THD$_{in\text{-}band}$) increases when input signal power grows. Signal-to-noise ratio (SNR) is defined as the ratio between signal power and integrated in-band noise power. The harmonic tones should be excluded when computing SNR. The SNDR (signal-to-noise-and-distortion ratio) is defined as the power difference between the signal power and integrated in-band noise power plus THD$_{in\text{-}band}$ in most of ADCs. SFDR is spurious-free dynamic range which is the power difference between signal and the largest harmonic tone or intermodulation tone as shown in Fig. 2.11(a); dynamic range (DR) means the power range of the input signal where the upper limit and lower limit are the largest allowable power that would not saturate the system and the power level equal to the integrated in-band noise power, respectively, as shown in Fig. 2.11 (b). IM3 is the power difference between signal and third intermodulation tones when employing two-tone test. Overall, SNDR and DR are the most critical indicators showing all the performance related to non-idealties of an ADC and the working range of the signal power.
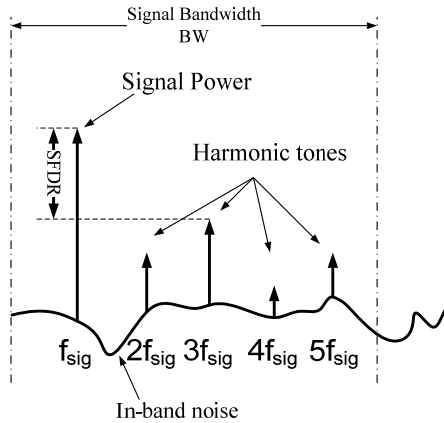
(a)
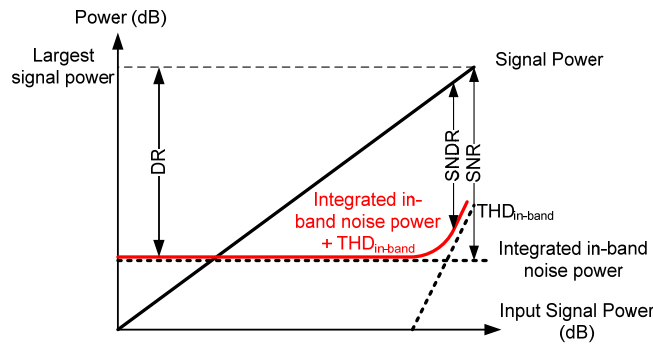


(b)

Fig. 2.11. Critical performance of an ADC
(a) output frequency spectrum (b) output power component v.s. input signal power.

However, as depicted in Fig. 2.12, because the signal frequency is much higher than signal bandwidth ($f_{sig}$ > BW) in the case of bandpass $\Sigma\Delta$ ADCs, harmonic tones ($2f_{sig}$, $3f_{sig...}$) will not fall into the desired bandwidth. The definition of the typical SNDR is invalid in this case since there is no in-band harmonic distortion. A new definition of SNDR for bandpass $\Sigma\Delta$ ADCs is considered as equation (2.4) in order to maintain its indication on performance related to both in-band noise and non-linearities.

$$SNDR_{\text{bandpass } \Sigma\Delta \text{ ADCs}} = \frac{Power_{signal}}{Power_{niose} + Power_{third\ intermodulation\ tones\ @\ two-tone\ test}}$$ (2.4)

where the power of third intermodulation tones should be measured under the condition that total power of two input signals in two-tone test is equal to the largest allowable signal level.
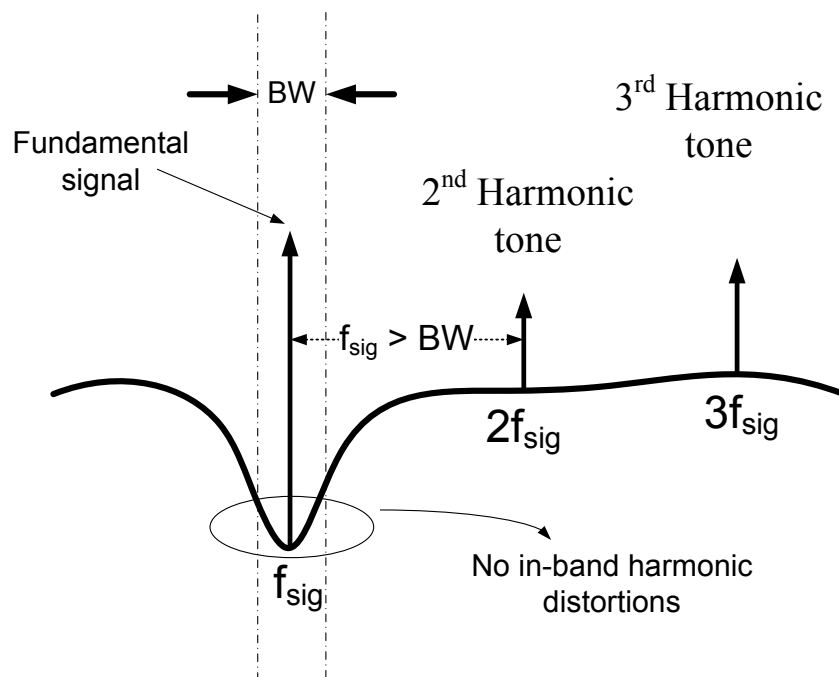


Fig. 2.12. The power spectrum of a bandpass $\Sigma\Delta$ ADC.

2.4 Conclusion

Due to its inherent characteristics, the high-IF architecture is one of the candidates with potential to realize the next generation receiver, which has to be able to support multiple services into a single chip. An architecture called multi-input, multi-output antenna (MIMO) high-IF architecture shown in Fig. 2.13 has been proposed to further relax the requirements of front-end RF circuits and simultaneously enhance the compatibility of this architecture to multiple standards.

However, the high-IF architecture bottleneck is the high requirements of the ADC. A bandwidth to accommodate the widest signal bandwidth in the different services, a signal frequency operating at IF frequency (> 100MHz), and a demanding resolution (> 11bit) of the ADC make the ADC design very challenging. The oversampling ADC, or called $\Sigma\Delta$ ADC, seems to have the potential to fulfill these requirements efficiently over other ADC architectures.

Therefore, in order to design a $\Sigma\Delta$ ADC to accommodate the requirements in the high-IF receiver architecture, Chapter III will go through the basic concepts and design issues to be considered.
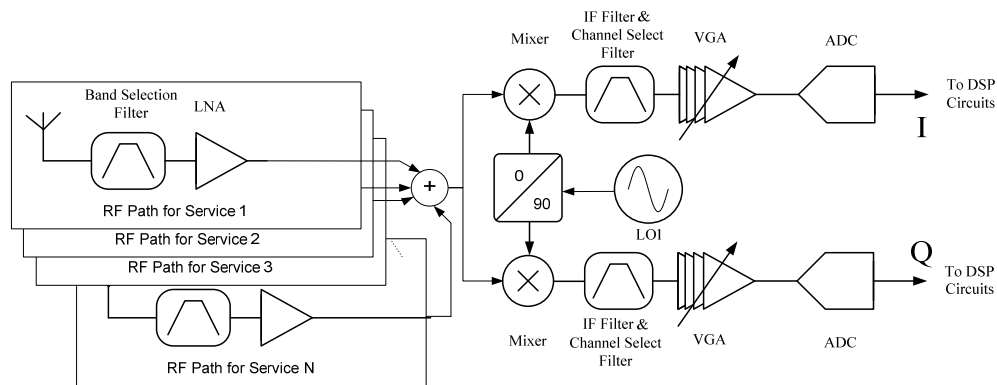


Fig. 2.13. The MIMO high-IF receiver architecture.

**CHAPTER III**

**OVERSAMPLING ΣΔ ADC**

3.1 Overview of ΣΔ ADC

3.1.1   Fundamentals on ΣΔ ADC

Sigma-delta ADCs can perform high resolution without the need of high-bit quantizer by forming a close-loop system with an embedded loop filter. Suppose there is the traditional flash n-bit ADC shown in Fig. 3.1. When the digitization is performed by the ADC, there are errors when comparing the original continuous-time input and the quantized output. The quantization noise appears at the ADC output and limits the signal-to-noise ratio performance (suppose there is no other noise source than quantization noise) as follows [7]:

$$SNR_{qutization} = 6.02 * n + 1.76 \tag{3.1}$$
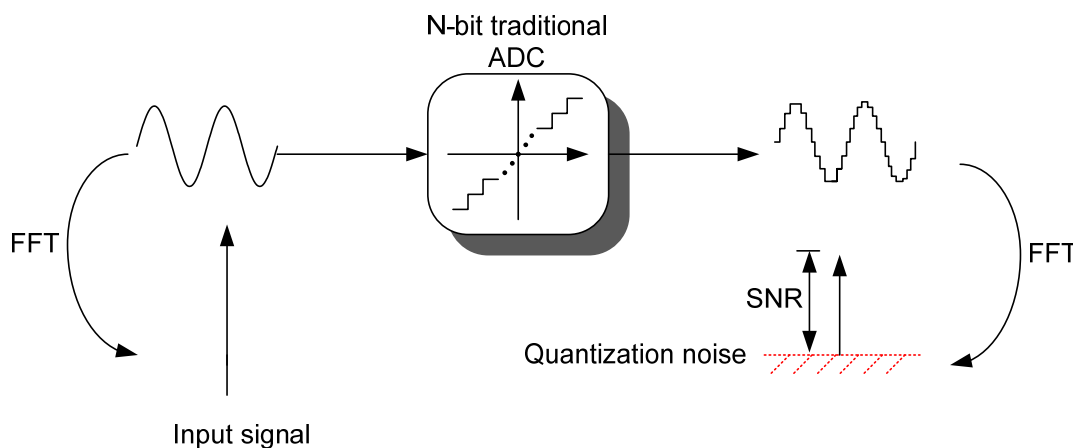


Fig. 3.1. The operation of the traditional n-bit ADC.

In ΣΔ ADCs, a close loop system composed by the loop filter, n-bit quantizer, and

feedback DAC is constructed as depicted in Fig. 3.2. There are still quantization errors but these can be minimized due to the oversampling effect. The quantization noise is modeled as a noise source after the quantizer. However, unlike the case of the traditional ADC, the quantization noise will be shaped by the transfer function of the close loop system since the input signal is injected in a different node.
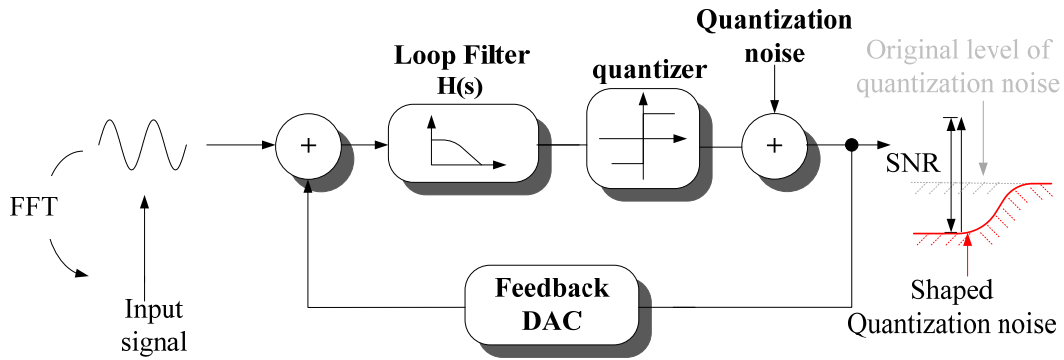


Fig. 3.2. The system of the ΣΔ ADC.

Based on the feedback theory, the transfer function for the quantization noise, defined as noise transfer function (NTF), is approximated as

$$NTF = \frac{1}{1+H(s)} \tag{3.2}$$

if the loop is linearized and assuming that the gain of the quantizer and DAC is unity. By using H(s) with high passband gain, the quantization noise will be further reduced. Regarding the input signal, the transfer function for the input signal (STF) is obtained as

$$STF = \frac{H(s)}{1+H(s)} \tag{3.3}$$

It can be observed that the signal appears at the output of the system without any

attenuation in the band of interest. Fig. 3.3 shows the NTF and STF of a ΣΔ ADC if an ideal second order lowpass loop filter is employed. The gain of the STF is equal to one while that of NTF is about zero. The high-pass NTF (in lowpass ΣΔ ADCs) or band-reject NTF (in bandpass ΣΔ ADCs) allow us to obtain better SNR without employing the quantizers with higher resolution or same SNR by using lower bit quantizers. Therefore, the resolution of ΣΔ ADCs depends not only on the resolution of the quantizer, but also on the filter's order and the sampling frequency, which are described in section 2.3.2.
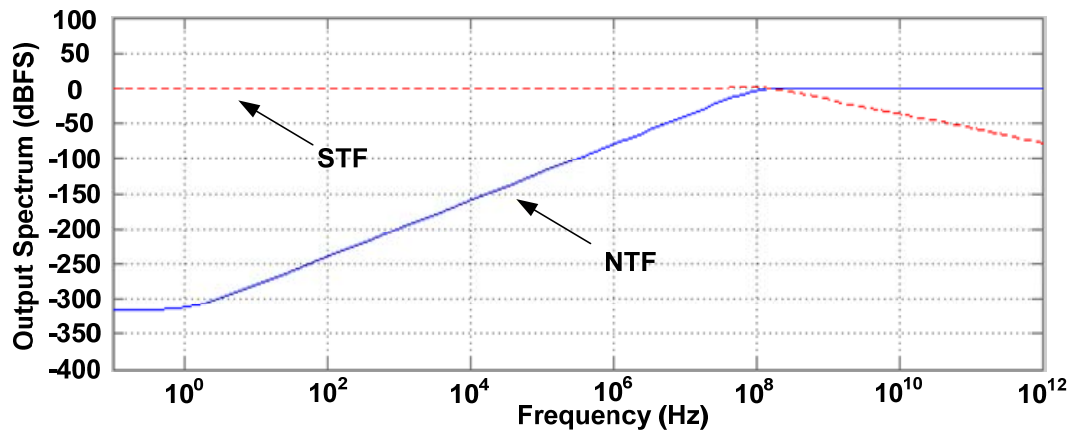


Fig. 3.3. The NTF and STF of the lowpass ΣΔ ADC with an ideal second order loop filter.

As a conclusion, in a ΣΔ ADC, the attenuation of the quantization noise demands on the loop gain, the total quantization noise power is determined by the resolution of the quantizer, and the sampling frequency $(F_s)$ spreads the total quantization noise power into the frequency range of DC to $F_s$ as shown in Fig. 3.4. [9] analyzed the relation between the SNR of a ΣΔ ADC and these three system parameters and obtained the equation (3.4):
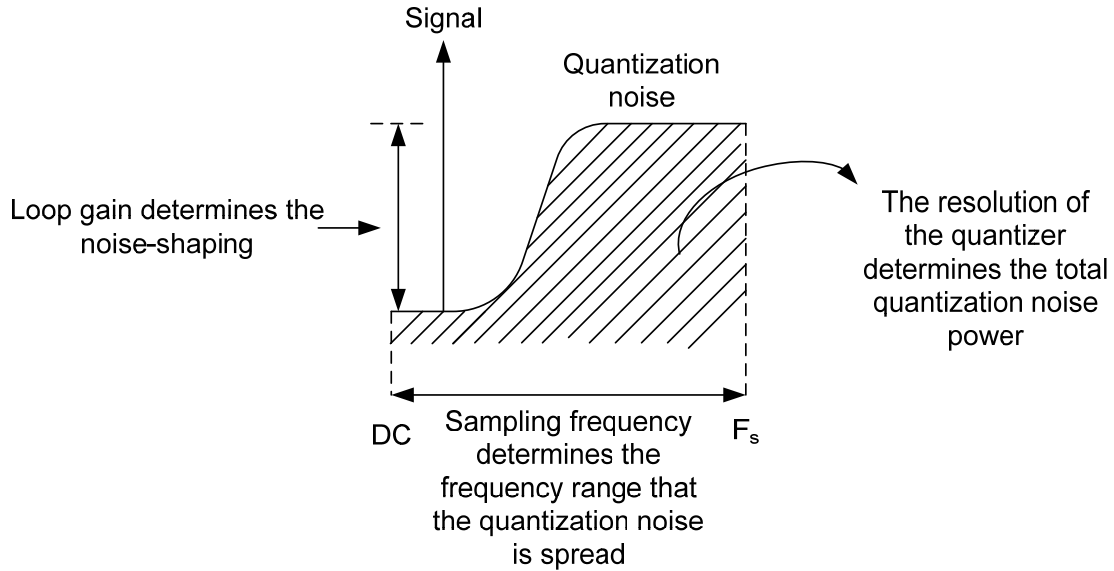
Fig. 3.4. The effect of the system coefficients to the output quantization noise.

$$SNR_{max} = 10 \log_{10}(\frac{1.5(N+1)OSR^{N+1}}{\pi^N}) + 6.02(B - 1) \qquad (3.4)$$

where N means the order of the bandpass loop filter (it will be 2N for the order of the lowpass loop filter), OSR is the oversampling ratio, which is $f_{sampling}/(2 \cdot$ signal bandwidth), and B is the bit number of the quantizer and feedback DACs. Increasing these parameters can improve the resolution of the ΣΔ ADC. However, there are always trade-off issues behind all optimization procedures. These the issues will be discussed in section 3.2.

3.1.2   The comparison between the discrete-time ΣΔ ADC and the continuous-time ΣΔ ADC

ΣΔ ADCs are mainly divided into two different categories based on the location of the sample-and-hold (S/H): discrete-time (DT) and continuous-time (CT) ADCs. Fig. 3.5 shows the block diagrams of these two architectures. For discrete-time type, because S/H

locates at the input stage, switch-capacitor filter is normally employed to process the discrete-time signal. The continuous-time ADC employs continuous-time loop filter since the S/H locates after the filter.
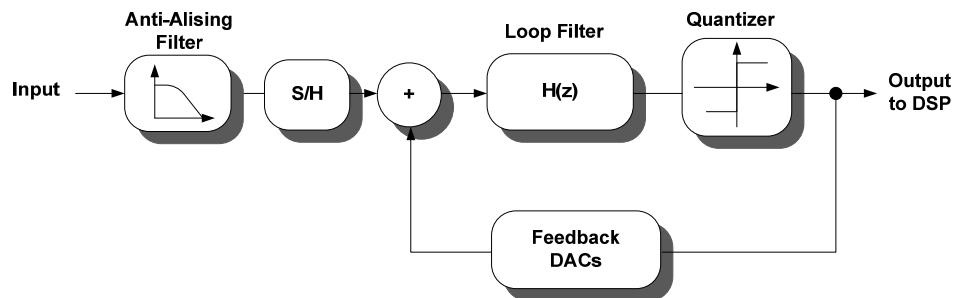


(a)
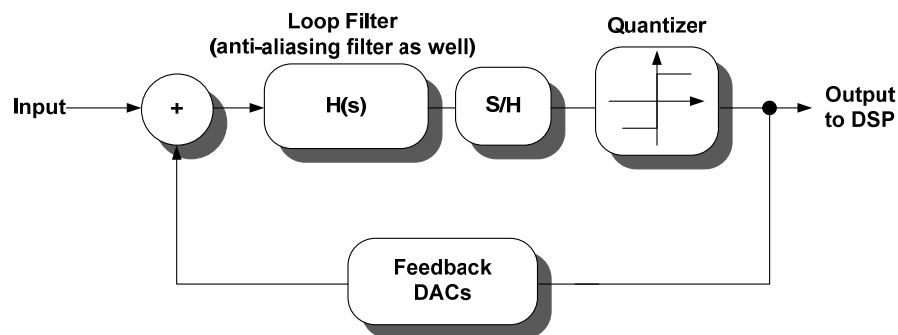


(b)

Fig. 3.5. Block diagrams of two different sigma-delta ADCs
(a) discrete-time (b) continuous-time.

Based on the high precision of the capacitor ratio in technologies and the low feedback charge at the switching instant in switch-capacitor DACs, low sensitivities to process variations and jitter noise are the greatest advantages of the discrete-time $\Sigma\Delta$ ADC because of the usage of the switch-capacitor filters and DACs. However, since the filter is after the signal sampler, an additional anti-alias filter before the ADC is needed

to prevent the aliasing effect. The total power consumption is therefore increased because of this additional anti-alias filter. Fig. 3.6 (a) presents the aliasing effect in the S/H. If an out-band blocker with the frequency of $f_s+f_x$ is injected into a S/H with sampling frequency of $f_s$, the aliasing effect will move this out-band blocker to the frequency of $f_s-f_x$. This aliased blocker is thus in the band of interest and degrades the system performance. An additional anti-aliasing filter can attenuate the out-band blockers in advance and alleviate the aliasing effect as depicted in Fig. 3.6 (b).



(a)



(b)
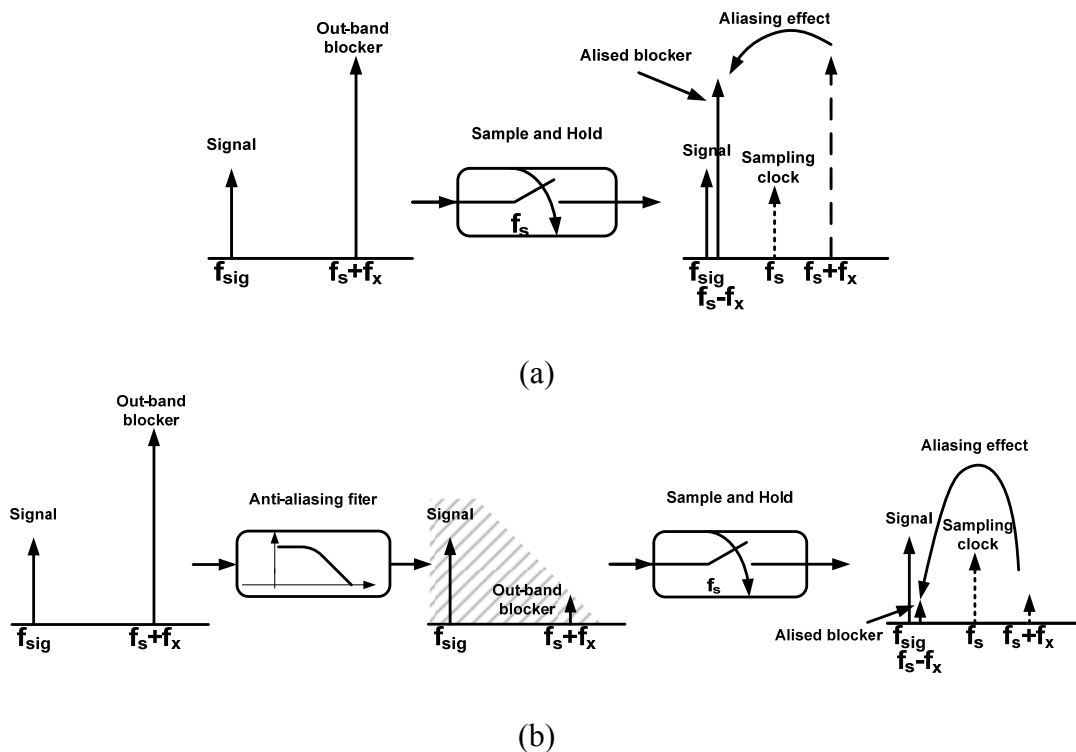
Fig. 3.6. The aliasing effect of the sampling and hold circuit
(a) without anti-aliasing filter (b) with anti-alias filter.

In addition, the speed of switch-capacitor (SC) filter is also constrained lower than few hundred MHz due to the operation fundamentals. In sampling phase, the input voltage needs to charge the sampling capacitor. The time-constant from the on-resistance of the switches and the sampling capacitor constraints the charge speed. In amplification phase, the amplifier needs certain time to react the large step at the input due to its limited bandwidth. The processing time in these two phases determines the operational speed of a SC filter. As a consequence, discrete-time $\Sigma\Delta$ ADCs are performed for low frequency applications based on the current technologies and circuit design techniques. For continuous-time type, the S/H is located after the loop filter. The filter operates as an anti-alias filter. Besides, the speed of the filter can be up to GHz range based on the topology and the realization. Therefore, in most of the bandpass $\Sigma\Delta$ ADC applications, continuous-time type is the choice to achieve the specifications [10].

1. The speed limit: the speed of DT $\Sigma\Delta$ ADC is limited by the amplifier's bandwidth and slew rate and the settling time during each transition. In contrast, the CT $\Sigma\Delta$ ADC operates continuously without any transition and the requirement of the amplifier's bandwidth is relaxed.

2. The need of extra anti-aliasing filter in front of ADC: The DT $\Sigma\Delta$ ADC requires an additional anti-aliasing filter before the S/H to attenuate the power of the out-band blockers that will alias back into baseband. In CT $\Sigma\Delta$ ADC, the loop filter can perform as the anti-alias filter because of its S/H.

With a decision on the categories of $\Sigma\Delta$ ADCs, next step is to determine the architecture of the loop filter.

3.1.3   The architecture of the loop filter: CRFF and CRFB

Based on the architecture of the loop filter, ΣΔ ADCs can be also divided into two different topologies: the cascade of resonators with feed forward (CRFF) and the cascade of resonators with feedback (CRFB). These two topologies can be implemented in both discrete-time and continuous-time domains.

Taking a $4^{th}$-order CT ΣΔ ADC for example, Fig. 3.7 shows two different architectures. In CRFF architecture all the output of the integrators feed forward to the input of the quantizer and there is an additional path directly from input to the quantizer. In CRFB, instead of feed-forward paths, there are feedback paths between integrators and DACs. Both architectures have enough degree of freedom to control the desired STF and NTF, and both have their own advantages and drawbacks.

In CRFF, synchronization issues are minimum since there is only one feedback DAC. The input signal is directly passed to the input of the quantizer through b5 path in CRFF making the swing of the internal nodes between integrators smaller and relaxing the linearity requirement of the filters. However, the design of the adder in front of the quantizer in CRFF is a challenge especially in the application with high sampling frequency. The adder is connected to several resistive and capacitive loads but the bandwidth requirement is extremely large to prevent excessive loop delay. In addition, with non-ideal integrators in the ADCs, the out-band blocker rejection is minimized in CRFF due to the b1 feedforward path. Fig. 3.8 depicts the difference of the out-band blocker rejections in $2^{nd}$-order ΣΔ ADCs with CRFF and CRFB architectures by comparing their STFs. Both ADCs have the same NTF. $2^{nd}$-order and $1^{st}$-order out-band blocker attenuations are achieved in CRFB and CRFF architectures respectively. In

currently reported works, both architectures are popular based on the different applications and different considerations.



(a)



(b)
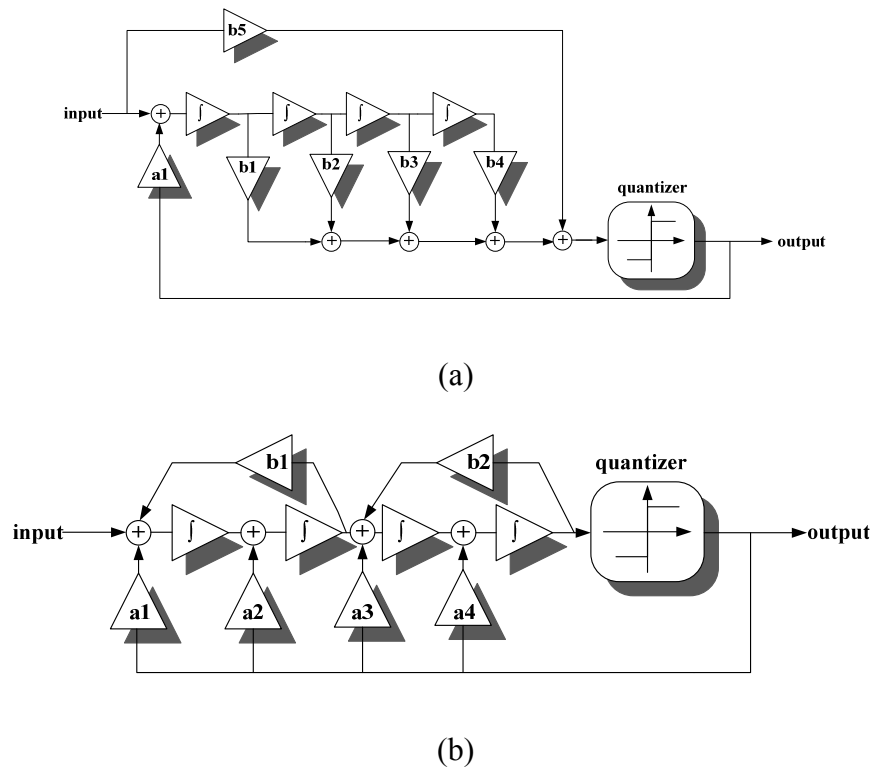
Fig. 3.7. Two different architectures of loop filter in $\Sigma\Delta$ ADC (a)CRFF (b)CRFB.
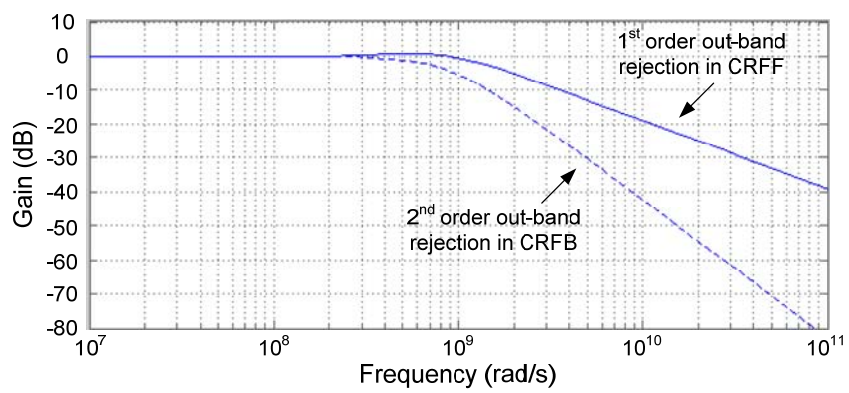


Fig. 3.8. The comparison of STFs in CRFF and CRFB architectures.

3.1.4    Multi-stage noise-shaping (MASH)

The MASH architecture was developed to achieve higher resolution. In this architecture, by cascading the noise-shaping loop, the actual order of noise-shaping can be higher than that of each individual loop. The DT architecture is plotted in the Fig. 3.9.
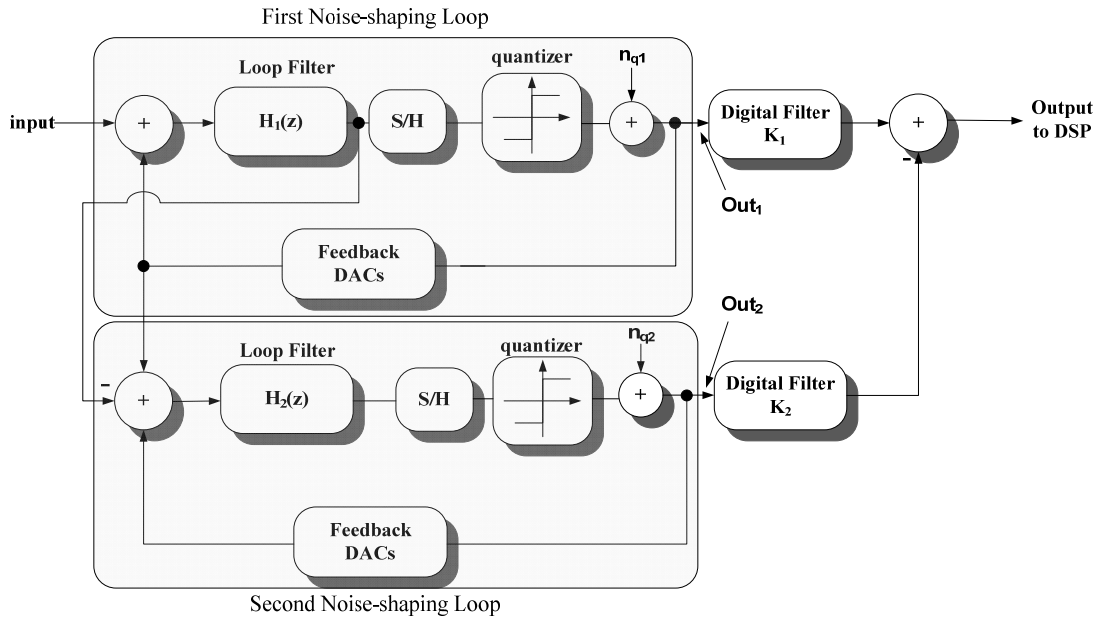


Fig. 3.9. The architecture of a DT MASH ΣΔ ADC.

The main concept of the ΣΔ ADC is to shape the quantization noise of the first loop again by employing a second loop. Suppose the quantization noise in the first loop and the second loop are $n_{q1}$ and $n_{q2}$, respectively. The output of the quantizer in first loop and that in the second loop will be given as

$$Out_1 = STF_1 \cdot input + NTF_1 \cdot n_{q1} \tag{3.5}$$

$$Out_2 = STF_2 \cdot n_{q1} + NTF_2 \cdot n_{q2} \tag{3.6}$$

By designing the digital filters $K_1$ and $K_2$ with the relation as below

$$K_1 \cdot NTF_1 = K_2 \cdot STF_2 \tag{3.7}$$

A solution that $K_1 = k \cdot STF_2$ and $K_2 = k \cdot NTF_1$ (k is a constant) is able to be reached from (3.7). As a result, the overall output will be

$$Out = K_1 \cdot Out_1 - K_2 \cdot Out_2 = k \cdot STF_1 \cdot STF_2 \cdot input - k \cdot NTF_1 \cdot NTF_2 \cdot n_{q2} \tag{3.8}$$

The quantization noise in the first loop is perfectly cancelled out while that in the second loop is noise-shaped by $NTF_1$ and $NTF_2$. If second order loops are used, the overall noise-shaping is now fourth order. In the ideal case, this is an excellent solution that an architecture achieves the same noise-shaping with less order loop filter and thus better stability condition.

However, under PVT variations, the equation (3.7) may not be satisfied. (3.9) presents the output of the ADC with variations. $NTF_1$' and $STF_2$' are the actual transfer functions composed by $NTF_1 + NTF_{1\Delta}$ and $STF_2$ $NTF_{2\Delta}$, respectively. The terms of $NTF_{1\Delta}$ and $STF_{2\Delta}$ are the errors due to PVT variations. The output of the ADC is now as

$$Out = K_1 \cdot Out_1 - K_2 \cdot Out_2 = k \cdot \left( STF_1 \cdot STF_2 \cdot input + NTF_1' \cdot STF_2 \cdot n_{q1} \right) -$$
$$k \cdot \left( NTF_1 \cdot STF_2' \cdot n_{q1} + NTF_1 \cdot NTF_2 \cdot n_{q2} \right) \tag{3.9}$$

An additional term of $k \cdot (STF_2 NTF_{1\Delta} - NTF_1 STF_{2\Delta}) \cdot n_{q1}$ in the overall output results in more serious degradation on quantization noise performance of the $\Sigma\Delta$ ADC as depicted in (3.10).

$$Out = k \cdot STF_1 \cdot STF_2 \cdot input - k \cdot NTF_1 \cdot NTF_2 \cdot n_{q2} +$$
$$k \cdot n_{q1}(STF_2 \cdot NTF_{1\Delta} - NTF_1 \cdot STF_{2\Delta}) \tag{3.10}$$

The issue is called noise leakage and is the dominant problem when designing a MASH architecture. Typically, 5% coefficient mismatch results in 6dB SNR degradation in a MASH21 ΣΔ ADC [11]. Normally DT MASH ΣΔ ADC is more popular than CT MASH architecture since the switch-capacitor filters can achieve higher design accuracy than any other analog filters. This accuracy will help the system to hold the relation in equation (3.7). Therefore, in high speed applications, the MASH architecture is not a proper option for the ΣΔ ADCs.

## 3.1.5   DAC pulse selection

There are mainly three typical DAC pulses used in the continuous-time ΣΔ ADCs: return-to-zero (RZ), half-delayed-return-to-zero (HRZ), and non-return-to-zero (NRZ). The waveform of these three DAC pulses and the describing equations are depicted in Fig. 3.10 [10].

Every DAC pulses result in different s-domain transfer function when processing impulse invariant to convert the desired Z-domain NTF. Due to the characteristics of different pulses, these three kinds of DAC pulses have different sensitivities to jitter effects and excess loop delay. For example, as will be demonstrated in the following sections, the NRZ presents less sensitivity to jitter effects but is more sensitive to the excess loop delay; the RZ is worse on jitter but performs better with excess loop delay while the HRZ has poor performances on both jitter effect and excess loop delay. The detail of the reasons in these effects will be discussed in the jitter and excess loop delay sections. Therefore, before designing a ΣΔ ADC, an important decision on DAC pulses is definitely required based on the specifications and applications on jitter effect and excess loop delay.
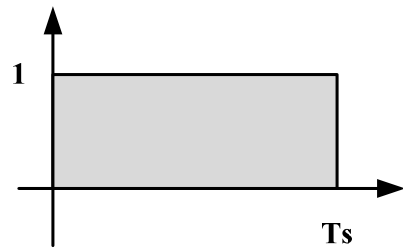
$$\hat{r}_{NRZ}(t) = \begin{cases} 1, 0 \le t < 0 \\ 0, otherwise \end{cases}$$

$$\hat{R}_{NRZ}(s) = \frac{1 - e^{-sT_s}}{s}$$
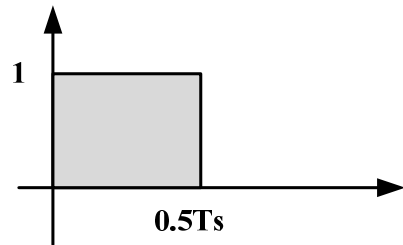
$$\hat{r}_{RZ}(t) = \begin{cases} 1, 0 \le t < 0.5Ts \\ 0, otherwise \end{cases}$$

$$\hat{R}_{RZ}(s) = \frac{1 - e^{-sT_s/2}}{s}$$
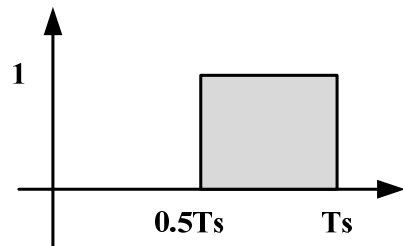
$$\hat{r}_{HRZ}(t) = \begin{cases} 1, 0.5Ts \le t < Ts \\ 0, otherwise \end{cases}$$

$$\hat{R}_{HRZ}(s) = e^{-sT_s/2} \frac{1 - e^{-sT_s/2}}{s}$$

Fig. 3.10. Common DAC pulses.

3.2 Design Issues of A Continuous-Time ΣΔ ADC

The ΣΔ ADC achieves high resolution without employing a high-bit quantizer by noise-shaping the quantization noise with the loop filter. However, the quantization noise is not the only noise source presented in the loop. Other noise sources and non-linearities from the components in the system would affect the performance and degrade the system resolution. Being aware of all the physical sources of related non-idealities and currently reported solutions would help developing new techniques to alleviate the issues.

3.2.1   Stability

Stability is always an issue in closed loop systems. Especially when increasing the order of the loop filter to achieve better resolution, the stability of the closed loop system is threatened by additional zeros and poles [12]. To check the stability of the system, the phase portrait technique can be utilized in both CT and DT ΣΔ ADC architectures since a ΣΔ ADC is a non-linear close loop system [13].

Suppose there is a 2$^{nd}$-order ΣΔ ADC as shown in Fig. 3.11 where the quantizer is modeled as an unity gain stage with the addition of the quantization error term $n_Q$ due to its operational characteristics. Vin, Vx, Vn, and Ve are the voltage of different nodes in the system. Under the assumption of sinusoidal wave operation in the quantizer, the $n_Q$ can be model as

$$n_q = \frac{8}{\pi^2} \cdot \frac{v_{FS}}{2^{(B+1)}} (\sin(w_s t) - \frac{1}{9}\sin(3w_s t)\cdots\cdots)$$

(3.11)

Based on the loop analysis, an ODE equation can be obtained as

$$\ddot{v}_e = k_1 v_{in} - b_1 \frac{16}{\pi^2} \frac{v_{FS}}{2^{(B+1)}} \cdot OSR \frac{16}{\pi^2} \frac{v_{FS}}{2^{(B+1)}} + f_s \cdot OSR - b_2 \dot{v}_e - b_1 k_1 \cdot v_e \quad (3.12)$$
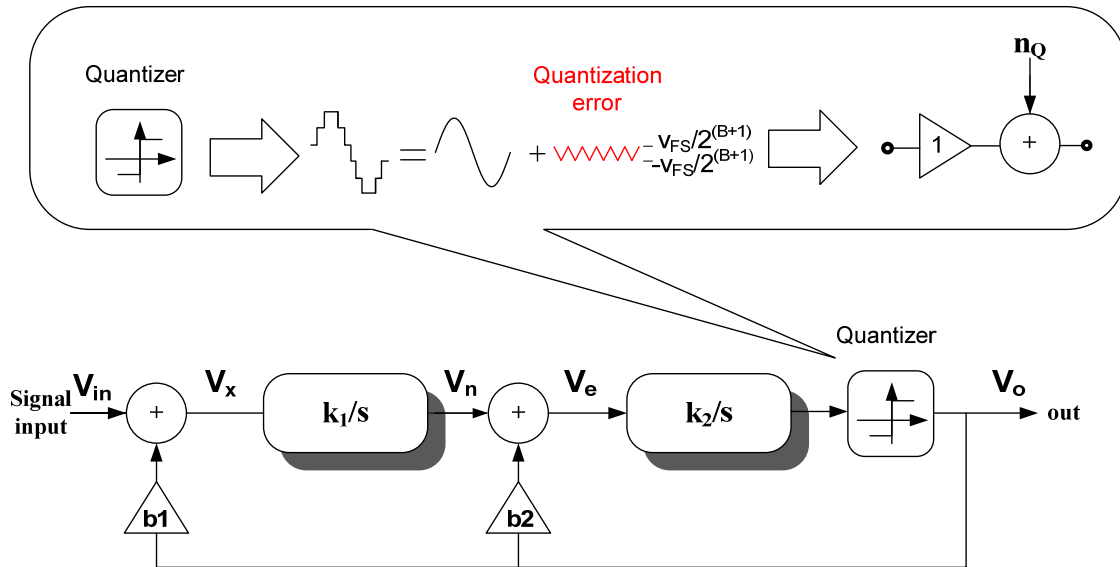


Fig. 3.11. A 2nd-order $\Sigma\Delta$ ADC with approximated quantizer model.

From (3.12), all the coefficients such as the full scale and bit number of the quantizer, OSR, sampling frequency, the amplitude of input signal, and the feedback parameters will determine the stability condition of the system. Commands "dfield7" or "pplane7" in Matlab can help solving (3.12) with different initial conditions and the result is depicted in Fig. 3.12. From Fig. 3.12, since all lines are converged into a point, it presents that the 2nd-order $\Sigma\Delta$ ADC with 2-bit quantizer, 40 of OSR, and 800MHz sampling frequency is stable.
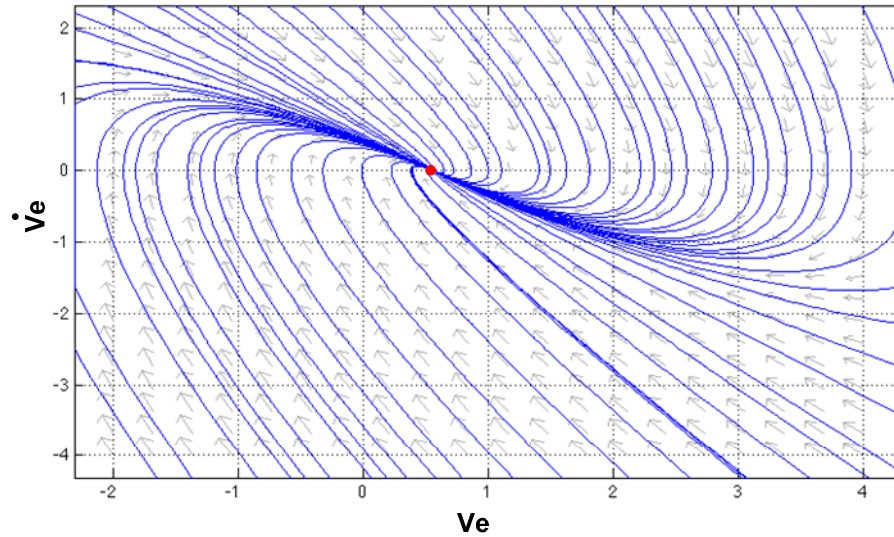
Fig. 3.12. The phase portrait of a 2nd-order ΣΔ ADC.

For the higher order ΣΔ ADC, the phase portrait analysis can be used as well and the higher order ODE equation from the system will be obtained. By plotting the speed of error versus error magnitude as Fig. 3.12, the stability conditions of the system with different system coefficients and different initial conditions can be estimated. Thus, the sufficient stability condition can be achieved during the system planning phase. The simulation-based stability check in the system simulation phase is also recommended to confirm the system stability.

3.2.2 Non-linearities

In a single-bit ΣΔ ADC, the sources of non-linearities are basically from the non-linearities of the loop filter. As shown in Fig. 3.6, either CRFF or CRFB has integrators in the loop filter. The non-linear Op-amps within the integrators contribute the harmonic distortions, which degrade the resolution of the ADC. By assuming there are two filter stages in loop filter, Fig. 3.13 models the distortion contribution of each filter stage as extra terms D1 and D2.
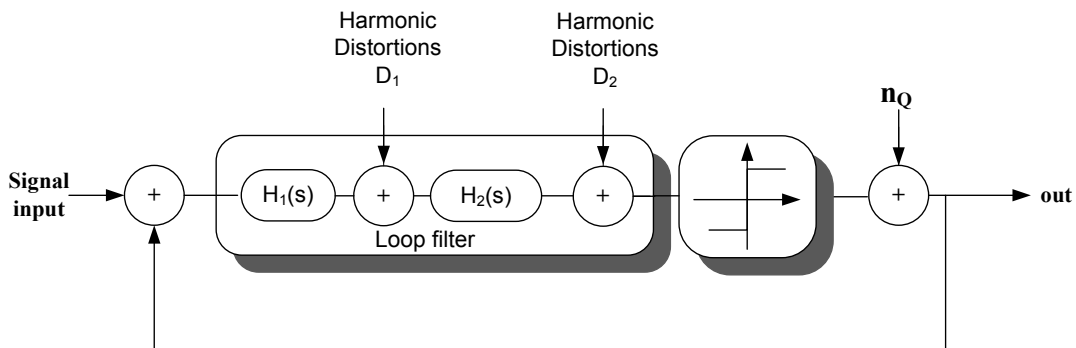


Fig. 3.13. The model of the non-lineairties from loop filter in a ΣΔ ADC.

The closed loop transfer function for $D_1$ and $D_2$ thus can be determined as below.

$$\frac{out}{D_1} = \frac{H_2(s)}{1+H(s)} \tag{3.13}$$

$$\frac{out}{D_2} = \frac{1}{1+H(s)} = NTF \tag{3.14}$$

(3.13) and (3.14) show that the distortions of the second stage are noise-shaped as the quantization noise and that of the first stage are partially noise-shaped by the loop; this

makes the non-linearity of the first filter stage dominate the linearity performance of a $\Sigma\Delta$ ADC.

If increasing the bit number of the quantizer, another critical linearity issue appears: the unit current source mismatch in multi-level DACs. This mismatch generate the distortions $D_{DAC}$ at the output of the DAC as depicted in Fig. 3.14. Since the DAC is connected to the input stage, $D_{DAC}$ will pass through the system as input signal and degrades the performance of the ADC. Taking a 2-bit $\Sigma\Delta$ ADC with switch current DACs as shown in Fig. 3.15, there are three identical current sources controlled by the thermometer code from the output of the quantizer to produce a four-level feedback. In ideal case, the current of the current sources are identical and, hence, there is no distortion in the two-tone test of a $\Sigma\Delta$ ADC. However, random static mismatches between devices are presented in all the components and transistors in the chip; this mismatch changes the current flowing on current sources by random errors $\Delta_1$, $\Delta_2$, $\Delta_3$. The differences between levels of the feedback are no longer identical and thus the static mismatch introduces the distortions into the system. This non-linearity from the DAC feeding the signal back to the input stage is not noise-shaped by the closed loop and the signal-to-noise-and-distortion ratio (SNDR) of the system is hence degraded. Therefore, without a solution for this issue, the improvement on ADC resolution by increasing the number of bits in the DAC and quantizer is limited.

To alleviate this issue, several solutions have been reported; e.g. noise-shaping dynamic element matching loop (NSDEM) [14], tree-structure DEM [15], Data-weighted algorithm (DWA [16]) or butterfly shuffler [17]. These techniques either randomize or shape the non-linearity, as shown in Fig. 3.16.

Fig. 3.14. The model of the distortions from DAC in a $\Sigma\Delta$ ADC.



Fig. 3.15. The source of device mismatch and the effect on the resolution of a 2-bit $\Sigma\Delta$ ADC.

By building a close loop system in DACs, NSDEM (Fig. 3.15 (a)) technique employs noise-shaping DACs in a $\Sigma\Delta$ ADC to attenuate the non-idealities from the DACs including the distortions. Tree-structure DEM (Fig. 3.15 (b)), DWA (Fig. 3.15(c)) and Butterfly shuffler (Fig. 3.15 (d)) all uses the switches or shifters controlled by the pseudo-random codes generated by the digital logic circuitry to randomly connect the DACs to different output codes from the quantizer. This randomization translates the static errors (distortions) into dynamic errors (white noise) and hence, the SNDR is improved when the distortions dominate the ADC resolution. The threat to the system stability is the common issue of these four techniques due to the delay contribution from the extra processing in the feedback path.
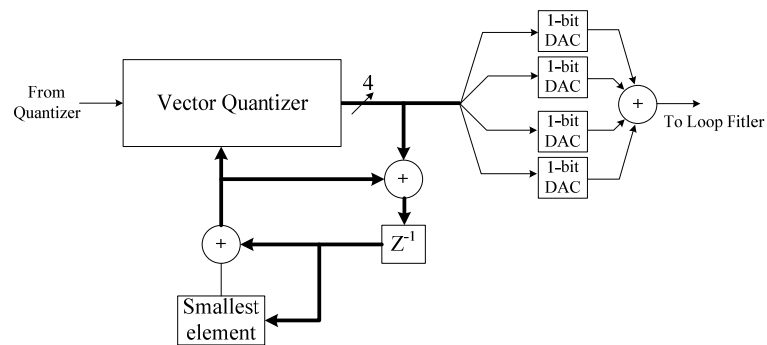


(a)
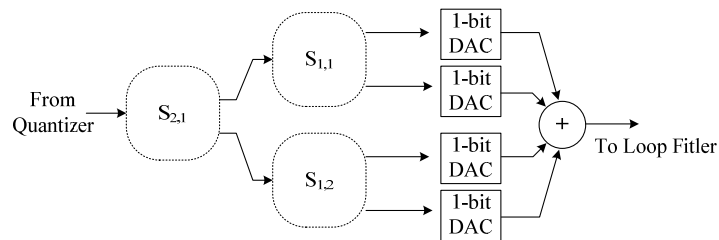


(b)

Fig. 3.16. Four general different schemes to randomize or shape the mismatch
(a) NSDEM (b) tree-structure DEM.

(c)



(d)
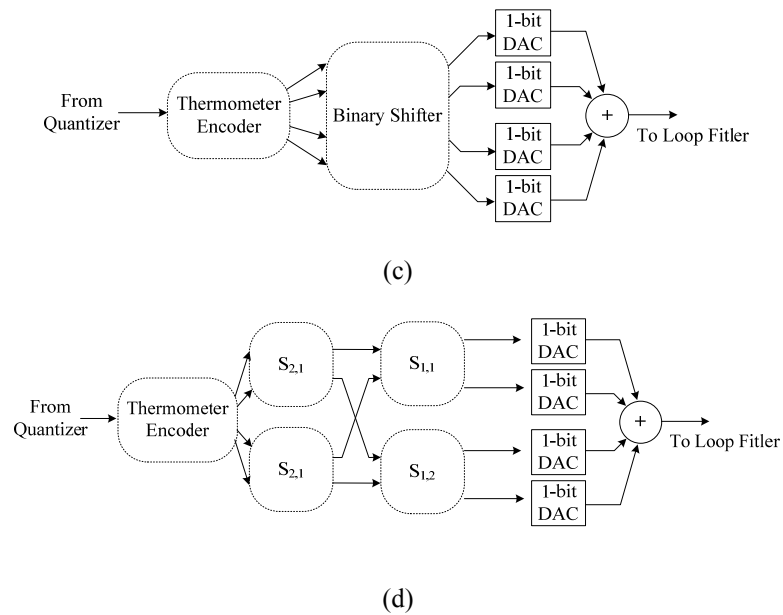
Fig. 3.16. Continued (c) DWA (d) butterfly shuffler.

### 3.2.3   Jitter effect

Clock jitter accounts for the random variation on the transition time of a clock or any waveform from the oscillator or signal generator as shown in Fig. 3.17. This random transition variation can be modeled as an additional error expressed as

$$\sigma_e^2 = \sigma_y^2 \cdot \left(\frac{\sigma_t^2}{T_s}\right) \tag{3.15}$$

where $\sigma_y$ is the standard deviation associated with the average transition per period and the amplitude of the clock, $\sigma_t$ is the standard deviation of the timing error, and $T_s$ is clock period.
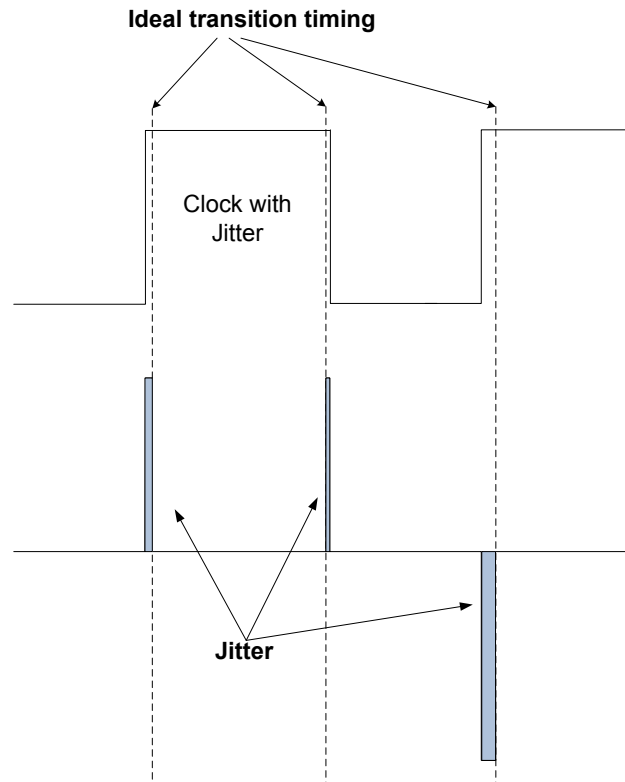
Fig. 3.17. The jitter effect on a square waveform.

When a reference clock with jitter is employed in a ΣΔ ADC, the digital circuits utilizing this clock translate this jitter noise into the system; this will cause the random variation on the feedback charge from DACs into the loop filter. As the input signal, the jitter noise from the DAC connecting to the input stage is not noise-shaped by the system and thus degrades the resolution of the ΣΔ ADC. [18] estimates the signal-to-jitter noise ratio (SJNR) as below

$$\text{SJNR} = 10 \log_{10} \frac{\text{OSR} \cdot V_{in}^2}{2 \cdot \sigma_y^2 \cdot \left(\frac{\sigma_t}{T_s}\right)^2} \tag{3.16}$$

where $v_{in}$ is the amplitude of the input signal and OSR is the oversampling ratio. $\sigma_y$ is different for different system architectures. In the design with low sampling frequency,

since the variation of the charge only take very low portion of the total feedback charge, the jitter effect responding on the degradation of the resolution is not obvious in spite of low over-sampling ratio. As a consequence, the jitter noise is usually one of the important issues that have to be considered in advance in order to achieve the required resolution with high sampling frequency. The SJNR comparison in Fig. 3.18 demonstrates that the systems with higher sampling frequency are more sensitive to the jitter noise.
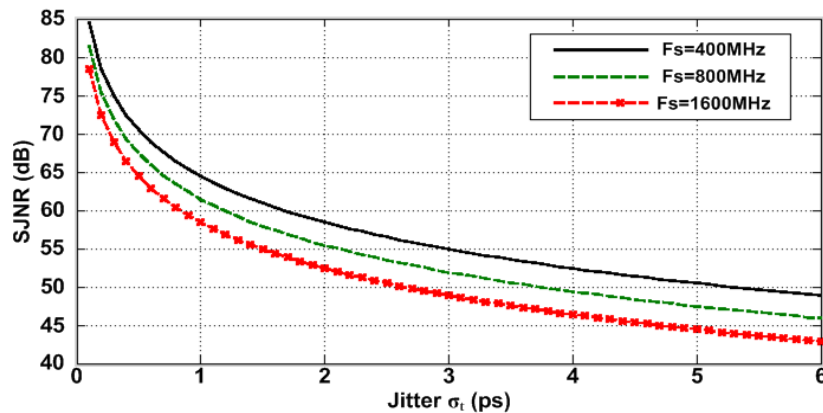
Fig. 3.18. The SJNR comparison between the systems with different sampling frequencies.

Different architectures of DACs or different pulse shape will result in different levels of the jitter sensitivity. The switch-capacitor type (SC) DAC used in the discrete-time ΣΔ ADC has better performance on jitter than the switch-current DAC because the transitions always happen in the settled condition of the DAC feedback. The NRZ switch-current DAC is better than the RZ and HRZ DACs since there is at most one transition in one sampling period while the other two have at most two transitions.

Instead of using the square pulse shape, some of the reported works use different signal shapes such as triangular or sinusoidal ones to prevent the large level transitions as square wave. Therefore to consider the effects of jitter noise of a continuous-time $\Sigma\Delta$ ADC with high-frequency sampling clock is extremely important. The phase noise performance of the oscillator generating reference clock is then a key component that may limit the ADC's performance. (Phase noise and jitter describe the same physical noise source of an oscillator in two different aspects. Phase noise is in frequency domain while jitter is in time domain. There are functions to translate from one to the other [19]).

### 3.2.4   Excess loop delay

There is always processing delay in digital circuitries. For example, most of the quantizers need half sampling period to sample and quantize the signal. A delay margin of a clock period is usually left in advance to allow the delay from the input of quantizer to the output of the DAC when designing a $\Sigma\Delta$ ADC. However, due to process, voltage, and temperature (PVT) variations, the actual delay can never be predicted accurately. The extra delay from the delay margin is defined as the excess loop delay. The excess loop delay changes the loop transfer function and degrades the ADC resolution and stability.

Z-domain root locus can be used to systematically analyze the effect of the excess loop delay.  Taking a 6th-order single-bit $\Sigma\Delta$ ADC shown in Fig. 3.19, H(z) is the Z-domain loop transfer function including one sampling period delay and is expressed as (3.17).

$$H(z) = \frac{2.736z^5 - 0.1144z^4 + 2.794z^3 - 0.1144z^2 + 0.9477z - 0.00332}{z^6 + 2.768z^4 + 2.559z^2 + 0.7901} \quad (3.17)$$

$Z^{-d}$ is the term associated with the excess loop delay and d presents the excess loop delay as the percentage of the sampling period. The NTF is then obtained as

$$NTF = \frac{1}{1 + H(z) \cdot z^{-d}} \quad (3.18)$$
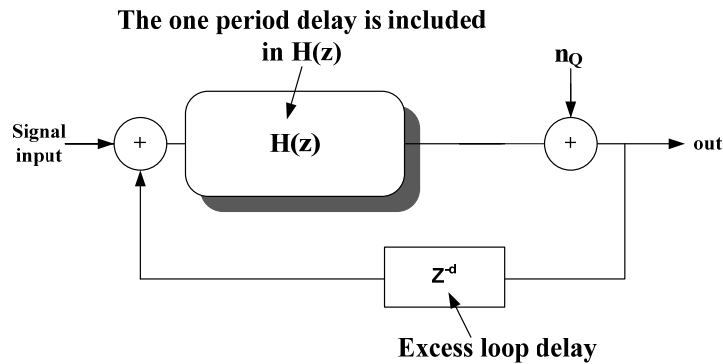


Fig. 3.19. The block diagram of a 6th-order single-bit $\Sigma\Delta$ ADC.

Fig. 3.20 depicts the root locus of the NTF under different level of excess loop delay (d=0~100%). With no excess loop delay ($z^{-d}$=1), all the poles and zeros are in the unite circle and system is stable. The excess loop delay term inserts a pole-zero pair into the system and moves all the poles. When d > 20% of the sampling period, two of the poles are out of the unite circle and the stability condition is invalid. Therefore, the excess loop delay has to be less than 20% of the sampling period to ensure the stability in this case.
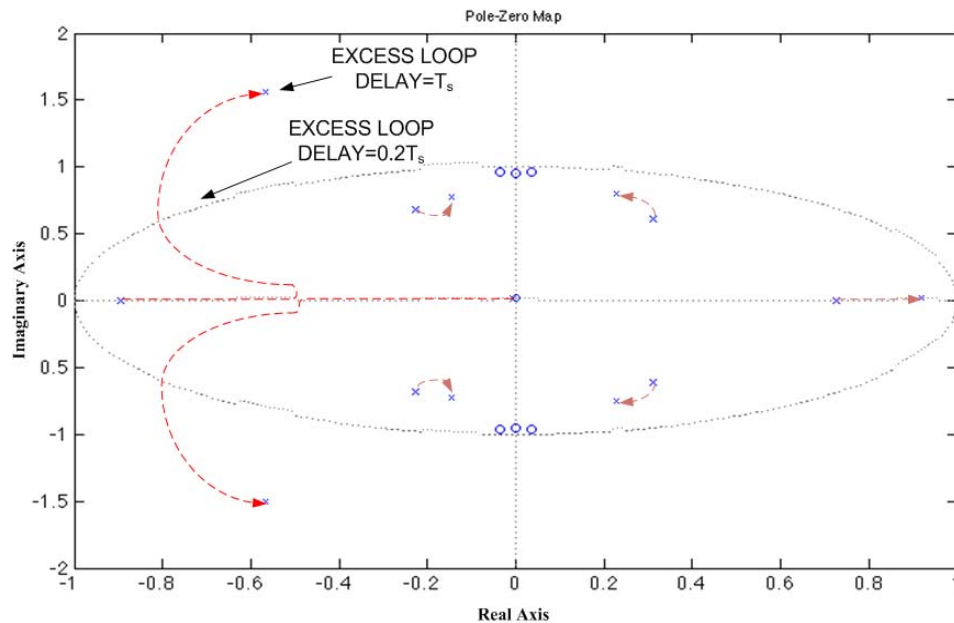
Fig. 3.20. The root locus of NTF of a 6$^{th}$-order binary $\Sigma\Delta$ ADC under different excess loop delay.

The excess loop delay is especially a serious issue in high OSR applications. If the sampling frequency is increased from 100MHz to 10GHz, it means that the affordable excess loop delay to ensure the system stability decreases from 2n second to 20p second which is shorter than the delay contribution from a transmission line.

There are two methods to compensate the excess loop delay. One is to build a fast feedback path from the output of the quantizer to its input; another is to adopt a programmable delay compensator in the global feedback path. Forming a fast feedback path is mainly to compensate the change of the NTF caused by the excess loop delay. Suppose there is a 2$^{nd}$-order $\Sigma\Delta$ ADC shown in Fig. 3.21 (a) where d is the excess loop delay in terms of the percentage of sampling period. The system open loop transfer

function H(z) should be expressed as (3.19) such that a 2$^{nd}$-order noise shaping can be obtained (NTF =$1/(1+H(z))=(1-z^{-1})^2$).

$$H(z) = \frac{2z-1}{(z-1)^2} \tag{3.19}$$

Assuming there is a 100% excess loop delay (d=1), equation (3.19) with the additional term of z$^{-1}$ cannot achieve the required NTF. By employing the additional fast feedback path with gain of k, the compensated open loop transfer function can be obtained as

$$H'(z) = \frac{(b1+b2)z-b2}{(z-1)^2} \cdot z^{-1} + k = \frac{kz^2+(b1+b2-2k)z+k-b2}{z(z-1)^2} \tag{3.20}$$

(3.19) can be obtained by using b1=1, b2=2, and k=2 in (3.20). Thus, the excess loop delay effect can be compensated. Fig. 3.21(b) depicts the method employing a programmable delay compensator. By sensing the total feedback delay in the chip and adjusting the delay level in the delay compensator, the excess loop delay can be minimized. However, both methods require the extra calibration mechanism to detect the exact loop delay and program the feedback coefficients or the required delay from delay compensator.
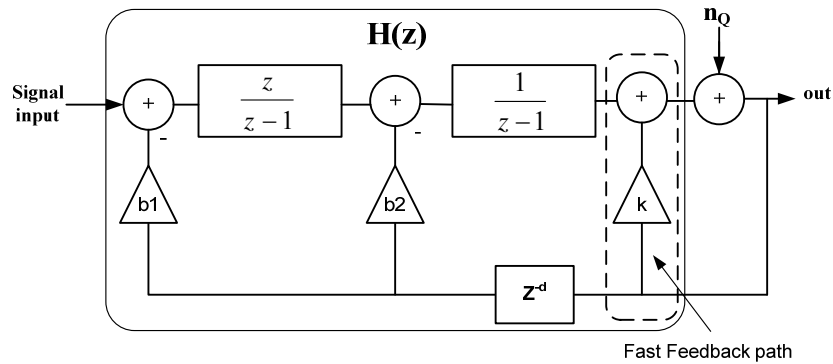
(a)
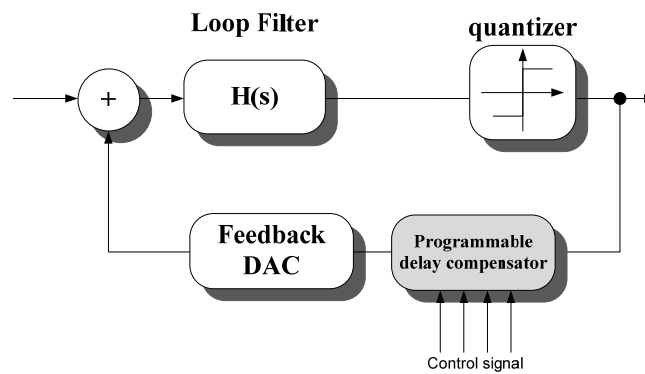


(b)

Fig. 3.21. Two methods to solve the issue of excess loop delay
(a) A fast feedback path (b) The programmable delay compensation.

## 3.3 Design Flow of A ΣΔ ADC

Based on the previous sections, we can conclude the comparison between different ΣΔ ADC architectures as below.

1. CT ΣΔ ADCs are suitable for applications with high sampling frequency due to the usage of continuous-time loop filters and prevents the extra anti-aliasing filter

before it. However, it is more sensitive to the jitter effect and PVT variations comparing with a DT one.

2. CRFF architecture relaxes the linearity requirements for the filters while CRFB has higher out-band blocker rejection. CRFF requires an adder with wide bandwidth before the quantizer to prevent the contribution on loop delay while CRFB has synchronization issues between DACs.

3. Increasing the number of quantizer bit (B), filter order (N), and oversampling ratio (OSR) in equation (3.4) can all achieve higher signal-to-quantization-noise (SQNR). However, increasing B causes the non-linearity effect from the device mismatch in the DACs; increasing N threatens the stability of the closed loop system since more poles and zeros are introduced; increasing OSR worsens the jitter performance, increases the power consumption of the digital circuits, and shrinks the allowable processing delay margin for digital circuitries to maintain the performance and stability. As a result, without complete considerations on these trade-offs, the improvement on SQNR by increasing B, N and OSR are limited.

4. Regarding the pulse shape of the DAC, SC DACs have the best jitter performance but it is not suitable for CT $\Sigma\Delta$ ADCs. NRZ DACs have better jitter performance but higher sensitivity to the excess loop delay comparing with RZ and HRZ DACs.

With above considerations, a complete design flow is plotted in Fig. 3.22. This design flow includes the design of DT and CT, LP and BP $\Sigma\Delta$ ADCs. The detail noise budgeting, loop transfer function derivation, and system simulation are presented in the

Chapter IV and Chapter V with actual specifications and considerations on non-idealities.
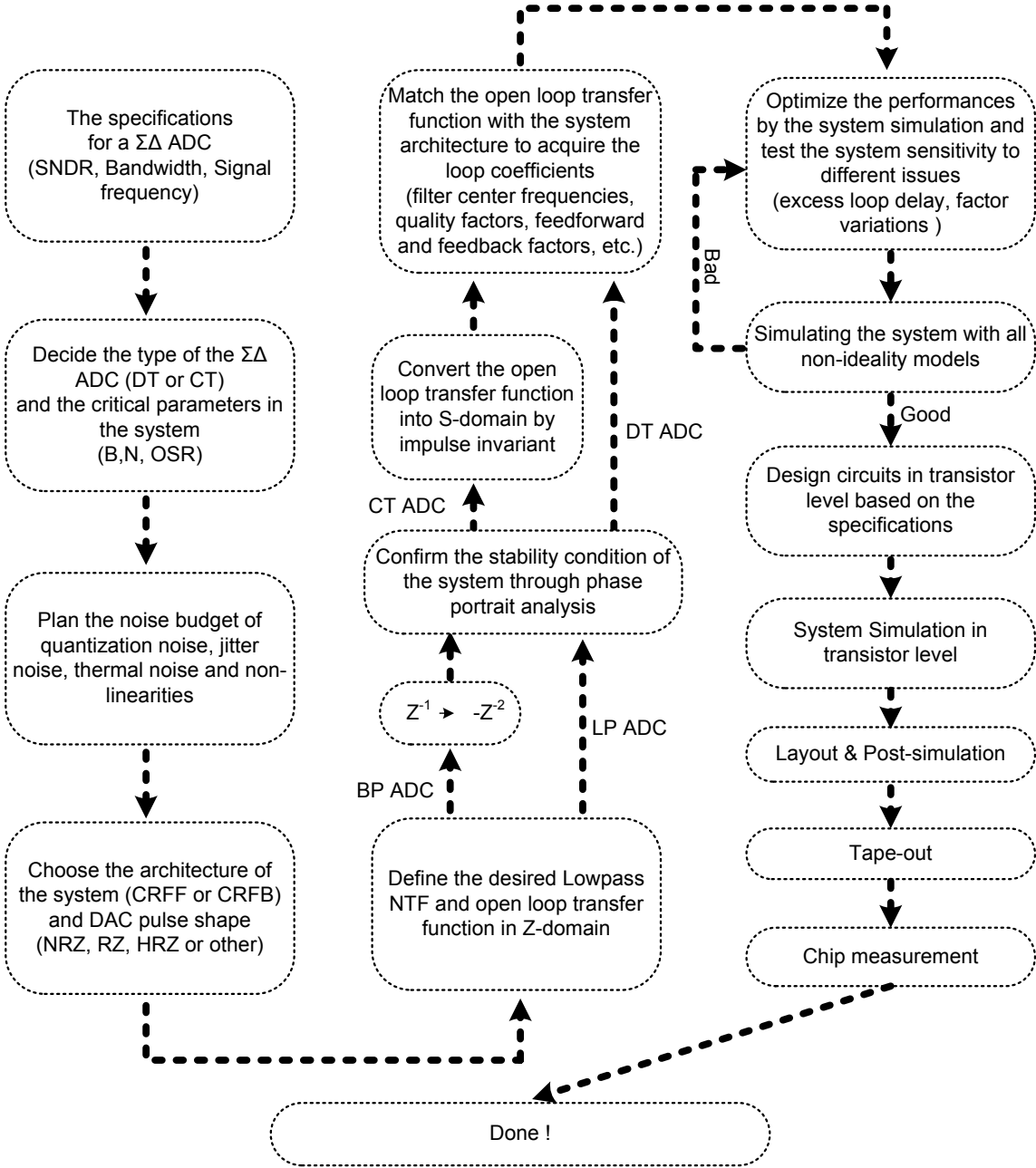


Fig. 3.22 Complete design flow of a ΣΔ ADC.

## 3.4 Literature Survey

In this section, the currently reported LP and BP ΣΔ ADCs are listed in the Table 3.1 in order to observe the choice of system architecture, loop filter architecture, DACs, and the critical system parameters such as number of quantizer bit, loop filter order and oversampling ratio [8], [20]- [30].

Table 3.1 Literature survey of the reported ΣΔ ADCs

| Ref | Type | IF (MHz) | Fs (MHZ) | BW (MHz) | SNDR @ BW | Power (mW) | Technology |
|-----|------|----------|----------|----------|-----------|------------|------------|
| [20] | 5$^{th}$ CT 1bit LP ΣΔ | - | 150 | 2 | 63dB | 2.7 | CMOS; 0.25um |
| [21] | 3rd CT 4bit LP ΣΔ | - | 640 | 20 | 74dB | 32 | CMOS; 0.13um |
| [22] | 3$^{rd}$ CT 1bit LP ΣΔ | - | 640 | 10 | 66dB | 7.5 | CMOS; 0.18um |
| [23] | 4$^{th}$ DT 4bit LP ΣΔ | - | 100 | 4 | 67dB | 11.76 | CMOS; 90nm |
| [24] | 2$^{nd}$ CT 5bit LP ΣΔ | - | 900 | 20 | 67 | 40 | CMOS; 0.13um |
| [25] | 2$^{nd}$ DT MESH BP ΣΔ | 40 | 60 | 2.5 | 69dB | 150 | CMOS; 0.18um |
| [26] | 4$^{th}$ CT 4bit BP ΣΔ | 44 | 264 | 8.5 | 71dB | 375 | CMOS; 0.18um |
| [27] | 2$^{nd}$ DT 1bit BP ΣΔ | 60 | 240 | 1.25 | 52dB | 37 | CMOS; 0.35um |
| [28] | 4$^{th}$ DT 4bit BP ΣΔ | 40 | 60 | 1 | 63dB | 16 | CMOS; 0.35um |
| [29] | 4$^{th}$ CT 1bit BP ΣΔ | 950 | 3800 | 1 | 59dB | 75 | SiGe; 0.25um |
| [30] | 4$^{th}$ CT 1bit BP ΣΔ | 2000 | 40000 | 60 | 55dB | 1600 | SiGe; 0.13um |
| [8] | 2$^{nd}$ CT 1bit LP ΣΔ | - | 40000 | 500 | 37dB | 350 | SiGe; 0.13um |

From Table 3.1, it is obvious that the DT ΣΔ ADC with switch-capacitor topology is only adopted when the sampling frequency is lower than few hundred MHz [22], [24], [26], [27]. Although the table doesn't show the system architectures of the designs, CRFF and CRFB are equally popular in different specifications and applications. However, in the designs with high sampling frequency, the CRFB is more frequently employed to avoid the contribution to the loop delay from the adder before the quantizer. In high OSR applications, most of the cases adopt 1-bit quantizer in order to prevent the non-linearity from device mismatch of multi-bit DACs. For the designs with multi-bit DACs, different dynamic element matching techniques are used to alleviate the mismatch issues. Due to the consideration on the cost, CMOS is the major technology to implement the designs of ADCs while SiGe BiCMOS technology is used in the RF ADCs with operational frequency higher than 1GHz.

Based on the design considerations in this chapter and the observation from the literatures listed in Table 3.1, we can start designing the ΣΔ ADC in different specifications. Chapter IV describes the design of a 200MHz IF CT CRFB BP ΣΔ modulator with 10MHz BW for the multi-standard application in high-IF receiver architectures. Chapter V presents the implementation of a 25MHz bandwdith $5^{th}$-order CT CRFF LP ΣΔ modulator with time-domain 3-bit quantizer and DAC for WiMAX application to alleviate the non-linearity issues from device mismatches of multi-level DACs by employing pulse-width modulation (PWM) technique.

**CHAPTER IV**

**A SELF-CALIBRATED 6$^{TH}$-ORDER 200MHZ IF BANDPASS ΣΔ MODULATOR**

**WITH OVER 68DB SNDR IN 10MHZ BANDWIDTH**

4.1 Introduction

The direct conversion receiver using an oversampling lowpass digitizer is popular nowadays since the signal is digitized at baseband. However, the digitization of high-IF channels presents several advantages over the lowpass counterpart since it does not suffer from flicker noise and static and dynamic offset issues. In the case of the digitalization by means of ΣΔ modulators, for the same oversampling ratio both bandpass and lowpass structures require similar clock frequencies as well as similar complexity for quantizer and DACs. The major difference is in the realization of the loop filter where the power consumption of this portion mainly depends on the operational frequency (IF frequency). Therefore, the requirements of low power, wide bandwidth, high signal frequency and high resolution lead to a very challenging bandpass ADC design.

So far, several papers reported the solutions for the bandpass architecture. The papers reported in [31] and [32] used multi-stage noise-shaping (MASH) bandpass discrete-time sigma-delta (ΣΔ) modulator and double-sampling to achieve 69dB signal-to-noise+distortion-ratio (SNDR) in 2.5MHz bandwidth at 40MHz intermediate frequency and 52dB SNDR in 1.25MHz bandwidth at 60MHz center frequency, respectively. The architecture reported in [26] reached 77dB Signal-to-Noise Ratio (SNR) in 8.5MHz bandwidth and 44MHz intermediate frequency by implementing a modified feedforward bandpass continuous-time ΣΔ modulator whose first stage is

directly coupled to the mixer employing an off-chip passive inductor. The solution reported in [28] adopted 2-path time-interleaved discrete-time $\Sigma\Delta$ modulator to obtain 65dB SNDR in 1MHz bandwidth at 40MHz operation frequency. By designing in 0.25um SiGe technology and 0.13um SiGe technology, respectively, [29] achieved 59dB SNDR in 1MHz bandwidth at 950MHz center frequency while RF $\Delta\Sigma$ modulators employing passive resonators have [30] achieved 55dB SNDR in 60MHz bandwidth at 2GHz center frequency. The architecture reported in [33] covers 0-1GHz frequency range by employing lowpass continuous-time $\Sigma\Delta$ modulator in 0.13um SiGe technology. A common denominator in the aforementioned architectures is the need of efficient calibration techniques to ensure loop stability and optimal ADC resolution.

In this chapter, the specifications of the ADC for high-IF receiver are shown in Table 4.1. With no specific location of the intermediate frequency in all wireless standards, a 200 MHz frequency was chosen to avoid the effects of flicker noise as well as to push the state of art for the ADC design in standard TSMC CMOS 0.18$\mu$m technology. With fs/4 architecture, the sampling frequency is set to 800MHz, a factor of 4 of the operational frequency. The 10MHz bandwidth and 12-bit resolution were selected to accommodate the bandwidth and resolution requirements for video applications. Based on these requirements, a 6th-order bandpass continuous-time $\Sigma\Delta$ modulator achieving a peak SNDR of 68.4dB when measured in 10MHz bandwidth is presented. Also, a unique software-based calibration method is proposed to tolerate the Process-Voltage-Temperature (PVT) variations.

The system planning including noise budgeting and the proposed architecture are addressed in section 4.2. In section 4.3, the circuit implementation of each critical block

is described. The software-based calibration approach is presented in Section 4.4, while Section 4.5 shows the measured modulator performance. The conclusions are provided in the section 4.6. The appendix in section 4.7 discusses the distortion analysis of a two-integrator loop active-RC filter with 3 stage amplifiers.

Table 4.1 The specifications of the CT BP ΣΔ modulator

| Specification | Value |
|---|---|
| IF signal frequency | 200MHz (Fs/4) |
| Clock frequency (Fs) | 800MHz |
| Signal bandwidth | 10MHz |
| Target SNDR | >74dB |
| Technology | TSMC 0.18um CMOS technology |

4.2 System Planning

In this section, the system planning of the bandpass ADC is discussed to achieve the required specifications by arranging the noise contributions from different noise sources, determining the required system transfer function, and analyzing the coefficients of the proposed system architecture.

4.2.1   Noise and distortion budgeting

In order to achieve the required signal-to-noise and distortion-ratio (SNDR), a detailed and practical planning on all different non-idealities such as quantization noise, jitter noise, thermal noise and building blocks non-linearities are needed.

- Quantization noise

As most of the $\Sigma\Delta$ modulators [27][31], the signal-to-quantization noise ratio (SQNR) is normally over designed to ensure that quantization noise only contributes a small portion of the noise budget. By employing a fixed OSR=40 and the equation (3.4), $4^{th}$-order architecture with 2-bit quantizer and DACs will give us 75dB SQNR, which is very close to our target and will make the other specifications of noise budget too difficult to be realized. As a result, the $6^{th}$-order architecture with 2-bit quantizer and DACs is chosen and the theoretical peak SQNR will be less than 80dB.

- Jitter noise

Clock jitter effects are significant due to the usage of the high clock frequency. To reduce the jitter noise contribution, non-return-to-zero (NRZ) DACs are employed. In this design, an off-chip clock is used; hence the clock jitter is fundamentally limited by

the performance of the external clock generator. By employing fs/4 architecture with NRZ DAC, the signal-to-jitter noise ratio can be estimated as [34]

$$SNR_{jitter} = 10log_{10}\left[\frac{2*OSR}{(\sigma_t\pi f_s)^2}\right],$$ (4.1)

where $\sigma_t$ is the standard deviation of the jittered clock. For $\sigma_t = 0.4ps$, the achievable SNR$_{jitter}$ is around 79 dB.

- Thermal noise

Basically, every circuit will contribute with thermal noise to the output of the modulator. However, since it is used in close loop with large in-band gain, only the thermal noise from input stage is critical. To achieve the specifications, the signal-to-thermal noise-ratio has to be on the order of 80dB. Hence, the input referred noise of the system has to be less than 8nV/Hz$^{1/2}$ when 10MHz bandwidth is considered and the full scale range is 250mV. The required input referred noise of the filter is assigned as 7nV/Hz$^{1/2}$ while DAC output thermal noise is limited to 4nV/Hz$^{1/2}$ in order to achieve modulator's SNDR=74dB.

- Distortion

After considering the noise contributions due to quantization, jittered clock, and thermal noise, the signal-to-distortion ratio (SDR) would be in the range of 76dB. The noise budget is presented in Table 4.2 based on the requirements of the resolution and the feasibility of the circuit performance. The linearity requirement for the first filter section would be in the range of 77dB; the 2-bit DAC has to be in the same order of magnitude.

Table 4.2 Noise budget for different noise source

| Parameter | Signal-to-the noise-ratio |
|---|---|
| Quantization noise | < 80dB |
| Jitter noise | 79dB |
| Thermal noise | 80dB |
| Non-linear distortion | 77dB |
| Total noise+distortion | ~74dB |

4.2.2   Transfer function analysis

Since 6th-order 2-bit architecture has been selected, the open loop transfer function from the DACs to the quantizer can be determined to achieve the required NTF. First, the equivalent lowpass 3rd-order Z-domain NTF is attained and used to develop the required 6th-order bandapss NTF through the conversion from z[-1] to –z[-2] (for the Fs/4 architecture of the modulator only),

$$NTF_{lowpass} = (1 - z^{-1})^3 \xrightarrow{z^{-1} \to -z^{-2}} NTF_{bandpass} = (1 + z^{-2})^3 \qquad (4.2)$$

The open loop transfer function (TF(z)) of the system is thus obtained from (4.2) and the definition of the NTF as follows.

$$NTF_{bandpass} = (1 + z^{-2})^3 = \frac{1}{1+TF(z)} \Rightarrow TF(z) = \frac{-3z^4 - 3z^{-2} - 1}{z^6 + 3z^4 + 3z^2 + 1} \tag{4.3}$$

However, due to the required 10MHz bandwidth, a pole-splitting technique, as shown in Fig. 4.1, is adopted to ensure the flat passband instead of locating all the poles at same frequency.
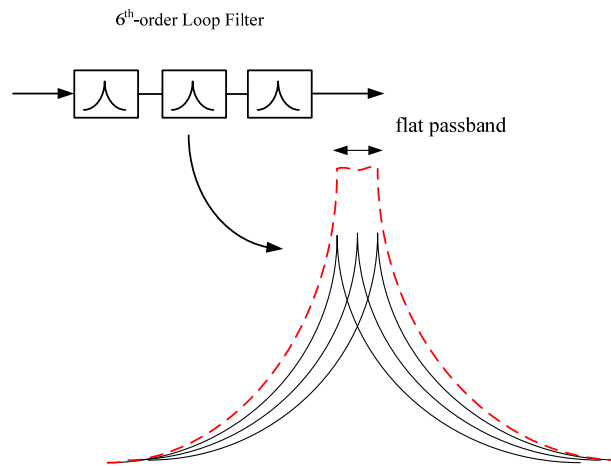


Fig. 4.1. Pole-splitting technique.

Based on the consideration of the loop stability, pole arrangements as quasi-linear phase inverse Chebyshev bandpass transfer function is employed. In this design, the pole locations are arranged at 195MHz, 200MHz, and 205MHz respectively by using the command "cheby2" with the required order (3) and bandwidth (192MHz & 208MHz for stopband frequencies) in Matlab and hence the TF(z) in (4.3) are modified as

$$TF(z) = \frac{-2.994z^4 - 2.994z^2 - 1}{z^6 + 2.994z^4 + 2.994z^2 + 1} \tag{4.4}$$

where the quality factors of poles in this step are assumed as infinite. To account for the quantizer delay and the processing delay from digital circuitries, a sampling period delay margin (a $z^{-1}$ term) is taken out from (4.4) to maintain the stability of the loop.

$$TF(z) = z^{-1}[TF'(z)] \tag{4.5}$$

$$TF'(z) = \frac{-2.994z^5 - 2.994z^3 - z}{z^6 + 2.994z^4 + 2.994z^2 + 1} \tag{4.6}$$

TF'(z) is converted into a continuous time transfer function using the impulse invariant z to s transformation since the modulator only converts the data at the sampling instants. (4.7) shows the general equation of the impulse invariant transformation [10].

$$\frac{y_o}{z - z_k} \xrightarrow{impulse\ invariant} \frac{s_k}{s - s_k} \cdot \frac{y_o}{z_k^{1-\alpha} - z_k^{1-\beta}} \tag{4.7}$$

In (4.7), α and β are the timing of the rising edge and falling edge of the DAC pulse in one normalized sampling period ($0 \leq \alpha < \beta \leq 1$). For example, α is equal to 0 and β is equal to 1 in the NRZ pulse while α is equal to 0 and β is equal to 0.5 in the RZ pulse. $s_k$ in (4.7) is the transferred pole location which can be obtained as

$$z_k = e^{s_k T_s} \Rightarrow s_k = \frac{\ln z_k}{T_s} \tag{4.8}$$

The s-domain open loop transfer function TF'(s) is thus obtained as

$$TF'(s) = \frac{1.4*10^9 s^5 + 2.6*10^{18}s^4 + 6*10^{27}s^3 + 6.7*10^{36}s^2 + 5.3*10^{45}s + 3.4*10^{54}}{s^6 + 1.9*10^8 s^5 + 4.8*10^{18}s^4 + 6*10^{26}s^3 + 7.5*10^{36}s^2 + 4.7*10^{44}s + 3.9*10^{54}}$$

$$\tag{4.9}$$

by splitting TF'(z) into six 1$^{st}$-order functions using the Matlab command "residue" and employing the transformation in (4.7). Fig. 4.2 shows the frequency spectrum of the NTF = 1/(1+TF'(s)) in s-domain. There is a 60dB noise-shaping in the band of interest.
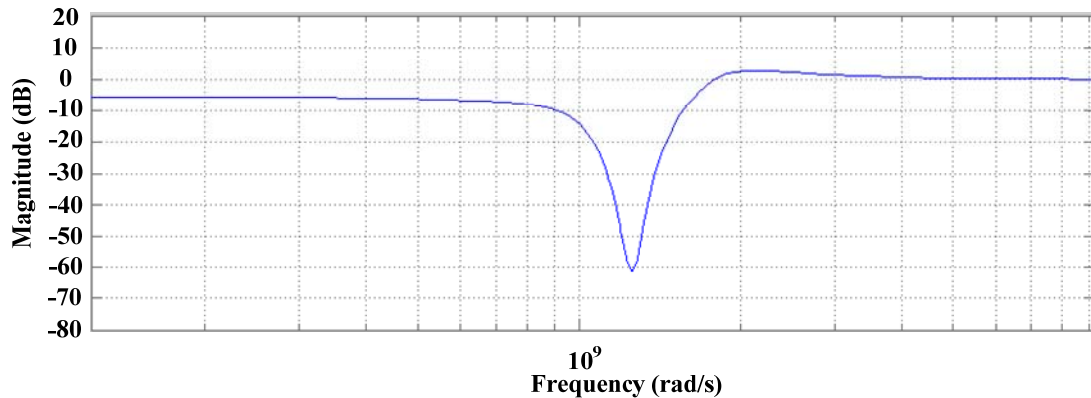


Fig. 4.2. The frequency spectrum of the NTF.

### 4.2.3 Proposed architecture

Clocked at 800MHz, the 6$^{th}$-order 2-bit architecture shown in Fig. 4.3 was developed to provide significant rejection of the blockers as well as enough noise shaping in the frequency range of interest. Since the unequal rise/fall time of DAC pulses would generate the distortions at the output of the DACs and degrade system performance due to the feedback charge difference between DAC feedback current when DAC control signal is 1 and that when DAC control signal is 0 [35], the modulator is implemented differentially to compensate the effect.
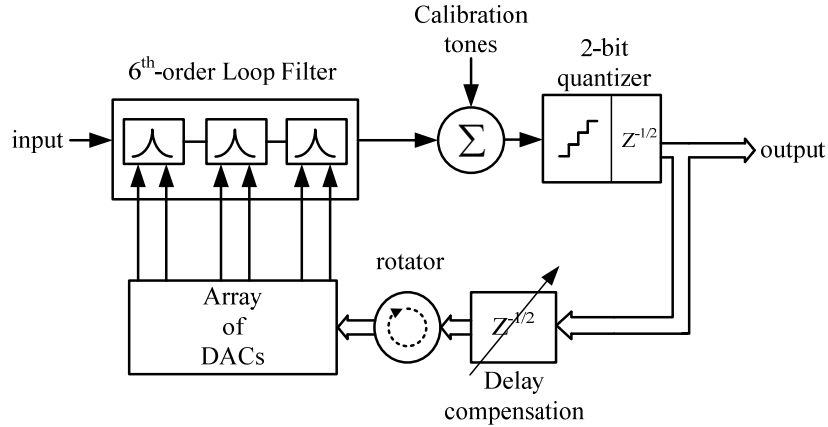
Fig. 4.3. Block diagram of the 6$^{th}$-order modulator architecture.

The topology consists of the cascade of three resonators with feedback (CRFB) from 6 NRZ 2-bit DACs that inject the feedback signal into the loop filter. As described in previous section, the loop filter is implemented using a quasi-linear phase 6$^{th}$-order inverse Chebyshev bandpass filter and composed by three cascaded second-order bandpass filters where the center frequencies are set to 200MHz, 205MHz, and 195MHz, respectively, to ensure the required flat in-band gain at the desired frequency range. The adder block before quantizer is used to couple the filter's output and the multi-bit quantizer, as well as to inject the test tones required for architecture calibration. A two-bit quantizer samples the filter output and digitizes it with a half cycle clock delay. A programmable delay element compensates the whole loop delay into one sampling period to maintain system stability and to compensate the delay mismatches among digital blocks. The rotator pseudo-randomizes the mismatch between current branches of each current-steering DAC and then converts the static error into random noise. All the ADC parameters such as DAC currents and passband gain and pole quality factor of

each filter stage are obtained by matching the open-loop transfer function of the continuous-time modulator with equation (4.9).

## 4.2.4 System simulations

In this dissertation, Matlab and Simulink are the main tools to check the system performance and the affects of the all the non-idealities. By setting the fixed-step type and ode5 solver option in configuration parameters to achieve better simulation accuracy, the Simulink model of the proposed architecture is depicted in Fig. 4.4, where the non-ideal issues such as input referred noise and non-linearities of filters, current mismatch in DACs, jitter noise [36], excess loop delay, limited rising and falling time of the sampling clock, and the cut-off effect of power supply are all modeled. The detail is depicted in the section 4.8.

With 400000-point simulation in Simulink, Fig. 4.5 shows the output frequency spectrum of the modulator in Simulink. The peak SNR is 75dB when signal is 0dBr, where the reference voltage is 0.25V.

Fig. 4.4. The Simulink model of the proposed modulator with all non-idealities.
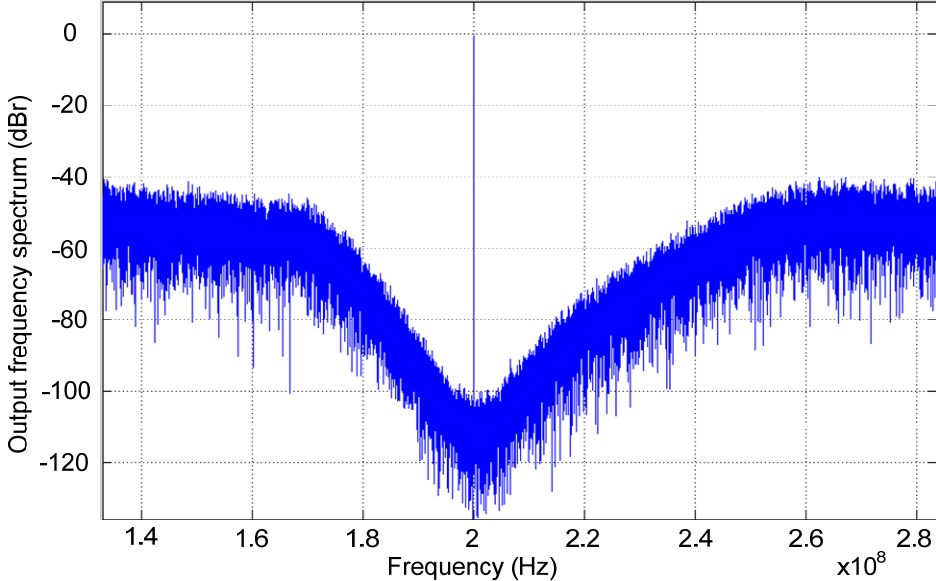
Fig. 4.5. The output spectrum of the proposed architecture in Simulink.

4.3 Circuit Implementation of critical blocks

4.3.1    Loop filter

   The modulator's resolution demands the passband gain and quality factor (Q) of each biquadratic stage to be 20dB and 20, respectively. To achieve the modulator's dynamic range specifications, the biquadratic specifications are set at IM3 < -77dB at $v_{in}$=200mV$_{RMS}$ and input referred noise density under 7nV/Hz$^{1/2}$. Additionally, the filter topology must be able to combine the filter's input and DAC output current; hence large filter's signal swing is expected. To satisfy all these requirements, the active-RC two-integrator-loop filter topology is employed, as depicted in Fig. 4.6.
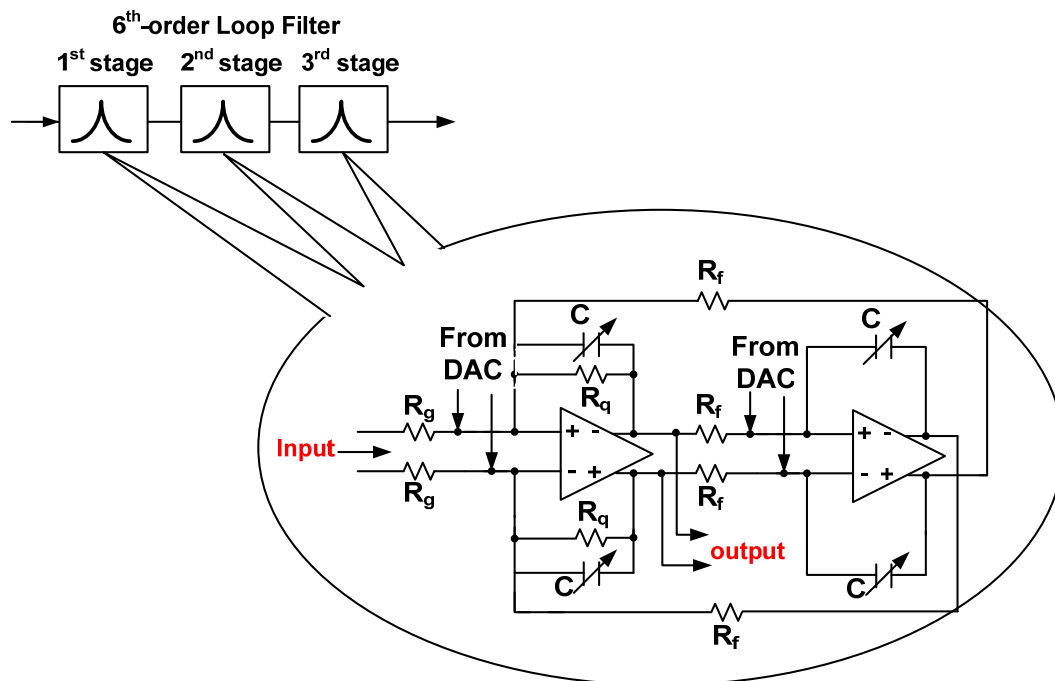


Fig. 4.6. Active-RC type loop filter schematic.

As equation (4.10), the transfer function of the filter demands not only the passive components but also the gain of the amplifier at 200MHz.

$$\frac{V_{out}}{V_{in}} = \frac{\frac{\left(1+\frac{1}{A}\right)}{\left(1+\frac{2}{A}\right)}s\left(\frac{1}{R_gC}\right)+\frac{\frac{1}{A}\left(\frac{1}{C^2R_fR_g}\right)}{1+\frac{2}{A}}}{s^2+s\frac{\frac{1}{CR_q}+\frac{1}{A}\left(\frac{2}{CR_q}+\frac{1}{CR_g}+\frac{1}{CR_f}\right)}{\left(1+\frac{2}{A}\right)}+\frac{\frac{1}{C^2R_f^2}+\frac{1}{A}\left(\frac{1}{C^2R_fR_q}\right)}{\left(1+\frac{2}{A}\right)}} \tag{4.10}$$

Therefore, the required filter's linearity and frequency response (20dB passband gain and Q=20) demand 35dB gain in the amplifier's open-loop gain at 200MHz; for a typical single-pole operational amplifier this means a Gain-BandWidth (GBW) product over 10 GHz. Parasitic poles must be above this frequency to provide a phase margin better than 45 degrees. The gain requirements cannot be achieved using a single stage amplifier because the amplifiers are resistively loaded; hence efficient multi-stage amplifiers are required for this application. In order to make the solution exportable to deep-submicron technologies, the usage of cascode stages is avoided; instead, a multi-stage architecture with feed-forward compensation is adopted [37]. Fig. 4.7 shows the single-ended amplifier's architecture that consists of 3 gain stages to provide a DC gain of 59dB and an additional feed-forward stage to compensate its phase response.
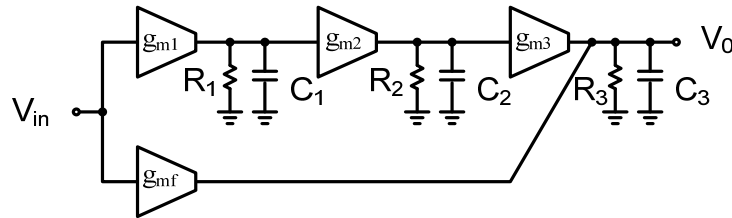


Fig. 4.7. Block diagram of amplifier with feed-forward.

With the feed-forward path, the transfer function of the amplifier can be obtained as

$$\frac{V_0}{V_{in}} = \frac{A_{v1}A_{v2}\left(\frac{gm_3}{C_3}\right)}{(s+w_{o1})(s+w_{o2})(s+w_{o3})} + \frac{\frac{gm_f}{C}}{s+w_{o3}} = \frac{A_{v1}A_{v2}\left(\frac{gm_3}{C_3}\right)+(s+w_{o1})(s+w_{o2})\frac{gm_f}{C}}{(s+w_{o1})(s+w_{o2})(s+w_{o3})} \qquad (4.11)$$

where $A_{v1}= gm_1/C_1$ and $A_{v2}= gm_2/C_2$ are the DC gain of the first and second stage. $w_{o1}=1/(R_1C_1)$, $w_{o2}=1/(R_2C_2)$, and $w_{o3}=1/(R_3C_3)$ are the frequency of poles lumped to the output of the $1^{st}$, $2^{nd}$, and $3^{rd}$ stages, respectively. Parameters $g_{m3}$ and $g_{mF}$ are the transconductance gain of the 3rd stage and feed-forward stage, respectively. Therefore, the feed-forward path generates 2 left-hand-side complex zeros located at

$$\omega_{Z1,2} = -\left(\frac{\omega_{01}+\omega_{02}}{2}\right)\left(1\pm j\sqrt{\left(\frac{A_{V1}A_{V2}g_{m3}}{g_{mF}}\right)\left(\frac{\omega_{01}/\omega_{02}}{(1+\omega_{01}/\omega_{02})^2}\right)}\right) \qquad . \qquad (4.12)$$

By determining the appropriate $gm_F$, these two zeros will appear around the unity gain bandwidth, leading to an improvement of amplifier's phase margin. Due to the relaxed settling time requirements for continuous-time $\Sigma\Delta$ modulators, these high frequency zeros can usually be tolerated [28][34]. Fig. 4.8 shows the comparison of Cadence simulation results: the un-compensated amplifier provides an overall DC gain of 70dB and a voltage gain of 54dB at 200MHz but -80 degree phase margin at unity gain frequency when loaded by a capacitor of 1pF capacitor. With feed-forward compensation, the phase margin exceeds 55 degrees. Table 4.3 summarizes the amplifier's frequency compensation results. In this design, the gain of the first stage and second stage are maximized since the gain of the last stage is sacrificed to ensure enough phase margin by using a feedforward path.
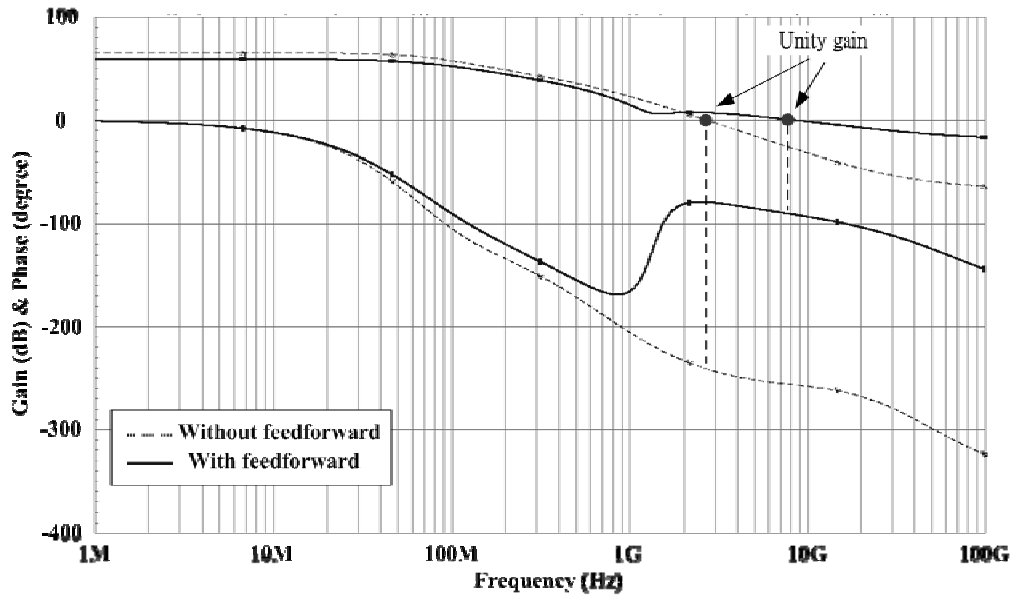
Fig. 4.8. Frequency response for the proposed amplifier.

Table 4.3 Amplifier poles, zeros and gain

|  | **Without feedforward** | **With feedforward** |
|---|---|---|
| **1st stage** | Adc=27dB<br><br>fpole=367.6MHz | Adc=27dB<br><br>fpole=367.6MHz |
| **2nd stage** | Adc=25dB<br><br>fpole=73.8MHz | Adc=25dB<br><br>fpole=73.8MHz |
| **3rd stage** | Adc=17.9dB<br><br>fpole=93MHz | Adc=7dB<br><br>fpole=287MHz |
| **overall** | Adc=70dB<br><br>A@200MHz=54dB | Adc=59dB<br><br>A@200MHz=46dB |
|  | $f_u$=2.51GHz<br><br>phase margin= -80$^o$ | $f_u$=6.26GHz<br><br>phase margin = 55$^o$ |

Determining the value of resistors and capacitors in the loop filter to match the gain and Q requirements is a straightforward step after having an OPAMP with high gain at 200MHz. Filter's thermal noise of the input stage will not be noise-shaped and may dominate the modulator's resolution. The input referred noise of the first biquadratic filter can be obtained as

$$\overline{v_{n,total}}^2 = 4kTR_g\,(1+\frac{1}{A_{vpeak}^2}(1+\frac{1}{Q}(1+(\frac{w}{w_o})^2)))+\frac{v_{n,amplifier}^2}{A_{vpeak}^2}(1+(\frac{R_g}{R_f})^2)$$
$$+i_{n,DAC}^2\cdot R_g^2(1+(\frac{w_o}{w})^2)$$

(4.13)

where $A_{Vpk}$ is the peak gain of the filter transfer function, and $\omega_0$ and Q are the filter's center frequency and poles quality factor, respectively. $v_{n,amplifier}$ and $i_{n,DAC}$ are the output referred noise of amplifiers and output referred current noise of DACs, respectively. From (4.13), it is evident that the proper selection of $R_g$ is critical to achieve the required noise performance. Other passive component values are computed from $R_g$ and the specifications of the filter, such as Q value and $\omega_0$. To optimize for noise, the resistance values must be scaled down; the evident trade-offs are higher power consumption and more demanding amplifier's requirements. Passive filter's components used in the modulator are given in Table 4.4. The total over input referred noise is $6.9nV/\sqrt{Hz}$ where the noise contributions from the passive components, amplifiers and DACs are $4nV/\sqrt{Hz}$, $1.6nV/\sqrt{Hz}$, and $1.3nV/\sqrt{Hz}$, respectively.

Table 4.4 Detail values of components in the first filter

| Component | Value |
|:---:|:---:|
| Rg | 1k ohm |
| Rq | 10.92k ohm |
| Rf | 940 ohm |
| C | 840 fF |

Since modulator's linearity is a strong function of the first filter stage, a very linear loop filter is required. By employing a fully differential architecture, the even order harmonic components are ideally cancelled out, leaving the third order distortion as the most critical one. As demonstrated in section 4.7 and the related paper, [38], the third-order inter-modulation distortion (IM3) of the closed-loop amplifier is proportional to the IM3 of the open-loop amplifier and inversely proportional to $(1+A_{V1}A_{V2}A_{V3})^3$, where $A_{V3}$ is the gain of the last stage including the feedback factor.

The signal strength monotonically increases when traveling through the 3 amplification stages, making the third stage of the amplifier the critical one for signal linearity. With the assumption of the first and second stages with gain $A_{V1}$ and $A_{V2}$, respectively, present enough linearity, the overall non-linear amplifier's output current can then be represented as

$$i_{out} = g_{m3}(A_{V1}A_{V2}V_{in}) + \frac{1}{8}\frac{g_{m3}}{V_{dsat3}^2}(A_{V1}A_{V2}V_{in})^3 = Gm_1 V_{in} + Gm_3 V_{in}^3 \quad (4.14)$$

where $gm_3$, $v_{dsat3}$, $Gm_1$ and $Gm_3$ are the small signal transconductance, overdrive voltage of the amplifier's $3^{rd}$ stage, the equivalent overall first and third non-linear terms respectively. It can be noticed that Amplifier non-linearity drastically increases with $A_{V1}A_{V2}$ and, therefore, the truth is that the filter's linearity is not significantly improved by increasing $A_{V1}A_{V2}$. Cadence results show us a filter's IM3 in the range of -60dB even if the amplifier's gain at 200MHz is in the order of 40 dB. To overcome this issue, the amplifier is further linearized to achieve the required filter's IM3.

The non-linear lossless integrator can be represented as depicted in Fig. 4.9. Since the amplifier gain stages are frequency dependent terms, Volterra series can be used for the linearity analysis of the basic integrator.
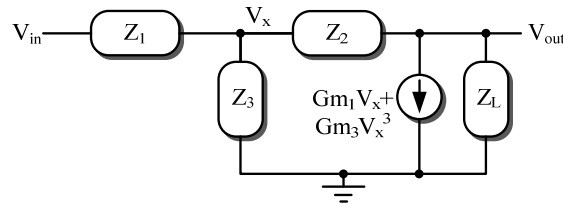


Fig. 4.9. Macromodel for the lossless integrator.

To get more insight on the linearity limitations of the system, the approach suggested in [38] is used here instead of the more complex Volterra series analysis. Assuming that the output voltage can be expressed as

$$V_{out} = b_1 V_{in} + b_3 V_{in}^3 \tag{4.15}$$

where $b_1$ is the fundamental gain of the integrator and $b_3$ is the third order gain. The non-linear equivalent circuit is analyzed in section 4.7, leading to the following expressions for the output voltage coefficients

$$b_1 = \frac{Y_1(Y_2 - Gm_1)}{(Y_2 + Y_L)(Y_1 + Y_2 + Y_3) + Y_2(Gm_1 - Y_2)} \tag{4.16}$$

$$b_3 = \frac{Gm_3 Y_1{}^3 (Y_2 + Y_L)^3 (Y_1 + Y_2 + Y_3)}{\left((Y_2 + Y_L)(Y_1 + Y_2 + Y_3) + Y_2(Gm_1 - Y_2)\right)^4} \tag{4.17}$$

The second order harmonic coefficients are not considered since fully differential architectures are utilized. The third intermodulation distortion IM3 can be obtained from (4.15), (4.16), and (4.17) as

$$IM3 \cong \frac{3}{4} \left| \frac{\left(\frac{Gm_3}{Gm_1 - Y_2}\right)\left(\frac{Y_1}{Y_1 + Y_2 + Y_3}\right)^2}{\left(1 + \left(\frac{Gm_1 - Y_2}{Y_1 + Y_2 + Y_3}\right)\left(\frac{Y_2}{Y_2 + Y_L}\right)\right)^3} \right| (v_{in})^2 = \frac{3}{4} \left| \frac{\left(\frac{Gm_3}{Gm_1 - \frac{1}{Z_2}}\right)\left(\frac{1}{1 + \frac{Z_1}{Z_2} + \frac{Z_1}{Z_3}}\right)^2}{(1 + LG)^3} \right| (v_{in})^2, \tag{4.18}$$

where LG stands for loop gain by $LG = \left(\frac{Gm_1 - Y_2}{Y_1 + Y_2 + Y_3}\right)\left(\frac{Y_2}{Y_2 + Y_L}\right)$. In the case of the bandpass architecture, all parameters must be evaluated at 200MHz. As expected, to linearize the integrator, it is mandatory to increase LG as much as possible. Since $Z_1$, $Z_2$, $Z_3$ and $Z_L$ are determined by filter and noise specifications, the only parameter that can be optimized is $Gm_3/Gm_1$. Assuming that LG>>1 at the frequency range of interest, a simplified expression for IM3 is obtained

$$IM3 \cong \frac{3}{4} \left| \left(\frac{Gm_3}{(Gm_1 - Y_2)^4}\right)(Y_1 + Y_2 + Y_3)(Y_1)^2 \left(\frac{Y_2 + Y_L}{Y_2}\right)^3 \right| (v_{in})^2 \tag{4.19}$$

For the case of the 3-stage amplifier, according to (4.15), $Gm_1 = (A_{V1}A_{V2})gm_3$ and $Gm_3 = \frac{1}{8}\frac{(A_{V1}A_{V2})^3}{V_{dsat3}^2}gm_3$ leading to

$$IM3 \cong \frac{3}{32} \left| (1 + s(R_g \| R_3)C)(1 + sR_L C)^3 \right| \left| \left(\frac{\left(1 + \frac{R_g}{R_3}\right)}{(A_{V1}A_{V2})(gm_3 R_g)^3}\right) \right| \left(\frac{V_{in-pk}}{V_{dsat3}}\right)^2 \tag{4.20}$$

where s=jω is the frequency variable. Since the signal applied to the 3$^{\text{rd}}$ stage is the amplifier's input voltage amplified by $A_{V1}A_{V2}$, the integrator's IM3 is reduced by

$A_{V1}A_{V2}$ only and not by the cubic power of the entire loop gain suggested by the closed loop systems theory. Small IM3 values require large 3$^{rd}$ stage transconductance ($gm_3$) value as well as large overdriving voltage $V_{dsat3}$. Since the signal at the gate of M3 is large, to avoid the presence of hard non-linearities, the third stage may require light source degeneration to accommodate the large input power.

The noise and IM3 trade-off is evident from (4.13) and (4.20). While lower noise requires small $Rg_1$ values, better IM3 figures require large $Rg_1$. Typical values for IM3 with $V_{in-pk}=V_{dsat3}$ and $A_{V1}A_{V2}=40$dB are around -60dB but increase rapidly for larger input values. To obtain better IM3 figures at high frequencies without sacrificing the noise level, it is proposed to linearize the amplifier's 3$^{rd}$ stage. As demonstrated in [39], the differential pairs can be linearized by using an additional amplifier connected in anti-parallel with the third stage. Ignoring the source degeneration resistors in the cross-coupled differential pair, the amplifier's output current can be computed as

$$i_{out} \cong (gm_3 - gm_L)(A_1 A_2 V_{in}) + \frac{1}{8}\left(\frac{gm_3}{V_{dsat3}^2} - \frac{gm_L}{V_{dsatL}^2}\right)(A_1 A_2 V_{in})^3 \qquad (4.21)$$

The auxiliary circuit is designed such that its main transconductance $gm_L$ is smaller than $gm_3$, but its third harmonic distortion is designed to be similar to that of the main transistor such that the cross-coupling circuitry partially cancels the main device harmonic distortion. This approach suggests using a non-linear compensating circuit since $v_{dsatL}<v_{dsat3}$; unfortunately this approach is very sensitive to PVT variations. Light source degeneration circuitry in both transistors $M_3$ and $M_L$ extends amplifier's linear range and introduces an additional degree of freedom as shown in the following expression

$$i_{out} \cong \left(\frac{gm_3}{1+N_3} - \frac{gm_L}{1+N_L}\right)(A_1 A_2 V_{in}) + \frac{1}{8}\left(\frac{gm_3}{(1+N_3)^3 V_{dsat3}^2} - \frac{gm_L}{(1+N_L)^3 V_{dsatL}^2}\right)(A_1 A_2 V_{in})^3 \quad (4.22)$$

where $N_3$ and $N_L$ are the source degeneration factor of $M_3$ and $M_L$, respectively. The amplifier is therefore linearized based on (4.22) and the conditions that $\frac{gm_3}{1+N_3} \gg \frac{gm_L}{1+N_L}$ and

$\frac{gm_3}{(1+N_3)^3 V_{dsat3}^2} = \frac{gm_L}{(1+N_L)^3 V_{dsatL}^2}$. The circuit schematic of the proposed amplifier is depicted

in Fig. 4.10.
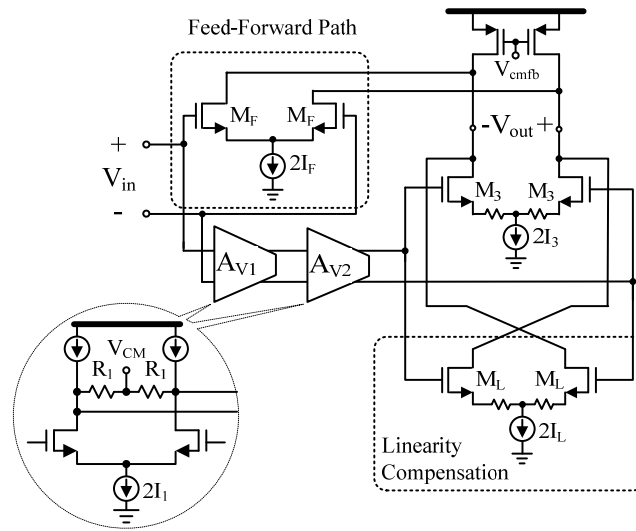


Fig. 4.10. Block diagram of amplifier with an dditional linearity aid.

With the exception of the last stage, every single stage is resistively terminated to fix the DC common mode level avoiding the use of several common-mode feedback circuits that increases both area and power consumption. Although these resistors (R1) limit the DC voltage gain, they increase the associated pole's frequency, which is more critical for the bandpass modulator. These resistors do not have a major effect on intermediate stages voltage gain at 200MHz. The DC level of the amplifier last stage is controlled

using a common-mode feedback; the common-mode error is fedback to the node $V_{cmfb}$ to regulate the output level at 0.9V. Cadence results depicted in Fig. 4.11 show that selecting $M_L$ with an overall transconductance gain four times smaller than $gm_3$, IM3 is around -63dB at the desired output swing if the stand-alone source degeneration technique is used. IM3 figures improve over 15 dB for input signals up to -17 dBVpk (two tone input signal with differential amplitude of 400mVpk-pk) if the additional linearization technique is used. A comparison chart of IM3 performance between un-linearized and linearized filters is shown in Fig. 4.12. There is a 17.23dB improvement on IM3 performance when output signal is -20dBVpk or below. The reason that improvement degrades to 8.87dB when output peak-to-peak signal is -11dBVpk is due to the change of gm3 in (4.21) and the un-perfect cancellation of third harmonic distortions. Corner simulations depicted in Fig. 4.13 show that IM3 is lower than -74dB with statistical process variation models for a two-tone differential input signal of 200 mVpk. The additional noise, power, and area added by the auxiliary circuitry increased amplifier's budget by .5%, 6% and 0.2%, respectively, but the improvement on amplifier's linearity is remarkable.
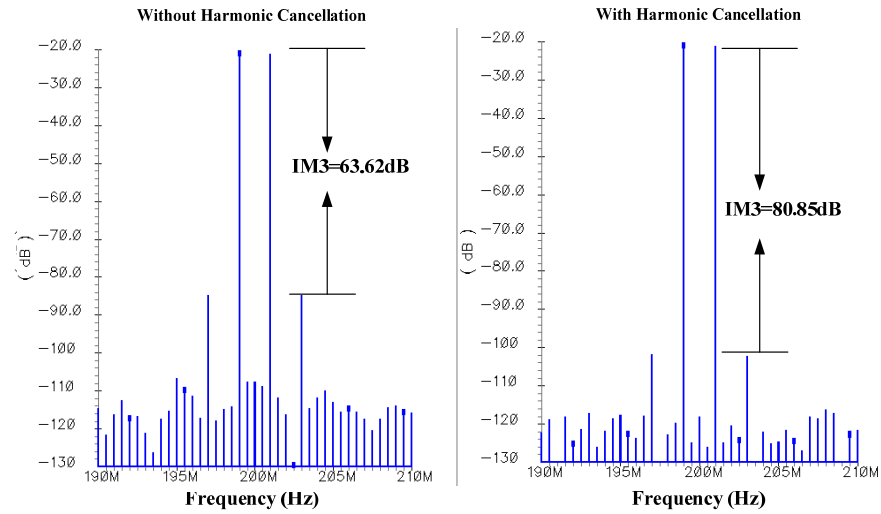
Fig. 4.11. IM3 performance of amplifier with and without linearity aid.
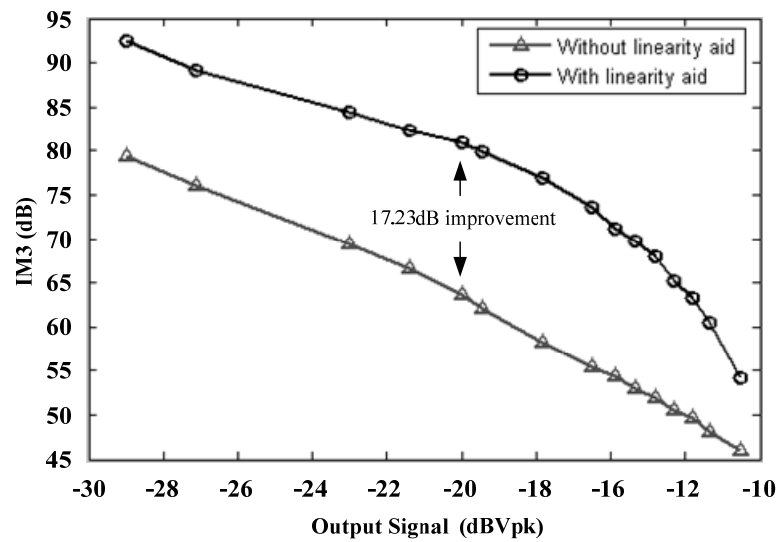


Fig. 4.12. IM3 performance of 2$^{nd}$ order filter in different output signal level.
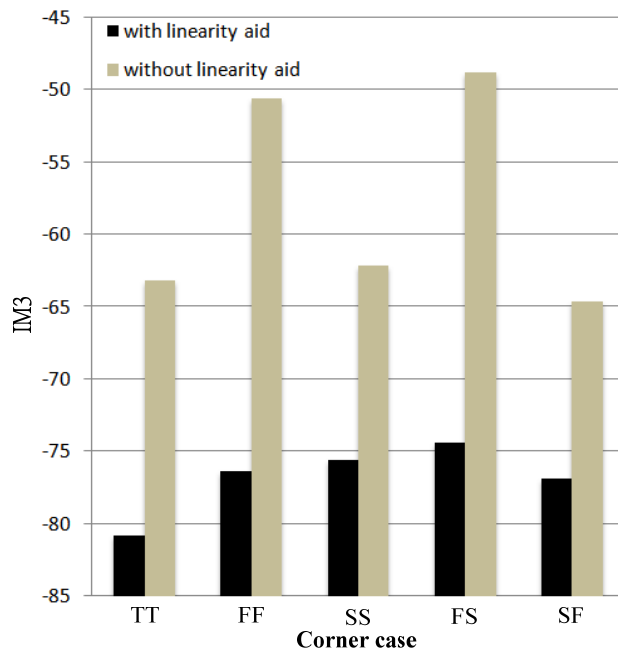
Fig. 4.13. Loop filter IM3 performance for different technology corners.

### 4.3.2 Summing amplifier and 2-bit flash quantizer

The summing amplifier and quantizer are depicted in Fig. 4.14. The function of the summing amplifier is mainly to increase the signal swing in order to fully-load the quantizer, and to support the injection of the two test tones to perform digital calibration for the modulator; this amplifier attenuates the digital glitches from the comparators that couple back to the filter. The source degeneration resistors R4 increase the amplifier input impedance. Large bandwidth is a necessity to minimize the significant excess loop delay contribution. A compromised R3 value is chosen to fit these two requirements. The final design of the summing amplifier yields a gain of 6dB, with 800MHz bandwidth and IM3 of -50dB. The 2-bit quantizer architecture is a conventional topology composed by 3 double differential pairs that compare the filter's output with 3 different voltage references coming from a reference ladder. The circuit schematic and

timing scheme are shown in Fig.4.14 where $\Phi_1$ is the amplification phase and $\Phi_2$ is the latching phase. It also employs an auto zeroing technique at the output of the first stage to compensate the differential DC offsets. Table 4.5 lists the detailed transistor sizes and component values of the circuit.

Table 4.5 Transistor devices and bias conditions for the sampling amplifier and 2-bit quantizer

| Device | Size | Device | Size |
|--------|------|--------|------|
| M1 | (2) 7.2u/180n | Cs1 | 750fF |
| M2 | (2) 6.0u/180n | Cs2 | 750fF |
| M3 | (4) 7.2u/180n | R2 | 500 ohms |
| M4 | (2) 1.8u/180n | R3 | 600 ohms |
| M5 | (8) 1.8u/180n | R4 | 325 ohms |
| M7 | (20) 3.6u/360n | Msw | (2) 1.8u/180n |
| M8 | (40) 3.6u/360n | Mbias | (30) 7.2u/360n |
| MbiasN | (30) 7.2u/360n | IbiasP | 3mA |
| SwitchN | (8) 4.5u/180n | Iblas | 700uA |
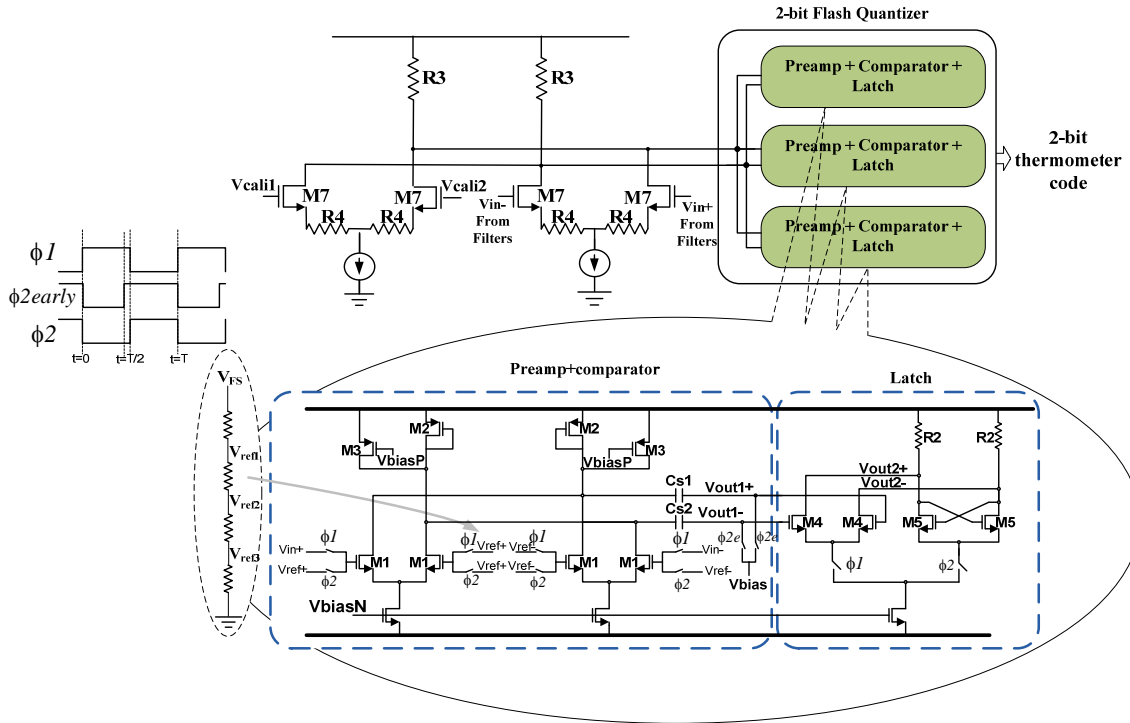
Fig. 4.14. Schematic of the summing amplifier with following comparators and latches.

### 4.3.3  $Z^{-1/2}$ delay compensator

As demonstrated in section 3.2.4, excess loop delay may change the closed loop pole locations of the modulator's transfer function and increase the order of the transfer function [40]. Fig 4.15 shows the SNR degradation in different level of excess loop delay in the modulator. In this plot, |excess loop delay| < 10% is a safe margin which has no serious SNR degradation.
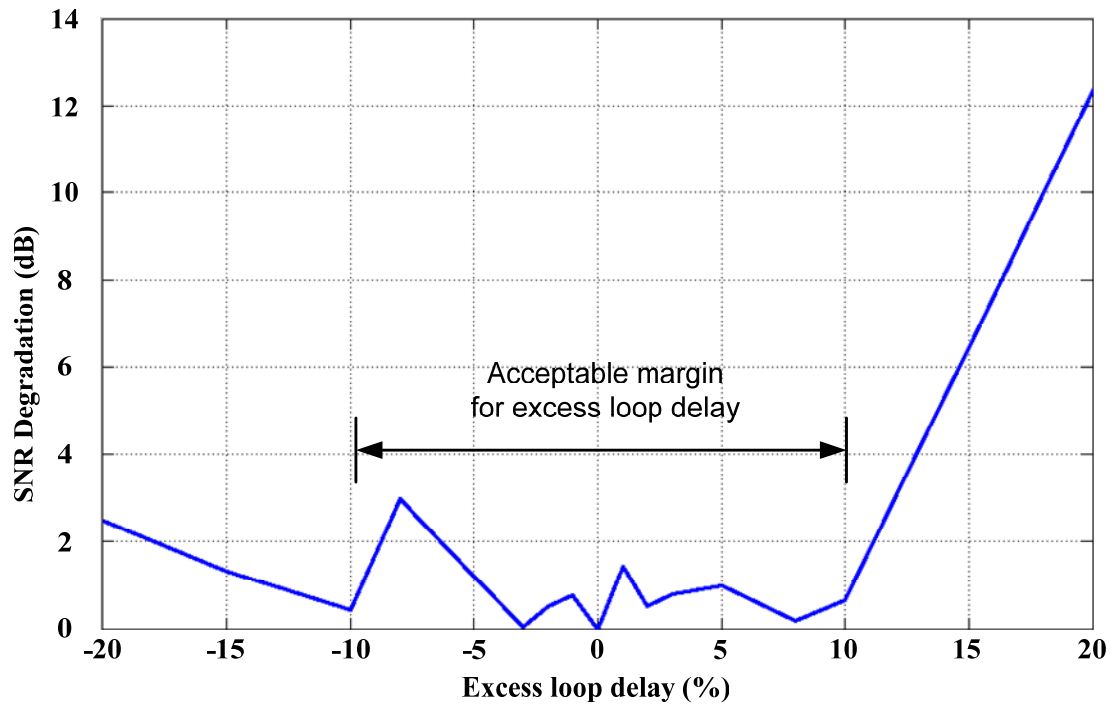
Fig. 4.15. SNR degradation in different level of excess loop delay.

However, excess loop delay is rather difficult to estimate, since it is subject to process and temperature variations. To prevent the modulator from these issues, a programmable delay block that is able to compensate for loop delay errors was added. As depicted in Fig. 4.16, the clock signal passes through a cascade of digital inverters to generate a 16 sequentially delayed clocks that are properly selected to ensure the variation of excess loop delay errors within 5% of the clock period. Using a 16-to-1 multiplexer with 4 control bits the delayed clocks is selected by the calibration controller. By utilizing this calibrated clock, the digital data is synchronized to drive the DAC within the required loop delay.
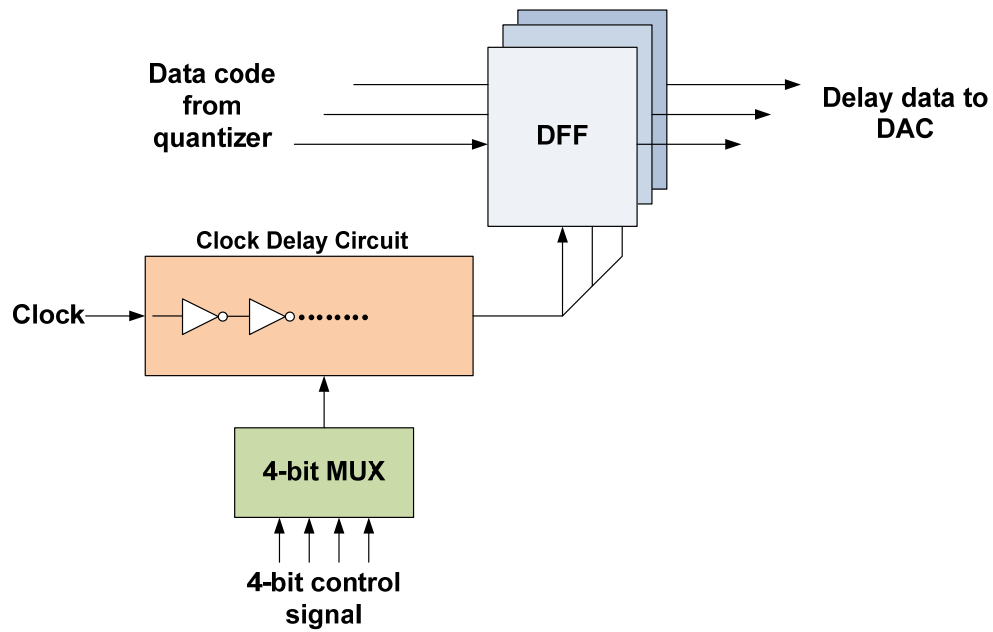
Fig. 4.16. The block diagram of the excess loop delay compensator.

### 4.3.4   2-bit DACs with rotator

Since the multi-bit DAC suffers from device mismatch due to PVT variations, it introduces non-linearities into the system. DAC non-linearities generate out-band noise folding into baseband as well as in-band harmonic distortion components that degrade modulator's SNDR. Simulation results show that the SNDR degradation due to different level mismatch between devices in the DAC is shown in Fig. 4.17.
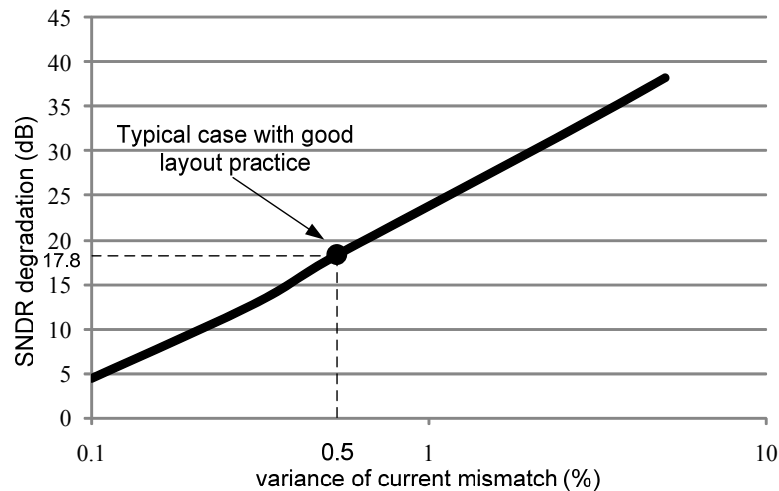
Fig. 4.17. SNDR degradation versus DAC current sources mismatch.

A DAC with 0.5% current source mismatch can be generally achieved when optimized layout techniques are employed. The modulator's SNDR may be degraded by up to 18dB in this case. To alleviate this issue, several solutions have been proposed; noise-shaping dynamic element matching loop (NSDEM) [14], or tree-structure DEM [15] to either randomize or shape the non-linearity. These methods, however, usually add significant loop delay that cannot be tolerated when using high frequency clock frequencies. The excess loop delay should be maintained under 0.05Ts seconds to ensure enough modulator resolution and loop stability [10]. To overcome the non-linearity from current mismatch with affordable processing delay, a data-weighted averaging (DWA) algorithm based on the technique reported in [16] is implemented as shown in Fig. 4.18. Fig. 4.18(b) presents an example of the rotator element selection pattern with five total current sources.
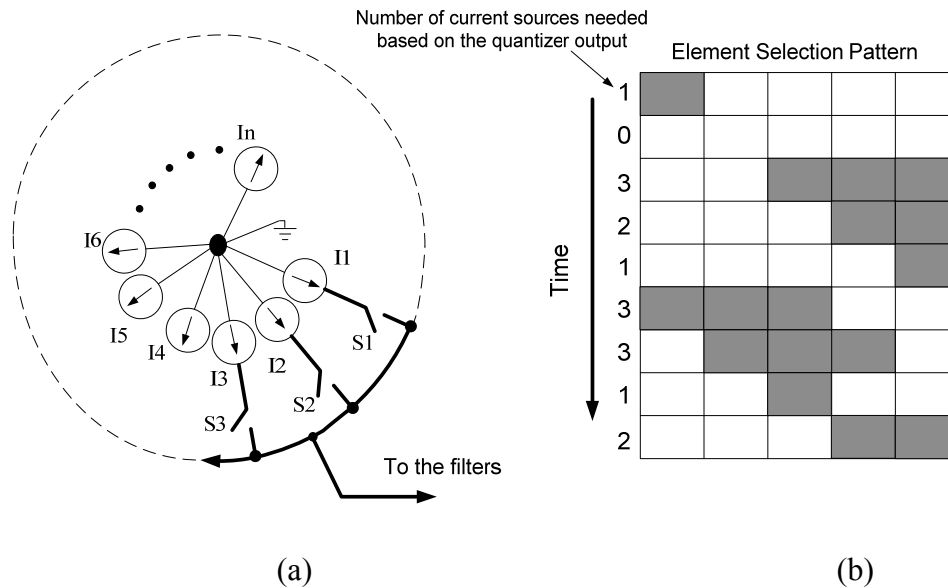
Fig. 4.18. Concept of data-weighted averaging using a 1-step clockwise rotator: a) the rotator architecture and b) the element selection pattern employing five current sources.

By employing additional current branches than needed in the regular DAC, the rotator circulates clockwise selecting 3 current sources in every clock period. Although this algorithm is not a true randomizer, it has been shown enough for achieving the required DAC linearity when common-centroid layout techniques to minimize systematic errors in the current sources are employed. In addition, longer length of transistors and cascode current sources are used to further enhance the matching of DAC current sources. Due to the remaining DAC non-linearity, part of the out-of-band noise is folded back into baseband, then raising the modulator noise floor by 4.7dB. The noise floor is reduced by 2.2dB and 4.2 dB by adopting the rotator with 3 out of 4 current branches and 3 out of 5 current sources, respectively. Additional power due to the extra branches of DAC and digital circuit control is also a trade-off when selecting the number of rotating current sources. To determine the optimal number of branches in the DAC,

the improvement on the traditional modulator's figure-of-merit can be estimated from the power/additional number of bits obtained with the rotator. The figure of merit is defined as $FoM = \dfrac{Power}{2^{ENOB} * (2 * BW)}$ where ENOB is the effective number of bits and BW is the modulator's bandwidth. We define the FoM improvement as follows

$$FoM_{improvement} = \frac{FoM_{rotator}}{FoM_{original}} = \frac{Power_{rotator}}{Power_{original}} * \frac{1}{2^{\frac{(SNDR_{rotator} - SNDR_{original})}{6.02}}} \quad , \qquad (4.23)$$

where the subscript "rotator" stands for modulator performance with the rotator activated, while "original" indicates the performance of the modulator without rotator. The architecture was extensively simulated and SNDR figures were obtained for both cases; equation (4.23) is plot in Fig. 4.19 assuming 0.5% device mismatches. Significant improvement is achieved with three out of five DAC branches. For this case, the modulator's SNDR improves over 12dB, while SQNR improves by 2 dB.
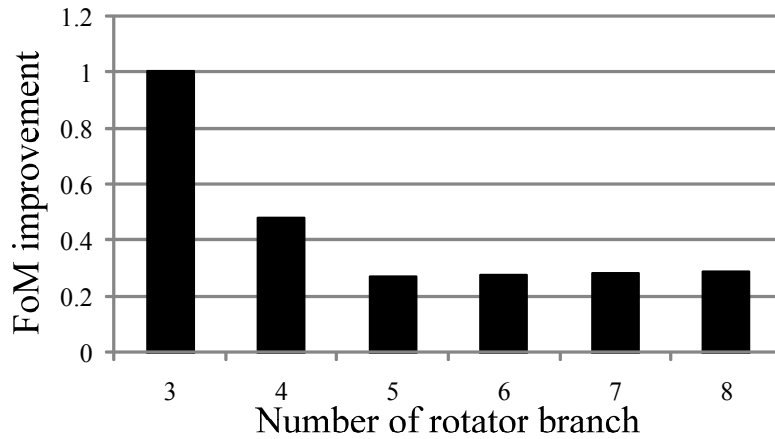


Fig. 4.19. FoM improvement under 0.5% current mismatch versus number of rotating branches.

4.4 Software-Based Calibration

One of the most critical drawbacks of continuous-time $\Sigma\Delta$ modulator is the lack of accuracy due to process, voltage and temperature (PVT) changes that may lead to over 25% variations on the system time constants. To alleviate this problem, the master-slave tuning techniques have been successfully used, however, it has to be accompanied by additional calibration schemes since tuning the loop filter is not enough to guarantee the best operation of the entire ADC loop [10], [41]-[43]. The optimally-tuned ADC requires corrections for the filter's center frequency deviations, excess loop delay and tolerances in DAC coefficients. These issues are partially alleviated by optimizing the architecture using double delay resonators and feedforward techniques[10]. Another approach measures in the digital domain the slope of the notch-shaped noise coming out of the ADC [41]. This approach is however affected by the power of the incoming out-of band information in on-line calibration schemes and it is difficult to optimize system performance. Optimization of individual building blocks and use of programmable delay lines for the calibration of the loop delay and reconfigurable filter-oscillator system for notch tuning were also reported in [43]. A recently reported calibration technique from us employs a tone at the desired ADC center frequency [44] to effectively measure the Noise Transfer Function (NTF) at the center frequency.

The goal of the proposed calibration approach is to minimize as much as possible the most critical modulator parameter –NTF- through the tuning of a number of loop parameters obtained from the system response when injecting two auxiliary and non-critical test tones at the input of the quantizer. The proposed calibration approach is depicted in Fig. 4.20 where two out-of-band calibration tones are injected at the input of

the quantizer to be the representative of the quantization noise. The software detects these two tones at the output of the modulator and tunes the system coefficients such as center frequencies of the filters, delay of the programmable delay block, and the current value of the DACs to recover the system performance from the variations.
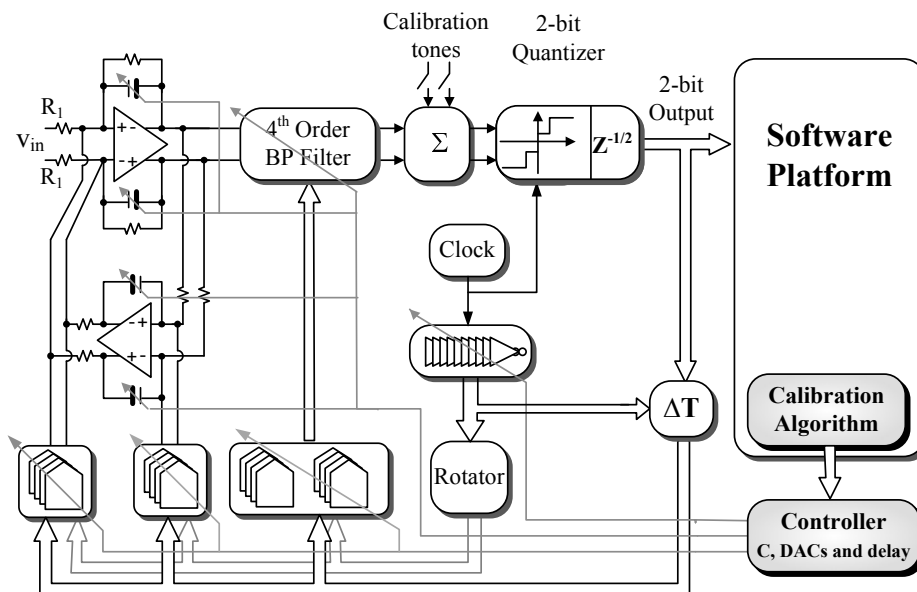


Fig. 4.20. Block diagram of the 6th order modulator architecture with the proposed software-based Calibration.

The frequencies of the test tones are selected to be out of the passband of the BP-sigma-delta modulator but close enough to the modulator's passband. Since the test tones are applied at the output of the loop, its noise is shaped by loop transfer function and the auxiliary circuitry has very little effect on the dynamics of the loop. During calibration, the spectrum of the modulator is measured by digital signal processor (DSP) and discrete-Fourier-transform (DFT), and the power of the tones emulating the quantization noise is evaluated. The calibration processing flow is plotted as Fig. 4.21.

First, the software detects the average power at the frequencies of test tones without injecting the test tones and compares that with the average power after injecting the test tones. If these two average powers are the same, the un-stability of the loop is detected and the software begins tuning the delay of the loop. The most sensitive coefficient of the system, through timing control in Fig. 4.20 is adjusted till the difference of the average powers appears. The center frequency tuning is the next calibration step once the stability condition is achieved.
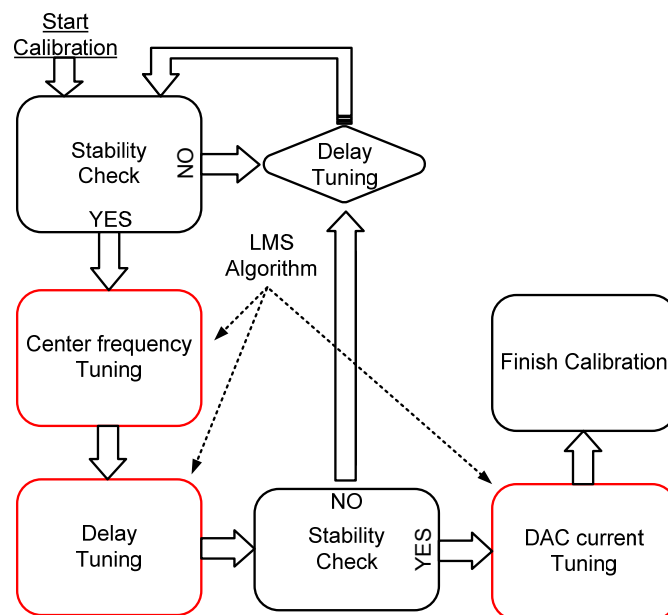


Fig. 4.21. The calibration flow chart.

An adaptive least mean square (LMS) algorithm, given in equation (4.24), adjusts sequentially the center frequencies of the loop filters with the aim of minimizing and equalizing the power of the testing tones.

$$|w(n+1) - w(n)| \leq quant[e(n)] \cdot K \qquad (4.24)$$

where w(n) is the center frequency of filters; e(n) is the power difference between two calibration tones and K a constant in $n^{th}$ iteration, respectively. "quant" presents that the discrete tunings are employed in this design. By detecting the average power of the test tones and comparing it repeatedly, the delay tuning after center frequency tuning intend minimizing the excess loop delay to optimize the NTF. Note, due to the system's high sensitivity to the excess loop delay, another stability check is employed after delay tuning. DAC current tuning is conducted in the same method with delay tuning and targets to the same goal: NTF optimization. Both delay tuning and DAC current tuning adopts the adaptive LMS algorithm as well to ensure the convergence of the calibration procedure.

Fig. 4.22 shows the process of the proposed calibration for the 200MHz BP-sigma-delta modulator. Two tones with 208MHz and 192MHz frequency are used. The initial center frequency of the loop is around 225MHz due to PVT variations. By detecting the difference of these two tones in digital domain at the output, the passband of the filter is tuned appropriately as shown in Fig. 4.22(b). Finally, the frequency calibration is completed. The two testing tones show comparable power level as shown in Fig. 4.22(c). Since the loop tuning approach relies on power estimation in software and on the well controlled frequency of the test tone, the algorithm is quite robust and ensures the optimization of NTF in the bandpass modulator.

(a)               (b)              (c)
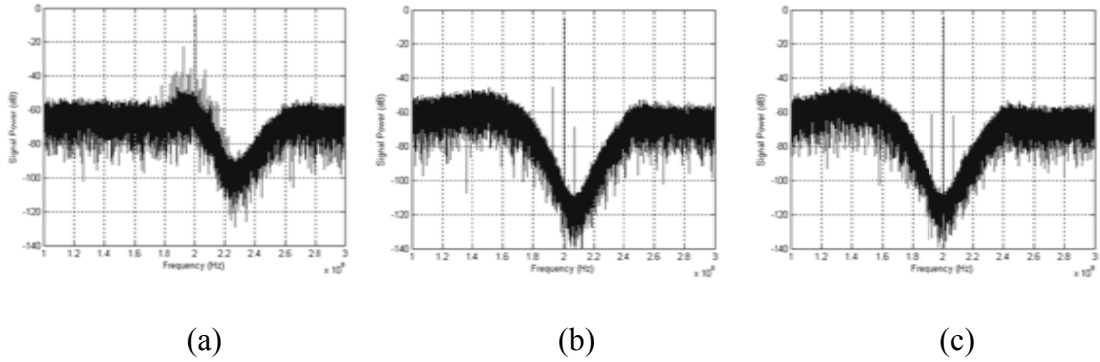
Fig. 4.22. The modulator calibration process
(a) uncalibrated modulator, (b) calibration after 6 iterations and (c) calibration after 20 iterations.

Fig. 4.23(a) shows how the power of the two test tones changes as the calibration takes place. At the same time, the power of the in-band quantization noise is reduced while the signal power remains unchanged.
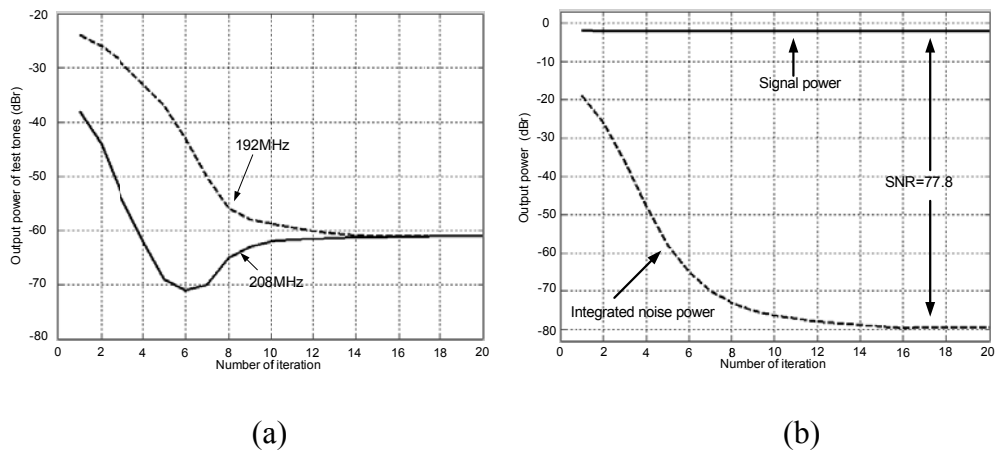


(a)                         (b)
Fig. 4.23. Power of the test tones and SNR simulations vs. the number of iterations of the calibration scheme for PVT variations on the modulator
(a) Power of test tones after calibration:-61dB
(b) Power of in-band noise after calibration:-79.8dB.

4.5 Experimental Results

The 6th-order bandpass $\Sigma\Delta$ modulator was fabricated in the TSMC 0.18μm 1P6M CMOS technology; Fig. 4.24 shows the chip microphotograph.
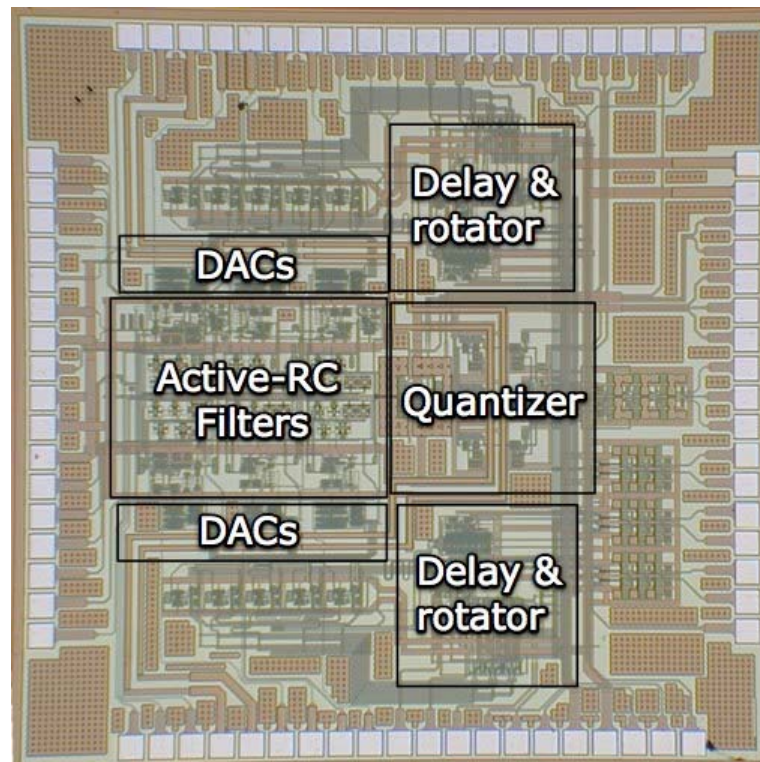


Fig. 4.24. Microphotograph of the chip.

The 200MHz bandpass $\Sigma\Delta$ modulator occupies an active area of 2.48mm$^2$ and the modulator was assembled into a QFN-80 package. The ADC's reference voltage is set to 0.25V. The total power consumption including clock buffers is 160mW; static power consumption is 126mW from a single supply voltage of 1.8V. Both differential input signal and sampling clock are generated by using off-chip signal generators. The 2-bit thermometer modulator output codes are captured by using an external oscilloscope

synchronized at 800Msample/sec and then post-processed using Matlab. Fig. 4.25 illustrates the test-bench of the modulator measurement. Signal generators are used to generate the required input signal, sampling clock, and two calibrations tones and an Oscilloscope is employed to catch the synchronized data from the output of the modulator. By transferring the data to the PC, the software of Matlab post-processes the data, displays the measurement results, and calibrates the system coefficients.
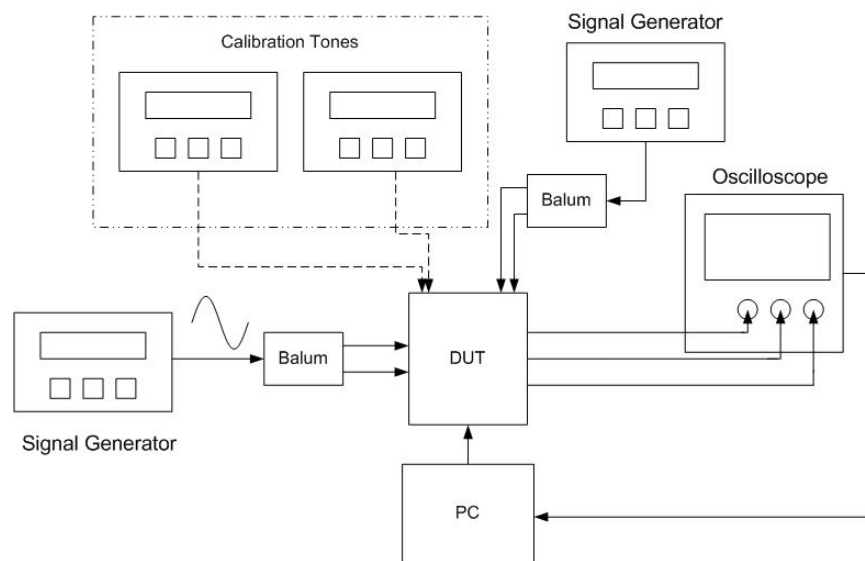


Fig. 4.25. The test-bench of the modulator measurement.

During modulator calibration, two extra signal tones at 220MHz and 180MHz are injected at the quantizer input. A 200 MHz tone was also injected at the modulator input. By detecting the power difference of these two tones at the output spectrum, the RC filter time constants are tuned based on the calibration algorithm; the experimental modulator tuning sequence is shown in Fig. 4.26.

The power of the calibration tones is measured; the power difference of the tones (Fig. 4.26a) indicates that the loop filter's center frequency must be increased, which is

done by reducing the value of the filter's integrating capacitors. The algorithm continues running until the power of the calibration tones are equalized; then it is assumed that the modulator center frequency is tuned. Due to the finite resolution of the bank of capacitors, there is a 2dB error in the power of the two test-tones after calibration, as depicted in Fig. 4.26d. Once the modulator center frequency is adjusted, the delay element and DAC coefficients are tuned until the power of the calibration tones is minimized; the entire process may take over 30 iterations.
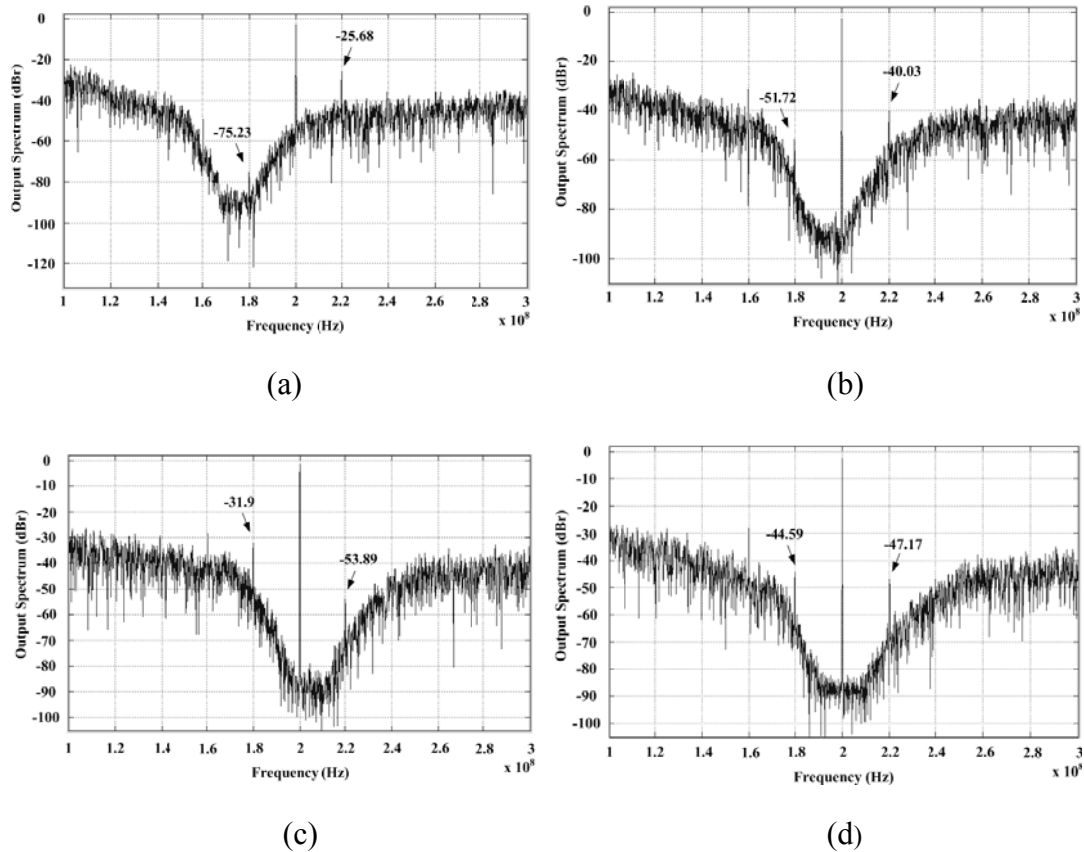


Fig. 4.26. Measured calibration process
(a) initial condition (b) calibration after 3 iterations (c) calibration after 6 iterations and (d) final calibration after 20 iterations.

Since most of the generator noise is located around the oscillating frequency and to minimize its noise contribution during modulator characterization, the modulator noise floor was measured employing a single out-of-band tone at 160 MHz as shown in Fig. 4.27. The measured RMS noise floor is around -100 dBr while noise resolution bandwidth is 20KHz. It results in over 70dB peak SNR when measured in 10MHz bandwidth. The third-order intermodulation distortion of the modulator is measured employing a two-tone test signal; the tones are 1.56MHz apart from each other. As depicted in Fig. 4.28. The power of each input tone is -8dBr (measured with respect to the reference voltage of 250mV) and the measured third-order intermodulation distortion is -73.5dB.
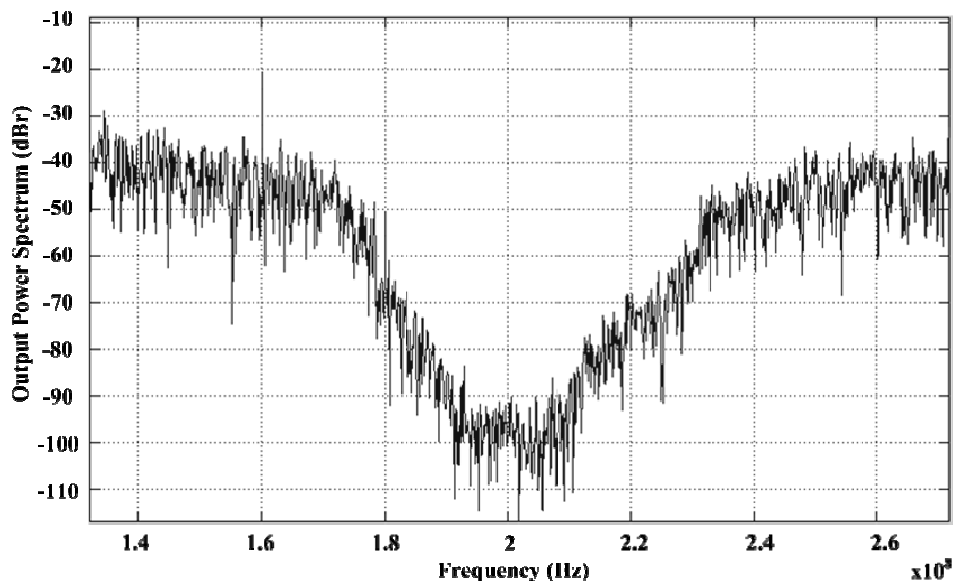
Fig. 4.27. Measured output spectrum with out-of-band input signal.
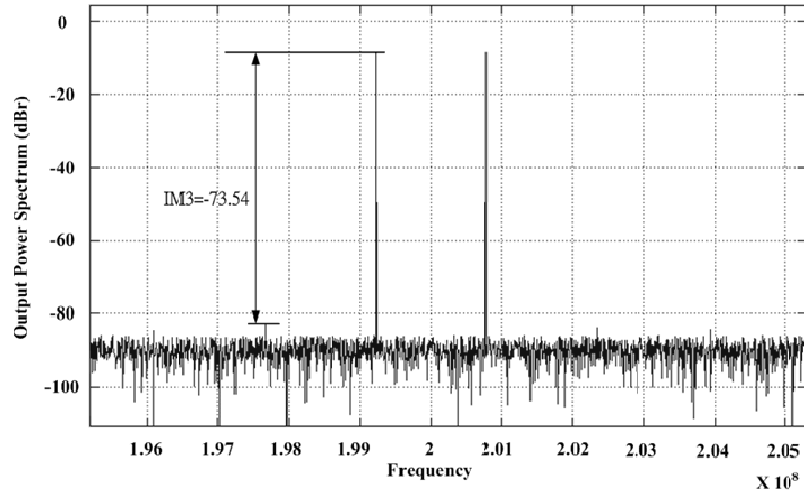
Fig. 4.28. Measured output spectrum in two-tone test.

As a result, the peak SNDR is 68.4dB in a bandwidth of 10MHz based on the measured SNR and IM3 at -2dBr overall output power. The SNDR behavior with different input signal levels is illustrated in Fig. 4.29, which shows about 70dB dynamic range. Table 4.6 summarizes the modulator's measured results. Peak SNDR measured in a bandwidth of 10MHz and 20MHz are 68.4 dB and 62.7 dB, respectively.
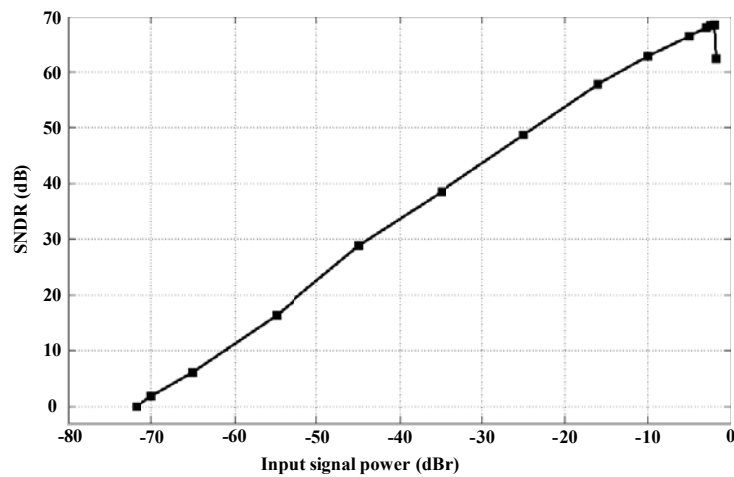


Fig. 4.29. SNDR versus input signal at 200MHz.

Table 4.6 Performance summary of the BP ΣΔ Modulator

|  | TSMC 0.18μm CMOS |
|---|---|
| Power Supply | 1.8V |
| IF Frequency | 200 MHz |
| Clock Frequency | 800 MHz |
| Bandwidth | 10 MHz |
| Peak SNR @ 10MHz Bandwidth | 70.03 dB |
| Peak SNR @ 20MHz Bandwidth | 62.71dB |
| IM3 @ -5dBr | -73.5 dB |
| Peak SNDR @ 10MHz Bandwidth | 68.4dB |
| Dynamic Range | 70dB |
| Power Consumption | 160 mW |
| Core area | 2.48 mm$^2$ |

Table 4.7 provides a comparison of the proposed architecture with previously reported bandpass modulators and ADCs. Comparing with the works using mainstream CMOS technologies, this design achieved the highest operational frequency, the widest bandwidth of the modulator, and the best linearity performance. In the last column, the classic figure of merit (FoM) is employed to compare the efficiency of the topologies.

$$FoM = \frac{Power}{2^{ENOB} * (2 * BW)}$$

(4.25)

Although [28] and [29] achieved higher operational frequency by employing more advanced SiGe technologies, the FoM of the works are not comparable to our design. A

comparison between the FoM for various BP ΣΔ modulators versus signal frequency is shown in Fig. 4.30, where this design achieves the better FoM than the state-of-art of continuous-time BP ΣΔ modulators.
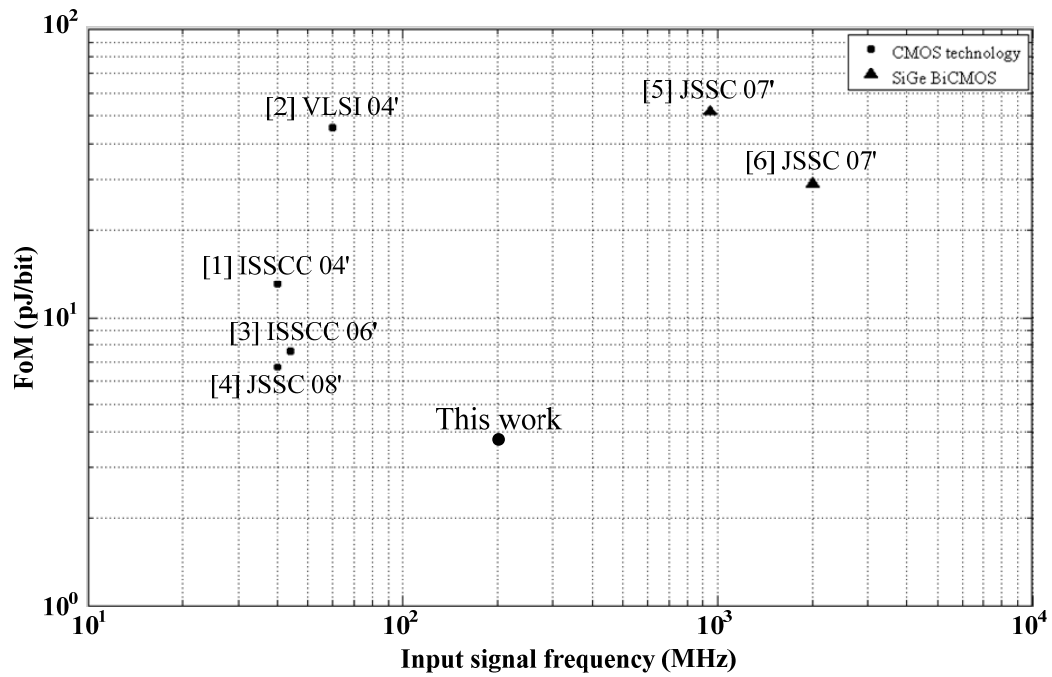


Fig. 4.30. FoM comparison versus center frequency of the BP ΣΔ modulators.

Table 4.7 Comparison with previously reported BP ΣΔ modulators

| Reference | Technology | Fs | IF (MHz) | Bandwidth | Peak SNDR | IM3 | Power | Area mm² | FoM (pJ/bit) |
|---|---|---|---|---|---|---|---|---|---|
| [26] BP$^\Delta$ | CMOS;0.18um | 264MHz | 44 | 8.5 MHz | 71dB$^\#$ | -72dB | 375mW* | 2.5 | 7.6* |
| [28] BP | CMOS;0.35um | 60MHz | 40 | 1MHz | 63dB$^\#$ | 68dB | 16mW | 0.44 | 6.69 |
| [29] BP | SiGe; 0.25um | 3800MHz | 950 | 1 MHz | 59dB | -62dB | 75mW** | 1.08 | 51.5** |
| [30] BP | SiGe; 0.13um | 40GHz | 2000 | 60MHz | 55dB | - | 1.6W* | 2.4 | 29* |
| [31]BP | CMOS;0.18um | 60MHz | 40 | 2.5 MHz | 69dB | - | 150mW | - | 13 |
| [32] BP | CMOS;0.35um | 240MHz | 60 | 1.25 MHz | 52dB | -51dB | 37mW | 1.2 | 45.5 |
| This work | CMOS;0.18um | 800MHz | 200 | 10MHz | 68.4dB | -73.5dB | 160mW* | 2.48 | 3.72* |

$^\Delta$: This is an I/Q realization using an off-chip inductor

$^\#$: $SNDR = \frac{Signal\ Power}{Noise+IM3-component}$

*: doesn't include the power consumption of clock generator

**: only static power consumption

4.6 Conclusion

A 200MHz IF 6$^{th}$-order continuous-time bandpass ΣΔ modulator with 800MHz sampling clock is designed and implemented in 0.18μm CMOS technology. The proposed calibration scheme optimizes the NTF and makes the topology tolerant to PVT variations. The modulator achieves a peak SNDR of 68.4dB in a 10MHz bandwidth and a remarkable FoM of 3.72 pJ/bit which outperform the previously reported architectures. The total power consumption is 160mW from a single 1.8V power supply. 24% of the power consumption is employed in the analog section while the remaining power is used for digital drivers, quantizer, programmable delay, rotator and DAC controller. Therefore, this architecture will significantly benefit from scaled technologies.

4.7 Appendix A: Distortion Analysis of The Basic Closed-Loop System

The lossless integrator can be analyzed following the approach proposed by Sansen [38]. Although this approach is not precise, it allows us to obtain simpler solutions that make it possible to identify the critical issues while linearizing the amplifier. The basic amplifier to be analyzed is depicted in Fig. 4.9. Let's assume that the closed loop output voltage can be expressed as,

$$Vout = b_1 V_{in} + b_3 V_{in}^3, \tag{A.1}$$

where b1 and b3 are the first and third order coefficients, respectively, and are obtained as follows

$$b_1 = \frac{dV_{out}}{dV_{in}}\Big|_{v_{in}=0} \tag{A.2}$$

$$b_3 = \frac{1}{6}\frac{d^3V_{out}}{dV_{in}^3}\Big|_{v_{in}=0} \tag{A.3}$$

Basic nodal analysis of the topology at $V_x$ and $V_{out}$ allow us to obtain the following results

$$\frac{(V_{in}-V_x)}{Z_1} = \frac{V_x-V_{out}}{Z_2} + \frac{V_x}{Z_3} \tag{A.4}$$

$$\frac{V_x-V_{out}}{Z_2} = gm_1V_x + gm_3V_x^3 + \frac{V_{out}}{Z_L} \tag{A.5}$$

From equations A.4 and A.5 it follows that

$$V_{out} = \frac{V_{in}(Y_1(Y_2-Gm_1))-\frac{Gm_3(V_{in}Y_1+V_{out}Y_2)^3}{(Y_1+Y_2+Y_3)^2}}{(Y_2+Y_L)(Y_1+Y_2+Y_3)+Y_2(Gm_1-Y_2)} \tag{A.6}$$

Inserting A.1 into A.6 and making use of A.2, the following expression for b1 can be obtained

$$b_1 = \frac{Y_1(Y_2-Gm_1)}{(Y_2+Y_L)(Y_1+Y_2+Y_3)+Y_2(Gm_1-Y_2)} \tag{A.7}$$

A similar procedure for finding b3 yields,

$$b_3 = \frac{Gm_3Y_1{}^3(Y_2+Y_L)^3(Y_1+Y_2+Y_3)}{((Y_2+Y_L)(Y_1+Y_2+Y_3)+Y_2(Gm_1-Y_2))^4} \tag{A.8}$$

In this derivations, it was assumed that the even-order harmonic coefficients can be ignored due to the fully differential nature of the architecture. However, these non-linear terms can be easily determined following a similar strategy. The integrator's IM3 is then obtained from (A.1), (A.7) and (A.8) as

$$IM3 = \frac{3}{4}\left|\frac{\left(\frac{Gm_3}{Gm_1-Y_2}\right)\left(\frac{Y_1}{Y_1+Y_2+Y_3}\right)^2}{\left(1+\left(\frac{Gm_1-Y_2}{Y_1+Y_2+Y_3}\right)\left(\frac{Y_2}{Y_2+Y_L}\right)\right)^3}\right|(v_{in})^2 \tag{A.9}$$

Notice that the amplifier's loop gain (LG) is given by $LG = \left(\frac{Gm_1-Y_2}{Y_1+Y_2+Y_3}\right)\left(\frac{Y_2}{Y_2+Y_L}\right)$. As

expected, the larger the loop gain the better the system linearity. Assuming that LG>>1

at the frequency range of interest, a simplified expression for IM3 is obtained

$$IM3 \cong \frac{3}{4}\left|\left(\frac{Gm_3}{(Gm_1-Y_2)^4}\right)(Y_1+Y_2+Y_3)(Y_1)^2\left(\frac{Y_2+Y_L}{Y_2}\right)^3\right|(v_{in})^2 \qquad (A.10)$$

In the case of the loss-less integrator, (A.10) around the integrator's unity gain frequency

becomes

$$IM3 \cong \frac{3}{4}\left|\left(\frac{Gm_3}{(Gm_1)^4}\right)\left(\frac{1}{R_g}\right)^2\left(\frac{1}{R_g||R_3}\right)(1+sR_LC)^3\left(1+s(R_g||R_3)C\right)\right|(v_{in})^2 \qquad (A.11)$$

It should be remarked that all parameters must be evaluated at 200MHz. According to

(5), $\frac{G_{m3}}{G_{m1}} = \frac{1}{8}\frac{(A_{V1}A_{V2})^2}{V_{dsat3}^2}$ and $G_{m1} = g_{m3}(A_{V1}A_{V2})$, leading to

$$IM3 \cong \frac{3}{32}\left|\left(\frac{1+\frac{R_g}{R_3}}{(A_{V1}A_{V2})(gm_3R_g)^3}\right)\left((1+sR_LC)^3\left(1+s(R_g||R_3)C\right)\right)\right|\left(\frac{v_{in}}{V_{dsat3}}\right)^2 \qquad (A.12)$$

To verify the theoretical results, a comparison with cadence results are shown in Fig.

4.31. The default setting of the integrator is shown in Table 4.8.

Table 4.8 Default coefficients of the simulated integrator

| Coefficient | Value |
|---|---|
| $Gm_1$ | 158mA/V |
| $Gm_3$ | 6725.2A/V$^3$ |
| $Z_1 = Z_3 = R_g$ | 1k ohm |
| $Z_2 = 1/(sC_1)$ | 1pF |
| $Z_L = R_L$ | 1.25k ohm |
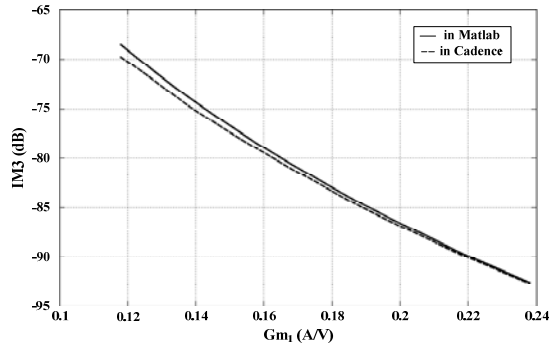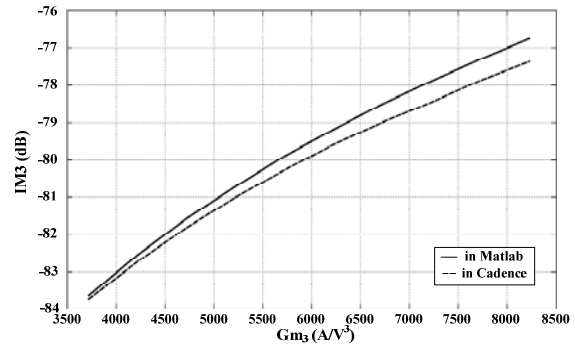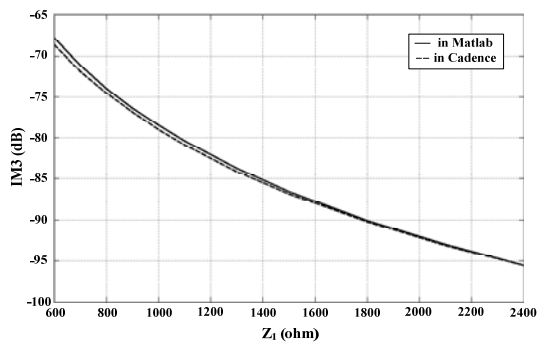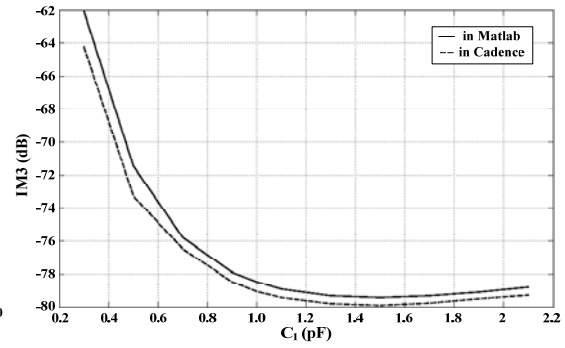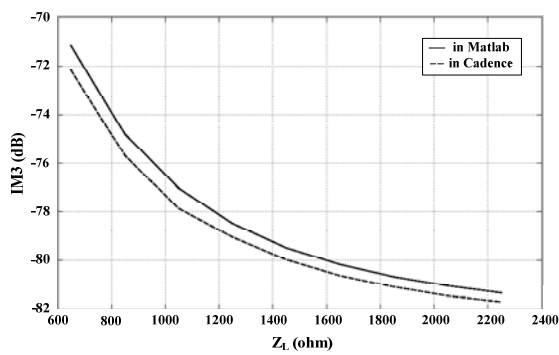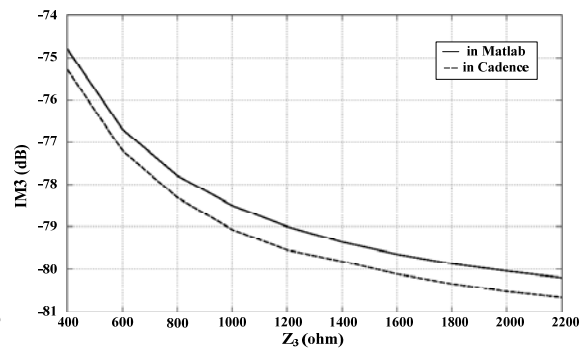
Fig. 4.31. The IM3 trend when sweeping
(a) $Gm_1$ (b) $Gm_3$ (c) $Rg_1$ (d) $C_1$ (e) $Z_L$ (f) $Z_3$.

4.8 Appendix B: System Simulation in Simulink

As shown in Fig. 4.4, the system is modeled in Simulink to exam the modulator performance. By setting the fixed-step type and ode5 solver option in configuration parameters, Simulink can achieve better simulation accuracy for the modulator. However, there is an accuracy trade-off between the number of the captured point at the output of the modulator and the simulation time. To achieve efficient simulations with acceptable simulation accuracy, 40000 points of the modulator output are captured and processed in each simulation. The captured data are processed by using the command "FFT" in Matlab to acquire the system performance in frequency domain.

Since there is no difference between voltage signal or current signal in Simulink, gain stages are used to model the transconductance of the gm stages and current-steering DACs. For each of the $2^{nd}$-order biquads of the loop filter, two transfer function blocks are employed to model the transfer function from the input of the first amplifier and the input of the second amplifier to the bandpass output of the two-integrator loop architecture, respectively. A rising edge-triggered digital integrator with the sampling clock is modeled as the S/H. The output of the integrator follows the signal from the loop filter at the moment of the clock rising edge. By using the integration value of 0, the output is thus maintained at that value at the rest of time till next rising edge. The continuous-time transport delay is used to model the processing delay of the digital circuitries including the quantizer and the logic gates in feedback path. In ideal case, the value is set to $1/F_s$. The effect of excess loop delay to the system can be simulated by changing the delay.

Composed by the comparators with different reference voltage, the behavior model of the 2-bit quantizer is built. The rotator is modeled by employing a counter and D-flip flops based on its behavior.

All the non-idealities of the modulator are considered in the Simulink to ensure the system performance. For example, the non-linear performance and the input referred thermal noise of the filter biquads are modeled by using the extra blocks parallel connecting with input gm stages. The white noise models the thermal noise of the circuit while the cubic power block followed by a gain stage presents the third order harmonic distortions. The saturation blocks are used to simulate the saturation effect from power supplies. The jitter noise effect of modulator is simulated by placing the build-in jitter noise block in the feedback path. The static current mismatch in DACs are modeled by cascading extra gain stages with DACs where the gain of these gain stages are randomly picked in every simulation by using the command "rand" in Matlab.

# CHAPTER V

# A 25MHZ BANDWIDTH 5TH-ORDER CONTINUOUS-TIME LOWPASS SIGMA-DELTA MODULATOR WITH 67.7DB SNDR INTRODUCTION

5.1 Introduction

Different wireless standards such as WiMAX have been developed in recent years due to the high demand for faster data rate in portable wireless communications, which has pushed bandwidths up to a few tens of megahertz. In addition, among all the receiver architectures, the zero-IF architecture is popular because of its high power efficiency. Due to the emphasis on efficiency, the use of high-resolution lowpass sigma-delta ($\Sigma\Delta$) analog-to-digital converters (ADCs) with wide bandwidth is essential in multi-standard applications to accommodate receiver bandwidth requirements. For example, the $\Sigma\Delta$ ADC reported in [24] achieves 72dB signal-to-noise-and-distortion ratio (SNDR) over 10MHz bandwidth by employing a 5-bit voltage-controlled oscillator (VCO)-based quantizer. Also, with 10MHz bandwidth, a peak SNDR of 82dB was reached in [45]. A $\Sigma\Delta$ ADC with 50-level time-to-digital-converter (TDC) and pulse-width modulation (PWM) in the feedback path was presented in [46], reaching 20MHz bandwidth and 60dB SNDR. Other CMOS implementations in [47] and [48] achieved resolutions of 69dB SNDR and 70dB SNDR over 20MHz by using a discrete-time MASH architecture with two 4-bit quantizers and a 3$^{rd}$-order continuous-time (CT) architecture with 4-bit quantizer, respectively. Excellent performance was reported in [21] for a 12-bit modulator with 20MHz bandwidth. Designed in SiGe technology, the 1-bit lowpass $\Sigma\Delta$ modulator in [8] extends the bandwidth to 1GHz with 37.1dB SNDR.

This chapter presents a 5$^{th}$-order CT lowpass ΣΔ modulator that utilizes multi-phase operation to attain 67.7dB SNDR over a 25MHz bandwidth. Clocked at 400MHz, the proposed architecture contains a 3-bit two-step quantizer, a level-to-PWM converter in the feedback path, and a one-bit digital-to-analog converter (DAC) to obtain multi-bit feedback with a PWM scheme. This approach can be accommodated to most CT ΣΔ modulators in order to alleviate the non-linearity problems caused by unit element mismatch of conventional multi-bit DACs. Ultra-clean clocks are generated by an inductor-capacitor (LC) tank VCO and complementary injection-locked frequency divider (CILFD) to ensure multi-phase digital signals with low time-domain jitter noise. To meet the noise and linearity requirements, a carefully designed active-RC loop filter topology was employed. The digital-intensive prototype consuming 48mW was fabricated in Jazz Semiconductor 0.18μm CMOS technology.

Table 5.1 The specifications of the CT LP ΣΔ modulator

| Specification | Value |
|---|---|
| **Clock frequency (Fs)** | 400MHz |
| **Signal bandwidth** | 25MHz |
| **Target SNDR** | > 68dB |
| **Technology** | Jazz 0.18um CMOS technology |
| **Supply** | 1.8V |

5.2 System Planning

5.2.1   Noise budgeting

The noise budgeting and system planning of the CT LP ΣΔ modulator are necessary to ensure its performance. Table 5.2 shows the noise budgeting for each noise source.

Table 5.2 Noise budget for different noise source

| Parameter | Signal-to-the noise-ratio |
|-----------|---------------------------|
| SQNR | > 73dB |
| SJNR | > 73dB |
| STNR | > 76dB |
| SDR | > 74dB |
| SNDR | > 68dB |

Usually, by using the time-domain feedback DAC, the system is more sensitive to the jitter noise than that with conventional NRZ multi-bit DACs due to more frequent transitions of the feedback pulses. As a result, the jitter noise may dominate the system noise analysis. 73dB of SJNR is assigned in this design. Due to the low oversampling ratio (OSR=8) and wide required bandwidth (25MHz), the achievable signal-to-quantization noise-level is only 61.8dB when employing $5^{th}$-order 1-bit system. The system stability is a very critical issue if higher order system is adopted. To lower the quantization noise level without complicating the system architecture, 3-bit quantizer and DACs is preferred in this prototype. Therefore, a $5^{th}$-order system architecture with

3-bit quantizer and DACs is employed. For the thermal noise and distortion, since their contributions can be minimized by reducing the input resistors of the filters and employing the PWM technique in the feedback digital circuitries (will be explained in section 5.2 and 5.6.1), they are arranged at 76dB and 74dB, respectively.

## 5.2.2 Transfer function analysis

A 5$^{th}$-order lowpass NTF is expected in the system and thus the open loop transfer function of the system can be determined.

$$NTF_{lowpass} = (1 - z^{-1})^5 = \frac{1}{1+TF(z)} \Rightarrow TF(z) = \frac{-(z-1)^5+z^5}{(z-1)^5} \tag{5.1}$$

To ensure modulator's stability and required bandwidth, the pole arrangements as quasi-linear phase inverse Chebyshev lowpass transfer function is employed and the command of "cheby2" in Matlab is used to determine the poles' locations. After impulse invariant transformation as (4.7), the s-domain open loop transfer function is given as

$$TF(s) = \frac{7.14s^5+5.28*10^9s^4+2.11*10^{18}s^3+6.1*10^{26}s^2+8.5*10^{34}s+1.4*10^{43}}{s^5+1.5*10^8s^4+4.1*10^{16}s^3+3.7*10^{24}s^2+3.5*10^{32}s+9.4*10^{39}} \tag{5.2}$$

where the pole frequencies are located at 24.5MHz, 16.7MHz, and 6.71MHz, respectively. The STF=TF/(1+TF) and NTF=1/(1+TF) based on (5.2) are depicted in Fig. 5.1 where the in-band attenuation of NTF is larger than 56dB and the passband gain is 6.2dB in STF. Although the gain of NTF is not flat in the range of DC to 25MHz, the 56dB attenuation on quantization noise can deliver required SQNR. With the open loop transfer function in (5.2), all the coefficients in the system can be determined once the system architecture is chosen.
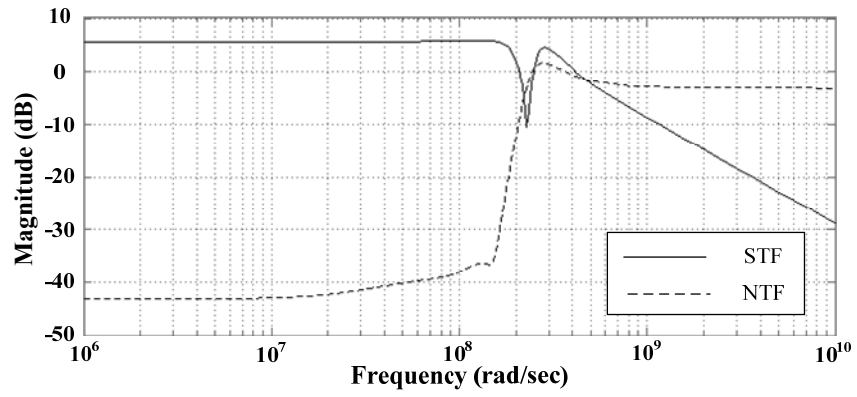
Fig. 5.1. The plot of STF and NTF.

### 5.2.3    System architecture

The proposed fully-differential 5$^{\text{th}}$-order lowpass $\Sigma\Delta$ modulator with sampling frequency of 400MHz for 25MHz signal bandwidth (BW) is depicted in Fig. 5.2.
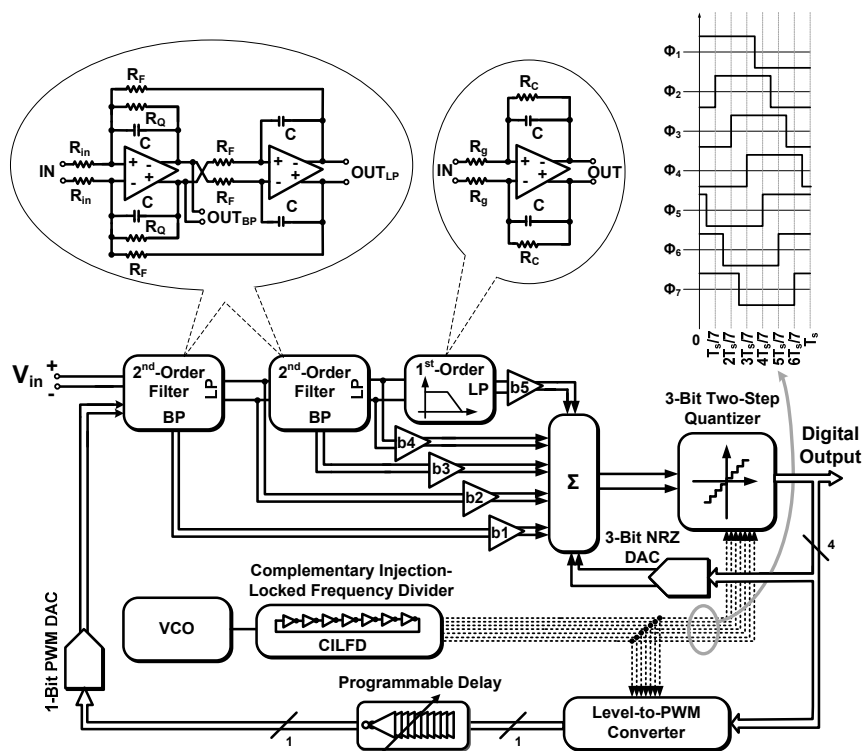


Fig. 5.2. System architecture of the proposed 5$^{\text{th}}$-order CT modulator.

A feedforward architecture has the advantages that only one accurate DAC is required and that signal swings at the internal nodes of the loop filter can be maintained low, improving the linearity performance of the overall system. To ensure flat passband gain in the loop filter from DC to 25MHz as well as loop stability, a 5$^{\text{th}}$-order quasi-linear phase inverse Chebyshev lowpass filter with 49dB pass-band gain is employed, which consists of two cascaded 2$^{\text{nd}}$-order lowpass sections and a lossy integrator. Both outputs (lowpass and bandpass) of each 2$^{\text{nd}}$-order section are fed forward to allow full

control over the coefficients in the loop transfer function. The respective 3-dB frequencies are set to 24.5MHz, 16.7MHz, and 5.71MHz. The quality factors of the first and second stage are 7.5 and 1.6, respectively. A high-Q first stage and the smallest possible feedforward coefficients were selected to improve the anti-aliasing characteristics of the topology under consideration of the constraints associated with the noise transfer function. The summing amplifier ($\Sigma$) couples all feedforward paths to the quantizer input. A 3-bit two-step quantizer is employed; and the level-to-PWM converter translates the multi-bit signal into a time-domain digital PWM signal such that only a 1-bit current-steering DAC is required for global feedback with 3-bit equivalence. This realization avoids performance degradation originated from current mismatch linked to conventional multi-bit DACs. The non-idealities of the local feedback DAC (3-bit NRZ DAC in Fig. 5.2) at the quantizer input are noise-shaped by the modulator loop, making this DAC design less critical. A standard 3-bit DAC was chosen for the local feedback to reduce the effect of excess loop delay. A 2.8GHz LC tank VCO and a ring oscillator type CILFD produce low-jitter clock signals at 400MHz with seven evenly distributed phases ($\Phi_1$-$\Phi_7$) for the digital logic of the quantizer and the level-to-PWM converter. The simulation result of the proposed system architecture gives 73.4dB SNR in 25MHz bandwidth as shown in Fig. 5.3.
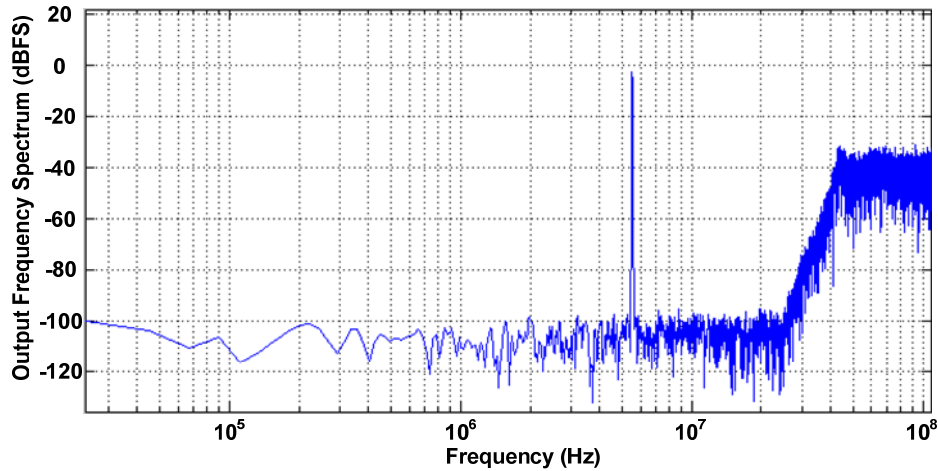
Fig. 5.3. The simulated output spectrum of the proposed modulator.

## 5.3 Level-to-PWM Converter

Due to the requirements of wide bandwidth and high resolution, combinations of multi-bit quantizer and DACs generating multi-level signals as shown in Fig. 5.4a are commonly employed [9]. $Q_{inj}$ is the charge injected by a feedback DAC per sampling period $T_s$, which is obtained by scaling the amplitude of current I in seven increments ($\alpha$). Multi-bit DAC nonlinearity from device mismatch due to process variations will generate out-band noise that folds into the frequency range of interest as well as in-band harmonic distortion components that degrade the modulator's SNDR. Solutions such as noise-shaping dynamic element matching (DEM) [14], tree-structure DEM [15], and the data weighted averaging technique [16] were proposed in the past to reduce the DAC linearity degradation from mismatch. However, improvements in wideband ADCs are usually limited due to restrictions on loop delay and increased noise levels from the

randomization procedure. Alternatively, time-domain digital signal processing concepts based on [49] can be employed in practice [46] for enhanced performance.



$$Q_{inj} = (\alpha I)T_s$$

*where:*

$$\alpha = [0, \frac{1}{7}, \frac{2}{7}, .... 1]$$

(a)



$$Q_{inj} = I(\alpha T_s)$$

*where:*

$$\alpha = [0, \frac{1}{7}, \frac{2}{7}, .... 1]$$
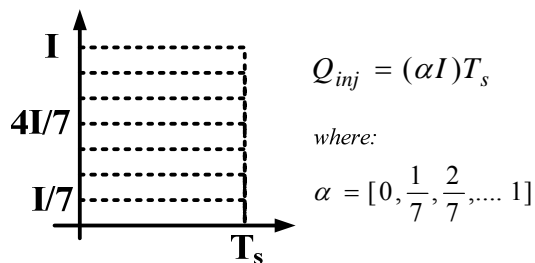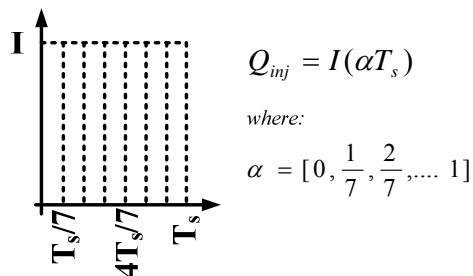
(b)

Fig. 5.4 Multi-bit output
(a) the conventional 3-bit NRZ DAC, (b) the 7-phase 1-bit DAC.

In this work, a single-level DAC having an output waveform with variable pulse width per sampling period generates a 3-bit charge injection feedback as shown in Fig. 5.4b. Since only one inherently linear single-level DAC produces different feedback charge levels at the loop filter input, the current mismatch problem of multi-amplitude DACs is avoided. Instead of employing the PWM in the signal path [46], the proposed level-to-PWM converter is implemented in the feedback path to convert the digital codes

from the 3-bit quantizer to time-domain PWM signals compatible with a single-level DAC as shown in Fig. 5.5. The sampling clocks with the required phases for level-to-PWM converter are generated precisely by a VCO followed by a ring-type injection-locked frequency divider. The programmable delay composed by a cascade of inverters, a MUX, and a flip-flop is employed to compensate the processing delay in the global feedback path.
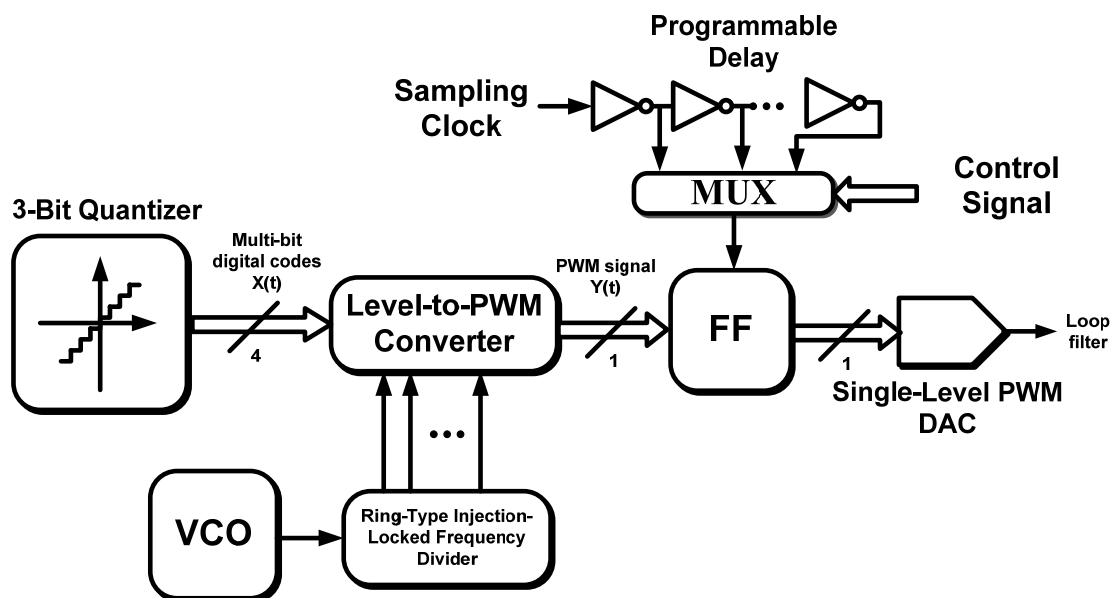


Fig. 5.5. Level-to-PWM converter in the feedback path.

The pulse shapes are arranged as symmetric as possible within a clock period to minimize power of potential aliasing tones [50]. Table 5.3 lists the pseudo-symmetric high ("1") and low ("0") amplitude levels of the 1-bit DAC during the seven intervals with the corresponding binary code representations; and two examples are visualized in Fig. 5.6.

Table 5.3 Pulse arrangement of the 7-phase time-domain feedback DAC signal

| Binary Code Equivalent | $0 - T_s/7$ | $T_s/7 - 2T_s/7$ | $2T_s/7 - 3T_s/7$ | $3T_s/7 - 4T_s/7$ | $4T_s/7 - 5T_s/7$ | $5T_s/7 - 6T_s/7$ | $6T_s/7 - T_s$ |
|---|---|---|---|---|---|---|---|
| 000 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 001 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 010 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 011 | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| 100 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 101 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |
| 110 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 111 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |



(a)                                                       (b)
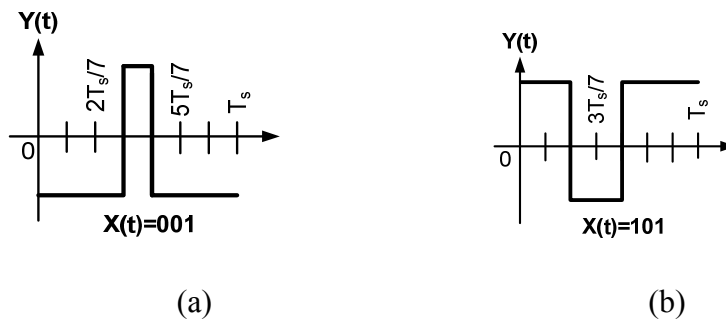
Fig. 5.6. Example pulse shapes for two quantizer output codes

(a) 001 (b) 101.

The drawback of employing multi-phase time-domain signals is increased sensitivity to jitter noise because of larger and more frequent DAC output transitions compared to a conventional 3-bit non-return-to-zero (NRZ) DAC. In general, the maximum signal-to-jitter-noise ratio (SJNR) can be analytically estimated as [10]:

$$SJNR_{peak} = 10\log_{10}\left( \frac{T_s^2 \cdot OSR}{2 \cdot \sigma_y^2 \cdot \sigma_\beta^2} \right)$$

(5.3)

where OSR = $1/(2 \cdot BW \cdot T_s)$, $\sigma_\beta$ is the clock jitter standard deviation, and $\sigma_y$ is the standard deviation of [y(n) - y(n-1)]; with y(n) being the nth combined digital output of the modulator. With the presented architecture and pulse arrangement, $\sigma_y^2 = 8.96$ was obtained through simulations in Matlab. The SJNR of the modulator with level-to-PWM converter was evaluated in comparison to a conventional 3-bit modulator. Fig. 5.7 shows the simulated SNR performance vs. clock jitter for the proposed modulator and a 3-bit modulator with conventional NRZ DAC (400MHz sampling). With $\sigma_\beta \approx 0.5ps$, the SJNR limit of the PWM DAC is 5dB lower than for a conventional 3-bit NRZ DAC at 400MHz. However, the single-element PWM DAC is not affected by SNDR reduction from unit current source mismatches as the 3-bit NRZ DAC. From Fig. 5.7, the clock jitter requirement for SNDR > 68dB with the proposed modulator is $\sigma_\beta < 0.54ps$.
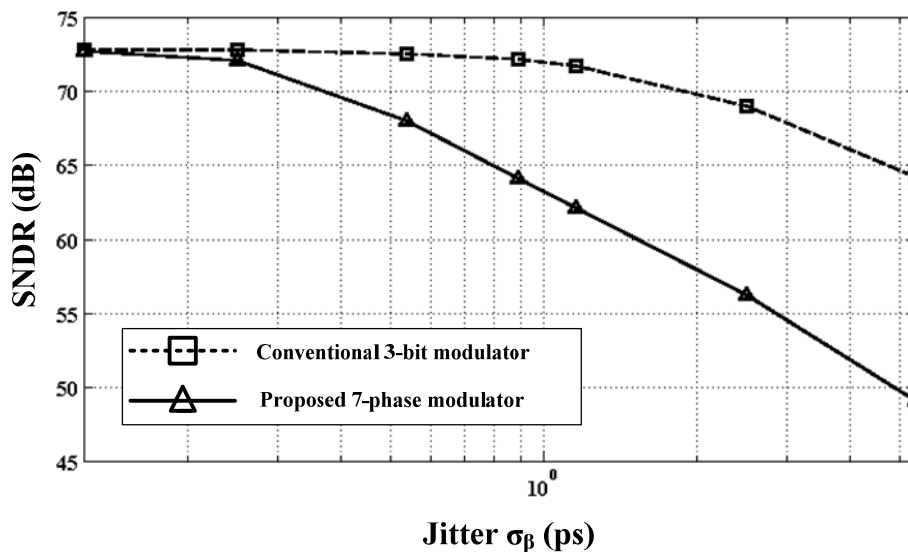


Fig. 5.7. SNR (SQNR+SJNR) vs. jitter of the proposed modulator with the 7-phase feedback DAC compared to the conventional 3-bit modulator/DAC with 400MHz sampling.

The nonlinearity of the PWM DAC due to static timing mismatches can be evaluated from a feedback charge error comparison relative to the conventional 3-bit DAC. Fig. 5.8 visualizes the worst-case peak-to-peak charge errors for each code, which are resultants of static mismatch $\Delta I_i$ for each current cell in the conventional DAC and static timing error $\Delta T_j$ of clock phase $\Phi_j$ in the PWM DAC. $\Delta T_j$ originates from the static CILFD mismatches and unequal propagation delays due to routing parasitics. The ideal feedback charge per code is identical for both DACs. Notice that the errors depend on mismatches in up to seven unit elements of the conventional DAC, but only up to two timing phases with the PWM scheme. Assuming equal mismatches ($\Delta I_i = \Delta I$, $\Delta T_j = \Delta T$) yields worst-case errors of $\pm 7\Delta I \cdot T_s$ and $\pm 2\Delta T \cdot I$ for conventional and PWM DACs, respectively. Letting $\delta_{\%I} = \Delta I/(I/7)$ and $\delta_{\%T} = \Delta T/(T_s/7)$ be the percent standard deviations of the mismatches in each case, the worst-case errors are $\Delta Q_{conv.-worst} = \pm 7\delta_{\%I} \cdot (I/7) \cdot T_s$ and $\Delta Q_{PWM-worst} = \pm 2\delta_{\%T} \cdot I \cdot (T_s/7)$. Monte Carlo post-layout simulations including delay mismatches in all clock phases showed that $\delta_{\%T} = 0.16\%$ as a result of the synchronizing effect from the injection-locking. Since $\delta_{\%I}$ is typically 0.5% with good layout practices for a standard DAC, the anticipated worst-case linearity error of the PWM DAC is favorably lower. Assuming that two timing mismatches are accumulated in the case of the PWM-based ADC, all mismatches in the conventional realization are accumulated, and errors are un-correlated in both cases; the induced third harmonic distortion (HD3) comparison ratio can be estimated as derived in the section 5.9:

$$\frac{HD3_{PWM}}{HD3_{conventional}} \cong \left( \sqrt{\frac{2}{N}} \right) \left( \frac{\delta_{\%T}}{\delta_{\%I}} \right), \qquad (5.4)$$

where N is the number of DAC levels. For N = 7 and the aforementioned distributions, the linearity of the proposed PWM DAC outperforms the conventional DAC by 15.3dB based on (5.4).
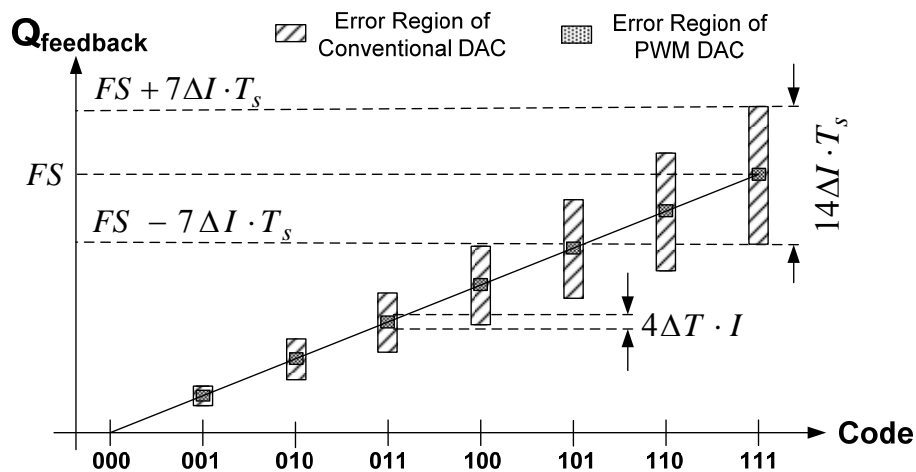


| $\lvert \Delta Q \rvert$ | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
|---|---|---|---|---|---|---|---|---|
| Conventional DAC | 0 | $\Delta I_1 \cdot T_s$ | $\sum_{i=1}^{2} \Delta I_i \cdot T_s$ | $\sum_{i=1}^{3} \Delta I_i \cdot T_s$ | $\sum_{i=1}^{4} \Delta I_i \cdot T_s$ | $\sum_{i=1}^{5} \Delta I_i \cdot T_s$ | $\sum_{i=1}^{6} \Delta I_i \cdot T_s$ | $\sum_{i=1}^{7} \Delta I_i \cdot T_s$ |
| PWM DAC | 0 | $(\Delta T_4 + \Delta T_5) \cdot I$ | $(\Delta T_3 + \Delta T_5) \cdot I$ | $(\Delta T_3 + \Delta T_6) \cdot I$ | $(\Delta T_3 + \Delta T_6) \cdot I$ | $(\Delta T_3 + \Delta T_5) \cdot I$ | $(\Delta T_4 + \Delta T_5) \cdot I$ | $2\Delta T_1 \cdot I$ |

Fig. 5.8. 3-bit DAC linearity error comparison: conventional vs. PWM.

5.4 Complementary Injection-Locked Frequency Divider

To generate the multi-phase signals, a LC tank VCO and complementary injection-locked frequency divider (CILFD) were combined for good phase noise performance with low power consumption [51]. Phase noise of injection-locked stages in a ring is high-pass filtered by the loop dynamics, making the ring oscillator's output phase noise after locking mainly a function of the lower VCO noise. The injection signal is generated with a 2.8GHz LC tank VCO to obtain seven phases at 400MHz with equal duty cycles using a divide-by-7 CILFD.

5.5 3-Bit Two-Step Current-Mode Quantizer

Traditional two-step flash ADC architectures are a subset of subranging ADCs that typically consist of a sample-and-hold (S/H), a most-significant bit(s) (MSB) ADC, a DAC, a gain block, and a least-significant bit(s) (LSB) ADC [52]. A two-step flash conversion has the benefit that the output bits from two low-resolution ADCs can be combined to obtain higher precision while reducing the number of comparators that a conventional flash ADC would require for the same resolution. In comparison to conventional flash architectures, multi-step quantization can reduce area and power consumption when multiple clock phases/cycles are available. Successive approximation ADCs are not constrained to low-speed operation anymore as a result of higher achievable clock frequencies with modern CMOS technologies. Hence, several flash alternatives or adaptations involving successive approximations have been reported in recent years at progressively higher conversion speeds [53]-[56]. The proposed

architecture is a two-step ADC that combines a 1-bit MSB decision with a second TDC step during which the input is successively compared to reference levels ramped in discrete increments.

The on-chip clock frequency and number of phases were selected according to the design requirements associated with the PWM feedback DAC. As illustrated in Fig. 5.9, the quantizer utilizes the seven clock signals to control four sequential comparison instances ($\tau_1$-$\tau_4$), which cuts the number of comparators from seven to four with respect to a typical 3-bit flash ADC. The two-step process makes the MSB available after the first step, creating timing margin for the digital control logic that sets up the PWM DAC. An implicit TDC method during the second step resolves the remaining bits in a similar manner as the TDC quantizer in [46]. However, a discrete reference ramp rather than a continuous ramp is generated for comparison with the input signal. Since the algorithm only has three LSB quantization steps, the discrete ramp is a simple alternative that also gives the option to calibrate each reference level individually if necessary.
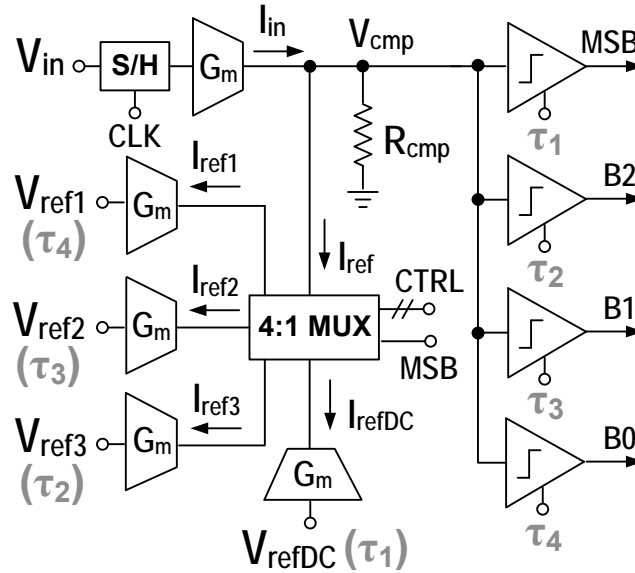
Fig. 5.9. Single-ended equivalent block diagram of the quantizer.

The quantizer operates as follows with regards to the topology in Fig.5.9 and corresponding timing diagram in Fig. 5.10.
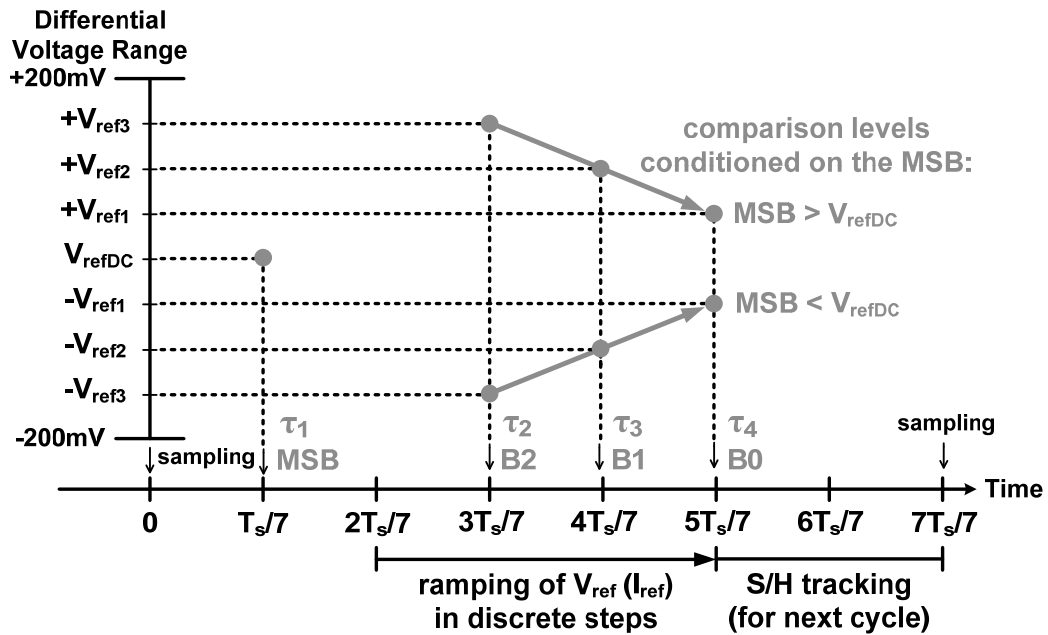


Fig. 5.10. Timing of the quantization decisions.

The differential input signal $V_{in}$ is sampled with a S/H circuit at the beginning of the 400MHz master clock having a period $T_s$, and then it is converted to current $I_{in}$ via a transconductance stage ($G_m$). First, the MSB is resolved after $\tau_1$ seconds by comparing $I_{in}$ to the current from $V_{refDC}$ applied to an identical $G_m$ stage. Depending on the timing control bits (CTRL) and the MSB decision, a multiplexing configuration (MUX) is utilized to compare $I_{in}$ to current $I_{ref}$ derived from the appropriate differential reference voltage ($\pm V_{ref1}...\pm V_{ref3}$) during each subsequent instant ($\tau_2$-$\tau_4$). The order of the subranging comparisons and output bits was chosen based on the timing needs in the multi-phase DAC control circuitry because larger signal magnitudes require DAC feedback pulse changes early in the next clock cycle. Comparison resistor ($R_{cmp}$) converts the difference in currents into a positive or negative voltage. Only the binary result of the current-mode comparison is stored using a latched comparator for each of the four time slots. Thus, the latch states represent the instant in time at which the discrete reference ramp has crossed the input signal level, providing the time-domain information needed by the PWM DAC. Table 5.4 summarizes the quantization ranges for the differential input voltage signal and the corresponding output bits stored in latches. These latches are accessed directly in the next clock cycle to determine the appropriate switching instants for the PWM DAC.

Table 5.4 3-bit quantization ranges and output codes

| Differential Input Ranges | MSB | B2 | B1 | B0 | Binary Code Equivalent |
|---|---|---|---|---|---|
| 200mV to 150mV | 1 | 1 | 1 | 1 | 111 |
| 150mV to 100mV | 1 | 0 | 1 | 1 | 110 |
| 100mV to 50mV | 1 | 0 | 0 | 1 | 101 |
| 50mV to 0V | 1 | 0 | 0 | 0 | 100 |
| 0V to -50mV | 0 | 1 | 1 | 1 | 011 |
| -50mV to -100mV | 0 | 1 | 1 | 0 | 010 |
| -100mV to -150mV | 0 | 1 | 0 | 0 | 001 |
| -150mV to -200mV | 0 | 0 | 0 | 0 | 000 |

## 5.6 Circuit Implementation

### 5.6.1  Loop filter

Noise, linearity, power, and offset requirements decrease from the first stage to the third stage of the loop filter due to the noise-shaping of non-idealities in the second and third filter stages by the closed-loop system. This makes the noise and distortion introduced by the first stage most critical for overall performance. After having identified the demands for input-referred noise density under $7nV/Hz^{1/2}$ and third-order intermodulation products (IM3) less than -72dB, the first two-integrator-loop active-RC filter in Fig. 5.2 was designed with sufficient linearity as well as relatively small input resistors ($R_{in}$ = 1K$\Omega$), large integrating capacitors (C = 1pF), and amplifiers having gain greater than 40dB at 25MHz for adequate thermal noise levels. Resistors $R_F$ and $R_Q$ in the first section have values of 6.5K$\Omega$ and 40K$\Omega$, respectively.

The fully-differential schematic of the amplifiers for the two-integrator loop filter is shown in Fig. 5.11. A two-stage topology with feedforward compensation was adopted

[37] to satisfy the high amplifier gain and bandwidth requirements. Using this technique, the negative phase shift introduced by the poles in the main path is compensated with the positive phase shift introduced by the left-hand plane (LHP) zero due to the feedforward path. Cascode stages are avoided to make the solution exportable to technologies with lower supply voltages. The first stage ($MN_1$, $MP_1$) of the amplifier is designed to have high gain and a dominant pole determined by the parasitic capacitances and overall resistance at the drain of $MN_1$. The output swing of this stage does not have to be high because the signal is further amplified in the second stage. The shunt-feedback resistors $R_1$ provide the required common-mode detection [57] and feedback to stabilize the amplifier's first stage. These polysilicon resistors are sufficiently large to prevent sacrificing significant gain. Transistors $MP_1$ are sized such that the DC voltage of the first stage output matches the DC voltage required for the input of the second stage. The second-stage transconductance gain is composed of $gm_{P2B}+gm_{N2}$ from transistors $MP_{2B}$ and $MN_2$, where $MP_{2B}$ reuses the bias currents from $MN_3$ and $MN_2$ to save power. Transistors $MP_{2A}$ are used to accommodate the common-mode feedback (CMFB) control. The second and feedforward ($MN_3$) stages are optimized for large gain up to 25MHz. Since stage two affects the overall linearity, transistors $MN_2$, $MP_{2A}$, and $MP_{2B}$ are biased with high saturation voltages (> 200mV) to allow larger signal swings.

The DC level at the second stage output is controlled using a CMFB circuit consisting of $R_2$, $C_2$, $MN_4$, and $MP_4$. The output common-mode level is detected with resistive averaging ($R_2$), and the error is fed back to node $V_{CMFB}$ for regulation of the output level. Stability is enhanced by adding a small capacitor $C_2$ to introduce a LHP zero in the CMFB path. Simulations showed that amplifier gain larger than 44dB at

25MHz and IM3 below -73.5dB with 400mV$_{p-p}$ output swing are achieved in all process and temperature corners. Furthermore, capacitor banks with ±30% tuning range were employed for compensation of time constant variations.
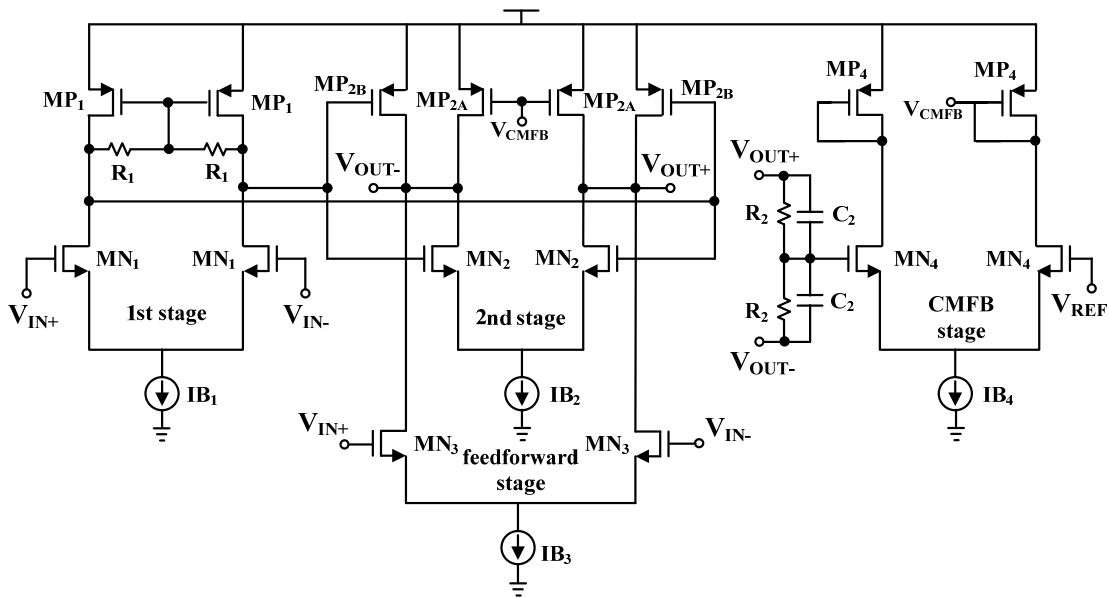


Fig. 5.11. Schematic of the amplifier employed in loop filter.

### 5.6.2   Summing amplifier

The summing amplifier is a critical analog block since it is used for the local feedback path around the quantizer. For precise equivalence between discrete and continuous-time loop transfer functions it is required to maintain exactly one sampling period delay in the local feedback path. This gives rise to a stringent bandwidth requirement for the design of the summing amplifier displayed in Fig. 5.12 because the bandwidth of the summing stage mainly depends on the RC time constant associated with its resistors.
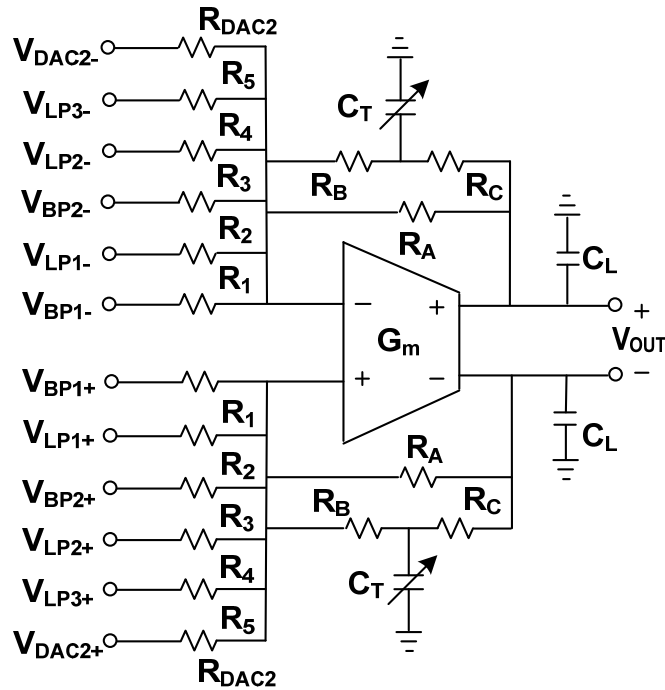
Fig. 5.12. Summing amplifier stage.

The conventional feedback resistor is split into two pieces, and one of them is replaced by a T-RC network. This feedback network creates a zero-pole pair, which introduces positive excess phase in the overall transfer function to adjust for the group delay of the summing node. Capacitor $C_T$ is tuned to optimize the loop delay in the local feedback path consisting of the summing amplifier, quantizer, and secondary NRZ DAC. The feedback network with zero $\omega_z = 1/[(R_B \| R_C) \cdot C_T]$ and pole $\omega_p = (R_A + R_B + R_C)/(R_B R_C C_T)$ will not affect the loop stability significantly because the zero-pole pair is placed at frequencies higher than the bandwidth of the summing amplifier. However, it introduces negative group delay at low frequencies. Phase $\theta$ of the summing amplifier transfer function can be obtained as

$$\theta(\omega) = \tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) \ . \tag{5.5}$$

The corresponding group delay ($\tau_{delay}$) can be derived by taking the derivate of the phase:

$$\tau_{delay} = -\frac{d\theta(\omega)}{d\omega} = -\frac{(\omega_z - \omega_p)(\omega^2 - \omega_z\omega_p)}{(\omega^2 + \omega_z^2)(\omega^2 + \omega_p^2)} \quad . \tag{5.6}$$

This group delay is negative at frequencies that are lower than $\omega_z$, $\omega_p$, and the unity gain bandwidth of the amplifier. Hence, the overall delay in the local feedback loop can be adjusted by changing the zero and pole frequencies through tuning of capacitor $C_T$.

### 5.6.3  3-bit two-step current-mode quantizer

With the discussion of the quantizer operation in section 5.4, Fig. 5.13 displays the schematic of the quantizer core in which the current-mode comparisons are made. All devices with the same labels are equal-sized and matched in the layout. The simplified S/H circuit represents a transistor-level implementation with gate-bootstrapping [58], and the AND gates effectively function as time-controlled MUX.
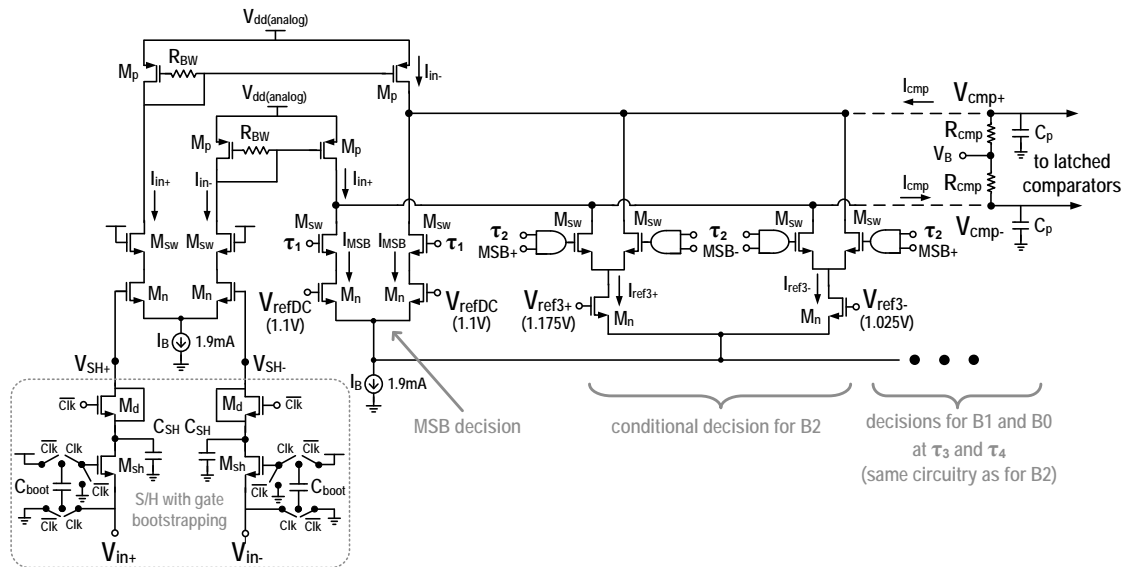


Fig. 5.13. Simplified schematic of the current-mode quantizer core circuitry.

For each reference current step, the polarity of this differential voltage is resolved by the following latched comparator. Polysilicon resistors ($R_{BW}$) extend the bandwidth of the current mirrors [59] for high-frequency operation according to:

$$BW_{mirror} = g_{mp}/2C_{gsp} \xrightarrow{resistive\_compensation} BW_{mirror} = \tfrac{1}{2\pi}\sqrt{g_{mp}/(R_{BW} \cdot C_{gsp}^2)} \ , \quad (5.7)$$

where $g_{mp}$ and $C_{gsp}$ are the transconductance and gate-source capacitance of $M_p$, correspondingly. With $R_{BW} = 330\Omega$, the simulated 3-dB bandwidth of the current mirrors is 3.36GHz, which is sufficiently high to prevent it from becoming the factor that limits comparison speed. More critical is that speed performance is ensured by selecting the value of resistors $R_{cmp}$ such that the RC time constant formed with parasitic capacitance $C_p$ at the comparison nodes ($V_{cmp+}$, $V_{cmp-}$) does not impose limitations. After switch $M_{sw}$ closes to compare the current from the input signal with the appropriate reference at each instant, the difference current $I_{cmp} = I_{cmp+} - I_{cmp-}$ will cause a step response which can be modeled with a first-order approximation:

$$V_{cmp(t)} = 2 \cdot I_{cmp} \cdot \left( R_{cmp} - R_{cmp} \cdot e^{-\frac{t}{R_{cmp} \cdot C_p}} \right). \quad (5.8)$$

Note that $V_{cmp(t)}$ settles within 5% of its final value after approximately $3 \cdot R_{cmp}C_p$ seconds. In this design, $R_{cmp}$ is 400$\Omega$ and the capacitance from transistor and layout parasitics ($C_p$) is approximately 250fF, resulting in an approximate time constant close to 100ps and permitting adequate time for settling within the $T_s/7 \approx 360$ps intervals. Nevertheless, it is only critical for $V_{cmp}$ to be larger than the resolution of the latched comparator that resolves whether $V_{cmp}$ is positive or negative. This zero-crossing event occurs earlier than the settling moment, allowing time to pre-charge the nodes inside the activated latch by its preamplifier within the comparison time windows. Since the timing

at this comparison node has significant impact on the quantizer resolution, the current-mode operation involving sequential comparisons by switching between reference currents makes this topology attractive in deep submicron technology. For example, a simulated design of the quantizer circuitry in 90nm CMOS meets the same design specifications with less than one tenth of the power consumption as a result of smaller parasitic capacitances at critical nodes and higher $f_T$ of transistors. The reference voltages at the gates of the differential pairs do not require buffers having low output impedance. Thus, they can be supplied with off-chip references as in this prototype or they can be generated with on-chip bias circuitry consuming minimal power. The clocked comparators connected to $V_{cmp}$ in Fig. 5.9 are implemented with the fully-differential circuit shown in Fig. 5.14.
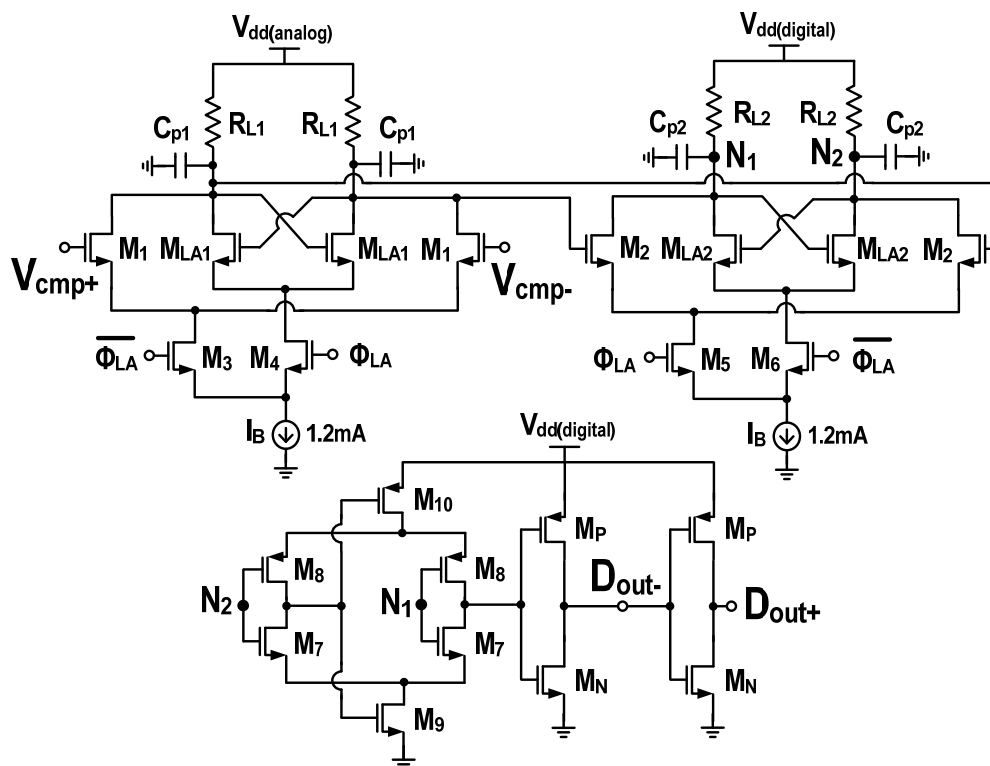


Fig. 5.14. Latched comparator schematic.

In the tracking phase, $\Phi_{LA}$ is low and bias current $I_B$ is steered into the preamplifier stage consisting of input transistor $M_1$ and load resistor $R_{L1}$. To save power, the bias current is reused in the latch phase (high $\Phi_{LA}$) when it flows into $M_{LA1}$. Devices $M_2$, $R_{L2}$, $M_{LA2}$ form a second preamplification and latch stage, but this stage is controlled by the phase-reversed latch signal to hold the decision for almost one clock period ($T_s$). Note, the tracking ($\overline{\Phi_{LA}}$) and latching ($\Phi_{LA}$) phase durations in the first stage are $T_s/7$ and $6T_s/7$, respectively. Polysilicon resistor loads ($R_{L1}$, $R_{L2}$) are employed in the latches for high-speed operation. Transistors $M_7$-$M_{10}$ form a self-biased differential amplifier [60] which creates a rail-to-rail output during the long latch phase to drive the subsequent CMOS inverter ($M_P$, $M_N$). The timing in the first latch is critical, and the following equation was obtained by making appropriate substitutions into the analysis results from [61] to aid the design decisions:

$$t_{LA1} = \frac{C_{p1}}{g_{mLA1}} \cdot \ln\left( \frac{\Delta V_{LA1}}{2 g_{m1} R_{L1} (V_{cmp+} - V_{cmp-})} \right),$$ (5.9)

where $\Delta V_{LA1}$ is the differential output voltage swing of the first latch, $g_{mLA1}$ and $g_{m1}$ are the transconductances of $M_{LA1}$ and $M_1$, respectively; and $C_{p1}$ represents the parasitic capacitances. Since $C_{p1}$ and $g_{mLA1}$ are the two dominant parameters in equation (5.9), the sizes of $M_1$ and $M_{LA1}$ were optimized and the routing in layout was planned to minimize the parasitic capacitance and maximize the transconductance. Thus, the latching time $t_{LA1}$ can be minimized. Analytical expressions for the device parameters with impact on the input-referred offset voltage can be derived based on the analyses in [62]-[64]. Monte Carlo simulations were performed to assess that the static offset voltages of the latched comparator and current-mode core are expected to cause errors less than 10% of the 50mV quantization step, which are noise-shaped by the modulator. However, the

reference voltages could be adjusted to change the quantization ranges individually and compensate for static offsets in the quantizer circuitry.

### 5.6.4 Level-to-PWM converter

The fully-differential block diagram of the level-to-PWM converter is shown in Fig. 5.15. The pulse waveforms are generated with SR latches, which change states at the rising edges of the clock signals with different phases from the CILFD. In every sampling period, the AND gates determine the appropriate pulse shape to be passed through the 5-input OR gate to the 1-bit DAC according to the output codes of the quantizer, which are the time-domain information bits stored in latches as described in Section II-D. A programmable delay block is included in the feedback path to avoid SNR degradation by ensuring that the excess loop delay is within 5% [41]. It is constructed with a series of digital inverters producing eight different clock delays and a MUX having 3-bit control for manual adjustment in this prototype design with an approximate delay range from 0 to 2T/7.
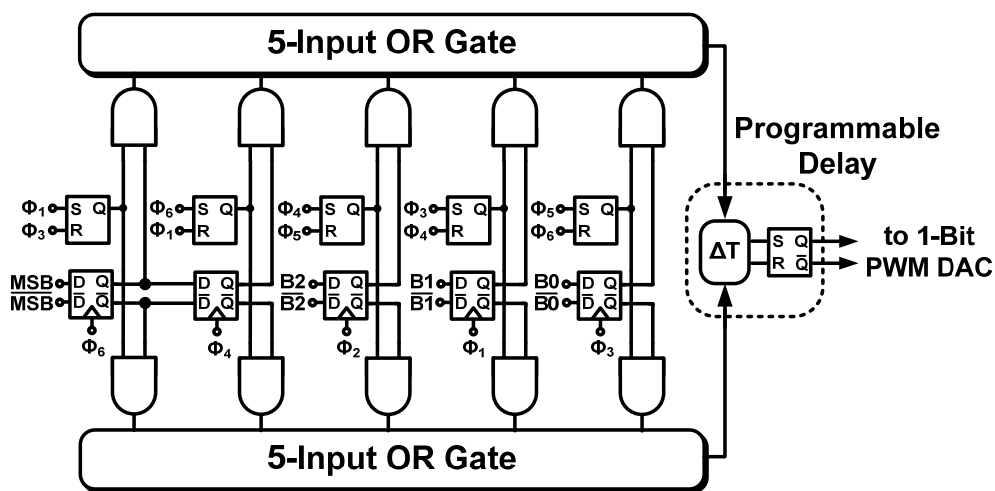


Fig. 5.15. Implementation of the level-to-PWM converter.

After accounting for the logic propagation delays in the nominal corner, the delay margin from level-to-PWM converter to DAC is almost T/7 because events are triggered by clock phases at the end of the cycle. Thus, the nominal programmable delay is set to T/7 for zero overall excess loop delay. The delayed differential PWM signals are synchronized by an additional SR latch that precedes the 1-bit PWM DAC, and the layout as well as routing were planned carefully to minimize the timing mismatches of the differential paths.

5.6.5    Complementary injection-locked frequency divider

A 400MHz clock with seven phases is utilized in several blocks of the modulator. The clock generation is performed with a 2.8GHz VCO whose differential output signal is injected into a divide-by-7 CILFD, providing outputs at 400MHz with seven equally-spaced phases. Fig. 5.16 shows the divide-by-7 CILFD composed of seven ring-oscillator stages for the proposed multi-phase modulator; details can be found in [51].
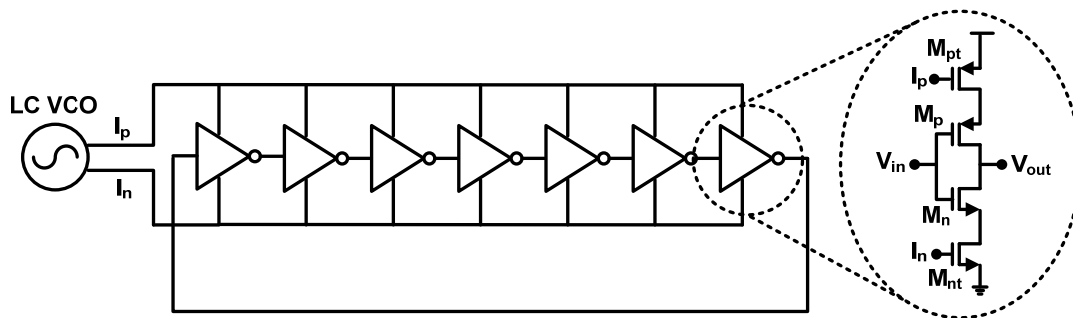


Fig. 5.16. Complementary injection-locked frequency divider (CILFD) diagram.

Every stage has an upper tail-injection transistor, $M_{pt}$, and a bottom tail-injection transistor, $M_{nt}$. Inverter transistors ($M_p$, $M_n$) are placed between the upper and bottom tail transistors, while being interconnected to form a ring. The free-running frequency of

the ring-oscillator is controlled through the DC bias voltage at the gate terminals of the tail transistors. Hence, the delay of each stage is adjusted to match the overall ring-oscillator frequency to the VCO signal that is coupled to the tail transistors via capacitors.

The phase noise of the ring oscillator outputs is mainly determined by the lower phase noise of the injected VCO signal when the stages are locked [65]. With $n$ inverters in a ring, the phase noise of a CILFD can be approximated as

$$PN_{(CILFD)} \cong PN_{(VCO)} - 10\log_{10}(2n+1)^2 \; . \tag{5.10}$$

This equation agrees well with the simulated phase noise of the divide-by-7 CILFD: the injection signal from the 2.8GHz VCO presents phase noise of -119dBc/Hz at 1MHz offset frequency, and the divide-by-7 CILFD outputs show phase noise of -136dBc/Hz at 1MHz offset.

5.7 Measurement Results

Fig. 5.17 displays the chip microphotograph of the multi-phase CT 5$^{th}$-order lowpass $\Sigma\Delta$ modulator fabricated in Jazz Semiconductor 0.18μm 1P6M CMOS technology, which was assembled in a QFN-80 package. It occupies a total area of 2.6mm$^2$, including the VCO and CILFD but excluding pads and ESD protection circuitry. The power consumption from a 1.8V supply is 48mW. Of this power, 27mW (56%) is consumed by the quantizer and level-to-PWM converter. Since the switching frequencies are up to 2.8GHz, a significant power reduction is expected from technology scaling of these blocks because they largely contain circuitry with dependence on switching speed

and therefore become more efficient as the $f_T$ of transistors increases. The outputs of the

CILFD were measured with a spectrum analyzer to assess the quality of the multi-phase

clock signals in the frequency domain, and the measurement in Fig. 5.18 is from one of

the CILFD outputs achieving 0.6ps RMS jitter integrated from 4KHz to 1MHz

frequency offset, where the low-noise external source locks the on-chip VCO [65].

Accordingly, the $SJNR_{peak}$ from equation (5.3) is approximately 67dB, which in

contrast with the measured results suggests that the modulator is more robust to jitter

than estimated. The four output bits (MSB, B2…B0) of the quantizer were captured with

a 4-channel oscilloscope synchronized at 400Msamples/s prior to post-processing in

Matlab.
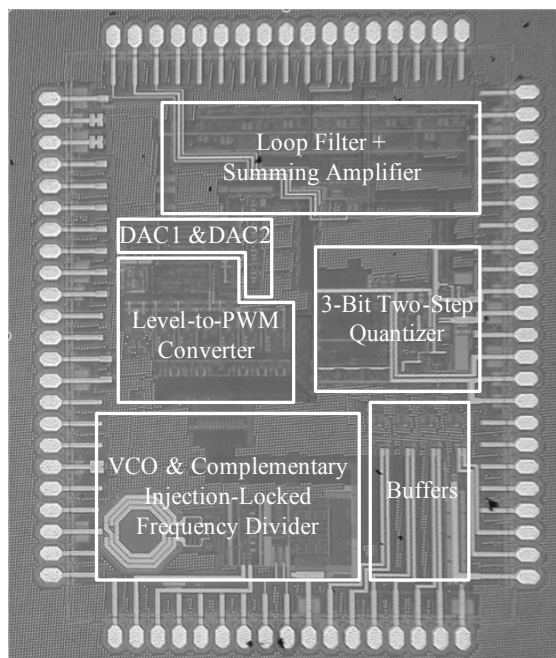


Fig. 5.17. Chip microphotograph (2.6mm$^2$ area, excluding pads and ESD circuitry).
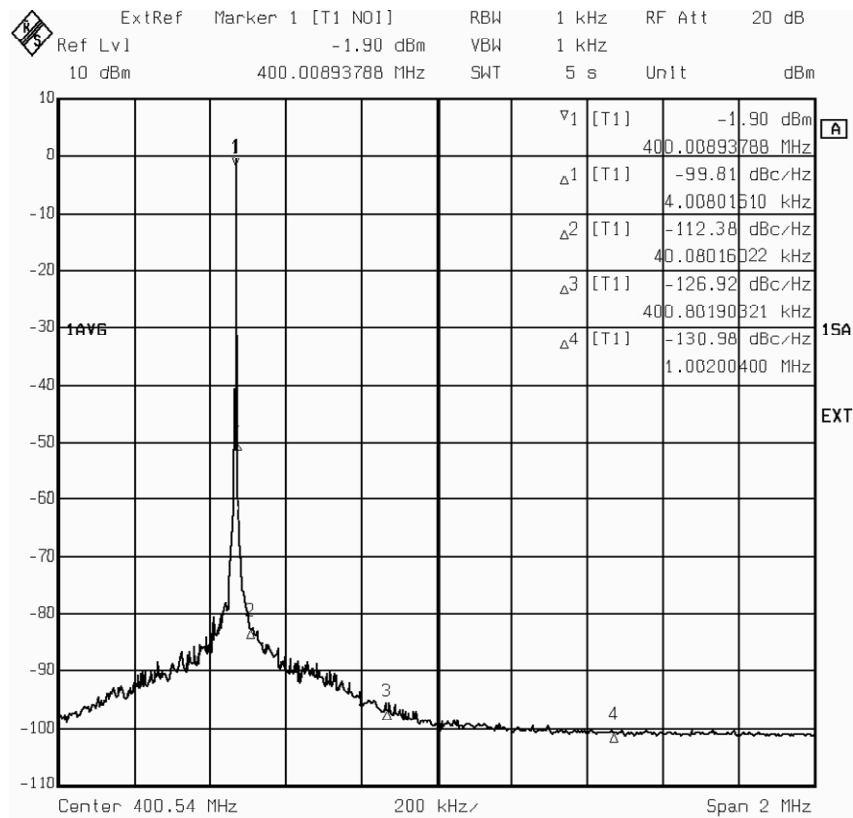
Fig. 5.18. Measured spectrum of one CILFD output.

Fig. 5.19 shows the output spectrum of the modulator with an input of -2.2dBFS at 5MHz. Based on the noise bandwidth of 6.1kHz during the measurement, the average noise floor is around -145dBFS/Hz and the peak SNR is 68.5dB in 25MHz bandwidth. The third-order harmonic distortion (HD3) in this case is 78dB below the test tone, which demonstrates the high linearity properties of both loop filter and DAC. The peak SNDR including the harmonic tones in the 25MHz bandwidth is 67.7dB. The measured SNR and SNDR for different input signal powers are plotted in Fig. 5.20, in which the 69dB dynamic range (DR) is annotated.
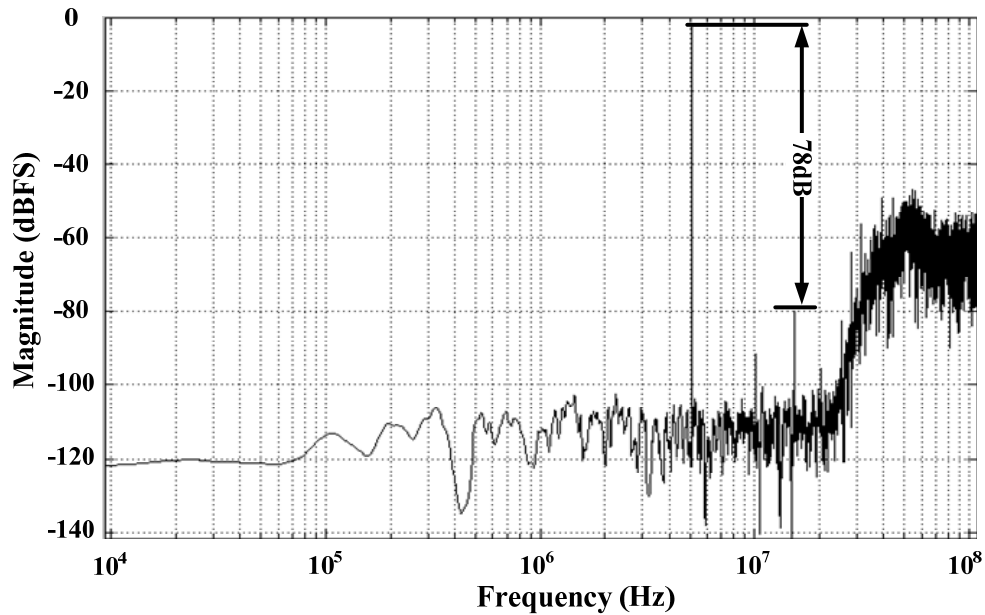
Fig. 5.19. Measured output spectrum of the modulator with a -2.2dBFS input at 5.08MHz.

Linearity performance was characterized by injecting two tones with 2MHz separation, each having a power of -5dBFS. The IM3 from two-tone tests at different frequency locations is plotted in Fig. 5.21. An increased IM3 at higher frequency can be observed because the linearity in the amplifiers of the loop filter is frequency-dependent.
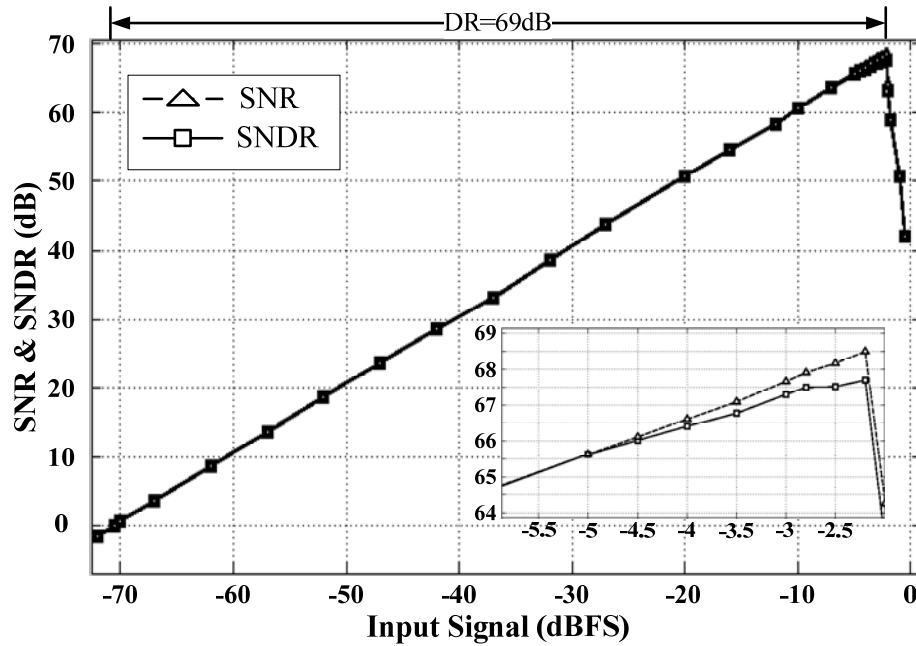
Fig. 5.20. Measured SNR and SNDR versus input signal power.
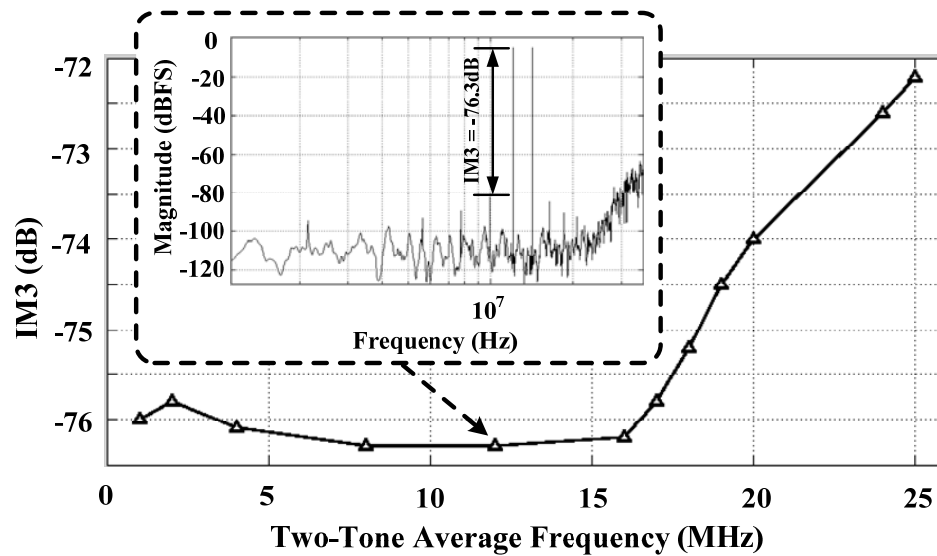


Fig. 5.21. IM3 vs. average frequency of two -5dBFS input tones separated by 2MHz.

To emulate the appearance of a blocker from another channel, an additional measurement with -10dBFS input power at 390MHz (10MHz offset from the clock frequency) was conducted to assess the blocker rejection capability of the modulator. As evident from Fig. 5.22, the blocker aliases into the desired band due to the sampling operation, but the power level of this in-band interference is attenuated down to -66dBFS, achieving 56dB blocker rejection. This property is highly desirable for broadband applications because the anti-aliasing in the modulator relaxes the filtering requirements for the preceding blocks in the receiver chain.
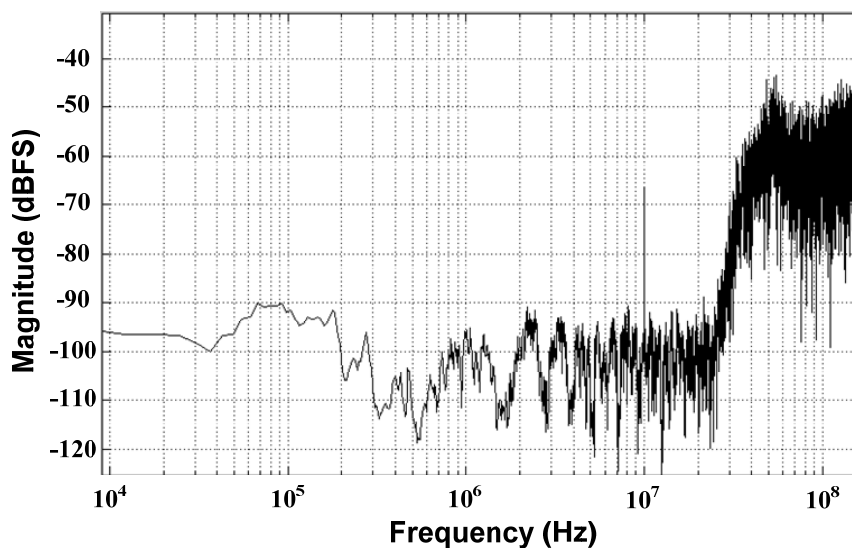
Fig. 5.22. Aliasing test: measured output spectrum with a -10dBFS input tone at 390MHz.

Table 5.5 presents an overview of the modulator performance. The power budget is 44mW for the modulator core, 2.5mW for the VCO and locked ring oscillator, and 1.5mW due to clock buffers. Table 5.6 shows a comparison between the proposed

modulator architecture and recently reported modulators based on the following figure-of-merit (FoM):

$$FoM = \frac{Power}{2^{ENOB} * (2 * BW)} \cdot$$

(5.11)

Although fabricated in an economical technology, the achieved 444fJ/bit FoM of the proposed modulator core is competitive with the current state of the art while providing high rejection to strong blockers. In addition, a FoM improvement is anticipated if the solution is exported to deep submicron technologies, which would lower the quantizer and level-to-PWM converter power as a result of more efficient switching operations.

Table 5.5 Summary of the measured ADC performance

| Technology | Jazz 0.18μm CMOS |
|---|---|
| Power Supply | 1.8V |
| Clock Frequency | 400MHz |
| Bandwidth | 25MHz |
| Peak SNR / SNDR* @ 25MHz Bandwidth | 68.5dB / 67.7dB |
| SFDR | 78dB |
| IM3 (-5dBFS per tone) | < -72dB |
| Dynamic Range | 69dB |
| Power Consumption | 48mW |
| Area without pads &ESD protection | 2.6mm$^2$ |

* Includes total in-band distortion power and noise.

Table 5.6 Comparison with previously reported LP ΣΔ ADCs

| Reference | Technology | $F_s$ | BW | Filter Order | Peak SNDR | Power | FoM (fJ/bit) |
|---|---|---|---|---|---|---|---|
| [24] JSSC 2008 | 130nm CMOS | 950MHz | 10MHz | 2 | 72dB | 40mW* | 500 |
| [45] ISSCC2008 | 180nm CMOS | 640MHz | 10MHz | 5 | 82dB | 100mW[†] | 487 |
| [46] ISSCC2009 | 65nm CMOS | 250MHz | 20MHz | 3 | 60dB | 10.5mW[†] | 319 |
| [47] ISSCC2007 | 90nm CMOS | 340MHz | 20MHz | 4 | 69dB | 56mW[#] | 608 |
| [47] ISSCC2008 | 90nm CMOS | 420MHz | 20MHz | 4 | 70dB | 28mW[†] | 271[Δ] |
| [21] JSSC 2006 | 130nm CMOS | 640MHz | 20MHz | 3 | 74dB | 20mW[†] | 122 |
| [8] JSSC 2009 | 130nm SiGe | 40GHz | 1GHz | 2 | 37.1dB | 350mW[†] | 2990 |
| This work | 180nm CMOS | 400MHz | 25MHz | 5 | 67.7dB | 48mW* (44mW[†]) | 484* (444[†]) |

\* Includes clock generation circuitry.
[†] For modulator circuitry only.
[#] Includes digital calibration of RC spread & noise cancellation filter.
[Δ] Discrete-time modulator (would require anti-aliasing filter for comparable blocker rejection).

5.8 Conclusion

Application of time-based processing methods in CT $\Sigma\Delta$ modulator shifts more operations into the digital realm, improving the system's robustness, scalability, and potential for power savings. A $5^{th}$-order CT LP $\Sigma\Delta$ modulator using 3-bit time-domain quantization and feedback has been demonstrated in a 0.18μm CMOS process. Nonlinearities from element mismatch of traditional multi-level DACs are circumvented because the 3-bit feedback is realized with an inherently linear single-element PWM DAC. Since low-jitter clocks are essential in time-based CT $\Sigma\Delta$ modulators, the required jitter performance is accomplished by means of an injected-locked clock generation technique which provides 400MHz clock signals with seven phases.

The measured peak SNDR of the modulator with 25MHz bandwidth is 67.7dB, while the SFDR and DR are 78dB and 69dB, respectively. Its power consumption is 48mW from a 1.8V supply. Approximately 56% of this power is dissipated in the quantizer and the level-to-PMW converter, which mainly contain circuits based on high-frequency switching. Technology scaling is expected to significantly enhance the efficiency of the proposed modulator architecture via power reduction in the digital circuitry.

5.9 Appendix: Non-Linearity Analysis of Device Mismatch in The Proposed PWM Pulses

There is always device mismatch at fabrication. Fig. 5.23 shows the digital circuitries for the conventional multi-level digital signal and the proposed PWM digital signal. In the conventional multi-level digital signal, the 3-bit feedback signal is generated by employing the DAC composed by seven parallel identical current sources. The device mismatch results in errors between current sources. Regarding the case with the proposed PWM digital signal, the 3-bit feedback signal depends on the pulse width of the control signal to the switch in the single-level DAC. The device mismatch mainly affects the timing errors between different clock phases.  Both mismatch effects generate harmonic distortions and degrade SNDR of the system. In this section, the linearity performance in both cases are analyzed and compared based on the feedback charge error from the mismatch effect.

Considering the case of the conventional (N+1)-level DAC first, and assuming that the individual current source mismatches are random with Gaussian distributions; the worst-case RMS value of the charge error from mismatch for the highest code can be computed as

$$Q_{e\_RMS(\max)} \cong \sqrt{N} \cdot Q_{ideal\,/\,step} \cdot \delta_{\%I} \,, \tag{5.12}$$

where $\delta_{\%I}$ is the standard deviation of the mismatch error present in each unit current source, $Q_{ideal/step} = (I \cdot T_s)/N$ is the feedback charge per level in one clock cycle. For the proposed DAC only two errors are accumulated, leading to:

$$Q_{e\_RMS(\max)} \cong \sqrt{2} \cdot Q_{ideal\,/\,step} \cdot \delta_{\%T} \,, \tag{5.13}$$

where $\delta_{\%T} = \Delta T/(T_S/N)$ is the static timing mismatch standard deviation of a single clock phase. $Q_{e\_RMS(\max)}$ is the worst-case error, but the actual nonlinearity error is a function of

signal power which is referred to as $Q_{e\_RMS(code)}$ in the following analysis. Assuming that the systematic errors are such that the DAC input-output relationship follows a sinusoidal error function, the actual feedback charge can be expresses as follows:

$$Q_{out} = Q_{ideal} + Q_{e\_RMS(code)} \cong (IT_S)\left(\frac{v_i}{v_{PK}}\right) + \left(Q_{e\_RMS(max)}\right)\sin\left(\frac{\pi v_i}{2v_{PK}}\right). \quad (5.14)$$

Notice that $Q_{e\_RMS(code)} = Q_{e\_RMS(max)}$ is the full-scale charge error when input voltage $v_i$ is equal to peak input $v_{PK}$ as visualized in Fig. 5.24. Third harmonic distortion can be estimated by expanding the sinusoidal function and retaining the third-order component of the Taylor series:

$$HD3 \cong \left(\frac{1}{24}\right)\left(\frac{Q_{error}}{IT_S}\right)\left(\frac{\pi}{2}\right)^3\left(\frac{v_i}{v_{PK}}\right)^2. \quad (5.15)$$

Substituting (5.12) and (5.13) into (5.15) yields the following HD3 ratio for comparison of the PWM and conventional DACs:

$$\frac{HD3_{PWM}}{HD3_{conventional}} \cong \left(\sqrt{\frac{2}{N}}\right)\left(\frac{\delta_{\%T}}{\delta_{\%I}}\right). \quad (5.16)$$
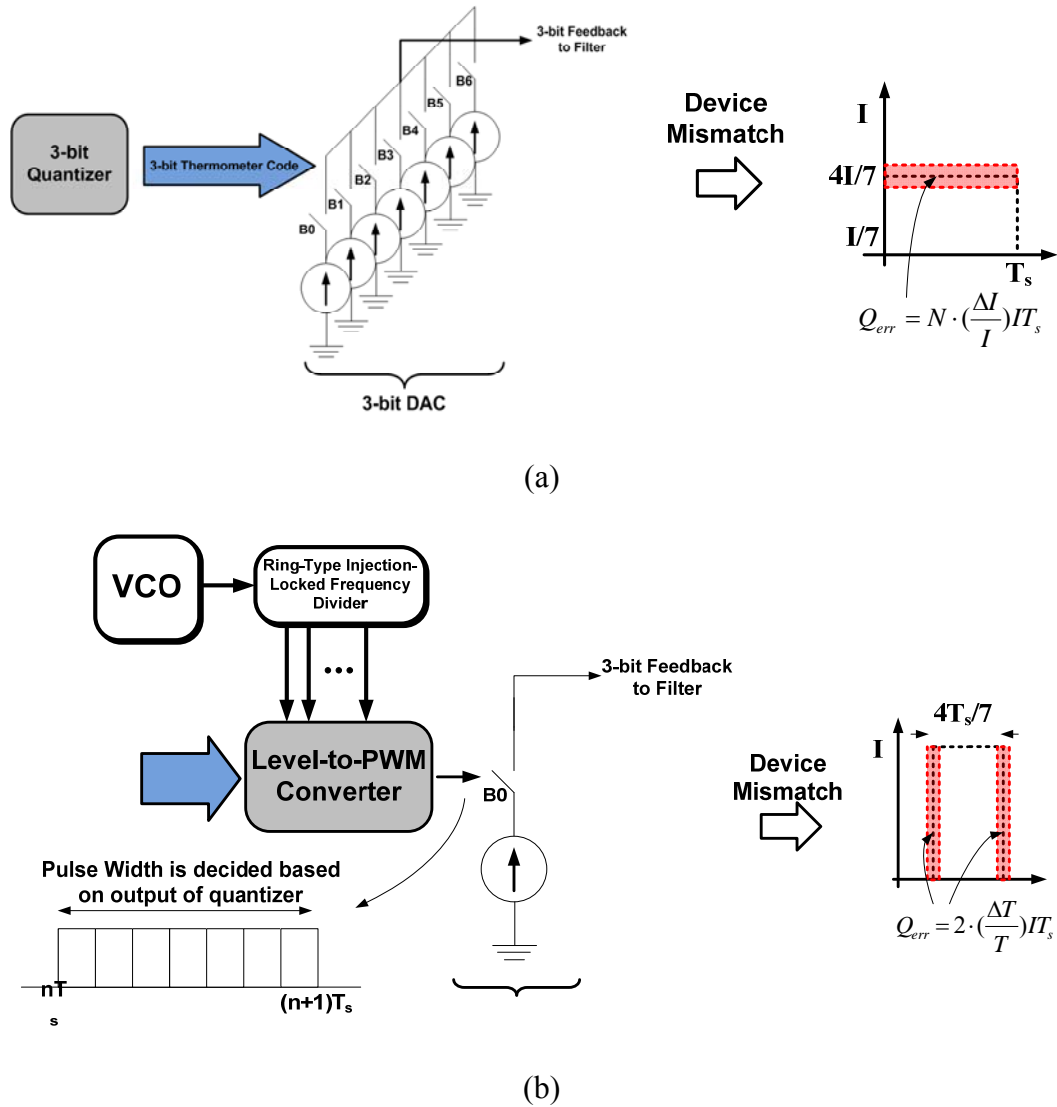
(a)



(b)

Fig. 5.23. The digital circuitries and device mismatch effect of (a) conventional multi-level digital signal (b) the proposed PWM digital signal.
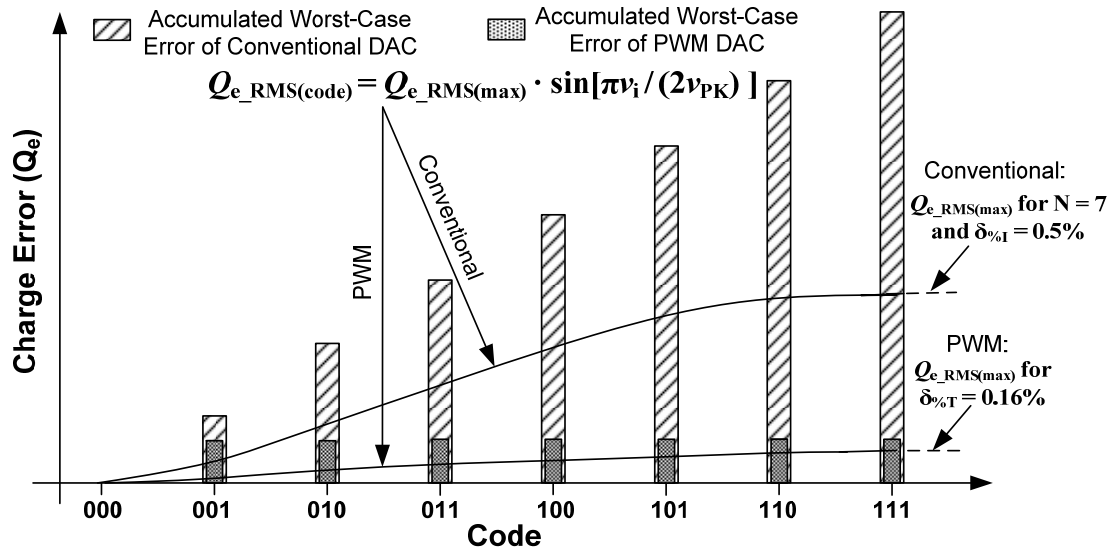
Fig. 5.24. Feedback charge error comparison.

**CHAPTER VI**

**CONCLUSION**

The analog-to-digital converter is one of the most critical blocks within the receiver of the wireless communication system based on its function to digitalize the analog signal. Among all kinds of the ADCs, the ΣΔ ADC is one of the designers' preference because of its high efficiency and high resolution, especially continuous-time ΣΔ ADCs. Continuous-time ΣΔ ADCs, which have built-in anti-aliasing filters and no speed limit on the filter circuits, can enhance the receiver efficiency further compared to discrete-time ΣΔ ADCs. As a result, the efforts are focused on the design of continuous-time ΣΔ ADC in this dissertation. A bandpass continuous-time ΣΔ ADC for software-defined radio receiver architecture and a lowpass continuous-time ΣΔ ADC for zero-IF architecture are implemented and measured for wideband multi-standard applications.

In the bandpass continuous-time ΣΔ ADC, a $6^{th}$-order 2-bit CRFB architecture at 200MHz intermediate frequency is implemented to achieve the required resolution at 10MHz bandwidth. To prevent the performance degradation from parasitic harmonic distortion components, the linearity performance of the two-integrator loop active-RC filter at the input stage is addressed and a rotator to pseudo-randomize the current mismatch of DACs is employed. In addition, due to the high sensitivity of the continuous-time system to the process, voltage and temperature variation, a robust software based calibration scheme is proposed to recover the system performance from variations by injecting two out-band test tones at the input of the quantizer to emulate the quantization noise. The measurement results of 68.4dB peak SNDR (11-bit resolution) at 10MHz with 160mW power consumption fully demonstrate the proposed concepts in

TSMC 0.18um CMOS technology.

For the design of the lowpass continuous-time $\Sigma\Delta$ ADC, the pulse-width modulation concept is implemented in time-domain two-step 3-bit quantizer and DACs in order to alleviate the current mismatch issue, which results in SNDR degradation. Compared with a conventional 3-bit NRZ DAC, the time-domain DAC (level-to-PWM converter + single-bit DAC) with appropriate pulse arrangement has 15.5dB improvements on linearity under the same level device mismatch. Ring-type complementary injection-locked frequency divider is utilized to support the required reference clocks and alleviate the jitter sensitivity. The $5^{th}$-order 3-bit CRFF system fabricated in Jazz 0.18um CMOS technology achieves 67.7dB SNDR at 25MHz bandwidth and 78dB SFDR. The 444fJ/bit FoM is comparable to the state-of-art while technology scaling is expected to significantly enhance the efficiency of the proposed modulator architecture via power reduction in the digital circuitry due to the high demand of fast switches in time-domain circuits.

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