HIGH GAIN TRANSFORMERLESS DC-DC CONVERTERS FOR RENEWABLE ENERGY SOURCES

A Thesis

by

NICHOLAS AARON DENNISTON

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2010

Major Subject: Electrical Engineering

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ABSTRACT

High Gain Transformerless DC-DC Converters

for Renewable Energy Sources. (May 2010)

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Co-Chairs of Advisory Committee: Dr. Prasad Enjeti
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Renewable energy sources including photovoltaic cells, fuel cells, and wind turbines require converters with high voltage gain in order to interface with power transmission and distribution networks. These conversions are conventionally made using bulky, complex, and costly transformers. Multiple modules of single-switch, single-inductor DC-DC converters can serve these high-gain applications while eliminating the transformer.

This work generally classifies multiple modules of single-switch, single-inductor converters as high gain DC-DC converters transformers. The gain and efficiency of both series and cascade configurations are investigated analytically, and a method is introduced to determine the maximum achievable gain at a given efficiency. Simulations are used to verify the modeling approach and predict the performance at different power levels. Experimental prototypes for both low power and high power applications demonstrate the value of multiple module converters in high gain DC-DC converters for renewable energy applications.

DEDICATION

To my family, for giving me everything I needed to succeed.

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Finally, thanks to my family and to my fiancée – for your unfailing support, and for never asking if I was finished with my thesis yet.

NOMENCLATURE

BB	Buck-boost
CCCS	Current-controlled current source
CCM	Continuous conduction mode
DCM	Discontinuous conduction mode
EAR	Equivalent averaged resistance
ESR	Equivalent series resistance
FC	Fuel cell
f_S	Switching frequency
HVDC	High voltage direct current
i_x, v_x	Instantaneous current, voltage of node x
I_x, V_x	Average current, voltage of node x
$I_{x\text{-}rms}$, $V_{x\text{-}rms}$	Root-mean-square value of current, voltage of node x
pu	Per-unit value
PV	Photovoltaic
PWM	Pulse-width modulation
RF	Ripple factor
r_x	Resistance (actual) of branch x
r_X	Equivalent averaged resistance of branch x
SCR	Silicon-controlled rectifier (thyristor)

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CHAPTER I

INTRODUCTION

1.1 Renewable energy sources

The supply and conversion of energy is of critical importance to the safety and sustainability of human life. For years fossil fuels such as coal and oil have formed the backbone of the energy supply chain, but the rapid growth of both population and energy demand has exposed the limitations of these fuels. Fossil fuels are a limited resource, and it is widely accepted that most easily extracted reserves will be exhausted within about thirty years. Additionally, the combustion of fossil fuels releases greenhouse gasses such as carbon dioxide which are believed to contribute to global warming. Presently most oil reserves are found in politically instable regions, and developed nations spend large amounts of money in both defense spending and foreign aid to ensure secure fuel supplies from these regions. The myriad economic, environmental, and political challenges inherent to fossil fuels have sparked great interest in renewable energy sources (RES) such as photovoltaic energy, fuel cells, and wind power.

It is estimated that the amount of solar energy that strikes this planet daily is more than one thousand times the current global energy demand [1]. Solar energy can be converted to electrical energy with photovoltaic (PV) cells, which are specialized semiconductors that generate electrical current when irradiated with light. PV cells can be connected in series to generate higher voltages and paralleled to generate higher curr-

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This thesis follows the style of *IEEE Transactions in Power Electronics*.

ents, but manufacturing and materiel restrictions limit the number of cells that can be combined. PV cells exhibit a power source characteristic, so the output voltage of a PV assembly varies inversely with the current drawn by the connected load; a 24 V nominal cell will provide 48 V at light loads but only 24 V at full rated power. The low output voltage and its wide fluctuation present challenges in the design of power electronics converters that interface the PV cell to the grid.

Fuel cells (FC) are electrochemical devices that use a chemical reaction to convert hydrogen fuel into electrical energy. Hydrogen is drawn into a membrane where it is split into protons and electrons. The electrons are collected as electrical energy and used in an external circuit; on their return, the electrons combine with the protons and atmospheric oxygen to create water and heat. No toxic byproducts or greenhouse gasses are produced in the reaction, and the efficiency of the reaction is much higher than that of the internal combustion engine. Each cell produces electrical voltages on the order of 1 V, so several cells must be combined in series to create useful voltages. However, mechanical challenges in providing equal fuel and air flows limit the number of cells that can be combined. Like PV cells, fuel cells also exhibit a power source characteristic with a similar 2-to-1 output voltage variation over the full power range.

Wind power is a more mature technology, and more than 100 GW of capacity has been installed throughout the world. Wind energy is used as a prime mover to generate electrical power from rotating machines. While most PV and FC assemblies generate voltages on the order of tens of volts, wind turbines can be designed to generate voltages above one thousand volts. While this voltage can be easily integrated in small amounts at the distribution level, many countries (Denmark, Spain, Germany, etc.) are turning to wind power to supply large percentages of their electrical energy usage. These large blocks of power can be moved much more efficiently at transmission level voltages on the order of hundreds or thousands of kilovolts, so power electronics converters with large DC conversion ratios are needed to interface wind farms with the grid.

All three of the methods discussed above generate electrical energy using clean, renewable energy without generating toxic byproducts or combustion gasses, and they are available throughout the globe without regard to national wealth or politics. These sources provide power at low voltage and high current (compared to output levels), and the large currents result in high semiconductor conduction losses that reduce efficiency. All three sources, whether for portable power or stationary bulk generation, also require power electronics converters with large DC conversion ratios in order to interface with the AC grid. This thesis discusses the design of power electronic converters that can interface renewable energy sources to the grid with high efficiency.

1.2 Limitations of conventional boost converters

The ideal voltage transfer characteristic of the well-known single switch boost converter can be derived from inductor volt-second balancing as $1/(1-D)$ where D is the switch duty cycle. This ideal gain is reduced due to parasitic losses in semiconductor on-resistances, diode forward voltages, and inductor DC resistances. Fig. 1 shows the voltage gain of the conventional continuous conduction mode (CCM) boost converter plotted vs. D for several values of inductor DC resistance r (expressed as a percentage of load resistance). For practical values of r in the low power range (between 1% and 5%) the maximum gain is limited to less than 5 V/V.

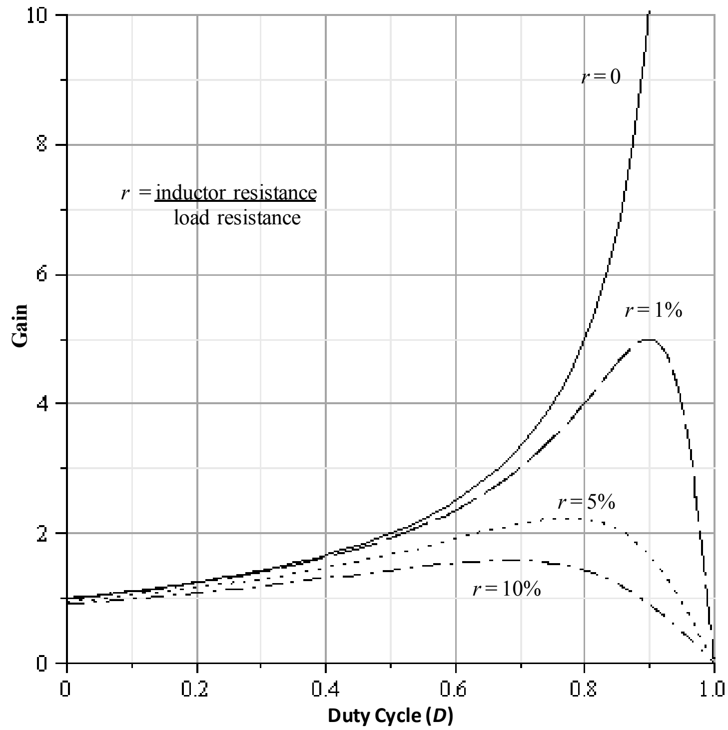


Fig. 1. Boost gain (CCM) vs. duty cycle D. Increasing inductor resistance quickly limits achievable gain.

Two problems with the voltage transfer function of the conventional boost converter are evident from Fig. 1:

1. The $1/(1-D)$ characteristic requires large duty cycles for large voltage boosts. Large duty cycles are a problem at high frequencies when the switch may not have sufficient time to turn off before the start of the next switching period.

2. Parasitics such as inductor DC resistances limit gain at large duty cycles and result in low converter efficiencies. The dissipated energy causes heating and requires additional thermal management.

Many applications requiring high gain use transformers to provide additional voltage boosting. The transformer also provides galvanic isolation between input and output. While the general shape of the transfer characteristic is identical to Fig. 1, the magnitude is boosted by the turns ratio n of the transformer. This allows the converter to operate at a smaller duty cycle which in turn reduces conduction losses. The additional gain provided by the turns ratio is balanced by other design challenges. While properly designed transformers can reduce the voltage stress on the primary side switch, the voltage stress on the secondary diode is increased by the same factor. High frequency transformer cores introduce additional loss mechanisms, and ensuring tight couplings between primary and secondary windings becomes very difficult for large n. Uncoupled (leakage) inductance induces voltage spikes across semiconductors that must be managed with complicated or lossy snubber circuitry to avoid switch failure. Transformers are costly, complex, and bulky and make up a substantial portion of both circuit volume and circuit cost. In applications that do not require galvanic isolation it is highly desirable to eliminate the transformer entirely.

1.3 Survey of existing research

Several high gain transformerless DC-DC converters have been reported in the literature. An approach discussed in several proposed converters uses coupled inductors to extend gain, assist in turning off rectifier diodes, or both. Wai et al. [2] propose a boost converter with a coupled inductor that provides both additional gain and regenerative snubbing. Wuhua et al. [3] propose a converter using a complicated coupled inductor to provide high gains and lossless snubbing. Wai et al. [4] propose a multiple-input converter for fuel cell vehicles that uses coupled inductors to provide additional gain and alleviate reverse recovery problems. Although these converters are called transformerless, the coupled inductors operate much like transformers with all of the associated benefits and disadvantages. Gain can be enhanced and switch stress can be reduced through proper choice of n, but diode stresses increase by the same factor. The circuits require complicated snubbers to alleviate the leakage energy of the coupled inductors which add to component counts and complexity. The design of coupled inductor magnetics is no less complicated than that of multiple-output, high-frequency transformers; inter-winding coupling must be very tight to minimize leakage inductances and avoid core saturation.

Luo et al. [5-7] describe an alternative series of high gain DC-DC converters known as Luo converters. Starting with either an inverse-SEPIC converter or a buck-boost converter with output filter, Luo adds sets of capacitors, inductors, and diodes to reach high gains at low duty cycles. The low duty cycles allow greater converter efficiency even after accounting for the losses in the additional series elements, but both the component count and the converter order increase dramatically. The large number of components, multiple series semiconductor drops, and complicated small signal response appear to limit the practical applications of Luo converters.

Recent research has examined combinations of basic converter configurations. Ayyanar [8] and Giri [9] describe general input-output connections using multiple basic converter modules, although their work focuses mostly on ISOP (input-series, output-parallel) connections for large voltage step-down ratios. Vorperian [10] presents results of a 10kV-to-400V step-down converter using multiple low-voltage DC-DC forward converter modules. These approaches provide modularity, which increases reliability and simplifies maintenance; however, these approaches all use multiple high frequency isolation transformers to allow arbitrary series and parallel connections of the converter outputs. Palma et al. [11] and Duran-Gomez et al. [12] propose series connections of a single-level or two-level boost converter and an identical buck-boost converter to increase gain without additional circuit complexity. The combination of a boost converter and a buck-boost converter allows the use of a shared neutral and removes the need for transformer isolation when connecting the outputs in series. Cascade connections of multiple converters have been reported for some time, including the cascaded boost converter for server applications reported by Huber and Jovanovic in [13]. These latter three converters appear well suited for extension to general high gain transformer-less converters.

1.4 Research objective

The purpose of this research is to investigate the use of multiple modules of series- or cascade-connected transformerless DC-DC converters to provide the high voltage gain needed to interface renewable energy sources to electrical grids. Each multiple module converter arrangement will be analyzed generally in a per-unit system, and semiconductor voltage and current stresses will be compared. Factors limiting gain and efficiency will be identified, and strategies for mitigating these factors will be discussed. The use of the multiple module approach for renewable energy sources will be studied in both low-power and high-power applications.

Low-power renewable energy applications use low voltage FC or PV sources that supply energy to a standard AC power interface such as a laptop power supply. Many standard PV or FC modules haves full load output voltages of 24 V, but a single-phase 120 V_{rms} inverter requires a DC input of 200 V – a gain of more than 8 V/V. This work investigates the use of a series-connected multiple module converter operated in discontinuous conduction mode (DCM) to provide the necessary gain. The steeper voltage transfer characteristic of DCM operation results in larger gains at lower duty cycles, reducing conduction losses. DCM operation also allows the switch to turn on at zero current and the diode to turn off at zero current, reducing switching losses. The rectifier diode is replaced with a MOSFET synchronous rectifier to eliminate diode reverse recovery losses and to further reduce conduction losses. A series-connected multiple-module DCM converter is shown that achieves a gain of 8.33 V/V with low conduction losses.

In high-power applications renewable energy sources are connected to the grid and can supply large blocks of power. High voltage transmission reduces current-induced (I^2R) losses in transmission lines and converters, and DC transmission allows power to be moved to distant demand centers more efficiently than AC transmission. The low per-unit parasitic elements and long switching periods available in high power applications allow the use of CCM converters with large duty cycles. It is shown that multiple module configurations can achieve high gains at high efficiencies in these applications. The advantages of series- and parallel-connected multiple module configurations in high power HVDC transmission are demonstrated through simulations, comparisons to conventional approaches, and low-power prototypes achieving gains of up to 29 V/V.

1.5 Thesis outline

Chapter I of this thesis introduces the challenges inherent in extracting usable electrical energy from renewable energy sources. The disadvantages of the conventional CCM boost converter are identified, and existing approaches to overcoming these disadvantages are presented.

Chapter II discusses the importance of efficiency in renewable applications and introduces the principle of energy conservation [14] to accurately model conduction losses in non-ideal single-switch boosting converters. Generalized models including conduction losses in CCM and DCM converters are developed that include effects of non-zero inductor current ripple.

Chapter III introduces the proposed multiple module approach. The series connection and the cascade connection are defined, and the six configurations of single-switch boosting converters are presented. Voltage gain and efficiency equations incorporating parasitic losses are derived in the per-unit system for each of the six configurations. Design considerations balancing gain and efficiency are developed, and the performance of the six configurations is compared through simulation. It is shown that cascade converters can provide high gain, but efficiency falls off quickly at large duty cycles. It is also shown that series converters provide less gain, but high efficiency can be maintained over a wider range of duty cycles.

Chapter IV applies the concepts of the multiple module approach to low-power renewable energy sources. A series converter in DCM operation is used to overcome the poor slope of the CCM voltage transfer characteristic, and the output rectifier diodes of each converter are replaced with synchronous rectifiers to increase the efficiency. Full DC transfer functions including parasitic losses are derived using the principle of energy conservation and verified via simulation. A design procedure is developed based on efficiency and gain targets. Experimental results are shown for a converter that achieves a gain of 8.33 V/V at 200 W.

Chapter V applies the concepts of the multiple module approach to high-power wind energy generation. A design example is presented for a high voltage DC transmission (HVDC) application. The multiple module approach is then compared to other HVDC approaches and is shown to perform well in terms of component counts, voltage isolation levels, reliability, and semiconductor stresses. Experimental results from low power prototypes reaching gains up to 29 V/V are presented.

Chapter VI summarizes the results of the thesis, presents general conclusions on the applications of compound converters, and identifies areas of future study to advance the work.

CHAPTER II

CONDUCTION LOSS MODELING

2.1 Principle of energy conservation

In this chapter a method of accurately modeling conduction losses and efficiency is introduced. Efficiency is an important characteristic in high-gain renewable energy applications. Inefficient conversion of energy from renewable sources increases the number of sources needed to meet energy demand with a corresponding increase in cost. Heat from losses increases device failure rates and reduces reliability. For renewable sources in remote locations reduced reliability is a major concern. Thermal strategies for safely dissipating heat increase the size and cost of a converter. All of these concerns can be mitigated by high efficiency converters. Accurate models of conduction losses are essential for accurate predictions of converter accuracy.

Modeling strategies for DC-DC converters fall into two main categories: state-space averaging [15, 16] and averaged-circuit modeling [17, 18]. Both analysis techniques assume no ripple in the average inductor current when modeling parasitic losses like inductor DC resistances. Because losses are caused by rms currents, not average currents, and the rms value of terminal currents is always greater than or equal to the average value, the no-ripple assumption underestimates the losses incurred. While the errors from the no-ripple assumption are relatively small in CCM where the average and rms currents are close in value, this approach severely underestimates losses in DCM where the rms current is significantly larger than the average current. In both cases, more accurate conduction loss models will provide better predictions of converter performance.

The principle of energy conversion [14] provides a powerful tool for accurately modeling conduction losses in DC-DC converters. The principle of energy conservation is used in averaged-circuit modeling to include non-zero ripple effects by replacing a parasitic element with an equivalent element. The equivalent element dissipates the same power when carrying the average current that the actual element dissipates when carrying the rms current. The equivalent element is used in place of the actual element for calculating DC transfer functions, small-signal transfer functions, and efficiencies.

Eq. (1) expresses the power relationship used in the principle of energy conservation and can be used to derive the equivalent averaged resistance (EAR) for any mode of operation by substituting in the correct relationship between average and rms currents. Note that parasitic elements modeled by an ideal DC voltage source, such as diode forward voltages, dissipate power only according to average currents and will not transform under this relationship.

$$I_{x,rms}^2 r_x = I_x^2 r_{x,EAR} \tag{1}$$

To apply the principle of energy conservation the relationship between the terminal average currents and rms currents must be known. For example, this relationship is given in CCM by (2), where the ripple factor *RF* is defined as the peak ripple amplitude divided by the average value (Fig. 2). The subscript '*x*' is either *L* for inductor, *S* for switch, or *D* for diode. From (1-2), the EAR in CCM is given by (3). This resistance allows the effect of non-zero ripple current to be more accurately modeled.

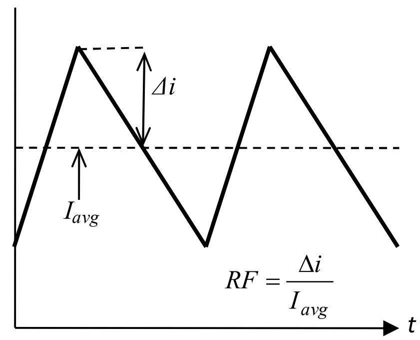


Fig. 2. Definition of ripple factor (RF).

$$I_{x,rms} = I_x \sqrt{1 + \frac{RF^2}{3}} \tag{2}$$

$$r_{x,EAR} = \left(1 + \frac{RF^2}{3}\right) r_x \tag{3}$$

The principle of energy conservation also allows parasitic resistances from one branch to be reflected into a common circuit branch and summed. Eq. (1) can again be used for this reflection by replacing r_x with the EAR of (3) and observing the relationships between rms and average terminal currents. For the boost and buck-boost converters operating in CCM the average currents are related by (4), and the rms currents are related by (5). Note that all rms quantities in CCM are defined in terms of the average inductor current. Henceforth actual resistances will be designated with lower-case subscripts (r_s, r_{ds}), and an EAR will be designated with upper-case subscripts (r_S, r_{DS}). Resistances reflected from branch A to branch B will be designated as $r_{A \to B}$.

$$I_L = \frac{1}{D} I_S = \frac{1}{1-D} I_D \tag{4}$$

$$I_{L,rms} = \sqrt{1+\frac{RF^2}{3}} I_L = \frac{1}{\sqrt{D}} I_{S,rms} = \frac{1}{\sqrt{1-D}} I_{D,rms} \quad (5)$$

The reflected EAR can be found from the substitution of (4) and (5) into (1). For example, the equivalent EAR of the switch on-resistance (r_S) in the inductor branch can be found by replacing r_s with r_S and $r_{s,EAR}$ with $r_{S \to L}$ in (1). The EAR of the switch on-resistance (r_S) reflected to the inductor branch ($r_{S \to L}$) is then found from (1) and (5) by inspection as Dr_S.

2.2 Per-unit system

The per-unit (pu) system allows circuits of different power levels and operating voltages to be compared easily. Transforming a circuit into an equivalent representation in the per-unit system changes the device parameters, electrical quantities, and losses from absolute magnitudes into relative magnitudes. All quantities of interest in a circuit are normalized according to the input power and voltage, which are defined as the base quantities and are taken as equal to 1.

Once the base quantities have been determined, all other voltages and currents of interest are divided by the base quantity to give a normalized value. These normalized values can be directly compared to normalized values from other pu circuits without regard to actual voltage and current values; this allows the performance and losses of different circuits to be compared by inspection.

2.3 Conduction losses in CCM converters

The single-switch converters that provide boosting of the input voltage are the boost converter and the buck-boost converter, and they are henceforth referred to collectively as the boosting converters. To demonstrate the use of the principle of energy conservation, the equivalent averaged parasitic elements will be determined for the boosting converters operating in CCM. The EARs will then be reflected into the diode branch. The following assumptions are made:

1. Diodes are modeled as a forward voltage V_f.
2. Switches are IGBTs and are modeled as a forward voltage V_f.
3. Inductor losses are modeled as a resistance r_l.
4. Switching and core losses are neglected.
5. Converters operate in continuous conduction mode (CCM).
6. The pu system is used with a normalized input voltage of 1 and a normalized input power of 1.

The EAR (r_L) of the inductor resistance r_l can be calculated from (1) and from the relationship between the average and rms current values in CCM given by (2) as shown in (3). Because the IGBT and diode are modeled as a DC voltage, they are not affected by ripple current; therefore, both elements are modeled with an equivalent averaged forward drop $V_F = V_f$. Now that the rms behavior has been encapsulated into averaged elements, the IGBT drop and inductor EAR can be reflected into the diode branch using the average current relationships. The calculations are shown in (6-7). $V_{F,S}$ represents the forward drop of the IGBT in the switch branch, and $V_{F,S \to D}$ represents this value reflected into the diode branch. Similarly, r_L represents the EAR of the inductor in the inductor branch, and $r_{L \to D}$ represents this value reflected into the diode branch.

$$V_{F,S} I_S = V_{F,S \to D} I_D \quad \to \quad V_{F,S \to D} = V_{F,S} \frac{I_S}{I_D} \quad \to \quad V_{F,S \to D} = V_{F,S} \frac{D}{1-D} \tag{6}$$

$$r_L I_L^2 = r_{L\to D} I_D^2 \quad \to \quad r_{L\to D} = r_L \frac{I_L^2}{I_D^2} \quad \to \quad r_{L\to D} = \frac{r_L}{(1-D)^2} \tag{7}$$

Fig. 3 shows the reflection of the equivalent averaged parasitic elements into the diode branch for a CCM boost converter. The portion of the circuit to the left of the dotted line is made up only of ideal elements, while the portion to the right (neglecting the capacitor) includes all parasitic elements in series with the load impedance. In a DC analysis the portion to the left of the dotted line is replaced with a CCM PWM switch model [17], and the inductor and capacitor are replaced by a short circuit and an open circuit, respectively. The voltage at the dotted line would then be given by the ideal gain of the boosting converter. This voltage can be treated generally as $M_{ideal}V_{in}$ in the boosting converters without regard to the converter type as shown in Fig. 4.

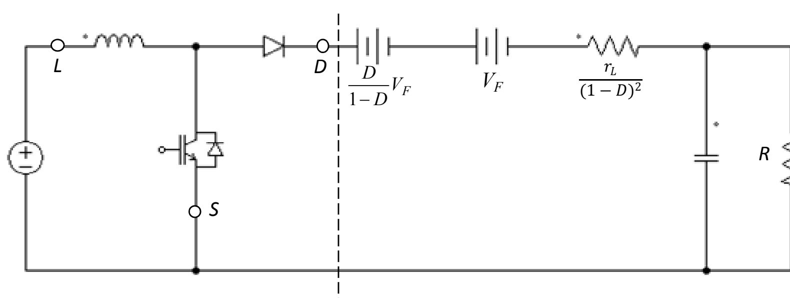


Fig. 3. CCM boost converter model with averaged parasitic elements reflected into diode branch.

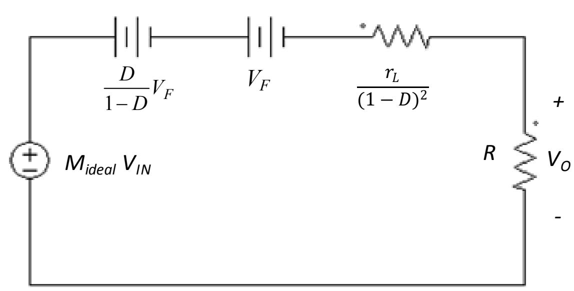


Fig. 4. Generalized CCM boosting converter DC model with parasitic losses.

2.4 Conduction losses in DCM converters

Converters operate in DCM when the inductor current falls to zero before the start of the next period. This mode of operation adds a third state where the current is zero in both the switch and the diode; additionally, the diode conduction interval becomes a function both of the switch conduction interval and of the load. The branch currents are shown in Fig. 5 where DT_S is the conduction interval of the switch and D_2T_S is the conduction interval of the diode. The inductor conduction interval is $(D+D_2)T_S$.

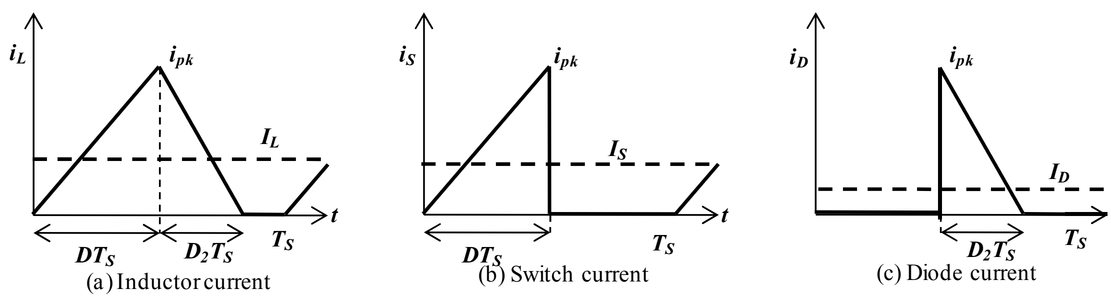


Fig. 5. Branch currents in DCM. All DCM current waveforms have triangular shapes.

The relationships between the average and rms values of each terminal current must be determined to calculate the parasitic EARs. Then the relationship between the average terminal currents must be determined to allow reflection of EARs into appropriate branches. The conduction losses in DCM boost and buck-boost converters will be modeled according to the following assumptions:

1. Converters operate in DCM.
2. Switches are MOSFETs and are modeled as a resistance r_{ds}.

3. MOSFET synchronous rectifiers are used in place of diodes and are modeled with a resistance r_{ds}.

4. Inductor losses are modeled as a resistance r_l.

Based on Fig. 5 the average and rms currents are given by (8) and (9), respectively. The EARs shown in (10) are obtained by substituting (8) and (9) into (1).

$$I_L = \frac{1}{2} i_{pk}(D + D_2) \quad I_S = \frac{1}{2} i_{pk} D \quad I_D = \frac{1}{2} i_{pk} D_2 \tag{8}$$

$$I_{Lrms} = i_{pk}\sqrt{\frac{D+D_2}{3}} \qquad I_{Srms} = i_{pk}\sqrt{\frac{D}{3}} \qquad I_{Drms} = i_{pk}\sqrt{\frac{D_2}{3}} \tag{9}$$

$$\begin{aligned} r_S &= \frac{4}{3}\frac{1}{D} r_{ds} \\ r_D &= \frac{4}{3}\frac{1}{D_2} r_{ds} \\ r_L &= \frac{4}{3}\frac{1}{D+D_2} r_l \end{aligned} \tag{10}$$

The next step is to reflect the switch and inductor EARs into the same branch, where they can be series-combined into a single parasitic resistance. Using (8) and (10) to reflect all resistances into the diode branch gives (after some algebra) the expression in (11). Using reasoning similar to the analysis of Section 2.3, the DCM boosting converters can be generally modeled as shown in Fig. 6. In Chapter IV a DCM modeling approach is presented that simplifies the expression of (11) into a form similar to (7).

$$r = \frac{4}{3}\frac{D+D_2}{D_2^2}(r_l + r_{ds}) \tag{11}$$

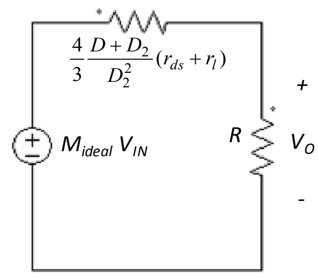


Fig. 6. Generalized DCM boosting converter DC model with parasitic losses.

2.5 Conclusions

In this chapter the importance of efficiency in renewable applications was discussed, and the principle of energy conservation was introduced to accurately model conduction losses. It was shown that increased losses from rms currents containing ripple can be modeled by using equivalent averaged parasitic elements. The relationships between average and rms terminal currents are developed for CCM and DCM converters, and the EARs are derived for both cases. Generalized models for the CCM and DCM converters considered in this work that incorporate parasitic elements are introduced.

CHAPTER III

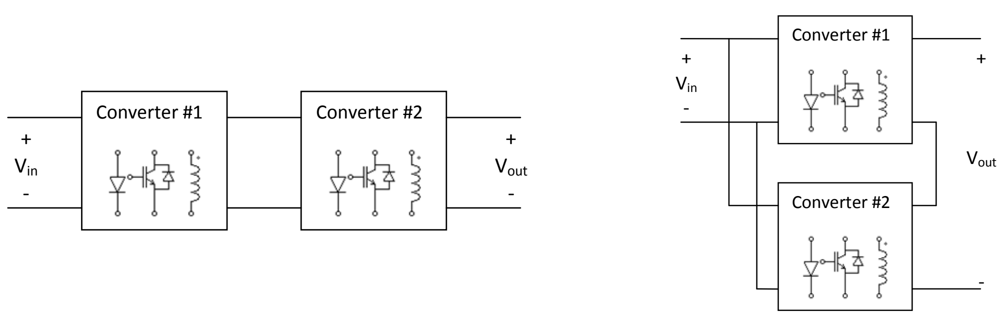
MULTIPLE MODULE CONVERTER SYSTEMS

3.1 Description

Renewable energy sources often require high gain DC-DC converters to interface with the electric grid. Traditionally high gain DC-DC conversion has required transformer-based conversion. In low power applications, where operating frequencies are not limited by switching losses, the transformer is much smaller than a line-frequency transformer. However, the large turns ratios required for high gain require complex winding arrangements, and the converter must withstand large transient spikes from imperfect coupling between windings. Transformers in high power converters with limited operating frequency are much larger and still experience the same complexity and transient issues. Many renewable applications do not require galvanic isolation, so eliminating the transformer is highly desirable from cost and size perspectives.

Multiple module DC-DC converters can provide high voltage gain and high efficiency while eliminating the transformer and its accompanying drawbacks. Converters can be arranged in cascade, where the output of the first converter becomes the input of the second (Fig. 7a), or in series, where the converter outputs are connected in series while the input source is shared (Fig. 7b). The multiple module approach is quite general, and many combinations of converter types and operating modes can be used. However, single-switch, single-inductor boosting converters (boost and buck-boost) are especially suited for multiple module operation due to their simplicity and low parts count. These converters also provide inherent voltage clamping; the voltage across the non-conducting semiconductor is clamped to a fixed voltage by the conducting semiconductor. The two types of single-switch boosting converters can be combined in three possible configurations for both series and cascade multiple module converters: boost/boost, buck-boost/buck-boost, and boost/buck-boost. These converters are referred to in this work as the boost, BB, and hybrid converters, respectively.

In this chapter expressions for gains and efficiencies are developed for the six converters introduced above, and the performances are compared. Parasitic losses are incorporated for better accuracy using the principle of energy conservation as discussed in Chapter II. Although the base analysis is independent of the type and operation mode of the base converters, for clarity the gain and efficiency expressions are extended to the specific examples of CCM converters using high-power IGBTs as the active switch and high-power diodes as the passive switch as in Section 2.3. Analysis will be extended to low-power DCM synchronous converters in Chapter IV.



(a) Cascade configuration (b) Series configuration

Fig. 7. Multiple module converter configurations. Each converter is a single-inductor, single-switch converter.

3.2 Cascade modeling

The cascade configuration shown in Fig. 7a connects the output of the first converter to the input of the second converter. Each converter processes the full input power and must be rated accordingly. The three combinations of cascade multiple module converters are shown in Fig. 8. Each converter is characterized by a gain *M*, an input power *P*, and an output voltage V_O. This general characterization allows the converter gains and efficiencies to be derived without specifying the type of each converter as discussed in Chapter II. The converter module connected directly to the input source is designated as converter 1.

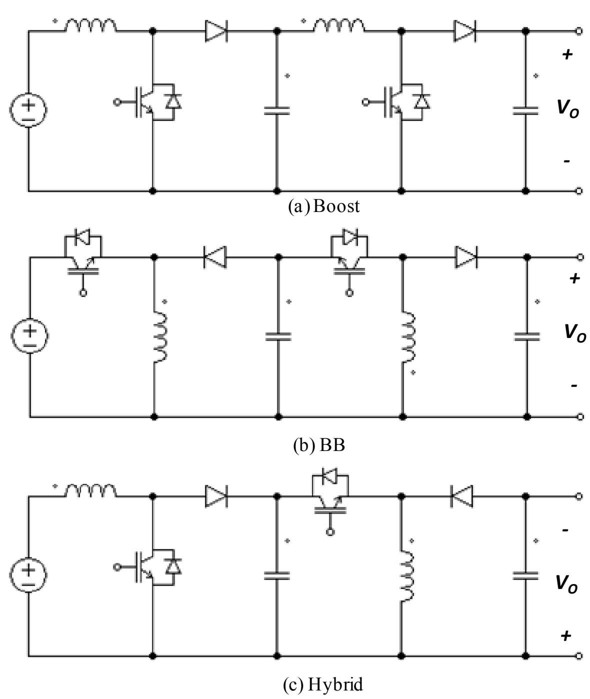


Fig. 8. Multiple module cascade converters.

To derive an equation for the total converter gain the loss elements are assumed equal on a pu basis for each converter. Converter 1 has a smaller pu output resistance ($R_{O1pu}=V_{O1}^2/P=M_1^2$) than Converter 2 ($R_{O2pu}=V_{O2}^2/P=M_1^2M_2^2$), so the parasitic resistance of the stage 1 has equal pu magnitude but smaller absolute magnitude than that of stage 2. It is also assumed that each converter is operated at the same duty cycle; while this assumption is not required, it simplifies the resulting equations for comparison purposes. Based on these assumptions the gain of the general cascade converters is given by (12), and the efficiency is given for the special case of CCM converters with IGBT switches and rectifier diodes in (13). M_i refers to ideal converter gain, η_i refers to the converter efficiency, $V_{F,pu}$ refers to the pu IGBT/diode drop, and $r_{L,pu}$ refers to the pu EAR of the inductor.

$$M_{casc} = M_1 M_2 \eta_1 \eta_2 \tag{12}$$

$$\eta_i = \left(1 - \frac{V_{F,pu}}{M_i(1-D)}\right)\left(\frac{1}{1+\frac{r_{L,pu}}{(1-D)^2}}\right) \tag{13}$$

This equation neglects the increase in load that is seen by the first converter due to second stage parasitic resistance, but from substitution of Fig. 4 into the circuits of Fig. 8 it can be shown that, for small parasitic elements, this effect is only significant for D very near 1. At large enough duty cycles the parasitic resistance of the second stage dominates the load resistance, and the efficiency of the first stage approaches 50% (assuming equal pu resistances for each stage) while the efficiency of the second stage approaches zero. For equal stage pu resistances of 0.001 and for D=0.9 there is less than 1% difference in stage efficiencies when neglecting this loading effect.

From (13), the combined IGBT/diode loss term is independent of duty cycle in CCM boost converters ($M_i=1/(1-D)$). In CCM BB converters ($M_i=D/(1-D)$) the combined IGBT/diode term is inversely dependent on D; however, for large gain ($D\approx1$) the losses are approximately independent of duty cycle. The pu forward voltages are often negligible in high power devices; for example, the Eupec DD400S33K2C 3.3kV 400A IGBT shows a worst-case forward drop of 3.5V [19]. For a base input voltage of 1000V the pu forward voltage is only 0.0035 (0.35%). In the remainder of the analysis the combined IGBT/diode term will be neglected.

If the ripple factors in each converter are assumed equal, the $\eta_1\eta_2$ term becomes η^2 for any combination of converters. If the losses from the forward drop V_F are neglected, (13) can be solved for D as in (14) for converters operating in CCM. This equation gives the maximum cascade duty cycle in CCM that can achieve a specified efficiency under a constraining parasitic resistance.

$$D_{\max,casc} = 1 - \sqrt{r_{L,pu}\,\frac{\eta^{1/2}}{1-\eta^{1/2}}} \qquad (14)$$

The maximum duty cycle for an efficiency of 95% (D_{max}) is calculated in Table 1 for different parasitic resistances and ripple factors using (14), where M_{tot} represents the overall gain of the CCM cascaded stages at this duty cycle. Small parasitic resistances and ripple factors extend the range of D over which high efficiencies can be achieved.

Table 1
Cascade CCM converters: maximum duty cycles and gains for 95% efficiency

$r_{L,pu}$	RF		Boost (Fig. 8a)	BB (Fig. 8b)	Hybrid (Fig. 8c)
		D_{max}		0.558	
0.005	20%	M_{tot}	4.627	1.443	2.584
		D_{max}		0.543	
0.005	50%	M_{tot}	4.328	1.278	2.352
		D_{max}		0.517	
0.005	80%	M_{tot}	3.865	1.032	1.997
		D_{max}		0.802	
0.001	20%	M_{tot}	23.137	14.9	18.567
		D_{max}		0.796	
0.001	50%	M_{tot}	21.642	13.705	17.222
		D_{max}		0.784	
0.001	80%	M_{tot}	19.323	11.874	15.145

The assumption in Table 1 of equal ripple factors for each CCM converter requires closer examination. Ripple factor equations are derived from inductor volt-seconds in (15), where f_s is the switching frequency. For $D\approx1$ the expressions are identical.

$$RF = \begin{cases} \dfrac{V_{IN}^2}{2 f_S L P} D & (boost) \\ \dfrac{V_{IN}^2}{2 f_S L P} D^2 & (buck-boost) \end{cases} \tag{15}$$

Converter 2 sees an input voltage that is M_1 times larger than converter 1, so the inductance of converter 2 must be M_1^2 times larger to maintain the same ripple factor. From an electrical perspective, the volt-seconds of the second inductor are increased by a factor of M_1 while the allowable change in current is reduced by the same factor; this requires the inductor to compensate for both factors and increase by M_1^2. In very high gain converters the inductance of converter 2 may be impractically large, and a compromise must be made between increased ripple factor and decreased inductor size. In this case the efficiency terms in (12) must be evaluated separately. Table 1 shows, however, that the effects of ripple factor decrease as parasitic resistances decrease. Converters with extremely small parasitic resistances can tolerate larger rms currents (large *RF*) because the $I_{rms}^2 r$ losses remain small; with sufficiently small parasitic resistances, increased rms currents due to large *RF* will not result in poor efficiency.

Cascade converters offer potential for large gains due to the multiplicative effect, but the efficiency losses compound quickly for the same reason. The entire input power is processed twice, and the losses quickly become a limiting factor with large parasitic resistances. Interleaving can be applied to reduce parasitic resistances and inductor sizes while increasing reliability. The individual modules can allow larger ripple factors for decreased inductor sizes, or the inductances can be held constant to increase overall efficiency. In either case the physical inductor size is reduced due to the smaller current magnitudes. The ability to interleave converters is a major strength of the multiple module approach, especially in high-power applications where reliability concerns often vastly outweigh cost concerns. If one interleaved module fails, the converter can operate at a reduced rating instead of failing entirely. The failed unit can be replaced without bringing the entire converter offline.

Cascade converters suffer from other practical issues. Converter 1 experiences intermediate voltage stresses and large current stresses while converter 2 experiences large voltage stresses and small current stresses. This will likely require the use of semiconductors with different ratings in the converters and will increase inventory requirements because of limited component interchangeability. Control is also difficult because of the interaction between converters, and the first converter must be operated at a lower bandwidth to maintain stability.

3.3 Series modeling

The series configuration shown in Fig. 7b connects the inputs of the converters in parallel and the outputs in series. Practically, only the series hybrid converter can be directly connected in this fashion. Fig. 9a shows a directly connected series boost converter where the output of the bottom converter is shorted to the input return. The series BB converter experiences the same effect when directly connected. This effect can be eliminated with the addition of a cascaded buck-boost converter between the input source and the bottom converter as shown in Fig. 9b. The additional converter acts as a voltage inverter and operates at $D \approx 0.5$ for M=-1. The efficiency loss of the cascaded converter is minimal (assuming negligible losses from forward drops) due to the small duty cycle; for example, the second term of (13) for a buck-boost converter evaluates to 99.5% for a 0.001 pu inductor resistance and 100% ripple factor operated at D=0.5.

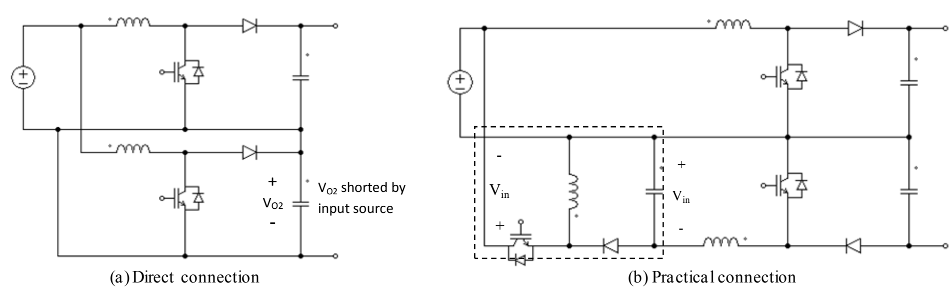


Fig. 9. Practical multiple module series boost converter. Additional BB converter in (b) inverts the input voltage.

The series BB and series hybrid converters are shown in Fig. 10. The series hybrid benefits from the inversion properties of the bottom buck-boost converter because the source neutral can be shared between both converters without an additional buck-boost converter. Each converter in the multiple module arrangement provides half the voltage gain and processes half the input power. The top converter is referred to as converter 1, and the bottom converter is referred to as converter 2. The additional inverting buck-boost converter in the series boost and series BB converters is neglected in the efficiency analysis. Each converter is characterized by a gain M, an input power P, and an output voltage V_O. This general characterization allows the converter gains and efficiencies to be derived without specifying the type of each converter as discussed in Section 2.3. The gain of the series converters is derived in (16) using the same assumptions found in Section 3.2, and the efficiency expression is expanded for the special case of CCM converters with IGBTs as active switches and diodes as passive switches in (17). The factoring of (16) for series hybrid converters requires that the diode efficiency terms are approximately equal ($D\approx1$); at lower duty cycles the efficiency of the buck-boost converter will be less, and this factoring will not be exact.

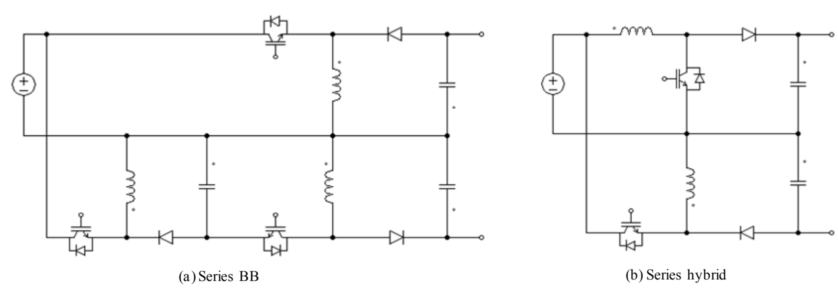


Fig. 10. Multiple module series BB and series hybrid converters.

$$M_{series} = (M_1 + M_2)\eta \tag{16}$$

$$\eta = \left(1 - \frac{V_{F,pu}}{M_i(1-D)}\right)\left(\frac{1}{1+\frac{r_{L,pu}}{(1-D)^2}}\right) \tag{17}$$

Neglecting forward drops, (17) is solved for D to determine the maximum duty cycle for a specified efficiency in (18) for CCM boosting converters. The maximum duty cycle for 95% efficiency is calculated in Table 2 for different parasitic resistances and ripple factors. Small parasitic resistances and ripple factors extend the duty cycle range over which high efficiency can be achieved. The ripple factor equations of (15) are also valid for series converters. The inductors, however, are (approximately) equal in each converter because the converters see the same input voltage.

$$D_{\max,series} = 1 - \sqrt{r_{L,pu}\frac{\eta}{1-\eta}} \tag{18}$$

Table 2
Series CCM converters: maximum duty cycles and gains for 95% efficiency

$r_{L,pu}$	RF		Boost (Fig. 9b)	BB (Fig. 10a)	Hybrid (Fig. 10b)
0.005	20%	D_{max}		0.690	
		M_{tot}	6.124	4.224	5.174
0.005	50%	D_{max}		0.679	
		M_{tot}	5.923	4.023	4.973
0.005	80%	D_{max}		0.66	
		M_{tot}	5.596	3.696	4.646
0.001	20%	D_{max}		0.861	
		M_{tot}	13.693	11.793	12.743
0.001	50%	D_{max}		0.857	
		M_{tot}	13.243	11.343	12.293
0.001	80%	D_{max}		0.848	
		M_{tot}	12.514	10.614	11.564

The gain of series converters is lower than the gain of cascade converters because of the additive effect, but series converters offer many advantages. Each converter processes only half the input power, and the total input power is only processed once (as opposed to twice in the cascade converters). The gains in efficiency allow a larger range of duty cycle operation. For example, data from Tables 1 and 2 for r=0.005 show that the maximum gain at 95% efficiency in the series converters is higher than that of the cascade converters due to the larger available range of duty cycles. This advantage disappears at lower parasitic resistances.

Semiconductors in series converters experience only half the total voltage stress, a decided advantage in high voltage converters where several switches must be combined in series to withstand the rated voltage. Semiconductors in both converters have identical ratings, reducing the inventory requirements. Control is decoupled, and independent controllers can be used. This independent operation allows a variation of boosting and control strategies beyond the basic operation described here. One possible control scheme in high power applications is based on a series hybrid converter. The boost converter would provide the majority of the gain at a low switching frequency to minimize switching losses. The buck-boost converter would operate at a higher switching frequency and fine tune the gain in response to fast load transients. This control scheme would offer fast transient response while minimizing switching losses. Another option involving the series hybrid is to operate the two converters at equal gains instead of equal duty cycles. The bottom buck-boost converter must be operated at a greater duty cycle, so the efficiency terms can no longer be factored as in (17); however, at large duty cycles and small parasitics the additional losses are negligible.

3.4 Simulations and performance comparison

The multiple module converters discussed in this chapter were simulated in the SIMPLIS simulator from Transim to verify the modeling assumptions. High power CCM converters with IGBT switches and rectifier diodes were chosen as the base converters. All component values were normalized with a base input voltage of 1 and a base input power of 1. IGBT and diode forward drops (V_F) of 0.0015 pu and an inductor DC resistance of 0.001 pu were specified for the parasitic elements. A 1 kHz switching frequency was selected to be consistent with the high power converters specified.

Inductances were chosen using (15) to limit *RF* to 50% at maximum duty cycle ($D \approx 1$) and were held constant for all duty cycles. Capacitances were chosen to limit output voltage ripple caused by inductor current ripple to 2% peak-to-peak at minimum duty cycle (50%) via (19); they were then held constant for all duty cycles. The pu circuit parameters are listed in Table 3. Note that these values are pu values and would be scaled based on the actual application; therefore, the relative magnitude of the parameters is more instructive than the absolute magnitude of the parameters.

$$C = \frac{\Delta Q/V}{\Delta V/V} = \frac{I_O D T_S/V}{\Delta V/V} = \frac{D T_S}{R(\Delta V/V)} \qquad (19)$$

Voltage and efficiency data was obtained with a parametric sweep of the duty cycle. To maintain a constant input power the pu output resistance (M_i^2) was defined as an expression evaluated at each sweep point. The parasitic resistances were then set as percentages of this value.

Table 3
Simulation circuit parameters for pu CCM converters

All Converters			Cascade (Fig. 8)	Series (Fig. 9b, 10)
f_S	1 kHz	L_1	1.2 mH	2.5 mH
$r_{L,\,pu}$	0.001	L_2	350 mH	2.5 mH
$V_{F,pu}$	0.0015	C_1	24 mF	100 uF
RF	50%	C_2	6 mF	100 uF

The simulated gains and efficiencies for the six multiple module high-power CCM converters are shown in Fig. 11. The converters within a class demonstrated similar efficiencies, so a restricted range is displayed to highlight the small differences.

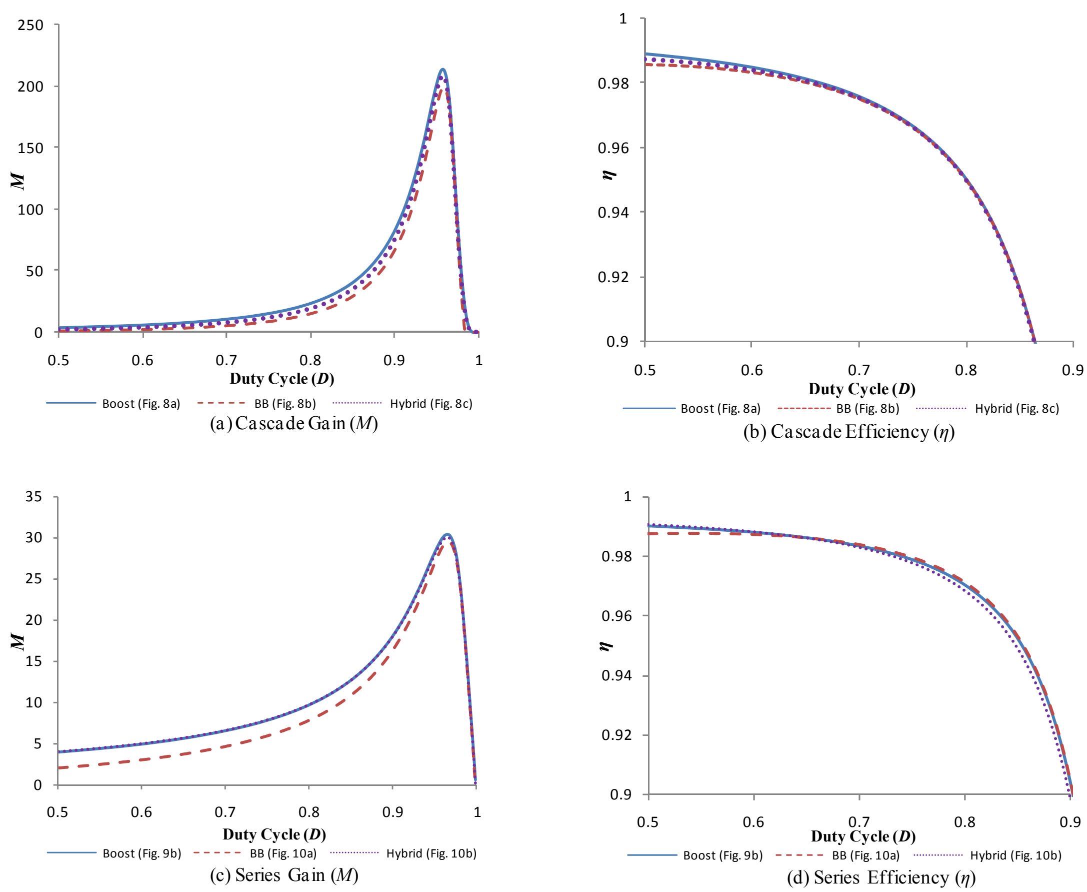


Fig. 11. Simulations results for pu CCM multiple module converters: gain and efficiency.

Fig. 11a shows that the three multiple module cascade converters have similar gains, especially at large duty cycles, and validates the factoring introduced in (13). The peak voltage gain is over 200, but the efficiency (Fig. 11b) at this duty cycle is low. The converters using at least one BB converter show a lower efficiency at small duty cycles due to the effect of diode forward voltage as discussed in Chapter II.

Fig. 11c shows the gains of the three multiple module series converters. Note that in the simulation of the series-hybrid converter the two converters are operated at equal gains instead of equal duty cycles. This configuration reaches the same gain as the series-boost with only a slight loss of efficiency (Fig. 11d). The fall-off in efficiency at large duty cycles is due to increased inductor losses from the larger buck-boost duty cycle required to maintain equal gains. The maximum gain for the series converters is approximately 30, or less than one-sixth of the cascade gain, but high efficiency is achieved over a larger range of duty cycles. As in the cascade converters the series-BB converter slightly underperforms in both gain and efficiency; however, it does offer source inversion. Table 4 shows excellent agreement between the simulation results and the calculations from Tables 1 and 2.

Table 4
Comparison of simulated and calculated results for maximum duty cycles in pu CCM converters at η=95%, *RF* =50%

	D_{max}, calc.	D_{max}, sim.	M, calc.	M, sim
Cascade Boost (Fig. 8a)	0.796	0.800	23.14	23.76
Cascade BB (Fig. 8b)	0.796	0.800	14.90	15.20
Cascade Hybrid (Fig. 8c)	0.796	0.800	18.57	19.00
Series Boost (Fig. 9b)	0.857	0.854	13.70	13.02
Series BB (Fig. 10a)	0.857	0.855	11.79	11.21
Series Hybrid (Fig. 10b)	0.857	0.854	13.70	13.02

3.5 Conclusions

In this chapter the multiple module approach was introduced. Large voltage gains can be achieved by connecting multiple single-switch DC-DC converters in cascade or in series. Models including parasitic conduction losses were presented for each multiple module configuration, and general transfer functions were derived without referencing the base type of the converters. It was shown that cascade connections provide high gain, but the efficiency falls off quickly at large duty cycles. Parasitic elements must be minimized in order to take full advantage of the gain potential of cascade converters. It was shown that series converters provide less gain, but high efficiency can be maintained over a wider range of duty cycles. Both configurations can provide increased reliability and reduced parasitic losses through interleaving. Gain and efficiency were verified with pu simulations of high-power CCM converters. The performance of the pu CCM multiple module converters is summarized in Table 5.

Table 5
Summary of pu CCM multiple module configurations

Configuration	M	Gain	Efficiency	L_2/L_1 ratio	Source Inversion?
Cascade boost (Fig. 8a)	$\left(\frac{1}{1-D}\right)^2 * \eta^2$	Highest	Low	M_1^2	No
Cascade BB (Fig. 8b)	$\left(-\frac{D}{1-D}\right)^2 * \eta^2$	High	Low	M_1^2	No
Cascade hybrid (Fig. 8c)	$-D\left(\frac{1}{1-D}\right)^2 * \eta^2$	Higher	Low	M_1^2	Yes
Series boost (Fig. 9b)	$\left(\frac{2}{1-D}\right) * \eta$	Medium	Highest	1	No
Series BB (Fig. 10a)	$\left(\frac{-2D}{1-D}\right) * \eta$	Lowest	Medium	1	Yes
Series hybrid (Fig. 10b) (equal gains)	$\left(\frac{2}{1-D_{boost}}\right) * \eta$	Medium	High	1	Either

CHAPTER IV

A DCM OPERATED HIGH GAIN CONVERTER FOR LOW POWER APPLICATIONS

4.1 Introduction

Renewable energy sources such as photovoltaic cells and fuel cells are low-voltage, high-current energy sources. The output characteristics follow a constant power curve where output voltage decreases as load current increases. The voltage output from a single cell is on the order of 1 to 2 volts, and modules are created by combining several cells in series. At the relatively low power levels of consumer modules (from a few watts to a few kilowatts), module output voltages are limited to a few tens of volts by size constraints and engineering challenges such as fuel and coolant distribution. The output voltage typically varies on a 2:1 scale from no-load to high-load, so power electronics converters are required to provide steady output voltages for single-phase inversion and grid connection. These converters face their greatest challenge at full load when the cell output voltage is at its minimum and the input current is at its maximum. At low power levels the pu semiconductor losses are larger than those found in high power converters, and high efficiency is difficult to reach.

Traditionally, high-frequency transformers have been used to provide large voltage gains at the cost of greater bulk, increased semiconductor stresses, and leakage spikes that must be managed. Low-power conventional single-switch converters operating in CCM cannot provide large voltage gains due to large pu parasitic elements that limit gain at large duty cycles. Additionally, converters in these power ranges are normally operated at high switching frequencies to reduce component sizes. This restricts the maximum duty cycle so that semiconductors have enough time to turn off fully. These considerations eliminate CCM single-switch transformerless converters from consideration.

Discontinuous conduction mode (DCM) exhibits a voltage gain characteristic with a steeper slope at low duty cycles, allowing large gains to be reached at small duty cycles. Inductor sizes decrease, which improves transient response, but the larger peak currents cause increased conduction losses. Careful optimization is needed to balance the efficiency gains from reduced duty cycles and the efficiency losses from increased peak currents. Further efficiency gains are made possible by the low output voltages in single-phase applications; lower voltages allow rectifier diodes to be replaced with MOSFET synchronous rectifiers. Reverse recovery effects are eliminated, and conduction losses now depend on the MOSFET on-resistance instead of a constant voltage drop. DCM also has the beneficial effect of turning off the output rectifier at zero current and turning on the active switch at zero current, reducing switching losses. A careful design can manage the conduction losses while benefitting from reduced switching losses, and high efficiencies can be achieved at low power levels.

This chapter investigates the use of a multiple module DCM-operated series hybrid converter (Fig. 12) to interface low power, low voltage renewable sources to the grid. The converter will provide the DC link necessary for single-phase inversion. A complete DC model is presented that uses the principle of energy conservation to accurately model parasitic effects, and a design procedure is developed. Modeling will be verified through simulation and an experimental prototype of a 200W, 24V-to-200V converter.

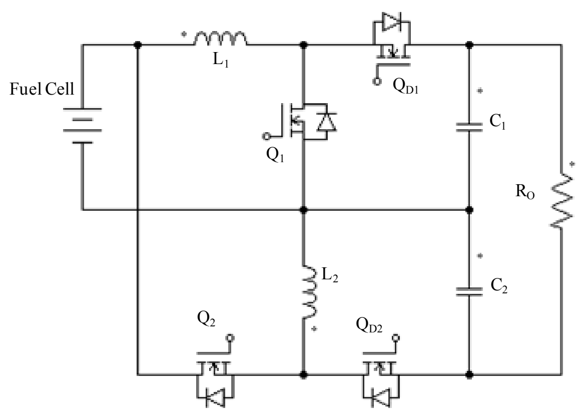


Fig. 12. DCM series hybrid synchronous converter.

4.2 DCM modeling

In DCM the inductor current falls to zero before the end of the switching period, introducing a third state of circuit operation. Many different DCM modeling approaches have been presented, including state-space methods [16], sampled data methods, and circuit-averaging methods [18]; the methods are summarized and compared by Sun in [20], and an averaged model including the dependency of the diode conduction time D_2 on switch duty ratio D_1 (D in this work) is presented. In [21] Reatti introduces a variation of the model of [20] using only controlled current sources which appears functionally identical to Sun's model. This current-controlled current source (CCCS) model lends itself well to the principle of energy conservation due to its explicitly defined terminal currents.

The CCCS model is shown in Fig. 13. The switch and diode are replaced by this three-terminal model with connections made at the location of the switch (*S*), diode (*D*), and inductor (*L*). The peak current can be expressed in terms of terminal voltages from inductor volt-seconds as in (20). T_S is the switching period, and V_{xy} is the voltage between terminals *x* and *y* where each terminal is *S*, *D*, or *L*. The relationship in (20) is approximate because it neglects the reduction in inductor volt-seconds from parasitic element drops, but the effects of these elements are negligible in a well-designed converter. The parameter μ is defined in (21) and represents the ratio of the switch conduction interval to the inductor conduction interval. It is the DCM analog to *D*.

$$\boldsymbol{i_{pk}} = \begin{cases} \frac{DT_S}{L} V_{SL} \\ \frac{D_2 T_S}{L} V_{LD} \end{cases} \tag{20}$$

$$\boldsymbol{\mu} = \frac{D}{D+D_2} = \frac{1}{1+\frac{V_{SL}}{V_{LD}}} \tag{21}$$

D_2 can be determined from the equation for I_L in (8) and from (20) as shown in (22). This result is identical to the duty cycle constraint given in [20]. Substituting (22) into (21) results in an equation for μ that is dependent on the switch on-time, circuit parameters, and terminal voltages and currents (23). The parameter *K* [22] is a direct measure of the "depth" of DCM operation and is defined as 2*L*/*RT*. The terminal current expressions in Fig. 13 are obtained by substituting (20) and (23) into (8).

$$\boldsymbol{D_2} = \frac{2LI_L}{DT_S V_{SL}} - D = \frac{KRI_L}{DV_{SL}} - D \tag{22}$$

$$\mu = \frac{D^2 T_S}{2L} \frac{V_{SL}}{I_L} = \frac{D^2}{KR} \frac{V_{SL}}{I_L} \tag{23}$$

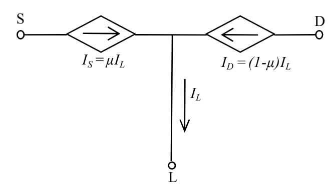


Fig. 13. Current-controlled current source model of PWM switch in DCM.

The definition of μ in (21) can be used to simplify the combined EARs in synchronous DCM converters given in (11) in Section 2.4. For consistency with the previous references, the combined resistance is reflected into the inductor branch by multiplying by $(1-\mu)^2$ and using (21) to eliminate D_2, resulting in (24). This equation for r is the DCM analog of r_L in (7) for synchronous converters.

$$r = \frac{4}{3} \frac{\mu}{D} (r_l + r_{ds}) \tag{24}$$

The PWM switch model of Fig. 13 is substituted point for point into the DC models for a boost converter and a buck-boost converter (Fig. 14) to derive the voltage transfer characteristic in the presence of parasitic resistances. The output voltage of the boost converter (Fig.14a) is given by a voltage divider across (V_{DL}+V_{LS}); the polarity is reversed because the current sources are oriented opposite to the original model. Similarly, the output voltage of the buck-boost converter (Fig. 14b) is given by a voltage divider across V_{LD}. After using (21) to express V_{LD} as a function of V_{SL} (the input source in both converters) and μ, the gain and efficiency of each converter can be written generally as (25) and (26). $M_{CCM}(D\rightarrow\mu)$ represents the ideal CCM gain equation of each converter with D replaced by μ, and η is the efficiency.

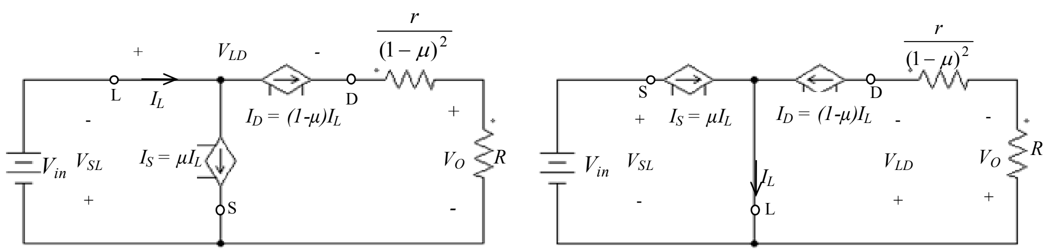


Fig. 14. DC averaged models for DCM synchronous boosting converters.

$$M = M_{CCM}(D \rightarrow \mu)\eta \tag{25}$$

$$\eta = \frac{1}{1+\frac{r}{R(1-\mu)^2}} = \frac{1}{1+\frac{r_{pu}}{(1-\mu)^2}} \tag{26}$$

The gain and efficiency equations above are given in terms of μ, which is in turn given in terms of terminal voltages and currents. These quantities can be eliminated by expressing the ratio V_{SL}/I_L in (23) as a ratio of the output voltage to the output current for each circuit. For both circuits I_L can be written as $I_D/(1\text{-}\mu)$ from Fig. 13. In the boost converter V_{SL} is the input voltage and can be written as $(1\text{-}\mu)V_{DS}$ where $(1\text{-}\mu)$ equals the inverse of the ideal gain and V_{DS} is the output voltage. The ratio of the output voltage to the output current is equal to R. The definition of μ in a boost converter is then given by (27). This is a quadratic equation in μ that can be easily solved. The procedure is completely analogous in the buck-boost converter. The equations for μ and M in DCM converters are summarized in Table 6.

$$\boldsymbol{\mu_{boost} = \frac{D^2}{KR}(1 - \mu_{boost})^2 R} \tag{27}$$

Table 6
Gain and efficiency equations for DCM synchronous boosting converters

	Boost Converter (Fig. 14a)	Buck-Boost Converter (Fig. 14b)
M(μ)	$\boldsymbol{\frac{1}{1-\mu}\eta}$	$\boldsymbol{\frac{\mu}{1-\mu}\eta}$
μ(D,K)	$\boldsymbol{1 + \frac{K}{2D^2}\left(1 - \sqrt{1 + \frac{4D^2}{K}}\right)}$	$\boldsymbol{\frac{1 - \sqrt{\frac{K}{D^2}}}{1 - \frac{K}{D^2}}}$
M(D,K)	$\boldsymbol{\frac{1 + \sqrt{1 + \frac{4D^2}{K}}}{2}\eta}$	$\boldsymbol{\frac{D}{\sqrt{K}}\eta}$
η	$\boldsymbol{\frac{1}{1 + \frac{r_{pu}}{(1-\mu)^2}} = \frac{1}{1 + \frac{\frac{4}{3}\frac{\mu}{D}(r_l + r_{ds})}{R(1-\mu)^2}}}$	

4.3 Conduction losses in DCM

From Table 6 it is apparent that conduction losses in DCM converters depend on the parasitic resistances and on μ, which is a function of duty cycle, circuit parameters, and load. Components must be selected carefully to maximize efficiency. The parameter K provides the design flexibility needed to achieve a specified performance with given components.

K provides an indicator of the depth of discontinuous operation. Its critical value derives from the boundary between CCM and DCM operation and is determined by setting the inductor current ripple amplitude equal to the inductor average current. Because the inductor current ripple magnitude and average inductor current values are the same for boost and buck-boost converters, the equation for both is given by (28). The duty cycle-dependent terms are then separated from the circuit parameter terms to provide a definition for the critical value of *K* in (29), where *M* is the ideal CCM gain expression and D_{CCM} is the duty cycle needed to reach *M* in CCM. This equation assumes no losses; i.e., *M* is given by the ideal gain equation in CCM.

$$\frac{V_{in}DT_S}{2L} = \frac{V}{R(1-D)} \tag{28}$$

$$K_{crit} = \frac{2L}{RT_S} = \frac{D(1-D)}{M} \tag{29}$$

Circuits operating with a *K* less than the critical value will operate in DCM, while circuits operating with a *K* larger than the critical value will operate in CCM. From the definition of *K* it is apparent that, for the same load and switching frequency, decreasing *L* will result in deeper DCM operation. This corresponds to an increasing peak inductor current and an increasing interval of zero inductor current. It is also apparent from Table 6 that a smaller value of *K* will result in a smaller duty cycle required to meet the same voltage gain. Reducing *K* then has opposing effects on a circuit: the smaller conduction time intervals reduce conduction losses, but the higher peak currents increase conduction losses. It is therefore of great practical importance to determine the optimal value of *K* for high efficiency operation.

Inductor choice also provides some design flexibility in meeting efficiency goals. Practical power inductors are specified with a quality factor *Q* defined as the ratio of the ac impedance ωL to the effective DC resistance r_l. For a given *Q,* large inductances result in large DC resistances. While it can be shown that the efficiency terms in synchronous CCM converters and synchronous DCM converters have the same form

($r_{EAR}/(1\text{-}D)^2$), the large inductances required for CCM operation will result in larger DC resistances and lower efficiencies. The parameter K can be rewritten as (30) below.

$$\boldsymbol{K = \frac{2Lf_S}{R} = \frac{\omega L}{\pi R} = \frac{Qr_l}{\pi R} = \frac{Q}{\pi} r_{l,pu}} \tag{30}$$

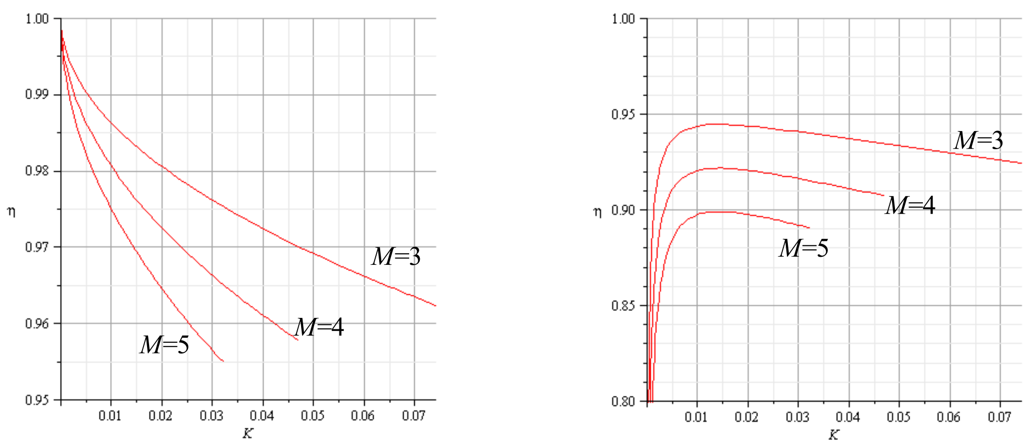
From (30) it is apparent that, for a given Q technology and circuit operating point, reducing K reduces the effective DC resistance. This would also reduce the duty cycle and semiconductor conduction intervals for a given gain. If semiconductor resistance is neglected, maximum efficiency will occur at minimum K/minimum r_l. If semiconductor resistance is not neglected, however, then additional losses will be incurred in the switches at small values of K from increased peak currents. It is expected that the efficiency benefits of decreasing the duty cycle will eventually be offset by the increasing losses from small K and increased peak currents.

The analytic method to determine the optimal K would begin by substituting the equations for μ into the overall gain equations of Table 6 to express M as a function only of D and K. By treating M as a constant and solving the resulting gain equation for D, an expression for duty cycle in terms of K (i.e., Q and r_l) for a given M can be derived. This equation can be used to eliminate D from the efficiency equations of Table 6, leaving efficiency as a function only of K and a constant M. This equation could then be maximized with respect to K by differentiating, setting the result equal to 0, and solving for the optimal K. However, the multiple radicals in the expressions make determining a usable closed-form solution difficult even with a symbolic solver.

Alternatively, several efficiency equations were plotted in Maple over a varying K for a given Q and M; varying K in this case corresponds to varying L and r_l

simultaneously. From Table 6, (24), and (30), the total equivalent averaged per-unit parasitic resistance r can be written as in (31). The Maple software package is used with Table 6 and (31) to eliminate D from the efficiency equations (leaving it as a function of K and M only) and to plot efficiency vs. K for some numerical values of M, r_{ds}, and Q in Fig. 15 below. The range of K is constrained to lie below its critical value to maintain DCM operation.

$$\boldsymbol{r_{pu} = \frac{4}{3}\frac{\mu(K,D)}{DR}\left(r_{ds} + \frac{\pi K}{Q}\right)} \tag{31}$$



(a) r_{ds}=0, Q=75 (b) r_{ds}=1 mΩ, Q=75

Fig. 15. Determining optimal K for maximum efficiency in DCM synchronous operation.

Fig. 15a shows that, for zero semiconductor resistance, efficiency improves as K (and therefore r_l) is minimized. Figure 15b, however, shows that for non-zero semiconductor resistance the efficiency increases with decreasing K up to a maximum and falls off extremely quickly afterward. This sharp slope is due to the rapidly increasing losses in the semiconductors from increasing peak currents. Maple was used to determine the value of K at the maximum of each of the curves of Fig. 15b and to substitute this value back into (30) to determine the optimal r_l. For each curve the optimal r_l was found to be equal to the chosen r_{ds}. The optimal K at a specified gain then depends on device design parameters Q and r_{ds}; the inductance L can later be determined from Q and the choice of switching frequency. Increasing efficiency requires either a better Q technology, a lower resistance MOSFET, or both.

4.4 DCM design procedure

Although it has been shown that an optimal K can be selected as a function of Q and r_{ds}, no guidelines for selecting semiconductors (r_{ds}) and inductors have been given. The two fundamental design concerns of a power supply are gain and efficiency, and the components should be selected to meet these specs. Therefore, constraints are developed from the gain and efficiency equations of Table 6. The key is to determine the value of μ (DCM analog of D) at which the converter must be operated to meet the specifications.

The first constraining equation is obtained by from the overall gain equation in the first row of Table 6. The efficiency η can be eliminated from this equation using the last row of Table 6, leaving M as a function of μ and r_{pu}. This equation can be solved for μ as shown in (32) for the DCM boost and BB converters. This equation gives the range of μ that can meet the gain requirement M without regard to efficiency.

$$\boldsymbol{\mu_{gain}} = \begin{cases} \frac{1}{2M}\left(2M - 1 - \sqrt{1 - 4M^2 r_{pu}}\right) & (\boldsymbol{boost}) \\ \frac{1}{2(M+1)}\left(2(M+1) - 1 - \sqrt{1 - 4M(M+1) r_{pu}}\right) & (\boldsymbol{BB}) \end{cases} \tag{32}$$

The second constraining equation is obtained by solving the efficiency equation in the last row of Table 6 directly for μ (33). This equation has the same form as (18) in

Chapter III, which gave the maximum CCM series duty cycle for a desired efficiency. Eq. (33) is valid for both the DCM boost converter and the DCM BB converter.

$$\boldsymbol{\mu_\eta = 1 - \sqrt{r_{pu}\frac{\eta}{1-\eta}}} \tag{33}$$

Figure 16 shows the plot of (32) and (33) for a DCM boost converter with a gain of 4.1667 and an efficiency of 90%. The red line represents the μ required to meet the gain equation; any point exactly on this line will satisfy the specified gain. The blue line represents the 90% boundary of the efficiency region; any (μ, r_{pu}) pair to the left of this line will meet or exceed the efficiency specification. The intersection of the two lines represents the maximum pu EAR that will allow both specifications to be met. This value of r_{pu} can be substituted into the gain equations of Table 6 to determine μ, and the designer can estimate the ratio of μ to D to estimate the maximum allowable r_{ds}.

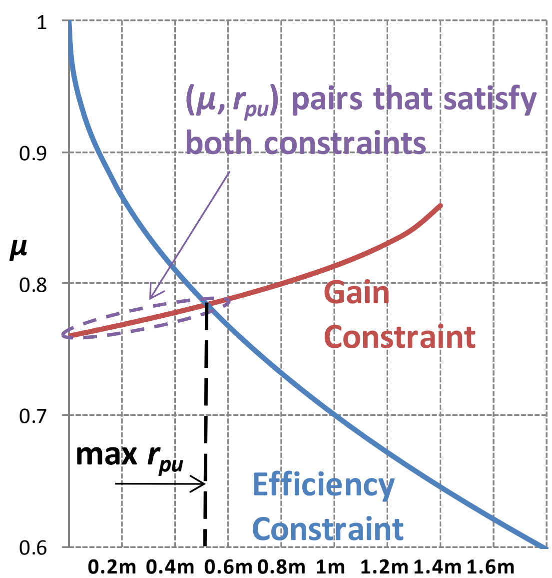


Fig. 16. Determining operating boundaries of a DCM synchronous boost converter.

The full design procedure is detailed below.

1. *Determine maximum allowable conduction resistances*

   Use the graphical approach based on Table 6 equations. Assume a μ-to-D ratio based on the gain and efficiency specification.

2. *Select MOSFET*

   Choose a MOSFET with an r_{ds} that makes up half of the allowable resistance.

3. *Determine critical K values to maintain DCM operation from (29).*

4. *Check actual K to ensure DCM operation from (30).*

   Use the Q of the available technology and an inductor resistance equal to r_{ds}.

5. *Determine steady state D from Table 6 equations*

   D can be determined from the equation for μ using K from Step 4.

6. *Determine μ using Table 6 and verify the assumption of Step 1*

   If the actual μ-to-D ratio is not equal to the assumption, Steps 1-6 should be iterated.

7. *Select inductance and switching frequency*

   Use the definition of Q and the chosen r_l.

8. *Select output capacitor*

   Assuming that output ripple is determined almost entirely by the ESR of the output capacitor, a capacitor can be chosen according to (34).

$$\boldsymbol{\Delta V = ESR(i_{pk}) = ESR\frac{V_{in}DT_S}{L}} \tag{34}$$

   The capacitance must be large enough that the voltage rise from the charging interval D_2 is much smaller than the ESR rise, which is usually the case with an electrolytic bulk capacitor. For a low-ESR capacitor, (35) is derived from charge balance and should be used instead. Capacitor rms current rating must also be considered.

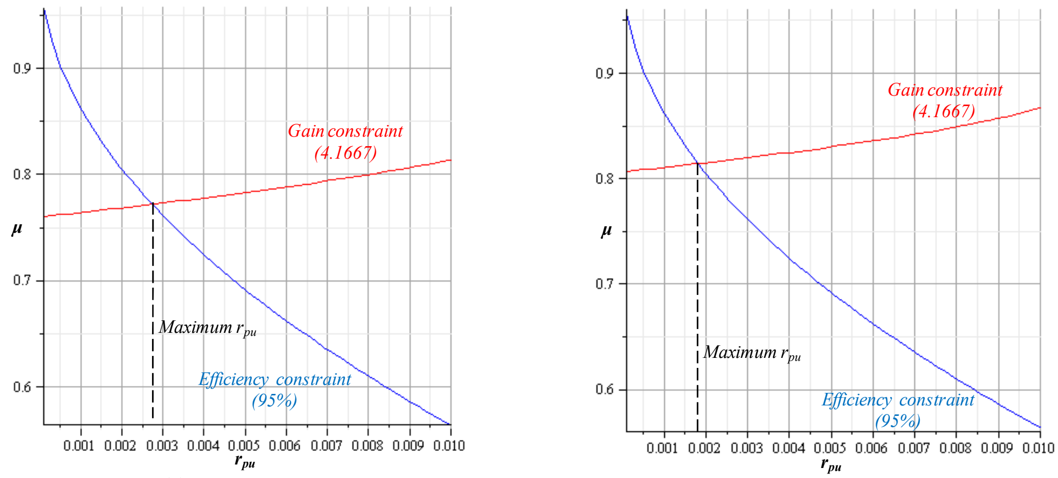
$$\boldsymbol{C = \frac{\Delta Q}{\Delta V} = \frac{\int_0^{D_2}\left(i_{pk} - \frac{V_{off}}{L}t\right)dt}{\Delta V}} \tag{35}$$

4.5 Design example

A design example will now be presented to illustrate the procedure with a multiple module series hybrid DCM converter. This converter could be used as the DC link to a quasi-square wave inverter for small portable applications. The converter specifications are listed in Table 7. Each converter will be designed to provide half the voltage gain (*M*=4.16667), so the converters will be operated at independent duty cycles. The duty cycle of the buck-boost converter will therefore be larger, and the efficiency will be lower. Each converter can be designed independently.

Table 7
Design specifications for DCM series hybrid synchronous converter (Fig. 12)

Input voltage	24 V	Output power	200 W
Output voltage	200 V	Efficiency	95%
Voltage gain	8.3333	Inductor *Q*	75
Voltage ripple	2% peak-to-peak		



(a) DCM Boost (b) DCM BB

Fig. 17. Determining maximum allowable MOSFET resistances for design example. The MOSFET will be selected to meet the stricter BB converter requirements.

Fig. 17 graphically demonstrates Step 1 for the specifications in Table 7. The blue lines represent the boundary of the μ-region where efficiency is greater than or equal to 95%, and the red lines represent the set of μ-values that are sufficient to meet the gain specifications. Note that the maximum r_{pu} represents the EAR of the sum of r_l and r_{ds}, which should be equal for optimal efficiency. The calculated maximum r_{pu} values are shown in Table 8. The maximum allowable r_{ds} is then based on an initial guess of 2 for the μ-to-D ratio in (24). IRFB4127 MOSFETs with an r_{ds} of 23 mΩ were chosen to meet the requirements for both converters with some margin for error.

To ensure DCM operation the critical K values are evaluated using (29). The critical K values are 0.0401 for the boost converter and 0.0345 for the BB converter. Using (30) with an inductor Q of 75 and an inductor resistance of 23 mΩ gives an operating K of 0.0055, which ensures DCM at full load in both converters. The required duty cycle D can now be determined from the equations for $M(D,K)$ and $\mu(D,K)$ that are given in Table 6.

The results for K, D, μ , and μ-to-D ratios are shown in Table 8. Note that the initial guess for the μ-to-D ratio in Step 2 was incorrect. The procedure is iterated using the correct μ-to-D ratios, and the new values of r_{ds} are also shown in Table 8. Because the on-resistance of the IRFB4127 MOSFET is less than the new maximum values, no other quantities need to be updated. After arbitrarily choosing a switching frequency of 100 kHz, the inductance is determined from the definition of Q (with r_l = 23 mΩ). The peak currents are then calculated as shown in (20). Assuming electrolytic output capacitors, the required ESR is then determined from (34) and shown in Table 8. The rms capacitor current can be determined from the difference between the diode rms current and the average output current. The diode conduction interval can be determined from (22).

Table 8
Procedure to determine circuit parameters for design example

	Try 1		Try 2	
	Boost	BB	Boost	BB
Max r_{pu}	0.0027	0.0018	0.0027	0.0018
μ/D guess	**2**	**2**	**2.8**	**2.6**
Max r_{ds}, r_l	51 mΩ	34 mΩ	37 mΩ	26 mΩ
Selected r_{ds}, r_l	23 mΩ	23 mΩ	23 mΩ	23 mΩ
K	0.0055	0.0055	0.0055	0.0055
D	0.27	0.31	0.27	0.31
μ	0.76	0.81	0.76	0.81
μ/D	**2.8**	**2.6**	**2.8**	**2.6**
choose f_S			100 kHz	
L			2.7 µH	
i_{pk}			25 A	28 A
Max ESR			70 mΩ	
D_2			0.077	0.072
$I_{C,rms}$			4 A	4.2 A

4.5.1 Simulation results

The multiple module series hybrid converter was simulated (closed-loop) in SIMPLIS, a piecewise-linear simulator from Transim designed for accurate simulation of switching circuits. The inductor for each circuit was 2.7 μH with 23 mΩ DC resistance. Three 330 μF electrolytic capacitors (Nichicon UCS2D331MHD) were paralleled at each output to withstand the ripple current and lower the ESR to 267 mΩ. This ESR is almost four times the permissible limit, so the output voltage will not meet the specifications. To reduce ripple further, the gating signals of the converters will be interleaved by 180 degrees. The peaks due to ESR will no longer coincide, and the overall ripple will be cut in half. MOSFETs were initially simulated at Level 0, which includes conduction losses but neglects switching losses. The losses in the converter are tabulated in Table 9, and the output voltage waveforms are shown in Fig. 18.

Table 9
Summary of losses in simulated DCM converter (Fig. 12) with electrolytic capacitors

Loss Element	Boost, Lvl 0	BB, Lvl 0	Boost, Lvl 2	BB, Lvl 2
Inductor	1.68 W	2.38 W	1.79 W	2.56 W
Active MOSFET	1.33 W	1.99 W	3.00 W	4.67 W
Synchronous MOSFET	0.41 W	0.45 W	0.85 W	1.06 W
Capacitor ESR	4.05 W	4.68 W	4.25 W	4.88 W
TOTAL	**7.47 W**	**9.50 W**	**9.89 W**	**13.2 W**

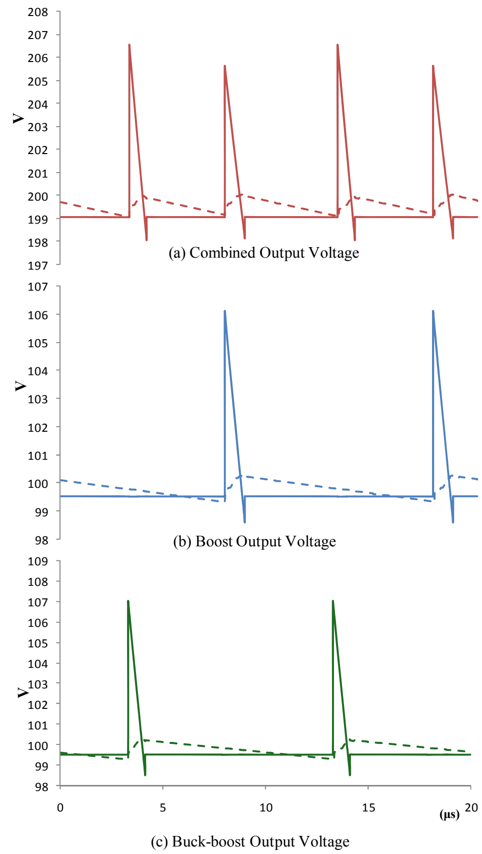


Fig. 18. DCM synchronous series hybrid (Fig. 12) simulated output voltages (Level 0). Solid lines are with high-ESR electrolytic output capacitors; dashed lines are with low-ESR film output caps. Note that the interleaved gating signals have doubled the output voltage frequency.

Table 9 shows that the Level 0 losses are dominated by the ESR, which was not accounted for in the analysis; the overall efficiency is 92% (neglecting switching losses). However, the sum of the inductor, active switch, and synchronous switch losses were kept to less than 5 W per converter. A reduction in capacitor ESR will greatly increase the efficiency while reducing the peaking in the output voltage response. The simulation was repeated with the output capacitance replaced by a 10 μF capacitor with an ESR of 10 mΩ (similar to EPCOS B23676G4106). Capacitor ESR losses were reduced to less than 200 mW each, and the overall simulated efficiency at Level 0 increased to 96.0%.

A second SIMPLIS simulation was run using the Level 2 MOSFET model. This model includes the effects of the MOSFET parasitic capacitances, so switching losses are included. Switching losses occur from active switch turn-off, synchronous switch turn-on, and capacitive losses from the drain-source capacitances. When the inductor current falls to zero, the DC voltage across the inductor disappears. The charge on the MOSFET drain-source capacitances causes oscillations as the voltage at the switch node (connection of switch, diode, and inductor) settles to a third and final value (the supply voltage in the boost converter or ground in the BB converter). This situation is shown in Fig. 19. The energy in these oscillations is absorbed by parasitic resistances, increasing switching loss. From Table 9 it can be seen that the losses in the MOSFETs more than double when switching losses are considered in Level 2 while inductor and ESR losses remain relatively constant. The overall efficiency reduces to 89.8%. Replacing the electrolytic output capacitors with metal-film capacitors eliminates almost all of the ESR losses, and the overall efficiency increases to 93.7%. Switching losses can be reduced by switching at a lower frequency.

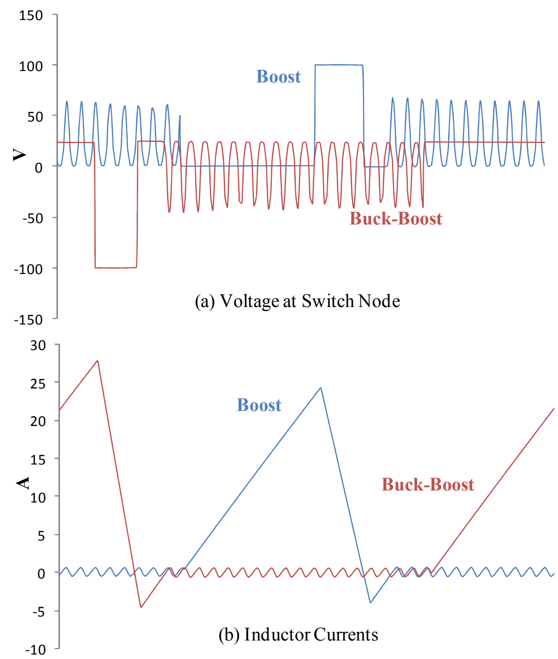


Fig. 19. Simulated oscillation at switch node from MOSFET drain-source capacitance (Level 2).

4.5.2 Experimental results

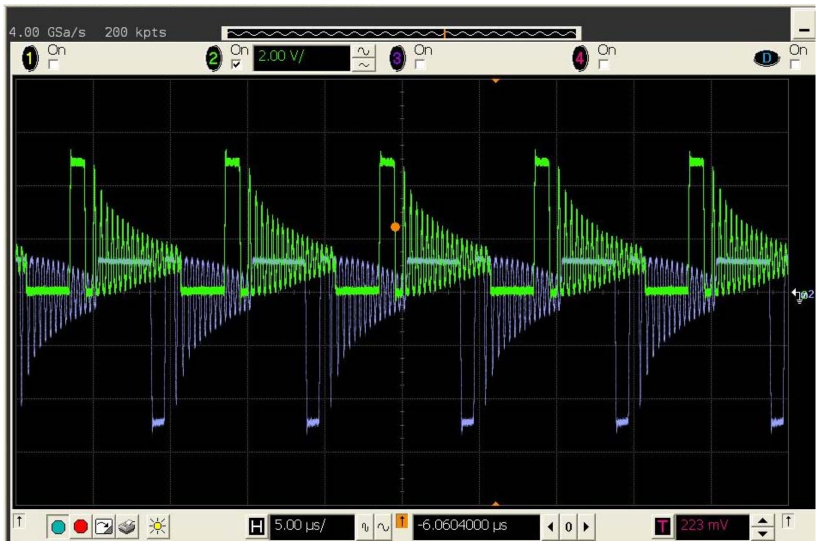
Next an experimental prototype was built to verify the simulation results. The IRFB4127 MOSFETs were mounted on an Aavid Thermalloy 533522B02552G dual TO-220 heat sink. The inductor was constructed from 7 turns of 6mm^2 wire on a 55256-A2 core from Magnetics, Inc. for an inductance of 2.7 μH. The measured inductor Q at 100 kHz was 60, resulting in an effective r_l of 28 mΩ. In order to handle the high current ripple at both the input and the output (3) 330 μF Nichicon UCS2D331MHD electrolytic capacitors were paralleled at input and output for a total capacitance of 1 mF (approximate ESR of 268 mΩ). A 100 nF ceramic capacitor and a 1 μF polypropylene film EMI suppression capacitor were added at input and output to improve the high frequency decoupling. The boost and buck-boost gating signals were interleaved at 180^o to reduce the output voltage ripple caused by the large ESR of the output capacitors.

The active gate signals were provided by a Texas Instruments TMS320F2812 fixed-point DSP mounted on a Zwickau adapter board. An HCPL-2231 optocoupler and a Zetex ZXGD3001TA gate driver were used to drive the boost active MOSFET from the DSP gating signal, and a custom off-board transformer isolated gate driver was used to drive the BB active MOSFET. Both synchronous MOSFETs were driven with an IR1167 synchronous gate driver that switched the MOSFETs based on V_{DS} sensing instead of gating signals. As the active switch turns off and the inductor current begins to flow through the body diode of the synchronous switch, the chip senses the negative drain-source voltage and triggers the gate of the synchronous switch. As the inductor current falls and the drain-source voltage approaches zero, the chip turns the gate off.

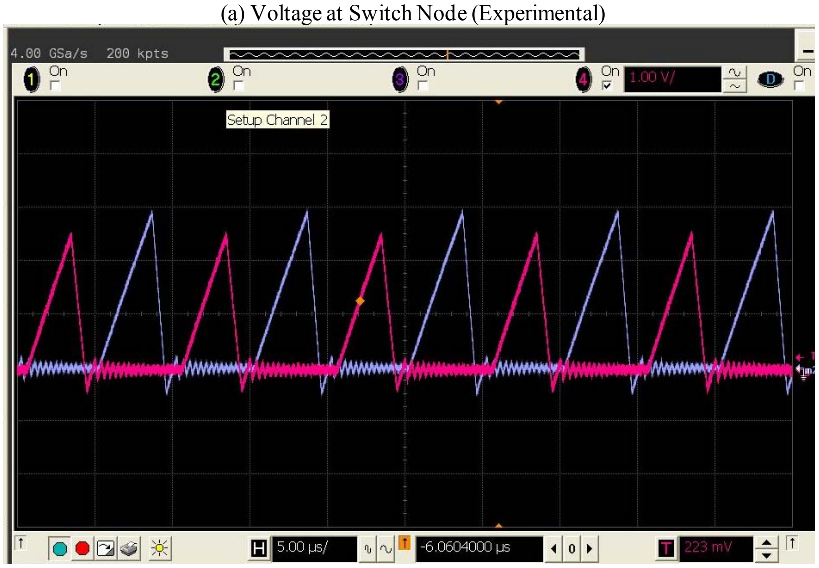
An XFR60-20 60 V, 20 A DC power supply supplied the input power, and a Chroma 63202 500 V, 50 A electronic load was connected at the output. Input power was estimated by multiplying the values from the digital voltage and current readouts on the DC power supply. Output voltage and power was read directly from the load digital display. Waveforms were obtained with an Agilent Infiniium MSO8104A 1GHz scope using an Agilent N2772A 20 MHz 20:1 differential voltage probe and an Agilent N2782A 50 MHz 10:1 current probe. The experimental results are summarized in Table 10, and the switch node voltage and inductor currents are shown in Fig. 20.

Table 10
Summary of experimental results for DCM synchronous series hybrid converter (Fig. 12)

	Input Current	Input Power	Output Power	Losses	Efficiency
Boost (separate)	4.6 A	110.4 W	100 W	10.4 W	90.5 %
BB (separate)	5.0 A	120.0 W	100 W	20.0 W	83.3 %
Combined	9.6 A	230.4 W	200 W	30.4 W	86.8 %



(a) Voltage at Switch Node (Experimental)



(b) Inductor Currents (Experimental)

Fig. 20. Oscillation at switch node from MOSFET drain-source capacitance (experimental). The traces in (a) (boost – green, BB-purple) show the voltage at the switch node of each converter; it begins at the input voltage during the active switch on-time, rises to the output voltage during the synchronous switch on-time, and then exhibits damped ringing during the period when both switches are off. The traces in (b) (boost-pink, BB-purple) show the inductor currents; note the low-magnitude of the oscillation during the period when both switches are off.

For the experimental boost converter, the losses in Table 10 (10.4 W) are very close to the predicted losses in Table 9 (9.89 W). The experimental buck-boost converter showed heavier losses (20.0 W) than predicted in the simulation (13.2 W). Some of the losses in both experimental converters come from the ESR of the input capacitance, which was not accounted for in simulation. The actual inductor Q was lower than 75, so the increased effective resistance also contributed to the additional losses. Because the input voltage was measured at the input source instead of the converter input, a small part of the additional losses can be attributed to losses in the input cables. The resistance of the PCB copper traces also contributed additional losses, especially in the long trace connecting the BB inductor to its switch node.

The performance of the experimental prototypes can be greatly improved by the use of improved capacitors. Substituting a single low-ESR film capacitor for the three paralleled electrolytic capacitor would reduce the ESR from 267 mΩ to less than 10 mΩ and eliminate almost 9 W of losses while improving the output voltage ripple. The overall efficiency of the experimental prototypes would be expected to rise from 86.8% to 90.3%. The smaller footprint of the input and output capacitance would reduce the overall converter size. A better PCB layout would also contribute to lower losses by minimizing track length and the associated resistance and inductance.

4.6 Conclusions

In this chapter the multiple module approach was extended to low power renewable applications. It was shown that the steeper voltage transfer characteristic of DCM operation enables high voltage gain to be achieved at smaller duty cycles. A DC model that accurately models parasitic conduction effects was developed using the principle of energy conservation. A design procedure was developed that determines component choices based on gain and efficiency specifications. A 200 W series-hybrid multiple module converter operated in DCM was demonstrated that achieved a gain of 8.33 V at 86.6% efficiency.

CHAPTER V

HIGH GAIN CONVERTER CONFIGURATIONS FOR HIGHER POWER APPLICATIONS

5.1 Introduction

Research in harnessing and delivering electrical power from renewable energy sources (RES) has skyrocketed as political and economic concerns have threatened traditional fossil fuel supplies. Wind energy is the most mature RES, and more than 100 GW of capacity has been installed throughout the world. Offshore wind energy is especially promising for many reasons [23]. The lack of topological variation over the ocean increases the accuracy of energy predictions, and the wind speed (and available energy) increases with increasing distance from the shore. Noise and visibility considerations are greatly reduced. Larger wind turbines can be used offshore, and models in excess of 5 MW are currently being marketed. Offshore installations also have accompanying disadvantages. Reliability concerns are even more important because of the difficulty in servicing offshore wind farms. Distance is also a major issue; the increased energy production must be transmitted over longer distances.

Efficient transmission of the generated power over such long distances normally requires boosting of voltages to high levels with high voltage AC transmission (HVAC). However, HVAC requires three conductors to transmit power, and the inductive nature of the cables consumes reactive power. The distance that power can be transmitted via

HVAC underground or submarine cables is limited due to capacitive charging currents that can consume a significant portion of the cable capacity [24].

HVDC transmission can overcome many of the drawbacks of HVAC transmission. The advantages of HVDC transmission include the lower line cost and right-of-way requirements due to fewer conductors, the ability to transfer power between two asynchronous AC systems, and superior long distance transmission [24]. The resulting savings in offshore wind applications that require long transmission distances can offset the increased cost of HVDC converter stations. HVDC is divided into two main categories: line commutated converters (LCC), or conventional HVDC, and self-commutated converters, or HVDC Light.

Conventional HVDC, a robust and reliable technology which has been in use for decades, uses an AC transformer and a twelve-pulse thyristor bridge at both the rectification side and the inversion side. The bidirectional flow of active power can be controlled by varying the thyristor firing angle; however, large variations in firing angle require large variations in reactive power. Conventional HVDC always consumes reactive power, so reactive power compensation is required to maintain the voltage stability of the AC grid side [24]. In order to apply conventional HVDC to offshore wind power applications, the wind farm AC-to-DC link requires an AC transformer with a large turns ratio to boost the output from a few hundred volts to a few hundred kilovolts. The large turns ratio will result in poorly coupled windings with large leakage inductances and large capacitive charging currents [25]; the result is increasing losses and voltage spikes that can destroy the semiconductors. The twelve-pulse rectifier draws large harmonic currents of order $12n\pm1$ that cause heating and loss in the transformer. Minimizing flux density in order to limit core losses and avoid saturation requires a large core that increases the bulk and cost of the transformer.

HVDC Light replaces line-commutated thyristors with self-commutated semiconductors such as IGBTs and IGCTs (Insulated Gate-Commutated Thyristors). HVDC Light holds several advantages over conventional HVDC. Active power and reactive power can be controlled independently, and the converter can be operated near unity power factor. While conventional HVDC requires a stiff synchronous AC source, which is a problem when connecting offshore wind farms during grid fault conditions, HVDC Light can synchronize a balanced set of 3-phase voltages for "black start" [24]. To apply HVDC Light to offshore wind applications, the complex AC boosting transformer in the AC-to-DC link can be replaced with a much simpler isolation transformer and a high gain DC-DC converter using self-commutated semiconductors. The low switching frequencies and low pu parasitic losses of high power semiconductors and the unidirectional power flow (from the wind farm to the grid) allow the use of multiple module CCM converters with large duty cycles.

This chapter investigates the use of the multiple module approach to provide a DC bus suitable for interfacing offshore wind turbines to the grid. A design example of a CCM cascade boost converter is presented to demonstrate the multiple module concept in a high voltage, high power converter. The multiple module approach is then compared to a conventional HVDC converter and a theoretical full-bridge DC-DC converter in terms of reliability, device counts and ratings, and isolation levels. Experimental results from 500W prototypes of the six multiple module converters are then presented to validate the multiple module concept.

5.2 Design example and simulation

The multiple module approach will be illustrated with a design example of a CCM cascade boost converter (Fig. 21). The converter is designed to condition the output of a single offshore 1 kV_{L-L} wind turbine for HVDC transmission. The turbine output voltage will be rectified by an ideal 12-pulse rectifier with negligible ripple, so the converter input voltage will be 1.35 kV_{DC}. Converter specifications are shown in Table 11. The converters will be operated at a switching frequency of 1 kHz to comply with the limited switching frequency of the high voltage switches.

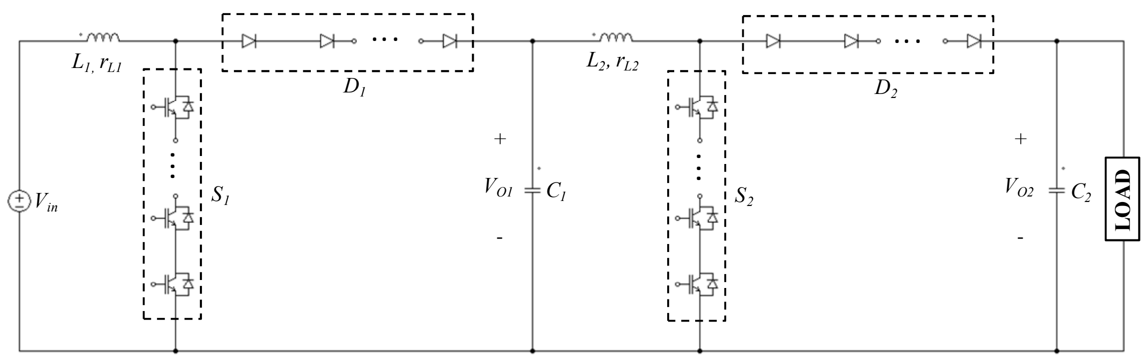


Fig. 21. High voltage multiple module cascade boost converter for high power design example.

Table 11
Converter specifications for high power design example (Fig. 21)

$V_{turbine}$ (line-to-line, rms)	1 kV	M_1, M_2	9.9 V/V
P_O	1 MW	V_{O1}	13.4 kV
V_{IN}	1.35 kV	I_{in1}	750 A
V_{O2}	132 kV	I_{in2}	75 A
M_{tot}	98 V/V	RF_1, RF_2	50%
Output voltage ripple	0.2%	f_S	1 kHz

The inductor design will be considered first. The inductance can be determined by rearranging (15) as shown in (36), and resulting inductances values (assuming $D \approx 1$) are shown in Table 12. The large difference in the inductance magnitude was predicted in the discussions of Chapter III. Note, however, that the energy product (LI^2) of the two inductors is the same, so it is expected that the inductors will be of roughly the same physical size.

$$L = \frac{V_{IN}{}^2 DT_S}{2(RF)P} = \frac{DT_S}{2RF}\frac{V_{IN}{}^2}{P} = L_{pu}\frac{V_{IN}^2}{P} \tag{36}$$

The DC resistance of the cables will be assumed to dominate the inductor resistive losses, and all core and hysteresis losses are neglected. Inductor resistances are chosen based on typical transmission cable data in [26]; the cable length is assumed to be 1 km for simplicity. This length includes only the cables used in the converter; the DC transmission cable to the onshore collection site is not included in the analysis. The proper cable diameter depends not only on the thermal limit but also on voltage regulation and on economic tradeoffs between the cost of cable losses and the cable cost. A 50% thermal loading is assumed to balance regulation, losses, and cost, so the cable is rated at twice the inductor current. The DC resistance of the first inductor is 20 mΩ, and the DC resistance of the second inductor is 400 mΩ. For per-stage base output resistances of 180 Ω and 17.4 kΩ, these conduction resistances correspond to pu resistances of 111×10^{-6} and 22×10^{-6}, respectively.

Capacitor sizes are determined by the magnitude of the inductor current ripple and by the desired output voltage specification. For example, the 2GUA high voltage capacitors from ABB are rated at 180 A and up to 25 kV [27]. The capacitors are chosen such that the ripple on each stage output voltage is less than 0.2% peak-to-peak. The output capacitor of a boost converter must supply the output current during the switch on-time. The capacitances are found by rearranging (19) as shown in (37); values are shown in Table 12. All capacitor parasitics, such as ESR and ESL, are neglected.

$$C = \frac{DT_S}{R\Delta V/V} = \frac{DT_S}{\Delta V/V}\frac{P}{M^2 {V_{in}}^2} = C_{pu}\frac{P}{V_{IN}^2} \tag{37}$$

The semiconductors in Fig. 21 (S_1, S_2, D_1, D_2) must be made up of series-combined IGBTs and diodes to extend the individual device voltage ratings; the rated voltages of the application are beyond the ratings of individual semiconductors. These series strings, or valves, will be designed to withstand up to twice the rated DC voltage. Boost converter IGBTs and diodes must withstand the output voltage in the off state. The current maximum IGBT collector-emitter voltage is 6.5 kV, and the corresponding IGBT saturation voltage is 4.8 V for a 600 A device [27]. All individual semiconductors are rated at 6.5 kV with a forward drop of 5 V per device for simplicity. Due to mismatching between the series connected devices, external components are required to force equal voltage sharing in both steady state and transient conditions. These balancing networks are not considered in this analysis.

Table 12
Component values for high power design example (Fig. 21)

L_1	1.8 mH	Series devices in S_1	4
L_2	180 mH	V_f of S_1	20 V
r_{l1}	20 mΩ	Series devices in D_1	4
r_{l2}	400 mΩ	V_f of D_1	20 V
C_1	2.7 mF	Series devices in S_2	41
C_2	30 μF	V_f of S_2	205 V
D_1	0.902	Series devices in D_2	41
D_2	0.900	V_f of D_2	205 V

The operating duty cycle of each stage and the efficiency can now be calculated using the analysis of Chapter III and the values from Table 12. Table 13 compares the calculated output voltage and efficiency to a SIMPLIS simulation of the design example (Fig. 22). The simulation substantiates the analysis.

Table 13
Comparison of calculated and simulated results for high power design example (Fig. 21)

	Calculated	Simulated
V_{O1}	13.4 kV	13.4 kV
V_{O2}	132 kV	131.7 kV
η	95.7%	93.9%

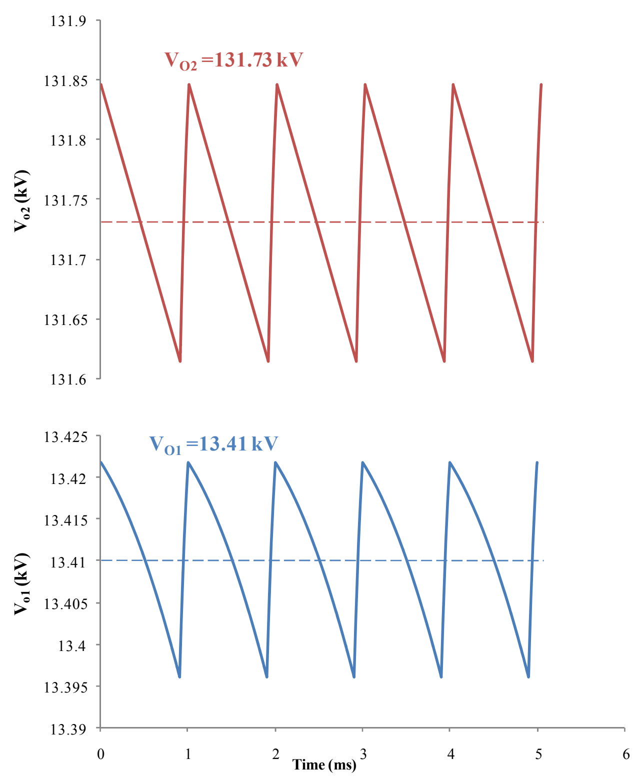


Fig. 22. Simulated converter output voltages for high power design example. Top: V_{O2}. Bottom: V_{O1}.

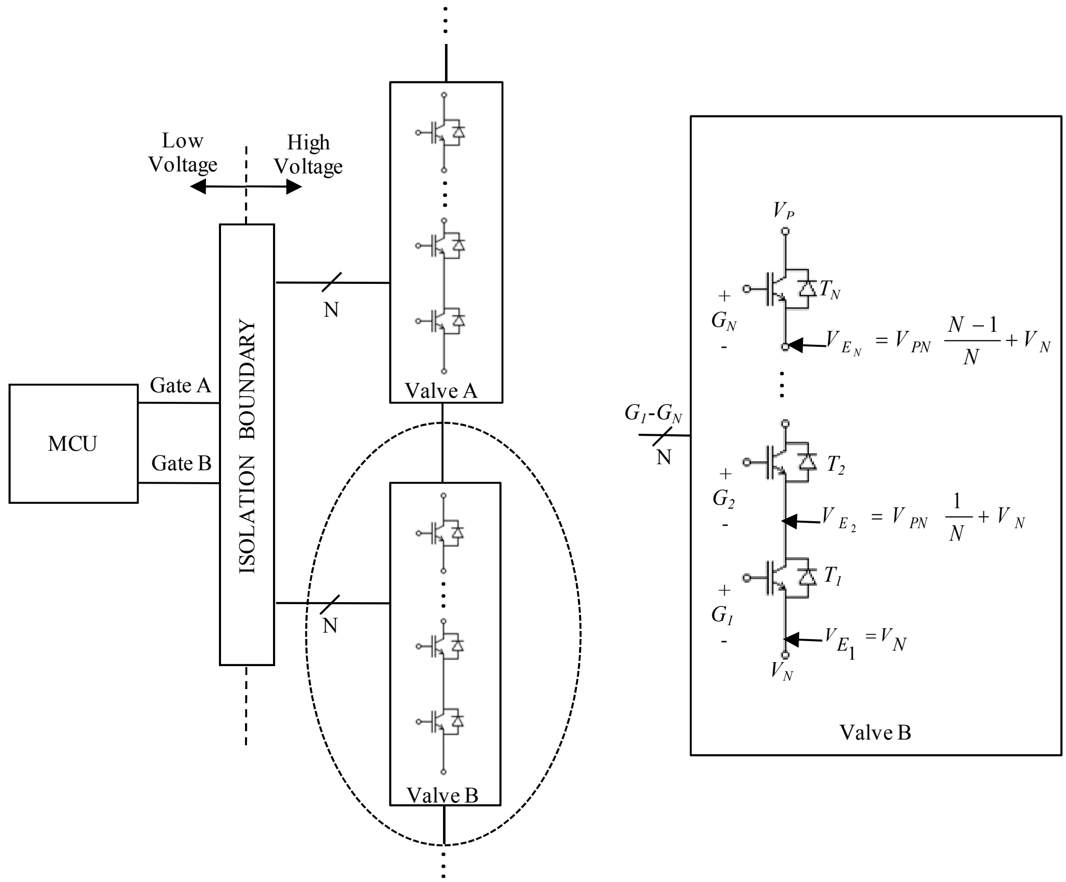
5.3 Evaluation of multiple module approach in HVDC converters

Now the multiple module converter approach is evaluated against other HVDC approaches in regards to device counts and ratings, isolation levels, and reliability. The input source for the comparison is a 1 MW wind turbine with an output of 1000 $V_{LL,rms}$. This voltage is boosted to 132 kV for HVDC transmission. Approach A presents a conventional HVDC converter that uses a line frequency AC transformer and a twelve-pulse thyristor bridge. Approach B presents a theoretical full-bridge converter that uses a 1 kHz DC-DC transformer. Approach C presents a multiple module cascade boost-boost converter. Approach D presents a multiple module series hybrid converter preceded by a line frequency AC transformer with a turns ratio of 4. The converters are modeled with the assumptions below.

1. Switching losses are neglected (f_s = 1 kHz).
2. No snubbers or rate limiters are used.
3. Leakage inductance is neglected; this would be a severe problem in approaches A and B due to the large turns ratios, so this assumption underestimates the negatives of these approaches.
4. All devices are ideal.
5. All currents are ripple-free.

Each switch or diode in the schematic diagram is made up of several series connected devices to withstand the rated voltage. A string of such devices will be referred to as a valve, and the individual devices will be referred to as switches or diodes. The valve stresses are assumed to be equally distributed among all the semiconductors within the valve. Semiconductor ratings are taken from the Eupec catalog [19]. The analysis of each approach will determine the total number of parallel and series devices required to meet the valve current and voltage rating as well as the total number of devices.

High voltage isolation is required to properly drive the semiconductors within a valve. A block diagram describing isolation of gate drivers is shown in Fig. 23a. Although each device in a valve is gated at the same time, the gating signal must be referred to the level of each individual emitter (IGBT valve) or cathode (thyristor valve) within the valve. The voltage across the valve is equally distributed across the semiconductors as shown in Fig. 23b. When the valve is off ($V_{PN} \neq 0$), each semiconductor emitter/cathode has a potential that is $1/N$ times V_{PN} greater than the emitter/cathode of the semiconductor below it. The highest isolation required during the valve off-time is then given by the emitter/cathode of the top semiconductor, which is approximately equal to the valve off-voltage for large N. When the valve is on ($V_{PN} = 0$), the isolation requirement equals V_N and is set by the external circuit. The larger of these two values determines the isolation level of the converter.



(a) High voltage isolation of gate signal (b) Detail of Valve B

Fig. 23. Gate drive isolation for valves. A microcontroller provides a gating signal for each valve as shown in (a). This signal is then duplicated for *N* semiconductors in the valve and level shifted as determined in (b). Although the voltage at the valve's lower connection point may be low, the offset voltage required to drive the upper semiconductors can still be very large. The isolation circuit must be able to withstand this voltage.

5.3.1 Conventional HVDC converter

The conventional HVDC approach is shown in Fig. 24. This approach requires a line frequency AC transformer with a large turns ratio and two secondaries (Y and Δ) for the twelve-pulse rectifier. The maximum output voltage of an SCR bridge is 1.35 times the line-to-line input voltage, so each transformer must provide a line-to-line gain of 50x for a total maximum gain of 135. Each SCR bridge sees half the reflected input voltage, so the thyristors must withstand the peak of one half of the reflected input sine wave. The SCR bridges are controlled to reduce the output from 135 kV to 132 kV. The isolation level depends on the grounding point. If the DC return is grounded, the isolation level is determined during the conduction time of the highest voltage SCR valve. When this valve conducts, the isolation circuit must withstand the full output voltage of 132 kV. If the ground is placed at the midpoint (connection of the two 6-pulse bridges), the isolation requirement is cut in half; the cathodes of the highest SCR valve withstand 66 kV, and the cathodes of the lowest SCR valve withstand -66 kV. The current and voltage ratings of the semiconductors are shown on Fig. 24.

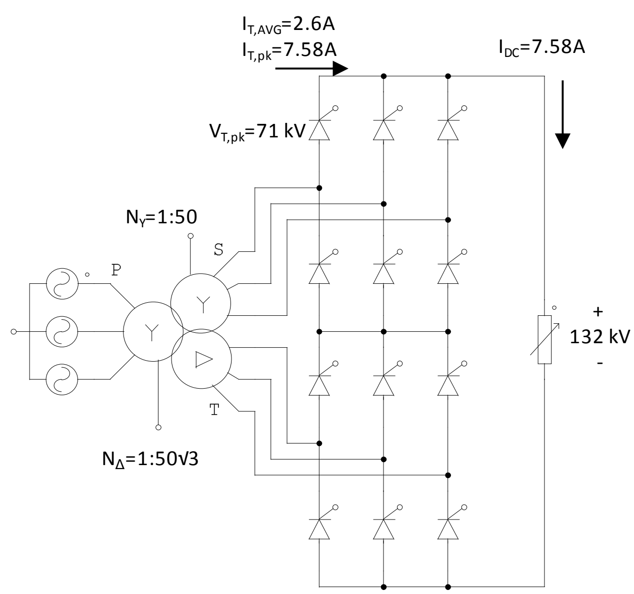


Fig. 24. Conventional HVDC (Approach A).

5.3.2 Full-bridge converter

The full-bridge circuit is shown in Fig. 25. A six-pulse bridge is used to rectify the wind turbine output and to provide a 1.35 kV output voltage. The remaining gain is provided by a high-frequency (1 kHz) transformer with n = 150 and by a switch valve duty cycle of 0.33. High frequency transformers with large turns ratios are difficult to design in high voltage, high power applications. Problems include poor coupling from large turns ratios, dielectric losses in insulation, and core losses from non-sinusoidal excitation [25]. For purposes of comparison it is assumed that an acceptable transformer can be designed. Although the switch valves must only withstand the rectifier's output voltage (1.35 kV), the diode valves must withstand twice the reflected rectifier voltage (405 kV). The isolation level is determined during the conduction time of the upper switches in the bridge, which are connected to the 1.35 kV input source at turn-on. The current and voltage ratings of the semiconductors are shown on Fig. 25.

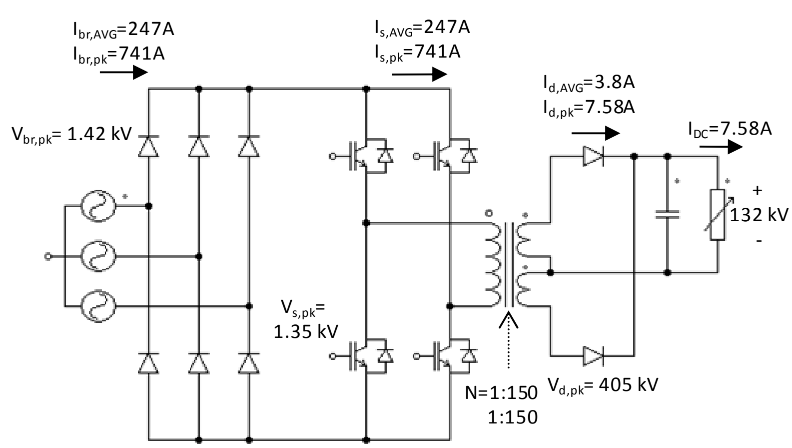


Fig. 25. Full-bridge converter (Approach B).

5.3.3 Multiple module cascade boost converter

The cascade boost configuration is shown in Fig. 26. The wind turbine output is rectified and fed to the cascade converter. The cascade configuration must boost the 1.35 kV rectifier output to 132 kV (98x). Each boost converter is designed to provide a gain of 9.9 at a duty cycle of 0.899. The switch and diode valve voltage stresses in a boost converter are equal to the stage output voltages. The average diode valve currents equal the stage output currents, and the average switch valve currents equal *D* times the stage input currents. The peak values of switch and diode valve currents are determined by the inductor current. Because each stage uses a single active valve that is connected to a fixed (ground) potential, the isolation level is determined during the switch off time. The gate drive of the top switch in a valve is driven from a voltage approximately equal to the valve's withstand voltage (Fig. 23b). The isolation level of the first stage is 13.4 kV, and the isolation level of the second stage is 132 kV. The current and voltage ratings of the semiconductors are shown on Fig. 26.

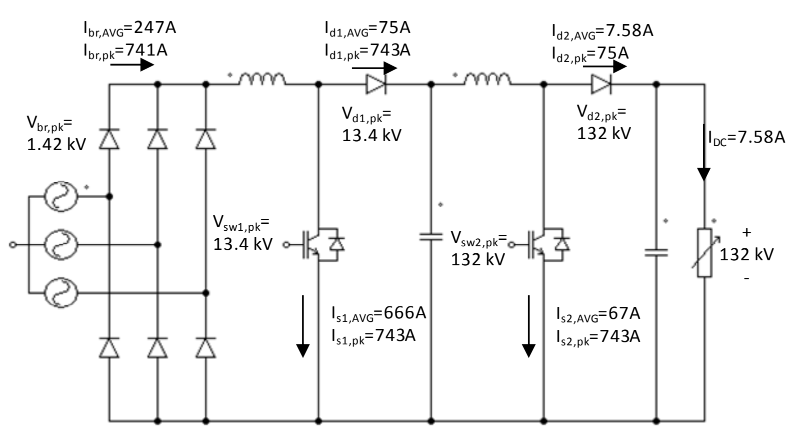


Fig. 26. Multiple module cascade boost converter (Approach C).

5.3.4 Multiple module series hybrid converter

The series hybrid converter is shown in Fig. 27. Because of the lower gain of this converter an AC transformer with a 4x turns ratio is added before the rectifier. In a practical converter this transformer would be much simpler than the AC transformer in Approach A due to the small turns ratio, and the leakage inductance would be much smaller. The remaining 33x of gain must come from the rectifier (1.35) and the series converter (24.4). The converters are designed for equal gains of 12.2 and equal input powers of 500 kW. The boost duty cycle is 0.918, and the BB duty cycle is 0.924. Each converter operates from equal input voltages and therefore draws equal input currents. All semiconductors will be rated per the slightly larger BB requirements. The BB valves must withstand the sum of the half the output voltage and the input voltage. The BB switch valves carry the average value of the input current. The diode valves in both converters carry the average output current. The peak current is given by the inductor current. The required isolation levels depend on the choice of the ground reference. If the DC return is used as ground, then the isolation level is determined by the top switch in the boost converter switch valve as in Approach C (132 kV). If the ground reference is located at the DC midpoint instead, the isolation levels are determined by the approximate maximum (boost) and minimum (BB) emitter voltages in the off-state (±66 kV). Current and voltage ratings of the semiconductors are shown on Fig. 27.

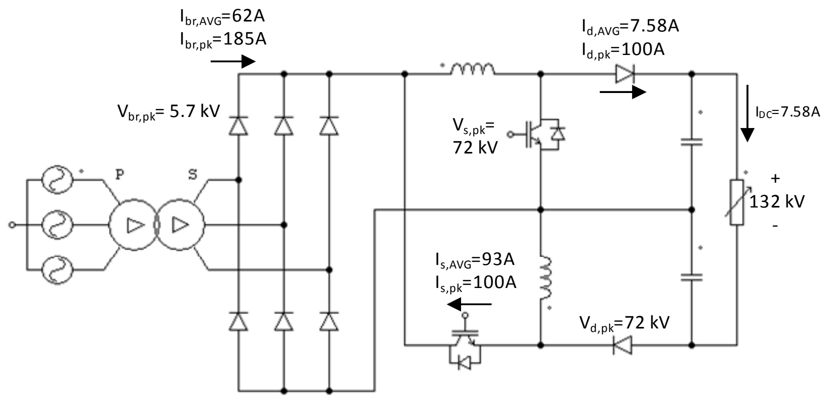


Fig. 27. Multiple module series hybrid converter (Approach D).

5.3.5 Discussion

The approaches discussed are summarized in Table 14. The device voltage ratings were determined by doubling the calculated maximum withstand voltage to allow for a maximum overshoot of 2 pu; the device current ratings are double the current stresses to provide a margin of safety. Devices were selected from the Eupec catalog [19] based on the minimum number needed to withstand these derated valve voltage and current stresses. The specifications of the catalog device (V_{semi} and I_{semi}) were used to calculate the number of series and parallel devices in each valve. The number of devices per valve was then multiplied by the number of valves to reach the total device count.

The device counts in the multiple module cascade (Fig. 26) and series (Fig. 27) converters are much smaller than that of the conventional HVDC (Fig. 24) and full-bridge (Fig. 25) converters. A smaller device count simplifies implementation by reducing external balancing network components, snubbers, and rate-limiters that are required for series-connected devices. Smaller device counts mean fewer failure points and higher reliability.

Table 14
Comparison of HVDC approaches: device ratings, device counts, isolation levels

	Device	Eupec P/N:	V_{off} (kV)	Derated (kV)	V_{semi} (kV)	Series in Valve	I_{DC} (A)	Derated (A)	I_{semi} (A)	Parallel in Valve	Total per Valve	Valves	Total	Isolation Level (kV)
A (Fig. 24) Conventional HVDC	SCR	T201N	72	143	6.5	22	2.5	5	245	1	22	12	**264**	132/±66
B (Fig. 25) Full-Bridge	SCR	T1220N	1.42	2.8	2.8	1	247	500	1220	1	1	6	**260**	1.35
	IGBT	FZ800R33KF2C	1.35	2.7	3.3	1	247	500	800	1	1	4		
	Diode	DD200S65K1	405	810	6.5	125	3.8	8	200	1	125	2		
C (Fig. 26) Cascade Boost	SCR	T1220N	1.42	2.8	2.8	1	247	500	1220	1	1	6	**100**	132
	C1 IGBT	FZ600R65KF2	13.4	26	6.5	4	666	1200	600	**2**	8	1		
	C1 Diode	DD200S65K1	13.4	26	6.5	4	75	150	200	1	4	1		
	C2 IGBT	FZ200R65KF2	132	264	6.5	41	67	135	200	1	41	1		
	C2 Diode	DD200S65K1	132	264	6.5	41	7.6	16	200	1	41	1		
D (Fig. 27) Series Hybrid	SCR	T571N	5.7	11.5	6.5	2	62	130	540	1	2	6	**104**	132/±66
	IGBT	FZ200R65KF2	72	143	6.5	23	86	175	200	1	23	2		
	Diode	DD200S65K1	72	143	6.5	23	7.6	16	200	1	23	2		

The voltage levels of the valve devices are important because devices built to withstand higher voltages are both more expensive and lossier due to doping requirements. The conventional HVDC approach (Fig. 24) requires 264 6.5 kV devices, while the full-bridge approach (Fig. 25) requires 250 6.5 kV, 4 3.3 kV devices, and 6 2.8 kV devices. The cascade approach (Fig. 26) uses only 94 6.5 kV devices and 6 2.8 kV devices, and the series approach (Fig. 27) uses 104 6.5kV devices.

The isolation levels are similar for all but the theoretical full-bridge converter (Fig. 25) because the gate drive for the topmost IGBT or SCR in a valve must be referenced to at least half of the output voltage. The cascade converter has no natural midpoint, so the gate drive of the top switch must be referenced to near the full output voltage. The multiple module approaches are still superior due to the number of drives required. The rectifier in conventional HVDC (Fig. 24) with a grounded midpoint requires one gate drive with +66 kV isolation and two gate drives with -66 kV isolation in each leg for a total of nine gate drives with ±66 kV isolation. The cascade approach (Fig. 26) requires only two gate drives with 13.4 kV isolation for the first converter and one gate drive with 132 kV isolation for the second. The series converter (Fig. 27) with grounded midpoint requires only four gate drives with 66 kV isolation.

Perhaps the most important concern in converters used for power transmission is reliability. The multiple module approach is superior to the other approaches in terms of reliability due to the ability to interleave modules. A single converter module can be constructed from several interleaved phases that process a fraction of the input power. If one of these phases fails, the converter operates at a reduced capacity instead of going off-line. In contrast, the failure of a single valve in a conventional HVDC converter (Fig. 24) or full-bridge converter (Fig. 25) forces the entire converter offline. Neither thyristor bridges nor transformer-based converters can be easily interleaved to increase reliability.

5.4 Prototype circuits

Prototypes of each of the six multiple module converters were constructed to experimentally verify the multiple module approach. The circuit parameters and devices are listed in Table 15. A 15 V input supply was used to demonstrate large voltage gain while maintaining the maximum output voltage under the equipment ratings. Gating signals were generated with a TMS320F2812 DSP from Texas Instruments mounted in a Zwickau adapter board. The duty cycle was varied from D=0.5 to a maximum of D=0.92; testing was terminated earlier in the cascade converters at duty cycles that would result in an output voltage of 500V for an ideal (lossless) converter. A Magna PQDiii 50 V, 65 A DC power supply provided the input voltage, and a Chroma 63202 500 V, 50 A electronic load provided the variable load.

Table 15
Prototype circuit parameters and device data

V_{in}	15 V	P_{in}	500 W	f_S	1 kHz
Semiconductors	**Rated Voltage**	**Rated Current**	**Manu.**	**Part Number**	V_f
Series IGBT	1000 V	60 A	Fairchild	FGL60N100BNTD	1.8 V
Cascade-1 IGBT	600 V	200 A	STMicro	STGE200NB60S	1.2 V
Cascade-2 IGBT	1000 V	60 A	Fairchild	FGL60N100BNTD	1.8 V
Diodes	600 V	60 A	IXYS	DSEI60-06A	1.8 V
Inductors	**Value**	**Rated Current**	**Manu.**	**Part Number**	r_l
Series	500 µH	150 A	Hammond	195B150	1.8 mΩ
Cascade, stage 1	500 µH	150 A	Hammond	195B150	1.8 mΩ
Cascade, stage 2	2x 10mH	50 A	Hammond	195J50	2x 23 mΩ

The modeling and simulations in Chapter III assumed small pu IGBT/diode forward voltages. While this assumption is valid for devices working at the actual power and voltage levels of the application, it is not valid at the power and voltage levels of the prototypes. The forward voltages of the semiconductors listed in Table 15 ranged from 1.2V to 1.8V. These values are significantly higher on a pu basis (0.08 to 0.12 for a 15 V input) than those assumed in modeling and simulation (0.0015). The losses are therefore expected to be greater in the prototypes. Also, the assumption of equal pu losses in each stage is violated because similarly rated devices are used in both prototype stages.

The IGBT/diode efficiency term of (13) evaluates to 88% for a single boost converter with a 15V input (assuming full 1.8V drops across all semiconductors). This efficiency term of (13) for a single buck-boost converter ranges from 76% at D=0.5 to 86% at D=0.85. These losses are approximately independent of load current and represent the upper limit to the efficiency of each prototype converter. The efficiency of the prototype series boost and series BB converters are lower still because of the additional BB converter that is cascaded with converter 2. Both bottom converters see an input of approximately 15 V, so the efficiency losses multiply. The IGBT/diode term of (13) for the cascaded connection of converter 2 is (0.76)(0.88) = 67% for the series boost converter and a worst case of (0.76)(0.76) = 58% at D=0.5 for the series BB converter. The efficiency is expected to be higher in a converter with small pu forward voltages.

The effect of the diode/IGBT drop is less pronounced in the cascade converter prototypes. While the bottom two converters in series boost and series BB configurations see (approximately) equal input voltages, in a cascade configuration the second stage converter sees a much larger input voltage than the first stage. In the prototype, where similarly rated devices were used in each stage, the magnitude of the second stage IGBT/diode loss term in (13) decreases on a pu basis as the first stage output voltage (second stage input voltage) increases. The efficiency of the second stage increases with increasing duty cycles/input voltages. Using the prototype of the cascade boost converter as an example, the IGBT/diode loss term of (13) in the second stage evaluates to 97% when the first stage output voltage reaches 60 V. The first stage IGBT/diode loss term in (13) evaluates to 88% for all duty cycles.

The results of prototype testing of the six multiple module converters are shown in Fig. 28 (blue data points). A simulation for each converter using the actual circuit values and parasitic drops is also shown in Fig. 28 (red line). This simulation provides a more accurate benchmark for evaluating the performance of the prototypes. In the simulation of series boost and BB converters the duty cycle of the inverting converter was fixed at 55% (allowing for IGBT/diode losses), but in the prototypes this duty cycle was adjusted to fine-tune the power drawn from the source. The resulting inverter output voltage in the series converter prototypes therefore varied from 15 V at D=0.5 to 12.7 V at D=0.92. Testing for the cascade converters was terminated at duty cycles that would result in an output voltage greater than 500 V in an ideal (lossless) converter. The minimum D for the cascade-BB was limited to 0.67 to keep the second stage current beneath the ratings of the cables and components. At each data point either the load (cascade converters) or the inverting duty cycle (series converters) was adjusted to draw an average current of 33 A from the source (500 W).

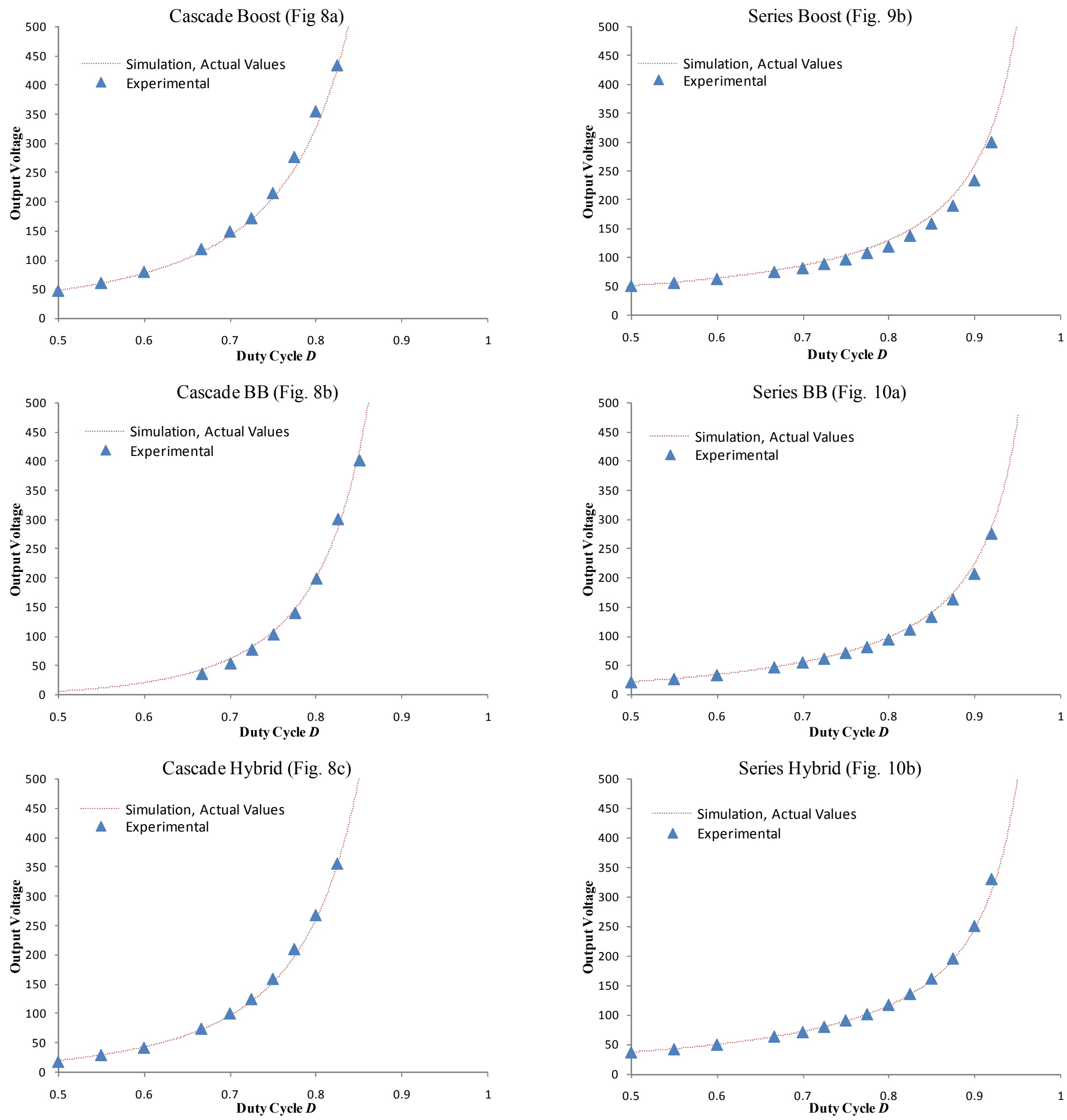


Fig. 28. Experimental output voltages of low power multiple module converter prototypes. Experimental results closely track simulations with actual component values.

The experimental results track the simulation results very closely. Although IGBT/diode losses in the prototypes resulted in lower output voltages than calculated, the degradations remained consistent across the duty cycle range. The series converters performed poorly as all individual converters saw a small input voltage and a correspondingly large pu IGBT/diode forward voltage. The series hybrid performed the best, reaching an output voltage of 330 V at D=0.92 for a gain of 22 V/V. The output voltage in the series boost and series BB converters could not match the performance of the series hybrid because of the losses in the extra inverting converter. The cascade converters performed better than the series converters as the second stage saw a much smaller pu IGBT/diode forward voltage and had a much higher efficiency. The cascade boost reached a maximum output voltage of 435 V at D=0.825 for a gain of 29 V/V.

Although IGBT/diode losses were large in the prototypes, the duty cycle-dependent losses from the inductor resistance did not become large enough to limit the converter gain. This was shown in Fig. 1 to be the major limitation in extending the operating duty cycle of boosting converters. In high voltage, high power applications with small pu IGBT/diode forward voltages the multiple module configurations should perform at high efficiencies even at extreme duty cycles.

5.5 Conclusions

In this chapter the multiple module approach was applied to high power wind energy applications. A design example was presented to illustrate the use of the multiple module approach in high power wind energy HVDC applications. The multiple module approach performs well when compared to other HVDC approaches according to device counts and ratings, isolation levels, and reliability. Experimental results were presented for low power prototypes that reached gains of up to 29 V/V.

CHAPTER VI

CONCLUSIONS

6.1 Summary of work

Renewable energy sources such as photovoltaic cells, fuel cells, and wind turbines show great promise in meeting worldwide energy demand in the face of increasing pressures on conventional fossil fuels. PV cells and fuel cells are often used in low voltage applications and show a 2:1 variation in output voltage from no load to full load. They are often integrated into the energy system at the distribution level. Offshore wind farms must transmit high power produced at a few kilovolts over long distances, and integration can be made at the transmission level. Both applications require large step-up ratios and high efficiencies that are beyond the capability of conventional transformerless converters. Converters with large step-up ratios that eliminate transformers enable reductions in cost, bulk, and complexity. This work proposed the use of multiple module converters as high gain DC-DC converters for interfacing renewable energy sources to electrical grids.

The importance of accurate modeling of conduction losses in renewable energy applications was introduced in Chapter II, and the principle of energy conservation was used to accurately model the effect of conduction resistances, diode forward voltages, and non-zero current ripple in CCM and DCM converters. This accurate modeling is essential to understanding the limits of the achievable voltage gains of multiple module converters.

In Chapter III the multiple module approach was presented as a means for providing high voltage gain in renewable energy applications. Modules of basic single-switch boosting converters were combined in series or cascade to provide increased gains. Duty cycle constraints were developed for cascade and series multiple module converters that relates the maximum gain achievable at a desired efficiency. It was shown that the use of single-switch converter modules simplifies interleaving, which can reduce input current and output voltage ripples, reduce parasitic resistances, and increase reliability. The reliability inherent in interleaving is a great asset in high power renewable generators feeding the transmission system where failures can lead to overall system instability. Pu simulations were presented that verified the performance of multiple module configurations operating at extreme duty cycles.

In Chapter IV this work extended the multiple module approach to low voltage, low power renewable PV or fuel cell applications. A multiple module series hybrid converter operated in DCM was demonstrated that provided a gain of 8.33 V/V from a 24 V, 200 W input source without using a transformer. Simulation and an experimental prototype confirmed that high gains can be reached with multiple module converters operated under the steeper voltage transfer characteristic of DCM.

In Chapter V this work demonstrated the multiple module approach in high power, high voltage wind energy applications. It was demonstrated that low pu parasitic losses and relatively long switching periods allow high efficiencies to be reached even at extreme duty cycles. It was demonstrated that the multiple module approach outperforms conventional approaches in terms of device counts, device ratings, and reliability, and the isolation levels of the multiple module approach are comparable or superior. The multiple module approach was verified with low voltage prototypes that reached gains of up to 29 V/V at 500 W.

6.2 Further work

The multiple module approach can be extended in several ways. The approach is quite general; any non-isolated converter can be combined for increased gain. If switching losses dominate conduction losses in a given application, multiple modules of resonant converters can be combined in series or parallel. Alternatively, modifications can be made to the single-switch boosting converters to mitigate switching losses.

For example, one disadvantage of the single-switch CCM boosting converters is the diode reverse recovery current. The large current turn-off slopes in CCM induce large reverse current pulses as the diode removes its stored junction charge. These pulses increase switch current stress and can lead to overheating and device failure. Silicon carbide (SiC) diodes, which exhibit negligible reverse recovery effects, can be used in place of conventional silicon diodes to reduce switching loss. This modification should further enhance multiple module configuration operation.

In this work all multiple module configurations were operated at equal duty cycles, but several different control schemes can be used. For example, there is some advantage to operating each converter in a cascade configuration at different duty cycles to provide damping at different load levels. Operating each converter at different gains may provide a way to optimize overall losses.

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VITA

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