DESIGN TECHNIQUES FOR HIGH SPEED LOW VOLTAGE AND LOW POWER

NON-CALIBRATED PIPELINE ANALOG TO DIGITAL CONVERTERS

A Dissertation

by

RIDA SHAWKY ASSAAD

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2009

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Edgar Sanchez-Sinencio
	Frederick Strieter
	Mahmoud El-Halwagi
Head of Department,	Costas N. Georghiades

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ABSTRACT

Design Techniques for High Speed Low Voltage and Low Power Non-Calibrated

Pipeline Analog to Digital Converters. (December 2009)

Rida Shawky Assaad, B.S., Texas A&M University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

The profound digitization of modern microelectronic modules made Analog-to-Digital converters (ADC) key components in many systems. With resolutions up to 14bits and sampling rates in the 100s of MHz, the pipeline ADC is a prime candidate for a wide range of applications such as instrumentation, communications and consumer electronics. However, while past work focused on enhancing the performance of the pipeline ADC from an architectural standpoint, little has been done to individually address its fundamental building blocks. This work aims to achieve the latter by proposing design techniques to improve the performance of these blocks with minimal power consumption in low voltage environments, such that collectively high performance is achieved in the pipeline ADC.

Towards this goal, a Recycling Folded Cascode (RFC) amplifier is proposed as an enhancement to the general performance of the conventional folded cascode. Tested in Taiwan Semiconductor Manufacturing Company (TSMC) 0.18µm Complementary Metal Oxide Semiconductor (CMOS) technology, the RFC provides twice the bandwidth, 8−10dB additional gain, more than twice the slew rate and improved noise

performance over the conventional folded cascode—all at no additional power or silicon area. The direct auto-zeroing offset cancellation scheme is optimized for low voltage environments using a dual level common mode feedback (CMFB) circuit, and amplifier differential offsets up to 50mV are effectively cancelled. Together with the RFC, the dual level CMFB was used to implement a sample and hold amplifier driving a single-ended load of 1.4pF and using only 2.6mA; at 200MS/s better than 9bit linearity is achieved. Finally a power conscious technique is proposed to reduce the kickback noise of dynamic comparators without resorting to the use of pre-amplifiers. When all techniques are collectively used to implement a 1Vpp 10bit 160MS/s pipeline ADC in Semiconductor Manufacturing International Corporation (SMIC) 0.18µm CMOS, 9.2 effective number of bits (ENOB) is achieved with a near Nyquist-rate full scale signal. The ADC uses an area of 1.1mm^2 and consumes 42mW in its analog core. Compared to recent state-of-the-art implementations in the 100-200MS/s range, the presented pipeline ADC uses the least power per conversion rated at 0.45pJ/conversion-step.

To my dear parents, my cherished sisters, and my beloved wife.

ACKNOWLEDGEMENTS

I have been privileged to be a graduate student in the Analog and Mixed Signal Center at Texas A&M University for the past few years leading to this dissertation. My experience was filled with learning opportunities from a unique faculty and student body. I would like to begin by thanking my advisor, Dr. Jose Silva-Martinez, for his invaluable insights into circuit design that brought about this work, endless patience with a demanding student, and support and guidance in matters both academic and personal. I also would like to thank Dr. Edgar Sanchez-Sinencio for serving on my committee and the different perspectives by which he approached and analyzed technical and non-technical matters alike. I owe a debt of gratitude to Dr. Frederick Strieter for steering me to analog circuit design from solid-state device physics and for working with him for many years as a teaching assistant. I am also grateful to Dr. Mahmoud El-Halwagi for his open door, listening ears and encouraging words when the going got rough.

Many friendships were made in the midst of circuit design chaos that made this experience all the more memorable. Chinamaya, David, Alberto, Artur, Wennie, Julio, Faisal, Nozahi, John, Raghavendra, Felix, and many more, thank you for an amazing journey; you have taught me many things through your character and example. Special thanks go to Ella, Tammy and Jeanie for bearing with my relentless questions and always having the answer. Finally, thanks to my parents for shaping me into the man I am, my sisters for their encouragement, and my wife for her endurance, kindness, faith and love.

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CHAPTER I

INTRODUCTION

The advancements of CMOS technologies continue to enable the growth of digital systems in size, complexity and robustness. Consequently, more and more signal processing functions are diverted from the analog to the digital domain for increased reliability and reduced cost. Such diversion is illustrated in the simplified consumer digital photography example of Fig. 1. When charge-coupled devices (CCD) were the predominant sensor base, analog conditioning was performed on the picture before it was digitized to simplify the digital processing. As CMOS technologies continued to mature, they brought by the development of CMOS sensors and increased digital signal processing (DSP) power. Now, many of the functions previously performed in the analog domain are carried out in the digital domain with enhanced performance.
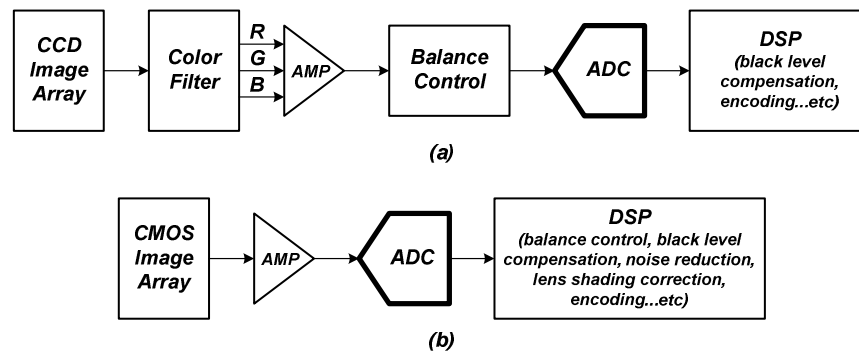
Fig. 1. Consumer digital photography, (a) before and (b) after the development of the CMOS sensor arrays.

This domain shift, however, places stringent requirements on the analog to digital converter (ADC). In the digital photography example of Fig. 1, the signal bandwidth of the ADC in Fig. 1(b) needs to be greater than that in Fig. 1(a) to capture the finer details necessary for the additional digital processing; this generally translates to a higher speed and/or resolution for the ADC.

A. Motivation

The dominion of DSP over core functions of microelectronics systems continues to push the development of high performance ADCs forward, but not without obstacles. The first hurdle is the adaptation of analog circuit design to the low voltage supplies of modern CMOS technologies; reduced device gain and reduced signal swing are a couple of examples of the difficulties faced.

A survey of CMOS ADCs, which shows the resolution/bandwidth plane of different ADC architectures found in recent literature is summarized in Fig. 2 [1]-[29]. A key observation is that oversampling $\Delta\Sigma$ ADCs [1]-[6] are dominant where high resolution is needed in a limited signal bandwidth, whereas single-step Flash ADCs [7]-[11] push the signal bandwidth envelope for low resolutions. A best line fit of their combined data reveals that multi-stage conversion ADCs [12]-[29], of which the pipeline ADC is the most prevalent architecture, are on the frontier of high speed and high resolution ADCs. This is due to the wide variety of consumer electronics—digital cameras, camcorders, cell phones, digital radio, GPS ... etc—that demand such high performance on both fronts. The increased portability of such systems, however, adds

another critical obstacle to analog circuit design: low power consumption.

Previous work tackled the low voltage low power obstacles of analog design in pipeline ADCs from an architectural level; the optimization of bit resolutions per pipeline stage, amplifier sharing among stages and digital calibration techniques are some examples. While these techniques have proved effective, they withdrew attention away from the fundamental performance of the individual pipeline ADC building blocks. This work will focus on robust low voltage design techniques that reduce power consumption in these blocks without sacrificing, if not improving, performance. The target is a pipeline ADC with 10bit resolution and a signal bandwidth around 100MHz, since these specifications seem fitting for many applications as concluded from Fig. 2.
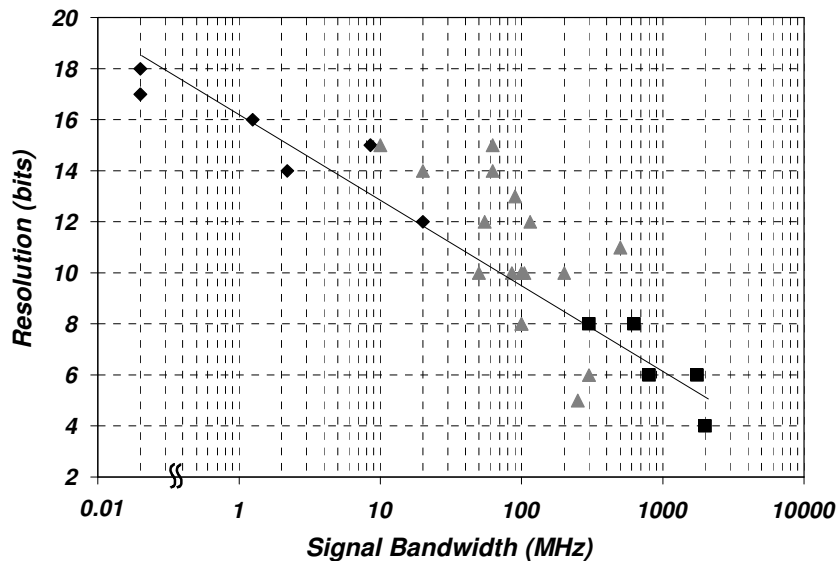
Fig. 2. Survey of recent literature; ♦ oversampling, ■ single-step and ▲ multi-step conversion ADCs.

B. Research Contribution

The linearity of the pipeline ADC is limited primarily by the performance of the amplifiers and comparators which together make the bulk of its building blocks. Foreground and background digital calibration can be used, but are costly—even unnecessary—for resolutions at or below 12bits. Therefore, it is imperative to advance the analog design techniques on the transistor level. This is achieved in this research by:

- A systematic approach of extracting the non-linearity sources in pipeline ADCs and how they translate to the required specifications of amplifiers and comparators, thus eliminating the need for digital calibration.

- A novel Recycling Folded Cascode amplifier that enhances the majority of the fundamental performance metrics of the conventional folded cascode, and promises significant savings in both power dissipation, and silicon area. The proposed circuit modifications to the conventional Folded Cascode are simple and inexpensive in terms of design, and are robust in low voltage environments.

- A dual level CMFB approach to optimize the auto-zeroing offset cancellation scheme in low voltage environments, which has a direct impact on the performance of pipeline ADCs using high bit resolutions per stage.

- A power conscious technique to reducing the kickback noise of dynamic comparators that are indispensable to the implementation of low power and low voltage pipeline ADCs.

Moreover, the circuit design techniques proposed are not limited to pipeline ADCs, but may also be adopted by many other discrete and continuous time applications.

C. Dissertation Organization

Chapter II of this dissertation gives an overview of ADCs. The principles of sampling and quantization are presented, and the major static and dynamic metrics commonly used to quantify the performance of ADCs are described. A survey of the recent ADCs in literature concludes the chapter and highlights the role and domain of pipeline ADCs among different ADC architectures.

Chapter III presents the pipeline ADCs in a systematic manner. The architecture is first introduced, and then broken down into the basic building blocks where the sources of the main non-idealities are identified and translated into design specifications. Low voltage implementation concerns and power optimization techniques are also presented. Amplifiers are discussed in Chapter IV; the amplifier limitations previously highlighted in Chapter III are closely examined in Chapter IV and their physical origins are presented. Moreover, some amplifier enhancement techniques are covered.

Chapter V is devoted to the proposed recycling folded cascode amplifier. It covers the design methodology of the amplifier and analytically demonstrates its enhanced performance over the conventional folded cascode.

In Chapter VI, the dual level CMFB approach is introduced and its application to optimize the direct auto-zeroing offset cancellation scheme in low voltage environments is described and demonstrated.

Chapter VII discusses the implementation of low voltage low power dynamic comparators and presents a power conscious technique to reduce their kickback noise without relying on preamplifiers.

Chapter VIII includes the experimental results supporting the proposed circuit techniques; a comparison of the conventional and recycling folded cascode amplifiers performances, a 10bit 200MS/s Sample and hold amplifier and simulations of a 10bit 160MS/s pipeline ADC are presented.

The dissertation is concluded in Chapter IX.

CHAPTER II

OVERVIEW OF ADCS

Analog to Digital Converters (ADCs) are the bridge connecting the sensed physical realm to the world of computation. Portable electronics, instrumentation equipment and communications are but a handful of applications where ADCs are at the heart of what humans can perceive and machine can understand. The principal function of ADCs, as the name implies, is the conversion of analog continuous signals to digital binned data-points through the processes of sampling and quantization as depicted by Fig. 3, which shows a signal $x(t)$ before and after conversion.
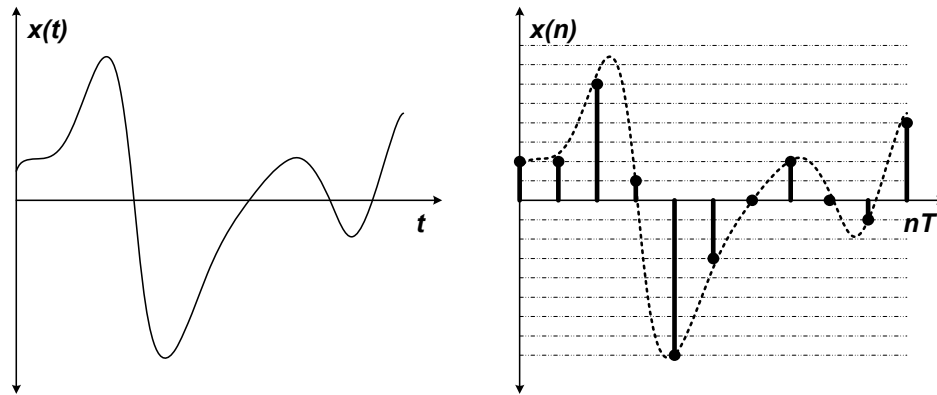
Fig. 3. A continuous analog signal $x(t)$ before (left) and after (right) conversion.

The resolution of the digital data, or the smallest discernible value by the ADC, is defined by the number of bits N representing the digital data and the signal full-scale range (*FS*, or V_{FS} for voltage) an ADC can handle. This is commonly referred to by Δ—

the value represented by the least significant bit of the digital output, 1 *LSB*—and can be expressed as in (1).

$$\Delta = \frac{V_{FS}}{2^N - 1} \cong \left. \frac{V_{FS}}{2^N} \right|_{N \gg 1} \tag{1}$$

A. Sampling

Digital data are discrete in time; this is the result of sampling. A general block diagram of a discrete-time ADC is given in Fig. 4. The first step in analog-to-digital conversion is sampling the analog data so it can be quantized and it is often performed at a uniform rate determined by the ADC sampling clock period T_S.
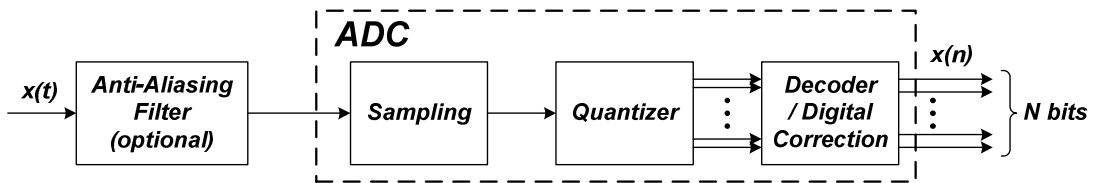
Fig. 4. A general discrete-time ADC block diagram.

There are several considerations to the quality of the sampled signal that need be taken during the sampling process, and perhaps the most critical is fulfilling Nyquist-Shannon sampling theorem [30]-[31], which states: a bandwidth limited signal *x(t)*, whose maximum spectral component is at f_B, can be reconstructed without loss of information if it was sampled at f_S, where $f_S > 2f_B$. Ideally, the sampling process yields a

sequence of delta functions whose amplitude is that of the input signal at the sampling instance, and for uniform sampling with time period T_S, the output can be given by (2).

$$x(t) \xrightarrow{\text{sampling}} x(nT_S) = \sum_{n=-\infty}^{\infty} x(t)\delta(t - nT_S) \qquad (2)$$

In the time domain, the sampled signal looks as shown in Fig. 3 (right) with valid values at integer intervals of T_S. As for the frequency domain, Fig. 5 shows the spectra of the input signal before and after sampling. The sampling process replicates the signal's spectrum at integer intervals of the sampling frequency f_S. If, however, the condition set by the sampling theorem was not met, the replicated signal spectra overlap. This spectral overlap is commonly referred to by aliasing. When a sampled signal is reconstructed, only the spectral content in the range $\{-f_S/2, f_S/2\}$ is used. Clearly in the case of Fig. 5(c) the signal is corrupted. This is represented in the time domain in Fig. 6, where a high frequency signal can be mistaken for a low frequency signal due to aliasing [32]. Another form of aliasing occurs if the signal spectrum had some noise or unwanted content beyond f_B. Once sampled, this noise is folded back into the range $\{-f_S/2, f_S/2\}$, thus corrupting the signal. Hence the use of anti-aliasing filters, as shown in Fig. 4, is desirable before an ADC in systems where the signal is noisy or contains unwanted content beyond the bandwidth of interest f_B.
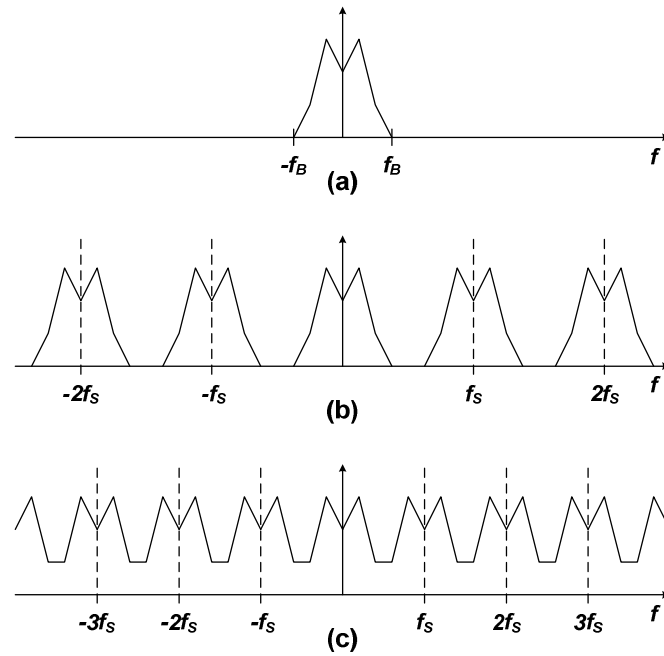
Fig. 5. Signal spectra, (a) before sampling, (b) after sampling with $f_S > 2f_B$, (c) after sampling with $f_S < 2f_B$.
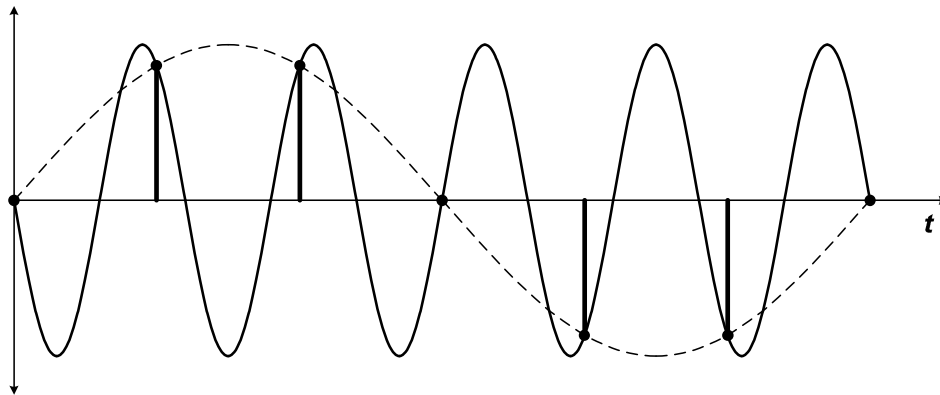
Fig. 6. Samples (dots) of original signal (solid) producing aliased signal (dashed).

B. Quantization

Digital data are discrete in magnitude; this is the result of quantization. Quantization is perhaps the fundamental differentiating feature between analog and digital data. While analog data can take any value within a specified range, digital data can only assume fixed and predetermined values within the same range. This was presented in Fig. 3 (right), where the sampled data do not necessarily take the same magnitude as the analog data, but the closest predetermined value that causes the least amount of error.

(a)

(b)
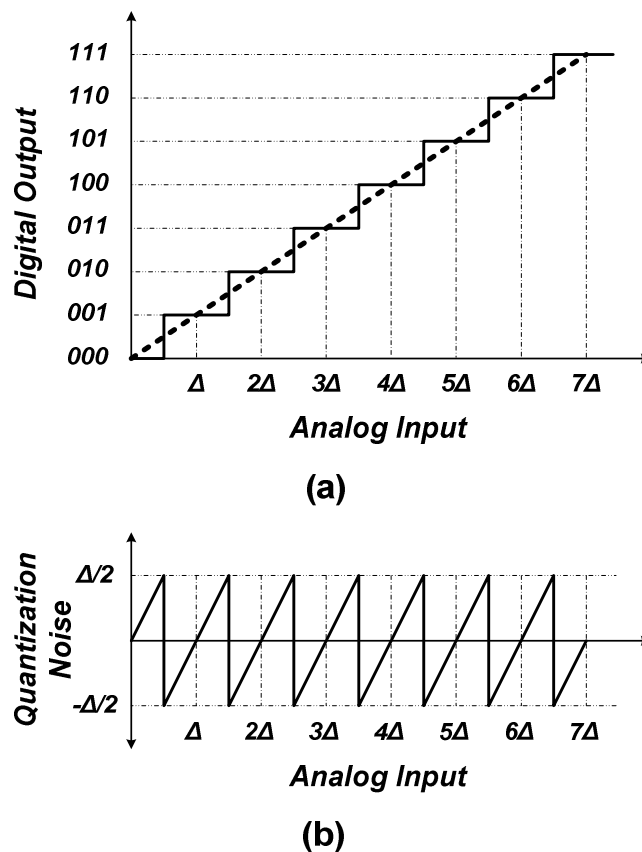
Fig. 7. Ideal characteristic of a 3bit ADC; (a) mapping function,
(b) quantization noise.

The ideal characteristic mapping function of a 3bit ADC and its quantization error are given in Fig. 7. The main principal of the quantization process is to place the analog input in predefined bins of width Δ corresponding to a single digital code with a maximum absolute error of $\Delta/2$ or ½ *LSB*. The errors introduced to the signal in the process are referred to as quantization noise. Under the assumptions that all quantization levels are exercised with equal probability independent of the input and that a large number of uniform quantization levels are used, the quantization noise power can be expressed by (3) [33]. These assumptions, while inaccurate, provide a very good approximation for resolutions greater than 4bits.

$$P_Q = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e_q^2 \cdot de_q = \frac{\Delta^2}{12} \tag{3}$$

C. Static ADC Metrics

ADCs implemented in silicon do not share the ideal characteristics shown in Fig. 7. Several performance metrics are used to measure an ADC's deviation from its ideal characteristic, and here we discuss some of the static metrics which measure the ADC's performance independent of time or the input signal. A depiction of these metrics is given in Fig. 8.

A transfer characteristic of an ADC such as the one in Fig. 8 can be obtained using a slow ramp signal for the input that spans the whole range of the ADC. The ramp needs to be slow enough such that each code is hit 10s or 100s of times. The collected

data can then be plotted such that the number of hits per code represents the code width. The ideal code width can also found from the speed of the ramp.
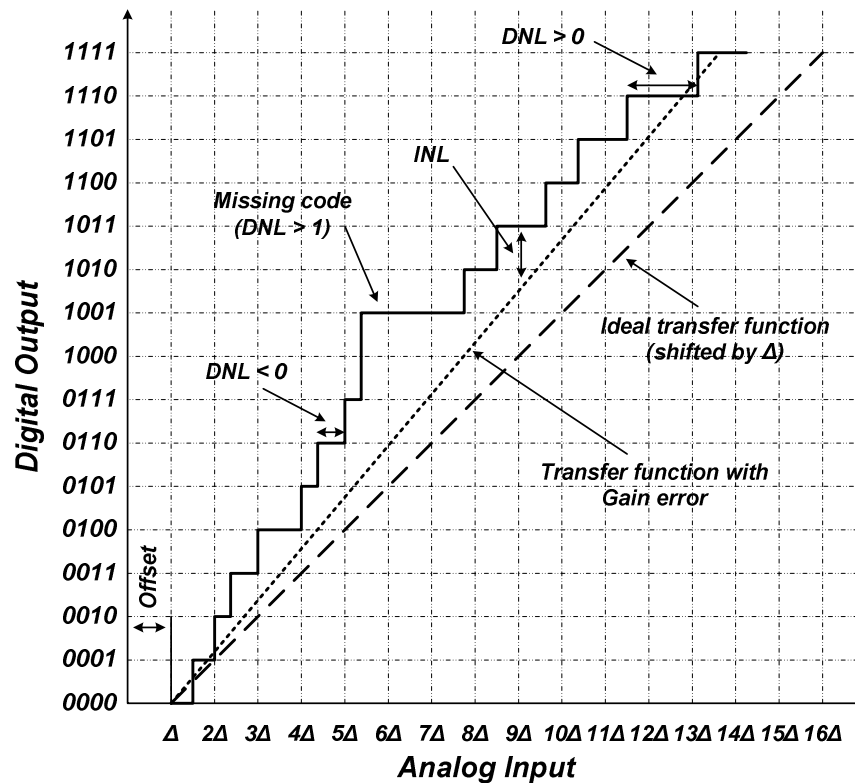
Fig. 8. Static errors in a 4bit ADC.

1. Gain

A gain error is a deviation in the slope of the real transfer characteristic of an ADC from the ideal transfer characteristic. The most practical method to evaluate the gain error is using the endpoint-fit line of the ADC output, as it can provide insight into the ADC dynamic performance. Another method of evaluating the gain error is the best-line fit of the transfer characteristic, which generally yields a smaller gain error value.

2. Offset

The offset changes the ADC transfer function by shifting the code transition points by the offset's value. The offset is simply measured by extracting the horizontal intercept of the first code transition less ½ *LSB*.

3. Differential Nonlinearity (DNL)

A deviation in the real code width from the ideal code width *Δ*, 1 *LSB*, in the transfer function of an ADC constitutes a *DNL* error. *DNL* is measured after the gain and offset errors are compensated for in the real transfer characteristic of the ADC. In severe cases where the *DNL* exceeds 1 *LSB*, some digital codes cannot be represented by any analog input—missing codes—and the ADC effectively loses 1bit of resolution. Therefore, practical ADCs are designed with a *DNL* range of {-½ *LSB*, ½ *LSB*}.

4. Integral Nonlinearity (INL)

The *INL* is the summation of buildup of *DNL* over the span of the ADC transfer function. It can be evaluated using (4). Note that if the endpoint-fit line method was used to evaluate the gain error, $INL_1 = INL_{2^N-1} = 0$, and the shape of the *INL* plot could accurately predict some of the dynamic performance metrics of the ADC [34]-[35].

$$INL_k = \sum_{l=1}^{k} DNL_l \qquad (4)$$

D. Dynamic ADC Metrics

The dynamic performance of an ADC is strongly related to the input signal bandwidth and conversion speed, and hence its dynamic metrics are generally evaluated for a specific set of conditions. The overall dynamic performance of the ADC is then performed by adjusting a single variable in the set of conditions, and repeating the measurement until the whole ADC range is characterized. A graphical representation of some of the most frequently used dynamic measurements is given in Fig. 9.
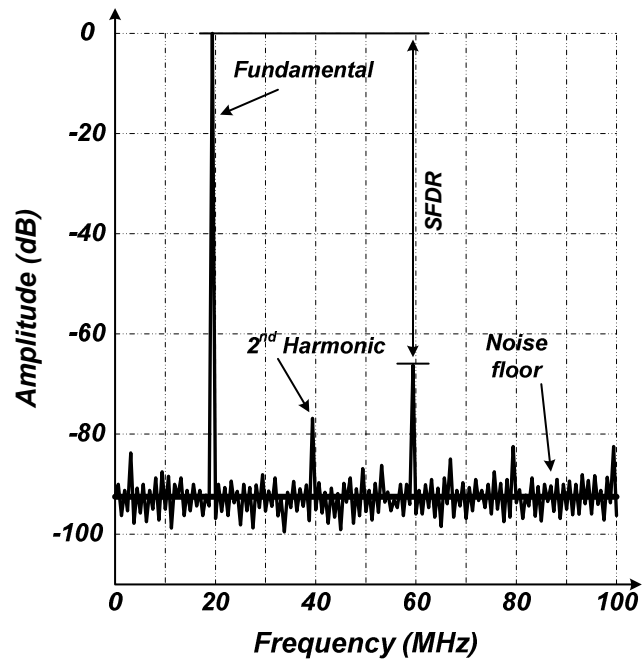
Fig. 9. A spectrum of a non-ideal 10bit ADC.

1. Signal to Noise Ratio (SNR)

Spectral noise of the ADC is the random fluctuations that determine the smallest

detectable signal. In Fig. 9 the noise floor level is roughly -92dB; any signal below this level is undetectable. The *SNR* is the ratio between the power of the *FS* signal, generally a sinusoid, and the total noise generated by the ADC within the bandwidth of interest. The errors induced by the quantization process set the limit for *SNR* and the signal to quantization noise ratio can be evaluated using (5).

$$SNR_Q = 10\log\frac{V_{FS}^2/2}{\Delta^2/12} \cong 6.02N + 1.76 \quad [dB] \tag{5}$$

2. Signal to Noise and Distortion Ratio (SNDR)

The ADC spectrum of Fig. 9 contains spurs that rise above the noise floor. These spurs are classified as distortion. In general distortion is harmonic to the fundamental, occurring at integer multiples of the fundamental frequency. The quality of the ADC output signal is degraded by distortion. This degradation can be quantified using *SNDR*. Similar to the *SNR*, the *SNDR* measures the ratio of *FS* signal power with respect to combined power of noise and distortion components.

3. Spurious Free Dynamic Range (SFDR)

The ratio of *FS* signal root-mean-square (rms) value to the rms value of the highest spur in the ADC spectrum is the *SFDR*. This is generally, but not necessarily, equivalent to the ratio of the fundamental to the 3rd harmonic component in fully-differential ADCs.

4. *Effective Number of Bits (ENOB)*

For a noiseless ADC—apart from quantization noise—the *SNR* given by (5) will show that the ADC effectively has *N* bits of resolution. However, the noise and distortion added by the ADC components result in a smaller value for *SNR* and *SNDR* than that predicted by (5). This translates into an effectively lower resolution than what the ADC was designed for. By equating either *SNR* or *SNDR* to SNR_Q given by (5) and solving for *N* we can determine the *ENOB* as in (6) of the ADC. The *ENOB* of practical ADCs is within 1bit of what the ADC was designed for.

$$ENOB = \frac{SNDR - 1.76}{6.02} \tag{6}$$

E. *ADC Architectures*

While ADC characterization is virtually the same for all ADCs, ADC architectures differ according to their respective applications. ADCs can be divided into two major groups from an operation standpoint: oversampling ADCs and Nyquist Rate ADCs. Oversampling ADCs, as the name implies, use a clock frequency $f_S >> 2f_B$. The result is a significantly lower noise floor compared to Nyquist rate ADCs, which benefits the ADC *SNR* and dynamic range and increases its resolution beyond 16bits [36]. This, however, is at the expense of a very narrow signal bandwidth and hence finds use primarily in high fidelity audio systems and some communication and medical systems.

Nyquist rate ADCs follow the Nyquist-Shannon sampling theorem and hence their bandwidth is solely dependent on how fast can a signal be accurately sampled for a

desired resolution, which in turn is limited by the technology process used. These ADCs can be further divided into two sub-groups: single-step and multi-step conversion ADCs, where the first sub-group is predominately based on the Flash architecture and the second on Sub-Ranging architectures such as successive approximation, time-interleaved and pipeline ADCs [37], where the latter is the main focus of this dissertation.

CHAPTER III

PIPELINE ADCS

Pipeline ADCs are Nyquist rate data converters that are able to achieve resolutions up to 14bits and sampling rates beyond 100MHz while maintaining a high *SNDR* and *SFDR* performance. They are ideal for many applications such as instrumentation (digital oscilloscopes, spectrum analyzers, and medical imaging), communications (video, radar and software radio), and consumer electronics (digital cameras, flat panel displays and high-definition TV). This extensive range of applications along with the design challenges posed by modern day CMOS technologies had been a motivating force behind developing new techniques to enhance the overall performance of pipeline ADCs, particularly its power consumption. In this chapter the pipeline ADC architecture is introduced and the limiting attributes of its building components are highlighted. This is done in an effort to propose new design techniques that can be applied in a low voltage environment and build a pipeline ADC that is very competitive with the state-of-the-art implementations in literature [13], [15], [16], [23], [26].

A. *Pipeline ADC Architecture*

The conceptual block diagram of Fig. 10 describes the basic architecture of a pipeline ADC with a resolution of *N* bits. It consists of a front-end sample and hold (S/H), several pipeline stages (or cells) and a digital decoder. Each pipeline stage

resolves *M* bits using a sub-ADC where $M < N$. The digital to analog converter (DAC)

converts the *M* bits back to analog and the result is subtracted from the original signal

thus generating a residue. This residue represents the signal portion not yet resolved by

the ADC and is passed on to the following stage for further processing. An amplification

$G = 2^M$ is applied to the residue to keep its dynamic range equal to the full scale signal,

V_{FS}. This is necessary to allow the use of the same reference voltages in all stages for

simplicity, and to also relax the design requirements of the sub-ADCs in subsequent

stages given that otherwise the residue gets too small to process. At the end of

conversion, the *M* bits resolved by each pipeline stage are decoded with appropriate

delays corresponding to each stage and synchronized to form the *N* bits of the ADC.
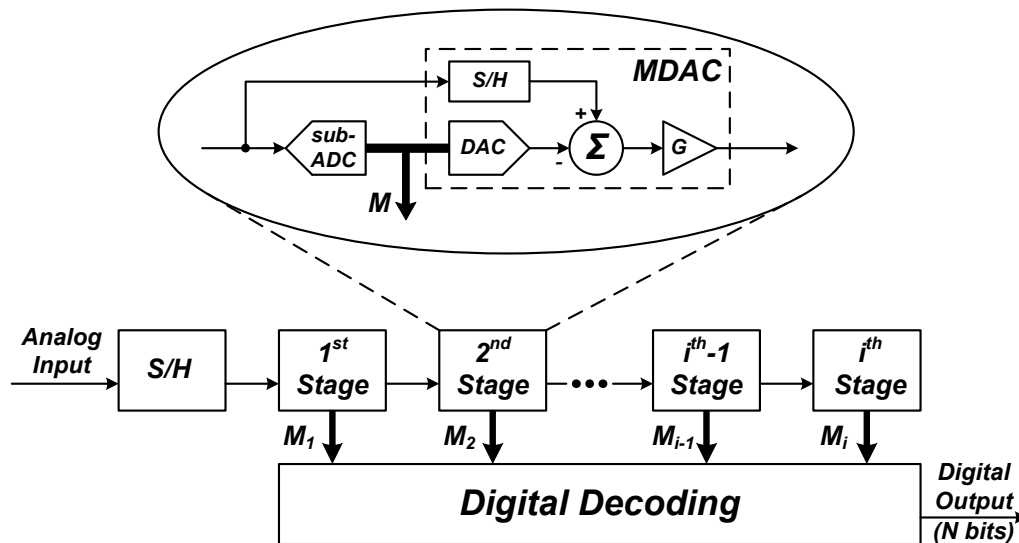
Fig. 10. The basic architecture of a pipeline ADC.

Despite its sequential manner of data conversion, the speed of the pipeline ADC is not adversely affected. The use of a S/H in each stage ensures that a new signal sample can be acquired every clock cycle while the older samples progress down the pipeline, hence the name. This processing scheme is illustrated in Fig. 11. There is a time latency at startup, however, which amounts to the clock cycles needed to fill up the pipeline. Henceforth, the pipeline ADC generates a new output for every clock cycle.

S/H	$V_{in}(n)$	$V_{in}(n+1)$	$V_{in}(n+2)$				
1st Stage	$M_1(n-1)$	$M_1(n)$	$M_1(n+1)$		$M_1(n+i-3)$		
2nd Stage	$M_2(n-2)$	$M_2(n-1)$	$M_2(n)$		$M_2(n+i-4)$	$M_2(n+i-3)$	
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\cdots$	$\vdots$	$\vdots$	$\vdots$
$i\text{-}1^{th}$ Stage		$M_{i-1}(n-2)$	$M_{i-1}(n-1)$		$M_{i-1}(n)$	$M_{i-1}(n+1)$	$M_{i-1}(n+2)$
i^{th} Stage			$M_i(n-2)$		$M_i(n-1)$	$M_i(n)$	$M_i(n+1)$
Output					$N(n-2)$	$N(n-1)$	$N(n)$

$nT_S \qquad (n+1)T_S \quad (n+2)T_S \quad \cdots \quad (n+i-2)T_S \quad (n+i-1)T_S \quad (n+i)T_S$

Fig. 11. Staggered signal processing scheme of pipeline ADCs.

There are many variants to the pipeline ADC configuration of Fig. 10. Particularly, the number of bits resolved in each stage is not necessarily kept the same, and modifying the division of bits among stages can have a significant impact on the overall ADC performance as will be demonstrated in later sections. Also, the last stage is typically implemented using only a sub-ADC, or low resolution Flash ADC, since there is no need to generate a residue.

1.   1.5bits/Stage Pipeline Cell

The most fundamental pipeline stage implementation commonly used for high speed is the 1.5bits/stage cell. It is shown in Fig. 12 side by side next to its predecessor the 1bit/stage pipeline cell. The sub-ADCs are implemented using comparators. The S/H, DAC, summation and residue amplification are implemented using the SC amplifier, which makes the multiplying DAC (MDAC). The ideal transfer functions of the 1bit/stage and 1.5bits/stage pipeline cells are given by (7) and (8) respectively, where V_R is a reference voltage. The reference voltage, V_R, also defines the full scale range; V_{FS} $= 2V_R$. Moreover, the capacitor values here are nominally equal to implement a gain G of 2; $C_1 = C_2 = C$.

$$
V_{OUT} = \begin{cases} V_{IN}\left(1+\dfrac{C_2}{C_1}\right)+V_R\dfrac{C_2}{C_1} \;, & V_{IN} < 0 \\[3mm] V_{IN}\left(1+\dfrac{C_2}{C_1}\right)-V_R\dfrac{C_2}{C_1} \;, & V_{IN} > 0 \end{cases}
\tag{7}
$$

$$
V_{OUT} = \begin{cases} V_{IN}\left(1+\dfrac{C_2}{C_1}\right)+V_R\dfrac{C_2}{C_1} \;, & V_{IN} < -\dfrac{V_R}{4} \\[3mm] V_{IN}\left(1+\dfrac{C_2}{C_1}\right) \;, & -\dfrac{V_R}{4} < V_{IN} < \dfrac{V_R}{4} \\[3mm] V_{IN}\left(1+\dfrac{C_2}{C_1}\right)-V_R\dfrac{C_2}{C_1} \;, & V_{IN} > \dfrac{V_R}{4} \end{cases}
\tag{8}
$$
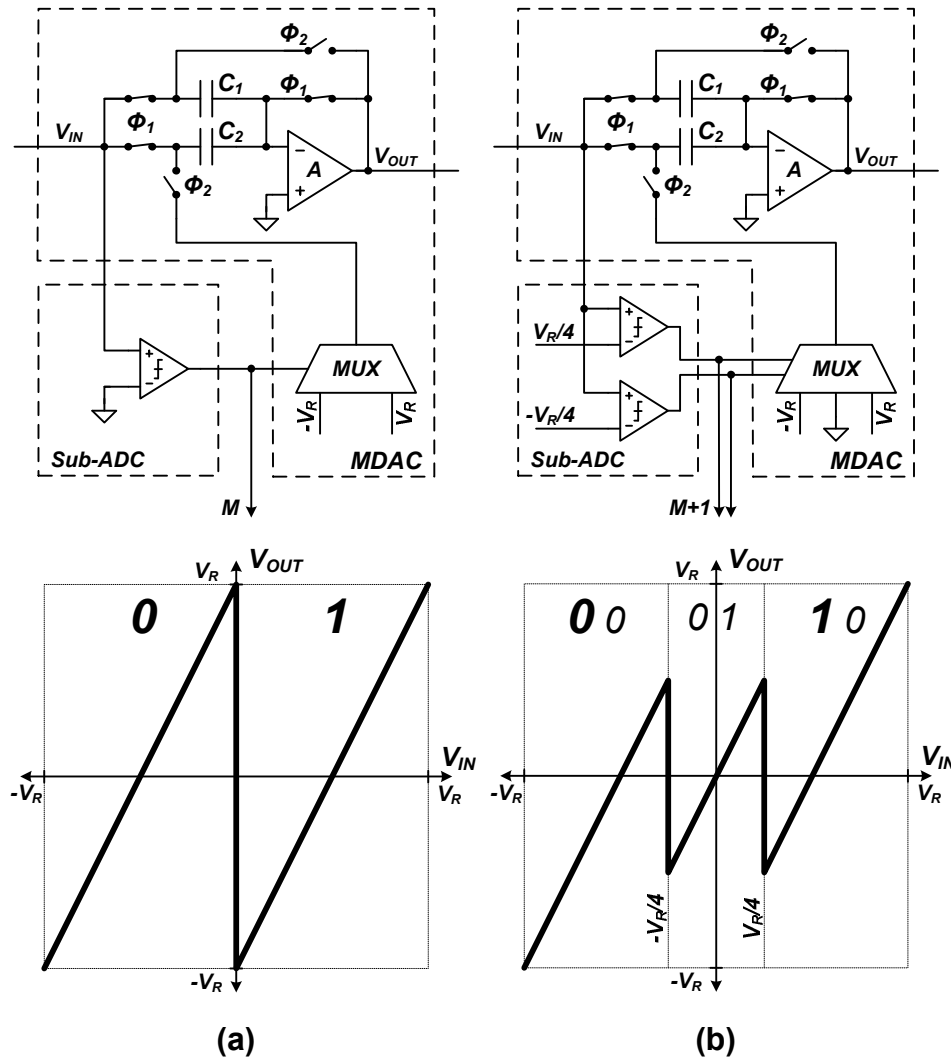
Fig. 12. Pipeline cell implementation and transfer function, (a) 1bit/stage and (b) 1.5bits/stage.

In reality, the transfer functions of (7) and (8) suffer errors from imperfections in circuit implementation. For example, suppose the decision level of the 1bit/stage is shifted by δ due to a comparator offset, then the output exceeds the $\{-V_R, V_R\}$ range by 2δ. If the error 2δ is greater than the quantization noise of the remaining stages, $V_R/2^{Nr}$ ($\frac{1}{2}$ *LSB*), where *Nr* is the resolution of the remaining pipeline stages, a conversion error

occurs and the resolution of the whole ADC is reduced. Hence, such an error is most severe in the early stages of the ADC. On the other hand, the 1.5bits/stage shifts the original decision level and adds another to avoid exceeding the output range. By choosing the decision levels $\pm V_R/4$, the immunity of the 1.5bits/stage against comparator offsets is maximized. The transfer functions of the 1bit/stage and 1.5bits/stage including offsets in the sub-ADC are shown in Fig. 13; offsets as large as $V_R/4$ can be tolerated in 1.5bits/stage without exceeding the range $\{-V_R, V_R\}$.
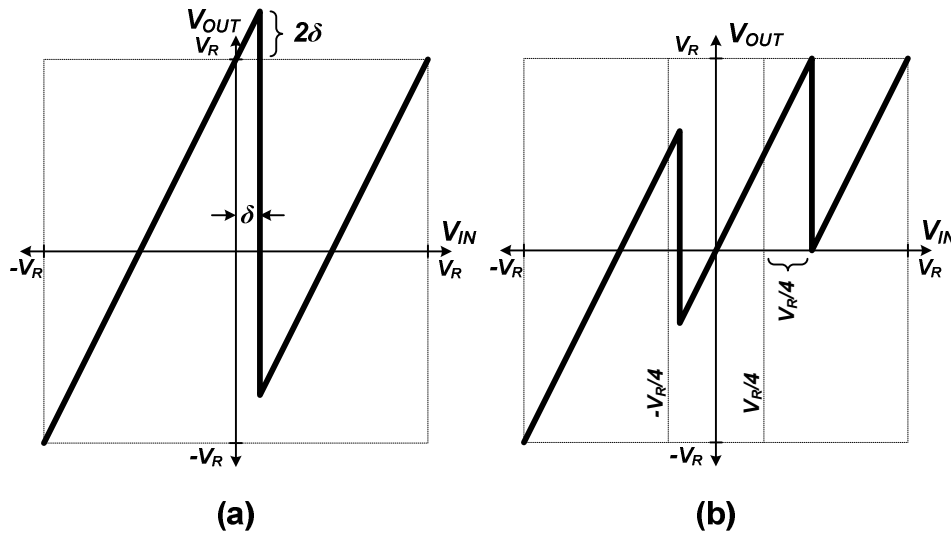
Fig. 13. Sub-ADC offset effects on (a) 1bit/stage and (b) 1.5bits/stage pipeline cells.

The use of an additional decision level in the 1.5bits/stage is called digital correction [38], and ADCs utilizing this correction method are named redundant signed digit (RSD) ADCs [39]. The correction is realized in the fact that the stage now gives 2 bits instead of 1. These 2 bits, however, are incomplete as not all 2 bit levels are used in

the 1.5bits/stage. The most significant bit (MSB) is the actual bit resolved, while the *LSB* acts as an uncertainty flag; codes **0**0 and **1**0 are a certain 0 and 1 respectively, but 01 denotes a result needing further processing. If an uncertainty arises from an input within $\pm V_R/4$ but close to either decision level, it may quickly be resolved by the next stage, but an uncertainty arising from an input closer to 0 may need the whole pipeline to resolve it. Also, as 1 bit is used for correction, the gain of the stage *G* (Fig. 10) remains 2^M instead of 2^{M+1}. Finally, the digital decoding and correction process is a weighted summation of the *M+1* bits from all stages for a given input sample and is depicted in Fig. 14 for a 4-stage 4bit pipeline ADC with a single comparator for the last stage.

Stage	2^3	2^2	2^1	2^0		*Stage*	2^3	2^2	2^1	2^0
M_1	X					M_1	X	X		
$+ M_2$		X				$+ M_2$		X	X	
$+ M_3$			X			$+ M_3$			X	X
$+ M_4$				X		$+ M_4$				X
N	X	X	X	X		N	X	X	X	X
	(a)						(b)			

Fig. 14. Summation of stage bits to make output code of a 4bit ADC; (a) 1bit/stage and (b) 1.5bits/stage.

2. *Higher Resolutions/Stage*

Digitally corrected pipeline stages with higher bit resolutions are possible and are often used in higher resolution ADCs (12-14bits). They are easily derived from the original cells without digital correction by adding additional comparators to the sub-

ADC, and evenly separating their decision levels by $V_R/2^M$ symmetrically around 0 input. A 2.5bits/stage pipeline cell is presented in Fig. 15 with its ideal transfer function, which is given in (9). While higher resolutions/stage offers attractive benefits as will be demonstrated later, two main aspects need to be considered in their implementation. First, increasing the number of comparators means power-efficient designs need to be adopted. Second, the immunity against sub-ADC errors is reduced.
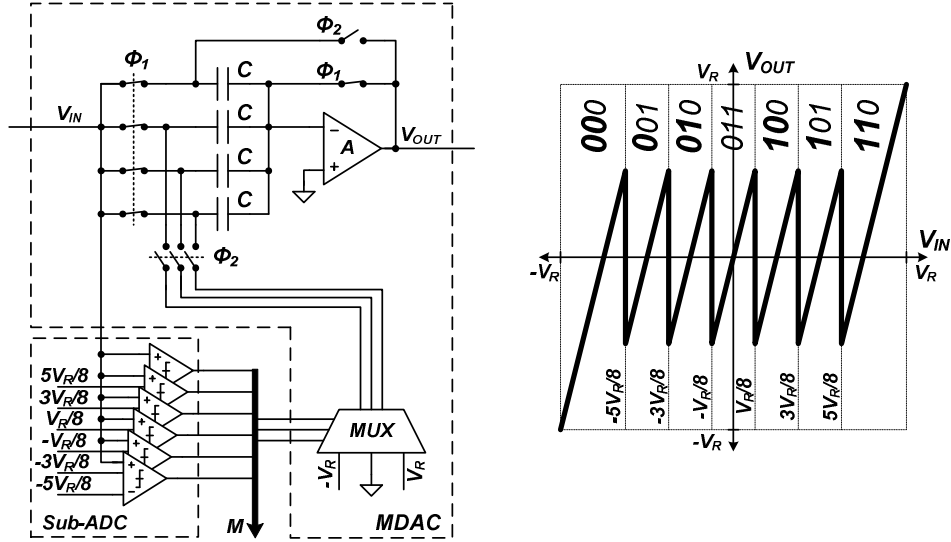
Fig. 15. A 2.5bits/stage pipeline cell implementation and transfer function.

$$V_{OUT} = \begin{cases} 4V_{IN} + 3V_R \ , & V_{IN} < -5V_R/8 \\ 4V_{IN} + 2V_R \ , & -5V_R/8 < V_{IN} < -3V_R/8 \\ 4V_{IN} + V_R \ , & -3V_R/8 < V_{IN} < -V_R/8 \\ 4V_{IN} \ , & -V_R/8 < V_{IN} < V_R/8 \\ 4V_{IN} - V_R \ , & V_R/8 < V_{IN} < 3V_R/8 \\ 4V_{IN} - 2V_R \ , & 3V_R/8 < V_{IN} < 5V_R/8 \\ 4V_{IN} - 3V_R \ , & V_{IN} > 5V_R/8 \end{cases} \qquad (9)$$

B. Implementation of Pipeline Stages

The following sub-sections treat the implementation of the front-end S/H and the individual pipeline stages. The topologies most commonly used to realize these functions are presented, and whenever applicable the limitations or concerns regarding their performance in low voltage environments are addressed.

1. Front-End S/H

The front-end S/H is a SC circuit that relies greatly on the performance of amplifier used to implement it. Here we examine the topology from a functional standpoint; the effects of amplifier non-idealities are examined in section *C*, while their physical sources, low voltage limitations and the amplifier architectures best suited for pipeline ADCs are discussed in detail in Chapter IV.

The flip-around S/H [40] is perhaps the most adopted architecture for the pipeline ADC front-end. It is given in Fig. 16 in the single-ended form along with the non-overlapped clock phases used to perform its function and operates as follows. During the sampling phase, Φ_1, the amplifier is reset providing a virtual ground at *x*, and the input is sampled on C_{SH}. Hence, the charge stored on C_{SH} by the end of Φ_1 referenced to *x* is given by (10). In the holding phase, Φ_2, C_{SH} is flipped-around and connected to the output. The charge stored on C_{SH} by the end of Φ_2 referenced to *x* is now given by (11). Since there is no discharge path for C_{SH} between Φ_1 and Φ_2, the charge is conserved and the output can be expressed by (12). As for the early falling-edge phase, Φ_{1e}, it is used to implement a technique commonly known as bottom-plate sampling; it

defines the sampling moment and effectively minimizes switching errors associated with charge injection and clock feed through, especially in fully-differential implementations.
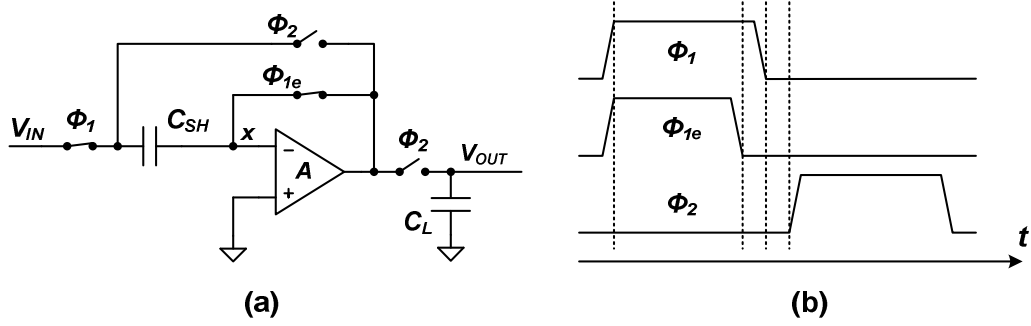
Fig. 16. The flip-around S/H; (a) circuit realization and (b) non-overlapped clocking scheme.

$$q_{\Phi 1} = C_{SH} V_{IN} \tag{10}$$

$$q_{\Phi 2} = C_{SH} V_{OUT} \tag{11}$$

$$q_{\Phi 1} = q_{\Phi 2} \quad \Rightarrow \quad V_{OUT} = V_{IN} \tag{12}$$

There are several benefits to the flip-around S/H that led to its popularity. The resetting of the amplifier during Φ_1 samples the amplifier offset on C_{SH}, which is then effectively cancelled in Φ_2; this is known as direct auto-zeroing [41]. Another benefit is the relaxation of the amplifier slew rate requirement for Nyquist-rate input signals; the resetting of the amplifier in Φ_1 ensures a maximum step of half the full-scale input between consecutive samples, while track and hold circuits or S/H with previous output memory experience a full-scale step between samples at Nyquist-rate. Finally, during Φ_2 the amplifier feedback factor is almost unity, which reduces its bandwidth requirement.

2. Sub-ADC

The sub-ADC can be divided into two parts, analog and digital. The analog part is implemented using comparators, which generate a thermometer code representing the position of the input with respect to pre-set voltage references; the circuit realization and design considerations of comparators are presented in detail in Chapter VII. As for the digital part of the sub-ADC, it is a simple thermometer-to-binary decoder. The complete implementation of a 1.5bits/stage sub-ADC showing the thermometer-to-binary decoder is depicted in Fig. 17, and a truth table of the logic is given in Table 1.
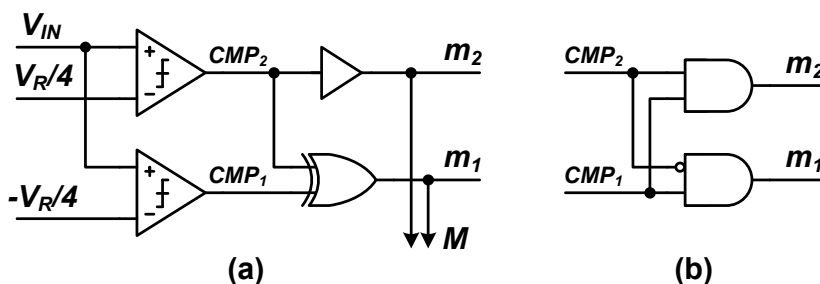
Fig. 17. A 1.5bits/stage sub-ADC, (a) circuit realization and (b) an alternative thermometer-to-binary decoder.

TABLE 1
A 1.5BITS/STAGE LOGIC TABLE

CASE	V_{IN}	CMP_2	CMP_1	M_2	M_1
1	$V_{IN} < -V_R/4$	0	0	0	0
2	$-V_R/4 < V_{IN} < V_R/4$	0	1	0	1
3*	$V_{IN} < -V_R/4,\ V_{IN} > V_R/4$	1	0	X (0)	X (1)
4	$V_{IN} > V_R/4$	1	1	1	0

* Not feasible, but can simplify logic implementation if used; X = don't care.

3. MDAC

The MDAC in Fig. 10 acts as a DAC, S/H, adder and gain stage. For the 1.5bits/stage pipeline cell given in Fig. 12(b), the DAC can be realized as shown in Fig. 18 following the logic of Table 2. Note that the implementation of the switch signals S_2 and S_3 overlap with m_1 and m_2 from the sub-ADC.
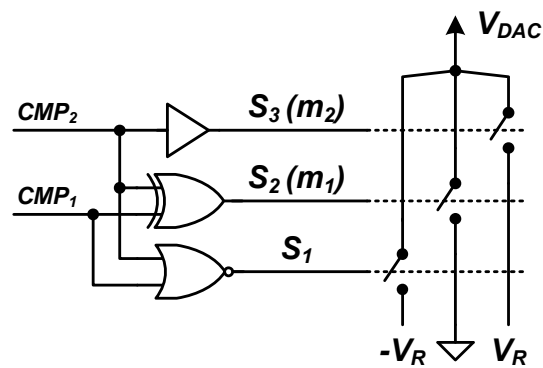
Fig. 18. A 1.5bits/stage DAC.

TABLE 2
A 1.5BITS/STAGE DAC LOGIC TABLE.

CMP_2	CMP_1	S_3	S_2	S_1	V_{DAC}
0	0	0	0	1	$-V_R$
0	1	0	1	0	0
1	1	1	0	0	V_R

As for the S/H, adder and gain stage, they are all embedded in the SC amplifier of Fig. 19(a); the individual functions are depicted in Fig. 19(b-d). The SC amplifier uses the same non-overlapped clocking scheme of Fig. 16(b), and its operation is described as

follows with all charge referenced to the virtual ground node x. In Φ_1 the input V_{IN} is sampled on C_1 and C_2 as shown in Fig. 19(b), and the total stored charge at the end of this phase is given by (13). In Φ_2 the amplifier is reconfigured; C_1 is connected to the amplifier output, while C_2 is connected to the DAC output, V_{DAC}. The total stored charge at the end of Φ_2 is given by (14). While the charge stored on C_1 and C_2 has changed between Φ_1 and Φ_2, no charge has been lost or added to the system and hence the change in charge is attained by redistribution. By charge conservation, the transfer function of the SC amplifier is expressed by (15), which demonstrates the gain applied to V_{IN}, the inversion of V_{DAC} and their summation. For the 1.5bits/stage pipeline cell, C_1 and C_2 are nominally equal to achieve a gain of 2.
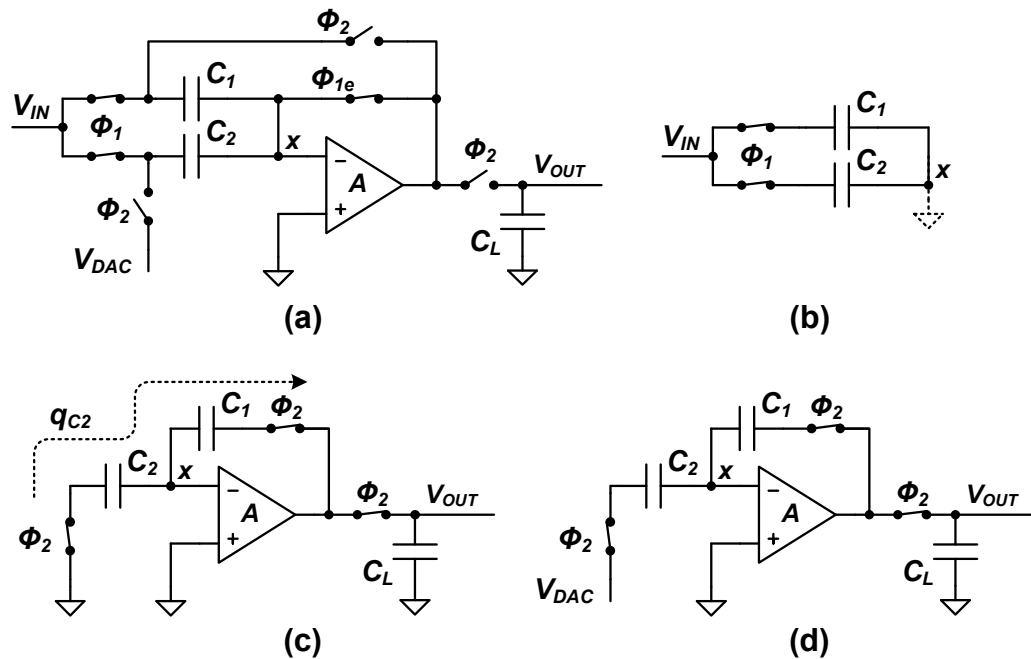
Fig. 19. SC amplifier used in 1.5bits/stage MDAC; (a) overall SC amplifier, (b) S/H function in Φ_1, (c) gain stage by charge redistribution in Φ_2 and (d) inversion of V_{DAC} and addition to V_{IN} when super-positioned on (c).

$$q_{\Phi 1} = \begin{cases} q_{C1,\Phi 1} = C_1 V_{IN} \\ q_{C2,\Phi 1} = C_2 V_{IN} \end{cases} \tag{13}$$

$$q_{\Phi 2} = \begin{cases} q_{C1,\Phi 2} = C_1 V_{OUT} \\ q_{C2,\Phi 2} = C_2 V_{DAC} \end{cases} \tag{14}$$

$$\Delta q_{C1} + \Delta q_{C2} = 0 \quad \Rightarrow \quad V_{OUT} = V_{IN}\left(1 + \frac{C_2}{C_1}\right) - V_{DAC}\frac{C_2}{C_1} \tag{15}$$

The same result in (15) can be obtained by applying superposition and considering V_{IN} and V_{DAC} individually. Considering V_{IN} only, the amplifier is configured in Φ_2 as shown in Fig. 19(c), and C_2 is discharged. However, x acts as a virtual ground and the charge is not lost, but transferred to C_1. Now C_1 holds the charge of C_1 and C_2 from the previous phase, which generates to a higher voltage across C_1, and hence V_{IN} is amplified by $(C_1 + C_2)/C_1$. Now considering V_{DAC} only, the amplifier is configured in Φ_2 as shown in Fig. 19(d), which is an inverting topology with gain $-C_2/C_1$. By adding the outputs of each scenario, the transfer function is identical to that given by (15).

The SC amplifier in Fig. 19(a) shares many benefits with the flip-around S/H in Fig. 16(a); this is expected since the flip-around S/H is a special case of the SC amplifier in Fig. 19(a) with $C_2 = 0$. Nonetheless, they also share the same low voltage limitation. The direct auto-zeroing technique used in these circuits to cancel the amplifier offset relies on the input and output common modes of the amplifier to be the same. Low voltage applications (1.2V), however, dictate different input and output common modes, where the first is set to optimize the amplifier for speed and the latter for signal swing.

Hence, direct auto-zeroing cannot be used. This is explored further in Chapter VI, where a dual level common mode feedback (CMFB) is proposed to alleviate this issue and reinstate the use of the direct auto-zeroing technique to cancel the amplifier offset. Other amplifier limitations and their effects on the MDAC performance are examined in section *C*.

4. Switches

Switches are a fundamental component of SC circuits and play a significant role in their performance. The simplest implementation of a switch is a single MOS device, as depicted in Fig. 20. The *ON* phase Φ_1 is an active high (V_{DD}) or active low (*GND*) for an NMOS and PMOS switches respectively. When the switch is *ON*, the MOS device operates in the linear region and its resistance R_{ON} is expressed by (16) for an NMOS, where *W* and *L* are the device dimensions, C_{ox} is the oxide capacitance, μ is the carrier mobility, V_{GS} is the gate to source voltage and V_T is the threshold voltage.
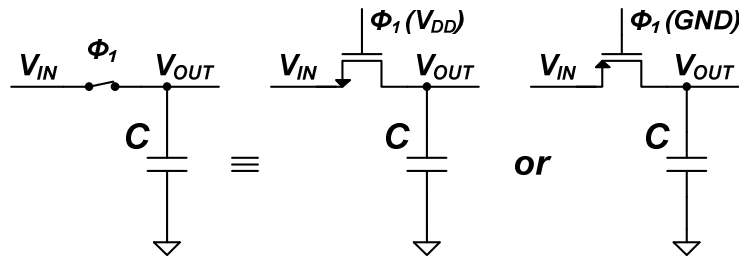
Fig. 20. Switch implementation using a single MOS device.

$$R_{ON} = \frac{L}{\mu_N C_{ox} W (V_{GS} - V_T)} \tag{16}$$

While the realization of switches as in Fig. 20 is straight-forward, their implementation in modern CMOS technologies poses many challenges. Here we discuss the most fundamental challenge: to turn the switch on; the effects of switches on performance are reserved for section *C*.

The minimum requirement for a MOS switch to turn on is $V_{GS} > V_T$. This means, and according to Fig. 20, that V_{IN} needs to be at least a V_T below V_{DD} for an NMOS, or a V_T above *GND* for a PMOS. The low voltage supplies imposed by modern CMOS technologies severely limit the input range satisfying these conditions such that a simple implementation MOS switches as in Fig. 20 is no longer feasible; this is depicted in Fig. 21 where both NMOS and PMOS switches are *OFF* around the ideal signal range centered around $V_{DD}/2$.
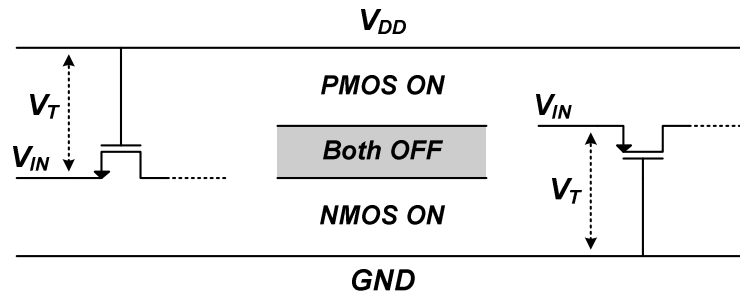
Fig. 21. Low voltage limitations on single MOS switches.

Several techniques have been developed to tackle this limitation, and the bootstrapping technique is quite possibly the most utilized [42]. Conceptually, the bootstrapping technique is presented in Fig. 22(a). When the switch is turned on in Φ_1, the pre-charged capacitor C_B is applied across the gate and source of M_{SW} thereby fixing

its V_{GS} to V_{DD} as shown in Fig. 22(b). This enables V_{IN} to take any value in the {*GND*, V_{DD}} range without turning off the switch. Moreover, not only does the use of bootstrapping minimize R_{ON} by maximizing V_{GS}, but also helps keep its value fixed for any V_{IN} and hence reduce its non-idealities. However, bootstrapping comes with a high price; every bootstrapped switch needs an independent C_B, which is fairly sizable (>0.5pF) to maintain a steady voltage. Nevertheless, bootstrapping is indispensable for high resolution (12-14bits) pipeline ADCs.
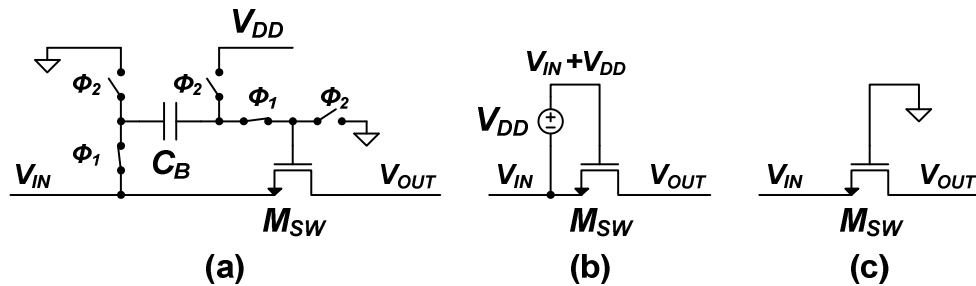
Fig. 22. Bootstrapped switch; (a) conceptual implementation, (b) *ON* operation in Φ_1 and (c) *OFF* operation in Φ_2.

Another technique, which is more technology based, is the use of dual gate oxide (DGO) processes. In these processes, two types of MOS devices are used, where one is optimized for speed and low voltage operation (thinner oxide), and the other is optimized for input/output (I/O) interfaces and can tolerate higher voltage stresses (thicker oxide). Some examples are the 65nm/90nm/130nm CMOS in 1.2/2.5V and 0.18µm CMOS in 1.8/3.3V. Therefore, the switch and its clocking scheme can be implemented with I/O devices, while the rest of the analog blocks are implemented with

low voltage devices as shown in Fig. 23(a). While the implementation is not costly since both MOS device masks are standard is the process, the I/O devices have smaller μ_N and larger V_T, which makes it difficult to minimize R_{ON} without using large dimensions. Moreover, R_{ON} is not fixed with V_{IN} swing as V_{GS} is not constant. These shortcomings limit the use to 8-10bits of resolution.

On the other hand, regulated power supplies as proposed in [13] and [23] may be used. Although the use of the technique as depicted in Fig. 23(b) is not how it was intended in [13] and [23], the basic principle is to provide a supply level $V_{DD,R}$ that is higher than the low voltage supply, $V_{DD,L}$ (V_{DD} in Fig. 21). Hence, the useful range of the low voltage MOS device is extended without excessive oxide stress. This approach reclaims many benefits of using the fast low voltage MOS device as a switch, but R_{ON} still varies with V_{IN} and the resolution is limited to less than 12bits.
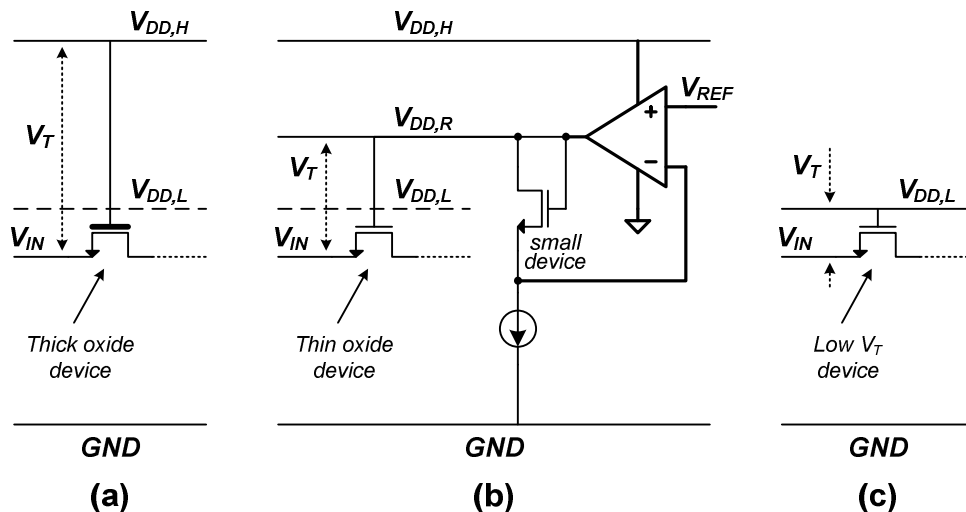
Fig. 23. Other MOS switch implementations using (a) an I/O device, (b) a regulated supply and (c) a low V_T device.

Finally, and in recent years, low V_T devices have been adopted as switches in pipeline ADCs [15], and their use is shown in Fig. 23(c). The robustness of the low V_T MOS devices may still be a topic for debate, but certainly has improved as they are becoming standard devices with the increased integration of systems on single chips. Nonetheless, they still suffer the same variable R_{ON} as the previously discussed techniques. With proper sizing, resolutions up to 10bits may be attainable.

In summary, the bootstrapped switch is still the best option as far as linearity (up to +14bits) and robustness are concerned. However, if the target resolution is below 12bits, then the techniques in Fig. 23 may provide a cheaper, but reliable, alternative solutions.

C. Performance Limitations

The non-idealities of the SC circuit components used to implement the front-end S/H and MDAC can introduce conversion errors that limit the performance of the pipeline ADC. The main causes for such errors are the capacitor mismatch, finite amplifier gain, finite amplifier bandwidth, amplifier offset, distortion and finite switch resistance. The following sub-sections the effects of each on the transfer function of a 1.5bits/stage pipeline cell are examined, and the minimum requirements for the first stage MDAC in a 1Vpp 10bit 160MS/s pipeline ADC are evaluated. Also, graphical representations of the effects on the 1bit/stage will be included to aid the discussion. The physical sources of amplifier non-idealities and the low voltage challenges of implementing robust amplifiers are discussed in detail in Chapter IV.

1. Capacitor Mismatch

The capacitors used in 1.5bits/stage pipeline cell are nominally equal; $C_1=C_2=C$. Process variations and design imperfections, however, induce mismatches between the capacitor values, which result in errors in the transfer function. Equation (17) shows the transfer function (15) of the pipeline cell in the presence of capacitor mismatch. The mismatch considered in (17) is relative; one capacitor with respect to the other.

$$
\begin{aligned}
V_{OUT} &= V_{IN}\left(1+\frac{C+\Delta C}{C}\right)-V_{DAC}\left(\frac{C+\Delta C}{C}\right) \\
&= 2V_{IN}\left(1+\frac{\Delta C}{2C}\right)-V_{DAC}\left(1+\frac{\Delta C}{C}\right)
\end{aligned}
\tag{17}
$$

The ideal transfer function (dotted) and one affected by a positive capacitor mismatch (solid) are shown in Fig. 24. The 1bit/stage experiences a gain conversion error as the output is beyond the range $\{-V_R,\ V_R\}$. Likewise, the 1.5bit/stage is corrupted even with its output being within $\{-V_R,\ V_R\}$, and the error is maximized at $V_{IN} = 0$ if we consider a potential comparator offset of $\pm V_R/4$. To maintain the performance of the overall ADC, the maximum error must be less than the quantization noise—half an *LSB* of the remaining stages. This is expressed by (18) where the maximum error is obtained by using $V_{IN} = 0$ and $V_{DAC} = V_R$ in (17). Given that the capacitor value is determined by its dimensions and process parameters, a simple model for the capacitor mismatch is derived and presented in (19), where W, L, C_{ox}, ε_{ox} and t_{ox} are the capacitor width and length, oxide capacitance, permittivity and thickness respectively.
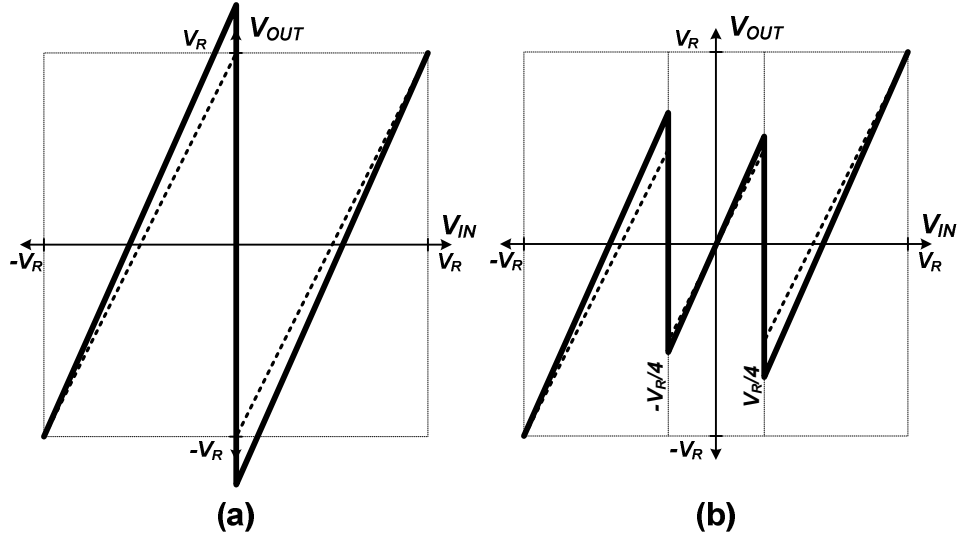
Fig. 24. Effect of positive capacitor mismatch on (a) 1bit/stage and (b) 1.5bits/stage.

While variations in the oxide thickness are process dependent and out of the designer's control, the choice of the capacitor dimensions is crucial to reducing mismatch errors; for metal-insulator-metal (MIM) capacitors in 0.18μm CMOS with a density of ~1fF/μm², a *3σ* mismatch of less than 0.2% — 9bit accuracy — between two 1pF capacitors is achievable. Also, the dependency of the mismatch error on the resolution of the remaining stages as demonstrated by (18) is very significant, because it allows for the implementation of 12-14bit non-calibrated pipeline ADCs if higher bit resolution stages (3.5 or 4.5) are utilized in the first stage [43].

$$V_R \frac{\Delta C}{C} < \frac{2V_R}{2^{Nr+1}} \quad \Rightarrow \quad \frac{\Delta C}{C} < \frac{1}{2^{Nr}} \tag{18}$$

$$C = WLC_{ox} = WL\frac{\varepsilon_{ox}}{t_{ox}} \quad \Rightarrow \quad \frac{\Delta C}{C} \equiv \frac{\sigma C}{C} = \sqrt{\left(\frac{\sigma W}{W}\right)^2 + \left(\frac{\sigma L}{L}\right)^2 + \left(\frac{\sigma t_{ox}}{t_{ox}}\right)^2} \tag{19}$$

Finally, while the MDAC performance is prone to capacitor mismatch errors, the flip-around S/H previously discussed is not, even in the fully-differential realization. This is confirmed by examining its transfer function given by (12), where it is clearly capacitor independent. Hence the capacitor size of the front-end S/H need only be as large as dictated by the noise requirement as will be explained in section *E*. This is another strong advantage for the flip-around S/H over other S/H implementations.

2. *Finite Amplifier Gain*

The transfer functions (7)-(9), (12) and (15) were derived assuming an ideal amplifier. Consider the non-ideal MDAC amplifier in Fig. 25 with finite gain *A*, parasitic capacitance C_P and input offset V_{OS}. By conserving the charge at *x* between clock phases and adding capacitor mismatch, the 1.5bits/stage transfer function given by (15) is modified to (20), which for now ignores the effects of V_{OS}. Here $\beta_{\Phi2}$ is the amplifier feedback factor during Φ_2 and is given by the last term in (21) for a general *M* bit pipeline stage using digital correction and neglecting capacitor mismatch.
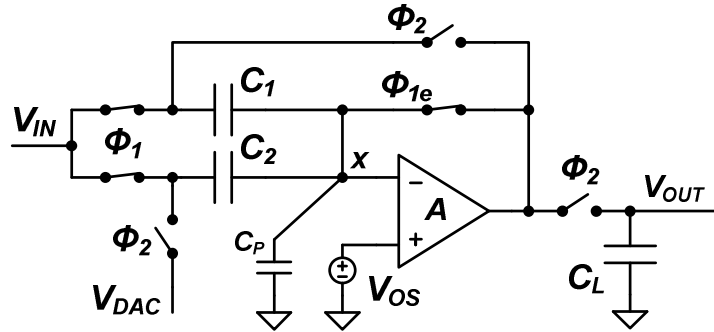
Fig. 25. A 1.5bits/stage loaded MDAC with amplifier non-idealities.

$$V_{OUT} \cong \left(1 - \frac{1}{\beta_{\Phi 2} A}\right)\left[2V_{IN}\left(1 + \frac{\Delta C}{2C}\right) - V_{DAC}\left(1 + \frac{\Delta C}{C}\right)\right] \tag{20}$$

$$\beta_{\Phi 2} = \frac{C_1}{C_1 + C_2 + C_P} \cong \frac{1}{2^M\left(1 + \frac{C_P}{2^M C}\right)} \tag{21}$$

The finite gain also results in a gain error similar to capacitor mismatch. However, unlike capacitor mismatch which affects individual terms in the transfer function and can be positive or negative, the finite gain error scales the whole transfer function and is always negative as seen in Fig. 26. It reaches its maximum when V_{IN} = -V_R, 0, V_R, which needs to be kept under ½ LSB of the remaining stages. Ignoring all errors but the finite gain, the minimum gain required is given by (22).
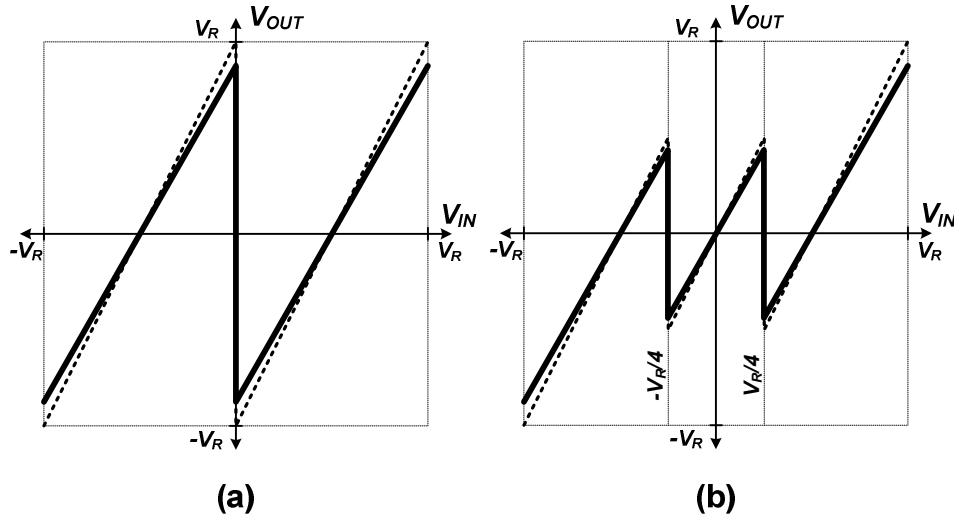
Fig. 26. Effect of finite amplifier gain on (a) 1bit/stage and (b) 1.5bits/stage.

$$\frac{V_R}{\beta_{\Phi 2} A} < \frac{2V_R}{2^{Nr+1}} \quad \Rightarrow \quad A > 2^{Nr+M}\left(1 + \frac{C_P}{2^M C}\right) \tag{22}$$

This shows that the gain of the amplifier in the first 1.5bit/stage MDAC needs to be at least 2^N at maximum output swing ($Nr = N-1$, $M=1$). For a 10bit ADC, the gain of the first MDAC amplifier needs to be at least 60.2dB, ignoring C_P. Since this gain is at maximum output swing, the nominal gain may need to be an order of magnitude (20dB) greater than the limit set by (22); that is 80.2dB. As for the front-end flip-around S/H, recall that it is a special case of the 1.5bits/stage MDAC when $C_2=0$. For the same 10bits ADC and using (22), the minimum S/H amplifier gain needs to be greater than 60.2dB at maximum output swing.

3. Finite Amplifier GBW

The amplifier speed is limited by its gain bandwidth product (GBW) and its configuration feedback factor. Together they define the system time constant τ, which is given by (23) for the 1.5bits/stage MDAC during Φ_2. On the other hand, the functions performed by the MDAC are time limited; since Φ_1 and Φ_2 are symmetric, the maximum time allocated for the MDAC to generate the output is half the clock period, $T_S/2$. As the input to the MDAC is best modeled by a step, and the output is reset during Φ_1, the transfer function of the 1.5bits/stage may be further modified to give (24).

$$\tau = \frac{1}{\beta_{\Phi2}GBW} \tag{23}$$

$$V_{OUT} \cong \left(1 - e^{-\frac{T_S\beta_{\Phi2}GBW}{2}}\right)\left(1 - \frac{1}{\beta_{\Phi2}A}\right)\left[2V_{IN}\left(1 + \frac{\Delta C}{2C}\right) - V_{DAC}\left(1 + \frac{\Delta C}{C}\right)\right] \tag{24}$$

Therefore, the incomplete settling due to the finite amplifier *GBW* applies another scaling factor to the transfer function similar to the finite amplifier gain, and results in the same effect as in Fig. 26. This error is maximum when $V_{IN} = -V_R, 0, V_R$, and needs to be less than ½ *LSB* of the remaining stages. Considering only the effect of the finite amplifier *GBW*, a minimum specification is set by the condition in (25). For the first stage MDAC operating at 160MS/s with 5% clock non-overlap and assuming $C_P = 0.2C$, a minimum *GBW* of 745MHz is required. As for the front-end S/H with similar assumption, a minimum GBW of 450MHz is needed. In a real design, however, the *GBW* values implemented for the front-end S/H and the MDAC amplifier almost double these calculated values; this will be examined in section *F*.

$$V_R\, e^{-\frac{T_S \beta_{\Phi_2} GBW}{2}} < \frac{2V_R}{2^{Nr+1}} \;\;\Rightarrow\;\; GBW > \frac{2^{M+1}}{T_S}\left(1+\frac{C_P}{2^M C}\right)\ln 2^{Nr} \tag{25}$$

4. Amplifier Offset

The effect of the amplifier offset as depicted by Fig. 25, can be incorporated in (24) to generate (26). Ignoring all other errors, the offset causes a vertical shift in the transfer function as demonstrated by Fig. 27. The MDAC implementation of Fig. 25, however, uses direct auto-zeroing offset cancellation making the error negligible; in Φ_1 the offset is sampled on C_1 and C_2 by resetting the amplifier, and is then used in Φ_2 to compensate the offset error at the output. This is confirmed in (26) with the factor $(1+A)$, and offsets as large as 10s of millivolts are effectively reduced well below 1mV.

$$V_{OUT} \cong \left(1 - e^{-\frac{T_S \beta_{\Phi 2} GBW}{2}}\right)\left(1 - \frac{1}{\beta_{\Phi 2} A}\right)\left[2V_{IN}\left(1 + \frac{\Delta C}{2C}\right) - V_{DAC}\left(1 + \frac{\Delta C}{C}\right) + \frac{V_{OS}}{\beta_{\Phi 2}(1 + A)}\right] \quad (26)$$

(a)　　　　　　　　　　(b)
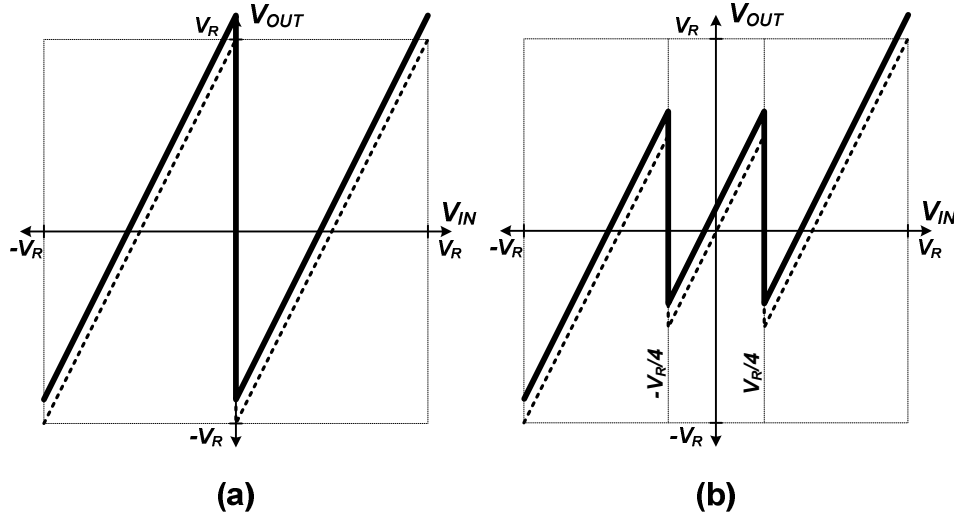
Fig. 27. Effect of amplifier offset on (a) 1bit/stage and (b) 1.5bits/stage.

5. *Amplifier Distortion*

When the output values get closer to $\pm V_R$ the MDAC shows nonlinear effects as depicted in Fig. 28. This behavior is attributed to distortion in the amplifier. The two dominant distortion factors are the amplifier slew rate (SR) and variable gain. The *SR* sets the maximum current the amplifier can provide to charge/discharge its load, which for large output values may be smaller than the current necessary to maintain the exponential settling of (24), thus introducing larger settling errors than for smaller output values. Similarly, the amplifier gain is variable for different output values. It is at its maximum when $V_{OUT} = 0$, and minimum when $V_{OUT} = \pm V_R$. Both the *SR* and variable gain contribute to the bowing effect in the transfer function of Fig. 28, which can be

included in the transfer function as seen in (27), where $\overline{V_{OUT}}$ as expressed by (28) is the

expected output with no *GBW* or *SR* limitations.

$$V_{OUT} \cong \overline{V_{OUT}} \left(1 - \frac{SR}{\overline{V_{OUT}} \beta_{\Phi2} GBW} e^{-\left[1 + \beta_{\Phi2} GBW \left(\frac{T_S}{2} - \frac{\overline{V_{OUT}}}{SR} \right) \right]} \right) \tag{27}$$

$$\overline{V_{OUT}} \cong \left(1 - \frac{1}{\beta_{\Phi2} A} \right) \left[2V_{IN} \left(1 + \frac{\Delta C}{2C} \right) - V_{DAC} \left(1 + \frac{\Delta C}{C} \right) + \frac{V_{OS}}{\beta_{\Phi2}(1+A)} \right] \tag{28}$$
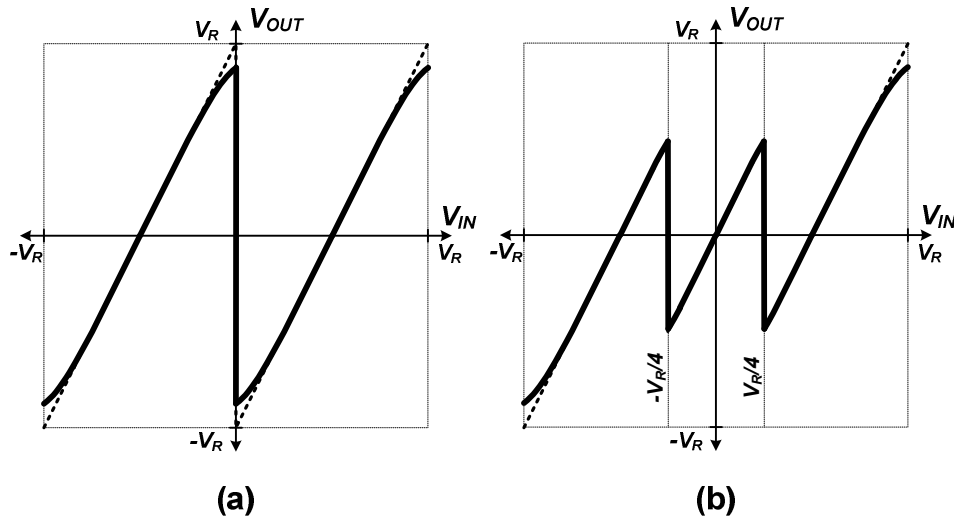
Fig. 28. Effect of amplifier distortion on (a) 1bit/stage and (b) 1.5bits/stage.

The maximum distortion error is at $\overline{V_{OUT}} = \pm V_R$, which needs to be kept smaller

than ½ *LSB* of the remaining stages to maintain the linearity of the ADC; this is

described by (29). Using (29), however, an analytical limit on the *SR* cannot be directly

obtained. In Appendix A the amplifier slewing behavior is analyzed and it is

demonstrated that by allotting a portion δ of the maximum output step V_R to be achieved by slewing, the minimum required SR can be given by (30), whereas the ratio of slewing time, t_{slew}, with respect to $T_S/2$ can be given by (31).

$$\frac{SR}{\beta_{\Phi 2}GBW}e^{-\left[1+\beta_{\Phi 2}GBW\left(\frac{T_S}{2}-\frac{V_R}{SR}\right)\right]} < \frac{2V_R}{2^{Nr+1}} \tag{29}$$

$$SR > \frac{2V_R}{T_S}\left[\delta + (1-\delta)\ln\left(2^{Nr}(1-\delta)\right)\right] \tag{30}$$

$$\frac{t_{slew}}{T_S/2} = \frac{\delta}{\delta + (1-\delta)\ln\left(2^N(1-\delta)\right)} \tag{31}$$

Because of the amplifier slewing, the GBW needs to be increased over what is described by (25) to ensure the amplifier settles to the desired accuracy within $T_S/2$. The relation given by (32) shows the ratio of the new $GBW_{w/slew}$ with respect to the original GBW in terms of the scaling factor δ. The percentage of settling time spent slewing, (31), and the normalized GBW of (32) are presented in Fig. 29.

$$\frac{GBW_{w/slew}}{GBW} = \frac{\delta + (1-\delta)\ln\left(2^{Nr}(1-\delta)\right)}{(1-\delta)\ln\left(2^{Nr}\right)} \tag{32}$$

Considering the first stage MDAC ($Nr = 9$) of the pipeline ADC, a 1Vpp output range means that the maximum step is 500mV. If while slewing the amplifier reaches 350mV ($\delta = 0.7$), then according to (30) a minimum SR of 370V/μs is required, t_{slew}

constitutes about 30% of the settling time, and the $GBW_{w/slew}$ needs to be increased 20% over the original GBW (745MHz $\rightarrow$ 895MHz). Using the same assumptions for the front-end S/H, a SR of at least 410V/µs is needed with a $GBW_{w/slew}$ of 540MHz.
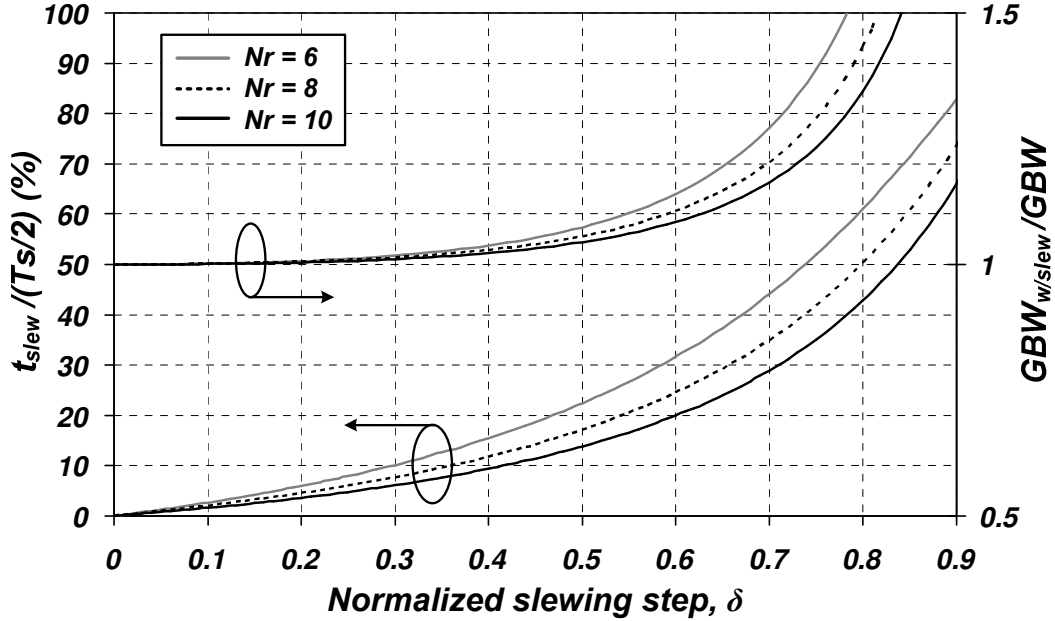
Fig. 29. Effect of amplifier SR on GBW requirement.

6. *Finite Switch Resistance*

Considering the MDAC states of Fig. 19(b) and (d), which are repeated in Fig. 30 for convenience with switch names, we notice the switches are in the charging path of capacitors C_1 and C_2. Given their finite resistance described by (16), they introduce a settling time constant and cause errors within the limited settling time $T_S/2$.
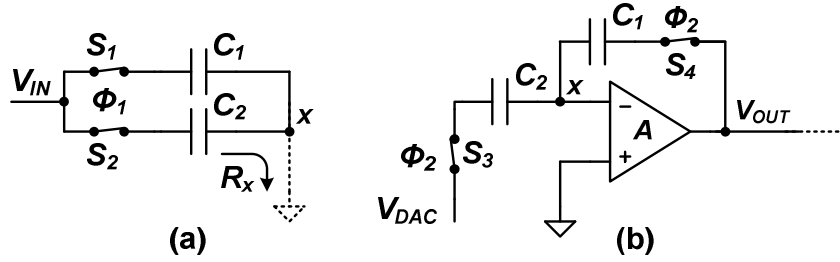
Fig. 30. A 1.5bits/stage MDAC in (a) sampling phase, Φ_1, and (b) multiplying and holding phase, Φ_2.

From Fig. 30(a), it is safe to assume that S_1 and S_2 have the same R_{ON}, as they are generally sized the same and experience the same operating conditions. Therefore, for $C_1 = C_2 = C$, the time constant τ_1 associated with charging either C_1 or C_2 can be expressed by (33), where R_x is the resistance looking into the node x. As for Fig. 30(b), we can define two time constants associated with V_{OUT} charging C_1 and V_{DAC} charging C_2; these are given by τ_2 and τ_3 in (34) and (35) respectively.

$$\tau_1 = C_{1,2}\left(R_{ON1,2} + 2R_x\right) \tag{33}$$

$$\tau_2 = C_1 R_{ON4} \tag{34}$$

$$\tau_3 = C_2 R_{ON3} \tag{35}$$

These time constants affect the charge stored on C_1 and C_2 at the end of either clock phase—$T_S/2$ of settling time—as shown in (36)-(38) assuming no amplifier limitations, and the error is demonstrated by α compared to the original (13)-(15).

$$q_{\Phi 1} = \begin{cases} q_{C1,\Phi 1} = C_1 V_{IN} \left(1 - e^{-\frac{T_S}{2\tau_1}} \right) = \alpha_1 C_1 V_{IN} \\[4mm] q_{C2,\Phi 1} = C_2 V_{IN} \left(1 - e^{-\frac{T_S}{2\tau_1}} \right) = \alpha_1 C_2 V_{IN} \end{cases} \tag{36}$$

$$q_{\Phi 2} = \begin{cases} q_{C1,\Phi 2} = C_1 V_{OUT} \left(1 - e^{-\frac{T_S}{2\tau_2}} \right) = \alpha_2 C_1 V_{OUT} \\[4mm] q_{C2,\Phi 2} = C_2 V_{DAC} \left(1 - e^{-\frac{T_S}{2\tau_3}} \right) = \alpha_3 C_2 V_{DAC} \end{cases} \tag{37}$$

$$\Delta q_{C1} + \Delta q_{C2} = 0 \quad \Rightarrow \quad V_{OUT} = \frac{\alpha_1}{\alpha_2} V_{IN} \left(1 + \frac{C_2}{C_1} \right) - \frac{\alpha_3}{\alpha_2} V_{DAC} \frac{C_2}{C_1} \tag{38}$$

While the terms α_1/α_2 and α_3/α_2 are the source of the error, they offer a couple of solutions. First, using a brute force approach, the resistances associated with the time constants (33)-(35) can be reduced to make α very close to unity; the capacitors C_1 and C_2 may also be reduced to achieve the same effect, but there are matching and noise limitations on their values which may prohibit their reduction. Second, τ_1, τ_2 and τ_3 can be matched, such that α_1, α_2 and α_3 are all equal.

The second approach, while elegant, is quite problematic to implement because R_{ON} can be variable. The R_{ON} expression associated with Fig. 31 is given by (39), which is an expansion of (16), and shows the dependency of the resistance on V_{IN}, the gate voltage V_G, and the bulk voltage V_B.
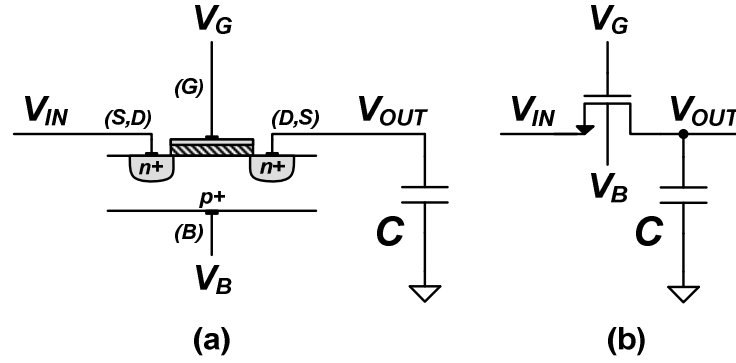
Fig. 31. Four terminal NMOS switch; (a) cross-sectional view and (b) schematic view.

$$R_{ON} = \frac{L}{\mu_N C_{ox} W \left(\underbrace{V_G - V_{IN}}_{V_{GS}} - \underbrace{\left[V_{T0} + \gamma \left(\sqrt{|2\phi_{FB} + V_{IN} - V_B|} - \sqrt{|2\phi_{FB}|} \right) \right]}_{V_T} \right)} \tag{39}$$

For a fixed V_G and V_B, it is clear that as V_{IN} increases, V_{GS} decreases and V_T increases, and effectively R_{ON} is increased. This dependence of R_{ON} on V_{IN} is why it is impractical to match τ_1, τ_2 and τ_3 and make α_1, α_2 and α_3 all equal. Moreover, it is another source for distortion in the MDAC transfer function as depicted in Fig. 32, which unlike the amplifier distortion is asymmetric. This distortion asymmetry is due to V_{DAC}. While V_{IN} and V_{OUT} cover the whole $\{-V_R, V_R\}$ range, V_{DAC} takes fixed values ($-V_R$, 0 or V_R) according to which region V_{IN} falls into. Hence, α_3 is fixed for a particular V_{DAC} value, whereas α_1 and α_2 are continually changing. To a weak approximation α_1 and α_2 track and so α_1/α_2 is fairly constant, but α_3/α_2 experiences a clear and distinct jump as V_{DAC} changes from $-V_R$ to V_R.
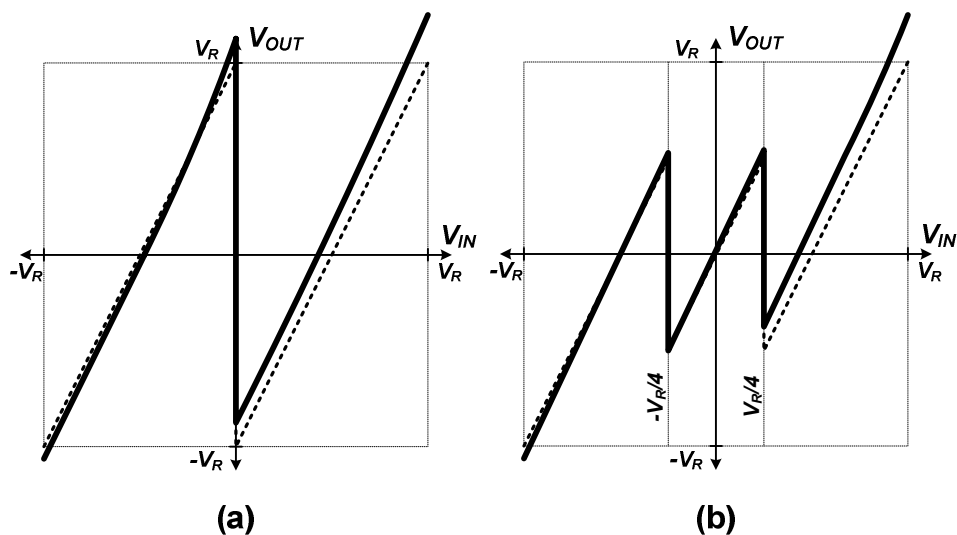
Fig. 32. Effect of variable switch resistance on (a) 1bit/stage and (b) 1.5bits/stage.

The maximum error caused by the switches occurs at $V_{IN} = V_R$, but to express it analytically and extract a set of switch requirements is no easy task. Fortunately, modern CMOS technologies offer small device lengths L and high oxide capacitance C_{ox} which naturally reduce R_{ON} without a lot of design effort. However, this brute force approach may only go up to 12bits of resolution.
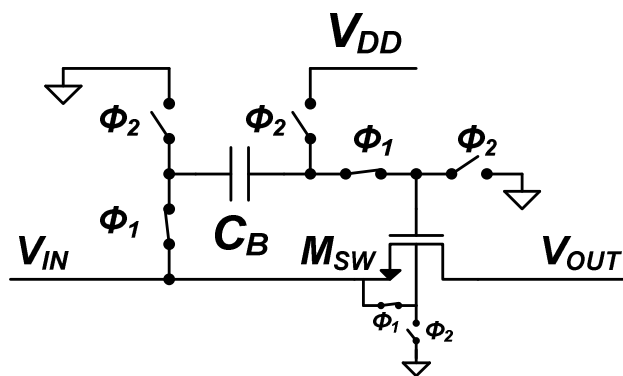
Fig. 33. Modified bootstrapped switch with bulk connections.

On the other hand, there are effective design techniques that ensure high switch linearity and virtually eliminate the R_{ON} dependency on V_{IN}. Consider for example the modified bootstrapped switch with bulk connections in Fig. 33; the bootstrapping effectively keeps V_{GS} constant independent of V_{IN}, while the bulk switching eliminates the V_T dependency on V_{IN} when the switch is on, and grounds the bulk when the switch is off for maximum V_{IN}/V_{OUT} isolation.

D. DNL and INL

The common factor of all the errors examined in section *C* is that they are repeatable for the same V_{IN}, and hence can be used to estimate the *DNL* and consequently the *INL* of the pipeline ADC.

We begin by rewriting the MDAC transfer function of (27) and (28) as shown in (40), where ε_S, ε_A and ε_C represent the error components due to settling (*SR* and *GBW* limitations), amplifier gain and capacitor mismatch respectively. Note that the finite switch resistance effects were not considered, as the amplifier settling limitations generally pose more design challenges than the switches.

$$V_{OUT} \cong (1-\varepsilon_S)(1-\varepsilon_A)\left[2V_{IN}\left(1+\frac{\varepsilon_C}{2}\right)-V_{DAC}(1+\varepsilon_C)+\varepsilon_A V_{OS}\right] \qquad (40)$$

By expanding (40) and neglecting second order errors, the MDAC transfer function simplifies to (41) taking into account that the capacitor mismatch and V_{OS} are

random and therefore can be either positive or negative; their sign reversal in (41) is to maximize the error.

$$V_{OUT} \cong \underbrace{2V_{IN} - V_{DAC}}_{Ideal} - \underbrace{\left[2V_{IN}\left(\varepsilon_S + \varepsilon_A + \frac{\varepsilon_C}{2} \right) - V_{DAC}\left(\varepsilon_S + \varepsilon_A + \varepsilon_C \right) + \varepsilon_A V_{OS} \right]}_{error} \qquad (41)$$

Collectively, the error in (41) is maximized at $V_{IN} = 0$, $V_{DAC} = \pm V_R$, considering a potential comparator offset of $\pm V_R/4$. This is expressed by (42) for $V_R \gg V_{OS}$, and needs to be kept smaller than ½ *LSB* of the remaining stages as described by (43). Unlike section *C* where each MDAC error was considered individually for demonstration purposes, (43) is more practical as it limits all errors under the quantization noise, which guarantees a maximum *DNL* of ½ *LSB* if (43) is fulfilled by all pipeline stages; naturally the front-end S/H also needs to fulfill (43) for a total ADC resolution *N*.

$$V_\varepsilon = V_R\left(\varepsilon_S + \varepsilon_A + \varepsilon_C + \varepsilon_A \frac{V_{OS}}{V_R} \right) \cong V_R\left(\varepsilon_S + \varepsilon_A + \varepsilon_C \right) \qquad (42)$$

$$V_R\left(\varepsilon_S + \varepsilon_A + \varepsilon_C \right) < \frac{2V_R}{2^{Nr+1}} \quad \Rightarrow \quad \varepsilon_S + \varepsilon_A + \varepsilon_C < \frac{1}{2^{Nr}} \qquad (43)$$

As for *INL*, it is the buildup of the S/H and MDAC errors through all stages and can be given by (44) at the output of the front-end S/H for a pipeline ADC of *N* 1.5bits/stage. To limit the *INL* to less than ½ *LSB*, the condition set by (45) needs to be

met, which is very difficult to analyze as the individual stage errors are not correlated. Nonetheless, an absolute worst case scenario can be evaluated assuming all stages have the same error and it builds up with the same sign; this is described in (46).

$$INL = V_R \left[\left(\varepsilon_S + \varepsilon_A + \varepsilon_C \right)_{SH} + \frac{1}{2^{N-1}} \sum_{i=1}^{N-1} 2^{N-(i+1)} \left(\varepsilon_S + \varepsilon_A + \varepsilon_C \right)_i \right] \tag{44}$$

$$V_R \left[\left(\varepsilon_S + \varepsilon_A + \varepsilon_C \right)_{SH} + \frac{1}{2^{N-1}} \sum_{i=1}^{N-1} 2^{N-(i+1)} \left(\varepsilon_S + \varepsilon_A + \varepsilon_C \right)_i \right] < \frac{2V_R}{2^{N+1}} \tag{45}$$

$$\frac{2^N - 1}{2^{N-1}} \left(\varepsilon_S + \varepsilon_A + \varepsilon_C \right) < \frac{1}{2^N} \quad \Rightarrow \quad \left(\varepsilon_S + \varepsilon_A + \varepsilon_C \right) < \frac{1}{2 \left(2^N - 1 \right)} \tag{46}$$

Considering the front-end S/H and comparing (43) with (46), the error tolerance is halved. Moreover, (46) assumes that all stage errors are the same and hence becomes very demanding and inefficient in the design of the last stages where accuracy can be significantly relaxed. Therefore, as far as *INL* is concerned, it is best to analyze it from a statistical approach where the errors are scaled with each stage but are random and uncorrelated as described by (45).

E. Noise

ADC quantization noise was the result of the conversion process, and is used in design to mask over well-defined and predictable circuit non-idealities. However, there is another source of non-ideality that cannot be predicted and can influence the ADC performance. Electronic noise—random fluctuations of voltage and/or current—

contributed by the circuit components is added to the output of each pipeline stage and builds up through the ADC. Using the pipeline ADC diagram of Fig. 10, and representing the output noise power of stage i by $v_{no,i}^2$, the total ADC input referred noise power $v_{n,tot}^2$ can be expressed as in (47), where G_i is the gain of the ith stage.

$$v_{n,tot}^2 = \frac{v_{no,SH}^2}{G_{SH}^2} + \frac{v_{no,1}^2}{(G_{SH}G_1)^2} + \frac{v_{no,2}^2}{(G_{SH}G_1G_2)^2} + \cdots + \frac{v_{no,i-1}^2}{(G_{SH}\cdots G_{i-1})^2} + \frac{v_{no,i}^2}{(G_{SH}\cdots G_i)^2} \qquad (47)$$

It is clear that the early stages are the dominant noise contributors and need to be considered carefully in design; the front-end S/H alone may contribute more than 50% of $v_{n,tot}^2$. To better understand the noise behavior of the pipeline ADC, however, we examine the two fundamental contributors of noise: switches and amplifiers.

1. Switches

The noise generated by the finite on-resistance of switches is characterized as thermal noise. Its model is presented in Fig. 34 where R_{sw} is the switch resistance and $v_{n,sw}^2$ is its noise power spectral density defined by (48) [44]. Here, k_B and T represent Boltzman's constant and the absolute temperature respectively.

$$v_{n,sw}^2 = 4k_B T R_{sw} \cdot \Delta f \qquad (48)$$
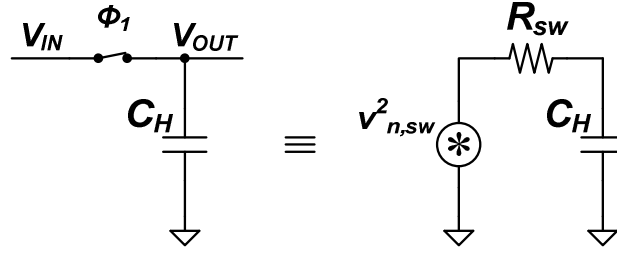
Fig. 34. Switch resistance noise model.

The noise sampled on C_H is transferred to the next stage and has to be analyzed to evaluate its effect on the overall ADC performance. It is necessary to consider the integrated noise power over all frequencies to account for the aliased noise due to sampling. This is evaluated in (49), and the result shows that the total noise power is solely dependent on the capacitance value and can only be reduced by increasing C_H.

$$v_{n,C_H}^2 = 4k_B T R_{sw} \int_0^\infty \frac{df}{1 + \left(2\pi f\, R_{sw} C_H\right)^2} = \frac{k_B T}{C_H} \tag{49}$$

For simple passive sampling as that modeled in Fig. 34, (49) can be used in conjunction with the quantization noise of the ADC to determine the minimum capacitance required such that the effect of switch resistance noise on the linearity and resolution of the overall ADC is diminished; this is expressed by (50).

$$\frac{k_B T}{C_H} < \frac{\left(2V_R\right)^2}{12\left(2^N\right)^2} \quad \Rightarrow \quad C_H > 3\frac{2^{2N} k_B T}{V_R^2} \tag{50}$$

2. *Amplifiers*

Amplifiers also contribute to the noise seen at the output of the ADC. Consider Fig. 35, which depicts all the noise sources present for both the sampling and holding phases in an *M* bit/stage MDAC based on the example of Fig. 15. To see how the amplifier affects the noise performance of the pipeline cell, we need to analyze the total output noise. Once evaluated, the output noise can be referred back to the input to formulate a figure of merit for amplifier noise and determine the minimum capacitance needed to keep the overall thermal noise of the MDAC below the ADC's quantization noise requirements. This analysis is the subject of Appendix B, where it is demonstrated that the input referred noise of an MDAC can be expressed by (51), where $m = 2^M-1$ and α_n is given by (52)—a similar noise analysis is presented in [45], but assumes a passive sampling approach and thus ignores the amplifier noise in the sampling phase.
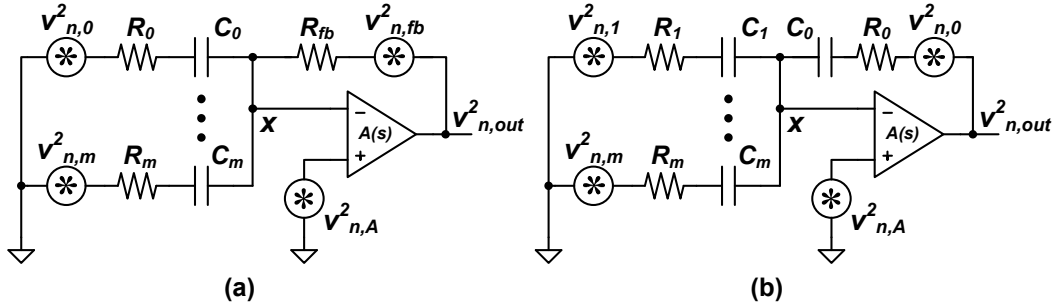
Fig. 35. Noise sources present in an M bit/stage MDAC for (a) sampling phase and (b) holding phase.

$$v_{n,in}^2\Big|_{MDAC} = \frac{k_B T}{(m+1)C_L}\left[\gamma\left(1+\eta\right)+\frac{2gmR_{sw}}{(m+1)}\right]+2\frac{k_B T}{(m+1)C_u}\left(1+\alpha_n\right) \qquad (51)$$

$$\alpha_n = \frac{1}{1+\omega_u R_{sw} C_u} + \frac{m}{2\left(1+\dfrac{\omega_u^2 R_{sw}^2 C_u^2}{1+\omega_u R_{sw} C_u}\right)} + \frac{\gamma(1+\eta)}{gmR_{sw}\left(1+\dfrac{1}{\omega_u R_{sw} C_u}\right)} \qquad (52)$$

The input referred MDAC noise shows that the contributions of the switches and amplifier to the MDAC noise are limited by the unit capacitance, C_u, used in the MDAC and effective loading capacitance, C_L, seen by the amplifier. Also, the use of multi-bit/stage pipeline cells has an added filtering effect on the total noise; this added benefit of lower noise, however, is a direct trade-off with the speed of the pipeline ADC due to the reduced feedback factor of the MDAC amplifier. Another trade-off occurs between the amplifier bandwidth and switch time constant, which is exemplified in α_n; setting $R_{sw}C_u$ significantly smaller than $1/\omega_u$ results in the switch resistance noise dominating, and vice versa. Nonetheless, a good compromise is achieved when $R_{sw}C_u \approx 1/\omega_u$, where power consumption can be optimized. Further power optimization can be realized if C_L—the loading of the following stage—is recognized as a function of C_u and the MDAC gain, which defines the capacitor scaling along the pipeline stages [46]. Finally, (51) can also be used to evaluate the input referred noise of the S/H by using m = 0.

F. Conclusions

The primary focus of this chapter was the analysis of all the underlying phenomena that govern the performance of the pipeline ADC from an analog standpoint. Through numerous derivations, many analog circuit design limitations were linked to characteristic errors in the ADC, and boundaries of their acceptable bounds where

established to facilitate the design process of a non-calibrated pipeline ADC. The amplifier in particular was identified as a major contributor to ADC errors, and hence Chapter IV is devoted to its study. On the other hand, while amplifier errors can be alleviated by design, capacitors and switches remain as the ultimate limitation in non-calibrated pipeline ADC. This is mostly evident from the DNL/INL analysis where capacitor mismatch dominates the performance, and also from the study of MDAC noise where a lower bound is primarily set by $k_B T/C_u$.

CHAPTER IV

AMPLIFIERS

It was demonstrated in Chapter III that amplifiers in pipeline ADCs have a direct and major role in the operation of the individual pipeline stages by performing active sampling and residue amplification. Consequently, the amplifier limitations have a direct impact on the overall ADC performance, which for high speed and very high (>12 bits) resolutions may require the ADC to be digitally calibrated.

This chapter focuses on the study of the performance metrics that govern the design of amplifiers and influence the accuracy of pipeline ADCs. Each performance metric will be discussed using an actively-loaded differential pair amplifier as an example, and keys to high speed design will be highlighted. Also, some optimization methods on the transistor level will be discussed that are applicable to low voltage and low power applications. Then, the fundamental amplifier topologies commonly used in SC applications will be compared for their suitability in a high speed, low voltage and low power pipeline ADCs, along with some techniques of amplifier performance enhancement and the challenges associated with their implementations.

A. The Differential Pair Amplifier

An actively-loaded differential amplifier is shown in Fig. 36 for single-ended and fully-differential configurations. In the following sections, many amplifier aspects will be discussed based on Fig. 36. In order to facilitate the discussion, frequent reference

will be made to the square law I-V model of MOS devices [47], which for an NMOS

device in saturation is expressed by (53) where μ_N, C_{ox}, W, L, V_{GS}, V_{T_N} and V_{GSTN} are the

electron mobility, gate oxide per unit area, width, length, gate-source, threshold, and

overdrive voltages respectively. While this simple model does not take into account

many of the secondary effects seen and modeled for state-of-the-art CMOS technologies

[48], it serves as a reasonable first-order approximation to MOS device behavior.

Nevertheless, secondary order effects will be presented as the need arise and where

applicable.
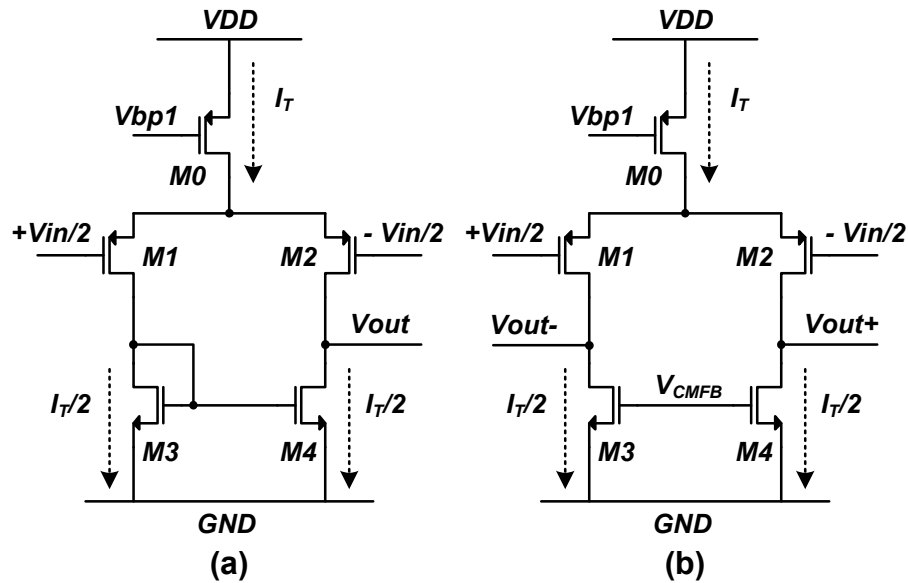
Fig. 36. The differential pair amplifier; (a) single-ended and (b) fully-differential.

$$I_{D0} = \frac{1}{2}\mu_N C_{ox} \frac{W}{L}\left(V_{GS} - V_{T_N}\right)^2 = \frac{1}{2}\mu_N C_{ox} \frac{W}{L} V_{GSTN}^2, \tag{53}$$

1. *Bandwidth*

The bandwidth of an amplifier is the first indicator to its speed performance. It is also a measure of the frequency bandwidth for which the amplifier's gain is larger than unity, and is commonly referred to as the gain bandwidth product (*GBW*). There are several factors on which the amplifier's *GBW* depends; the CMOS technology used, device size, quiescent operating point, driven load and amplifier architecture are some examples.

CMOS technology has been aggressively scaling down in device size over the past four decades to accommodate a lager number of gates per unit area. The scaling down of device size also improved the bandwidth. The most commonly used figure of merit to quantify the maximum speed for a given CMOS technology is the transit frequency, f_T [49], at which the small signal drain current to gate current ratio of a MOS device is unity, and can be expressed by (54). We can deduce from (54) that the speed of CMOS devices and hence a CMOS amplifier can be enhanced by increasing the overdrive voltage, V_{GST}, or reducing the device channel length, L.

$$f_T \cong \frac{\mu}{2\pi}\frac{V_{GST}}{L^2} \tag{54}$$

From a designer's perspective, however, the amplifier's transconductance and load determine its bandwidth, and hence its speed. The transconductance, *gm*, is the amplifier's ability to convert the input voltage signal into a current that drives the output load, and is defined for an NMOS operating in saturation by (55). Note that all three

forms of *gm* are equivalent, but provide a different view into the design variables.

$$gm = \frac{\partial I_D}{\partial V_{GS}}\bigg|_{const.V_{DS}} = \mu_N C_{ox} \frac{W}{L} V_{GSTN} = \frac{2I_D}{V_{GSTN}} = \sqrt{2\mu_N C_{ox} \frac{W}{L} I_D} \qquad (55)$$

The importance of the amplifier transconductance is best illustrated by the small signal macro-model of Fig. 36(a) given in Fig. 37. Here the output voltage, *Vout*, is the sum of currents (i_1-i_2) driving the given output load (R_L||C_L). Since the differential pair, *M1* and *M2*, of the amplifier in Fig. 36(a) are identical, the differential gain of the amplifier in Fig. 36(a) can be expressed by (56). We can now find the bandwidth, or *GBW*, of the amplifier by setting (56) to unity and solving for *s* (*jω*), which results in (57). Clearly, the *GBW* is highly dependent on the device size, quiescent operating point and the load driven as exemplified through *gm* of equation (55) and C_L.

Fig. 37. Small signal macro-model of Fig. 36(a) assuming a load R_L||C_L.

$$A(s) = \frac{Vout}{Vin} = \frac{gm_{1,2}R_L}{1 + sC_L R_L} \tag{56}$$

$$GBW \cong \frac{gm_{1,2}}{C_L} \tag{57}$$

2. Gain

Amplifiers are seldom used in an open-loop configuration; in analog design, one does not rely on the absolute value of the amplifier's gain. Consider the low frequency gain value of (56), $A(0) = gm_{1,2}R_L$, and suppose the amplifier had no external loading such that R_L is its intrinsic output impedance. While the transconductance, $gm_{1,2}$, can be fairly predicted by setting the associated parameters in (55), the amplifier's intrinsic output impedance cannot due to channel length modulation [47].

A MOS device enters the saturation region when V_{DS} exceeds V_{GST}. Then the channel is said to be pinched-off from the drain. With further increase in V_{DS}, the MOS device is driven deeper into saturation and the channel length is reduced to $L_{eff} < L$ as seen in Fig. 38, giving rise to channel length modulation.
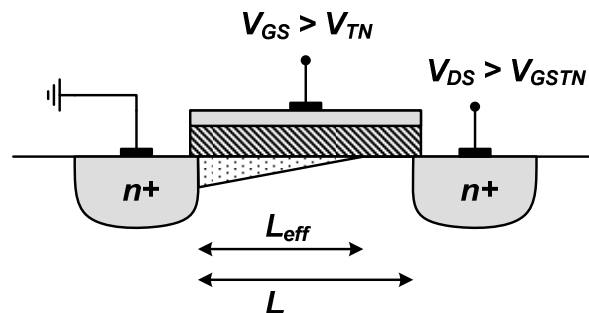
Fig. 38. Channel length modulation phenomenon in MOS devices.

The channel length modulation can be incorporated in the square law I-V model of (53) to yield (58), where I_{D0} is the ideal drain current expressed by (53). Using (58) we can express the intrinsic output impedance of a MOS device as in (59). We can again derive the transconductance, *gm*, from (58) and together with (59), express the intrinsic gain A_i = *gm* r_{ds} of a MOS device as in (60).

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L_{eff}}V_{GST}^2 \equiv \frac{1}{2}\mu C_{ox}\frac{W}{L}V_{GST}^2\left(1+\lambda V_{DS}\right) = I_{D0}\left(1+\lambda V_{DS}\right) \qquad (58)$$

$$r_{ds} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1}\Bigg|_{const.V_{GS}} = \frac{2L}{\mu_N C_{ox}W V_{GSTN}^2\lambda} = \frac{1}{\lambda I_{D0}} \qquad (59)$$

$$A_i = \frac{2\left(1+\lambda V_{DS}\right)}{\lambda V_{GSTN}} \qquad (60)$$

Equations (59) and (60) demonstrate the uncertainty in the intrinsic output impedance and gain of a MOS device, and hence of an amplifier. However, because amplifiers are used in a closed loop configuration, i.e. using feedback, this gain uncertainty is of little concern. Fig. 39 shows a simple example of an amplifier in closed loop for which the gain *Vout/Vin* is given by (61). For a sufficiently large intrinsic amplifier gain *A*, *Vout/Vin* is virtually independent of *A* and is set by the capacitor ratio C_1/C_2. Nonetheless, (60) highlights the importance of the quiescent operating point of the MOS device, and can give an approximate measure of the maximum intrinsic MOS gain achievable for a particular CMOS technology.
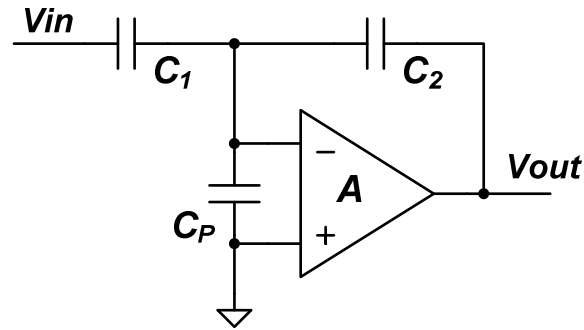
Fig. 39. An example of a closed loop amplifier circuit.

$$\frac{Vout}{Vin} = -\frac{C_1}{C_2}\left(1+\frac{C_1+C_2+C_P}{A\,C_2}\right)^{-1} \cong -\frac{C_1}{C_2}\left(1-\frac{C_1+C_2+C_P}{A\,C_2}\right) \qquad (61)$$

What is critical for low voltage applications and can be deduced from (60) is how the amplifier gain is related to the output swing. For large signals, the quiescent operating point of a MOS device can no longer be considered fixed as with small signals, but is incrementally changing; as the output swings closer to either supply rail, the quiescent V_{DS} of the respective device decreases and hence the gain is reduced. This has to be closely considered in low voltage applications, where the signal swing needs to be maximized while maintaining the highest gain possible.

3. Phase Margin

Although the macro-model of Fig. 36(a) provides a good approximation of the small signal amplifier behavior, it overlooks the parasitics of the current mirror now modeled in Fig. 40. The mirrored current, i^{*}_{1}, is no longer identical to the source i_{1},

which modifies the overall gain expression as given by (62). Unlike (56), the gain expression in (62) is a two-pole system, and its significance is best explained by examining the phase of *Vout*. Since the amplifier transfer function is variable with frequency, it results in a magnitude and phase change at the output. Given the complex nature of the gain expression (*s=jω*), the phase is given by the cumulative effect of the poles and zeros, and the general phase expression is given by (63) for a transfer function with *n* poles (*ω_p*) and *m* zeros (*ω_z*).
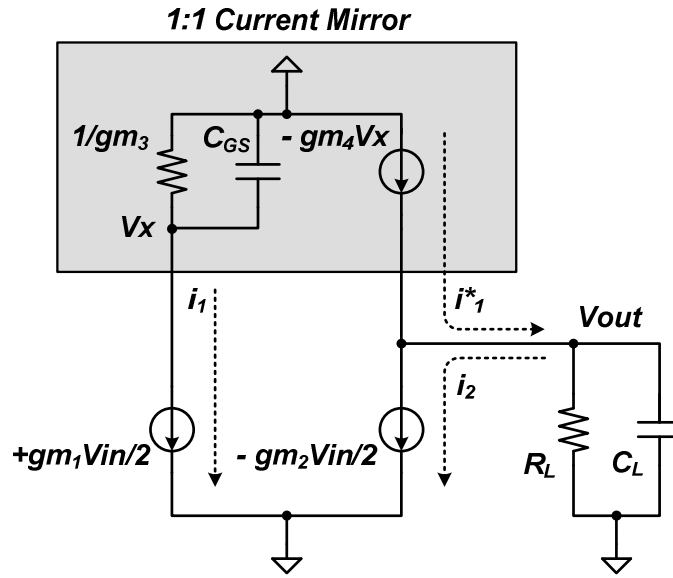
Fig. 40. Improved small signal macro-model of Fig. 36(a).

$$A(s) = \frac{Vout}{Vin} \cong \left(i_1^* - i_2\right)\left(\frac{R_L}{1 + sC_LR_L}\right) = \frac{gm_{1,2}R_L\left(1 + sC_{GS}/2gm_{3,4}\right)}{\left(1 + sC_LR_L\right)\left(1 + sC_{GS}/gm_{3,4}\right)} \qquad (62)$$

$$\theta(\omega) = \sum_{l=1}^{n} \tan^{-1}\left(\frac{\omega}{\omega_{pl}}\right) - \sum_{k=1}^{m} \tan^{-1}\left(\frac{\omega}{\omega_{zk}}\right) \qquad (63)$$

Using (63) we can express the phase of (56) and (62) as in (64) and (65) respectively, where $C_{GS} = C_{gs3}+C_{gs4}$. From (64) and (65), we see the phase is negative and decreasing with frequency in the presence of poles. This is potentially problematic with closed-loop amplifier configurations such as in Fig. 39, and detailed analyses are presented in [50]-[51]. However, an intuitive way to analyze this is as follows. The magnitude of the amplifier transfer function is generally a decreasing function of s, similar to (56) and (62). Suppose for some transfer function with multiple poles that the phase shift between *Vout* and *Vin* exceeds 180° at some frequency ω_o while the amplifier's gain is greater than unity ($\omega_o < GBW$), then the output of the amplifier in Fig. 39 will oscillate indefinitely and become unstable.

$$\theta(\omega)\big|_{(iii5)} = -\tan^{-1}\left(\frac{\omega}{1/C_L R_L}\right) \tag{64}$$

$$\theta(\omega)\big|_{(iii11)} = -\tan^{-1}\left(\frac{\omega}{1/C_L R_L}\right) - \tan^{-1}\left(\frac{\omega}{gm_{3,4}/C_{GS}}\right) + \tan^{-1}\left(\frac{\omega}{2\,gm_{3,4}/C_{GS}}\right) \tag{65}$$

The phase margin is a measure of how far is the amplifier from being unstable and is measured at $s=GBW$. The phase margin is also a good indicator to the amplifier ability to reach steady state should a fast time-varying signal, such as a step function, be applied to its input. This is illustrated in Fig. 41 by considering the 0.1% step response settling time of the amplifier in Fig. 36(a) when used as in Fig. 39 for $C_1 = C_2$, $C_P = 0$, $A(0) = 60$dB, $GBW = 100$MHz and different phase margin values.
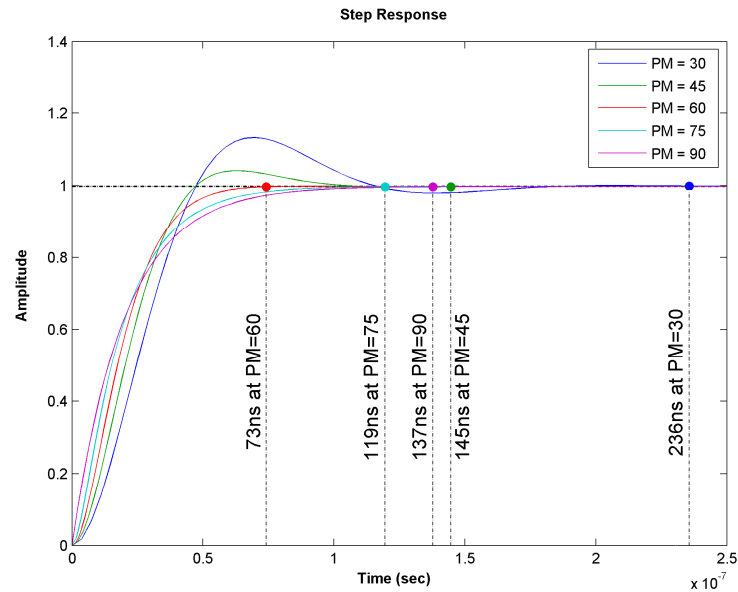
Fig. 41. Closed loop step response of the amplifier in Fig. 36(a) for different phase margin values.

The results of Fig. 41 lead to the conclusion that a phase margin around 60° is ideal for high speed performance. Indeed, this is the case for the chosen settling error (0.1%) and if there are no pole-zero doublets within the amplifier's *GBW*. If on the other hand the latter is the case, the frequency of the doublet and separation between the pole and zero can dominate the settling behavior and significantly slow down the amplifier's response [52]-[53].

The amplifier architecture can also play a role in determining the speed. The transfer function of (62) demonstrated that the presence of the current mirror *M3:M4* in Fig. 36(a) led to the addition of a pole-zero pair that may hinder the speed of the amplifier if not considered in design. On the other hand, the fully differential amplifier in Fig. 36(b) does not suffer the same limitation. Fig. 42 shows the macro-model of the

fully differential amplifier in Fig. 36(b) and (66) describes the amplifier's transfer function. Note that (66) is identical to (56). Unlike the single ended amplifier, the two signal paths in the fully differential amplifier are identical and their summation at the output does not generate a pole-zero pair that can slow down the speed. This is one of numerous advantages for using fully differential amplifiers over their single ended counterparts.
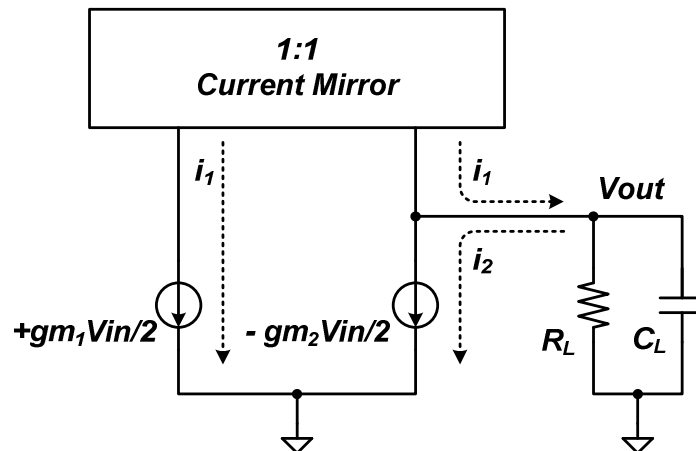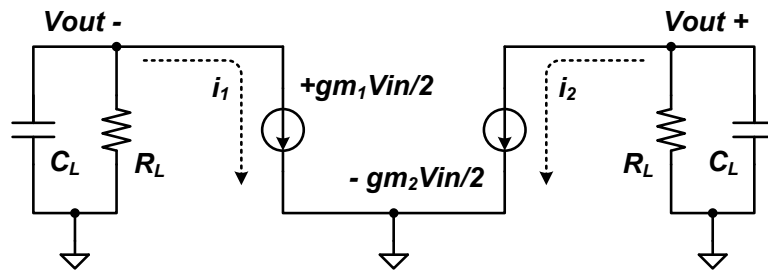

Fig. 42. Small signal macro-model of Fig. 36(b) assuming a load $R_L||C_L$.

$$A(s) = \frac{(Vout+) - (Vout-)}{Vin} = \frac{gm_{1,2}R_L}{1 + sC_L R_L} . \tag{66}$$

4. Slew Rate

In SC application, the settling time and accuracy of a circuit is crucial to good linearity. Consider the single ended amplifier of Fig. 36(a) configured as in Fig. 39, and for simplicity refer to its gain transfer function as in (56). The time-domain step response can then be described by (67), where the feedback factor, β, is $C_2/(C_1+C_2+C_P)$, and closed loop amplifier gain, α, is given by (68).

$$Vout = -\alpha \cdot Vin \left(1 - e^{-\beta \cdot GBW \cdot t}\right) \qquad (67)$$

$$\alpha = \frac{C_1}{C_2}\left(1 + \frac{1}{\beta\, A(0)}\right)^{-1} \qquad (68)$$

Given sufficient time, the final value is that described by (61). However, the maximum time allocated for the amplifier to settle is limited by half the sampling clock period, T_S. This emphasizes the maximization of the amplifier GBW through circuit configuration selection, and β through input parasitic consideration, especially when high accuracy settling is desired. However, this is only half the picture.

Equation (67) holds true if and only if the amplifier is capable of handling any level of input. In reality the amplifier's ability to drive current into its output impedance is generally limited by the amount of current available to bias it. In Fig. 36, $M0$ is referred to as the tail of the amplifier, which provides the tail current I_T. For large step inputs, one of the input drivers enters into the subthreshold region (shuts off), while the other is strongly driven to conduct all of I_T. The current I_T is then driven directly, or indirectly through the current mirror, into the output load. In this operation mode, the amplifier is said to be slewing, and the linear settling behavior described by (67) is no longer valid. The rate at which the output voltage changes with respect to time in the slewing mode defines the slew rate, SR, of the amplifier as described by (69).

$$SR = \frac{\partial Vout}{\partial t} = \frac{I_T}{C_L} \qquad (69)$$

Now it can be shown that *Vout* may be expressed by (70) when the slew rate is taken into account for zero initial conditions [54]—derivations are also available in appendix A. Furthermore, given an absolute settling error ε_S, the overall settling time t_S is expressed by (71) and the slewing time t_{slew} and linear settling time t_{lin} are given by (72) and (73) respectively.

$$Vout = \begin{cases} SR \cdot t \, , & t < t_{slew} \\ -\alpha \cdot Vin \left(1 - \dfrac{SR}{\alpha \cdot Vin \cdot \beta \cdot GBW} \cdot e^{-\beta \cdot GBW (t - t_{slew})} \right), & t > t_{slew} \\ -\alpha \cdot Vin \left(1 - e^{-\beta \cdot GBW \cdot t} \right), & t_{slew} \leq 0 \end{cases} \tag{70}$$

$$t_S = t_{slew} + t_{lin} = \frac{\alpha \cdot Vin}{SR} + \frac{1}{\beta \cdot GBW} \left[\ln \left(\frac{SR}{\varepsilon_S \alpha \cdot Vin \cdot \beta \cdot GBW} \right) - 1 \right] \tag{71}$$

$$t_{slew} = \frac{\alpha \cdot Vin}{SR} - \frac{1}{\beta \cdot GBW} \tag{72}$$

$$t_{lin} = \frac{1}{\beta \cdot GBW} \ln \left(\frac{SR}{\varepsilon_S \alpha \cdot Vin \cdot \beta \cdot GBW} \right) \tag{73}$$

The fastest settling performance is inarguably that for all-linear settling, which can be proven by taking the derivative of (71) with respect to *SR*, and substituting the outcome in (72). More importantly, however, using (72) we can find the maximum input step for which no slewing will occur. The result is given by (74).

$$Vin \Big|_{no\,slew} \leq \frac{SR}{\alpha \cdot \beta \cdot GBW} = \frac{V_{GST}}{\alpha \cdot \beta} \tag{74}$$

The expression in (74) shows that slewing is inevitable for high speed Nyquist rate SC applications such as pipeline ADCs. In such applications the input step size between consecutive cycles can be in the order of the system's full-scale voltage, V_{FS}, which is much larger than (74) predicts. In part, the amplifier's input pair V_{GST} is limited to the range of 100-200mV to maximize signal headroom and input common mode range. On the other hand, α and β are set by the amplifier's configuration and their product can loosely be considered unity for high speed designs. These conditions yield a maximum non-slewing step of roughly 0.2 V_{FS} in present-day CMOS technologies. Therefore the only viable approach to reducing the settling time is to enhance both *SR* and *GBW* of the amplifier, and hence it is critical to account for the amplifier slewing performance in the power budget.

5. *Distortion*

By examining the square law I-V relationship in (53) we can conclude that the MOS transistor is not a linear device. However, through the use of feedback, CMOS amplifiers are used successfully to implement highly linear functions. Intuitively, because of the high amplifier gain, the positive and negative input terminals of the amplifiers experience a virtual short; that is the amplifier's input terminals seem fixed about the ideal quiescent operating point for any input signal.

The paradox of feedback, however, is the use of a non-linear device to linearize itself. The transfer function described by (61) is ideally given by the ratio C_1/C_2, but the finite amplifier gain results in an error term. When an input is applied, the output swing

modulates the V_{DS} of the output devices thereby changing the amplifier gain and subsequently the error term in the transfer function. To reflect this behavior, (61) is modified to (75) where the gain is now a function of the input. Also, Fig. 43 depicts this graphically for the absolute values of (61) and (75). The result is an input dependent gain error for large output swings and consequently observable distortion at the output, which is undesirable in many applications such as pipeline ADCs.

$$\frac{Vout}{Vin} = -\frac{C_1}{C_2}\left(1 + \frac{C_1 + C_2 + C_P}{A(Vin)\,C_2}\right)^{-1} \cong -\frac{C_1}{C_2}\left(1 - \frac{C_1 + C_2 + C_P}{A(Vin)\,C_2}\right) \tag{75}$$
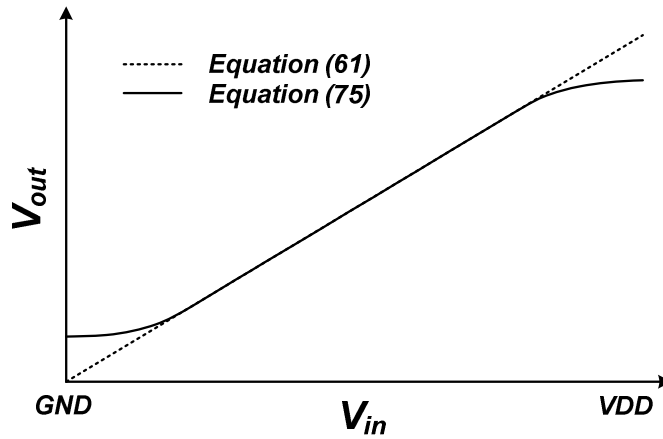
Fig. 43. Amplifier gain degradation for large output swings.

Another source of distortion is the *SR* limited settling. Consider the flip-around S/H amplifier discussed in Chapter III. For the case of all-linear settling, the final output is expressed by (76) where all parameters with the $_{SH}$ subscript have the same previous

definitions, but pertaining to the flip-around S/H. Note that the error term is independent of *Vin* and therefore is a fixed for all input values. If the settling becomes *SR* limited, however, then the output is expressed by (77).

$$Vout = -\alpha_{SH} Vin \left(1 - e^{-\beta_{SH} GBW \frac{T_S}{2}} \right) \tag{76}$$

$$Vout = \begin{cases} -\alpha_{SH} Vin \left(1 - e^{-\beta_{SH} GBW \frac{T_S}{2}} \right), & Vin \le \dfrac{V_{GST_{SH}}}{\alpha_{SH} \beta_{SH}} \\ -\alpha_{SH} Vin \left(1 - \dfrac{SR_{SH}}{\alpha_{SH} Vin \cdot \beta_{SH} GBW} \cdot e^{-\left[1 + \beta_{SH} GBW \left(\frac{T_S}{2} - \frac{\alpha_{SH} Vin}{SR_{SH}} \right) \right]} \right), & Vin > \dfrac{V_{GST_{SH}}}{\alpha_{SH} \beta_{SH}} \end{cases} \tag{77}$$

From (76) we conclude that for the all-linear settling, the value of $T_S/2$ is irrelevant as far as distortion is concerned, because it will result in a consistent gain error for all values of *Vin*. The same is true for the *SR* limited settling, but for a small range of input values. As *Vin* crosses the limit described in (74), the settling error becomes input dependent and results in distortion. This is depicted in Fig. 44, where the thick solid trace is the input, and thin solid trace and dotted trace are the all-linear and *SR* limited settling of the S/H output respectively. The upper traces are the real-time waveforms, while the bottom traces are the end-points plot of the S/H output in the hold phase. Note that the input trace is shifted forward in time by half a clock cycle to correspond to the end points of the S/H traces. In the shaded regions of Fig. 44, the output is compressed for the *SR* limited case, whereas otherwise it follows the all-linear settling curve.

Therefore, when considering SC linear applications, the linearity is often expressed as a maximum settling error specification; say ε_{max}, which for the S/H example above is expressed by (78).
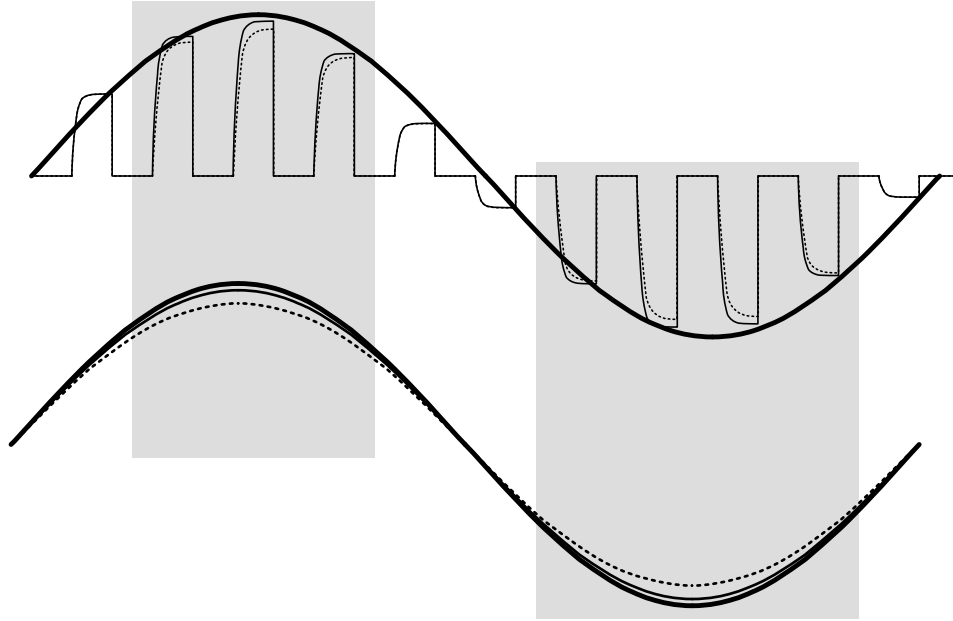
Fig. 44. Slew rate induced distortion for fixed settling time, $T_S/2$; thick solid: *Vin*, thin solid: *Vout* (linear settling) and dashed: *Vout* (slew rate limited settling).

$$\varepsilon_{\max} \geq \frac{SR_{SH}}{\alpha_{SH} Vin_{\max} \cdot \beta_{SH} GBW_{SH}} \cdot e^{-\left[1 + \beta_{SH} GBW_{SH}\left(\frac{T_S}{2} - \frac{\alpha_{SH} Vin_{\max}}{SR_{SH}}\right)\right]}, \qquad Vin_{\max} > \frac{V_{GST_{SH}}}{\alpha_{SH} \beta_{SH}} \qquad (78)$$

6. *Noise*

Noise in circuits can be generally defined as spontaneous fluctuations in current, voltage or temperature that set the lower limit on measurements taken on a system under test [55]. In many applications, such as data converters, continuous time filters and audio

amplifiers, these fluctuations are the limiting factors in a design's dynamic performance.

There are two dominant noise sources that affect the performance of CMOS circuits, namely the thermal and flicker noise. Thermal noise is attributed to the random charge carrier motion in a conductor due to the ambient temperature. As for the flicker noise, the major contributor is the interaction of the charge carriers with the Si-SiO$_2$ interface, where the carriers are trapped and then released back into the channel in a random process [55]. These noise sources can be modeled in MOS devices as a current source in parallel with the device representing the power spectral density, which is given by (79) where the first and second terms represent the thermal and flicker noise contributions respectively. Here, k_B, T, γ, K_F and f represent Boltzman's constant, the absolute temperature, noise factor, process dependent flicker noise coefficient and frequency respectively. Equation (79) is a simplified form of other complex models [56]-[57], but is very useful for design.

$$\overline{i_o^2} = \left(4k_BT\gamma\, gm + \frac{K_F I_D}{C_{ox}L^2 f} \right) \cdot \varDelta f \tag{79}$$

To aid the derivation of the amplifier noise, we refer to the amplifier noise model in Fig. 45 from which we can express the maximum noise seen at the output by (80). To minimize clutter, the thermal and flicker noise components will be examined separately by substituting (79) into (80).
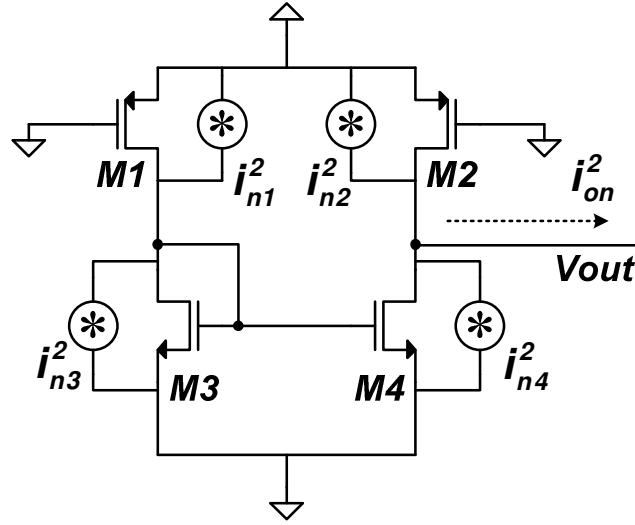
Fig. 45. Noise sources modeled for the amplifier in Fig. 36(a).

$$\overline{i_{on}^2} = i_{n1}^2 + i_{n2}^2 + i_{n3}^2 + i_{n4}^2 \tag{80}$$

Beginning with the thermal noise, the total noise seen at the output is expressed by (81), which is the simplified form if we account for $gm_1=gm_2$ and $gm_3=gm_4$. Referring the amplifier's noise to the input makes it easy to compare with the input signal, and to do so we divide the output noise by the square of the amplifier's transconductance gm_1. The result is given by (82).

$$\overline{i_{on}^2} = 8k_{\mathrm{B}}T\gamma\left(gm_1 + gm_3\right)\cdot \varDelta f \tag{81}$$

$$\overline{v_{iT}^2} = \frac{\overline{i_{on}^2}}{Gm^2} = \frac{8k_{\mathrm{B}}T\gamma}{gm_1}\left(1 + \frac{gm_3}{gm_1}\right)\cdot \varDelta f$$

$$= \frac{8k_{\mathrm{B}}T\gamma}{\sqrt{2\mu_P C_{ox} I_{D1}(W_1/L_1)}}\left(1 + \sqrt{\frac{\mu_N}{\mu_P}\frac{(W_3/L_3)}{(W_1/L_1)}}\right)\cdot \varDelta f \tag{82}$$

Following the same approach with respect to the flicker noise component, the output noise and input referred noise are given by (83) and (84) respectively. Note that the results of (81)-(84) are the same for the fully differential amplifier of Fig. 36(b) since the sum of currents at the output is the same.

$$\overline{i_{on}^2} = \frac{I_D}{C_{ox}f}\left(2\frac{K_{FP}}{L_1^2} + 2\frac{K_{FN}}{L_3^2}\right)\cdot \Delta f \tag{83}$$

$$\overline{v_{i\,1/f}^2} = \frac{\overline{i_{on}^2}}{Gm^2} = \frac{2I_D}{gm_1^2 C_{ox}f}\left(\frac{K_{FP}}{L_1^2} + \frac{K_{FN}}{L_3^2}\right)\cdot \Delta f$$

$$= \frac{K_{FP}}{\mu_P W_1 L_1 C_{ox}^2 f}\left[1 + \frac{K_{FN}}{K_{FP}}\left(\frac{L_1}{L_3}\right)^2\right]\cdot \Delta f \tag{84}$$

There are a few conclusions that can be drawn from (82) and (84) regarding the amplifier's noise. First, and foremost, the *gm* of the input pair has a huge impact on the overall amplifier noise performance. Note that referring the output noise to the input was done through the input pair *gm*, and hence it is crucial to maximize the input *gm* beyond any other transistor; in a truly low noise amplifier, the maximum *gm* is that of the input pair. Second, the sizing plays a direct role in the noise performance. From (82) we see the ratio of the dimensions of *M1* and *M3* and also in (84) in terms of the channel length and input pair area. Moreover, a closer look at (84) shows that the flicker noise expression is a quadratic function of L_1, and hence there exists a value for L_1 at which the flicker noise is minimized and is given by (85).

$$L_1 = L_3 \sqrt{\frac{K_{FP}}{K_{FN}}} \tag{85}$$

Finally, the device type is also a factor in the amplifier's noise. Both (82) and (84) contain parameters that are device type dependent, namely the mobility $\mu_{N,P}$ and the flicker noise coefficient $K_{FN,P}$. This brings up the question of which device type is most suitable for the input pair for the best noise performance. To answer part of the question, let us first consider the device mobility. The electron mobility μ_N is 3-4 times faster than the hole mobility μ_P in semiconductors [58]-[59], and hence it is best to use NMOS devices as the input pair to minimize the thermal noise.

On the other hand, in CMOS technologies the transistors gates are commonly n+ polysilicon, which result in a buried-channel-like behavior for PMOS devices that minimizes the interaction of the carriers with the Si-SiO$_2$ interface and consequently the flicker noise coefficient [60]-[62]. This results in K_{FP} to be an order of magnitude smaller than K_{FN}, and hence PMOS devices are ideal as input pair devices to minimize the flicker noise. For p+ polysilicon gates, however, K_{FP} and K_{FN} are of the same order.

Therefore, the answer as to which device type is more suitable for low noise amplifier design seems different for each type of noise. Nonetheless, in light of the advancement of CMOS technologies, the contribution of each noise type is also different. From (79), the thermal noise has a flat behavior with frequency, while the flicker noise is inversely proportional to frequency. Equating the two noise components and solving for f, yields the noise corner frequency, f_{nc}, given by (86).

$$f_{nc} = \frac{K_F I_D}{4k_B T \gamma \, gm C_{ox} L^2} = \frac{K_F V_{GST}}{8k_B T \gamma C_{ox} L^2} \qquad (86)$$

Using (86), the noise corner frequency of present-day CMOS technologies is in the 100s of MHz, which makes the flicker noise the major contributor to amplifier noise in many applications. Hence, for overall noise performance, it is generally better to use PMOS devices as the input pair of amplifiers.

In summary, to optimize the noise performance of amplifiers for high speed, low voltage and low power applications, one can follow these guidelines:

- Use PMOS devices for the input pair, unless p+ polysilicon is used for the gate material, or extremely high speed applications (GHz range) are targeted.

- Maximize I_D of the input pair within the given power budget.

- Maximize the area and the aspect ratio of the input pair devices (*WL* and *W/L*).

- Once all device aspect ratios are defined, use (85) to set the value of the input pair channel length, but maintain the aspect ratio.

7. *Process Variations*

Amplifiers are ideally symmetric by design, but once fabricated a zero-input signal commonly results in a finite output. This behavior is attributed to minor asymmetries that are either systematic or random but together constitute what is known by offset. Systematic offset is imposed on the amplifier by the design and choice of

quiescent operating points of devices and can be reduced by good design practices. Random offset, on the other hand, is the result of manufacturing process variations.

Manufacturing process variations are a result of finite lithography resolution, non-uniform oxide thickness growth and doping profiles across the wafer's plane. A mismatch model [63] based on the study of equal area rectangular devices, states that the one-dimensional variance of a parameter P can be expressed by (87) where A_P is the area proportionality constant for parameter P, W and L are the device dimensions, S_P is the variation of P with spacing, and D_x is the distance between two devices along x. In practice, critical devices such as the input pair or current mirrors are interdigitated or cross-coupled, and hence D_x approaches zero, and the second term of (87) can be neglected. Using (53), the drain-current variance due to process variation can be expressed as in (88) assuming $\sigma^2(V_T)$ and $\sigma^2(\beta_I)$ are uncorrelated [63]-[66]. Here β_I represents $\mu C_{ox} W/L$. Equation (88) is very useful, because from a circuit analysis stand point, the drain-current variance can be treated as a small signal that can be referred to the gate of the MOS device through its transconductance, gm. The result is given by (89).

$$\sigma^2(P) = \frac{A_P^2}{WL} + S_P^2 D_x, \tag{87}$$

$$\sigma^2(I_D) = 4I_D^2 \frac{\sigma^2(V_T)}{V_{GST}^2} + I_D^2 \frac{\sigma^2(\beta_I)}{\beta_I^2} \tag{88}$$

$$\sigma^2(V_{GS}) = \sigma^2(V_T) + \frac{1}{(gm/I_D)^2} \frac{\sigma^2(\beta_I)}{\beta_I^2} \tag{89}$$

It was demonstrated in [67] that for nominal biasing conditions ($V_{GST} < 650\text{mV}$), $\sigma^2(V_T)$ is the dominant mismatch factor. Moreover, in analog design the term gm/I_D is generally maximized, which further supports the dominance of $\sigma^2(V_T)$ and reduces the effect of the second term of (89). Therefore, we can reduce (89) to (90) to describe the gate-referred (input-referred) current variance in MOS devices. Here A_{V_T} is the area proportionality constant for the threshold voltage, V_T.

$$\sigma^2(V_{GS}) \cong \sigma^2(V_T) = \frac{A_{V_T}^2}{WL} \tag{90}$$

Using (90), the input offset variance can be expressed as the sum of all device drain current variances at the amplifier's output, and then referred to the input using the amplifier's gm. This analysis is quite similar to the noise analysis and the noise model of Fig. 45 can be used here, but with the substitution of $\sigma^2(I_D) = gm^2\sigma^2(V_{GS})$ for $\overline{i_n^2}$. Thus, the total output current variance and input offset variance of the amplifier in Fig. 36(a) are given by (91) and (92) respectively, which again is the simplified form if we account for $gm_1=gm_2$ and $gm_3=gm_4$.

$$\sigma^2(I_D)\Big|_{output} = 2\left[gm_1^2\left(\frac{A_{V_{TP}}^2}{W_1L_1}\right) + gm_3^2\left(\frac{A_{V_{TN}}^2}{W_3L_3}\right)\right] \tag{91}$$

$$\sigma^2(V_{OS}) = 2\left[\left(\frac{A_{V_{TP}}^2}{W_1L_1}\right) + \frac{gm_3^2}{gm_1^2}\left(\frac{A_{V_{TN}}^2}{W_3L_3}\right)\right] = 2\frac{A_{V_{TP}}^2}{W_1L_1}\left[1 + \frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{L_1}{L_3}\right)^2\right] \tag{92}$$

Note again that the results in (91) and (92) are the same for the fully differential amplifier of Fig. 36(b). Moreover, a minimum offset can be achieved for a particular design if the length of the input pair device is sized as in (93).

$$L_1 = L_3 \sqrt{\frac{\mu_P}{\mu_N} \cdot \frac{A_{V_{TP}}}{A_{V_{TN}}}} \qquad (93)$$

Before we discuss the design guideline for low input offset, let us examine the parameter A_{V_T}. From a physical approach, it was noticed experimentally that A_{V_T} scales down with the gate oxide thickness t_{ox} [63], regardless of the device type, and a theoretical expression of this relationship is given by (94) [67], where D_{Total} is the total dopant implant dose in the bulk material of the device, q is the electron charge and ε_{ox} is the silicon oxide permittivity.

$$A_{V_T} = \sqrt{\frac{D_{Total}}{2} \cdot \frac{q}{\varepsilon_{ox}}} \cdot t_{ox} \qquad (94)$$

Therefore, as CMOS technologies scale down in terms of t_{ox}, the matching characteristics are enhanced through the reduction seen in A_{V_T}. Yet, this is not fully reflected in device matching since the device dimensions are also scaled down and the matching performance can actually become worse. What is interesting, however, is the dependence on the doping dose in the bulk. With advanced CMOS technologies, low V_T

devices are becoming more robust and their use in low voltage applications more diverse. Their lower V_T is achieved by a counter type implant in the bulk region immediately under the gate where the channel is formed. This effectively reduces the total dose and improves their matching performance over regular devices.

In conclusion, the following design guidelines can be adopted for low input offset amplifiers:

- Maximize the width of the input pair devices.

- Maximize the length of devices apart from the input pair.

- Set the input pair device length as given by (89).

- Use low V_T devices if they can support the design requirements.

- The best type of device for the input pair is dependent on the A_{V_T} parameter for each device type.

B. Amplifiers for Pipeline ADCs

The preceding discussion demonstrated the many aspects of amplifier design, and the choice of the amplifier architecture to use in a pipeline cell must consider all to guarantee proper performance within the boundaries imposed by power and area. Fig. 46 shows the three fundamental topologies that are commonly seen in pipeline ADCs, and they are the Telescopic, Current Mirror and Folded Cascode OTAs. The following is a brief comparison of each and a presentation of their key performance metrics; detailed expressions of their performance metrics are given in Appendix C.
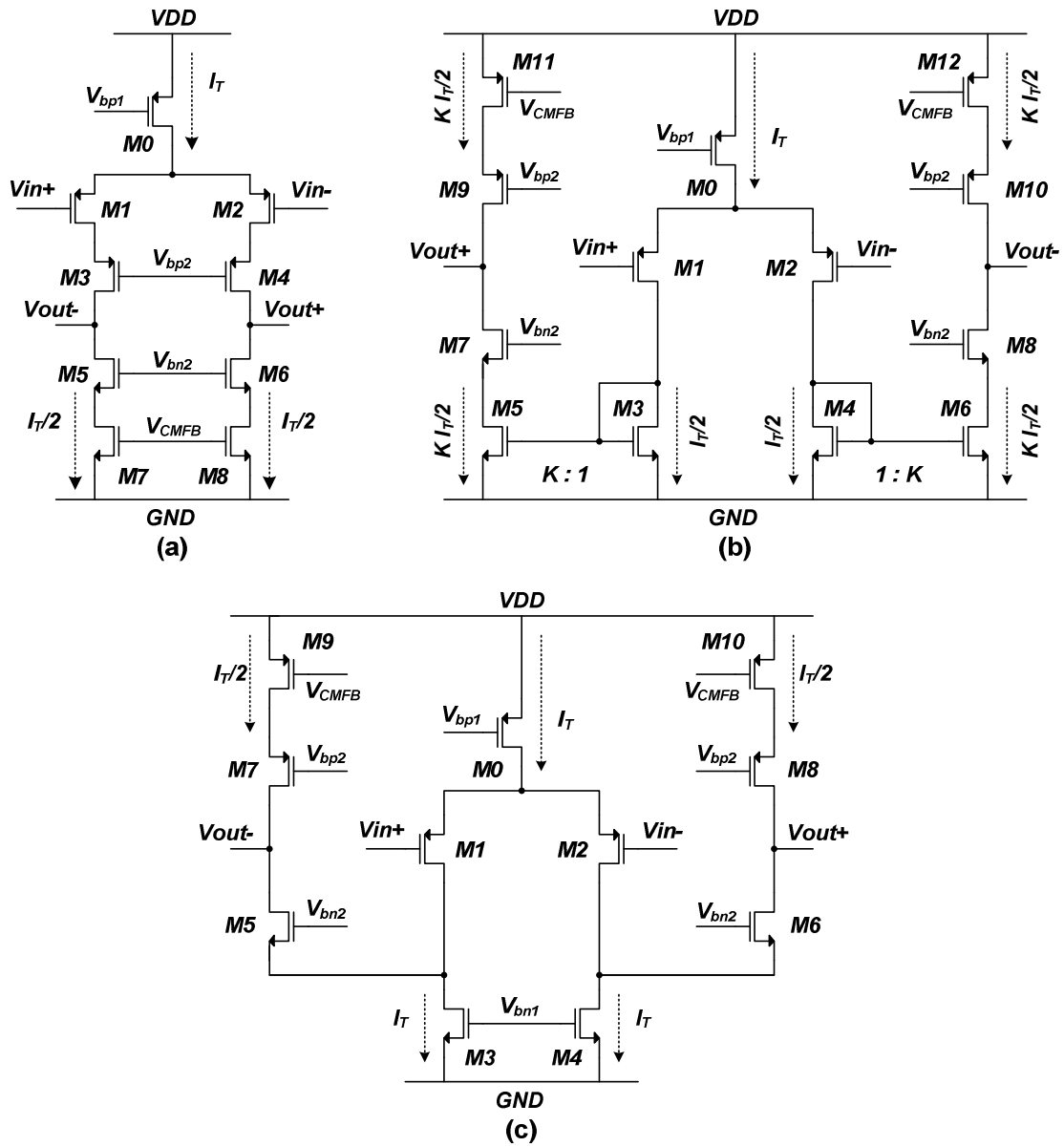
Fig. 46. Fundamental OTA architectures; (a) telescopic, (b) current mirror
and (c) folded cascode.

If we assume the transconductance gm_1 of M_1 to be the same for all amplifiers in Fig. 46, then the summary of parameters in Table 3 can easily be used to summarize the strengths and weakness of each amplifier topology as follows.

TABLE 3
FUNDAMENTAL PARAMETER SUMMARY OF OTAS SEEN IN FIG. 46

Parameter	Telescopic	Current Mirror	Folded Cascode
Minimum Supply	$V_{GS} + 3V_{DS,sat}$	$V_{GS} + 2V_{DS,sat}$	$V_{GS} + 2V_{DS,sat}$
Maximum Signal Swing	$V_{DD} - 5V_{DS,sat}$	$V_{DD} - 4V_{DS,sat}$	$V_{DD} - 4V_{DS,sat}$
Total Current (I_{TOT})	I_T	$I_T(1+K)$	$2I_T$
Transconductance (Gm)	gm_1	Kgm_1	gm_1
LHP Poles	2	3	2
Slew rate (for a C_L load)	$\dfrac{I_T}{C_L}$	$\dfrac{KI_T}{C_L}$	$\dfrac{I_T}{C_L}$
Input Referred Thermal Noise $*(16kT/3gm_1)$	$\left(1 + \dfrac{gm_7}{gm_1}\right)$	$\left(1 + \dfrac{gm_3}{gm_1} + \dfrac{gm_5 + gm_{11}}{K^2 gm_1}\right)$	$\left(1 + \dfrac{gm_3 + gm_9}{gm_1}\right)$
Efficiency (Gm/I_{TOT})	$\dfrac{gm_1}{I_T}$	$\dfrac{Kgm_1}{(K+1)I_T}$	$\dfrac{gm_1}{2I_T}$

The Telescopic OTA is undoubtedly the most power efficient amplifier. It also has the best frequency response in term of the number of poles and zeros and their locations, and the least noise contribution. On the other hand, it requires a higher supply than both the Current Mirror and Folded Cascode OTAs, and leaves the least headroom for signal swing at the output, which makes it the least suitable for low voltage applications despite its other strengths. Overall, the Telescopic OTA is best suited for designs that require very high speed and low noise performance where the signal swing is not very critical.

The Current Mirror OTA is superior to the Telescopic in term of low voltage

operation. It can also deliver a higher slew rate performance and a wider GBW, but at the expense of higher power dissipation. However, its noise contribution is the highest of all amplifiers, and its efficiency is lesser than that of the Telescopic OTA. Furthermore, while the efficiency can be enhanced by increasing K, the frequency response is degraded as K plays a significant role is the placement of one of its poles. Overall, the Current Mirror OTA is best suited for low voltage and large signal swing applications, where the noise, speed and power performances are not very critical.

Finally, the Folded Cascode OTA is the comfortable medium of both the Telescopic and Current Mirror OTA. It shares a good low voltage performance with the Current Mirror OTA, but without the additional noise. It also shares a very good frequency performance with the Telescopic OTA, but a degraded efficiency. Overall, the Folded Cascode OTA is suitable for a larger range of applications where speed, noise and signal headroom are valued. It is not surprising then to see the increased use of the Folded Cascode amplifier in the literature in state-of-the-art designs whether as a single stage or the first stage in a multi-stage amplifier [26], [68]-[73].

C. Amplifier Enhancement

Some of the amplifier requirements needed to implement pipeline cells cannot be satisfied by a simple OTA as those presented in section B. For example, a 200MS/s 10bit resolution MDAC requires an amplifier with a minimum gain of 66dB to keep the static settling errors within ½ *LSB*. Yet, in modern CMOS technologies the gain attainable by any of the OTAs in Fig. 46 may not exceed 50dB while operating at that speed. To

overcome this limitation, amplifier enhancement techniques are widely used with the most common being multi-stage cascading and regulated cascode gain boosting.

1. Multi-Stage Amplifiers

Gain enhancement using multi-stage amplifiers is a well-established technique that relies on the cascading of two or more gain stages as depicted by the Miller compensated example in Fig. 47. The low frequency gain of the multi-stage amplifier is the product of all cascaded gain stages; $A = A_1A_2$ for the example in Fig. 47. However, each additional gain stage introduces another low frequency pole, which limits the bandwidth of the amplifier and more importantly increases the risk of instability. Therefore, multi-stage amplifiers utilize different compensation techniques to overcome such limitations [74], and the most popular is the Miller compensation represented by the dashed lines in Fig. 47.
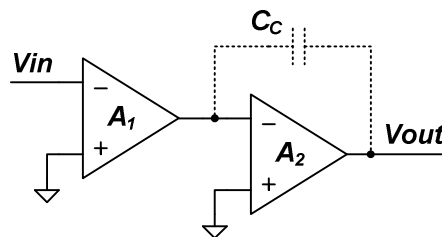
Fig. 47. Miller compensated multi-stage amplifier.

In addition to the increased gain of the overall amplifier, multi-stage amplifiers can utilize the full supply range for signal swing by adopting a rail-to-rail output stage.

This is a significant advantage in low voltage applications as it maximizes the noise tolerance. However, multi-stage amplifiers are often bulky and power hungry due to the use of compensation capacitors, and while some techniques attempt to alleviate these drawbacks, multi-stage amplifiers are still no match to the speed and power efficiency of a single stage amplifier.

2. *Gain Boosting*

Another amplifier enhancement technique is the regulated cascode gain boosting. Instead of cascading several amplifiers to increase the gain, the regulated cascode gain boosting approach relies on active feedback to limit the V_{DS} variations at the source of the cascode device. This is illustrated in Fig. 48 for a Telescopic OTA, but can readily be applied to Current Mirror and Folded Cascode OTAs as well.

The feedback loop of the auxiliary amplifier and the cascode transistor enhances the output impedance, and thus increases the amplifier gain [75]. An advantage of this approach over multi-stage amplifiers is the transparency of the gain enhancement to the signal path; it does not add low frequency poles that slow down the amplifier or compromise its stability. However, as is the case with any feedback loop, some conditions must be satisfied as expressed by (95). Namely, the *GBW* of the auxiliary amplifier needs to be greater than the closed loop bandwidth of the main amplifier, and less than its non-dominant pole; the first condition guarantees no pole-zero doublets within the closed loop bandwidth that may introduce slow settling components, while the second ensures the stability of the auxiliary amplifier and cascode transistor loop.

$$\omega_{-3dB}\big|_{Closed\ Loop} < \omega_{u}\big|_{Boosting} < \omega_{P2}\big|_{main\ opamp} \tag{95}$$
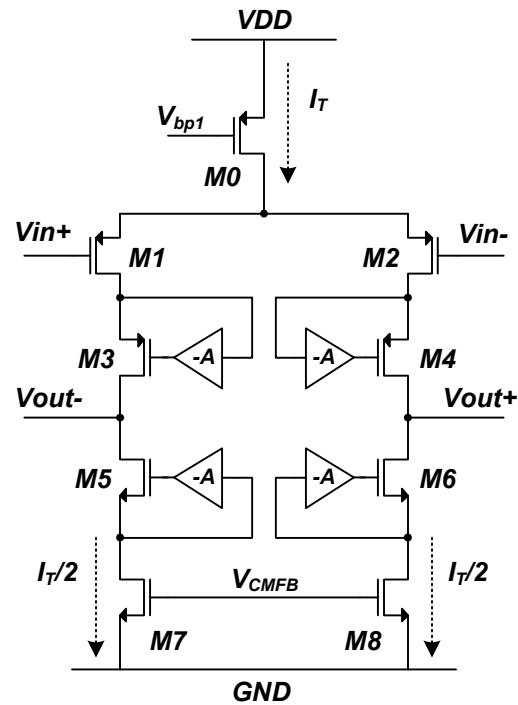
Fig. 48. Regulated cascode gain boosting applied to a telescopic OTA.

Overall, as the auxiliary amplifiers only drive their respective cascode device, they are quite small, which makes the regulated cascode gain boosting method more efficient than utilizing a multi-stage amplifier from a power and area stand point. However, the main drawback to the regulated cascode approach is the limited head for the output swing.

D. Conclusions

Numerous aspects of amplifier design have a direct impact on the performance of pipeline cells. Through a systematic approach, key performance metrics of amplifiers were derived and discussed with a focus on building robust amplifiers for the application of high speed, high resolution and high efficiency S/H and MDAC pipeline cells. Particular emphasis was given to distortion, noise and offset as they are detrimental to the operation of such cells. Moreover, a survey of the fundamental OTA architectures is undertaken to isolate the best overall design for high speed, low voltage and low power applications. Finally, the widely used gain enhancement techniques are described, and for optimum efficiency the regulated cascode gain boosting approach is recommended. However, a combination of gain boosted first stage followed by a rail-to-rail output stage serves as the best compromise.

CHAPTER V

RECYCLING FOLDED CASCODE[*]

Chapter IV highlighted the strengths of the Folded Cascode (FC) amplifier, which recently has become one of the most commonly used amplifier architectures in low voltage pipeline ADCs whether in the single or multi-stage form. Therefore, it is not surprising to see efforts in the literature aimed to enhance its performance, and other amplifiers in general.

Earlier work to enhance the performance of the FC used multi-path schemes [76] and [77]. Other multi-path schemes such as [78] and [79] were applied to the Current-Mirror OTA to specifically enhance the output impedance and slew rate, and to emulate a class AB output stage operation. The concept behind these schemes is to split the input signal among several paths whose sum at the amplifier output is in phase—similar to a current mirror active load in single-ended amplifiers. This may result, however, in numerous low frequency pole-zero pairs in the amplifier's open loop transfer function that may render it useless for high speed applications such as in Nyquist ADCs. While [76]-[79] may fall in that category of slower amplifiers, they nevertheless form the basis of the proposed modification to the FC amplifier presented in Section *A*.

A. Proposed Folded Cascode Amplifier

The conventional FC is shown again in Fig. 49 for convenience. Note how transistors *M3* and *M4* are the two transistors in the signal path that conduct the most current, and in many designs have the largest transconductance. However, their role is strictly limited to providing a folding node for the small signal current generated by the input differential pair *M1* and *M2*.

Fig. 49. The conventional folded cascode amplifier.

To address this inefficiency, a modified FC amplifier is presented in Fig. 50. The proposed modifications are intended to use *M3* and *M4* as driving transistors [80], and proceed as follows. First, the input differential pair, *M1* and *M2* (Fig. 49), are split in half to produce transistors *M1a, M1b, M2a,* and *M2b* (Fig. 50). Next, *M3* and *M4* (Fig.

49) are split to form the current mirrors *M3a:M3b* and *M4a:M4b* with a ratio of *K:1* (Fig. 50), where *K* is chosen to be 3 *strictly* to maintain the same current consumption as the FC in Fig. 49; naturally *K* has to be *greater than* 1 to maintain current in the output devices *M5-M10*. The diode connected transistors, *M3b* and *M4b*, are cross-coupled with the input transistors, *M2b* and *M1b*, to ensure the small signal currents added at the sources of *M5* and *M6* are in phase. Finally, cascode devices may be added inside the diode connection of *M3b* and *M4b* to reduce the current dependency on V_{DS} and improve matching in the current mirrors. The modified Folded Cascode will be referred to by the Recycling Folded Cascode (RFC), since we are reusing, or recycling, existing devices and currents to perform an additional task.
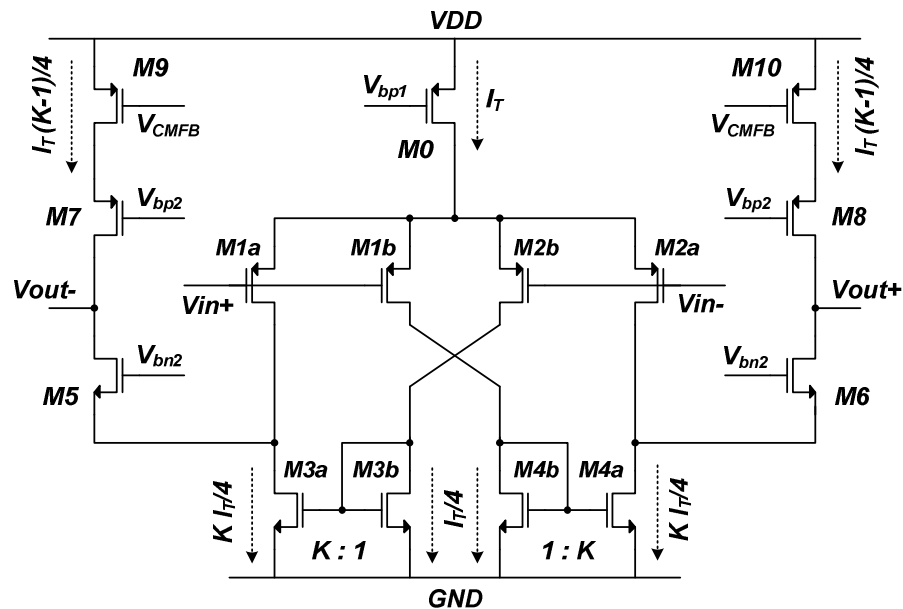
Fig. 50. The recycling folded cascode (RFC) amplifier.

B. Recycling Folded Cascode Characteristics

The modifications presented in Section *A* provide the RFC with enhanced features over the FC. In this section, various amplifier merits will be derived for the RFC to present these enhancements quantitatively, similar to Chapter IV. This will also help examine the costs associated with the proposed modifications from a design perspective.

1. Small Signal Transconductance

We first examine the amplifier's transconductance, *Gm*. By finding the short-circuit current at the output of the RFC with respect to its input, its small signal transconductance can be expressed as in (96). Since *M1* in the original FC is twice the size of *M1a* and conducts twice the amount of current for the same bias conditions, then $gm_{1,FC} = 2gm_{1a,RFC}$. Using this result and by substituting for the value of $K = 3$ in (96), the low frequency transconductance of the RFC is demonstrated to be twice that of the FC for the same power consumption. In other words, for the same capacitive load, the *GBW* of the RFC is twice as wide as that of the FC.

$$Gm_{RFC} = gm_{1a}(1 + K) \tag{96}$$

2. Low Frequency Gain

It was demonstrated that $Gm_{RFC} = 2Gm_{FC}$, which results in a 6dB gain enhancement for the same output impedance. However, Ro_{RFC} is also enhanced over Ro_{FC}. The expression for Ro_{RFC} is given by (97) and that of Ro_{FC} by (98). Because of the

modifications in RFC, *M2a* and *M4a* conduct less current than their counterparts *M2* and *M4* of the FC, which enhances their intrinsic output impedance, r_{ds}. It is this enhancement in r_{ds2a} and r_{ds4a} that adds an additional 2–4dB to the gain of the RFC. Therefore, an overall low frequency gain enhancement of 8–10dB can be seen in the RFC compared to the FC; settling errors associated with the finite amplifier gain are thus reduced by a factor of ~3 for a RFC over a FC.

$$Ro_{RFC} \cong gm_6 \, r_{ds6} \left(r_{ds2a} \| r_{ds4a}\right) \| gm_8 \, r_{ds8} \, r_{ds10} \tag{97}$$

$$Ro_{FC} \cong gm_6 \, r_{ds6} \left(r_{ds2} \| r_{ds4}\right) \| gm_8 \, r_{ds8} \, r_{ds10} \tag{98}$$

3. Phase Margin

The phase margin was identified in Chapter IV as a good indicator to the transient response of an amplifier. The expected phase margin expression of the RFC is given by (99), and the corresponding pole-zero locations by (100). The pole-zero locations in the s-domain are depicted in Fig. 51; it is assumed that all non-dominant poles-zeros are beyond ω_u for stability and good phase margin.

$$PM_{RFC} = 180° - \tan^{-1}\left(\frac{\omega_u}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right) - \tan^{-1}\left(\frac{\omega_u}{\omega_{p3}}\right) + \tan^{-1}\left(\frac{\omega_u}{\omega_{z1}}\right) \tag{99}$$

$$\omega_u = \frac{Gm_{RFC}}{C_L}, \ \omega_{p1} = \frac{-1}{Ro_{RFC}C_L}, \ \omega_{p2} \cong \frac{-gm_{3b}}{(1+K)Cgs_{3b}}, \ \omega_{p3} \cong \frac{-gm_5}{Cgs_5}, \ \omega_{z1} = (1+K)\omega_{p2} \tag{100}$$
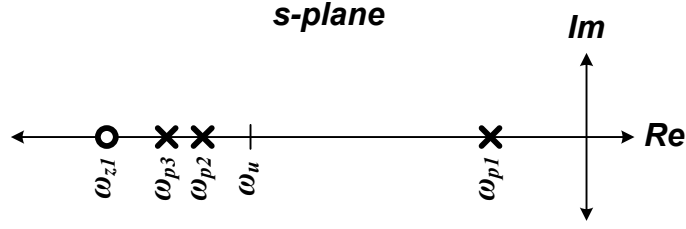
Fig. 51. Pole-zero locations of the RFC in the s-domain.

In comparison with the FC, the RFC has the same poles, but also an additional pole-zero pair, ω_{p2} and ω_{z1}, associated with the current mirrors *M3a*:*M3b* (and *M4a*:*M4b*). However, this pole-zero pair is associated with NMOS devices, which puts it at a high frequency. Moreover, the choice of *K* plays a significant role in determining the phase margin, so the selection of *K* will be limited by the amplifier application; for high speed applications *K* is ideally chosen such that $\omega_{p2} > 3\omega_u$, which can be used to place an upper boundary on *K* as described by (101).

$$\omega_{p2} > 3\omega_u \quad \Rightarrow \quad K < \sqrt{\frac{gm_{3b}C_L}{3gm_{1a}Cgs_{3b}} - 1} \tag{101}$$

4. Slew Rate

For this derivation, we again assume a single-ended capacitive output load, C_L, and a large signal seen at the inputs of the RFC. Suppose *Vin+* goes high, it follows that *M1a* and *M1b* turn off, which forces *M4b* and *M4a* to turn off. Consequently, the drain potential of *M4a* rises and *M6* is turned off whereas *M2a* is forced into deep triode. This directs the tail current, I_T, into *M2b*, which in turn is mirrored by a factor *K* (*M3b*:*M3a*)

into *M5*. Therefore, the total current discharging C_L at *Vout-* is $I_T(3K+1)/4$. On the other hand, only $I_T(K-1)/4$ is available to charge C_L at *Vout+*. This results in a common mode error, which is corrected by the common mode feedback such that the current discharging/charging C_L at either output is the same and equal to $KI_T/2$. The reverse chain of events occurs when *Vin-* goes high, and the end result is a symmetric slew rate expressed by (102) for a differential load of $C_L/2$. The FC slew rate is repeated in (103).

$$SR_{RFC} = \frac{KI_T}{C_L} \qquad (102)$$

$$SR_{FC} = \frac{I_T}{C_L} \qquad (103)$$

By examining (102) and (103), and substituting for the value of $K = 3$, the slew rate of the RFC is enhanced 3 times over the FC for the same power consumption. This, however, is the maximum theoretical limit for this K value. In an actual design the devices assumed to fully turn off still conduct some residual current, and hence reduce the amount reaching the output. Moreover, the accuracy of the current mirrors is degraded for large transients. Nevertheless, with proper sizing and biasing of devices, a slew rate enhancement greater than 2 can be realized for $K = 3$.

5. Noise

The modifications proposed in the RFC add additional devices and alter the signal path. It is therefore imperative to study their effects on the noise performance.

For the purpose of comparison with the FC, the thermal and flicker noise components of the RFC are examined individually to reduce clutter, and following the same procedure adopted in Chapter IV. We begin by evaluating the output current thermal noise PSD of the RFC, which is expressed in (104). Note that the cascode devices are excluded in (104), as their noise contribution was shown to be negligible in Chapter IV.

$$\overline{i_{oT}^2} = 4k_BT\gamma\left[2gm_{1a} + 2K^2 gm_{1b} + 2gm_{3a} + 2K^2 gm_{3b} + 2gm_9\right] \tag{104}$$

By observing that $gm_{1a} = gm_{1b}$, and $gm_{3a} = Kgm_{3b}$, (104) becomes

$$\overline{i_{oT}^2} = 8k_BT\gamma\left[gm_{1a}\left(1+K^2\right) + gm_{3a}\left(1+K\right) + gm_9\right]. \tag{105}$$

The result in (105) can be referred to the input through the amplifier transconductance, Gm_{RFC}, given by (96) to result in the input referred thermal noise PSD.

$$\overline{v_{iT}^2} = \frac{\overline{i_{oT}^2}}{Gm_{RFC}^2} = \frac{8k_BT\gamma}{gm_{1a}\left(1+K\right)}\left[\frac{\left(1+K^2\right)}{\left(1+K\right)} + \frac{gm_{3a}}{gm_{1a}} + \frac{gm_9}{gm_{1a}\left(1+K\right)}\right] \tag{106}$$

Or equivalently by substituting the *gm* expression of (55),

$$\overline{v_{iT}^2} = \frac{8k_BT\gamma}{\sqrt{\frac{\mu_P C_{ox}\left(W/L\right)_{1a} I_T}{2}}}\left[\frac{\left(1+K^2\right)}{\left(1+K\right)^2}\right. $$
$$\left. + \frac{1}{1+K}\sqrt{K\frac{\mu_N}{\mu_P}\frac{\left(W/L\right)_{3a}}{\left(W/L\right)_{1a}}} + \frac{1}{\left(1+K\right)^2}\sqrt{\left(K-1\right)\frac{\left(W/L\right)_9}{\left(W/L\right)_{1a}}}\right] \tag{107}$$

To minimize the thermal noise component, we can maximize I_T and $(W/L)_{1a}$ and minimize $(W/L)_{3a}$, $(W/L)_9$ and K. However, K has to be *greater than* 1. Otherwise, *M5-M10* will conduct zero current.

Now considering the output current flicker noise PSD, we can write

$$\overline{i_{of}^2} = \frac{I_T}{2C_{ox}f}\left[\frac{K_{FP}}{L_{1a}^2} + K^2\frac{K_{FP}}{L_{1b}^2} + K\frac{K_{FN}}{L_{3a}^2} + K^2\frac{K_{FN}}{L_{3b}^2} + (K-1)\frac{K_{FP}}{L_9^2}\right] \qquad (108)$$

By observing that $L_{1a} = L_{1b}$, and $L_{3a} = L_{3b}$, (108) becomes

$$\overline{i_{of}^2} = \frac{I_T}{2C_{ox}f}\left[(1+K^2)\frac{K_{FP}}{L_{1a}^2} + K(1+K)\frac{K_{FN}}{L_{3a}^2} + (K-1)\frac{K_{FP}}{L_9^2}\right] \qquad (109)$$

To obtain the input referred flicker noise PSD, we refer (109) to the input through *Gm_{RFC}*, which results in

$$\overline{v_{if}^2} = \frac{\overline{i_{of}^2}}{Gm_{RFC}^2} = \frac{K_{FP}}{\mu_P C_{ox}^2 W_{1a}L_{1a}f}\left[\frac{(1+K^2)}{(1+K)^2} + \frac{K}{(1+K)}\frac{K_{FN}}{K_{FP}}\left(\frac{L_{1a}}{L_{3a}}\right)^2 + \frac{(K-1)}{(1+K)^2}\left(\frac{L_{1a}}{L_9}\right)^2\right] \qquad (110)$$

To minimize the flicker noise component, we can maximize W_{1a}, L_{3a} and L_9 and minimize K. Once L_{3a}, L_9 and K are set, a minimum value for (110) occurs at

$$L_{1a} = \left[\frac{K(1+K)}{(1+K^2)}\cdot\frac{1}{L_{3a}^2} + \frac{(K-1)}{(1+K^2)}\cdot\frac{1}{L_9^2}\right]^{-1/2} \qquad (111)$$

Finally, in order to have a meaningful comparison between the noise performance of the FC and the RFC, (106) and (110) need to be transformed in terms of the parameters found in (C-29) and (C-30) of Appendix C respectively. To do so we note that $gm_{1a} = 2gm_1/(1+K)$, $gm_{3a} = Kgm_3/(1+K)$, $W_1 = 2W_{1a}$, $L_{1a} = L_1$, $L_{3a} = L_3$ and $K = 3$. The transformed (106) and (110) are given by (112) and (114), whereas (C-29) and (C-30) are repeated here in (113) and (115), respectively. A first look through (112)-(115) is inconclusive as to which has lesser noise. However, since two terms in (112) and (114) are smaller than their counterparts in (113) and (115), it is likely the RFC has a lesser or equivalent noise to that of the FC.

$$\overline{v_{iT,RFC}^2} = \frac{8k_B T\gamma}{gm_1}\left[\frac{5}{4} + \frac{3}{4}\frac{gm_3}{gm_1} + \frac{1}{4}\frac{gm_9}{gm_1}\right] \tag{112}$$

$$\overline{v_{iT,FC}^2} = \frac{8k_B T\gamma}{gm_1}\left[1 + \frac{gm_3}{gm_1} + \frac{gm_9}{gm_1}\right] \tag{113}$$

$$\overline{v_{if,RFC}^2} = \frac{K_{FP}}{\mu_P C_{ox}^2 W_1 L_1 f}\left[\frac{5}{4} + \frac{3}{2}\frac{K_{FN}}{K_{FP}}\left(\frac{L_1}{L_3}\right)^2 + \frac{1}{4}\left(\frac{L_1}{L_9}\right)^2\right] \tag{114}$$

$$\overline{v_{if,RFC}^2} = \frac{K_{FP}}{\mu_P C_{ox}^2 W_1 L_1 f}\left[1 + 2\frac{K_{FN}}{K_{FP}}\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_9}\right)^2\right] \tag{115}$$

6. *Input Offset*

The input offset variance of the RFC can be expressed as the sum of all device drain-current variances seen at the output, and then referred to the input using Gm_{RFC}.

Using (86), where A_{V_T} is the area proportionality constant of V_T according to Pelgrom's mismatch model [63], we can write the RFC output drain-current variance as

$$\sigma^2(I_D) = 2\left[A_{V_{TP}}^2 \left(\frac{gm_{1a}^2}{W_{1a}L_{1a}} + K^2 \frac{gm_{1b}^2}{W_{1b}L_{1b}} \right) + A_{V_{TN}}^2 \left(\frac{gm_{3a}^2}{W_{3a}L_{3a}} + K^2 \frac{gm_{3b}^2}{W_{3b}L_{3b}} \right) + A_{V_{TP}}^2 \frac{gm_9^2}{W_9 L_9} \right] \quad (116)$$

By observing that $W_{1a} = W_{1b}$, $L_{1a} = L_{1b}$, $W_{3a} = KW_{3b}$, $L_{3a} = L_{3b}$, $gm_{1a} = gm_{1b}$, and $gm_{3a} = Kgm_{3b}$, (116) becomes

$$\sigma^2(I_D) = 2\left[gm_{1a}^2 \frac{A_{V_{TP}}^2}{W_{1a}L_{1a}}(1 + K^2) + gm_{3a}^2 \frac{A_{V_{TN}}^2}{W_{3a}L_{3a}}(1 + K) + gm_9^2 \frac{A_{V_{TP}}^2}{W_9 L_9} \right] \quad (117)$$

The result in (117) can be converted to the input referred offset through Gm_{RFC}, which after some algebra gives the input offset variance as

$$\sigma^2(V_{OS,RFC}) = 2\frac{A_{V_{TP}}^2}{W_{1a}L_{1a}}\left[\frac{(1 + K^2)}{(1 + K)^2} + \frac{K}{(1 + K)}\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{L_{1a}}{L_{3a}}\right)^2 + \frac{(K - 1)}{(1 + K)^2}\left(\frac{L_{1a}}{L_9}\right)^2 \right] \quad (118)$$

To minimize the input offset, we can maximize W_{1a}, L_{3a} and L_9, and minimize K. Once W_{1a}, L_{3a}, L_9 and K are set, a minimum value for (118) occurs at

$$L_{1a} = \left[\frac{K(1 + K)}{(1 + K^2)}\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2 \frac{1}{L_{3a}^2} + \frac{(K - 1)}{(1 + K^2)} \cdot \frac{1}{L_9^2} \right]^{-\frac{1}{2}} \quad (119)$$

Again, for a meaningful comparison between the FC and the RFC, (118) needs to be transformed in terms of the parameters found in (C-32). To do so we note that $W_1 = 2W_{1a}$, $L_{1a} = L_1$, $L_{3a} = L_3$ and $K = 3$. The transformed (118) is given by (120), whereas (C-32) is repeated here in (121) for convenience.

$$\sigma^2\left(V_{OS,RFC}\right) = 2\frac{A_{V_{TP}}^2}{W_1 L_1}\left[\frac{5}{4} + \frac{3}{2}\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{L_1}{L_3}\right)^2 + \frac{1}{4}\left(\frac{L_1}{L_9}\right)^2\right] \tag{120}$$

$$\sigma^2\left(V_{OS,FC}\right) = 2\frac{A_{V_{TP}}^2}{W_1 L_1}\left[1 + 2\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_9}\right)^2\right] \tag{121}$$

Once again, a first look at (120) and (121) is inconclusive as to which has lesser input offset. However, since two terms in (120) are smaller than their counterparts in (121), it is likely the RFC has a lesser or equivalent input offset to that of the FC.

7. Efficiency

In Chapter IV an efficiency parameter, η, was defined as the ratio of the amplifier transconductance to the quiescent DC current consumed. Here we examine the efficiency of the RFC, which is expressed in (122).

$$\eta_{RFC} = \frac{Gm_{RFC}}{I_T + \frac{I_T}{2}\left(K-1\right)} = \frac{gm_{1a}\left(1+K\right)}{\frac{I_T}{2}\left(1+K\right)} = \frac{2gm_{1a}}{I_T} \tag{122}$$

The result in (122) is of great interest. Recall that gm_1 of the FC is twice gm_{1a} of the RFC. This means the efficiency of the RFC is twice that of the FC given by (C-28), or equal to that of the Telescopic given by (C-6). More importantly, the efficiency of the RFC is independent of the current mirror factor K, unlike the efficiency of the current mirror OTA described by (C-17).

8.   *Area and Power*

Amplifier design is application specific. However, the amplifier bandwidth, gain and slew rate are arguably the most critical design criteria. The foregoing analysis shows that for practically the same area and power consumption, the RFC delivers twice the bandwidth, $8-10$dB expected higher gain, and more than twice the slew rate of the FC. Now suppose we take the RFC (call it RFC1) and reduce the widths of all devices by half to produce RFC2, *where RFC2 now occupies half the area and uses half the current of the RFC1, and hence the FC*. It follows that (96), (102), (112), (114), and (120) become (123), (124), (125), (126), and (127) respectively.

$$Gm_{RFC2} = \frac{gm_1}{4}(1+K) \tag{123}$$

$$SR_{RFC2} = \frac{KI_T}{2C_L} \tag{124}$$

$$\overline{v_{iT,RFC2}^2} = \frac{8k_BT\gamma}{gm_1}\left[\frac{5}{2} + \frac{3}{2}\frac{gm_3}{gm_1} + \frac{1}{2}\frac{gm_9}{gm_1}\right] \tag{125}$$

$$\overline{v_{if,RFC2}^2} = \frac{K_{FP}}{\mu_P C_{ox}^2 W_1 L_1 f} \left[\frac{5}{2} + 3\frac{K_{FN}}{K_{FP}} \left(\frac{L_1}{L_3}\right)^2 + \frac{1}{2}\left(\frac{L_1}{L_9}\right)^2 \right] \qquad (126)$$

$$\sigma^2\left(V_{OS,RFC2}\right) = 2\frac{A_{V_{TP}}^2}{W_1 L_1} \left[\frac{5}{2} + 3\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2 \left(\frac{L_1}{L_3}\right)^2 + \frac{1}{2}\left(\frac{L_1}{L_9}\right)^2 \right] \qquad (127)$$

Examining (123) shows the RFC2 to have the same transconductance as the FC, whereas (124) shows the RFC2 still has a better slew rate than the FC. Equations (125)-(127), however, demonstrate a degradation in noise and input offset compared to RFC1, and hence FC.

C. Characterization

To validate the theoretical results, a FC amplifier was designed as a benchmark in a mainstream 0.18μm CMOS process using core devices. The design procedure followed proven analog design practices; a large input pair in weak/moderate inversion to maximize bandwidth and minimize noise and offset, and current mirror devices with long channels biased in strong inversion to improve accuracy and output impedance. The main constraint applied to the design is a power budget of 800μA. Once the FC design was finalized, RFC1 and RFC2 were derived as outlined in Sections *A* and *B.8*.

A single-ended version of the amplifiers was used in the setup of Fig. 52 to simplify the characterization. To preserve the high output impedance and limit the DC output current drawn, *R* was set to be 560kΩ. As for C_1 and C_2 they were set to 2.2pF and 2.5pF respectively, which yields an overall load of 3.6pF.
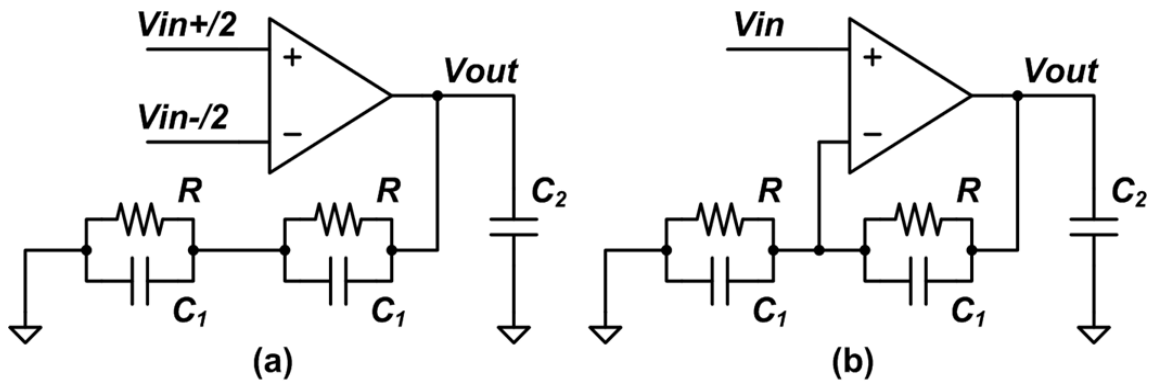
Fig. 52. Amplifier characterization setup; (a) AC response and noise and (b) transient response and input offset.
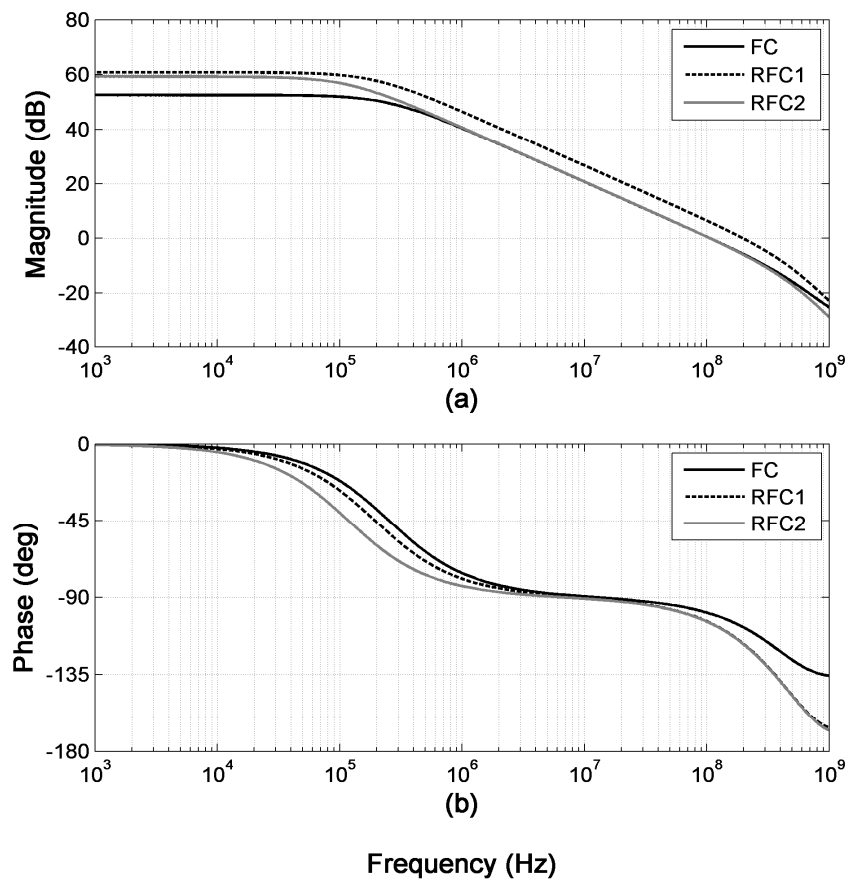
Fig. 53. Amplifiers AC response; (a) magnitude and (b) phase.

As seen in Fig. 53, RFC1 indeed has a wider bandwidth and higher gain than the FC, whereas RFC2 has virtually the same bandwidth, but higher gain than the FC. The higher gain of RFC2 is not surprising; while RFC1 has +6dB gain due to an enhanced Gm, RFC2 has +6dB gain because it consumes half the current—the additional ~3dB improvement is attributed to $M2a$ and $M4a$ as explained in Section $B.2$.

On the other hand, the phase response shows some degradation for both RFC1 and RFC2 with respect to the FC. This is to be expected. As discussed earlier, the addition of current mirrors in the signal path ($M3a$:$M3b$-$M4a$:$M4b$) introduces additional pole-zero pairs. However, these pole-zero pairs are for an NMOS low gain current mirror, which are at high frequencies. Moreover, by satisfying the condition set by (101) for the upper limit of K, the degradation in the phase margin should not significantly affect the transient response of the amplifiers; here the phase margins of the FC, RFC1 and RFC2 are 80.6°, 62.5° and 75.1° respectively.

For the transient response shown in Fig. 54, the input signal was a 500mVpp 10MHz pulse with a common mode level of 450mV. This results in an output of 1Vpp centered at 900mV ($V_{DD}/2$) using the configuration in Fig. 52(b). Undoubtedly, RFC1 has a superior slew rate performance than FC as seen in Fig. 54(a). RFC2 too has a better slew rate performance, which is seen more clearly in Fig. 54(b) as a higher peak output current. Moreover, the settling behavior of both RFC1 and RFC2 was not affected by the phase margin degradation in comparison to FC.
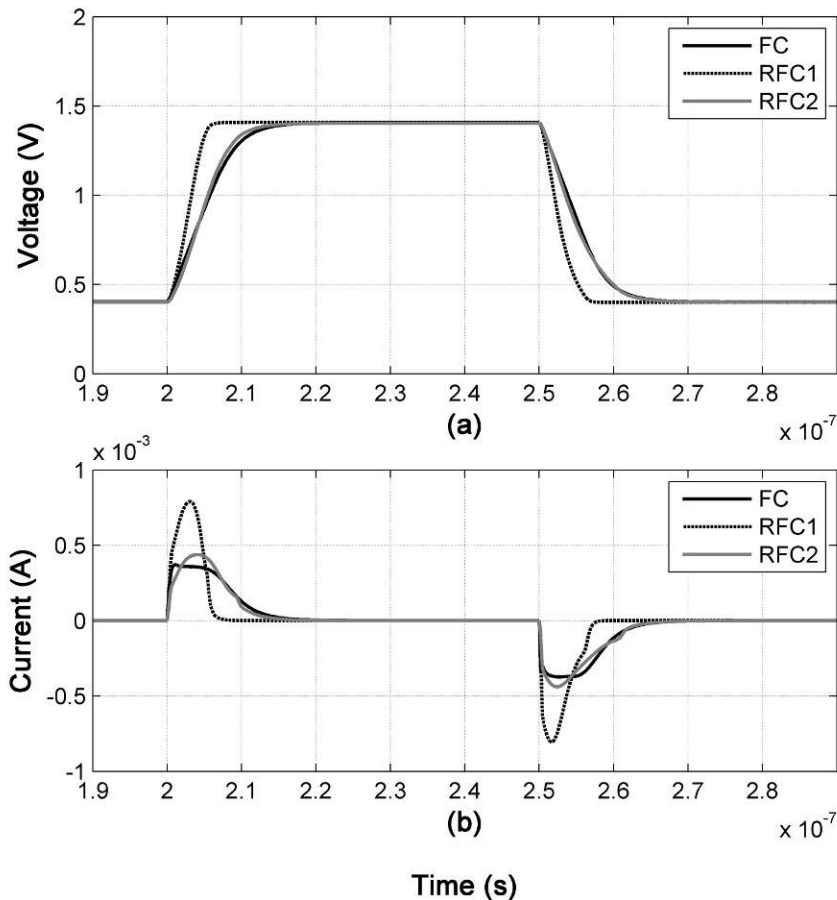
Fig. 54. Amplifiers transient response; (a) output voltage and (b) total output current.

The input offset was measured by applying a 450mV DC input and observing the output in a Monte Carlo simulation. The offset was extracted using (128), where β_{FB} is the feedback factor and A is the amplifier's DC gain, and used to create Fig. 55. While the offset standard deviation is similar for both FC and RFC1, it is larger for RFC2 as demonstrated by (127). Also, a non-zero mean is observed in Fig. 55 due to systematic offset, *not* random process variations. This systematic offset has two components. First, there is a finite current drawn by the load (*2R*), which causes an imbalance in the

currents of the output devices. Second, the feedback network sets the output to 900mV, while ideally *Vout* should follow the gate voltage of *M9*; in the single-ended version of the amplifiers, *M9* in Fig. 49 and Fig. 50 is diode connected to bias *M10*. This systematic offset is more evident in FC because of the lower DC gain.

$$V_{OS} = Vout\left(\beta_{FB} + \frac{1}{A}\right) - Vin \tag{128}$$
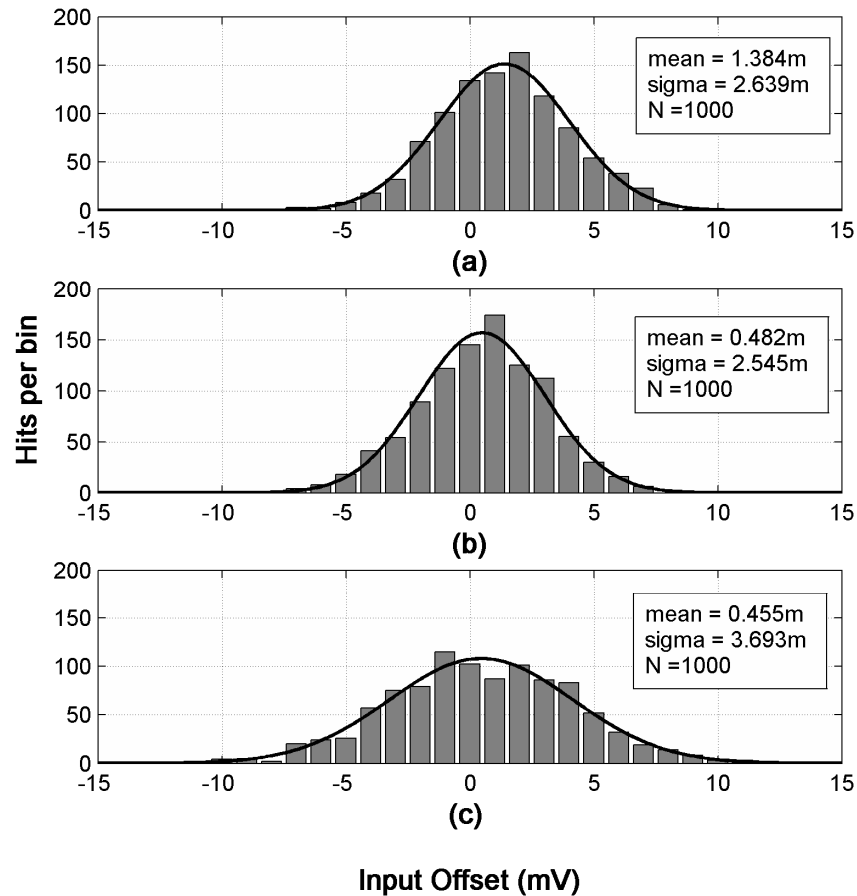
Fig. 55. Input offset distributions; (a) conventional folded cascode, (b) recycling folded cascode 1 and (c) recycling folded cascode 2.

As for noise, Fig. 56 shows the PSD of the input referred noise for the FC, RFC1 and RFC2 over the bandwidth 1Hz–100MHz. Note how the flicker noise dominates the noise performance of advanced CMOS technologies as discussed in Chapter IV. From Fig. 56 we can see how the RFC1 has a better noise performance than the FC, and RFC2 clearly has a worse noise performance as predicted by (125) and (126).
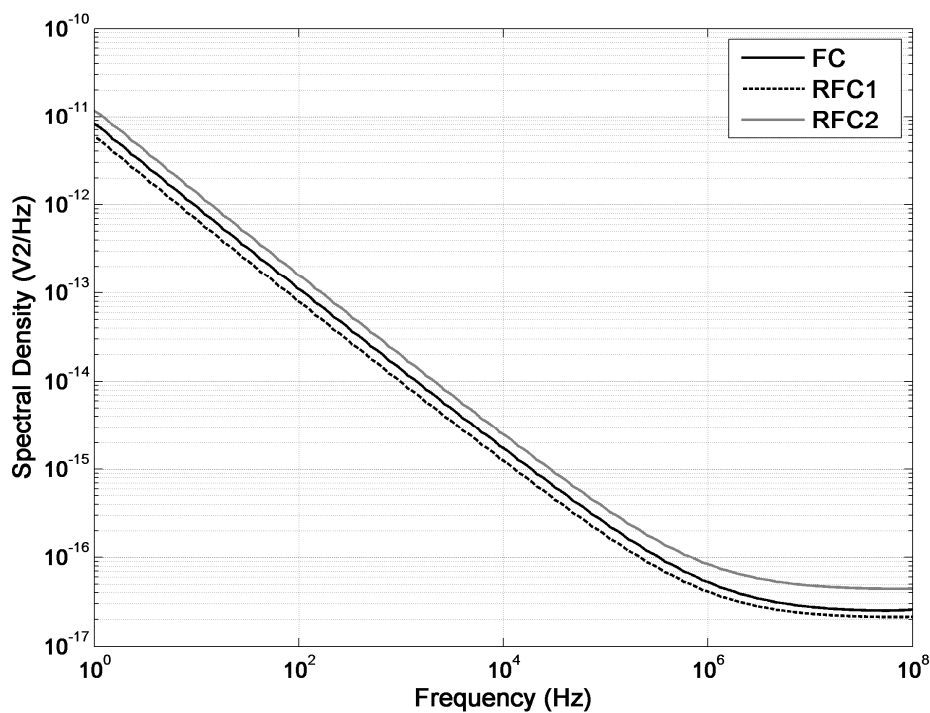
Fig. 56. Input referred noise power spectral density.

A summary of the discussed results is shown in Table 4. In addition, the 0.1% settling time is also included to demonstrate that indeed the modifications proposed to the FC amplifier do enhance the overall general performance.

TABLE 4
AMPLIFIER CHARACTERIZATION RESULTS

Parameter	FC	RFC1	RFC2
Power [μA]	796	782	394
DC Gain [dB]	52.63	60.91	59.32
GBW [MHz]	106.3	197.2	105.9
Phase Margin [deg]	80.6	62.5	75.1
Capacitive Load [pF]	3.6	3.6	3.6
Slew Rate (average) [V/μs]	99.3	231.1	116.5
0.1% Settling Time [ns]	21.7	11.6	21.7
Input Offset (3σ) [mV]	7.917	7.635	11.079
Input Noise (1Hz-100MHz) [μVrms]	53.16	48.48	69.71

D. The Parameter K

Thus far, the analysis and results have been for a single value of K, which was chosen to be 3. This choice was solely made to minimize device changes and keep the area and power consumption of the RFC1 equal to the FC, and hence served as a good example for comparison. However, K can take any value greater than 1. The choice of K is design specific, and hence is left to the designer's judgment. Nonetheless, here are some guidelines.

By steadily increasing *K* we get a:

- Larger transconductance

- Higher slew rate

- Degrading phase margin (best phase margin achieved at K = 1)

- Degrading noise performance (minimum noise achieved at K = 1)

- Degrading offset performance (minimum offset achieved at K =1)

E. Conclusions

It has been demonstrated, both in theory and simulation results, that the proposed modifications to the conventional folded cascode, using the same area and power budgets, can boost the gain, bandwidth and slew rate without affecting the noise performance or introducing excess offset. On the other hand, by using half the area and half the power budgets of the conventional folded cascode, the proposed amplifier is still capable of delivering the same or even better dynamic performance, but on the expense of a 1.7dB noise increase and up to 40% added offset.

CHAPTER VI

COMMON MODE FEEDBACK[*]

The use of fully-differential amplifiers has several advantages over their single-ended counterparts; an increased output signal range, a better phase response and high tolerance to common mode noise are a few examples. Unlike single-ended amplifiers, however, their output common mode (CM) level—the level about which the signal alternates—is not well defined.
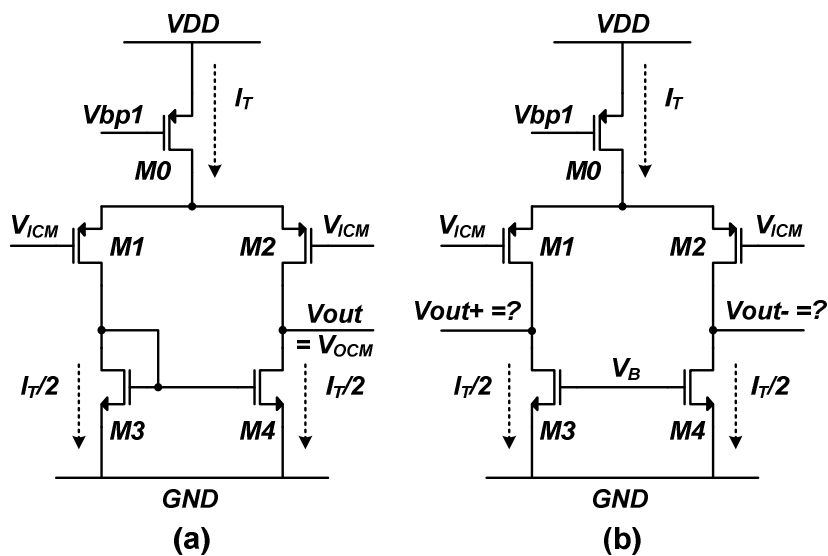
Fig. 57. The differential pair amplifier; (a) single-ended and (b) fully-differential.

Consider the single-ended amplifier in Fig. 36(a), and suppose an external feedback network is designed to set the input terminals at V_{ICM} and the output at V_{OCM}.

The current generated by the V_{ICM} through *M1* creates a voltage drop across the diode connected transistor *M3*, which in turn dynamically biases *M4*. This dynamic bias ensures that the difference of the current through *M2* and *M4* flowing into the amplifier load will generate V_{OCM}.

On the other hand, if the differential version of the same feedback network is applied to the fully-differential amplifier in Fig. 57(b), and *M3* and *M4* had a same fixed gate bias V_B, then the outputs will drift and saturate to one of the supply rails rendering the amplifier useless. This happens because the difference between the currents generated in *M1* and *M2* by V_{ICM} from that generated in *M3* and *M4* by V_B is not necessarily what is needed to establish and sustain V_{OCM} at the output. Hence, additional feedback is needed to dynamically bias *M3* and *M4* and set the output CM level to V_{OCM}. This is known as common mode feedback (CMFB), and a general fully-differential amplifier representation with CMFB is given in Fig. 58.
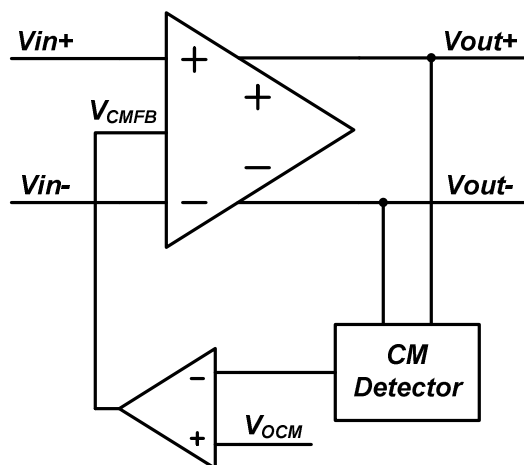
Fig. 58. Fully differential amplifier with CMFB.

In Fig. 58, a CM detector is used to extract the CM level of the output, which given its differential nature is a simple averaging process. In order to capitalize on the output signal headroom of fully-differential amplifiers, the output CM is generally centered between the supply rails, especially in low voltage applications. This is achieved by a comparison with V_{OCM} where the outcome is fed back to the amplifier to adjust its bias levels; in the case of the amplifier in Fig. 57(b), V_{CMFB} replaces the bias V_B of *M3* and *M4* so that their currents adjust to match those of *M1* and *M2* and set V_{OCM} as the CM output.

A. *Continuous Time vs. Switched Capacitor CMFB*

CMFB implementations can be classified under two main categories, continuous time and SC. Generally, a SC CMFB is favored in a SC system such as a pipeline ADC since the clock phases necessary for its operation are preexistent. However, the preferred choice of SC CMFB is not just based on mere convenience. Continuous time CMFB is based on transistors which increase the power budget, and often use current mirrors which introduce extra poles in the CMFB loop that effectively reduce its bandwidth and stability [81]-[82]. These shortcomings are mostly alleviated in SC CMFB.

B. *Switched Capacitor CMFB*

The most commonly used SC CMFB implementation is presented in Fig. 59 [83]. In this implementation capacitors C_2 perform the CM detection by simply averaging the output voltage. As for the comparison with V_{OCM} as seen in Fig. 58 it is performed in two

phases. During Φ_1 capacitors C_1 are pre-charged to the difference of the desired output

CM level V_{OCM} and the ideal voltage V_{REF} needed to bias the current sources/sinks in the

amplifier to achieve the desired level. In Φ_2 the charge of C_1 is shared with C_2 such that

the voltage across C_2 becomes V_{OCM} - V_{REF}. Should the average of *Vout+* and *Vout-* be

different than V_{OCM} by some δ, then V_{CMFB} is shifted by the same δ from V_{REF} which

represents a unity gain comparison. This repeats over a few cycles where eventually δ

approaches 0 if the common mode loop gain is sufficiently large.
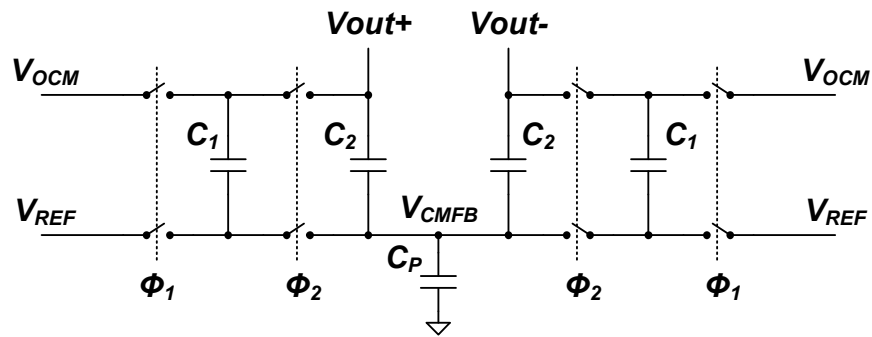
Fig. 59. Classical switched capacitor CMFB circuit.

There are some considerations necessary for an efficient implementation of a SC

CMFB. Primarily, we consider the CMFB loop bandwidth. The capacitors C_2 increase

the differential mode (DM) load and therefore should be minimized so as not to

significantly slow down the amplifier. However, as V_{CMFB} biases the gate of a current

source/sink, there is a finite parasitic capacitance C_P at that node. C_P along with C_2

determine the high frequency feedback factor β of the CMFB loop where $\beta = 2C_2/(2C_2$

$+ C_P)$. To maximize the CMFB loop bandwidth, β needs to be maximized which creates

a trade-off between the DM bandwidth and CMFB loop bandwidth. Fortunately, while it is beneficial to have a fast CMFB loop, it is not necessary for it to be comparable to the differential mode (DM) loop. This is because CM disturbances are generally small and the accuracy at which the CM is set can be an order of magnitude lower than that needed by the DM. Additional considerations pertaining to the time needed to reach stead-state and the absolute steady-state conditions are detailed in [84].

C. Dual Level CMFB

The direct auto-zeroing technique [41] presented in Chapter III is a reliable and power conscious method to eliminate the low frequency disturbances and amplifier DC offset in applications where the amplifier is reset in one of the clock phases. Some examples of circuits using the direct auto-zeroing technique to reduce amplifier offset are the S/H and MDAC shown in Fig. 60, which are extensively used in pipeline ADCs. The output of the S/H and MDAC during Φ_2 are given by (129) and (130) respectively, where V_{OS} is the amplifier offset, M is the effective number of bits resolved in the pipeline stage and $\beta_{\Phi 2}$ is the amplifier feedback factor during Φ_2. Hence the output is virtually offset free for a sufficiently high open loop gain, A.

$$V_{OUT,\,SH} = \alpha_1 V_{IN} + \frac{\alpha_1 V_{OS}}{(1+A)} \quad, \qquad \alpha_1 = \frac{A}{1+A} \tag{129}$$

$$V_{OUT,\,MDAC} = \alpha_2 2^M V_{IN} + \frac{\alpha_2 2^M V_{OS}}{(1+A)} \quad, \qquad \alpha_2 = \frac{\beta_{\Phi 2} A}{1+\beta_{\Phi 2} A} \tag{130}$$
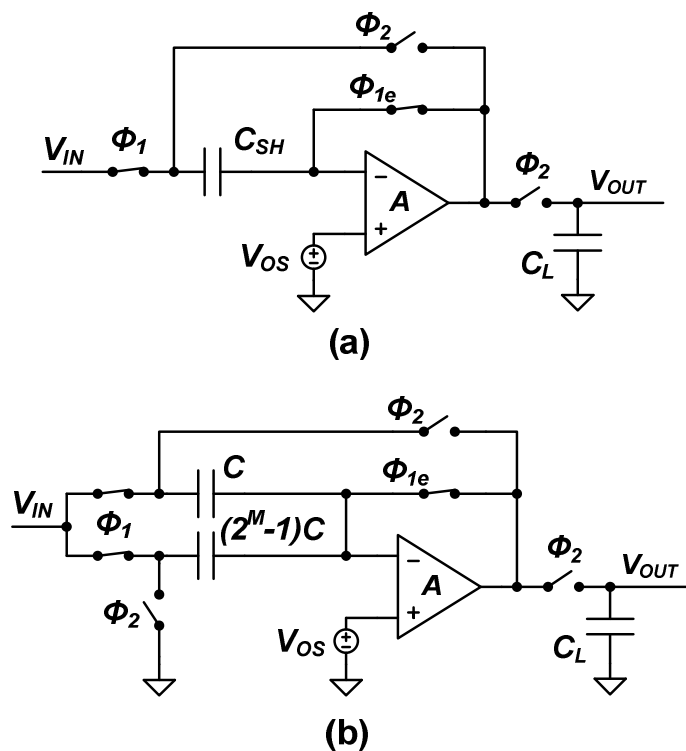
Fig. 60. Direct auto-zeroing offset cancellation in (a) flip-around S/H and (b) pipeline stage MDAC.

In low voltage applications, however, amplifiers are designed such that V_{DD} is in the order of $V_{GS}+2V_{GST}$, which forces the input and output CM, V_{ICM} and V_{OCM}, to be different as illustrated in Fig. 61 for a folded cascode, and prohibits the use of direct auto-zeroing. Hence, current low voltage examples of pipeline ADCs [85]-[87] rely solely on digital correction to overcome the amplifier input offset, which translates to a comparator offset in the next stage. Instead of resetting the amplifier during Φ_1, the input and output terminals are shorted to the appropriate V_{ICM} and V_{OCM} so the amplifier is properly biased during Φ_2. The offset then appears at the output without reduction—the term $(1+A)$ is eliminated from (129) and (130)—and is most severe for the MDAC

where in fact it is amplified; a 10mV input offset in a 2.5bits/stage pipeline stage MDAC

is seen as 40mV at the output and leaves little room for comparator offsets to be

corrected. As it is quite common for non-calibrated pipeline ADCs to utilize high

resolution stages at the beginning of the pipeline to overcome capacitor mismatch, offset

cancellation becomes necessary. In this dissertation, a dual level CMFB is presented to

alleviate this issue.

Fig. 61. Different input and output CM in a low voltage folded cascode amplifier.

In Fig. 62(a) an improved implementation [88] of the classical SC CMFB is

shown, which has the advantage of balancing the load in applications where the

amplifier is used in both clock phases. The drawback, however, is the added switches

and capacitors. By removing C_2 and introducing two CM levels, V_{ICM} and V_{OCM}, a dual

level CMFB is achieved and is shown in Fig. 62(b). The operation of the dual level

CMFB is as follows. During Φ_1 the output CM is set to V_{ICM}. Thus by resetting the

amplifier as in Fig. 60, the offset is sampled and the amplifier is biased properly in preparation for Φ_2. During Φ_2 the output CM is switched to V_{OCM} to maximize the output swing. Hence, direct auto-zeroing is reinstated to actively cancel the offset, despite the different input and output CM of low voltage applications.
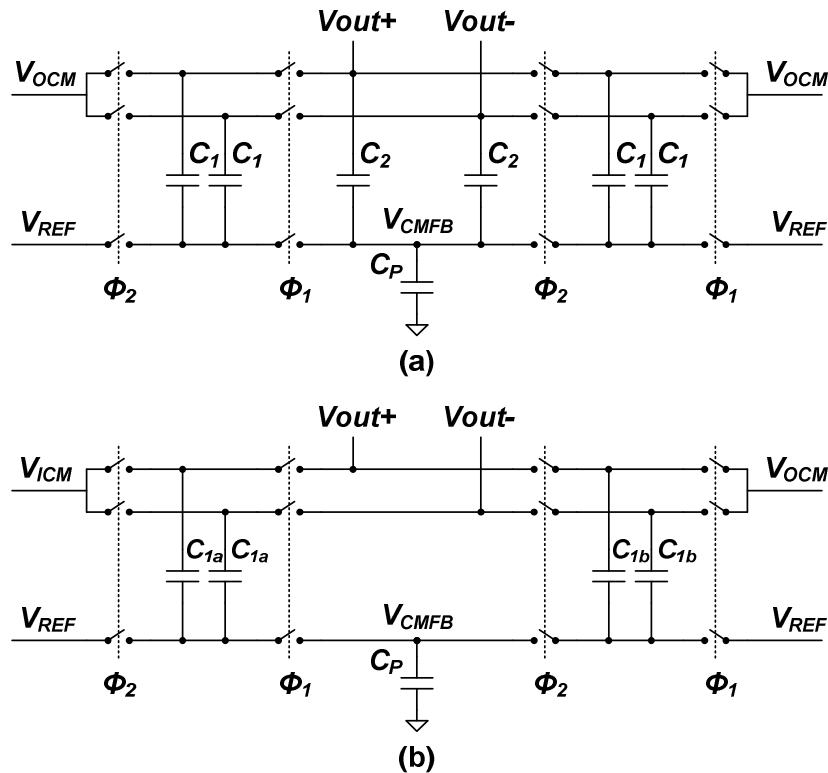
Fig. 62. Switched capacitor CMFB circuits; (a) improved classical circuit and (b) dual level CMFB.

Such dynamic change in the CM output is simulated in TSMC 0.18µm CMOS for the fully-differential implementation of the S/H shown in Fig. 60(a), using the recycling folded cascode amplifier with gain boosting and a supply of 1.2V at sampling rate of 100MS/s. The S/H has a total single-ended capacitive load of 1.4pF. The

waveforms in Fig. 63 show the change in V_{CMFB} and output CM for each clock phase; V_{ICM} is around 300mV to optimize the biasing of a PMOS driver, and V_{OCM} is 600mV to maximize the output swing.
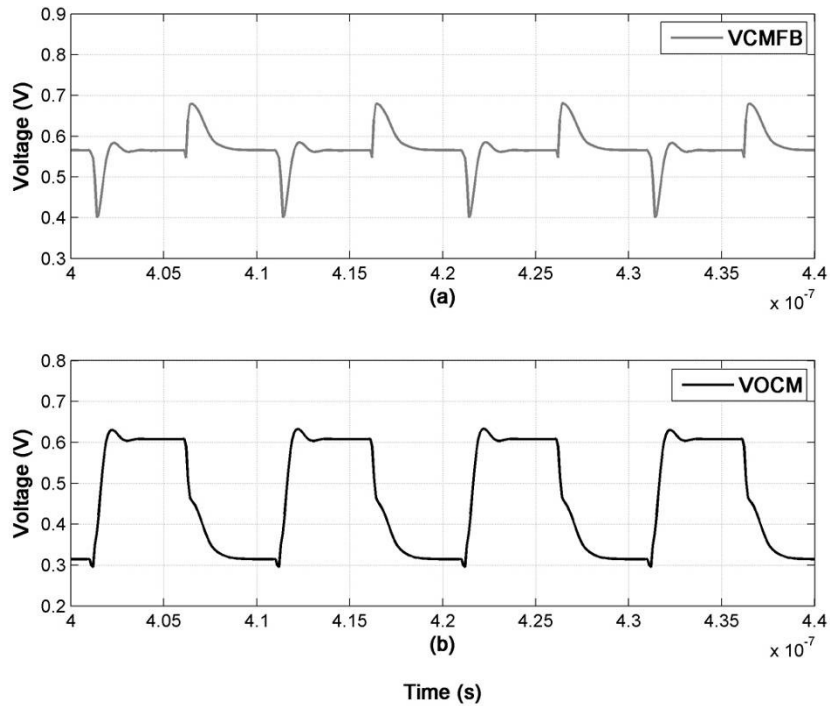
Fig. 63. Dynamic change in output common mode using a dual level CMFB circuit; (a) V_{CMFB} and (b) output CM.

For the CM step of 300mV shown here, the amplifier can completely switch CM levels in less than 2ns within 1% accuracy. An input differential offset of 50mV was imposed in the schematic similar to Fig. 60(a), and Fig. 64 shows the input and sampled output signals demonstrating effective offset sampling in the reset phase and cancellation in the hold phase for a 500mVpp 12.6MHz signal.
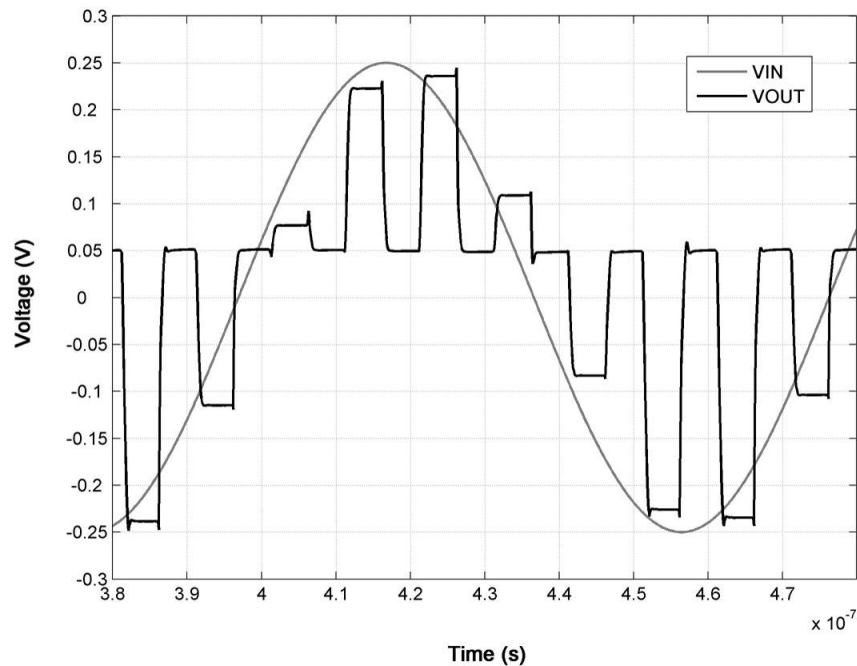
Fig. 64. Sampled signal in a flip-around SHA showing 50mV sampled offset and offset free held output.

D. Design Concerns of Dual Level CMFB

Similar to the classical SC CMFB, there are some considerations with the dual level CMFB. These considerations can be either static and thus related to the steady-state performance, or dynamic and are best analyzed from the frequency domain perspective.

1. Static Performance

The principal function of the dual level CMFB is to change the CM output level for each clock phase thereby enabling the use of direct auto-zeroing in low voltage applications. When setting the output CM level to V_{ICM}, the V_{DS} drop across the output devices is reduced and so is the gain, which may imply a reduced efficiency in offset

reduction according to (129) and (130). This, however, is not a major issue for multi-stage amplifiers as the gain is mostly provided by the first stage(s) and the last stage is designed for rail-to-rail swing. As for single stage cascode amplifiers, gain boosting techniques are necessary for small settling errors and can be designed to provide sufficient gain even when the output is at V_{ICM}; a gain of only 40dB reduces an effective output offset of 50mV down to 500µV, which has negligible impact on the accuracy of a pipeline stage even at high bits/stage resolution.

Another concern arises from potential different amplifier offsets when the output CM is set to V_{ICM} and V_{OCM}. Again, multi-stage amplifiers are immune to such change, because the last stage contributes negligible offset and isolates the output from the previous stage, thus maintaining the same amplifier offset for both output CM values. Single-stage amplifiers, however, may be affected. It was demonstrated in Chapter IV that the offset contribution of cascode devices is negligible as long as the devices directly connected to the supply rails are kept in saturation. This is further affirmed when gain boosting is used. Therefore, as long as V_{ICM} is greater than one V_{GST} away from the supply rails such that the rail devices are kept in saturation, the offset of single-stage amplifiers will be virtually the same when the CM is set to either V_{ICM} or V_{OCM}.

2. *Dynamic Performance*

The cost of removing C_2 (see Fig. 62) means that for the brief time of clock non-overlap, the amplifier has no CM control. However, high sampling rates have 100-200ps of clock non-overlap, which minimize the risk by allowing for minor CM drifts. Another

aspect of the removal of C_2 is the loss of the direct high frequency CM path. Instead, the finite resistance of the switches added in series with either C_{1a} or C_{1b} has a mild low pass filter effect, which can be optimized with proper switch and capacitor sizing without adversely affecting the CMFB bandwidth. Moreover, the CM feedback factor given here by $\beta = 2C_{1a,b}/(2C_{1a,b}+C_P)$, where C_P represents the parasitics at V_{CMFB} can be optimized to the best compromise in speed and stability.

An added benefit of a CMFB circuits is the additional CM noise reduction they provide to fully-differential amplifiers. However, amplifiers using SC CMFB have been demonstrated to be vulnerable to poor power supply rejection (PSR) performance, [83] and [89], and therefore the PSR of the dual level CMFB is analyzed and compared to the classical implementation. To begin, a fully-differential folded cascode amplifier with CMFB circuit connections is shown in Fig. 65. The CMFB can be substituted with the classical implementation of Fig. 59, or the dual level CMFB of Fig. 62(b). Also shown in Fig. 65 are simple implementations of how to generate V_{REF}, V_{OCM} and V_{ICM}.
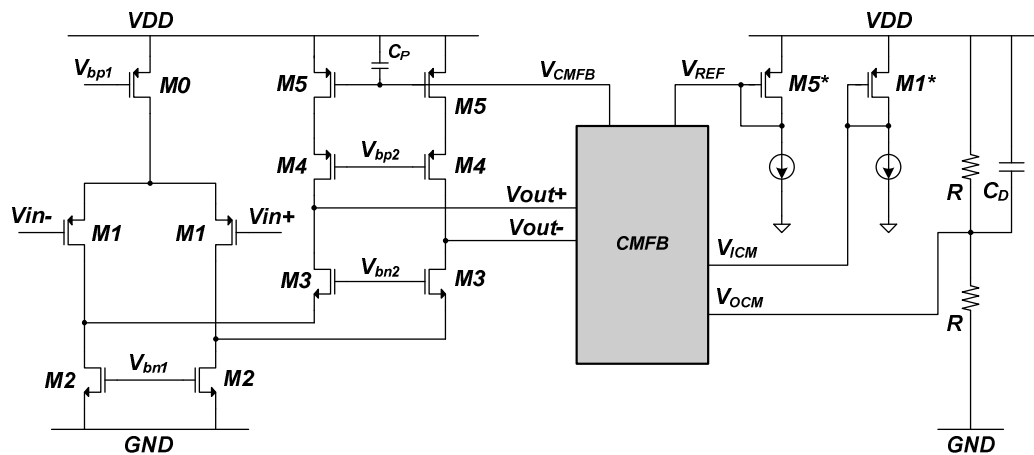
Fig. 65. Fully-differential folded cascode amplifier with CMFB connections.

For the small signal analysis, consider the simplified half-circuit model of Fig. 65 given in Fig. 66 for the classical and dual level CMFB circuits. The amplifier A_{CM} has $M5$ as input driver and shares the same load as the folded cascode. A noise source, v_n, is imposed on V_{DD} and a portion leaks to V_{REF}, V_{OCM} and V_{ICM} with factors of α and γ. The CM output noise is denoted by v_{ocm}. By conserving charge between clock phases, the PSR of the classical and dual level CMFB circuits seen at Φ_2 can be expressed by (131) and (132) respectively. The PSR is defined here as v_{ocm}/v_n, which is desired to be <<1.
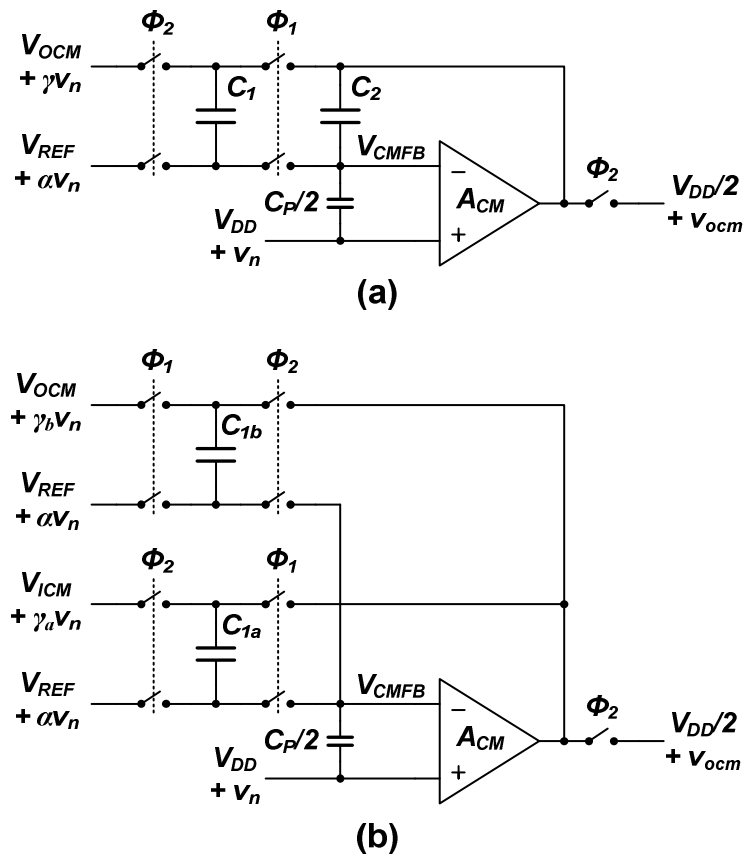
Fig. 66. Half-circuit small signal model of CMFB loop; (a) classical CMFB, and (b) dual level CMFB.

$$PSR_{Classic} =$$

$$\frac{(C_1+C_2)-z^{-1}\left[C_1(\alpha-\gamma)+C_2\right]}{\left(1+\dfrac{1}{A_{CM}}\right)\left[(C_1+C_2)+\dfrac{C_P(C_1+C_2)}{2C_2(1+A_{CM})}-z^{-1/2}\left(\dfrac{C_PC_1}{2C_2(1+A_{CM})}\right)-z^{-1}\left(C_2+\dfrac{C_P}{2(1+A_{CM})}\right)\right]} \quad (131)$$

$$PSR_{dl,CMFB} = \frac{C_{1b}-z^{-1/2}\left[C_{1b}(\alpha-\gamma_b)-C_{1a}\right]-z^{-1}C_{1a}(\alpha-\gamma_a)}{\left(1+\dfrac{1}{A_{CM}}\right)\left[C_{1b}+\dfrac{C_P}{2(1+A_{CM})}+z^{-1/2}C_{1a}-z^{-1}\left(\dfrac{C_P}{2(1+A_{CM})}\right)\right]} \quad (132)$$

However, for sufficiently high gain, (131) and (132) can be simplified and given by (133) and (134).

$$PSR_{Classic}\Big|_{A_{CM}\gg1} = \frac{(C_1+C_2)-z^{-1}\left[C_1(\alpha-\gamma)+C_2\right]}{(C_1+C_2)-z^{-1}C_2} \quad (133)$$

$$PSR_{dl,CMFB}\Big|_{A_{CM}\gg1} = \frac{C_{1b}-z^{-1/2}\left[C_{1b}(\alpha-\gamma_b)-C_{1a}\right]-z^{-1}C_{1a}(\alpha-\gamma_a)}{C_{1b}+z^{-1/2}C_{1a}} \quad (134)$$

To compare the low frequency performance of both CMFB circuits we substitute $z=1$ ($\omega=0$); the results are given in (135) and (136), and indicate the same modest PSR performance for $C_{1a} = C_{1b}$. It is worth to mention, however, that the leakage of v_n onto V_{REF} defined by α, is very close to unity for a wide bandwidth, and hence the PSR performance is dominated by the leakage of v_n onto V_{OCM}, defined by γ. In Fig. 65, V_{OCM} was generated by a resistive voltage divider, which transfers half of v_n onto V_{OCM} resulting in poor PSR. If on the other hand V_{OCM} was generated from a quite source, the PSR of the SC CMFB can be greatly improved. In Fig. 67 the PSR of the dual level

CMFB was simulated using transient periodic steady state analysis; Fig. 67(a) shows α, γ_a and γ_b versus frequency up to $f_s/2$, and Fig. 67(b) shows the PSR of different noise combinations onto V_{ICM} and V_{OCM} for $C_{1a} = C_{1b}$. Clearly, a quite V_{ICM} and V_{OCM} can significantly improve the PSR performance.

$$PSR_{Classic}\big|_{\omega \to 0} = 1 - \alpha + \gamma \tag{135}$$

$$PSR_{dl,CMFB}\big|_{\omega \to 0} = \frac{C_{1b}(1 - \alpha + \gamma_b) + C_{1a}(1 - \alpha + \gamma_a)}{C_{1b} + C_{1a}} \tag{136}$$
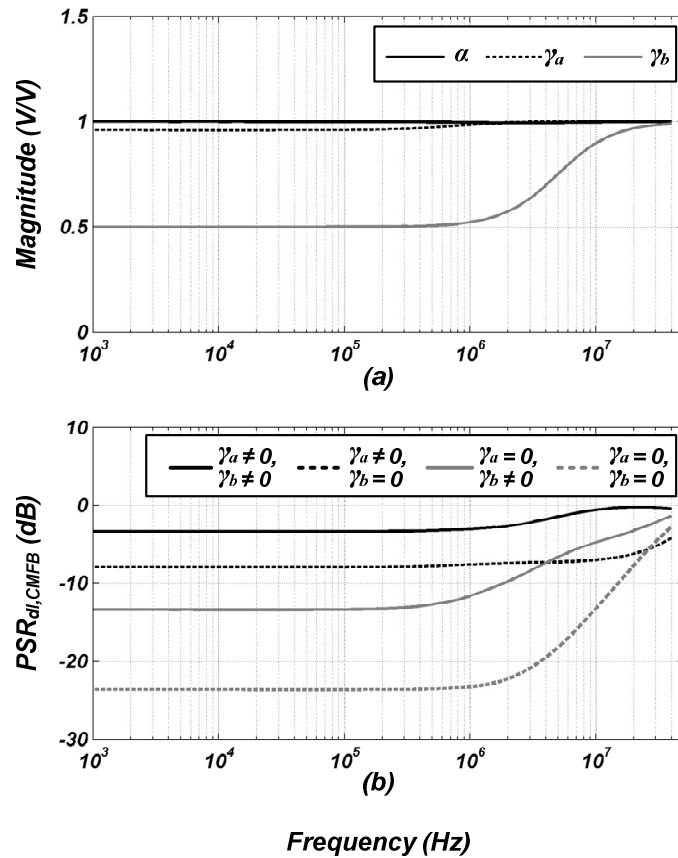
Fig. 67. Effects of supply noise components on the PSR of the dual level CMFB.

As for the high frequency PSR performance, the parasitics and the reduced amplifier gain will have an impact. The high frequency PSR can be found by substituting $z = -1$ ($\omega=\infty$) in (131) and (132) once all powers of z have been changed to positive integers. The results are given by (137) and (138) respectively. Note that both CMFB circuits have again almost the same performance where $1+\alpha-\gamma$ approaches unity at high frequencies in agreement with Fig. 67; γ approaches unity because of the deglitching capacitor C_D in Fig. 65.

$$PSR_{Classic}\Big|_{\omega\to\infty} = \frac{1-\alpha+\gamma}{\left(1+\dfrac{1}{A_{CM}}\right)\left(1+\dfrac{C_P C_1}{C_2\left(1+A_{CM}\right)}\right)} \tag{137}$$

$$PSR_{dl,CMFB}\Big|_{\omega\to\infty} = \frac{C_{1b}\left(1+\alpha-\gamma_b\right)-C_{1a}\left(1+\alpha-\gamma_a\right)}{\left(1+\dfrac{1}{A_{CM}}\right)\left(C_{1b}-C_{1a}\right)} \cong \frac{1+\alpha-\gamma_{a,b}}{\left(1+\dfrac{1}{A_{CM}}\right)} \tag{138}$$

E. Conclusions

The presented dual level CMFB aids the robust implementation of direct auto-zeroing offset cancellation techniques under low voltage conditions, and its effectiveness has been demonstrated with a S/H example. The static errors of the dual level CMFB are negligible so long as sufficient amplifier gain is maintained. As for the dynamic performance, speed optimization techniques were discussed, and the PSR was analyzed and shown to be similar to that of the classical CMFB.

CHAPTER VII

COMPARATORS

Comparators are functional blocks in many analog circuits, particularly pipeline ADCs. In Chapter III, it was demonstrated that the sub-ADC block of a pipeline cell is predominately based on a group of comparators with a handful of supplemental logic gates. In this chapter we discuss the circuit implementation of comparators with a focus on their uses in pipeline ADCs.

A. Comparator Architectures

The main function of a comparator is to amplify the difference between two signals to a level large enough to be detected by subsequent digital circuitry in a very short time. The first architectural difference among comparators is the input signal type, which can be either voltage or current in nature, but in the case of pipeline ADCs voltage comparators are the most widely used. Another architectural difference is the method by which the input difference is amplified to reach logic values, which classifies comparators into amplifier-type or latch-type.

1. Amplifier-Type Comparators

Amplifiers are most commonly used in a closed loop configuration, but if used in open loop can also function as comparators. However, amplifier-type comparators seldom find use in high speed applications. First, the amplifier gain is strongly related to

its output swing, which degrades significantly near rail-to-rail operation necessary to drive subsequent digital circuits; this may require cascading of several amplifiers to achieve the necessary gain, thereby needlessly increasing the complexity, area and power consumption of the comparator. Second, the amplifier is ultimately limited by its slew rate in charging/discharging its load; to achieve a faster rail-to-rail transition will generally dictate a higher bias current. Therefore, amplifier-type comparators are rarely seen in practical application, apart from slow and low cost designs [90].

2. *Latch-Type Comparators*

At the heart of a latch-type comparator is a pair of back-to-back inverters—a latch—from which this comparator type gets its name. Latch-type comparators are generally faster than amplifier-type comparators due to the positive feedback loop of the latch. To briefly examine how a latch-type comparator functions, consider the conceptual schematic in Fig. 68(a). Focusing on the latch alone, and assuming the following small-signal parameters for the inverters: transconductance gm_{Latch}, conductance $g_{O,Latch}$ and output capacitance C_{Latch}, we can write the following KCL equations at the output of each inverter.

$$gm_{Latch}V_A + g_{O,Latch}V_{\bar{A}} + C_{Latch}\frac{dV_{\bar{A}}}{dt} = 0 \tag{139}$$

$$gm_{Latch}V_{\bar{A}} + g_{O,Latch}V_A + C_{Latch}\frac{dV_A}{dt} = 0 \tag{140}$$

Equations (139) and (140) can be combined as seen in (141), where $V_\Delta = V_A - V_{\overline{A}}$. When integrated, (141) results in (142) where τ_{Latch} represents the latch time constant. Therefore, to enhance the speed of the latch, one needs to minimize the load capacitance at the nodes V_A and $V_{\overline{A}}$ and maximize the transconductance of the inverters; with proper design, decision times in the order of 100s of pico seconds can be achieved.

$$\left(gm_{Latch} - g_{O,Latch}\right) V_\Delta - C_{Latch} \frac{dV_\Delta}{dt} = 0 \tag{141}$$

$$V_\Delta = V_\Delta(0)\, e^{\frac{\left(gm_{Latch} - g_{O,Latch}\right)}{C_{Latch}} t} = V_\Delta(0)\, e^{\frac{t}{\tau_{Latch}}} \tag{142}$$
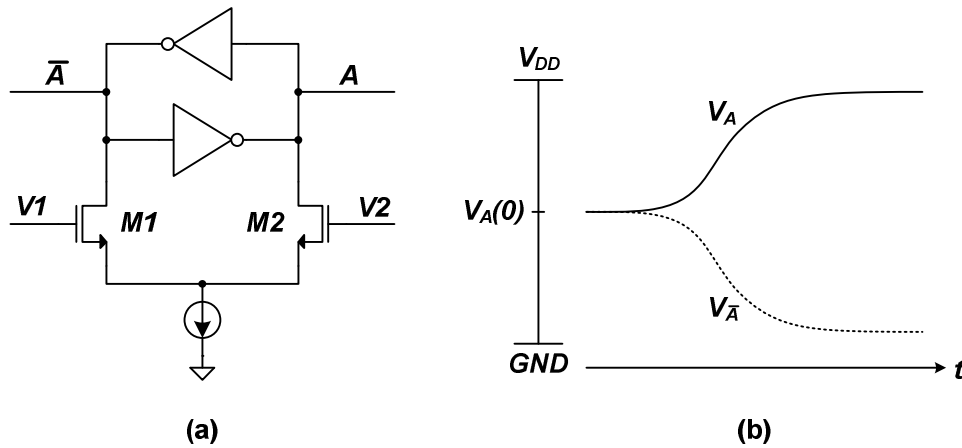
Fig. 68. Latch-type comparator; (a) conceptual schematic and (b) time-domain waveforms.

The exponential behavior of the latch described by (142) is triggered by the input pair *M1* and *M2*; according to the values of *V1* and *V2*, a small differential current is

generated which causes an imbalance in the charge held by the output capacitance at V_A and $V_{\bar{A}}$ thus triggering the exponential behavior of the latch. The resulting time-domain waveforms of V_A and $V_{\bar{A}}$ are shown in Fig. 68(b); beginning at some initial value $V_A(0)$, V_A and $V_{\bar{A}}$ start drifting exponentially towards opposite supply rails. This exponential behavior eventually dampens as the inverters saturate at either rail due to the conductance $g_{O,Latch}$ increasing and transconductance gm_{Latch} diminishing. Once the latch reaches a stable condition, it will retain that state until reset for a new comparison to take place. Therefore, latch-type comparators are naturally clocked comparators and are commonly followed by an SR latch to preserve their output after reset for post processing while waiting for a new comparison event to take place.

Because of their high speed operation and fairly low power consumption, latch-type comparators are preferred over amplifier-type comparators, and are extensively used in ADCs, particularly in Pipeline and Flash ADCs. The following sections are devoted to the sub-division of latch-type comparators: Static and Dynamic.

B. Static Comparators

Static comparators continually conduct a fixed and known bias current regardless of the comparator state; reset or latched. There are several topologies that fall under this category, and are easily classified as class A or class AB output similar to the comparator architectures of Fig. 69.

1. Class A Output

First, let us consider the class A output comparator in Fig. 69(a) [91]-[93]. When V_{Latch} is HIGH, *M1-M4* pre-amplify the difference V_{IP} - V_{IN} and the result is injected as a differential current via *M5-M6* and triggers the latch *M7-M8*. When V_{Latch} goes LOW, *S1* and *S2* pull the comparator outputs to V_{DD}, while *S3* blocks the current path in the latch. Hence, during either phase the steady state current flowing through the comparator is I_B. This topology is fairly fast and can achieve a low input offset by optimizing the operating points and dimensions of *M1-M4*. A simpler class A output comparator topology can be implemented by feeding the output of *M1-M2* directly into a PMOS cross-coupled load. However, this approach eliminates the preamplifier and thus makes the comparator slower and more vulnerable to kickback noise as will be demonstrated in later sections.

Fig. 69. Static latch-type comparators; (a) class A and (b) class AB output.

2. Class AB Output

Now we consider the class AB output comparator in Fig. 69(b) [94]-[98]. When V_{Latch} is HIGH, *M1-M2* convert the difference V_{IP} - V_{IN} into current, which is directly injected into the output nodes thereby triggering the latch *M3-M6*. Here, and unlike Fig. 69(a), the latch is implemented in a true push-pull manner and hence is class AB output. When V_{Latch} goes LOW, *S1* shorts the output nodes, while *S2* blocks the current path in the latch. The outputs finally settle at roughly V_{DD} - $V_{T(3,4)}$. For low voltage applications, this may not be large enough to be considered logic HIGH, and therefore a reset mechanism similar to that of Fig. 69(a) may be used. As for the power consumption, and similar to the class A output comparator, the steady state current during either phase flowing through the comparator of Fig. 69(b) is I_B.

An advantage of the class AB output over the class A is the shorter regeneration time in the latch due to a larger transconductance—(gm_3 + gm_5) for class AB vs. gm_7 only for class A output—which makes it a faster comparator. However, class AB output comparators may suffer worse input referred offset than class A due to the larger latch transconductance. Nonetheless, because pipeline cells use digital redundancy as in the 1.5bits/stage, they are fairly immune to comparator offsets, which makes class AB output comparators the more attractive choice.

C. Dynamic Comparators

The principal drawback of static comparators is the constant use of power regardless of the comparator being latched or reset. While the power consumed per

comparator could be small, pipeline ADCs may have +20 comparators whose total power may amount to a significant value. Dynamic comparators aim to resolve this inefficiency by consuming power only when needed, and like static comparators there are several variants of dynamic comparators, but virtually all have the same basic core as either architecture of Fig. 70 [99]-[101].
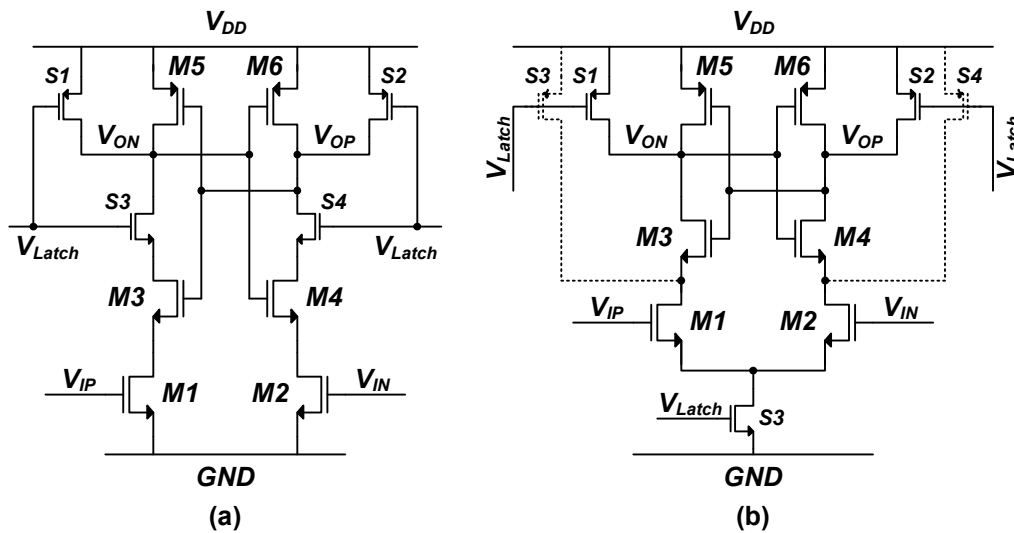
Fig. 70. Dynamic latch-type comparators; (a) resistive and (b) differential pair input.

1. Resistive Divider Input

We begin by analyzing the operation of the resistive divider dynamic comparator in Fig. 70(a). When V_{Latch} is LOW, $S1$ and $S2$ pull the comparator outputs and thus the gates of $M3$-$M6$ to V_{DD}, while $S3$ and $S4$ ensures that $V_{DS(1-4)} = 0$, and hence $V_{GS(3,4)} = V_{DD}$. Note that in this operation mode, the comparator conducts no current. As V_{Latch} goes HIGH, $S1$ and $S2$ release the gates of $M3$-6 while $S3$ and $S4$ pull the drains of $M3$ and $M4$ towards V_{DD}. At this stage, $M3$ and $M4$ enter saturation mode. However, $M1$ and

M2 are operating in triode and act as voltage controlled resistors. Assuming that *M3-M6* are all well-matched, the imbalance of the voltage drop across the r_{ds} of *M1* and *M2* is amplified by *M3* and *M4* thereby triggering the latch.

Once the regeneration is complete, one of the comparator outputs is held at V_{DD} while the other is at *GND*, and the comparator conducts no current. If the V_{Latch} signal had a 50% duty cycle, then the comparator conducts current no more than 50% of the time, which is a significant reduction in power consumption compared to the static latch-type comparators. Naturally, however, the sizing of the devices will dictate the current conducted when the comparator is in the regeneration phase and needs to be limited.

As for its input referred offset, the resistive divider dynamic comparator performance is modest at best. Transistors operating in triode are poorly matched as they are very sensitive to V_{DS} and process variations. Moreover, triode devices *M1* and *M2* have very small gain—near or smaller than unity—which may amplify any mismatch in *M3* and *M4* when referred to the input. Nonetheless, because of the inherent digital redundancy in pipeline cells, offsets in the order of 100mV may be tolerated for 1.5-2.5bits/stage even in low voltage applications, making the resistive divider comparator a viable option for its low power consumption.

2. *Differential Pair Input*

Now consider the differential pair dynamic comparator in Fig. 70(b), neglecting *S3* and *S4*. In the reset phase, when V_{Latch} is LOW, the outputs are held at V_{DD} and hence *M*3 and *M*4 are configured in a diode connection, but conduct no current because *S3* is

off. Also, and due to the diode connection, the sources of *M3* and *M4* and drains of *M1* and *M2* are held at approximately V_{DD} - $V_{T(3,4)}$. The moment V_{Latch} turns HIGH, *M1-M4* are all in saturation and *M1* and *M2* act as a differential pair steering current to either output according to their inputs, and triggering the latch.

Compared to the resistive divider comparator, the power consumption of the differential pair is quite similar; both comparators consume current only in the regeneration phase. However, the differential pair input is superior as far as input referred offset is concerned, and its performance is comparable to that of static comparators. This enhanced performance is primarily attributed to *M1* and *M2* being in saturation when the comparator is latched. Moreover, with the inclusion of *S3* and *S4*, the input referred offset of the differential pair comparator is further enhanced; with *S3* and *S4* included, only *M1* and *M2* are in saturation when the comparator is latched and hence become the sole dominant contributors to input offset. There is, however, a trade-off for using the differential pair comparator over its resistive divider counterpart; the resistive divider comparator has a wider input range.

D. Kickback Noise

The preceding discussion spanned the operation of several comparator architectures and key comparator design issues such as power consumption and input referred offset. Another aspect to be examined here, and perhaps the most critical for high speed and low voltage comparator design, is kickback noise.

The inputs and outputs of a comparator are not perfectly isolated. Thus, the rail-

to-rail transients seen at the output are likely to leak back to the input of the comparator resulting in kickback noise, which can be quite problematic depending on its magnitude and the circuit configuration driving the comparator. In a pipeline ADC for example, the input to a pipeline cell is applied to the comparators of the sub-ADC and sampled by the cell's S/H. Kickback noise generated by the comparators may corrupt the sampled value resulting in conversion errors. This is demonstrated in Fig. 71, where *A* represents the amplifier of the previous stage in the *HOLD* phase, with input and feedback capacitors C_I and C_F respectively; C_L represents the sampling capacitor of the following stage; and *Comp* is a single-path representation of the comparator where the input and output are coupled through capacitor C_C.
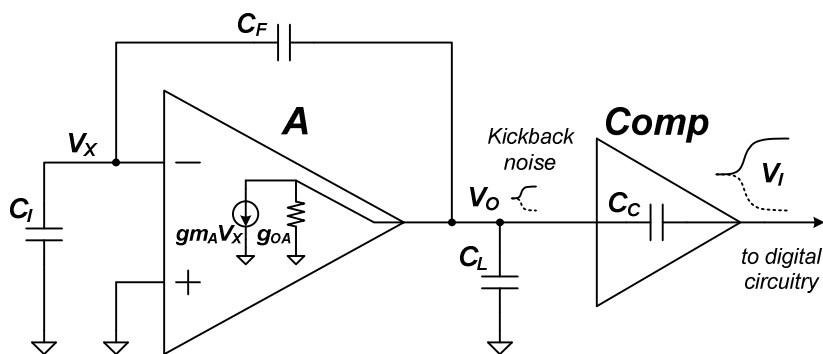
Fig. 71. Kickback noise modeling in a pipeline cell.

Regarding the rail-to-rail transient at the comparator output as a source V_I, we can find the effects of the kickback noise coupling on the sampled value of the next pipeline cell by evaluating V_O across C_L; this is expressed by (143), where $\beta_A = C_F/(C_F + C_I)$ is the feedback factor of amplifier *A*. The kickback noise transfer

function of (143) has a zero at $\omega = 0$ and a high frequency pole ω_{pk} given by (144). Since the comparator is aimed to react very fast, the location of ω_{pk} and the maximum magnitude of the kickback noise transfer function given by (145) for which $\omega >> \omega_{pk}$, are of greater interest.

$$\frac{V_O}{V_I} = \frac{sC_C}{\beta_A gm_A + g_{OA} + s[C_C + C_L + C_F(1-\beta_A)]} \tag{143}$$

$$\omega_{pk} = \frac{\beta_A gm_A + g_{OA}}{C_C + C_L + C_F(1-\beta_A)} \cong \frac{\beta_A gm_A}{C_C + C_L + C_F(1-\beta_A)} \tag{144}$$

$$\left.\frac{V_O}{V_I}\right|_{max} = \left.\frac{V_O}{V_I}\right|_{\omega>>\omega_{pk}} = \frac{C_C}{C_C + C_L + C_F(1-\beta_A)} \tag{145}$$

Through the examination of the modeling results, we make two observations regarding the reduction of kickback noise. First, ω_{pk} coincides with the amplifier's bandwidth, ω_{-3dB}. Intuitively, closed loop wide bandwidth amplifiers such as those used in high speed pipeline ADCs force V_O to behave as a low impedance node, which has a natural tendency to dissipate kickback noise quickly. This is only true as long as the frequency of the transients caused by kickback noise is below the amplifier's ω_{-3dB}, which is maximized when $\beta_A = 1$. Therefore, a possible approach to minimize kickback noise is to design the amplifier's time constant τ_A driving the comparator to be smaller than that of the latch as expressed by (146), and in so doing maximize the amplifier's immunity against kickback noise.

$$\tau_A = \frac{C_C + C_L + C_F(1 - \beta_A)}{\beta_A gm_A + g_{OA}} < \frac{C_{Latch}}{gm_{Latch} - g_{O,Latch}} = \tau_{Latch} \qquad (146)$$

Nevertheless, relying solely on the condition set by (146) to reduce kickback noise may not be practical as it may require increasing the power consumption of amplifier A. This leads to the second observation; the kickback noise magnitude is strongly related to the value of the coupling capacitor, C_C. Indeed, if C_C is reduced, so would be the kickback noise, and that is precisely what almost all kickback noise reduction techniques aim to accomplish.

Before we discuss these techniques, however, let us take a closer look at (145). Note that the values of C_L, C_F and β_A are all predefined by the architecture used to implement the pipeline cells. Also, it seems that a smaller β_A, and thus a larger number of bits per stage, would minimize the kickback noise. On the other hand, and due to capacitor scaling, C_L and C_F become increasingly smaller as the number of bits per stage increases, whereas C_C remains unchanged as the same comparator architecture is generally used throughout the ADC; this effectively increases the effects of kickback noise in latter stages of the pipeline ADC. Moreover, a smaller β_A would reduce the amplifier's natural ability to suppress kickback noise by lowering ω_{pk} as expressed in (144). Therefore, to maximize the pipeline ADC natural immunity against kickback noise induced conversion errors, the use of smaller number of bits per stage is encouraged, especially when an aggressive capacitor scaling approach is used.

1. Kickback Noise Reduction in Static Comparators

In addition to the natural approach of kickback noise reduction outside of the comparator, some design techniques are used to physically limit the value of C_C and here we discuss the most relevant to static comparators.

First, we examine the preamplifier approach [37], [81]. The kickback noise leakage through C_C can be reduced if a preamplifier is inserted between the previous stage amplifier and the latched comparator; this is similar to Fig. 69(a), where *M1-M4* represent the preamplifier and is modeled in Fig. 72.
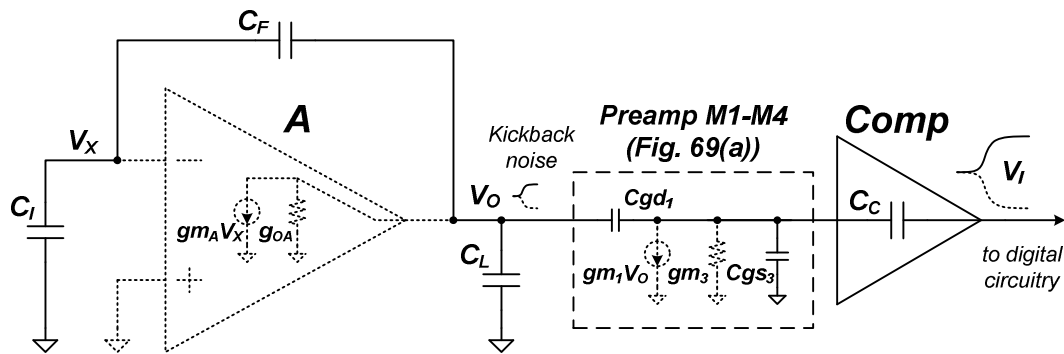
Fig. 72. Kickback noise modeling in a pipeline cell with a preamp driven comparator.

Naturally, deriving the kickback noise transfer function at V_O is more complex than that of Fig. 71, but from an intuitive standpoint, Cgd_1 introduces another zero at $\omega = 0$ and gm_3 introduces another low impedance node in the kickback noise path to dissipate it. It is simple, however, to determine the maximum magnitude of the kickback noise transfer function by evaluating the capacitive path represented in solid lines in Fig. 72; the result is given by (147).

$$\frac{V_O}{V_I}\bigg|_{max,w/\,preamp} = \frac{Cgd_1}{Cgd_1 + C_L + C_F\left(1 - \beta_A\right)} \cdot \frac{C_C}{C_C + Cgs_3 + \dfrac{Cgd_1\left(C_L + C_F\left(1 - \beta_A\right)\right)}{Cgd_1 + C_L + C_F\left(1 - \beta_A\right)}} \qquad (147)$$

Note that (147) is quite similar in form to (145), but there is an added term that is always less than unity. This new term is another tool with which the designer may reduce kickback noise. For example, increasing Cgs_3 directly enhances kickback noise reduction. Nonetheless, the use of preamplifiers to drive the comparators has two main drawbacks. First, the preamplifier adds to the power consumption of the overall comparator. Second, the preamplifier introduces another pole in the signal path ($\omega_p \approx gm_3/Cgs_3$), which slows the comparator response. Both drawbacks make the use of preamplifiers less favorable in high speed and low power designs, despite their effectiveness in reducing kickback noise.

Another approach to kickback noise reduction commonly seen in static comparators is the passive cross-coupled capacitive neutralization as seen in Fig. 73. In the absence of a preamplifier, Cgd in Fig. 73 represents the kickback noise coupling path, and since *M1* and *M2* are generally in saturation it is primarily assumed by the gate-drain overlap capacitance, Cgd_{ov}. With the addition of a cross-coupled pair half the size of *M1* and *M2*, an alternate path for kickback noise is created that counteracts the effect of *Cgd*. Thus the superposition effect of $V_{\bar{A}}$ through Cgd_1 and that of V_A through *(M1)/2* is ideally zero, which leaves V_1 unaffected. The same applies to V_2.

There are, however, some limitations to the use of the cross-coupling neutralization technique in practice as mismatch between of *M1,2* and *(M1,2)/2* is

unavoidable; physical mismatch in size is a limitation induced by process variations, which leads to imperfect kickback noise cancellation. Moreover, saturation conditions in short channel devices are no longer characterized by the classical channel pinch-off where charge vanishes at the drain [56]. Therefore $Cgd_{1,2}$ can be considerably different from Cgd_{ov} provided by *(M1,2)/2* creating an even greater mismatch and consequently only modest kickback noise reduction.
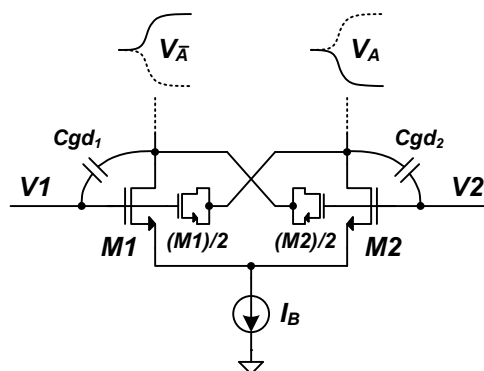
Fig. 73. Passive cross-coupled capacitive neutralization technique.

Finally, an additional technique to reduce the effects of kickback noise is the insertion of cascode devices inline with the differential pair of the comparator as pictured in Fig. 74. Cascode devices are commonly used in amplifiers to enhance their gain by limiting the output induced signal variations across the r_{ds} of the device they are isolating. The same concept can be extended to comparators, but to isolate *Cgd* of *M1* and *M2* from the output. Thus, the effect of $V_{\bar{A}}$ on the drain of *M1* and V_A on the drain of *M2* is initially reduced by the gains of *MC1* and *MC2* respectively. Eventually, *MC1* and *MC2* enter triode and lose their gain as V_A and $V_{\bar{A}}$ reach the supply rails. Therefore, it is

crucial to ensure the bulk terminals of *MC1* and *MC2* are grounded and not shorted to their sources. This guarantees a resistive path, however small, between the drains and sources of *MC1* and *MC2* that impedes the propagation of kickback noise to *V1* and *V2*. Otherwise, Cdb_{C1} and Cdb_{C2} create an easy high frequency path for the kickback noise to propagate to the inputs of the comparator.
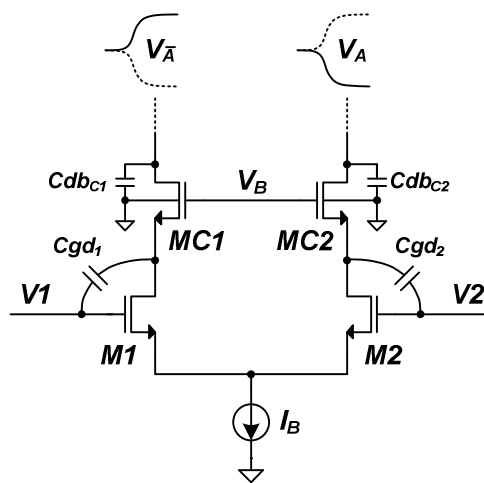
Fig. 74. Kickback noise isolation using cascode devices.

While perhaps the most effective approach to kickback noise reduction, the use of cascode devices shares a drawback with the preamplifier approach, and that is the insertion of an additional pole ($\omega_p \approx gm_{C1}/Cgs_{C1}$) in the signal path which slows the response of the comparator. Moreover, the use of cascode devices may be problematic as voltage supplies continue to shrink. Nonetheless, when used together, as is the common practice, the preceding techniques can significantly reduce the kickback noise of latch-type static comparators.

2. Kickback Noise Reduction in Dynamic Comparators

The techniques described in the previous section are not strictly associated with static comparators, but can also be used to with dynamic comparators. However, because of the different mechanisms of operation and propagation of kickback noise in dynamic comparators compared to their static counterparts, these techniques may not be very effective or efficient. For example, the use of a static power consuming preamp with a dynamic comparator is counter productive as far as power saving is concerned. This section begins with a description of how kickback noise is generated in dynamic comparators, followed by a presentation of a commonly used sampling-based kickback noise reduction technique, and finally proposes a new power conscious approach to kickback noise cancellation.

In static comparators, the primary leakage path of kickback noise was through the gate-drain capacitance, *Cgd*, of the input pair *M1* and *M2*. This is not always the case in dynamic comparators. For instance, Fig. 75(a) shows an enlarged partial schematic of the differential pair dynamic comparator of Fig. 70(b), including explicit representation of the gate-drain parasitics and key waveforms. Unlike the static comparators where the drain potentials of *M1* and *M2* begin at the same voltage and end at opposite supply rails, thus generating kickback noise, the drain potentials of *M1* and *M2* in dynamic comparators begin at the same voltage and end at the same supply rail, which is *GND* in this case.

Hence, and from a signal perspective, it seems that Cgd_1 and Cgd_2 do not provide a leakage path for kickback noise as they experience the same input step. However, what

is not seen in Fig. 75(a) is the dependency of Cgd_1 and Cgd_2 on their respective input values, and it is this input voltage dependency that creates a path for kickback noise. This path is strongest when the differential input is at its maximum ($Cgd_1 \neq Cgd_2$), and virtually nonexistent when the differential input is very small ($Cgd_1 \approx Cgd_2$). The resistive divider dynamic comparator is more sensitive to this kickback noise path as *M1* and *M2* are normally operating in triode, unlike the differential pair comparator where *M1* and *M2* begin their operation in saturation; suppose a maximum differential input is applied to the resistive divider comparator with *V1 > V2*, then it is likely that *M2* is off while *M1* is in deep triode making $Cgd_1 >> Cgd_2$ and inducing a significant kickback signal at the inputs.
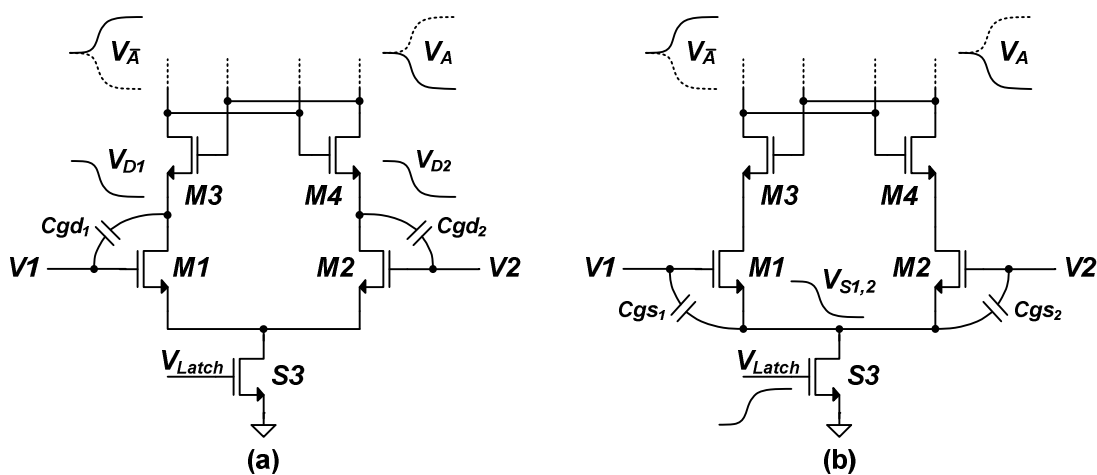

Fig. 75. Kickback noise coupling in dynamic comparators; (a) through *Cgd* and (b) through *Cgs*.

There is also another kickback noise path that is found in dynamic comparators and not static comparators, and that is through Cgs_1 and Cgs_2. The differential pair

comparator is more vulnerable to this path due to the presence of a latched switch at the sources of $M1$ and $M2$ as seen in Fig. 75(b). When V_{Latch} is LOW, the source potential $V_{S1,2}$ of $M1$ and $M2$ is approximately at max$\{V1,V2\} - V_{T(1,2)}$. As V_{Latch} goes HIGH, $V_{S1,2}$ is pulled to GND generating a step that is fed back to the inputs through Cgs_1 and Cgs_2. Similar to the kickback noise path through Cdg described earlier, this path is strongest when the differential input is at its maximum ($Cgs_1 \neq Cgs_2$), and virtually nonexistent when the differential input is very small ($Cgs_1 \approx Cgs_2$). The resistive divider comparator can too suffer from this kickback noise path but at a much smaller scale; if the routing parasitic to GND has a sizable resistance R_{GND}, then the inrush current as the comparator is latched can create a step across R_{GND} leading to kickback noise through Cgs_1 and Cgs_2.

Unfortunately, none of the kickback noise reduction techniques used for static comparators are robust against voltage-dependent capacitors. Therefore, to overcome the effects of kickback noise in dynamic comparator, a sampling based approach is used [102]. This is demonstrated in Fig. 76 for a sub-ADC comparator in a pipeline cell, and the operation is based on a two-phase clock cycle synchronous with that of the pipeline ADC. In the sampling phase, Φ_1, the input and reference voltages are sampled on C_{IN} and C_R respectively, and in the holding/latching phase, Φ_2, the charge is redistributed and applied to $M1$ and $M2$ and the comparator is latched. Any kickback noise is now completely isolated from the inputs due to the sample and hold process. Instead, the comparator kickback noise is dumped on $C_{IN} + C_R$ at either input and the error is compensated for by the digital redundancy of the pipeline cell. The only error seen at the original inputs, $Vin+$ and $Vin-$, is the clock feed-through from the switches.
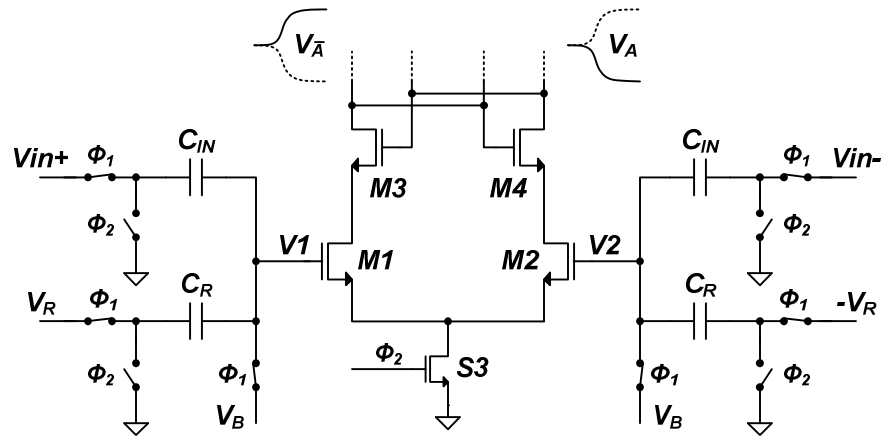
Fig. 76. Kickback noise reduction using a charge redistribution capacitive input circuit.

It is clear that the sampling-based technique is an effective approach to kickback noise cancellation. However, it is not the most economical. First, the capacitor mismatch between C_{IN} and C_R adds directly to the overall mismatch of the comparator, and hence C_{IN} and C_R cannot be overly small to limit offset degradation. Second, the use of sampling capacitors adds significantly to the area once the total number of comparators in the ADC is considered. Finally, the timing sequence used in the sampling-based kickback noise cancellation technique adds indirectly to the power consumption.

To qualify the last statement, consider Fig. 77 of a pipeline cell and its corresponding timing scheme. The settling time of the amplifier is expected to be $t_{s,exp}$ which is equal to the duration of Φ_2. However, since the comparator is latched at the beginning of Φ_2, there is a delay time t_{d1} until the comparators fully regenerate. Next, a digital propagation delay t_{d2} is spent before the proper signal is sent to the MUX. Finally, another delay time t_{d3} is wasted before the proper V_{DAC} value is selected and applied to the amplifier. Therefore, the amplifier ends with only $t_{s,act}$ which can be in the order of

100s of pico seconds less than $t_{s,exp}$. As a result, and to achieve the required settling accuracy in $t_{s,act}$, the amplifiers need to be faster and that can only be achieved by increasing their power budget since the loads are predefined by matching and thermal noise requirements and cannot be reduced.
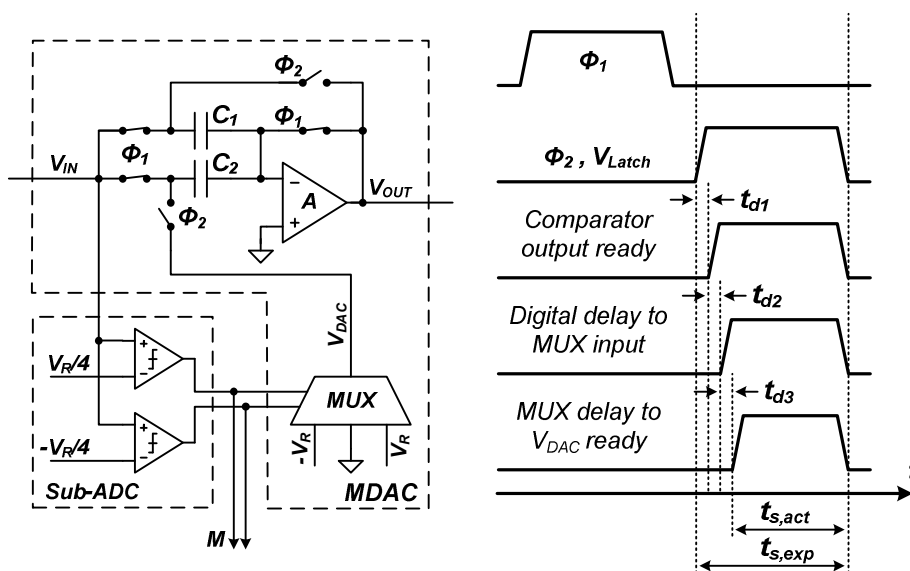
Fig. 77. A pipeline cell and its corresponding timing and delay scheme.

In an effort to reduce the kickback noise of dynamic comparators without excessively compromising the power and area budgets, a replica approach and a different timing scheme are proposed, which are geared towards the differential pair dynamic comparator. First we reexamine the timing scheme as given by Fig. 78 where the main change from Fig. 77 is the separation of V_{Latch} from Φ_2; V_{Latch} now goes HIGH halfway into Φ_1 and LOW synchronous to Φ_1. This separation of V_{Latch} from Φ_2 provides ample time for comparator regeneration, digital delay propagation and selection of the

proper V_{DAC} before is Φ_2 enabled. Thus, the amplifier indeed utilizes all of Φ_2 for settling and an increase in its power consumption for these delays as in the case of the sampling approach is avoided.
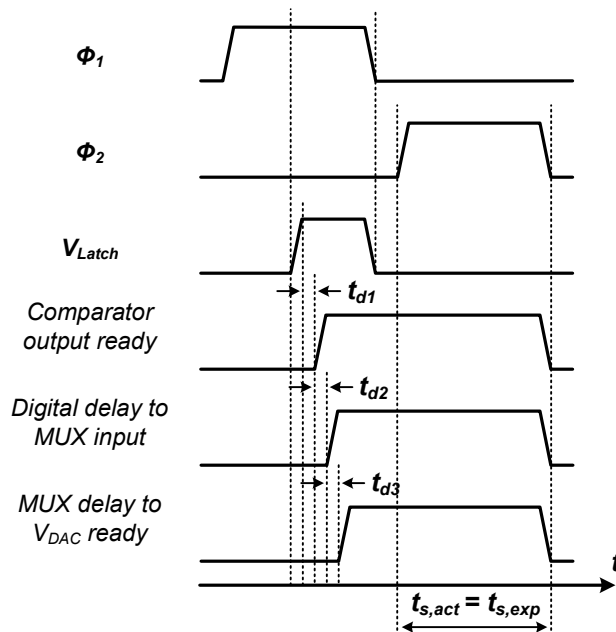
Fig. 78. Proposed timing scheme for kickback noise reduction.

A concern may arise from the timing scheme of Fig. 78 in regard to the comparator being latched before the MDAC of the previous pipeline stage has completely settled at the end of Φ_1. However, since the settling requirement of an MDAC is far stringent than the input requirement of a sub-ADC, latching the comparator halfway through Φ_1 will not result in decision errors. Consider for example the first MDAC in a 1.5bits/stage of a 10bit ADC. The error in the final settling of the MDAC needs to be within 0.05% (½ *LSB* of 9+1 bits), which translates to a minimum of

7.6 time constants. On the other hand, due to the inherent digital redundancy of the sub-ADC and the output being only 2bits, the accuracy of the input to the comparators needs to be within 12.5% (½ *LSB* of 2 bits), which is only 2 time constants. If indeed the comparators are latched halfway into Φ_1, then the MDAC of the previous stage would have settled to within 2.2% (3.8 time constants) and an accurate comparator decision is guaranteed. Moreover, latching the comparators early maximizes the time for the amplifier to naturally recover from kickback noise as discussed at the beginning of section *D*.

In addition to the timing scheme, the proposed approach makes use of a comparator replica to counteract the step seen at the sources of *M1* and *M2* when the comparator is latched. This is demonstrated in Fig. 79 along with the necessary latch signals. The replica is intended to be an exact copy of the comparator, but only sharing the input connections. To generate the replica latch signal V_{Rep}, an inversion of V_{Latch} and Φ_1 are passed through an AND gate. Hence, the comparator and replica are only latched during the duration of Φ_1 to save on power. Neither the rising edge of V_{Rep} nor the falling edge of V_{Latch} is of significance as they occur with the rising and falling edges of Φ_1. The crossing of V_{Rep} and V_{Latch} is where the kickback noise reduction takes place.

The area increase for the replica is disadvantageous but necessary to be able to replicate the dynamics of the kickback noise through *Cgs* of *M1* and *M2*. Moreover, a replica is only needed for the first few pipeline stages. Once the capacitor scaling of stages is ceased and the last pipeline stage is copied down, the resolution becomes rather coarse and the pipeline cells more tolerant to kickback noise, and thus a replica is no

longer necessary. Therefore, the comparator area is not doubled, but perhaps increased by 40% if a replica is no longer used beyond the fourth pipeline stage based on a 1.5bits/stage architecture. Finally, the replica does not provide perfect cancellation as the dynamics of the voltage-dependent capacitors are difficult to match precisely. Nonetheless, together with the timing scheme good results can be achieved.
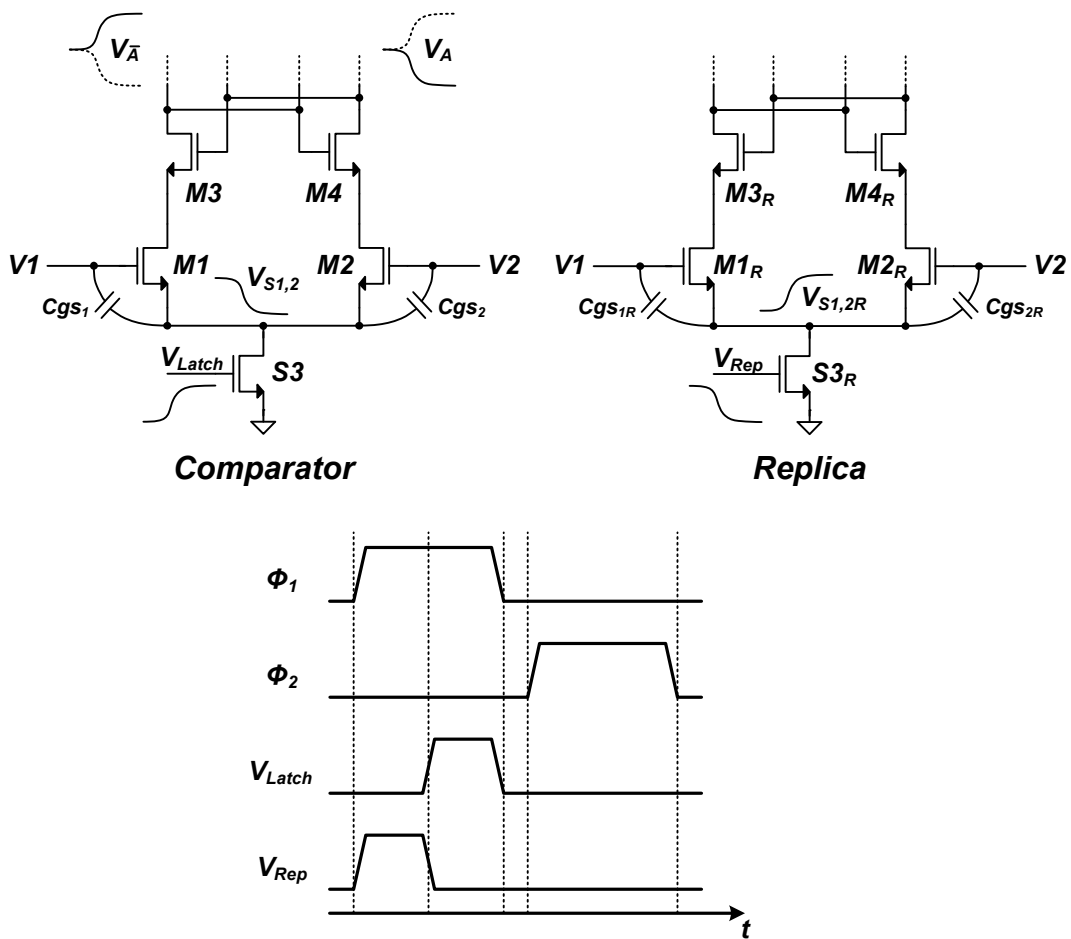
Fig. 79. Proposed kickback noise reduction approach including the core comparator, a replica and the associated timing scheme.

E. Comparator Implementation and Simulation Results

The comparator architecture used in the pipeline ADC is based on the dynamic differential pair input comparator and the proposed kickback noise reduction technique discussed in the previous section. Here the focus is shifted to the implementation of the comparator used in the pipeline ADC of this work and the simulation results.

The comparator presentation thus far was based on single ended input comparators, but in a pipeline ADC all signals are take differential form. To convert the comparator from single to differential input, one need only modify the differential pair as in Fig. 80. Moreover, since the differential input pair operate in saturation when the comparator is latched, the switching threshold of the comparators is adjusted by scaling the dimension of *M1* and *M2* as expressed by (148) [99]-[101].
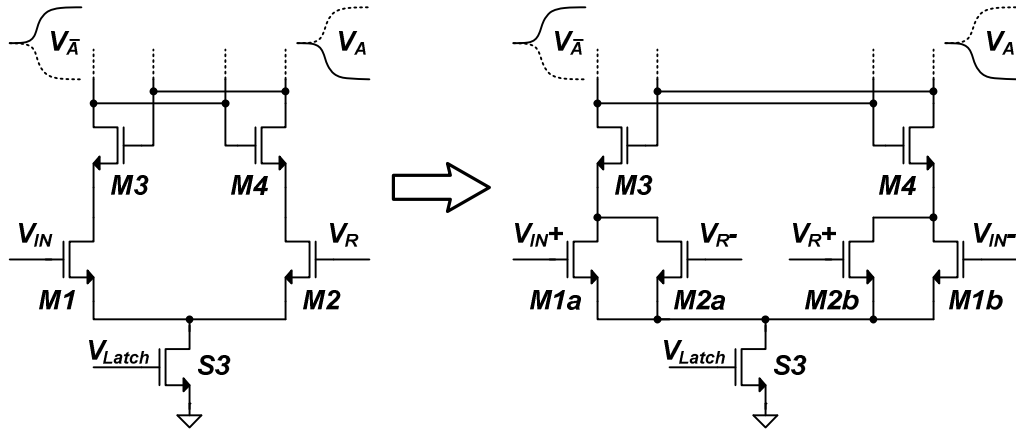
Fig. 80. Transformation of a single-ended input comparator to fully differential.

$$V_{IN}\big|_{Threshold} = V_{IN}^+ - V_{IN}^- = \frac{(W/L)_2}{(W/L)_1}\left(V_R^+ - V_R^-\right) = \frac{(W/L)_2}{(W/L)_1}V_R \tag{148}$$

For the following simulation results, the setup used a model for a first stage MDAC with 90dB DC gain, 1.35GHz *GBW* and total capacitive load of 2.0pF to drive the comparator differentially based on Fig. 71. The MDAC is sampling a 10MHz signal at 200MS/s with a 1Vpp swing. The waveforms in Fig. 81 show the output of the MDAC without a comparator; with a comparator but no kickback noise reduction; and with a comparator and proposed kickback noise reduction.
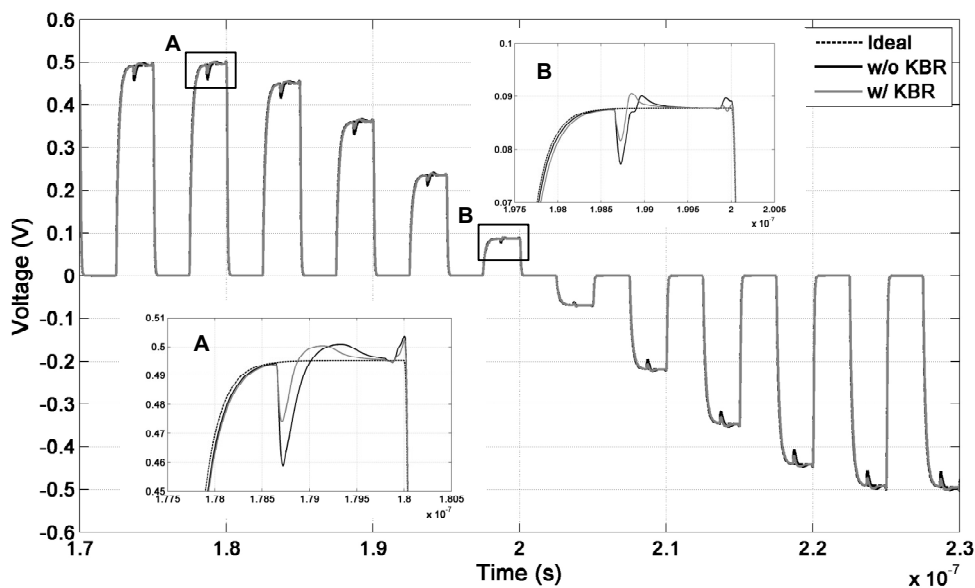
Fig. 81. The effect of kickback noise on MDAC output.

Note how the magnitude of the kickback noise follows that of the input signal due to the voltage-dependent capacitance that dominates the leakage path as previously discussed. This is fairly clear from the enlarged sections where the magnitude of the glitches is larger for larger inputs and vice versa. Also, while the proposed technique

does not fully eliminate the kickback noise as apparent from the presence of glitches, the overall charge injected from the comparator and replica help bring the final settling value closer to the ideal case. In the case of the comparator alone the final value was 715µV greater than the ideal case (0.73 *LSB*), whereas using the proposed kickback noise reduction technique the final value was only 153µV (0.16 *LSB*) away.

As for timing, using the proposed scheme and sampling at 200MHz, the comparator has roughly 1ns to fully regenerate. In Fig. 82, the outputs of the comparator V_A and $V_{\bar{A}}$ are captured along with V_{Latch}. The worst case regeneration time occurs for the smallest input and is typically 380ps, which leaves ample time to account for digital circuitry and MUX delays.
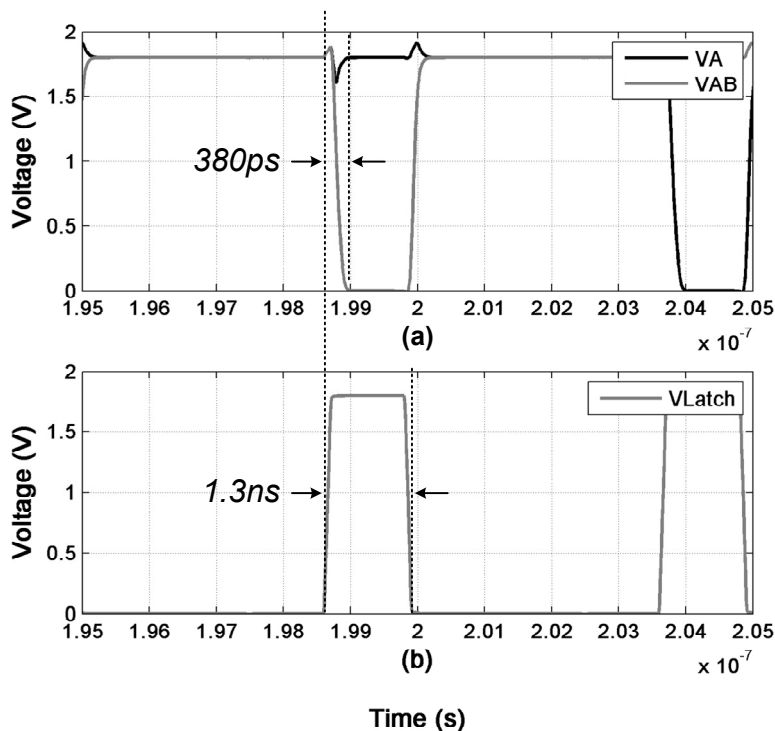
Fig. 82. Comparator regeneration time; (a) outputs V_A and $V_{\bar{A}}$ and (b) V_{Latch}.

Finally, the greatest advantage of the dynamic comparators is their low power consumption, and Fig. 83 shows the total transient current of the comparator including the replica used for kickback noise reduction. Notice how the current transient is characterized with three distinctive spikes per sampling period (5ns), which indicate the shoot-through currents as the comparator and replica latches are activated. These spikes, however, decay quickly as the comparator regenerates. The average power consumption of the comparator including the replica is 120μA, which amounts for a total power of 1.8mA for the whole ADC—approximately 6.9%. This can be further improved if a slight non-overlap is established for V_{Latch} and V_{Rep} to drive the PMOS and NMOS devices separately and minimize shoot-through.
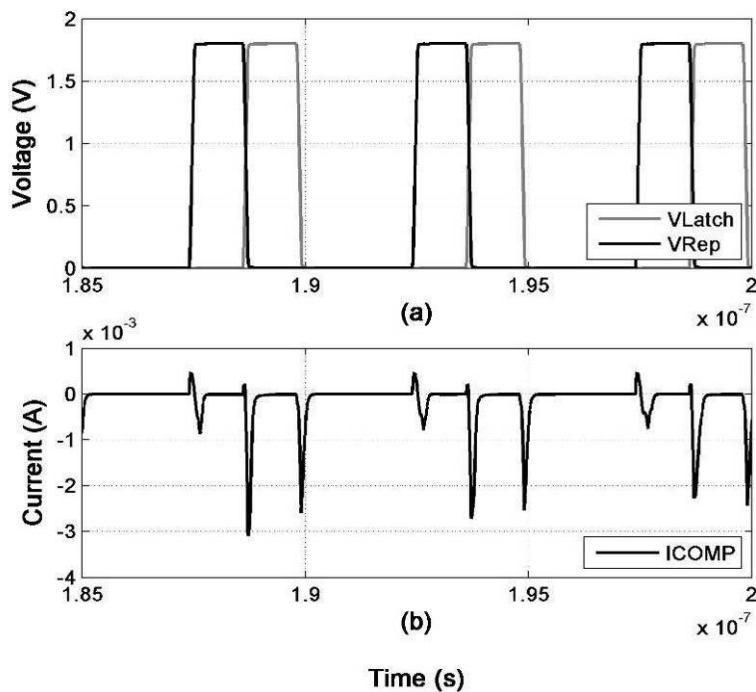
Fig. 83. Comparator and replica total current; (a) control signals V_{Latch} and V_{Rep} and (b) total transient current.

In summary, through a survey of the different comparator types and analysis of kickback noise behavior, a power conscious technique for kickback noise reduction is proposed for dynamic differential pair input comparators. When examined with a true MDAC, the proposed technique proved useful in reducing the error caused by kickback noise such that the settling error is within 0.16 *LSB*. This is achieved through the use of a timing scheme that allows the amplifier to capitalize on its natural kickback noise rejection, and a replica which reduces the kickback noise by superposition of opposite polarity signals. Moreover, the proposed technique is power efficient despite the fact that it relies on a replica approach, as it ensures the maximum allowable settling time for the amplifiers through the elimination of digital circuit and MUX delay intrusions into the HOLD phase of the MDAC.

CHAPTER VIII

SIMULATION AND EXPERIMENTAL RESULTS

The discussion in the preceding chapters demonstrated the direct effects of the amplifier performance on that of the pipeline ADC, and the challenges that come with high speed, low voltage and low power design. For that purpose, a new amplifier topology—the recycling folded cascode—was proposed that effectively addresses many of these limitations.

In this chapter, the simulation and experimental results of the research are presented. First, the conventional folded cascode and the recycling folded cascode are examined. Then, a S/H amplifier suitable for a 1Vpp 10bit Pipeline ADC with up to 200MS/s, which is built on the recycling folded cascode and employing the dual level CMFB is presented. The prototype amplifiers and the S/H were fabricated on the same die using TSMC 0.18µm CMOS technology, and the die was packaged in a QFN40 chip. To facilitate the testing, a PCB was designed to accommodate both test setups, and provide easy access to multiple points in the signal path for verification. Fig. 84 shows the bonded die in the open cavity QFN40 package, and Fig. 85 shows the PCB used in the test. Finally, a complete low voltage, low power, 10bit, 160MS/s pipeline ADC is discussed, highlighting the performance with respect to state-of-the-art present implementations.
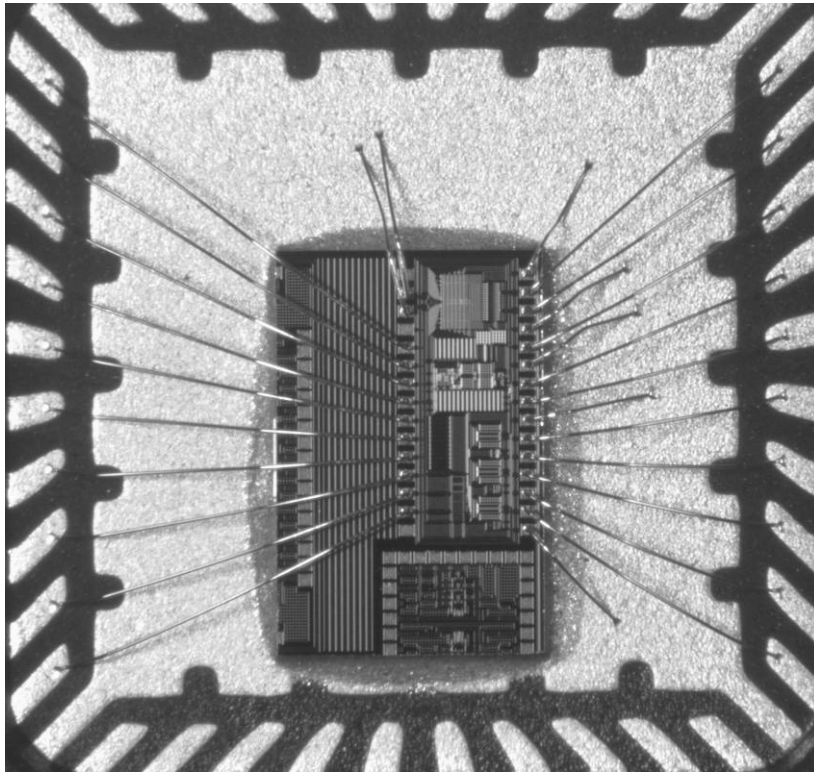
Fig. 84. Amplifiers and S/H prototype chip.
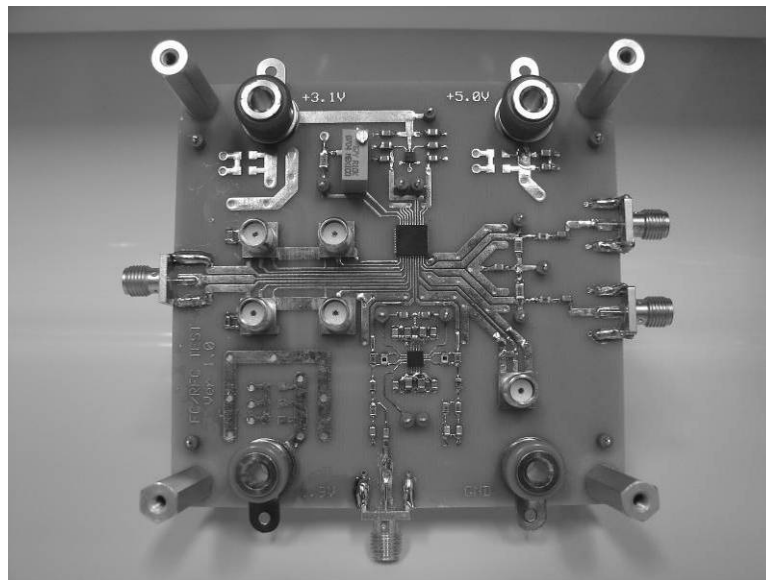
Fig. 85. Prototype chip characterization PCB.

A. Recycling Folded Cascode

The simulation results of the prototype amplifiers were presented in the characterization section of Chapter V. Here we examine the experimental results. The prototype amplifiers, FC, RFC1 and RFC2 were fabricated in a closed loop configuration driving the same on-chip load, and biased with 800µA for the FC and RFC1, and 400µA for RFC2. Fig. 86 shows the amplifiers and their respective loads as they appear on silicon; the FC, RFC1 and RFC2 measure roughly 4700, 5000, and 3000µm^2 respectively. The amplifiers configuration is shown schematically in Fig. 87 with the load and test setup. The internal load $R \| C_1$ and C_2 are 560kΩ\|2.16pF and 2.5pF respectively. As for C_3, it represents the total parasitic capacitance of the output PCB trace and the oscilloscope probe.
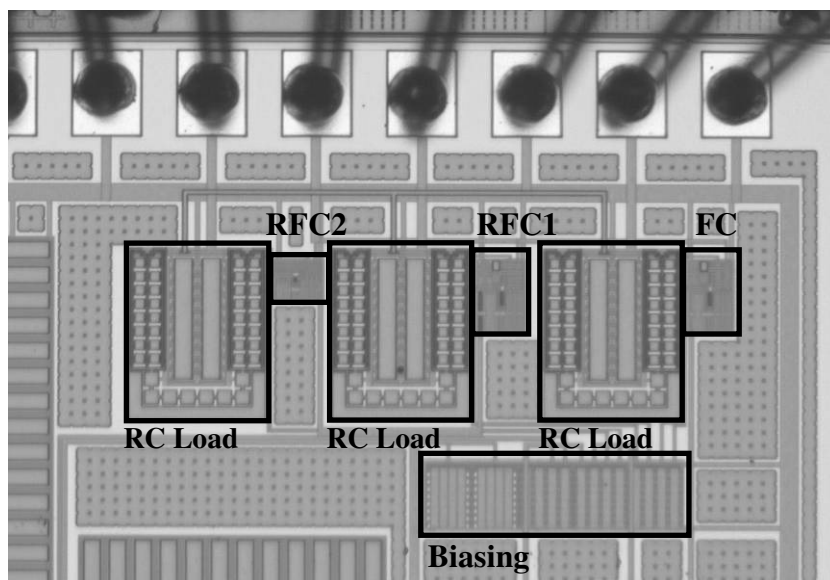
Fig. 86. Enlarged die section showing the FC, RFC1 and RFC2 with their loads.
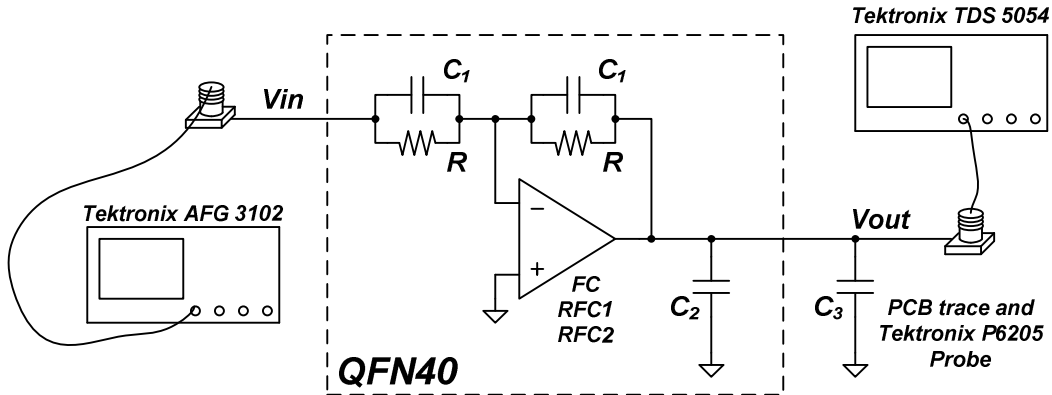
Fig. 87. Amplifier prototype test setup.

The single-ended setup in Fig. 87 is used to simplify the characterization of several metrics, for which the results are presented in the following sub-sections.

1. Gain Bandwidth

The amplifiers are configured in an inverting gain configuration. The closed loop gain expression, A_{CL}, is given by (149), where Z_1 is $R\|C_1$ and $A(s)$ is the amplifier gain as a function of frequency. At $s = jGBW$, the amplifier's gain is unity and the closed loop gain magnitude becomes 1/3. Therefore, the GBW is obtained by simply sweeping the frequency of a signal with known amplitude (500mVpp) and noting the frequency where the gain drops to 1/3 (-9.5dB). The experimental results are given in Fig. 88.

$$A_{CL} = -\frac{Z_1}{2Z_1}\left(\frac{A(s)}{1+\frac{Z_1}{2Z_1}A(s)}\right) = -\left(\frac{A(s)}{2+A(s)}\right) \tag{149}$$
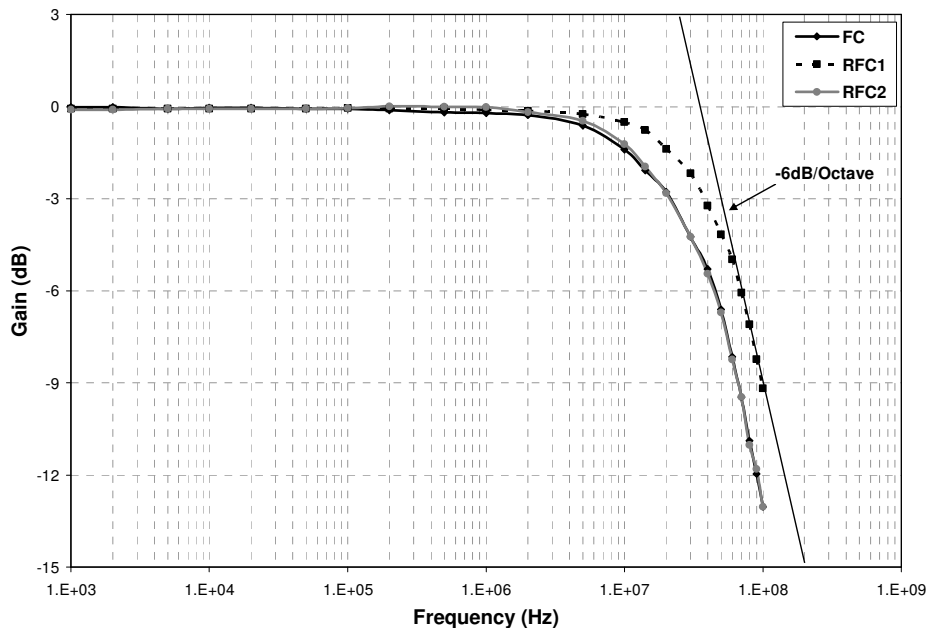
Fig. 88. Experimental frequency sweep of FC, RFC1 and RFC2 amplifier outputs.

The first observation is that the frequency performance of the FC and RFC2 is virtually identical despite RFC2 using only half the area and half the power of the FC. The frequency at which the gain of the FC and RFC2 amplifiers falls to -9.5dB is roughly 70MHz, in disagreement with the simulation results in Chapter V. This is because in the simulations results the parasitic capacitance of the PCB traces and the oscilloscope probes was not taken into account. By accounting for 0.25pF of PCB trace capacitance and 2pF for the Tektronix P6205 active FET probe, the simulated load is increased by 60%, which reduces the simulated *GBW* (115MHz) of the FC and RFC2 to 72MHz, in good agreement with the experimental results. As for the RFC1, the frequency range of the Tektronix AFG 3102 was limited to 100MHz, and hence the response was extrapolated with a -6dB/octave slope as shown in Fig. 88. Through

extrapolation the *GBW* of the RFC1 is found to be 110MHz. However, the GBW of the RFC1 was expected to be twice that of the FC. This discrepancy is the result of the different PCB trace capacitance seen by RFC1. Fig. 89 is a closer look at the PCB traces associated with each amplifier and their differences. Given the width of the traces and thickness of the PCB, the trace capacitance for the FC, RFC1 and RFC2 can be calculated to be 0.18pF, 1.39pF and 0.24pF respectively. In addition to the 2pF input capacitance of the Tektronix P6205 active FET probe, the overall capacitive load seen by the FC, RFC1 and RFC2 is 5.76pF, 6.97pF and 5.82pF respectively. The difference in trace capacitance for the FC and RFC2 is negligible when compared to the overall load (~1%). However, the trace capacitance for the RFC1 increases the overall load by 21%. When this is taken into account and by normalizing the *GBW* with respect to the FC capacitive load, the *GBW* of the RFC1 becomes 133.1MHz, almost twice (1.9 times) the *GBW* of the FC.
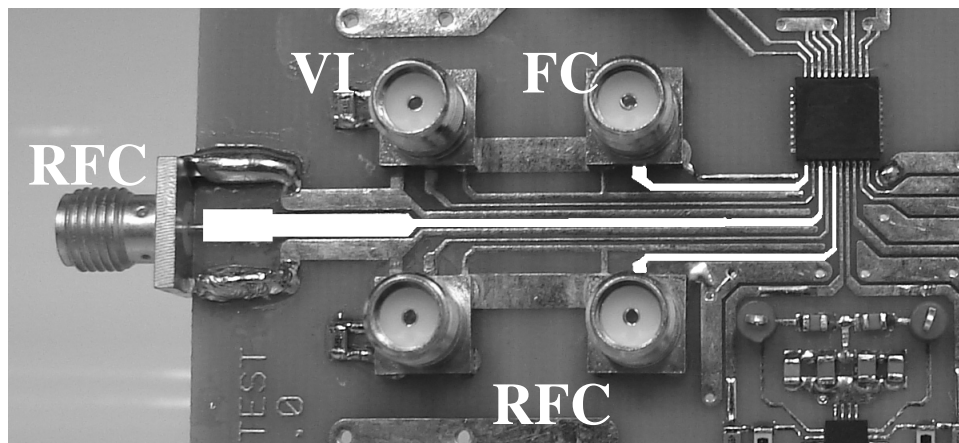
Fig. 89. PCB trace differences for the FC, RFC1 and RFC2 amplifiers.

An alternative way to measure the GBW is by applying a small step signal and measuring the settling time. Fig. 90 shows the step response of the prototype amplifiers to a 10MHz, 100mVpp step signal. The amplitude of 100mVpp ensures that the amplifiers will not slew as predicted by (28). The FC and RFC2 traces are closely overlapped indicating similar *GBW*, while the RFC1 clearly demonstrates a higher *GBW*. The settling time of the FC, RFC1 and RFC2 to an accuracy of 1% is 20.7ns, 13.2ns and 20.8ns respectively. This translates to a GBW of 70.7MHz for the FC, 110.9MHz for RFC1 and 70.4MHz for RFC2, in good agreement with the frequency sweep results.
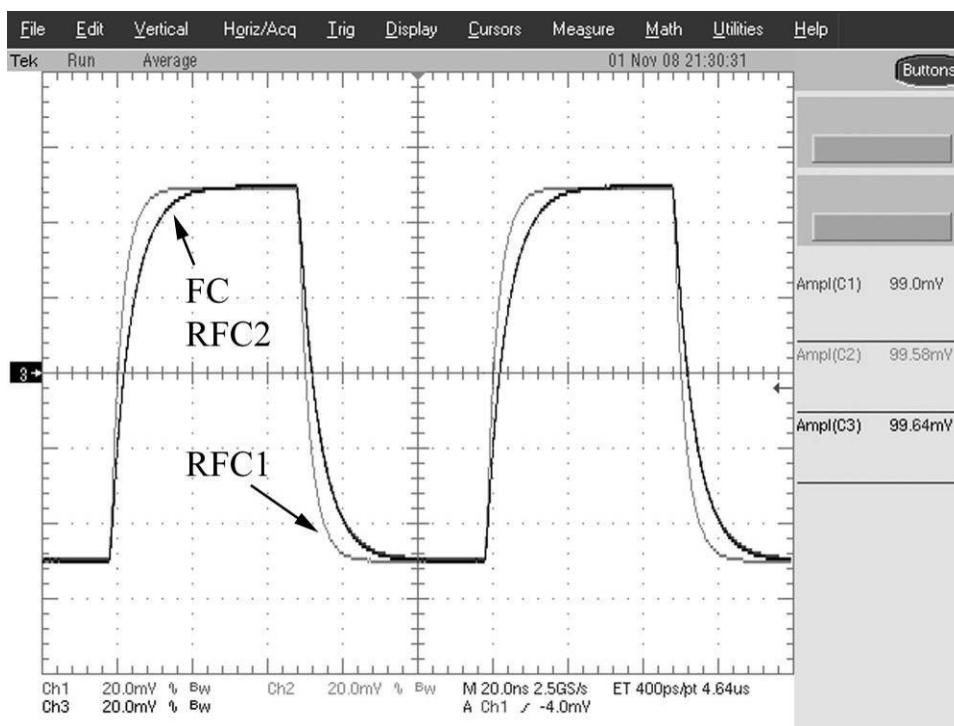
Fig. 90. Small signal step response of the FC, RFC1 and RFC2 amplifiers.

2. *Slew Rate*

The amplifiers are forced to slew if the input is greater than the maximum described by (28), which is roughly 200mV. The output response of the FC, RFC1 and RFC2 amplifiers to a 5MHz, 1Vpp input step is shown in Fig. 91. From Fig. 91, the RFC1 has a clearly improved *SR* over the FC despite the same bias current. Moreover, at half the bias current, the *SR* of the RFC2 is slightly better than the FC. The average *SR* of the FC, RFC1 and RFC2 normalized to the FC total capacitive load is 42.15V/µs, 94.13V/µs and 48.12V/µs respectively; that is the *SR* of the RFC1 is enhanced 2.23 times over the FC for the same bias current, while that of the RFC2 is enhanced 1.14 times over the FC for half the bias current.
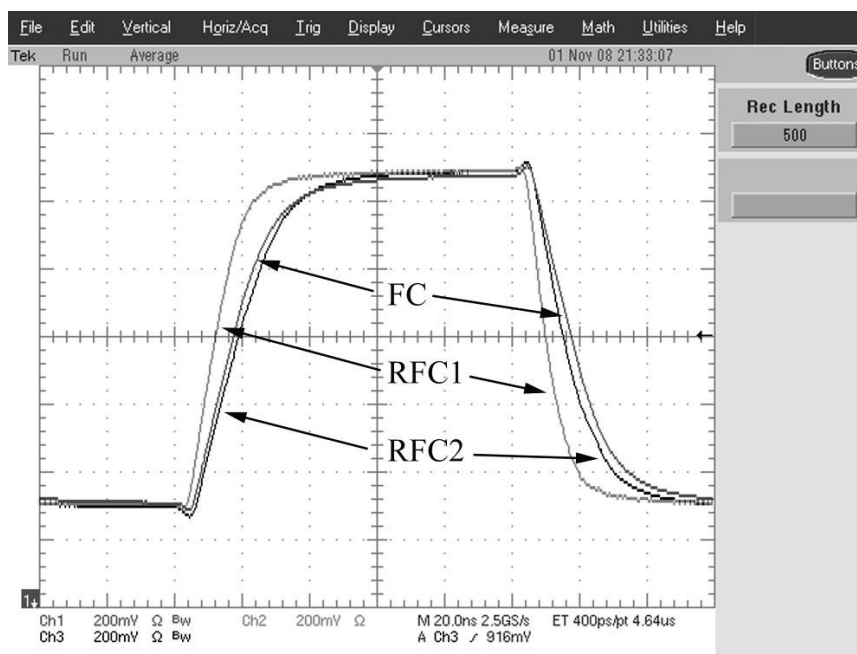
Fig. 91. Large signal step response of the FC, RFC1 and RFC2 amplifiers.

3. Distortion

The linearity of the amplifiers can be measured through their distortion behavior. A 1Vpp two tone test centered at 1MHz and separated by 100kHz (500mVpp at 0.95MHz and 500mVpp at 1.05MHz) was applied to all amplifiers and the FFT data of the outputs was captured using the Tektronix TDS 5054 and plotted in MATLAB. The results for the FC, RFC1 and RFC2 are given in Fig. 92. The third intermodulation distortion, *IM3*, is -61.7dB for the FC, -66.1dB for RFC1 and -61.6dB for RFC2.

In Chapter IV the amplifier slew rate effects were considered for step inputs. For continuous signals, the *SR* can indicate the maximum input frequency as given by (150), where the output voltage is a time-varying signal $A_m cos(2\pi f_{in}t)$, with amplitude A_m and frequency f_{in}. According to (150) and the average *SR* results presented earlier, the FC, RFC1 and RFC2 amplifiers can support signals up to 13.4MHz, 29.9MHz and 15.3MHz respectively without slewing.

$$SR \geq \frac{\partial Vout}{\partial t} = 2\pi f_{in} A_m \sin(2\pi f_{in}t)\big|_{\max} \quad \Rightarrow \quad f_{in} \leq \frac{SR}{2\pi A_m} \qquad (150)$$

Therefore, the distortion is solely due to the reduced amplifier gain around 1MHz. The FC and RFC2 have almost identical *GBWs* and hence it is not surprising to see them have similar IM3 performance, as they have the same voltage gain around 1MHz. The RFC1, on the other hand has a wider *GBW* and hence a higher gain around 1MHz, which explains the improved IM3 performance. According to the absolute *GBW*

results, the open loop gain at 1MHz of the FC and RFC2 amplifiers is 36.6dB and the gain of the RFC1 amplifier is 40.8dB. The difference in gains is in good agreement with the difference in *IM3* performance for the FC, RFC1 and RFC2.

4. Summary

The overall summary of the FC, RFC1 and RFC2 performance is presented in Table 5. Overall, if one intends to better utilize the power, RFC1 proved to be a more efficient amplifier. It provides a higher gain, almost twice the *GBW*, better than twice the average *SR*, a better *IM3* and a lower noise and offset—all while utilizing the same power and virtually the same silicon area. On the other hand, for half the power and almost half the area, the same performance of the FC can be replicated using RFC2, on the expense of an increase in noise and input offset.
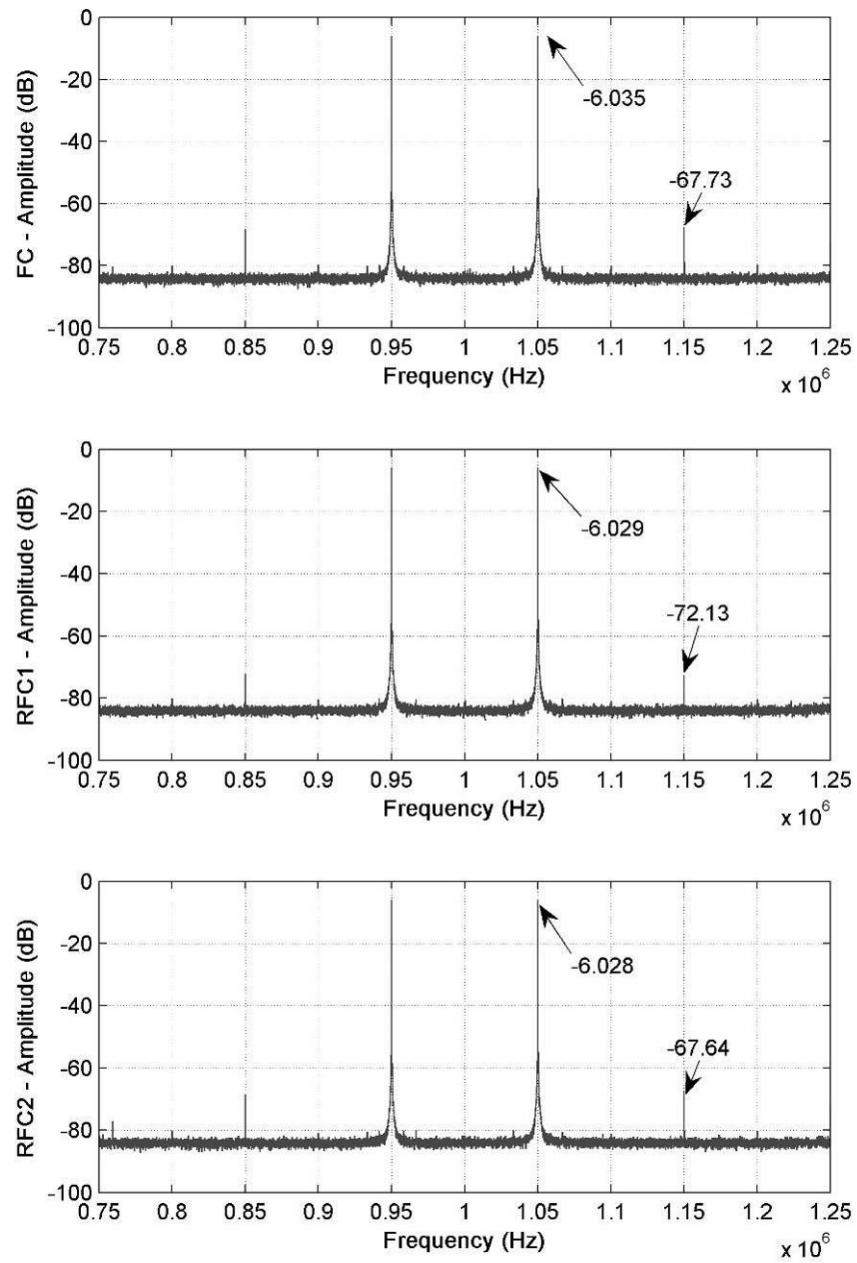
Fig. 92. Two tone FFT spectrums of the FC, RFC1 and RFC2 for a 1Vpp signal centered at 1MHz and separated by 100kHz.

TABLE 5
SIMULATION AND EXPERIMENTAL RESULTS PERFORMANCE SUMMARY OF THE FC, RFC1
AND RFC2 AMPLIFIERS

Parameter	FC	RFC1	RFC2
Power (µA)	800	800	400
Area (µm^2)	4712.9 (53.8 x 87.6)	4958.2 (56.6 x 87.6)	3001.8 (58.4 x 51.4)
GBW (MHz)	70.7	110.9 (134.2*)	70.4
Load C_L (pF)	5.76	6.97	5.82
DC Gain (dB)	46.02 (52.63**)	53.56 (60.91**)	54.89 (59.32**)
SR+ (V/µs)	42.75	65.13 (78.81*)	41.09
SR- (V/µs)	41.55	90.45 (109.44*)	55.14
Average SR (V/µs)	42.15	77.79 (94.13*)	48.12
IM3—1Vpp input at 1MHz (dB)	-61.7	-66.1	-61.6
Input integrated noise (µVrms) (1Hz – 100MHz)**	53.16	48.48	69.71
Input offset – 3σ (mV)**	7.92	7.64	11.08
Settling Time – 1% (ns)	20.7	13.2 (10.91*)	20.8

* Normalized to the FC capacitive load
** Simulation results

B. Sample and Hold

The front end of a pipeline ADC is the S/H amplifier. A flip-around S/H architecture was designed for a 10 bit 1Vpp pipeline ADC and fabricated in TSMC 0.18µm CMOS technology as an application of the recycling folded cascode. The S/H also utilized the low voltage two-stage gain boosting technique discussed in Chapter IV and the dual level CMFB discussed in Chapter VI. An enlarged section of the die where the S/H amplifier is placed is shown in Fig. 93, where C_{SH} and C_C are the sample and hold and coupling capacitors respectively.
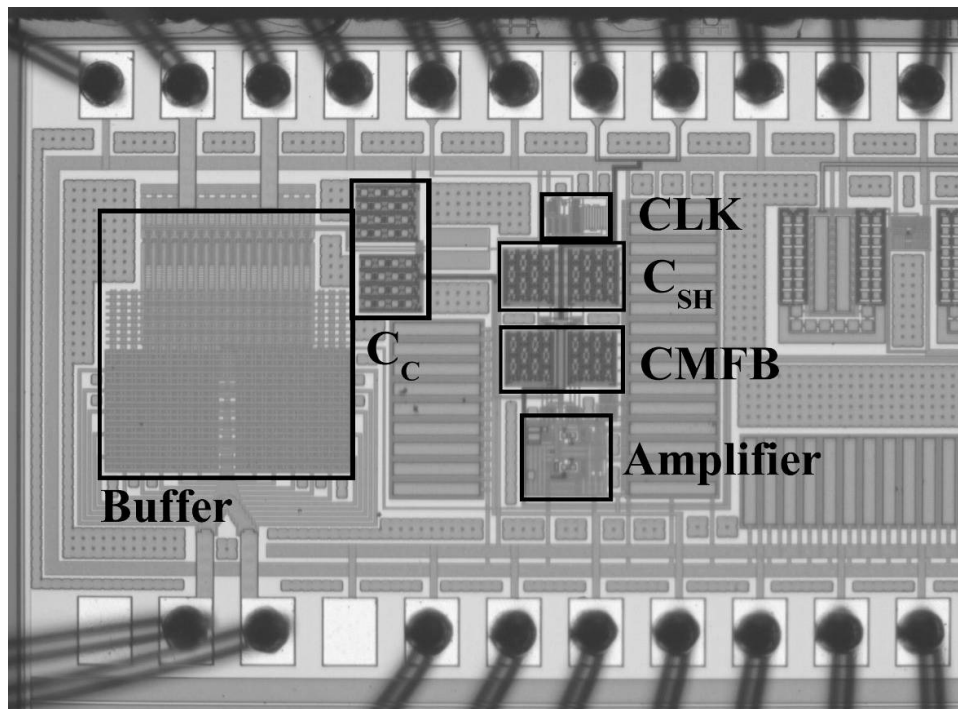
Fig. 93. Enlarged die section showing the S/H amplifier and open drain buffer.

Fig. 94. S/H test setup.

The test setup used to characterize the S/H is given in Fig. 94, showing all components and their values. As the testing is done at high frequencies, careful choice of components was necessary to improve impedance matching between the equipment used and the PCB. The single-ended input signal was converted to fully differential using the THS4513 wideband low distortion fully differential amplifier. Also, the THS4513 configuration acts as an anti-aliasing filter, with a corner frequency of 96.5MHz. The clock phases necessary for operation were generated on chip using a self-biased amplifier [103] and the logic shown in Fig. 95, which in simulations guaranteed a 50% duty cycle $\pm 2\%$ for different corners and temperatures up to a *CLK* input of 250MHz in a 1.8V domain. The switches were implemented using NMOS low V_T devices, which eliminated the use of bootstrapping techniques. The *CLK* input was provided by either a pure sinusoidal waveform from the Tektronix AFG 3102 up to 100MHz, or the HP 81110A pulse/pattern generator up to 200MHz.

Fig. 95. On-chip generation of S/H clock phases.

In practice the S/H will drive the input of the first pipeline stage, which is a small capacitive load compared to the bondpad and equipment input parasitics. Therefore, to facilitate the testing, a highly linear open drain buffer was designed to support the drive capability. However, as the S/H and the output buffer operate from different supply domains, AC coupling was necessary. Overall, the total capacitance seen at the output of the S/H is 2 pF. Assuming all-linear settling, a *GBW* of 700MHz is necessary for the S/H amplifier to settle to 10 bit accuracy at 200MS/s. However, taking into account that slewing is inevitable, the S/H was designed with *GBW* of 0.935GHz and more than 60° of phase margin. The simulated AC response is given in Fig. 96.
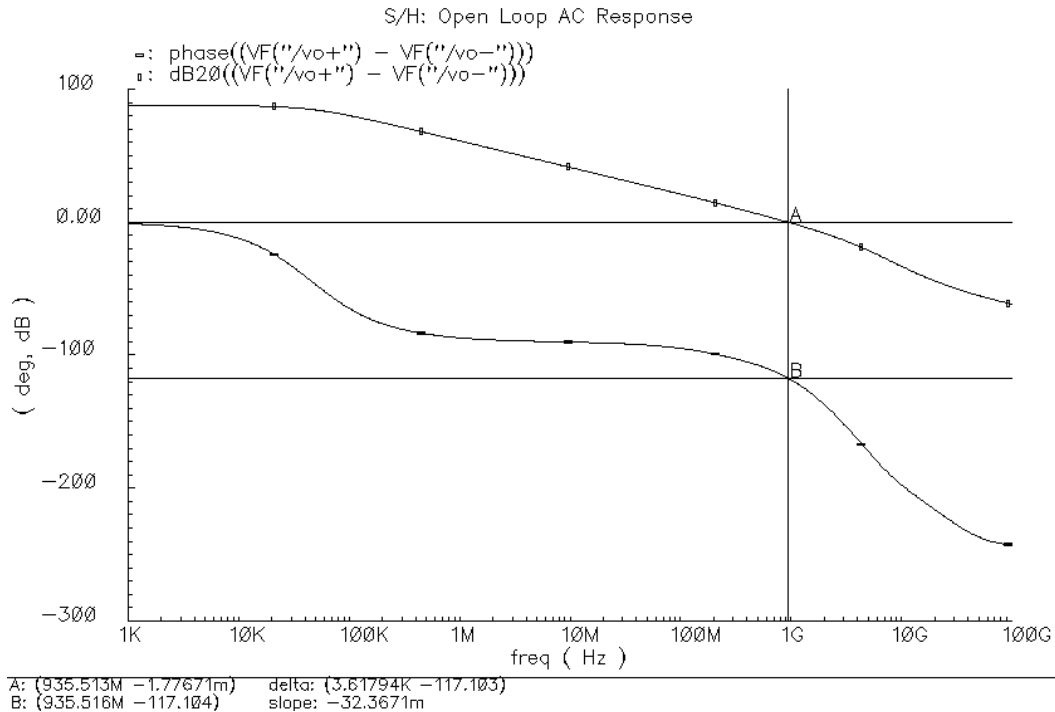
Fig. 96. S/H amplifier AC response.

To verify functionality, the S/H amplifier was first tested at a 100MS/s for various input frequencies up to and beyond the Nyquist rate. For this purpose the Tektronix AFG 3102 dual signal generator was used. This simplified the capture of the signals on the Tektronix TDS 5054 as both signals come from the same source. Figs. 97, 98 and 99, show trace captures on the Tektronix TDS 5054 for an input of 5MHz, 50MHz and 75MHz respectively.
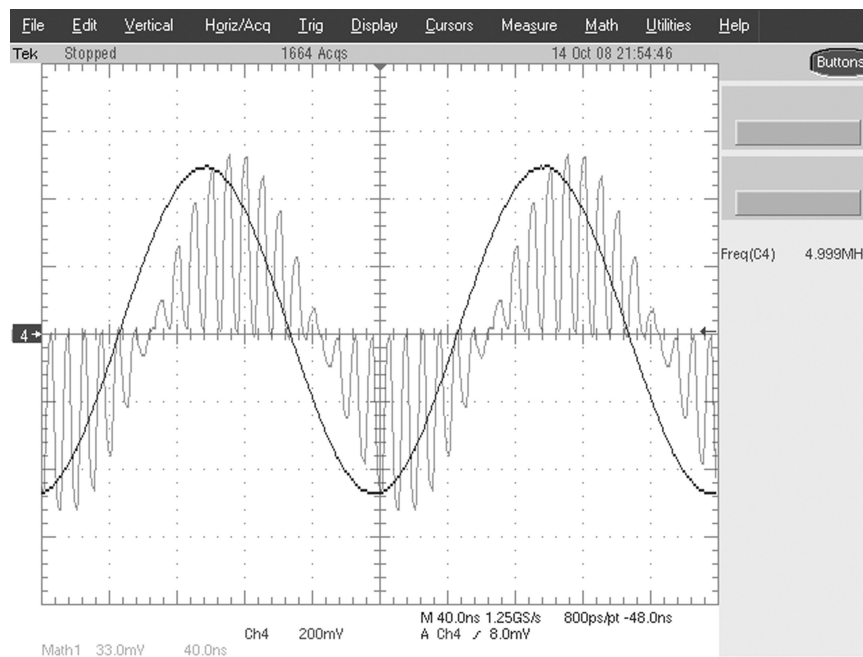
Fig. 97. 5MHz input and S/H output at 100MS/s.
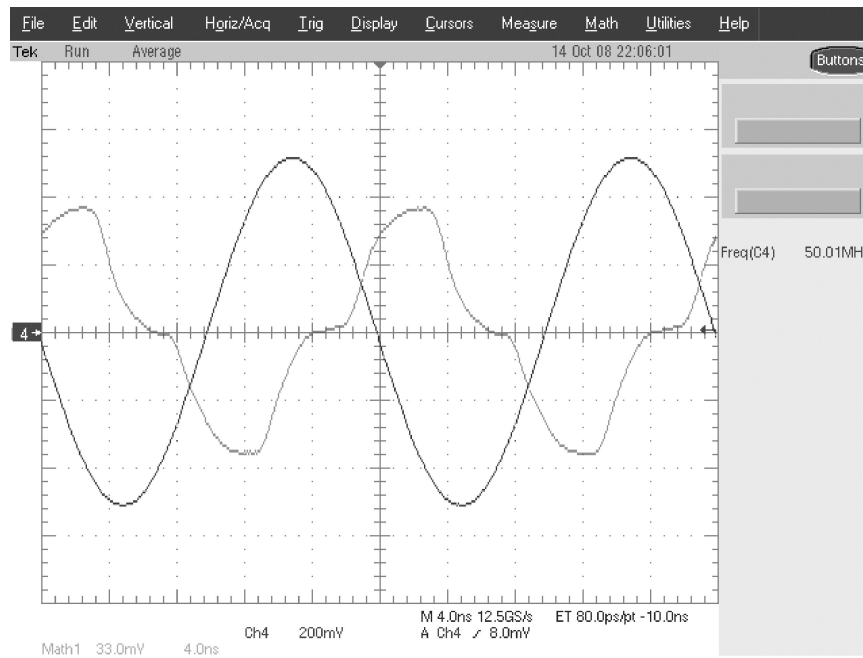
Fig. 98. 50MHz input and S/H output at 100MS/s.
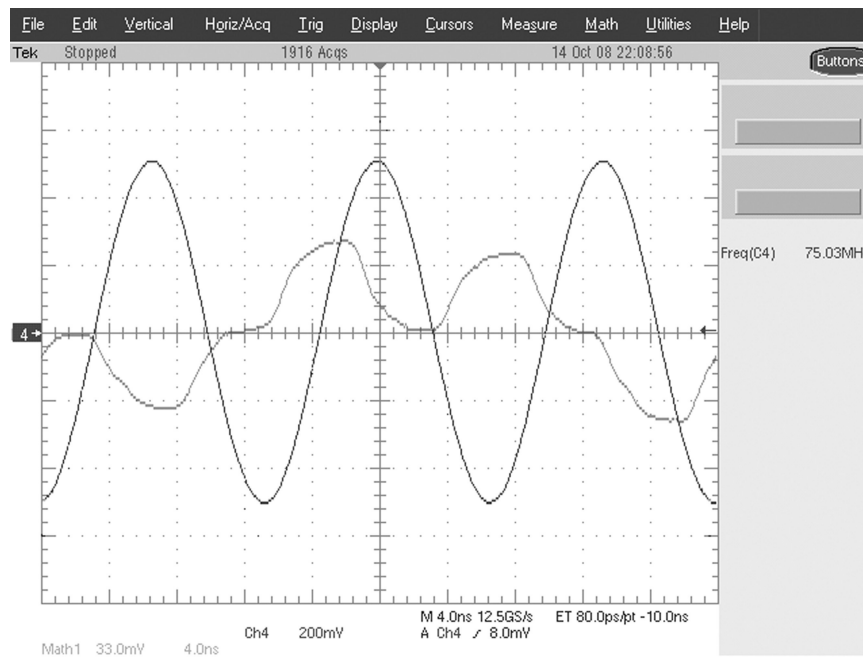
Fig. 99. 75MHz input and S/H output at 100MS/s.

The results shown in Figs. 97-99 confirm functionality of the S/H amplifier. More specifically, the functionality of the low voltage gain boosting, the dual level CMFB and the use of low V_T devices as switched are verified. One note, however, is the attenuated output level with respect to the input signal. By examining the signal path from the Tektronix AFG 3102 to the Tektronix TDS 5054, the THS4513 configuration contributes an attenuation of 0.95, the internal coupling an attenuation of 0.5, the output buffer an attenuation of 0.92 and finally the output matching network with an attenuation of 0.375. This results in a total attenuation of 0.164, which is in good agreement with the results seen in Figs. 97-99.

To step up the sampling frequency to 200MS/s, the HP 81110A pulse/pattern generator was used for *CLK*. For this test, the FFT function of the Tektronix TDS 5054 was used to capture the output data of the S/H amplifier and processed in MATLAB to generate the plots. A single tone test was first performed near the Nyquist sampling limit using a 90MHz full scale (1Vpp) input. The results are shown in Fig. 100. The spectrum of the S/H amplifier shows an *HD3* of 57.32dB. As the spectrum is clear of any other spurs, the *SFDR* is also 57.32dB. As for the *SNR*, the noise floor seen in Fig. 100 is dominated by the noise of the equipment used and the output buffer. Nonetheless, assuming a 10bit noise floor, the *ENOB* can be calculated to give 9.03 bits. As for Fig. 101 and 102, they show the results of a two tone test with tones of 500mVpp each centered at 90MHz and separated by 100kHz. The spectrum is clear of any spurs, apart from the intermodulation distortion seen in Fig. 102, yielding an *IM3* of 51.34dB.
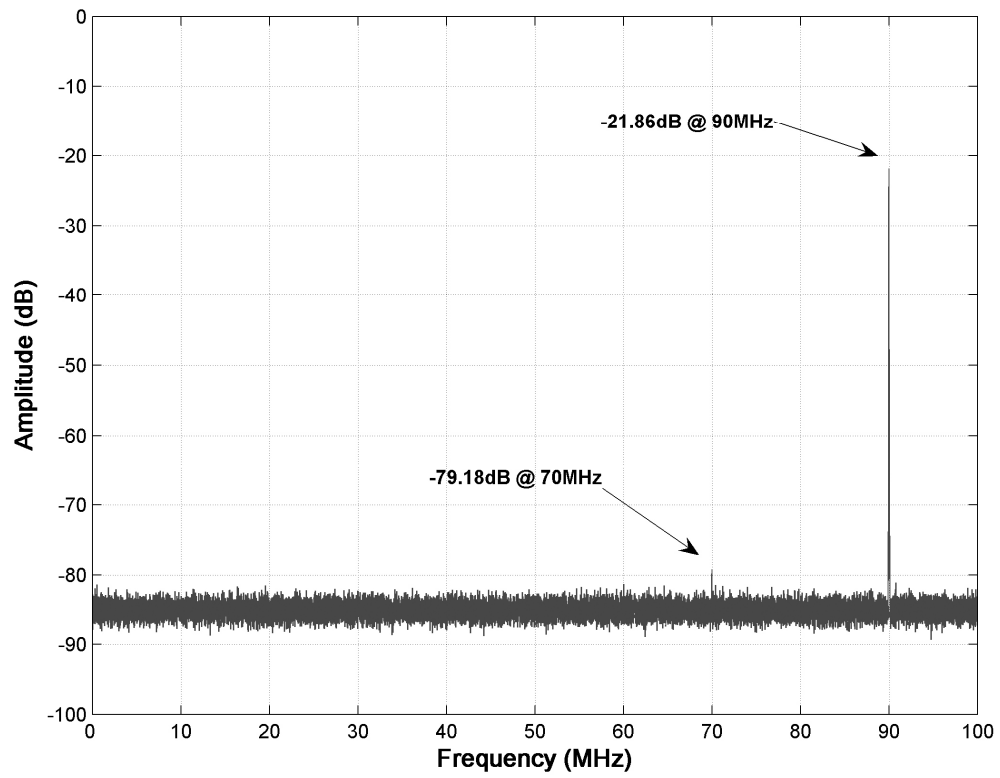
Fig. 100. S/H output spectrum for a 1Vpp, 90MHz input sampled at 200MHz.
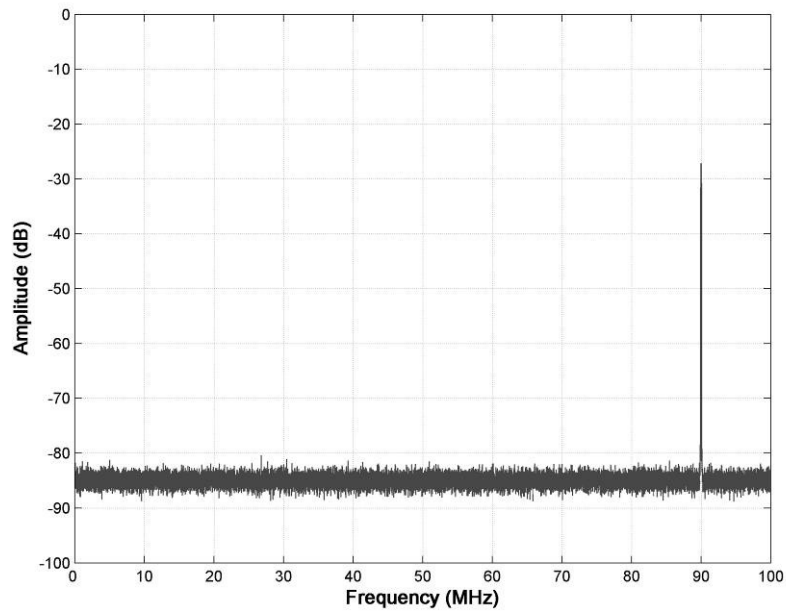
Fig. 101. S/H output spectrum for a 2 tone 1Vpp input centered at 90MHz and separated by 100kHz, sampled at 200MHz.
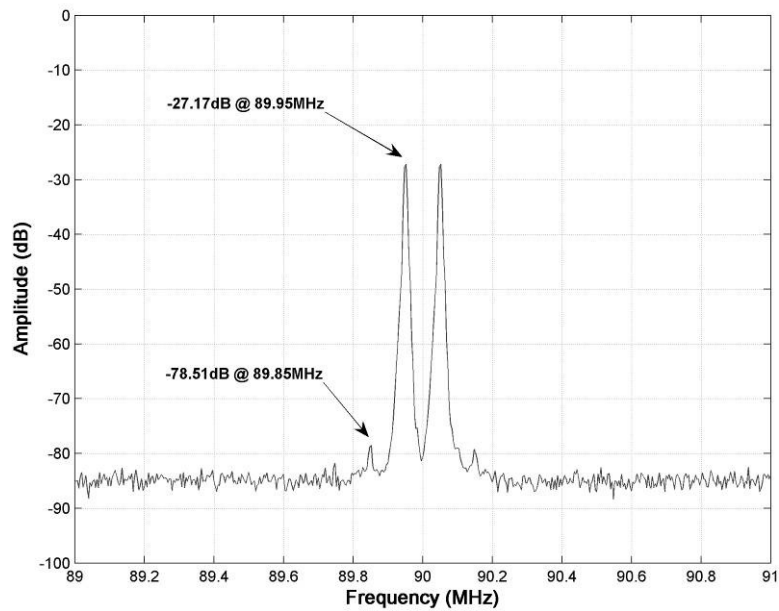
Fig. 102. Expanded spectrum of Fig. 101.

C. Pipeline ADC

A 10bit, 1Vpp, 160MS/s pipeline ADC was designed using the techniques presented in the previous chapters, and laid-out using SMIC 0.18µm CMOS technology. The general architecture of the pipeline ADC and layout of the whole chip are presented in Fig. 103 and Fig. 104 respectively. The individual building blocks in Fig. 103 are based on those discussed in Chapter III, using the gain boosted RFC amplifier with dual level CMFB and dynamic comparators with kickback noise reduction where applicable. Grey and white blocks operate from 1.2V and 1.8V supplies respectively.
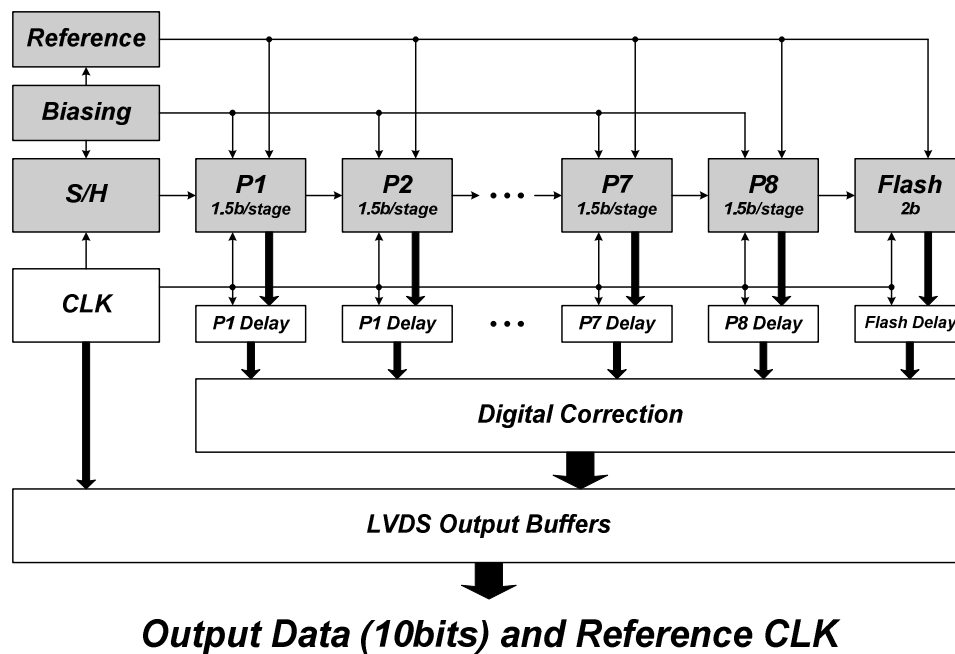
Fig. 103. Block diagram of pipeline ADC designed in SMIC 0.18µm CMOS technology.
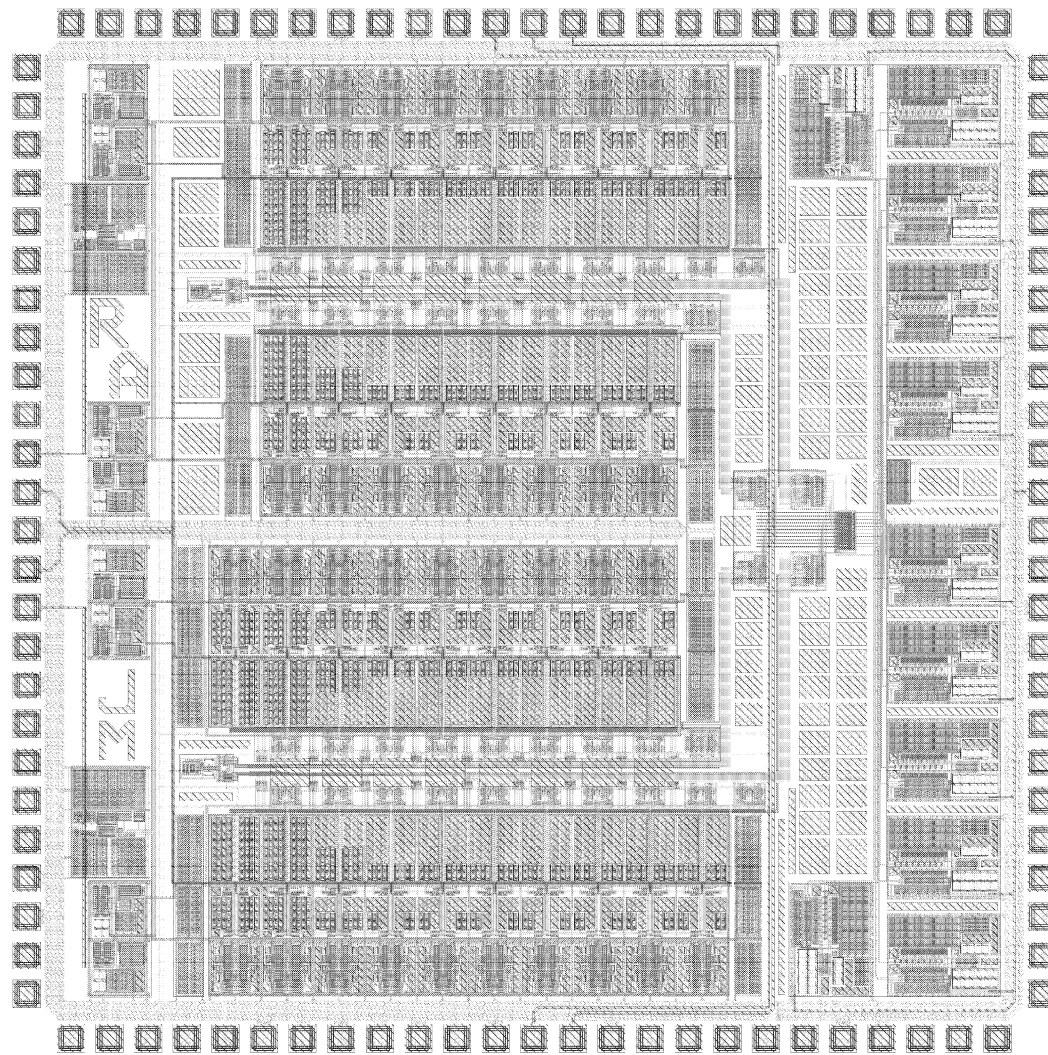
Fig. 104. Complete pipeline ADC layout in SMIC 0. 18µm measuring 4x4mm^2 and featuring 4 separate ADCs multiplexed to the LVDS output drivers.

The most challenging block in the pipeline ADC is the amplifier used to implement the MDAC of the first pipeline stage. It needs to settle within 0.1% (10bit accuracy) in less than 2.8ns for 160MS/s at full scale input (1Vpp). For that purpose, a 1.45GHz bandwidth amplifier is designed with 55° of phase margin and Fig. 105 shows its AC response. To demonstrate functionality of the internal blocks, a small input is applied to the ADC and the output of the S/H, P1 and P2 stages are plotted in Fig. 106. This shows the multiply by 2 function of the pipeline cells and the capability to handle a 1Vpp swing.
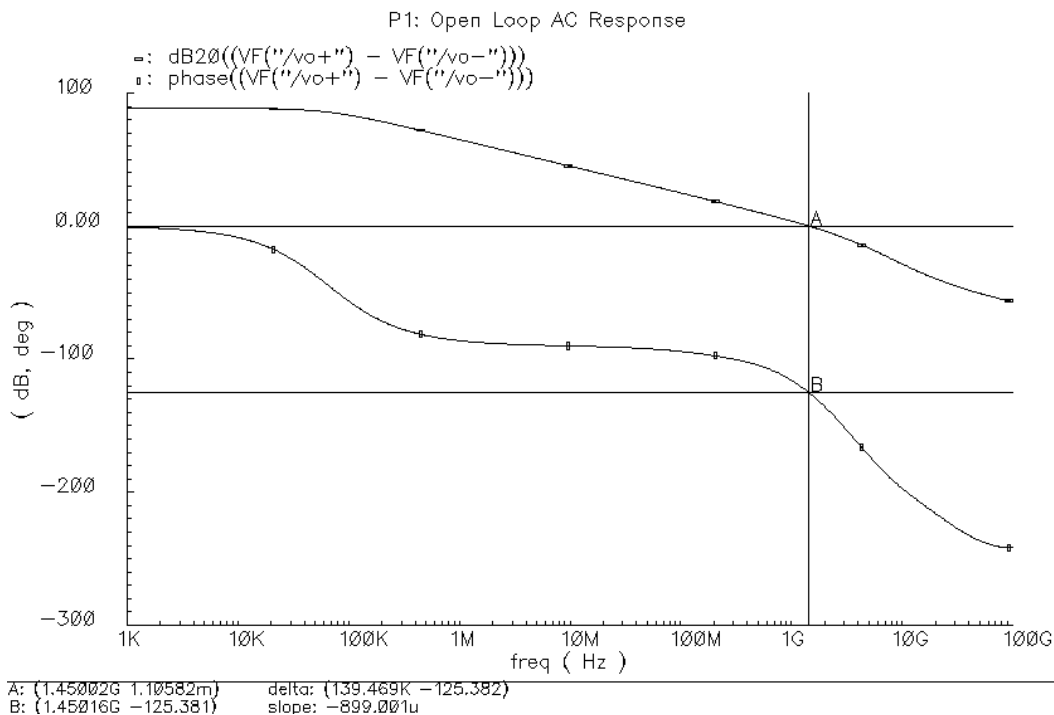
Fig. 105. First pipeline stage amplifier AC response.
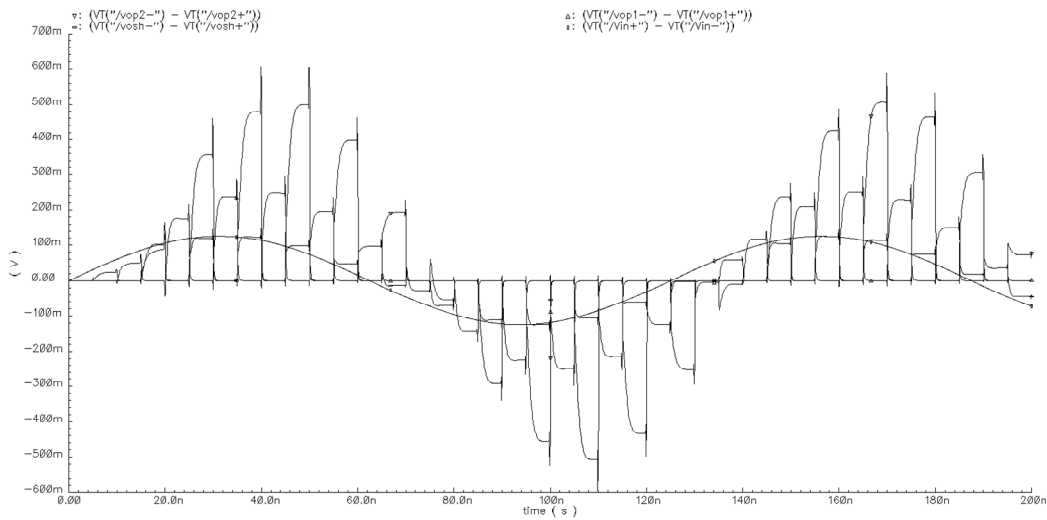
Fig. 106. Transient simulation of pipeline ADC showing the input signal and outputs of the S/H, P1 and P2 blocks.

Sampling at 160MS/s, a *FS* single tone near the Nyquist sample rate at 78MHz was applied as an input to the pipeline ADC. The FFT plot is given in Fig. 107. The only visible spur is that of the third harmonic, and the *HD3* is 62.46dB. Also from Fig. 107, the calculated *SNDR* is 57.12 which translates to an *ENOB* of 9.19. A figure of merit (*FoM₁*) used to measure the efficiency of an ADC is described by (151), which links the ADC power *P* to the resolution *ENOB* and sampling frequency f_S. The efficiency is quantified as pJ/conversion-step. However, to incorporate the added speed advantage of newer CMOS technologies over older ones in the comparison, a modified version of (151) given in (152) can be used. In (152), the transit frequency $f_{T,other}$ of other CMOS implementations is normalized to that of the device under test, $f_{T,DUT}$. Thus, the resulting *FoM₂* is more design based than technology based.
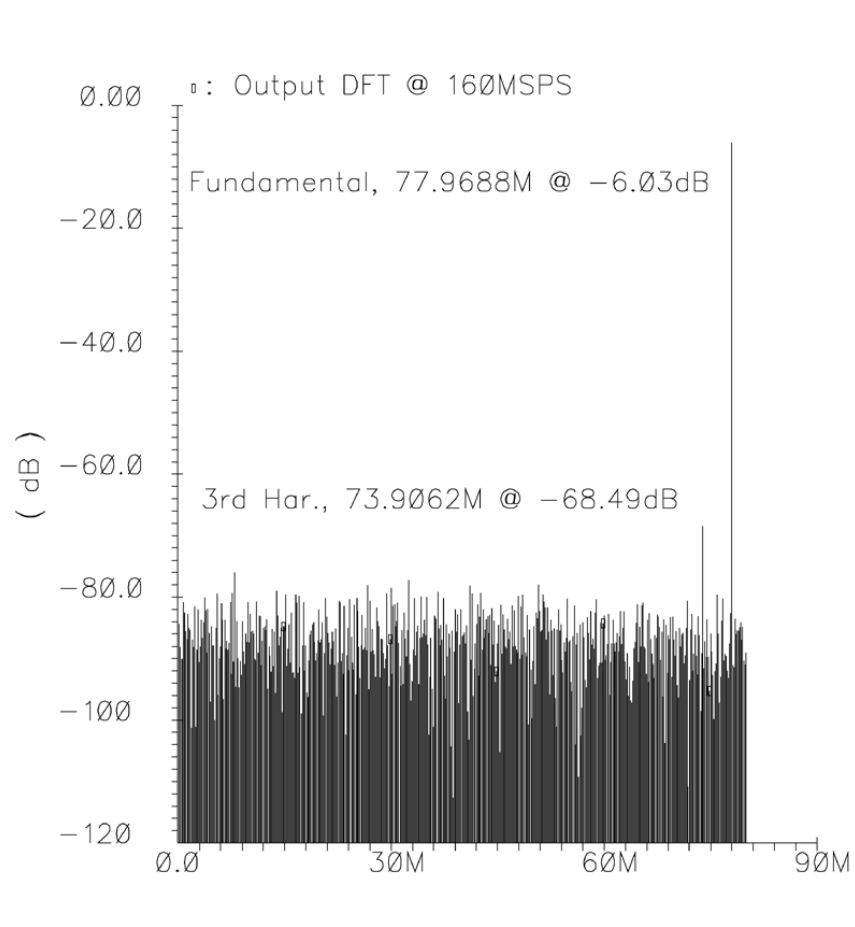
Fig. 107. 1k FFT ADC spectrum for f_{IN} = 78MHz at 160MS/s.

$$FoM_1 = \frac{P}{2^{ENOB} f_S} \qquad (151)$$

$$FoM_2 = \frac{P}{2^{ENOB} f_S} \cdot \frac{f_{T,Other}}{f_{T,DUT}} \qquad (152)$$

A comparison of the pipeline ADC presented here with recent state-of-the-art implementations of comparable resolution in literature is summarized in Table 6.

TABLE 6
PERFORMANCE SUMMARY OF RECENT STATE-OF-THE-ART PIPELINE ADCS

Parameter	[13]	[15]	[16]	[19]	[23]	[26]	This Work*
CMOS Technology	0.18/0.35 μm	90nm	130nm	130nm	0.18/0.35 μm	90nm	0.18 μm
Resolution	10bits	10bits	10bits	10bits	10bits	10bits	10bits
f_S [MHz]	170	200	400	100	210	205	160
Supply [V]	3.3	1.2	1.2	3	1.8	1.2	1.2
Vin [Vpp]	2	0.8	1.2	2	1.5	1	1
Power [mW]	180	55	160	72	140	**40**	42
Area [mm^2]	0.85	1.26	4.2	**0.54**	1.5	1	1.1
$SNDR$ [dB]	57.8	53.6	53.7	56.3	**59.3**	53.9	57.12
$SFDR$ [dBc]	70.3	66.5	60.9	67.5	**85.9**	61.8	62.46
$ENOB$	9.31	8.61	8.63	9.06	**9.56**	8.66	9.19
FoM_1 [pJ/Conv-Step]	1.67	0.71	1.01	1.35	0.88	0.48	**0.45**
FoM_2 [pJ/Conv-Step]	1.67	1.97	1.82	2.43	0.88	1.35	**0.45**

* Simulation Results

From Table 6, the pipeline ADC presented in this work demonstrates the highest potential efficiency. Considering the technology of implementation, the presented work is twice as efficient as a similar 0.18µm CMOS implementation, but using 27% smaller area. The presented work also shows a slightly better efficiency than similar 90nm CMOS implementations with only 10% increase in area.

CHAPTER IX

CONCLUSIONS

The pipeline ADC is a popular architecture that finds use in a wide range of applications with resolutions up to 14bits and +100MHz sampling speeds. The current approach to its design puts a lot of emphasis on the architectural level, rather than finding new techniques to enhance the performance on the transistor design level. In order to propose such new techniques, a thorough study of the pipeline ADC behavior was undertaken, highlighting the main limitations posed by the individual building blocks. This study concludes that the majority of errors are attributed to the performance metrics of the amplifier used in the front-end S/H and MDACs.

A Recycling Folded Cascode (RFC) amplifier was proposed as a replacement to the conventional folded cascode to remedy or reduce many of its limitations. It has been demonstrated, both in theory and experimental results, that the RFC can achieve twice the gain bandwidth, 8-10 additional gain and at least twice the slew rate as the conventional folded cascode, without adding noise, degrading offset or using additional area or power. Moreover, the recycling folded cascode was confirmed to be robust low voltage environments.

To tackle the amplifier offset effects, the direct auto-zeroing offset cancellation scheme is optimized for low voltage environments using a dual level CMFB circuit, and it was shown that amplifier differential offsets up to 50mV are effectively cancelled. Together with the RFC, the dual level CMFB was used to implement a fully-differential

flip-around sample and hold amplifier driving a single-ended load of 1.4pF and using only 2.6mA, and at 200MS/s better than 9bit linearity is achieved.

Finally the kickback noise of dynamic comparators was addressed using a power conscious technique that replicates the noise with the opposite polarity such that the overall effect is reduced.

Together, these techniques were used in the design of a non-calibrated 1Vpp 10bit 160MS/s pipeline ADC in SMIC 0.18µm CMOS technology. The ADC is composed of a simple architecture; a front-end S/H, eight 1.5bits/stage pipeline cells and a 2bit flash. The ADC uses an area of $1.1mm^2$ and consumes 42mW in its analog core, and with a near Nyquist-rate full scale signal, 9.2 *ENOB* is achieved. Compared to recent state-of-the-art implementations in the 100-200MS/s range, the presented ADC design uses the least power per conversion rated at 0.45pJ/conversion-step.

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APPENDIX A

AMPLIFIER SETTLING PERFORMANCE UNDER SLEWING CONDITIONS

Consider the switched-capacitor amplifier given in Fig. A-1. Under no slewing conditions, *Vout(t)* is expressed by (A-1) in Φ_2 where the time constant $\tau = 1/(\beta GBW)$ and $\beta = C_{SH}/(C_{SH}+C_P)$. Given sufficient time, the final value of Vout(t) is given by (A-2). However, as the amplifier is limited by its slew rate (SR) when tracking fast transients, the settling no longer follows the exponential behavior.
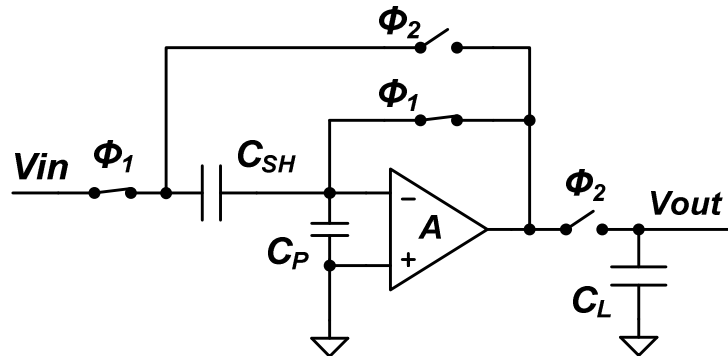
Fig. A-1. A switched-capacitor amplifier.

$$Vout(t) = Vin \left(1 + \frac{1}{\beta A}\right)^{-1} \left(1 - e^{-\frac{t}{\tau}}\right) = \alpha Vin\left(1 - e^{-t\beta GBW}\right) \qquad \text{(A-1)}$$

$$Vout(\infty) \equiv \overline{Vout} = \alpha Vin \qquad \text{(A-2)}$$

An amplifier settling with *SR* limitation is depicted by Fig. A-2. The settling can be divided into two regions, *SR*-limited and *GBW*-limited, and if given sufficient time,

the final value will be limited by the amplifier DC gain only.
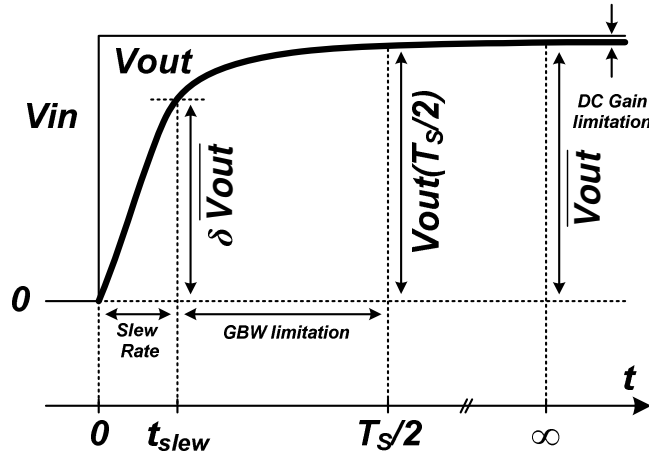
Fig. A-2. Amplifier settling with SR limitation.

The *SR* is defined as the rate of change of *Vout(t)* with respect to time as given by (A-3), where I_{SR} is the maximum current the amplifier can provide to charge/discharge its effective load C_{Leff}. Since the value given by (A-3) is a linear quantity, *Vout(t)* can be expressed by (A-4) in the *SR*-limited portion of the amplifier settling.

$$SR = \frac{\partial Vout(t)}{\partial t} = \frac{I_{SR}}{C_{Leff}} = \frac{I_{SR}}{C_L + \beta C_P} \qquad (A-3)$$

$$Vout(t) = SR \cdot t, \qquad t \leq t_{slew} \qquad (A-4)$$

As the amplifier enters the *GBW*-limited region, the remainder of the input step takes an exponential settling behavior and can be described by (A-5).

$$Vout(t) = SR \cdot t_{slew} + \left(\overline{Vout} - SR \cdot t_{slew}\right)\left(1 - e^{-\frac{(t-t_{slew})}{\tau}}\right)$$

$$= \overline{Vout} - \left(\overline{Vout} - SR \cdot t_{slew}\right) e^{-\frac{(t-t_{slew})}{\tau}}, \qquad t \geq t_{slew}$$

(A-5)

Note that (A-4) and (A-5) satisfy the boundary value condition between the *SR*-and *GBW*-limited settling regions at $t = t_{slew}$, but they also need to preserve continuity at the same boundary as described by (A-6). This is evaluated in (A-7), which defines t_{slew} such that continuity is preserved.

$$\left.\frac{\partial Vout(t)_{(A-4)}}{\partial t}\right|_{t=t_{slew}} = \left.\frac{\partial Vout(t)_{(A-5)}}{\partial t}\right|_{t=t_{slew}}$$

(A-6)

$$SR = \frac{1}{\tau}\left(\overline{Vout} - SR \cdot t_{slew}\right) \implies t_{slew} = \frac{\overline{Vout}}{SR} - \tau$$

(A-7)

Using (A-2) and (A-7) we can find the maximum input step *Vin* such that no slewing will occur as shown by (A-8). However, *GBW* can be expressed by (A-9), where the transconductance of the input differential pair $gm = I_T / V_{GST}$, I_T is the total tail current of the differential pair and V_{GST} is the overdrive voltage $V_{GS} - V_T$. Moreover, for many amplifiers the current I_{SR} is equivalent to the differential pair tail current I_T. Therefore, the maximum input step *Vin* for no slewing conditions can be expressed by (A-10).

$$t_{slew} = \frac{\alpha Vin}{SR} - \tau \leq 0 \implies Vin \leq \frac{\tau \cdot SR}{\alpha} = \frac{I_{SR}}{\alpha \beta GBW C_{Leff}}$$

(A-8)

$$GBW = \frac{gm}{C_{Leff}} = \frac{I_T}{V_{GST} C_{Leff}} \tag{A-9}$$

$$Vin \leq \frac{I_{SR}}{\alpha \beta GBW C_{Leff}} = \frac{V_{GST}}{\alpha \beta} \tag{A-10}$$

The result in (A-10) is significant as it demonstrates that amplifier slewing is inevitable in low voltage applications as V_{GST} is limited to 100-200mV and $\alpha\beta$ is roughly unity, whereas input steps can be as large as 500mV, especially in Nyquist-rate ADCs. Hence it is important to consider the settling time needed to attain a given accuracy in the presence of slewing and not solely rely on the *GBW* calculation given by (A-1).

We can rewrite *Vout(t)* as in (A-11) by substituting t_{slew} from (A-7) in (A-5) and using $\tau = 1/(\beta GBW)$. Then, for a given absolute settling error ε_S, we can find the settling time t_S as given by (A-12). By subtracting t_{slew} from (A-12) we get the time spent in the *GBW*-limited region, t_{lin}, given in (A-13).

$$Vout(t) = \overline{Vout} - \frac{SR}{\beta GBW} e^{-\left[1 + \beta GBW \left(t - \frac{\overline{Vout}}{SR}\right)\right]}, \quad t \geq t_{slew} \tag{A-11}$$

$$\varepsilon_S = \frac{SR}{\beta GBW} e^{-\left[1 + \beta GBW \left(t_S - \frac{\overline{Vout}}{SR}\right)\right]} \Rightarrow t_S = \frac{\overline{Vout}}{SR} + \frac{1}{\beta GBW}\left[\ln\left(\frac{SR}{\varepsilon_S \beta GBW}\right) - 1\right] \tag{A-12}$$

$$t_{lin} = \frac{1}{\beta GBW} \ln\left(\frac{SR}{\varepsilon_S \beta GBW}\right) \tag{A-13}$$

On the other hand, and as it is the case with switched-capacitor circuits, the final

settling value is determined at half the clock period $T_S/2$, which is then used to determine the requirements of the *GBW* and *SR* of the amplifier according to a desired final error. For this purpose we can express $Vout(T_S/2)$ in terms of $T_S/2$ for the different settling regions as shown in (A-14). From the previous discussion, most amplifiers in low voltage applications will fall under the second expression in (A-14).

$$Vout\left(\frac{T_S}{2}\right) = \begin{cases} SR\dfrac{Ts}{2}, & t_{slew} \geq \dfrac{T_S}{2} \\[2em] \overline{Vout} - \dfrac{SR}{\beta GBW} e^{-\left[1+\beta GBW\left(\frac{T_S}{2} - \frac{\overline{Vout}}{SR}\right)\right]}, & t_{slew} \leq \dfrac{T_S}{2} \\[2em] \overline{Vout}\left(1 - e^{-\beta GBW\frac{T_S}{2}}\right), & t_{slew} \leq 0 \end{cases} \qquad \text{(A-14)}$$

In ADCs the settling error is generally expressed in terms of bit resolutions. So for *N* bits desired accuracy, the error can be expressed by (A-15), but a direct analytical solution for either *SR* or *GBW* is not possible.

$$\varepsilon_S = \frac{SR}{\beta GBW} e^{-\left[1+\beta GBW\left(\frac{T_S}{2} - \frac{\overline{Vout}}{SR}\right)\right]} < \frac{\overline{Vout}}{2^N} \qquad \text{(A-15)}$$

This difficulty is alleviated, however, by introducing a parameter δ, which represents the portion of $\overline{Vout}$ that is covered in the *SR*-limited region as depicted in Fig. A-2, and can be used to substitute for βGBW as shown in (A-16). Using (A-16) with (A-

15), and after some algebra, an expression for the minimum *SR* necessary for *N* bits accuracy is reached, which is given in (A-17). The result of (A-17) can be applied to (A-16) to find a similar expression for *GBW*, which is given in (A-18).

$$t_{slew} = \frac{\overline{Vout}}{SR} - \frac{1}{\beta GBW} = \delta \frac{\overline{Vout}}{SR} \quad \Rightarrow \quad \beta GBW = \frac{SR}{\overline{Vout}(1-\delta)} \tag{A-16}$$

$$SR > \overline{Vout} \frac{2}{T_S} \left[\delta + (1-\delta)\ln\left(2^{Nr}(1-\delta)\right) \right] \tag{A-17}$$

$$GBW_{w/slew} > \frac{2}{\beta T_S} \left[\frac{\delta}{(1-\delta)} + \ln\left(2^{Nr}(1-\delta)\right) \right] \tag{A-18}$$

If we considered the *GBW* needed for *N* bits accuracy in the absence of *SR* limitation as given by the third expression of (A-14), the result would be (A-19). By normalizing (A-18) with respect to (A-19) we get (A-20).

$$GBW > \frac{2}{\beta T_S} \ln\left(2^{Nr}(1-\delta)\right) \tag{A-19}$$

$$\frac{GBW_{w/slew}}{GBW} = \frac{\delta + (1-\delta)\ln\left(2^{Nr}(1-\delta)\right)}{(1-\delta)\ln\left(2^{Nr}\right)} \tag{A-20}$$

Moreover, by rearranging (A-17) to express the $T_S/2$ and using the first half of (A-16), we can normalize t_{slew} with respect to $T_S/2$ as in (A-21).

$$\frac{t_{slew}}{T_S/2} = \frac{\delta}{\delta + (1-\delta)\ln(2^N(1-\delta))}$$

(A-21)

Expressions (A-20) and (A-21) are plotted for $N = 6$, 8, and 10 with respect to δ in Fig. A-3, to demonstrate the effect of *SR* on the *GBW* requirement of the amplifier. For example, if while slewing the amplifier covers $0.7\overline{Vout}$, and a settling accuracy of 8 bits is required, then t_{slew} constitutes about 35% of the settling time, and the $GBW_{w/slew}$ needs to be increased by at least 20% over the original *GBW* where the amplifier *SR* was not accounted for.
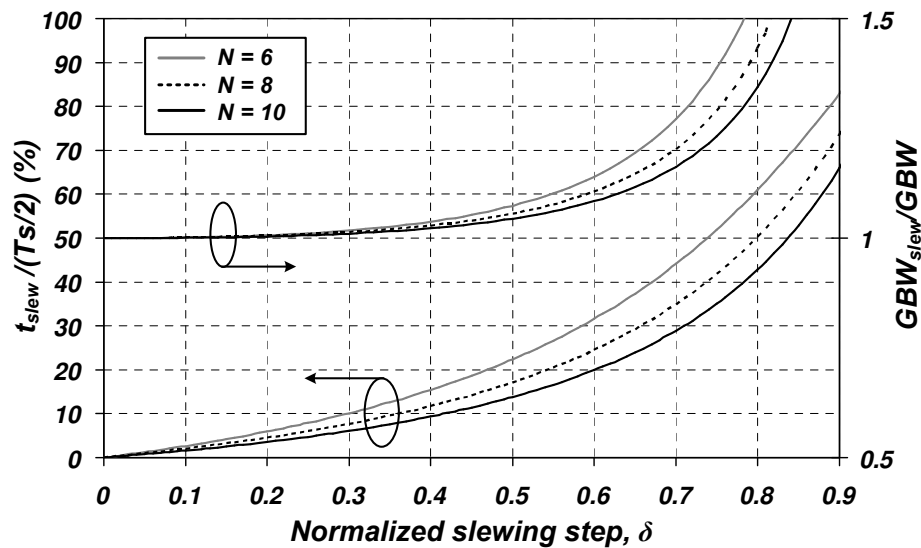

Fig. A-3. Effect of amplifier *SR* on *GBW* requirement.

APPENDIX B

MDAC NOISE ANALYSIS WITH ACTIVE SAMPLING

Switches and amplifiers are the fundamental contributors to the noise seen at the output of an MDAC. All noise sources present for both the sampling and holding phases in an *M* bit/stage MDAC are shown in Fig. B-1. Here, the power spectral density of the amplifier's input referred noise is denoted by $v_{n,A}^2$, whereas the subscripts *fb*, and *0* through *m*, where $m = 2^M-1$, represent the feedback and input switches and capacitors respectively. The forthcoming analysis will aim to find the total noise at the output to see how the switches and amplifier affect the MDAC noise performance.
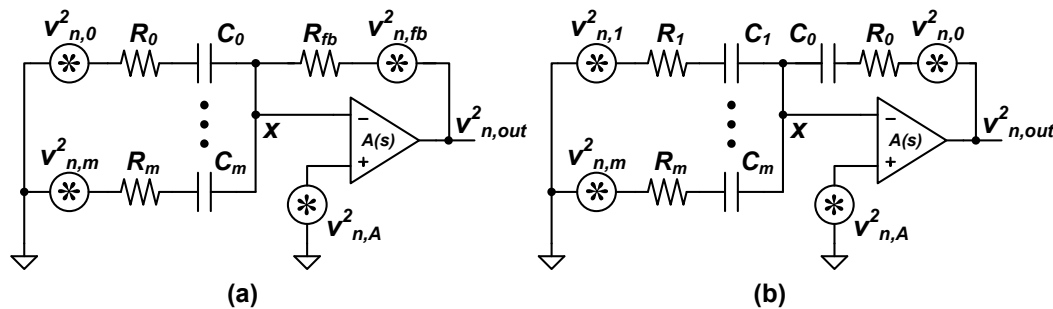
Fig. B-1. Noise sources present in an M bit/stage MDAC for (a) sampling phase and (b) holding phase.

Beginning with the sampling phase, the integrated noise on each capacitor is examined. Referring to Fig. B-1(a), and using $R_0..R_m=R_{sw}$, and $C_0..C_m=C_u$, the circuit can be described by (B-1)-(B-3). Here, *A(s)* is the amplifier transfer function and is defined by ω_u/s for simplicity, where ω_u is the amplifier unity gain frequency.

$$\frac{1}{R_{sw}}\left[v_x - \left(v_{n,out} + v_{n,fb}\right)\right] + \frac{sC_u}{1 + sR_{sw}C_u}\left[\sum_{i=0}^{m}\left(v_x - v_{n,i}\right)\right] = 0 \qquad \text{(B-1)}$$

$$v_{n,out} = A(s)\left(v_{n,A} - v_x\right) \cong \frac{\omega_u}{s}\left(v_{n,A} - v_x\right) \qquad \text{(B-2)}$$

$$v_{n,C_0} = \frac{v_x - v_{n,0}}{\left(1 + sR_{sw}C_u\right)} \qquad \text{(B-3)}$$

By substituting (B-1) and (B-2) into (B-3), the noise power stored on C_0 can be expressed as shown in (B-4), where $H_1(s)$, $H_2(s)$, $H_3(s)$ and $H_4(s)$ are given by (B-5), (B-6), (B-7) and (B-8) respectively.

$$v_{n,C_0}^2 = \left|H_1(s)\right|^2 \cdot v_{n,0}^2 + \left|H_2(s)\right|^2 \cdot v_{n,A}^2 + \left|H_3(s)\right|^2 \cdot v_{n,fb}^2 + \left|H_4(s)\right|^2 \cdot \sum_{i=1}^{m} v_{n,i}^2 \qquad \text{(B-4)}$$

$$H_1(s) = -\frac{1 + s\left(\dfrac{1}{\omega_u} + R_{sw}C_u\right) + s^2\dfrac{R_{sw}C_u}{\omega_u}(m+1)}{\left(1 + sR_{sw}C_u\right)\left(1 + s\left(\dfrac{1}{\omega_u} + R_{sw}C_u\right) + s^2\dfrac{R_{sw}C_u}{\omega_u}(m+2)\right)} \qquad \text{(B-5)}$$

$$H_2(s) = \frac{1}{1 + s\left(\dfrac{1}{\omega_u} + R_{sw}C_u\right) + s^2\dfrac{R_{sw}C_u}{\omega_u}(m+2)} \qquad \text{(B-6)}$$

$$H_3(s) = \frac{\dfrac{s}{\omega_u}}{1 + s\left(\dfrac{1}{\omega_u} + R_{sw}C_u\right) + s^2\dfrac{R_{sw}C_u}{\omega_u}(m+2)} \qquad \text{(B-7)}$$

$$H_4(s) = \frac{s^2 \dfrac{R_{sw}C_u}{\omega_u}}{\left(1 + sR_{sw}C_u\right)\left(1 + s\left(\dfrac{1}{\omega_u} + R_{sw}C_u\right) + s^2 \dfrac{R_{sw}C_u}{\omega_u}(m+2)\right)} \tag{B-8}$$

Next, the square magnitude of $H_1(s)$, $H_2(s)$, $H_3(s)$ and $H_4(s)$ is to be integrated over the frequency range $\{0,\infty\}$ to find the total noise power. A closed form solution for these integrals, however, is not easily achieved due to the complex roots of the second order transfer function in the numerator of (B-5) and denominators of (B-5)-(B-8). To alleviate this difficulty, we can drop the term $(m+1)$ and $(m+2)$ from (B-5)-(B-8) thereby transforming (B-5)-(B-8) to (B-9)-(B-12) respectively.

$$H_1(s) = -\frac{1}{\left(1 + sR_{sw}C_u\right)} \tag{B-9}$$

$$H_2(s) = \frac{1}{\left(1 + sR_{sw}C_u\right)\left(1 + \dfrac{s}{\omega_u}\right)} \tag{B-10}$$

$$H_3(s) = \frac{\dfrac{s}{\omega_u}}{\left(1 + sR_{sw}C_u\right)\left(1 + \dfrac{s}{\omega_u}\right)} \tag{B-11}$$

$$H_4(s) = \frac{s^2 \dfrac{R_{sw}C_u}{\omega_u}}{\left(1 + sR_{sw}C_u\right)^2\left(1 + \dfrac{s}{\omega_u}\right)} \tag{B-12}$$

Naturally, the simplification introduces an error, which is clearly visible in Fig. (B-2), where (B-5)-(B-8) are plotted for m = 1, 2, 3, along with (B-9)-(B-12); the values for R_{sw}, C_u and ω_u used in the plots were 100Ω, 1pF and 5G rad/s respectively.
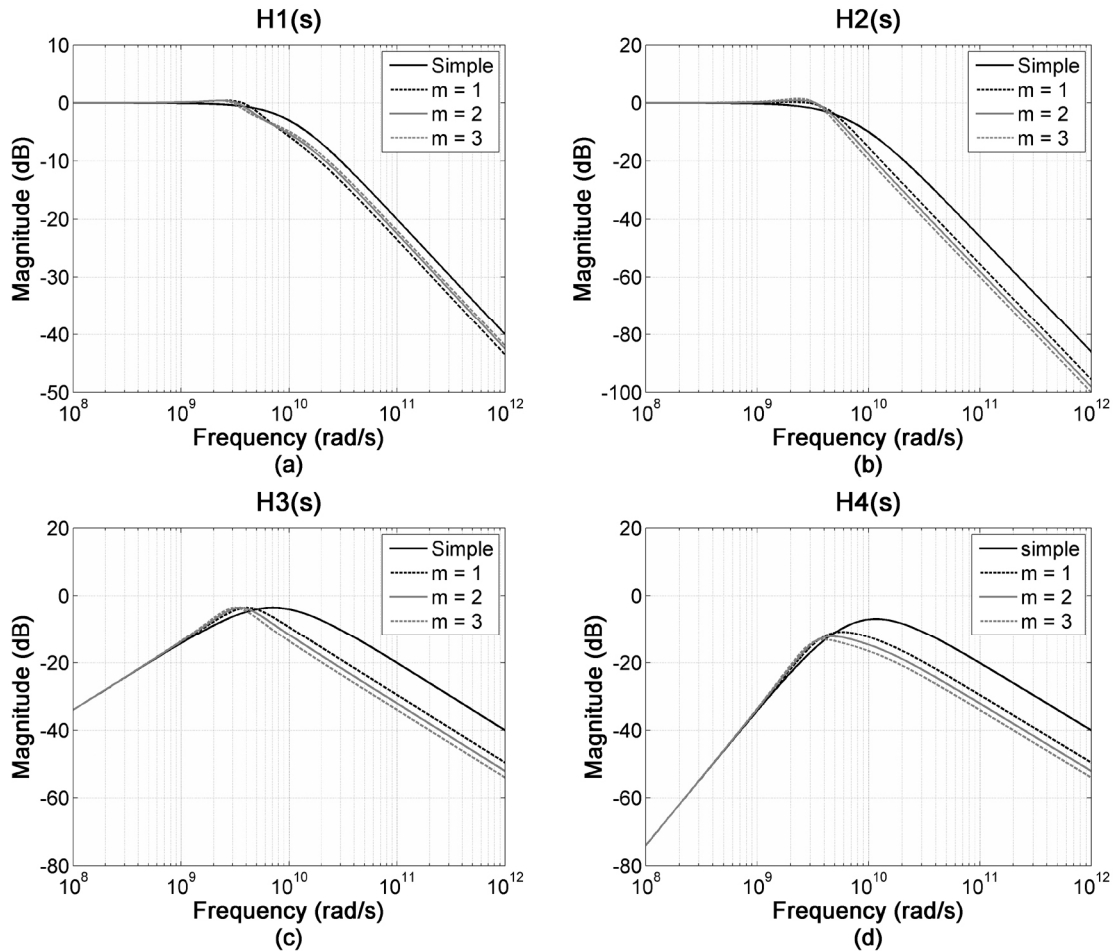

Fig. B-2. The magnitude plots of the original and simplified transfer function; (a) $H_1(s)$, (b) $H_2(s)$, (c) $H_3(s)$ and (d) $H_4(s)$.

While, this shows that (B-9)-(B-12) will yield an over estimate for the integrated noise, the resulting closed form integrals make for a more useable hand calculations tool

that inherently leaves a comfortable margin for design error. The final integral values are now given in (B-13)-(B-16).

$$\int_0^\infty |H_1(s)|^2 \cdot df = \frac{1}{4R_{sw}C_u} \tag{B-13}$$

$$\int_0^\infty |H_2(s)|^2 \cdot df = \frac{1}{4R_{sw}C_u\left(1+\dfrac{1}{\omega_u R_{sw}C_u}\right)} \tag{B-14}$$

$$\int_0^\infty |H_3(s)|^2 \cdot df = \frac{1}{4R_{sw}C_u\left(1+\omega_u R_{sw}C_u\right)} \tag{B-15}$$

$$\int_0^\infty |H_4(s)|^2 \cdot df = \frac{1}{8R_{sw}C_u\left(1+\dfrac{\omega_u^2 R_{sw}^2 C_u^2}{1+\omega_u R_{sw}C_u}\right)} \tag{B-16}$$

The computed integrals of (B-13)-(B-16) can now be substituted in (B-4) to get the total noise power sampled on C_0, which is given by (B-17).

$$v_{n,C_0}^2 = \frac{v_{n,0}^2}{4R_{sw}C_u} + \frac{v_{n,A}^2}{4R_{sw}C_u\left(1+\dfrac{1}{\omega_u R_{sw}C_u}\right)} + \frac{v_{n,fb}^2}{4R_{sw}C_u\left(1+\omega_u R_{sw}C_u\right)}$$
$$+ \frac{\displaystyle\sum_{i=1}^m v_{n,i}}{4R_{sw}C_u\left(1+\dfrac{\omega_u^2 R_{sw}^2 C_u^2}{1+\omega_u R_{sw}C_u}\right)} \tag{B-17}$$

The thermal noise power spectral density of a resistor is defined by (B-18) [44],

while the input referred noise of an amplifier can be modeled by (B-19) [49], where gm is the input pair transconductance, γ is a process dependent excess noise co-efficient and η is the amplifier architecture noise factor.

$$v_{n,sw}^2 = 4k_B T R_{sw} \cdot \Delta f \tag{B-18}$$

$$v_{n,A}^2 = \frac{4k_B T \, \gamma(1+\eta)}{gm} \cdot \Delta f \tag{B-19}$$

Using (B-18) and (B-19) in (B-17) yields the final form of v_{n,C_0}^2, which is the same for any v_{n,C_i}^2 as the characteristic equations (B-1)-(B-3) apply to any capacitor in Fig. B-1(a). The final result is given in (B-20). During the holding phase, Fig. B-1(b), all the noise power stored on the capacitors $C_0 .. C_m$ is transferred to the now feedback capacitor C_0. Therefore the sampling phase component of the output noise can be expressed by (B-21).

$$v_{n,C_i}^2 \Big|_{\Phi_S} = \frac{k_B T}{C_u} \left[1 + \frac{1}{1+\omega_u R_{sw} C_u} + \frac{m}{2\left(1 + \frac{\omega_u^2 R_{sw}^2 C_u^2}{1+\omega_u R_{sw} C_u}\right)} + \frac{\gamma(1+\eta)}{gmR_{sw}\left(1 + \frac{1}{\omega_u R_{sw} C_u}\right)} \right] \tag{B-20}$$

$$v_{n,out}^2 \Big|_{\Phi_S} = \frac{Q_{n,tot_S}^2}{C_0^2} = \sum_0^m v_{n,C_i}^2 \Big|_{\Phi_S} = (m+1) \cdot v_{n,C_i}^2 \Big|_{\Phi_S} \tag{B-21}$$

As for the holding phase component of the output noise, it can be evaluated using

Fig. B-1(b), which is characterized by (B-22) and (B-23).

$$v_x - \left(v_{n,out} + v_{n,fb}\right) + \sum_{i=0}^{m}\left(v_x - v_{n,i}\right) = 0 \tag{B-22}$$

$$v_{n,out} = A(s)\left(v_{n,A} - v_x\right) \cong \frac{\omega_u}{s}\left(v_{n,A} - v_x\right) \tag{B-23}$$

Using (B-22) and (B-23) to eliminate v_x, the output noise power in the holding phase, $v_{n,out}^2\big|_{\Phi_H}$, can be expressed by (B-24), where $H_5(s)$ is given by (B-25).

$$v_{n,out}^2\big|_{\Phi_H} = \left|H_5(s)\right|^2 \cdot \left[(m+1)\, v_{n,A}^2 + \sum_{i=1}^{m} v_{n,i}^2\right] \tag{B-24}$$

$$H_5(s) = \frac{1}{1 + \dfrac{s(m+1)}{\omega_u}} \tag{B-25}$$

For the final form of the holding phase output noise, the square magnitude of $H_5(s)$ is integrated over the frequency range $\{0,\infty\}$, and (B-18) and (B-19) are substituted for $v_{n,i}^2$ and $v_{n,A}^2$ respectively. This results in (B-26), where ω_u is substituted with gm/C_L, and C_L being the effective loading capacitance.

$$v_{n,out}^2\big|_{\Phi_H} = \frac{k_B T}{C_L}\left[\, gmR_{sw} + \gamma(1+\eta)(m+1)\,\right] \tag{B-26}$$

The total noise seen at the output of the MDAC is the summation of (B-21) and (B-26), and is given in (B-27) where α_n is described by (B-28). Note that (B-21) is doubled for a fully differential implementation as well as the effect of the switch resistance in (B-26). Also, it is common practice to refer this noise to the input of the pipeline cell for a meaningful comparison with the input signal. This is accomplished by simply normalizing the output noise to the square of the MDAC gain *(m+1)*, and is demonstrated by (B-29).

$$v_{n,out}^2\big|_{MDAC} = \frac{k_B T}{C_L}\left[2gmR_{sw} + \gamma\left(1+\eta\right)\left(m+1\right)\right] + 2\left(m+1\right)\frac{k_B T}{C_u}\left(1+\alpha_n\right) \tag{B-27}$$

$$\alpha_n = \frac{1}{1+\omega_u R_{sw} C_u} + \frac{m}{2\left(1+\dfrac{\omega_u^2 R_{sw}^2 C_u^2}{1+\omega_u R_{sw} C_u}\right)} + \frac{\gamma\left(1+\eta\right)}{gmR_{sw}\left(1+\dfrac{1}{\omega_u R_{sw} C_u}\right)} \tag{B-28}$$

$$v_{n,in}^2\big|_{MDAC} = \frac{k_B T}{\left(m+1\right)C_L}\left[\gamma\left(1+\eta\right) + \frac{2gmR_{sw}}{\left(m+1\right)}\right] + 2\frac{k_B T}{\left(m+1\right)C_u}\left(1+\alpha_n\right) \tag{B-29}$$

In conclusion, the noise contributions of the switches and amplifier to the MDAC noise are limited by the unit capacitance, C_u, used in the MDAC and the effective loading capacitance, C_L, seen by the amplifier. Moreover, the use of multi-bit/stage pipeline cells has an added filtering effect on the total noise. However, this added benefit of lower noise is a direct trade-off with the speed of the pipeline ADC.

APPENDIX C

OPERATIONAL TRANSCONDUCTANCE AMPLIFIER PARAMETERS

Referring to the OTAs in Fig. 46, the following is a summary of key performance metrics expressions, based on the following assumptions: all amplifiers are driving a capacitive load C_L, cascode devices are treated as source degenerated devices for noise and offset calculations and hence are neglected due to their small transconductance, and finally M denotes the transistor aspect ratio W/L.

A. *Telescopic OTA (TL)*

$$Gm_{TL} = gm_1 \tag{C-1}$$

$$A(0) = Gm_{TL}R_{OUT} \cong gm_1 \cdot \left(gm_3 r_{ds1} r_{ds3} \| gm_5 r_{ds5} r_{ds7}\right) \tag{C-2}$$

$$PM = 180 - \tan^{-1}\left(\frac{GBW}{\omega_{P1}}\right) - \tan^{-1}\left(\frac{GBW}{\omega_{P2}}\right) \tag{C-3}$$

$$GBW = \frac{gm_1}{C_L}, \qquad \omega_{P1} = \frac{1}{R_{OUT}C_L}, \qquad \omega_{P2} \cong \frac{gm_3}{C_{gs3}} \tag{C-4}$$

$$SR = \frac{I_T}{C_L} \tag{C-5}$$

$$\eta = \frac{Gm_{TL}}{I_{total}} = \frac{gm_1}{I_T} \tag{C-6}$$

$$\overline{v_{iT}^2} = \frac{8k_B T\gamma}{gm_1}\left(1 + \frac{gm_3}{gm_1}\right) \cdot \Delta f = \frac{8k_B T\gamma}{\sqrt{2\mu_P C_{ox} I_{D1} M_1}}\left(1 + \sqrt{\frac{\mu_N}{\mu_P}\frac{M_3}{M_1}}\right) \cdot \Delta f \tag{C-7}$$

$$\overline{v_i^2/_f} = \frac{2I_D}{gm_1^2 C_{ox} f} \left(\frac{K_{FP}}{L_1^2} + \frac{K_{FN}}{L_7^2} \right) \cdot \Delta f = \frac{K_{FP}}{\mu_P W_1 L_1 C_{ox}^2 f} \left[1 + \frac{K_{FN}}{K_{FP}} \left(\frac{L_1}{L_7} \right)^2 \right] \cdot \Delta f \qquad \text{(C-8)}$$

$$\overline{v_i^2/_f}\bigg|_{\min} \quad \Rightarrow \quad L_1 = L_7 \sqrt{\frac{K_{FP}}{K_{FN}}} \qquad \text{(C-9)}$$

$$\sigma^2(V_{OS}) = 2 \frac{A_{V_{TP}}^2}{W_1 L_1} \left[1 + \frac{\mu_N}{\mu_P} \left(\frac{A_{V_{TN}}}{A_{V_{TP}}} \right)^2 \left(\frac{L_1}{L_7} \right)^2 \right] \qquad \text{(C-10)}$$

$$\sigma^2(V_{OS})\big|_{\min} \quad \Rightarrow \quad L_1 = L_3 \sqrt{\frac{\mu_P}{\mu_N}} \cdot \frac{A_{V_{TP}}}{A_{V_{TN}}} \qquad \text{(C-11)}$$

B. Current Mirror OTA (CM)

$$Gm_{CM} = K \cdot gm_1 \qquad \text{(C-12)}$$

$$A(0) = Gm_{CM} R_{OUT} \cong K \cdot gm_1 \cdot \left(gm_7 r_{ds7} r_{ds5} \| gm_9 r_{ds9} r_{ds11} \right) \qquad \text{(C-13)}$$

$$PM = 180 - \tan^{-1} \left(\frac{GBW}{\omega_{P1}} \right) - \tan^{-1} \left(\frac{GBW}{\omega_{P2}} \right) - \tan^{-1} \left(\frac{GBW}{\omega_{P3}} \right) \qquad \text{(C-14)}$$

$$GBW = \frac{K \cdot gm_1}{C_L}, \quad \omega_{P1} = \frac{1}{R_{OUT} C_L}, \quad \omega_{P2} \cong \frac{gm_7}{C_{gs7}}, \quad \omega_{P2} \cong \frac{gm_3}{C_{gs3}(1+K)} \qquad \text{(C-15)}$$

$$SR = \frac{K \cdot I_T}{C_L} \qquad \text{(C-16)}$$

$$\eta = \frac{Gm_{CM}}{I_{total}} = \frac{K \cdot gm_1}{(K+1)I_T} \qquad \text{(C-17)}$$

$$\overline{v_{iT}^2} = \frac{8k_B T \gamma}{gm_1} \left(1 + \frac{gm_3}{gm_1} + \frac{gm_5}{K^2 gm_1} + \frac{gm_{11}}{K^2 gm_1} \right) \cdot \Delta f$$

$$= \frac{8k_B T \gamma}{\sqrt{2\mu_P C_{ox} I_{D1} M_1}} \left(1 + \sqrt{\frac{\mu_N}{\mu_P} \frac{M_3}{M_1}} + \frac{1}{K^2} \sqrt{\frac{\mu_N}{\mu_P} \frac{M_5}{M_1}} + \frac{1}{K^2} \sqrt{\frac{M_{11}}{M_1}} \right) \cdot \Delta f \qquad \text{(C-18)}$$

$$\overline{v_i^2}_{1/f} = \frac{2I_D}{gm_1^2 C_{ox} f}\left(K^2 \frac{K_{FP}}{L_1^2} + K^2 \frac{K_{FN}}{L_3^2} + K \frac{K_{FN}}{L_5^2} + K \frac{K_{FP}}{L_{11}^2}\right) \cdot \Delta f$$

$$= \frac{K_{FP}}{\mu_P W_1 L_1 C_{ox}^2 f}\left[1 + \frac{K_{FN}}{K_{FP}}\left(\frac{L_1}{L_3}\right)^2 + \frac{1}{K}\frac{K_{FN}}{K_{FP}}\left(\frac{L_1}{L_5}\right)^2 + \frac{1}{K}\left(\frac{L_1}{L_{11}}\right)^2\right] \cdot \Delta f \qquad \text{(C-19)}$$

$$\overline{v_i^2}_{1/f}\bigg|_{min} \quad \Rightarrow \quad L_1 = \left[\frac{K_{FN}}{K_{FP}}\left(\frac{1}{L_3}\right)^2 + \frac{1}{K}\frac{K_{FN}}{K_{FP}}\left(\frac{1}{L_5}\right)^2 + \frac{1}{K}\left(\frac{1}{L_{11}}\right)^2\right]^{-1/2} \qquad \text{(C-20)}$$

$$\sigma^2(V_{OS}) = 2\frac{A_{V_{TP}}^2}{W_1 L_1}\left[1 + \frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{L_1}{L_3}\right)^2 + \frac{1}{K}\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{L_1}{L_5}\right)^2 + \frac{1}{K}\left(\frac{L_1}{L_{11}}\right)^2\right] \qquad \text{(C-21)}$$

$$\sigma^2(V_{OS})\big|_{min} \quad \Rightarrow \quad L_1 = \left[\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{1}{L_3}\right)^2 + \frac{1}{K}\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{1}{L_5}\right)^2 + \frac{1}{K}\left(\frac{1}{L_{11}}\right)^2\right]^{-1/2} \qquad \text{(C-22)}$$

C. Folded Cascode OTA (FC)

$$Gm_{FC} = gm_1 \qquad \text{(C-23)}$$

$$A(0) = Gm_{FC}R_{OUT} \cong gm_1 \cdot \left(gm_5 r_{ds5}\left(r_{ds1}\|r_{ds3}\right)\|gm_7 r_{ds7} r_{ds9}\right) \qquad \text{(C-24)}$$

$$PM = 180 - \tan^{-1}\left(\frac{GBW}{\omega_{P1}}\right) - \tan^{-1}\left(\frac{GBW}{\omega_{P2}}\right) \qquad \text{(C-25)}$$

$$GBW = \frac{K \cdot gm_1}{C_L}, \quad \omega_{P1} = \frac{1}{R_{OUT}C_L}, \quad \omega_{P2} \cong \frac{gm_5}{C_{gs5}} \qquad \text{(C-26)}$$

$$SR = \frac{I_T}{C_L} \qquad \text{(C-27)}$$

$$\eta = \frac{Gm_{FC}}{I_{total}} = \frac{gm_1}{2I_T} \qquad \text{(C-28)}$$

$$\overline{v_{iT}^2} = \frac{8k_BT\gamma}{gm_1}\left(1 + \frac{gm_3}{gm_1} + \frac{gm_9}{gm_1}\right) \cdot \Delta f = \frac{8k_BT\gamma}{\sqrt{2\mu_P C_{ox} I_{D1} M_1}}\left(1 + \sqrt{2\frac{\mu_N}{\mu_P}\frac{M_3}{M_1}} + \sqrt{\frac{M_9}{M_1}}\right) \cdot \Delta f \quad \text{(C-29)}$$

$$\overline{v_{i\,1/f}^2} = \frac{2I_D}{gm_1^2 C_{ox} f}\left(\frac{K_{FP}}{L_1^2} + \frac{2K_{FN}}{L_3^2} + \frac{K_{FN}}{L_9^2}\right) \cdot \Delta f$$

$$= \frac{K_{FP}}{\mu_P W_1 L_1 C_{ox}^2 f}\left[1 + 2\frac{K_{FN}}{K_{FP}}\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_9}\right)^2\right] \cdot \Delta f \quad \text{(C-30)}$$

$$\overline{v_{i\,1/f}^2}\Bigg|_{min} \quad \Rightarrow \quad L_1 = \left[2\frac{K_{FN}}{K_{FP}}\left(\frac{1}{L_3}\right)^2 + \left(\frac{1}{L_9}\right)^2\right]^{-1/2} \quad \text{(C-31)}$$

$$\sigma^2(V_{OS}) = 2\frac{A_{V_{TP}}^2}{W_1 L_1}\left[1 + 2\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{L_1}{L_3}\right)^2 + \left(\frac{L_1}{L_9}\right)^2\right] \quad \text{(C-32)}$$

$$\sigma^2(V_{OS})\Big|_{min} \quad \Rightarrow \quad L_1 = \left[2\frac{\mu_N}{\mu_P}\left(\frac{A_{V_{TN}}}{A_{V_{TP}}}\right)^2\left(\frac{1}{L_3}\right)^2 + \left(\frac{1}{L_9}\right)^2\right]^{-1/2} \quad \text{(C-33)}$$

VITA

Rida Shawky Assaad received his Bachelor of Science degree in electrical engineering from Texas A&M University in May 2002. He joined the Analog and Mixed Signal Center at Texas A&M University in August 2002 and received his Ph.D. degree in electrical engineering in December 2009. During 2005 he was an assistant lecturer at the Electrical and Computer Engineering Department where he taught the introductory course to electronics. He was an intern IC designer with Mobile Integrated Solutions at Texas Instruments, Dallas, in the fall of 2007 and 2008. His research interests include the design and optimization of base-band amplifiers and high resolution analog-to-digital converters.

Mr. Assaad can be reached at the Analog and Mixed Signal Center, Weisenbaker Engineering Research Center, Texas A&M University, College Station, TX 77843-3128. His email address is: rida@tamu.edu.