FILTER DESIGN CONSIDERATIONS FOR HIGH PERFORMANCE CONTINUOUS-TIME LOW-PASS SIGMA-DELTA ADC

A Thesis

by

VENKATA VEERA SATYA SAIR GADDE

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2009

Major Subject: Electrical Engineering

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Approved by:

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ABSTRACT

Filter Design Considerations for High Performance Continuous-time Low-pass Sigma-delta ADC. (December 2009)

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Continuous-time filters are critical components in the implementation of large bandwidth, high frequency, and high resolution continuous-time (CT) sigma-delta (ΣΔ) analog-to-digital converters (ADCs). The loop filter defines the noise-transfer function (NTF) and hence the quantization noise-shaping behavior of the ΣΔ modulator, and becomes the most critical performance determining part in ΣΔ ADC.

This thesis presents the design considerations for the loop filter in low-pass CT ΣΔ ADC with 12-bits resolution in 25MHz bandwidth and low power consumption using 0.18μm CMOS technology. Continuous-time filters are more suitable than discrete-time filters due to relaxed amplifier bandwidth requirements for high frequency ΣΔ ADCs. A fifth-order low-pass filter with cut-off frequency of 25 MHz was designed to meet the dynamic range requirement of the ADC. An active RC topology was chosen for the implementation of the loop filter, which can provide high dynamic range required by the ΣΔ ADC. The design of a summing amplifier and a novel method for adjusting the group delay in the fast path provided by a secondary feedback DAC of the ΣΔ ADC are presented in detail. The ADC was fabricated using Jazz 0.18μm CMOS technology.

The implementation issues of OTAs with high-linearity and low-noise performance suitable for the broadband ADC applications are also analyzed in this work. Important design equations pertaining to the linearity and noise performance of the Gm-C biquad filters are presented. A G_m-C biquad with 100MHz center frequency and quality factor 10 was designed as a prototype to confirm with the theoretical design equations. Transistor level circuit implementation of all the analog modules was completed in a standard 0.18μm CMOS process.

To god

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I would like to express my most sincere thanks to my advisor, Dr. Jose Silva-Martinez, who has been a great source of inspiration and support throughout my graduate studies. When I first approached him to start my research, he accepted me as his student in spite of my limited knowledge in analog and mixed signal design. The endless doubts from my side never seemed to bother him, and he patiently answered all my questions. The long discussions with him have helped me to understand different aspects of analog design, and I am greatly indebted to him for his guidance, encouragement and support during my graduate studies.

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1. INTRODUCTION

1.1 Motivation

The recent technological growth in the wireless communication industry indicates a strong need for ultra-high performance analog-to-digital converters (ADCs) for future wireless radios. Radio frequency (RF) and analog/mixed-signal technologies pay essential and critical role for the success of wireless communications industry. Single-chip multimode, multiband, and multi-standard wireless radio implementations are instrumental for advancing the state-of-the art wireless communication products. This would help the next generation receivers that require support for multiple service providers on a single wireless device [1].

Next generation wireless receivers need support for multiple standards on a single chip. Numerous communications standards have been introduced in the recent past. The most common wireless communication applications are shown in Fig. 1.

Figure 1 Different wireless applications and standards

This thesis follows the style and format of the *IEEE Journal of Solid-State Circuits*.

The cell phone communication standards include GSM (Global System for Mobile communications), GPRS (General Packet Radio Service), EDGE (Enhanced Data rate for GSM Evolution), CDMA (Code Division Multiple Access), AMPS (Advanced Mobile Phone Systems), UMTS (Universal Mobile Telecommunication System) etc. The standards used in communication networks include WLAN (Wireless Local Area Network), Bluetooth, WI-MAX (Worldwide Interoperability for Microwave Access) and UWB (Ultra Wide Band). The satellite communication standards include GPS (Global Positioning System) standard.

A generic block diagram of wireless receiver is shown in Fig. 2. The architecture of the wireless receiver defines the location of ADC in a receiver chain. If the ADC is placed close to the antenna, important functions such as filtering and frequency translation can be performed in digital domain, which reduces receiver's complexity and increases flexibility. Depending on the architecture of the receiver, the ADC needs to digitize an RF, intermediate-frequency (IF), or the baseband signal. Therefore, the location of ADC in a receiver affects the overall performance, complexity, power dissipation, size and cost of a wireless receiver. A flexible wireless radio should be able to deal with the narrowband / high-dynamic range requirements of cellular standards as well as the wideband / low-dynamic range requirements of WLAN and WiMAX standards, in combination with other standards like Bluetooth and digital video broadcasting-handheld (DVB-H). In this context, it becomes extremely important to explore the ADC architectures that enable reconfiguration and full integration in a RF transceiver.

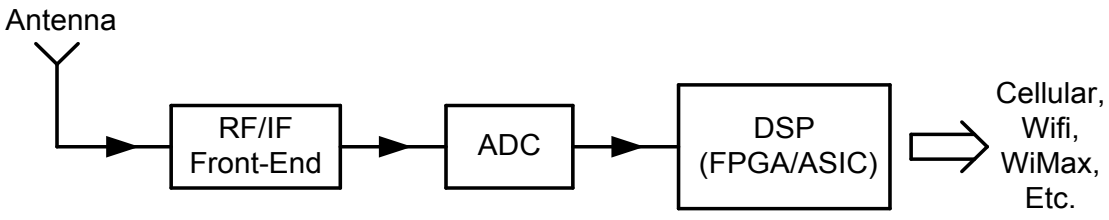


Figure 2 Generic block diagram of a wireless receiver

The sigma-delta (ΣΔ) ADCs provide an effective way to implement high-performance ADCs without stringent matching requirements or calibration. They allow inherent trade-off between bandwidth and dynamic range. Therefore, they are suitable for multi-standard implementations of wireless radio as they provide a variable bandwidth and dynamic range. They lower the specifications for the anti-aliasing filter in front of the ADC. Also, the adjacent interferers fall into the same band as the shaped quantization noise and the digital filters can remove both quantization noise and interferers. Applications like WLAN and WiMAX require wideband ADCs that can digitize both the desired and adjacent-channel interferes, resulting in high dynamic range (DR) requirements. However, the high bandwidth and high dynamic range requirements make the real circuit implementation of ΣΔ modulators challenging.

In the design of high performance sigma-delta modulators, the use of analog loop filters is unavoidable. The transfer function of the loop filter defines the quantization noise-shaping behavior of the ΣΔ modulator. The stability of ΣΔ modulator mainly depends on the location of poles and zeros in the loop filter. Hence, the loop filter becomes a major performance determining part in a ΣΔ ADC. For applications requiring wide bandwidth and high resolution, the design of analog filters is becoming increasingly difficult.

1.2 Overview of analog filters

Next generation communication systems require high dynamic range filters that can be integrated on the same chip. The technology and implementation techniques are very important issues to be considered in the design of loop filters in sigma-delta ADCs. The design of CMOS analog filters can broadly be divided into two categories, namely continuous-time and discrete-time techniques [2]. Switched-capacitor and switched-current techniques are examples of discrete-time or sampled-data implementations. The active RC filter, MOSFET-C filters and OTA-C filters are the popularly known continuous-time filter implementations. An integrator is the basic building block in the

implementation of analog filters. Example implementations of discrete-time and continuous-time integrators are shown in Fig. 3a and Fig. 3b respectively.

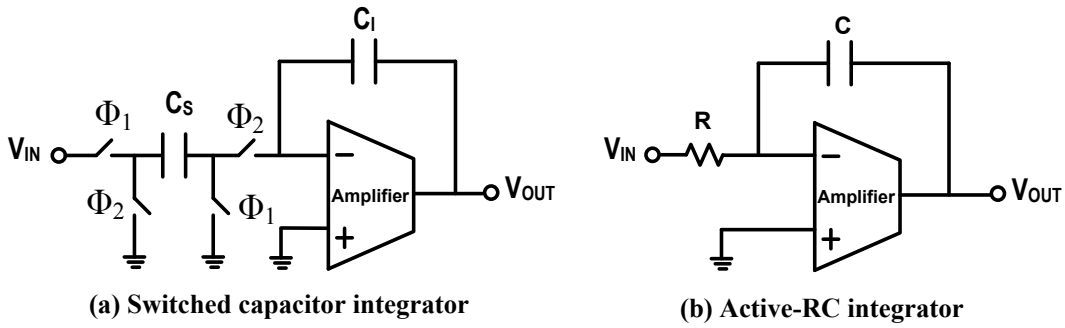


Figure 3 Examples of discrete-time and continuous-time integrators

1.2.1 Discrete-time filters

Discrete-time filters use multiple clock phases that are non-overlapping in time. In switched capacitor techniques the main characteristics are determined by the clock frequency and the capacitor ratios. These two parameters are almost independent of the process and temperature variations. The high accuracy of the integrator time constant is the major advantage of discrete-time techniques. Furthermore, as the input of the opamp is a virtual ground node, the distortion is very low. In low frequency applications, the high dc gain and high gain-bandwidth of the CMOS operational amplifiers make these filters insensitive to the parasitic capacitors. However, these advantages of switched-capacitor filters are not necessarily maintained for high frequency applications. This is mainly due to the finite dc gain and finite gain bandwidth of the operational amplifiers, the finite resistance of the switches and the clock feed-through.

In high frequency applications the operational amplifier has to be fast enough to settle to the correct output within a half time period of the sampling clock. For a settling precision of 0.1%, the settling time should be higher than the gain-bandwidth of the operational amplifier at least by a factor 7. However, due to contribution of the feedback

factor even larger GBWs are required. In order to guarantee the stability of the closed loop system, the second pole of the operational amplifier should be placed around three times higher than the GBW. For high frequency applications, it is very difficult to satisfy these requirements. The dc gain of the opamp has to be high enough to minimize the signal swing at its input terminals. And, the circuit becomes parasitic insensitive and allows the total charge and discharge of the capacitors. Otherwise the precision of the filters is reduced and the harmonic distortion increases rapidly.

In general, sampled-data filters need an anti-aliasing filter to band limit the frequencies of the input signal. Due to the sampling, high frequency noise can be aliased on to the base band which increases the in band noise reducing the filter's dynamic range. In wireless applications, where in several information channels must be separated it is not possible to use sampled data filters due to aliasing effect. A filtering technique that avoids many of the disadvantages with discrete-time techniques is the continuous-time filtering technique.

1.2.2 Continuous-time filters

In the earlier generation of continuous-time filters the basic network elements were inductor, capacitor and resistor. With the evolution of the integrated circuits, the inductors have been replaced by equivalent networks composed of active devices and capacitors. The resulting topologies are called active RC filters. The active devices of the active RC filters are either OPAMPs or OTAs. Aliasing problems are not present in continuous-time filters, which is beneficial when having to handle large interferers. In continuous-time filters based on OTA-C techniques, integrator time constants depend on C/g_m ratios. Due to the lack of virtual grounds and low impedance nodes, the time constants are not very well controlled. They are affected by the process, temperature variations and parasitic capacitors. In addition to these, the active filters are very sensitive to the OTA non-idealities including finite dc gain, finite bandwidth, parasitic poles and zeros.

The active RC filters use OPAMPs, resistors and capacitors as basic elements. In the present day CMOS technology, the resistors can be implemented either as diffused or poly-silicon resistors. The linearity of the polysilicon resistors is quite good enough and the accuracy of resistors ratios can be as good as 1%. But, the accuracy of the RC products can be as worse as 30%. The RC product is a strong function of both process and temperature variations. Unfortunately, the frequency of poles and frequency of zeros is determined by RC products. Typically, the quality factor of the filter is determined by resistors and/or capacitor ratios. Because the filters are more sensitive to variations in the frequency of the poles than the quality factors, the accuracy of the active RC filters is quite low. The accuracy of these filters can be improved by including certain kind of tuning, either on chip or externally.

1.3 Overview of analog-to-digital converter architectures

Digital circuits require very small area and provide extremely large dynamic range at very low cost. Hence, digital signal processing (DSP) has gained momentum in the present decade. However, the digital signal processors have to interface with the real analog world. Therefore, high performance data converters become critical for extremely fast paced improvements of DSP. As the digital signal processing is moved closer to the receiving antenna, the demands on the speed and dynamic range of the analog-to-digital converter become increasingly severe.

There are two broad classifications of ADCs based on the relation between the sampling frequency and the bandwidth of the input analog signal. They are Nyquist-rate and oversampled ADCs. As shown in Fig. 4, in data converters the speed is always traded with the resolution. Flash architectures are the fastest topology but they provide the lowest resolution. The folding, sub-ranging and pipeline ADC architectures are in the very high speed and medium to low resolution category. The successive approximation and sigma-delta ADCs provide high/medium speed and fall in high resolution category. The incremental and integrating dual ramp ADC architectures fall in the low speed and

very high resolution category [3]. Power consumption increases with increase in the sampling frequency. All the ADC architectures, except sigma-delta, fall under Nyquist rate category. The sigma-delta ADC is an example of oversampling ADC.

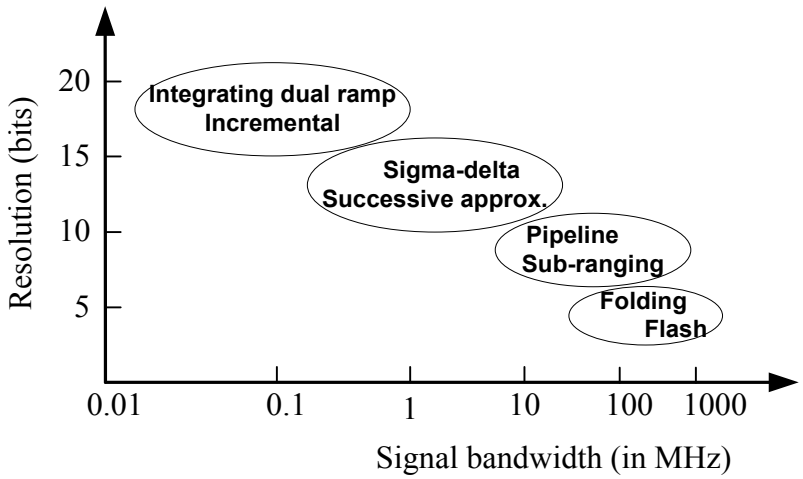


Figure 4 Classification of different ADC architectures based on resolution and speed

This thesis presents the design considerations for the loop filter in low-pass continuous-time sigma-delta ADC with 12-bits resolution in 25MHz bandwidth and low power consumption using 0.18µm CMOS technology. The main target of this work is to identify and design a suitable filter architecture that satisfies the ADC system-level requirements. It involves designing loop filter that can provide signal-to-noise-and-distortion-ratio (SNDR) greater than 72dB. In this context, this thesis presents the implementation details of two popular filter realization topologies, namely, G_m-C and active-RC. Active-RC topology is preferred over its G_m-C counterpart due to the high linearity requirements.

1.4 Organization of the thesis

There are seven sections in the thesis. Section 1 provides a brief introduction to the architecture of generic wireless receiver and different communication standards. A

brief note on the popular ADC architectures is presented. The importance of analog filters in the design of next generation wireless receivers is identified.

In section 2, properties of the ideal sigma-delta modulator are presented. The architectural differences between continuous-time and discrete-time sigma-delta ADCs are discussed. Some of the system level issues in the implementation of continuous-time sigma-delta modulators are explained. Various performance parameters of the sigma-delta ADCs are discussed in brief.

In section 3, system level design of 12-bit resolution, 25MHz input signal bandwidth continuous-time low-pass sigma-delta ADC is presented. The important system level considerations for determining the open loop filter transfer function of the sigma-delta modulator are presented. An overview of the system implementation is presented together with the behavioral simulation results.

In section 4, theory and simulation results of the G_m-C band pass filter are discussed. The linearity and noise performance of the OTA and the biquadratic cell are analyzed in a detailed manner. The simulations results for a biquad designed to operate at 100MHz center frequency with a quality factor of 10 are presented. It is shown that the linearity of the biquad depends on the frequency separation between the input-tones used for IM3 measurement.

In section 5, the design of a 5^{th} order active low-pass filter for a continuous-time sigma-delta ($\Sigma\Delta$) ADC is presented. The circuit implementation details of the amplifiers used in the integrator stages are presented. The design of a summing amplifier and a novel method for adjusting the group delay in the fast path provided by a secondary feedback DAC of the $\Sigma\Delta$ ADC are presented in detail.

In section 6, the layout and simulation results of the 5^{th} order active low-pass filter are presented. The chip micrograph, test setup and preliminary experimental results of the $\Sigma\Delta$ ADC are presented in this section. Summary and conclusions are provided in section 7.

2. PROPERTIES OF THE SIGMA-DELTA MODULATOR

This section gives an overview of the basic operation of ideal sigma-delta modulator. The architectural differences between continuous-time and discrete-time sigma-delta ADCs are discussed. Some of the system level implementation issues of continuous-time sigma-delta modulators are presented. Various performance parameters of the sigma-delta ADCs are discussed in brief.

2.1 Analog-to-digital conversion

The process of sampling a continuous time analog signal can be treated as multiplying the signal by a train of impulses spaced by T_s seconds. T_s represents the sampling time interval expressed as the inverse of sampling frequency, F_s. Mathematically, the time-domain representation of sampling operation of a continuous-time signal X(t) that produces a sampled output signal $X_s(t)$ given by

$$X_s(t)= \sum_{n= -\infty}^{\infty} X(t)\ \delta(t-nT_s) \tag{2.1}$$

where, n is an integer and δ is the ideal impulse function. If X(f) represents the Fourier transform of X(t), the frequency domain representation of equation (2.1) can be obtained as

$$X_s(f) = X(f) \sum_{n=-\infty}^{\infty} \frac{1}{T_s}\ \delta(f - nF_s) \tag{2.2}$$

From equation (2.2), it can be seen that the sampling operation modulates the input signal by carrier frequencies that are integer multiples of sampling frequency (F_s, $2F_s$, $3F_s$ etc.). Since the real world signals are band-limited the maximum signal frequency (F_{sig}) defines the minimum sampling rate requirement. As per Nyquist sampling theorem, the minimum sampling frequency required is twice the maximum signal bandwidth. The minimum sampling frequency that recovers the original signal

perfectly from sampled signal is commonly referred as Nyquist sampling rate which is expressed as

$$F_{Nyquist} = 2 * F_{sig} \quad (2.3)$$

The conceptual diagrams showing the Nyquist-rate and the oversampling ADC architectures are presented in Fig. 5a and Fig. 5b respectively.

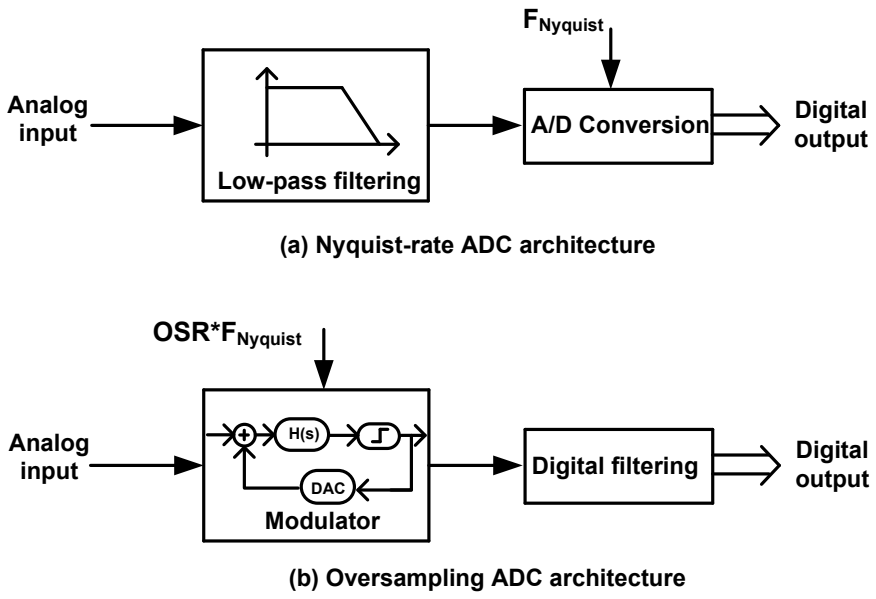


Figure 5 Basic A/D conversion architectures

The sampling frequency of oversampled ADCs is much higher than the Nyquist sampling rate. The power of the quantization noise that originates from analog-to-digital conversion process spreads from DC to $F_s/2$. Therefore, the in band quantization noise power of the oversampling ADC is reduced by the oversampling ratio (OSR). For example, an oversampling ratio of 2 produces a 3-dB improvement in the signal-to-quantization-noise ratio. Spreading of quantization noise power in an oversampling ADC is exemplified in Fig. 6. Oversampling ratio is expressed in terms of sampling frequency and input signal bandwidth as $OSR = F_s/2*F_{Sig}$.

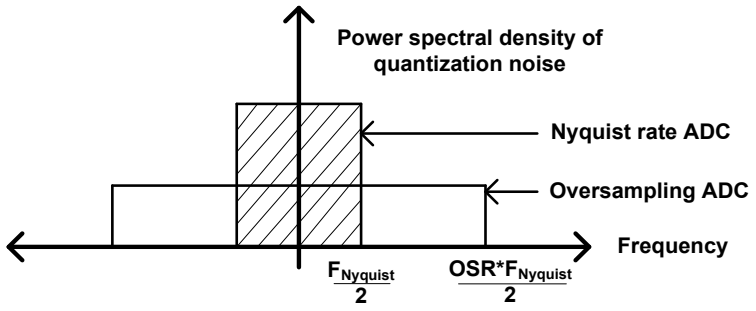


Figure 6 Power spectral density of quantization noise for different ADC architectures

2.2 Ideal sigma-delta modulator

Oversampling and noise-shaping are the basic principles involved in the operation of sigma-delta analog-to-digital converters. The oversampling spreads the quantization noise over the entire sampling frequency and hence reduces the quantization noise floor in the signal bandwidth. The sigma-delta operation shapes the quantization noise such that the in-band noise is decreased while the out-of-band noise is increased. The conceptual diagram of ΣΔ modulator is shown in Fig. 7. It consists of a loop filter followed by a quantizer, with a digital-to-analog converter (DAC) completing the negative feedback loop.

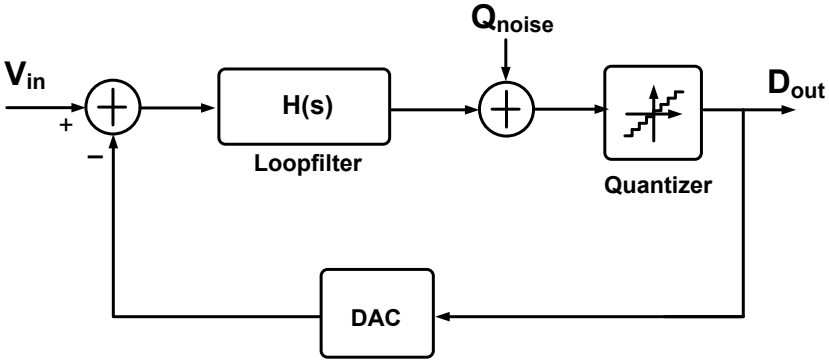


Figure 7 Block diagram of ideal sigma-delta modulator

The quantization noise (Q_{noise}) is assumed as random or white noise which is additive. For small signal analysis of ΣΔ modulator, a linear model is used and a unity gain transfer function is assumed for DAC and quantizer blocks. H(s) represents the transfer function of the loop filter, therefore, the signal transfer function (STF) and noise transfer function (NTF) of the ΣΔ modulator are given in equations (2.4a) and (2.4b) respectively. Therefore, the modulator output (D_{out}) can be expressed as given in equation (2.4c).

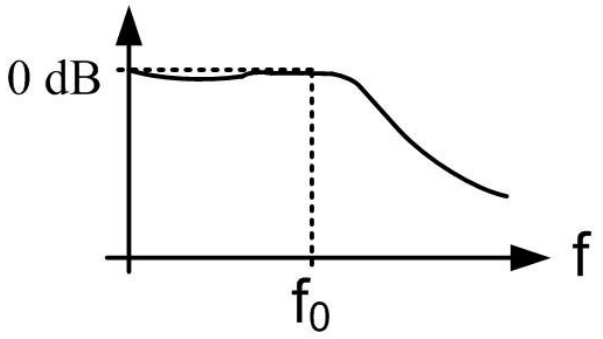
$$\mathrm{STF} = \frac{D_{out}}{V_{in}} = \frac{H(s)}{1 + H(s)} \tag{2.4a}$$

$$\mathrm{NTF} = \frac{D_{out}}{Q_{noise}} = \frac{1}{1 + H(s)} \tag{2.4b}$$

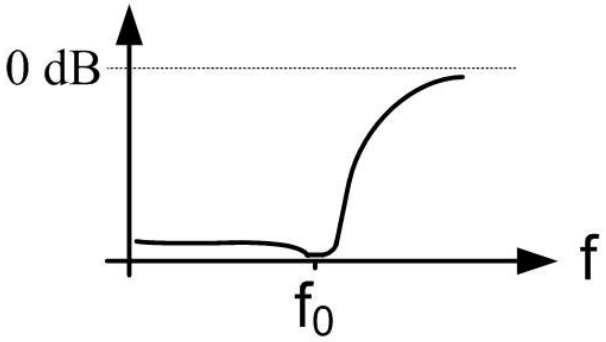
$$D_{out} = \mathrm{STF} * V_{in} + \mathrm{NTF} * Q_{noise} \tag{2.4c}$$

In case of a lowpass ΣΔ modulator, a lowpass filter transfer function that provides high passband gain is used as H(s). The plots of STF and NTF transfer functions of ΣΔ modulator employing a lowpass filter are depicted in Fig. 8a and Fig. 8b respectively.

Some of the important advantages of the sigma-delta ADCs can be summarized as follows. Since major portion of the sigma-delta ADC contains digital circuits, their integration with other digital circuitry becomes easy and the cost of implementation reduces. By nature, the sigma-delta modulators provide inherent anti-aliasing due to high oversampling ratio and inherent filtering. High resolution can be achieved using sigma-delta ADCs by exploiting the noise shaping characteristics of the modulator. Importantly, the noise shaping can be obtained without affecting the STF. These advantages make the sigma-delta modulators a good choice for implementing wireless radios.



(a) Signal Transfer function (STF)

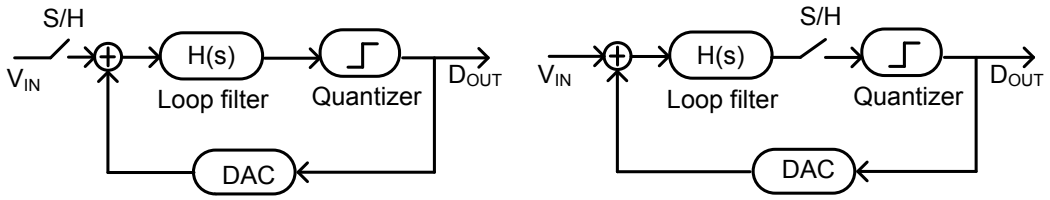


(b) Noise Transfer function (NTF)

Figure 8 Typical STF and NTF for a lowpass ΣΔ modulator

2.3 Continuous-time and discrete-time sigma-delta modulators

The sigma-delta modulators are classified into two types based on the location of the sample-and-hold (S/H) block. If the sampling operation is performed outside the sigma-delta loop the resulting modulator is called discrete-time modulator. And, if the sampling operation is performed inside the sigma-delta loop the resulting architecture is referred as continuous-time sigma-delta modulator. The loop filter of discrete-time sigma-delta modulators is implemented using switched-capacitor techniques and the loop filter of continuous-time sigma-delta modulator is implemented using continuous-time techniques. The conceptual diagrams of the discrete-time and continuous-time sigma-delta architectures are shown in Fig. 9a and Fig. 9b respectively.



(a) Discrete-time sigma-delta modulator (b) Continuos-time sigma-delta modulator

Figure 9 The discrete-time and continuous-time sigma-delta modulators

Switched capacitor (SC) circuits have been the dominant discrete-time (DT) techniques used for implementing the loop filters in SDMs. This is primarily due to the ease with which monolithic SC filters can be designed and their high-linearity. However, the amplifiers in SC filters require several time constants to settle and impose severe bandwidth requirements at high sampling frequencies [4], [5]. Therefore, continuous-time (CT) techniques have been introduced as an alternative for implementing loop filters for high bandwidth applications [6]. Sampling errors and out-of-band signals which alias into the passband are suppressed by the high in-band gain of the CT loop filter. The absence of sampling switches enables the circuit implementation of the CT filter in low-voltage technologies.

Besides the advantages with respect to large bandwidth and low-power consumption, CT loop filters are more difficult to design and simulate than SC filters. CT components show a higher variation with process-, supply-voltage, and temperature (PVT) spread. The linearity of the continuous time filters is limited due to the inherent non-linear behavior of MOS transistors. The conflicting requirements of low-power and low-noise makes filter design challenging at high frequencies. The over-sampling-ratio (OSR) of the ΣΔ modulator is traded with the order of the loop filter to achieve high signal-to-quantization-noise ratio (SQNR) at high sampling frequencies. This introduces other issues in terms of stability and excess delay in the ΣΔ modulator loop. Over the past few years of research in SDMs, it has been shown that CT implementation of ADCs can extend the input frequency range from a few hundreds of kilohertz up to a few tens of megahertz in a very power efficient manner [7]-[12].

The advantages of continuous-time sigma-delta modulators over their discrete-time counterparts make them good candidates for future wireless communications [13], [14]. The sampling errors of the sample and hold (S/H) circuit are shaped as the quantization noise since the S/H is placed inside the loop. Also, the CT filter implementation suits well for the high frequency applications, as the sampling frequency is not limited by the charge transfer accuracy requirements. By nature, CT sigma-delta modulators are not sensitive to settling behavior. Contrary to CT modulators, in a DT modulator, large glitches appear on the op-amp virtual ground node of op-amp-RC integrators due to switching transient. Hence, the CT modulator achieves better linearity performance. Further to this, when the sigma-delta modulator is integrated into a complete wireless transceiver in baseline CMOS, glitches generated in DT modulators can potentially couple to other critical blocks of the receiver, such as voltage-controlled oscillators (VCO), LNA and mixers, and can seriously degrade the receiver sensitivity. However, the clock jitter of the feedback DAC in CT sigma-delta modulators is a main issue at high sampling frequency. Multi-bit sigma-delta implementations can circumvent this problem to certain extent.

The continuous-time modulator is obtained by replacing the discrete-time loop filter by continuous-time one. Therefore, the two modulators behave exactly the same. The mapping between CT and DT domain usually employs the impulse invariant transformation as we require the open loop impulse response to be similar [6]. This transformation maps the frequencies linearly from $-\pi/(2T_s)$ to $\pi/(2T_s)$ while other frequencies will be aliased. The z-domain transfer function of the loop filter is transformed into to s-domain transfer function for realizing the continuous-time filter. The impulse invariant transformation ensures that the properties of both the structures are the same in terms of performance.

2.4 Non-idealities in continuous-time sigma-delta modulators

The functionality of ideal ΣΔ modulator described in previous section shows that high-dynamic range can be achieved using higher-order loop filter which provides sufficient pass-band gain that suppresses the in-band quantization noise. However, there are certain non-ideal effects to be considered with regards to circuit implementation. Some of the critical non-idealities of continuous-time sigma-delta modulators include circuit noise, distortion, component mismatches, clock jitter and excess loop delay.

2.4.1 Circuit noise

In practical CMOS circuit implementations, noise is introduced by active transistors and passive resistors. For high frequency and high bandwidth applications the thermal noise of transistors and resistors plays a crucial role in determining dynamic range performance. Since the loop filter is the very first block in the forward path of sigma-delta modulator, its nonidealities appear directly at the output spectrum. Similarly, the noise introduced by the feedback DAC is not shaped by the loop. The noise of loop filter and feedback DAC can be represented using the equivalent voltage noise sources $V_{n,filter}$ and $V_{n,DAC}$ respectively as shown in Fig. 10.

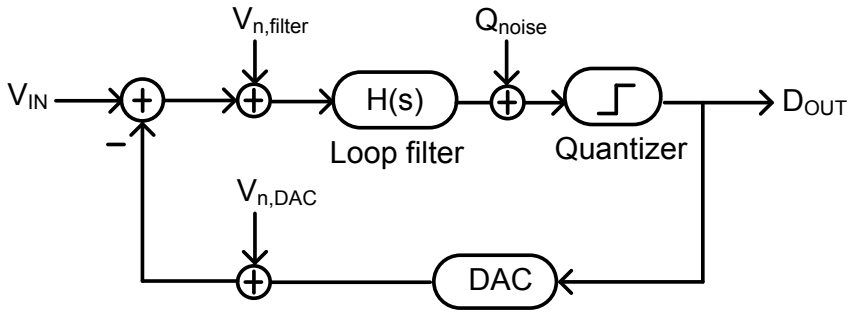


Figure 10 Model of sigma-delta modulator with important noise sources

Assuming that the quantizer and the DAC provide linear gain of one, the total input referred noise can be expressed as given in equation (2.5).

$$V_{n,in} = \frac{H(s)}{1+H(s)} V_{n,filter} + \frac{H(s)}{1+H(s)} V_{n,DAC} + \frac{1}{1+H(s)} Q_{noise} \quad (2.5)$$

From equation (2.5), it can be seen that the quantization noise (Q_{noise}) is shaped by the loop gain. However, the noise of the loop filter and feedback DAC see the same transfer function as that of the input signal (STF). Therefore, it is important to minimize circuit noise and distortion from filter and the feedback DAC. Other noise may come from clock jitter and power supply. For optimum dynamic range performance, the total circuit noise contribution must be less than the quantization noise floor of the ΣΔ modulator.

2.4.2 Non-linearity

The inherent nonlinearities present in circuits introduce harmonic distortion in band and degrade the dynamic range of the ADC. Fully differential circuit implementations can eliminate even-order harmonics and the third order harmonic distortion is the most significant. The major contribution of distortion comes from the non-linear behavior of transistors in the loop filter. Any non-linearity of the loop filter directly appears at the output of the modulator as inter-modulation components. Increasing the saturation voltage of the input transistors reduces the distortion as much as possible. However, it will only help to some extent and is only valid for transistor operating in strong inversion. The suppression of harmonic distortion means increasing the linear range of operation of transistors which demands more power.

Nonlinearity of integrators used in the realization of the loop filter is one of the major factors limiting the achievable SNR of CT ΣΔ ADC. The linearity requirements of the first stage of the filter are more critical for the overall performance of the modulator. DAC mismatch errors become another major source of nonlinearity in CT ΣΔ

modulators that use multi-bit quantization. The non-linearity of the DAC and first stage of filter are most critical because they are added directly to the input signal.

2.4.3 Component mismatches

The component mismatches change the frequency response of the loop filter transfer function in sigma-delta modulator. In case of a continuous-time filter, the location of poles and zeros is determined by the product of resistors and capacitors. However, RC product varies with process and temperature variations. Typically, a tuning circuitry and calibration scheme are used to achieve high resolution. Multi-bit quantizers are employed in sigma-delta modulators to improve the modulator resolution, to improve stability with higher order loop filters and to reduce clock jitter sensitivity. However, multiple levels of the quantizer can introduce non-linearity due to mismatches. Component mismatch errors between multiple DAC elements will directly appear at the input of the modulator without any noise shaping.

2.4.4 Excess loop delay

In a sigma-delta modulator the output of the quantizer drives the feedback DAC and the output of the DAC is fedback to the input of the filter. However, the transistors in DAC and comparator have finite response time. Therefore, there is a finite amount of delay from the sampling clock edge to the change in the output at the feedback node. This delay is commonly referred as excess loop delay and it is significant in continuous-time sigma-delta modulators. Excess loop delay changes modulator transfer function characteristics and affects the stability and dynamic range performance. Excess loop delay is a major concern in high frequency, large bandwidth sigma-delta modulators. Tunability can be incorporated into the coefficients of the loop filter to combat with the excess loop delay. The plot shown in Fig. 11 demonstrates the SNR degradation due to

excess loop delay in CT ΣΔ ADCs. As it can be seen from figure, the system becomes sensitive to excess loop delay variations greater than ±6% of the sampling time period.

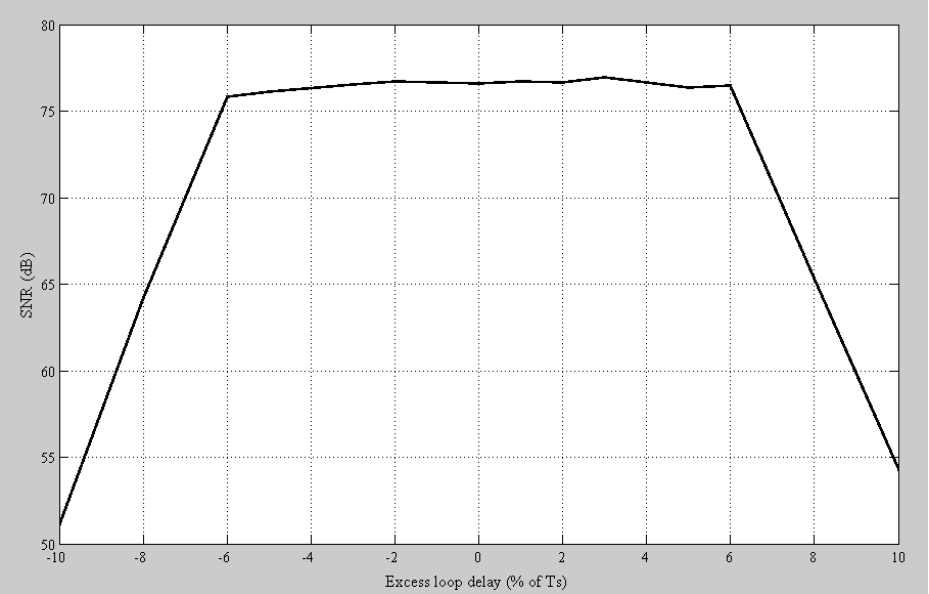


Figure 11 SNR degradation due to excess loop delay in CT ΣΔ ADC

2.4.5 Clock jitter

In continuous sigma-delta modulators the feedback mechanism is commonly implemented as integration of the feedback signal over a finite-time window. In most of the cases the feedback DAC produces rectangular current or voltage pulses. Any variation in the duty-cycle of the pulses appears as finite error in the integration. Since the clock jitter causes a random variation in the pulse width of the DAC, it adds a random phase noise to the output bit stream of the modulator. In other words, the timing uncertainty in the sampling clock causes an amplitude error in the continuous-time signal. However, this problem is not severe in discrete-time sigma-delta modulators based on switched capacitor filters. This is because of the exponential change transfer that happens between two capacitors in a given time window. Therefore, the clock jitter is a critical issue in sigma-delta modulators. The effect of jitter can directly be related

with the number of clock transitions required for producing DAC's output. Therefore, feedback DACs employing return-to-zero (RZ) mechanism produce low dynamic range performance as compared with the non-return-to-zero (NRZ) DACs. An analytical expression for upper limit to SNR due to jitter for a continuous-time sigma-delta modulator with Non-Return-to-Zero DAC is given below,

$$\mathrm{SNR} = 10.\log\left[\frac{V_{in}^2.\,\mathrm{OSR}.\,2^{2N}.\,T_s^2}{8.\,\alpha.\,\sigma_t^2}\right] \tag{2.6}$$

where, V_{in} is the amplitude of the input signal, α is the value which describes the quantization error variation, OSR is the oversampling ratio, N is the number of quantization levels and jitter is assumed to be Gaussian random process with the standard deviation σ_t and the spectrum of the jitter is white. As the sampling frequency increases, the clock jitter becomes the dominant limit in the SNR performance of the ADC. And, SNR becomes proportional to OSR rather than OSR^{2N}. SNR degradation due to the effect of increase in the jitter standard deviation in CT ΣΔ ADC is shown in Fig. 12.

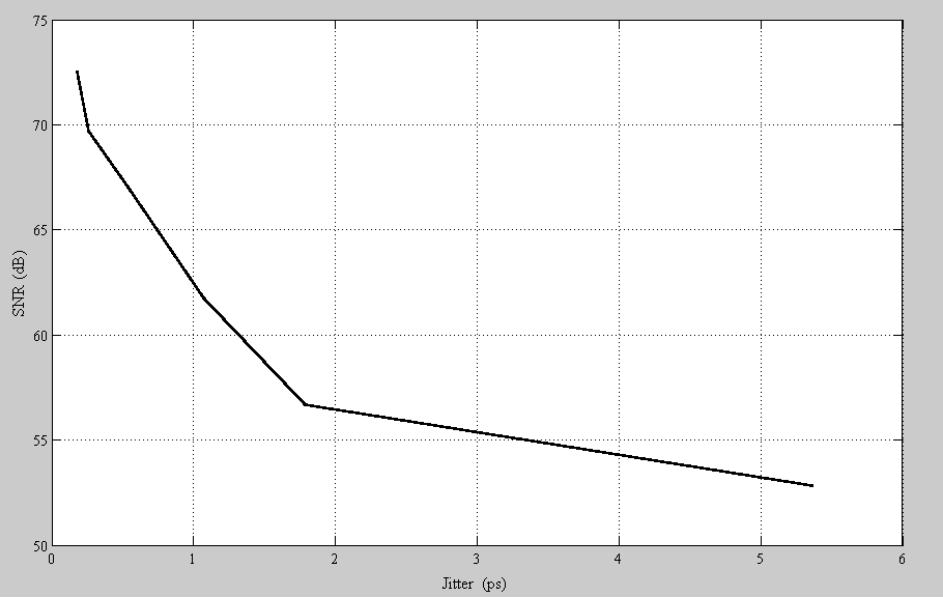


Figure 12 SNR degradation due to the effect of jitter in CT ΣΔ ADC

2.5 Performance parameters of sigma-delta modulators

The performance of Nyquist rate ADC's is measured using time-domain statistical parameters like differential nonlinearity (DNL), integral nonlinearity (INL) etc. However, these errors have no practical meaning when it comes to oversampling sigma-delta modulators. The most important specification of sigma-delta modulators includes dynamic range, signal-to-noise-and-distortion-ratio, dynamic range and power consumption.

2.5.1 Signal-to-noise-and-distortion ratio (SNDR)

SNDR is the ratio of the maximum signal power to the total noise and distortion power in a specific band. In an ideal sigma-delta modulator, the total noise and distortion power is equal to the quantization noise power. However in practical circuit implementation the performance is degraded by the circuit noise and nonlinearity. The main noise contribution comes from thermal noise and flicker noise of transistors and other noisy elements. The nonlinear nature of circuits generates harmonics that can degrade the performance when they fall in band. The noise and distortion can be separately quantified using two different parameters signal-to-noise ratio (SNR) and signal-to-distortion ratio (SDR). For optimum performance, a good balance between SNR and SDR needs to be maintained in the design of sigma-delta modulator [15].

2.5.2 Dynamic range (DR)

The dynamic range of a sigma-delta modulator is defined as the ratio of the maximum input signal to the minimum input signal that can be applied. It is often specified as the resolution of the sigma-delta ADC. The relation between the dynamic range and resolution of a modulator is expressed as

$$\text{Resolution (in bits)} = (\text{DR(in dB)} - 1.76)/6.02 \tag{2.7}$$

3. DESIGN OF CONTINUOUS-TIME SIGMA-DELTA MODULATOR

This section presents the details of the system level design of 12-bit resolution, 25MHz signal bandwidth continuous-time low-pass sigma-delta ADC. The important system level considerations that affect the stability of the modulator are considered for determining the transfer function of the open loop filter transfer function. An overview of the implementation of system is presented together with the behavioral simulation results.

3.1 Introduction

The architecture of the continuous-time sigma-delta modulator mainly determines its performance. The important architectural level choices include order of the loop filter, single-loop or cascaded architectures, and, single-bit or multi-bit quantizer. Higher order sigma-delta modulators are more suitable for high-frequency, high-resolution applications because they relax the over-sampling requirements. A single loop implementation consumes less power than cascaded architectures. And, cascaded modulators need a precise matching between the analog and digital coefficients. Multi-bit implementation of the quantizer increases the SNR (6dB per each quantizer bit), but it may suffer from mismatches in the feed-back DAC. System level design of the sigma-delta modulator involves determining the loop transfer function, finding the proper loop topology and modeling various non-ideal effects to determine the specifications for each building block. In this work, a 5^{th} order, single-loop and 3-bit quantizer architecture is chosen for the implementation of 25MHz bandwidth, 12-bit resolution continuous-time low-pass sigma-delta ADC.

3.2 Loop filter transfer function

The most common method to design a CT modulator is to first find the equivalent DT modulator loop filter and then transform it to continuous-time using impulse invariant transformation [16]. However, the design of loop filter transfer function of a continuous-time sigma-delta modulator has a strong dependence on the pulse shape of the feedback DAC. The analog loop filter used in continuous-time sigma-delta modulators requires large dynamic range due to significant peak to average ratio of the resulting signals [17]. Sigma-delta modulator with L^{th} order noise transfer function (NTF) given by $(1-z^{-1})^L$ can achieve dynamic range (DR) given by

$$\mathrm{DR\ (in\ dB)} = 10 * \log_{10}\left[\frac{3}{2}\frac{(2\mathrm{L}+1)\mathrm{OSR}^{2\mathrm{L}+1}}{\pi^{2\mathrm{L}}}\right] + 6.02 * (\mathrm{N}-1) \tag{3.1}$$

where, OSR is the oversampling ratio, L is the order of the modulator and N represents the number of bits in quantizer. For the desired wideband, high resolution modulator, the noise transfer function is more complex. And, the above equation gives a qualitative guidance on selecting the system parameters - OSR, L and N. Based on extensive MATLAB simulations, a fifth order, 3-bit topology is chosen with OSR of 8.

The transfer function of the loop filter is chosen to have Chebyshev type I response with order 5, peak-to-peak ripple equal to 0.5dB and pass-band edge frequency 24MHz. The Chebyshev type I response provides sharp pass-band to stop-band transition which is very important for suppressing the quantization noise in ΣΔ modulators. The pass-band of the Chebyshev type I filter exhibits equiripple behavior. The order of the filter is equal to the number of reactive components needed to realize the filter. Elliptic filters provide even steeper roll-off by allowing ripple in the stop-band. This will however result in less suppression of quantization noise in the stop-band. The open loop filter transfer function used in low-pass ΣΔ ADC to achieve a SQNR of 75dB with 25MHz bandwidth in SIMULINK is given in equation (3.2).

$$H(z) = \frac{1.838\,z^{-1} - 4.992\,z^{-2} + 5.781\,z^{-3} - 3.137\,z^{-4} + 0.7227\,z^{-5}}{1 - 4.503\,z^{-1} + 8.295\,z^{-2} - 7.802\,z^{-3} + 3.744\,z^{-4} - 0.7331\,z^{-5}} \quad (3.2)$$

A simplified model of the continuous time sigma-delta modulator is shown in Fig. 13 using z-domain transfer function. K_{DAC1} and K_{DAC2} are the primary and secondary feedback DAC coefficients. H(z) represents the open loop filter transfer function. Modeling the quantization error as an input independent additive white noise, the system becomes linear and a small signal analysis can be used to describe the system behavior. Therefore, the input to output voltage transfer function is obtained as

$$\frac{V_{OUT}}{V_{IN}} = \frac{H(z)}{1 + z^{-1}[K_{DAC\,1}H(z) + K_{DAC\,2}]} \quad (3.3)$$

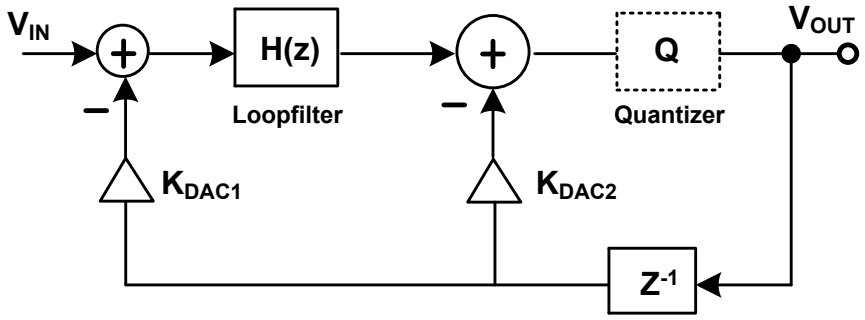


Figure 13 Simplified model of the continuous time sigma-delta modulator

The stability of the loop depends on the loop gain term in the denominator given by equation (3.4). Using equation (3.2) the loop gain can be computed as

$$\text{Loop gain} = G(z) = z^{-1}[K_{DAC\,1}H(z) + K_{DAC\,2}] \quad (3.4)$$

$$G(z) = z^{-1}\frac{0.5 - 0.413z^{-1} - 0.845z^{-2} + 1.88z^{-3} - 1.26z^{-4} + 0.35z^{-5}}{1 - 4.50z^{-1} + 8.29z^{-2} - 7.80z^{-3} + 3.74z^{-4} - 0.73z^{-5}} \quad (3.5)$$

The Bode magnitude and phase response plots of the loop gain and open loop filter transfer function are shown in Fig. 14. The plot shows a phase margin of approximately 145 degrees and a gain margin of -18.5 dB.

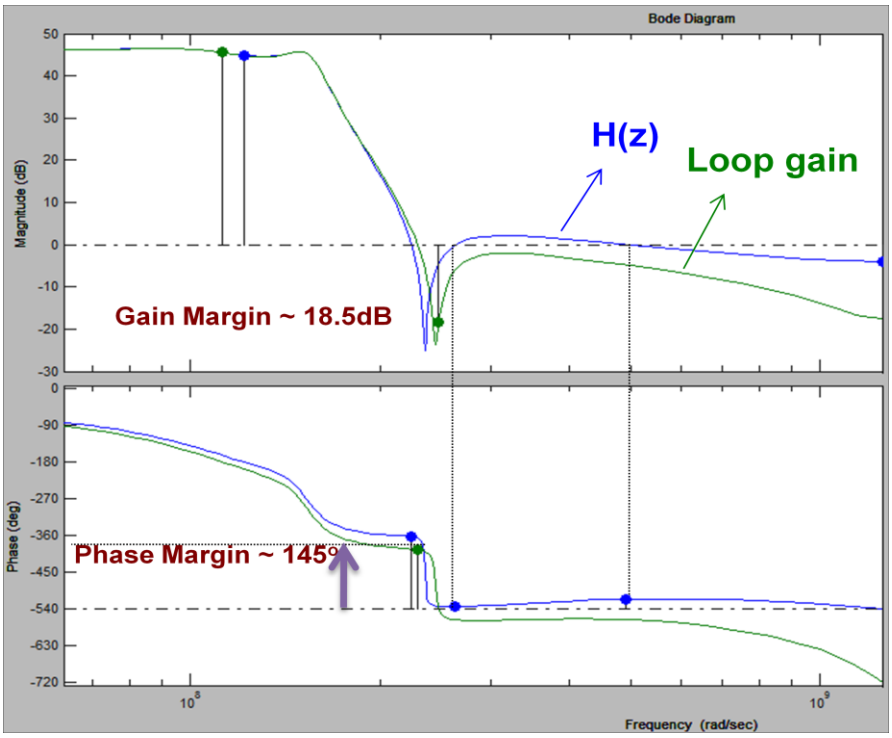


Figure 14 Bode plot showing H(z) and Loop gain, G(z)

3.3 Modulator loop topology

The commonly used loop filter architectures for single stage modulators are of two kinds. One is cascade of integrators with distributed feed-back (CIFB) and the other is cascade of integrators with feed-forward summation (CIFF). The CIFB topology requires multiple DACs feeding back to the input of each integrator stage. Whereas, the CIFF topology requires only two accurate DACs and an additional summing stage to perform feed-forward summation of integrator outputs. However, the CIFB topology

offers better anti-aliasing behavior and is less susceptible to peaking in the signal transfer function.

The feed-forward architecture offers several advantages when compared to the feedback architecture. The signal swing at the internal nodes of the modulator is relaxed in case of feed-forward architecture. The performance requirements of the later stages can be relaxed when compared to the requirements of the former stages in feed-forward architecture. This helps in reducing the power consumed by the non-critical blocks. Therefore, the selection of the modulator loop topology greatly affects the circuit implementation of the loop filter. A feed-forward topology is selected for the implementation of the continuous-time sigma-delta modulator. The s-domain transfer function of the loop filter is obtained as equation (3.6) from impulse invariant transformation of the z-domain transfer function.

$$H(s) = \frac{5.25e6\,(s^2 + 3.842e8\,s + 8.821e16)(s^2 + 1.606e5\,s + 5.567e16)}{(s + 3.58e7)(s^2 + 6.78e7\,s + 1.1e16)\,(s^2 + 2.04e7\,s + 2.37e16)} \quad (3.6)$$

The transfer function of the 5th order loop filter can be simplified to obtain 2nd order and 1st order transfer functions for ease of implementation. The complete filter transfer function is realized as the sum of three different filter blocks with feed-forward summation. Assuming that the operational amplifiers are ideal, the transfer function of the loop filter can be expressed as

$$H(s) = K_1\left(\frac{A_1\frac{s}{\omega_{01}} + A_2}{1 + \frac{s}{\omega_{01}Q_1} + \frac{s^2}{\omega_{o1}^2}}\right) + K_2\left(\frac{K_1}{1 + \frac{s}{\omega_{01}Q_1} + \frac{s^2}{\omega_{o1}^2}}\right)\left(\frac{A_3\frac{s}{\omega_{02}} + A_4}{1 + \frac{s}{\omega_{02}Q_2} + \frac{s^2}{\omega_{o2}^2}}\right) \quad (3.7)$$

$$+ K_3\left(\frac{K_1}{1 + \frac{s}{\omega_{01}Q_1} + \frac{s^2}{\omega_{o1}^2}}\right)\left(\frac{K_2}{1 + \frac{s}{\omega_{02}Q_2} + \frac{s^2}{\omega_{o2}^2}}\right)\left(\frac{A_5}{1 + \frac{s}{\omega_{o3}}}\right)$$

where ω_{o1}, ω_{o2} and ω_{o3} are the cut-off frequencies of each filter stage. Q_1 and Q_2 represent the quality factor of first and second biquadratic sections. K_1, K_2 and K_3

represent the low frequency gains of each stage. The coefficients A_1, A_2, A_3, A_4 and A_5 are realized as ratio of resistors performing weighted addition of the outputs of the integrators. Table 1 summarizes the coefficient values.

Table 1 Various parameters used in the realization of the filter transfer function

Coefficient	Value	Coefficient	Value
ω_{01}	$2\pi \times 24.5 \times 10^6$	K_3	7.7
ω_{02}	$2\pi \times 16.7 \times 10^6$	A_1	0.5685
ω_{03}	$2\pi \times 5.71 \times 10^6$	A_2	1.0369
Q_1	7.5	A_3	0.5953
Q_2	1.55	A_4	0.7611
K_1	6	A_5	0.8743
K_2	6		

3.4 Overview of system implementation

The system level block diagram of continuous-time lowpass sigma-delta (CT LP ΣΔ) ADC is shown in Fig. 15. Multiple feed-forward architecture is employed in the loop filter and two accurate feedback DACs are required in the feedback path [18]. The forward path consists of a fifth order Chebyshev lowpass filter and a three-bit quantizer to guarantee the desired signal-to-quantization-noise ratio (SQNR). The output of the quantizer is a digitized version of the filter's output with an embedded half-period delay ($z^{-1/2}$). The output digital bit stream is in voltage mode and the programmable delay block provides another $z^{-1/2}$ delay to complete the full one period delay required in the loop. The digital output, D_{out}, in voltage mode is converted into current by a time-variant single bit DAC and injected back into the filter to close the negative feedback loop. The multi-phase DAC uses a single unit element avoiding the mismatch errors that are common in multi-element implementations. However, the multi-phase DAC demands an accurate clock with low jitter performance. Hence, an LC-tank oscillator with injection-

locked frequency divider is implemented to provide a built-in reference clock with low phase noise. A secondary feedback DAC is employed to enhance the tolerance to the excess loop delay [9]. The delay in the secondary feedback loop formed by the summing amplifier, quantizer and the secondary DAC is critical for the stability of the system. Therefore, the summing amplifier needs to be very fast and demands more power. The group delay of the summing amplifier is enhanced by the introduction of a zero-pole pair in its feedback network. The important system level design parameters for low-pass ΣΔ ADC are presented in Table 2.

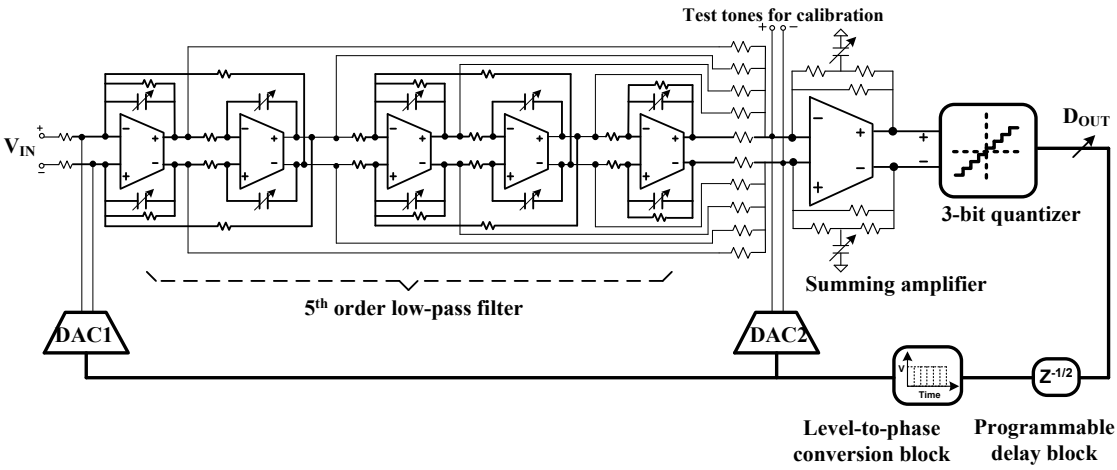


Figure 15 System level block diagram of CT LP ΣΔ ADC

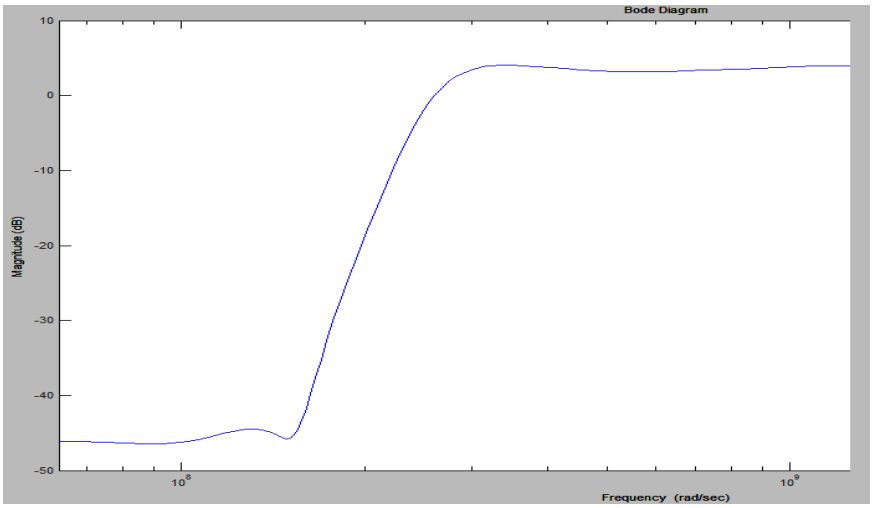
Table 2 System level design parameters for low-pass ΣΔ ADC

Design parameter	Value
Signal bandwidth	25 MHz
Sampling frequency	400 MHz
Over-sampling ratio (OSR)	8
Order of noise shaping	5^{th} order
Quantizer resolution	3 bits
Supply voltage	1.8 V
Targeted resolution	12 bits
CMOS Technology	0.18μm

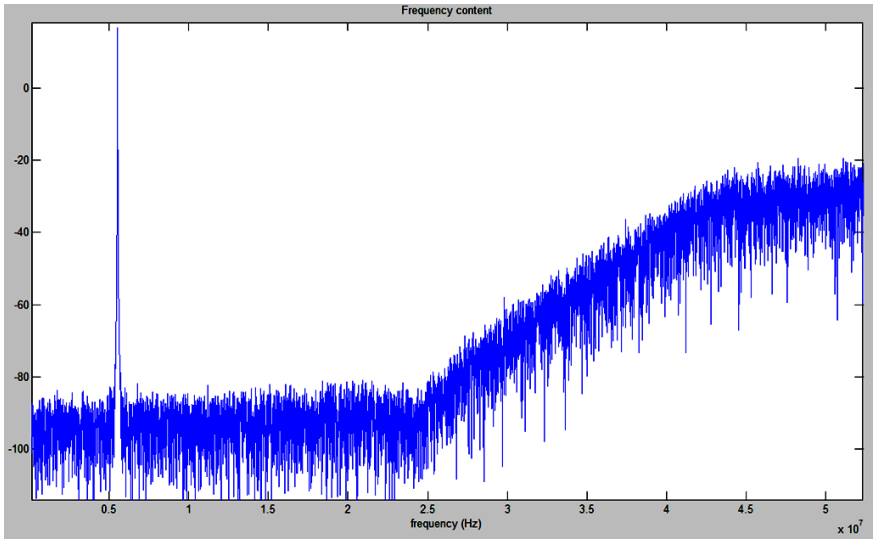
3.5 Behavioral simulations of the system

The expected NTF of the ADC and its output spectrum obtained from the 3-bit output data are shown in Fig. 16a and Fig. 16b respectively. The input signal is a sine wave at 5.533 MHz and the sampling frequency is 400 MHz. The measured SQNR at the output of the ADC is 74dB in 25MHz signal bandwidth. The SNR was calculated for 65536 samples and a step size of $T_s/20$ (T_s is the time period of the sampling clock) is used for simulating the model, which ensures good accuracy for behavioral simulations.

One of the major challenges in the design of high performance CT LP ΣΔ ADCs is the design of analog loop filter. In this case, demanding high-performance analog filters are needed to shape the in-band quantization noise and improve the overall SNDR of the system. The summing amplifier block is another critical block for the high speed operation. It needs large bandwidth to guarantee stability of the system by compensating for the excess loop delay introduced by the analog loop filter. This work mainly focuses on the implementation of the analog loop filter for 12-bit resolution 25MHz bandwidth CT LP ΣΔ ADC.



(a) NTF of ADC



(b) Output spectrum of ADC

Figure 16 The NTF and the output spectrum of the CT LP SD ADC

4. DESIGN OF G_m-C BIQUADRATIC FILTER

This section presents the theory and simulation results of the G_m-C band pass filter designed for high-performance continuous-time applications. The linearity and noise performance of the OTA and the biquadratic cell are analyzed in a detailed manner. The simulation results of the G_m-C biquad designed to operate at a center frequency of 100MHz and a quality factor of 10 are presented. Some important mathematical relations concerning noise and linearity of the G_m-C biquadratic structure are presented. It is shown that the linearity of the biquad depends on the frequency separation between the input-tones used for IM3 measurement. It is also shown quantitatively that the input referred noise power of the biquad is approximately 3 times that of the stand-alone OTA at the center frequency of the biquad.

4.1 G_m-C integrator

Integrators are the basic building blocks used in continuous-time and discrete-time filters. G_m-C is the most popular technique used to implement integrators in high-frequency continuous-time filters. G_m-C integrators have robust stability due to their open-loop operation [19]. Integrators used in high speed continuous-time applications have small load capacitors and large transistors with high transconductance (ω_o is proportional to g_m/C). Therefore, parasitic capacitance can be a significant portion of the total capacitance value. As a result, the time constant of the integrator is sensitive to process and temperature variations.

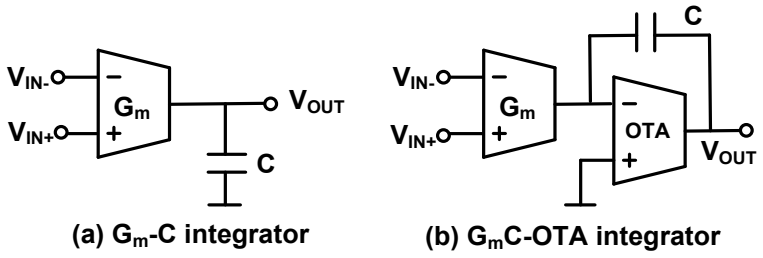


Figure 17 Popular G_m-C integrator architectures

Two popular G_m-C integrator structures employed in high frequency continuous time filters are shown in Fig. 17. The basic G_m-C integrator which is obtained by loading a transconductor with a capacitor at the output is shown in Fig. 17a. Assuming that the G_m-cell has very high output impedance and the parasitic capacitance at the output node is negligible compared to the load capacitance, the voltage transfer function of the circuit is obtained as

$$\frac{V_{OUT}}{V_{IN+} - V_{IN-}} = \frac{g_m}{sC} \tag{4.1a}$$

If g_o is the finite output impedance and C_p is parasitic capacitance at the output node, the transfer function is obtained as

$$\frac{V_{OUT}}{V_{IN+} - V_{IN-}} = \frac{g_m}{g_o} \frac{1}{1 + s\left(\frac{C + C_p}{g_o}\right)} \tag{4.1b}$$

Therefore, the low-frequency gain of the G_m-C integrator depends on the transconductance (g_m) and the finite output impedance ($r_o = 1/g_o$) of the transconductor. To increase the dc gain of the integrator without increasing the power consumption, it may be required to use some kind of cascoding at the output of the G_m-cell. However, with the reduction in power supply voltages cascoding may reduce the output voltage swing capability of the integrator. Further to this, the time constant of G_m-C integrator is sensitive to parasitic capacitances.

Fig. 17b shows another version of integrators used in continuous time applications namely, G_m-C-OTA integrators. Some of the issues associated with G_m-C integrators can be overcome in G_m-C-OTA integrators, in which a virtual ground is formed at the output of a linear transconductor stage. The capacitor connected in a feedback loop around one OTA creates a virtual ground at the output of the other OTA [20]. With this technique the transconductor does not need to have any significant output voltage swing capability. And, cascoding at the output is not necessary because the DC gain is provided by the two cascaded stages. Furthermore, the integrator time constant is not affected by the parasitic capacitances at the output of the transconductor.

The G_m-C-OTA approach is very similar to the conventional Opamp-RC technique. But, the key difference is that it is not necessary to drive any resistive load. So, a simple OTA can be used to drive the integrating capacitor. On the other side, this technique requires extra power which is required by the additional OTA. Also, the OTA introduces excess phase which may not be tolerable for very high frequency filters. However, this topology can be advantageous in terms of the dynamic range and SNR at intermediate frequencies.

4.2. OTA architecture

The performance of a G_m-C biquad relies heavily upon the performance of the transconductor. For high performance continuous-time applications, good linearity and low noise are the critical specifications in designing the transconductor. A high frequency transconductor with good linearity, low-noise and high DC gain requirement uses relatively large transistors, thus increasing the parasitic capacitance at the critical nodes. For fully differential operation, a CMFB is also needed at each output which further increases the parasitics. As a result, the effective transconductance $G_{m,eff}$ has to be increased to obtain the desired center frequency of the biquad.

The G_m-C-OTA shown in Fig. 18 consists of a highly linear G_m stage and an output OTA stage. The transconductor (G_m) stage is formed by the input NMOS transistor pair (M_1) loaded by a pair of PMOS transistors (M_2) with resistive (R_D) feedback to set the common-mode voltage. The value of R_D is chosen to be larger than the output resistance of the G_m stage in order not to decrease the differential output resistance. This arrangement makes it possible to have approximately unity common mode gain and hence no CMFB is required for this stage. The source degeneration resistor (R_S) is used to obtain good linearity for the G_m-stage. The linearity is further improved by using a non-linear source degeneration technique implemented with an auxiliary differential pair that is a scaled copy of the main G_m stage. Also, the voltage swing at node V_{INT} of the G_m stage is small which helps to achieve good linearity.

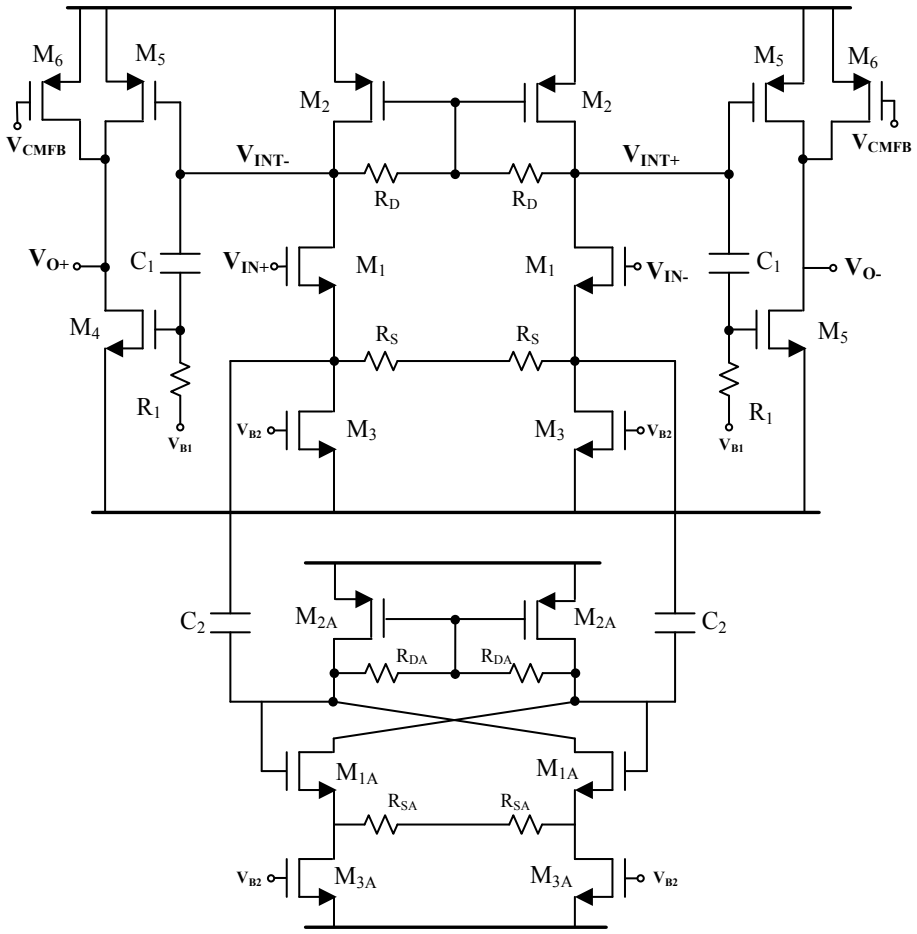


Figure 18 Circuit level implementation of the OTA

The OTA output stage (M_4, M_5 and M_6) mainly provides good output swing capability and enough DC gain to keep the voltage swing at V_{INT} as low as possible. The pseudo-differential operation of the OTA stage provides better large signal linearity performance. The output common-mode voltage is set by the common-mode feedback (CMFB) circuit which adjusts the current in the transistor M_6. The integrating capacitor is connected between the nodes V_{INT} and V_O (not shown in Fig.18). The capacitors C_1 and C_2 are used to isolate the DC bias points of the respective nodes. V_{B1} and V_{B2} are the bias voltages which are obtained using current mirror biasing. The transistor dimensions, resistor and capacitor values, and bias currents of the OTA are given in Table 3.

Table 3 Transistor dimensions, device values and bias conditions for OTA

Device	Dimensions	Device	Value
M_1	(48) 2µm / 900 nm	M_{3A}	(4) 4 µm / 600 nm
M_2	(24) 6 µm / 300 nm	R_D	80 KΩ
M_3	(24) 3 µm / 600 nm	R_S	350 Ω
M_4	(28) 3 µm / 400 nm	C_1	5 pF
M_5	(36) 6 µm / 300 nm	C_2	5 pF
M_6	(10) 6 µm / 300 nm	R_{DA}	1 KΩ
M_{1A}	(3) 2 µm / 300 nm	R_{SA}	350 Ω
M_{2A}	(4) 6 µm / 300 nm	R_1	10 K Ω

4.2.1 Noise analysis of G_m-C-OTA integrator

The input referred voltage noise density of the G_m-C-OTA integrator stage (shown in fig.16) is mainly dominated by the input G_m stage. The noise of the output (OTA) stage is attenuated by the gain of the first (G_m) stage. Hence, the main noise contribution comes from the noise of the G_m stage. The total input referred voltage noise density of the G_m stage can approximately be written as given in equation (4.2).

$$v_{n,in}^2 = \frac{i_{n,out}^2}{G_{m,eff}^2} \approx \frac{1}{G_{m,eff}^2}\left[2\left(i_{n,M_1}^2 + i_{n,M_2}^2 + i_{n,M_3}^2 + i_{n,R_D}^2 + i_{n,R_S}^2\right)\right] \tag{4.2}$$

In the above expression, $G_{m,eff}$ is effective transconductance of the G_m stage, i_n^2 stands for current noise density, and v_n^2 stands for voltage noise density. The output referred current noise densities from the devices M_1, M_2, M_3, R_D and R_S can be expressed as given equations (4.3a)-(4.3f).

$$i_{n,M_1}^2 = \frac{4KT\gamma}{g_{m1}} G_{m,eff}^2 \tag{4.3a}$$

$$i_{n,M_2}^2 = 4KT\gamma g_{m2} \tag{4.3b}$$

$$i_{n,M_3}^2 = 4KT\gamma g_{m3}\left(G_{m,eff}R_S\right)^2 \tag{4.3c}$$

$$i_{n,R_D}^2 = 4KT.\frac{1}{R_D} \tag{4.3d}$$

$$i_{n,R_S}^2 = 4KT.\frac{1}{R_S} \tag{4.3e}$$

$$G_{m,eff} = \frac{g_{m1}}{1 + g_{m1}.R_S} \tag{4.3f}$$

$$\therefore v_{n,in}^2 \approx 8KT\left[\frac{\gamma}{g_{m1}} + \gamma g_{m2}\frac{1}{G_{m,eff}^2} + \gamma g_{m3}{R_S}^2 + \frac{1}{R_S G_{m,eff}^2} + \frac{1}{R_D G_{m,eff}^2}\right] \tag{4.4}$$

where k is the Boltzmann constant, T the temperature in degrees Kelvin, γ is the noise coefficient, and g_{mi} is the small-signal transconductance of the transistor used as a current source. The total input referred noise of the OTA at 100MHz is obtained as 10.7nV/√Hz.

4.2.2 Linearity analysis of G_m-C-OTA

The linearity of the transconductance (G_m) stage is very important in G_m-C-OTA integrator shown in fig.18. The linearity of the OTA can be characterized using a two-tone test by measuring third-order inter-modulation distortion, IM3. Assuming all transistors are operating in saturation region, the large signal behavior of the output current of the source degenerated fully differential G_m stage can be obtained in terms of first and third order transconductance parameters (g_{m1} and g_{m3}) as below.

$$i_d = \frac{g_{m1}}{1 + g_{m1}.R_S} v_{in} + \frac{g_{m3}}{(1 + g_{m1}.R_S)^4} {v_{in}}^3 + \cdots \tag{4.5}$$

From equation (4.5), it is noted that the third order harmonic distortion (HD3) is,

$$HD3 = \frac{1}{16}\frac{g_{m3}}{g_{m1}}\left[\frac{1}{(1 + g_{m1}.R_S)^3}\right]{v_{in}}^2. \tag{4.6}$$

The saturation region square model approximation of the MOS transistor yields approximate equations for g_{m1} and g_{m3} [21] as below.

$$g_{m1} = \frac{1}{2}\frac{\sqrt{\mu_n C_{ox}(W/L)I_T}}{1 + \frac{2}{\varepsilon_{crit}}\sqrt{\frac{I_T}{WL\mu_n C_{ox}}}} \tag{4.7a}$$

$$g_{m3} = -\frac{1}{8}\frac{\sqrt{\mu_n C_{ox}(W/L)I_T}}{\left(\frac{I_T L}{W\mu_n C_{ox}}\right)\left(1 + \frac{2}{\varepsilon_{crit}}\sqrt{\frac{I_T}{WL\mu_n C_{ox}}}\right)^3} \tag{4.7b}$$

where μ_n and C_{ox} are process dependent mobility and oxide capacitance parameters; W and L are width and length of the input differential pair transistor; I_T is the tail current;

ε_{crit} is the critical electric field, and v_{DSAT} is the saturation voltage. An expression for IM3 can be computed as given in equation (4.8a).

$$\mathrm{IM3} \approx 3 \times \mathrm{HD3} = \frac{3}{16}\frac{g_{m3}}{g_{m1}}\left[\frac{1}{(1+g_{m1}.R_S)^3}\right]{v_{in}}^2 \tag{4.8a}$$

Therefore, the linearity of the transconductor can be improved by increasing the source degeneration resistor. However, the overall transconductance of the OTA decreases and results in increased noise levels. Also, the presence of the current source transistor M_3 changes the effective source degeneration resistor and hence the linearity of the OTA. Therefore, the IM3 can be expressed as,

$$\mathrm{IM3} = \frac{3}{16}\frac{g_{m3}}{g_{m1}}\left[\frac{1}{(1+g_{m1}.(R_S||r_{o3}))^3}\right]{v_{in}}^2. \tag{4.8b}$$

where r_{o3} is the output impedance of the current source transistor, M3. The non-linear source degeneration technique implemented with the auxiliary differential pair aims at cancelling the third order non-linearity of the transconductance cell [22]. Perfect cancellation of nonlinearities is difficult to achieve due to process and temperature variations.

4.2.3 OTA simulation results

The standalone OTA designed in 0.18µm CMOS technology consumes 10.5mW power with 1.8V power supply. A load capacitor of 2.8pF is connected across the second stage of the OTA and the unity gain frequency of the OTA is 100 MHz. Table 4 summarizes the simulation results for the OTA for 5 different process corners.

Table 4 Simulation results of the standalone OTA

Parameter	NOM	FAST	FASTSLOW	SLOWFAST	SLOW
DC gain (in dB)	54.7	53.96	55.1	53.9	55.25
GBW (in MHz)	100.7	104.61	103.25	98.04	97.66
Phase Error @ 100MHz	-0.314^o	+0.4^o	-0.77^o	+0.05^o	-0.95^o
IM3 @ $V_{out, p-p}$ = 400mV	-92 dB	-76.2dB	-83.08dB	-87.08dB	-87.7dB
Input referred Noise density @100MHz (in nV/√Hz)	10.7	10.68	10.57	11.05	10.89

AC magnitude and phase response of the OTA is presented in Fig. 19. The DC gain of the OTA is 54 dB and the unity gain frequency is 100MHz. Also, the phase error at 100MHz is found to be -0.31^o. The simulated linearity test of the OTA for 400 mV_{p-p} swing is shown in Fig. 20. The IM3 is -92 dB with two input tones applied at frequencies 99MHz and 101MHz.

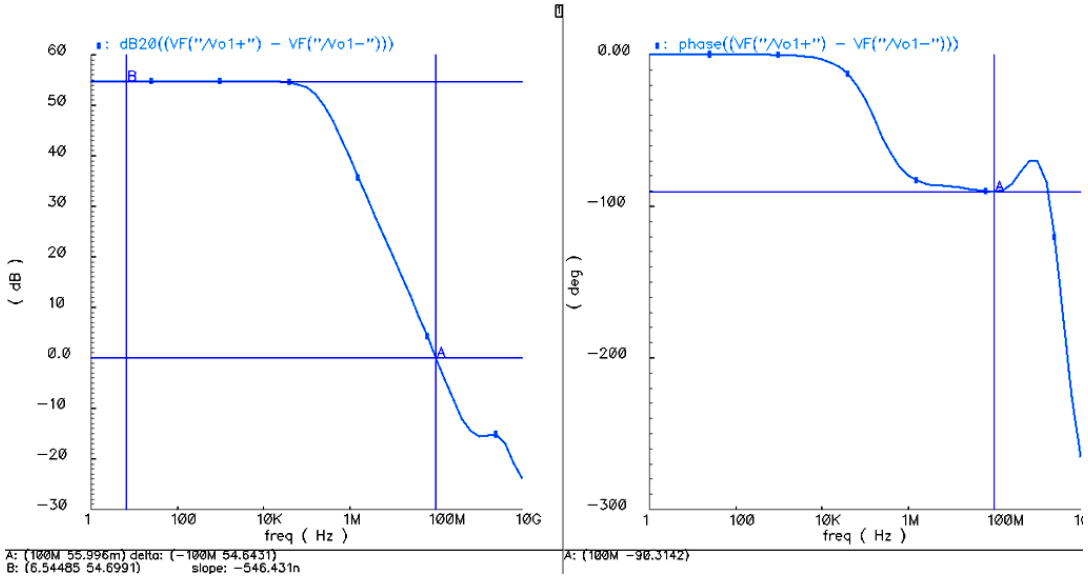


Figure 19 AC response showing DC gain and excess phase of the OTA

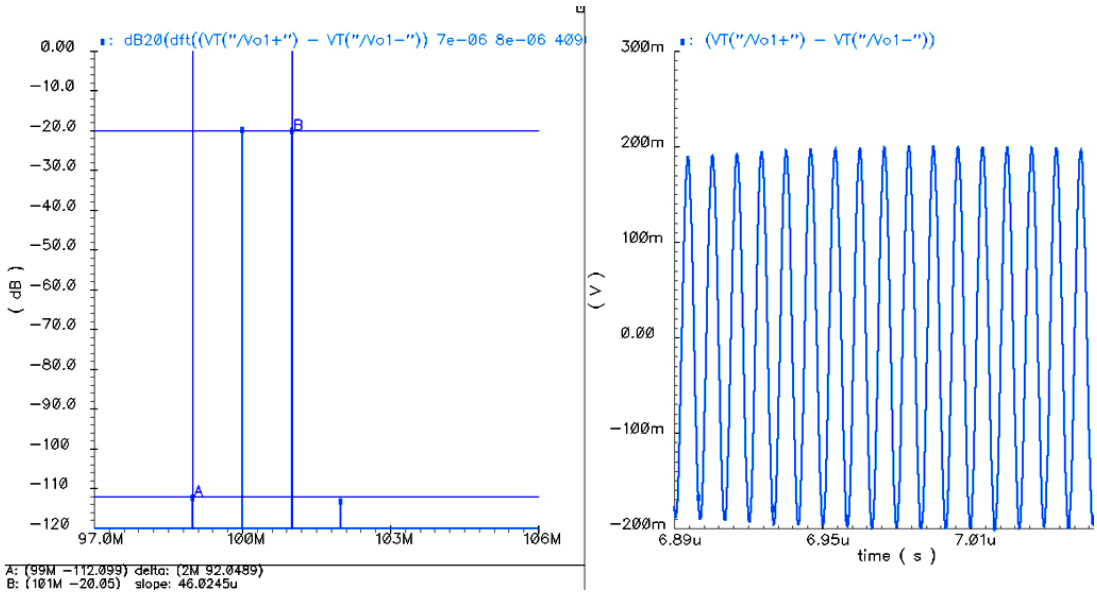


Figure 20 IM3 measurement for the standalone OTA

The input referred noise spectral density of the OTA is shown in Fig. 21. The thermal noise density is found to be 10.78nV/√Hz at 100MHz.

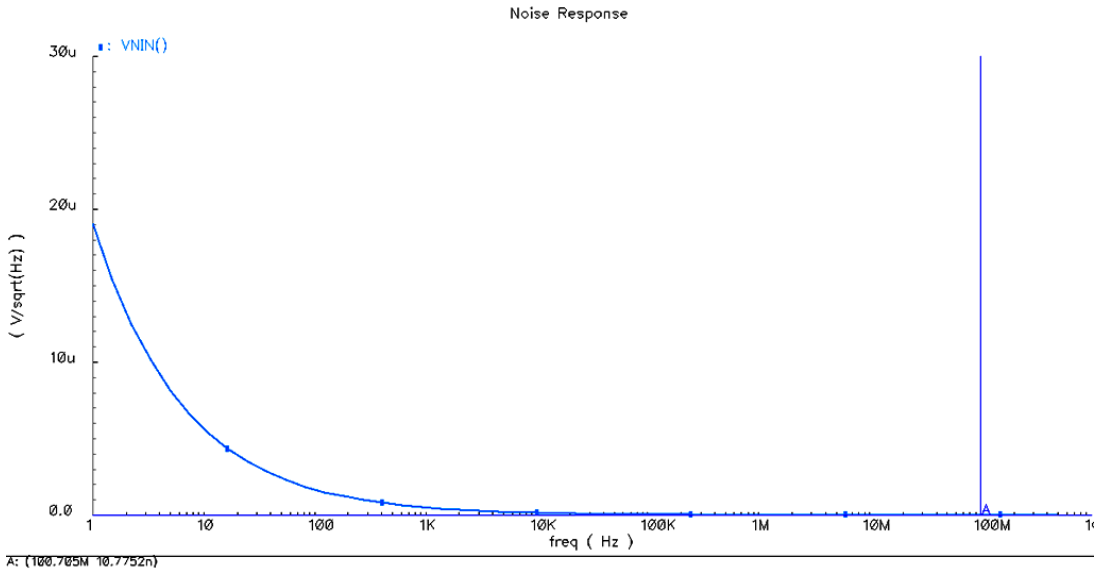


Figure 21 Input referred noise spectral density of the standalone OTA

4.3 The G_m-C biquadratic cell

The G_m-C biquadratic filter implemented using three OTAs is shown in Fig. 22. The effective transconductance of OTA_1, OTA_2 and OTA_3 is represented by g_{m1}, g_{m2} and g_{m3} respectively. OTA_2 and OTA_3 form a resonator whose equivalent impedance seen from node V_{out} is expressed as given in equation (4.9).

$$Z_L = sL = \frac{sC_2}{g_{m2}g_{m3}} \tag{4.9}$$

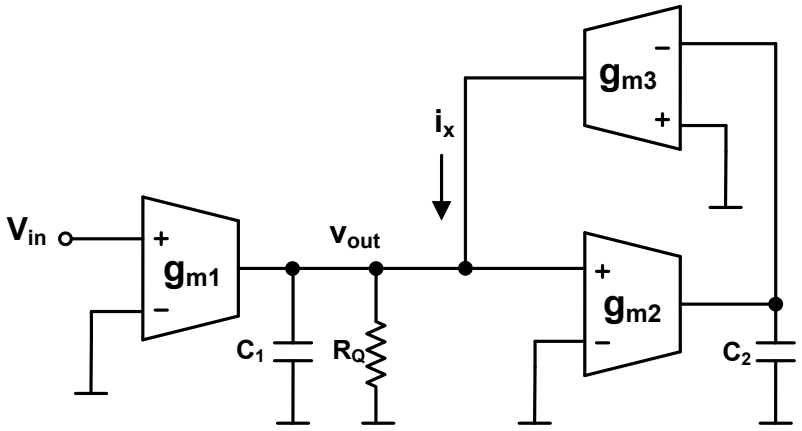


Figure 22 Schematic of the single-ended version of the biquadratic OTA-C filter

In a first order approximation, the following transfer function is obtained from the analysis of the biquadratic band-pass filter as given in equation (4.10). The important performance parameters of the band pass filter are center frequency (ω_0) and bandwidth (BW).

$$H_{BP}(s) = \frac{V_{OUT}}{V_{in}} = \frac{\frac{g_{m1}}{C_1}\, s}{s^2 + \frac{s}{R_Q C_1} + \frac{g_{m2}g_{m3}}{C_1 C_2}} = \frac{\omega_o\, s}{s^2 + BW\, s + {\omega_o}^2} \tag{4.10}$$

4.3.1 Linearity analysis of the G_m-C biquad

There are many sources of non-linearity in the G_m-C biquad. In this section, the non-linearity of the biquad is analyzed by considering the three main sources of non-linearity. They are: 1) Non-linear transconductance of the main OTA, 2) Non-linear output impedance of the OTA and 3) Non-linearity introduced by the resonator. The G_m-C biquadratic cell with the parameters required for analyzing its linearity performance is shown in Fig. 23. The first order and third order transconductance parameters of OTA_i are represented by g_{m1i} and g_{m3i} respectively. Also, the first order and third order output conductance parameters of OTA_i are represented by g_{O1i} and g_{O3i} respectively. It should be noted that for linearity analysis, only the third order non-linear terms are considered. Even order non-linear terms can be cancelled by choosing fully differential architectures and higher order odd terms can be ignored for simplifying the analysis.

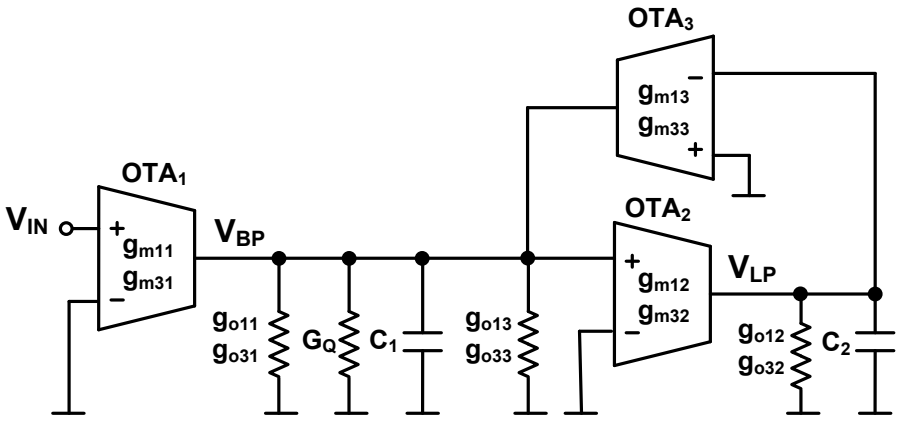


Figure 23 Schematic of the biquadratic OTA-C filter with non-linear elements

A. Non-linear OTA

Consider the G_m-C biquadratic filter with ideal resonator (G_L) shown in Fig. 24. The first and third order transconductance parameter is represented by g_{m11} and g_{m13}

respectively. The non-linearity is mainly produced by the third order term; therefore higher terms can be ignored. The output current (i_{out}) can be expressed as,

$$i_{out} = (g_{m11} + g_{m13}.{v_{in}}^2)v_{in}. \tag{4.11a}$$

The non-linearity can be measured in terms of intermodulation distortion. Two sinusoidal tones with amplitude A, and angular frequencies ω_1 and ω_2 are used for the input such that:

$$v_{in} = \frac{A}{2}\cos(\omega_1 t) + \frac{A}{2}\cos(\omega_2 t) \tag{4.11b}$$

Therefore, from equation (4.11) and equation (4.11),

$$\begin{aligned} i_{out} = {} & \left(\frac{g_{m11}A}{2} + \frac{9g_{m13}A^3}{32}\right)(\cos(\omega_1 t) + \cos(\omega_2 t)) \\ & + \left(\frac{3g_{m13}A^3}{32}\right)(\cos((2\omega_1 - \omega_2)t) + \cos((2\omega_2 - \omega_1)t) \\ & + \cos((2\omega_1 + \omega_2)t) + \cos((2\omega_2 + \omega_1)t)) \\ & + \left(\frac{g_{m13}A^3}{32}\right)(\cos(3\omega_1 t) + \cos(3\omega_2 t)) \end{aligned} \tag{4.11c}$$

The second term contains the intermodulation products. Intermodulation distortion is measured as the power ratio of the intermodulation products to one fundamental tone. Therefore,

$$IM3 = \frac{\frac{3g_{m13}A^3}{32}}{\frac{g_{m11}A}{2} + \frac{9g_{m13}A^3}{32}} \tag{4.11d}$$

Equation (4.11) can be simplified as below, by assuming that g_{m13} is smaller than g_{m11}.

$$IM3 = \frac{3g_{m13}A^2}{16g_{m11}} \tag{4.11e}$$

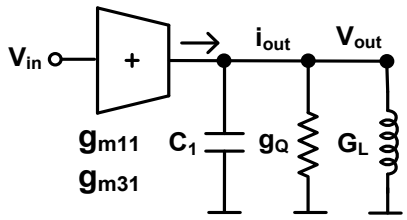


Figure 24 G_m-C filter with ideal resonator

Assuming that the transconductance of OTA is the only non-linear element in the schematic shown in Fig. 24, a relation for third order inter-modulation distortion can be obtained from equation (4.11e) as,

$$\mathrm{IM3} = \frac{3}{16}\frac{g_{m31}}{g_{m11}} v_{in}{}^2 \tag{4.12}$$

B. Non-linear output resistance

Consider the G_m-C biquad shown in Fig. 25 with g_{ds11} and g_{ds13} as the first order output conductance parameters of OTA_1 and OTA_3 respectively. The third order conductance parameters are shown as g_{ds31} and g_{ds33} for OTA_1 and OTA_3 respectively.

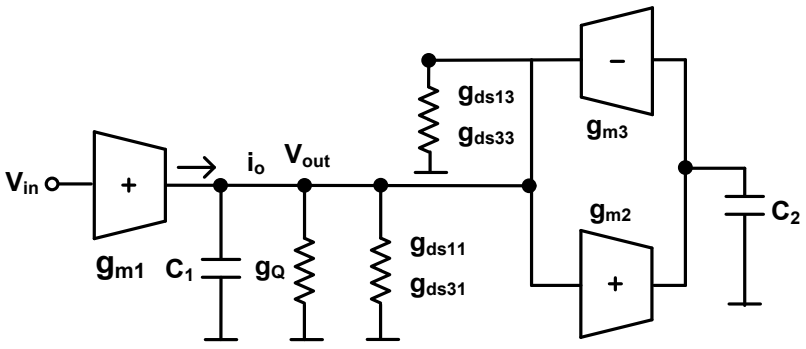


Figure 25 Gm-C biquad with non-linear output impedance of OTA

The output current can be expressed as,

$$i_o = \left(sC_1 + g_Q + g_{ds11} + g_{ds13}\right) v_{out} + \left(g_{ds31} + g_{ds33}\right) {v_{out}}^3. \quad (4.13)$$

Assuming that the input OTA is linear, a relation for third order inter-modulation distortion can be obtained as,

$$IM3 = \frac{3}{16} \frac{g_{ds31} + g_{ds33}}{sC_1 + g_Q + g_{ds11} + g_{ds13}} {v_{out}}^2. \quad (4.14)$$

Equation (4.14) shows that the filter non-linearity is directly proportional to third order output conductance parameters of OTA_1 and OTA_3.

C. Non-linear resonator

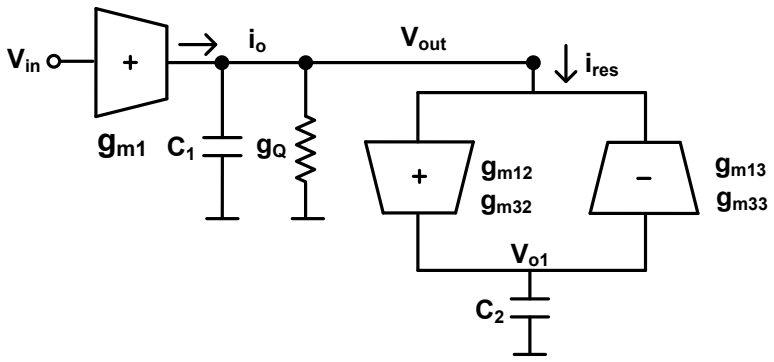


Figure 26 Gm-C biquad with non-idealities in resonator

Consider the resonator part of the biquadratic section shown in Fig. 26. It consists of OTA_2 and OTA_3 connected back-to-back. The first order transconductance parameters of OTA_2 and OTA_3 are denoted as g_{m12} and g_{m13} respectively. And, the third order transconductance parameters are denoted as g_{m32} and g_{m33} respectively. In this analysis fully differential implementation is assumed and the second order transconductance parameters can be ignored. Also the higher order transconductance

parameters can be ignored in the analysis. The expression for node voltage V_{01} can be written as,

$$V_{o1} = \left(g_{m12} + g_{m32}.{V_{out}}^2\right)\frac{V_{out}}{sC_2}. \tag{4.15}$$

Also, the output current of the resonator can be expressed as given in equation (4.16a). It is further simplified in equations (4.16b) and (4.16c).

$$i_{res} = \left(g_{m13} + g_{m33}{V_{01}}^2\right)V_{o1} \tag{4.16a}$$

$$i_{res} = \left[g_{m13} - g_{m33}\left(\frac{{g_{m12}}^2 - 2\,g_{m32}\,g_{m12}\,{V_{out}}^2 + {g_{m32}}^2{V_{out}}^4}{(sC_2)^2}\right){V_{out}}^2\right]\times \tag{4.16b}$$

$$\left(\frac{g_{m12} - g_{m32}.{V_{0ut}}^2}{sC_2}\right)V_{0ut}$$

$$i_{res} = \left[\frac{g_{m12}g_{m13}}{sC_2}\right]V_{out} - \left[\frac{g_{m13}g_{m32}s^2{C_2}^2 + {g_{m12}}^3g_{m33}}{(sC_2)^3}\right]{V_{out}}^3 + \ldots \tag{4.16c}$$

For the entire bi-quadratic section shown in Fig. 26, if it is assumed that the transconductance stage (g_{m1}) is linear, it produces linear output current (i_o). The output impedance of OTA is assumed to be much higher than R_Q ($g_Q >> g_{out}$) and the total output current (i_o) is expressed as,

$$i_o = \left(g_Q + sC_1\right)v_{out} + i_{res}. \tag{4.17a}$$

Substituting i_{res} in equation (4.17a) gives the expression in equation (4.17b).

$$i_o = \left[\left(s^2 + s\frac{g_Q}{C_1} + \frac{g_{m12}g_{m13}}{C_1C_2}\right)\frac{C_1}{s}\right]V_{out} + \left[\left(s^2 + \frac{{g_{m12}}^3 \cdot g_{m33}}{{C_2}^2 \cdot g_{m13} \cdot g_{m32}}\right)\frac{g_{m13} \cdot g_{m32}}{s^3 C_2}\right]{V_{out}}^3 + \cdots \quad (4.17b)$$

From equation (4.17b), a relation for the third order inter-modulation distortion is expressed as given in equation (4.17c).

$$IM3 = \frac{3}{16}\frac{\left[\left(s^2 + \frac{{g_{m12}}^3 g_{m33}}{{C_2}^2 g_{m13} g_{m32}}\right)\frac{g_{m13}g_{m32}}{s^3 C_2}\right]{V_{out}}^2}{\left(s^2 + s\frac{g_Q}{C_1} + \frac{g_{m12}g_{m13}}{C_1C_2}\right)\frac{C_1}{s}} \quad (4.17c)$$

Equation (4.17c) can be rearranged to obtain equation (4.17d)

$$IM3 = \frac{3}{16}\frac{g_{m13}g_{m32}}{s^3 C_2 g_Q}\left(s^2 + \frac{{g_{m12}}^3 g_{m33}}{{C_2}^2 g_{m13} g_{m32}}\right)\frac{s\,\frac{g_Q}{C_1}}{\left(s^2 + s\frac{g_Q}{C_1} + \frac{g_{m12}g_{m13}}{C_1C_2}\right)}{V_{out}}^2 \quad (4.17d)$$

To get a simplified expression, it is assumed that the OTA stages of the resonator are identical and hence, $g_{m12} = g_{m13}$, $g_{m32} = g_{m33}$ and $C_1 = C_2$. Therefore, equation (4.17d) is simplified to get equation (4.17e).

$$IM3 = \frac{3}{16}\frac{\omega_o}{s^3}\frac{g_{m32}}{g_Q}(s^2 + {\omega_o}^2)\frac{A_{v,peak}\ s}{s^2 + BW\,s + {\omega_o}^2}{V_{out}}^2 \quad (4.17e)$$

And hence, IM3 can be expressed as given in equation (4.17f).

$$IM3 = \frac{3}{16}\underbrace{\frac{g_{m32}\omega_o A_{v,peak}}{g_Q}}_{\text{constant term}}\underbrace{\left(\frac{(s^2 + {\omega_o}^2)}{s^2(s^2 + BWs + {\omega_o}^2)}\right)}_{\text{frequency depedent term}}{V_{out}}^2 \quad (4.17f)$$

From the above simplified expression it can be seen that the non-linearity of the G_m-C biquad with a practical resonator depends on many factors. There is a constant term, a frequency dependent term and the output amplitude term.

The frequency dependent term was plotted in MATLAB and its magnitude response is shown in Fig. 27. It is a combination of the notch filter and the high pass filter response. It can be easily noted that if the frequency of operation is close to the center frequency, the magnitude of the third order harmonic becomes zero. Further to this, the magnitude of IM3 is directly proportional to the output amplitude and the third order non-linear transconductance parameter of the OTA. In general, third order non-linear transconductance of the OTA limits its overall linearity performance. In the present case, the transconductance is linearized using non-linear source degeneration by means of an auxiliary differential pair. The Table 5 presents the linearity test results for the G_m-C biquadratic band pass filter. From the table, it is observed that the IM3 degrades as the separation between the two input tones is widened. A plot of IM3 vs. frequency spacing obtained from cadence simulation results is shown in Fig. 28.

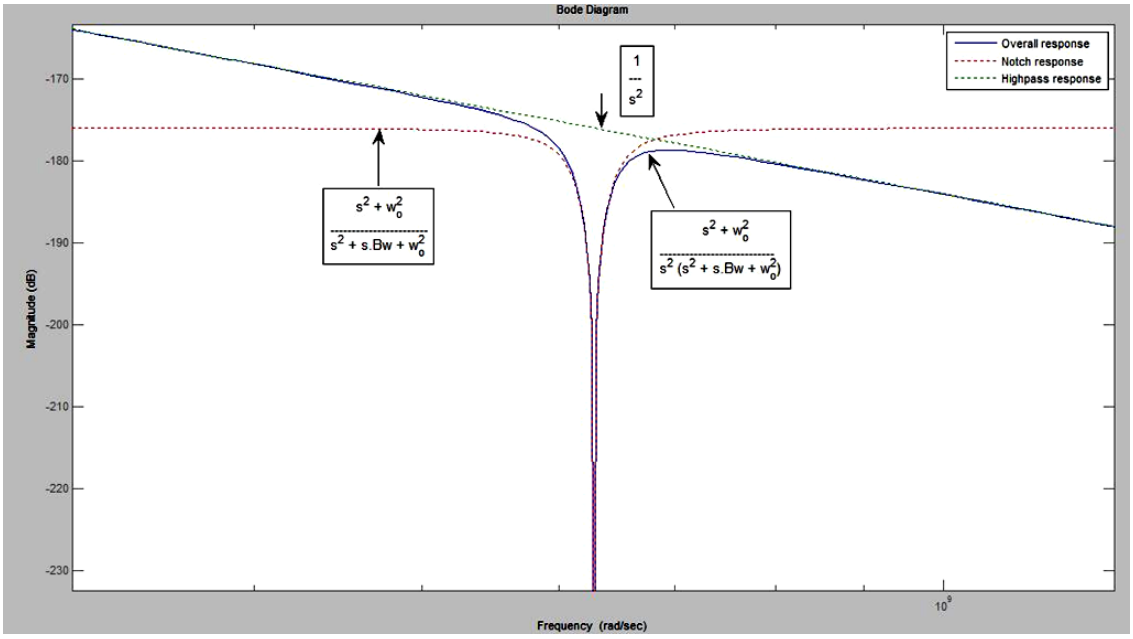


Figure 27 Dependence of IM3 on frequency of operation of G_m-C biquad

Table 5 Linearity test for G_m-C biquad (Quality factor = 10) for different input frequencies

Frequency of two input tones	Separation, Δf	IM3 (V_{amp} = 400mV_{p-p})
99.5 MHz, 100.5 MHz	1 MHz	-79.7182 dB
99 MHz, 101 MHz	2 MHz	-77.3634 dB
98.5 MHz, 101.5 MHz	3 MHz	-76.2002 dB
98 MHz, 102 MHz	4 MHz	-75.5994 dB
97.5 MHz, 102.5 MHz	5 MHz	-75.4191 dB
97 MHz, 103 MHz	6 MHz	-75.1771 dB
96.5 MHz, 103.5 MHz	7 MHz	-75.1465 dB
96 MHz, 104 MHz	8 MHz	-75.1315 dB
95.5 MHz, 104.5 MHz	9 MHz	-74.8356 dB
95 MHz, 105 MHz	10 MHz	-74.7341 dB
90 MHz, 110 MHz	20 MHz	-73.2794 dB

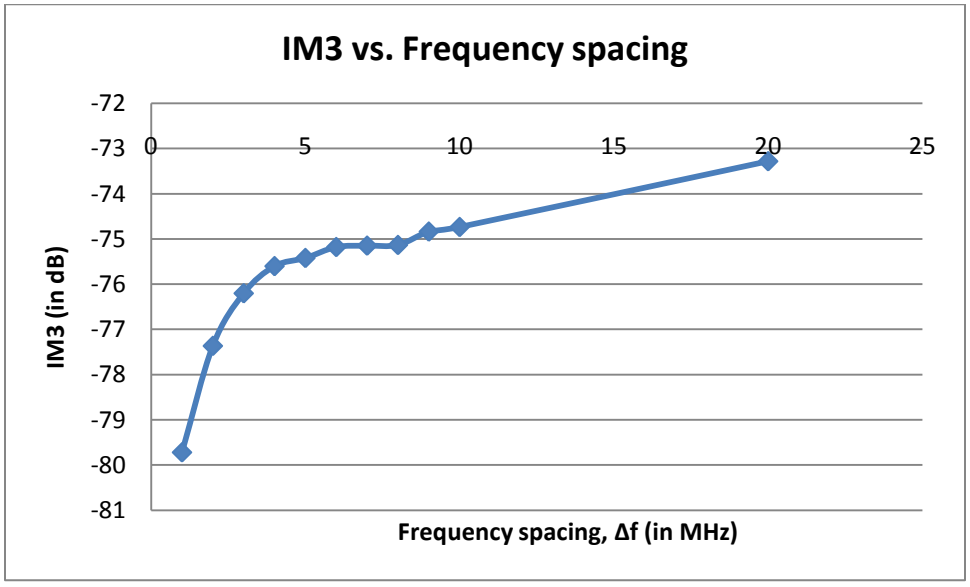


Figure 28 Simulation results showing IM3 vs. frequency spacing for G_m-C biquad

4.3.2 Noise analysis of the G_m-C biquad

The total input referred thermal noise of the G_m-C biquadratic filter shown in Fig. 29 is computed in this section. Flicker noise will not be considered because it can be ignored for most of the practical high frequency band pass applications. Thermal noise is one of the fundamental limitations when designing high performance continuous time G_m-C filters. Let v_{n1}^2, v_{n2}^2 and v_{n3}^2 be the input referred voltage noise density of OTA_1, OTA_2 and OTA_3 respectively as expressed in equation (4.18a). It is assumed that, all input referred noise sources associated to the different OTAs are assumed to be uncorrelated.

$$v_{ni}^2 = \frac{4kT\gamma}{g_{mi}};\ i = 1, 2, 3 \tag{4.18a}$$

The current noise density can equivalently be represented as in equation (4.18b).

$$i_{ni}^2 = {g_{mi}}^2 . v_{ni}^2 = 4kT\gamma g_{mi};\ i = 1, 2, 3 \tag{4.18b}$$

The current noise density of the resistor R_Q is given by the following expression given.

$$i_{nQ}^2 = \frac{4kT}{R_Q} \tag{4.18c}$$

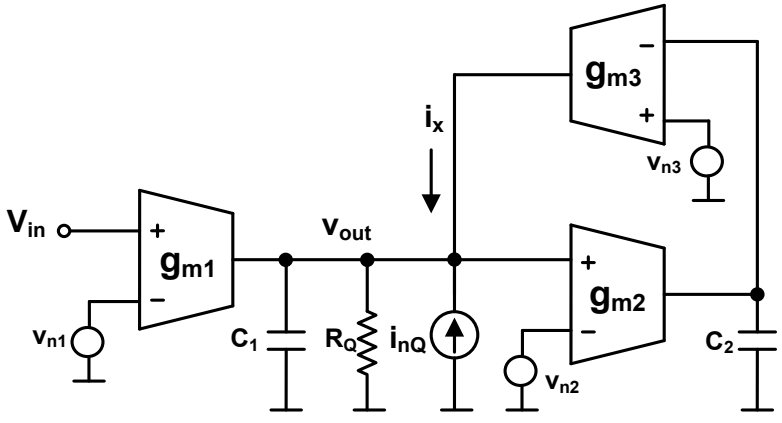


Figure 29 Schematic of the biquadratic OTA-C filter with noise sources

The total current noise density at the output node is contributed by current noise densities of OTA_1, OTA_2, OTA_3 and R_Q given by (4.19a) and (4.19b).

$$i_{ni}^2 = i_{n1}^2 + i_{nQ}^2 + i_x^2 \tag{4.19a}$$

$$i_{ni}^2 = {g_{m1}}^2 . v_{n1}^2 + \frac{4kT}{R_Q} + {g_{m3}}^2 \left[v_{n3}^2 + {g_{m2}}^2 . \left(\frac{1}{\omega C_2} \right)^2 . v_{n2}^2 \right] \tag{4.19b}$$

Hence, the total input referred noise voltage density is computed as given in equation (4.19c). Equation (4.19c) is further simplified to get equation (4.19d).

$$v_{n,total}^2 = \frac{1}{{g_{m1}}^2} \left[4kT\gamma g_{m1} + \frac{4kT}{R_Q} + {g_{m3}}^2 \left[\frac{4kT\gamma}{g_{m3}} + \frac{4kT\gamma}{g_{m2}} . {g_{m2}}^2 . \left(\frac{1}{\omega C_2} \right)^2 \right] \right] \tag{4.19c}$$

$$v_{n,total}^2 = \frac{4kT\gamma}{g_{m1}} \left[1 + \frac{1}{g_{m1}\gamma R_Q} + \frac{g_{m3}}{g_{m1}} \left[1 + \frac{g_{m2} \cdot g_{m3}}{(\omega C_2)^2} \right] \right] \tag{4.19d}$$

It may be assumed that the OTA stages of the resonator and of the biquad are identical. Hence, $g_{m2} = g_{m3}$ and $C_1 = C_2$ can be substituted in equation (4.19d) to get a simplified expression,

$$v_{n,total}^2 = \frac{4kT\gamma}{g_{m1}} \left[1 + \frac{1}{\gamma A_{v,peak}} + \frac{Q}{A_{v,peak}} \left[1 + \frac{{\omega_o}^2}{\omega^2} \right] \right]. \tag{4.19e}$$

For high-Q filters, the quality factor is approximately the same as the peak gain and it is greater than one. The power of total input referred voltage noise at the center frequency of the G_m-C biquadratic filter is approximately,

$$v_{n,total}^2 = v_{n1}^2 \left[2 + \left(\frac{\omega_o}{\omega} \right)^2 \right]. \tag{4.19f}$$

Therefore, the input referred noise voltage of the biquad is $\sqrt{3}$ times that of the stand-alone OTA. And hence, the SNR of the Bi-Quad is mainly dependent on the SNR of the OTA.

4.4 Biquad simulation results

Table 6 summarizes the performance results obtained for the G_m-C band pass filter designed in 0.18µm CMOS technology. The biquad has a center frequency of 100MHz and quality factor equal to 10. The input referred noise voltage of the biquad is observed as 21.14 nV/√Hz, which is approximately √3 times that of the standalone OTA as seen in Table 4.

Table 6 Gm-C band pass filter simulation results

Parameter	Value
Center frequency	100 MHz
Peak gain	20 dB
IM3 (at 400mV_{p-p})	< -75 dB
Input referred voltage noise	18.74 nV/√Hz
Integrating capacitor	2.8 pF
Power Consumption	28.8 mW
Supply voltage	1.8 V

Table 7 summarizes the simulations results obtained for the G_m-C band pass filter for different process corners. Note the IM3 of the band pass filter is < -62 dB for an input amplitude of 400mV_{p-p}. It can also be observed that that the IM3 is only < -52dB

for the OTA without non-linear source degeneration. So, non-linear source degeneration can guarantee an IM3 improvement of 10dB across process corners.

Table 7 Gm-C band pass filter simulation results across process corners

Parameter	NOM	FAST	SLOW	SLOWFAST	FASTSLOW
Center frequency (in MHz)	100.4	103	97.5	97.72	103
Peak gain (in dB)	20.2	19.2	21.5	19.72	20.89
IM3 (400mV p-p) with nonlinear source degeneration (in dB)	-75	-63	-62.6	66.34	66.4
IM3 (400mV p-p) without nonlinear source degeneration (in dB)	52.6	52.4	53	52.9	51.7

The plot shown in Fig. 30 presents the magnitude and phase response for the G_m-C band pass filter. It is noted that center frequency of the filter is 100MHz and there is a phase shift of 180^o. The peak gain of the filter is 20dB at the center frequency, and hence the quality factor, Q is10.

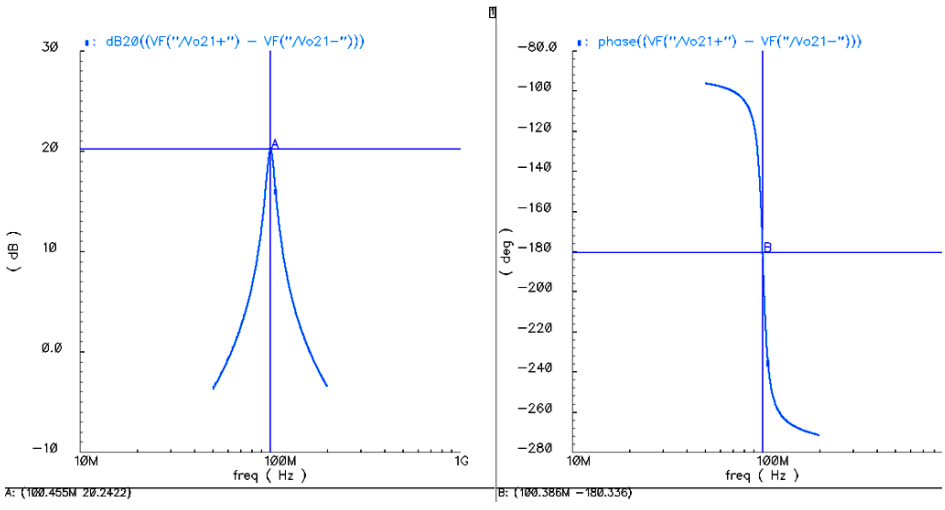


Figure 30 Magnitude and phase response of the G_m-C band-pass biquad

The Linearity measurement of the biquad for 400 mV_{p-p} swing is shown in Fig. 31. The simulated IM3 is -75 dB with two input tones applied at frequencies 99.5MHz and 100MHz.

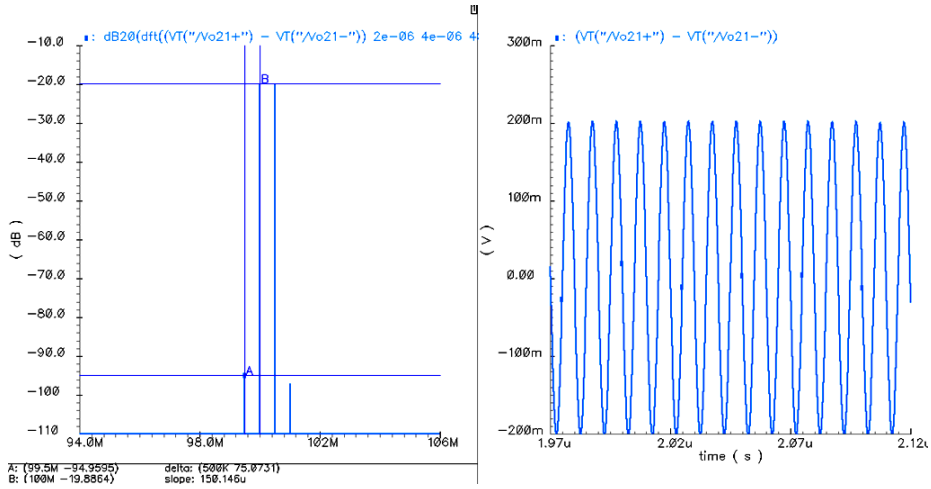


Figure 31 IM3 measurement for the G_m-C biquadratic filter

The plot shown in Fig. 32 presents the response of IM3 vs. input peak amplitude of the G_m-C band pass filter. It should be noted that the IM3 degrades by 12dB for every octave increase in input amplitude.

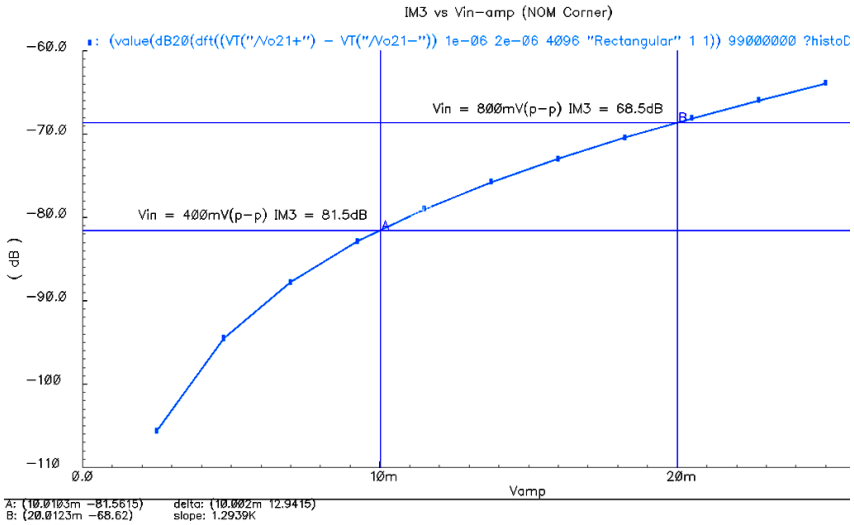


Figure 32 IM3 vs. input amplitude plot for the G_m-C band pass filter, Peak gain = 20dB.

The input referred voltage noise spectral density of the biquad is shown in Fig. 33. The thermal noise density is found to be 18.74 nV/√Hz at 100MHz. This value is approximately √3 times that of the stand alone OTA.

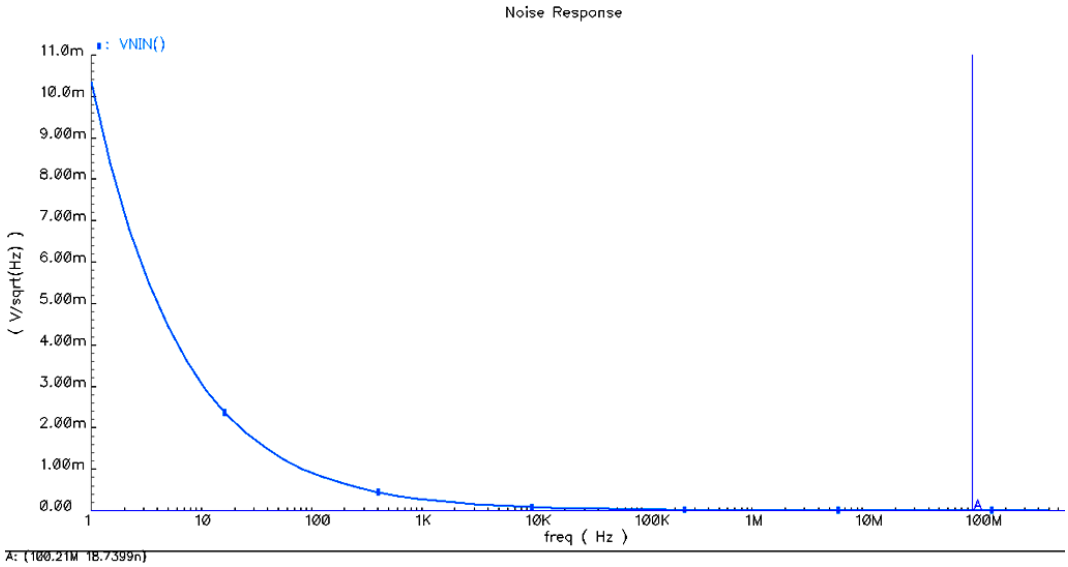


Figure 33 Input referred noise spectral density of the G_m-C biquad

5. DESIGN OF A 5TH ORDER ACTIVE-RC LOW-PASS FILTER

This section focuses on the design of a 5th order active low-pass filter for a continuous-time sigma-delta (ΣΔ) ADC. First, the structure and design equations of the two-integrator loop configuration for realizing the biquadratic filter are discussed in brief. Next, circuit implementation details of the amplifiers used in the integrator stages are presented. The design of a summing amplifier and a novel method for adjusting the group delay in the fast path provided by a secondary feedback DAC of the continuous-time ΣΔ ADC are presented in detail.

5.1 Introduction

A major challenge in the implementation of a low-pass CT ΣΔ ADC with 25MHz bandwidth and 12-bits resolution is the design of analog loop filter. Higher-order filters shape the in-band quantization noise and achieve high SQNR. The dynamic range of the filter must be high enough to achieve high SQNR. Conventionally, the loop filter of CT ΣΔ modulator is realized with active integrators, such as active-RC or G_m-C integrators [23]. Active-RC integrators provide better linearity at high frequencies than their G_m-C counterparts, but consume more power. Their design becomes challenging with the conflicting requirements of low-power and low-noise. Furthermore, the parasitic capacitances present at every node in active-RC circuits deteriorate the performance. Because of a potential large deviation of RC time-constant (±35%) in active-RC integrators, a tuning circuitry is also required.

The main non-idealities of active-RC integrators are caused by finite gain and finite unity gain-bandwidth product (GBW) of operational amplifiers. They alter the transfer characteristic of loop filters, thereby, degrading the overall performance of sigma-delta ADCs. Also, the performance of the modulator suffers from circuit noise and distortion introduced by the amplifiers used in integrator stages. In contrast to errors of the subsequent stages, the errors of the first integrator are not subjected to shaping

within the sigma-delta loop. Thus, the first integrator limits the noise and linearity specification of the entire ΣΔ modulator. Hence, the power dissipated by the first stage of a sigma-delta modulator is significant to the overall power consumption. A substantial amount of power can be saved by a proper circuit design of amplifiers used in the integrators.

5.1.1 Architectural considerations

The fifth order transfer function of the loop filter is realized using feed-forward architecture shown in Fig. 34. It can be realized as cascade of two second order resonator stages and a first order integrator stage. The outputs of the each stage are combined through multiple feed-forward paths. A summing node is required to perform weighted addition of the outputs of the integrators. The summing node also performs weighted addition of the secondary DAC feedback signal for compensating the excess loop delay. The summing point is also required for the injection of two test tones at the input of the quantizer in order to perform digital background calibration of the ADC.

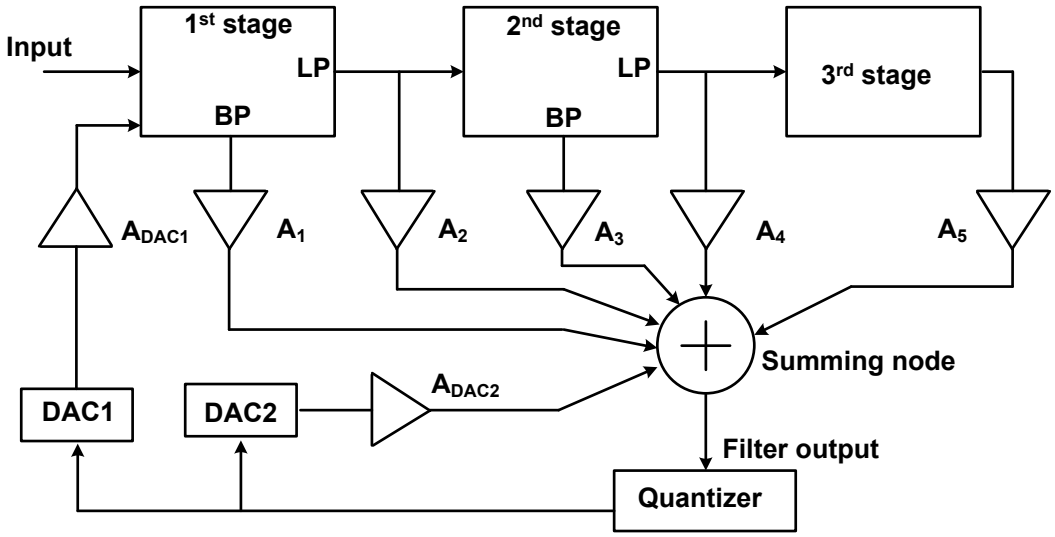


Figure 34 Feed-forward architecture of the 5th order loop filter

The feed-forward architecture has several advantages when compared with more common multiple-feedback approach. The feed-forward topology requires only two accurate DACs and the linearity requirements in the filter stages are eased by the low signal swings at internal nodes. Noise and distortion considerations necessitate the use of large bias currents in the first stage. Therefore, the bandwidth of the first stage opamp can be expected to be higher than the rest of the stages. This can be used as advantage in the feed-forward design, since the first integrator needs to have the least delay. Hence, the large bias currents in the first stage, which are needed for noise reasons, are more efficiently used in a feed-forward loop filter.

5.1.2 Design considerations

The three stages of the filter have decreasing performance requirements (in terms of noise, linearity, power and offset) from the first stage to the third stage. The first and second stages implement two complex pole-pairs that are placed at 24.5MHz and 16.7MHz. The third integrator stage implements a real pole which is placed at 5.71MHz. Since the desired in-band signal flows across the loop filter in ΣΔ modulators, having a very linear filter is necessary. Any non-linearity in the filter gets reflected as spurs in the output spectrum of the modulator. All in-band noise corrupts the desired signal content. For optimum performance, a good balance between signal-to-noise ratio (SNR) and signal-to-distortion ratio (SDR) needs to be maintained in the design of the loop filter [15].

The noise and distortion introduced by the first stage of the filter are most critical for the overall performance of the filter. The nonidealities of second and third stages are noise shaped and the performance requirements are relaxed. Since the summing amplifier is on the shortest path of the loop and its delay cannot be compensated for by the secondary feedback DAC, it is a critical component for the loop stability. The unity gain bandwidth of the summing node should be higher than the sampling frequency by at least five times. To meet this requirement, the transconductance of the summing

amplifier needs to be increased, which results in increased power consumption. The important performance requirements of the fifth-order loop filter are listed in Table 8.

Table 8 Performance requirements of each stage of the filter

Block	Order	DC-gain	Cut-off frequency	Quality factor	Linearity, IM3	Noise, SNR
First stage	2	15.5 dB	24.5 MHz	7.51	< -72 dB	> 72 dB
Second stage	2	15.5 dB	16.7 MHz	1.54	< -60 dB	> 60 dB
Third stage	1	17.7 dB	5.71 MHz	-	< -50 dB	> 50 dB
Summing stage	-	25.0 dB	> 800MHz	-	< -60 dB	> 60 dB
Complete filter	5	48.5 dB	25.0 MHz	-	< -72 dB	> 72 dB

5.2 Design of amplifier

The design of amplifiers used in analog filters has become increasingly difficult in state-of-the-art deep sub-micron CMOS technologies with reduced supply voltages. The, thermal noise floor of the amplifier used in the first stage of the filter has to be lower than the quantization noise for optimal performance of the modulator. The third order inter-modulation (IM3) performance of the amplifier in the first stage of the filter is important in order to tolerate the presence of strong blockers at the input of the ADC. High quality-factor (Q) is required in the first stage to maintain sharp pass-band to stop-band transition for obtaining high-quality noise shaping. Therefore, an operational amplifier with high passband gain and high bandwidth is required in the first stage of loop filter. With 25MHz signal bandwidth and 400MHz sampling frequency, the bandwidth requirement of the amplifier used in the very first integrator was determined as 1.5GHz with system-level simulations. Also, DC-gain of at least 50dB is necessary for low in-band distortion. The filter must employ fully-differential circuitry throughout to minimize sensitivity to supply and substrate noise coupling.

5.2.1 Amplifier architecture

The amplifier used in the first integrator stage needs to satisfy high gain and bandwidth requirements. It is not trivial to design an amplifier with both high gain and GBW because of contradicting design requirements. High-gain amplifiers use cascode and multi-stage architectures, long channel devices and low bias currents. High-bandwidth amplifiers use single stage architectures, high bias currents and short channel devices. Two basic approaches for designing a high gain amplifier are cascode (vertical) approach or cascade (horizontal) approach. The signal swing in cascode amplifiers is constrained by the power supply voltage, which is a problem for low voltage designs. In cascaded amplifiers, each amplifier stage contributes a pole. Miller compensation schemes trade bandwidth for stability.

To satisfy the high gain and bandwidth requirements, a two-stage amplifier with feed-forward compensation is adopted [24]. In this technique, the negative phase shift introduced by the poles in the forward path is compensated by the positive phase shift introduced by the LHP zero in the feed-forward path. The dominant pole is not pushed to lower frequencies since a LHP zero is created without using any Miller capacitor, resulting in a higher gain-bandwidth product with fast step response. The settling time requirement of the amplifier is relaxed for the continuous time filters, hence the settling time degradation due to influence of pole-zero pair [25] can be tolerated. The block diagram of the amplifier with feed-forward compensation technique is shown in Fig. 35.

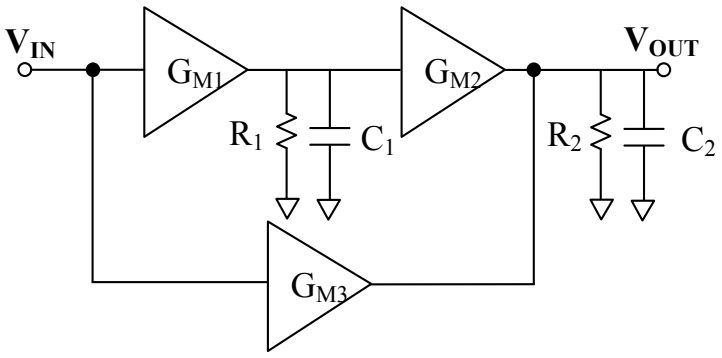


Figure 35 Block diagram of the amplifier with feed-forward compensation technique

The transfer function of the amplifier can be obtained by assuming a single pole response for the three OTA stages G_{M1}, G_{M2} and G_{M3}. There exist two main poles in the amplifier at locations given by $\omega_{p1} = 1/R_1C_1$ and $\omega_{p2} = 1/R_2C_2$. The voltage transfer function from input to the output of the amplifier can be obtained as

$$H(s) = \left(\frac{G_{M1}R_1}{1+\frac{s}{\omega_{p1}}}\right)\left(\frac{G_{M2}R_2}{1+\frac{s}{\omega_{p2}}}\right) + \left(\frac{G_{M3}R_2}{1+\frac{s}{\omega_{p2}}}\right) \tag{5.1a}$$

Assuming that $G_{M2} \approx G_{M3}$, equation (5.1a) can be simplified as

$$H(s) = G_{M2}R_2\,(1+G_{M1}R_1)\frac{\left(1+\frac{s}{(1+G_{M1}R_1)\omega_{p1}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{5.1b}$$

Therefore, the feed-forward path in the amplifier creates a LHP zero which can be used to compensate for the phase shift introduced by the non-dominant pole, ω_{p2}. The effect of second pole can be cancelled by choosing $\omega_{p2} = \omega_{p1}\,(1+G_{M1}R_1)$. However, pole-zero mismatches may yield bad settling performance, which is typically not critical for continuous time loop filter implementation.

5.2.2 Amplifier circuit implementation

The fully-differential circuit implementation of the amplifier is shown in Fig. 36. The use of cascode stages is avoided, to make solution exportable to more advanced technologies with lower supply voltages. The first stage (MN_1, MP_1) of the amplifier is designed to have a high gain and dominant pole at its output. The pole location is determined by the parasitic capacitances at the output of the first stage. The output swing of this stage need not be high because the signal is further amplified by the gain of the second stage. The second (MN_2, MP_2) and feed-forward (MN_3) stages are optimized for high bandwidth and medium gain performance. The transconductance of the second and feed-forward stages should be increased as much as possible to the push poles to higher frequencies. For better linearity, MN_2 and MP_2 are designed to have high V_{DSAT} (> 200mV) due to high signal swing at the output of the second stage. The first and the feed-forward stages are the main contributors to the input-referred thermal noise of the amplifier.

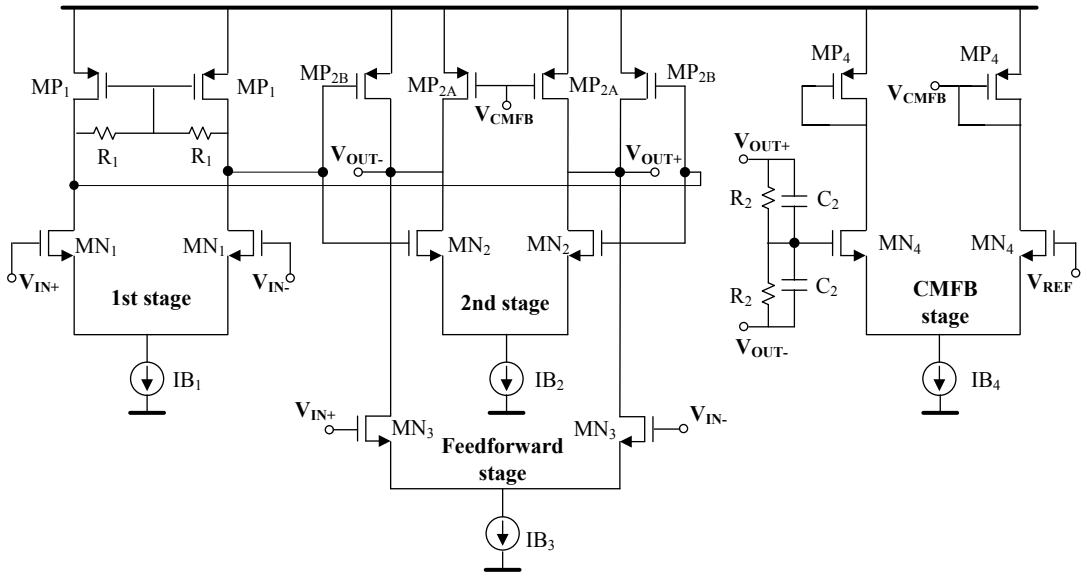


Figure 36 Schematic of the amplifier used in the loop filter

The DC common-mode level at the output of the first stage is set to 1.2V using a shunt-feedback resistive load of R_1 [26]. The DC level at the output of the second stage of the amplifier is controlled using a common-mode feedback circuit (CMFB) consisting of MN_4 and MP_4. The output common-mode level is detected using resistive averaging (R_2), and the common-mode error is fed back to the node V_{CMFB} to regulate the output level to 1.1 V. The stability of the common-mode loop is enhanced by adding a small capacitor C_2 that introduces a LHP zero in the common-mode path. The component values and parameters of the amplifier in the first stage of the loop filter are listed in Table 9. The amplifier was optimized with respect to stability, noise, linearity and power. The subsequent integrators employ the same amplifier structure, but consuming less power. Table 10 present transistor dimensions, device values and bias conditions of amplifier I and amplifier II designed for the loop filter implementation.

Table 9 Transistor dimensions, device values and bias conditions for amplifier I

Device	Dimensions	Device	value
MN_1	(5) 30µm / 600 nm	IB_1	450 µA
MP_1	(7) 9.0 µm / 400 nm	IB_2	800 µA
MN_2	(4) 7.0 µm / 400 nm	IB_3	600 µA
MP_{2A}	(4) 9.0 µm / 400 nm	IB_4	600 µA
MP_{2B}	(10) 9 µm / 400 nm	R_1	80 KΩ
MN_3	(5) 12 µm / 300 nm	R_2	80 KΩ
MN_4	(5) 24 µm / 300 nm	C_2	100 fF
MP_4	(4) 9.0 µm / 400 nm		

Table 10 Transistor dimensions, device values and bias conditions for amplifier II

Device	Dimensions	Device	value
MN_1	(3) 14µm / 600 nm	IB_1	200 µA
MP_1	(2) 3.5 µm / 400 nm	IB_2	300 µA
MN_2	(4) 7.0 µm / 400 nm	IB_3	200 µA
MP_{2A}	(2) 5.5 µm / 400 nm	IB_4	200 µA
MP_{2B}	(4) 9.5 µm / 400 nm	R_1	80 KΩ
MN_3	(3) 12 µm / 300 nm	R_2	80 KΩ
MN_4	(5) 8 µm / 300 nm	C_2	100 fF
MP_4	(2) 5.5 µm / 400 nm		

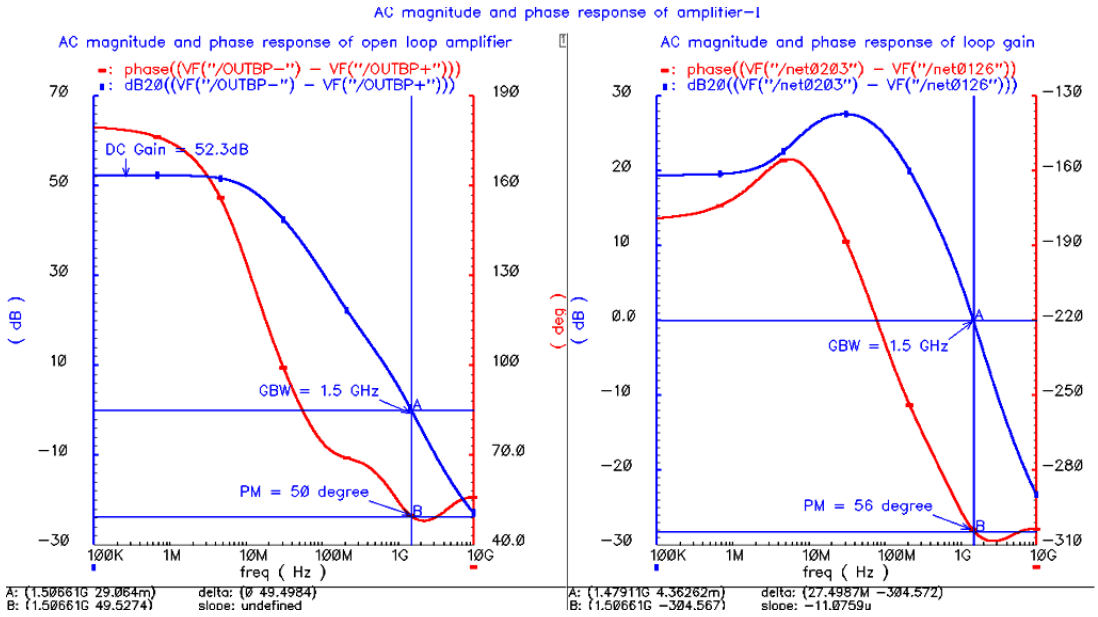
5.2.3 Simulation results of the amplifier

The important performance parameters obtained from two different version of amplifiers designed for the loop filter are summarized in Table 11.

Table 11 Summary of performance parameters for amplifier I and II

Performance parameter	Amplifier I	Amplifier II
DC-gain	52 dB	42 dB
Gain bandwidth product	1.5 GHz	890 MHz
Input referred integrated noise (in 25 MHz)	19.02 µV	30.18 µV
Power consumption	4.5 mW	1.7 mW

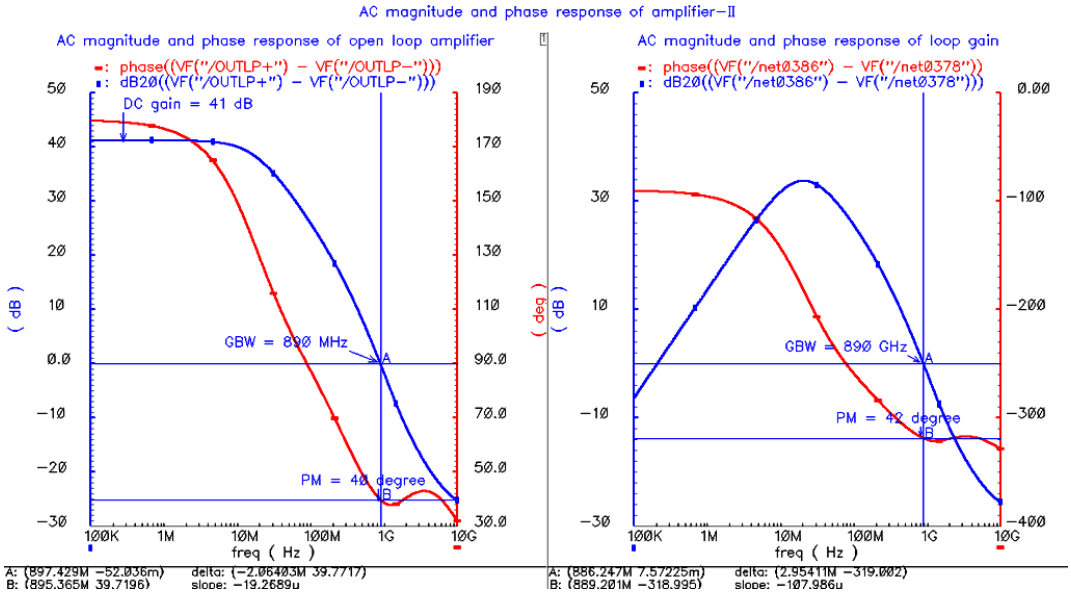
Simulation results showing AC magnitude and phase response plot of the amplifier I are shown in Fig. 37a. The phase margin is 50^{o} at unity gain frequency of 1.5GHz. It has a DC gain of 52dB, while voltage gain is 44dB at 25MHz. The amplifier is used in a two-integrator loop filter. Therefore, the total loop gain needs to be considered for analyzing the stability. The loop gain is expressed as the product of amplifier open loop transfer function and the feedback factor.



(a) AC response of the amplifier (b) Simulated loop gain

Figure 37 Simulated AC responses for amplifier I

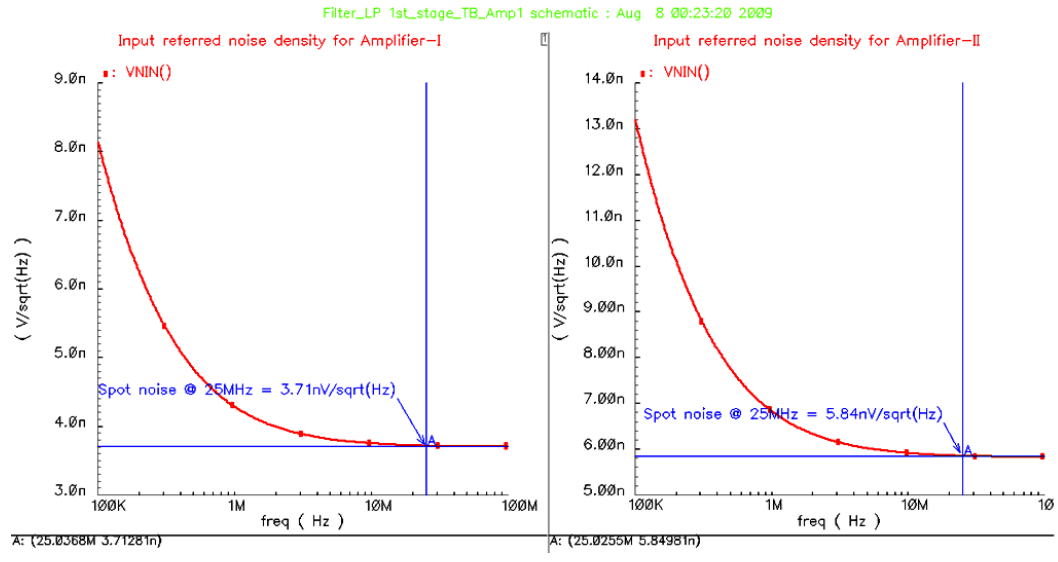
To simulate the loop gain, a break point is inserted at the input of the amplifier and a test input is applied at the break point. Simulated loop gain is shown in fig. 37b. The AC magnitude and phase response plots of the amplifier II are shown in Fig. 38.



(a) Open loop response (b) Loop gain of the amplifier

Figure 38 Simulated AC responses for amplifier II

The input-referred noise spectral density plot for both amplifiers is shown in Fig. 39. The spot noise at 25MHz is 3.71nV/√Hz and 5.84nV/√Hz for amplifier I and II respectively.



(a) Amplifier I (b) Amplifier II

Figure 39 Input referred noise density of amplifier used in loop filter

The AC response of the CMFB loop is shown in Fig. 40. The transient response in Fig. 41 demonstrates the common-mode loop stability for a common mode step input current of 50µA (10% of the bias current). The 1% settling value of the common-mode voltage shows an offset is approximately 18mV from the ideal output voltage.

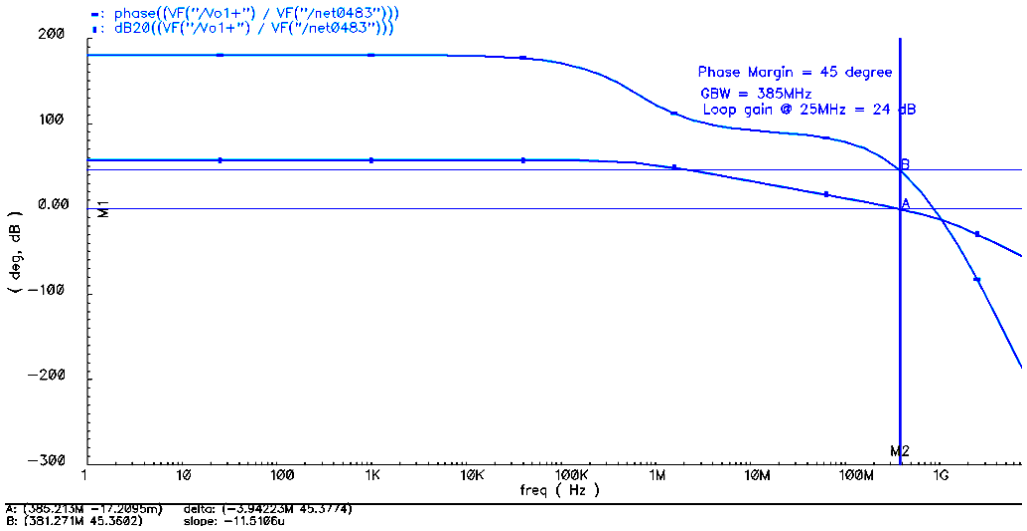


Figure 40 Common-mode loop AC magnitude and phase response

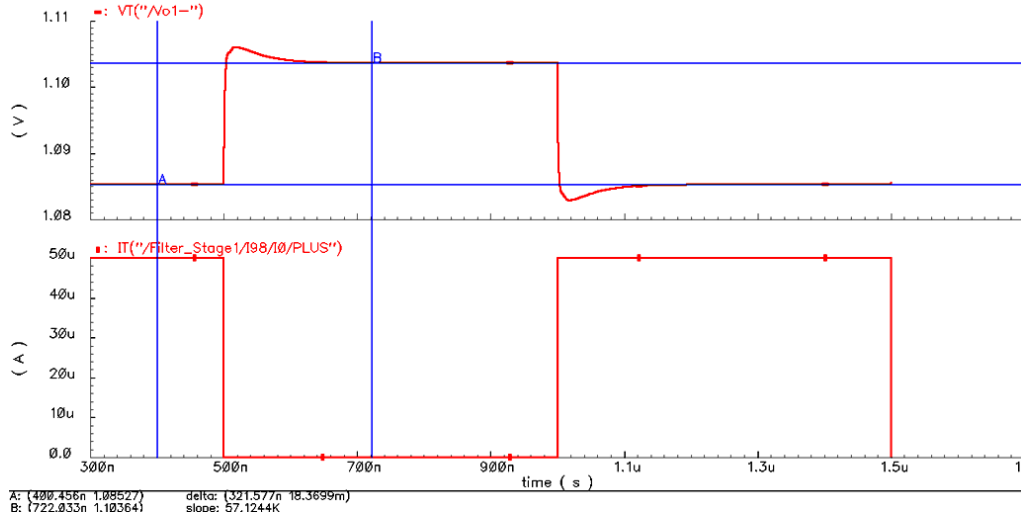
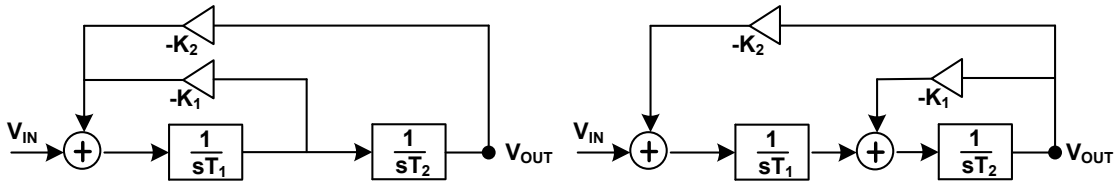


Figure 41 Step response of CMFB loop

5.3 Second order filter realization

The first stage and second stages of the filter both have 2nd order transfer functions realized with the two-integrator loop configuration. There exist two different configurations of the two-integrator loop systems as shown in Fig. 42. The first one is the summed feedback (SF) type and the other one is the distributed feedback (DF) type. In the SF type, the outputs of all the integrators are fed back to the first integrator input. In the DF type, the output of last integrator is fed back to the inputs of all integrators. Two-integrator loop structures provide very low sensitivity to component variations and they can be cascaded easily for higher order filter design. The summed-feedback structure provides low-pass and band-pass outputs which are independently controlled in the loop filter.



(a) Summed feed-back structure (b) Distributed feed-back structure

Figure 42 Two-integrator loop configurations

5.3.1 Design considerations

The two-integrator loop structure used for the implementing the first stage of the filter is shown in Fig. 43. A summed feed-back type two-integrator loop provides lowpass and band-pass outputs. Assuming that the amplifiers provide large gain, the transfer functions for the biquad can be obtained as given below.

$$A_{LP} = \frac{V_{O,LP}}{V_{IN}} = \frac{R_2/R_3}{1 + sC_2\frac{R_2R_4}{R_1} + s^2C_1C_2R_2R_4} \tag{5.2a}$$

$$A_{BP} = \frac{V_{O,BP}}{V_{IN}} = \frac{sC_2R_4(R_2/R_3)}{1 + sC_2\frac{R_2R_4}{R_1} + s^2C_1C_2R_2R_4} \tag{5.2b}$$

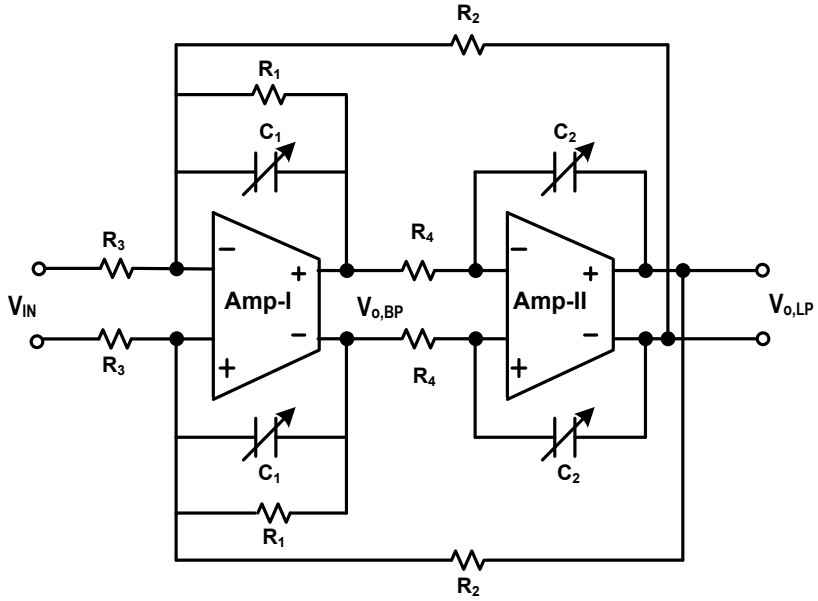


Figure 43 Two-integrator loop biquad

Therefore, the design equations can be obtained as

$$\omega_0^2 = \frac{1}{R_2R_4C_1C_2} \tag{5.3a}$$

$$Q = \frac{R_1}{\sqrt{R_2R_4}}\sqrt{\frac{C_1}{C_2}} \tag{5.3b}$$

$$A_0 = \frac{R_2}{R_3} \tag{5.3c}$$

where A_0 is the DC gain, ω_0 is the cut-off frequency, and Q is the quality factor of the biquad. For simplicity, it can be assumed that $R_2 = R_4$ and $C_1 = C_2$ to get cut-off frequency, quality factor and low-frequency gain expressions are

$$\omega_0 = \frac{1}{R_2 C_1} \tag{5.4a}$$

$$Q = \frac{R_1}{R_2} \tag{5.4b}$$

$$A_0 = \frac{R_2}{R_3} \tag{5.4c}$$

Therefore, Q and A_0 are determined by the ratio of resistors, and ω_0 can be tuned using C_1. The values of resistors and capacitors in the biquadratic section can be chosen to match the gain and Q requirements. However, thermal noise of the first stage needs to be minimized as it directly appears at the output of the modulator. The input-referred noise of the two-integrator loop filter can approximately be expressed as

$$V_{in,n}^2 = 4kTR_3\left[1 + \frac{R_3}{R_2} + \frac{R_3}{R_1}\right] + 4kTR_4|sC_2R_4|^2 \tag{5.5}$$

$$+ \left[V_{n,a1}^2 + V_{n,a2}^2|sC_2R_4|^2\right]\left|\frac{R_3}{R_1} + sC_1R_3\right|^2$$

In the above expression, $V_{n,a1}^2$ and $V_{n,a2}^2$ represents the input-referred noise of the first and second amplifiers respectively. It can easily be observed that the main noise contributions come from the first amplifier and the input resistor R_3 at low frequencies. Hence, the value of R_3 is chosen such that it satisfies the noise requirement, and then the values of other resistors and capacitors can be determined from filter specifications. At high frequencies, the noise introduced by R_4 and the second amplifier also becomes important.

The integrator time constants can vary due to PVT variations of absolute values of resistors and capacitors. To compensate for this, capacitor banks that can provide ±30% tuning range are implemented. Three control bits (b_2, b_1 and b_0) are used for each capacitor to adjust the cut-off frequency. The switches are placed towards the virtual ground side of the amplifier so that the ON resistance of the switches is constant (independent of the signal swing). The size of the switches is chosen such that the ON-resistance (inversely proportional to W/L of the transistor) is minimized. On the other side, the parasitic capacitance at the virtual ground node of the amplifier increases when the switch size is increased indefinitely. Therefore, a nominal aspect ratio of 100 (W = 18μm and L = 0.18 μm) was chosen in this design. PMOS switches are chosen for the implementation because they provide higher gate-to-source voltage than NMOS switches when they are ON. An example of tuning mechanism is shown in Fig. 44 for a single-ended integrator stage.

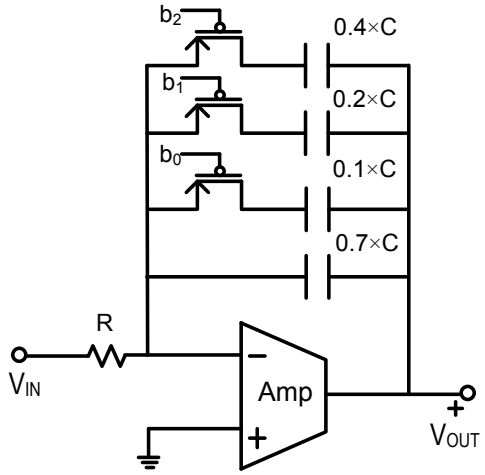


Figure 44 Capacitor tuning mechanism for a single-ended integrator stage

The parameters used in the implementation of the first biquad are listed in Table 12.

Table 12 Component values used in the implementation of first biquad of loop filter

Parameter	Value
R_1	40.00 KΩ
R_2, R_4	6.498 KΩ
R_3	1.083 KΩ
C_1, C_2	0.7 pF – 1.4 pF

The simulation results obtained for the first stage of the filter are given in table 13. The cut-off frequency is 24.43 MHz with quality factor being 7.55.

Table 13 Important performance parameters of the first stage of filter

Performance parameter	Value
Cut-off Frequency	24.43 MHz
Pass band Gain	15.53 dB
Quality factor	7.55
IM3 (400mV p-p)	-73.5 dB
Input referred integrated noise (in 25MHz)	41.13μV
Power consumption	6.2 mW

The parameters used in the implementation of second biquad are listed in Table 14.

Table 14 Component values used in the implementation of second biquad of filter

Parameter	Value
R_1	28.00 KΩ
R_2, R_4	18.18 KΩ
R_3	3.03 KΩ
C_1, C_2	0.35 pF – 0.7 pF

The simulation results obtained for the first stage are summarized in Table 15. The cut-off frequency is 16.67 MHz with quality factor being 1.55.

Table 15 Important performance parameters for second stage of filter

Performance parameter	Value
Cut-off Frequency	16.67 MHz
Pass band Gain	15.5 dB
Quality factor	1.55
IM3 (600mV p-p)	-80 dB
Input referred integrated noise (in 16.7 MHz)	61.75 µV
Power consumption	3.4 mW

Simulation results of the first and second biquad stages using two integrator loop configuration are summarized in section 6.

5.4 First-order integrator stage

The third stage of the filter implements a first-order integrator with a real pole realized using the circuit configuration shown in Fig. 45. Assuming that the amplifier provides large gain, the transfer function given in equation (5.6) is derived for the lossy integrator circuit configuration.

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1}{R_2}\left(\frac{1}{1 + sR_1C_1}\right) \tag{5.6}$$

Therefore, the design equations can be obtained as

$$\omega_0 = \frac{1}{R_1C_1} \tag{5.7a}$$

$$K = \frac{R_1}{R_2} \tag{5.7b}$$

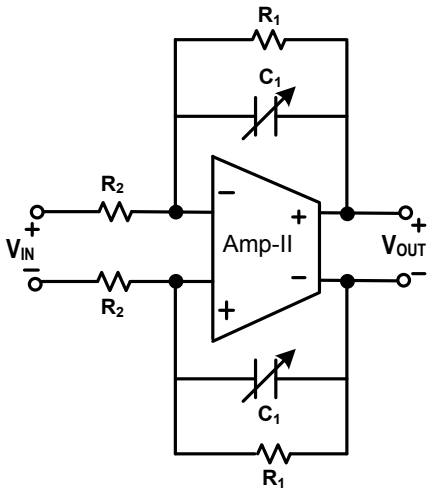


Figure 45 Third stage of the loop filter

where K is the DC gain and ω_0 is the cut-off frequency of the integrator. Therefore, the value of K is determined by the ratio of resistors, and ω_0 can be tuned using C_1. The values of resistors and capacitors in the integrator can be chosen to match the gain and bandwidth requirements of the third stage. The capacitor banks that can provide ±30% tuning range are implemented for each capacitor to adjust the location of the pole implemented by the integrator. The parameters used in the implementation of the third stage of loop filter are listed in Table 16.

Table 16 Component values used in the implementation of first biquad of loop filter

Parameter	Value
R_1	29.30 KΩ
R_2	3.635 KΩ
C_1	0.7 pF – 1.4 pF

The simulation results obtained for the first stage are given in table 17. Simulation results of the third integrator stage of the filter are summarized in section 6.

Table 17 Important performance parameters for third stage of filter

Performance parameter	Value
Cut-off Frequency	5.71 MHz
Pass band Gain	17.7 dB
IM3 (600mV p-p)	-72 dB
Input referred integrated noise (in 5.71MHz)	357 μV
Power consumption	1.7 mW

5.5. Summing amplifier

A simplified block diagram demonstrating the role of summing amplifier is shown in Fig. 46. The summing amplifier is used to perform weighted addition of the outputs of the integrators in the loop filter with feed-forward ΣΔ modulator architecture. It also serves as buffer between the quiet analog filter and the very noisy quantizer with digital circuitry. In CT ΣΔ modulators, the excess loop delay needs to be compensated by means of a secondary feedback DAC path. The summing amplifier provides a direct path to the quantizer input for adding the feedback signal from a second DAC. It is also required for the injection of test tones at the input of the quantizer in order to perform digital background calibration of the ADC.

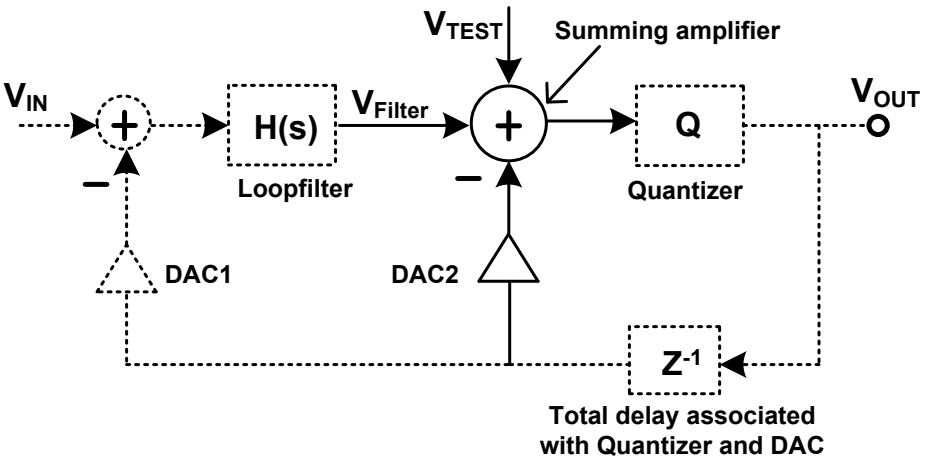


Figure 46 Block diagram showing the summing node in the ΣΔ modulator

The parasitic poles present in the amplifiers of the integrators in the loop filter introduce excess loop delay, which can potentially cause instability to the modulator. One way of mitigating this problem is to use wideband amplifiers in the filter at the expense of power dissipation. An alternative approach is to use low-speed amplifiers and compensate for the excess delay introduced. A conventional way of combating excess loop delay is to have a direct path around the quantizer using a second DAC [9]. This

path needs to be very fast and should not add any extra delay. Therefore, the unity gain bandwidth of the summing amplifier should be higher than the sampling frequency by at least five to six times. To meet this requirement, the transconductance of the summing amplifier should be increased which results in increased power consumption. Any extra delay in the direct path needs to be taken into account when calibration of the loop delay is performed.

5.5.1 Stability considerations

The single-ended representation of the summing amplifier is shown in Fig. 47. The input resistance and the feedback impedances are represented by R_{IN} ($1/G_{IN}$) and Z_F ($1/Y_F$) respectively. The transconductance and the output impedance of the OTA are G_m and R_O ($1/G_O$) respectively. The parasitic capacitance associated with the input of the OTA is shown as C_p at node V_X. The summing amplifier drives the sample-and-hold block of the quantizer, and the load capacitance is represented as C_L. The small signal model of the circuit is shown in Fig. 47.

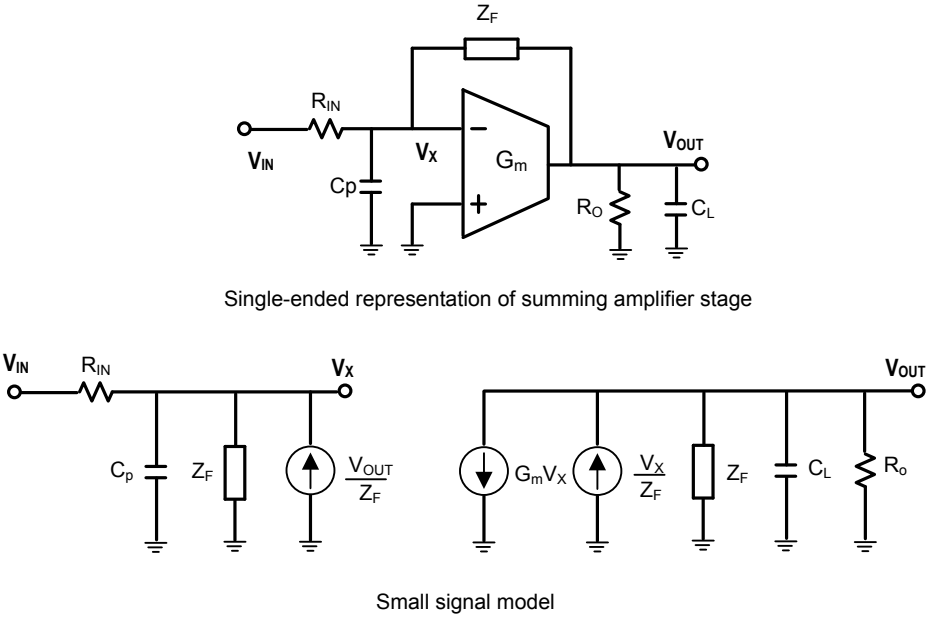


Figure 47 Simplified representation of the summing amplifier stage

The summing amplifier stage requires large bandwidth to provide minimum delay in the direct (fast) path. Due to the presence of parasitic poles at higher frequencies, the stability can become an issue. Therefore, the effect of parasitic poles on the loop gain needs to be analyzed. From the small signal model, the transfer function from input to output can be obtained as

$$\frac{V_{OUT}}{V_{IN}} = \frac{\text{Forward path}}{1 + \text{Loop Gain}} \tag{5.8a}$$

$$\text{Loop Gain} = \frac{Y_F}{Y_F + G_{IN} + sC_p} \frac{G_m - Y_F}{Y_F + G_O + sC_L} \tag{5.8b}$$

The single time constant model for the OTA $[G_m = G_{m0}/(1 + s/\omega_{p-OTA})]$ and resistive feedback, R_F ($1/G_F$), can be substituted in the expression for loop gain to get

$$\text{Loop Gain} = \frac{G_{m0}R_F - 1}{\left(1 + \frac{R_F}{R_O}\right)\left(1 + \frac{R_F}{R_{IN}}\right)} \frac{\left(1 - \frac{s}{(G_{m0}R_F - 1)\omega_{p-OTA}}\right)}{\left(1 + \frac{sC_p}{G_F + G_{IN}}\right)\left(1 + \frac{sC_L}{G_F + G_O}\right)\left(1 + \frac{s}{\omega_{p-OTA}}\right)} \tag{5.9}$$

From the above equation, there exist three poles in the left half-plane (LHP) and one zero in the right half-plane (RHP). The dominant pole is at the output of the amplifier due to the load capacitance, C_L. Other non-dominant poles exist due to the parasitic input capacitance, C_p, and the parasitic pole in the OTA. Furthermore, the pole present in the OTA gives rise to a RHP zero which degrades the phase response. In order to maintain stability at large bandwidths, it is required to push the unwanted poles and zero to the higher frequencies. The location of poles and RHP zero are given as

$$\omega_{\text{dominant}} = \frac{1}{C_L\,(R_F||R_O)} \tag{5.10a}$$

$$\omega_{\text{non-dominant 1}} = \frac{1}{C_p\,(R_F||R_{IN})} \tag{5.10b}$$

$$\omega_{\text{non}-\text{dominant }2} = \omega_{\text{p}-\text{OTA}} \tag{5.10c}$$

$$\omega_{\text{RHP}-\text{zero}} = (G_{m0}R_F - 1)\omega_{\text{p}-\text{OTA}} \tag{5.10d}$$

5.5.2 Summing amplifier design requirements

The summing amplifier is a critical analog block in the feed-forward sigma-delta architecture with a direct feedback path around the quantizer. For, the precise equivalence between discrete and continuous-time loop transfer functions, it is required to maintain exactly one sampling clock delay in the direct feedback path. This gives rise to stringent requirements for the design of summing amplifier. Assuming a single pole response of the amplifier and ignoring the effect of parasitic poles, the closed-loop transfer function of the summing node can be obtained as

$$\frac{V_{OUT}}{V_{IN}} = G_{m,eff}\, R_{out,eff} = -\left(\frac{G_m R_F - 1}{R_{IN} + R_F}\right)\frac{R_{OUT}}{1 + sC_L R_{OUT}} = -\frac{A_{CL}}{1 + sC_L R_{OUT}} \tag{5.11a}$$

$$A_{CL} = \frac{G_m R_F - 1}{G_m R_{IN} + 1} \tag{5.11b}$$

$$R_{OUT} = \frac{R_{IN} + R_F}{G_m R_{IN} + 1} \tag{5.11c}$$

The closed loop gain (A_{CL}) and equivalent output resistance (R_{OUT}) are expressed as given in equations (5.11b) and (5.11c). The closed-loop bandwidth ($f_{p,cl}$) is given by $1/(2\pi C_L R_{OUT})$. And, the phase response can be shown as

$$\Phi(\omega) = -\tan^{-1}\left(\frac{\omega}{\omega_{p,cl}}\right) \tag{5.12}$$

The delay introduced by the closed loop summing amplifier can be obtained by taking derivative of the phase response as given below

$$\tau_{delay} = -\frac{d\Phi(\omega)}{d\omega} = \frac{\omega_{p,cl}}{\omega^2 + \omega_{p,cl}^2} \tag{5.13}$$

The maximum loop-delay that can be tolerated in the direct path around the quantizer defines the bandwidth requirement for the amplifier as depicted in Fig. 48. It is known that the total loop delay must be one sampling clock period ($T_s = 1/F_s$). The quantizer and DAC introduce a half cycle delay and the maximum delay that can be tolerated in the summing stage is $T_s/2$. The summing amplifier should be able to handle both the in-band information coming from the filter and the feedback input coming from the secondary DAC.

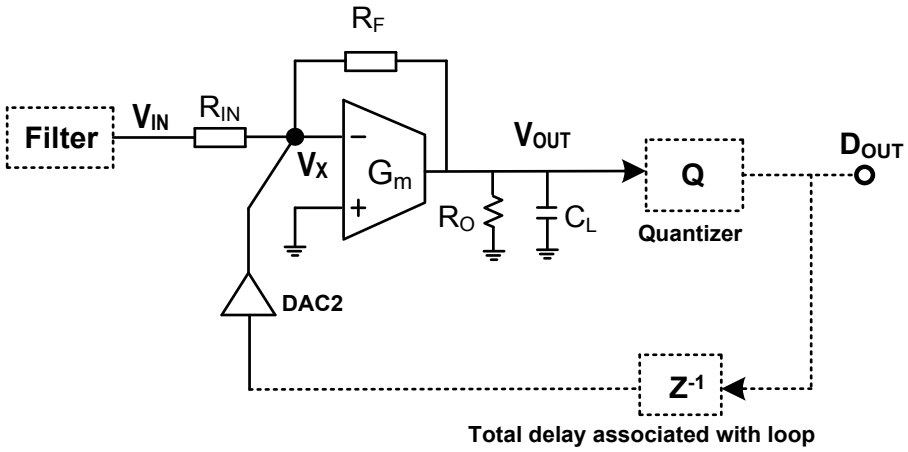


Figure 48 The direct path formed by summing stage around the quantizer

From the equation (5.13) it can be seen that the delay is a function of frequency and it reduces as the frequency increases. Therefore, the delay is most critical for the in-band information. Also, it should be noted that the group delay is almost constant for the in-band information. It is also required that the closed-loop bandwidth of the summing stage should be higher than the signal bandwidth (f_{sig}) to process the feedback information from the secondary DAC. Since $f_{p,cl} >> f_{sig}$, the tolerable delay in the summing amplifier can be approximated as given below

$$\tau_{delay} \approx \frac{1}{\omega_{p,cl}} = \frac{T_s}{2} \tag{5.14a}$$

$$\therefore \omega_{p,cl} = 2F_s \tag{5.14b}$$

Therefore, the unity gain bandwidth (f_{GBW}) requirement for the summing amplifier is given by

$$f_{GBW} = A_{CL} f_{p,cl} = A_{CL} F_s/\pi \tag{5.15}$$

However, there exist other elements in the loop such as the quantizer, feedback DAC and digital logic, which can add additional delay due to their non-ideal circuit behavior. In this case, the amplifier must be able to react much quicker and the tolerable delay requirement can be even less than $T_s/2$ for the amplifier. Table 18 summarizes the GBW requirement of the summing amplifier for various tolerable delay values. In this implementation, the closed-loop gain is $A_{CL} \simeq R_F/R_{IN} = 3$ with $F_s = 400$ MHz.

Table 18 GBW requirement for summing amplifier

Excess loop delay	Expression for GBW	GBW of Summing amplifier
$T_s/2$	$2*A_{CL}*F_s/2\pi$	400 MHz
$T_s/3$	$3*A_{CL}*F_s/2\pi$	600 MHz
$T_s/4$	$4*A_{CL}*F_s/2\pi$	800 MHz
$T_s/5$	$5*A_{CL}*F_s/2\pi$	1 GHz
$T_s/6$	$6*A_{CL}*F_s/2\pi$	1.2 GHz
$T_s/8$	$8*A_{CL}*F_s/2\pi$	1.6 GHz
$T_s/10$	$10*A_{CL}*F_s/2\pi$	2 GHz

Therefore, the bandwidth of the summing stage mainly depends on the RC time constant associated with the resistors that are used to perform the weighted addition of the integrator outputs. The load capacitance is the sample-and-hold capacitor required

for the quantizer block. The value of feedback resistor (R_F) is chosen in such a way that the unity gain frequency of the summing stage is at least five times the sampling frequency. The input resistor R_{IN} is calculated from the coefficients required for each stage. Further reduction in R_F (and hence R_{IN}) increases the power consumption in the amplifiers used in the integrator stages, which have to drive equivalent load of the feedback network.

The open loop DC gain requirement of the summing amplifier comes from the tolerable error in the final value at the output of the summing amplifier. If A_{DC} is open loop DC-gain of the amplifier and β is the feedback factor, then the output of the amplifier can be expressed as

$$V_{OUT} = -\frac{R_F/R_{IN}}{1+\frac{1}{\beta A_{DC}}} \approx -\frac{R_F}{R_{IN}}\left(1-\frac{1}{\beta A_{DC}}\right) \tag{5.16}$$

Therefore, the percentage error of the final output is given below.

$$\varepsilon = \frac{1}{\beta A_{DC}} \times 100\% \tag{5.17}$$

The tolerable error in the final value is mainly defined by the quantizer threshold. For this design, a DC gain of 25dB was chosen, which ensures 10% or less static error in final value. It should be noted that this error is less significant because it is noise shaped by the sigma-delta operation.

5.5.3 Optimizing for group delay

The block-level implementation diagram of the summing node is shown in Fig. 49. The feedback network of the amplifier creates a zero-pole pair which introduces positive excess phase in the overall transfer function. This can be used to adjust for the group delay of the summing node. The capacitor C_T can be tuned to optimize the loop delay in the direct path consisting of summing amplifier, quantizer and the secondary feedback DAC. The impedance of the feedback network can be expressed as

$$Z_F = R_F \left[\frac{1 + {}^{s}/_{\omega_z}}{1 + {}^{s}/_{\omega_p}} \right] \tag{5.18a}$$

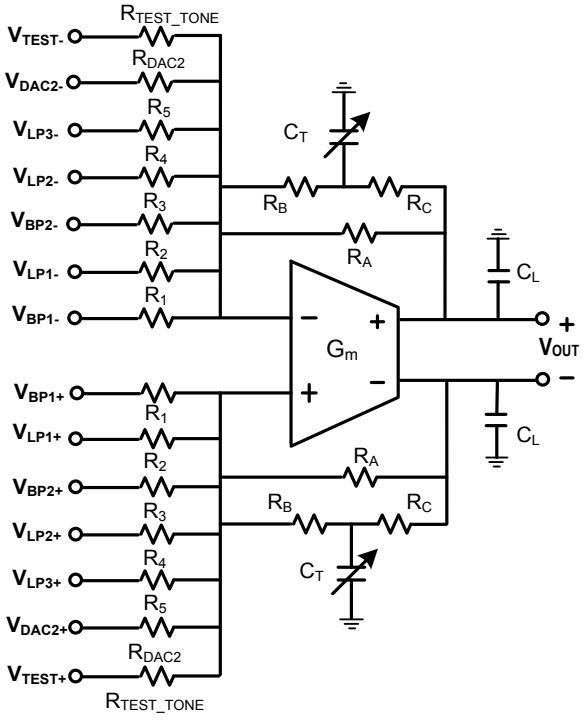


Figure 49 Block diagram of the summing amplifier stage

The expression of the frequency of the zero (ω_z), frequency of pole (ω_p) and low-frequency resistance (R_F) are given below.

$$\omega_z = \frac{R_B + R_C}{R_B . R_C . C_T} \tag{5.18b}$$

$$\omega_p = \frac{R_A + R_B + R_C}{R_B . R_C . C_T} \tag{5.18c}$$

$$R_F = \frac{R_A . (R_B + R_C)}{R_A + R_B + R_C} \tag{5.18d}$$

Assuming an ideal amplifier and ignoring the effect of parasitic capacitances, the overall transfer function of the summing stage (with all inputs tied to V_{IN}) is obtained as

$$\frac{V_{OUT}}{V_{IN}} = \left(\frac{G_m Z_F - 1}{G_m R_{IN} + 1}\right)\left[\frac{1}{1 + sC_L R_{OUT}}\right] \tag{5.19a}$$

where the equivalent input resistance (R_{IN}) is given by equation (5.19b) and equivalent output resistance is given by

$$R_{IN} = (R_1 \,||\, R_2 \,||\, R_3 \,||\, R_4 \,||\, R_5 \,||\, R_{DAC} \,||\, R_{TEST\ TONE}) \tag{5.19b}$$

$$R_{OUT} = \frac{R_{IN} + R_F}{G_m R_{IN} + 1} \tag{5.19c}$$

In equation (5.19a), the dominant pole can be computed by assuming that $Z_F = R_F$ (since the zero-pole pair is at high frequency) and the effect of zero-pole pair can be investigated by considering the first term.

$$\frac{G_m Z_F - 1}{G_m R_{IN} + 1} \approx \frac{G_m R_F - 1}{G_m R_{IN} + 1}\left[\frac{1 + {}^{S}/_{\omega_z}}{1 + {}^{S}/_{\omega_p}}\right] \tag{5.20a}$$

Therefore, the transfer function is obtained as

$$\therefore \frac{V_{OUT}}{V_{IN}} = \left(\frac{G_m R_F - 1}{G_m R_{IN} + 1}\right)\left[\frac{1 + {}^{s}/_{\omega_z}}{1 + {}^{s}/_{\omega_p}}\right]\left[\frac{1}{1 + sC_L R_{OUT}}\right] \quad (5.20b)$$

where ω_z and ω_p are given by equations (5.18b) and (5.18c). The component values of summing stage of loop filter are listed in Table 19.

Table 19 Component values of summing amplifier stage of loop filter

Parameter	Value
R_1	1.700 kΩ
R_2	2.875 kΩ
R_3	2.700 kΩ
R_4	2.530 kΩ
R_5	2.050 kΩ
R_{DAC2}	4.000 kΩ
R_{TEST_TONE}	20.00 kΩ
R_A	3.000 kΩ
R_B	3.000 kΩ
R_C	3.000 kΩ
C	80fF – 320fF

The feedback network with zero-pole pair will not affect the loop stability significantly because the zero-pole pair is placed at frequencies higher than the bandwidth of the summing amplifier. However, it introduces negative group delay at low frequencies. The phase (Φ) of the transfer function is obtained as

$$\Phi(f) = \tan^{-1}\left(\frac{\omega}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega}{\omega_p}\right) \quad (5.21)$$

Therefore, the group delay (τ_{delay}) can be obtained as the derivate of the phase.

$$\tau_{delay} = -\frac{d\Phi(\omega)}{d\omega} = -\frac{(\omega_z - \omega_p)(\omega^2 - \omega_z\omega_p)}{(\omega^2 + \omega_z^2)(\omega^2 + \omega_p^2)} \tag{5.22a}$$

At frequencies lower than the unity gain bandwidth of the amplifier (and hence lower than the frequency of zero and pole) the group delay can be simplified as

$$\tau_{delay} \approx \left(\frac{1}{f_p} - \frac{1}{f_z}\right) \tag{5.22b}$$

Therefore, the group delay introduced is negative (since $f_p < f_z$) and the feedback network reduces the group delay of the summing stage at lower frequencies. The group delay can be adjusted by changing the zero and pole frequencies via tuning of the capacitor C_T. Furthermore, the introduction of the zero-pole pair increases the group delay of the amplifier at higher frequencies (above unity gain frequency). However, this effect can be minimized by choosing the location of zero-pole pair at frequencies higher than unity gain frequencies. This reduces the tunable range of the group delay. This is due to the fact that the higher the frequencies of the zero-pole pair the lower their effect on the group delay of the amplifier at low frequencies. It should be noted that the group delay is constant for the in-band information. The tuning of group delay by adjusting capacitor C_T is shown in Fig. 50.

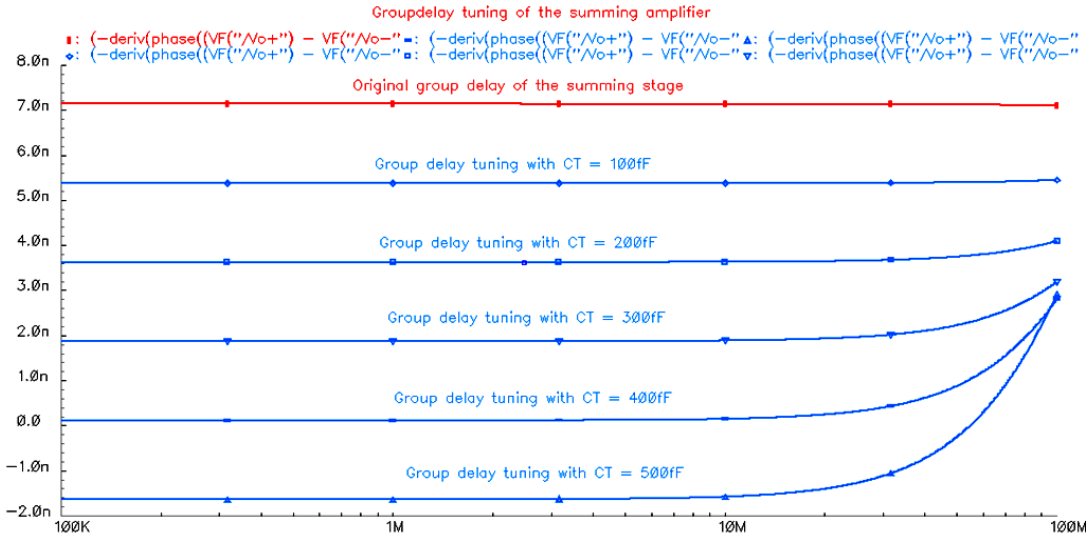


Figure 50 Tuning of group delay using C_T in direct (fast) path

The step response of the summing stage with and without the addition of zero-pole pair is shown in Fig. 51. It is observed that the rise time decreases with the tuning of the capacitor C_T to change the location of zero-pole pair.

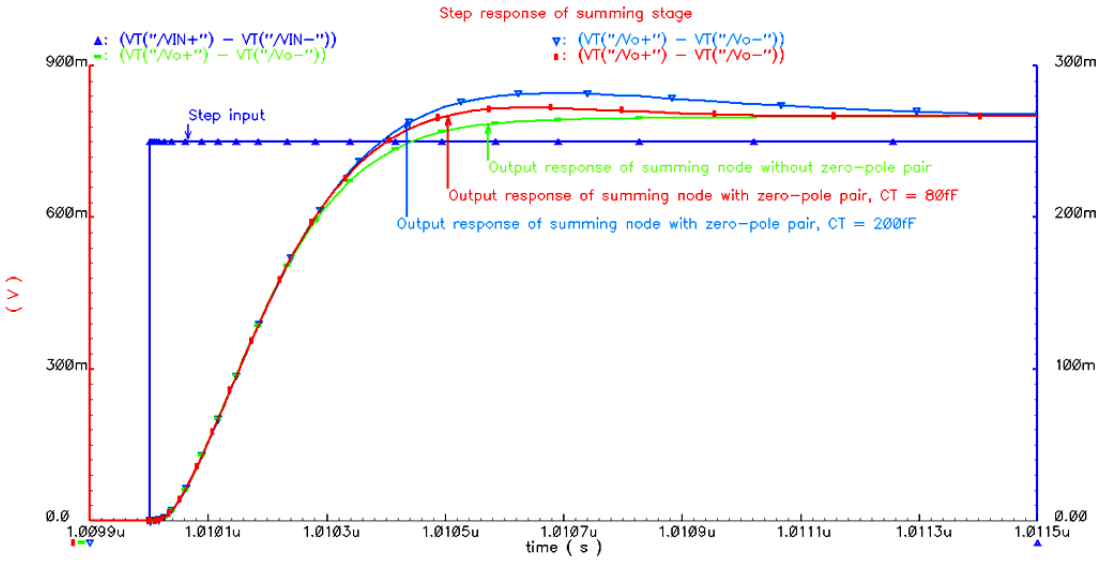


Figure 51 Step response of the amplifier stage

5.5.4 Circuit implementation of summing amplifier

The main concern in the design of the summing amplifier is the large bandwidth requirement. High speed is necessary because the summing amplifier is a critical block in the direct path. The linearity and noise requirements of the summing amplifier are not as stringent as $the filter because these errors are noise-shaped. The DC-gain specification of the summing amplifier should be such that the error in the weighted addition of integrator outputs is minimized. A gain of around 25dB is required to in order to attenuate the kickback effects, i.e. digital glitches from the comparators that couple back to the filter [27]. The fully-differential circuit implementation of the amplifier is shown in Fig. 52.

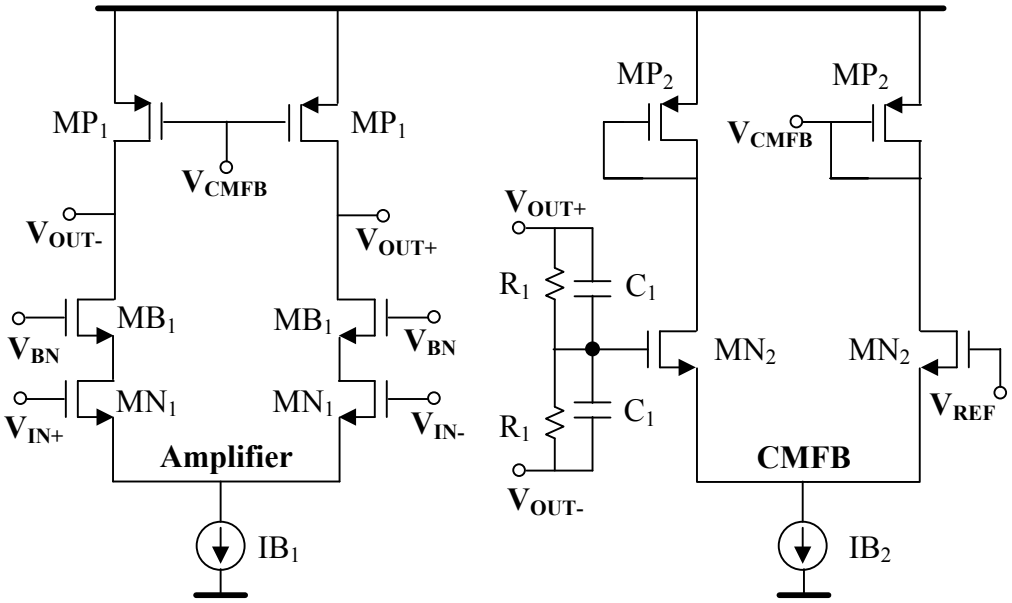


Figure 52 Schematic of the amplifier in loop filter

To satisfy the large bandwidth requirements and low gain requirement, a single stage amplifier (MN_1, MB_1 and MP_1) is used. The DC level at the output of the amplifier is controlled using a common-mode feedback circuit (MN_2, MP_2). The output common-mode level is detected by a resistive averaging using R_1, and the common-mode error is

fed back to the node V_{CMFB} to regulate the output level to 1.1 V. The stability of the common-mode loop is enhanced by adding a small capacitor C_1 that introduces LHP zero in the common-mode loop. The component values and parameters for the summing amplifier are listed in Table 20.

Table 20 Transistor dimensions, device values and bias conditions for amplifier

Device	Dimensions
MN_1	(5) 20 µm / 180 nm
MB_1	(1) 96 µm / 200nm
MP_1	(15) 8.4 µm / 200 nm
MN_2	(6) 16 µm / 300 nm
MP_2	(2) 8.4 µm / 200 nm
IB_1	5 mA
IB_2	600 µA
R_1	80 KΩ
C_1	100 fF

5.5.5 Summing amplifier simulation results

The performance parameters of the summing amplifier are summarized in Table 21.

Table 21 Important performance parameters of the summing amplifier

Performance parameter	**Value**
DC-gain	26 dB
Gain bandwidth product	3.5 GHz
Input referred integrated noise (in 25 MHz)	44.65 µV
IM3 ($600mV_{p-p}$)	-62 dB
Power consumption	10 mW

The simulated open-loop AC response of the amplifier is shown in Fig. 53. The phase margin is 75^{o} at unity gain frequency of 3.5 GHz and the DC gain is 26dB.

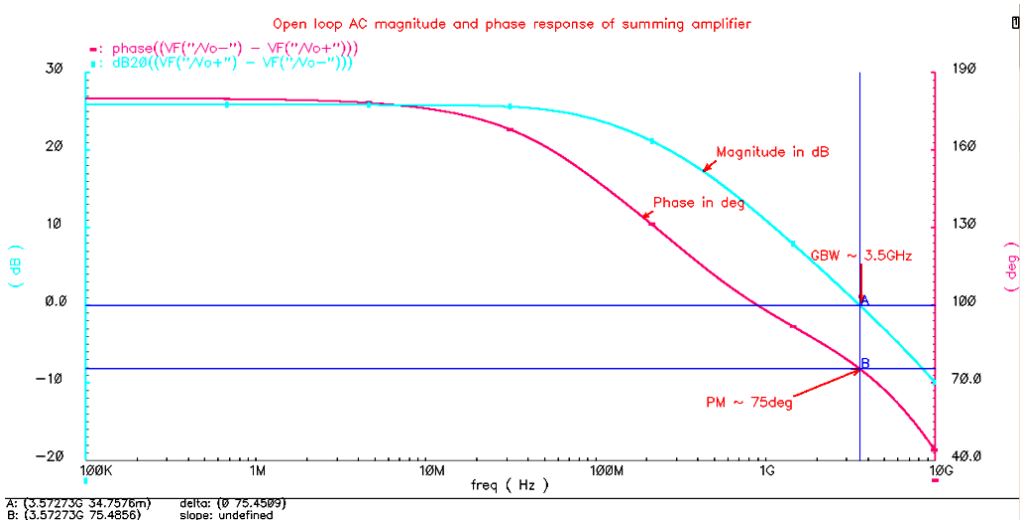


Figure 53 Open-loop AC response of the summing amplifier

Simulation result showing the closed loop AC response of the summing stage with and without the introduction of zero-pole pair in the feedback network is shown in Fig. 54.

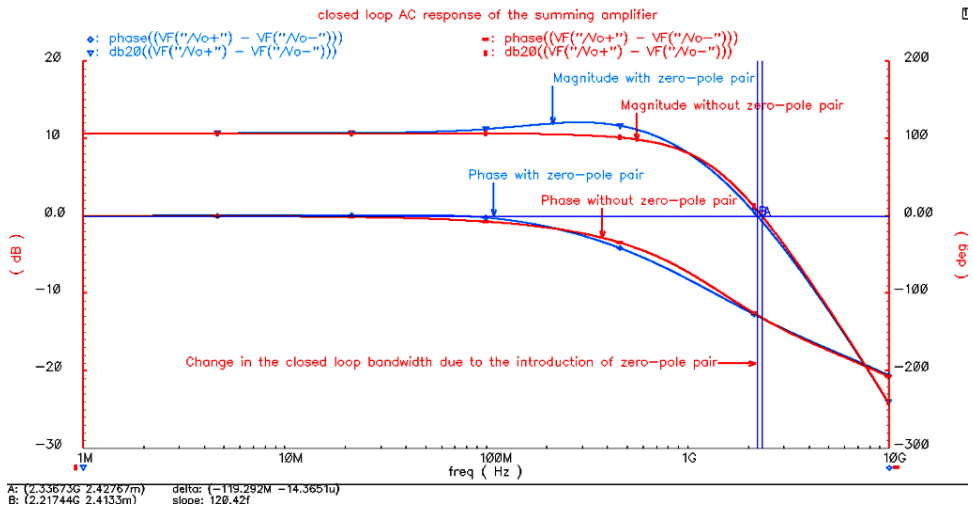


Figure 54 Closed-loop AC magnitude and phase response of the summing stage

The linearity of the summing stage was measured with two-tone test, and the simulated IM3 is 62dB as marked in Fig. 55.

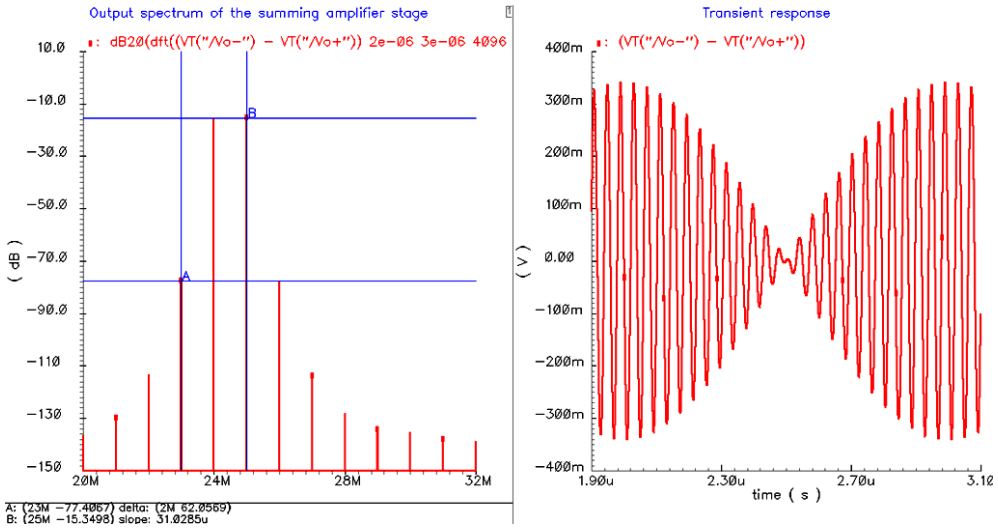


Figure 55 Linearity test of the summing amplifier, V_{out} = 600mV_{p-p}

6. RESULTS

6.1 Preliminary experimental results of CT LP ΣΔ ADC

The micrograph of the continuous-time low-pass sigma-delta modulator including all the building blocks is shown in Fig. 56. The analog and digital parts of the system are separated by guard rings to protect the sensitive analog modules from noisy digital blocks. The total silicon area of the modulator is 2.66mm × 2.08mm. The ADC was fabricated in 0.18µm CMOS technology thanks to Jazz semiconductors for providing the sponsorship.

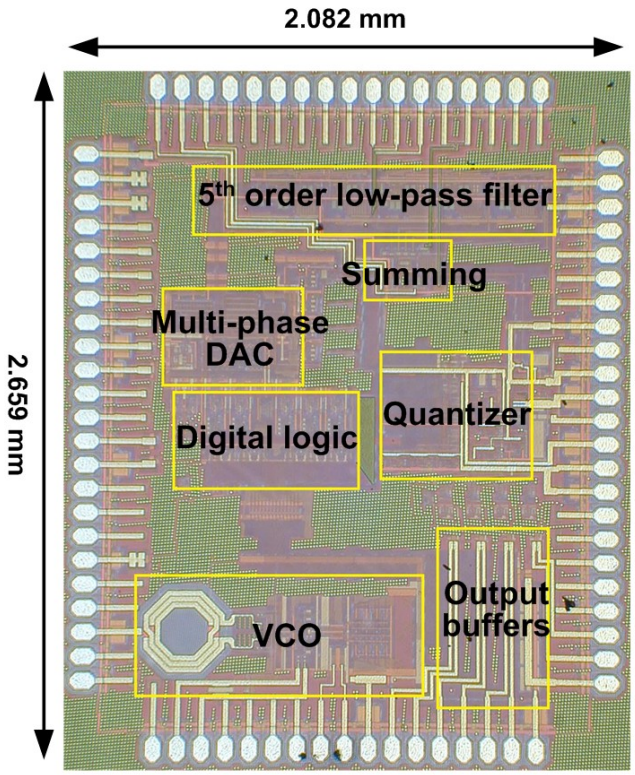


Figure 56 Chip micrograph of the CT LP SD ADC in CMOS 0.18µm technology

The layout of the 5th order lowpass filter designed for continuous-time sigma-delta ADC is shown in Fig. 57. The first stage is located such that the routing distance

from the input PADs is minimized. Summing amplifier is located very close to the DAC in order to reduce the routing parasitics in the fast path of the sigma-delta loop. Since the system contains digital circuits such as Quantizer, DAC, and digital logic, a guard ring is placed to separate the analog filter. The total area of the filter and summing node is approximately 1300µm × 600 µm.

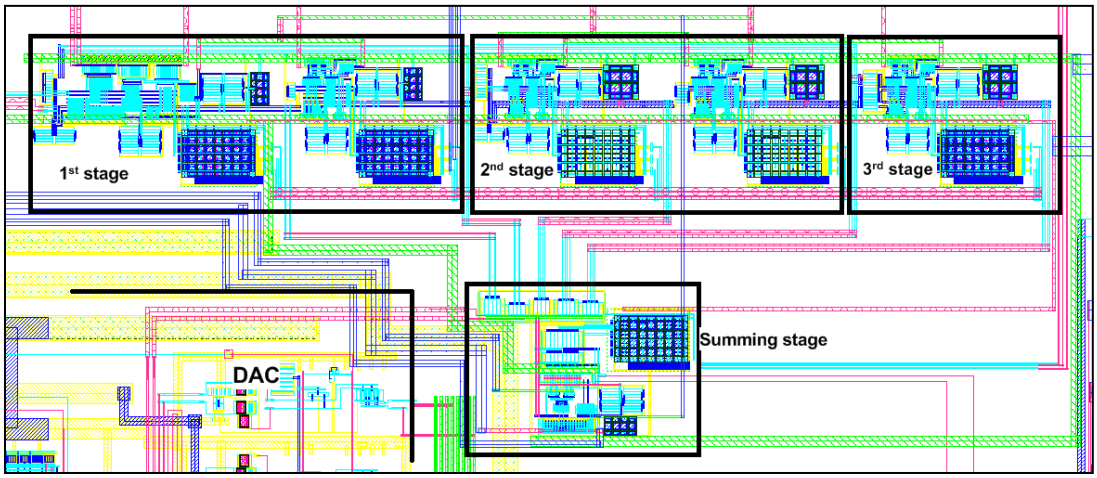


Figure 57 Layout of the fifth order low-pass filter

A picture of the printed circuit board (PCB) used testing and measuring the performance of CT LP SD ADC is shown in Fig. 58. The output spectrum of ADC with a -0.2dBFS input tone at 5.08MHz showing the noise shaping of sigma-delta ADC obtained from the experimental results is presented in Fig. 59. From experimental results, SNDR of 67.7dB is obtained for in 25MHz bandwidth.

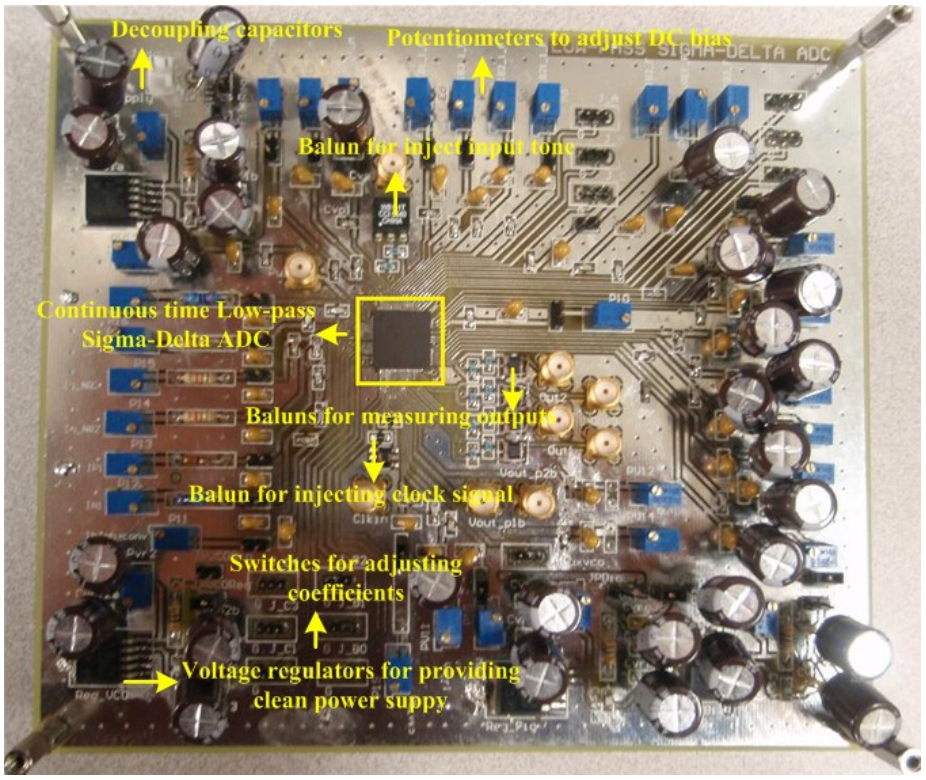


Figure 58 PCB test set-up for measuring the performance of CT LP SD ADC

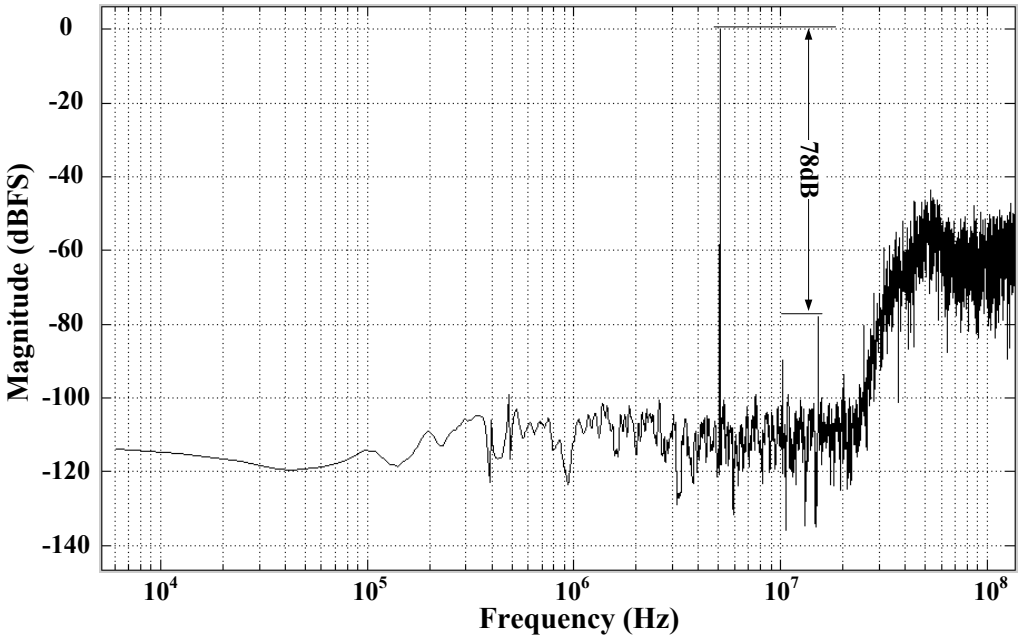


Figure 59 Output spectrum of CT LP SD ADC from experimental results

6.2 Simulation results for the 5th order low-pass filter

The important performance parameters of the 5th order loop filter obtained from post-layout simulation results are summarized in Table 22.

Table 22 Important performance parameters of the 5th order loop filter

Performance parameter	Value
DC-gain	48 dB
Cut-off frequency	24.5 MHz
Input referred integrated noise (in 25 MHz)	42.2 µV
IM3 (260mV$_{pp}$ at the output of summing node)	-72.5 dB
Power consumption	21.3 mW
Area	1300 µm × 600 µm
CMOS Technology	0.18 µm

Fig. 60 presents the magnitude and phase response of the complete loop filter.

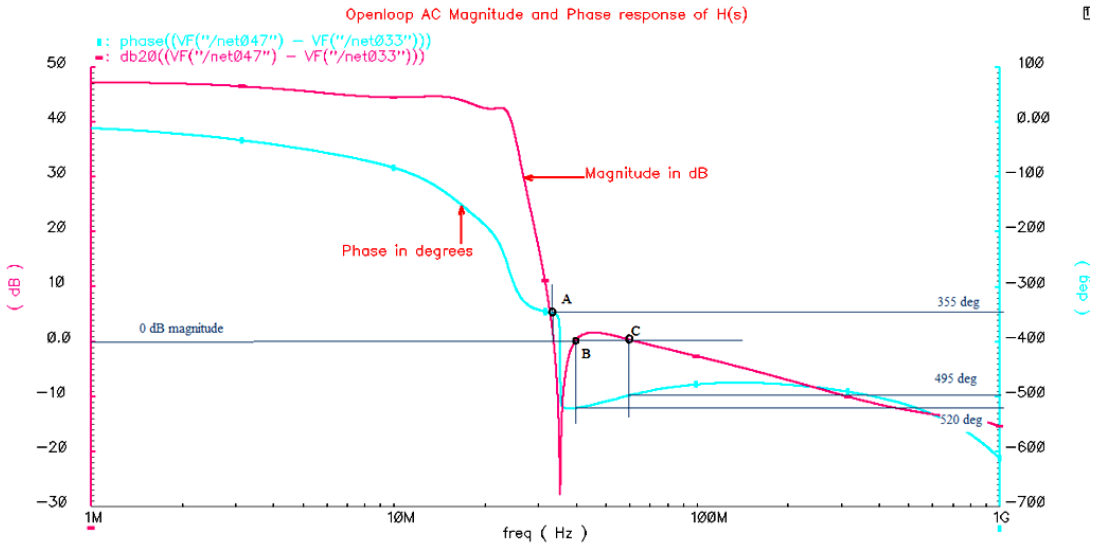


Figure 60 AC magnitude and phase responses of open loop filter [H(s)]

The secondary DAC feedback provides an additional zero in the overall loop filter transfer function and its effect is shown in Fig. 61. The coefficient of the DAC feedback is used approximately as 0.5.

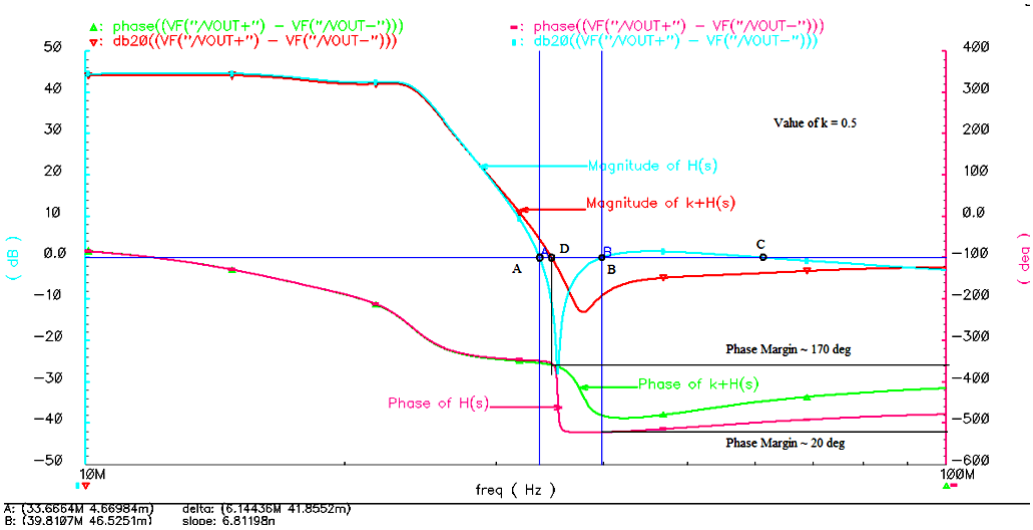


Figure 61 AC magnitude and phase responses of open loop filter transfer function [H(s)] and the effect of secondary DAC feedback [0.5+H(s)]

6.2.1 Simulation results for first stage of filter

The simulation results for the first stage of the filter are presented in this section. The AC magnitude and phase responses are shown in Fig. 62. The first biquadratic section is designed to have DC gain 15.5dB, quality factor 7.5 and cut-off frequency 24.5 MHz.

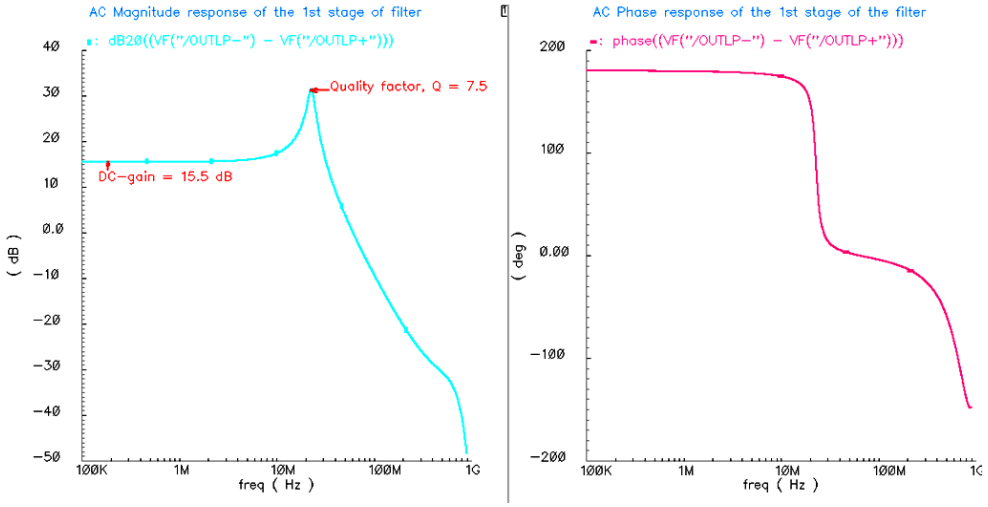


Figure 62 AC Magnitude and Phase response of the 1st stage of the filter

Fig. 63 shows the frequency tuning of the first stage of the filter using a bank of capacitors. The center frequency can be varied from 16MHz to 31MHz in 8 steps.

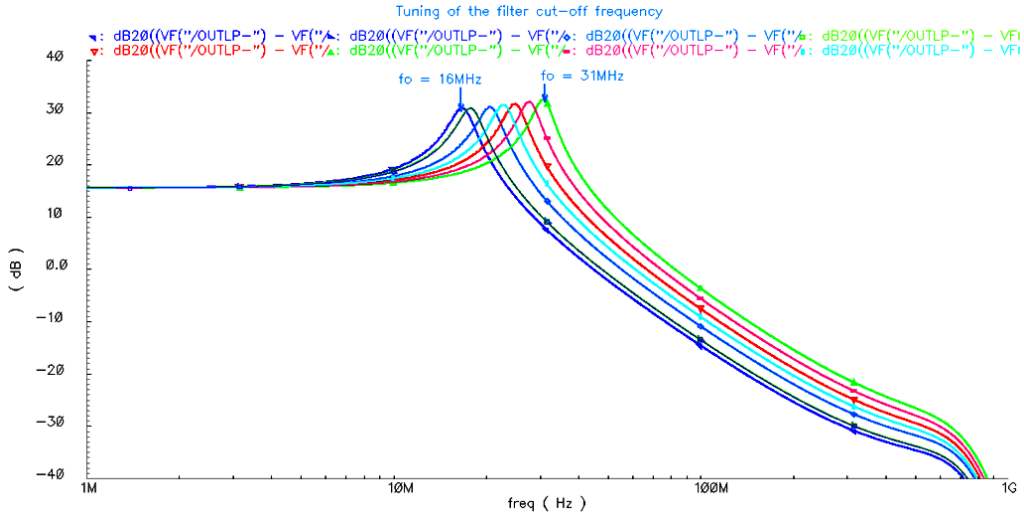


Figure 63 Tuning of cut-off frequency of first stage between 16MHz and 31MHz

Fig. 64 shows the step response of the first biquadratic section. An input step with 100mV differential amplitude is applied. The output faithfully follows the input and the amplitude is 600mV which corresponds to a gain of 15.56 dB.

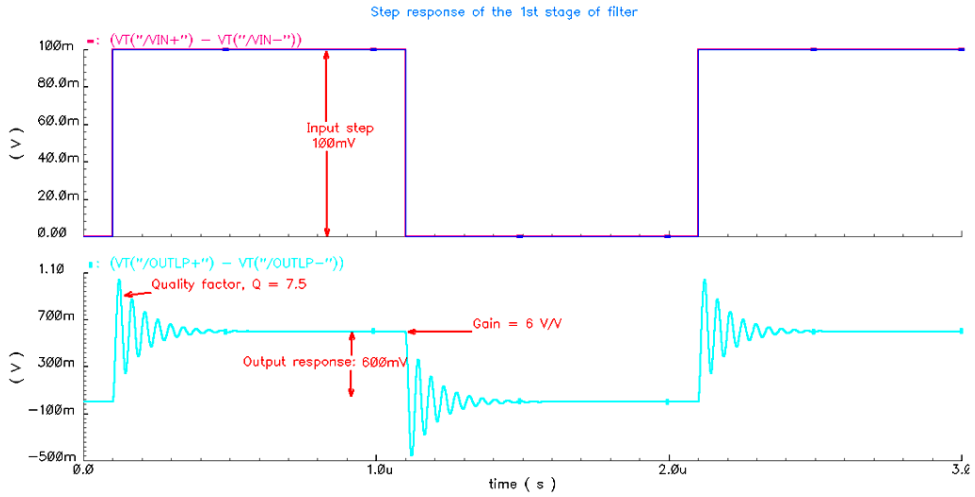


Figure 64 Step response of the first stage of the filter

Fig. 65 shows the output spectrum obtained from two-tone test for linearity measurement of first biquadratic section. Two input tones at frequencies 22.5MHz and 23.5MHz are applied and IM3 of -73.5dB is measured for output amplitude of 400mV$_{p\text{-}p}$.

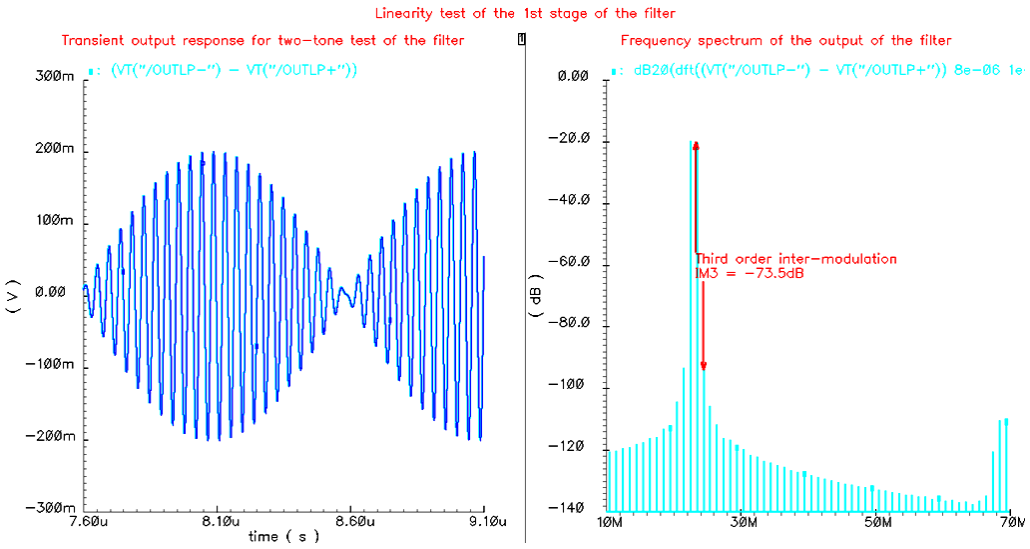


Figure 65 Linearity test of the first stage of the filter, Vout = 400mV$_{p\text{-}p}$

The total input referred integrated noise of the first biquadratic section is found to be 41.7 µV in 25 MHz bandwidth. The main noise contribution comes from the input

resistors of the two-integrator loop biquad. Fig. 66 presents the input referred integrated noise summary.

Window Expressions Info Help 58

Device	Param	Noise Contribution	% Of Total
/R0	rn	0.000362596	29.07
/R1	rn	0.000362596	29.07
I98.M17.mds	id	0.000168991	6.31
I98.M16.mds	id	0.000168991	6.31
/R5	rn	0.000147499	4.81
/R4	rn	0.000147499	4.81
/R7	rn	0.000135571	4.06
/R6	rn	0.000135571	4.06
I98.M11.mds	id	0.000123613	3.38
I98.M0.mds	id	0.000123613	3.38

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.000672556
Total Input Referred Noise = 4.16966e-05
The above noise summary info is for noise data

Figure 66 Input-referred integrated noise of the first stage of the filter in 25MHz bandwidth

Fig. 67 shows the input referred noise spectral density of the first biquadratic section. The in-band noise spectral density is approximately 8nV/√Hz at 25MHz.

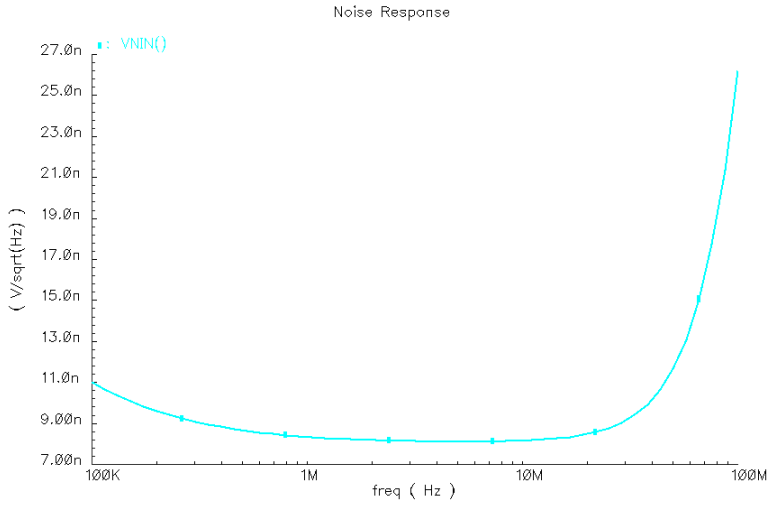


Figure 67 Input referred noise density of the first stage of the filter

6.2.2 Simulation results for second stage of filter

The simulation results for the second stage of the filter are presented in this section. The AC magnitude and phase responses are shown in Fig. 68. The second biquadratic section is designed to have DC gain 15.5dB, quality factor 1.55 and cut-off frequency 16.7 MHz.

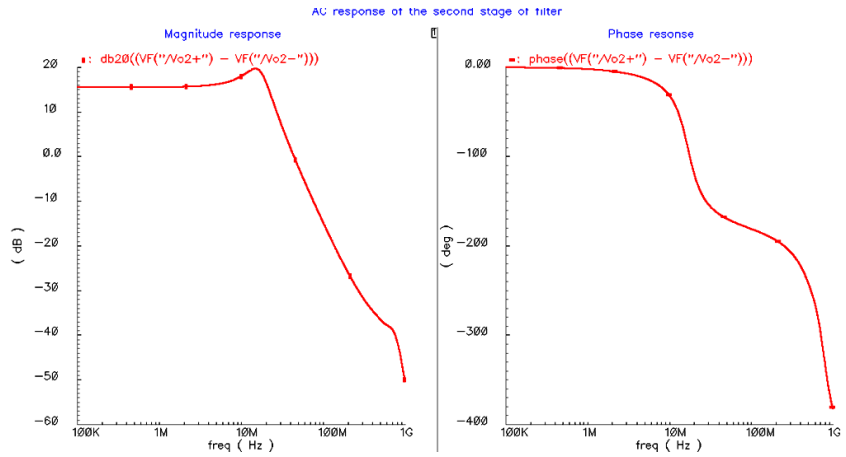


Figure 68 AC Magnitude and Phase response of the 2nd stage of the filter

Fig. 69 shows the frequency tuning of the second stage of the filter using a bank of capacitors. The center frequency can be varied from 11.5MHz to 19.5MHz in 8 steps.

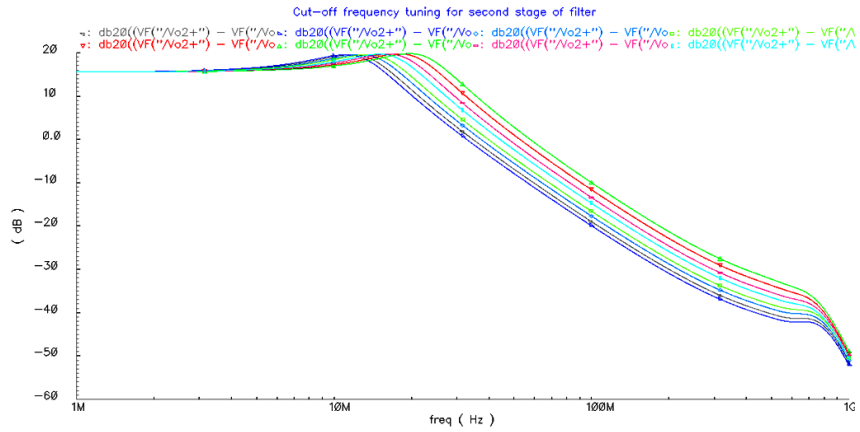


Figure 69 Tuning of cut-off frequency of second stage between 11.5MHz and 19.5MHz

Fig. 70 shows the step response of the second biquadratic section. An input step with 100mV differential amplitude is applied. The output faithfully follows the input and the amplitude is 600mV which corresponds to a gain of 15.56 dB.

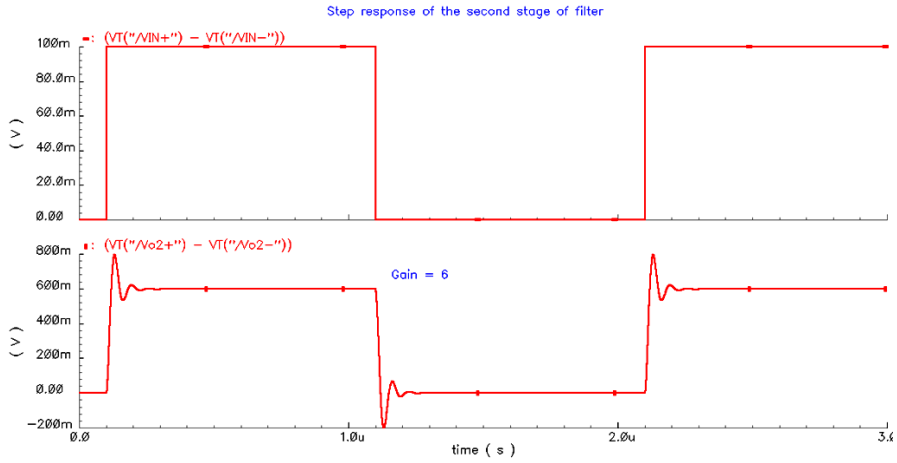


Figure 70 Step response of the second stage of the filter

Fig. 71 shows the output spectrum obtained from two-tone test for linearity measurement of first biquadratic section. Two input tones at frequencies 13MHz and 14MHz are applied and IM3 of -82.3 dB is measured for output amplitude of 600mV$_{p\text{-}p}$.

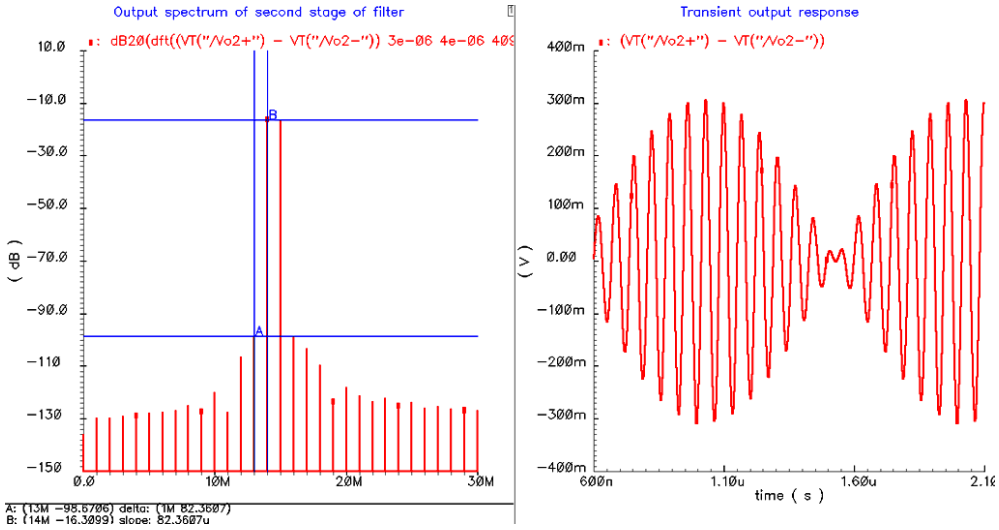


Figure 71 Linearity test of the second stage of the filter, Vout = 600mV$_{p\text{-}p}$

6.2.3 Simulation results for third stage of filter

The simulation results for the third stage of the filter are presented in this section. The AC magnitude and phase responses are shown in Fig. 72.

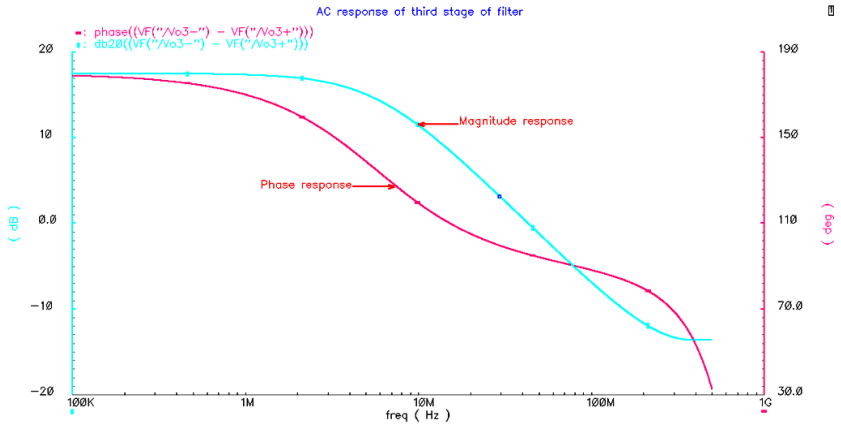


Figure 72 AC response of the third stage of the filter

The third stage is designed to have DC gain 17.7 dB and cut-off frequency 5.7 MHz. Fig. 73 shows the frequency tuning of the third stage of the filter using a bank of capacitors. The center frequency can be varied from 4.2MHz to 7.8MHz in 8 steps.

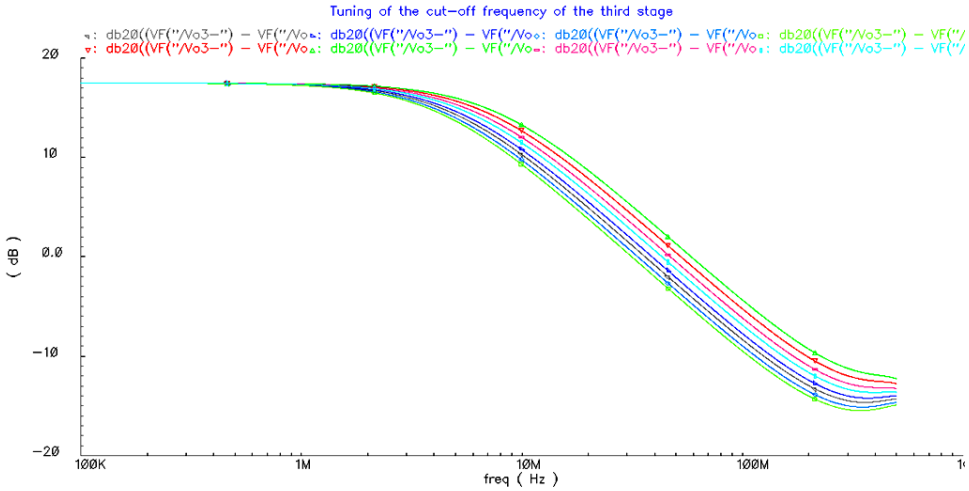


Figure 73 Tuning of cut-off frequency of third stage of filter from 4.2MHz to 7.8MHz

Fig. 74 shows the step response of the third stage of the filter. An input step with 100mV differential amplitude is applied. The output faithfully follows the input and the amplitude is 750mV which corresponds to a gain of 17.7 dB.

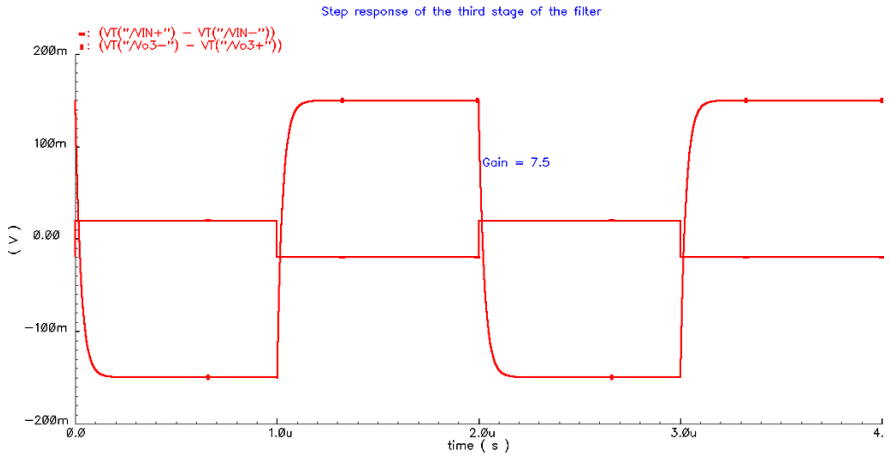


Figure 74 Step response of the third stage of the filter

Fig. 75 shows the output spectrum obtained from two-tone test for linearity measurement of first biquadratic section. Two input tones at frequencies 1MHz and 2MHz are applied and IM3 of -72.3 dB is measured for output amplitude of 600mV$_{p\text{-}p}$.

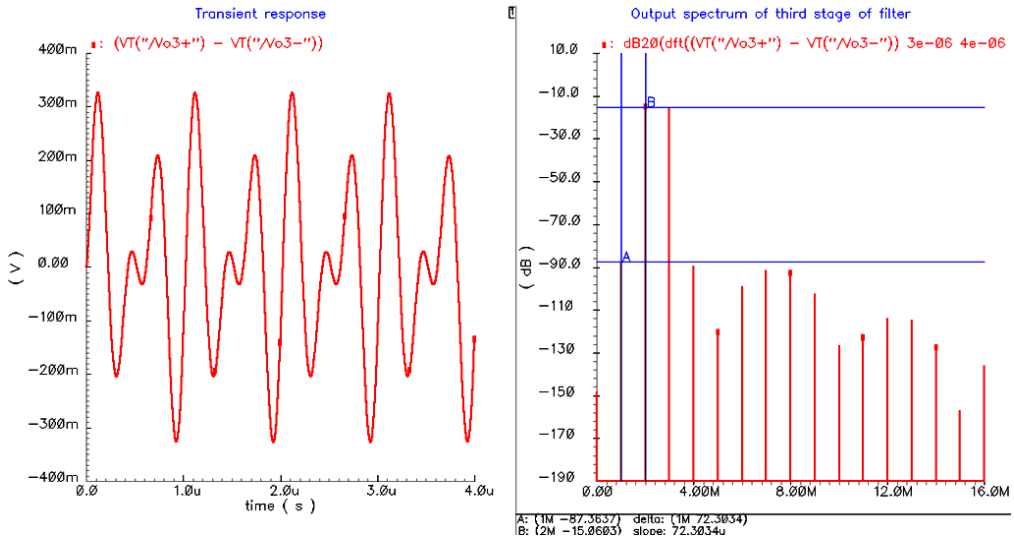


Figure 75 Linearity test of the third stage of the filter, Vout = 600mV$_{p\text{-}p}$

7. SUMMARY AND CONCLUSIONS

The sigma-delta modulator has become popular as digital-friendly ADC architecture because a substantial part of the signal processing is performed in the digital domain. In continuous-time sigma-delta ADC the sampling operation is performed after the loop filter. Hence, image signal rejection can be achieved with higher-order loop filtering. The performance of a continuous-time sigma-delta ADC mainly depends on its architecture and the implementation of the analog loop filter. The two popular techniques for the implementation of continuous-time filters are active RC and G_m-C.

In this work, the design considerations for the loop filter in low-pass CT ΣΔ ADCs were presented. Sigma-delta ADC with resolution of 12-bits in 25MHz bandwidth and low power consumption was implemented in 0.18μm CMOS technology. A fifth-order low-pass filter with cut-off frequency of 25 MHz was designed using an active-RC topology to meet the dynamic range requirement of the ADC. The design of a summing amplifier and a novel method for adjusting the group delay in the fast path provided by a secondary feedback DAC of the ΣΔ ADC were discussed in detail. The first biquadratic section demands for larger linear range which can allow increased internal signal strength without consuming significant static power. The amplifiers and components used in the second and third stages have relaxed specifications and are scaled to save power. Further saving in power can be achieved by using single OPAMP multiple feedback architectures for implementing biquadratic sections. The ADC was fabricated using Jazz 0.18μm CMOS technology.

Theoretical analysis and implementation issues of OTAs were presented with emphasis on high-linearity and low-noise performance suitable for the broadband ADC applications. Important design equations pertaining to the linearity and noise performance of the G_m-C biquad filters were derived. A G_m-C biquad with 100MHz center frequency and quality factor 10 was designed as a prototype to confirm with the theoretical design equations. It was shown that the linearity of the biquad depends on the frequency separation between the input-tones used for IM3 measurement. Non-linear

source degeneration improves the linearity (IM3) of the filter by 10dB. The linearity of the G_m-C biquadratic filters can be further enhanced by improving the linearity of the output stage. Transistor level circuit implementation of all the analog circuits was completed in a 0.18μm CMOS process.

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VITA

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