A BEHAVIORAL MODEL OF A BUILT-IN CURRENT SENSOR FOR I_{DDQ} TESTING

A Thesis

by

AMMAR GHARAIBEH

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2009

Major Subject: Computer Engineering

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Approved by:

Co-Chairs of Committee,	Duncan M. (Hank) Walker
	Jiang Hu
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ABSTRACT

A Behavioral Model of a Built-in Current Sensor for I_{DDQ} Testing.

(August 2009)

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Co-Chairs of Advisory Committee: Dr. Duncan M. (Hank) Walker
Dr. Jiang Hu

I_{DDQ} testing is one of the most effective methods for detecting defects in integrated circuits. Higher leakage currents in more advanced semiconductor technologies have reduced the resolution of I_{DDQ} test. One solution is to use built-in current sensors. Several sensor techniques for measuring the current based on the magnetic field or voltage drop across the supply line have been proposed. In this work, we develop a behavioral model for a built-in current sensor measuring voltage drop and use this model to better understand sensor operation, identify the effect of different parameters on sensor resolution, and suggest design modifications to improve future sensor performance.

DEDICATION

To my family who always believed in me encouraged me and supported me through everything.

ACKNOWLEDGMENTS

First of all, I thank God for all his blessings. I thank God for the gift of patience He gave me to do this research and I thank Him for the opportunity to meet all kinds of people through the research process.

Second of all, I thank my advisor Dr. Duncan M. (Hank) Walker for his guidance and patience in the last two years. It is been a pleasure working under such a great Professor.

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TABLE OF CONTENTS

Page

Page

LIST OF FIGURES

Page

Page

LIST OF TABLES

Page

1. INTRODUCTION

1.1 Introduction

The process in which defects in integrated circuits (ICs) are detected is called *testing*. With the rapid advance in semiconductor technology, the increasing number of transistors and the increase in circuit complexity, there is a constant need to improve test methods, test speed, test cost and defect coverage.

Currently, test cost constitutes more than 25% of the overall chip manufacturing cost, and it is increasing due to the increase in circuit complexity. In order to contain test cost, more advanced test methods must be developed. Such advances include reducing the test time per transistor and increasing defect coverage. The test time per transistor must fall so that the total test time per chip remains constant as transistor count increases. Increasing the defect coverage is necessary to maintain overall outgoing chip quality with rising transistor counts.

Integrated circuit tests are applied in a series of steps during design and manufacturing. These tests are shown in Fig. 1.

This thesis follows the style and format of *IEEE Transactions on Very Large Scale Integration (VLSI) Systems.*

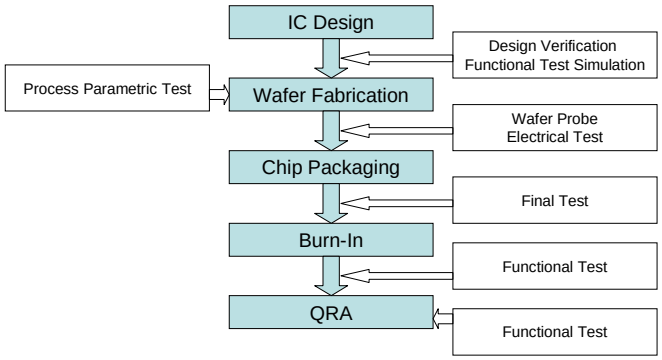

Fig. 1. IC Test Locations. [1]

During the design process, tests are applied to ensure that the design matches the specifications. These tests are applied via simulation to different levels of design abstractions, and their results compared. After manufacturing, chips are tested while still on wafers (wafer test) to detect most defects. These tests primarily detect defects that cause the chip to fail to function correctly. Chips that pass wafer test are then packaged and subject to final testing. The final test may be applied at different temperatures and voltages at full speed, to ensure that the chip operates at its rated speed over the environmental range. Optionally, chips may be subject to burn-in to accelerate early life failures, and then tested again. Samples of chips are selected for extensive testing for quality and reliability assurance (QRA).

1.2 Terms of Testing

Testing is done on integrated circuits in order to detect defects that occur during manufacturing. Examples of defects include shorts and opens in interconnect. The electrical behavior of these defects can be modeled as *faults*, such as a net stuck at a logic 0 or stuck at a logic 1. Tests can be divided into two groups: *Boolean tests* and *parametric tests*. In Boolean tests, a set of input vectors are fed to the Circuit Under Test

(CUT) and the corresponding outputs are observed. A fault is detected when the output response is different from the desired one. Boolean tests can be divided into *structural tests* and *functional tests*. Structural tests are generated using knowledge of the circuit structure and fault models. For example, a stuck-at fault test set is designed to detect stuck-at-0 and stuck-at-1 faults on all the gate inputs and outputs of the circuit. Other fault models that can be used include *bridging faults*, which model shorts between wires, and stuck-open faults, which model opens in wires. Functional tests test the correct function of the circuit against the specification, for example, that an adder will add correctly.

Parametric tests are used to measure continuous value parameters of the CUT, such as power consumption, operating voltage range, and maximum delay. Most parameters have specified acceptable ranges, outside of which the CUT is rejected. Even if the parameters are within the acceptable range, they might be far different from those of the general population, and so the CUT is termed an *outlier*. Research has shown that outlier chips are much more likely to fail during customer operation.

2. BACKGROUND

2.1 Introduction

In this section, the principles and the details of I_{DDQ} testing will be discussed along with its advantages and challenges.

2.2 Basics of I_{DDQ} Test

When CMOS circuits are in their quiescent state, there is a quiescent (I_{DDQ}) or leakage current from V_{DD} to GND due to subthreshold and gate oxide leakage in the transistors. This leakage varies exponentially with process parameters, temperature and voltage. In older and very low power technologies, the leakage current is small compared to the leakage caused by a short between two nets with opposing logic values, or opens that lead to a floating intermediate value on a gate input. The basic idea behind I_{DDQ} testing is to measure the quiescent current and reject those chips whose I_{DDQ} current is above a specified threshold, which is typically far below the maximum leakage current specification.

I_{DDQ} tests are typically performed by selecting a certain number of the Boolean test patterns, pausing after the pattern is applied to let the chip stabilize, and measuring the leakage current.

2.3 I_{DDQ} Test Advantages

I_{DDQ} testing has many advantages. First, I_{DDQ} tests achieve high defect coverage with a small number of tests, due to the complete visibility of the circuit via the power grid.

This also makes I_{DDQ} test very useful in diagnosing defect behavior or locations, since the defective behavior is immediately propagated via the power grid. Second, I_{DDQ} tests readily detect defects such as shorts and opens that are difficult to detect with Boolean tests, due to the difficult test requirements, or the small delay introduced by the defect [2]. Finally, I_{DDQ} tests can detect defects that are too subtle to cause functional failure, but that can cause a failure during customer operation. I_{DDQ} tests can thus avoid the need for expensive burn-in testing, or improve product quality [3].

2.4 I_{DDQ} Test Challenges

The main challenge to I_{DDQ} test is technology scaling. Deep submicron technologies have higher background leakage levels and higher leakage variation than older technologies. In older technologies, a single threshold could be used to reliably separate defective and defect-free chip populations, as shown in Fig. 2. In newer semiconductor technologies, there is no clear separation between defective and defect-free chips, as shown in Fig. 3.

The resolution of I_{DDQ} testing can be increased by estimating the defect-free I_{DDQ} value of a chip, in order to dynamically set a pass-fail limit. These techniques are known as I_{DDX} techniques [4]. A simple example is to use the wafer-level median I_{DDQ} as the estimate of defect-free I_{DDQ}. A widely used technique is to use the differences between I_{DDQ} tests, known as delta-I_{DDQ}. More advanced techniques use neighboring chips on the wafer to develop an estimate.

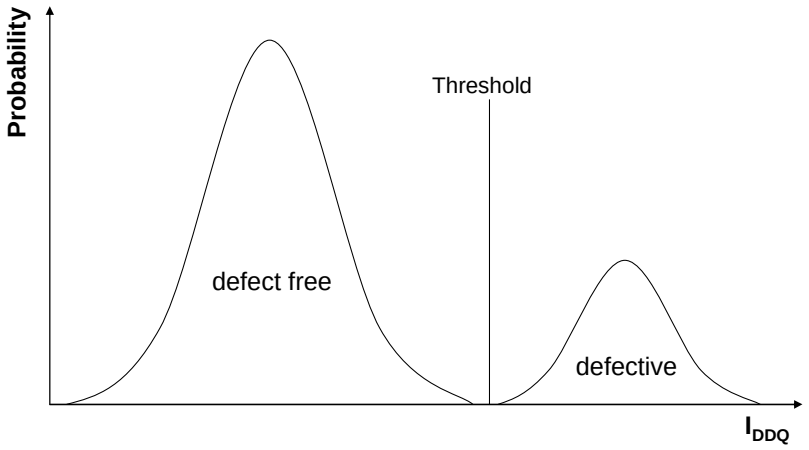

Fig. 2. Distribution of I_{DDQ} in Defective and Defect-Free Chips.

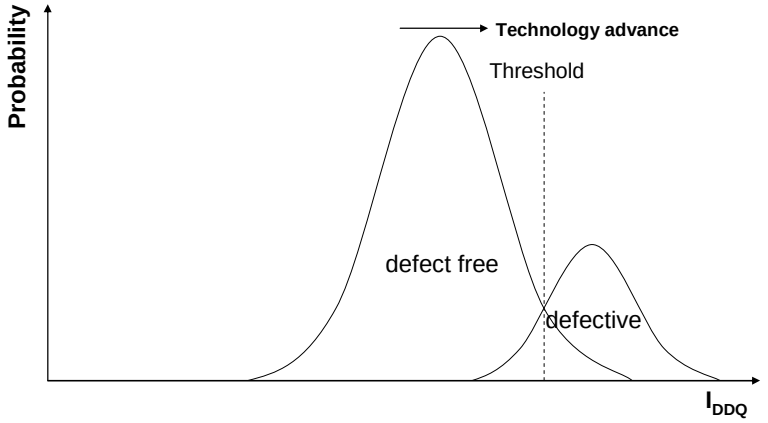

Fig. 3. Distribution of I_{DDQ} in Defective and Defect-Free Chips in Deep Submicron.

3. REVIEW OF BUILT-IN CURRENT SENSORS

3.1 Introduction

I_{DDQ} test can be performed either externally or internally. External testing is done by measuring the current flowing through the power pins on the CUT. This test can be done using the tester precision measurement unit (PMU) or a dedicated current sensor on the tester load board. PMU test can be performed with no additional hardware, but it is slow, due to the need to switch the PMU in and out of the supply, and allow the supplies to settle. Load board sensors are much faster, since there is no need to switch them in and out of the supply, but they require the load board to be designed with I_{DDQ} test in mind.

The problem with external testing is the decreasing test resolution, as discussed above, and the high transient currents that require large decoupling capacitors, that reduce I_{DDQ} test speed. Internal testing is done by using Built-in Current Sensors (BICSs) in series with the power grid. The main advantage of BICSs is the ability to use multiple sensors in the CUT, to virtually partition the power grid. This virtual partitioning reduces the background leakage current seen by each sensor, increasing the I_{DDQ} test resolution. BICSs have the potential for higher speed, due to the lower on-chip power grid capacitance.

3.2 BICS Challenges

Many BICS designs have been proposed, but the challenges BICSs face have prevented their widespread use in production. Some of these challenges are:

- *CUT Performance Degradation*: due to the voltage drop when sampling the quiescent current directly. Many BICS designs have used a series resistor, diode or BJT that causes a 10 to 30% degradation.

- *Pass/Fail and I_{DDQ} Level*: many BICS designs have produced a pass/fail signal. Even with BICSs, the leakage current has become high enough in high-performance circuits that I_{DDX} techniques must be used to determine pass/fail. This means that the BICS must provide the current level as an output. It is also useful to have current direction, since due to variations in metal resistance gradients, the current flow in a branch of the power grid can be in either direction.

- *Fabrication Process Compatibility*: some BICS designs use analog components that make their fabrication challenging in a standard digital process. For incorporation of BICSs into digital designs, it should use only digital technology.

- *External Reference*: an external current reference for the BICS will increase the hardware needed by the tester, and restricts placement of the BICS on the chip.

- *Adaptability*: most BICS designs cannot be modified for different current resolutions after being implemented on the chip.

- *Area Overhead*: most BICS designs have an area that precludes large numbers of them from being fabricated on chip.

3.3 BICS Requirements

In order for I_{DDQ} test to be feasible in modern technology, certain requirements must be met by any I_{DDQ} test method [5][6]. These requirements are:

- Good fault coverage: with the increase in circuit performance, most defects detected by BICS will only cause delay or reliability faults. This means that BICS designs must have sufficient resolution to apply I_{DDX} techniques.

- Circuit performance loss <1% and the BICS should not introduce additional power supply noise.

- No special semiconductor processing steps in a digital technology. Any additional steps will increase the cost of I_{DDQ} test.

- Minimize test speed compared to load board I_{DDQ} test methods. It is desirable for the test time to be less than 1ms/vector.

- Chip area overhead <1% for all the sensors needed to achieve the necessary resolution.

- Ability to measure current level and direction. Current level can be used in I_{DDX} algorithms and current direction can enhance the diagnosis abilities of the BICS.

- Ability to provide a digital output. The BICS must convert from the analog I_{DDQ} level to a digital value, so that it can be fed out via a scan chain. This permits integrating many sensors together and communication with the tester via standard digital tester interfaces.

4. BUILT-IN CURRENT SENSOR DESIGN

4.1 Introduction

The built-in current sensor considered in this thesis sensing the I_{DDQ} current indirectly by measuring the voltage drop across a segment of the power supply line. By using the parasitic resistance of the supply line, the BICS does not introduce any delay penalty. Van Lammeran [7] of Philips Semiconductors was the first to use this approach in production. He achieved good results, but used analog techniques that limited the scalability of his approach. The magnetic field generated by the quiescent current can be sensed without any delay penalty [8][9], but the BICS designs using this technique suffered from high noise levels and calibration drift [6][10]. Due to these disadvantages, a new digital BICS design that senses the voltage drop across the supply line was developed [1][11][12]. A series of sensors was fabricated in 1-μm, 350-nm and 180-nm technologies. In this research, we will only consider the 180-nm sensor design and measurement results. The 180-nm BICS design showed exciting characteristics in terms of robustness, area overhead, speed, and power consumption. However, the sensor did not live up to its expectations in terms of resolution. One of the primary purposes of this research is to understand the behavior of the sensor, so that a new improved sensor can be designed.

The following sections provide a detailed presentation of the sensor as well as a detailed explanation of the function of each component. Simulation results for each component can be found in [1].

4.2 Overview of the BICS

Fig. 4 shows the block diagram of the BICS.

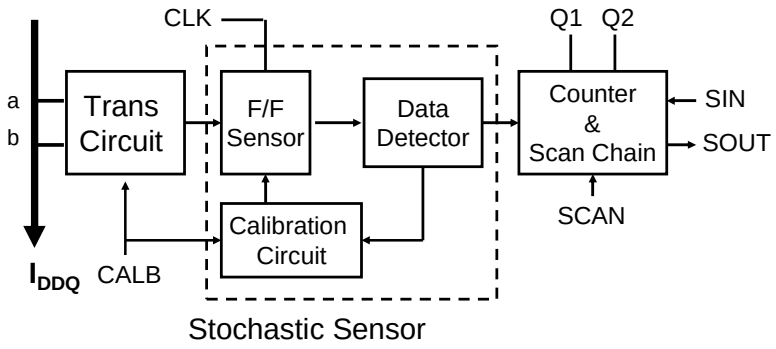

Fig. 4. Built-in Current Sensor (BICS) Block Diagram.

The sensor consists of a transmission circuit, a stochastic sensor that operates as an analog to digital converter, whose results are accumulated in a counter that also operates as a scan chain. The stochastic sensor consists of a flip-flop sensor, data detector and calibration circuit.

The operation of the BICS is as follows. The voltage drop across the supply line is fed to the flip-flop stochastic sensor by the means of the transmission circuit. The stochastic sensor amplifies the signal and compares it to the background noise to resolve either to a ‘0’ or ‘1’ every clock cycle. The probability of going either way depends on the signal to noise ratio (SNR) of the stochastic sensor and the input voltage. Depending on the mode of operation, measurement mode or calibration mode, the data detector output is fed either to the counter/scan-chain or to the calibration circuit. The data detector converts the flip-flop flip into clock pulses for the counter and calibration circuit. During measurement mode, the clock pulses from the data detector are collected in the counter, so the counter value will represent the digital value of the input voltage. The

behavior of the stochastic sensor and the counter can be modeled as an analog-to-digital converter with an output variance based on the sample size (number of clock cycles). During calibration mode, the calibration circuit eliminates any low frequency noise as well as any offsets due to mismatches in the flip-flop or calibration circuit itself.

The BICS is operated by alternating periods of calibration and measurement, in an auto-zeroing fashion. The advantages of a stochastic sensor are that it requires only a small area to implement an ADC, it can measure signals much smaller than the noise, and it uses primarily digital components.

The transmission circuit measures the voltage drop across the parasitic resistance of a section of the power supply line. The transmission circuit also filters high-frequency noise, and shorts its outputs to V_{DD} during calibration.

The sensor in this research is designed to measure the V_{DD} line. However, it can also be modified to sense the ground line. Because the sensor only measures the voltage drop on the supply parasitic resistance, it does not degrade the performance of the CUT. Additionally, due to the digital nature of the sensor, its power consumption is low when operating and it only consumes leakage power when it is off.

4.3 Transmission Circuit

The transmission circuit design is shown in Fig. 5. The input voltage is measured between *ina* and *inb* in the circuit, then transistors P0 and P1 pass these values to *outa* and *outb* which in turn are connected to the flip-flop stochastic sensor inputs. The transmission circuit operation depends on the calibration control signal (*calb*). When *calb*=0, the circuit operates in measurement mode and the input voltage is low-pass

filtered through transistors P0/N0 and P1/N1 and then fed to the flip-flop. The corner frequency of these low filters is about 1 GHz and the transistor dimensions are determined to minimize area and avoid limiting test speed. When *calb*=1, the circuit operates in calibration mode. In this case, P0 and P1 are turned off and the transmission circuit outputs are held at V_{DD} through P3, P4, and P5. This will allow the flip-flop to be calibrated before sensing, which in turn will reduce the drift requirements of the calibration circuit. In order to minimize the mismatches and noise, the transistor dimensions are larger than the minimum required by the used technology. Simulation results on the operation of the transmission circuit can be found in [1].

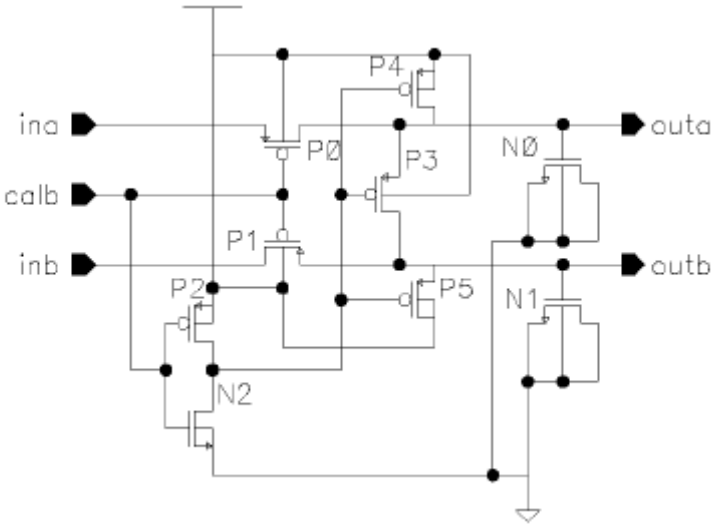

Fig. 5. BICS Transmission Circuit.

4.4 Flip-flop Stochastic Sensor

To measure small input voltage values, the flip-flop operates in the metastable region. By operating the flip-flop in the metastable region, the circuit achieves high gain and converts the analog input signal into a digital one. During measurement mode, the input signal is compared to the background noise in the flip-flop and a decision to flip to a ‘0’ or a ‘1’ is made. The output of the stochastic sensor is then collected in the counter. Due to the flip-flop being operated in metastable region, any random behavior or circuit mismatches will cause the flip-flop decision to settle into one of the stable states. Because of this sensitivity and the low amplitude of the input signal, frequent calibration of the flip-flop is required to maintain proper function of the sensor.

4.4.1 Flip-flop Stochastic Sensor Design

The flip-flop circuit is shown in Fig. 6. The outputs from the transmission circuit are fed to the differential pair inputs *inn/inp* in the flip-flop. The differential pair amplifies the input difference and feeds it into the flip-flop, which compares the input with the background noise to reach to a decision state of either a ‘0’ or a ‘1’. The transistors are sized so that the flip-flop will operate reliably at not much faster than 40 MHz, the same as the clock frequency, in order to minimize the noise. The flip-flop is calibrated using transistors N8 and N9. The main advantage of this design is that the output nodes *out_p/out_n* are charged to V_{DD}-|Vtp|-Vtn. This allows the internal nodes to be charged faster as well as the flip decision to be made faster. The purpose of transistor *P14* is to precharge and equalize the output nodes. This one transistor replaces two transistors in

the sense amplifier in [13], which allows for a reduced precharge voltage, which in turn lowers the power consumption and enhances the decision speed.

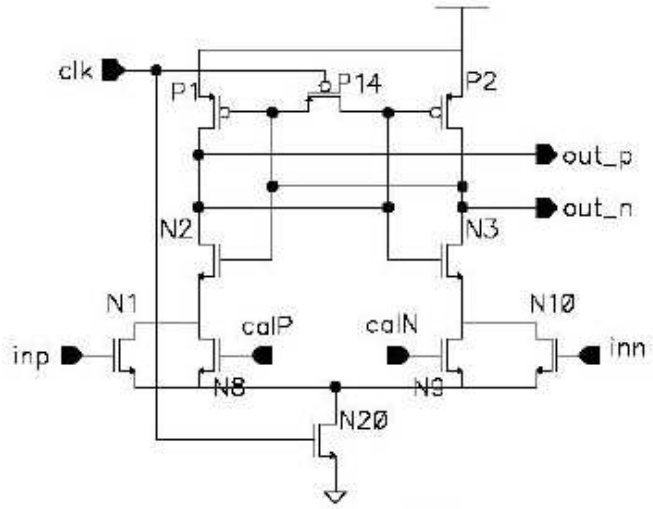

Fig. 6. BICS Flip-flop Stochastic Sensor.

4.4.2 Flip-flop Stochastic Sensor Behavior

When the stochastic sensor is operating in the metastable state, its response follows a Gaussian cumulative density function (CDF) [14][15], as shown in Fig. 7. When the input signal is much lower than the noise (near the center of the x-axis), the CDF can be approximated as a linear function. The magnitude of the input voltage is represented by the ‘0’ or ‘1’ decision probability, and the direction of the current is represented by the sign related to a probability of 0.5. The slope of the CDF is inversely proportional to the noise, which means that more clock cycles are required to reach the desired resolution as the noise increases. The noise does not introduce an offset because it has zero mean. Any offset introduced in the stochastic sensor is minimized with calibration. The outputs of the sensor are fed to the counter, which holds the digital representation of the flip-flop

probability, and so the input voltage magnitude. Thus, this sensor has the ability to measure the current level and this value can be used in I_{DDX} algorithms.

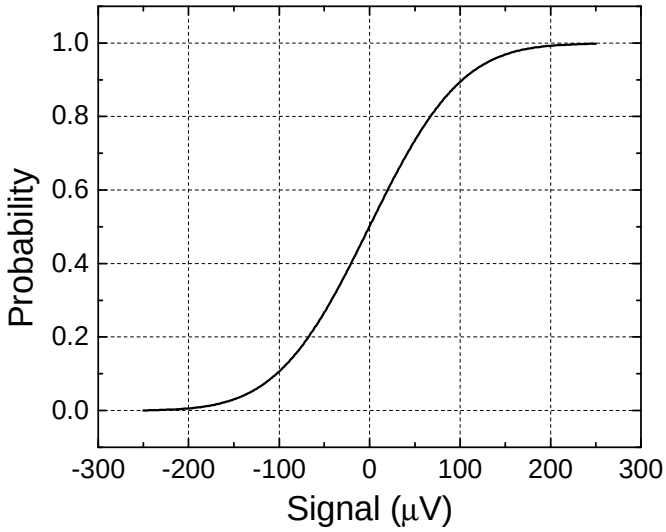

Fig. 7. Stochastic Sensor Cumulative Density Function.

The sampling variance for the stochastic sensor is given by [16]:

$$\frac{pq}{N} \sim \frac{0.25}{N} \tag{4.1}$$

and the standard deviation by:

$$\sigma = [\,pq / N\,]^{\frac{1}{2}} \sim \frac{0.5}{\sqrt{N}} \tag{4.2}$$

where N is the number of measurement cycles, and p and q are the probabilities to get a '1' from either side of the flip-flop which are almost equal to 0.5. In other words, quadrupling the number of clock cycles doubles the sensor resolution.

The probability of getting a ‘1’ is given by:

$$p \sim 0.5 \pm \frac{1}{\sqrt{2\pi}} \int_0^S \exp^{-1/2u^2}\, du \tag{4.3}$$

where *s* is the signal to noise ratio. When the signal is much lower than the noise, this probability can be approximated as [16]:

$$p \sim 0.5 \pm \frac{s}{\sqrt{2\pi}} \tag{4.4}$$

and the counter value after *N* measurements is given by:

$$N \cdot p \sim N \cdot 0.5 \pm \frac{N \cdot s}{\sqrt{2\pi}} \tag{4.5}$$

It is obvious that the flip-flop gain is inversely proportional to the noise. In order to achieve a certain measurement resolution, the minimum number of measurement cycles N has to be evaluated. It has been shown that the minimum *N* is given by [6]:

$$N \geq \frac{Z_\alpha^2}{s^2} \tag{4.6}$$

Z_α is found from a t-distribution table depending on the required confidence level.

4.4.3 Noise Analysis of the Flip-flop Stochastic Sensor

As mentioned above, the flip-flop compares the input signal with the background noise. This noise comes from different sources. The most important sources are external noise and the thermal noise of the transistors. Other noises, such as flicker noise and power supply line noise, have low frequency components and should be eliminated by auto-zeroing of the sensor with the calibration circuit.

The thermal and flicker noises of the transistors are given by:

$$S_{IW} = \begin{cases} \dfrac{4kT}{R_{FET}} & \textit{ohmic region} \\ \dfrac{8kTg_m}{3} & \textit{saturation} \end{cases} \tag{4.7}$$

$$S_{If} = \frac{2K_f K' I_{DQ}}{C_{OX} L^2 f} \tag{4.8}$$

where S_{IW} and S_{If} are the thermal noise and the flicker noise, respectively. T is the temperature in Kelvin, k is Boltzmann's constant, R_{FET} is the equivalent resistance of the transistor in the ohmic region, and g_m is the transconductance of the transistor. The flip-flop is clocked at 40 MHz, so the bandwidth of interest is from 40 MHz to the cutoff frequency, around 1 GHz. In this band, the flicker noise is highly dominated by the thermal noise and is not considered in simulations. In addition, auto-zeroing at about 100 kHz minimizes flicker noise.

4.5 Data Detector

The data detector circuit is shown in Fig. 8. During measurement mode, the data detector does not operate and the flip-flop outputs are passed through to the counter. During calibration mode, if the input *in* rises to '1', the data detector generates two charge pump clock pulses. One of those pulses is used to increase the calibration voltage on the flip-flop side that generates the '1' and the other pulse is used to pump down the other side, allowing for an unbiased decision for the next measurements. In order to preserve the correctness of the calibration; the two generated pulses need to be non-overlapping.

Another important feature of the sensor is the ability to preserve the counter value during calibration by holding the counter clocks stable during calibration. This allows for auto-zeroing operation, where calibration and measurement periods alternate, allowing the removal of low frequency noise and drift.

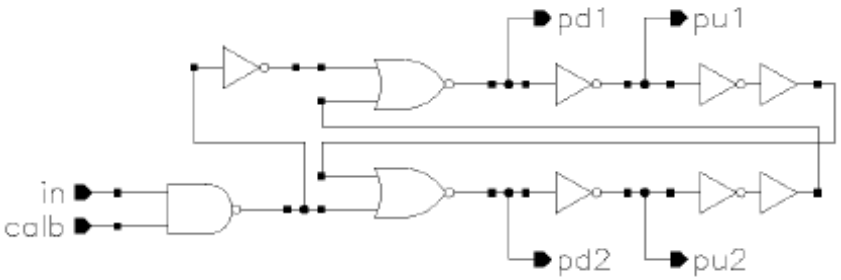

Fig. 8. BICS Data Detector Circuit.

4.6 Calibration Circuit

Calibration of the flip-flop stochastic sensor is a necessity because of unavoidable circuit mismatches, as well as the need to auto-zero to remove low-frequency noise and drift. Although the flip-flop circuit is symmetric, and theoretically should eliminate any common mode signal (i.e. infinite common mode rejection ratio – CMRR and power supply rejection ratio – PSRR), there will be some mismatches in the transistors. To reduce the effect of mismatches on the decision of the flip-flop, two of the calibration circuits shown in Fig. 9 are used. The calibration circuit introduces a small imbalance in the gate voltage of the calibration transistors *N8/N9* to counteract the mismatch effect. Depending on the flip-flop decision, the data detector generates pulses for the calibration circuits, which in turn control the gate voltage of the calibration transistors.

In the calibration circuit, transistors *P6/N6* behave as reservoir capacitors. These transistors are sized to balance their gate leakage. The capacitors are charged through charge pump transistors *P1/P7* and *N1/N2*, which provide symmetrical *pump-up/pump-down* paths. The charge pump transistors are controlled by nonoverlapping pulses *pu1/pu2* and *pd1/pd2* generated by the data detector.

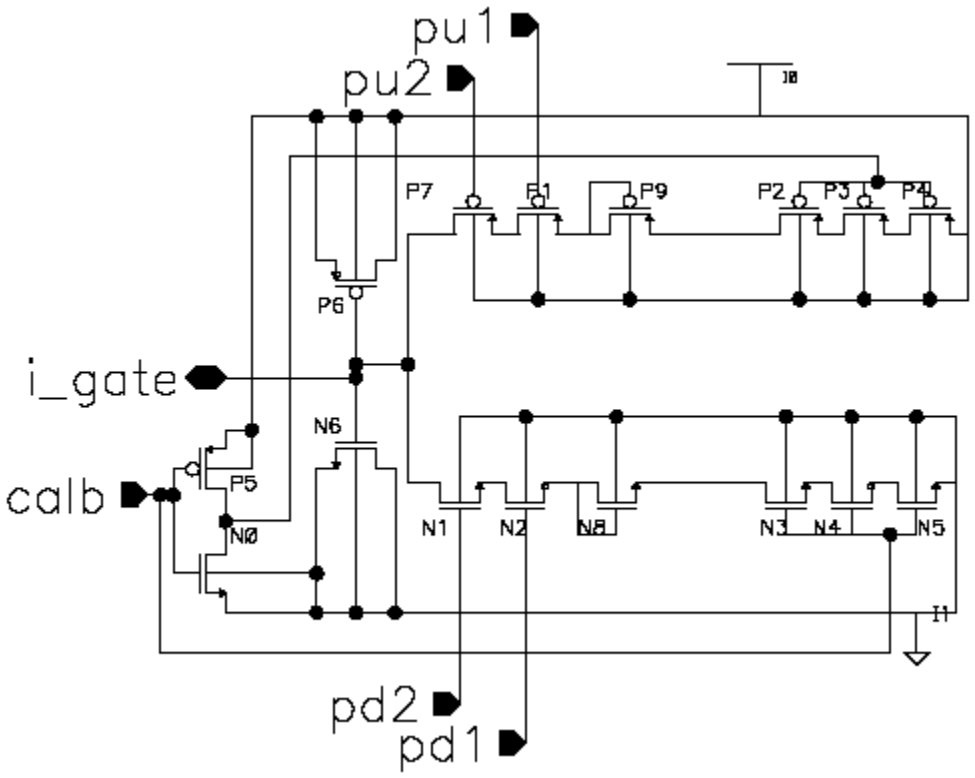

Fig. 9. BICS Calibration Circuit.

For the charging process, the parasitic capacitance between *P1/P7* is charged first by clocking *P1*, and then the charge is transferred to the reservoir capacitors when *P7* is clocked. Since the clocks do not overlap, the parasitic capacitance is either charging or discharging. Discharging of the reservoir capacitors is done similarly through *N1/N2*. When the calibration is done, stack transistors *P2/P3/P4* and *N3/N4/N5* are turned off.

This feature decreases the leakage, reducing the drift in calibration voltage until the next calibration period [17].

To increase the calibration resolution, the calibration voltage step size must also be minimized. This is achieved by placing diode-connected transistors *P9* and *N8* between the pump transistors and the stack transistors, to reduce the voltage seen on the pump transistors. This reduces the calibration voltage range while reducing pump step size.

Calibration circuit design is faced by two challenges. The first is high resolution, which can be achieved with a high capacitance ratio for the charge pump. This will reduce the voltage step size, but will increase the time required to cancel any offset. The primary offset is that due to process variation, so a smaller step size will require a longer initial calibration period to move the flip-flop into the metastable region. This longer initial calibration time is insignificant in the total sensor measurement time. Once in the metastable region, the time to achieve periodic recalibration is not very sensitive to the pump step size. The second challenge in calibration is limiting the drift while in measurement mode. This can be done by using high V_{TH} stack transistors and using a shorter measurement mode period.

Normal sensor operation alternates measurement and calibration periods after an initial calibration period, operating in auto-zeroing fashion. The frequency of recalibration is set in order to minimize offsets due to drift and improve resolution by zeroing out low-frequency noise. For example, if the sensor operates at 40 MHz, with 200 calibration cycles followed by 200 measurement cycles, then it is auto-zeroing at a 100 kHz rate. This essentially eliminates transistor flicker noise, low-frequency supply

and input noise, and temperature drift. The calibration capacitors need to maintain their voltage for 5 μs, so have very relaxed drift requirements.

4.7 Counter and Scan Chain

The counter and scan chain circuit is shown in Fig. 10. The circuit represents one cell and is able to store one bit. This circuit has two modes of operation. While in counter mode, the circuit acts as a toggle flip-flop, connected in series to form a toggle counter. This circuit has the advantage of low power, since the entire counter uses the same dynamic power as two bits toggling at full speed. Another property of the circuit is that it is designed so that all switching occurs after the flip-flop makes its decision, before the next clock cycle. This avoids any counter noise from being injected into the flip-flop.

While in scan mode, the stored value is scanned out, converted to an I_{DDQ} level and used in I_{DDX} algorithms. Zeros are scanned in at the same time. The signal to noise ratio of the flip-flop and the desired resolution specify the number of required counter/scan chain cells. The design considered here has a 24-bit up counter. A down counter is not needed, since its value is just $N - up\_count$. In theory, the flip-flop could remain in its metastable state at the end of the clock cycle, so that no count occurred, but this never occurred in previous experiments.

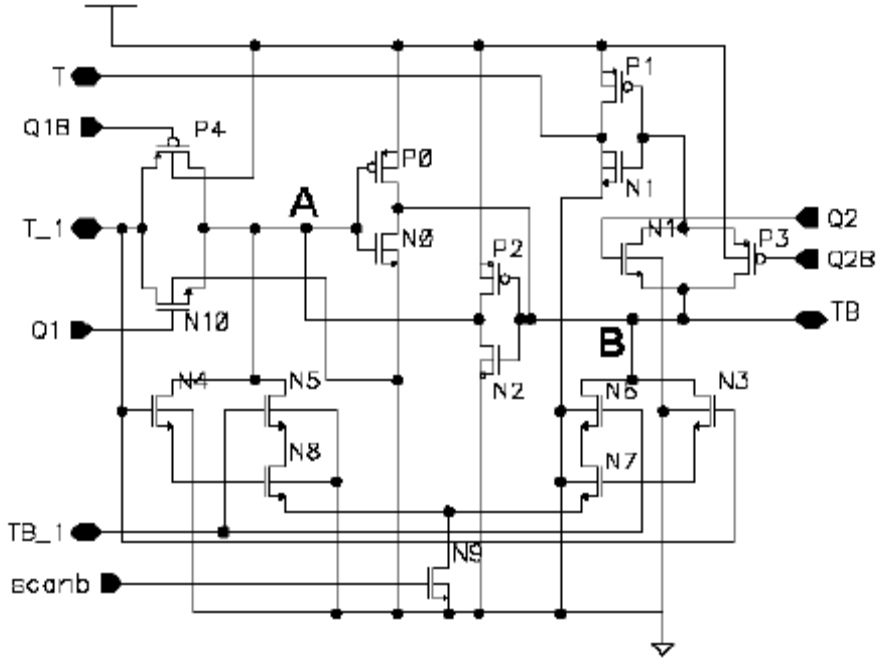

Fig. 10. BICS Counter/Scan Chain Cell.

5. BEHAVIORAL MODELING

5.1 Introduction

With the rapid advance of CMOS technology, more and more transistors are implemented on a single chip. This causes a proportional rise in circuit complexity. Verification of design, simulations, testing, and finding error locations becomes harder and takes a lot of time. This is where behavioral modeling can help. Behavioral modeling is used to manage circuit complexity by modeling the chip behavior at the system level. This is achieved by using simple blocks with enough accuracy to replace circuit components.

Behavioral modeling helps with the proper selection of system architecture and tradeoff analysis in top-down design, and in bottom-up design it saves tremendous time and memory compared to transistor level simulations [18]. The main challenge in behavioral modeling is to account for the important non-idealities in the circuit, such as noise, mismatches, and nonlinear effects. Finding accurate models for these non-idealities is the hardest part of the job of developing and verifying a behavioral model.

Several methods for behavioral modeling have been proposed, depending on the type of circuit. For complicated linear dynamic circuits, model order reduction techniques are used for interconnect analysis. For non-linear circuits, the developed models are only accurate depending on the accuracy of modeling the nonlinear effects. However, some practical behavioral modeling methods can be used. These methods can be divided into three groups [18]:

- *Regression method*: used to map the design space parameters into performance space parameters.

- *Hammerstein method*: used for non-linear continuous circuits to model the input-output behavior.

- *Sampled data models*: used for sampled data circuits such as sigma-delta modulators to replace the sampled data operation by delay units and static nonlinear functions.

Since the sensor can be viewed as a sampled data system, we follow the sampled data models in this research.

6. BICS BEHAVIORAL MODEL

6.1 Introduction

As mentioned in the previous section, the purpose of behavioral modeling is to simplify and speed up simulations that could become difficult at the transistor level. In the following sections, the behavioral model of each component of the BICS is discussed. While in measurement mode, the BICS behaves as an analog to digital converter (ADC), so any ADC model with the proper noise model should be sufficient. We then need to set the proper noise models and account for any mismatches to make the simulation as realistic as possible. All the models are then put together and the circuit is simulated. All the models are implemented and simulated using *Simulink*. A comparison between the behavioral model and the real circuit simulation results is conducted. Finally, we end with conclusions.

6.2 Transmission Circuit Model

The transmission circuit model is shown in Fig. 11. During the calibration phase, the inputs of the BICS are shorted. This is modeled by feeding zeros to the outputs during calibration. Zeros are used in order to simplify the following flip-flop model, which can then use adders on its inputs. During the measurement phase, the input signal is passed through and fed to the flip-flop stochastic sensor. The reset signal is required for the proper operation of the switch, since the switch model moves the switch after the specified number of clock cycles, but does not move it back until reset. Two switches are used for each side, one for alternating calibration and measurement every 200 cycles, and

the other for the initial 1000 calibration cycles. Since the initial calibration is performed only once, this switch does not need to be reset.

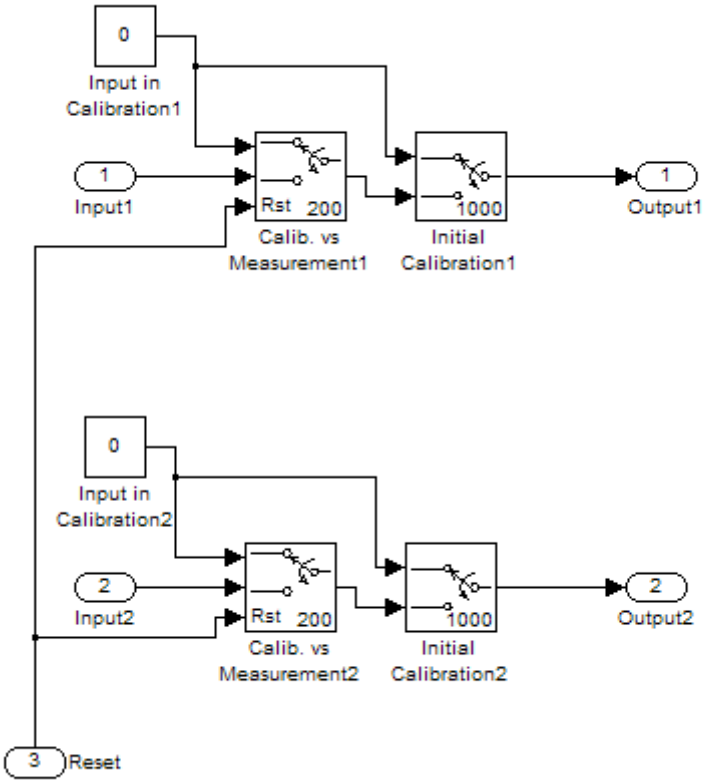

Fig. 11. Transmission Circuit Model.

6.3 Flip-flop Stochastic Sensor Model

The purpose of the flip-flop is to compare the input signal to the background noise while in measurement mode. During calibration mode, the flip-flop will compare the background noise with the calibration voltage from the charge pump circuit. A good model for the flip-flop is a simple comparator. This comparator has a switch on point and a switch off point. If the input is greater than the switch on point, the output of the comparator is ‘1’. If the input is less than the switch off point, the output is ‘0’. In this

model, the switch on and switch off points are equal. In order to make this model more accurate, we need to take into account the effects of the flip-flop noise and mismatches. Mismatches effectively introduce an offset. This offset can be modeled by a change in the switch on and switch off point or it can be modeled as an input to the comparator added to the original input signal. For simplicity, we decided to use the second option. The offset of 37 mV shown in the model is from measured data. The noise and calibration voltages are added to the input before comparison. A discussion about the noise model will be presented later. The complete flip-flop stochastic sensor is shown in Fig. 12.

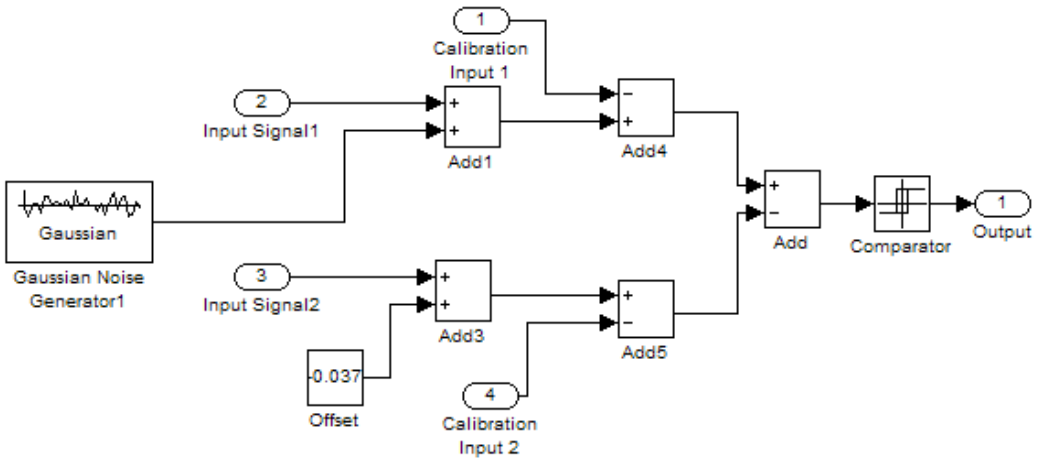

Fig. 12. Flip-flop Stochastic Sensor Model.

6.4 Data Detector

The purpose of the data detector is to convert the flip-flop decision into a counter pulse clock during measurement and into a calibration pulse clock during calibration. The data detector model is shown in Fig. 13. Since the first phase is a calibration phase, the data detector feeds the flip-flop directly to the calibration circuit. Meanwhile, the counter value is fixed by feeding it with zeros. In this model, a 1000 cycles of calibration is done

initially, then 200 cycles of measurements is done followed by 200 cycles of calibration. The number of cycles for each phase is controlled by the switch. The reset signal is required for the proper operation of the switch, as explained above.

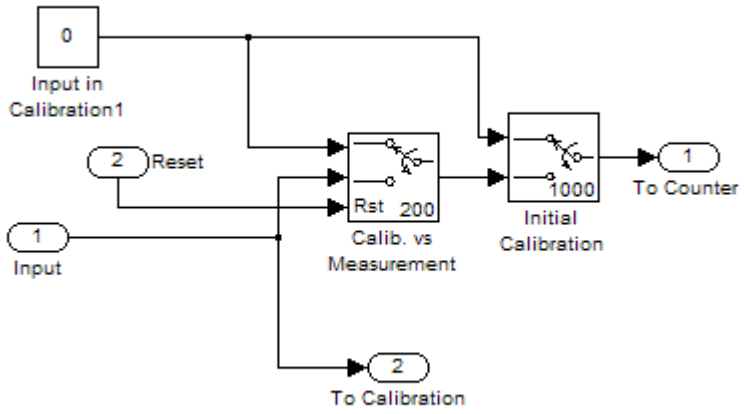

Fig. 13. Data Detector Model.

6.5 Calibration Circuit Model

As mentioned in the operation of the calibration circuit, the parasitic capacitors are being charged and discharged according to the applied clock signal. This can be modeled by series capacitors with switches to control the charging and discharging processes. The charge pump step size is determined by the capacitors ratio and clock frequency. A close model of the calibration circuit is shown in Fig. 14.

The purpose of the additional switches and memory is to hold the calibration voltage around a constant value during measurement phase.

Based on the flip-flop output, one of the relays in the calibration circuit is on and the other is off. The on value for both relays is ‘1’ and the off value is ‘0’. The value of the

pump-up and pump-down gain *K* are equal to the calibration voltage step size for the pump-up and pump-down, respectively. Because the input for the flip-flop is analog where the output of the calibration circuit is digital, an integrator is used in order to smooth the change in the calibration voltage.

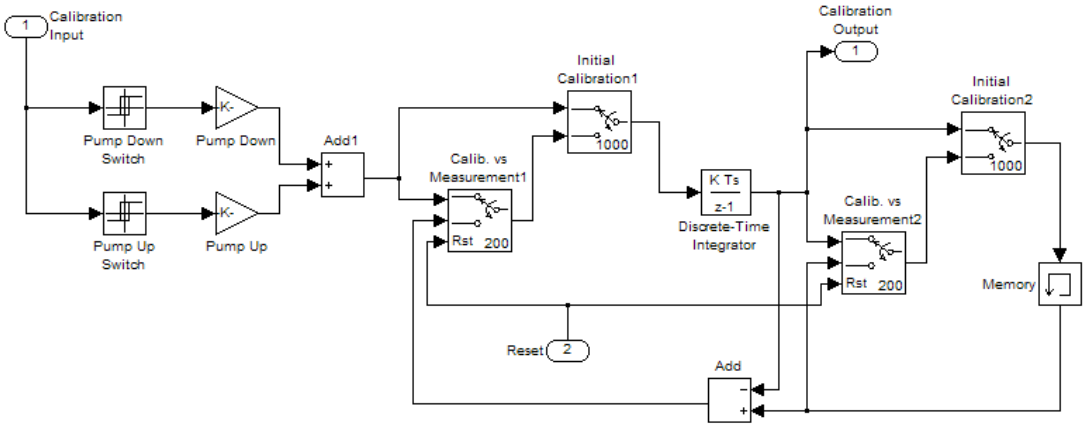

Fig. 14. Calibration Circuit Model.

The effect of calibration voltage drift was not included in the calibration circuit model. Measurements done on the actual 180-nm sensor showed a drift rate of the calibration voltage of 630μV/10ms. This means that in 200 cycles of measurement at 40 MHz, the calibration voltage will drift by at most 300 nV, which is two orders of magnitude smaller than the calibration pump step size. In practice, the drift rate would be even smaller, since the calibration capacitor voltages would be close to $V_{DD}/2$, so the calibration capacitor leakage paths would be nearly balanced.

6.6 Counter Model

The counter in the actual sensor is an up/down counter. This type of counter does not exist directly in *Simulink*. In order to model the counter we changed the flip-flop output

to be either a ‘1’ or a ‘-1’, and then add the outputs as the simulation runs. The counter model is shown in Fig. 15. The memory holds the counter value during calibration.

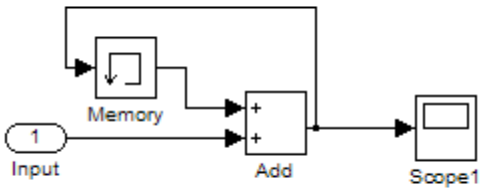

Fig. 15. Up/Down Counter Model.

6.7 Noise Model

There are several sources of noise that can affect the performance of the sensor circuit. The impact of the noise is usually measured by the signal to noise ratio (SNR), given by the following equation:

$$SNR = \frac{AverageSignalPower}{AverageNoisePower} \tag{6.1}$$

The first source of noise in CMOS circuits is thermal noise. This noise is generated due to the random movement of electrons in the circuit as a function of temperature [19]. This noise is also called white noise, because its spectral density is constant. White noise is usually associated with the resistance of an electrical component. The spectral density function of the white noise is given by:

$$S(f)=\begin{cases}\dfrac{4kT}{R_{FET}} & ohmic\ region\\ \dfrac{8kTg_m}{3} & saturation\end{cases} \tag{6.2}$$

where $k = 1.38\times10^{-23}$ J/K is Boltzmann's constant, T is the temperature in Kelvin, g_m is the transistor transconductance, and R_{FET} is the transistor equivalent resistance.

Any model of the white noise takes advantage of its zero mean property. White noise is usually modeled by a Gaussian probability distribution function (pdf) and that is what is used in our research.

The second source of noise is flicker noise. Flicker noise spectral density is inversely proportional to the frequency, and so is referred to as 1/f noise. If we alternate 1000 calibration and 1000 measurement cycles at 40 MHz, then auto zeroing will occur at a rate of 20 kHz. With 200/200 calibration/measurement cycles, the auto zeroing rate is 100 kHz. The auto zeroing process acts like a high pass filter with the corresponding corner frequency. Since the noise gain falls at the same rate that the flicker noise rises below the corner frequency, the net result is constant spectral density. Flicker noise beyond the corner frequency is small compared to the white noise, and so not included in our model.

The third source of noise is the power supply noise. Power supply noise comes from two sources; the first is noise generated by the power supply itself. This noise is usually dominated by low frequency noise (e.g. 60 Hz hum), which will be canceled by the auto zeroing process. The second source is the noise from other circuits coupled through the power supply lines. This noise will come from off-chip. In the case of our test chip measurements, this noise comes from the FPGA board generating the test waveforms. In real applications, this noise will come from the tester or active circuits on chip. They will

not come from the BICS itself, since at the 40 MHz clock rate, all BICS circuit switching starts after the flip-flop decision, and is completed before the next flip-flop decision, and so all self-generated supply noise is out of phase with the flip-flop. Supply noise is injected into the BICS in three places. First, it appears on the transmission circuit inputs via the supply line being sensed. The low pass filters in the transmission circuit will remove only the very high frequency noise. Second, the supply noise appears as common mode noise on the calibration nodes via the calibration capacitors. Third, the supply noise appears as common mode in the flip-flop via the PMOS pullup transistors. Mismatch in the flip-flop means the power supply rejection ratio (PSRR) and common mode rejection ratio (CMRR) are not infinite, so some of this noise will appear in the flip-flop, and must be included in the behavioral model. The input noise could be attenuated by reducing the corner frequency on the input low pass filters, with larger capacitors or longer channel PMOS transistors. Supply noise to the flip-flop and calibration capacitors can be reduced through additional on-chip and off-chip decoupling capacitors, but at the cost of chip area. The on-chip capacitor can be combined with additional supply line resistance to provide additional filtering of the supply noise.

The fourth source of noise in the BICS is clock noise. The clock noise comes from noise on the clock itself and noise due to clock jitter. The clock noise couples to the common node of the differential pair in the flip-flop via the gate-drain capacitor of the clock pulldown transistor. Its impact depends on flip-flop mismatch. Clocks generated by the data detector will have noise coupled from the supply and jitter. The noise will affect transistor drive strength, so cause variation in pump step size. Jitter will also cause variations in pump step size. Since the clock jitter follows a Gaussian distribution

[20][21], so will the variation in the charge pump. The expected variation in the pump step size is small compared to the pump step, which is already large compared to the signal being sensed. The clock noise coupled directly into the flip-flop is the dominant noise, but is smaller than the supply noise. Therefore, neither noise source was included in the noise model.

The last important source of noise is substrate noise. Substrate noise is present in CMOS circuits due to the sharing of the same substrate by all circuit parts. The substrate acts as a channel that transfers noise from different parts of the circuit [22]. As described above, the sensor is designed so that all internal noise is out of phase with the flip-flop switching, but in a higher speed design, this could be an issue, requiring flip-flop isolation from other circuits.

In our behavioral model, we used a Gaussian noise source connected to the flip-flop input with zero mean and a 3 mV standard deviation. The parameters of this source were taken directly from the measurements done on the actual sensor [1], which combines all noise sources on the flip-flop.

In this research, we will try to point out the effects of the different noises in the circuit especially the power supply noise. In order to do that, we will connect different noise sources to the model and vary their parameters to verify the correctness of the model, and then we will vary them again to see the effects of such variation.

7. SIMULATION RESULTS

7.1 Model Verification

After the model components were put together, we simulated the circuit and observed the gain of the circuit, the output offset and the calibration voltage. We started with the basic model in order to verify our model. In the basic model, we have the following parameters:

- Charge Pump Up = 84 μV
- Charge Pump Down = 47 μV
- Flip-flop Offset = 37 mV
- Flip-flop Noise = 500 μV
- 1000 Cycles of Initial Calibrations
- 200 Measurement Cycles followed by 200 Calibration Cycles
- A Total of 1M Cycles for sensor gain measurements
- A total of 2000 Cycles for calibration voltage measurements

The pump, offset and noise were taken from silicon measurements. The results of the basic model are shown in Fig. 16-17. Fig. 16 shows the difference in the number of ‘1’s and ‘0’s versus the difference in the input voltage. The figure shows a gain equal to 1218 counts/μV/ 1M measurement cycles. Fig. 17 shows one period of the calibration voltage of the basic model and shows a standard deviation equals to 1.09E-4. The following sections shows the effects of changing the charge pump ratio, the flip-flop stochastic sensor mismatch, number of measurement cycles versus number of calibration voltage, and noise increment on the system.

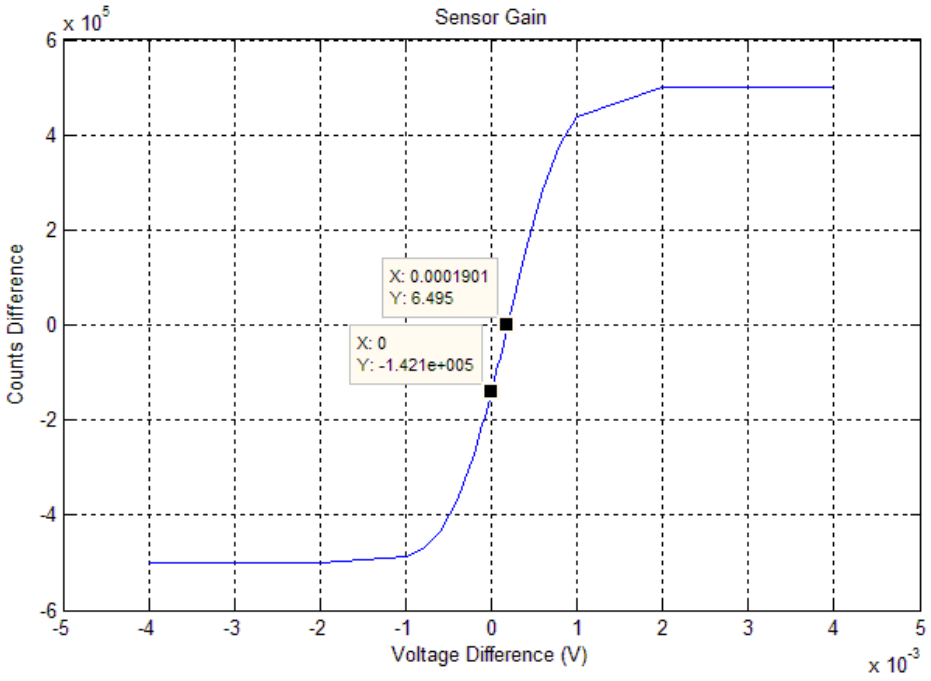

Fig. 16. Basic Model Sensor Gain.

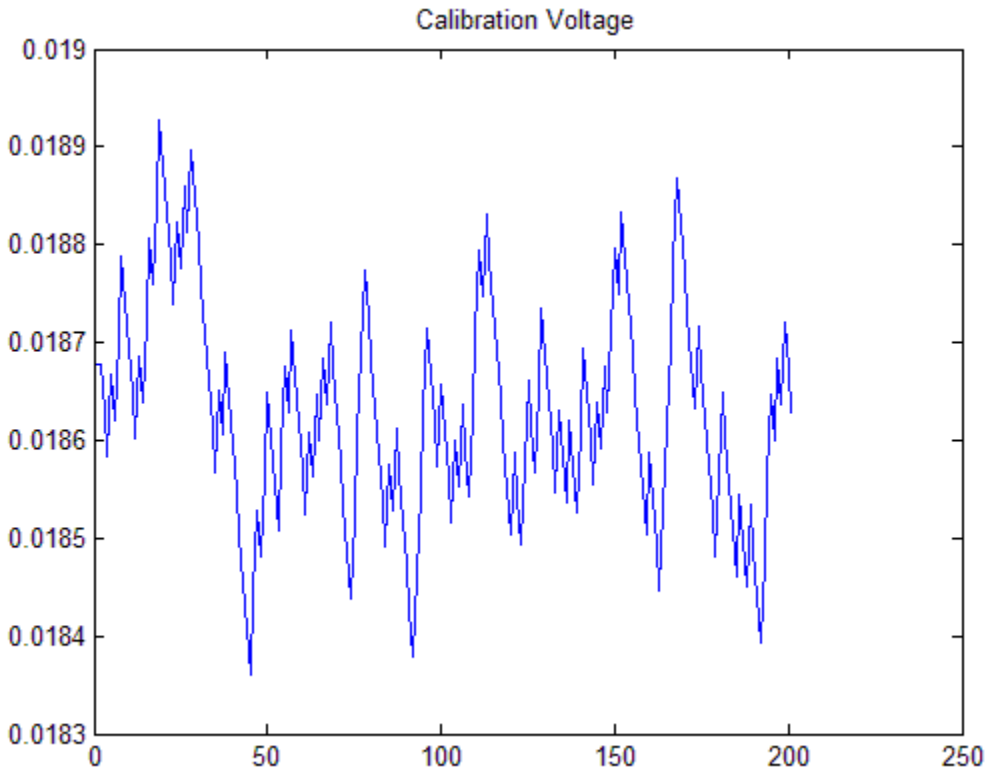

Fig. 17. Basic Model Calibration Voltage (Zoomed).

7.2 Charge Pump Ratio Effect

The value of the charge pump ratio directly affects the resolution of the system. In our simulations we varied the ratio of the charge pump as follows:

- Pump-up = Pump-down = 84μV
- Pump-up = Pump-down = 47μV
- Pump-up = Pump-down = 1μV

The sensor gain versus the charge pump ratio is shown in Fig. 18, while the calibration voltage is shown in the appendix. The first thing to notice is that the gain is slightly higher than the basic model gain. The increment is less than 4%. The second thing to notice is that the standard deviation decreases as the charge pump ratio decreases. The actual values of the gains and the standard deviation are presented in Table I in section 7.7. The last observation is that an equal charge pump up/down step size leads to the minimum output offset.

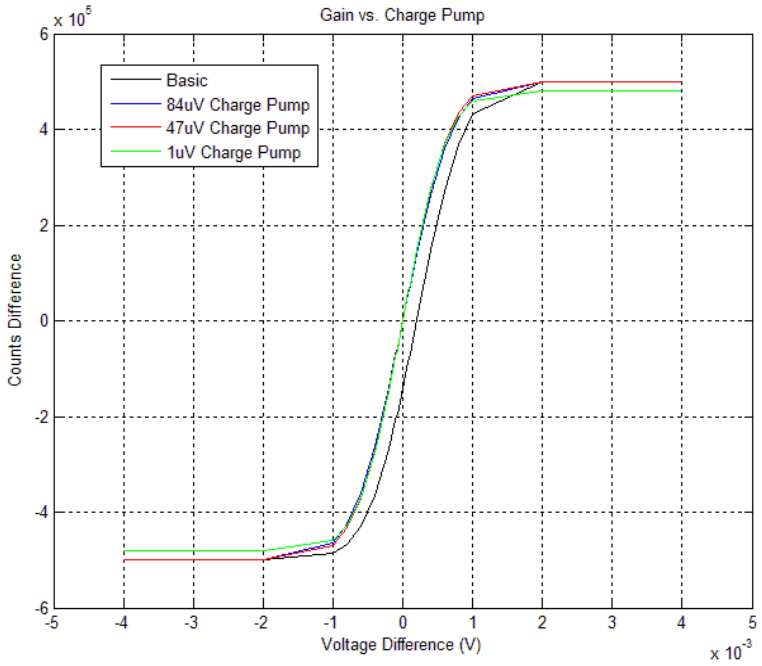

Fig. 18. Sensor Gain vs. Charge Pump Step Size.

7.3 Flip-flop Stochastic Sensor Mismatch Effect

As mentioned before, the flip-flop mismatch was modeled as an offset injected into the flip-flop. In our simulations, we considered offsets of 37 mV, 12 mV and 0 V. The actual sensor suffers from a 37 mV offset, which translates to a 3% mismatch [1]. One of the actual sensor goals was for the mismatch to be less than 1%. That is the reason for simulating the 12 mV offset. We also investigated the effect of an ideal case. Although this case is impossible in reality, it should give us more insight on the effect of reducing the mismatch. The effect on the sensor gain is shown in Fig. 19 while the effects on the calibration voltage are shown in the appendix.

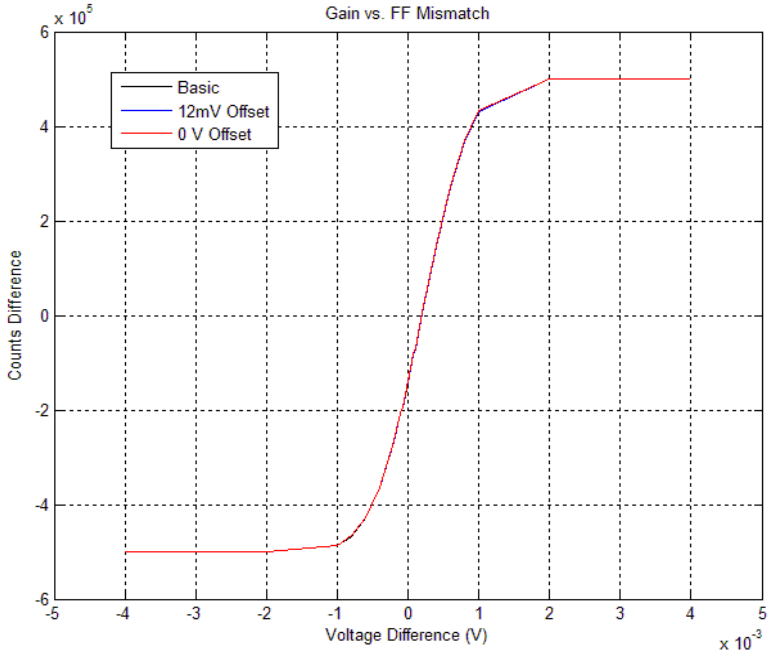

Fig. 19. Sensor Gain vs. Offset.

The first observation is that gain is slightly lower than the basic model by 4% for the 0 V offset case while it is the same for the 12 mV offset case. The lower gain for no offset is likely an artifact of the initial seed of the noise random number generator. The

standard deviation of the calibration voltage is also almost the same. In the case of the 0V offset, the operating range is higher than the basic model and the 12 mV offset case.

7.4 Measurement Cycles vs. Calibration Cycles Effect

After the initial calibration, the basic model performs 200 measurement cycles (MC) followed by 200 calibration cycles (CC). In this section, we investigate the effect of changing the measurement cycles vs. the calibration cycles. In theory, more calibration cycles will increase the immunity of the sensor against noise and mismatches and will reduce drift effects. We simulated the model for the following cases:

- 100MC followed by 100CC
- 500MC followed by 500CC
- 200MC followed by 100CC
- 100MC followed by 200CC

The effect on the sensor gain is shown in Fig. 20 while the effect on the calibration voltage is shown in the appendix.

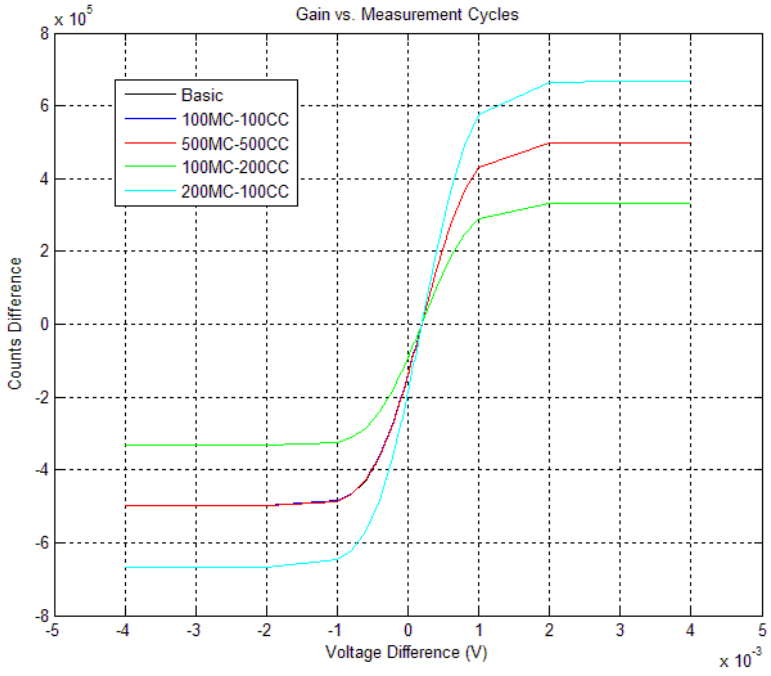

Fig. 20. Sensor Gain vs. Measurement Cycles.

The first observation is that the gain of the sensor increases when the measurement period is longer than the calibration period, but the operating range decreases. The reason for this is that fewer calibration cycles are needed than are actually used, so devoting more cycles to measurement increases the sensor gain, and correspondingly reduces the operating range. Analysis of cycle-by-cycle simulation results shows that only a few cycles are needed for the flip-flop to come back into calibration at the end of each measurement period.

7.5 Noise Change Effect

According to equation 4.4, the probability for the flip-flop to reach a '1' decision depends on the signal to noise ratio. This means that when the noise increases, the number of '1' counts will decrease. Our simulations show this effect. In our simulations,

we changed the noise by introducing a gain to the flip-flop noise generator. We varied this gain between 1.5 and 7. The effect on the sensor gain is shown in Fig. 21.

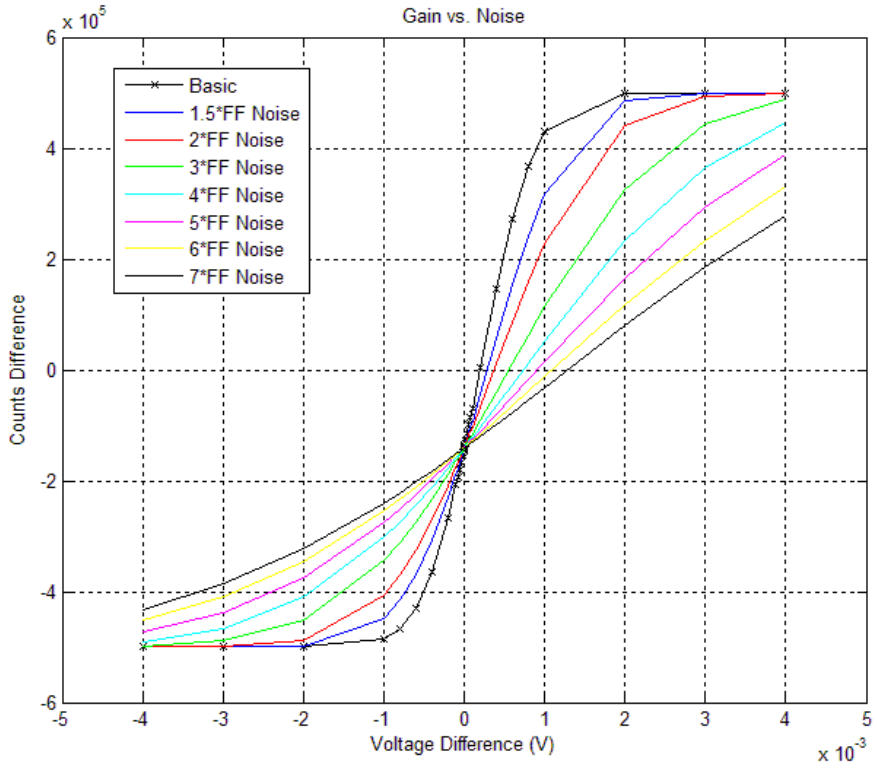

Fig. 21. Sensor Gain vs. Overall Noise.

As seen in the figure, the gain of the sensor decreases and the operating range increases as the noise increases. The effect on the calibration voltage is shown in the appendix.

An observation here is that the standard deviation of the calibration voltage increases with the noise, which is expected since the calibration circuit has to provide more voltage difference to compensate for the extra noise.

7.6 Best Combination?

In this section, we try what we believe is the best combination in terms of the sensor gain and the standard deviation of the calibration voltage. In this simulation, the model parameters are as follows:

- Charge Pump Ratio = 1 μV
- Offset = 12 mV
- 200 measurement cycles followed by 100 calibration cycles
- 15000 initial calibration cycles to allow the model to reach the steady-state
- Overall Noise = FF Noise

The results are shown in Fig. 22-23. Fig. 22 shows the sensor gain. The best combination has a gain of 1537 counts/ μV/1M Cycles. Fig.23 shows the calibration voltage of the best combination. Zooming into one period of calibration, it shows a standard deviation equals to 3.64E-6. Note that we use a non-zero offset in this "best" combination, since as shown earlier, a 0 V offset gave lower gain due to simulation artifacts.

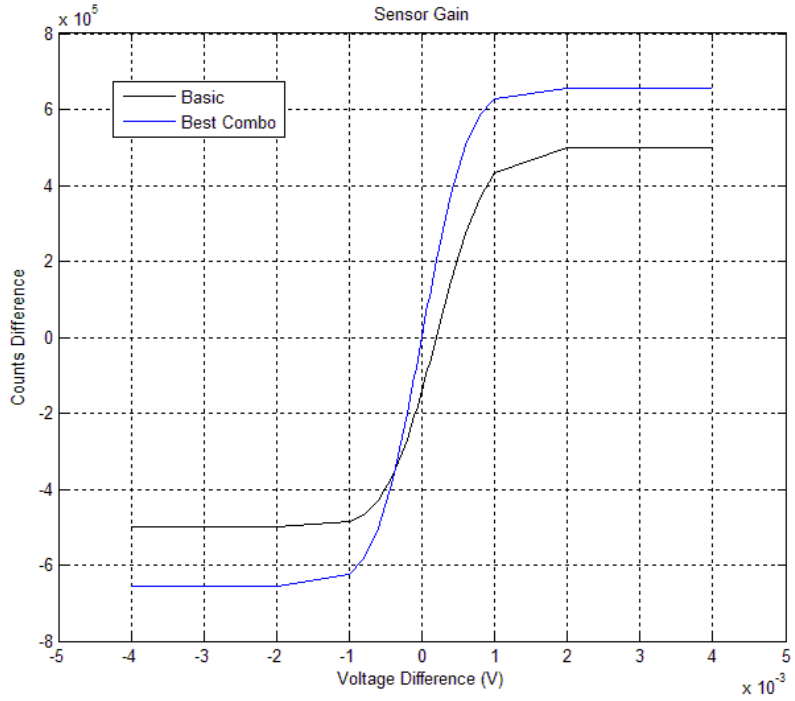

Fig. 22. Sensor Gain, Best Combination.

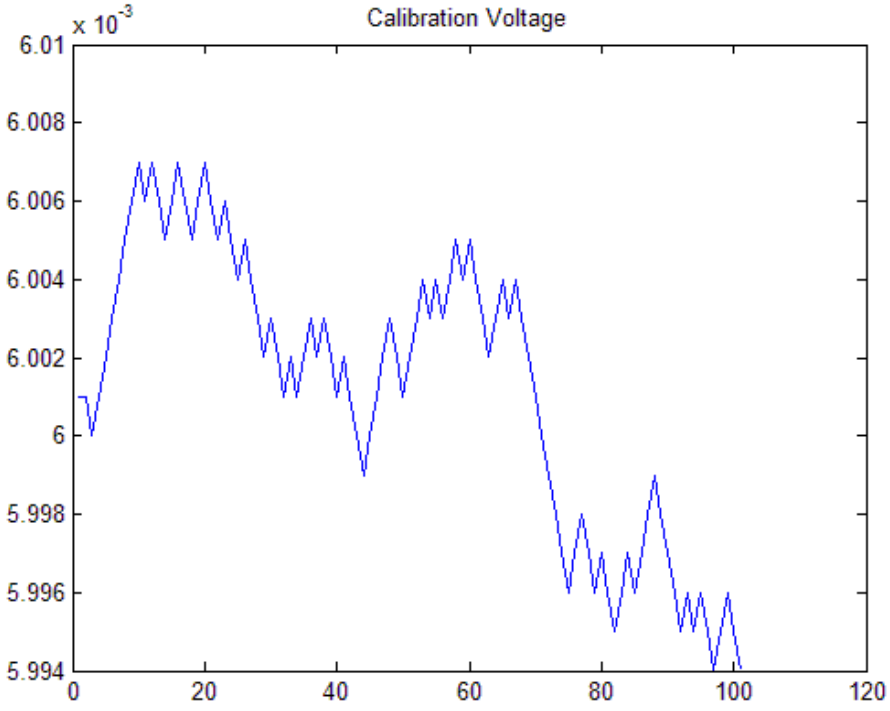

Fig. 23. Calibration Voltage Zoomed, Best Combination.

7.7 Summary

The results are summarized in Table I that shows the sensor gain, the output offset, and the standard deviation of the calibration voltage for each simulation case.

TABLE I. SUMMARY OF SIMULATION RESULTS

Case	Sensor Gain (Counts/μV/1M Cycles)	Output Offset (ΔCounts)	σ of Cal. (μV)
Basic Model	1050	-141094	109
84μV Pump	1076	352	128
47μV Pump	1088	866	80.1
1μV Pump	1060	-92	3.19
Offset = 12mV	1050	-141110	108
Offset =0	1018	-138890	109
100MC-100CC	1050	-138214	94.5
500MC-500CC	1052	-140604	110
100MC-200CC	1400	-91320	98.3
200MC-100CC	1431	-186003	118
Noise = 1.5*FF Noise	826	-142010	110
Noise = 2*FF Noise	664	-139786	123
Noise = 3*FF Noise	468	-140854	144
Noise = 4*FF Noise	360	-140708	183
Noise = 5*FF Noise	290	-140450	194
Noise = 6*FF Noise	242	-140800	220
Noise = 7*FF Noise	208	-141432	236
Best Combination	1208	2569	3.64

The simulation results with the basic model show a gain of 1218 counts/μV and an offset of -141,094 counts for 1M clock cycles, assuming a 500 μV flip-flop noise level. This noise level is extracting from measurements of the transfer characteristics of a standalone 180-nm flip-flop, calibrated with DC voltages. Measurements on the 180-nm sensor system with self-calibration shows a gain of 973 counts/μV and an offset of 2300 counts for 4M clock cycles. The noise level inferred from the transfer characteristic is 3.5 mV.

The difference between the two noise values is 3.46 mV. The four noise sources not accounted for in simulation were supply noise fed into the flip-flop via the calibration nodes, inputs and PMOS devices, clock noise fed into the flip-flop, calibration capacitor drift, and variation in calibration voltage for each measurement period.

The capacitor drift analysis provided earlier showed that the measured drift is two orders of magnitude smaller than a single calibration pump step size, so is an insignificant factor. Even if the drift was significant, it would show up as an offset in the measurement results, since the flip-flop offset is always in the same direction, so the calibration capacitor voltages will have a nominal value, and always drift in the same direction (towards $V_{DD}/2$). The clock configuration between the standalone flip-flop and full sensor system is the same, so the 500 μV noise inferred from the standalone flip-flop must include the clock noise. The measurement period-to-period variation in calibration voltage is related to the charge pump step size, with smaller variation for smaller step sizes. This slightly lowers the effective noise seen during measurement periods, which results in a slight increase in sensor gain, as shown in simulation. This noise source is small compared to the unexplained noise. Therefore the noise must primarily come from the supply.

The measured 37 mV offset of the flip-flop represents a 3% mismatch, so roughly 3% of common mode input, supply and calibration noise will appear on the flip-flop output. The extra 3.46 mV of noise could be explained by a 115 mV of high frequency supply noise. The tester was implemented with an FPGA board operating at 150 MHz, to generate 40 MHz clock signals for the BICS. These could be the source of high frequency noise seen on the supply. The BICS sensor chip was mounted on a wire-wrap board with

long wire-wrap wires between decoupling capacitors and the chip supply pins. Thus switching activity of all the BICS test structures on the chip, plus noise on the FPGA board, could inject significant noise into the BICS supply.

There were no quantitative supply noise measurements taken in [1], but anecdotal evidence suggested that noise of the necessary level was present. Due to changes in operating systems, FPGA boards and FPGA software, it was not possible to exactly duplicate the test conditions of [1]. An approximate test fixture was created using the original BICS prototype board and a newer FPGA board, the Xilinx Xup Vertix II Pro Development System. The test logic used in the original experiments was remapped to the new I/O pins and compiled for the board. Measurements were made with a Fluke 124 Industrial Scopemeter, operating as a 40 MHz oscilloscope. Measurements were made through a high pass filter to estimate the noise seen by the flip-flop after auto-zeroing. For the probes available, we used filters of 16 kHz and 6.6 kHz implemented in a wireless breadboard (protoboard). For both filters, the RMS supply noise measured at the chip was only 10 mV. We felt that the filters in combination with the protoboard were creating a low pass filter, so the protoboard was removed and the RMS noise level was measured at approximately 100 mV. We also found that not all the clocks were being generated for the chip, and were not able to diagnose to poorly documented FPGA code. Thus the BICS chip was not operating in its normal configuration during noise measurements. Given the considerable effort required to completely rewrite the FPGA code for the new board, we felt that the noise measurements were close enough to explain the inferred sensor noise.

8. CONCLUSIONS AND FUTURE WORK

A behavioral model of a voltage based built-in current sensor was developed and simulated. The results of the simulation show a very good match between the model and the actual sensor.

The effects of different parameters on the system were investigated. The value of the charge pump has a direct effect on the output offset and nearly no effect on the system gain. The number of measurement cycles versus the number of calibration cycles as well as the overall noise suffered by the system has a direct effect on the system gain.

Some key learnings of this research:

- The sensor gain and offset is not very sensitive to charge pump step size. A much smaller step size results in slightly higher gain, due to smaller measurement period-to-period calibration voltage variation.
- The sensor offset is sensitive to mismatch between the charge pump up and down step sizes. It is not very sensitive to pump step size.
- Calibration capacitor drift is not important except for very leaky capacitors.
- Once the sensor is in calibration, it takes very few calibration cycles to bring it back into calibration, for the negligible calibration capacitor drift assumed here. Beyond the initial calibration period (whose length depends on the calibration charge pump step size) clock cycles should be primarily devoted to measurement, to maximize the resolution for a given BICS total measurement time.

The primary conclusion of the modeling work is that the dominant noise source in the sensor is supply noise injected into the flip-flop via flip-flop mismatch. Future sensor designs must focus on reducing supply noise, reducing supply noise injection into the flip-flop, and reducing flip-flop mismatch. Larger flip-flop transistors would significantly improve matching, while only slightly increasing BICS area. The corner frequency of the input low pass filters can be significantly lowered with only a small increase in circuit area. A new design should include a low pass filter on the supply feeding the flip-flop and calibration capacitors. Given the calibration capacitors, this can be implemented by including a series resistance in the supply line and adding an additional decoupling capacitor.

The secondary conclusion is that the main calibration concern is equalizing charge pump up and down cycles to reduce the measurement offset. Given that the imbalance is due to the NMOS vs. PMOS junction parasitics on minimum size devices, this cannot be directly minimized by the designer without using significantly larger pump transistors and capacitors, greatly increasing sensor area. Since the offset is a function of process parameters (junction parasitics, flip-flop mismatch), it is essentially fixed for each sensor, so can be removed by I_{DDX} post-processing techniques.

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APPENDIX A

Charge Pump Change Effect:

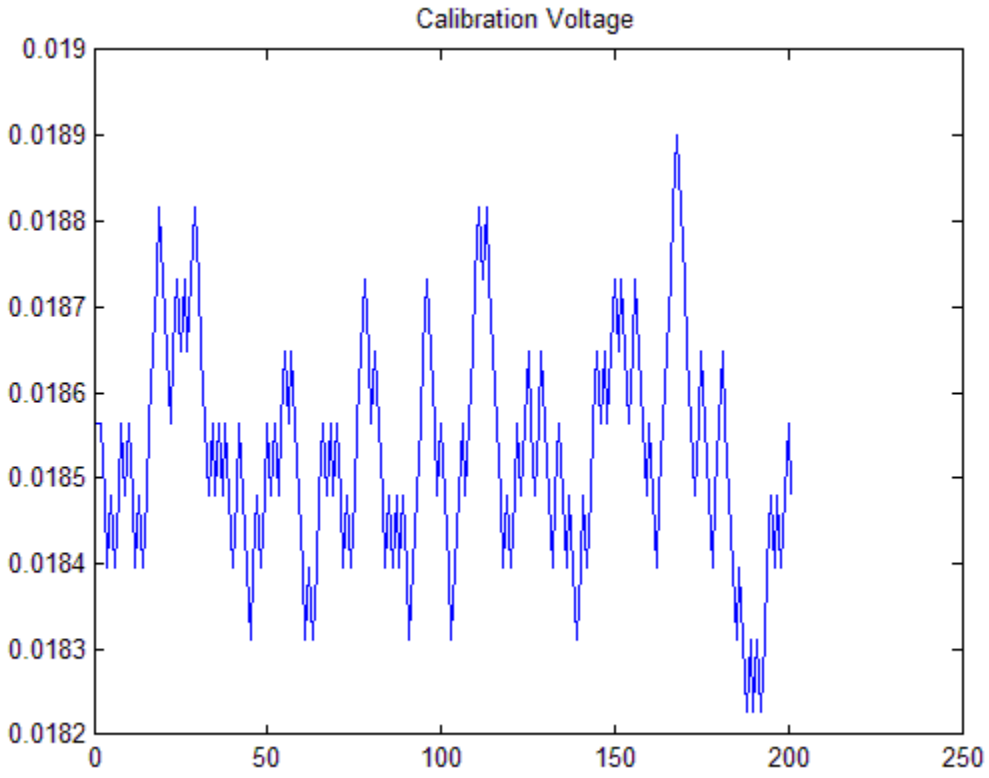

Fig. 24. Calibration Voltage (Zoomed), 84 µV Pump Step Size.

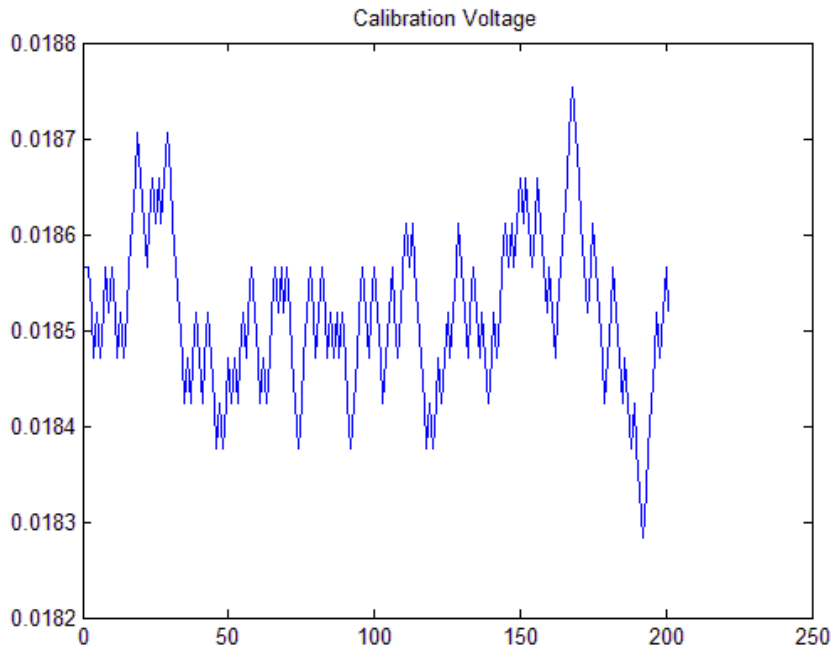

Fig. 25. Calibration Voltage (Zoomed), 47 µV Pump Step Size.

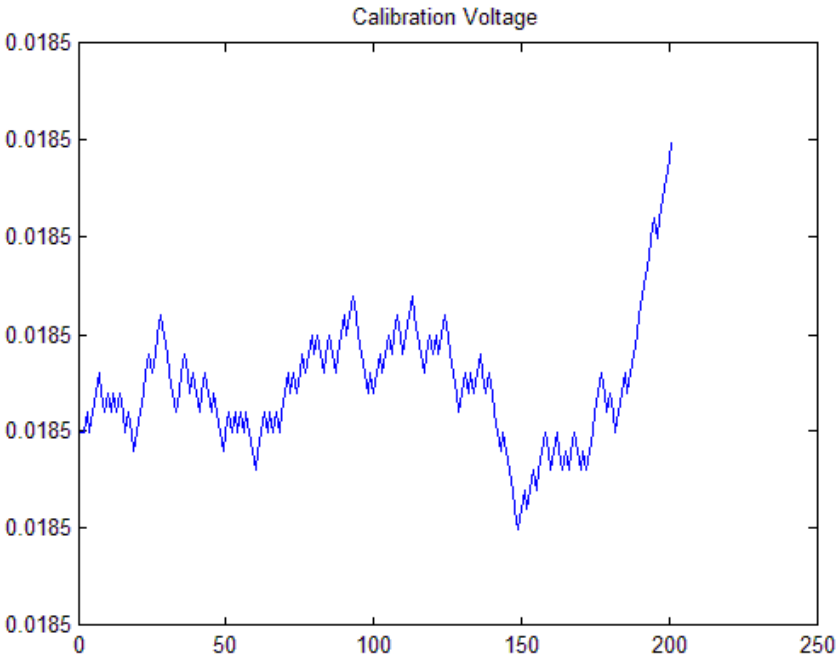

Fig. 26. Calibration Voltage (Zoomed), 1 µV Pump Step Size.

Offset Change Effect

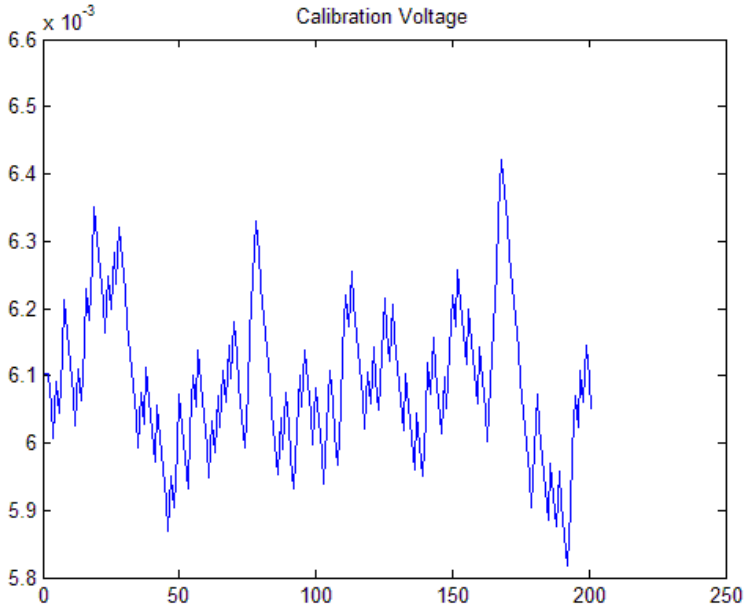

Fig. 27. Calibration Voltage (Zoomed), 12 mV Offset.

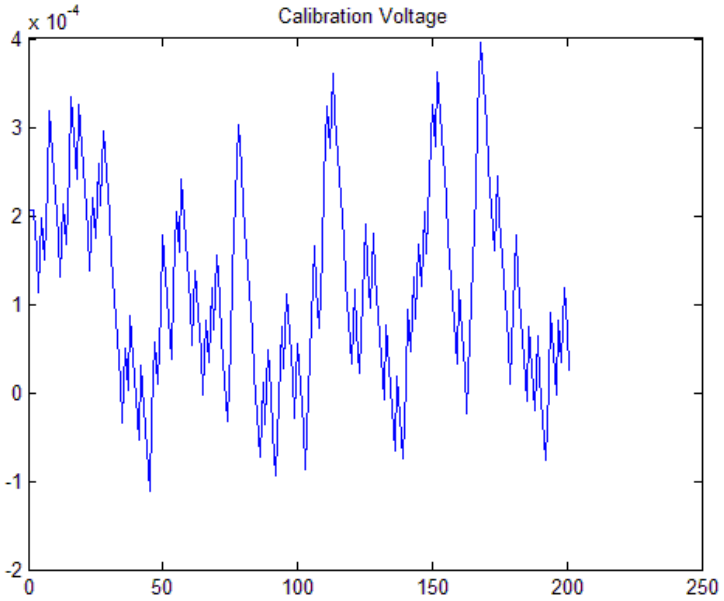

Fig. 28. Calibration Voltage (Zoomed), 0 V Offset.

Measurement Cycles vs. Calibration Cycles:

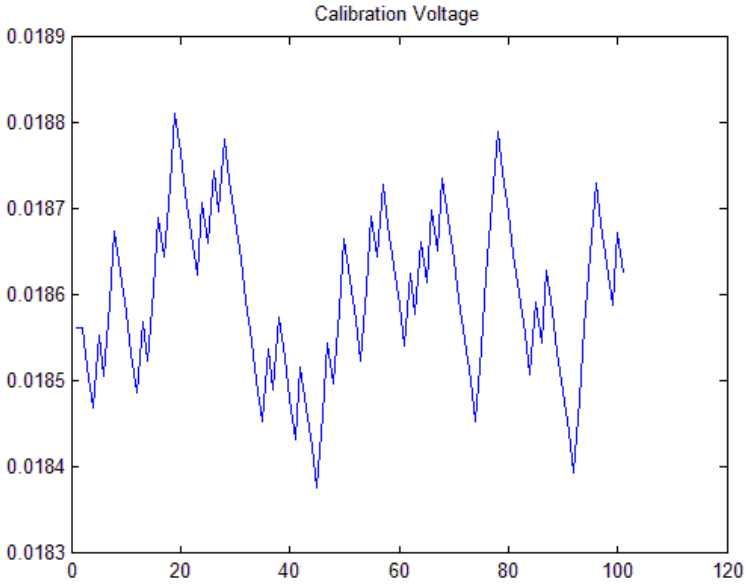

Fig. 29. Calibration Voltage (Zoomed), 100MC-100CC.

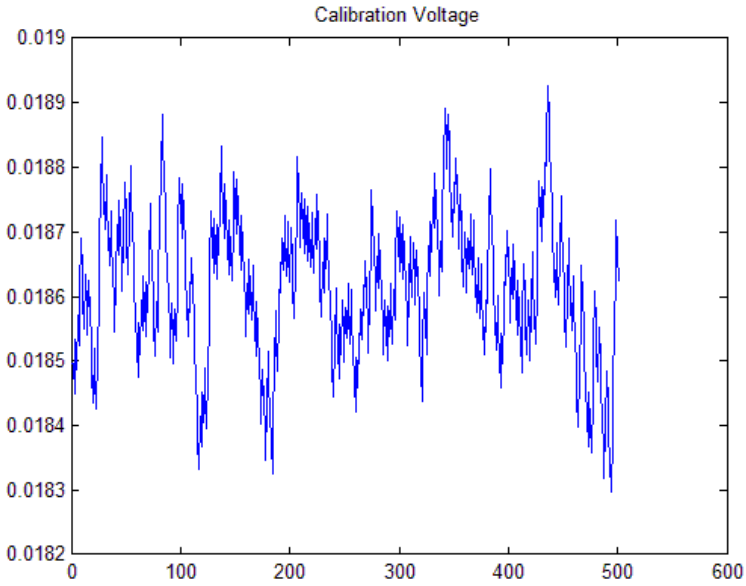

Fig. 30. Calibration Voltage (Zoomed), 500MC-500CC.

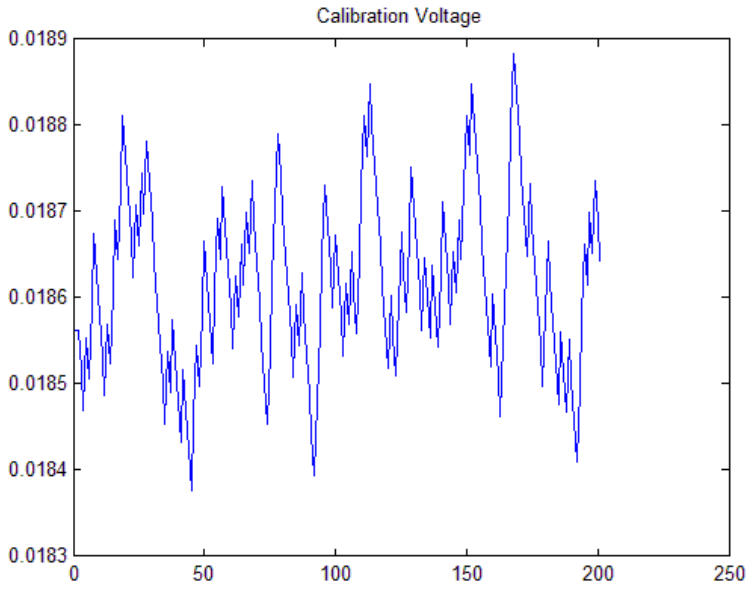

Fig. 31. Calibration Voltage (Zoomed), 100MC-200CC.

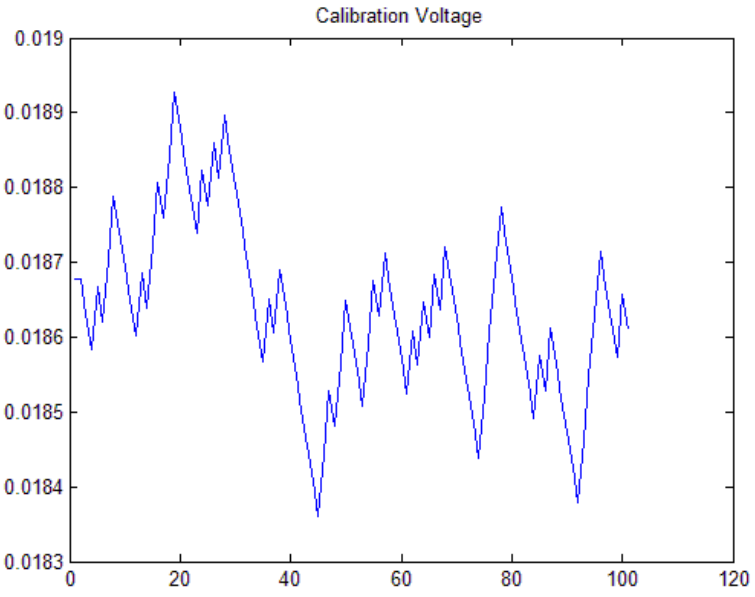

Fig. 32. Calibration Voltage (Zoomed), 200MC-100CC.

Noise Change Effect:

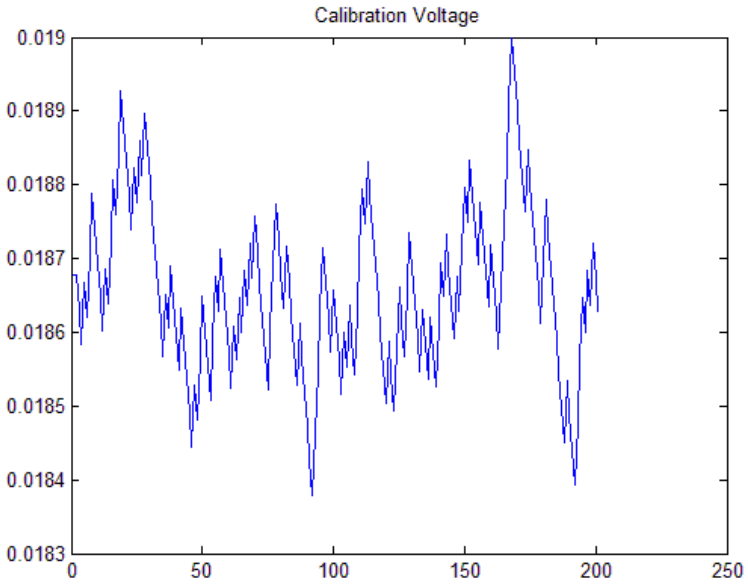

Fig. 33. Calibration Voltage (Zoomed), Overall Noise = 1.5 * FF Noise.

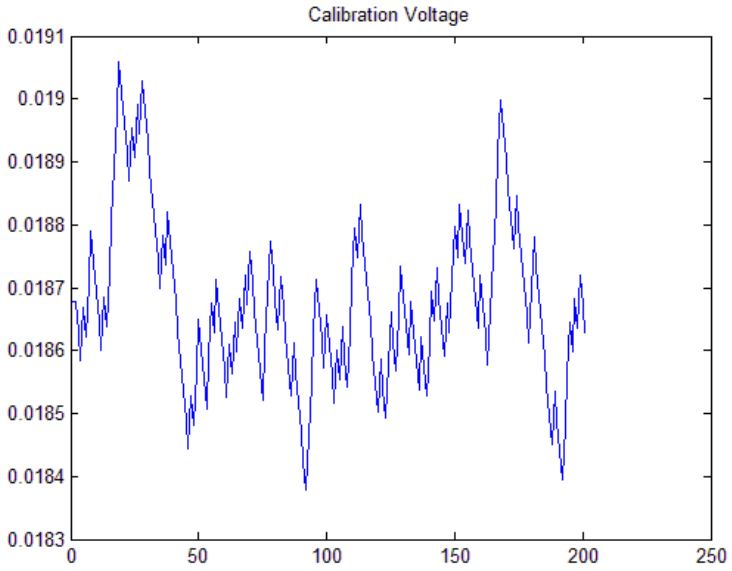

Fig. 34. Calibration Voltage (Zoomed), Overall Noise = 2 * FF Noise.

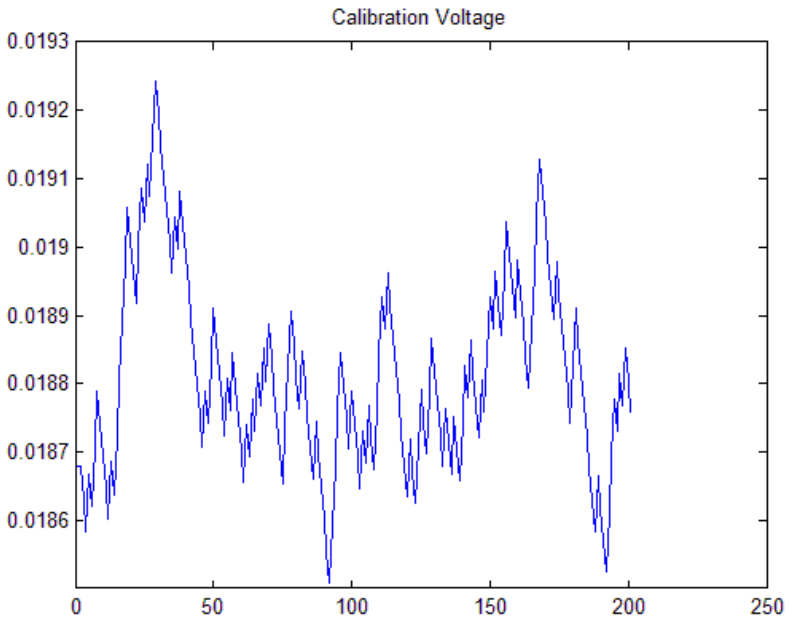

Fig. 35. Calibration Voltage (Zoomed), Overall Noise = 3 * FF Noise.

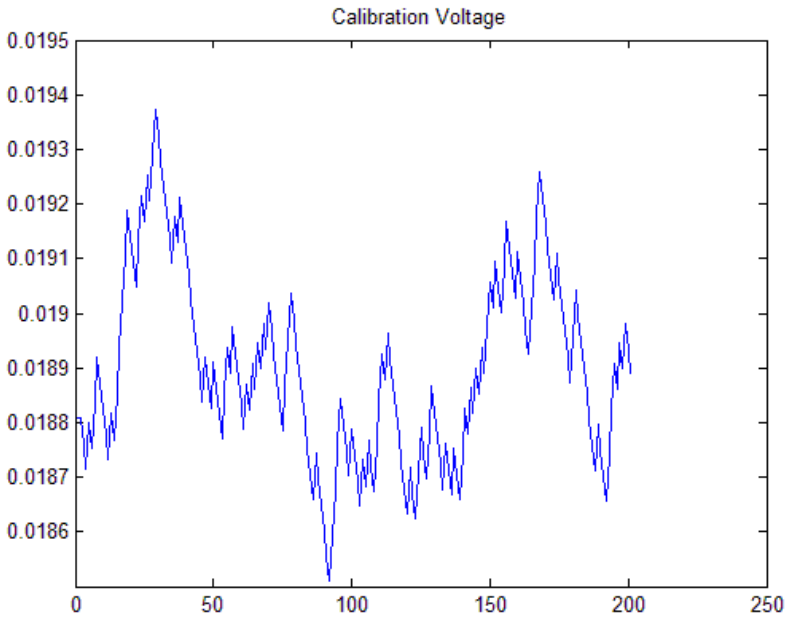

Fig. 36. Calibration Voltage (Zoomed), Overall Noise = 4 * FF Noise.

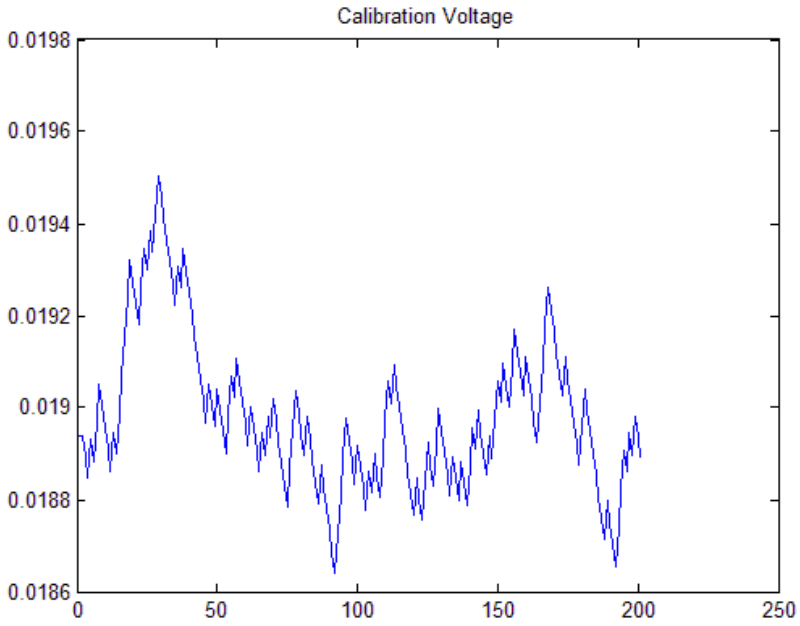

Fig. 37. Calibration Voltage (Zoomed), Overall Noise = 5 * FF Noise.

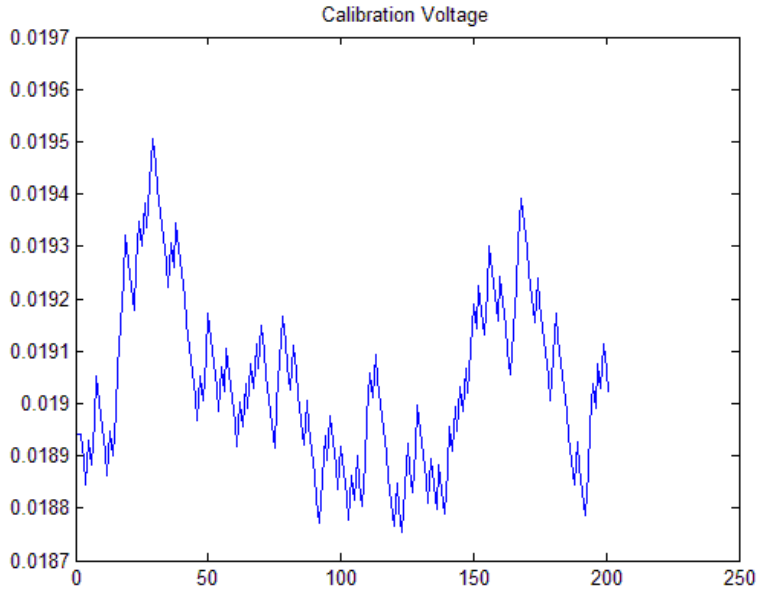

Fig. 38. Calibration Voltage (Zoomed), Overall Noise = 6 * FF Noise.

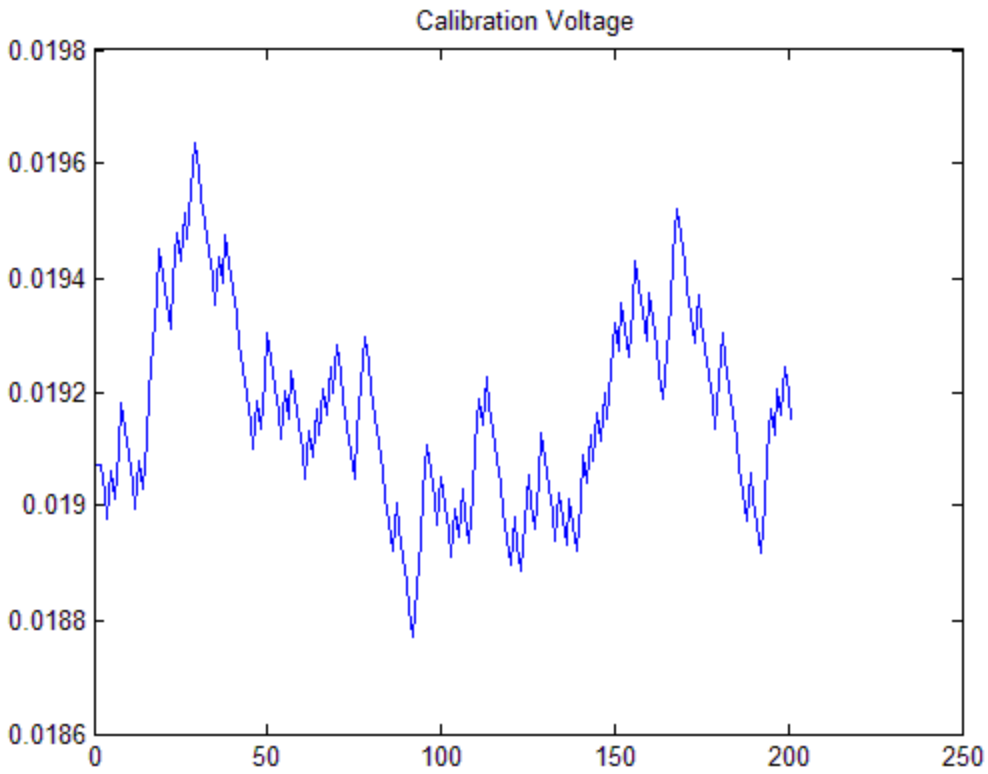

Fig. 39. Calibration Voltage (Zoomed), Overall Noise = 7 * FF Noise.

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