A VERSATILE REAL-TIME SPECTRAL ANALYSIS SYSTEM

A Thesis

by

MARK STEVEN HANCOCK

Submitted to the Graduate College of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 1986

Major Subject: Electrical Engineering

A VERSATILE REAL-TIME SPECTRAL ANALYSIS SYSTEM

A Thesis

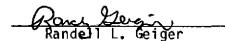
by

MARK STEVEN HANCOCK

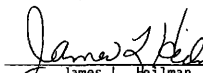
Approved as to style and content by:

B. Randall Jean
(Chair of Committee)

Richard W. Newton
(Member)



Randell L. Geiger
(Member)



James L. Heilman
(Member)

Jo W. Howze
(Department Head)

May 1986

ABSTRACT

A Versatile Real-Time Spectral Analysis System (May 1986)

Mark Steven Hancock, B.S., Texas A&M University

Chair of Advisory Committee: Dr. B. R. Jean

A variety of applications exist, such as the processing of radar scatterometer data and chirp FM radar signals, which require the analysis of the spectrum of the incoming signal. In order for these applications to be implemented in real-time, a system is needed which can compute a signal's spectrum and still be small and light enough to be considered portable.

Recent advancements in technology have allowed the design of such a system based on a charge coupled device (CCD) implementation of the chirp-Z transform (CZT). The design uses four multiplying digital-to-analog converters and a CCD quad chirp transversal filter to perform the CZT operation. By using a CCD transversal filter to implement the convolution operation of the transform, the vast amount of sequential processing which would normally be required to compute the spectrum of the signal are rather performed in parallel. This allows the system to keep pace with high system sampling rates and wide signal bandwidths. Also, because the CCD is small and very low power, the total system can be made small and lightweight.

ACKNOWLEDGEMENTS

I would like to express my thanks to the following people:

Dr. B. R. Jean for his technical guidance

Eugen Hriscu for helping put all of the figures together

Gloria Johnson and Christine Kapple for getting this document together

All of the friends and family that wouldn't let me give up.

TABLE OF CONTENTS

TABLE OF CONTENTS (continued)

TABLE OF CONTENTS (continued)

LIST OF FIGURES

LIST OF FIGURES (continued)

CHAPTER I

INTRODUCTION

In recent years, increased emphasis has been placed on the need for the development of versatile real-time spectral analysis systems. This has come about mostly because of an increasing number of applications which require spectral analysis and because of the ready availability of small microprocessor based computers which have allowed many existing applications to be performed in a real-time environment.

This report analyzes the design of one such spectral analysis system, identifies its deficiencies, and proposes an improved design. In this chapter several techniques are presented by which spectral analysis can be performed. The technique used by both the current and revised systems is identified and compared with the other techniques to identify its advantages and disadvantages. Also, two applications are discussed in which the revised system could be used to perform real-time data analysis.

A. Techniques for Spectral Analysis

There are many spectral analysis techniques. Roberts, Moule, and Parry [1] recently presented a paper which identifies a large number of these techniques. Four of the most popular of these techniques are reviewed here. These are: the filter bank, sliding filter, dispersive filter, and discrete Fourier transform techniques.

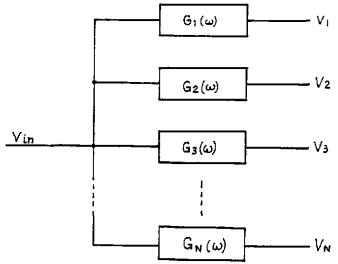
This thesis follows the style and format of the Proceedings of the IEEE.

1) Filter Bank Technique: The filter bank technique is the fastest of all the spectral analysis techniques. However, a comparatively large amount of hardware is required to implement it if both wide bandwidth and fine spectral resolution are desired.

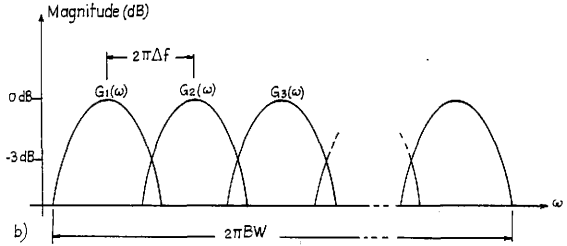
Figure 1 illustrates the filter bank technique. A large number of narrow band filters are placed in parallel. The bandwidths of the filters are equal to the desired spectral resolution, and the center frequencies are spaced evenly to cover the frequency band being analyzed. Each filter's output represents the energy contained within its particular band. The time required to estimate the spectral content of a signal using the filter bank technique is limited by filter propogation time, which is proportional to the inverse of the system's spectral resolution.

2) Sliding Filter Technique: The sliding filter technique requires much less hardware than the filter bank technique, but is much slower. In this technique, only a single filter is used. This filter is used to measure the spectral content of the input signal by sweeping its center frequency across the frequency band being analyzed. Figure 2 illustrates one method of accomplishing this.

In Figure 2 the input signal is mixed with a swept local oscillator. As the oscillator is swept, different sections of the input signal's spectrum appear in the pass band of the filter. The bandwidth of this filter is equal to the desired spectral resolution. Propogation time through the filter determines maximum sweep rate and thus minimum spectral estimation time. The fastest achievable spectral estimation time is $T = BW/\Delta f^2$ where BW is the system bandwidth, and Δf is the desired spectral resolution.



a)

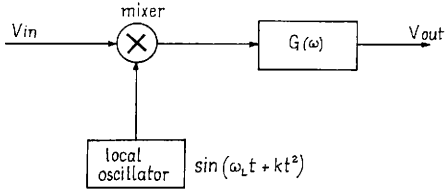


b)

$N = \frac{BW}{\Delta f}$

BW = system bandwidth
Δf = spectral resolution

Figure 1 - Filterbank Technique for Spectral Analysis
a) Block diagram
b) Filter frequency response characteristics



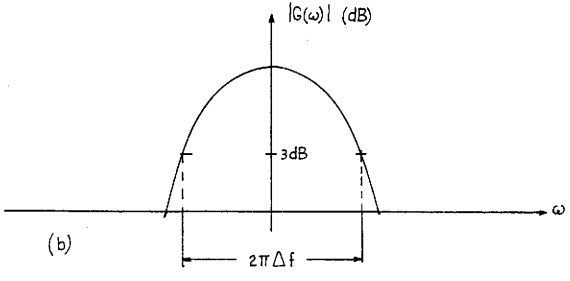
(a)

$\omega_L = \omega_o - \pi BW$

$k = \pi(\Delta f)^2$

Δf = spectral resolution

BW - system bandwidth



(b)

Figure 2 - Sliding filter technique for spectral analysis

a) Block diagram
b) Filter frequency response characteristics

The sliding filter technique is a popular technique for spectral analysis because of versatility and low cost. It is very slow, however, and thus not well suited for real-time systems. Laboratory spectrum analyzers commonly use this technique since they place more emphasis on low cost than high speed. The sliding filter technique is so easily implemented in hardware that a recent article described how to implement it using a single integrated circuit [2].

3) Dispersive Filter Technique: Dispersive filters have been used since the days of Isaac Newton to perform spectral analysis. During this early time, spectral analysis was being performed at optical frequencies. One common dispersive filter used was the prism. Not until the advent of surface-acoustic-wave (SAW) devices, and the recent development of magneto-standing-wave (MSW) devices, have dispersive filters been usable for spectral analysis of electrical signals.

Dispersive filters can directly compute the Fourier integral. To accomplish this, the Fourier integral must be mathematically rearranged to a form which is more easily implemented in hardware. By making the substitution

$$2w\tau = \left(\frac{w}{\mu}\right)^2 + (\mu\tau)^2 - \left(\mu\tau - \frac{w}{\mu}\right)^2 \tag{1.1}$$

the exponent is split into three parts. After rearranging terms, the Fourier integral

$$F(\omega) = \int_{-\infty}^{\infty} f(\tau)e^{-j\omega\tau}d_{\tau} \tag{1.2}$$

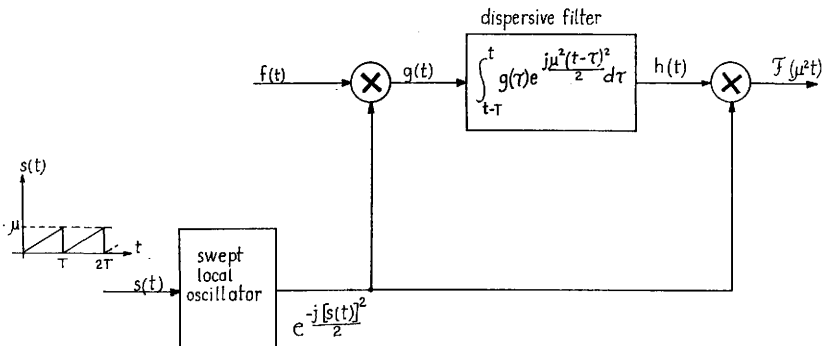


Figure 3. Dispersive filter technique for spectral analysis

becomes,

$$F(\omega) = e^{-j\frac{(\frac{\omega}{\mu})^2}{2}} \int_{-\infty}^{\infty} [f(\tau)e^{-j\frac{(\mu\tau)^2}{2}}]e^{\frac{j(\mu\tau - \frac{\omega}{\mu})^2}{2}} d\tau. \qquad (1.3)$$

This equation, sometimes called the "chirp transform," cannot be implemented in hardware because of the infinite integral. Also, the output of a dispersive filter should be represented as a function of time not radian frequency. These two requirements can be met by making the substitution $\omega = \mu^2 t$ and setting the integral limits to integrate over the past T seconds. With these alteration, Equation 1.3 becomes

$$F(\mu^2 t) \approx e^{-j\frac{(\mu t)^2}{2}} \int_{t-T}^{t} [f(\tau)e^{-j\frac{(\mu\tau)^2}{2}}] e^{j\frac{\mu^2(t-\tau)^2}{2}} d\tau. \qquad (1.4)$$

This equation can be implemented in hardware using a dispersive filter as shown in Figure 3. Three operations are required: convolution, pre-multiplication, and post-multiplication. The final operation (post-multiplication) is not required if only the spectral magnitude is desired. Post-multiplication affects only the phase of the spectral output. Pre-multplication and post-multiplication are performed using a swept local oscillator and two analog mixers. The convolution is performed using a dispersive filter. For a description of how a SAW dispersive filter can be used to implement the chirp transform consult Jack and Paige's paper [3] on Fourier transform processors.

The dispersive filter technique is very effective however,

current technology severely restricts the versatility of a spectral analysis system employing the technique. Alteration of the system's bandwidth or spectral resolution requires physical modification of dispersive filter, thus it is often not a selectable option. Also, the technique is generally limited to high frequency signals. The operating range of surface-acoustic-wave devices is limited to the 10 MHz to 1GHz frequency range [1] and magneto-standing-wave devices operate at even higher frequencies. The dispersive filter technique for spectral analysis is therefore limited to high frequency applications where system versatility is not required.

4) Discrete Fourier Transform Techniques: The discrete Fourier transform is the discrete time equivalent of the continuous time Fourier integral shown in Equation 1.2. This transform is very useful because it can be used to estimate the spectral content of a signal. The equation for the discrete Fourier transform is

$$F_k = \sum_{n=0}^{N-1} f_n e^{\frac{-2\pi jnk}{N}} \qquad k = 0,1,2,\ldots N-1. \tag{1.5}$$

If the sequence $\{f_n\}$ is generated by uniformly sampling f(t) N times in a period of time T, then $\{F_k\}$ will represent the estimates of the spectrum of f(t), uniformly spaced at intervals of 1/T in frequency.

Two major problems plague the discrete Fourier transform. These problems are aliasing and frequency leakage. Aliasing occurs when the input signal is sampled. Because of this sampling process, an infinte number of different signals f(t) can produce the identical sampled sequence $\{f_n\}$. This ambiguity in the time domain is also

transferred to an ambiguity in the frequency domain. The frequency domain ambiguity, or aliasing, causes frequencies which are separated by integer multiples of the sample frequency to be indistinguishable. The second problem, frequency leakage, is caused when f(t) is not periodic with period T. A discontinuity is introduced in to $\{f_n\}$ which causes a severe loss in spectral resolution. Details of the frequency leakage problem are deferred until Chapter II and Appendix A.

Direct computation of the discrete Fourier transform can require a large amount of time. Two techniques have been developed which reduce this amount of time. These techniques are the fast Fourier transform and the chirp Z-transform. Both transforms are mathematically identical to Equation 1.5 but their structure allows for easier implementation.

a) Fast Fourier Transform: The fast Fourier transform (FFT) is specifically designed for sequential machines (such as a digital computer). The transform was developed in 1965 by Cooley and Tukey [4]. It minimizes the number of sequential operations required to compute the discreter Fourier transform. Computation of the discrete Fourier transform from Equation 1.5 requires $4N^2$ real multiplications. If N is an integral power of 2, then the FFT can be used instead. By using the FFT to compute the discrete Fourier transform only $2N\log_2 N$ real multiplications are required. The fast Fourier transform accomplishes this increased speed through extensive re-use of intermediate results. For a transform of length N=512, the fast Fourier transform is in excess of one hundred times faster than the direct

computation of the discrete Fourier transform. The dominant disadvantages of the fast Fourier transform are cost, size, and power consumption. Recent development of high speed digital multipliers and high performance micro-processors have reduced the cost and size restrictions; however, these devices still consume large amounts of power. For additional details on the fast Fourier transform consult Cooley and Tukey's paper [4].

b) Chirp Z-Transform: The chirp Z-transform is another algorithm for computing the discrete Fourier transform. This transform is designed for easy implementation using a transversal filter. The chirp Z-transform is the discrete time equivalent of the chirp transform discussed earlier. It was presented by Bluestein [5] in 1968. By making the substitution $2nk = n^2 + k^2 - (n-k)^2$ the equation for the discrete Fourier transform can be rewritten to form the chirp Z-transform

$$F_k = e^{\frac{-j\pi k^2}{N}} \sum_{n=0}^{N-1} \left(f_n e^{\frac{-j\pi n^2}{N}}\right) e^{\frac{j\pi(n-k)^2}{N}} \qquad k = 0,1,2,\ldots N-1. \quad (1.6)$$

Another version of the transform is called the sliding chirp Z-transform. It is very similar but has different summation limits. The equation for the sliding chirp Z-transform is

$$F_k = e^{\frac{-j\pi k^2}{N}} \sum_{n=k}^{k+N-1} \left(f_n e^{\frac{-j\pi n^2}{N}}\right) e^{\frac{j\pi(n-k)^2}{N}} \qquad k = 0,1,2,\ldots N-1. \quad (1.7)$$

Both these transforms consist of three operations: pre-multiplication,

magnitude is desired. Figure 4 shows how both forms of the chirp Z-transform can be implemented in hardware.

The sliding version of the chirp Z-transform is more commonly used than the stationary version. This is because it is much faster and easier to implement. The structure of the sliding chirp Z-transform allows input sampling and transform computation to occur simultaneously. The sliding chirp Z-transform is the spectral analysis technique used by both systems presented in this report. A detailed analysis of both forms of the chirp Z-transform are discussed in Chapter II.

The most significant disadvantage of the chirp Z-transform is poor dynamic range. When implemented using a charge coupled device transversal filter, a dynamic range of 60dB is probably achievable. Higher dynamic ranges have been proposed as achievable [6], but practical considerations and the effects of frequency leakage make these levels difficult if not impossible to reach for a wide variety of input signals. System bandwidths from 4KHz to 2MHz have been achieved, and bandwidths from 25Hz to 10MHz have been proposed [6] as theoretically achievable. High speed, versatility, and low power consumption make the chirp Z-transform technique for spectral analysis an excellent choice for systems not requiring an extremely high dynamic range.

B. Applications Requiring Spectral Analysis

Many applications exist which require spectral analysis. Two such applications are real-time radar scatterometer and chirp fm radar data processing. In both of these applications, processing of the

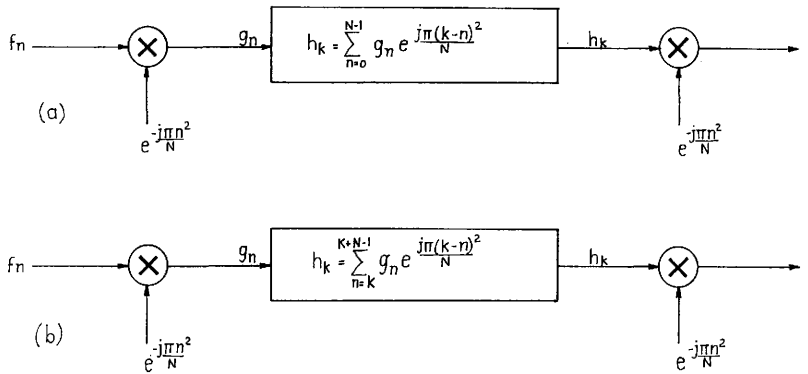


Figure 4. Implementing the Chirp Z-Transform

(a) Stationary Chirp Z-Transform
(b) Sliding Chirp Z-Transform

data requires the computation of its power spectrum. Performing this task in a real-time environment is difficult. The development of the two systems presented in this report was undertaken to overcome this difficulty. The current system was developed for NASA to aid in the real-time processing of radar scatterometer data. However, this system lacks the versatility to be used for other applications. A description of the two applications mentioned above is presented here to help identify the requirements for the spectral analysis system.

1) Real-Time Radar Scatterometer Data Processing: A radar scatterometer is a calibrated radar system which can be used to measure a target's radar scattering coefficient as a function of observation angle. Radar scatterometers are very effective tools in the field of remote sensing. Work done at the Remote Sensing Center at Texas A&M University has shown that scatterometers can be used to remotely monitor arctic ice type [7] and soil moisture content [8].

Airborne fan beam radar scatterometers employ the Doppler principle to resolve different observation angles. Figure 5 illustrates how this is accomplished. A CW radar beam is transmitted to the surface, scattered by the surface material, and received by an onboard antenna. The transmitted beam is very narrow in the cross track dimension and wide in the along track dimension. The Doppler effect causes the return from each angle to be shifted in frequency. The sum of return signals thus produces a result which has been spread in frequency by the Doppler effect. Separation of the received signal into the returns from each angle requires computation of the spectrum of the received signal. Computation of this spectrum is currently

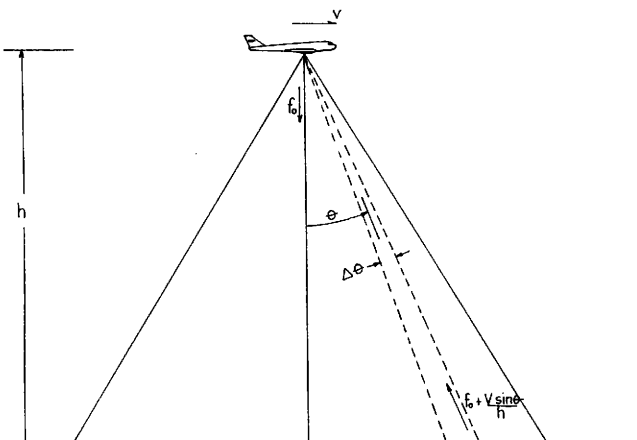


Figure 5 - Real-Time Radar Scatterometry

accomplished using the fast Fourier transform (FFT) technique for spectral analysis. Since the FFT requires a large amount of computational power, data must be recorded in real-time and post-processed on large ground-based computers. The resulting time lag between data acquisition and final product has proven to be excessive.

Real-time processing of scatterometer data would dramatically reduce costs, and data lag times. To accomplish this, a spectral analysis system is required which can real-time process the return signal. Because the system must be placed on board the aircraft, it should be small, low power, and lightweight.

In 1976 the Remote Sensing Center completed work on a real-time quick look radar scatterometer processor [9]. This processor used the sliding filter technique to perform its spectral analysis. Because the technique was too slow, data could not be fully processed for a large number of angles. Also, the system did not produce data of sufficient accuracy for analytical use. The processor did, however, accomplish three major tasks. It allowed for the verification of proper system operation, it helped identify which data should be post-processed on ground based computers, and it identified that full real-time data processing would soon be possible.

Full real-time processing of radar scatteroeter data was accomplished in 1979 [10] using the chirp Z-transform spectral analysis technique. The spectral analysis system contained within the processor, uses a charge coupled device to compute the transform. This device was developed by Texas Instruments in 1975 [6] and placed into production by Reticon in 1978. Development of this system has

proven that full real-time processing of radar scatterometer data is feasible using current technology. The development has also shown, however, that the system requires refinement. The refinement of this spectral analysis system is the subject of this report.

2) Chirp FM Radar Data Processing: Another application requiring spectral analysis is chirp fm radar data processing. This is because target range information is frequency encoded. For multiple targets, determination of target range requires the computation of the spectrum of the radar output signal. To explain this requirement, it is necessary to review the mechanics of such a radar system.

A block diagram of a simple chirp fm radar is shown in Figure 6. The radar functions are as follows. The swept local oscillator generates the linear fm signal shown in Figure 7b. This signal is transmitted, reflected by the target, and received by the antenna. Because of the finite speed of the transmitted signal, the received signal (Figure 7c) is delayed in time. Because the two waveforms are swept in frequency, the time delay produces a constant frequency difference. Mixing the two signals, then low-pass filtering the result, produces a sine wave whose frequency is this difference. Unfortunately, a higher freqency signal is also produced by the re-starting of the sweep process. This is shown in Figure 7d. The adverse effect of the high frequency sine wave can be minimized by using long sweep times. For single target systems, the range to the target can be obtained by measuring the frequency of the output signal.

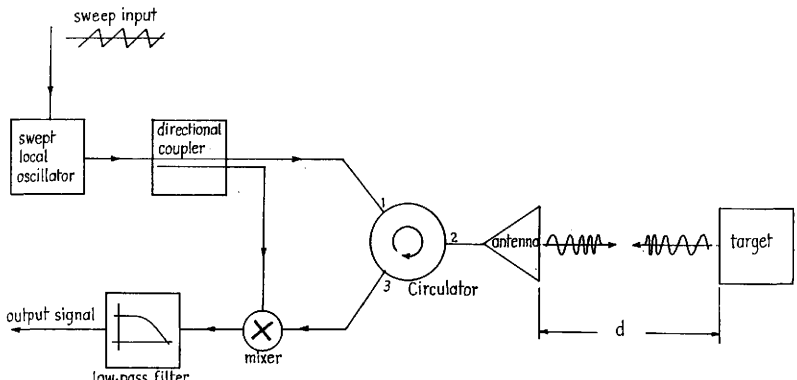


Figure 6 - Chirp FM Radar Block Diagram

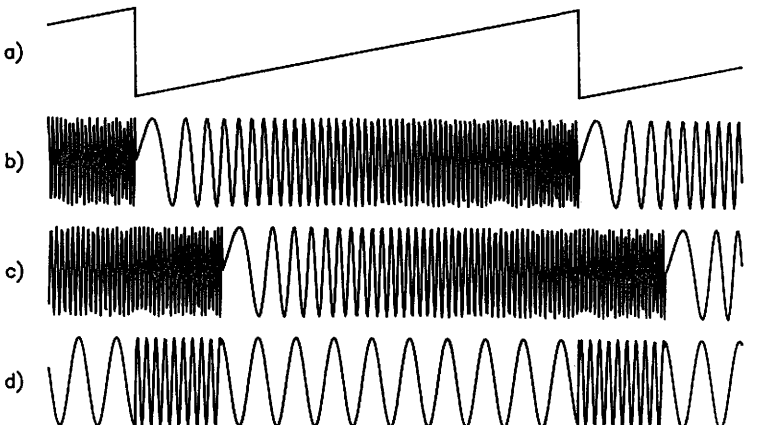


Figure 7 Chirp FM Radar Signals
a) Sweep Input
b) Transmitted Signal
c) Received Signal
d) Filtered Output

Multiple targets as well as other sorts of reflections are, unfortunately, the case of the real world. In these cases, the output signal is the sum of the results for each individual target or reflection. To separate these signals, the spectrum of the output signal must be computed. This can be performed using a spectral analysis system. To ensure flexibility of the radar system the bandwidth and spectral resolution of the spectral analyzer must be alterable. One application where this is particularly desirable is tracking a single target. Wide bandwidths are first used while searching for a target. Once the target has been found, the bandwidth is tightened down to more precisely identify its exact position and track it.

Spectral analysis systems which employ the discrete Fourier transform technique for spectral analysis are particularly useful in chirp fm radar systems. The bandwidths and spectral resolution are easily alterable, and the aliasing effect can often be used as an advantage in such applications as single target tracking. Of the two techniques discussed previously for computing the discrete Fourier transform, the chirp Z-transform appears to lend itself particularly well to the processing of chirp fm radar data. This is because the chirp Z-transform can be implemented using a charge coupled device to produce a small, lightweight, low power spectral analysis system. These attributes are especially important since chirp fm radar systems are used in aircraft where space, weight and power are at a premium.

C. Report Objectives

The Microwave Microelectronics Laboratory at Texas A&M University

is often involved in applications which require spectral analysis. The two applications previously discussed are examples of such work. Previously it has been the case to custom design hardware for each specific application. The advent of microprocessors has made is possible to design general purpose hardware and then write software to customize the system for a specific application. Unfortunately, current microprocessors do not have sufficient computing power to perform spectral analysis. The objective of this report is to design a versatile spectral analysis system which is easily interfaced to a microprocessor. This system must be capable of performing spectral analysis in real-time and allow alteration of its bandwidth and spectral resolution from software. To allow easy incorporation in current projects, the system is designed to plug directly into an Intel MULTIBUS standard card cage.

The design of the spectral analysis system is based on the chirp Z-transform. A charge coupled device manufactured by Reticon is used to implement the transversal filter. The design is based on a current design used for processing radar scatterometer data. Many modifications have been made to increase the system's performance and versatility. In the following chapters, the theoretical basis of the chirp Z-transform will be examined, the current spectral analysis system will be analyzed, and the revised design will be presented.

CHAPTER II

EXAMINATION OF THE CHIRP Z-TRANSFORM

A. Introduction

Both systems presented in this report utilize the chirp Z-transform to perform spectral analysis. This chapter examines both the mathematics of the transform and its hardware implementation.

B. The Chirp Z-Transform

In 1968, Bluestein [5] found that when a simple substitution was made into the equation for the discrete Fourier transform, the equation could be decomposed into three operations. The resulting equation he called the chirp Z-transform.

1) Derivation of the Chirp Z-transform: The chirp Z-transform (CZT) is formed by first starting with the equation for the discrete Fourier transform.

$$F_k = \sum_{n=0}^{N-1} f_n \, e^{\frac{-j\pi(2nk)}{N}} \qquad k = 0, 1, 2, \ldots N-1 \tag{2.1}$$

The Bluestein substitution is then used to break up the product term 2nk which appears in the exponential. The Bluestein substitution is

$$2nk = n^2 + k^2 - (n-k)^2 \, . \tag{2.2}$$

When the substitution is performed, and the resulting exponential is broken into three parts the result is the CZT.

$$F_k = e^{\frac{-j\pi k^2}{N}} \sum_{n=0}^{N-1} \left[f_n e^{\frac{-j\pi n^2}{N}}\right] e^{\frac{j\pi(n-k)^2}{N}} \qquad k = 0,\ 1,\ 2,\ \ldots\ N-1 \qquad (2.3)$$

It is very important to note from this derivation that the CZT is mathematically equivalent to the discrete Fourier transform. Both transforms exhibit the exact same properties and characteristics. The CZT, like the fast Fourier transform (FFT), is just a mathematical manipulation of the discrete Fourier transform which allows for easier computation.

2) Structure of the Chirp Z-transform: The advantage of the chirp Z-transfer is based on its structure. This structure allows the computation of the transform with just three operations: pre-multiplication, convolution, and post-multiplication. All three of these operations are easily implemented in hardware.

The first operation required in computing the CZT is pre-multiplication. In this operation, the input sequence $\{f_n\}$ is multiplied point-by-point by a sampled "down-chirp". A "down-chirp" is a linear fm waveform of decreasing frequency. This first operation produces a new sequence

$$g_n = f_n e^{\frac{-j\pi n^2}{N}} \qquad n = 0,1,2,\ldots N-1. \qquad (2.4)$$

The second operation required to compute the CZT is convolution. The pre-multiplied sequence g_n is convolved with an "up-chirp". Just like the "down-chirp," an "up-chirp" is a linear fm waveform, but of increasing rather than decreasing frequency. The result of the

convolution is

$$h_k = \sum_{n=0}^{N-1} g_n e^{\frac{j\pi(n-k)^2}{N}} \qquad k = 0,1,2,\ldots N-1. \tag{2.5}$$

The final operation required is post-multiplication. This operation multiplies the convolution result h_k by a "down-chirp". The result of post-multiplication is

$$F_k = h_k \, e^{\frac{-j\pi k^2}{N}} \qquad k = 0,1,2,\ldots N-1. \tag{2.6}$$

Post-multiplication is used to correct the phase of the convolved output h_k, producing the discrete Fourier estimates $\{F_k\}$. Many cases exist when the phase of the estimates is not required. In these cases the post-multiplication need not be done since it only effects the phase of the estimates and not their magnitude. This is very important since the output of the two systems discussed in this report compute power-spectral-density (PSD). Power-spectral-density is not dependent on the phase of the discrete Fourier estimates; because of this, pre-multiplication and convolution are the only operations required for computing power-spectral-density using the chirp Z-transform. This is much simpler than computation of power-spectral-density directly from the discrete Fourier transform.

3) The Sliding Chirp Z-transform: Another form of the chirp Z-transform is the sliding chirp Z-transform. The sliding transform is derived by performing the Bluestein substitution on the sliding discrete Fourier transform

$$F_k = \sum_{n=k}^{k+N-1} f_n e^{\frac{-j\pi(2nk)}{N}} \qquad k = 0,1,2,\ldots N-1. \qquad (2.7)$$

The equation for the sliding chirp Z-transform is

$$F_k = e^{\frac{-j\pi k^2}{N}} \sum_{n=k}^{k+N-1} \left(f_n e^{\frac{-j\pi n^2}{N}}\right) e^{\frac{j\pi(n-k)^2}{N}} \qquad k = 0,1,2,\ldots N-1. \qquad (2.8)$$

There is an important difference between the stationary and sliding chirp Z-transforms. For the stationary transform (equation 2.2), all the spectral estimates are computed using the same data. For the sliding transform, the data window slides in time as the estimates are computed. This means that every estimate is computed using a different data window. If the input sequence $\{f_n\}$ is periodic with period N, then the estimates produced by the stationary and sliding transforms will be identical. If not, then the estimates produced by the two transforms may differ. The exact nature of this difference is rather complicated. A detailed discussion of this difference is presented in Appendix A. When used for spectral analysis both transforms exhibit a comparable spectral resolution and dynamic range. This is because only the phase of the error terms differ between the transforms, and not their magnitude.

4) Windowing - Both the chirp Z-transform and discrete Fourier transform exhibit a property called "frequency leakage." "Frequency leakage" is the spilling over of a monotone input into several frequency estimates. It occurs when the input is not periodic with period NT_s where N is the transform length and T_s is the sample

interval. The reason for "frequency leakage" is that both transforms mathematically extend the input sequency $\{f_n\}$ to form a N periodic sequence. If the original input form which $\{f_n\}$ was obtained was not NT_s periodic, then this extention will produce discontinuities as illustrated in Figure 8. An illustration of this effect is shown in Figures 9 and 10. Both of these transforms represent the spectral estimates of a 512 point CZT of a sampled monotone input. For Figure 9 the input signal is

$$f(t) = e^{\frac{j2\pi(256)t}{512Ts}} . \tag{2.9}$$

Since this signal is NT_s (N = 512) periodic, no "leakage" is observed in the resulting estimates. For Figure 10 the input is not NT_s periodic. This input signal is

$$f(t) = e^{\frac{j2\pi(255.5)t}{512Ts}} . \tag{2.10}$$

The resulting estimates for this signal do exhibit "leakage" as shown in Figure 10. "Frequency leakage" is a major problem and is a significant contribution to a reduced signal-to-noise ratio and dynamic range when the chirp Z-transform or discrete Fourier transform is used for spectral estimation.

One technique for reducing "frequency leakage" is called windowing. The objective of this technique is to reduce the discontinuities produced by the extention of the input sequence. This is done by multiplying the sequence $\{f_n\}$ by a window sequence $\{w_n\}$. If $\{w_n\}$ is chosen so that the product $\{w_n f_n\}$ goes smoothly to zero at the ends, then the discontinuities caused by the extention

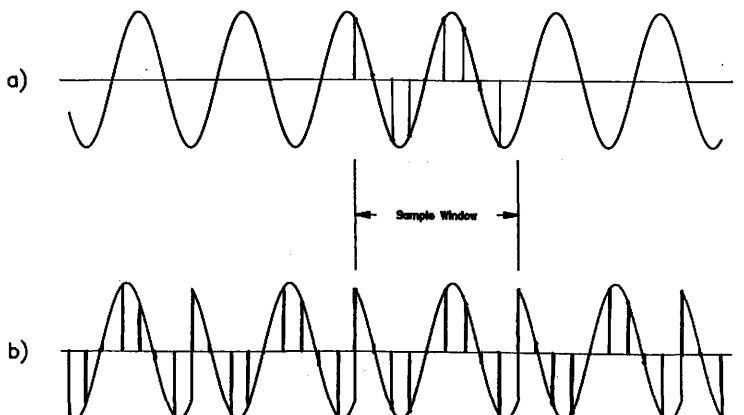


Figure 8 Time extention of a sampled signal
a) Original Signal
b) Time-extended signal

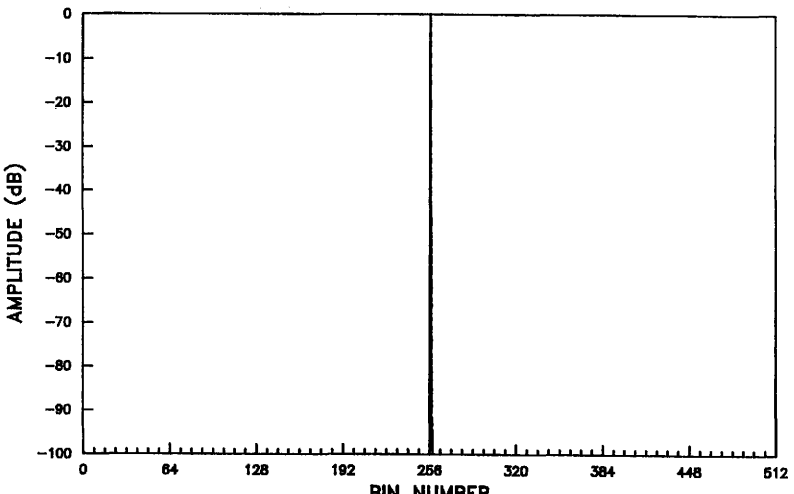


Figure 9 512−point CZT of a Signal in Bin 255.0 (Rectangular Window)

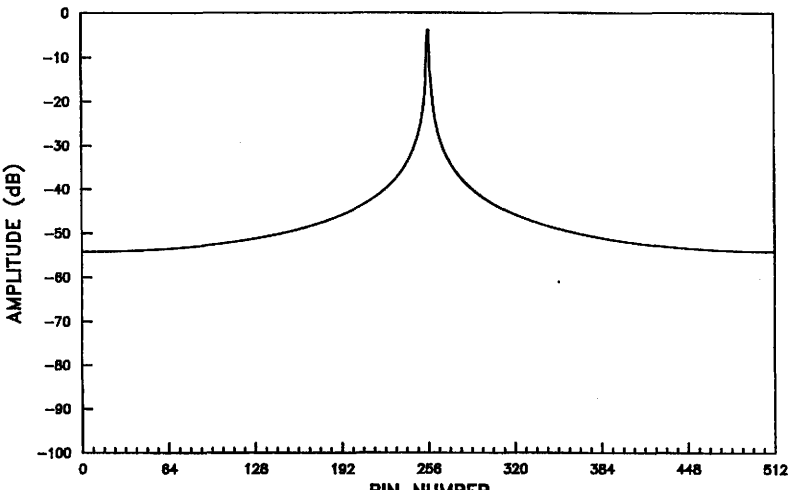


Figure 10 512-point CZT of a Signal in Bin 255.5 (Rectangular Window)

will be reduced. This in turn will reduce the amount of "frequency leakage." If windowing is applied to the stationary chirp Z-transform, the resulting equation will be

$$F_k = e^{\frac{-j\pi k^2}{N}} \sum_{n=0}^{N-1} \left(f_n w_n e^{\frac{-j\pi n^2}{N}}\right) e^{\frac{j\pi(n-k)^2}{N}} \qquad k = 0,1,2,\ldots N-1. \qquad (2.11)$$

For the sliding chirp Z-transform, the resulting equation will be

$$F_k = e^{\frac{-j\pi k^2}{N}} \sum_{n=k}^{N-1} \left(f_n e^{\frac{-j\pi n^2}{N}}\right) w_{n-k} e^{\frac{j\pi(n-k)^2}{N}} \qquad k = 0,1,2,\ldots N-1. \qquad (2.12)$$

Note that windowing for the stationary transform is performed during pre-multiplication while windowing for the sliding transform is performed in the convolution operation. The window must slide with the data in the sliding transform. In both these cases, the window sequence selected has a major effect on the best realizable resolution and dynamic range which can be obtained.

Many different windowing functions have been proposed. Harris [11] has researched the effects of windowing functions on the discrete Fourier transform. Because the discrete Fourier transform and chirp Z-transform are mathematically equivalent, Harris' work carries over to the CZT. Harris examined a variety of different windows and several figures of merit for evaluating and comparing them. Two figures of merit which seem to closely estimate worst case dynamic range and spectral resolution are maximum side-lobe level and 6dB bandwidth, respectively. Using these figures of merit it can be seen that the rectangular window has excellent resolution but poor dynamic range.

The Hanning window has significantly better dyanmic range at the loss of some resolution. The Dolph-Chebyshev window has both better dynamic range and better resolution than the Hanning window. Of all the windows surveyed by Harris, the Dolph-Chebyshev has the best overall performance; however, it is rarely used because of its significant mathematical complexity.

Both systems presented in this report can use either the rectangular window or the Hanning window. For the sliding chirp Z-transform, the windowing function must be placed within the transversal filter. The rectangular and Hanning windows are the only windows available in a charge-coupled device transversal filter. The spectral characteristics of the rectangular window have just been presented in Figures 9 and 10. Figures 11 and 12 present the same characteristics for the Hanning window. The Hanning window exhibits a much lower amount of "frequency leakage" than the rectangular window; however, the wider central lobe produces a poorer spectral resolution.

C. Implementing the Chirp Z-transform in Hardware

Although the chirp Z-transform appears to be much more complex than the discrete Fourier transform, it is actually much simpler to implement in hardware. This is because the convolution process in the chirp Z-transform is easily implemented using a transversal filter, and both pre-multiplication and post-multiplication can be implemented using a multiplying digital-to-analog converter. The discrete Fourier transform however, has no simple implementation in hardware and must therefore be computed using a digital computer. In many applications the cost and size limitations of such a computer can prove extremely

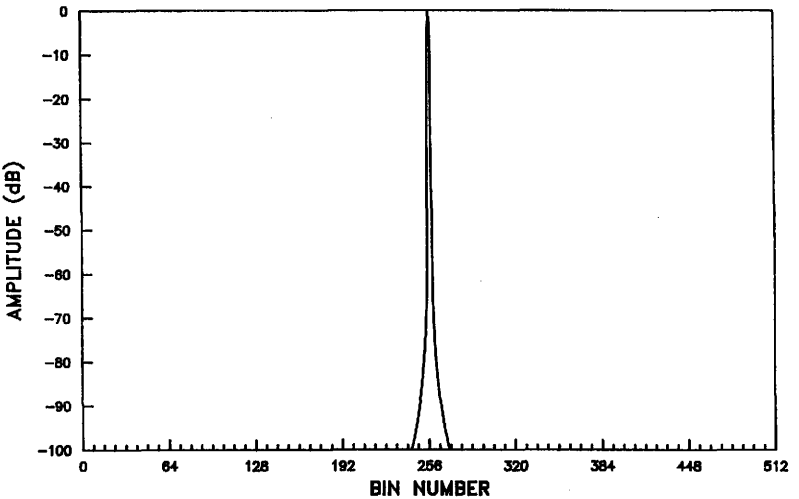


Figure 11 512−point CZT of a Signal in Bin 255.0 (Hanning Window)

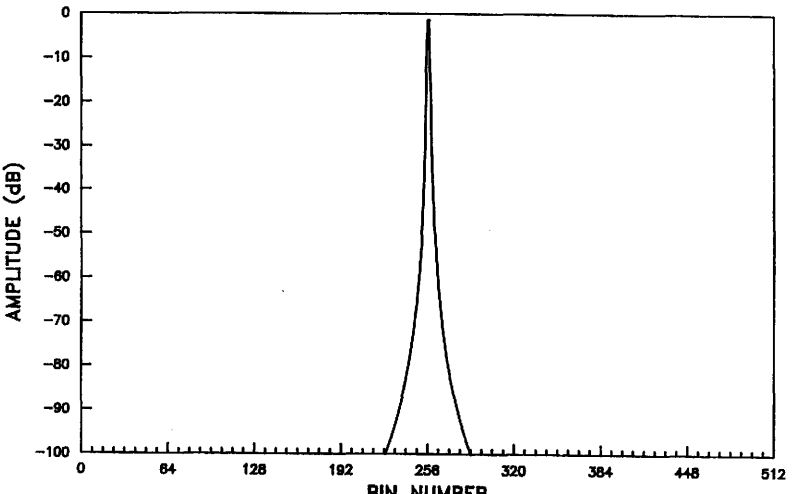


Figure 12 512-point CZT of a Signal in Bin 255.5 (Hanning Window)

prohibitive. This is especially true for large bandwidth signals, and thus high system sample rates.

A block diagram showing the hardware implementation of the chirp Z-transform is presented in Figure 13. This diagram shows that the implementation is composed of three operations: pre-multiplication, convolution, and post-multiplication. In the following discussion on the implementation of the chirp Z-transform, each of the three operations will be discussed separately.

1) Pre-multiplication: The pre-multiplication operation required in computing the CZT is easily implemented in hardware. Figure 14 shows an implementation which uses a multiplying digital-to-analog converter, a read-only memory, and a digital counter. The read-only-memory contains the sampled down-chirp required for pre-multiplication. These sampled values are addressed by the digital counter and supplied to the multiplying digital-to-analog converter which then multiplies them by the input sequence to produce a pre-multiplied output sequence.

2) Convolution: The convolution operation can be implemented in hardware using a transversal filter. A transversal filter is essentially a long series of delay elements whose outputs (called taps or bins) are individually weighted and summed to produce an output. Figure 15 illustrates the block diagram of a transversal filter.

The convolution differs slightly depending on whether the stationary or sliding chirp Z-transform is being computed. The difference is the data window over which the convolution is taken. For the stationary transform, this window is stationary and thus the equa-

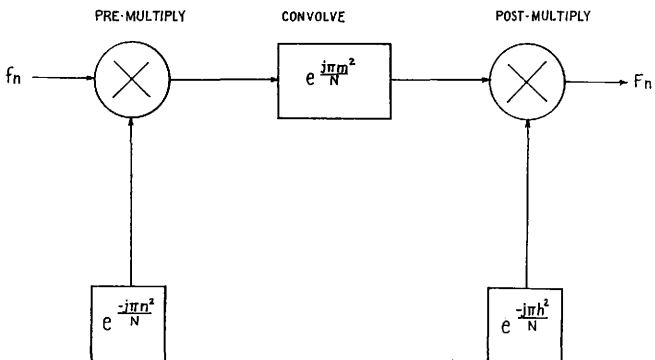


Figure 13 - Chirp Z-Transform Block Diagram

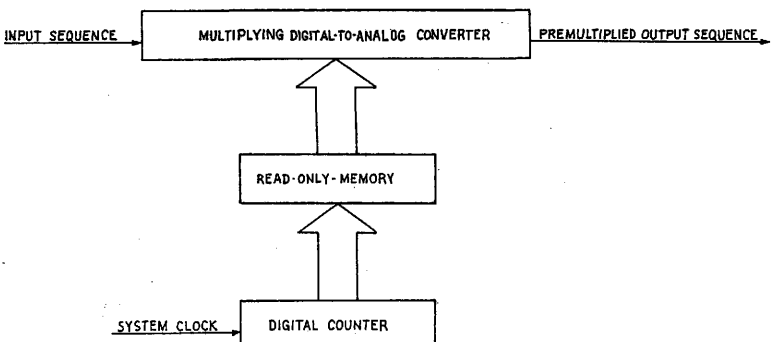


Figure 14 - Pre-multiplier

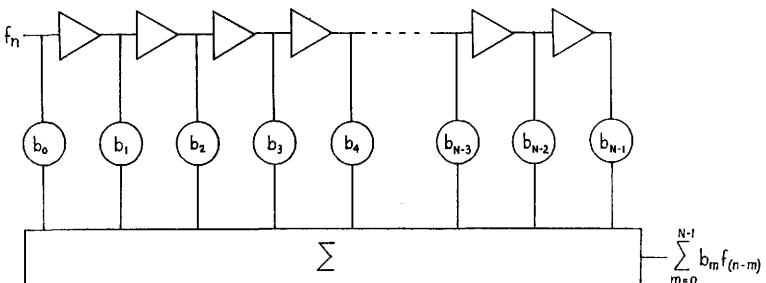


Figure 15 - Transversal Filter Block Diagram

tion for the convolution is

$$\sum_{m=0}^{N-1} g_m e^{\frac{j\pi(m-k)^2}{N}} \quad . \tag{2.13}$$

The sequence $\{g_m\}$ is the output sequence of the pre-multiplier. For the sliding transform, the data window slides. The equation for performing a sliding convolution is

$$\sum_{m=k}^{k+N-1} g_m e^{\frac{j\pi(m-k)^2}{N}} \quad . \tag{2.14}$$

Because of the different nature of the two convolutions, the implementation of each will be presented separately.

a) Stationary convolution: Two techniques exist for using a transversal filter to implement convolution required for the stationary chirp Z-transform. The first technique requires a transversal filter of length 2N where N is the length of the transform. The tap weights of the filter are two cycles of an up-chirp. A block diagram of such a transversal filter is shown in Figure 16. The transversal filter is first assumed to be initially filled with zeros. A single record of data is then loaded serially into the lower N bins of the transversal filter (the output is ignored during this time) to produce the configuration shown in Figure 17a. At this time the output of the transversal filter is

$$b_o = \sum_{m=0}^{N-1} g_m e^{\frac{j\pi m^2}{N}} \quad . \tag{2.15}$$

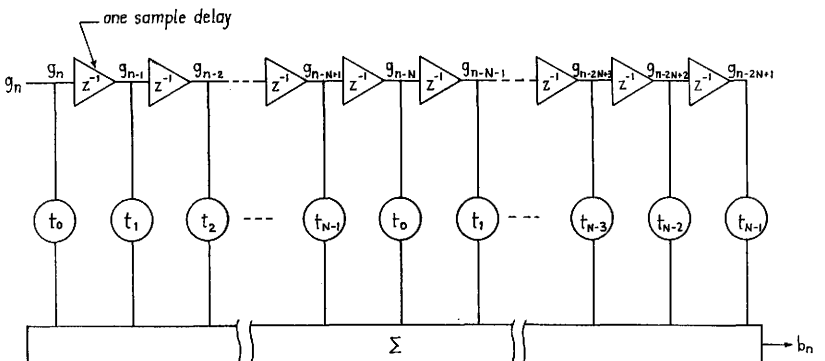


Figure 16 - Delay Line Implementation of Transversal Filter

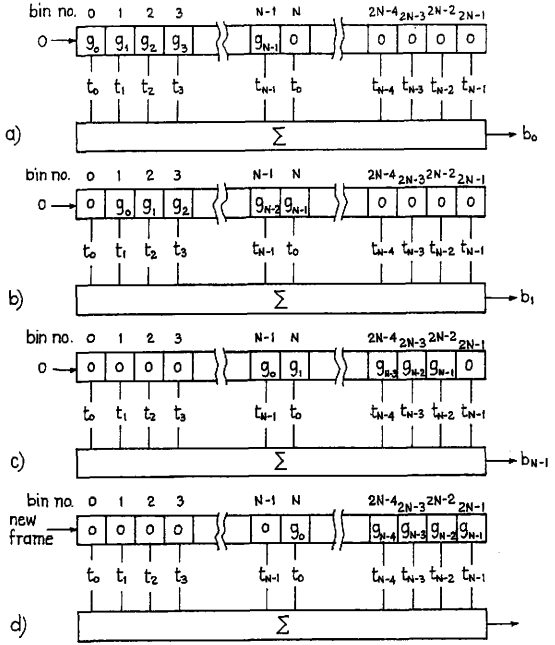


Figure 17 - Shifting-In-Zero's Technique for Performing a Stationary Convolution

This is the first term of the convolution expressed in equation 2.13. Likewise, every time a zero is shifted into the transversal filter, the resulting output will be the next sequential term of the convolution. Thus by shifting in N-1 zeros the N terms of the convolution are obtained. Figure 17 illustrates this sequence ending at Figure 17d when the Nth zero is shifted in. If the next data record is then shifted into the lower N bins of the transversal filter, the configuration shown in Figure 17a is obtained and the sequence has been brought full-circle. There are two disadvantages with this technique. The first is that 2N clock cycles are required to produce N outputs. The second is that a transversal filter of length 2N is required to compute a transform of length N. Thus, the technique works, but is inefficient.

The second technique for implementing a stationary convolution using a transversal filter is more efficient than the first. This technique can be developed by imagining the transversal filter shown in Figure 16 as being composed of two identical transversal filters of length N connected end-to-end. The output b_n is thus the sum of the outputs of the two shorter transversal filters. Because these two filters have identical tap wieghts, it is possible to combine them into a single transversal filter whose data is the sum of the data in the two original transversal filters. It is important to note that whenever a bin in the first transversal filter contains non-zero data, the data in the same bin in the second transversal filter is always zero, and vice versa. Because of this, a stationary convolution can be implemented using a transversal filter of length N as follows. The

filter is first loaded serially with a single data record (b_k is ignored during this time) to produce the configuration shown in Figure 18a. The output of the filter is now b_0 as in the other technique. Instead of now shifting in zeros, the data within the filter is rotated. The first of these rotations is shown in Figure 18b and produces the second convolutional output b_1. By rotating the data N-1 times, the N terms of the convolution are produced. At this point the Nth rotate is performed to ready the filter for re-loading. This technique is more efficient than the previous technique since it requires a transversal filter of length N as opposed to 2N; however, it is still inefficient because it requires 2N clock cyles (N cycles to load the filter and N cycles to compute the convolution) to produce N outputs. If it is necessary to overcome this inefficiency two of these filters can be placed in parallel so that one is loading while the other is computing and vice versa.

b) Sliding convolution: The convolution required for computing the sliding chirp Z-transform is much easier to implement using a transversal filter. This is because the data window over which the convolution is taken is continuously "sliding" in time. This "sliding" eliminates the need for pre-loading the transversal with data before the convolution can be computed. Because no pre-loading is required, a N point sliding convolution can be computed using a transversal filter in N clock cycles.

A technique which efficiently implements the sliding convolution uses a transversal filter of length N. The tap weights of this filter are one cycle of an up-chirp. If data is continuously fed into this

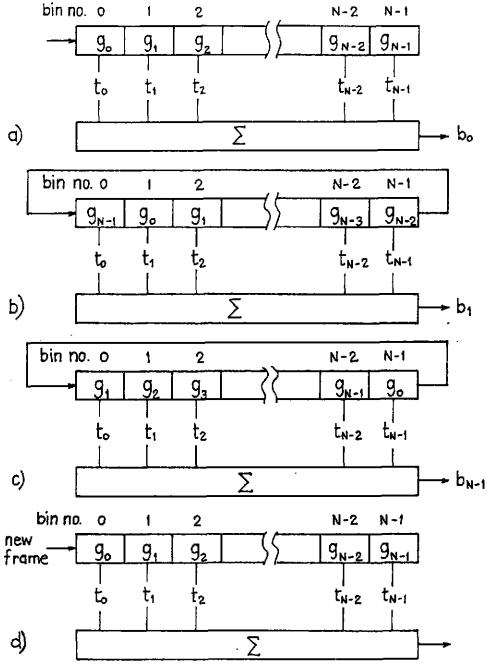


Figure 18 - Rotation Technique for Performing a Stationary Convolution

transversal filter the output will be

$$b_k = \sum_{m=k}^{k+N-1} g_m e^{-j\pi \frac{(m-k)^2}{N}} . \qquad (2.16)$$

This is the equation for the sliding convolution as expressed in equation 2.14. This is the technique used in both systems presented in this report.

c) Implementing a transversal filter: The above techniques all use a transversal filter to implement a convolution in hardware. One item that was not presented, however, was how to implement a transversal filter.

In order to implement a transversal filter in hardware, it is necessary to develop a delay line whose contents can be nondestructively sampled, multiplied by a constant, and then summed. This structure is presented in Figure 16. One technique for doing this employs a charge coupled device. Both systems presented in this report use this technique.

A charge coupled device is effectively an analog shift register. Data is stored in the device in the form of small charge packets held in potential wells on the surface of a semiconductor. These charge packets are shifted through the device by moving the potential wells. The theory for such a device was presented by Boyle and Smith in 1970 [12]. Experimental verification of the principles were presented by Amelio, Tompsett, and Smith [13].

A cross-sectional diagram of a charge coupled device is shown in Figure 19. The metal gates are used to form the potential wells where the charge packets reside. Clocking these gates allows the wells to

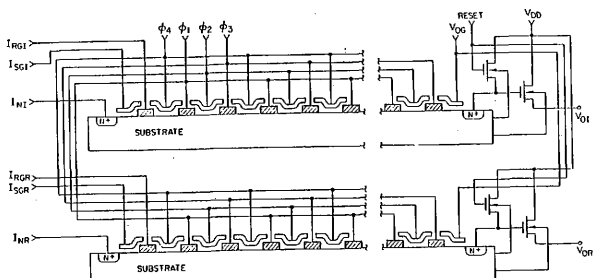


Figure 19 Cross-sectional Diagram of a CCD Transversal Filter

be moved along the length of the device. When these wells are moved, charge flows to the gates to offset the charge contained within the well beneath them. If the amount of charge flowing to the gate is measured, the amount of charge under the gate can be non-destructively sampled. If the gates are now split as shown in Figure 20, the sampled values can be weighted then summed. A charge coupled device can thus be used to implement a transversal filter. A detailed discussion on charge coupled devices and how they can be used to implement a transversal filter is presented in Appendix B.

3) Post-multiplication: The final operation performed in computing the chirp Z-transform is post-multiplication. This operation corrects the phase of the convolved output to produce the true spectral estimates $\{F_k\}$. Both systems presented in this report compute-power-spectral-density. Because power-spectral-density is phase independent, post-multiplication is not performed. In systems requiring phase information, post-multiplication operation, if needed, can be implemented using the same circuit used to perform the pre-multiplication operation. This circuit is shown in Figure 14.

D. Conclusion

The chirp Z-transform is a very efficient technique for computing the discrete Fourier transform. Because of its simplicity, the transform can be easily implemented in hardware using a CCD transversal filter. One very important consideration when using the transform is windowing. When the chirp Z-transform is used for spectral analysis, the windowing function chosen determines the best case spectral resolution and dynamic range of the system.

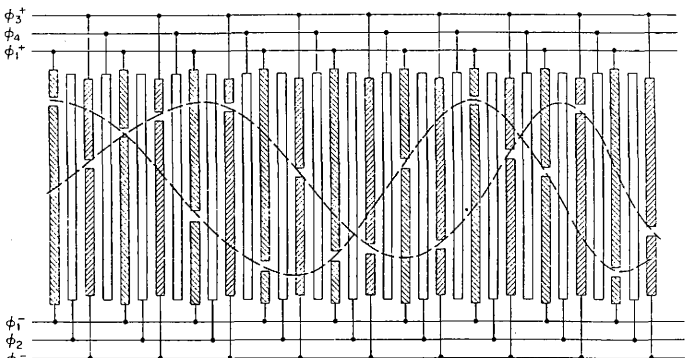


Figure 20 Gate Diagram of a CCD Transversal Filter

CHAPTER III

ANALYSIS OF THE CURRENT DESIGN

A. Introduction

The current spectral analysis system [10] was developed for the real-time processing of radar scatterometer data [10]. The design was developed under NASA Johnson Spacecraft Center contract number NAS9-15311. Because of its dedicated application the design has very little versatility, and because the design is the first of its kind, it has several drawbacks which merit its redesign.

This chapter presents a detailed analysis of the original design and clearly identifies the drawbacks that are to be corrected. To do this the original design is divided into blocks and evaluated in a block-by-block fashion. Discussion of the solution to the drawbacks is presented in to the next chapter.

B. Analysis of the Current System

A block diagram of the current spectral analysis system is shown in Figure 21. This diagram shows that the system can be broken down into nine major blocks. Of these nine blocks, two pair of blocks are identical. These are the two signal conditioners and the two input sample-and-holds. These blocks are used to prepare the input signal for spectral analysis as well as convert the continuous input f(t) to the sampled sequency {fn} required by the chirp Z-transform. Another block is the pre-multiplier. This block is used to perform the pre-multiplication operation discussed in Chapter II. Pre-multiplication is the first operation required in computing the chirp Z-transform.

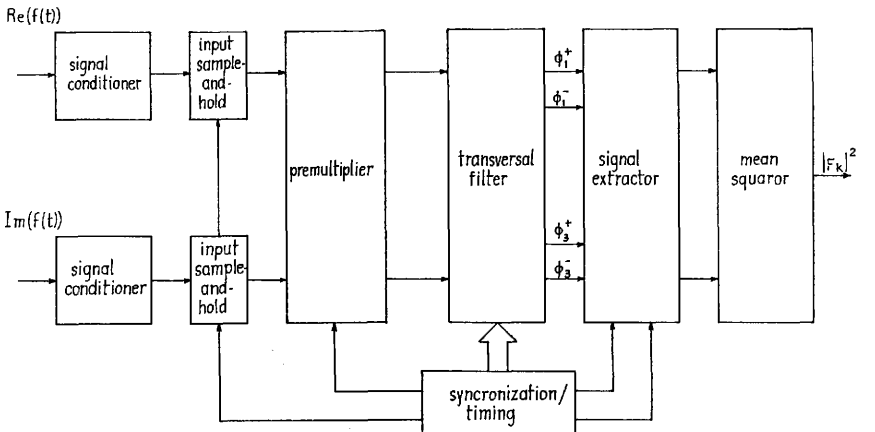


Figure 21 - Block Diagram of Current Design

The second operation required for computing the chirp Z-transform is convolution. The convolution operation is performed by the transversal filter and signal extractor blocks. Because the spectral analysis system computes power-spectral-density, the post-multiplication operation need not be performed. An explanation of why this is true was presented in Chapter II. The operation which is performed in place of post-multiplication is mean squaring. This operation computes power-spectral-density from the transveral filter. The ninth and final block is the synchronization/timing block. This block provides the other blocks with the clock signals they require. A detailed analysis of each of these blocks follows.

1) Signal conditioner: The signal conditioning block performs three important functions. These are: the elimination of the dc signal component, the prevention of aliasing, and the reduction of input noise. The means by which these functions are implemented however, produces some undesirable side effects.

The presence of a large dc component in the input signal can cause saturation of the transversal filter. This saturation occurs when the instantaneous input voltage rises above 2.0 volts or falls below -2.0 volts. To maintain maximum dynamic range, the input signal should make the best use of this voltage range as possible.

To eliminate the dc component, the signal conditioner has a first order high pass filter whose pole is at 28 Hz. The filter does eliminate the dc signal component, but also alters the spectral characteristics of the input signal. Thus, the output of the spectral analysis board will not be the true spectrum of the input signal, especially at low frequencies. This is very undesirable.

If the bandwidth of the input signal is too large aliasing will occur. Aliasing is described as follows. In a sample system, if the bandwidth of the input signal exceeds the sampling frequency, spectral components at frequencies greater than the sampling frequency become ambiguous with components just below the sampling frequency. This behavior is often described as a folding operation since frequencies that are higher than the sampling frequency appear to fold back on top of those that are lower. If aliasing occurs the output of the spectral analysis board will not be a true estimate of the spectrum of the incoming signal. The current spectral analysis board's sample rate is fixed at 9.0 KHz and thus the bandwidth of the signal must be less than 9.0 KHz to prevent aliasing. The current signal conditioner contains a two pole maximally flat Butterworth low pass filter which is used to prevent aliasing. The filter has an upper band edge at 5.9 KHz which limits the bandwidth of the signal exiting the signal conditioner to 11.8 KHz (i.e. a band from -5.9 KHz to 5.9 KHz). This filter is not narrow enough to prevent aliasing and does not allow analysis of signals which have a sufficiently small bandwidth but do not have a band center at dc. The filter also distorts the spectral characteristics of the signal being analyzed, especially at high frequencies. A side advantage of this filter is that it reduces the noise-bandwidth product of the input signal by reducing it's bandwidth.

Another problem which can be caused by the signal conditioner is called channel gain mismatch. This problem occurs when the gain through each of the two signal conditioners is not precisely matched.

To obtain the effect of this gain mismatch upon the system performance, it is possible to perform the analysis mathematically using the equation for the sliding discrete Fourier transform. It is by means of this transform that the system performs its spectral analysis. The equation for the discrete Fourier transform for an arbitrary complex input f_n is

$$F_k = \sum_{n=0}^{N-1} f_n e^{\frac{-2\pi jnk}{N}} \qquad k = 0, 1, 2, \ldots N-1. \tag{3.1}$$

If f_n is then broken into its real and imaginary parts, and a gain mismatch of value e is allowed in the imaginary channel, we obtain a new sequence

$$g_n = \mathrm{Re}(fn) + j(1+e)\mathrm{Im}(fn) = (1+\tfrac{e}{2})fn+(-\tfrac{e}{2})fn^*. \tag{3.2}$$

To find how the spectrum of this sequence is different from the previous spectrum F_k it is necessary to compute the discrete Fourier transform of the new sequence g_n. This is done as follows:

$$G_k = \sum_{n=0}^{N-1} g_n e^{\frac{-2\pi jnk}{N}} = \sum_{n=0}^{N-1} [(1+\tfrac{e}{2})fn+(-\tfrac{e}{2})fn^*]e^{\frac{-2\pi jnk}{N}}$$

$$= (1+\tfrac{e}{2})[\sum_{n=0}^{N-1} fne^{\frac{-2\pi jnk}{N}}]+(-\tfrac{e}{2})[\sum_{n=0}^{N-1} fne^{\frac{-2\pi jn(N-k)}{N}}]^*$$

$$= (1+\tfrac{e}{2})F_k+(-\tfrac{e}{2})F_{N-k}{}^*. \tag{3.3}$$

From this development it can be seen that G_k consists of two parts. The first part $(1 + e/2)F_k$, is the desired (signal) part. The second part, $(-e/2)F_{N-k}{}^*$, is the undesired (noise) part. From this a signal-to-noise ratio for noise caused by channel gain mismatch can be

calculated to be

$$SNR = \frac{\left|1+\frac{e}{2}\right|}{\left|\frac{-e}{2}\right|} = \left|1+\frac{2}{e}\right| \tag{3.4}$$

If the desired signal-to-noise ratio is known, then the allowable channel gain mismatch can be computed. For the case of a 60dB signal-to-noise ratio the allowable channel gain mismatch is 0.2%. This is far more accurate than the 5% accuracy of the components in the current signal conditioner.

2) Input sample-and-holds: The input sample and holds perform a rather simple but important function. They sample the continuous input signal f(t) to produce the sequence $\{f_n\}$ required for the computation of the chirp Z-transform. The sample-and-holds also hold the sampled value constant while supplying it to the pre-multiplier. This allows the pre-multiplier time to perform its function.

3) Pre-multiplier: A detailed block diagram of the pre-multiplier implemented in the current spectral analysis system is shown in Figure 22. Of the fourteen adjustment potentiometers twelve are contained in the pre-multiplier.

The main function of the pre-multiplier is to multiply the sampled input sequence by waveform linearly decreasing frequency ("down-chirp"). Because pre-multiplication involves complex quantities and because only real operations may be implemented in hardware, the complex pre-multiplication must be broken up into real operations as shown in Figure 23. In the current design the four real multipliers shown in Figure 23b are implemented using multiplying digital-to-analog converters (MDACs). An MDAC multiplies an incoming

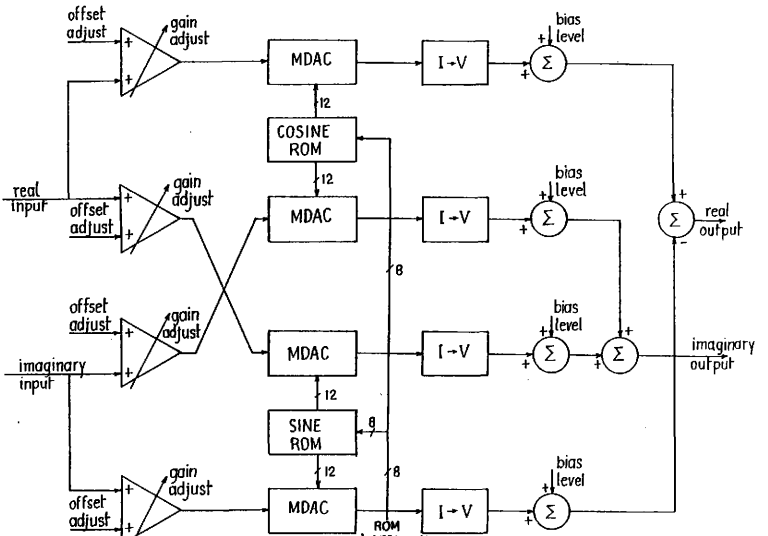


Figure 22 - Pre-Multiplier Block Diagram

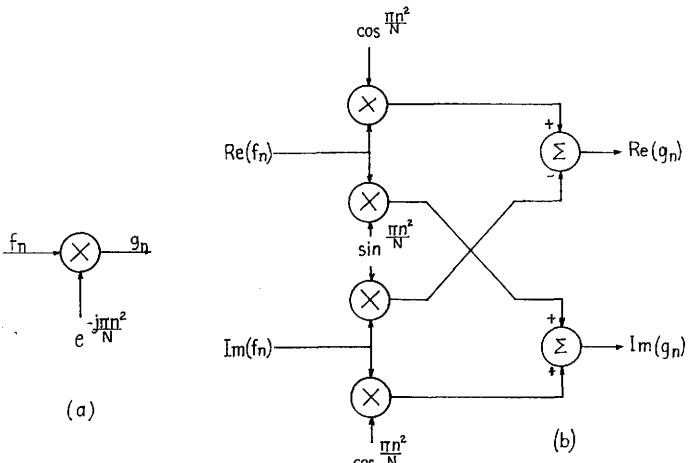


Figure 23 - Premultiplying by a down-chirp

(a) complex representation
(b) real implementation

analog signal by a digital quantity and provides the product in analog form. The output signal is a current rather than a voltage and must be converted to a voltage using a current to voltage converter.

One disadvantage of this technique is that when the "down-chirp" is expressed in digital form, quantization noise is produced by the coefficient inaccuracies. Assuming uniform quantization and a uniform distribution of the signal voltage, the quantization noise produced by an M bit MDAC will result in a signal-to-noise ratio of

$$SNR = 10_{log}(2^{2M}-1) \approx 6M \tag{3.5}$$

where SNR is in dB. For the MDACs used in the current design M=12. Thus these converters will produce a signal-to-noise ratio of 72 dB. This is sufficient because other noise sources will be much larger.

Another source of noise is the channel gain mismatch. This noise source was explained earlier in the discussion of the signal conditioners. In order to reduce this mismatch, variable gain amplifiers are included in front of the MDACs to allow matching of the channel gains. These amplifiers have adjustments to allow for the elimination of any dc offsets introduced by themselves or any previous element. Each of the four amplifiers possesses two adjustment potentiometers, for a total of eight adjustments. These adjustments must be reduced if not eliminated for the system to be practical.

A final requirement for the pre-multiplier is that its output must ride on a nominal 6V dc bias to meet the input requirements of the R5601 transversal filter. The dc bias level is provided by four adjustment potentiometers. These potentiometers also need to be

eliminated to produce a practical system. The above problems dictate the redesign of the pre-multiplier.

4) Transversal filter: The transversal filter block of the spectral analysis system performs the convolution required to compute the chirp Z-transform. This is done using the Reticon R5601 quad chirped transversal filter. The R5601 contains two 512 element charge coupled delay lines. Split electrode weighting is employed in the implementation of the transversal filter. The means by which this is done is described in Appendix B.

One major drawback of the R5601 is its lack of consistent documentation. Documentation on the R5601 consists of three items. These are the R5601 preliminary data sheet and two Reticon reports on spectral analysis boards which employ the filter in their design. Neither of the Reticon designs employ the R5601 in a manner which is consistent with the preliminary data sheet. The current spectral analysis system uses the same bias voltages, clock timing, and clock levels as the first of the two Reticon designs even though in some cases they are not consistent with the preliminary data sheet. This was done because the first Reticon design is that of the RC5601 spectral estimation board. This board is currently available from Reticon, and though it has some problems it has proven functional. The second design was never placed into production and thus possesses some uncertainty as to its functionality. The problem with the use of a previous design to specify bias voltages, clock timing and clock levels is that it is not known whether they produce optimal performance.

Another part of the transversal filter block is the clock drivers. These clock drivers convert the TTL level signals from the synchronization/timing block to the levels needed by the R5601. The drivers used are National DS0026 MOS clock drivers. These drivers meet all the requirements of the R5601 except that they do not provide a low level output voltage which is less than 0.4 volts. They provide a guaranteed low of only 1.0 volt. This higher level will produce an increase in the charge transfer error within the R5601.

5) Signal extractor: The purpose of the signal extractor is to convert the outputs of the CCD transversal filter to a voltage. Figure 24 shows the block diagram for the signal extractor. This diagram shows that the signal extractor is composed of two major parts: the differential current integrator (DCI) and the dc stabilizer. Three sample-and-holds are included in the signal extractor to bring the real and imaginary outputs into time synchronization.

a) Differential current integrator: The output of the CCD transversal filter is in the form of charge transferred along the major-phase clock lines. The real output is extracted by measuring the difference in charge flowing along the ϕ_1^+ and ϕ_1^- clock lines. The imaginary output is extracted by performing the same operation on the ϕ_3 clock lines. This task is accomplished by the differential current integrator. A schematic diagram of the differential current integrator used in the current spectral analysis system is shown in Figure 25. This circuit integrates the differential current (Q^+-Q^-) over the time when ϕ_R is low (switches open). To achieve this result two timing conditions must be met. First, ϕ must be low when ϕ_R is high. This is so that capacitors C^+, and C^-, are initially

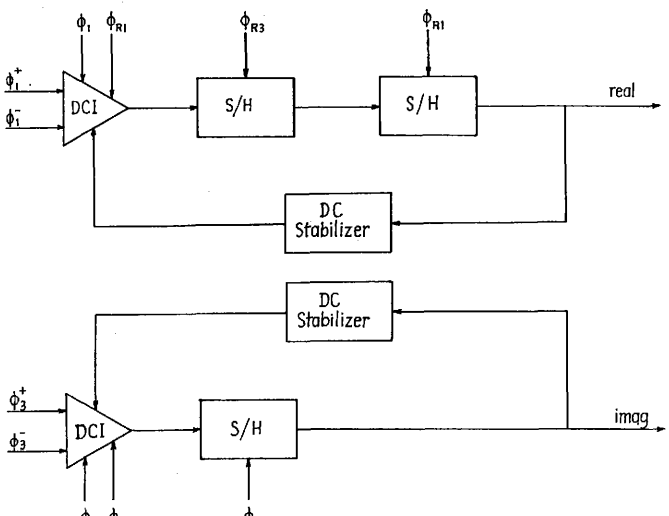


Figure 24 - Signal Extractor Block Diagram

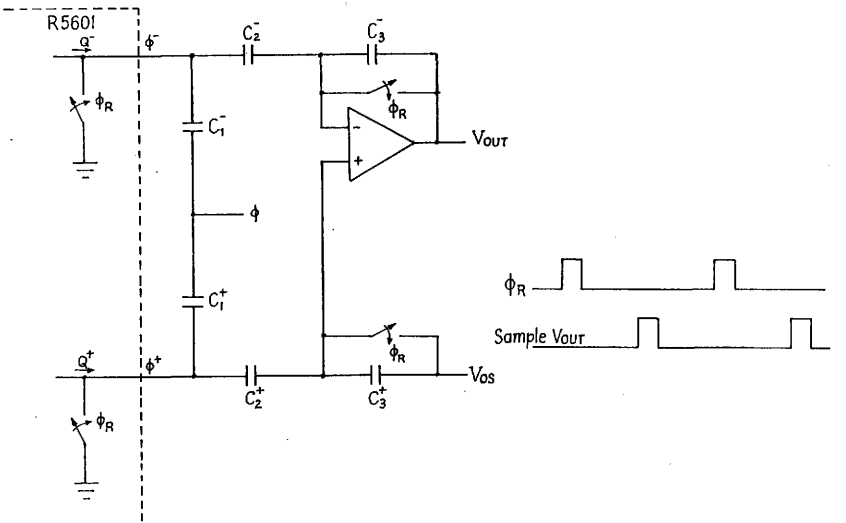


Figure 25 - Differential Current Integrator

discharged. Second, ϕ must remain high until the output is sampled. Both of these conditions are met by the clock timing shown in Figure 25. The requirement that V_{out} be sampled as shown in Figure 25 is achieved by the sample-and-holds shown in Figure 24 which immediately follow the differential current integrators. The third sample-and-hold is included to bring the two voltage outputs into time synchronization.

Another condition which must be met to insure the proper function of the differential current integrator is the matching of capacitors. The capacitor pairs C^+_1, C^-_1; C^+_2, C^-_2; and C^+_3, C^-_3 should be matched to at least 1% and preferably to 0.1%. This matching achieves two objectives. The first is to insure that ϕ^+ and ϕ^- obtain the same clock waveforms. This is essential to the function of the split-gate weighting technique used in the CCD transversal filter. The second is to insure a high common mode rejection ratio. This is very important because the magnitude of Q^+ and Q^- can be much much larger than their difference. The signal V_{DS} shown in Figure 25 is directly summed by the circuit into V_{out}. This input is used for the dc stabilization feedback loop shown in Figure 24.

b) DC stabilizer: The purpose of the dc stabilization loop is to eliminate the dc bias level within the output signal of the CCD transversal filter. This bias was introduced by the pre-multiplier to satisfy the input requirements of the CCD device. In order to eliminate the bias level, however, it is necessary to develop a criterion which identifies its presence. The criterion used by the current design relies on the assumption that the input signal to the spectral

analysis system contains only spectral components which are asynchronous to the system clock rate to assure that the phase of the output spectrum will be random. This is generally true for all the spectral components except the dc component which always has constant phase. The dc was supposedly eliminated by the input signal conditioner and should therefore not be present in the output spectrum. Because of the random phase of the output spectrum and the absence of a dc spectral component, if all the complex spectral estimates are averaged together over several records, the result should be ideally zero. If a bias level is present the bias level will be the average. Using this technique, the dc stabilizer consists of a lossy integrator with a relatively long time constant and a negative gain. This is the technique used in the current design.

Several problems exist with the dc stabilizer as it is currently implemented. The first problem is that the circuit contains a potentiometer which sets the initial dc feedback level. This initial feedback level gives the stabilizer a starting point close to the level desired. The second problem with the current dc stabilization loop is that the time constant is much too short, is approximately one record in length. This means that the stabilizer makes its estimate on only a single record where the theory requires several. A third problem with the current dc stabilizer is that it allows the dc level which is fed back to the differential current integrator to change during the processing of a record. This tends to distort the spectrum and can produce generally more undesirable effects than does the bias level it is trying to eliminate.

6) Synchronization/timing: The purpose of the synchronization/timing block is to provide clock signals to the various other blocks. The current system uses a 64 state digital counter driven by a fixed 576 KHz clock. The output of the counter is then used to address the contents of a read-only memory. The outputs of the memory are then used as control lines to provide the clock signals needed by the other system blocks. Two major problems exist with the current design of the synchronization/timing block. The first is that the clock rate is fixed with no way of changing it. This extremely limits the versatility of the system. The second is that the clock rate chosen produces a rather inconvenient 17.578 Hz spacing between spectral estimates. This unusual number makes computation of the center frequency of each spectral estimate rather difficult.

7) Mean squaror: The mean squaring operation is used to compute the complex magnitude of the spectral estimates. In the current design the mean squaring operation is performed digitally. This design consists of two analog-to-digital converters along with two combinational multipliers to perform the squaring operation. The advantage of this technique is that it is very accurate. The disadvantage is that it is very costly and consumes a large amount of power. Other means of performing this function would be worth investigating.

C. Circuit Layout and Construction

One major problem in the physical layout and construction of the current circuit board which causes a significant lowering of the signal-to-noise ratio of the system is the fact that the board interconnection is done using wire-wrap. The wire-wrap posts and wires serve very effectively as antennas to pick up noise from the

high frequency digital signals from the on-board logic as well as from other local boards.

A second problem involves the routing of the low level analog signals over wires containing digital signals. This happens on several occasions. The input signal first enters the board from the top connector to proceed to the left edge of the board passing across the read-only memories containing the pre-chirp signals as well as across the multiplying digital-to-analog converters. After passing these chips the signal then crosses them again to enter the pre-multiplier, picking up more noise along the way. After pre-multiplication the signal proceeds to cross the clock drivers picking up one last dose of noise before entering the R5601. Upon exiting the R5601 the signal is in the form of very low level charge packets. Because of the low level the wire lengths should be very short between the R5601 and the signal extractor. This is not the case of the current design.

A third problem with the construction of the current spectral analysis board has to do with the mean by which the components are mounted to the board. In most cases the problem is not major; however, in the case of certain capacitors which must be very accurately matched, the contact capacitance of the socket pins can produce an error as high as 3pF. For the capacitors in the signal extractor this can produce an error of from one to ten percent depending on the size of the capacitor. This is unacceptable since capacitors within the signal extractor should be matched to better than one percent.

D. Conclusion

Several drawbacks and problems exist with the current spectral analysis system. These deficiencies are caused by problems both with the design and with the means by which the design is implemented. They limit the performance as well as versatility of the system. The next chapter proposes a refined design to solve these problems.

CHAPTER IV

PRESENTATION OF THE REVISED DESIGN

A. Introduction

The revised spectral analysis system proposed in this chapter is presented as a solution to the problems of the current design. The system was designed to exhibit better performance characteristics as well as greater versatility than the current design. In several cases more than one solution is proposed. In these cases no clear-cut best solution to the problem exists, but rather the quality of the different solutions depends on the specific application for which the system is to be used. In order to present the design in an organized manner a block diagram of the revised system is presented and the design is discussed in a block-by-block manner.

B. Description of the Revised System

The block diagram of the revised spectral analysis system is shown in Figure 26. This block diagram is very similar to that of the current system shown in Figure 21. The diagrams are different, however, in that the revised system produces the spectral output in dB as well as magnitude. Also the signal conditioner and sample-and-hold blocks of the current system have been combined to form the input conditioner block of the revised system.

The addition of an output in dB was made for two reasons. The first reason is that the dB output is capable of maintaining a much larger dynamic range than the magnitude output of the current system when the signal is assaulted by low level noise. This noise is usually encountered when the output of the spectral analysis system is

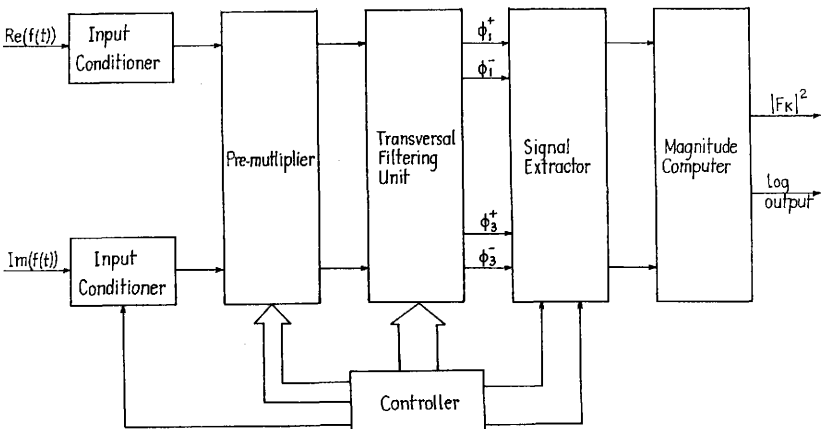


Figure 26 - Revised System Block Diagram

connected to the device or system desiring its output. The second reason for the addition of an output in dB is that in many applications this is a much more desirable form for the output. Conversion to this form can be a very difficult task when done in software.

The combination of the signal conditioner and sample-and-hold blocks into a single input conditioner block was done in order to allow more flexibility in the design of this block. The use of switching techniques allows both of these functions to be performed together within a single block.

1) Input conditioner: The signal conditioning block of the current system performs two major functions. These functions are elimination of the dc signal component and prevention of aliasing. The input conditioner replaces the signal conditioner and sample-and-hold blocks of the current design. It performs both the dc elimination and sample-and-hold functions of the two blocks it replaces, but does not contain an anti-aliasing filter.

a) Anti-aliasing filter: Three major reasons exist for not including an anti-aliasing filter in the current spectral analysis system. These reasons are:

1. the filter reduces system versatility
2. the filter increases channel gain mismatch
3. the filter is very difficult to implement over a wide range of system clock rates.

Because of these reasons an anti-aliasing filter was not included in the revised system. Thus it is the user's responsibility to assure that aliasing does not occur. This is done by limiting the bandwidth

of the input signal to less than or equal to the system clock rate.

The purpose of an anti-aliasing filter is to restrict the bandwidth of the incoming signal so that aliasing does not occur. A filter cannot, however, simply limit the bandwidth of a signal. It must instead restrict the frequency band within which the signal resides. In many cases requiring spectral analysis this can be very restrictive. To allow maximum versatility the restriction of the bandwidth of the input signal must be left to the system user.

As mentioned in the previous chapter, channel gain mismatch can significantly limit the signal-to-noise ratio of the spectral analysis system. Any filtering occuring in both input channels of the spectral analysis system must thus be very accurately matched to insure a good signal-to-noise ratio. This can be very difficult if not impossible to achieve over entire input frequency range especially to a 0.1% tolerance needed for a 60 dB signal-to-noise ratio.

Because the bandwidth to which the input signal is equal to the system clock rate, the bandwidth of the filter must change as the frequency of the system clock changes. The only type of filter capable of performing such a task is a switched capacitor filter. Implementing such a filter to cover the full range of system clock rates from 2 KHz to 200 KHz would be a major task in and of itself. One reason for this is that the filter itself requires an anti-aliasing filter which must be fixed at 200 KHz. Because of these reasons an anti-aliasing filter was not included in the revised system.

b) Sample-and-hold with dc filter: The input conditioner of the revised spectral analysis system performs two major functions.

These functions are: the removal of the dc component from the input signal and the conversion of the input signal to a uniformly sampled sequence.

The dc filtering and sample-and-hold operations are performed in a unique manner. In the current design these functions are performed in separate circuits. In the new design they are performed by a single circuit. A detailed block diagram of the circuit is shown in Figure 27. This design has several advantages over the design of the current signal conditioner.

The first of these advantages is that the new design does not degrade the spectral content of the input signal. In the current signal conditioner distortion is introduced by high-pass and low-pass filtering. These filters were included to perform dc filtering and anti-aliasing. The revised design remains direct-coupled during the processing of a record of spectral estimates and thus does not alter the spectral content of the signal. This is because the "set" signal shown in Figure 27 only occurs between records.

The second advantage of the revised design is that it allows less channel gain mismatch. This is because the gain through the device is only dependent on the gains of the two amplifiers. These gains can be very accurately controlled in the two channels. This was not the case of the current design where the gain was dependent on capacitor values within the two filters. Capacitors are difficult to obtain at the required 0.1% tolerance.

The implementation of the circuit shown in Figure 27 was done using a Signetics SD5000 D-MOS FET quad analog switch array and four Harris HA5105 operational amplifiers. A schematic showing the circuit

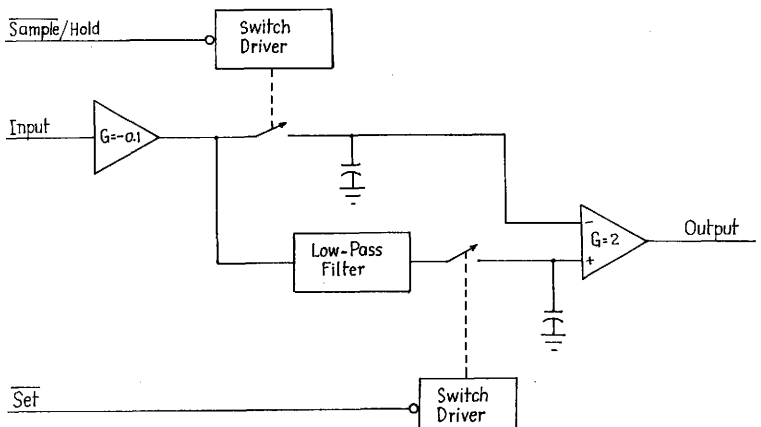


Figure 27 - Detailed Block Diagram for the Input Conditioner

implementation is shown in Figure 28. Two of the FET's in the switch array were used as switches while the other two were used as drivers. These switches were chosen primarily for their fast switching times and high breakdown voltages. The Harris operational amplifiers were chosen for their low input offset voltage and high slew rate. Two of the capacitors within the circuit must be silver-mica because of the potentially high switching rates. The six resistors noted should be of 0.1% tolerance to reduce channel gain mismatch problems. The circuit is designed with a gain of 0.2 so that a 20V peak-to-peak input signal will produce the 4V peak-to-peak signal desired by the pre-multiplier. The circuit is also designed to eliminate input dc signal components of up to 100V in magnitude. The two logic signal "sample/hold" and "set" to TTL level signals.

2) Pre-multiplier: The purpose of the pre-multiplier is to multiply the input signal by a complex down-chirp. This multiplication is the first step required for computing the chirp Z-transform. Unlike the current design, the pre-multiplier of the revised design does not contain a biasing or gain/offset adjustment stage. The biasing has been removed from the pre-multiplier block and placed in the transversal filter block. This was done because it is more easily and accurately done there than in the pre-multiplier. The gain/offset adjustment stage has been removed from the system because it is no longer needed. The elimination of these adjustments was accomplished by using precision components to match gain values and operational amplifiers with very low input offset voltages.

There is another difference between the pre-multiplier of the revised design and that of the current design. This difference is

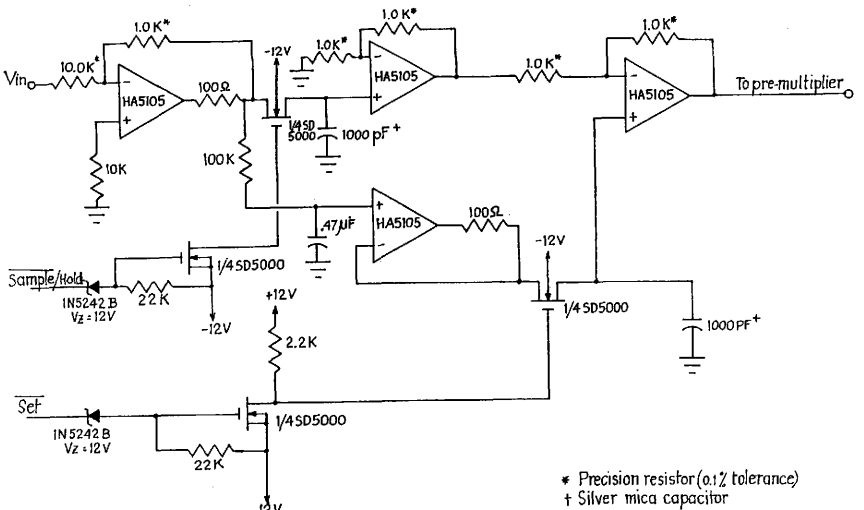


Figure 28 - Schematic for the Input Conditioner (Sample-and-Hold with DC Filter)

that the complex down-chirp is generated in the controller block. This is done for two reasons. First, it is done because the circuit which is used to produce the down-chirp also produces several signals required by the controller. The second reason is to reduce noise. This is based on the fact that the controller block will reside on a separate circuit board. This is done to try to separate the noise producing digital circuitry from the highly noise susceptible analog circuitry.

The schematic for the pre-multiplier is shown in Figure 29. Four multiplying digital-to-analog converters are used to calculate the four cross terms of the complex multiplication. These converters, Datel HA10BC's, can be clocked at speeds of over 700 KHz. They have less precision than the converters of the previous design, but this loss of precision produces no loss in performance. This is because the converters of the current design were more accurate than was necessary. The outputs of the multiplying digital-to-analog converters are in the form of current and must be converted to voltages. These voltage outputs are then combined to form the real and imaginary pre-chirped sequences. These are the input signals required by the transversal filter block. To reduce channel gain mismatch the resistors in the pre-multiplier block must be matched to 0.1% tolerance.

3) Transversal filtering unit: The transversal filtering unit of the revised system is composed of two major sections. These sections are the transversal filter, and its clock drivers. The clock drivers have been included within the transversal filter block because of their close association with the filter.

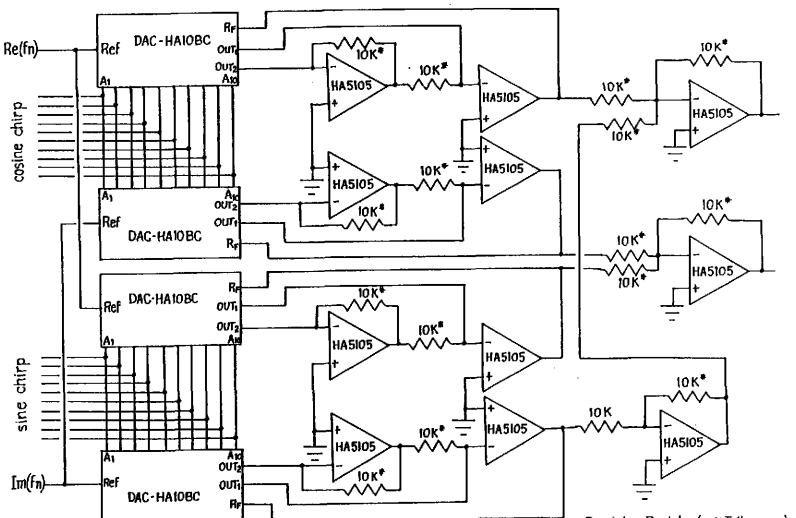


Figure 29 - Schematic for the Pre-Multiplier

a) Transversal filter: The transversal filter used in the revised system is the Reticon R5601. The R5601 is the same filter used in the current design. It is a 512 stage charge coupled device. The device uses split gate weighting to perform the transversal filtering. A more detailed description of how a charge coupled device can be used to implement a transversal filter is included in Appendix B.

Two versions of the R5601 quad chirped transversal filter are currently available. These are the R5601-1 and the R5601-2. They differ in two respects. The first difference is in the window function used. For the R5601-1 a rectangular window is used. This produces the finest possible resolution, but the highest sidelobes and thus the lowest dynamic range. The R5601-2 uses a Hanning window. This lowers the sidelobe levels; however, it also decreases the system's spectral resolution. A more detailed description of windows and their effect on system performance is included in Appendix A. A second difference between the two versions of the R5601 has to do with form of the "up-chirp" contained within the device. In the R5601-1 the "up-chirp" is of the form

$$\text{"up-chirp"} = e^{\frac{-j\pi n^2}{512}} \qquad n=0,1,2,\ldots 511 \qquad (4.1)$$

where n is the tap (or bin) number. In the R5601-2 the "up-chirp" is changed in phase and is of the form

$$\text{"up-chirp"} = e^{\frac{-j\pi(n-256)^2}{512}} \qquad n=0,1,2,\ldots 511 \qquad (4.2)$$

The effect of this phase change on the spectral analysis system is the re-ordering of the output spectral estimates. When the R5601-1 is used in the system the first output is the dc estimate. When the R5601-2 is placed in the system this dc estimate will be the 257th output. If desired, this effect can be countered by altering the pre-chirp waveform with the same phase shift. This is easily done since the pre-chirp waveform is contained in a read-only memory.

i) Biasing: As mentioned previously, the input signal of a CCD device must always be positive. The signal output of the pre-multiplier ranges between +2 volts and -2 volts. To shift this signal to a positive level, a dc bias of at least 2 volts must be introduced. Usually the bias level is larger. The larger bias level reduces the amount of charge transfer loss within the CCD device.

In the current spectral analysis system the required bias level was introduced in the pre-multiplier. This bias level was variable and could be adjusted using four potentiometers. In the revised system the bias level is introduced at the transversal filter. This bias level is fixed at six volts thus eliminating the need for the four adjustment potentiometers. The means by which the bias level is introduced is rather unique. Instead of raising the signal level above ground, the transversal filter is lowered below ground. The bias level required is in reference to the common pin of the CCD device. By placing this common pin at -5V an effective bias level of six volts is introduced. This technique also has the added advantage of reducing the voltages required for the clock levels.

ii) Clock and bias voltages levels: The R5601 requires several clock signals and bias voltages in order to operate properly. Of the 22 pins on the device one is a common pin, four are signal pins (two input and two output), four are bias input pins, and 13 are clock input pins. The required voltages for these pins are delineated in the R5601 data sheet. As noted in the previous chapter, many inconsistencies exist in the documentation as to the exact levels required for the clock and bias voltages. The levels chosen for the revised design are shown in Table 1. These levels were chosen to meet the requirements of the R5601. They were also chosen to make efficient use of the + 5 volts and + 12 voltages supplied by the Intel MULTIBUS. No additional voltage is required by the revised system. This allows the system to function in any MULTIBUS chassis without modification.

iii) Clock waveforms: Thirteen clock signals are required by the R5601. The shape and timing of these waveforms are very important to the performance of the spectral analysis system. The timing of these waveforms will not be discussed here. Timing considerations will be presented later in the section on the synchronization/timing block. The constraints on the shape of the clock signal are discussed here.

The R5601 data sheet places several contraints on the shape of the clock signals. The first constraint is on the low level clock voltage. This low level voltage must be no more than 0.4V above the voltage on the common pin of the R5601. It must also be no lower than the common pin voltage. A second constraint is that the clock signals must not possess any overshoot or undershoot. This is especially

TABLE 1 R5601 Clock and Bias Levels

R5601 pin #	Function	Symbol	Voltage*	
1	Substrate potential	Sub	-12	
3	Common	Com	- 5	
12	Signal channel output gate	V_{OG}	- 2	
20	Output supply voltage	V_{DD}	+12	
22	Corner bias voltage	V_{CB}	- 2	
4	Major phase split-gate clock line	ϕ_1^-	+ 7	one driver
6	Major phase split-gate clock line	ϕ_1^+	+ 7	
19	Major phase split-gate clock line	ϕ_3^-	+ 7	one driver
17	Major phase split-gate clock line	ϕ_3^+	+ 7	
21	Minor phase clock line	ϕ_2	0	
2	Minor phase clock line	ϕ_4	0	
16	Input sampling gate (real)	I_{SGR}	+ 7	one driver
7	Input sampling gate (imag.)	I_{SGI}	+ 7	
15	Input receiving gate (real)	I_{RGR}	+ 4.6	one driver
8	Input receiving gate (imag.)	I_{RGI}	+ 4.6	
11	Output Reset	RESET	+ 7	
5	Reset Clock for ϕ_1	ϕR1	+12**	
	Reset Clock for ϕ_3	ϕR3	+12**	

* For clock signals this is the high voltage, low voltage + -5V
** These clock signals have a low voltage of -12V

important for the four major phase split-electrode clock signals. A third and final condition is placed on the rise and fall times of major and minor phase clocks. The rise time of the major phase clocks as well as both the rise and fall times of the minor phase clocks should be between 10 ns and 50 ns. The major phase clock fall time should be between 50 ns and 100 ns.

b) Clock drivers: The clock drivers are a very important part of the transversal filtering unit. They convert the TTL level clock signals from the synchronization/timing block to the signal levels needed by the R5601. No currently marketed clock drivers were found that could meet all the requirements of the clock signals. To meet these requirements, custom clock drivers were designed using Signetics SD5000 D-MOS FET quad analog swith arrays. These switches were used because of their extremely fast switching times.

A schematic diagram of one of the clock drivers is shown in Figure 30. The clock driver is designed to switch between some positive voltage V and a low voltage of -5 volts. The driver is an inverting driver. The output is high (+V) when the input is low, and low (-5V) when the input is high. This was one criterion the previous driver did not meet. The output stage of the clock drivers is a push-pull stage. A push-pull stage was chosen so that very fast rise times can be achieved even when driving highly capacitive loads. Actual rise times are dependent on the load capacitance and high-level output voltage.

Not all of the R5601 clock signals require individual clock drivers. Only six separate drivers are needed. The sets of clock signals which can be driven by a single clock driver are delineated in

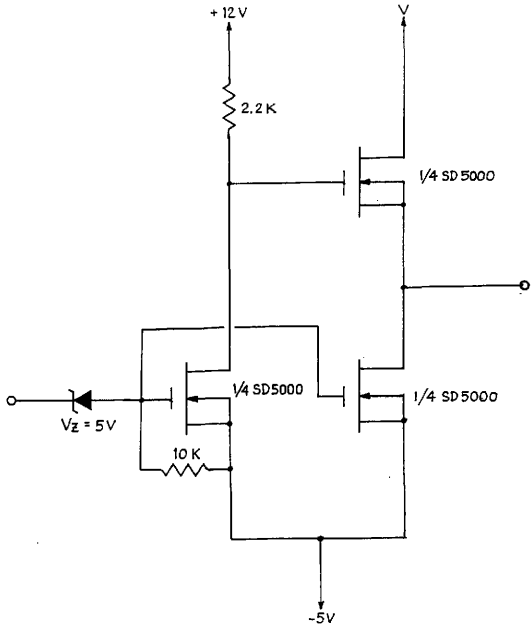


Figure 30 - Schematic of a CCD Clock Driver

Table 1. The drivers for the four major phase clock lines are actually contained in the signal extractor. The two reset clocks are also driven with clock drivers within the signal extractor. The reset clock signals have a low level of -12V.

4) Signal extractor: The signal extractor is the most important block in the spectal analysis system. It is responsible for extracting the convolved output from the R5601 and converting it to a voltage. A block diagram of the signal extractor is shown in Figure 31.

The signal extractor is comprised of two channels. Two channels are necessary because the output of the R5601 is complex and thus consists of a real and imaginary component. The real component is extracted using the first channel from the ϕ_1 clock lines. The imaginary component is extracted using the second channel from the ϕ_3 clock lines.

Each of these two channels is composed of three major subsections. These are: the differential current integrator (DCI), the synchronization sample-and-holds, and the dc stabilizer. Each of these sub-sections perform a major part of the signal extraction process and will be considered separately.

a) Differential current integrator: The convolved output of the R5601 is in the form of charge transferred along its split electrode clock lines. The purpose of the differential current integrator is to convert this output to a voltage. A brief discussion on the charge outputs of the R5601 is presented in order to help understand how this output can be extracted. A more complete discussion is presented in Appendix B.

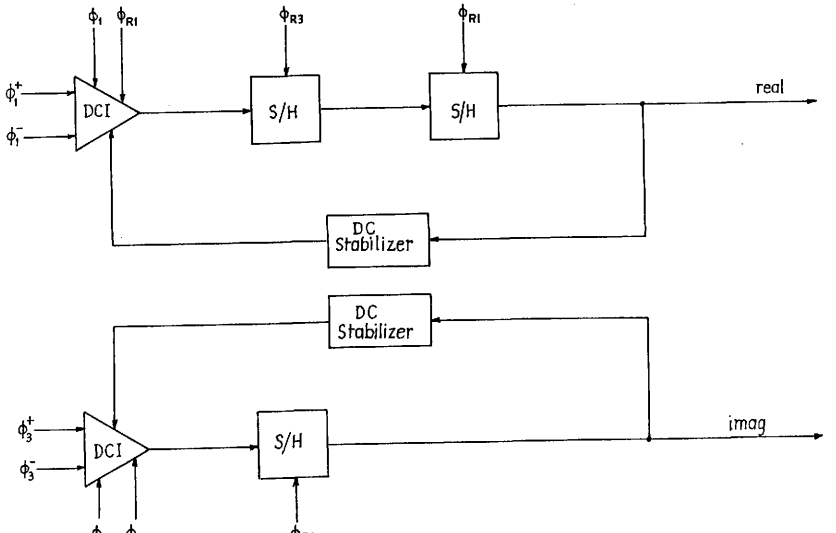


Figure 31 - Signal Extractor Block Diagram

The R5601 uses split gate weighting to perform its convolution. Because of this, the two major clock phases ϕ_1 and ϕ_3, must be supplied as two clock line pairs $\{\phi_1^+,\phi_1^-\}$ and $\{\phi_3^+,\phi_3^-\}$. The ϕ^+ line is one side of the split electrode and the ϕ^- line is the other. To extract the convolved output of the R5601, the difference in charge transferred along the two clock lines must be measured. The differential current integrator performs this function.

A schematic showing the differential current integrator for the revised spectral analysis system is presented in Figure 32. This design is considerably different from the one used in the current system. The design change has achieved several advantages. The first advantage is the reduction of capacitors required. In the current design, six precision capacitors were required. These capacitors had to be silver mica capacitors because of the fast clock rates and had to be matched to 0.1%. The new design requires only two capacitors. These capacitors must also be silver mica and matched to 0.1%. The trade off that takes place is that the new design requires three operational amplifiers. The current design requires only one operational amplifier. Another advantage of the new design is that the clock is directly coupled to the split gate electrodes. The current design does this coupling through a pair of 680 pF capacitors. This coupling can be seen in Figure 25. By direct coupling the split gate electrodes to the clock line they are more accurately held at the same potential. The looser capacitive coupling of the current design does not accurately achieve this objective.

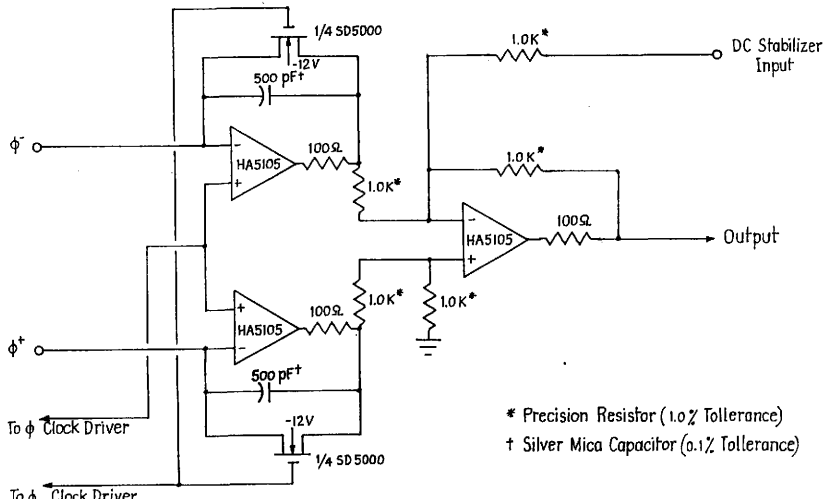


Figure 32 - Schematic of the Differential Current Integrator

b) Synchronization sample-and-holds: Three sample-and-holds are contained within the signal extractor. These sample-and-holds are shown in Figure 31. The sample-and-holds perform two functions. The single sample-and-hold in the ϕ_3 channel and the first sample-and-hold in the ϕ_1 channel perform the first function. This function is the sampling of the output of the differential current integrator. The reason for these sample-and-holds was presented in Chapter III. The output of the differential current integrator must be sampled just before the fall of the clock line which drives its split gate clock lines. This is achieved using the opposing reset lines as clocks for the sample-and-holds. The third sample-and-hold is required for synchronization. This is necessary because the extraction for the different channels occurs on different clock phases. The extra sample-and-hold in the ϕ_1 channel brings these two outputs into time synchronization.

The actual circuit for a sample-and-hold is rather simple. The schematic for this circuit is shown in Figure 33. The circuit consists of an SD5000 analog switch, a silver mica capacitor, and an operational amplifier. The Harris HA5105 operational amplifier is used because of its fast slew rate and low input offset voltage. The capacitor used is silver mica because of the high switching rates. The clock signal for the analog switch is supplied by a clock driver within the signal extractor.

c) Clock drivers: The signal extractor contains four clock drivers. These are for the ϕ_1,ϕ_3,ϕ_{R1}, and ϕ_{R3} clock lines. The ϕ_1 and ϕ_3 clock drivers are of the form shown in Figure 30. This is done because of the fast rise and fall times desired. The ϕ_{R1} and

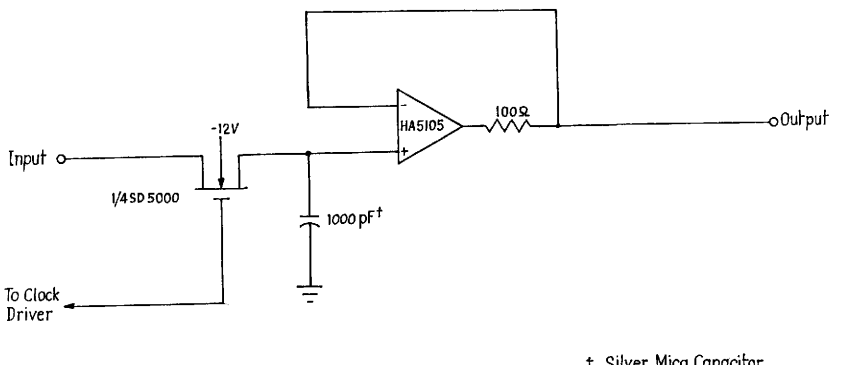


Figure 33 - Schematic of a Sample-and-Hold

ϕ_{R3} drivers are shown in Figure 34. These clock drivers are considerably simpler than the main phase drivers. They also have a different low level output voltage. The drivers are designed to supply a $\pm$12V clock signal from a TTL level input. Note that both types of drivers are inverting in nature.

d) DC stabilizer: The final part of the signal extractor is the dc stabilizer. The purpose of the dc stabilizer is to remove the unwanted dc bias present in the extracted signal. This bias was introduced in the transveral filtering unit to satisfy the input requirements of R5601.

The most difficult task in designing the spectral analysis system is designing an effective dc stabilizer. The performance of this dc stabilizer more severely limits the dynamic range ratio of the spectral analysis system than any other circuit element in the system.

The problem of designing a dc stabilizer to eliminate the bias present in the extracted signal is quite fundamental. In order to eliminate the bias level, some means of identifying its presence must be developed. To do this some sort of assumption must be made about the spectral characteristics of the signal being analyzed. Two such assumptions are spectral vacancy and random phase.

The assumption of spectral vacancy is rather simple. It assumes that a specific spectral estimate has a value of zero. The detection of the output bias level is done by simply sampling the estimate. Because the estimate should be zero, its value will be that of the output bias level.

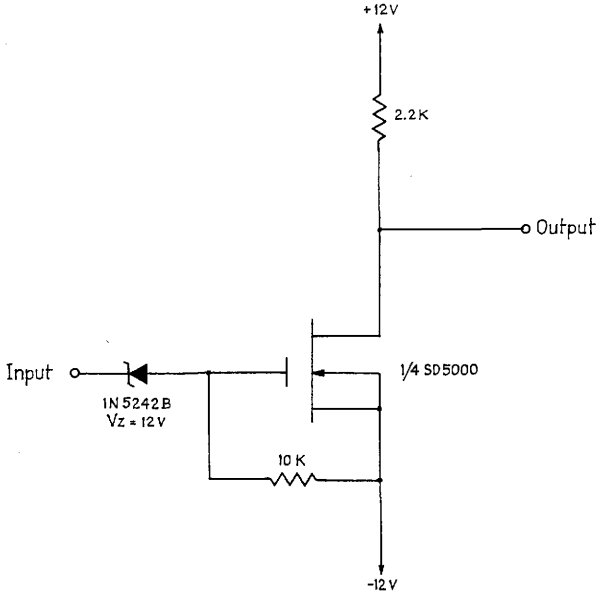


Figure 34 - Reset Clock Drivers

The problem with spectral vacancy is that it is not always an easy assumption to meet. One instance when the assumption of spectral vacancy is met is when the system contains a anti-aliasing filter. In such a case the spectral estimates outside of the pass-band of the filter should be zero. The existence of spectral leakage discussed in Chapter II tends, however, to limit this assumption. The revised system does not contain an anti-aliasing filter. For this reason the assumption of spectral vacancy is not used to detect the output bias level in the revised system.

The assumption of random phase is a much less limiting assumption. It is, however, more difficult to use in detecting the output bias level. Random phase is the assumption used in both the current and revised system to detect the output bias level.

The assumption of random phase states that the phase of any specific spectral estimate is random from record to record. This assumption is valid for a signal if it meets two criteria. First, it must contain no dc component. This is because a dc quantity is always constant in phase. Secondly, the signal must contain no component which is synchronous to the system clock rate. Such a component would also be constant in phase from record to record.

The revised system allows the user to select between two different techniques for eliminating the output bias. The first technique is analog. A circuit employing this technique is designed into the system. It can be enabled or disabled under software control. The second technique is a digital processing technique and is much more accurate than the analog technique. It, however, requires a significant amount of processing by the microprocessor. For this reason,

the digital method is not easly done at fast system clock rates.

i) An analog dc stabilizer: DC stabilization can be performed in an analog fashion. This is done by integrating the output spectral estimates over time. The random phase of each output spectral estimate will cause the output to be the accumulated dc bias level. This level must then be divided by the number of estimates integrated to produce the actual dc bias level.

A schematic showing the analog dc stabilizer used in the revised system is shown in Figure 35. The stabilizer uses switched capacitor techniques to perform the integration. This is done because of the sampled nature of spectral outputs. The integrator is designed to integrate continuously with a gain of 1/512. The integrator output is not, however, transferred to the output of the stabilizer until the end of the record. This is done so that the dc level feedback does not change in mid-record and thus distort the output spectrum. Also note the diode limiters on the input of the stablizer. These are provided to prevent abrupt changes in the dc stabilizer output level.

ii) A digital method for dc stabilization: Another method for dc stabilization can be performed by the microprocessor. For this technique, the analog dc stabilizer must be disabled. This can be done under software control. By disabling the analog dc stabilizer, the bias level is passed with the signal to the magnitude computer. The output spectral estimates will thus be composed of the true estimates and a dc bias level. This can be written as,

$$Fk' = Fk + (ROS + jIOS) \qquad (4.3)$$

where ROS and IOS are the real and imaginary bias levels. The mag-

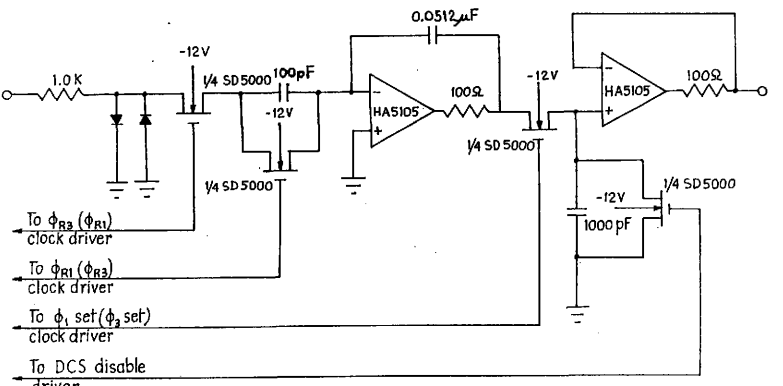


Figure 35 - DC Stabilizer for ϕ_1 (ϕ_3) Channel

nitude of this signal computed by the magnitude computer will be

$$|Fk'|^2 = |Fk|^2 + 2ROS[Re(Fk)] + 2IOS[Im(Fk)] + ROS^2 + IOS^2. \quad (4.4)$$

If this value is averaged over a large number of records N then the result will be

$$\frac{1}{N}\sum_{n=1}^{N}|Fk'|^2 = \frac{1}{N}\sum_{n=1}^{N}|Fk|^2 + \frac{2ROS}{N}\sum_{n=1}^{N}Re(Fk) + \frac{2IOS}{N}\sum_{n=1}^{N}Im(Fk) +$$

$$+ ROS^2 + IOS^2 \quad (4.5)$$

Because of the assumption of random phase the above equation becomes

$$\frac{1}{N}\sum_{n=1}^{N}|Fk'|^2 = \frac{1}{N}\sum_{n=1}^{N}|Fk|^2 + ROS^2 + IOS^2 \quad (4.6)$$

Also, because of random phase, if the values of Fk' are summed from record-to-record the values of ROS and IOS can be found.

$$IOS = \frac{1}{N}\sum_{n=1}^{N}Re[Fk'] \quad (4.7)$$

$$ROS = \frac{1}{N}\sum_{n=1}^{N}Im[Fk'] \quad (4.8)$$

Thus the true spectral estimates can be computed from the output spectral estimates by the equation

$$\frac{1}{N}\sum_{n=1}^{N}|F_k|^2 = \frac{1}{N}\sum_{n=1}^{N}[F_k'] - \left[\frac{1}{N}\sum_{n=1}^{N}Re(F_k')\right]^2 - \left[\frac{1}{N}\sum_{n=1}^{N}Im(F_k')\right]^2 \quad (4.9)$$

where Fk' is the output spectrum containing the unwanted bias levels. The size of N can be determined by performing the sums in equations 4.7 and 4.8 until they produce a constant over all k.

5) Magnitude computer: The purpose of the magnitude computer is to calculate the complex magnitude of output spectral estimates. The

current system did this digitally. This required a large amount of control which burdened the synchronization/timing unit. The revised magnitude computer is an analog circuit which requires no control signals. The revised magnitude computer also provides both a linear and logarithmic output. This allows the user to work with the output in either V^2 or dB. A schematic of the magnitude computer for the revised system is shown in Figure 36.

6) Controller: The controller is responsible for providing synchronization and timing to all the other system blocks. The controller also provides the digital down-chirp required by the premultiplier. All outputs of the controller are TTL level signals. Level translation of these signals is provided, where necessary, within the blocks to which the signal is supplied.

In the current system the controller provides for more than just synchronization and timing. A large part of the function of the current controller provides for processing of the output spectral estimates. These estimates are converted from analog to digital, squared, and summed to produce the power spectrum. The power spectral estimates are then accumulated record-by-record into a small on-board memory. Upon completion, the contents of the memory are then transferred to the system memory.

The revised system controller is much simpler than the controller of the current system, mainly because the output spectral estimates are neither converted to digital form nor processed and stored. The analog-to-digital conversion of the output spectral estimates and the processing and storage of the estimates account for most of the

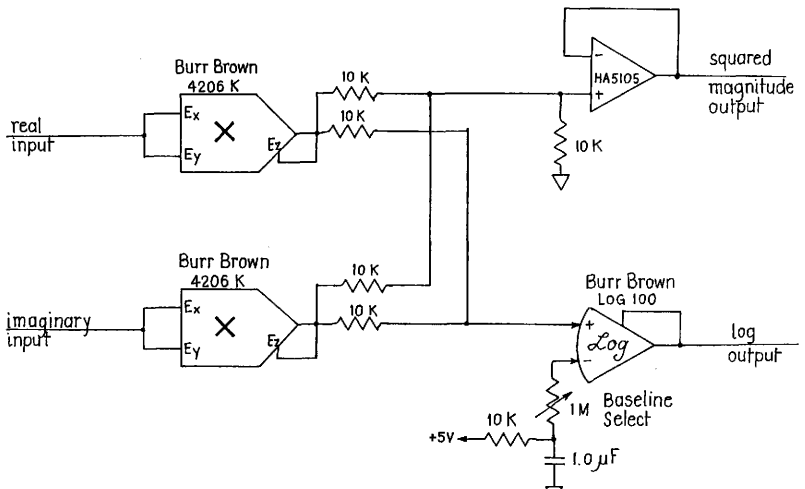


Figure 36 · Magnitude Computer

complexity of the current system controller. The analog-to-digital conversion can be performed with a commercially available A-to-D board. The processing and storage can be performed by the microprocessor. For this reason the analog-to-digital conversion, processing, and storage of the output spectral estimates is not included in the revised system.

A block diagram for the controller is shown in Figure 37. The controller resides on separate card from the other circuitry. This card is made by MDB and provides the MULTIBUS interface logic shown in the diagram. The MULTIBUS is a very versatile bus structure and supports a large number of products. A disadvantage of the bus is that interface design can be difficult. For this reason the MDB board was chosen to supply the interface logic. Another advantage of using a separate board for the controller is that it separates the digital and analog circuitry, thus reducing noise. Clock and control signals generated by the controller board are transferred to the analog board through the 60 pin auxillary connector. Use of this connector reduces the amount of cabling between the boards.

Besides the MULTIBUS interface logic, the controller consists of six other blocks. These blocks are shown in Figure 37. They are: the control latch, the sample rate latch, the clock rate divider, the multi-phase clock generator, the chirp generator, and the control logic.

a) Control and sample rate latches: The purpose of the control and sample rate latches are to hold the control and sample rate information which is transferred to the controller board. Each of the two latches are identical. A schematic showing the circuitry for these

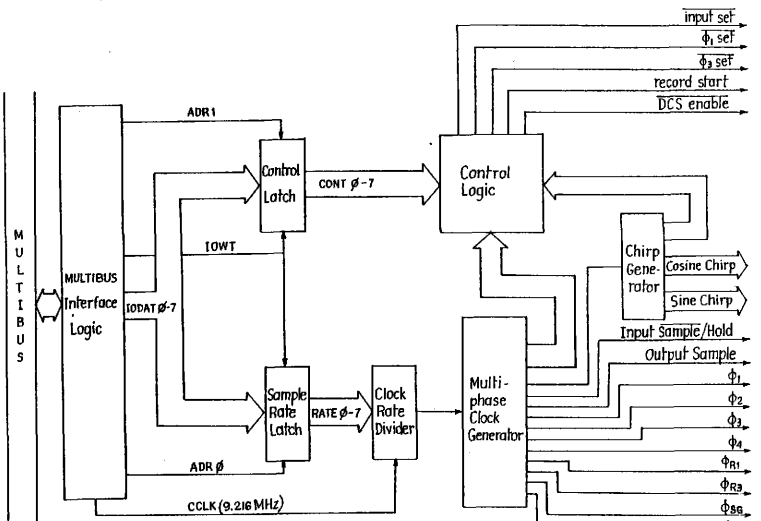


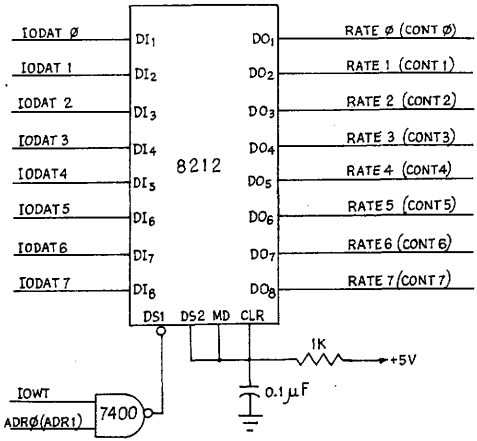
Figure 37 - Controller Block Diagram

latches is shown in Figure 38.

b) Clock rate divider: The clock rate divider supplies the clock signal for the multi-phase clock generator. This clock rate is fifteen times the system clock rate. The rate is selected by the data held in the sample rate latch. The clock rate supplied to the multi-phase clock generator is 4608ON Hz where N is the value of the number held in the sample rate latch. Because the multi-phase clock generator has 18 states the resulting system clock rate will be 256ON Hz. This will produce a 5N Hz spacing between spectral estimates.

The circuit used to implement the clock rate divider is shown in Figure 39. It consists of two parts. The first part is a seven bit binary to BCD converter. The second part is a BCD clock rate divider. A flip flop is included at the output of the divider to guarantee a fifty percent duty cycle.

c) Multi-phase clock generator: The purpose of the multi-phase clock generator is to produce the various clock waveforms required by the spectral analysis system. This is done using a counter which counts from zero to seventeen, a sixteen bit wide read-only memory, and a sixteen bit wide data latch. The schematic for the clock generator is shown in Figure 40. Four Schmidt trigger inverters are used in the circuit to delay the edge of the ϕ_1 and ϕ_3 clock lines. This is done to improve the charge transfer efficiency by separating slightly the edges of ϕ_1 and ϕ_3 from the edges of ϕ_2 and ϕ_4. The waveforms of the various clock signals generated by the circuit are stored in the read-only memory. This allows for a simpler and more versatile clock generator circuit. Clock waveforms are shown



Signals shown in parenthesis are for control latch.

Figure 38 - Sample Rate (or Control) Latch

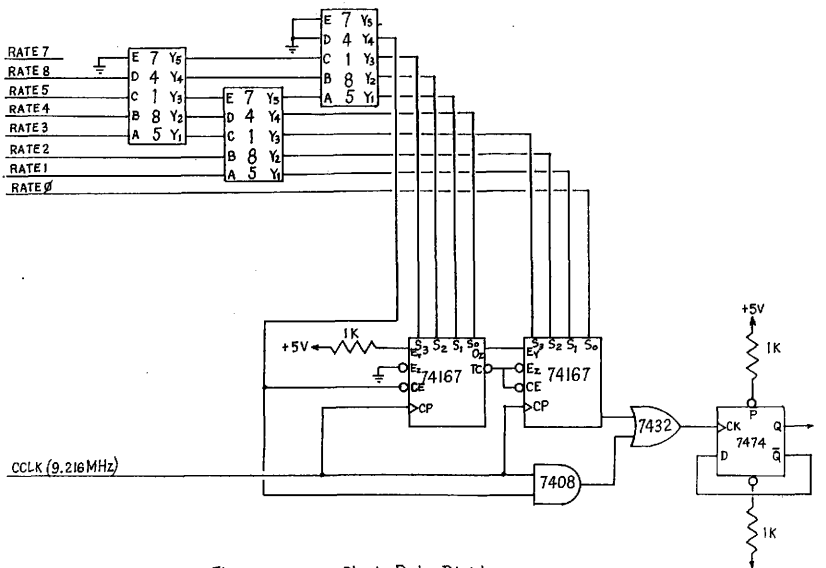


Figure 39 - Clock Rate Divider

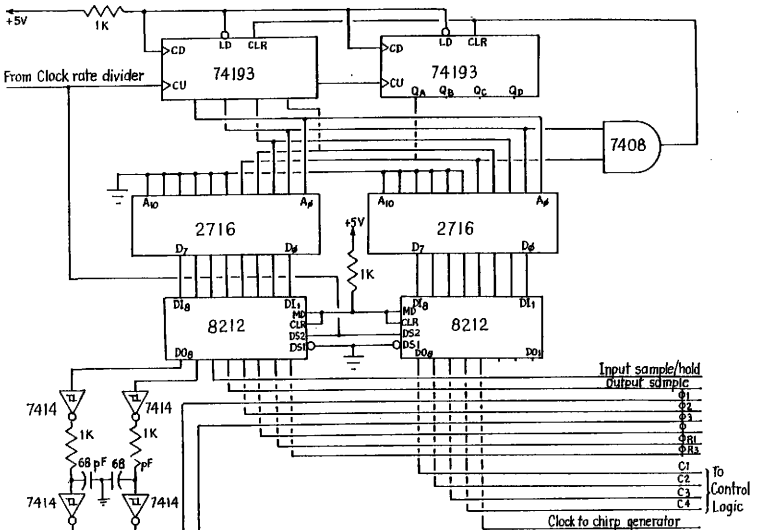


Figure 40 - Multi-phase Clock Generator

in Figure 41. Notice the delayed edges of ϕ_1 and ϕ_3.

d) Chirp generator: The purpose of the chirp generator is to generate the digital down-chirp required by the pre-multiplier. The means by which this is done is very similar to that of the multi-phase clock generator. The circuit consists of an eight bit binary counter and twenty-four bit wide read-only memory. The data latch present in the clock generator circuit is not required in the chirp generator. This is due to the significantly slower clock rate. Because the down-chirp is complex, both its real and imaginary part must be generated. Both are ten bit quantities. Two of the remaining four bits are used for control signals which supply inter-record timing to the control logic. A schematic of the chirp generator is shown in Figure 42.

e) Control logic: The purpose of the control logic is to produce the various control signals needed by the system. These control signals are distinguished from the clock signals in a rather simple way. Clock signals are always periodic with the system sample rate, control signals are not. The control logic block generates five control signals. These are: input set, ϕ_1 set, ϕ_3 set, record start, and DCS enable. All of these except DCS enable are periodic with period 512 T_s where T_s is the time between samples. DCS enable is used to enable or disable the dc stabilizer within the signal extractor. Its level is under software control through the control latch. The record start signal is used to signify to the user the start of a new output record. The other three control signals are used to set new dc stabilizer and dc input levels needed for the new record. Figure 43 shows the circuitry for the control logic block.

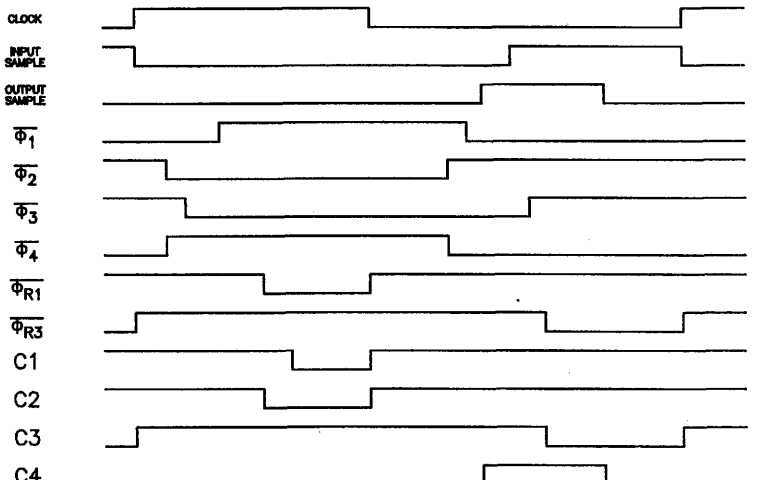


Figure 41 Multi–Phase Clock Generator Waveforms

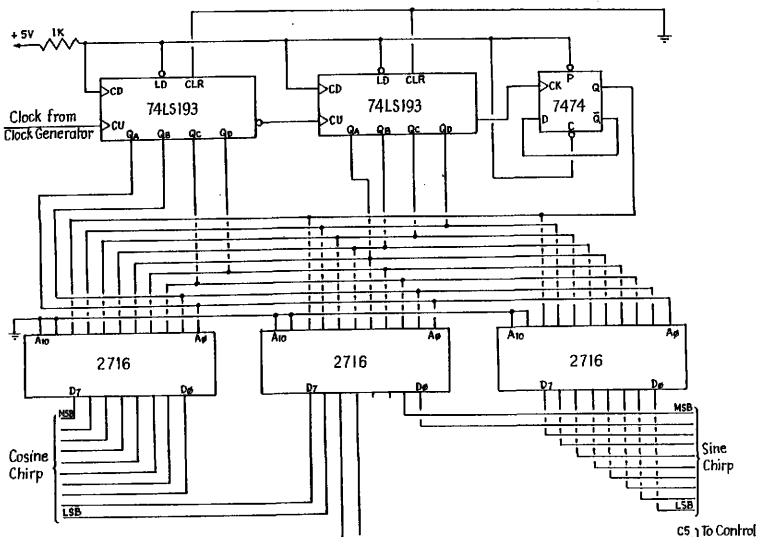


Figure 42 - Chirp Generator

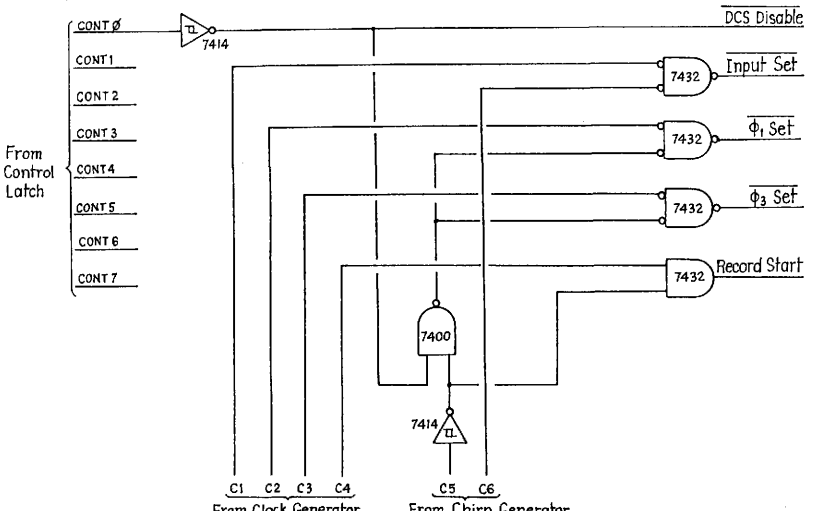


Figure 43 - Control Logic

C. Circuit Layout and Construction: Several considerations must be observed when laying out and constructing the revised system. These considerations aid in reducing system noise and increasing system performance.

The revised spectral analysis system is composed of two circuit boards. The first circuit board is the analog board. This board con tains all of the system's analog circuitry as well as a small amount of digital circuitry. The second board, the synchronization/timing board contains the circuitry resident within the synchronization/ timing system block just previously discussed. This block contains a majority of the digital circuitry required for the system.

1) The analog board: The analog board's circuitry resides on a Intel MULTIBUS prototyping board. The board is well suited for circuit construction. The board's hole spacings and supply bussing architecture allow easy construction using wire-wrap interconnection. The board possesses three card edge connectors, two in the rear and one in the front. One of the rear connectors is dedicated for connection to the MULTIBUS, the other is used to relay signals between the analog and synchronization/timing boards. The front connector is used for connection of the analog input signals to the system.

To reduce noise and increase performance, several precautions must be observed when constructing the analog board. The first precaution is de-coupling. To reduce noise coupled to system components through their supplies, all analog devices must be de-coupled. This de-coupling was not shown in the schematics presented in this chapter to prevent from cluttering the figures. Another precaution which

should be observed is to limit wire lengths. Wires which couple clock drivers to the devices they drive must be low in inductance to prevent transients. If driver wires must be long, several wires should be used in parallel to keep the inductance low. In the case of signal wires, if the wire must be longer than three to four inches, use a twisted pair to reduce noise coupling by mutual inductance. Wires connecting the output of the R5601 to the signal extractors should be kept to less than two inches. These wires should also be well isolated from the CCD clock lines. These wires carry very low level charge and are extremely suceptible to noise. Also, all capacitors within the signal extractor circuits should be soldered in place to prevent contact capacitance induced inaccuracies. Strict adherence to these various precautions should prove to provide better system performance.

2) The synchronization/timing board: The synchronization/timing board is constructed on a circuit board produced by MDB Systems Inc. This board provides the interface circuitry necessary to interface to the Intel MULTIBUS. Interconnection of the two system boards is achieved by the auxillary connector on the back of each board. This eliminates the cumbersome cabling used between the boards of the current system.

D. Conclusion

The revised spectral analysis system has been presented in this chapter as a solution to the problems of the current design. This revised system is much more versatile than the current system. Many

system attributes may be altered under software control. The revised system requires no alignment adjustments. This is a major feature of the revised system which increases its utility. The system also requires no additional supply voltages. The only voltage levels that are required are those supplied by the MULTIBUS. Considering all of these advantages, the revised system presented here is a major improvement over the current design.

CHAPTER V

CONCLUSIONS AND RECOMMENDATIONS

This report has presented the design for a versatile real-time spectral analysis system which is easily interfaced to a microprocessor. This design was developed for use in a wide variety of applications. The system design is based on a breadboard developed by the Remote Sensing Center at Texas A&M University for radar scatterometer data processing. This design was analyzed to identify its strengths, weaknesses and limitations. The results of this analysis was presented in Chapter III. Both systems perform their spectral analysis by using a CCD (charge coupled device) transversal filter to compute the Chirp Z-transform. Because the technique is relatively new, an examination of the transform was presented in Chapter II, additional details are also presented in two of the appendicies which follow. The new system design was presented in Chapter IV.

Since the beginning of this project, many advances in digital technology have occurred. These advances have allowed digital computation of discrete Fourier transform to compete with, and in some cases surpass, the speed and low power consumption obtainable using a CCD transversal filter based design. In extremely low power applications, all-on-one-chip designs based around a CCD transversal filter still have their place. One such design made by TI can compute a 512 point discrete Fourier transform at a 1.5 MHz sampling rate, maintaining a 63 dB signal-to-noise ratio and consuming less than 500mW.

[14] These performance levels can be achieved only when the entire design is placed on a single silicon chip. Such a design is beyond the scope of this report.

The spectral analysis system presented in Chapter IV represents the best design that could be achieved using a component level CCD transversal filter to implement the Chirp Z-transform. The system is extremely versatile and contains no alignment potentiometers. Sampling rates are selectable from 2.56 to 256 KHz with an expected signal-to-noise ratio of 40 dB. The power consumption is estimated at about 20 watts and is supplied totally from the standard voltages available on the Multibus backplane.

The performance limitations of a similar system using digital computation are set by the characteristics of its two major components. These components are the input analog-to-digital converter (ADC) and the FFT processor.

The input ADC of a digital spectral analysis system is the limiting component which determines both the maximum sampling rate and the signal-to-noise ratio of the system. The advent of the "flash" converter have reduced ADC conversion times by more than an order of magnitude. One such converter is the TRW TDC 1010. This converter is a 9 bit "flash" ADC and has a maximum conversion time of 50 nanoseconds. The 50 nanosecond conversion time allows sampling at rates up to 20 MHz. The 9 bit wide sample word limits the signal-to-noise ratio to about 54 dB. Both of these values exceed the anticipated values discussed above for a component level CCD based spectral analysis system.

If a better signal-to-noise ratio is desired, a wider converter can be used. This, however, will reduce the maximum sampling rate since wider converters are by necessity slower. Higher sampling rates can similarly be obtained if a lower signal-to-noise ratio is acceptable. Advances in ADC technology have allowed digital spectral analysis systems to exceed the maximum sampling rate and signal-to-noise levels achievable in CCD based analog systems.

The FFT processor of a digital spectral analysis system sets the maximum transform length and record processing speed of the system. The FFT (Fast Fourier Transform) is the most common algorithm used to compute the discrete Fourier transform because of its high speed when implemented on a numerical machine such as a computer. On large machines the FFT is usually computed using an array processor. Array processors allow parallel computations to be performed on long data arrays and thus can compute long FFT's with relative ease. Recently array processors have become available (and affordable) for smaller computers. One such processor is the FFT-523 by Ariel Corporation. It can compute a 1024 point FFT in only 9.2 milliseconds, and has a word width of 16 bits. If dual buffering is used, allowing sampling into one buffer to be performed while the other buffer is being processed, a continuous sampling rate of 100 KHz could be maintained without missing a single data point. This will allow spectral analysis to be done "on-the-fly" at 100 KHz as is done using the sliding chirp Z-transform, but without the undesirable varying phase of the sliding Chirp Z-transform's bandpass characteristics. The 16 bit word allows nearly 100 dB of dynamic range (and thus S/N) if a 16 bit wide

ADC is used. By using CMOS technology power comsumption was held to 10 watts which is better than the 20 watt total power consumption of the CCD component level system. The development of such FFT processors have allowed microcomputer based systems to compute an FFT in less than one percent of the time previously required using software based implementations of the FFT. This has allowed digital spectral analysis systems to compete at speeds previously only attainable by analog systems.

It is the conclusion of this report that while CCD based spectral analysis systems do have their place, a digital FFT based system would better fit the needs and applications of real-time spectral analysis. This conclusion is mostly based on the low signal-to-noise ratio and high cost of a component level CCD based system as compared to a digital system. It is recommended that further research and design efforts be placed in this direction.

REFERENCES

1. J.B.G. Roberts, G.L. Moule, and G. Parry, "Design and Application of Real-Time Spectrum-Analyzer Systems," IEEE Proceedings, Vol. 127, pp. 76-91, April 1980.

2. R.E. Holm, "Program a Spectrum Analyzer on a One-Chip Real-Time Signal Processor," Electronic Design, Vol. 23, November 8, 1979.

3. M.A. Jack and E.G.S. Paige, "Fourier Transform Processors Based on S.A.W. Chip Filters," Wave Electron., Vol. 3, pp. 229-247.

4. J.W. Cooley and J.W. Tukey, "An Algorithm for the Machine Computation of Complex Fourier Series," Math. Comput., Vol. 19, pp. 297-301, 1965.

5. L.I. Bluestein, "A Linear Filtering Approach to the Computation of the Discrete Fourier Transform," 1968 NEREM Rec., pp. 218-219.

6. R.W. Broderson, C.R. Hewes, and D.D. Buss, "A 500-Stage CCD Transversal Filter for Spectral Analysis," IEEE Trans. Electron Devices, Vol. ED-23, pp. 143-152, February 1976.

7. B.R. Jean, "Radar Studies of Arctic Ice and Development of a Real-Time Arctic Ice Type Identification System," Final Report 3005-6, Remote Sensing Center, Texas A&M University, December 1976.

8. J.A. Schell, et al., "Definition and Fabrication of an Airborne Scatterometer Radar Signal Processor," Technical Report 3128-2, Remote Sensing Center, Texas A&M University, December 1976.

9. J.A. Schell, et al., "Definition and Fabrication of an Airborne Scatterometer Radar Signal Processor," Final Report 3182-3, Remote Sensing Center, Texas A&M University, December 1976.

10. J.P. Classman, "The System and Hardware Design of Real-Time Fan Beam Scatterometer Data Processors," Final Report 3556, Remote Sensing Center, Texas A&M University, March 1976.

11. F.J. Harris, "On the Use of Windows for Harmonic Analysis with the Discrete Fourier Transform," Proceedings of the IEEE, Vol. 66, pp. 51-83, January 1978.

12. W.S. Boyle and G.E. Smith, "Charge Coupled Semi-Conductor Devices," Bell System Technical Journal, Vol. 49, pp. 578-593, April 1970.

REFERENCES (continued)

13. G.F. Amelio, M.F. Tompsett, and G.E. Smith, "Experimental Verification of the Charge Coupled Device Concept," Bell System Technical Journal, Vol. 49, pp. 593-600, April 1970.

14. R.C. Pettengill, et al., "A Monolithic 512 Point Chirp-Z Transform Processor," 1979 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, pp. 68-69.

15. C.L. Dolph, "A Current Distribution for Broadside Arrays Which Optimze the Realtionship Between Beam Width and Sidelobe Level," Proceedings IRE, Vol. 34, pp. 335-348, June 1946.

16. G.J. Vand Der Mass, "A Simplified Calculation for Dolph-Tchebycheff Arrays," J. Appl. Phys., Vol. 25, pp. 121-124, January 1954.

17. M.F. Tompsett, G.F. Amelio, and G.E. Smith, "Charge Coupled 8-bit shift Register,"Appl. Phys. Lett., Vol. 17, pp. 111-115, August 1970.

18. M.F. Tompsett, G.F. Amelio, W.J. Bertran, R.R. Buckley, W.J. McNamara, J.C. Mikkelsen, and D.A. Sealer, "Charge Coupled Imaging Device Experimental Results," IEEE Trans. Electron Devices, Vol. ED-18, pp. 992-996, November 1971.

19. W.J. Bertran, D.A. Sealer, C.H. Sequin, and M.F. Tompsett, "Recent Advances in Charge Coupled Devices," 1972 IEEE INTERCON Dig. Papers, pp. 292-293.

20. M.F. Tompsett and E.J. Zimany, "Use of Charge Coupled Devices for Analog Display," 1972 IEEE ISSCC Dig. Tech. Papers, pp. 136-137.

21. D.R. Collins, W.H. Bailey, W.M. Gosney, and D.D. Buss, "Charge Coupled Device Analogue Matched Filters," Electron Letters, Vol. 8, pp. 328-329, June 1972.

22. R.C. Pettengill, P.W. Bosshart, M. de Wit, and C.R. Hewes, "A Monolithic 512 Point Chirp-Z Transform Processor," 1979 IEEE ISSCC Dig. Tech. Papers, pp. 68-69.

23. C.H. Sequin and A.M. Mohlsen, "Linearity of Electrical Charge Injection into Charge Coupled Devices," IEEE J. SCC, Vol. SC-10, pp. 81-92, April 1975.

APPENDIX A

WINDOWING

The purpose of this appendix is to analyze the effects of windowing on the chirp Z-transform. This will be done in two parts. In the first part, the general spectral characteristics of the windowed chirp Z-transform will be analyzed. This analysis will identify the relationship between the chirp Z-transform spectral estimates and the true spectrum of the input signal. It will also identify the effects of a window function on this relationship. In the second part, the characteristics of several different windowing functions will be analyzed. Each of these functions will be analyzed to determine how they effect the capability of the windowed chirp Z-transform to perform spectral analysis.

Spectral Characteristics of the Windowed Chirp Z-Transform

Many times in the main body of this report the chirp Z-transform has been heralded as an effective means of estimating the spectrum of an input signal. It is now important to analyze the characteristics of this estimation. To do this, the chirp Z-transform is first related to the discrete Fourier transform to simplify further analysis. Next, the bandpass characteristic of the transform is derived, thus relating the chirp Z-transform estimates to the true spectrum of the input signal.

Relationship Between the Chirp Z-Transform and Discrete Fourier Transform: The chirp Z-transform and the discrete Fourier transform are mathematically identical transforms. The difference between the two transforms is only the way terms are organized in the expressions. This re-organization of terms allows for the chirp Z-

transform to be more easily implemented in hardware, but it also makes the transform much more cumbersome to analyze. The discrete Fourier transform is much easier to analyze because of its simpler mathematical expression. The following proof demonstrates that the two transforms are identical. Because of this identicality, further analysis can be performed on the discrete Fourier transform and the conclusions will directly apply to the chirp Z-transform.

There are two forms of the chirp Z-transform and the discrete-Fourier transform. These forms are the stationary and sliding transforms. Because these are seperate forms of each transform the proof of identicality will be performed seperately for each form.

Stationary transform: The stationary form of the windowed chirp Z-transform is defined by the following equation.

$$F_k = e^{-j\frac{\pi k^2}{N}} \sum_{n=0}^{N-1} \left[f_n w_n e^{-j\frac{\pi n^2}{N}} \right] e^{j\frac{\pi (n-k)^2}{N}} \qquad k = 0,1,2,\ldots N-1 \qquad (A.1).$$

In this expression, $\{f_n\}$ is the sampled input sequence, $\{w_n\}$ is the window sequence (sampled window function), and $\{F_k\}$ represents the output sequence (Fourier coefficients). This expression can be converted to the expression for the discrete Fourier transform through a series of mathematical manipulations. First, the three exponentials are grouped together inside the summation to form the expression

$$F_k = \sum_{n=0}^{N-1} f_n w_n \left[e^{-j\frac{\pi k^2}{N}} \; e^{-j\frac{\pi n^2}{N}} \; e^{j\frac{\pi (n-k)^2}{N}} \right] \qquad k = 0,1,2,\ldots\ldots N-1 \qquad (A.2)$$

Because the exponentials are of like base, the exponents can be added to produce

$$F_k = \sum_{n=0}^{N-1} f_n W_n \left[e^{-j\frac{\pi}{N}(k^2+n^2-(n-k)^2)}\right]$$
$$k = 0,1,2,.....N-1 \qquad (A.3).$$

Expanding the term $(n-k)^2$ and cancelling out opposing terms produces

$$F_k = \sum_{n=0}^{N-1} f_n W_n e^{-j\frac{2\pi nk}{N}}$$
$$k = 0,1,2,.....N-1 \qquad (A.4).$$

This is the expression for the stationary discrete Fourier transform which is thus, by this proof, mathematically identical to the stationary chirp Z-transform.

Sliding transform: The sliding form of the windowed chirp Z-transform is defined by the following equation.

$$F_k = e^{-j\frac{\pi k^2}{N}} \sum_{n=k}^{k+N-1} \left[f_n e^{-j\frac{\pi n^2}{N}}\right] \left[W_{n-k} e^{-j\frac{\pi(n-k)^2}{N}}\right]$$
$$k = 0,1,2,.....N-1 \qquad (A.5)$$

Terms in this expression are just as they were for the stationary transform. Just as before, the exponential terms are grouped within the summation to form the expression

$$F_k = \sum_{n=0}^{k+N-1} f_n w_{n-k} \left[e^{-j\frac{\pi k^2}{N}} e^{-j\frac{\pi n^2}{N}} e^{j\frac{\pi (n-k)^2}{N}} \right]$$

$$k = 0,1,2,.....N-1 \qquad (A.6).$$

The $(n-k)^2$ term is expanded and the exponents, since they are of like base, are added to produce the equation

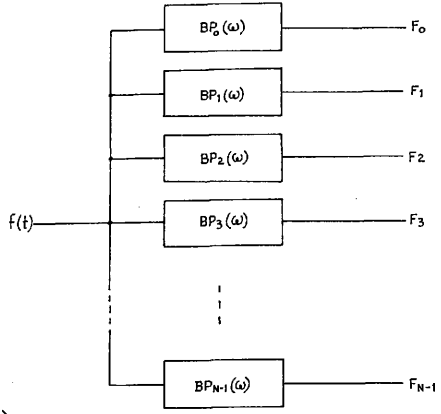
$$F_k = \sum_{N=k}^{k+N-1} f_n w_n e^{-j\frac{2\pi nk}{N}}$$

$$k = 0,1,2,.....N-1 \qquad (A.7).$$

This is the expression for the sliding discrete Fourier transform which is thus, by this proof, mathematically identical to the sliding chirp Z-transform.

The bandpass characteristics of the chirp Z-transform: When the chirp Z-transform is used for spectral analysis, the input sequence $\{f_n\}$ is generated by uniformity sampling the signal under analysis f(t). The output of the transform $\{F_k\}$ will then be estimates of the true spectrum $\mathbf{F(\omega)}$ of f(t).

One way to analyze the characteristics of this estimation is by considering each F_k to be the output of a filter bank whose input is f(t). Figure A-1 shows a diagram of this conceptualization and illustrates how each of the filters will have a transfer function $BP_k(\omega)$ which represents the bandpass characteritics of the filter. This function will be shifted in frequency for each sequential estimate and its shape will depend on the weighting sequence $\{w_n\}$ can be accomplished in two steps. The first step is to derive an



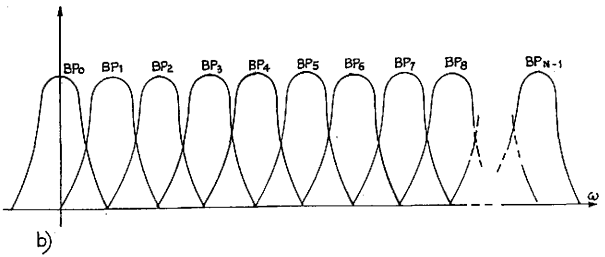


Figure A-1 Filter Bank Concept
a) Block Diagram
b) Frequency Response

equation for the uniformly sampled sequence $\{f_n\}$ and relate it to the true input spectrum $F(\omega)$. Next, this sequence is substituted into the sliding and stationary forms of the discrete Fourier transform. Recall that this transform is mathematicllly identical to the chirp Z-transform.

Relating $\{f_n\}$ to $F(\omega)$: The sequence $\{f_n\}$ is generated by uniformly sampling f(t). If this sampling rate is $\omega_s/2\pi$, then $\{f_n\}$ can be defined by

$$f_n = f(2\pi n/\omega_s) \quad n = 0,1,2,....N-1. \tag{A.8}$$

The input signal f(t) can now be related to its spectrum $F(\omega)$ by the inverse continuous-time Fourier transform

$$f(t) = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega)\, e^{j\omega t} d\omega. \tag{A.9}$$

By placing this expression for f(t) into equation A.8 the sequence $\{f_n\}$ can be expressed in terms of the input signal spectrum $F(\omega)$.

$$f_n = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega)\, e^{j\omega nt} d\omega. \tag{A.10}$$

Deriving $BP_k(\omega)$ for the stationary transform: The derivation first starts with equation A.4. This is the mathematical expression of the stationary discrete Fourier transform and is mathematically identical to the stationary chirp Z-transform by previous proof. If the expression for f_n shown in A.10 is placed

into the equation, the following results

$$F_k = \sum_{n=0}^{N-1} \left[\frac{1}{2\pi} \int_{-\infty}^{\infty} \mathbf{F}(\omega)\, e^{j\omega n t_d \omega}\right] w_n e^{-j\frac{2\pi nk}{N}} \qquad k = 0,1,2,\ldots N-1. \qquad (A.11)$$

To simplify this equation, all terms except $1/2\pi$ are brought inside the integral and the exponentials are combined

$$F_k = \frac{1}{2\pi} \int_{-\infty}^{\infty} \mathbf{F}(\omega) \left[\sum_{n=0}^{N-1} w_n e^{-jnT(\omega - \frac{2\pi k}{NT})}\right] d\omega \qquad k = 0,1,2,\ldots N-1. \qquad (A.12)$$

The term which describes the bandpass characteristics of the stationary transform can be extracted from this equation. It is,

$$BP_k(\omega) = \sum_{n=0}^{N-1} w_n e^{jnT(\omega - \frac{2\pi k}{NT})} \qquad k = 0,1,2,\ldots N-1. \qquad (A.13)$$

Note that the value of k only shifts the center frequency of the filter and does not alter its phase or magnitude. Because of this, the characteristics of all the output spectral estimates for the stationary transform are identical in shape but shifted in frequency.

Deriving $BP_k(\omega)$ for the sliding transform: The derivation starts with equation A.7. This equation is the definition of the siding discrete Fourier transform. It is mathematically identical to the expression for the sliding chirp Z-transform by previous proof. If the expression for f_n shown in A.10 is

substituted into equation A.7, the following results

$$F_k = \sum_{n=k}^{k+N-1} \left[\frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega)\, e^{j\omega n t_{dw}}\right] w_{n-k} e^{-j\frac{2\pi mk}{N}}$$
$$k = 0,1,2,\ldots N-1. \qquad (A.14)$$

This equation can be simplified by bringing all terms except $1/2\pi$ inside the integral and combining the exponentials.

$$F_k = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(w) \left[\sum_{n=k}^{k+N-1} w_n e^{-jnT\left(\omega-\frac{2\pi k}{NT}\right)}\right] d\omega$$
$$k = 0,1,2,\ldots N-1 \qquad (A.15)$$

Further simplification occurs when the summation is re-organized to start at zero.

$$F_k = \frac{1}{2\pi} \int_{-\infty}^{\infty} F(\omega) \left[\sum_{n=0}^{N-1} w_n e^{-j(n+k)T\left(\omega-\frac{2\pi k}{NT}\right)}\right] d\omega$$
$$k = 0,1,2,\ldots N-1 \qquad (A.16)$$

The term which describes the bandpass characteristics of the sliding transform can be extracted from this equation. It is,

$$BP_k(\omega) = \left[\sum_{n=0}^{N-1} w_n e^{jnT\left(\omega-\frac{2\pi k}{NT}\right)}\right] e^{jkT\left(\omega-\frac{2\pi k}{NT}\right)}$$
$$k = 0,1,2,\ldots N-1 \qquad (A.17)$$

Note that for the sliding transform the value of k not only shifts the center frequency of the filter but also affects the phase of its

bandpass characteristics. In most applications this phase variation produces no significant effects.

Spectral Characteristics of Different Windowing Functions

Now that the general equations for the spectral characteristics of the chirp Z-transform have been developed, it is important to utilize these equations to examine the characteristics of several specific windowing functions. A large number of different windowing functions exist, too large to do a complete of windows in this report. For this reason, three specific window functions have been chosen for analysis. These window functions are: the rectangular window, the Hanning window, and the Dolph-Chebyschev window. The spectral characteristics of both the stationary and sliding transform is analyzed for each windowing function.

Rectangular window: The rectangular window is the simplest of all the windowing functions. This window is defined as being unity for all values, that is,

$$w_n = 1 \qquad n = 0,1,2,....N-1. \tag{A.18}$$

When this window function is placed into the windowed chirp Z-transform the result is what is commonly called the unwindowed chirp Z-transform.

Stationary transform: The spectral characteristics of the stationary transform using the rectangular windowing function can be computed by substituting the equation of the windowing function (equation A.18) into the equation for the stationary chirp-Z transform

(equation A.13). This substitution produces the equation

$$BP_k(\omega) = \sum_{n=0}^{N-1} e^{jnT(\omega - \frac{2\pi k}{NT})} \qquad k = 0,1,2,\ldots N-1. \qquad (A.19)$$

This equation represents an arithmetic progresson and can thus be computed using the arithmetic progression formula. The arithmetic progression formula is

$$\sum_{n=0}^{N-1} a^n = \frac{a^n - 1}{a - 1} \quad . \qquad (A.20)$$

If the base a is defined as a complex exponential then the arithmetic progression formula (A.20) becomes

$$\sum_{n=0}^{N-1} e^{j\alpha n} = \frac{e^{j\alpha N} - 1}{e^{j\alpha} - 1} = \frac{\sin(\frac{\alpha N}{2})}{\sin(\frac{\alpha}{2})} \; e^{j\frac{\alpha(N-1)}{2}}. \qquad (A.21)$$

Substituting this result into equation A.19 yields

$$BP_k(\omega) = \left\{ \frac{\sin[\frac{NT}{2}(\omega - \frac{2\pi k}{NT})]}{\sin[\frac{T}{2}(\omega - \frac{2\pi k}{NT})]} \right\} e^{j[\frac{(N-1)T}{2}(\omega - \frac{2\pi k}{NT})]} \quad . \qquad (A.22)$$

This equation clearly identifies the magnitude and phase of the stationary chirp Z-transform using the rectangular windowing function. A plot of the magnitude function is presented in Figure A-2.

Sliding transform: The spectral characteristics of the sliding transform using the rectangular windowing function can be computed in a manner similiar to the above process. Substituting the equation for the rectangular window (A.18) into the equation for the bandpass characteristics of the sliding transform (A.17) yields

$$BP_k(\omega) = \left[\sum_{n=0}^{N-1} e^{jnT(\omega-\frac{2\pi k}{NT})}\right] e^{jkt(\omega-\frac{2\pi k}{NT})} \qquad k = 0,1,2,\ldots N-1 \qquad (A.23)$$

This equation can be simplified using the modified arithmetic progression formula shown in equation A.21.

$$BP(\omega) = \left\{\frac{\sin\left[\frac{NT}{2}(\omega-\frac{2\pi k}{NT})\right]}{\sin\left[\frac{T}{2}(\omega-\frac{2\pi k}{NT})\right]}\right\} e^{j\left[\frac{(N-1)}{(k+2)}T(\omega-\frac{2\pi k}{NT})\right]} \qquad (A.24)$$

Since the magnitude of the bandpass characteristics is identical for the stationary and sliding transforms, Figure A-1 also represents a plot of the magnitude of the bandpass characteristics of the sliding chirp Z-transform using the rectangular window.

Comments: Figure A-2 illustrates that the rectangular window produces very high peaks outside the central lobe. These peaks

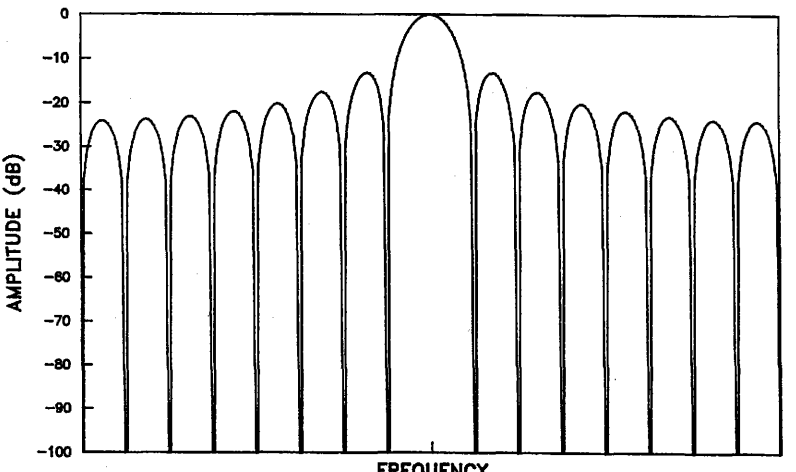


Figure A–2 Bandpass Characteristics of a 16–point Rectangular Window

are called side lobes. Side lobes are the cause of the "frequency leakage" effect discussed in Chapter II of this report. Because the nulls of the plot occur at mulitiples of the sampling rate, "frequency leakage" does not occur if the input signal is synchronous to the sample clock. Another characteristic of the rectangular window is its extremely narrow main lobe. The rectangular window produces the narrowest possible main lobe of all windowing functions.

Hanning window: The Hanning window is a commonly used windowing function. The form of the Hanning window is one cycle of a squared sine wave and can thus be described by the equation

$$w_n = \sin^2\left(\frac{n\pi}{N}\right) \qquad n = 0,1,2,....N-1. \tag{A.25}$$

by smoothly attenuating the input sequence, $\{fn\}$ to zero at its end points, the Hanning window reduces the large side lobes observed using the rectangular window, yet still maintains a form which allows for easy calculation.

Stationary transform: If the equation for the Hanning window (A.25) is placed into the general equation for the bandpass characteristics of the stationary transform, the following results

$$BP_k(\omega) = \sum_{n=0}^{N-1} \sin^2\left(\frac{n\pi}{N}\right) e^{jnt\left(\omega - \frac{2\pi k}{NT}\right)} \qquad k = 0,1,2,...N-1. \tag{A.26}$$

To simplify this equation, the sine squared function is broken up into a sum of complex exponentials to produce

$$BP_k(\omega) = \sum_{n=0}^{N-1} \left[-1/4\, e^{-j\frac{2n\pi}{N}} + 1/2 - 1/4 e^{j\frac{2n\pi}{N}}\right] e^{jnt(\omega-\frac{2\pi k}{NT})}$$

$$k = 0,1,2,\ldots N-1. \qquad (A.27)$$

Applying the modified arithmetic progression formula shown in A.21 yields the simpler expression

$$BP_k(\omega) = \left\{ -\frac{\sin\left[\frac{NT}{2}(\omega - \frac{2\pi K}{NT}) - \pi\right]}{4\sin\left[\frac{T}{2}(\omega - \frac{2\pi K}{NT}) - \frac{\pi}{N}\right]} e^{j\left[\frac{(N-1)T}{2}(\omega - \frac{2\pi k}{NT}) - \frac{\pi(N-1)}{N}\right]} \right.$$

$$+ \frac{\sin\left[\frac{NT}{2}(\omega - \frac{2\pi K}{NT})\right]}{2\sin\left[\frac{T}{2}(\omega - \frac{2\pi K}{NT})\right]} e^{j\left[\frac{(N-1)T}{2}(\omega - \frac{2\pi k}{NT})\right]}$$

$$\left. - \frac{\sin\left[\frac{NT}{2}(\omega - \frac{2\pi K}{NT}) + \pi\right]}{4\sin\left[\frac{T}{2}(\omega - \frac{2\pi K}{NT}) + \frac{\pi}{N}\right]} e^{j\left[\frac{(N-1)T}{2}(\omega - \frac{2\pi K}{NT}) + \frac{\pi(N-1)}{N}\right]} \right\}$$

$$K = 0,1,2,\ldots N-1 \qquad (A.28)$$

By re-arranging a few terms of this equation, another equation is produced which more clearly illustrates how the Hanning window produces lower sidelobes and a wider main lobe than the rectangular window.

$$BP_K(\omega) = \left\{ -\frac{1}{4} \frac{\sin\left[\frac{NT}{2}(\omega - \frac{2\pi(K+1)}{NT})\right]}{\sin\left[\frac{T}{2}(\omega - \frac{2\pi(K+1)}{NT})\right]} e^{j\left[\frac{(N-1)T}{2}(\omega - \frac{2\pi(K+1)}{NT})\right]} \right.$$

$$+ \frac{1}{2} \frac{\sin\left[\frac{NT}{2}(\omega - \frac{2\pi K}{NT})\right]}{\sin\left[\frac{T}{2}(\omega - \frac{2\pi K}{NT})\right]} e^{j\left[\frac{(N-1)T}{2}(\omega - \frac{2\pi K}{NT})\right]}$$

$$\left. - \frac{1}{4} \frac{\sin\left[\frac{NT}{2}(\omega - \frac{2\pi(K-1)}{NT})\right]}{\sin\left[\frac{T}{2}(\omega - \frac{2\pi(K-1)}{NT})\right]} e^{j\left[\frac{(N-1)T}{2}(\omega - \frac{2\pi(K-1)}{NT})\right]} \right\}$$

$$K = 0,1,2,\ldots N-1 \qquad (A.29)$$

This equation illustrates that the bandpass characteristics of the stationary transform using the Hanning widow can be decomposed into three parts. One part is identical to the equation for the bandpass characteristics of the stationary transform using the rectangular window (A.22) but one half the amplitude. The other two parts are the same equation except shifted one sample to the left and right, inverted, and at one fourth amplitude instead of one half. Because of the regular spacing of the sidelobes, these two extra parts aid in reducing the sidelobe levels by cancellation, but also cause the broadening of the mainlobe. The magnitude of equation A.29 is plotted in Figure A-3.

Sliding transform: By inserting the equation for the Hanning window (A.25) into the general equation for the bandpass characteristics of the stationary transform, the following equation results

$$BP_k(\omega) = \left[\sum_{n=0}^{N-1} \sin^2\left(\frac{n\pi}{N}\right) e^{jnt\left(\omega - \frac{2\pi k}{NT}\right)} \right] e^{jkt\left(\omega - \frac{2\pi k}{NT}\right)} \qquad k = 0,1,2,\ldots N-1 \qquad (A.30)$$

Simplifying this equation using the modified arithmetic progression yields

$$BP_K(\omega) = \left\{ -\frac{1}{4} \frac{\sin\left[\frac{NT}{2}\left(\omega - \frac{2\pi(K+1)}{NT}\right)\right]}{\sin\left[\frac{T}{2}\left(\omega - \frac{2\pi(K+1)}{NT}\right)\right]} e^{j\left[\frac{(N-1)T}{2}\left(\omega - \frac{2\pi(K+1)}{NT}\right)\right]} + \frac{1}{2} \frac{\sin\left[\frac{NT}{2}\left(\omega - \frac{2\pi K}{NT}\right)\right]}{\sin\left[\frac{T}{2}\left(\omega - \frac{2\pi K}{NT}\right)\right]} e^{j\left[\frac{(N-1)T}{2}\left(\omega - \frac{2\pi K}{NT}\right)\right]} - \frac{1}{4} \frac{\sin\left[\frac{NT}{2}\left(\omega - \frac{2\pi(K-1)}{NT}\right)\right]}{\sin\left[\frac{T}{2}\left(\omega - \frac{2\pi(K-1)}{NT}\right)\right]} e^{j\left[\frac{(N-1)T}{2}\left(\omega - \frac{2\pi(K-1)}{NT}\right)\right]} \right\} e^{j\left[\left(K + \frac{(N-1)}{2}\right)T\left(\omega - \frac{2\pi K}{NT}\right)\right]}$$

$$K = 0,1,2 \ldots N-1 \qquad (A.31)$$

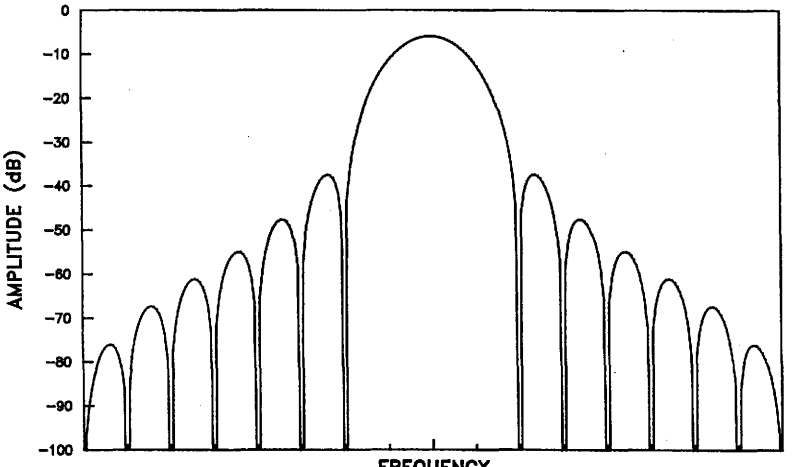


Figure A-3 Bandpass Characteristics of a 16-point Hanning Window

Since this equation differs from (A.29) only in the presence of a common phase term, the magnitude of the equations are equal. This means that the plot in Figure A-3 also represents the magnitude of bandpass characteristics of the sliding chrip Z-transform using the Hanning window.

Comments: The Hanning window produces lower sidelobes levels at the cost of a wider main lobe. This is easily seen by comparing figures A-2 and A-3. The first sidelobe level is reduced by 19dB when the Hanning window is used instead of the rectangular window. The width of the main lobe is increased by 60%.

Dolph-Chebyschev window: The Dolph-Chebyschev window function optimizes the trade off between side lobe height and mainlobe width. Dolph [15] developed the window function in 1946. He made use of the Chebyschev polynomials to develop the windowing function and prove that it produced the narrowest possible main lobe for a given maximum sidelobe height. Two major problems exist with this window function; complexity and uniform sidelobe height.

Complexity is a major pitfall of the Dolph-Chebyschev windowing function. When Dolph first presented it in 1946 [15], it was necessary to derive all the Nth order Chebyschev polynomials in order to produce all the equations which describe the Dolph-Chebyschev window for a N point transform. This was originally only a small problem since Dolph developed the window for use on phased array antenna with small numbers of elements. Current use of the window with discrete Fourier transforms of large numbers of points requires a massive mount of calculations just to compute the window function. Simplification have

been made to Dolph's original equations describing the window function [16]. Using these simpified equations, the window function is much easier to compute, but it is still very cumbersome for long transform lengths. Because of the complexity of the Dolph-Chebyschev window, no equations will be presented describing either the window or its bandpass characteristics.

A second problem with the Dolph-Chebyschev window is its constant sidelobe height. This is illustrated in Figure A-4 which presents the bandpass characteristics of the window. The window lowers the first sidelobe at the cost of raising latter ones. Because of this, the lower side lobe levels of the Dolph-Chebyschev window do not necessarily guarantee that less energy is contained in the sum of all the side lobes. Reduction of the energy contained in the sidelobes is a better indicator of a higher dynamic range ratio. Unfortunately, no closed form solution for a window possessing minimum energy in its sidelobes has yet been found.[11]

The Dolph-Chebyschev window does produce a significantly lower sidelobe level for a given main lobe width. If the main lobe width is set to be the same as that of the Hanning window, the highest sidelobe is reduced by 16dB. A deeper study is necessary in order to determine whether this lower sidelobe level is a true indicator of an improved dynamic range.

Conclusions

The effects of the choice of a window function on the performance of the chirp Z-transform is quite significant. The most significant trade off between the window functons seems to be main lobe width

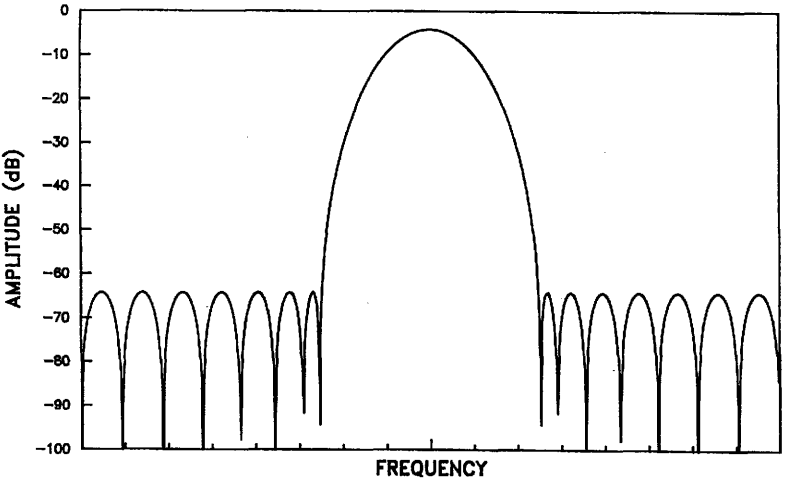


Figure A-4 Bandpass Characteristics of a 16-point Dolph-Chebyshev Window

(frequency resolution) and sidelobe level (dynamic range). Windows which tend to have low sidelobe levels also tend to have wide main lobes and vice-versa. One window which optimizes this trade off is the Dolph-Chebyschev window. This window, however, is very difficult to work with and is thus not very commonly used. Two other windows, the rectangular window and the Hanning window, are not optimal but are commonly used due to their simplicity.

APPENDIX B

CCD TRANSVERSAL FILTERS

The purpose of this appendix is to describe the history and theory of operations of charge coupled devices and to analyze their use as transversal filters. This information is presented to give a deeper understanding of the concepts on which CCD technology is based and how such a device can be used to implement a transversal filter.

History of Charge Coupled Devices

The concept of charge coupled semiconductor devices was first presented in 1970 by W. S. Boyle and G. E. Smith of Bell Laboratories.[12] They proposed that small packets of charge could be stored and moved about in MOS capacitors on the surface of a semiconductor device. Stored charge packets were in the form of minority carriers held in potential wells. These packets then could be moved about by moving the potential wells using the upper electrodes (or gates) of the MOS capacitors. Storage times were anticipated to be limited to a few seconds because of the thermally generated dark current at the semiconductor-oxide interface.[12] Maximum transfer speed and charge transfer efficiency were expected to be interrelated and mostly determined by the constant τ_0 (the time constant for transfer of charge from one potential well to another). For 0.4 mil (10μm) gate widths τ_0 was anticipated to be about 25nS.

To prove the concepts presented by Boyle and Smith, G. F. Amelio and M. F. Tompsett joined with Smith to fabricate a charge coupled device and measure its characteristics.[13] The experimental device was formed by growing 1200A thick dry oxide over a 10Ω-cm n-type <100>

oriented silicon substrate then depositing on a linear array of ten 4 mil x 4 mil (100μmx100μm) Cr-Au electrodes separated by .12mil (3μm) gaps. The device design was by no means optimal but was designed principally for easy fabrication. Testing of the device was done by avalanche injecting charge into the first electrode then shifting this charge to successive electrodes by clocking their gates. Charge transfer was monitored by observation of charge transfer to and from the substrate. A difference between the amount of charge transferred to the substrate when the gate is turned on and from the substrate when the gate is turned off represented charge retained within the device. Using this information the charge transfer efficiency of the device was calculated to be better than 98% for transfer times down to 100nS. These results showed that the charge coupled semiconductor device concept was implementable with current semiconductor technology.

Over the next two years, Tompett and several associates joined together to develop an 8 element device [17], a 96-element device[18] and a 500-element device.[19] These devices were used for a combination of applications and achieved transfer speeds up to 2MHz at 99.98% charge transfer efficiency. The 500 element device was designed for use as either a linear image sensor [19] or an analog delay line.[20] It worked well as both. This device showed that analog delay lines of substancial length were feasible.

During this time, D. R. Collins, W. H. Bailey, W. M. Gosney, and D. D. Buss at Texas Instruments, were examining the possibility of using CCD technology to implement an analog matched filter.[21] They

implemented two matched filters using the CCD as a transversal filter. Weighting and summing was achieved using a split electrode weighting scheme they developed. Their devices represented the first implementation of a CCD transversal filter.

Continued work at Texas Instruments under R. W. Brodersen, C. R. Hewes, and D. D. Buss produced a 500-stage CCD transversal filter for use in spectral filtering and Fourier analysis[6]. The device used the four-phase clocking technique and a new corner turning technique which allowed the device to be fabricated on a 180x100 mil die. The measured charge transfer efficiency for the device was 99.95% at a clock rate of 500KHz and transfer loss through the corners was estimated at about 0.5%. Overall performance of the device for Fourier analysis was very good for signal band widths up to 10MHz. The device's low power consumption and small size made it especially attractive for certain appliations. As a result, Reticon, a company in Sunnyvale, California begin manufacturing and marketing a 512 stage device based on the TI design. Unfortunately, the large amount of support circuitry for the device kept it from realizing its potential for implementing a small low power spectral analysis system.

Under a U.S. Army ERADCOM contract, R. C. Pettergill, P. W. Bosshart, M. DeWit and C. R. Hewes worked to provide an all-on-one-chip 512-stage spectral analysis IC.[22] The device was implemented on a 240x215mil NMOS IC using a $1^1/_2$ phase 3 level clocking scheme. Dynamic range of 63dB and a power consumption of 475Mw as observed at a 1MHz clock rate. To date this represents the most complex CCD transversal filter implementation.

CCD technology has grown quickly over a very short time. Many applications have been discovered for these devices ranging from optical imaging to digital memory systems. One application for CCDs is analog filtering and spectral analysis. This is achieved by using the CCD to implement a transversal filter. This is the application which will be discussed in the remainder of this appendix. Note that since CCDs are by nature basically transversal filters, the following information is helpful no matter what application the device is used in.

Principles of Operation

A transversal filter is simply a long series of delay elements whose outputs (called taps or bins) are individually weighted and summed to produce an output. Figure B-1 illustrates the block diagram of a transversal filter. This figure clearly shows that a transversal filter can be separated into two parts. The first part is the tapped delay line. Taps on the delay line are evenly spaced in time. The number of taps determines the length of the filter. The second part is the tapping/weighting/summing section. This part must non-destructively sample the tap outputs, multiply each by an independant constant, then sum them together. Both parts can be implemented using a charge coupled device.

CCD analog delay line: A charge coupled device is essentially an analog shift register. By clocking the device at a fixed rate it becomes an analog delay line. The cross-sectional view of such a device is illustrated in Figure B-2. A CCD delay line consists of three sections. These are the input, delay, and output sections. An explanation of the operation of each section follows. The delay sec

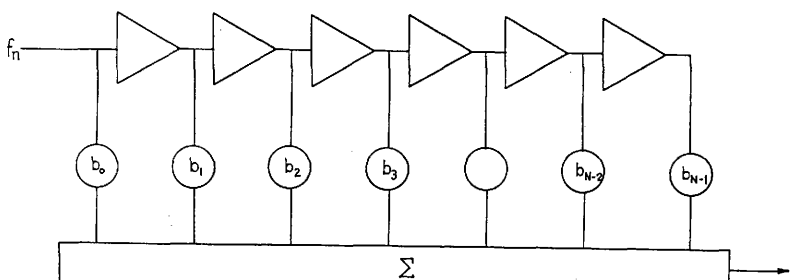


Figure B-1 Transversal Filter Block Diagram

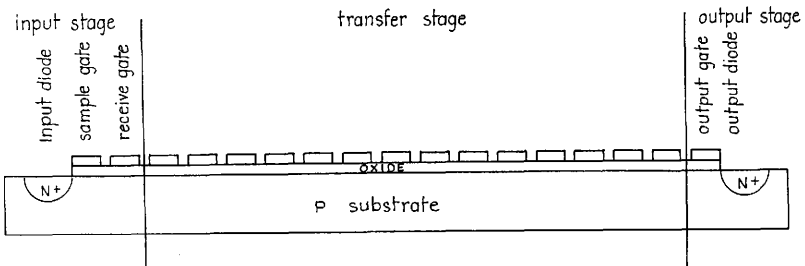


Figure B-2 CCD Delay Line Cross-sectional View

tion will be discussed first. This will make the explanation of the input stage and output stage clearer since both of these stages also contain delay elements.

Delay section: The main body of the CCD delay line is the delay section. This section holds charges packets generated by the input section and transfers them through the the device until they reach the output section. Charge is stored in this section in delay elements and transfered using one of several clocking techniques

Delay elements: The delay element is the most important item in a CCD delay line. It can be used to hold a charge packet or transfer it to an adjacent delay element by changing the potential of its upper electrode.

CCD delay elements are basically capacitors, but their special construction allows for direct charge transfer between the elements. Figure B-3 shows the 5 element cross-section of a CCD device. Note that the delay elements possess individual upper conducting electrodes and an insulator (silicon dioxide) just as capacitors do. The difference is the lower electrode. For a capacitor, the lower electrode is normally another individual conducting electrode. For a CCD device, the lower electrode is a shared doped semiconductor substrate. Because of this special lower electrode, charge packets in the form of minority carriers can be trapped in spatially defined depletion regions created by voltages applied to the upper electrodes or transferred freely to adjacent elements.

Figure B-3 shows the static state of 5 elements of an n-channel CCD device. The bulk (lower electrode) of this device has been tied

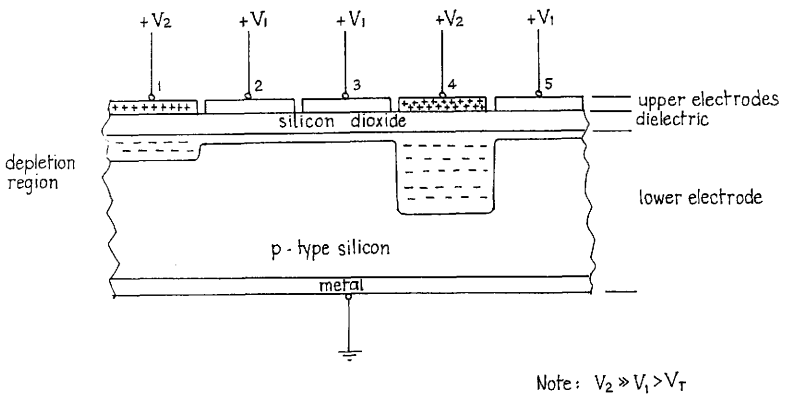
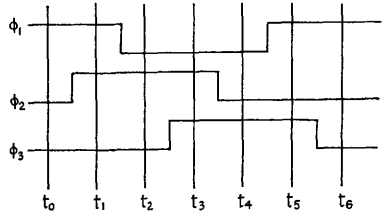


Figure B-3 5 Element Section of a CCD Delay Line

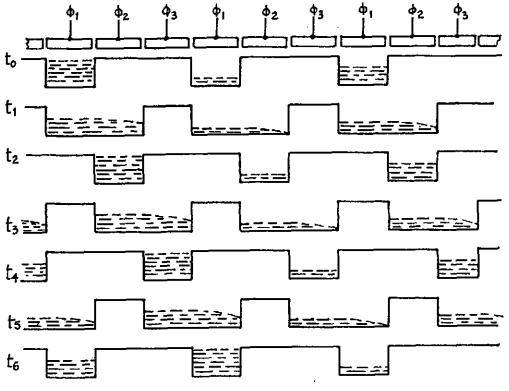
to ground and the upper electrodes of the device have been tied to a positive voltage V_1 or V_2. These voltages are chosen so that V_1 is greater than V_t (the threshold potential for production of an inversion under steady state conditions) and V_2 is much greater than V_1. This produces a potential well under the electrodes to which V_2 is attached (in this case, the first and fourth elements). Negative charge existing in the silicon substrate will congregate under these electrodes producing spatially defined depletion regions. A compensating positive charge will also flow through the gate lines to the gates to balance the negative charge packets in the substrate. These charge packets are created by input stage of the CCD device and are detected by the output stage. The size of the charge packet can be used to represent an analog data value. Charge packets can also be moved along the length of the CCD device by altering the potential of the upper electrodes of the CCD device. This caused the potential wells to move and thus the charge held in them. This altering of electrode potential is done by applying a sequence of clock waveforms to the gates of the device. A discussion of this technique follows.

Clocking techniques: Several different clocking techniques exist for transferring charge between the different delay elements. Of these techniques, three stand out as the most popular. These three techniques are: three-phase, four-phase, and $1^1/_2$ phase. These three techniques are discussed below.

Three-Phase technique: Probably the simplest clocking technique in use now is the three-phase technique. This technique is illustrated in Figure B-4. This figure shows the clock



a) Clock Waveforms



b) Charge Transfer

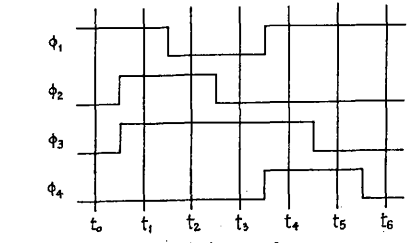
Figure B-4 Three-Phase CCD Clocking Technique

waveforms required, the lay-out of electrodes, and the motion of charge under these electrodes as the clock waveforms are sequenced. A full charge transfer sequence requires six states (t_0 through t_5). Thus, after t_5, the sequence begins again at t_0 (t_6 in the figure). Note that the state of the CCD channel is the same in t_6 as it was in t_0 except that the change has been shifted three elements down the delay line. This transfer of charge down the CCD delay line is caused by the alteration of the 6 CCD channel states between storage states (t_0, t_2, t_4) and transfer states (t_1, t_3, t_5). In a storage state, t_0 for example, a charge packet is held under every third delay element. This means that if N values are to be held in a three-phase CCD delay line, 3N delay elements will be required. Though it seems inefficient, charge packets cannot be placed at closer intervals and still be transfered using a three-phase clock. The reason for this can be seen by examining the other CCD channel state, the transfer state. During a transfer state, t_1 for example, two electrodes must be on (the source and destination) and a third electrode to be off to block transfer of charge to the next packet. Without this third electrode, all of the charge packets would be mixed during the transfer phase instead of remaining independent. Three-phase clocking was the clocking technique proposed in Smith and Boyle's original article on Charge Coupled Devices.[12]

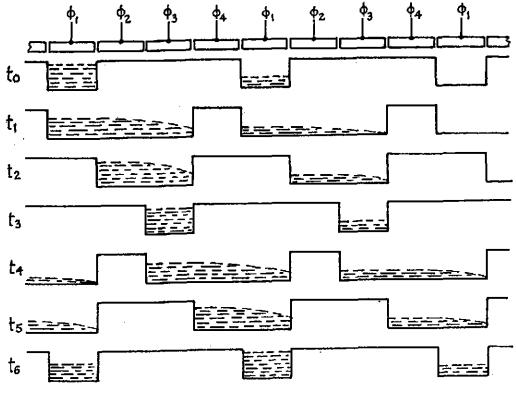
Four-phase technique: Another clocking technique is the four-phase technique. This technique is the very similar to the three-phase technique. A full charge transfer sequence requires six states (t_0 through t_5). This is the same number of states

required in the three-phase technique. These states as in the three phase technique, are divided into storage states and transfer states. These states do not alternate one for one between storage and transfer states as occured in the three-phase technique. Instead, two transfer states are required between each storage state. Figure B-5 illustrates this technique.

Since there are two transfer states for every storage state we shall divide the six states into storage states (t_0 and t_3), primary transfer states (t_1 and t_4) and secondary transfer states (t_2 and t_5). At first it appears from Figure B-5 that the secondary transfer states are not altogether necessary. These states are necessary for two reasons. First, the inclusion of the secondary transfer states increase charge transfer between ϕ_1 and ϕ_3 electrodes. Secondary transfer states break the long transfers into two adjacent transfers. A second reason for the secondary transfer state is to prevent charge from being "trapped" under the ϕ_1 or the ϕ_3 electrodes during a transfer. If no secondary transfer state is included, clock phases ϕ_1 and ϕ_2 in addition to ϕ_3 and ϕ_4 must fall together. If ϕ_2 or ϕ_4 fall first charge will be trapped, often causing it to transfer backward through the delay line. "Trapping" can also be caused by the ϕ_2 and ϕ_4 electrodes having lower gate capacitance than ϕ_1 and ϕ_3 electodes. Though the four-phase technique seems quite inefficient, it is very commonly used for implementing transversal filters with complex coefficients. This is becasue of two reasons. First, the two storage states can be effectivly used for the dual wieghting required for complex weighting coefficients. Second, the even number of clock phases allow for easier construction using alternating overlapped aluminum



a) Clock Waveforms



b) Charge Transfer

Figure B-5 Four-Phase CCD Clocking Technique

and polysilicon gates.

One and one-half phase technique: A third clocking technique is the one and one-half phase technique. This technique uses a different approach to prevent charge packets from transferring backwards along the delay line. Both the three phase and four-phase prevent reverse charge transfer by always keeping at least one clock phase turned off at all times. This produces a moving barrier which separates the charge packets from each other. The approach used in the one and one-half phase technique is to implant a p^+ doped region under the leading edge of each of the clock electrodes. The p^+ doped regions act like a one-way door for charge transfer by allowing charge to pass through the region but not allowing it to be held there. Figure B-6 illustrates the clock waveforms, physical layout and charge transfer flow under the electrodes.

Several differences exist between a one and one-half phase CCD device and the three-phase and four-phase devices discussed previously. One major difference is the clock waveform. For the three-phase and four-phase CCD devices, though the clock waveforms were different in shape and number, all were bi-level waveforms (the waveform amplitude only took on one of two distinct levels). The clock waveforms for a one and one-half phase device consists of a uni-level waveform and a tri-level waveform. Because a uni-level waveform only has one allowable amplitude it does not change over with time and is thus usually not considered a clock waveform but rather a fixed dc level. For CCD devices, however, the signals attached to the gates are designated as clock phases even if they are a dc level. For the

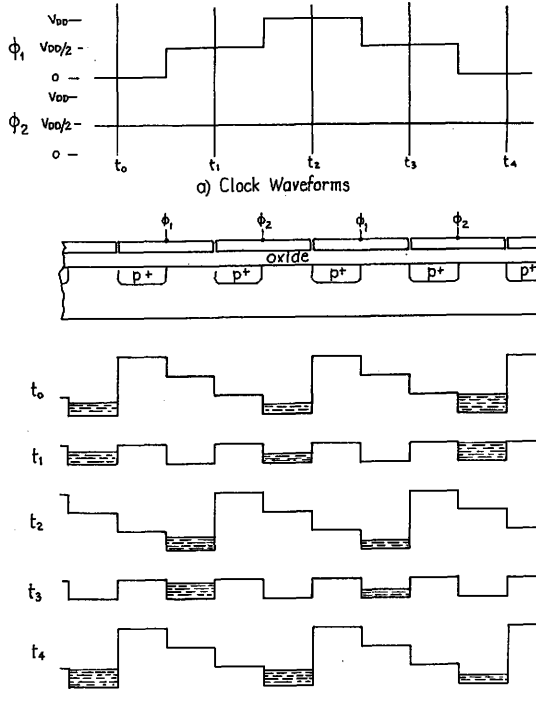


Figure B-6 1½-Phase CCD Clocking Technique

one and one-half phase CCD clocking technique the first phase is the tri-level waveform and the second (one-half phase) is the the uni-level waveform.

Input Section: The first stage of a CCD device is the input stage. This stage produces the charge packets which are shifted by the delay section and received by the output stage. Two injection mechanisms have been used for introducing charge packets into a CCD device. These are breakdown and source injection.

Injection of charge using non-destructive insulation breakdown was the first mechanism used with a CCD device. This mechanism was used for the first experimental verification of the Charge Coupled Device concept in 1970[12]. Charge was injected through a MOS gate by pulsing the gate with a narrow (60nS), high voltage (200V) signal. This non-destructively broke down the oxide layer under the gate and injected a charge packet into the substrate below. Though the mechanism worked, it wasn't very practical and is rarely used.

Another injection mechanism is source injection. This mechanism uses a diode and an input gate to form the source and gate of a MOS transistor. Using this technique, charge is injected into the substrate through the diode junction past the input gate and to the receiving gate. The amplitude of the charge packet is controlled by the difference between the input gate and diode potential (the transistors Vgs) and the available injection time. The size of the injected charge packet is defined by the MOS transistor equation by letting V_{IG} be the input voltage. V_{ID} is the voltage of the input diode, and τ be the total injection time. From this we get

$$Q = \left[\left(\frac{\mu C_{ox} W_I}{2L_I} \right) (V_{IG} - V_{ID} - V_T)^2 \right] \tau \qquad (B.1)$$

where μ is the carrier mobility in $cm^2/V\text{-}S$, C_{ox} is the oxide capacitance in pF/cm^2, W_I and L_I are the width and length of the input gate, V_T is the threshold voltage of the gate, and Q is the injected charge packet amplitude in pC. Note that this equation only applies as long as there is room enough for the delivered charge-packet Q at the receiving gate (the gate following the input gate). Since the receiving gate is basically functioning like a capacitor, the amount of charge it can hold is determined by the product of its voltage V_{RG}, gate area, and oxide capacitance. Thus,

$$Q_{max} = C_{ox} W_R L_R V_{RG}. \qquad (B.2)$$

This should be easily achieveable if τ is kept small.

One important feature of source injection is its versatility. From equation B.1 note that the squared term affords the input signal to be placed on either the input gate or input diode with equal result. Also, the injection time τ can be controlled in a variety of ways. One method is by pulsing either the input diode or input gate (which ever one is not being used for the input signal amplitude). Another method of controlling τ is by pulsing the receive gate to allow only a limited time to fill. A third method is by adding a gate between the input diode and input gate to selectively cut off the flow of charge. Different combinations of each of these options produces a

variety of different techniques by which the source injection can be used to inject charge into the channel of a CCD device. Three such techniques are Dynamic Injection, Diode Cutoff, and Potential Equilibrium[23].

Dynamic Injection: Probably the simplest source injection technique is Dynamic Injection. Figure B-7 illustrates this technique. The technique utilizes an input diode and a single input gate, The input signal is attached to the input diode and the gate V_{GG}. The sampling operating is performed by the first delay gate ϕ_1; thus the total injection time τ is determined by the pulse width of ϕ_1. From this information the relationship between the input signal amplitude V; and the charge packet amplitude Q using equation B.1. The relationship is

$$Q = \left[\left(\frac{\mu C_{ox} W_I}{2L_I} \right) (V_i - (V_{GG} - V_T))^2 \right] \tau \qquad (B.3)$$

Though the Dynamic Injection technique has the advantage of simplicity it also has three main disadvantages.

The first major disadvantage of the Dynamic Injection technique is clock dependance. Clock dependancy is caused by the use of the first transfer electrode to perform the input sampling operating. This means that the total charge injection time τ is determined by the pulse width of ϕ_1. Since ϕ_1 varies with the system sampling rate, the gain of the input stage will change. This not often acceptable because most systems utilizing CCD devices must be able to function at a wide range of different sampling rates.

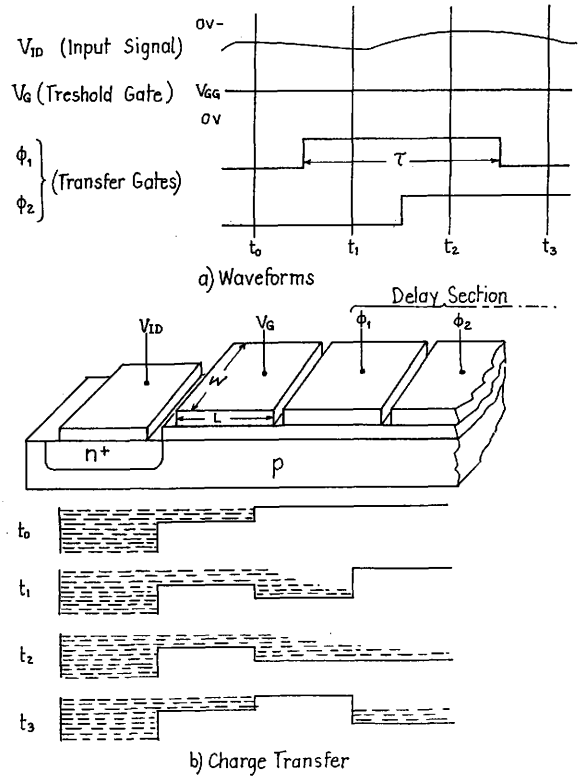


Figure B-7 Dynamic Injection Charge Introduction Technique

The second major disadvantage of the Dynamic Injection technique is a problem which occurs called reverse transfer leakage. This is caused by the fact that charge is still under the first transfer gate when it is tuned off during t_3 (see Figure B-7b). When this occurs, charge not only transfers towards the first transfer gate but also back towards the input diode. The percentage of charge transferring in each direction is dependant on the potentials of the three gates, the potential of the input diode, the clock waveshape and timing and the carrier transit time. The amount of reverse transfer leakage is thus very difficult to determine or control, resulting usually in the addition of noise into the size of the individual charge packets.

The third major disadvantage of the Dynamic Injection technique is its nonlinearity. This can be seen from a equation B.3. For CCD devices to be used in analog applications, the device usually must be linear. To alleviate the problem the device is biased up to the more linear region of the characteristic curve. This is done by limiting the V_i to small deviations and making V_{GG} as large as possible. If we assume tht $V_{GG} - V_T >> V_i > 0$ then equation B.3 becomes

$$Q \approx \left[\left(\frac{\mu C_{ox} W_I}{2L_I} \right) (V_{GG} - V_T)^2 - 2(V_{GG} - V_T)\, V_i \right] \tau. \qquad (B.4)$$

This equation in linear with respect to V_i.

Diode Cutoff: Another source injection technique is the Diode Cutoff technique. This technique alleviates the clock

dependency problem of the Dynamic Injection Technique by introducing a sampling gate as shown in Figure B-8. This additional gate causes the total injection time to be dependent on a new signal ϕ_S. Because ϕ_S is not used for the transfer of charge in the main CCD delay section, its pulse width can be held fixed for all system sampling rates. Note that the relationship between the input signal amplitude and charge packet amplitude is still the same as expressed by equation B.2 exept that τ now refers to the pulse width of ϕ_S instead of ϕ_1. Though the Diode Cutoff technique does eliminate the clock dependency problem of the Dynamic Injection technique, it still exhibits the same problem with reverse charge leakage and non-linearity.

Potential Equilibrium: The Potential Equalibrium technique for source injection is considerably different from the previous two techniques. In this technique, the input is applied to the gate rather than the input diode. This allows the input diode to be pulsed to perform the sampling operation. By pulsing the input diode rather than the gate the reverse charge leakeage problem can be eliminated. Figure A-9 illustrates the Potential Equilibrium source injection technique. Note that after the input diode is pulsed on, it is reverse biased to drain off any free charge left under the input gate.

Another advantage of the Potential Equilibrium technique is its linearity. Unlike the other two source injection techniques, the Potential Equilibrium technique relies on the filling of the receive gate and the draining off of excess charge not held back by the input gate. This allows the relationship between the input voltage amplitude and the injected charge amplitude to be determined by the gate charge capacity (equation B.2) rather than the product of the charge

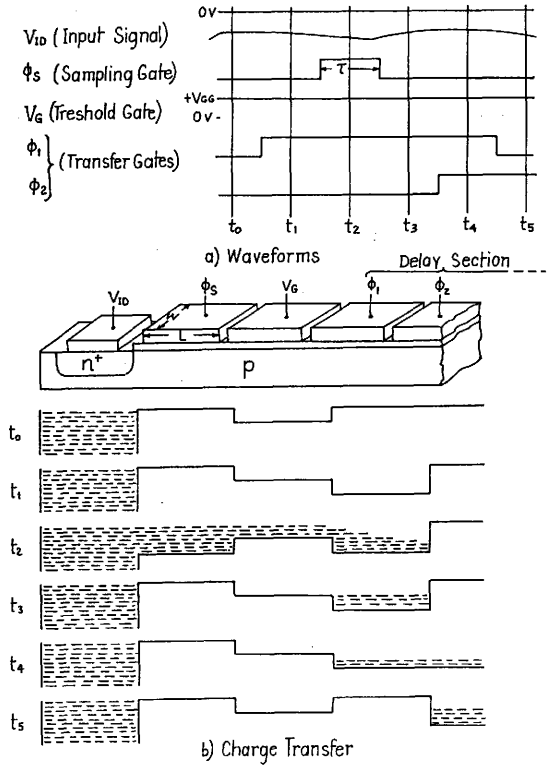


Figure B-8 Diode Cutoff Charge Introduction Technique

injection speed and the charge injection time (equation B.1). Note that equation B.2 is linear with respect to V_G where equation B.1 is not. Also, note that the other two source injection techniques can not make use of the mechanism described above since they attach the input signal to the input diode rather than the input gate. Equation B.2 is independent of the input diode voltage.

The equation which relates the input voltage and injected charge amplitude is easily derived. As mentioned above, this relationship is based on equation B.2. Note also, that equation B.1 must also be used to assure that the times τ_f and τ_r shown in Figure B-9 are sufficiently long to assure that equation B.2 remains valid. Two steps are involved in the charge injection. These are charge filling (t_2) and charge removal (t_3). Each step has is own set of determining equations.

During the charge filling step the receive gate is filled to a level which much exceed the height of the input gate. From equation B.2 the total amount of charge which can be held under the receive gate is

$$Q_{R_{max}} = C_{ox} W_R L_R V_{RG}. \tag{B.5}$$

If we subtract from this the amount of charge held above the potential of the receive gate the equation

$$Q_{R_{min}} = C_{oc} W_R L_R (V_{RG} - V_G) \tag{B.6}$$

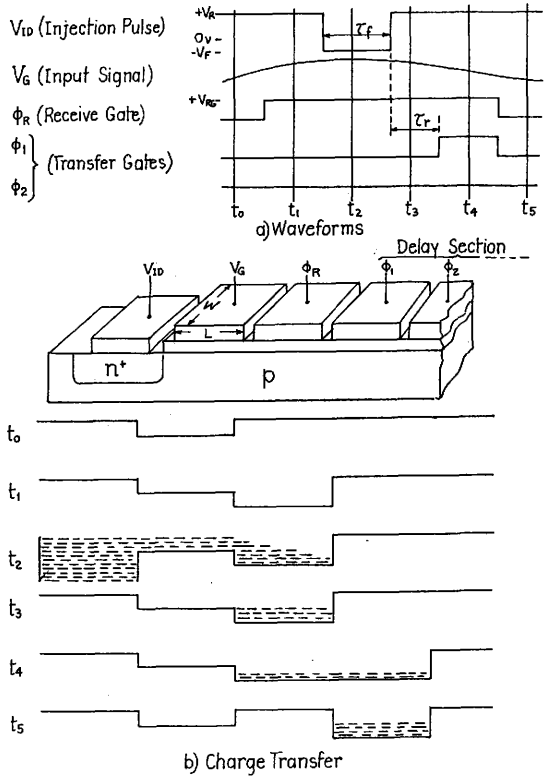


Figure B-9 Potential Equilibrium Charge Introduction Technique

is obtained. Since this is the minimum amount of charge required to be delivered to the receive gate during the charge filling step, the minimum filling time τ_f can be determined from equation B.1

$$\left[\left(\frac{\mu C_{ox} W_I}{2L_I}\right)(V_G - (-V_f) - V_T)^2\right]\tau_f > C_{ox} W_R L_R (V_{RG} - V_G) \qquad (B.7)$$

Noting that $W_I = W_R$ and rearranging terms we get

$$\tau_f > \left(\frac{2L_I L_R}{\mu}\right)\left(\frac{V_{RG} - V_G}{((V_G - V_T) + V_f)^2}\right) \qquad (B.8)$$

For a worst case input voltage of $V_G = 0$ this becomes

$$\tau_f > \left(\frac{2L_I L_R}{\mu}\right)\left(\frac{V_{RG}}{(V_f - V_T)^2}\right) \qquad (B.9)$$

By maintaining a high input diode forward bias voltage and designing in short gates, charge filling times can be easily kept under 100psec. For transversal filters designed to run at clock rates below 1MHz the charge filling time should not pose a problem, for higher clock rates the filling time could be a limiting factor. Note that for τ_f times which exceed the minimum filling time, overfilling of the receive gate will occur. This cannot be avoided since the minimum filling time is dependant on the input voltage V_G whereas τ_f is held fixed. Thus

if τ_f is made long enough to prevent underfilling at minimum V_G, overfilling will occur at maximum V_G. To remove overfilled charge, a second step is required called charge removal.

During the charge removal step, the input diode is reverse biased to remove all charge at the receive gate which is at a higher potential than the input gate. This is the amount of charge which was delivered which was in excess of the minimum receive charge defined by equation B.6. The time required for this charge removal should not be a problem. As long as V_r is larger than V_f and τ_r is at least as big as τ_f then sufficient time will exist for charge removal.

If both τ_f and τ_r are sufficiently long to allow complete charge filling and removal, the relationship between the charge delivered to the receive gate (Q) and the input signal voltage (V_i) is defined from equation B.6 as

$$Q = C_{ox} W_R L_R (V_{RG}-V_i). \tag{B.10}$$

Note that because Q refers to the charge amplitude rather than its polarity, Q must remain positive. Also, note that since V_i is applied to a gate it must always be held at a potential higher than the threshold voltage V_t for a depletion range to form under it. From these two relationships, the following limitation on the input voltage V_i is determined.

$$V_T < V_i < V_{RG} \tag{B.11}$$

This relationship must be satisfied for equation B.10 to be valid.

Of all the charge injection mechanisms, source injection of charge by the Dynamic Equalibrium technique appears to be the best. This technique is linear and does not suffer from clock timing dependency or reverse charge transfer loss. The technique does have a problem. This problem can be seen from equation B.10. Note from this equation that the potential of the receive gate can also funtion as a input signal. Any fluctuations of this gate level or any noise present on the gate line will be directly coupled into the system. For this reason, the receive gate clock line should be carefuly isolated and filtered if the Potential Equilibrium technique is used.

Output Section: The final stage of a CCD device is the output stage. This section transfers charge packets passed to it from the last element of the delay section to a charge detection circuit where the charge amplitude is converted to a voltage. Like the CCD input section, the output section is composed of a gate and a diode. The arrangement is illustrated in Figure B.2.

The mechanism by which the output stage extracts charge from the CCD device is very similar to the source injection mechanism used by the input stage to introduce charge into the CCD. Jut like the input stage, the output stage consists of a gate and diode. For the input stage these transform the gate and source of a MOS transistor. For the output stage, they form the gate and drain of a MOS transistor. In fact, the entire CCD device can be though of one long multi-gate MOS transistor with its source in the input section and its drain in the output section. Just as in a MOS transistor, charge enters the device through the source and exits through the drain. Note that the

clocking technique of a CCD allows only small incremental charge packets to leave the output stage as opposed to the continuous charge flow that is usually associated with operation of a MOS transistor. This can make the detection of the CCD charge output difficult.

Tapping/Weighting/Summing: The second major part of a transversal is responsible for non-destructively sampling (tapping) the contents of individual elements of the delay line, weighting these values, then summing the weighted values together to produce a single output value. This is illustrated in Figure B.1. Each operation can be performed using the CCD delay line just discussed. An explanation of how each operation is implemented follows.

Tapping: The first operation that must be implemented to allow the use of a delay line for a transversal filter is tapping. Tapping is the non-destructive measuring of the contents of the delay elements. For a CCD device, this would require that the amplitude of each charge packet within the device be measured without draining off or adding to it. One way this can be done is by measuring the amount of charge which flows to the gate which the charge packet is moved under. Figure B-10 illustrates the concept.

Initially, it is assumed that a charge packet of size Q is present under G_1. The charge is negative since charge held under a CCD substrate is in the minority of carriers (electrons for p-type doped silicon). Charge under G_i is held there by the positive potential applied to that gate. Note that the negative charge packet under G_1, will electrostatically attract an equal positive charge to G_1 through its clock line. This secondary charge packet will be trapped

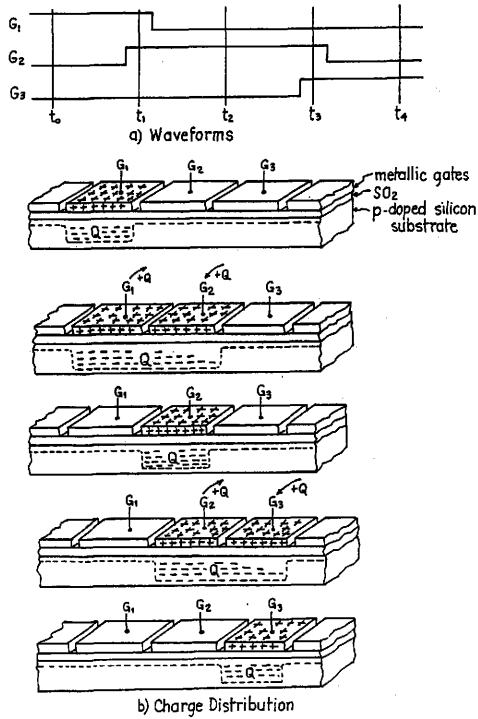


Figure B-10 -Primary and Secondary Charge Transfer in CCD

on the gate electrode since it is unable to pass through the insulating barrier under the gate to the substrate where the primary charge packet is held. Measuring the amplitude of the secondary charge packet provides an effective way of determining the contents of the CCD delay elements without effecting their value.

Measuring the size of the charge packets which reside on a gates of a CCD is easier than measuring the size of the charge packets which reside within the substrate of the CCD. The charge packets residing on the gates are isolated from each other and can be accessed directly through the individual lines which lead to them. This is not true for the charge packets within the substrate. These charge packets are not entirely isolated from each other, (if they were then they would not be able to be move through the device) nor are they accessable through individual lines. Measurement of the charge on the gates is easier, but measuring any absolute charge amplitude is difficult no matter where it resides.

Another alternative to measuring the absolute magnitude of the charge residing on the gate is to monitor the motion of charge to and from it. Note that charge motion to and from the gate will be observed a current flow through the gate clock line. This current can easily be measured by a variety of methods. One method is to place a capacitor in series with clock line of each gate. Charge passing "through" the capacitor will produce a voltage difference across the capacitor. The amount of charge passing to and from the gate can be determined by monitoring the voltage across the capacitor. Figure B-10 illustrates the motion of charge to and from the CCD gates as a

charge packet moves beneath them. Note tht gates adjacent to a charge packet are held at zero potential and hence have no charge beneath them. Because of this, the entire charge packet will transfer back and forth through the clock lines. This means that the relative charge motion actually represents the entire charge packet size. Tapping the contents of the elements of a CCD can be accomplished by measuring the charge transferring to and from its gates.

Weighting: Another operation required to implement a transversal filter is weighting of the tap values. Weighting is simply the scaling of each tap value by an independent constant. Weight values need only cover the range from plus unity through zero to minus unity. This is because the importance of weighting is the ratio of the tap to tap values. Any overall gain required can be affected at a later stage.

For a CCD, the most common technique for performing weighting is split-electrode weighting. This technique is illustrated in Figure B-11. Tapping of the delay element values is performed by measuring charge flowing to the CCD gates as just discussed. By splitting the gate electrode into two pieces (see figure), the charge packet can be divided up. By holding the clock line for each gate section (ϕ+ and ϕ-) at the same potential the charge under the entire gate area should be relatively uniform. Thus, the charge under each gate section should be proportionate in the area of that gate section. That is,

$$Q^{+} = [Q/(LW)]\,[W^{+}L] = Q[W^{+}/_{W}] \qquad (B.12)$$

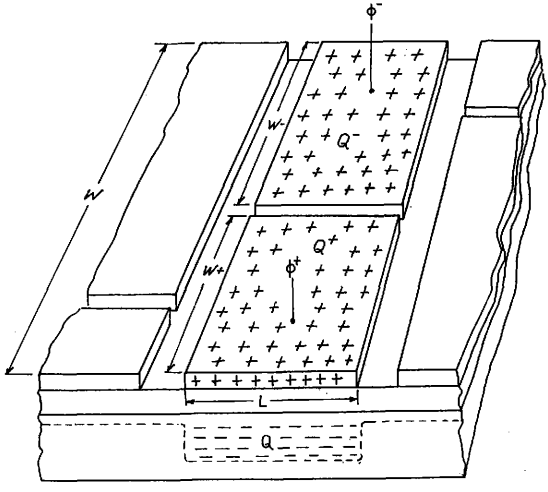


Figure B-11 Split Electrode Weighting

$$Q^- = [Q/(LW)]\,[W^-L] = Q[W^-/W] \tag{B.13}$$

These equations illustrate the split gate weighting technique where the width of the gate section (W^+ or W^-) is used to scale the charge packet amplitude Q to produce a weighted charge packet size (Q^+ or Q^-). The terms W^+/W and W^-/W are the weighting constants.

Before progressing on, it is important to note two things about the above equations. The first is that the two weighting constants W^+/W and W^-/W are not independent of each other. These constants must always sum to unity since W^+ and W^- sum to W. The second item to note about the above equations is that the weighting constants can only vary from zero to positive unity. This is a problem since most transversal filter functions are bipolar functions.

To implement a bipolar weighting function the difference is taken of the two weighted charge packets to produce a weighted charge packet Q'.

$$Q' = [Q^+ - Q^-] = Q\left[\frac{W^+ - W^-}{W}\right] = Q[2(W^+/W) - 1] \tag{B.14}$$

As W^+ varies from zero to W the value of the new weighting constant $[2(W^+/W) - 1]$ varies from minus unity to plus unity. Taking the difference of the charge flowing to the two different gate sections is more difficult than simply measuring the charge flowing through a single line but is achievable using a differential current integrator

(DCI). DCIs are discussed in the main body of this report.

Split gate weighting as described above is a simple and effective means of performing tap weighting in a CCD. Weight values range from minus unity to plus unity and are encoded in the gate mask of the CCD by setting the relative width of the two sections of each gate. The weighted contents for each gate is determined by taking the difference between the charge flowing to its two sections. To maintain the accuracy of the technique, care must be taken to assure the uniformity of the charge distribution i the CCD over the entire width of the channel. This involves care in the fabrication process and care to assure the two sections of each gate are held of precisely the same potential.

Summing: The final operating required to implement a CCD transversal filter is summing. This entails the summing together of all of the weighted tap values to form a single value. Of all of the operations so far this is probably the simplist to implement. Since the all of the weighted tap values are in the form of charge flowing along a clock line, the summation of all these values can be performed by simply tying together the clock lines for all of the gates in each section and sending these lines to a single DCI. Figure B-12 illustrates this. Note that for simplicity's sake, only the tapped gates are shown. As we noted in the earlier discussion on clocking techniques, multiple gate electrodes are required to form a single delay element. Usually only one of these gates per delay element will usually be used for tapping weighting and summing. The other electrodes are used solely for the controlling of the element-to-element

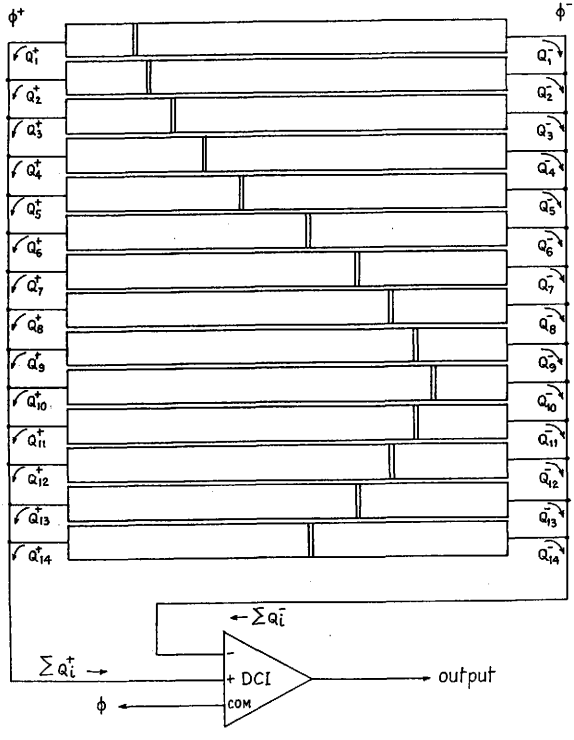


Figure B-12 Split Gate Summation

charge transfer process.

Conclusions: Current semiconductor technology allows for the implementation of a transversal filter using a charge coupled device. The device is relatively easy to implement and has the advantages of low power, small size and weight, low cost (in large volume quantities), and relatively fast clock speeds (10 MHz). A large number of prototype devices have been manufactured by a varied group of people [6],[17]-[22], but only one such device is available on the market. Note that since the weighting function of a CCD is set during the construction of the device, devices are very costly to design and fabricate for the first device, but are fairly inexpensive to produce if large quantities of the same device are needed. This often limits the number of applications in which CCD transversal filters can be used.

VITA

Mark Steven Hancock was born on November 2, 1957, in Topeka, Kansas, the son of Ret. Lt. Col. and Mrs. Kenneth J. Hancock. He received his Bachelor of Science in Electrical Engineering at Texas A&M University in May, 1979.

Mr. Hancock is currently employed as a Test Engineer at Intermedics, Inc. in Freeport, Texas. He can be reached there or at 105 Anyway #15, Lake Jackson, Texas 77566.

The principal typists for this thesis were Gloria Johnson and Christine Kapple.