DESIGN TECHNIQUES FOR LOW NOISE AND HIGH SPEED A/D CONVERTERS

A Thesis

by

AMIT KUMAR GUPTA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2006

Major Subject: Electrical Engineering

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Approved by:

Chair of Committee,	Edgar Sanchez-Sinencio
Committee Members,	Jose Silva Martinez
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ABSTRACT

Design Techniques for Low Noise and High Speed
A/D Converters. (December 2006)
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Chair of Advisory Committee: Dr. Edgar Sanchez-Sinencio

Analog-to-digital (A/D) conversion is a process that bridges the real analog world to digital signal processing. It takes a continuous-time, continuous amplitude signal as its input and outputs a discrete-time, discrete-amplitude signal. The resolution and sampling rate of an A/D converter vary depending on the application. Recently, there has been a growing demand for broadband (>1 MHz), high-resolution (>14bits) A/D converters. Applications that demand such converters include asymmetric digital subscriber line (ADSL) modems, cellular systems, high accuracy instrumentation, and medical imaging systems. This thesis suggests some design techniques for such high resolution and high sampling rate A/D converters.

As the A/D converter performance keeps on increasing it becomes increasingly difficult for the input driver to settle to required accuracy within the sampling time. This is because of the use of larger sampling capacitor (increased resolution) and a decrease in sampling time (higher speed). So there is an increasing trend to have a driver integrated on-chip along with A/D converter. The first contribution of this thesis is to present a new precharge scheme which enables integrating the input buffer with A/D converter in standard CMOS process. The buffer also uses a novel multi-path common mode feedback scheme to stabilize the common mode loop at high speeds.

Another major problem in achieving very high Signal to Noise and Distortion Ratio (SNDR) is the capacitor mismatch in Digital to Analog Converters (DAC) inherent in the A/D converters. The mismatch between the capacitor causes harmonic distortion, which may not be acceptable. The analysis of Dynamic Element Matching (DEM) technique as

applicable to broadband data-converters is presented and a novel second order notch-DEM is introduced. In this thesis we present a method to calibrate the DAC. We also show that a combination of digital error correction and dynamic element matching is optimal in terms of test time or calibration time.

Even if we are using dynamic element matching techniques, it is still critical to get the best matching of unit elements possible in a given technology. The matching obtained may be limited either by random variations in the unit capacitor or by gradient effects. In this thesis we present layout techniques for capacitor arrays, and the matching results obtained in measurement from a test-chip are presented.

Thus we present various design techniques for high speed and low noise A/D converters in this thesis. The techniques described are quite general and can be applied to most of the types of A/D converters.

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CHAPTER I

INTRODUCTION

1.1 Motivation

The increasing digitization in all spheres of electronics applications, from telecommunications systems to consumer electronics appliances, requires analog-to-digital converters (ADC's) with a higher sampling rate, higher resolution and low power consumption. There is also an increasing trend to reduce the system complexity by improving the dynamic range of A/D converter. For example the variable gain amplifier in front of the ADC can be eliminated if A/D converter used has sufficient dynamic range. The first generation of broadband ADC's (>1Mhz) bandwidth were pipelined ADC's, but there resolution was limited to 14 bits. High-resolution sigma-delta ADC's were generally designed for audio applications, dc testing and industrial applications with bandwidth < 100khz. Similarly high-resolution successive approximation ADC's had bandwidth in hundred's of kilohertz. With the growing demand of high resolution broadband ADC's, sigma-delta and SAR ADC's have been designed with bandwidths in excess of 1Mhz, and the envelope is getting stretched very fast. In this thesis we look at design techniques to design high resolution (>14 bit) and high bandwidth (>1Mhz) ADC's. The applications of such ADC's include wired and wireless communication systems, ADSL (Asymmetric Digital Subscriber Loop) modems, medical instrumentation such as CT scanner and MRI, vibration analysis, automatic test equipments, military SONAR (Sound Navigation and Ranging), high resolution scanners and spectrum analyzers.

1.2 Goals and achievement of the research

This research seeks to investigate techniques for design of high resolution broadband ADC's. Though the focus is on design of broadband sigma-delta ADC's, many of design techniques discussed are also applicable to other ADC types. While designing analog circuits, there are always a number of design tradeoffs to be made. There is always a

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This thesis follows the style and format of *IEEE Journal of Solid-State Circuits*.

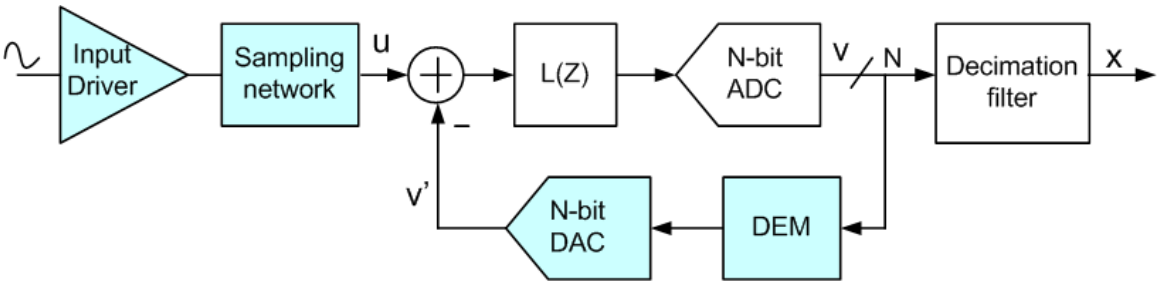


Fig 1.1. Block diagram of a typical oversampling ADC

trade-off between signal to noise ratio (SNR) and the spurious free dynamic range (SFDR). In this thesis we illustrate how this trade-off affects the design of input driver, the sampling network and the dynamic element-matching algorithm. We also studied various circuit techniques and analyzed the limits of performance that can be achieved with existing solutions and proposed new solutions where applicable. The block diagram of a typical sigma-delta ADC is shown in Fig 1.1. This works focuses on the highlighted blocks in the ADC. It is to be noted that though the quantizer (N-bit ADC) may be of low resolution, all the highlighted blocks need linearity commensurate with the overall linearity of the converter. Specific contributions of this thesis include

- Pre-charge scheme for input sampling network [1]: As the sampling capacitor size increases and sampling time reduces it becomes increasingly difficult for the input driver to settle to within required limits, thus limiting SFDR. The proposed pre-charge scheme relaxes the settling requirement of the driver; this leads to the reduced power consumption in input driver.
- A Multi-path common mode feedback scheme for the input driver [2], [3]: The bandwidth of the input driver has to increase in proportion to the increase in sampling rate. For high speed ADC's the input driver with bandwidths in excess of 100Mhz are commonplace. It is extremely difficult to stabilize the common mode feedback (CMFB) loop in such drivers. There is an additional problem of latching during power up if the driver has two-stages. The proposed method avoids the latch up problem and improves the stability of CMFB loop.

- A novel second order Dynamic element matching (DEM) technique is proposed for low over sampling sigma delta ADC's [4].
- A novel method to digitally calibrate DAC mismatch errors is presented. It is shown that a combination of digital calibration and DEM is optimal is terms of test/calibration time.
- The layout of capacitor array is very critical for DAC linearity. Various capacitor array layout techniques were studied and mismatch results were measured from a prototype test-chip.
- A state space approach to design of continuous time modulator (CTM) with delay in feedback path is developed [5]

1.3 Thesis organization

Chapter II looks at some applications of high-resolution broadband A/D converters. Chapter III discusses the design techniques for input drivers. Chapter IV presents various sample and hold design techniques. Chapter V reviews existing dynamic element matching techniques and presents an improved second order dynamic element matching technique. Chapter VI discusses digital correction techniques for A/D converters and proposes a new method to determine the calibration coefficient. Chapter VII studies the mismatch in capacitor array and presents the measurement results from a prototype test-chip. Chapter VIII presents a state space approach to design of continuous time sigma delta modulators with delay in feedback path.

CHAPTER II

APPLICATIONS OF BROADBAND HIGH RESOLUTION A/D CONVERTERS

In this chapter we look at some of the applications of broadband high-resolution A/D converters (resolution > 14bit, Bandwidth > 1Mhz).

2.1 Asymmetric Digital Subscriber Line (ADSL)

ADSL is a form of DSL (digital subscriber loop) a data communications technology that enables faster data transmission over copper telephone lines than a conventional modem can provide. The distinguishing characteristic of ADSL over xDSL is that the volume of data flow is greater in one direction than the other, i.e. it is asymmetric. Providers usually market ADSL as a service for people to connect to the internet in a relatively passive mode: able to use the higher speed direction for the "download" from the Internet but not needing to run servers that would require bandwidth in the other direction. The major advantage of high-speed ADSL services is that they can utilize the infrastructure of ordinary copper telephone wires, which are already installed in most commercial and residential buildings, for data transmission at a high or medium rate. Possible or emerging applications, which may take advantage of the high bandwidth of ADSL technology include video on demand, video conferencing, multi-media, distance learning and online services [6].

2.1.1 ADSL system architecture

As illustrated in Fig. 2.1, ADSL is a point-to-point data transmission scheme over the existing twisted-pair copper telephone wires between the ADSL service subscriber and the ADSL service provider's central office. The central office is connected to Internet. ADSL service is operated in conjunction with existing plain old telephone service (POTS). Discrete multi-tone modulation scheme has been chosen in ANSI T1.413 standard [7] for ADSL. With DMT, coding the frequency band from dc to 1.104 MHz is divided into 256 sub-channels equally spaced, each with 4.3125Khz bandwidth. The low

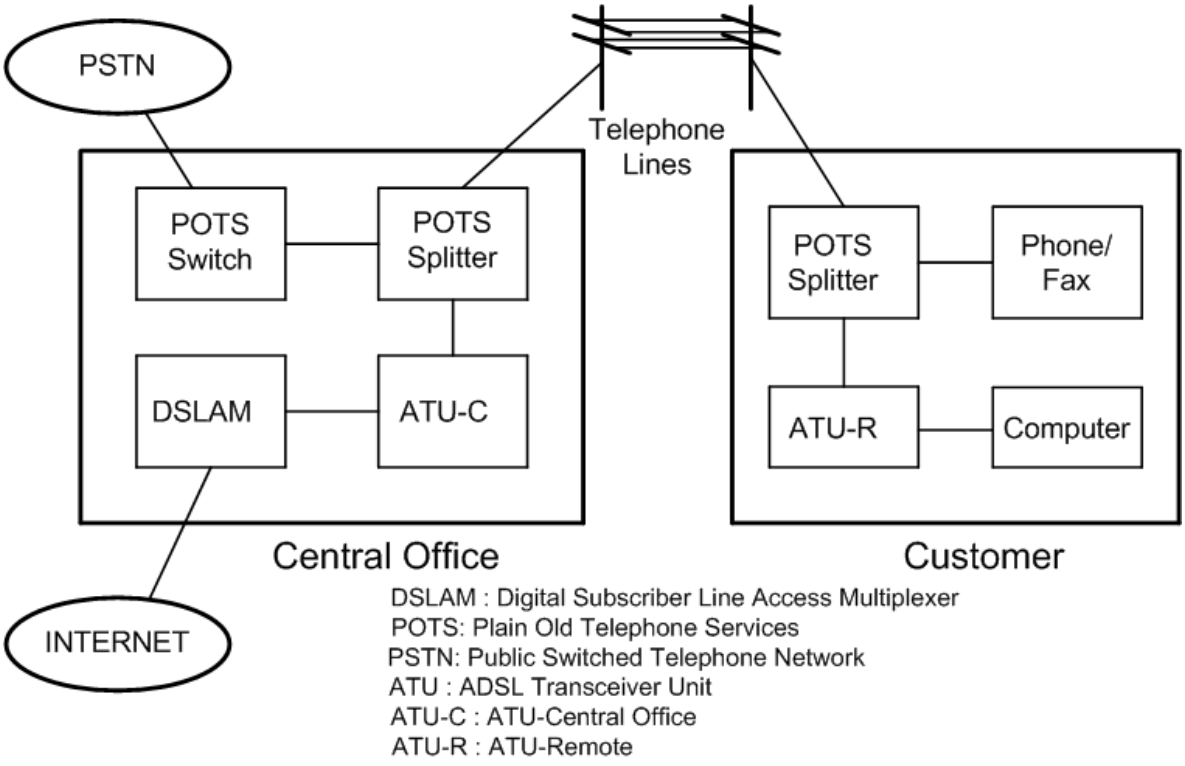


Fig. 2.1. ADSL system architecture

part of the frequency band is assigned to POTS services, while ADSL transmission utilizes higher frequency band. The frequency plan for ADSL is shown in Fig 2.2.With standard ADSL the band from 25.875 kHz to 138 kHz is used for upstream communication, while 138 kHz – 1104 kHz is used for downstream communication.

POTS signal and ADSL signal are separated and combined by the POTS splitters, one at the central office and one at ADSL service user (or subscriber)'s side. POTS splitter, which is bidirectional device, includes a low pass filter for POTS services and a high pass filter for the ADSL. It splits the incoming combined signal into POTS signal and ADSL signal. At the central office side, the low-passed POTS signal is forwarded to the POTS switch, which is connected to the Public switched telephone network (PSTN). While at the subscriber's side, the POTS signal is fed into telephone lines or fax machines. The high pass signal contains the ADSL information and is transferred to the

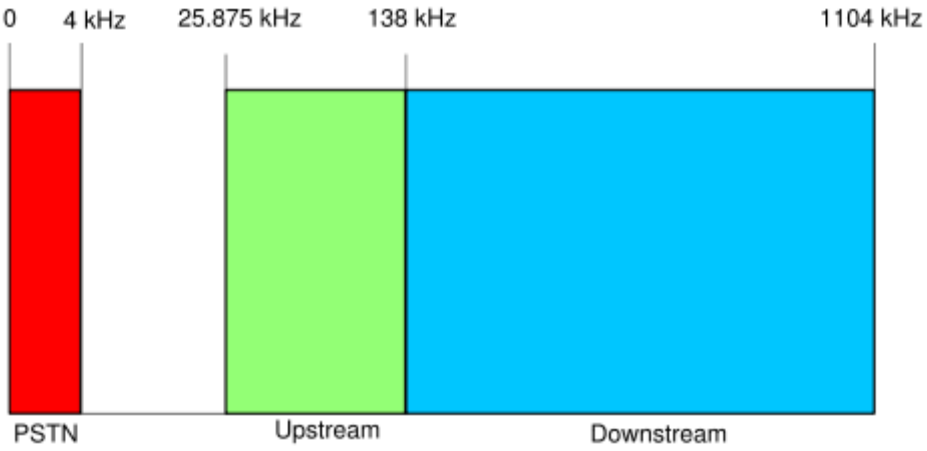


Fig. 2.2. Frequency plan for ADSL

ADSL modem or transceiver unit (ATU's). One ATU, ATU-R (ATU remote), resides in subscriber's home; while another ATU-C (ATU central office), resides in the central office. The POTS splitter also combines the POTS signal and ADSL signal to form the outgoing duplexed signal. Digital Subscriber Line Access Multiplexer (DSLAM), which is connected to the Internet, collects and combines ADSL signals from different subscribers in the vicinity at central office. Through DSLAM, the ADSL user can exchange information with Internet.

For conventional ADSL, downstream rates start at 256 kbits/s and typically reach 8 Mbits/s within 1.5 km (5000 ft) of the DSLAM equipped central office or remote terminal. Upstream rates start at 64 kbits/s and typically reach 256 kbits/s but can go as high as 1024 kbits/s.

2.1.2 A/D converter specifications

The block diagram of a typical ADSL receiver is shown in Fig 2.3. It consists of one or more AGC amplifiers controlled by DSP software, an analog low pass filter and an analog-to digital converter, the output of which is sent to DSP for further post processing such as digital low-pass filtering and demodulation. The bandwidth and dynamic range requirements for A/D converter are set forth in this section.

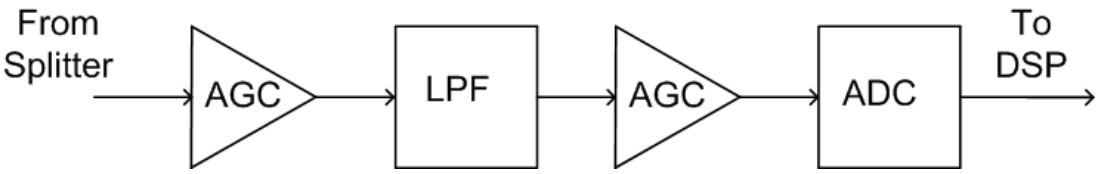


Fig. 2.3. ADSL receiver

It follows from the ADSL signal spectra shown in Fig 2.2 that a baseband A/D converter with a minimum conversion rate of 2.2Mhz for the downstream data and 276 Khz for the upstream data is needed to avoid aliasing of images into the signal band upon sampling. Theoretically the A/D converter at the central office can therefore be operated at a considerably lower speed than its counterpart at the remote user. However, to avoid the echo of transmitted downstream signal from being aliased into the signal band of interest at receiver, the A/D converter at the central office typically operates at sampling rates comparable to those at remote user [8]. The dynamic range requirement for the A/D converter in the receiver architecture of Fig 2.3 is set primarily by the input range that must be accommodated by the receiver at acceptable error rates and also by the amount of AGC preceding the digitization. Elimination of AGC stages would considerably reduce the amount of analog processing but would also invoke the need of an A/D converter with at least 16 bits of dynamic range at 2.2Msps. To avoid the need to meet such a severe performance requirement and its attendant power demands, most ADSL receiver implementations employ a modest amount of AGC control to reduce the A/D converter dynamic range requirements to less than 16 bits.

2.1.3 Future trends

The penetration of DSL technologies is increasing around the world. Fig 2.4 shows the DSL subscriber lines around the world at the end of year 2005 compared to year 2004 [9]. There is also an increased demand for bandwidth. A newer variant called ADSL2 provides higher downstream rates of up to 12 Mbits/s for spans of less than 2.5 km (8000 ft). More flexible framing and error correction configurations are responsible for these increased speeds. ADSL2+, also referred to as ITU G.992.5, boosts these rates to up

to 24 Mbits/s for spans of less than 1.5 km (5000 feet) by doubling the downstream spectrum upper limit to 2.2MHz. Thus the A/D converter has to operate at twice the speed. It appears likely that data rates will increase in near future, requiring higher bandwidth A/D converters.

2.2 Radio receivers

The main function of a radio receiver is the reception of a, possibly weak, desired channel from a wideband frequency spectrum containing strong interference signals, with a minimum specified signal-to-noise and distortion ratio. To accomplish these tasks of selectivity and sensitivity, filters and amplifiers are needed to suppress interference signals and to increase the desired channel power respectively. Because the desired channel band may be modulated at very high carrier frequencies, mixers are used to translate the channel to more appropriate lower frequencies. The analog-to-digital converter is becoming an important part of the receiver architecture. The place of the ADC determines which functions are implemented with analog circuitry and what functions are implemented in DSP.

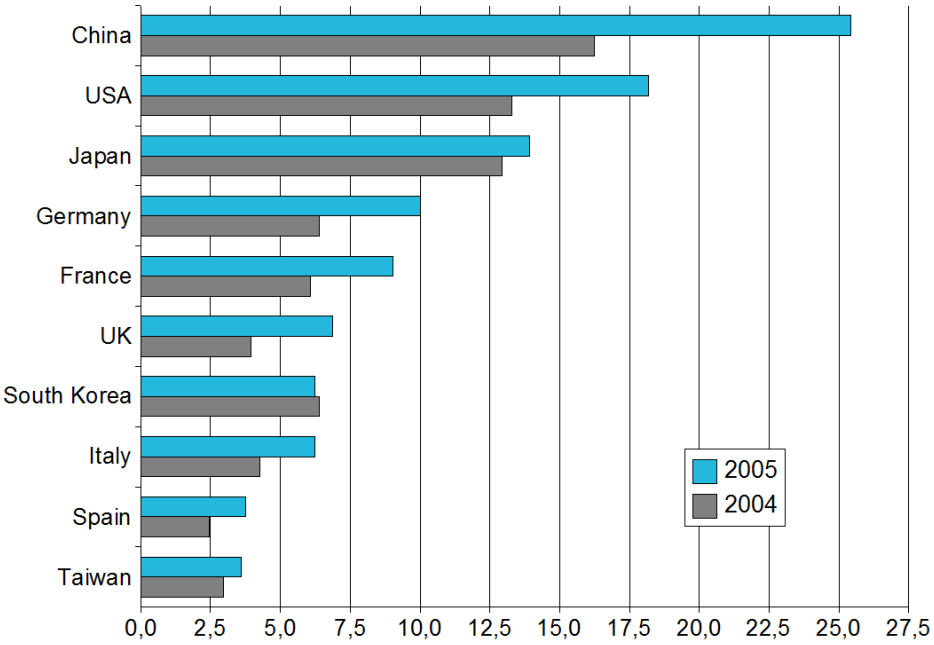


Fig. 2.4. Millions of DSL lines by countries at the end of 2005

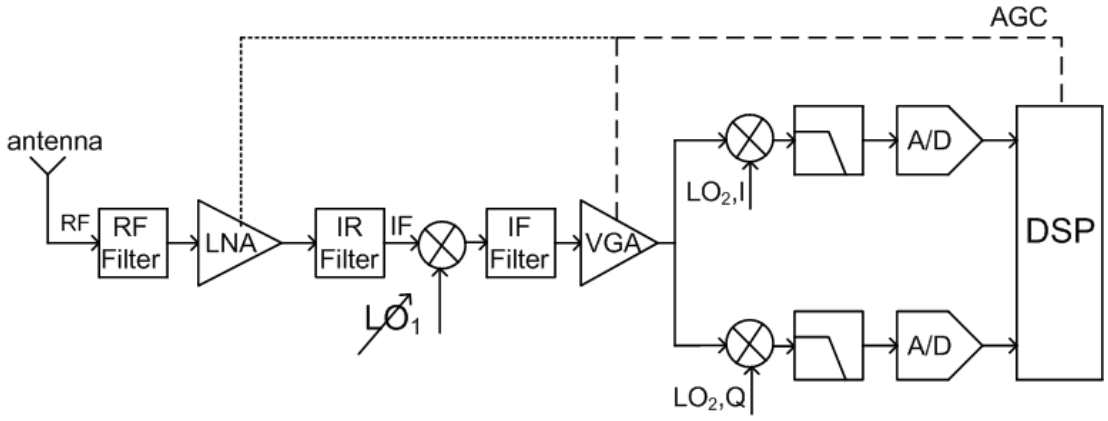


Fig. 2.5. Traditional superheterodyne receiver architecture

2.2.1 ADC placement in receiver

As the size of digital circuits as well as supply voltage (and hence power) decreases with each new technology node, it makes common sense to put more functionality into digital signal processor (DSP) to take advantages of these trends. Moreover, analog signal processing functionality such as filtering and frequency translation can be performed by DSP with almost any degree of perfection. Early digitization and increased digital signal processing makes it possible to have, programmable communication systems that can be easily be adapted to new standards and offer a high degree of flexibility through multi-mode operation. The requirements of ADC vary widely depending on where the ADC is placed.

Baseband A/D converter in the traditional heterodyne receiver of Fig 2.5 has the most relaxed requirement. This is because the interference signals have been filtered out by the channel filter and the desired channel is modulated down to DC or a low IF frequency. At DC or low-IF frequency, high linearity performance can be easily achieved.

At the other extreme is ultimate digital receiver architecture shown in Fig 2.6, also called as software radio. In software radio, a high speed, high-resolution data converter digitizes the RF signal directly at the antenna, with all further signals processing being

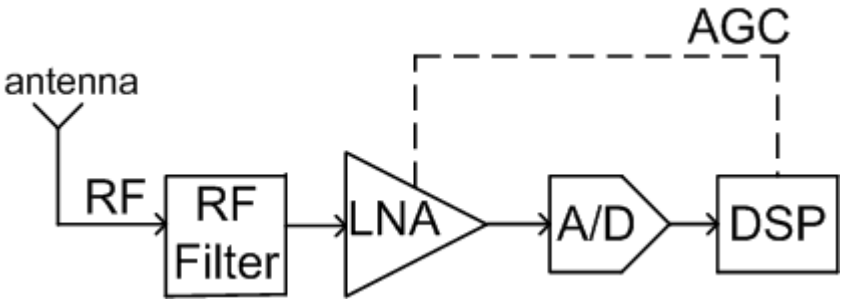


Fig. 2.6. Receiver with RF A/D conversion

handled in digital domain. Requirements on A/D converter in this architecture are extreme, as it has to handle the full antenna receiving power. This means that converter should have high dynamic range, high linearity, and large bandwidth at RF frequencies. This approach is infeasible in current technology nodes because of impractical power consumption.

Another possibility includes to digitize the IF, which may be not be very feasible if IF is high. Another possible approach is direct conversion receiver architecture shown in Fig 2.7. Here the RF is directly converted to DC or low-IF. After amplification and frequency down-conversion to baseband, two baseband A/D converters are used to individually digitize the in-phase and quadrature components. A continuous time anti-alias filter precedes the A/D conversion to avoid aliasing of out-of-band components into the frequency band of interest during the subsequent sampling operation performed by the A/D converter. The digitization process is followed by further digital processing, such as channel select filtering and demodulation. Thus channel select filtering is shifted to digital domain. Digital selection allows multiple standards to utilize the same handset or base station through a simple reprogramming of the DSP.

In cases of digital channel selection the dynamic range of A/D converter, must be large enough to avoid saturation in the presence of high-powered interferers that are digitized along with the desired signal. It is important to note that in architecture of Figure 2.7 AGC cannot be applied effectively to relax the A/D converter requirements since both the desired channel and adjacent channel interferers would be amplified by the

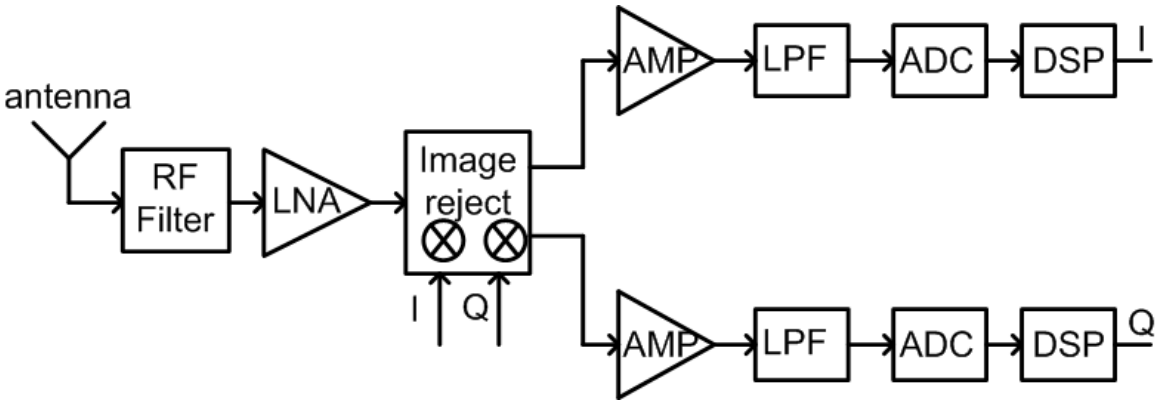


Fig. 2.7. Direct conversion receiver

same amount. Consequently, the dynamic range of the A/D converters must be large enough to enable extraction of a weak desired signal at an acceptable BER in presence of high-power interferers that are digitized along with the signal.

2.2.2 ADC specifications with digital channel selection

Table 2.1 summarizes the resolution and bandwidth requirements of a variety of RF standards place on the baseband analog-to digital interface in the architecture in Fig 2.7 [8].

Table 2.1. Baseband A/D converter specifications for various wireless standards

RF standard	Dynamic range	Minimum Nyquist rate
GSM	109dB	200khz
DECT	80dB	1.15Mhz
CDMA (IS-95)	90dB	1.23Mhz
3G	99dB	5Mhz
Bluetooth	73dB	1Mhz
IEEE 802.11(b)	73dB	1Mhz
Hiperlan	85dB	6Mhz

The A/D converter dynamic range required to meet a given standard is determined primarily by the receiver sensitivity and the power of worst-case channel interferers as specified by the standard. The bandwidth requirement is set by channel spacing and modulation scheme, which determines the fraction of channel spacing that can effectively be used. From Table 2.1 it can be concluded that RF receiver architectures employing digital channel-select filtering typically require an analog-to-digital interface capable of digitizing signal bandwidths in the megahertz range with accuracies in the order of 14 bits and higher. Furthermore, systems such as GSM, with signal bandwidths of only 100khz, may also benefit from baseband sampling rates in the megahertz-range through the simultaneous digitization of multiple channels. Multi-channel digitization is particularly useful in the base station of wireless communication systems, where multiple channels need to be digitized simultaneously. For example, for GSM, with a 25Mhz RF bandwidth two A/D converters with a Nyquist conversion rate of 4 MHz suffice to digitize the I & Q signals of all channels allocated to a single base station.

2.3 Vibration analysis

2.3.1 Introduction

Machinery downtime during normal shift operations is very costly due to lost production, but it is also avoidable. Preventative maintenance systems are being used to improve the operating efficiency of machinery used in factories, power plants, mining, and many other operations. Diagnostic electronics, used in newer preventative maintenance programs, monitor the operating parameters of the machine. For example, a roller mill may have several large electric motors and rollers, all of which have bearings, a hydraulic pump, and a variety of hydraulic actuators. A preventative maintenance system for this type of equipment could include electronic monitoring equipment to measure bearing vibration and temperature, hydraulic fluid pressure and temperature, and motor temperature [10].

Vibration analysis, which is the measurement of vibrations generated by moving parts in the frequency range of 50 Hz to 10 kHz, can be used to monitor the condition of bearings and other moving components. Ultrasonic analysis, an extension of vibration

machine bearing casings, and on some machines, on the rotating shafts. Changes are detected through spectral analysis of the generated frequencies in the moving components due to wear or damage. As parts wear, the magnitude of the vibrations and ultrasonic noise will increase. The level of vibration can be compared with established standards to assess the severity. An increase of about 12 dB indicates possible impending failure. Usually a full spectrum of the vibration is sampled, and using fast Fourier algorithms the component frequencies and their accelerations may be determined. Analyzing the frequencies and their harmonics helps locate the root cause of the vibration, allowing it to be remedied, and hopefully designed out. For example, high vibration at the frequency corresponding to the speed of rotation is usually due to unbalance. Degrading rolling element bearings give out increasing vibration signals as they wear. Special analysis instruments can detect wear even months before failure, giving ample warning to schedule replacement.

The system architecture for a PC-based vibration analyzer is illustrated in Figure 2.8 The development of system can be categorized as follows [11,12].

- Selection of proper vibration transducers based on the criteria of high frequency bandwidth, better sensitivity and ease in handling.
- Proper signal conditioning; amplification, filtering, and conditioning of the transducers signals, prior to interfacing with the computer
- Analog-to-digital conversion of high frequency vibration signals.
- Computation of frequency spectra of vibration signals. This allows evaluation of machine status by analysis of vibration spectra.

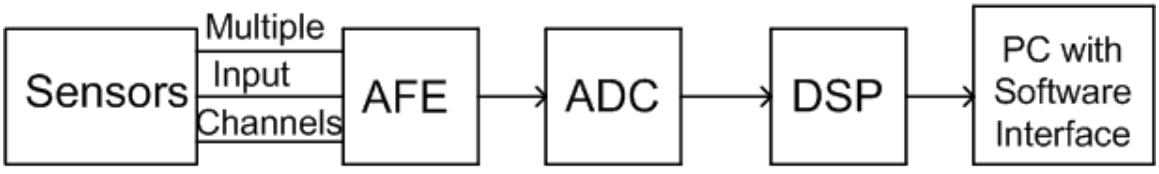


Fig. 2.8. System architecture for vibration analysis

In the PC-based vibration analyzer, multiple vibration signals are acquired in real-time with the help of fast, high-resolution data acquisition system. The data processing routines transform the digital time-domain data into frequency domain by using fast Fourier transform (FFT), and calculate signal auto- and cross-power spectral density functions and root mean square (rms) amplitude. The frequency spectra, or vibration "signatures," obtained by the computer are analyzed for machinery fault detection and identification using appropriate vibration criteria, as discussed earlier.

2.3.2 ADC specifications

The requirements of the data acquisition system employed for vibration monitoring are fast conversion speed (high sampling frequency), high signal resolution, and multi-input capability. Since the signal spectrum is limited to 40khz the Nyquist rate is only 80ksps.
To relax the requirement on anti-aliasing filtering it is common to use an over-sampling ratio of at least 1.5 i.e sampling rate of 120ksps. The requirement for higher speed occurs because typically 8-16 input channels are multiplexed. The resolution required is typically 14-16 bits. Even higher resolution ADC's are being designed for vibration analysis, to simplify the analog front end. The higher dynamic range of ADC's eliminates the need for a discrete low-noise programmable gain amplifier (PGA). This helps to reduce the system cost by making analog front end simpler, especially for system with many input channels.

2.4 Very high frequency SONAR

Sonar is an acronym for Sound Navigation and Ranging. There are two broad types of sonar in use. Passive sonar is a listening device that can determine the presence, characteristics and direction of marine noise sources. These sources may include biological noise (animal communication) and human sounds (e.g. ship or submarine noise). Passive sonar equipment is essentially an acoustic receiver, which emits no sound.
Active sonar is a technique that uses sound to determine relative positions of submerged objects (including submarines, fish, mines and wrecks of ships and aircraft) and the sea

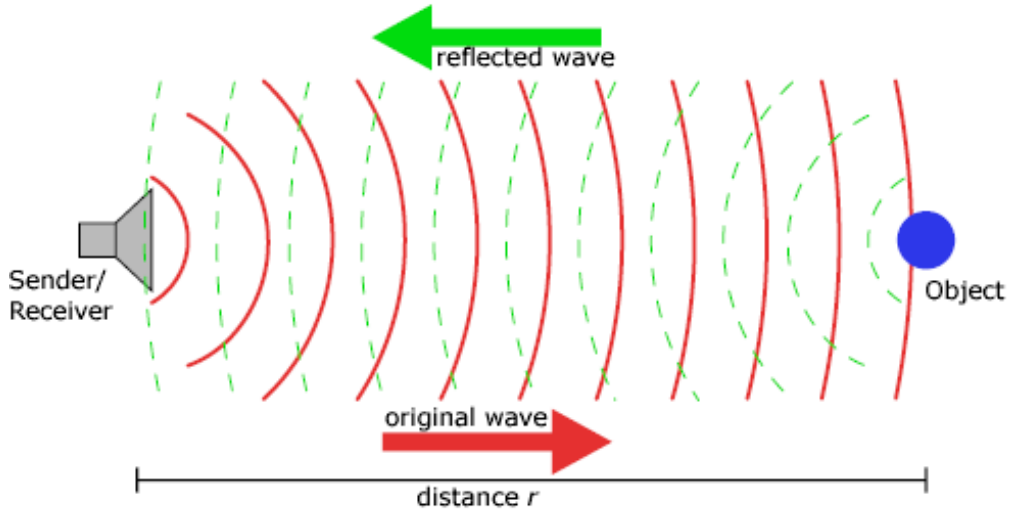


Fig. 2.9. SONAR operating principle

floor, by emitting a sound signal and listening for the echoes from the objects. Many different types of active sonar are used throughout the world's oceans by private, commercial and military vessels. These systems mirror the purpose of sonars used by some marine animals. Active sonar devices locate objects by the reflection of sound waves and remain an important means of underwater detection and navigation. The principle is illustrated in the Fig 2.9. Active sonar creates a pulse of sound, often called a "ping", and then listens for reflections of the pulse. To measure the distance to an object, one measures the time from emission of a pulse to reception.

Finding objects in turbid waters with underwater video is a problem due to the lack of visibility. High frequency acoustic signals suffer less scattering in turbid waters, so attempts have been made to produce an innovation in high-resolution underwater acoustic imaging [13]. Until recently, it was not possible to handle the computational load associated with sonars with many (perhaps 100-1000) receiving elements at high frequency (>1 MHz). The new systems coming onto the marketplace now use sparse arrays, to reduce the number of elements, and modern DSP power to achieve real-time imaging [14]. Research at Applied Physics Laboratory, and elsewhere has resulted in the advent of very high-resolution *acoustic imaging* systems, for example the DIDSON sonar. These systems use sound energy at very high frequencies (over 1 MHz) to

generate detailed acoustic maps of underwater features and objects. These systems allow increasingly greater resolution as the frequency increases but at the expense of range. The highest frequencies are only effective over short distances because of the rapid attenuation of high frequency sounds in seawater.

The acoustic imaging system can be used to:

- Expedite construction, repair, and maintenance of underwater structures.
- Provide safer conditions for employees engaged in environmental, wet construction, and structural inspection activities.
- Enable identification of endangered species, aid in underwater recovery operations, and detect cultural artifacts prior to construction projects.
- Determine proper placement of riprap.
- Inspect levees for failure sites.
- Enable the user to immediately and permanently log underwater images from inspections.

Most of the research in field of very high frequency SONAR is promoted by military and it is expected that High Frequency Sonar will play a more important role in future submarine missions as operations in the littorals require detailed information about the undersea environment to support missions requiring high-quality bathymetry, precision navigation, mine detection or ice avoidance.

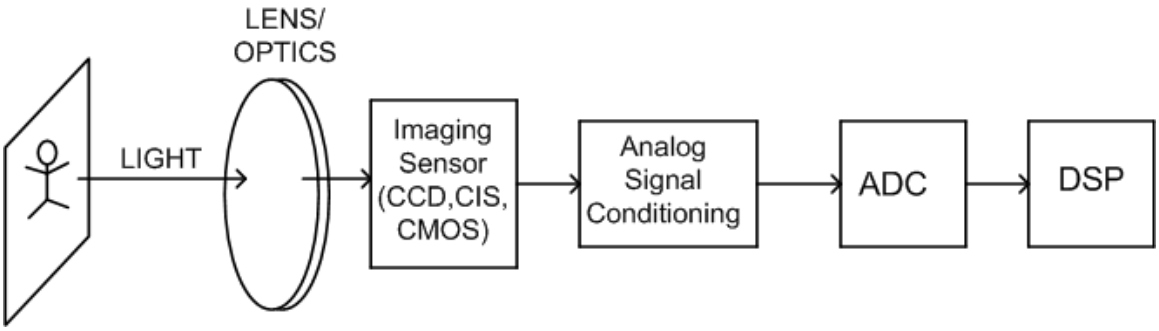


Fig. 2.10. Generic imaging system for scanners

2.5 High-end flatbed scanners

2.5.1 Introduction

Every imaging system starts with an image sensor. The signal from the sensor must be processed in the analog domain, converted to digital, and further processed in the digital domain. This allows the image to be analyzed, manipulated, and enhanced, prior to storage, display, transmission, and/or further processing. Imaging applications typically involve three chips—an image sensor, an analog front-end (AFE), and a digital ASIC. The AFE conditions the analog signal received from the image sensor and performs the analog-to-digital (A/D) conversion. The digital ASIC contains image processing and timing-generation circuitry. Fig 2.10 shows a block diagram of a typical imaging system. Additional application-specific circuitry following the digital image processing ASIC depends upon whether the imaging system is a camera, scanner or copier.

Image sensor: The *charge-coupled-device* (CCD) is widely used in consumer imaging systems such as scanners and digital cameras. The imaging sensor (CCD, CMOS, or CIS) is exposed to the image or picture much like film is exposed in a camera. The building blocks of a CCD are the individual light sensing elements called pixels. A single pixel consists of a photosensitive element, such as a photodiode or photo capacitor, which outputs a charge (electrons) proportional to the light (photons) that it is exposed to. The charge is accumulated during the exposure or integration time, and then the charge is transferred to the CCD shift register to be sent to the output of the device. The amount of accumulated charge will depend on the light level, the integration time, and the quantum efficiency of the photosensitive element. A small amount of charge will accumulate even without light present; this is called dark signal or dark current and must be compensated for during the signal processing. The pixels can be arranged in a linear or area configuration. Clock signals transfer the charge from the pixels into the analog shift registers, and then more clocks are applied to shift the individual pixel charges to the output stage of the CCD. Scanners generally use the linear configuration, while digital cameras use the area configuration. The analog shift register typically operates at pixel frequencies between 1 and 10 MHz for linear sensors, and 5 to 25 MHz for area sensors.

Analog front-ends: A typical AFE starts with an input clamp. The common-mode level of the image sensor's output signal could range from 0 V to more than 9 V, so the signal must be ac-coupled to the AFE. The input clamp restores the dc level of the signal to an optimum point within the supply range of the AFE. A sampling function follows the input clamp. AFEs designed to work with charge-coupled devices (CCDs) use a correlated double sampler (CDS). The CDS takes two samples of each pixel, one at the reset level and one at the video level, and performs a differential measurement between the two. The CDS improves the signal-to-noise ratio (SNR) by eliminating the correlated kT/C noise associated with the output stage of the CCD, and by attenuating low frequency drift. Contact image-sensors (CIS) and focal-plane arrays (FPA) used in commercial infrared (IR)-imaging applications typically output a single-ended, ground-referenced signal, and do not require a differential measurement. AFEs designed to work with these sensors use a sample-hold amplifier (SHA) in place of the CDS. A coarse black-level offset-correction stage is integrated with the CDS or SHA.

A programmable- (or variable-) gain amplifier (PGA or VGA) follows the CDS to amplify the signal and better utilize the full dynamic range of the A/D converter (ADC). A high-speed ADC converts the conditioned analog image signal to the digital domain, allowing for additional processing by a digital ASIC. The choice of an AFE for an imaging application depends on many factors, including: the type of sensor being used, dynamic range, resolution, speed, noise, and power requirements.

2.5.2 ADC specifications

Resolution: Professional scanning applications use the best CCDs available today. Graphic-arts scanners and film scanners may also use cooling mechanisms to control the temperature of the CCD, maximizing the SNR. Integration times will be as long as reasonable to maximize the dynamic range of the CCD output signal and increase the SNR. With CCD signals of up to 4 V commonly available in these applications, true 13- or 14-bit performance is achievable. In any imaging system, the AFE should not be the

limiting factor in performance, so for these high-end applications a true 14-bit AFE is necessary. Commercial solutions with 16-bit AFE are now commonly available [15].

Speed: To look more closely at the speed requirements for the AFE, consider typical copying specifications. For standard copying, a 300 dots-per-inch (dpi) scan is adequate. For a letter-sized document, color scanning at 300 dpi yields roughly 30 million pixels. Allowing for some processing overhead, scanning at a sample rate of 6 MHz (2 MHz/color) takes about 6 seconds, for a page rate of 10 pages per minute (ppm). To achieve 20 ppm, a sample rate of 12 MHz is needed—double the sample rate of most currently available scanner AFEs. A multifunction peripheral (MFP), which integrates the scanner/ fax/copier functions in a single unit, typically requires a higher speed AFE than a flatbed document scanner, but it still needs to function as a good-quality scanner (600 dpi or more). For this case, the resolution needed for a letter-sized document is approximately 120 million color pixels. For this resolution, a 6-MHz AFE can produce only about 2.5 ppm, and a 12-MHz AFE increases the throughput to about 5 ppm. Many newer MFPs on the market can support 8–10 ppm in color-copy mode, at 600 dpi resolution; this requires an AFE sampling rate of around 20 to 22 MHz [15].

CHAPTER III

INTEGRATED INPUT DRIVERS

3.1 Motivation

As the resolution and speed of the A/D converters increases, it becomes increasingly difficult to find a catalog operational amplifier (Opamp) to drive the switching input load of the ADC. A typical driver circuit for high speed ADC's, is shown in Fig 3.1. From the figure we observe that if we integrate the driver on ADC chip we can reduce the component count (the Opamp and all associated passives) as well as reduce a set of power supply, which is very desirable. The catalog opamps are mostly characterized with a resistive load in the datasheets. Hence to find a suitable opamp to drive an ADC, it becomes necessary to tweak the R and C at the input during measurements. The switched capacitor load presents the worst loading conditions for the driving opamp, which is not captured in datasheets. The switched capacitor load presents the driving amplifier with step inputs thus settling requirements on the driver is very stringent.

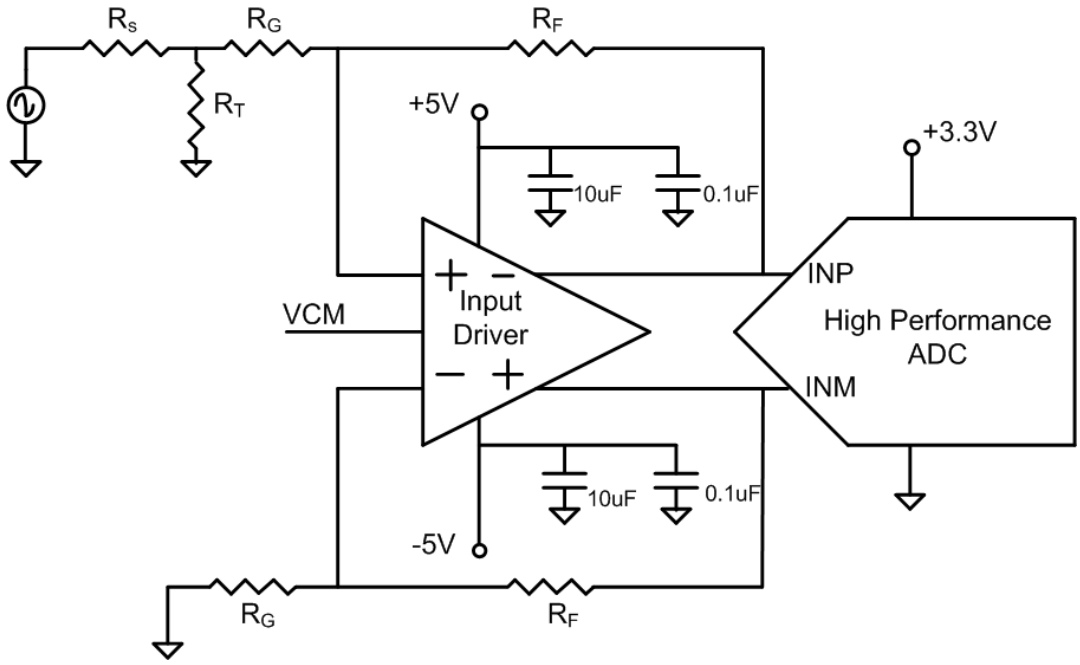


Fig. 3.1**.** An on-board amplifier driving a high performance ADC

As discussed in previous chapter there is a need for higher bandwidths with both better SNR and SFDR. This in turn means that to keep the same over-sampling ratio the clock frequency as well as the sampling capacitor size has to be increased. The SFDR of the sampled signal in these cases is limited by how fast the input amplifier can settle once it sees the step at the output, caused by the switching load. Since the available time to settle is only half clock cycle, it becomes extremely difficult for the amplifier to settle to 16-18-bit linearity as the clock frequencies increases and also as the value of capacitor being switched increases.

On the SNR front, traditionally a RC filter has been placed at the output of the buffer as shown in Fig 3.2 to filter out high frequency thermal noise from the driving opamp and resistors if any in the opamp configuration. This approach becomes less effective as the signal frequency increases, since the –3db bandwidth of the filter has to be increased to prevent signal attenuation implying that we will get more high frequency thermal noise. Also this technique prevents from achieving very good SFDR numbers as output of RC filter is a slow moving node and it takes a large settling time. This technique works only if the switching capacitor is a very small fraction of the capacitor in RC filter so that

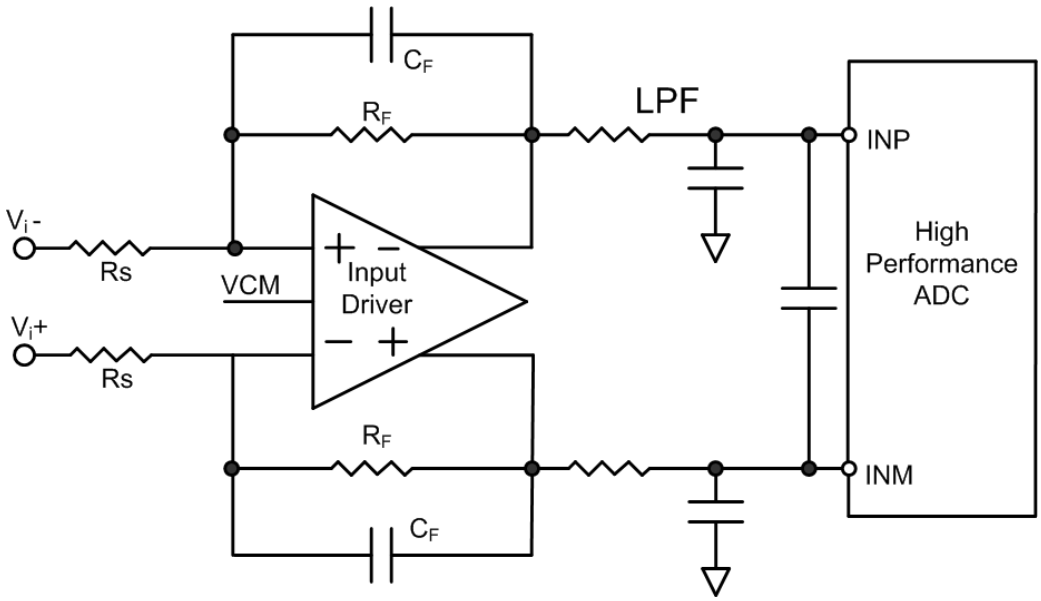


Fig. 3.2. Input buffer with an RC filter at the output to filter out noise.

majority of the charge is provided by the capacitor by charge sharing and then there must be sufficient time for output to settle to required accuracy. This is increasingly not the case in high speed over-sampling ADC's. The situation is no different for high speed pipelined ADC's and SAR ADC's. The solution that is proposed is applicable to all the before-mentioned ADC categories.

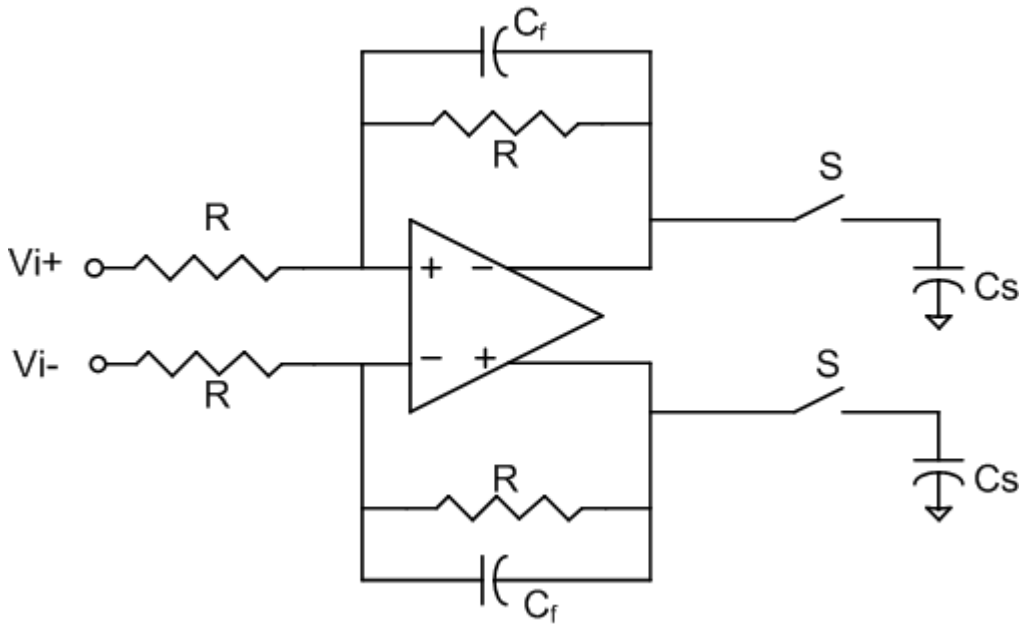
Another important concern is the high-speed catalog amplifiers are generally designed in BICMOS process. If the ADC is being designed in a slow CMOS process to achieve higher swings, then it may not possible to design very fast amplifiers (regardless of the power consumed it may not be possible to achieve very high Gain band-width and slew rate because of parasitic capacitances). One solution is to have a MCM (multi-chip module) with a BICMOS amplifier and the CMOS ADC in the same package. In this way, some parasitic inductance is avoided which may lead to better settling of the amplifier output. But this solution is not that simple from production point of view. Our proposed solution makes it possible to have an input buffer on-chip even with slow CMOS technologies and it is extremely simple, helps to reduce power and also improves SNR

3.2 A novel precharge scheme

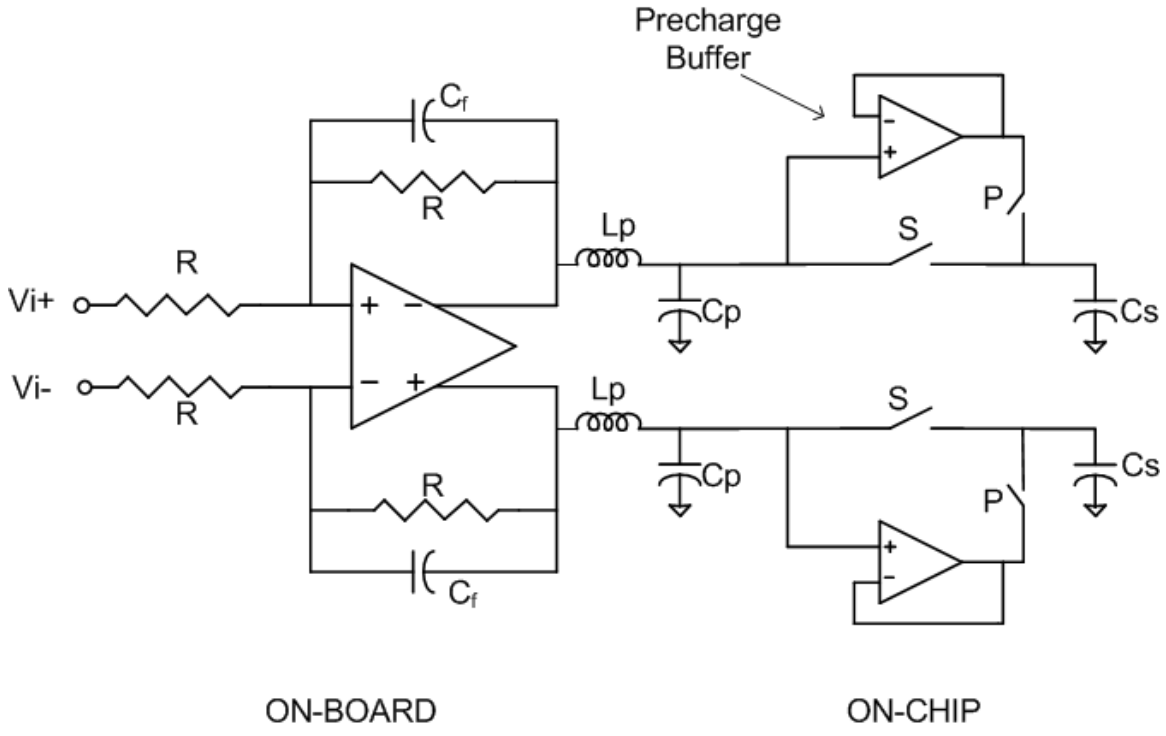
3.2.1 Existing approaches

For fully differential circuits, configuration shown in Fig 3.3(a) is traditionally used, with a possible addition of RC filter at the output. The circuit shows a continuous time amplifier, with a load (Cs) connected to it when the clock phase 'S' is high. This amplifier needs to be extremely fast to settle to desired accuracy in half clock cycle.

A pre-charge scheme has been used previously used in SAR converters to relax the requirements on the input driver and is illustrated in Fig 3.3b. The idea in this scheme is to relax the requirement on external amplifier by having an internal pre-charge buffer to provide the initial surge current and provide a coarse sampling of input. The precharge buffer drives the input during precharge phase 'P', after which external driver takes over in phase 'S'. This scheme mitigates the effect of parasitic inductance L_p on sampling. The pre-charge time is chosen to be about one-third the total sampling time.



(a) Integrated driver: Load Cs is switched in the sampling phase ('S'),



(b) Input driver with a precharge buffer.

Fig. 3.3. Existing approaches

One obvious disadvantage of this solution is that we need to use an additional buffer, which means additional power. Other concern is that the power consumption for pre-charge buffer may be exorbitant for over-sampling ADCs. To illustrate, let us assume that we want to design a 16 bit, 10Msps ADC. For a typical SAR ADC, the sampling time may be 20ns, but for a sigma-delta ADC with an over sampling ratio (OSR) of 8 the sampling time is just 6ns.

3.2.2 Proposed solution

The proposed solution [1] is shown in Fig 3.4. The idea is as follows. The amplifier needs to be very fast and accurate only when the ADC is sampling the input, in the other phase the amplifier is not really used. So in this phase, we configure the amplifier as a slow amplifier charging a large capacitor k*Cs (~10*Cs).

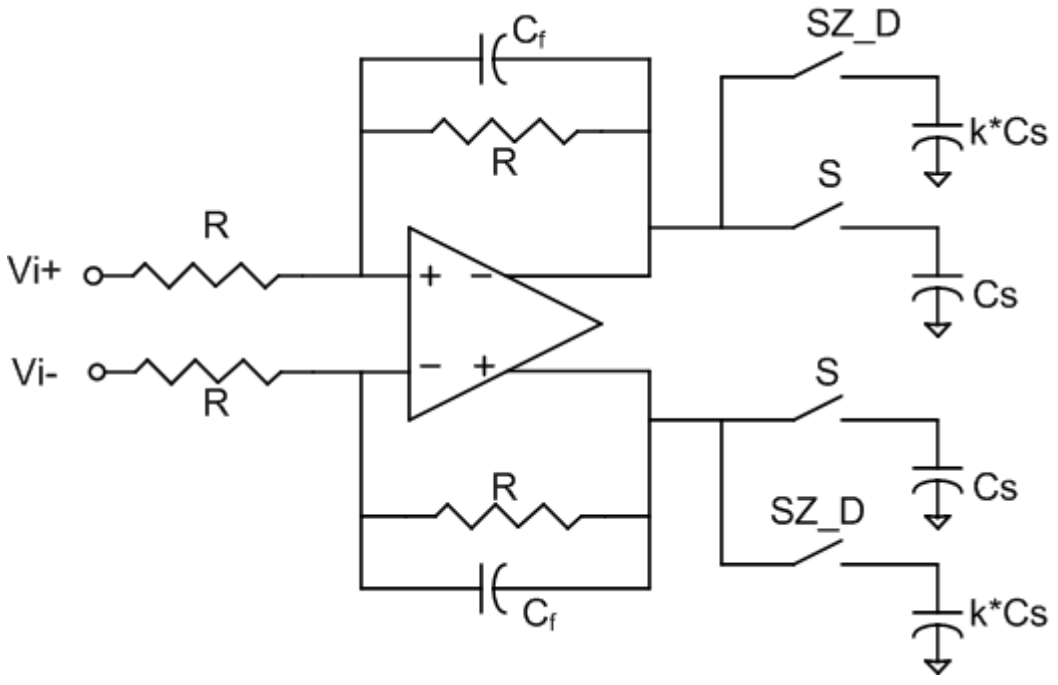


Fig. 3.4. Proposed solution. Amplifier sees a load capacitor of Cs in 'S' phase and k*Cs in SZ_D phase

The sampling phase is split in two parts. A coarse pre-charge phase, which is about one-eighth of the sampling time. In this phase amplifier is configured as slow amplifier, the charge to the sampling capacitor Cs is provided by the large capacitor at the output by charge sharing. The output reaches to within 10% of its final value in this phase (for k ~10). The second phase is fine sampling phase. In this phase amplifier is working at its normal speed, and the large capacitor is disconnected from the output. The amplifier now operates such that output settles to desired accuracy.

The timing is illustrated in Fig 3.5. The only additional signal that needs to be generated is SZ_D, which is just a delayed version of SZ, so is very easy to generate. This signal determines when the large cap is connected to the output/compensation cap in increased. 't_1' is the non-overlap time between sample and hold phase . 't_2' provides the early edge required for bottom plate sampling explained in chapter IV. 't_3' is the precharge time, during which sampling capacitor and precharge capacitor are connected together.

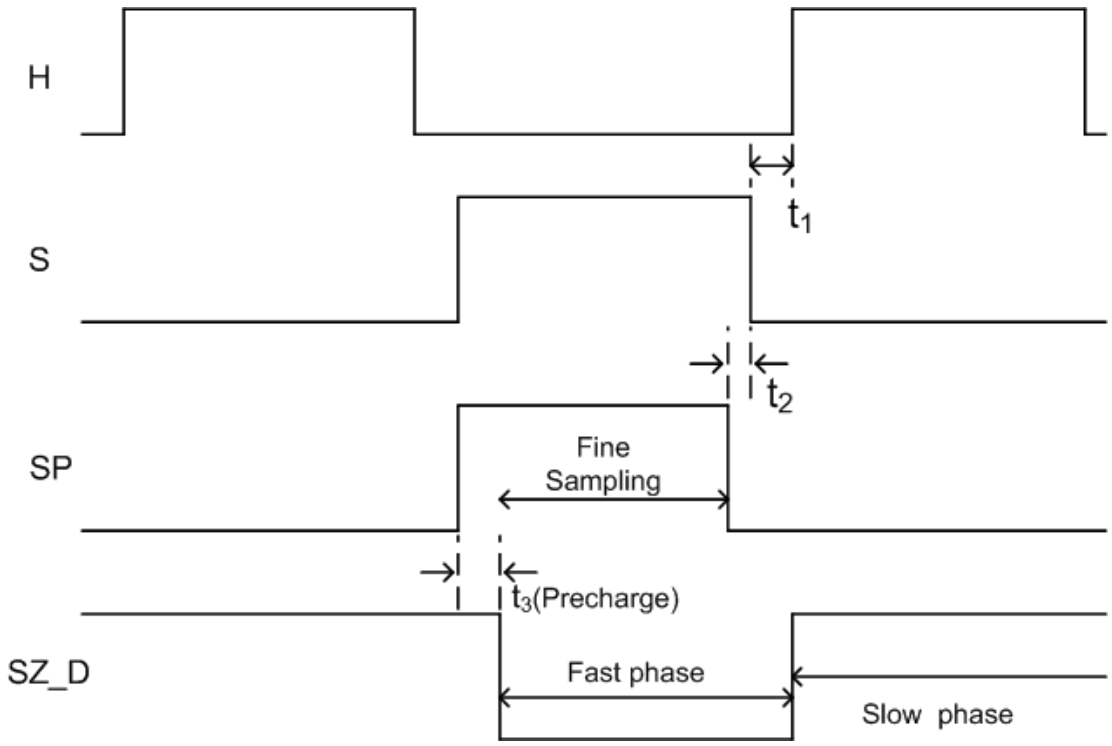


Fig. 3.5. Timing diagram for precharge scheme

To reduce the area penalty because of large precharge capacitors we can place the capacitors differentially as illustrated in Fig 3.6. This helps to reduce the precharge capacitor by a factor of two.

3.2.3 Simulation results

The scheme proposed is very general and can be used with any type of amplifier, either on-chip or on-board. We present the SFDR results for a specific case, in which the sampling capacitor is 25pF, clock frequency is 40Mhz, the max step at output is 3V differential, targeted SFDR is 100dB for 1Mhz input signal at –2dBFS, which is 4.8Vpp. Technology used is 0.5um CMOS technology. The pre-charge phase is about 1.5ns and the fine sampling phase is around 9ns. For the worst case step the output reaches 2.7V in 1.5n s, which corresponds to a slew rate of 1.8V/ns, which may be extremely difficult to achieve with CMOS amplifiers. The comparison of the SFDR of proposed scheme with traditional solution is shown in Fig 3.7. The amplifier used has a closed loop bandwidth of 270Mhz and a slew rate of 0.6V/ns.

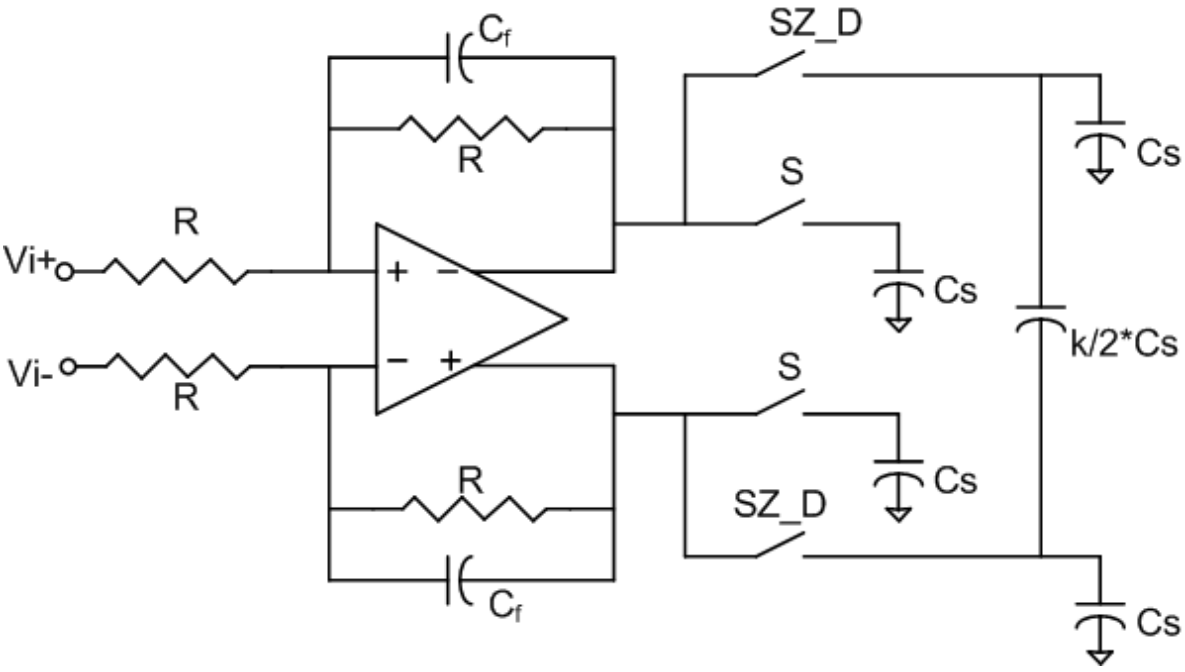


Fig. 3.6. Reducing area penalty by using differential capacitor.

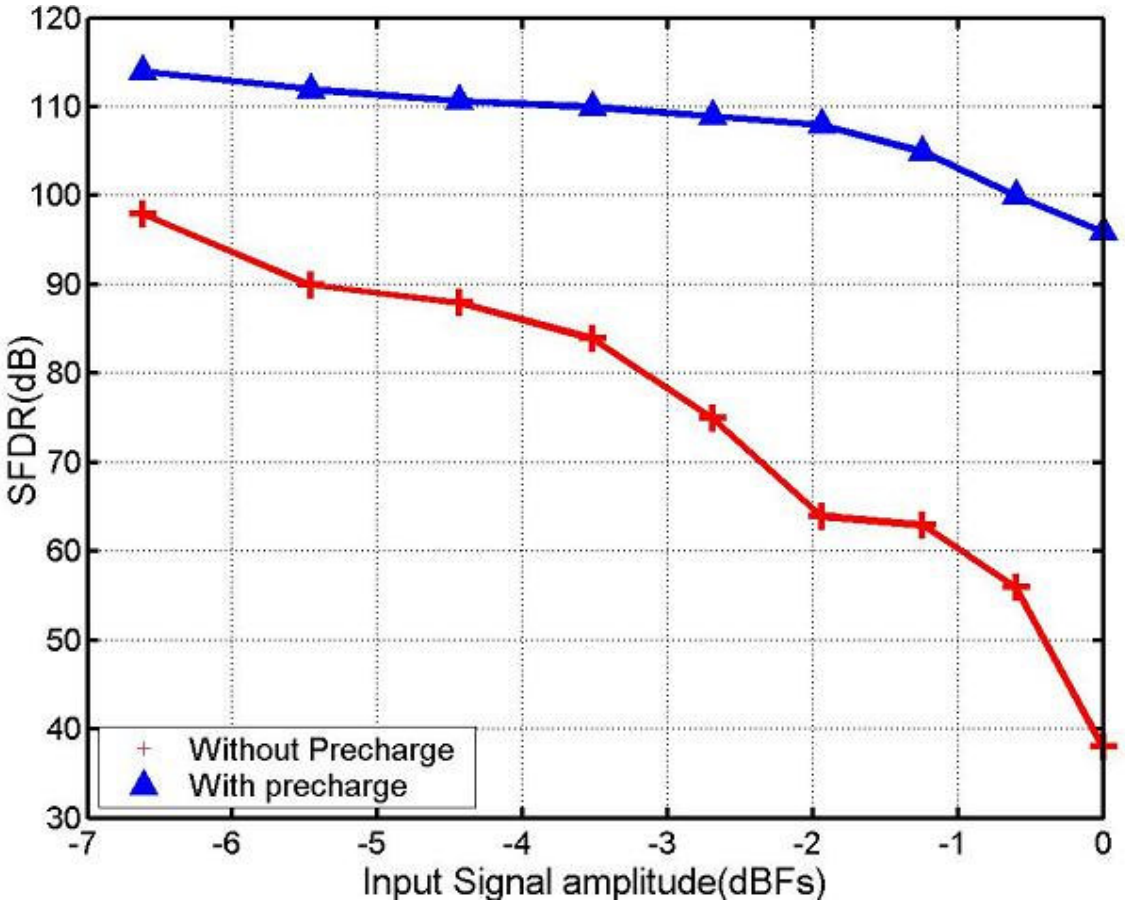


Fig. 3.7. Simulation results comparing the SFDR obtained with pre-charge scheme vs the scheme in Fig. 3.3a.

From Fig. 3.7 we observe that that compared to the traditional approach (Fig 3.3a) the SFDR improvement is around 50dB for larger signal amplitudes. Effectively this improvement is achieved using an opamps with lesser bandwidth, thereby reducing power. Also the SNR is improved due to the reduced bandwidth of the amplifier.

3.2.4 Advantages of proposed solution

- Proposed pre-charge scheme doesn't use any extra pre-charge buffer, so it will consume less power than solution in Fig 3.3b
- This scheme makes it possible to integrate input buffer with the ADC even in slow CMOS technologies

- Even if ADC is designed in a process where it is possible to design fast amplifiers, we [1]can save power by using this scheme by using a slower amplifier
- Finally for high frequency input signals it is not possible to put a RC filter at the output to filter out noise. The bandwidth in the sampling phase is determined by the op-amp bandwidth as well as input circuit time constant. Having a fast amplifier is detrimental from SNR point of view. The noise which is aliased into base-band will reduce if we reduce the bandwidth of the amplifier. This is especially true if the dominant source of noise is the noise from feedback resistors.

III Multipath common mode feedback scheme*

3.3.1 Introduction

Fully differential amplifiers are widely used in modern integrated circuits because of larger output swings and less susceptibility to common mode (CM) noise. One major disadvantage of these circuits is the need of a CMFB circuit to control the CM output voltage. The basic aim of the CMFB circuit is to sense the output CM voltage and use negative feedback to force it equal to desired CM voltage V_{REF}. This is illustrated in Fig 3.8. The differential output voltage is well defined for a given input voltage, but for an

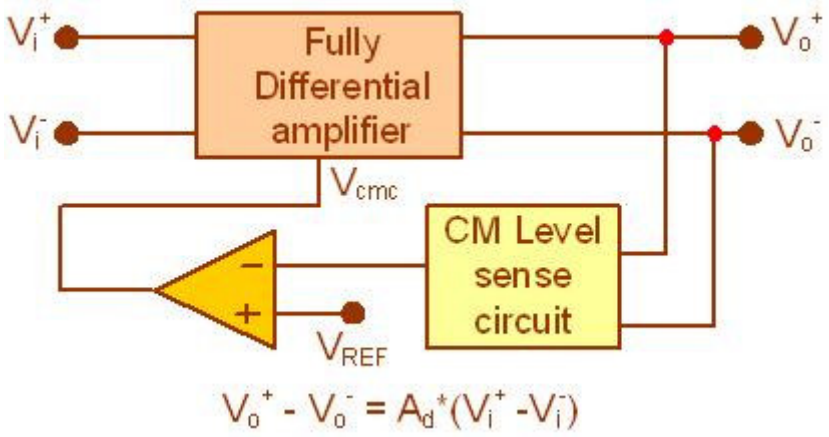


Fig. 3.8 A conceptual block diagram of the CMFB loop

* Part of this section has been reprinted from "Multipath common mode feedback scheme suitable for high speed two-stage amplifiers," by A.K.Gupta, V.Dhanasekaran, K.Soundarapandian and E.Sanchez-Sinencio, April 2006, Electronics Letters, vol. 42, no 9, pp. 499-500. Copyright IEE, 2006.

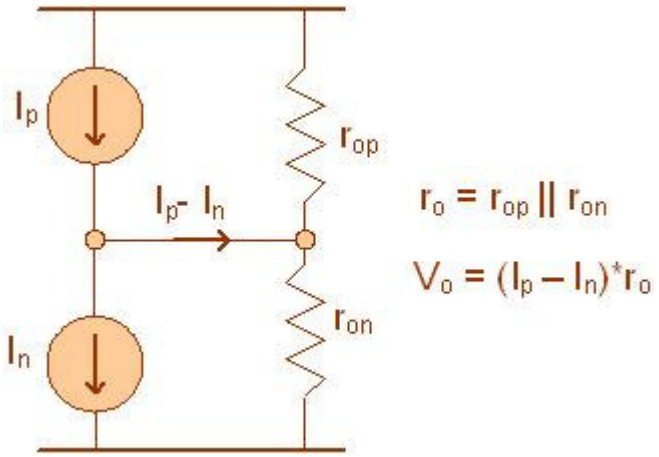


Fig. 3.9 Simplified model of a high gain differential amplifier

ideal amplifier the common mode rejection is infinite so input cannot define the output common mode level. The need for CMFB arises because in high gain amplifiers, we wish a p-type current source to balance an n-type current source. As illustrated in Fig 3.9 the difference between Ip and In must flow through the intrinsic output impedance of the amplifier, creating an output voltage change of (Ip-In)*ro. Since the current error depends on mismatches and 'ro' is quite high, the output may easily go to supply rails.

In this paper we analyze a case of practical interest in which the negative feedback loop is no longer effective because of positive feedback by external network, leading to output staying at rails [16]. The existing solutions [17] will need a large bandwidth in CMFB loop to alleviate the situation, making it difficult to compensate for high-speed designs. The proposed scheme tackles the problem by having large transconductance gain at low frequencies while having a low transconductance gain at high frequencies in the CMFB loop.

3.3.2 External positive feedback and latching states

One of the various methods to detect and feedback the CM correction signal as applicable to a two-stage amplifier is shown in Fig 3.10. Only a fraction (I3/(I3+I4)) of total current is controlled by the CM loop. The dc error in the CM output is given by

$$\Delta V_{OCM} = V_{REF} - V_{OCM} = \frac{\Delta I}{g_{m3} * A_1} \tag{3.1}$$

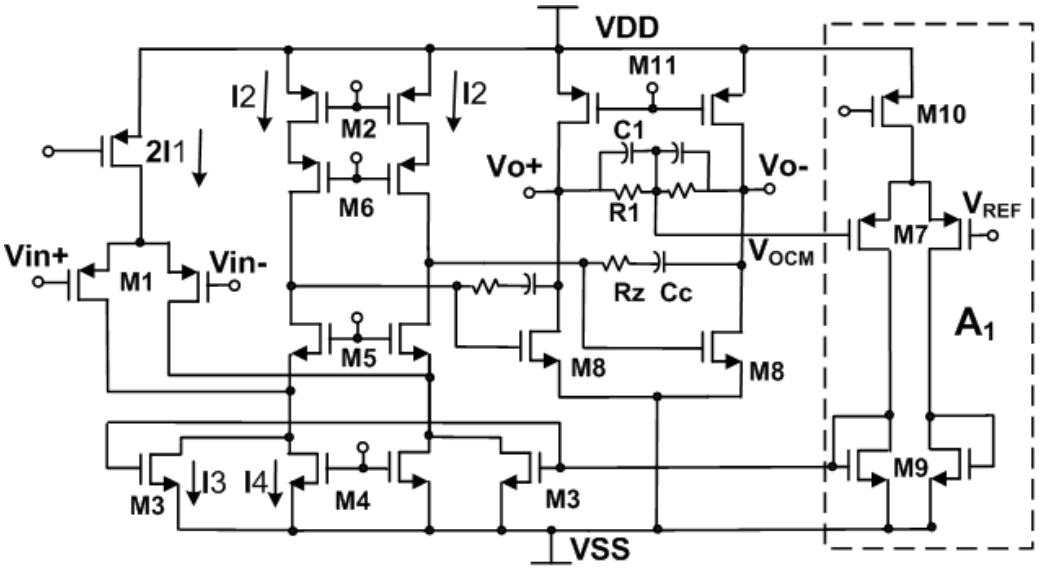


Fig. 3.10. A Two-stage Miller compensated amplifier with traditional resistor averaged CMFB scheme

where ΔI is the open-loop mismatch between the current sources ($I_{1o}+I_{2o}-I_{3o}-I_{4o}$) and A_1 is the voltage gain of common sense amplifier shown in broken lines in Fig1. Thus we observe that the error will reduce if we increase the transconductance gain ($g_{m3}A_1$).

For a two-stage amplifier, although the feedback through the external network is negative for differential signal, it is positive for the CM signals. In normal operating conditions, the negative feedback loop gain is much large compared to positive feedback loop gain so latter is not of much concern. The problem occurs during start-up or during large CM transients, in which case input differential pair turns off. If not designed properly output swings to rails and stays there. As noted in [16], many operational amplifiers have no built in provision to avoid these latching states. For the design in Fig 3.10, latching state will exist if $I_4 > I_2$ or $I_3 < I_1$. Thus to avoid the latching state CMFB loop should at least control I_1 amount of current. It is worth noting that this problem of latching states can exist even if we feed the CMFB to transistor M2 instead of M3 or if we had a NMOS input stage instead of a PMOS input stage.

In general it is more difficult to compensate the CMFB loop compared to the differential loop because of two additional poles in the former. The CM loop gain is given by (assuming that RHP zero due to Miller compensation is removed by nulling resistor R_z)

$$A_{CM}(s) = \frac{A_0(1+s/\omega_z)}{(1+s/\omega_d)(1+s/\omega_L)(1+s/\omega_f)(1+s/\omega_{cm1})(1+s/\omega_{cm2})} \tag{3.2}$$

where

$$A_0 \approx \frac{g_{m3}g_{m5}g_{m6}g_{m8}}{\left(g_{m6}g_{ds5}\left(g_{ds4}+g_{ds3}\right)+g_{m5}g_{ds2}g_{ds6}\right)\left(g_{ds11}+g_{ds8}\right)} * \frac{1}{2}\left(\frac{g_{m7}}{g_{m9}}\right), \qquad \omega_d \approx \frac{g_{m3} * A_1}{A_0 C_C}$$

, $\quad A_1 = \frac{g_{m7}}{2g_{m9}}$

$$\omega_f = \frac{g_{m5}}{C_{gs5}+C_{sb5}+C_{db1}+C_{gd1}+C_{db3}+C_{db4}} \quad , \ \omega_{cm1} = \frac{4}{R_1(4C_1+C_{gs7})}$$

$$\omega_{cm2} = \frac{g_{m9}}{C_{gs9}+C_{db9}+C_{gs3}} \ , \ \omega_L \approx \frac{g_{m8}}{C_L} \ , \ \omega_z = \frac{1}{R_1 C_1}$$

For $C_{gs7} << 4C_1$, $\omega_{cm1} \approx \omega_z$ so (2) simplifies to

$$A_{CM}(s) = \frac{A_0}{(1+s/\omega_d)(1+s/\omega_L)(1+s/\omega_f)(1+s/\omega_{cm2})} \tag{3.3}$$

For the circuit in Fig 3.10 differential loop bandwidth is given by $\beta g_{m1}/C_C$, while $A_1 g_{m3}/C_C$ gives CM loop bandwidth. Cc is generally chosen to compensate the differential loop optimally. Since feedback factor (β) doesn't affect CM loop bandwidth, for design with small β, it is possible to have $A_1 g_{m3}/C_C > \beta g_{m1}/C_C$ leading to CM stability issues. Solution mentioned in [17] and widely used is to reduce the fraction of current controlled by CMFB (reduce I_3) and hence reduce g_{m3}. This will lead to increased

dc CM error (1) and also if I_3 is made less than I_1 we will have latching states in the design.

3.3.3 Proposed solution

There are two contradicting requirements: for stability it is desirable to have small bandwidth, while for avoiding latching states it is desirable to have large bias currents. The proposed solution [2,3] illustrated in Fig 3.11(b) solves this problem by having two paths in the CM loop; a slow path (M3') and a fast path (M3''). The combination of the slow path and fast path determines the dc performance of the CM loop, while only the fast path determines the bandwidth of the loop. The slow path is created by having a series RC low-pass filter (R_2, C2) in the loop. The 3-dB bandwidth of this filter is set to about one-tenth of fast path bandwidth, which ensures that slow path is not active near unity gain bandwidth (UGB) of the loop. The bandwidth of the loop is determined by how the current I_3 is split between fast path (I_3'') and slow path (I_3'). Let us define I_3'' $=kI_3$ and I_3' $= (1-k)I_3$. If it is assumed that $\omega_{cm1} \approx \omega_z$ as in (3), we get following expression for loop gain

$$A_{CM}(s) = \frac{kA_0(1/k + s/\omega_{ps})g_{m9}}{(1+s/\omega_d)(1+s/\omega_L)(1+s/\omega_f)[s^2R_2C_pC_2 + sC_p + s(g_{m9}R_2+1) + g_{m9}]} \tag{3.4}$$

where

$\omega_{ps} = \frac{1}{R_2C_2}$ and $C_p = C_{gs9} + C_{db9} + C_{gs3''}$ with $g_{m9}R_2 >> 1$ (4) simplifies to

$$\begin{aligned} A_{CM}(s) &\approx \frac{kA_0(1/k + s/\omega_{ps})}{(1+s/\omega_d)(1+s/\omega_L)(1+s/\omega_f)(1+s/\omega_{pft})(1+s/\omega_{ps})} \\ &= \frac{A_0}{(1+s/\omega_d)(1+s/\omega_L)(1+s/\omega_f)}\left(\frac{k}{(1+s/\omega_{pf})} + \frac{1-k}{(1+s/\omega_{pf})(1+s/\omega_{ps})}\right) \end{aligned} \tag{3.5}$$

where

$\omega_{pf} = g_{m9}/C_p$

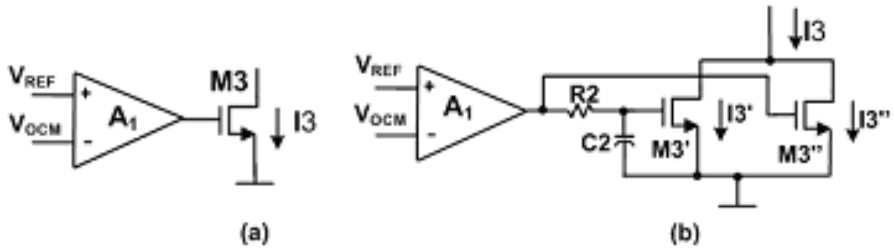


Fig. 3.11. Illustration of CMFB (a) Traditional CMFB scheme (b) Multi-Path CMFB scheme

Due to the multi-path scheme, the overall transfer function (4) has an additional pole and zero at low frequencies. Since both the pole and zero are at low frequencies compared to loop bandwidth, the overall response at high frequencies is just due to the fast path. The loop bandwidth is now given by $A_1 g_{m3''}/C_C = A_1 k g_{m3}/C_C$

Effect of having a pole-zero doublet on the settling response of the loop has been analyzed in [18]. If the doublet is at low frequency compared to loop bandwidth the magnitude of slow-settling component is small, and this is guaranteed in design by choice of low-pass filter (R_2C_2). As the pole-zero doublet spacing increases the magnitude of slow settling component increases. In this design zero will appear at 1/k times the pole frequency, so for a practical design k should not be too small ($k > 0.2$). For our design k was chosen as 0.5. The slow settling components become visible only if we desire very high settling accuracies, which is generally not the case with CM feedback circuit.

Another aspect, which deserves mention, is the fact that noise due to the R_2 in the filter appears as CM noise. Only a very small fraction (<1%) of this noise appears as differential noise as long as the matching between positive and negative branch of the amplifier is reasonable. An additional advantage of using multi-path approach is increase in dc transconductance gain and hence dc accuracy of the CM loop which may be critical in some designs [19]. This is a direct consequence of controlling a larger fraction of bias currents by CMFB.

3.3.4 Simulation results

Two amplifiers were designed in 0.5u CMOS technology, one with multi-path CMFB loop (k =0.5) and other with conventional design. Same amount of bias current is controlled in both CMFB loops (> I_1 to avoid latching states). Fig3.12 compares the CM loop ac response of both the amplifier. The UGB in the multi-path approach reduces from 100MHz to 65MHz while the phase margin (PM) improves from 24^o to 50^o. Fig 3.13 shows the CM output with a 400mV step on CM control signal. The conventional CMFB output exhibits ringing due to poor phase margin. Another observation is that there are no slow settling components visible in output with multi-path CMFB scheme.

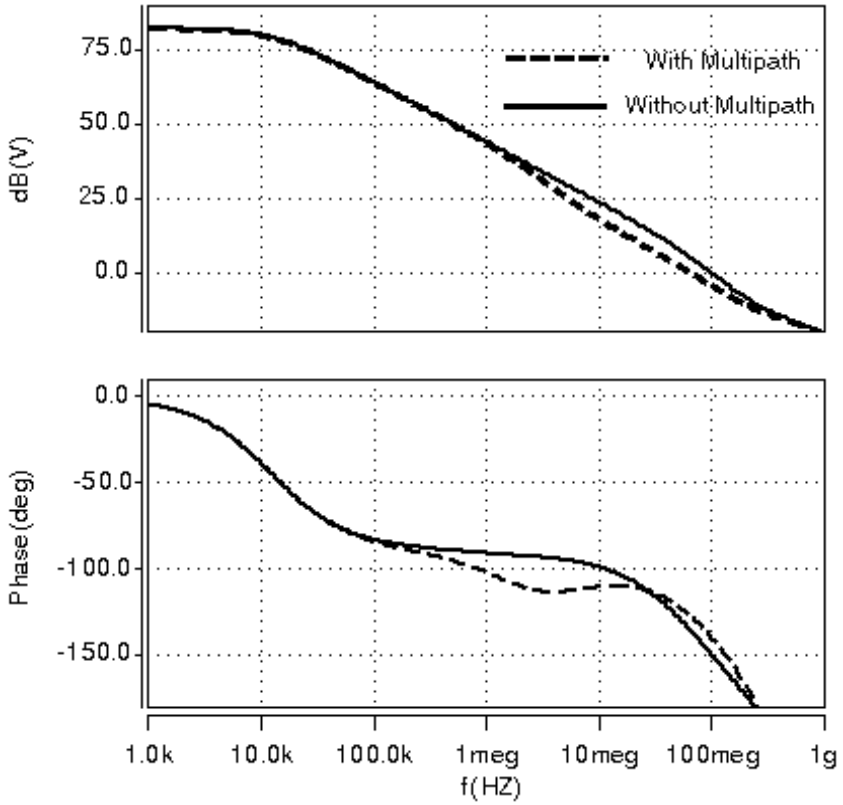


Fig. 3.12 AC response for CMFB Loop: Traditional CMFB (UGB = 100MHz, PM = 24^o) and Multi-path CMFB with I3' = I3'' = I3/2 (UGB = 65MHz, PM = 50^o)

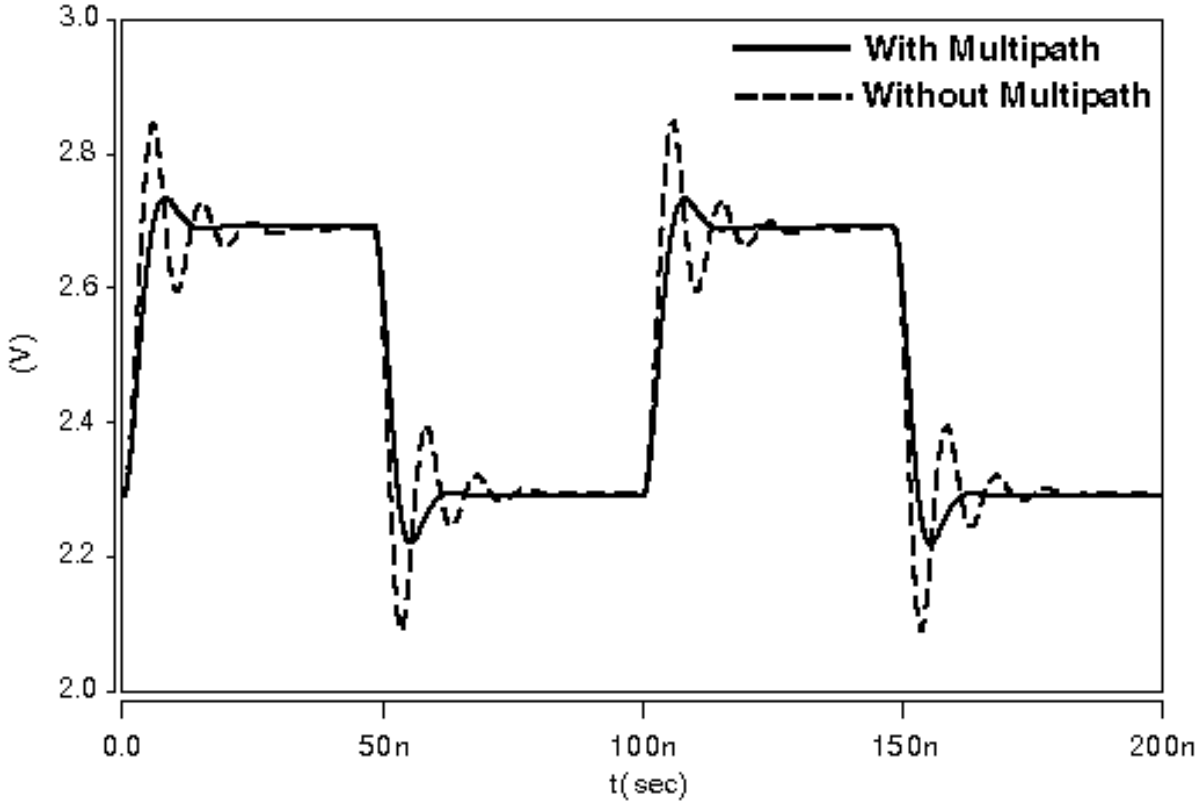


Fig. 3.13. Settling of the common mode output with a 400mV step on V_{REF}

CHAPTER IV
SAMPLING CIRCUITS

4.1 Introduction

In modulators, the amount of noise shaping is governed by the filtering provided by the integrators embedded in one or more stages. Noise injected in the forward path is shaped by the order of the filtering preceding it. All the integrators apart from the first have their imperfections like noise and distortion shaped by an order depending on the number of integrators preceding them. Therefore, the first integrator primarily governs the noise and linearity performance of the entire converter. One of the main causes of distortion in the first integrator is sampling distortion. This chapter focuses primarily on the fundamental problems in achieving high linearity and noise performance in the sampling network of the first integrator.

Usually when used as a switch MOS transistor is operated in triode region or linear region. The equivalent circuit for the transistor is a resistor whose value is controlled by the transistor gate voltage (Fig 4.1). When the switch is closed the value of on-resistance is in range of few ohms to a few kilo-ohms. In contrast, the resistance of an open switch is so high that in practice the switch is an open circuit.

The two critical specifications of the sampling network are sampling noise and sampling distortion. The sampling noise is determined by the value of sampling capacitors and once the capacitor value has been selected usually nothing more can be

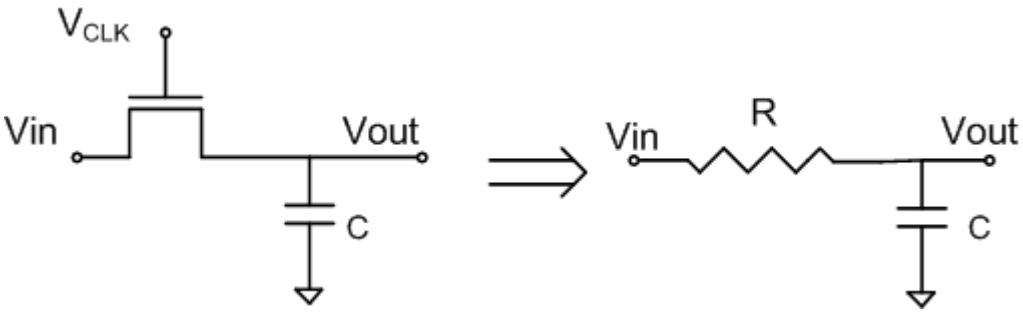


Fig. 4.1. Simplified sampling circuit; “on” switch charging a capacitor C through a resistor R

done about it unless we go for double sampling which gives 3db advantage in SNR [20]. In the next section we discuss the causes of non-linearity in sampling network. Then we look at various techniques to linearize the basic NMOS switch and present simulation results.

4.2 Factors causing non-linearity in sampling circuit

4.2.1 Voltage dependent turn –off moment

A MOS switch turns off when its gate –source voltage becomes less than the transistor threshold voltage. When the switch is on, the source voltage equals the input voltage. As a result of this and finite turn-off slope 'a' of the gate voltage, the delay Δt from the moment when the gate voltage starts to fall to the switch turn-off moment depends on the input voltage. It can be shown [21] that voltage dependent turn –off moment results in second harmonic distortion

$$HD_2 = 20\log\left(\frac{A\omega T_F}{2A_{CLK}}\right) \tag{4.1}$$

where A_{CLK} is the clock amplitude and T_F the clock fall time i.e A_{CLK} /a. There are basically three ways to get around this problem. First making the slope of the clock waveform steep reduces distortion. Second solution is to make the switch control voltage track the input signal. Last solution is to use a circuit topology in which the switch is operated around a constant voltage. This last technique has been used in the design example and is discussed in detail later.

4.2.2 Charge injection

A conducting MOS switch has a finite amount of mobile charge in its channel. When the transistor is turned off, this charge is distributed between the source, the drain, and bulk terminals of the device. To design accurate SC circuits the nature of this charge injection and redistribution phenomenon must be understood. Through the years the charge injection has been analyzed and discussed in various papers [22, 23, 24]. The amount of total inversion layer charge is dependent on the voltage V_{IN}

$$Q_{tot} = \mu C_{ox} WL(V_G - V_{IN} - V_T) \tag{4.2}$$

As the transistor is turned off, a part of inversion layer charge is leaked to the substrate. This phenomenon, known as charge pumping, is due to two effects, the capture of charge by interface traps and recombination in the channel and substrate. The substrate leakage occurs only when the gate voltage turn-off slope is extremely steep or the transistor channel is very long, and thus in practical switches this effect can be ignored. The distribution of charge is dependent on the impedance seen on both sides, the impedance of the driver and the clock waveform. When the transistor is turned off rapidly, the channel is cut-off before the potential difference between drain and source has time to even out and, as a result, the channel charge is equally divided between the source and drain terminals. On the other hand, a slow turn-off leaves time for the source and drain voltages to become equalized, which results in charge partitioning according to the impedance ratio.In practice, the charge injection has a non-linear component, which results in harmonic distortion. One of the techniques to minimize the effect of charge injection distortion is to use a technique called bottom plate sampling in which a constant amount of charge is injected regardless of the input. This technique has been used in the design and discussed in detail later.

4.2.3 Nonlinear time constant

When the input the signal amplitudes are large, accuracy and signal bandwidth are limited by distortion, which originates from the fact that switch on-resistance and stray capacitances are not constant but vary as functions of drain and source voltages. For a short channel device the on-resistance is [21]

$$R_{on} = \frac{1 + \frac{V_D - V_S}{E_C L}}{C_{ox}\mu_{eff}\frac{W}{L}\left[V_G - \frac{V_s}{2} - \frac{V_D}{2} - V_{To} - \gamma\left(\sqrt{V_S - V_B - 2\phi_F} - \sqrt{2\phi_F}\right)\right]} \tag{4.3}$$

where V_G, V_S, V_D and V_B are the voltages on the transistor's gate source drain and bulk terminals. By looking at the equation three different signal-dependent terms can

be identified. The first and most dominant term is the gate channel voltage V_G – $(V_S+V_D)/2$ in the denominator. The second term is the threshold voltage dependency on the source-bulk voltage (bulk effect) modeled with square root term in the numerator. Last term is the term in the numerator, which depends on the drain-source voltage, the critical electric field E_c and the device channel length.

The dominant non-linear parasitic capacitances are drain and source junction capacitances, which are given by

$$C_{jbx} = C_{j0} \cdot \left(1 - \frac{V_B - V_x}{V_o}\right)^{-M_j} \tag{4.4}$$

Where V_x is the drain or source voltage, C_{j0} is the junction capacitance with zero bias, V_o the bulk junction potential and M_j the bulk junction grading coefficient. There are basically two ways to reduce distortion: decreasing the absolute value of the time constant and making the time constant less non-linear.

4.3 Distortion analysis and design trade-offs

In the design of the sampling network signal to noise ratio (SNR) and total harmonic distortion (THD) requires opposing design parameters. For the switch in Fig 4.1. it is easily shown that the noise power is given by $v_n^2 = \frac{kT}{C}$, thus $SNR \ \alpha \ A^2 C$, where A is amplitude of input signal. Thus to increase SNR we must increase the sampling capacitor or increase the input amplitude. We next analyze how varying the sampling capacitor and input amplitude affects the THD.

The switch in the "on" state is modeled as a non-linear resistor dependent on input signal as

$$R = f(v_i) = Ro(1 + r_1 v_i + r_2 v_i^2 + ...) \tag{4.5}$$

This is illustrated in Fig 4.2. The capacitor is assumed to be linear, which is a good assumption, if we are using poly-poly or lateral flux capacitors.

$$V_o = v_i - V_{error} \tag{4.6}$$

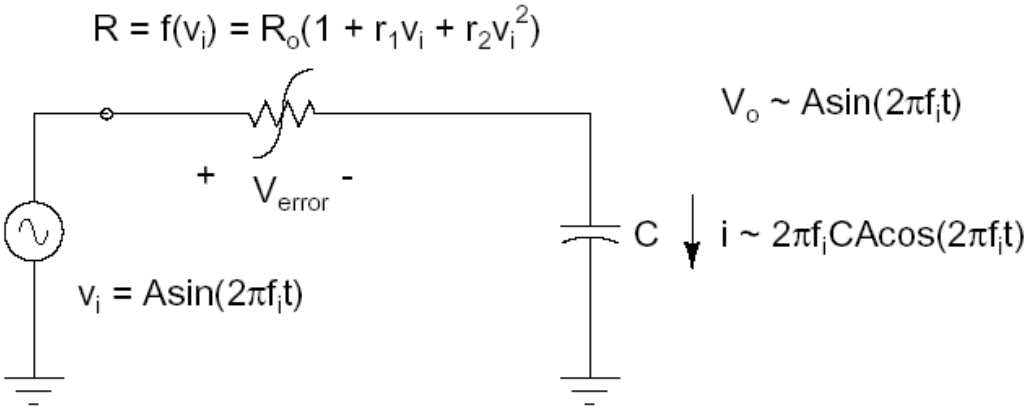


Fig. 4.2. Non-linear switch model

For estimation of distortion let us assume $V_{error} << V_o$, then

$$I_C \approx C\frac{dv_i}{dt} = 2\pi Af_iC\cos(2\pi f_i t) \tag{4.7}$$

$$V_{error} = RI_C = Ro(1 + r_1 v_i + r_2 v_i^{\,2})I_C \tag{4.8}$$

Substituting $v_i = A\sin(2\pi f_i t)$, we get

$$V_{error} \approx R_o\omega_i CA\cos(\omega_i t) + \frac{R_o r_1 \omega_i CA^2}{2}\sin(2\omega_i t) + \frac{R_o r_2 \omega_i CA^3}{4}\sin(3\omega_i t) \tag{4.9}$$

Since $V_o = v_i - V_{error}$, for V_o we get

$$HD_2 \approx \frac{R_o r_1 \omega_i CA}{2} \;;\quad HD_3 \approx \frac{R_o r_2 \omega_i CA^2}{4} \tag{4.10}$$

For fully differential circuits, HD_3 is the main concern for linearity. From the equation above we observe we note that to reduce HD_3 we can reduce C or A. This will lead to a reduction in SNR. If SNR is to be maintained constant, reducing the input amplitude will not reduce HD_3. So for constant SNR

$$HD_3 \;\alpha\; CA^2\omega_i R_o r_2 = (SNR)\omega_i R_o r_2 \tag{4.11}$$

Reduction in input signal frequency will reduce the harmonic distortion, but that is not a solution, as input signal frequency is a specification and cannot be changed. So there are only two possible solutions. The first is to reduce the absolute value of resistance (Ro). This entails increasing the switch size, with an associated increase in parasitic capacitance. Other alternative is to reduce r_2 i.e make the switch more linear. This is generally the preferred method. The switch size is chosen only, as large as is needed to meet the bandwidth requirement (see section 4.5). In next section we look at various approaches to linearize the sampling switch.

4.4 Linearizing the basic switch

Here we look at four different approaches used in literature to linearize the basic switch.

- **CMOS switch or transmission gate**: The commonly used switch, the transmission gate (Fig 4.3) can be considered a linearized circuit; as the signal voltage rises the increase in the on-resistance of the nMOS transistor is compensated by the decrease in pMOS on-resistance and vice versa. Similarly, as the voltage rises, the drain and source junction capacitances of the nMOS decrease, while in the pMOS the opposite happens. The relative sizing of the transistors can be optimized in order to minimize distortion, however it is rather sensitive to process parameters and thus it is not same in different process corners. Consequently, size optimization can yield only moderate linearity improvements.

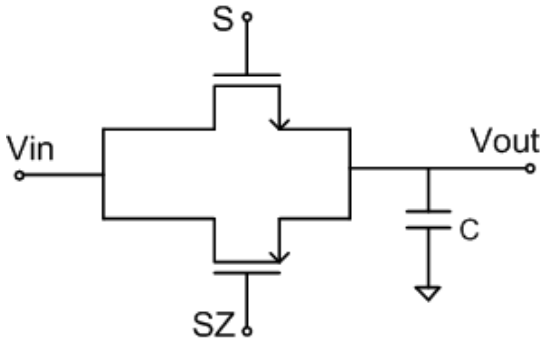


Fig. 4.3. CMOS switch / transmission gate

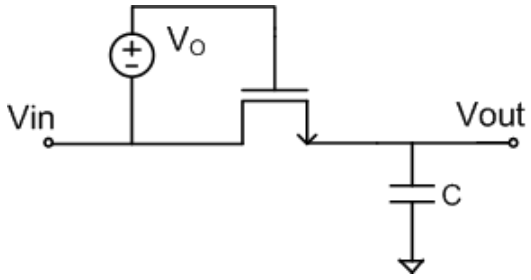
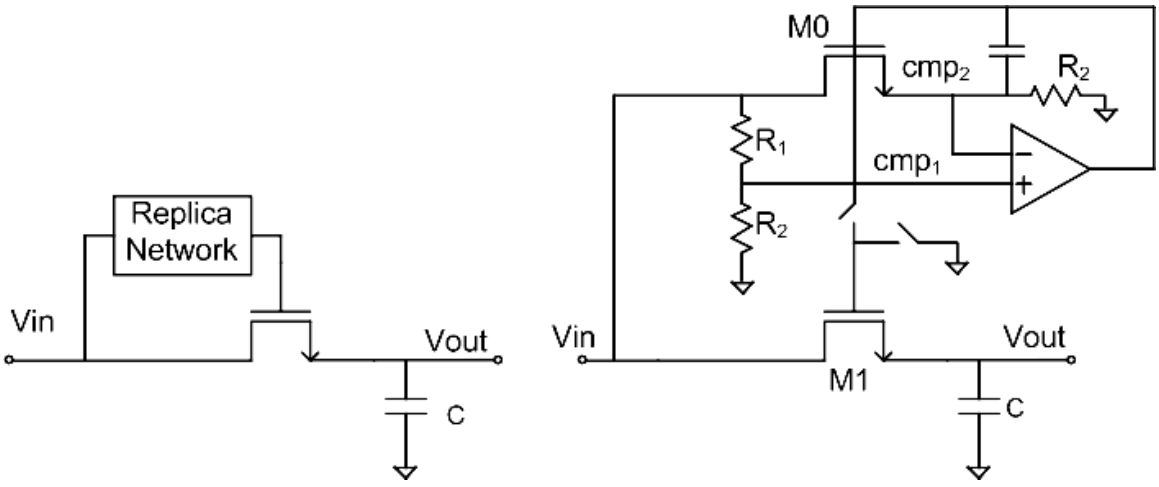


Fig. 4.4. Bootstrapped switch

- **Gate voltage bootstrapping:** The idea is to make the gate voltage track the input voltage with an offset Vo, which is, at its maximum, equal to supply voltage. This technique, called bootstrapping [25], is illustrated in figure 4.4, where a closed switch with a gate voltage with V_{IN} + V_O is shown. The switch gate source voltage in this circuit is constant and thus a major source of non-linearity in (4.4) is greatly attenuated, but something still needs to be done about the non-linear bulk effect. This technique has been implemented in this design and is discussed in detail later.
- **Replica sampling network:** The basic idea is maintain constant on-resistance of switch M1 rather than a constant V_{GS} as illustrated in Fig 4.5a. [20] Thus this approach eliminated the bulk effect also. In the implementation shown in Fig 4.5b the amplifier drives the gate voltage of M0 to maintain the equality of node voltages cmp2 and cmp1. This forces the resistance of M0 to be equal to R_1 for signal frequencies within the loop bandwidth of the loop formed by the amplifier, device M0, and resistor. It could hence be inferred from this scheme that there is a direct relationship between the amount of linearization of M0 and the loop bandwidth. The issue of meeting the open-loop linearity of a sampling network has thus been translated to a bandwidth issue.



(a) (b)

Fig. 4.5. Replica sampling network (a) The basic idea (b) Implementation

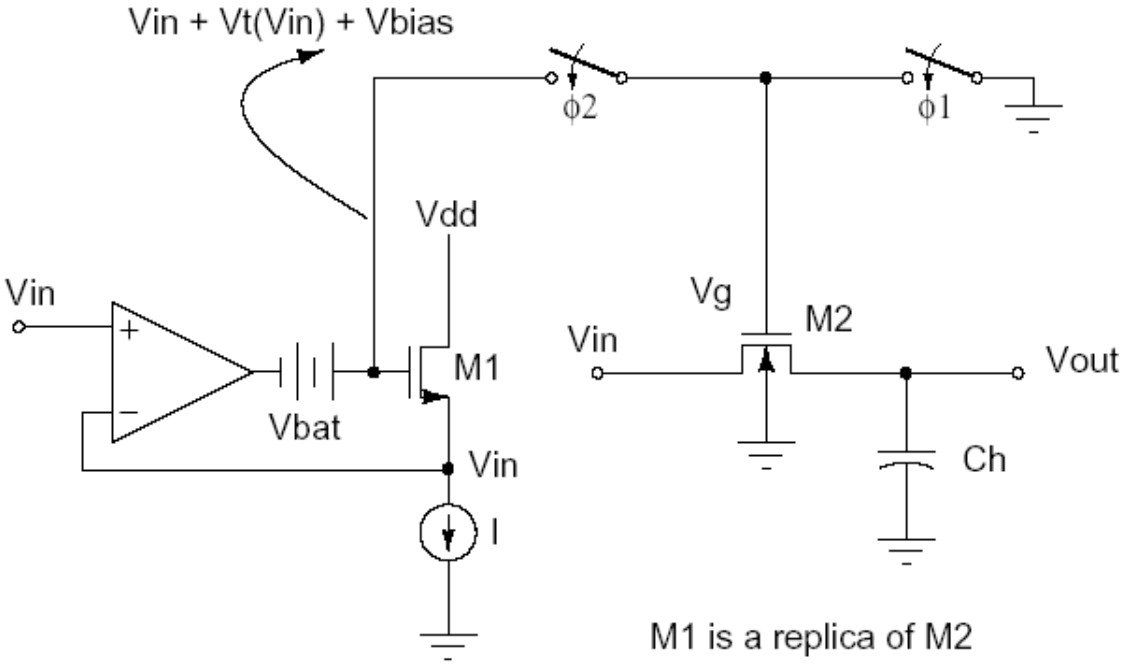


Fig. 4.6. Replica gds technique

Replica 'gds' technique : The scheme is shown in Fig 4.6 [26] . The nMOS sampling switch $M_1$is turned ON with the gate voltage of a replica FET M_2 carrying a constant current. The opamp forces the source of M2 to track the analog input. Thisway, the sampling switch copies the 'ron' of the replica, held constant by the fixed bias current. When the sampling switch turns off, the dummy switch Md switches in to balance the loading of the op amp.

4.5 Literature survey of performance

Since input switch is critical for achieving a high THD performance in any high speed/ high performance ADC many of published ADC's have employed some techniques to improve the performance of switch. But in most of the papers the performance achieved by the switch is not reported separately, so to make a comparison we can look at the SNDR numbers of reported ADC's. This is summarized in Table 4.1.Wherever the performance of switch is reported it is shown in Column 5 with the topology of switch in Column 6.

Most relevant comparison is with broadband sigma-delta ADC's with input signal frequencies > 1Mhz. Since many of the switch bootstrapping techniques have been developed initially for pipelined ADC's, a summary is provided for performance of pipelined ADC's with input signal frequencies > 1MHz in Table 4.2. The performance of the ADC's in terms of SNDR is inferior to those in Table 4.2, but the signal frequencies is generally higher. The targeted specifications for these ADC's are SFDR and hence they need linear switches. Besides the switches reported in ADC's in Table 4.1 & Table 4.2 some other switch topologies have been suggested in [43]-[45].

Table 4.1.Comparison table of reported switched capacitor broadband sigma-delta ADC's

Reference	Input signal frequency	SNDR	Technology	Switch THD (Simulated)	Switch topology
[20]	1.1Mhz	88dB	0.18u/0.35u 1.8V/3.3V CMOS	122dB@1.1Mhz 105dB@5Mhz	Replica bridge network
[27]	2Mhz	87dB	0.25u, 2.5V CMOS	102dB@2Mhz	Bootstrapped switch reported in [31]
[28]	1.25Mhz	87dB	0.5u, 5V CMOS	99db@1Mhz	Low Vt (+/-0.3V) transistors Transmission gate
[29]	1.25Mhz	88dB	0.6u,5V CMOS	98dB@1Mhz	Bootstrapped switch
[30]	1.25Mhz	89dB	0.65um, 5V CMOS	NA	NA
[31]	2Mhz	82dB	0.18u, 1.8V CMOS	NA	NA
[32]	100kHz	100dB	0.25u,CMOS	NA	NA
[33]	2.5Mhz	72dB	0.18u, CMOS	NA	Bootstrapped switch
[34]	1.1Mhz	80dB	0.13u, 1.5V CMOS	NA	Bootstrapped switch reported in [31]
[35]	1.5Mhz	71dB	0.18u,1.8V CMOS	NA	Bootstrapped switch reported in [36]
[37]	2.5Mhz	88dB	0.35u, 3V/5V CMOS	NA	Bootstrapped switch

Table 4.2. Some pipeline ADC's with improved switches reported in literature

Reference	Input signal frequency	SNDR	Technology	Switch THD	Switch topology
[25]	100kHz	58.5dB	0.6u, 1.5V CMOS	NA	Signal dependent boost
[38]	6Mhz	-	0.35u,3V	>100db@6Mhz	Variation of [25]
[26]	1Mhz	64dB	0.6u,3.3V CMOS	NA	Bootstrapped with feedback
[39]	15Mhz	75dB	0.25u, CMOS	NA	Improvement of [26]
[40]	1Mhz	73.6dB	0.18u, 1.8V CMOS	> 95dB @5.1Mhz	Techniques in [25] & [26]
[41]	5Mhz	28dB	0.5u, 5V CMOS	NA	NA
[42]	Upto 60Mhz	58.2dB@10Mhz 54.1dB@50Mhz	0.25u, 2.5V CMOS	NA	NA

4.6 Design example

In this example we look at design of a switch with a target SNDR of 100dB for >1Mhz input signal. The design implemented in this example is the bootstrapped switch with the implementation similar to [38]. The idea is to have a constant V_{GS} regardless of input, as suggested in Fig 4.4. The switched capacitor implementation of bootstrapping is shown in Fig 4.7.

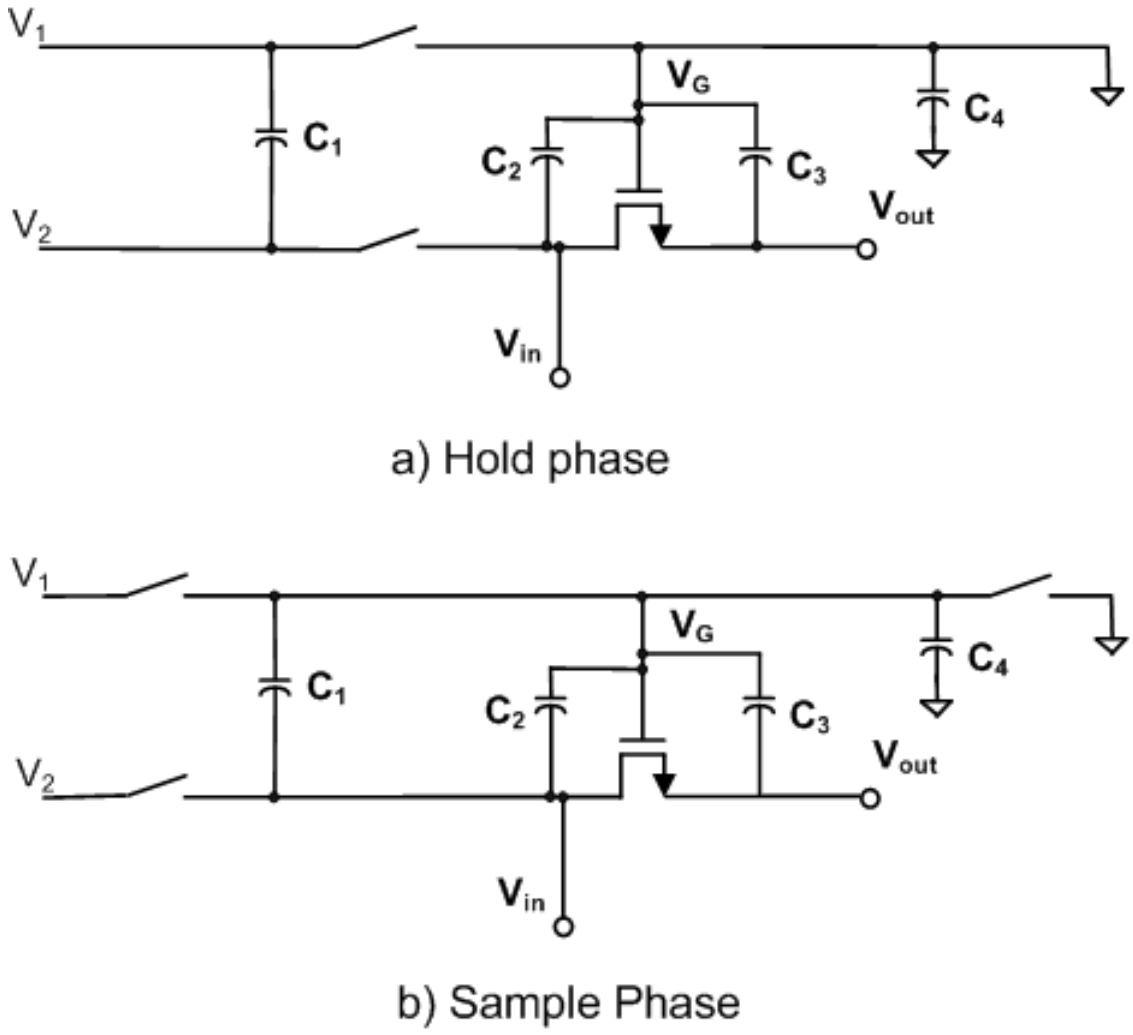


Fig. 4.7. Switched capacitor implementation of Bootstrapped switch

During the hold phase the capacitor C1 is precharged to V1 –V2. To turn the switch on, the capacitor is switched between the input voltage and the transistor gate. The gate voltage however is not the sum of the input voltage and the precharge voltage, since the parasitic capacitances associated with the switch transistor and auxiliary switches will cause some distortion.

The gate voltage is given by

$$V_G = (V_1 - V_2) + V_{in}(t) - \frac{C_4 V_{in}(t)}{C_{tot}} - \frac{C_2 V_{in}(t_o)}{C_{tot}} - \frac{C_3 V_{out}(t_o)}{C_{tot}} \qquad (4.12)$$

The first two terms are the desired ones, while the other two are unwanted. In order to minimize distortion, the parasitic capacitances have to be minimized and the bootstrapping capacitance made large.

The actual implementation of the circuit is similar to [38] and is shown in Fig 4.8. The circuit in Fig 4.8 still suffers from the non-linearity due to bulk effect. One possibility to eliminate bulk effect is to make the bulk voltage track the input during the sample phase, implementation is shown in Fig 4.9.

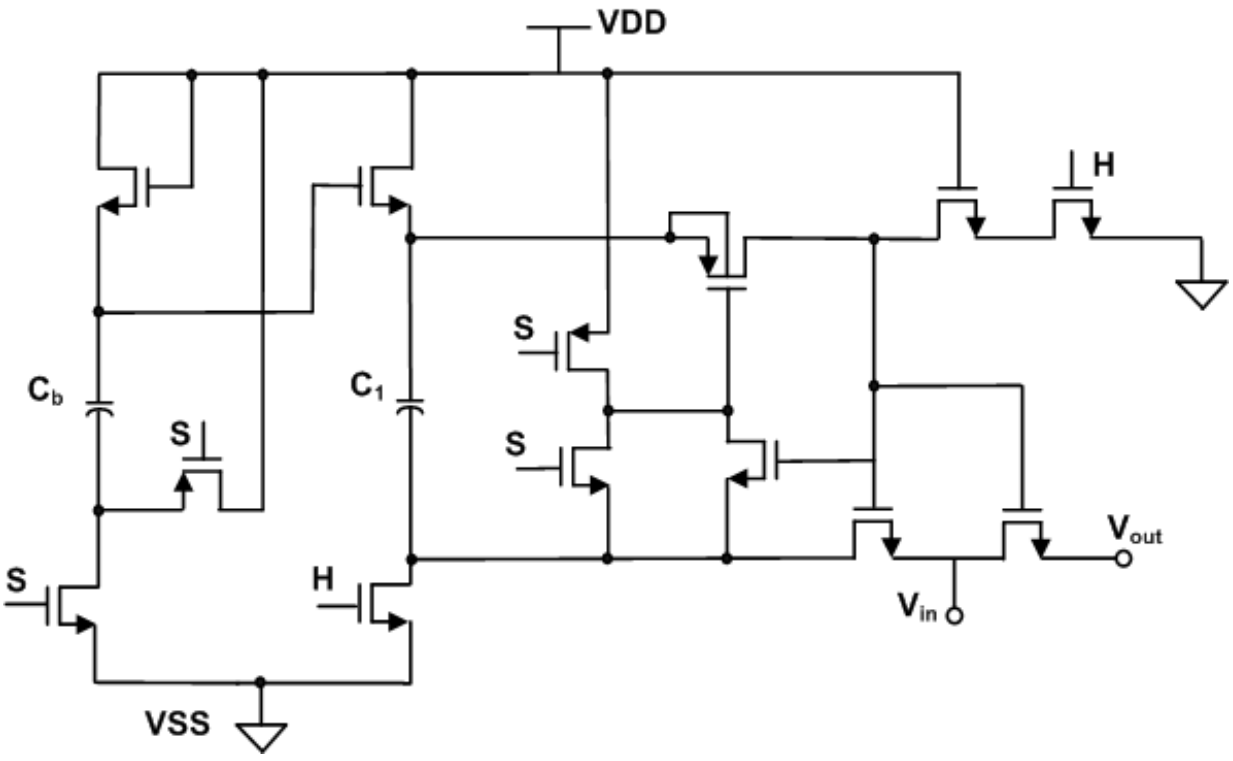


Fig. 4.8. Implementation of bootstrapped switch (C1 is the bootstrapping capacitor)

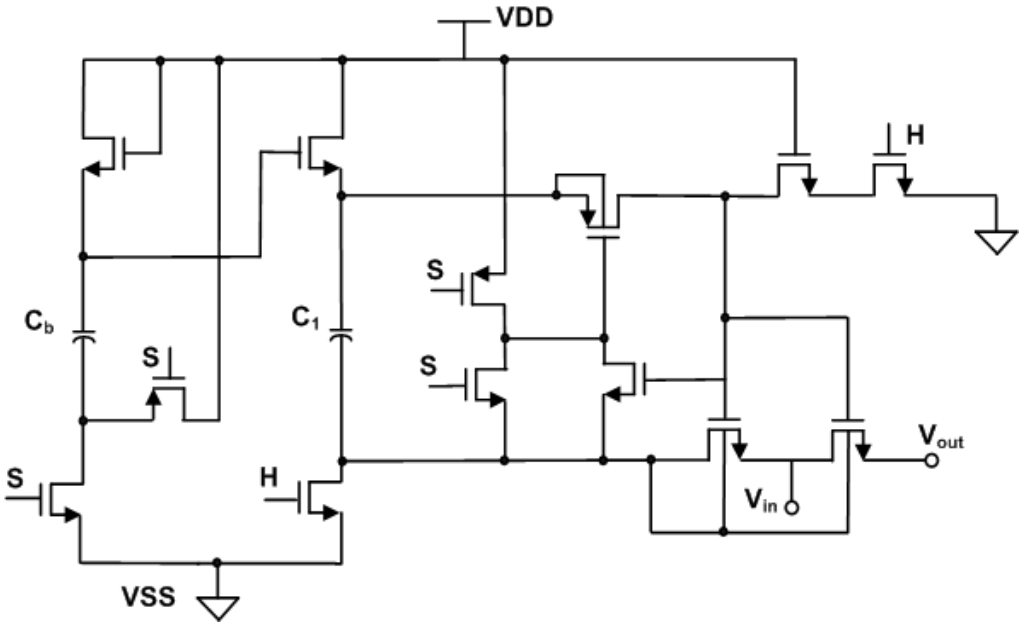


Fig. 4.9**.** Implementation of bootstrapped switch with bulk effect eliminated

Schematic of a typical switched capacitor integrator is shown Fig 4.10, with the sampling network implemented shown separately in Fig 4.11 with the timings for S, H and SP illustrated in Fig 4.12.

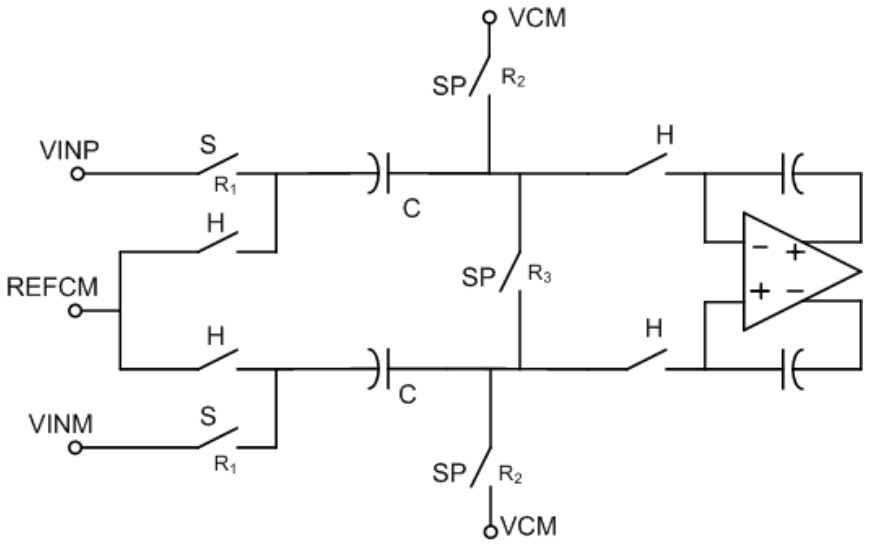


Fig. 4.10. A typical switched capacitor integrator

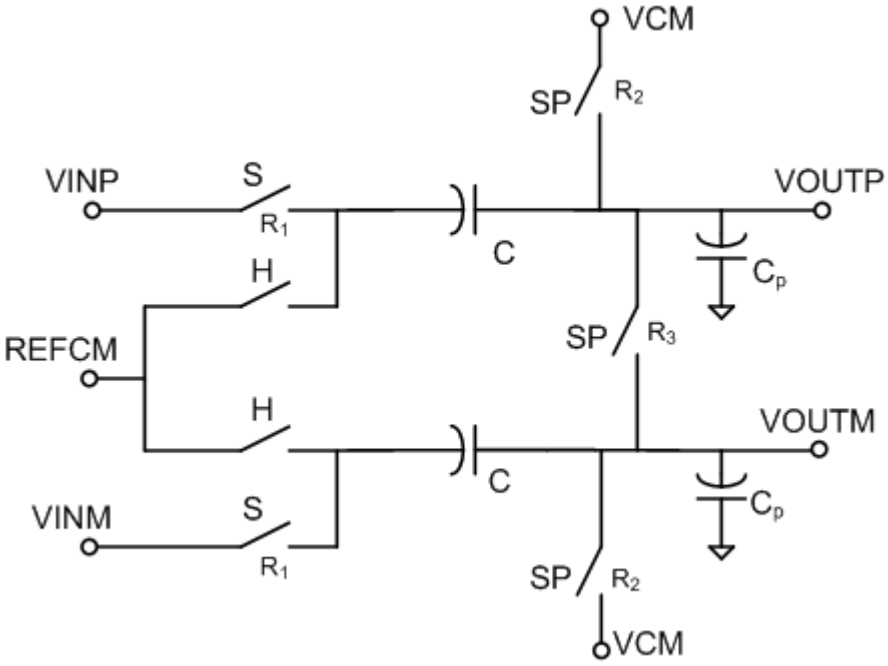


Fig. 4.11. Sampling circuit

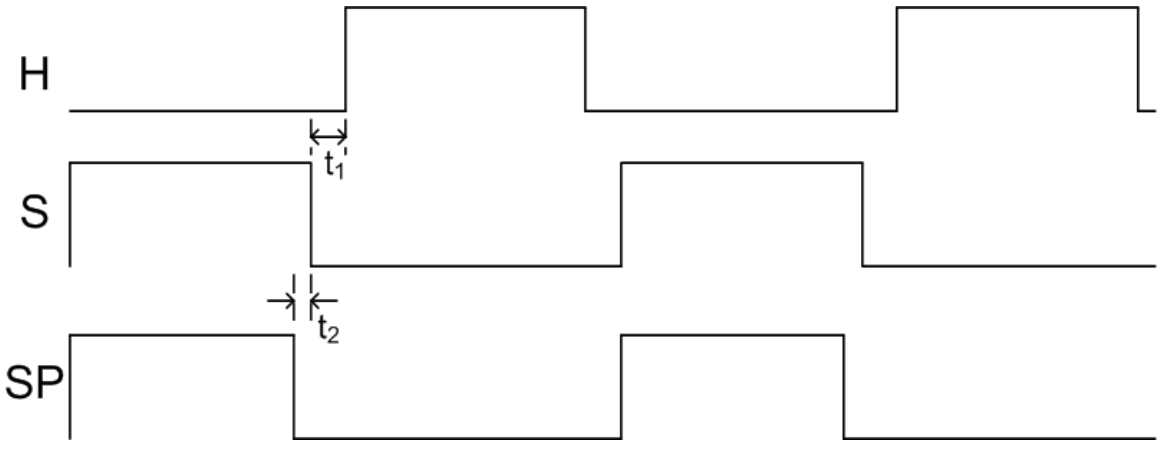


Fig. 4.12. Clock timings (a) illustrating the non-overlapping nature of S/ H and bottom plate sampling

Bottom Plate Sampling: The idea in bottom plate sampling is to make SP fall previous to S. Since once SP falls nodes 'Voutp' and 'Voutm' are floating the charge injection of S switch doesn't effect he sampled value. The charge injection of SP switch is constant regardless of input because it is always connected to VCM.

Next we consider the procedure for determining the switch sizes. Let us assume that the switch S is accurately modeled as a clock-voltage dependent resistor. When 'S' is high switch is considered to be on, with a resistance 'R'. When 'S' is low, the switch is considered to be off with and to have an infinite resistance.(Fig 4.1)

During the sample mode the input is connected across the capacitor through the switch. To find the acquisition time, t_a, the circuit can be modeled as a low-pass filter whose input turns on at time t = 0:

$$v_{in}(t) = \begin{cases} 0 & if \quad t < 0 \\ A\cos(\omega t) & \text{if } t \geq 0 \end{cases} \tag{4.13}$$

$$v_o(t) = -A\left[\frac{\alpha^2}{\alpha^2+\omega^2}\right]e^{-\alpha t} + A\left[\frac{\alpha^2}{\alpha^2+\omega^2}\right]\cos(\omega t) + A\left[\frac{\alpha\omega}{\alpha^2+\omega^2}\right]\sin(\omega t) \tag{4.14}$$

$$where \quad \alpha = \frac{1}{RC}$$

The first term in the equation represents the error made in the sampling because of non-zero acquisition time. This error decays exponentially with increasing time; the time constant is equal to $1/\alpha$ = RC. For inputs of any frequency, the magnitude of the coefficient of the first term is

$$A\left[\frac{\alpha^2}{\alpha^2+\omega^2}\right] \leq A \tag{4.14}$$

For a full-scale input, to limit the magnitude of the acquisition-time error to +/-1/2 LSB at a N-bit level

$$Ae^{-\alpha t} \leq \frac{2A}{2^{N+1}} \tag{4.15}$$

this implies $t \geq t_a$ where $t_a = N(RC)\ln(2)$

For an example design N =20, C =30pF, t = 10ns

$$R \le \frac{t}{NC\ln(2)} = \frac{10e-9}{20*30e-12*\ln(2)} = 24$$

Thus we choose **R = 24**

For the sampling network in Fig 4.11 effective resistance $R = R1 + (R_2 \parallel R_3/2)$

We can choose $R_2 = 10*R_3$; $R \approx R_1 + R_3/2$

Having a small SP switch helps reduce error due to charge injection thus R_3 is chosen larger than R_1; we choose R_1= 6 , R_3=36; VCM is assumed to have a maximum value of 1.5V i.e $(V_t + 2V_{on})$. With this assumption SP switches can be taken as NMOS only switches. Having a shorting SP switch helps reduce error due to differential charge injection.

Thus $R_3 = \frac{1}{\mu_n C_{ox}(W/L)(V_{GS} - V_T)}$ where (W/L) is aspect ratio for NMOS switch.

Sampling switch S is implemented with the topology in Fig 4. 9.

From equation (4.12) we know that choosing a large value of bootstrapping capacitor helps reduce distortion. But since a large capacitor means a large area and also a strong gate driver, we need to minimize the capacitor we can use for bootstrapping without sacrificing linearity.

Fig 4.13 shows the modulation of gate source voltage and the 'on' resistance by the input for a bootstrapping capacitor C1 = 4pF. Ideally we want the gate source voltage to be a constant equal to 5V.

Fig 4.14 shows the modulation of gate source voltage and the 'on' resistance by the input for a bootstrapping capacitor C1 = 8pF. Comparing Fig 4.13 with Fig 4.14 we observe that VGS has increased by 0.5V.

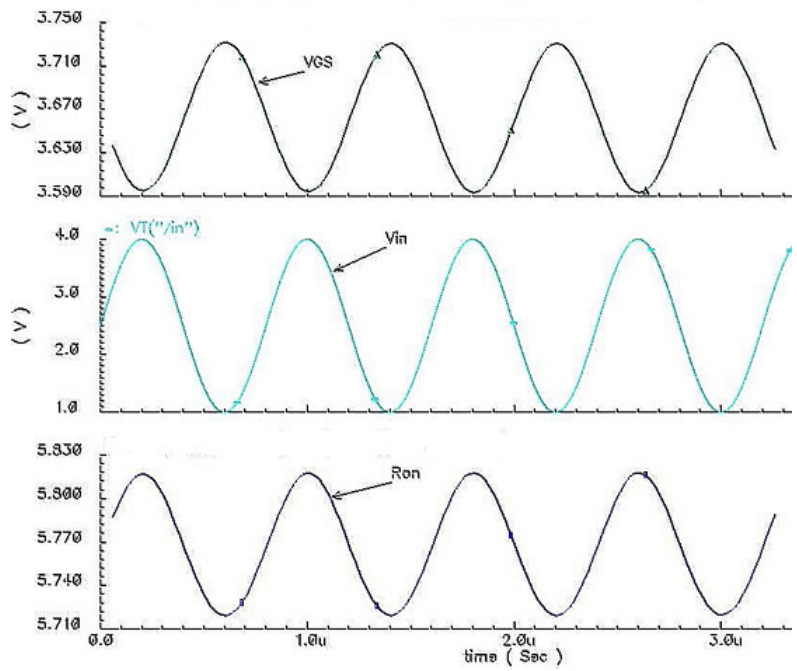


Fig. 4.13. Variation of gate source voltage and 'on' resistance with input (C1 = 4pF)

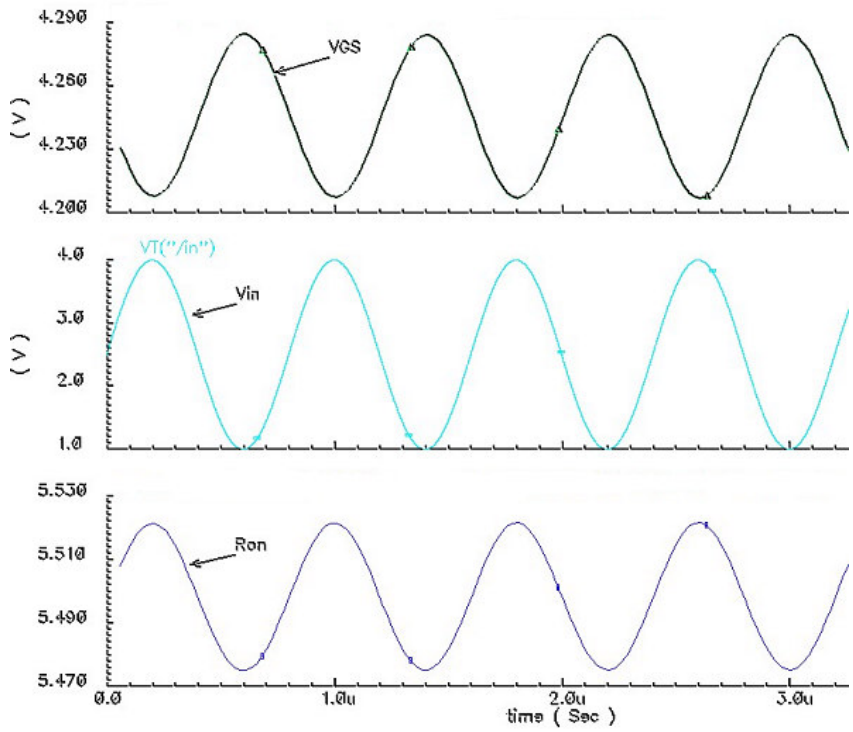


Fig. 4.14. Variation of gate source voltage and 'on' resistance with input (C1 = 8pF)

We want to determine how non-linear is Ron , so we take a FFT of the Ron waveform the result is shown in Fig 4.15. From the plot we obtain

$$R_o = 5.498 \qquad R_O r_1 A = 23.2m \qquad \frac{R_O r_2 A^2}{2} = 152.6\mu$$

Using the results from Section 4.3 we calculate the expected value of HD3 as

$$HD_3 \approx \frac{R_o r_2 \omega_i C A^2}{4} = \frac{152.6\mu * 6.28 * 1.25e6 * 25e-12}{2} = -156dB$$

To decide on the value of C1 a graph of THD Vs bootstrapping capacitor C1 is obtained, which is shown in Fig 4.16. From the figure we obtained that THD improves as the C1 is increased but after 4-5pF THD almost becomes constant. So for this design C1 was chosen as 4pF. Fig 4.17 shows a typical spectrum of the sampled signal. The variation of THD with input frequency is illustrated in Fig 4.18, with a sampling capacitor of 25pF. Analysis in section 4.3 predicted a 6db/octave degradation with input frequency, but the simulation results shows that degradation is much more rapid.

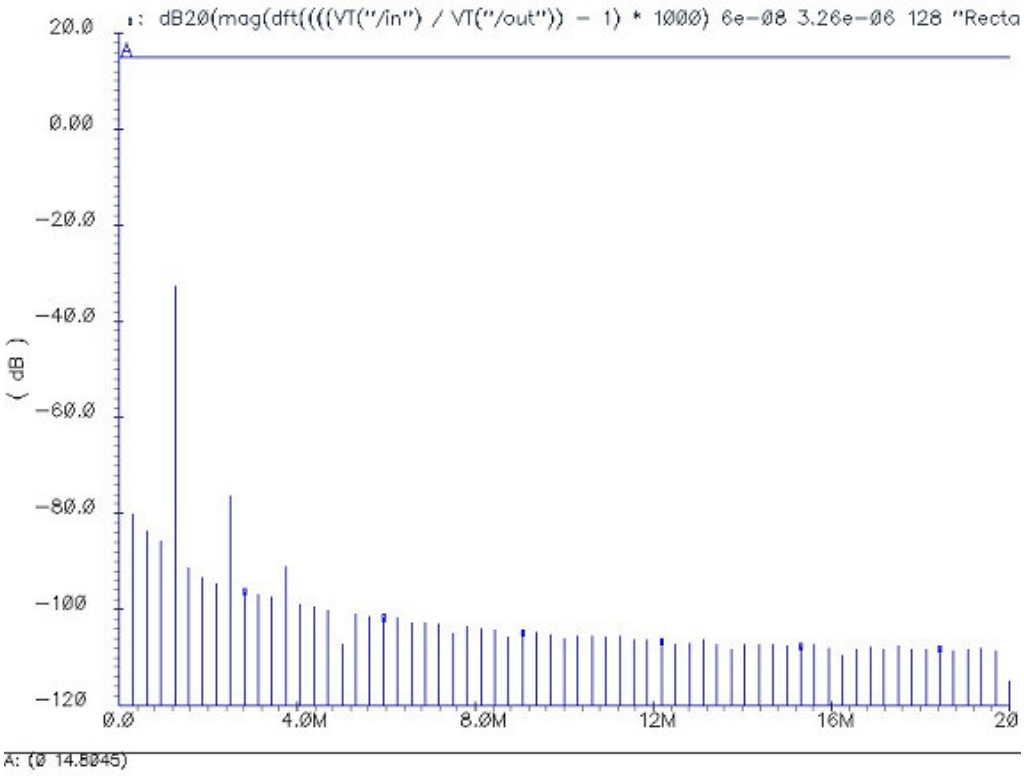


Fig. 4.15. Determining coefficients for 'ron'

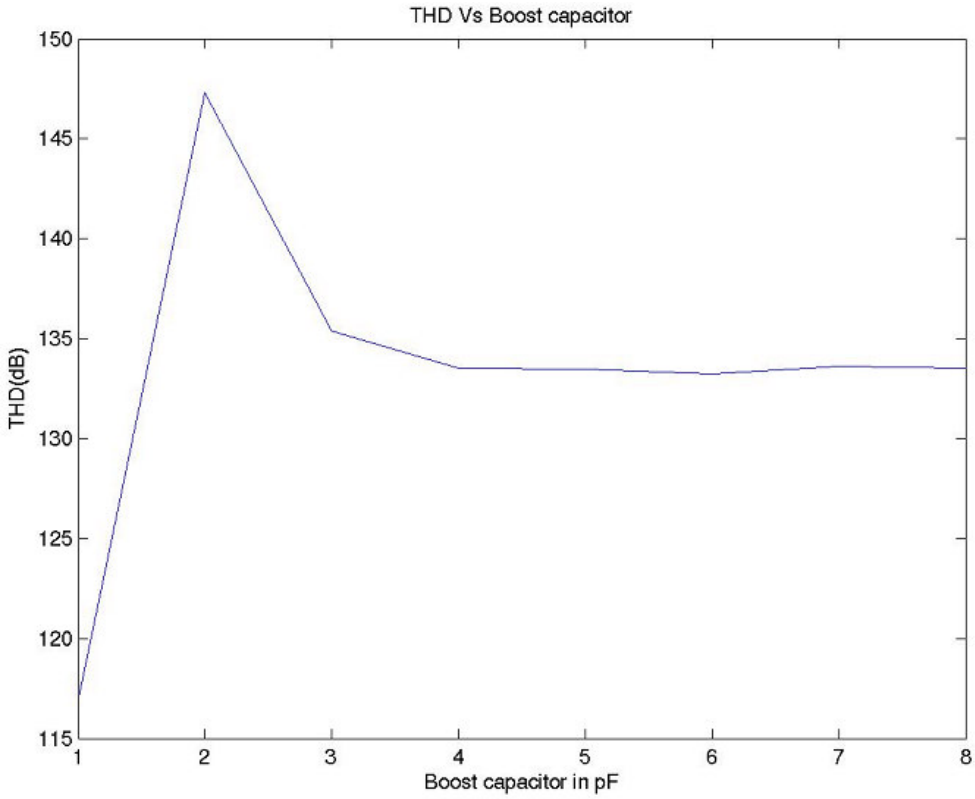


Fig. 4.16. Dependence of THD on bootstrapping capacitor C1.

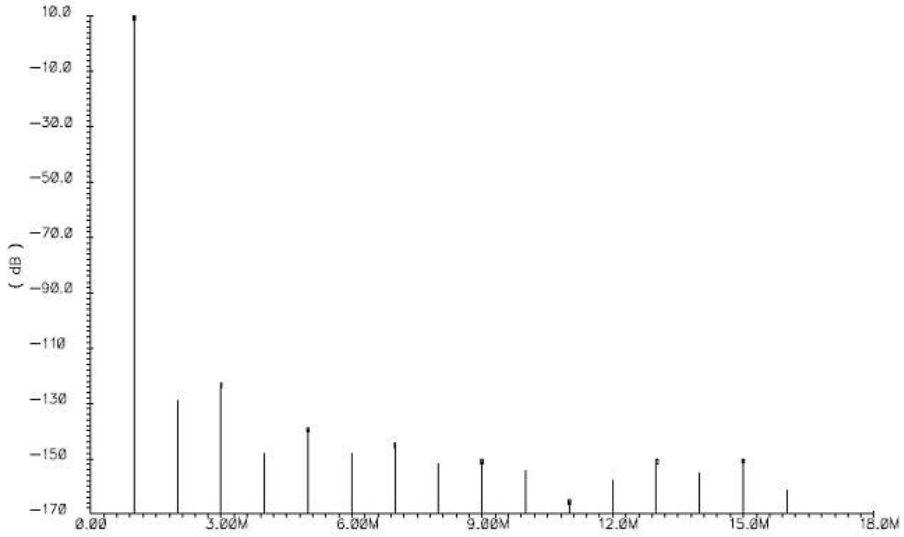


Fig 4.17. Typical spectrum of sampled signal (THD = 132dB)

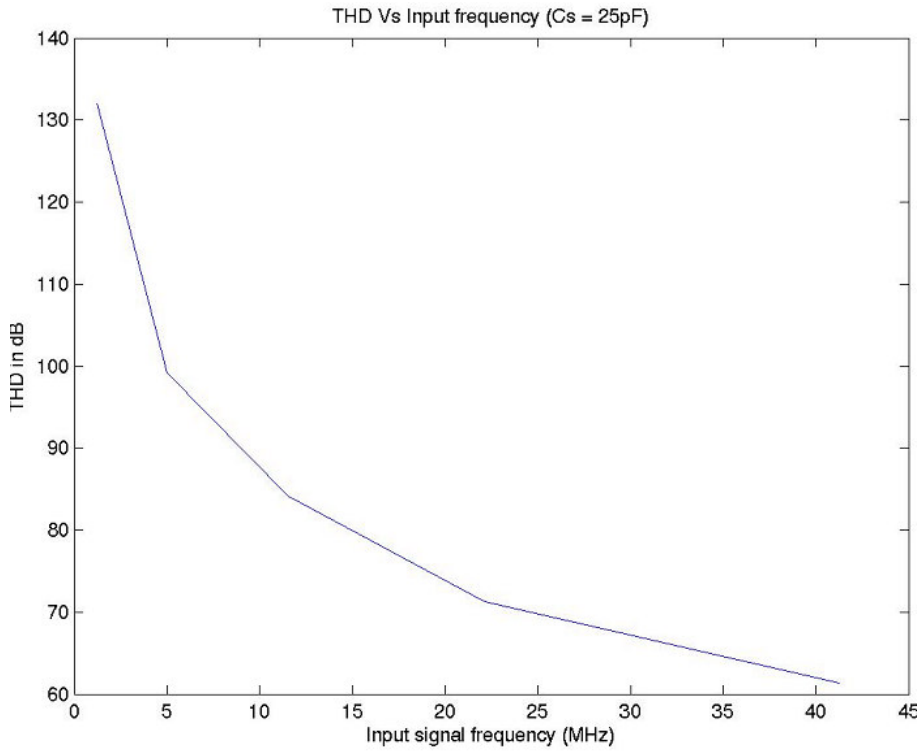


Fig. 4.18. Variation of THD with input frequency

CHAPTER V
SECOND ORDER DYNAMIC ELEMENT MATCHING TECHNIQUES FOR LOW OSR SIGMA-DELTA ADC*

5.1 Introduction

High-resolution delta sigma ADCs with low OSRs have been designed for broadband communication applications [27,32,37,46]. All these ADCs use multi-bit DACs in the first stage feedback path, to achieve high signal to quantization noise ratio. The mismatch in the DAC limits the linearity of the overall ADC. First order dynamic element matching (DEM) techniques have been used to improve the linearity and to shape the DAC mismatch noise out of base-band. The first order DEM techniques used are all variation of Data Weighted Averaging (DWA) technique [47]. The SNDR of these converters has been limited to about 90dB with exception of [32]. To achieve greater than 100dB SNDR (OSR <= 8), with first order DEM, we need to have extremely good element matching (<0.05%).

One approach to achieve the above performance would be to use digital calibration to eliminate the DAC mismatch errors [48]. Another possibility is to use a combination of digital calibration and first order DEM where digital calibration is used to correct the mismatch to less than 0.02% and then use first order DEM to shape out the remaining DAC noise. The third approach would be to use a higher order DEM that is analyzed in this chapter. A previous work [49] analyzes all the existing DEM techniques for low OSR ADC's and claims that at low OSR (OSR <=16) the effectiveness of second-order algorithms in suppressing the errors is no better than first order algorithms. In this paper we analyze second order DEM techniques for low OSR and show results that prove that it can give better performance, if a modified noise transfer function NTF is used.

Section II discusses the performance limitations of first order DWA. Section III analyzes the second order DEM techniques. Section IV proposes a modified second order

* Part of this chapter has been reprinted from "Second Order Dynamic Element Matching Techniques For Low OSR Sigma-Delta ADC," by A.K.Gupta , E.Sanchez-Sinencio, S.Karthikeyan, W.M. Koe and Y.I. Park, May 2006, Proc. IEEE ISCAS, pp.2973-2976. Copyright IEEE, 2006.

DEM that gives significantly improved SNDR performance for low OSR ADCs. The architecture of the ADC chosen is such that the quantization noise is well below 100dB. DEM is incorporated in first stage DAC that has 16 unit elements.

5.2 Evaluation of first order DEM

Data weighted averaging: The DWA algorithm is an element rotation algorithm, which aims to make the long-term, average use of each unit element in the DAC same, by rotating the pattern of unit elements. In Figure 5.1 we consider a DAC with 8 unit elements. Let the first code be 2, and then elements 1,2 will be used. Let the next code be 3, the elements used are 3,4,5. If the next code is 5, then elements 6-8 are used, then we wrap around and use elements 1,2. This we use all components sequentially, and as often as possible.

It is well known that DWA gives first order noise shaping, but at the same time it suffers from tones in the base band [37]. To alleviate this problem a number of techniques have been proposed [27,32,37,46,47,50], but the basic idea remains that we need to add some randomization to break the cyclic nature of DWA. As the amount of randomization is increased the tones disappear but the noise floor increases, since the energy contained in tones is distributed from dc to fs/2. Randomization proposed in [50] *RnDWA* chooses a random pointer location after every cycle is completed, while the one

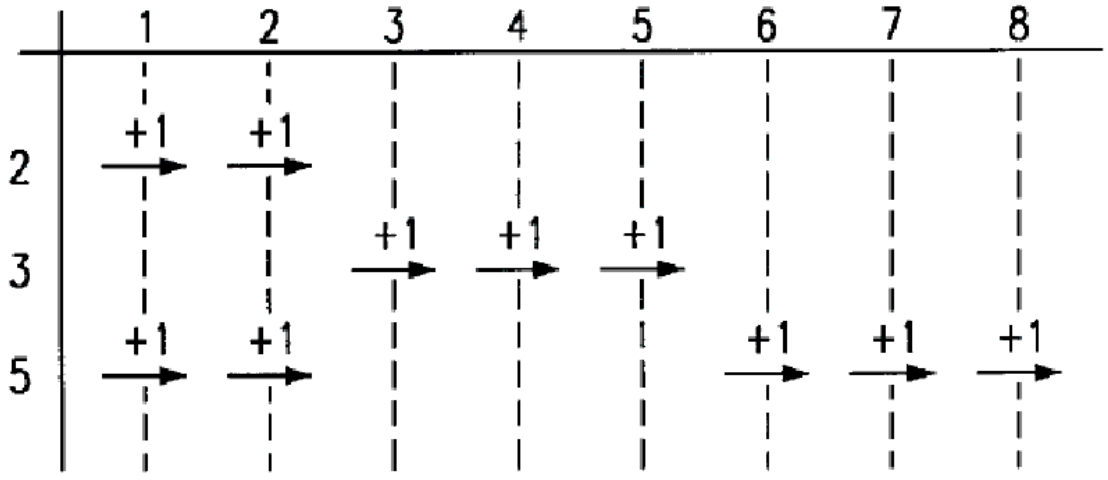
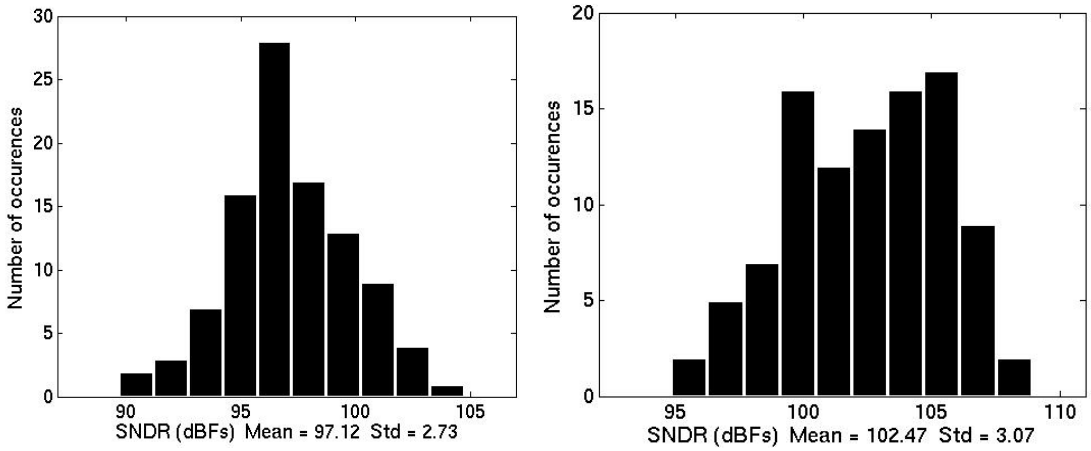


Fig. 5.1. Data weighted averaging



(a) (b)

Fig. 5.2. SNDR distribution a) mismatch 0.1% b) mismatch 0.05%
(Input signal: -6dBFs at Fs/80 with ARDWA)

in [37], *AR-DWA* chooses a random pointer after 'RI' clock cycles. This results in the former having lower SNDR than latter. The approach presented in [46] *Pseudo DWA* is quite similar to *AR- DWA* in that randomization is achieved by flipping the LSB of the input after n_{inv} clock cycles. In our simulations we used AR_DWA with random pointer being chosen after 512 clock cycles. This results in visible tones in the FFT, but they are out of base-band and the SNDR is very close to one achieved with DWA. Fig 5.2 shows a histogram of SNDR with 0.1% and 0.05% random mismatch respectively. To achieve an overall SNDR of 100 dB, SNDR due to mismatch noise should be at least 103dB, assuming equal contribution of kT/C noise and mismatch noise. From the figure we observe that for OSR =8 very few chips will achieve a SNDR of 100dB if matching is less than 0.05%. Thus there is a need to investigate higher order DEM techniques to improve noise performance.

5.3 Second order dynamic element matching

In all the second order DEM techniques proposed in literature, the idea is to shape the mismatch noise by NTF = $(1-z^{-1})^2$ as opposed to $(1-z^{-1})$ by DWA. If we can achieve this NTF, then second order DEM will always be superior to first order DEM regardless of

the over-sampling ratio. The second order DEM will lower the mismatch noise by 15dB/octave of oversampling compared to 9dB/octave of first order DEM. But the work done in [49] claims that for low OSR first order DEM outperforms the second order DEM, which indicates there is a discrepancy. In this section we look at existing second order implementations and try to figure out the cause for this discrepancy.

Vector based mismatch shaping was proposed in [51] for higher order DEM. It actually involves implementation of M digital noise shaping loops, where M is the total number of unit element in the DAC. One of the error feedback loops is illustrated in Figure 5.3. Let d_i be the deviation of i^{th} unit element from the average value of unit elements. It has been shown in [48] that the DAC error is given by

$$e_D(n) = h(n) * \sum_{i=1}^{M} [d_i . e_i(n)] \tag{5.1}$$

Thus $e_D(n)$ is a noise like signal shaped by H(z). The order of noise shaping is determined by that of H(z).This approach has been implemented for obtaining second order noise shaping in audio converters with high OSRs [52]. The major hardware complexity of this algorithm remains in the sorting of w_i array of length M.

A few variations of the above technique exist in the literature. Akira [53] proposes a modification to vector quantizer to alleviate the sorting problem. Akselrod [54] proposes a modified loop filter for vector quantizer, which is claimed to give better SNDR at larger amplitudes compared to error feedback structure. Henderson [55] suggests a Second Order DWA(2DWA) which needs a unit element to be used more than once in a single

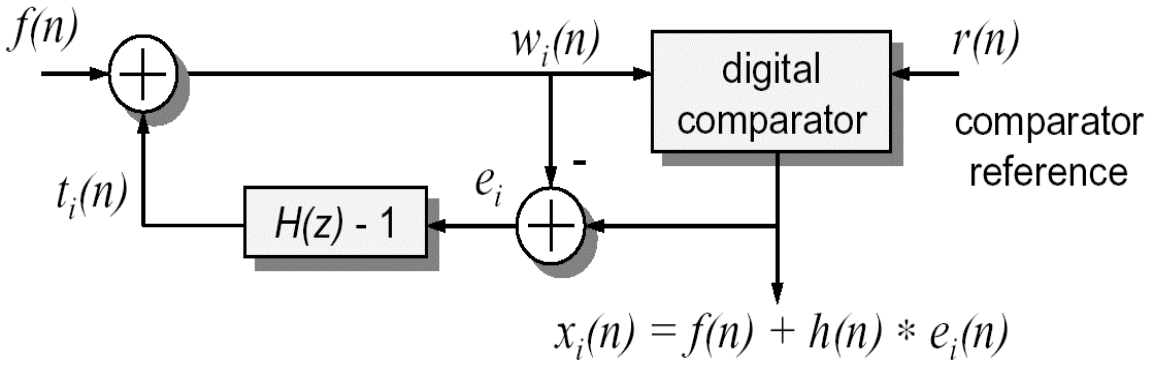


Fig. 5.3. Error feedback loop in vector mismatch shaping

clock cycle which is not feasible. So a modification to 2DWA has been proposed in so-called restricted second order DWA (R2DWA) [56]. A closer examination shows that R2DWA is exactly same as vector quantizer. In our simulations we use vector quantizer to implement second order DEM, with $H(z) = (1-z^{-1})^2$.

Fig 5.4 compares the DAC mismatch noise shaped by DWA, ideal second order and second order vector quantizer [51]. DWA achieves ideal first order noise shaping. As expected, ideal second order is always better than DWA. We observe that for vector quantizer, the mismatch noise rises at 40dB/decade indicating a second order transfer function. But it flattens out at about fs/8. Since the total noise due to mismatch is constant, a flattening of the noise PSD means that we will have more noise at lower frequencies compared to ideal second order. We will get better noise performance if the flattening occurs at higher

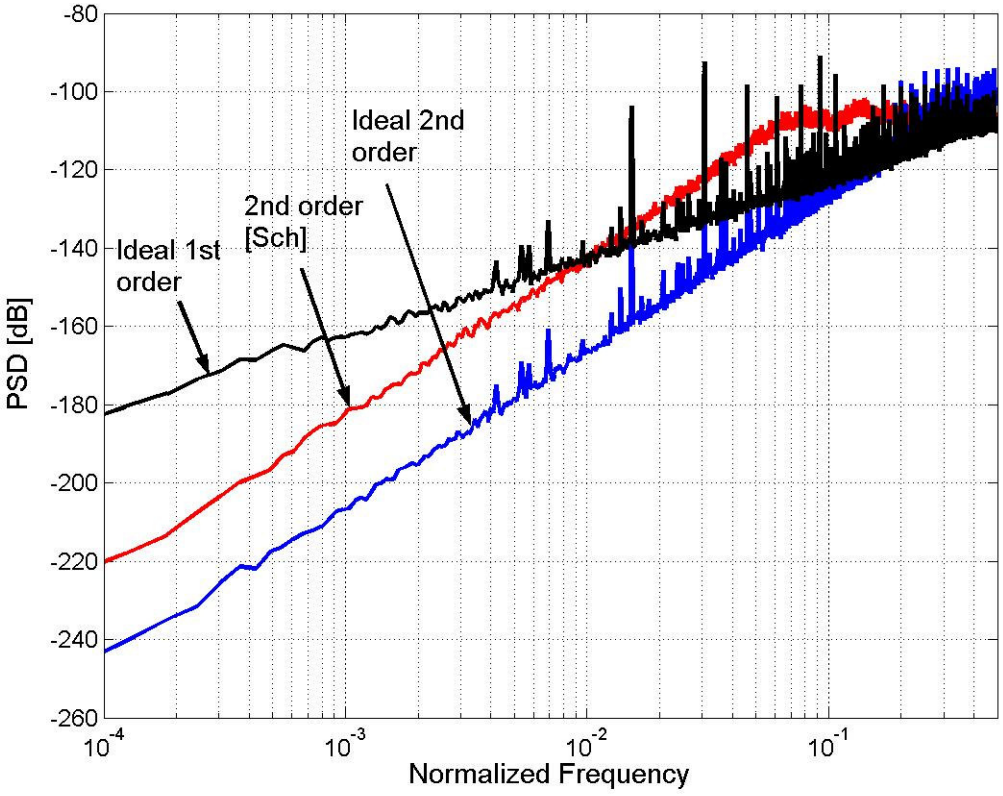


Fig. 5.4. DAC mismatch noise shaped by 1st order and 2nd order NTF ,
(fin = fs/80, Vin= -6dBFs)

frequencies. The PSD of second order vector quantizer is lower than DWA till about fs/32, so vector quantizer will perform better than DWA for OSR >=16.

Fig 5.5 shows the DAC mismatch noise shaped by the vector quantizer for two different signal levels. For –2dBFS signal flattening of PSD occurs at about fs/20 compared to fs/8 for –6dBFs signal. This leads to baseband noise being higher in the former case.

It has been explained in [57] that restrictive second order DWA doesn't allow for uniform element selection (cyclic element selection) thus taking longer time to obtain noise cancellations. This implies that restricted second order DWA can never achieve perfect $(1-z^{-1})^2$ shaping. This helps explain the deviation from the ideal behavior for vector quantizer as well since both implement the same algorithm. It is interesting to note that this flattening of noise spectral density also occurs for tree-structured second order DEM [58].

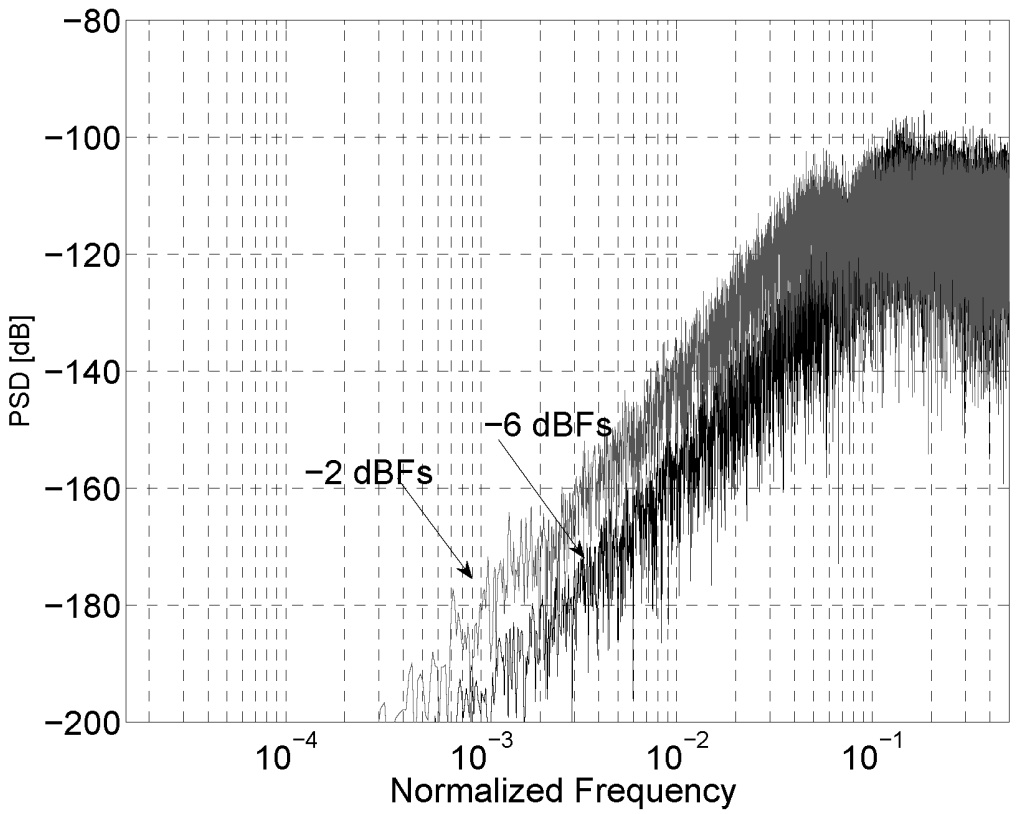


Fig. 5.5. DAC mismatch noise spectrum for two signal amplitudes, fin = fs/80

5.4 Proposed second order DEM

In all the second order DEM reported the noise transfer function is $(1-z^{-1})^2$. It is possible to place the zeros at $z = e^{\pm j\alpha}$, a special case of which is $\alpha = \pi/2$ which corresponds to band-pass DEM. The NTF is now given by

$$H(z) = 1 - 2z^{-1}\cos\alpha + z^{-2} \tag{5.2}$$

The zero placements is illustrated in Fig 5.6 for both NTF. By shifting the NTF zeros from z=1 to $z = e^{\pm j\alpha}$, the magnitude of the NTF in pass-band becomes equal to $K(\omega-\alpha)(\omega-\alpha) = K(\omega^2-\alpha^2)$. The integral of the square of this quantity over the passband is a measure of the in-band noise, and can be minimized by choosing α such that

$$I(\alpha) = \int_0^{\omega_B} (\omega^2 - \alpha^2)^2 \, d\omega \tag{5.3}$$

is minimized. The solution to this optimization problem can be obtained by differentiating $I(\alpha)$ with respect to α, and equating the result to zero. This gives

$$\alpha_{opt} = \omega_B / \sqrt{3} = \frac{\pi}{\sqrt{3} * OSR} \tag{5.4}$$

Since the ratio of $I(0)/I(\alpha_{opt}) = 9/4$, the expected SNR improvement is 3.5dB [48].

These results assume that DAC mismatch noise is white, which will be the case if selection of unit elements doesn't follow a fixed pattern. Substituting the value of α_{opt} in (2) for OSR = 8 gives

$$H(z) = \quad 1 - 1.948815663\, z^{-1} + z^{-2} \tag{5.5}$$

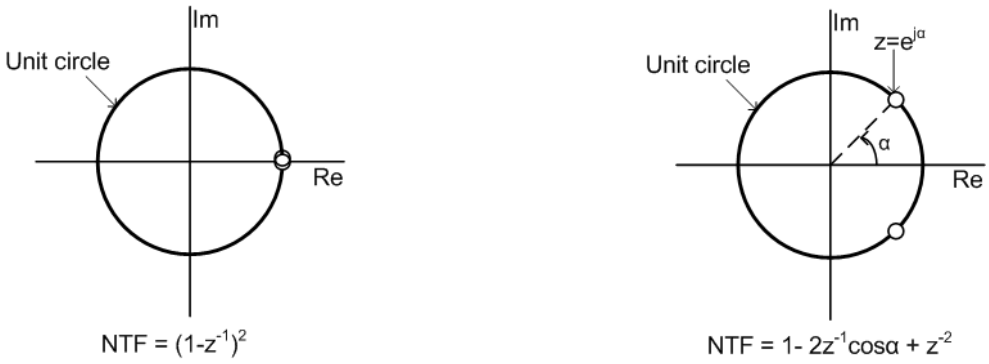
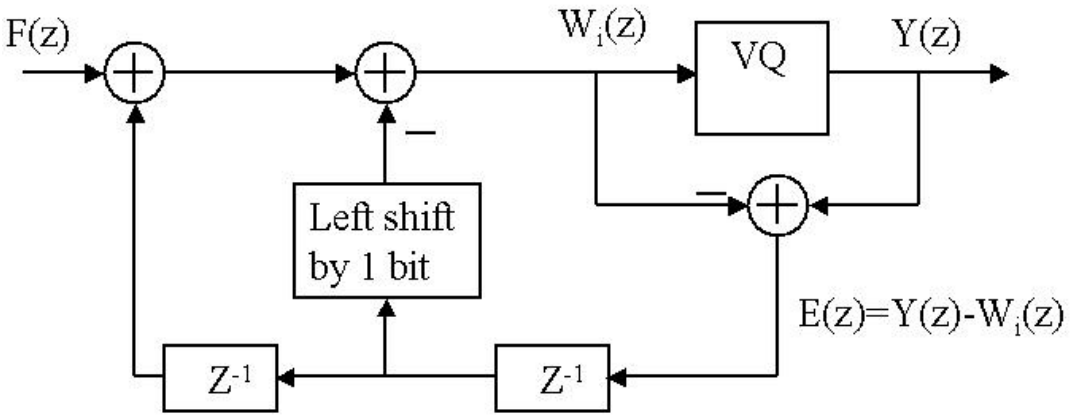
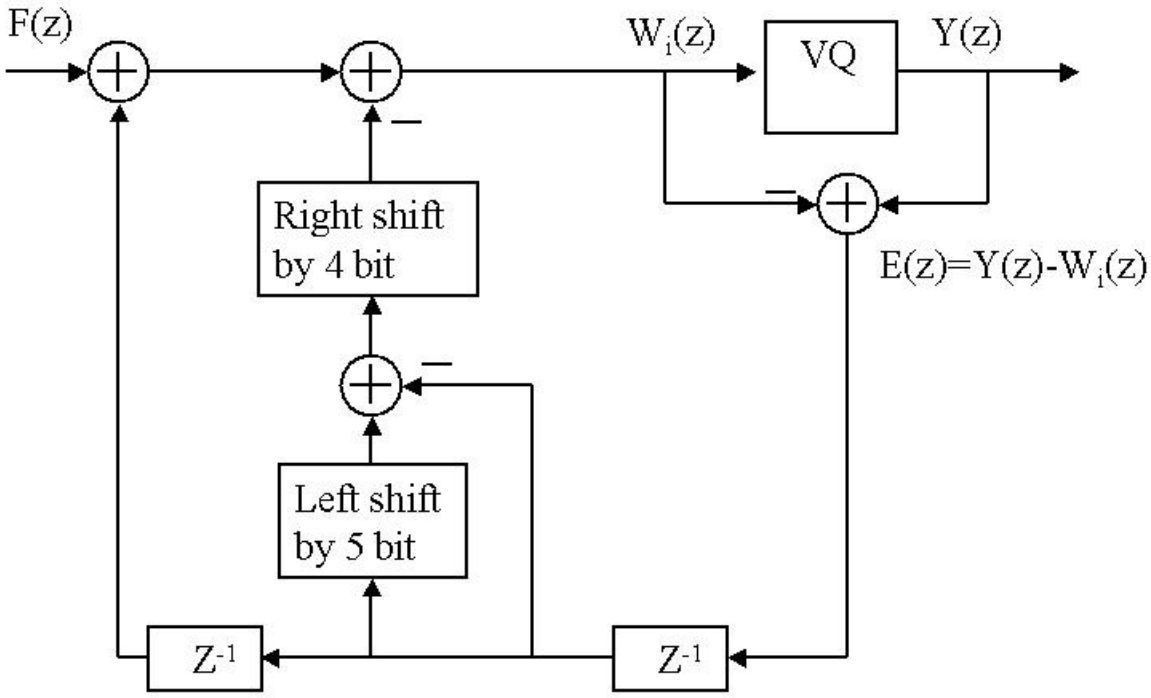


Fig. 5.6. Placement of zeros for different NTF



(a)



(b)

Fig.5.7. Second order error feedback loop

a) Zeroes at DC b) With notch at approximately Fs/25

We implement the second order DEM similar to vector quantizer with a modified loop filter containing a notch. Vector quantizer with both zeros at dc shown in Fig 5.7a requires only addition and shifting, whereas implementing (5.5) will need a multiplication.

To avoid the multiplication in (5.5) we implement the vector quantizer with the notch as shown in Fig 5.7(b). Now the multiplication is replaced by two additional shifts and a subtraction. The NTF is now given by

$$H(z) = \quad 1 - 1.9375\, z^{-1} + \, z^{-2} \tag{5.6}$$

This places the notch at $\omega_B/1.56685$, which is reasonably close to optimal. For an OSR of 8 this corresponds to fs/25. The DAC noise spectrum with this transfer function is as shown in Fig. 5.8. There are no spurious tones visible in the spectrum.

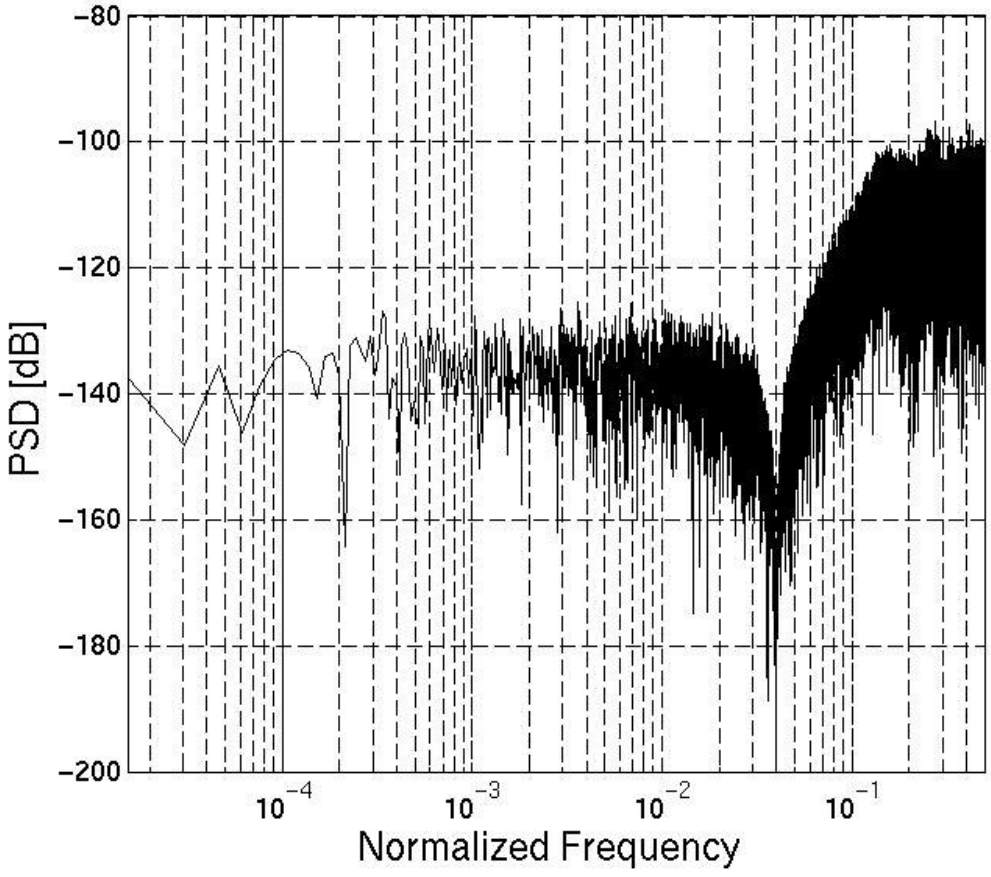


Fig. 5.8. DAC noise spectrum with a notch at Fs/25

Fig 5.9 compares the SNDR obtained by placing both the zeros at dc, to the one obtained by placing a notch at fs/25, for two different signal frequencies. We see an improvement of about 5-6dB for most of the signal range.

Fig 5.10 shows the SNDR obtained with 0.1% mismatch and 0.05% mismatch with the notch in DEM. We observe that compared to ARDWA in Fig 5.1, we have an improvement of about 6dB on average. The improvement in SNDR is at the cost of extra complexity involved in implementation of second order DEM, compared to DWA, which can be implemented easily.

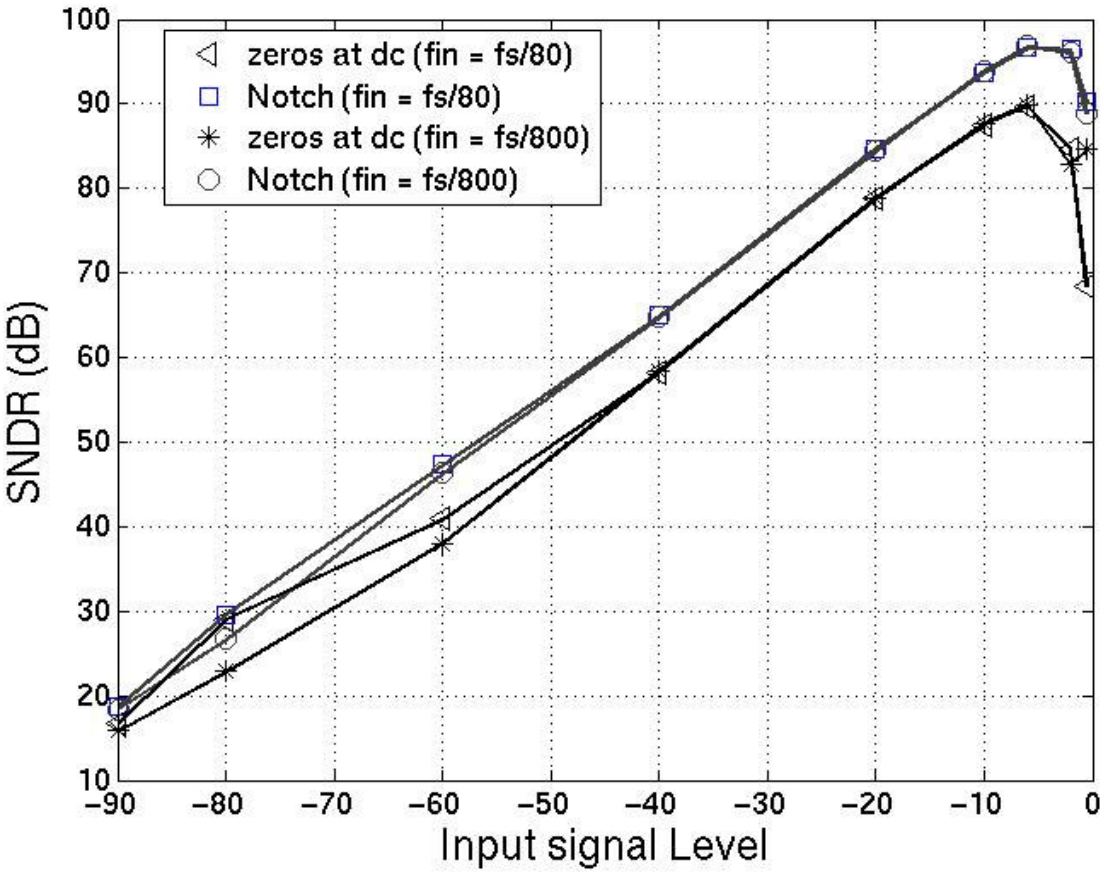
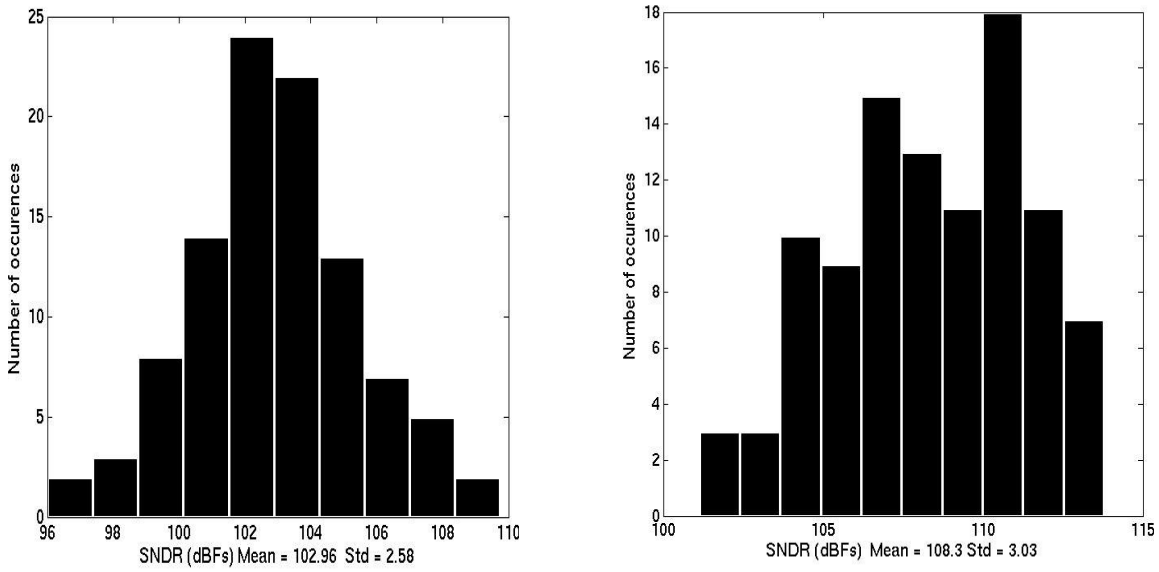


Fig. 5.9. SNDR vs input signal amplitude with zeroes at DC vs notch at Fs/25, for two different frequencies



(a) (b)

Fig. 5.10. SNDR distribution a) mismatch 0.1% b) mismatch 0.05%
(input signal : -6dBFs at Fs/80 2nd order DEM with notch)

5.5 Conclusion

In this chapter we analyzed second order DEMs as applicable to low OSR sigma delta ADC's. It is explained why first order DEM is better than second order at low OSR, with the existing solutions. It is shown that with optimal placement of the zeros of the second order DAC NTF, the second order DEM can give better SNDR at low OSR's compared to first order at the expense of additional digital hardware complexity.

CHAPTER VI
A CALIBRATION TECHNIQUE FOR HIGH-RESOLUTION BROADBAND ΔΣ ADC

6.1 Motivation

Broadband sigma-delta ADC's used for scientific instrumentation applications. (Signal Bandwidth > 1Mhz) typically use multi-bit feedback DAC. There are numerous advantages in having multi-bit DAC [48] . The quantization error is reduced by 6dB for every bit added to the resolution of the quantizer. The feedback loop becomes more linear, since variations of the effective gain of the quantizer with its input signal are reduced. Since the DAC input to loop filter changes less from sample to sample, the required slew rate of the input opamp of the loop filter is reduced. For ADCs with continuous time loop filters, the smaller steps in DAC waveform make the operation less sensitive to clock jitter. But there is one significant disadvantage of using multi-bit DAC. The linearity of the DAC determines the over-all linearity of the ADC and there may be tones in the output spectrum.

There have been two popular approaches to alleviate the problem. Dynamic element techniques have been used to convert the energy contained in the tones to white noise and shape the mismatch noise out of base-band [37,47]. This technique works very well for ADC's with large over-sampling ratios (OSR) but for low OSR converters most of the mismatch noise remains in base-band and the technique is not very effective [48,49]. The problem becomes acute as we target higher SNR while maintaining similar OSR. As observed in previous chapter if we target 100dB SNR with an OSR of 8, the yield may be limited to 50% if 0.1% mismatch is assumed.

Another technique used is to digitally correct for the capacitor mismatch error [59]. The idea is to characterize the DAC output voltages for all possible input codes and then used it for calibration. This technique works well for low OSR converters but has a couple of drawbacks. First it needs a very linear ADC to calibrate the internal DAC. In [59] a single bit modulator is built on-chip for calibration purpose. This would increase on chip area and power. The second disadvantage is that the DAC needs to be calibrated

to the resolution of over-all ADC. This needs a long calibration time, which may result in long test times if it is a one-time calibration.

Thus there is a need to find calibration techniques, which relax the linearity requirements of the ADC characterizing the DAC. Also the technique needs to be practical in terms of calibration test time. This chapter discusses the existing approaches, which include the DEM and blind calibration and the associated issues. Later a new practical idea is presented to alleviate the problem.

6.2 Existing approaches

6.2.1 Dynamic element matching [37,47]

The basic operating principle of delta-sigma conversion namely noise shaping has been used to reduce the effects of the non-linearity in a multi-bit DAC. Here 'noise' is the mismatch error introduced by the uneven spacings of the DAC levels, which is shaped out of the baseband. The scheme is illustrated in Fig 6.1. Dynamic element matching (DEM) block determines which unit elements are selected in the DAC for a given input code N.

One of the most common and easy to implement dynamic element matching technique is element rotation or Data Weighted Averaging [47]. The technique illustrated in Fig 6.2 aims to make long-term average of use of each unit element in the DAC same, by rotating the pattern of unit elements. In the Figure 2 n^{th} code uses elements 1-3, n+1 code uses element 4-6, n+2 code uses element 7-8 and wraps around the circle-using element 1.

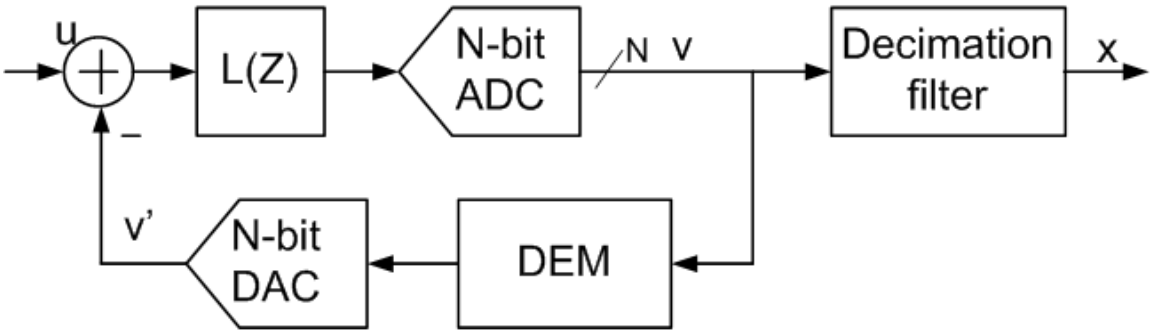


Fig. 6.1. Dynamic element matching

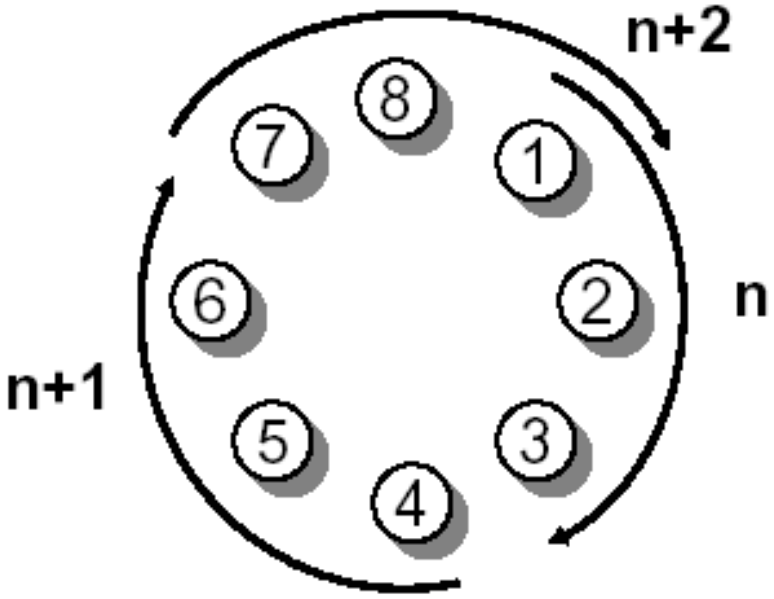


Fig. 6.2. Data weighted averaging

It can be shown that DWA shapes the mismatch noise by first order high pass filter function. DWA causes the output spectrum to have tones. This problem can be alleviated introducing some randomization in element selection [37] at cost of increased noise in baseband, thereby exhibiting a trade-off between SNR and SFDR.

Drawbacks of this approach:

Dynamic element matching techniques rely on over-sampling and noise shaping, and hence become ineffective for very low values of OSR (4-8), which are needed in broadband data converters [49].

6.2.2 Basic digital calibration

Fig 6.3 illustrates the basic correction scheme of a digitally corrected ΔΣ ADC. The digital correction stage following the modulator loop can simply be some memory element (register/ fuses), storing the accurate digital equivalents of the actual output values of N-bit DAC for all possible input codes. Thus for any loop output signal sample v (n), the analog output v' (n) of the DAC and the digital output w (n) of the correction stage are same. Since for sufficiently high inband loop gain the inband spectrum of v' (n) is very close to that of analog input u(n), and since v'(n) = w(n), it follows that inband spectrum of w(n) is very close to input spectrum.

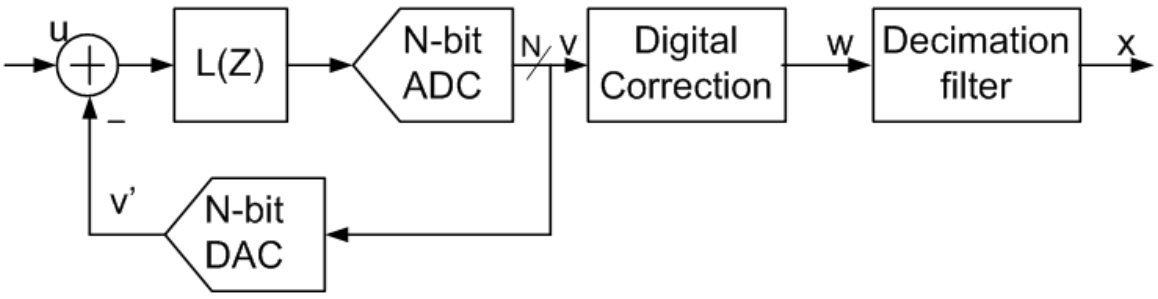


Fig. 6.3. A digitally corrected ΔΣ ADC

Drawbacks of this approach:

For a 20 bit over-all ADC accuracy the DAC has to be calibrated to 20bit accuracy. Technique proposed in [59] needs an on-chip one bit (hence linear ADC) to convert the DAC outputs to analog values. To calibrate to 20bit accuracy each code needs to be held for duration of at least 2^{20} clock periods, i.e a total of 2^{20+N} clock periods, which means long calibration times or test times (if calibration is done one time during test)

Output of the digital correction logic needs to have accuracy equal to over-all ADC, which will lead to increased word-length of the input to decimation filter. Techniques mentioned in [59] to reduce the word-length of output rely on having a large OSR and hence will not be applicable if OSR is low and the modulator is the first modulator in a MASH.

6.3 Proposed approach

As explained before the problem with DEM at low OSR is that there is enough baseband noise remaining in the base-band to degrade SNR. The amount of SNR degradation depends on the capacitor matching i.e. the total mismatch noise power. The idea in the approach presented in Fig 6.4 is to reduce the total mismatch noise power and then shape it out of the baseband. It may be possible to reduce the mismatch noise power by trimming the DAC unit elements as in [60], but this approach becomes impractical for small unit capacitors. In the proposed approach reduction of mismatch noise is done in digital domain and then DWA provides a first order shaping of this noise.

. The Digital correction again needs memory element storing the accurate digital equivalents of the actual output values of N-bit DAC for all possible input codes. The difference is that now the accuracy of codes stored can be significantly lower (12-14 bits). The pointer from DWA block is also utilized by Digital correction block to determine which unit elements are being used in a given code.

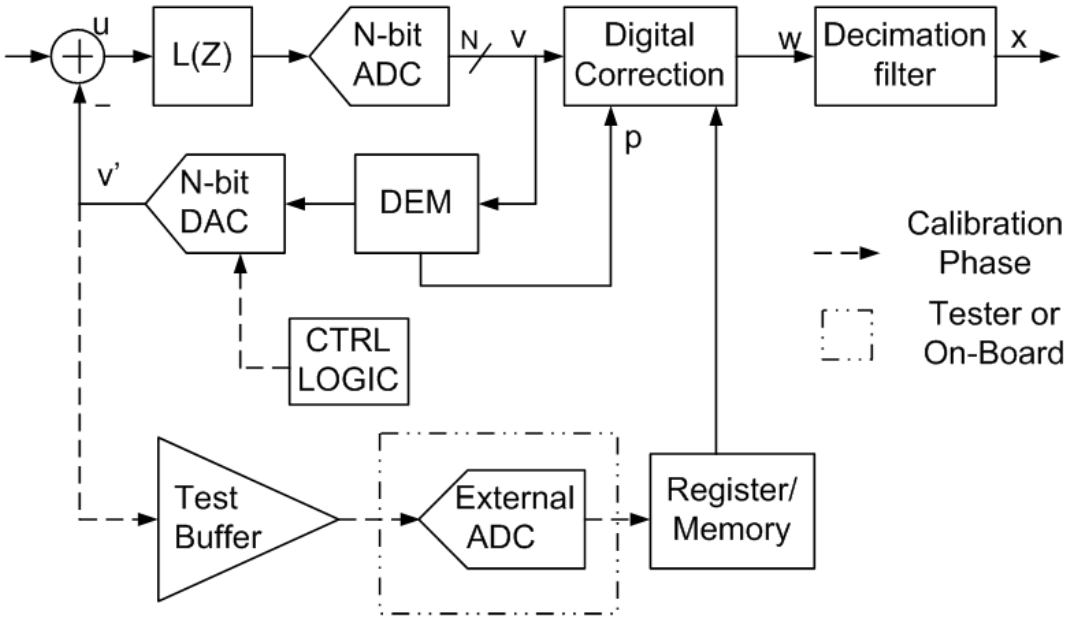


Fig. 6.4. ADC with DEM and digital correction

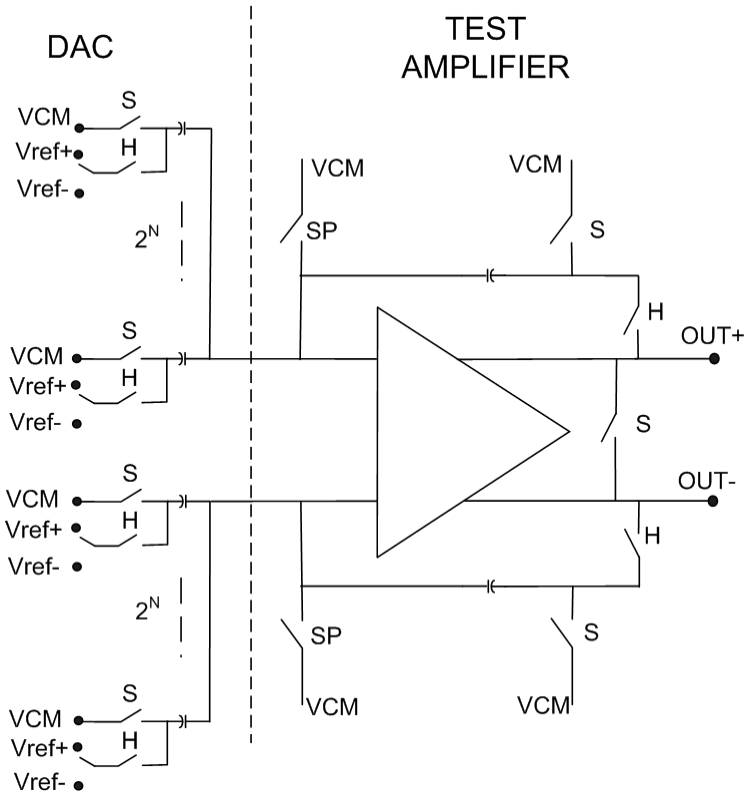


Fig. 6.5. Calibration setup

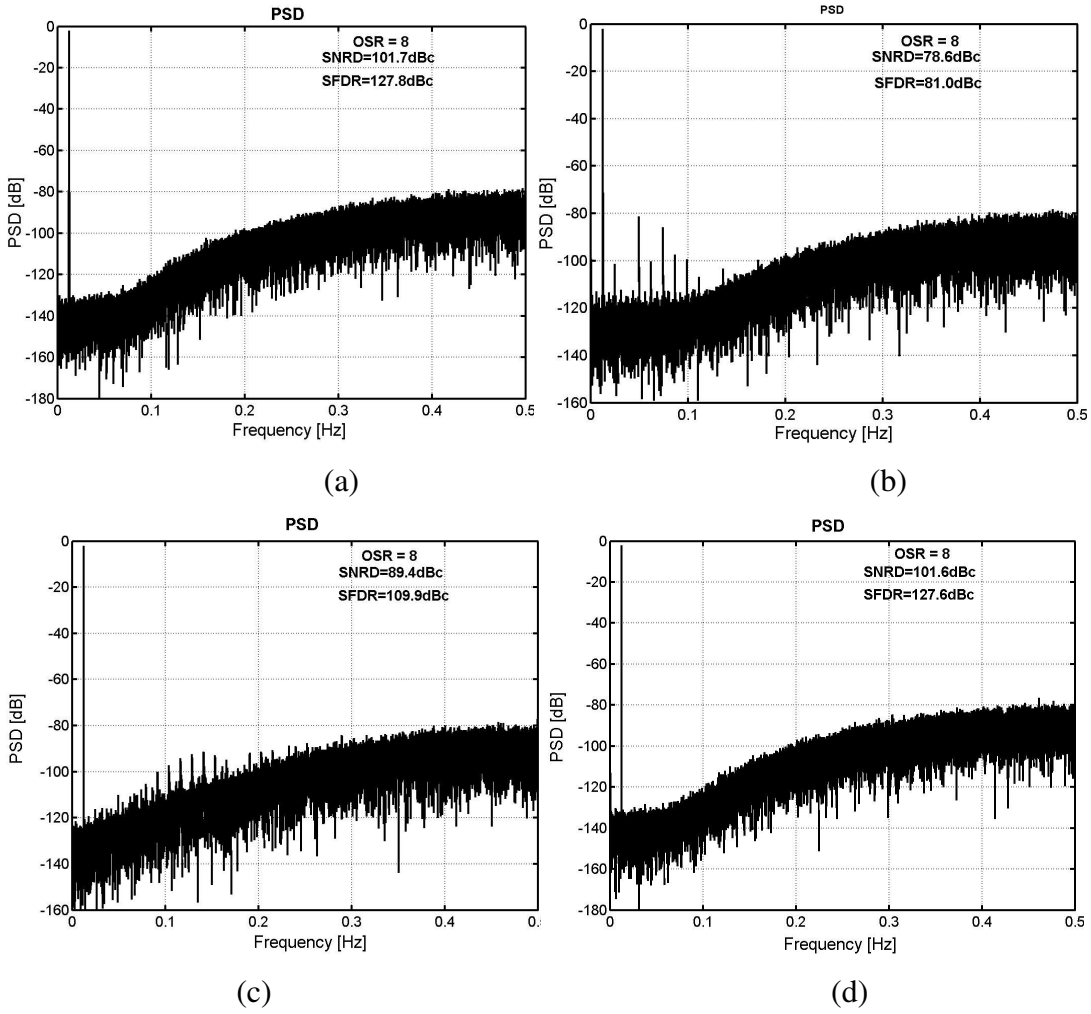


Fig. 6.6. Modulator output PSD (fin = fs/80, amplitude = -0.5dBFs)

a) Ideal DAC SNDR = 103.1dBc, SFDR = 129.6dBc

b) DAC with 0.1% mismatch SNDR = 73.6dBc SFDR = 80.3dBc

c) DWA: SNDR = 86.2dBc SFDR = 101.2dBc

d) DWA+ 12 bit correction: SNDR = 102.4dBc, SFDR = 125.9dBc

Calibration phase: Instead of having a single bit ADC on-chip for calibration the idea is to use an external ADC for calibration (one time calibration during test). Since we need to calibrate till only 12-14-bit accuracy, LFAC DIG available in Teradyne (catalyst) tester itself can be used for calibration. Only problem that remains is that DAC is a switched capacitor DAC and its output cannot be tapped directly. So we insert a buffer at the output of DAC (shown in Fig 6.5) and then convert its output to digital by external

ADC. A test-chip is being fabricated with the set-up in Fig 6.5 to verify the calibration phase and to ensure that we can indeed calibrate to 14-bit accuracy.

6.4 Simulation results

The scheme was applied to the first modulator in of an ADC with three stages MASH architecture. The DAC here is a four-bit DAC with 16 unit elements. It was assumed that capacitor matching is 0.1%. The results with ideal capacitor array give a SNDR of 103dBc with an OSR of 8 (Fig 6a). With 0.1% mismatch SNDR drops to 73.6dBc (Fig 6b). Using DWA improves SNDR to 86.2dBc still way below the ideal value (Fig 6c). We assume that the capacitor array is calibrated to 12-bit accuracy in our proposed approach; the results obtained are close to the ideal value.

6.5 Advantages of proposed solution

The proposed scheme reduces the requirement on the accuracy to which we calibrate the ADC. This in turn means smaller calibration time. If we calibrate to 14-bit accuracy instead of 18-bit we cut down test time by 16 times. We need not have a very accurate ADC on-chip we can probably use LFAC DIG available on tester. This will lead to reduction in chip area. Word-length of the internal bus is reduced; this leads to reduced digital hardware.

CHAPTER VII
CAPACITOR MISMATCH CHARACTERIZATION AND LAYOUT TECHNIQUES

7.1 Motivation

The D/A converter is a vital part of many electronics systems. In almost all A/D converters the linearity of D/A converter limits the resolution of the converter. The linearity of D/A converter is limited by the mismatch between unit cells (unit capacitors, for switched capacitor circuits). Mismatch between the capacitors of the array could be due to two reasons – random variation and systematic variation. Here systematic variation refers to spatial dependence of capacitor value. Patterning and etching variations during the fabrication of capacitor plates and dielectric thickness variations are examples of mismatch caused by process anomalies. Some of these results in random mismatch while others result in spatial dependence of the capacitor value.

Laying out each required capacitor as a sum of unit capacitors usually minimizes random variation. The entire array is surrounded by ring of dummy capacitors to make the environment of each interior capacitor the same. However, inspite of great care taken in layout it is impossible to completely remove the effect of random errors.

The effect of spatial variation can be reduced by grouping unit capacitors in such a way that the average capacitor value of the entire array. Spatial variations can be modeled a layout chosen to minimize such errors. Again, the extent of the error cancellation depends on the accuracy of modeling. Also there is a trade-off between canceling gradient effects and random mismatch. For example to cancel quadratic gradient, it is essential to split each unit cell into at least four parts, which leads to greater random variations. Also dividing a unit into four sub-units and placing them in four distant locations bring up the problem of routing the interconnection between them. Other disadvantage is that even though a unit is sub-divided into four separate sub-units, the total area of each sub-unit is more than 1/4 of the original unit. This is due to required minimum spacing between subunits dictated by the fabrication technologies. The increased number of interconnects cause the area to increase. Whether common centroid

layout, which cancels gradient, will perform better depends on what is limiting the performance: random variations or spatial variations.

The objective of this test chip is as follows

- To verify if we can get 12bit cap matching with 16 unit caps (1.5625pF) each.
- To study what is limiting the matching: whether gradient is dominant factor or random mismatch is dominant. To test this we are having a version with each unit cap split into smaller units to reduce effect of gradient.
- To study if the differential cap matching is inferior compared to single-ended cap matching. To this end we have a test option to measure the cap matching with single-ended cap array.
- To develop a method for measuring the cap-mismatch which can be extended to use for calibration if needed.
- To measure how the random mismatch varies with varying size of unit capacitors.

7.2 Mismatch characterization

Capacitor mismatch cannot be typically measured on discrete devices. This is because of the small capacitances involved and very low level of mismatch typically seen on capacitors. Commercial CV meters can measure approximately down to 1pF with 10% accuracy. High performance capacitors of test are in range of 1-5pF but require measurement accuracy at low ppm level. Below we discuss standard methods used for capacitor characterizations and then present the method we selected for characterization.

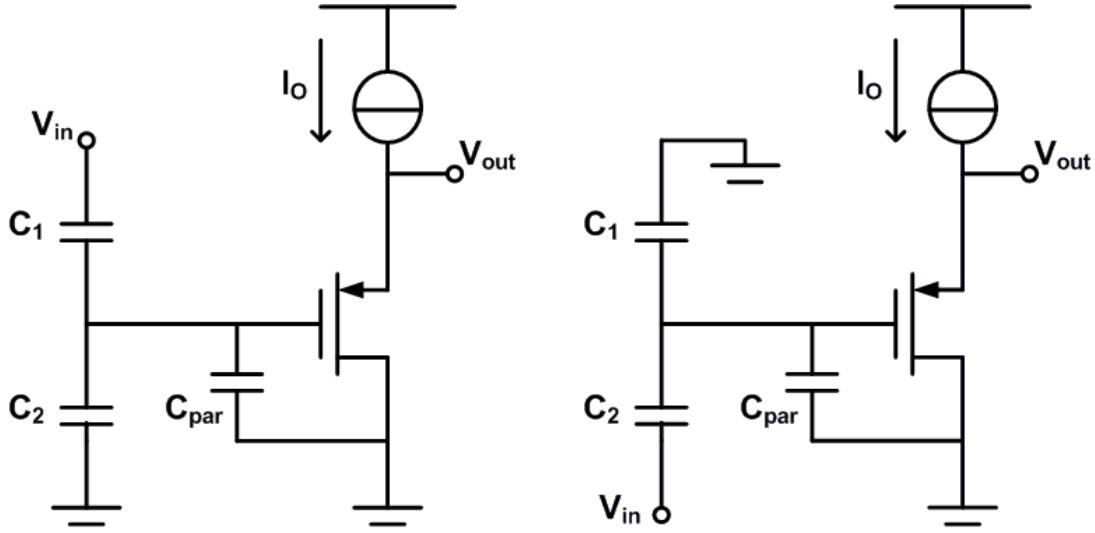
7.2.1 Floating gate measurement technique

A typical test structure for measuring capacitor mismatch is shown in Fig 7.1 [61]. Two capacitors of equal size are connected in series. The common node is connected to the gate of a PMOS transistor. The voltage on this (floating) middle node is monitored at V_{out} using a source follower that is biased with a fixed current source e.g current source from a parametric tester. By applying two different input voltages ($N_{in,lo}$ and $V_{in,hi}$) with C_1 connected to V_{in} (C_2 grounded) and measuring the corresponding output voltages ($V_{out,lo}$ and $V_{out,hi}$) at the source of MOSFET, the slope S_1 can be determined, as illustrated in Fig

7.2 . The measurement is repeated with V_{in} connected to C_2 and C_1 grounded. The result is slope S_2. By using S_1 and S_2, most parasitic effects are averaged out. Capacitor mismatch is calculated as follows:

$$S_1 = \frac{C_1}{C_1 + C_2 + C_{par}};\ S_2 = \frac{C_2}{C_1 + C_2 + C_{par}};$$

$$\frac{\Delta C}{C} = 2.\frac{C_1 - C_2}{C_1 + C_2} = 2\frac{S_1 - S_2}{S_1 + S_2} \tag{7.1}$$



(a) Setup for measuring S_1 (b) Setup for measuring S_1

Fig. 7.1. Floating gate capacitance measurement method

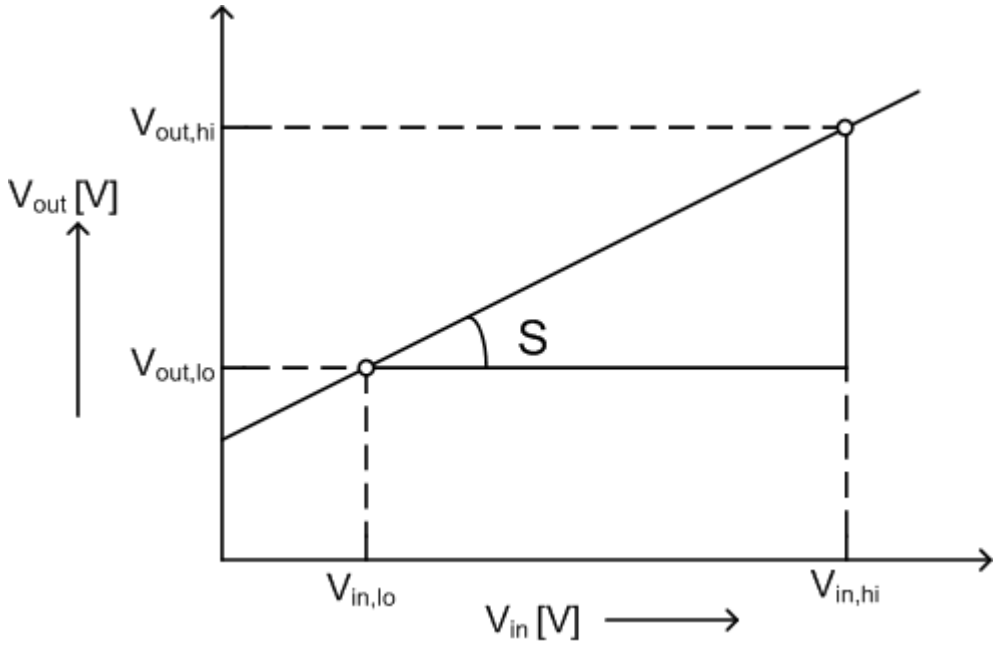


Fig. 7.2. Determination of slope S for floating gate capacitance measurement method

7.2.2 Charge based capacitance measurement

Another method for characterization of capacitor is CBCM (charge-based capacitance measurements) introduced in [62]. CBCM has very good resolution that allows for measurement of capacitances in femto-farad range. The only equipment needed for the CBCM method is an accurate ammeter for the measurement of a DC supply current. Figure 7.3 shows the principle of classical version of CBCM.

The test structure consists of a pair of NMOS and PMOS transistors connected in a "pseudo" inverter configuration, each has its own gate input. The pseudo inverter structure on the left is identical to the one on right in every manner, with both loaded by capacitors C1 & C2 whose mismatch is to be characterized. The left and right structures are driven by two non-overlapping clock signals. When the PMOS transistor turns in will draw charge from VDD to charge up the target capacitances. This amount of charge will then be subsequently discharged through the NMOS transistor into the ground. An ammeter measures this charging current. The difference between the two DC average currents is used to extract the mismatch between the two test capacitors.

$$I - I' = C_1.V_{dd}.f - C_2.V_{dd}.f = \Delta C.V_{dd}.f \qquad (7.2)$$

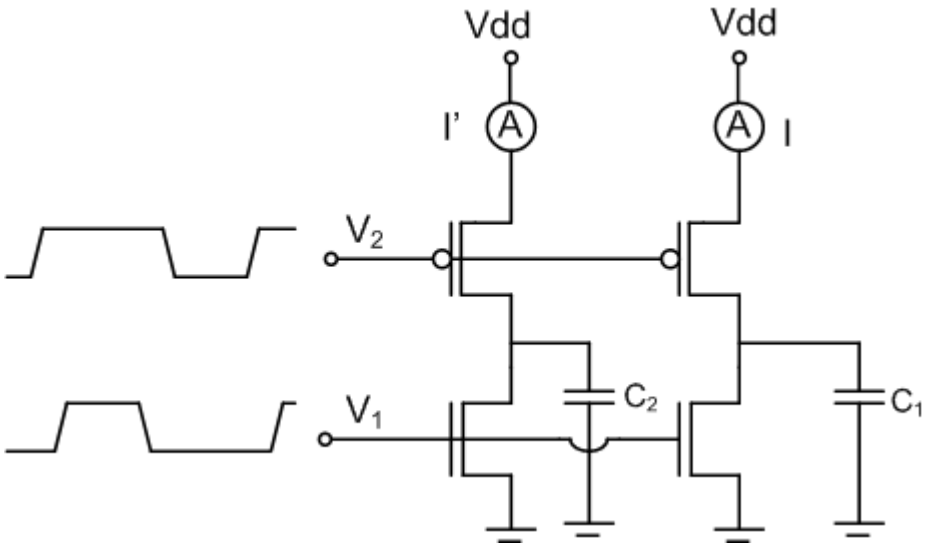


Fig. 7.3 Test structure for CBCM method

7.2.3 Proposed method

Both the methods presented above are suitable for characterizing the mismatch between two unit capacitors. For our case we have a DAC with 16 unit capacitors and we wish to characterize the relative mismatch between them. The idea is to switch one capacitor at a time to the reference and observe the output. The output of the DAC cannot be directly loaded so we buffer it with an amplifier as shown in Fig 7.4. The output of the amplifier is not a dc value, so a dc meter cannot be used to measure the output of the DAC. We need to use a properly synchronized ADC to capture the output of DAC. A possible test setup is illustrated in Fig 7.5. The same setup can be used to obtain calibration coefficients in an ADC. Then the buffer used can be on of the amplifiers used for integrators.

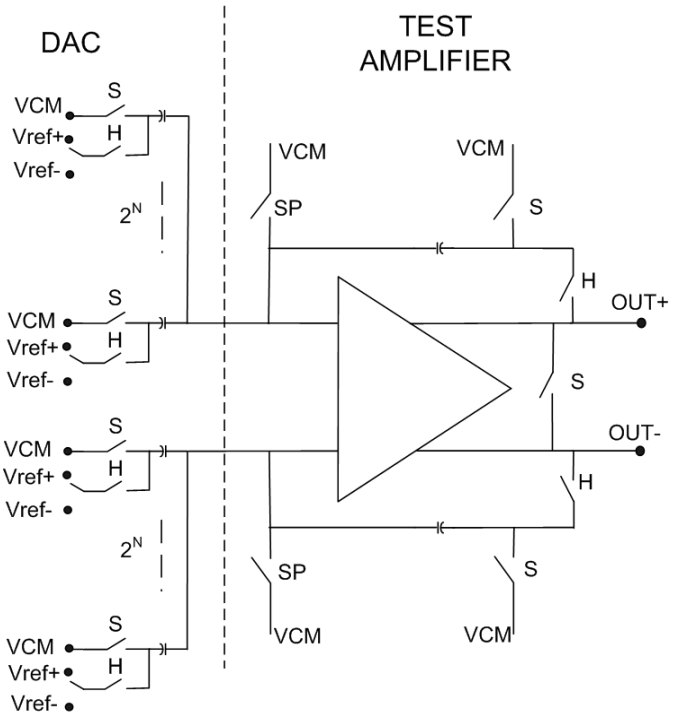


Fig. 7.4. Switched capacitor DAC followed by a buffer

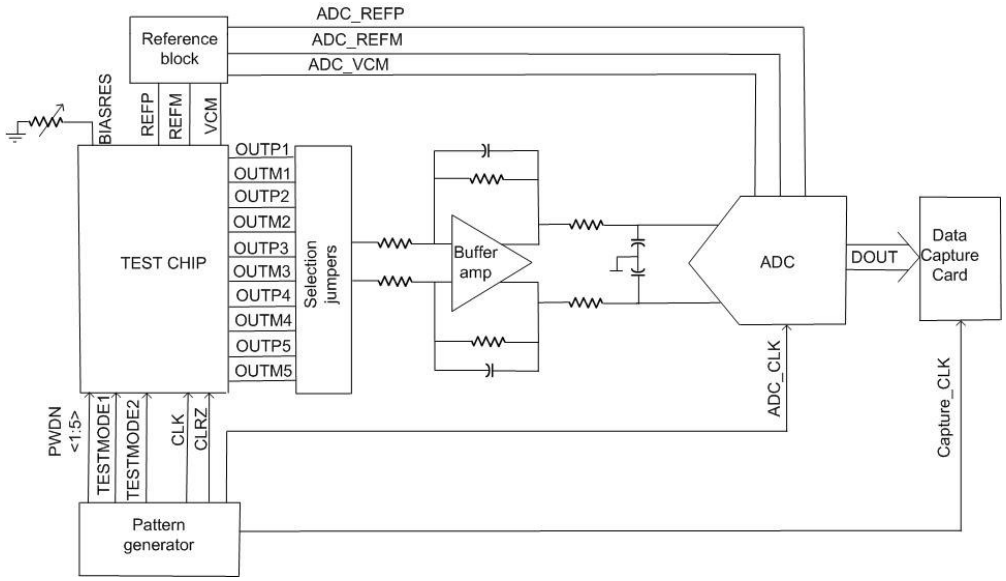


Fig. 7.5 Block diagram of test setup for characterization

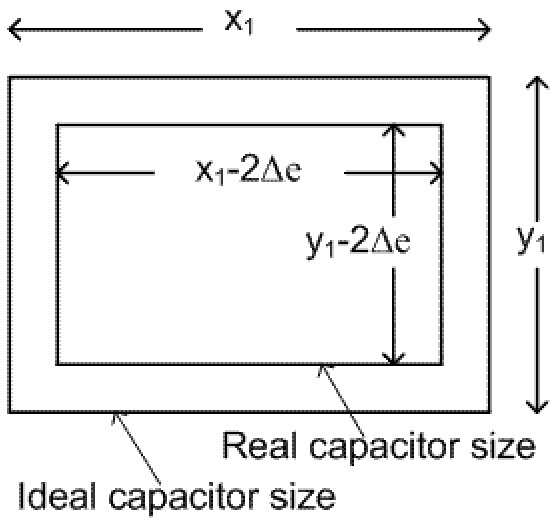


Fig. 7.6. Capacitor errors due to over-etching

7.3 Layout techniques

7.3.1 Capacitor matching: The major sources of error in realizing capacitors are due to overetching and the oxide thickness gradient across the surface of the chip [63]. The former effect becomes less dominant for large capacitor sizes. Let us assume that a capacitor has an absolute overetching given by Δe and its ideal dimensions are given by x_1 and y_1, then its real dimensions are given by $x_{1a} = x_1 - 2\Delta e$ and $y_{1a} = y_1 - 2\Delta e$, then the real capacitor size is given by

$$C_a = C_{ox} x_{1a} y_{1a} = C_{ox}(x_1 - 2\Delta e)(y_1 - 2\Delta e) \tag{7.4}$$

Thus the error in real capacitor is given by

$$\Delta C_t = C_{ox} x_{1a} y_{1a} - C_{ox} x_1 y_1 = C_{ox}[-2\Delta e(x_1 + y_1) + 4\Delta e^2] \tag{7.5}$$

When this error is small then the second order term can be ignored and equation (7.5) can be approximated by

$$\Delta C_t = -2\Delta e(x_1 + y_1) C_{ox} \tag{7.6}$$

the relative error in capacitor is therefore given by

$$\varepsilon_r = \frac{\Delta C_t}{C_{ideal}} = \frac{-2\Delta e(x_1 + y_1) C_{ox}}{x_1 y_1} = -C_{ox} \Delta e \frac{Perimeter}{Area} \tag{7.7}$$

Let us now compare the relative errors for unit-cells with different areas i.e different capacitances values. Let the dimensions be $x_2 = kx_1$ and $y_2 = ky_1$ then

$$\varepsilon_{r2} = \frac{\Delta C_t}{C_{ideal}} = \frac{-2\Delta e(kx_1 + ky_1)C_{ox}}{k^2 x_1 y_1} = \frac{-2\Delta e(x_1 + y_1)C_{ox}}{kx_1 y_1} = \frac{\varepsilon_r}{k} \tag{7.8}$$

Thus we obtain

$$\frac{\varepsilon_{r2}}{\varepsilon_r} = \sqrt{\frac{Area_1}{Area_2}} \quad \text{i.e} \quad \varepsilon_r \, \alpha \, \frac{1}{\sqrt{\text{Area}}} \tag{7.9}$$

This means that matching is improved for larger unit cells. Thus splitting unit cells to cancel gradients will have adverse effect on random mismatch due to overetching.

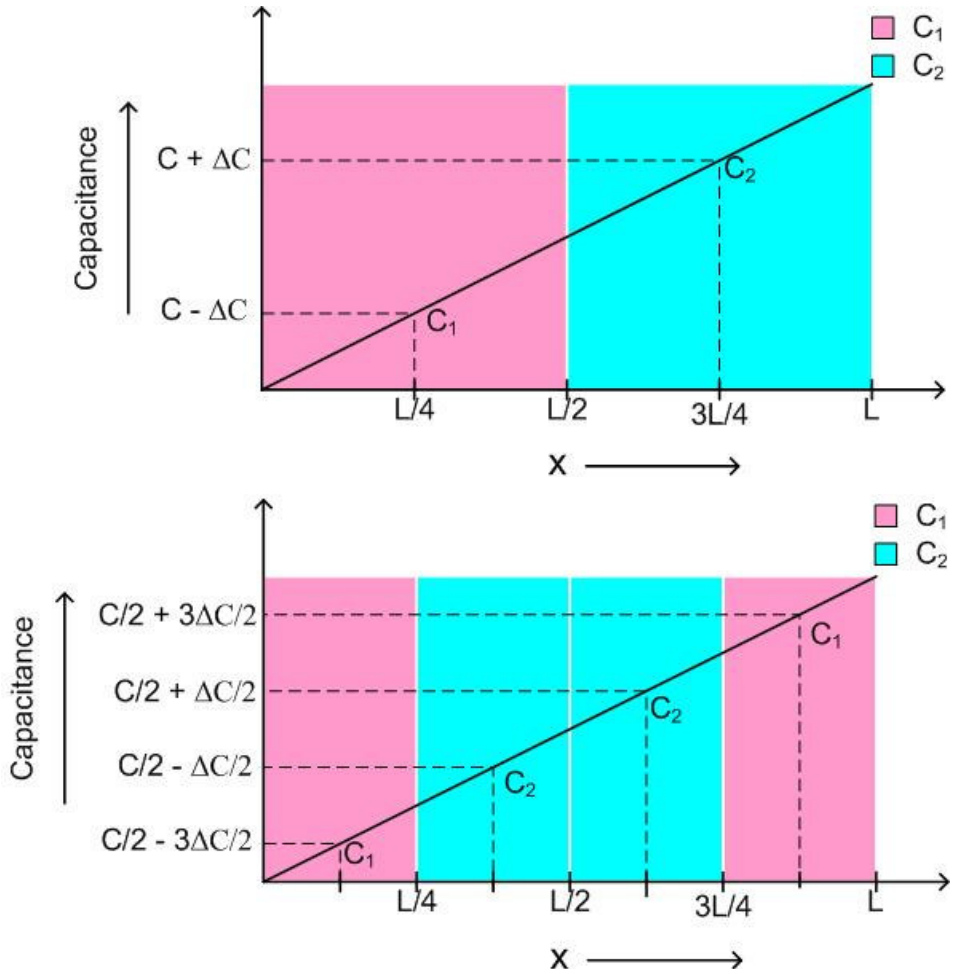


Fig. 7.7 Linear gradient: a) Illustration b) Canceling the gradient

7.3.2 Canceling linear gradients

Let us assume that there is a linear gradient in x direction as shown in Fig 7.7a. We want to match two capacitors C_1 and C_2, but because of gradient there is a mismatch of $2\Delta C$ in between them. To cancel linear gradient we must do a common centroid layout, this requires splitting the unit cell in two halves. The placement of the half-cells is shown in Fig 7.7b. From the figure we observe that

$$C_1 = C_1(L/8) + C_1(7L/8) = [C/2 - 3\Delta C/2] + [C/2 + 3\Delta C/2] = C$$
$$C_2 = C_2(3L/8) + C_2(5L/8) = [C/2 - \Delta C/2] + [C/2 + \Delta C/2] = C \qquad (7.10)$$

and gradient effect is cancelled. The drawback is that splitting the unit cells will cause the random mismatch to increase. The common centroid layout will cancel linear gradients for capacitor arrays with more than two capacitors. As an example the following arrangement will cancel linear gradient for a capacitor array with four matched capacitors

$C_1\ C_2\ C_3\ C_4\ C_4\ C_3\ C_2\ C_1$

7.3.3 Canceling quadratic gradients

We assume that there is a quadratic gradient in x-direction as illustrated in Fig 7.8a. We wish to match a capacitor array with four matched capacitor. Let us approximate the quadratic gradient with a linear approximations as shown in Fig 7.8a, then with this approximation C1 = C4 = C- $\Delta C/2$ C2 = C3 = C+ $\Delta C/2$, thus there is a mismatch of ΔC between unit cells.

To cancel the quadratic gradient we split the unit cell into four quarters. The capacitors are laid out such that the layout has an axis of symmetry at the centre. Each half on either side of axis of symmetry also has an axis of symmetry at its centre. This is illustrated in Fig 7.8b. It is easy to see that this layout will also cancel linear gradients in x direction.

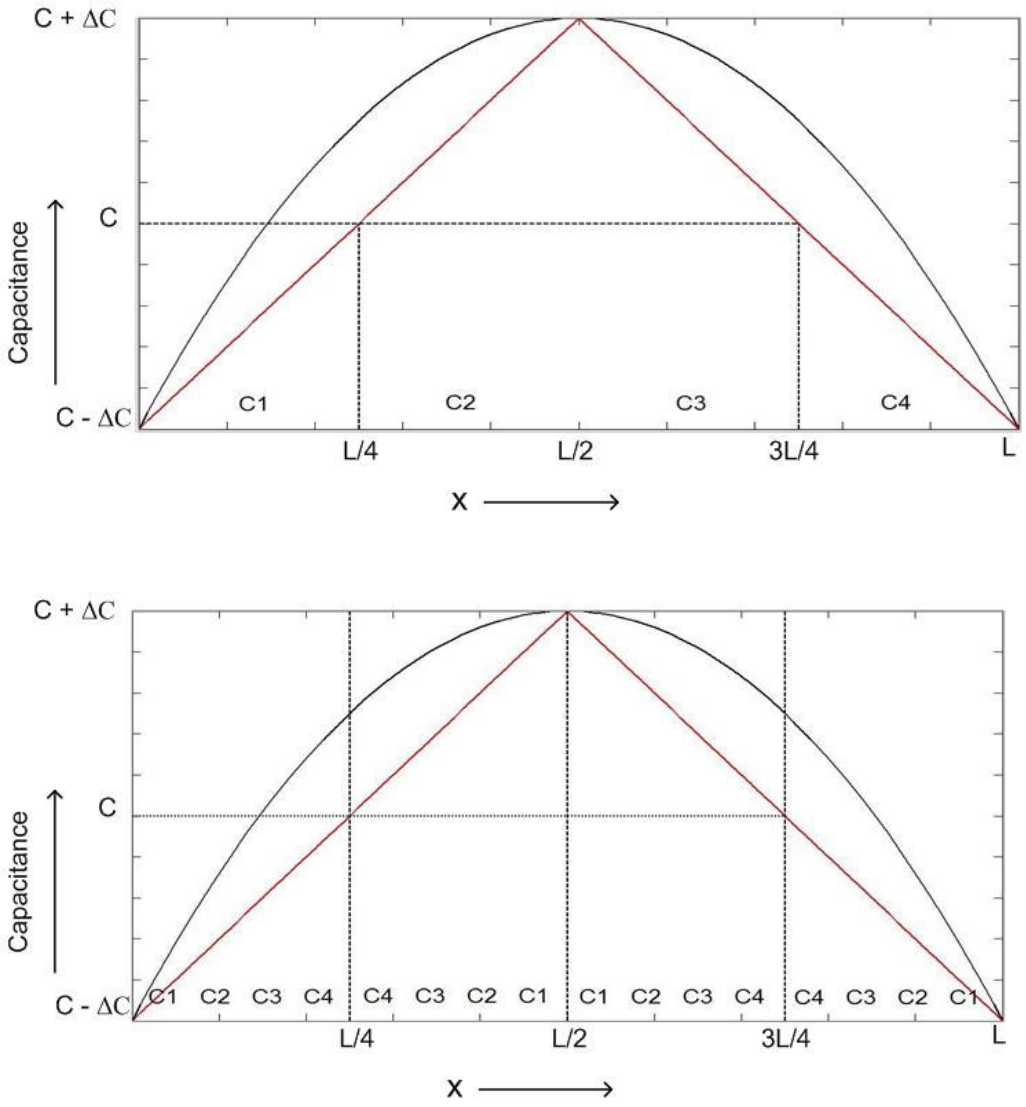


Fig. 7.8 Quadratic gradients: a) Illustration b) Canceling the gradient

7.3.4 Unit cell

The layout of the unit cells and associated interconnects is very critical for good matching [64]. Fig 7.9 shows the layout of unit cell used for thus test-chip. The unit caps have square top plates with chamfered corners. The capacitors are placed over NWELL for noise isolation. Top plates on each side are connected together and are routed on metal 2. Routing of bottom plates is more critical as each of them goes to a separate net.

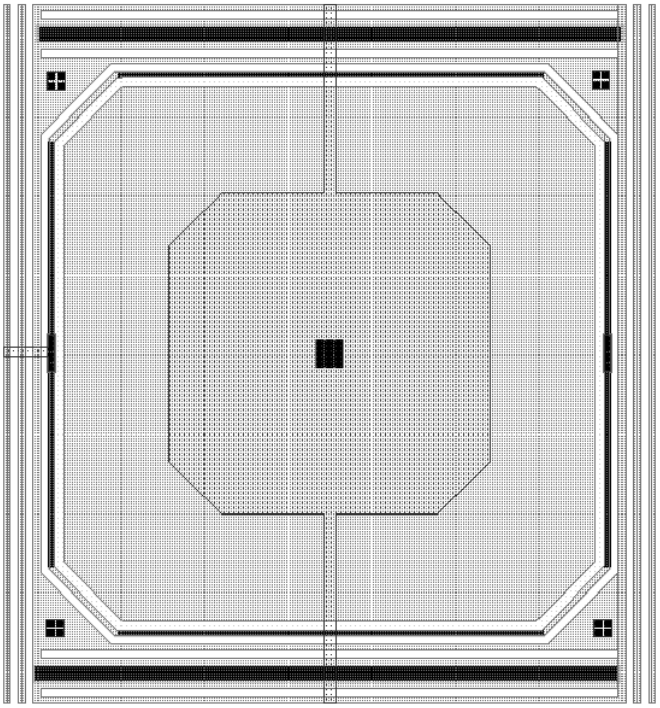


Fig. 7.9. Layout of the unit cell

Bottom plate routing is done in metal 1. The routing is built as a part of unit cell. Though this increases the area of unit cell it helps keep all the routings identical hence avoiding systematic mismatch errors. A ring of dummy caps surrounds capacitor arrays.

7.3.5 Proposed capacitor layouts

In this test-chip we built a DAC with 16 unit elements each with a nominal value of 1.5625pF giving a total capacitor of 25pF. The capacitor array had three different versions. Besides this one more version was built with half the size of unit cell.

Version 1: This is illustrated in Fig 7.10a; there is no attempt to cancel gradients in this version. The n –side is a mirror image of the p-side. Each unit cap is 1.5625pF

Version 2: This is illustrated in Fig 7.10b. Here each unit cap is divided into two half cells (781.25fF) and the capacitors are arranges so as to cancel linear gradients. Total size of each unit element is still 1.5625pF

Version 3: This is illustrated in Fig 7.10c. Here each unit cap is split into four quarters and the quarter cells are arranged so as to cancel quadratic gradients. Total size of each unit element is still 1.5625pF

Version 4: This version is same as Version 1 except that each unit capacitor is half of that in latter. Ignoring gradient effects, from theory we expect the mismatch in version 4 to be $\sqrt{2}$ times the mismatch in version 1.

7.4 Test setup

The test-chip has two test modes. In one test mode we measure the mismatch for differential capacitor array, whereas in second test mode we measure the single-ended cap mismatch. Only one unit element is switched at a time. There is a 4 bit counter inside which selects the unit capacitor to be chosen at a given instance. Ideally we expect an output equal to VREF/16 each time, but because of capacitor mismatches the outputs vary from each other.

For the single-ended case n-side is switched to common mode voltage in both the phases. The ADC used for this characterization is ADS1271. We used ADS1271 Evaluation module (EVM) shown in Fig 7.11 (a) as a daughter board. We designed a motherboard shown in Fig 7.11 (b) on which our test-chip socket is present. This motherboard interacts with the data capture card and pattern generator. The ADS1271 EVM is docked onto the motherboard as illustrated in Fig 7.11(c). The socket used is OZTEK 48pin TQFP socket. The version selection and test mode selection is done through jumpers on the motherboard.

D	D	D	D	D	D	D	D	D	D
D	1p	5p	9p	13p	13m	9m	5m	1m	D
D	2p	6p	10p	14p	14m	10m	6m	2m	D
D	3p	7p	11p	15p	15m	11m	7m	3m	D
D	4p	8p	12p	16p	16m	12m	8m	4m	D
D	D	D	D	D	D	D	D	D	D

a) Version 1

D	D	D	D	D	D	D	D	D	D
D	1p	5p	9p	13p	13m	9m	5m	1m	D
D	2p	6p	10p	14p	14m	10m	6m	2m	D
D	3p	7p	11p	15p	15m	11m	7m	3m	D
D	4p	8p	12p	16p	16m	12m	8m	4m	D
D	16p	12p	8p	4p	4m	8m	12m	16m	D
D	15p	11p	7p	3p	3m	7m	11m	15m	D
D	14p	10p	6p	2p	2m	6m	10m	14m	D
D	13p	9p	5p	1p	1m	5m	9m	13m	D
D	D	D	D	D	D	D	D	D	D

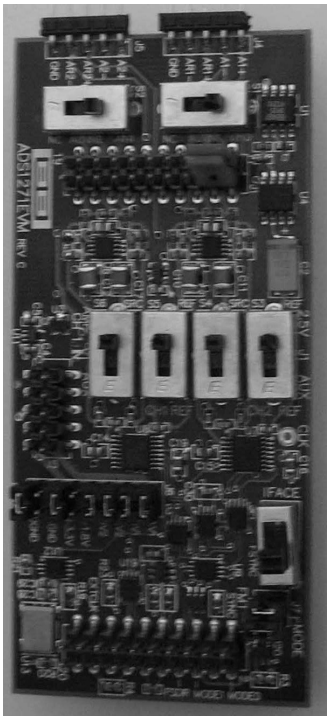
b)Version 2

D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D	1	5	9	13	16	12	8	4	4	8	12	16	13	9	5	1	1	5	9	13	16	12	8	4	4	8	12	16	13	9	5	1	D
D	2	6	10	14	15	11	7	3	3	7	11	15	14	10	6	2	2	6	10	14	15	11	7	3	3	7	11	15	14	10	6	2	D
D	3	7	11	15	14	10	6	2	2	6	10	14	15	11	7	3	3	7	11	15	14	10	6	2	2	6	10	14	15	11	7	3	D
D	4	8	12	16	13	9	5	1	1	5	9	13	16	12	8	4	4	8	12	16	13	9	5	1	1	5	9	13	16	12	8	4	D
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D

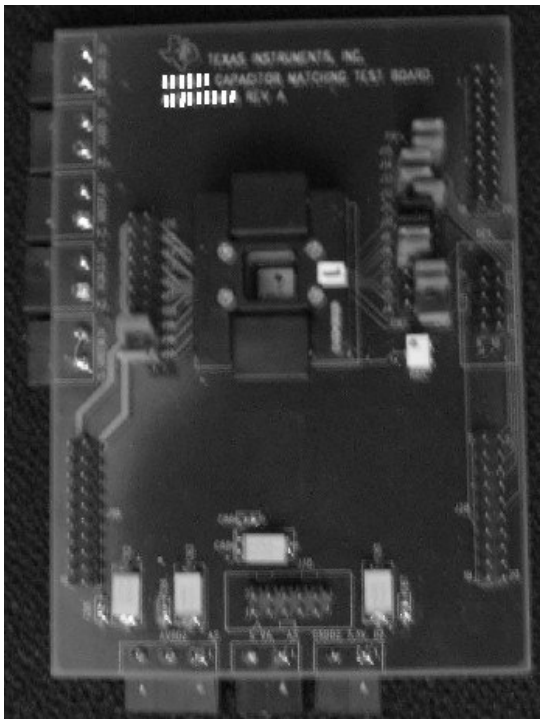
P-side N-side

c) Version 3

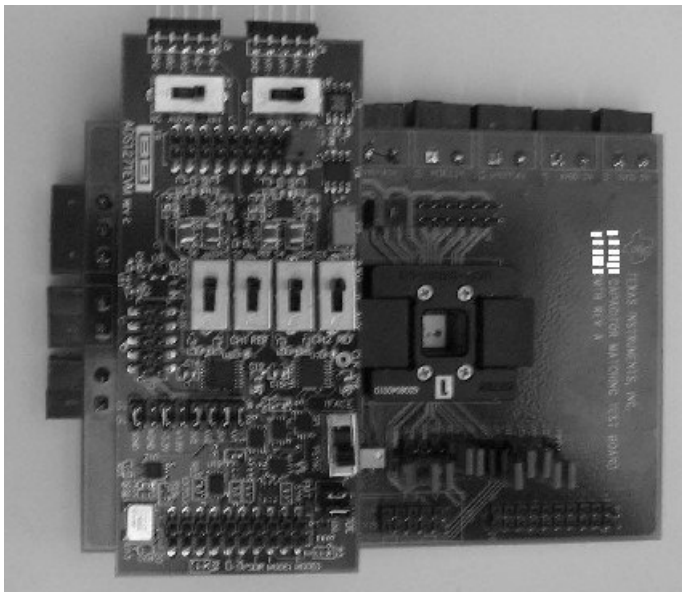
Fig. 7.10. Different capacitor layouts



(a)



(b)



(c)

Fig. 7.11. Test boards a) Daugther Board b) Motherboard c) Daughter board docked on mother board

7.5 Measurement results

Fig 7.12 shows the die-photo of the test-chip. The results were averaged to obtain a measurement accuracy of 16 bits. Fig 7.13 shows the mismatch results for differential capacitor array while Fig 7.14 shows the results for single ended capacitor error. The results are based on data collected from 33 devices.

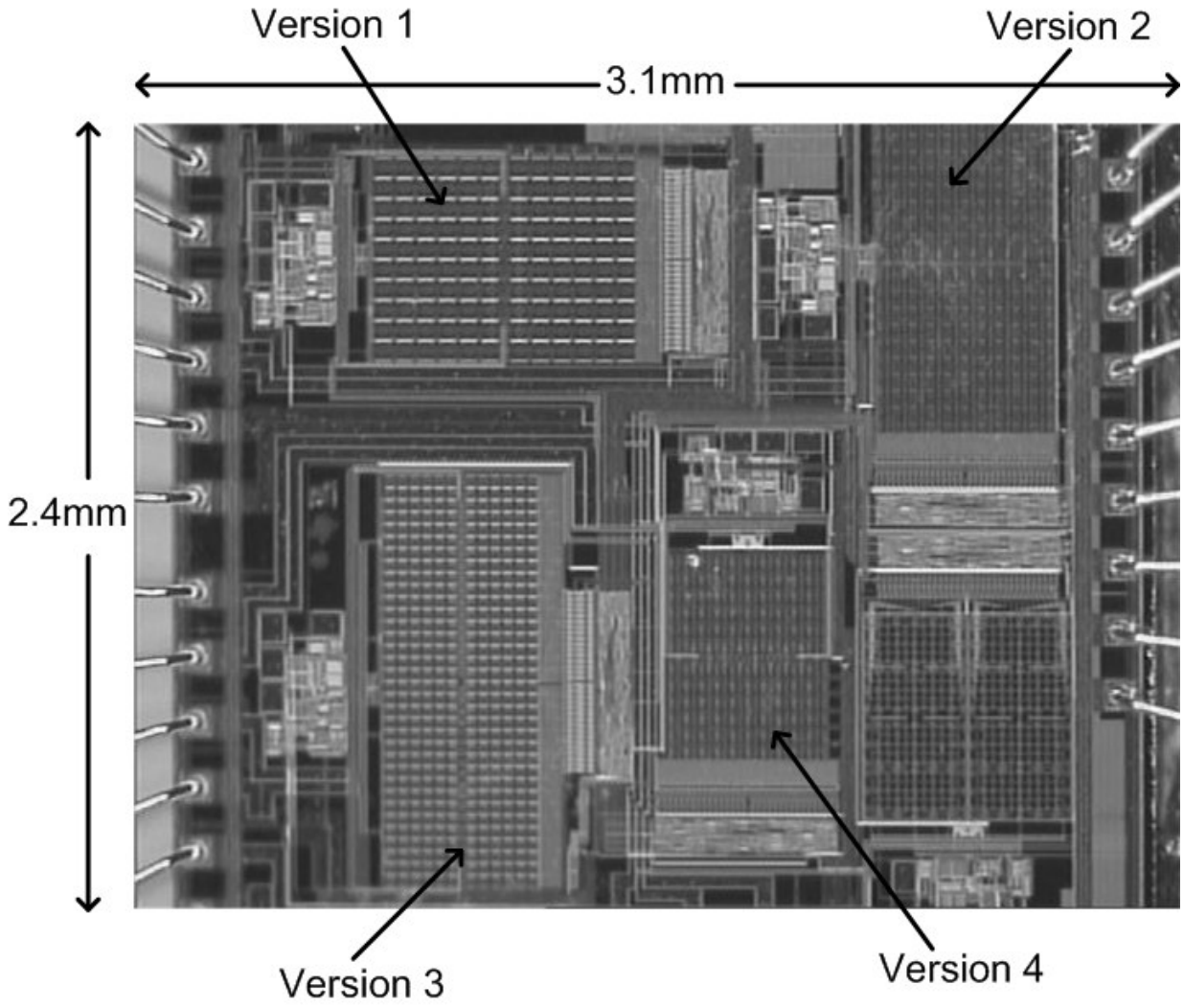
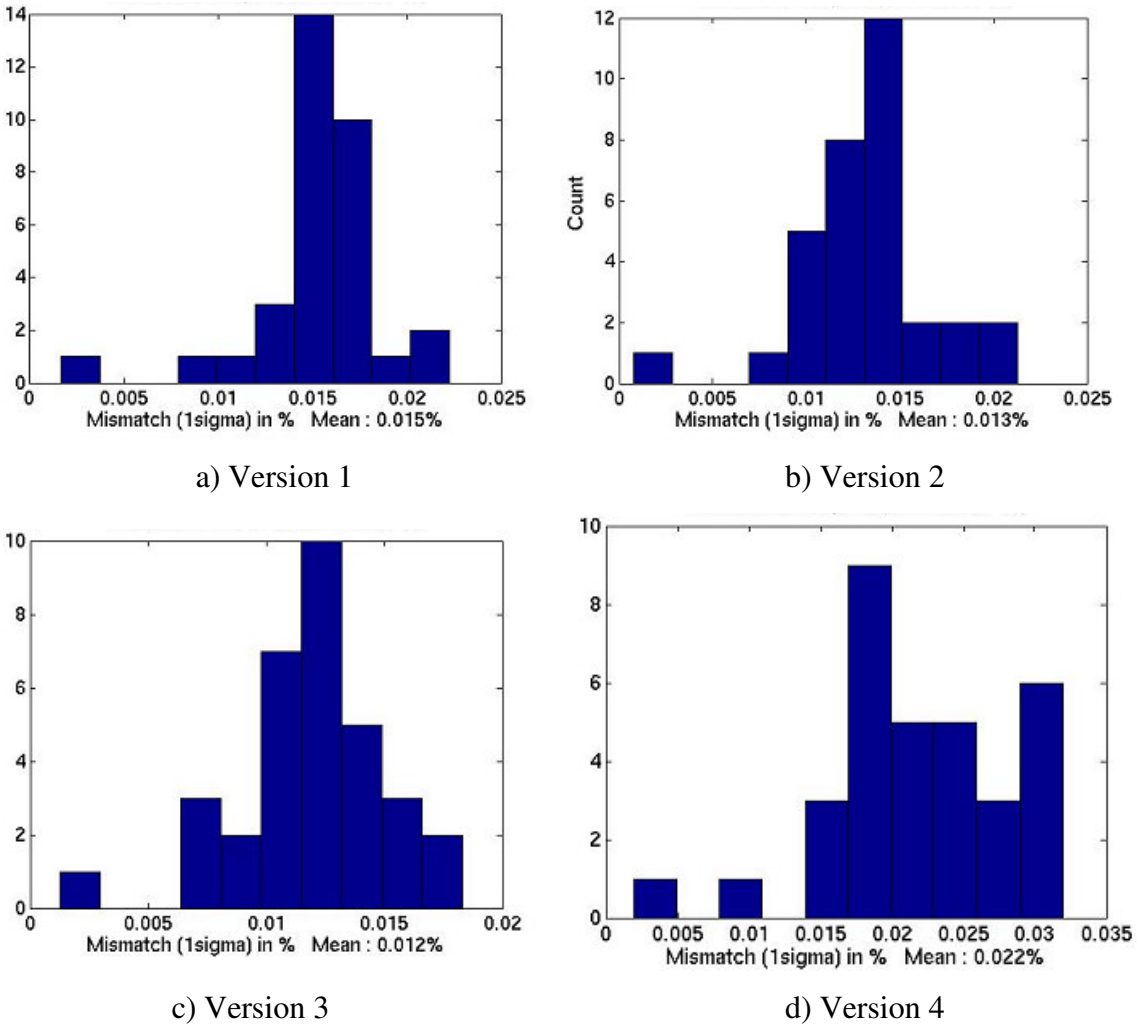


Fig. 7.12. Die photo of the test-chip

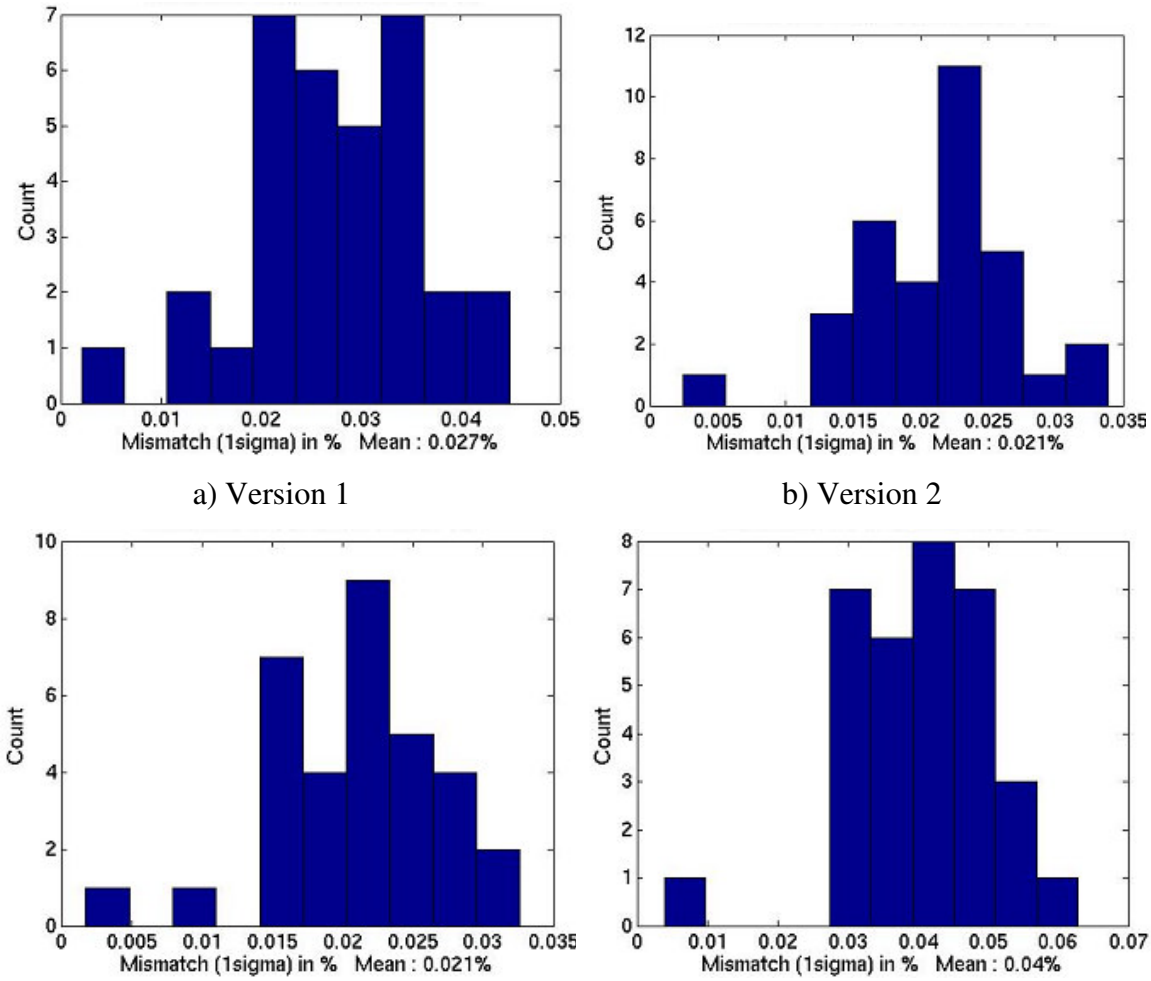
Fig 7.15 shows the mismatch coefficient for each unit elements for different versions. It is clear from the figure that version 1 has systematic errors whereas version 3 has mostly random mismatch. Best results are obtained with quadratic gradient cancellation. The mismatch (1 sigma) for half sized cap array is 1.44 times the mismatch for version1. The mismatch results are summarized in Table 7.1



a) Version 1 b) Version 2

c) Version 3 d) Version 4

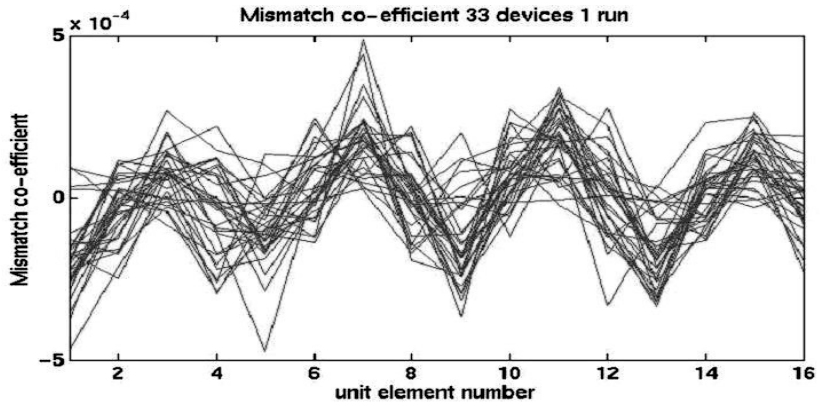
Fig. 7.13. Mismatch (1 sigma) for differential capacitor array



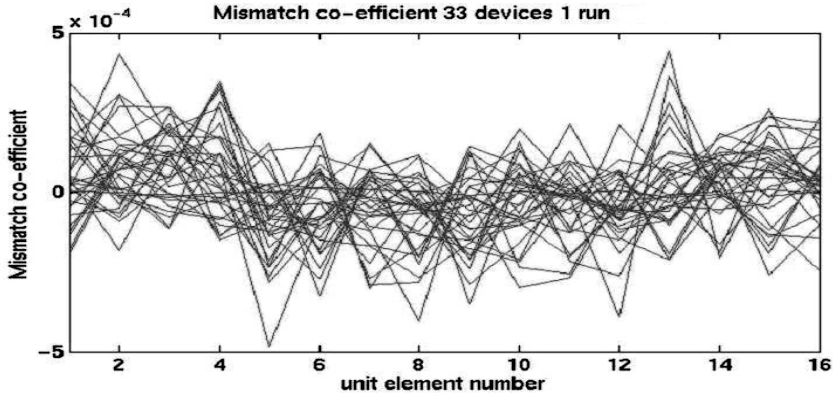
a) Version 1 b) Version 2

c) Version 3 d) Version 4

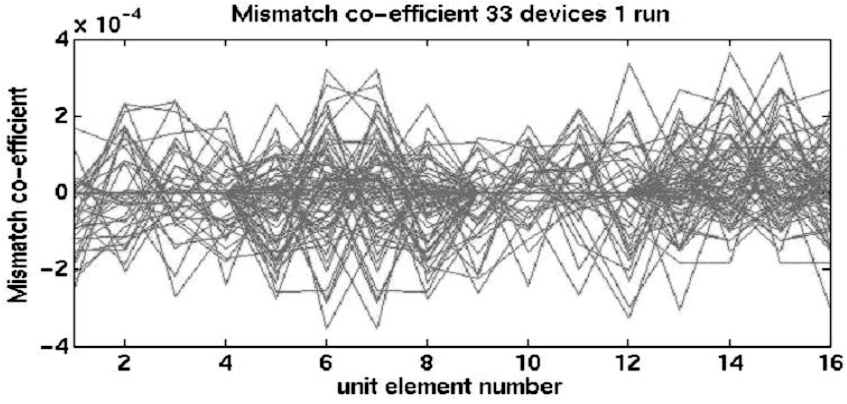
Fig. 7.14. Mismatch (1 sigma) for single-ended capacitor array



a) Version 1



b) Version 2



c) Version 2

Fig.7.15. Mismatch coefficient for 16 unit elements

Table 7.1. Mismatch results summary

Version	Differential mismatch (Mean sigma)	Single-ended mismatch (Mean sigma)
Version 1: No gradient cancellation, unit = 1.5625pF	1.51e-4	2.72e-4
Version 2: Linear gradient cancellation, unit = 1.5625pF	1.33e-4	2.13e-4
Version 3:Quadratic gradient cancellation, unit = 1.5625pF	1.18e-4	2.11e-4
Version 4 : No gradient cancellation, unit = 1.5625pF	2.18e-4	3.99e-4

7.6 Conclusion

In this section we present a method to characterize capacitor mismatch in multi-bit DAC. The mismatch coefficients determined in this way can be used for calibration in a delta sigma ADC as discussed in last chapter. Next we present different methods of canceling gradient effects in a capacitor array. A test chip was built with four different versions of capacitor array. From the measurement results obtained we conclude that quadratic gradient cancellation gives the best results. This chip validates the result from equation (7.7) that random matching improves as square root of area.

CHAPTER VIII
BROADBAND CONTINUOUS TIME ΣΔ ADC*

8.1 Introduction

Continuous time sigma delta modulators (CTM) are increasing becoming popular for low power broadband analog to digital conversion. A block diagram of CTM is shown in Fig 8.1. Here a continuous time loop filter replaces the discrete time loop filter and the sampling is moved from in front of loop filter to after the loop filter. There are lots of advantages in designing high-resolution broadband converters using continuous time techniques. Below we list some of them

- **High speed input drivers are not required:** As discussed in Chapter II, the input driver of a switched capacitor ADC sees a switching load and the output of the driver must settle within half a clock cycle. The step at the output is the worst loading condition for the input driver. For a CTM there is not sampling at the input so the input doesn't see any switching load. The input driver only sees a resistive load if active RC integrator is used or gate/ base impedance if gm-C filter is used.
- **Boost switches are not required:** The design of sampling network is relaxed to a great extent. The error introduced in the sampling process is now attenuated by the loop gain so a simple CMOS switch will mostly suffice.
- **Higher sampling rates are possible**: This is due to the fact that the integrators are no longer clocked so the bandwidth requirements on the amplifiers for integrators are eased.
- **Inherent anti-aliasing property:** Continuous time modulators have an inherent anti-aliasing property. The amount of filtering depends on the order of loop filter and the architecture of loop filter. Loop filters with feed forward architecture have only first order roll –off at high input frequencies.

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*Part of this chapter has been reprinted from "State space approach to design of continuous time sigma delta ADC with delay in feedback path," by A.K.Gupta, E.Sanchez-Sinencio, August 2006, Proc. IEEE MWSCAS. Copyright IEEE, 2006.

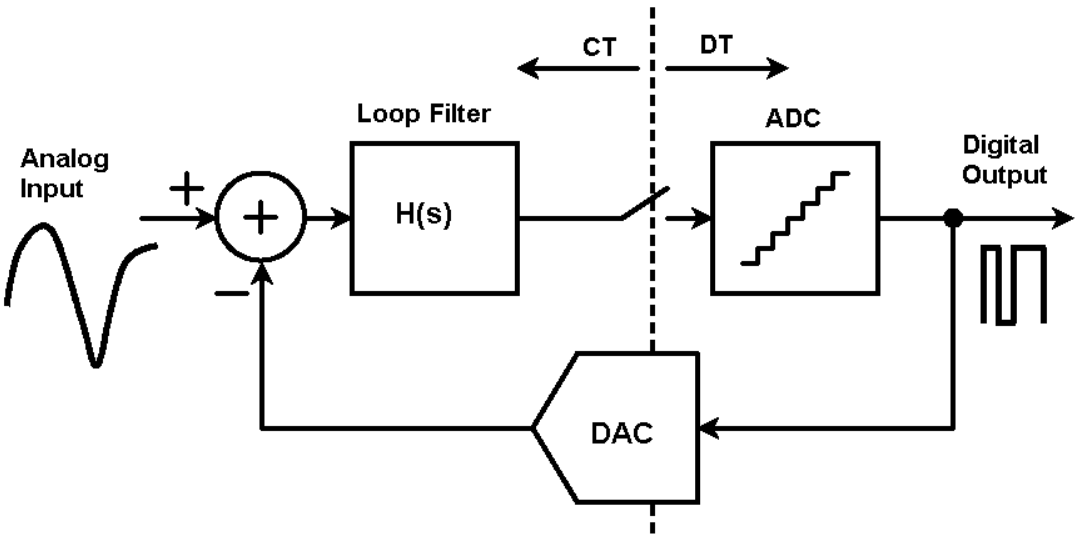


Fig. 8.1. General block diagram of continuous time sigma delta modulator

- **Lower power consumption:** This is a direct consequence of using lower bandwidth amplifiers. Also getting rid of the input driver reduces power consumption. Since there is no sampling in loop filter the wide band thermal noise doesn't fold to baseband leading to better SNR performance.

There also some issues in designing CTM, which are discussed below:

- **Not scaleable with clock frequency:** Unlike their discrete time counterparts, the continuous time modulators do not scale with clock frequency. This means that a CTM designed to operate with a clock frequency of 100Mhz will not operate with a clock of 25Mhz.
- **Excess Loop delay:** This arises due to finite response time of the flash ADC and feedback DAC. Ideally the delay from time the ADC samples to the time DAC provides feedback should be zero. But in any actual circuit there is a finite delay in the comparator and DAC. It leads to instability in the modulator and results in degradation in SNR. In earlier work the attempt was made to keep this delay to less than 10% of the clock period. This generally meant fast comparators consuming lot of power. A solution to this problem shown in Fig 8.2 was first presented in [65] and then implemented in [66,67]. The idea is to provide an additional feedback path, which

provides the first output of desired impulse response. Now comparators have half clock time to provide decision, so they can be slowed down, saving power. We will look in detail, on designing modulators with delay in feedback path in next section.

- **Clock jitter:** Continuous time modulators are more sensitive to clock jitter than their DT counterparts. One option to reduce sensitivity to jitter is to increase the number of levels in the feedback DAC. Other option is to use a switched capacitor DAC instead of a current mode, but it requires use of high bandwidth opamps in the integrators and so is not very desirable.
- **Asymmetry in DAC waveform:** In general CTM's are sensitive to the shape of DAC pulse; any non-uniformities will tend to degrade performance. Specifically unequal rise/fall time of DAC pulses lead to non-linearity. It has been argued in [68] that fully differential circuits are inherently symmetric, so this is not a problem if using fully differential circuits. But [69] claims that the THD performance for them is limited by asymmetry in DAC waveforms, as even though the design is meant to be fully differential, it may not be the case in final implementation. The use of RZ DAC pulse will solve the problem, but will lead to increased sensitivity to jitter. Only solution is to make DAC waveforms should be made as steep as possible.
- **Nonlinearity of feedback DAC:** This is same as in discrete time modulators. Dynamic element matching (DEM) and calibration techniques discussed in chapter V and chapter VI can be used.

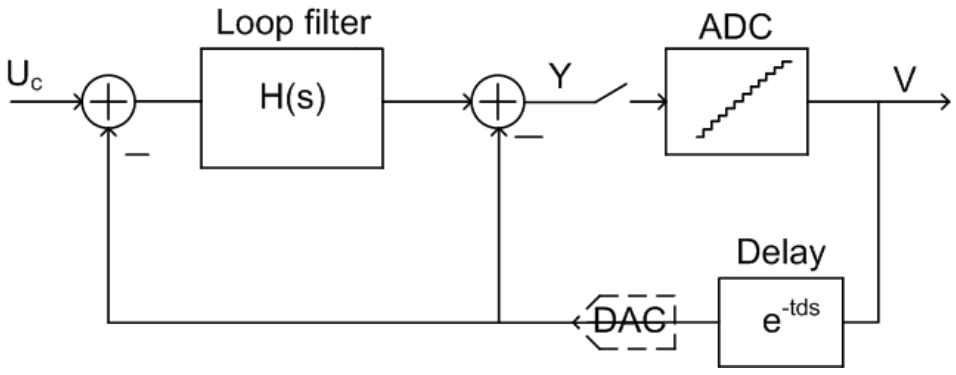


Fig. 8.2. Excess loop delay compensation with additional feedback path.

Table 8.1. Recent continuous time sigma delta modulators

Reference/yr/ Affiliation	Signal BW	SNR	DR	SNDR	Power (mW)	Process
[66] 2004 /TAMU	1.1Mhz	84dB	93dB	83dB	62mW	0.5uCMOS
[67] 2005/ TI, Dallas	600khz	77dB	_	74dB	6.0mW	90nm, CMOS
[69] 2005/ Infenion Technologies, Austria	2Mhz	72dB	_	71dB	3mW	0.13um, CMOS
[70] 2005/ TI, Dallas	600khz	86dB	_	_	5.4mW	90nm, CMOS
[71] 2004 / Philips, The Netherlands	1Mhz	_	89dB	_	2mW	0.18u CMOS
[72] 2004 / Philips, The Netherlands	10Mhz	_	67dB	_	122mW	0.18u CMOS
[73] 2005/ ADI / Wilmington, MA	20Hz-20Khz	106dB	_	99dB	18mW	0.35u CMOS

Despite the problems associated with design of CTM, some high performance very low power CTM have been designed recently and are summarized in Table 8.1. It appears that while choosing architecture for broadband high-resolution ADC, continuous time sigma-delta modulator is a very serious contender. It is becoming very popular in smaller CMOS technologies, which have significant amount of gate leakage current. Since the loop filter in CTM doesn't sample the signal gate leakage is not a serious concern.

In the next section we develop a state-space based approach for design of CTM with delay in feedback path

8.2 State space approach to design of CTM with delay in the feedback path

Excess loop delay is one of the major sources of instability and signal to noise ratio (SNR) degradation in continuous time sigma delta modulators. This delay is simply the time between the quantizer clock and the DAC current pulse. It has been shown that such a delay increases the order of loop filter by one and hence degrades the stability of the loop [74]. One of the solutions is to provide an additional feedback path just before the quantizer. This feedback path affects only the first sample of the impulse response. This solution shown in Fig 8.1 was originally suggested in [65] and successfully implemented in [66], [67].

The design of CTM is generally done by first designing a discrete time modulator with the loop transfer function G(z) and then transforming it to continuous time H(s) by using an 'impulse invariant' transformation. This transformation can be carried out by either z-transform techniques [74] or state space techniques [75]. In previous work [76], modified z-transform has been used to determine the coefficient of the modulator in Fig 8.2 with arbitrary delay t_d in the feedback path. An optimization method has been suggested in [77] to match the impulse response of delayed and non-delayed transfer function. In this paper we present state space based approach to design the CTM with arbitrary delay in feedback path. This is an extension of work in [75] and leads to very simple design procedure using MATLAB.

We also analyze the CTM with resonators in the loop filter and see that it leads to an infinite series in state space form. It is shown that using some results from the z-transform theory can greatly simplify the design procedure for such CTM

8.2.1 Design with delay in feedback loop

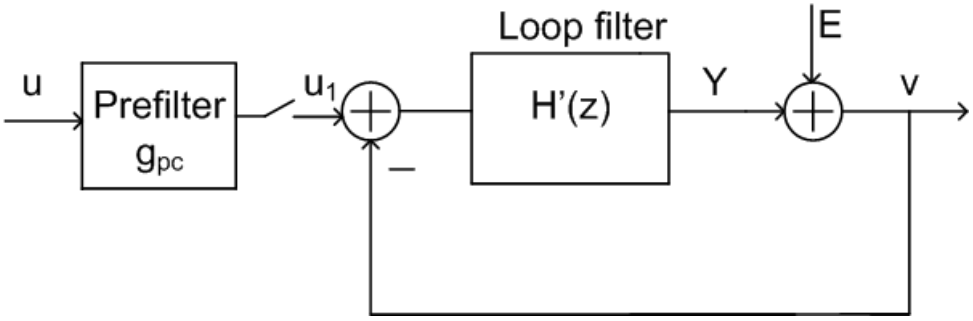
The design procedure starts with designing a discrete time modulator (DTM) with loop transfer function G(z) and then converting it to a continuous time modulator (CTM) such that impulse response of the DTM and CTM at the sampling instant of quantizer is same. We proceed to model the CTM in discrete time, with a pre-filter conditioning the input signal before sampling [75]. This is illustrated in Fig 8.3a, where input signal u is filtered

by a filter g_{pc} and then sampled to give a discrete input signal u_1. Loop filter is assumed to be of order n and feedback to be of NRZ (non-return to zero) type.

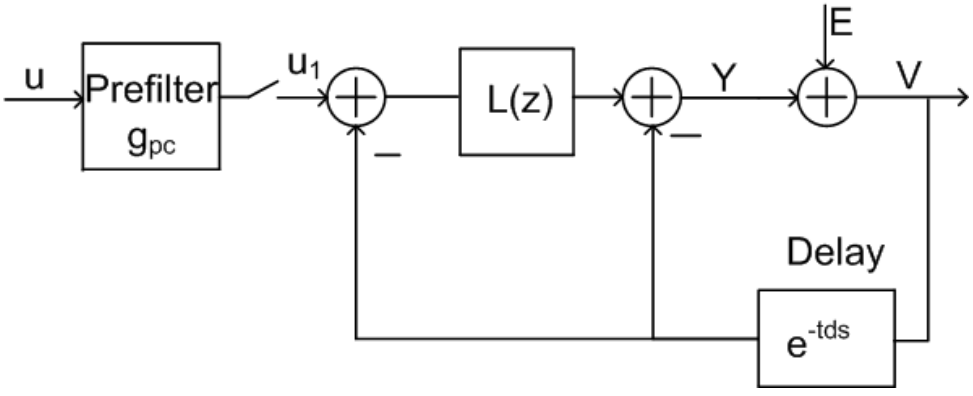
The continuous time modulator in Fig 8.2 has state equations

$$\dot{x}(t) = A_c x(t) + B_c \begin{bmatrix} u(t) \\ v(t - t_d) \end{bmatrix} \tag{8.1}$$

where t_d is the delay in feedback path. It is possible to arbitrarily increase the feedback delay, if properly timed additional feedback paths are provided at the summing node before quantizer. But there is no advantage in having a delay greater than one clock period (T), so in this analysis we will assume that $0 < t_d <= T$.



(a) With delay and additional feedback incorporated in H'(z)



(b) Another representation with $H'(z) = [1+L(z)]e^{-std}$

Fig. 8.3. Discrete time equivalent of continuous time modulator

Equation (8.1) can be solved to give

$$x(t) = e^{A_c(t-t_o)}x(t_0) + \int_{t_0}^{t} e^{A_c(t-\tau)}B_c\begin{bmatrix} u(\tau) \\ v(\tau - t_d) \end{bmatrix}d\tau \tag{8.2}$$

If we let t_0 = kT and t= kT+T, equation (8.2) becomes

$$x(kT+T) = e^{A_cT}x(kT) + \int_{kT}^{kT+T} e^{A_c(kT+T-\tau)}B_c\begin{bmatrix} u(\tau) \\ v(\tau - t_d) \end{bmatrix}d\tau \tag{8.3}$$

Now change of variable from $\tau = kT + T - \lambda$ and defining Bc = [B_{c1}, B_{c2}] gives

$$x(kT+T) = e^{A_cT}x(kT) + \int_0^T e^{A_c(\lambda)}B_{c1}[u(kT+T-\lambda)]d\lambda + \int_0^T e^{A_c(\lambda)}B_{c2}[v(kT+T-\lambda-t_d)]d\lambda \tag{8.4}$$

We note here that output v of the quantizer is piecewise continuous-time signal which changes value only at the sampling instant of the quantizer. If there is no time delay (t_d =0), there will be only one value of v in the second integral. With non-zero t_d , as λ varies from 0 to T, the value of v changes from v(kT) to v(kT-T). Thus second integral can be evaluated as two separate integrals giving

$$x(kT+T) = e^{A_cT}x(kT) + \int_0^T e^{A_c(\lambda)}B_{c1}u(kT+T-\lambda)d\lambda + \int_0^{T-t_d} e^{A_c(\lambda)}B_{c2}v(kT)d\lambda + \int_{T-t_d}^{1} e^{A_c(\lambda)}B_{c2}v(kT-T)d\lambda \tag{8.5}$$

The first integral in equation (8.5) represents a collection of n prefilters

$$g'_{pc} = e^{A_c(\lambda)}B_{c1} \tag{8.6}$$

Each filter connects the input to one of the states in the discrete time model. The output of the prefilters are given by

$$u_1 = u(kT) * g'_{pc} \tag{8.7}$$

To simplify notations let us define

$$\alpha_1 = e^{A_cT} \quad ; \ \beta_1 = \int_{T-t_d}^{1} e^{A_c(\lambda)}B_{c2}d\lambda \quad ; \ \beta_2 = \int_0^{T-t_d} e^{A_c(\lambda)}B_{c2}d\lambda \tag{8.8}$$

Now if we normalize time with respect to T, we can write equation (8.5) as

$$x(k+1) = \alpha_1 x(k) + u_1(k) + \beta_1 v(k-1) + \beta_2 v(k) \tag{8.9}$$

If we want to get above in state space form, we must eliminate term containing v(k-1) from the right side. This can be done if we define a new state $x_{n+1}(k) = v(k-1)$. Thus the state space representation for CT modulator is given by

$$\begin{bmatrix} x(k+1) \\ x_{n+1}(k+1) \end{bmatrix} = \begin{bmatrix} \alpha_1 & \beta_1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} x(k) \\ x_{n+1}(k) \end{bmatrix} + \begin{bmatrix} \beta_2 \\ 1 \end{bmatrix} v(k) + \begin{bmatrix} 1 \\ 0 \end{bmatrix} u_1(k)$$

$$y(k) = [C_c \quad D_{c2}] \begin{bmatrix} x \\ x_{n+1} \end{bmatrix} + [D_{c1} \quad 0] \begin{bmatrix} u \\ v \end{bmatrix} \tag{8.10}$$

Thus we observe that equation (8.10) is one order higher than the original continuous time system with which we started. This result has been derived earlier in [74] using z-transform techniques. The loop filter transfer can be found using

$$H'(z) = C'(zI - A')^{-1} B_2' \tag{8.11}$$

where

$$A' = \begin{bmatrix} \alpha_1 & \beta_1 \\ 0 & 0 \end{bmatrix}, \quad B_2' = \begin{bmatrix} \beta_2 \\ 1 \end{bmatrix}, \quad C' = [C_c \quad D_{c2}] \tag{8.12}$$

For the continuous time modulator to have same impulse response as DTM we must now equate G(z) to H'(z). To illustrate the procedure we take example of a second order CT modulator shown in Fig 8.4. We wish to determine the coefficients [b_1, b2, b3] such that CTM has same impulse response as DTM defined by

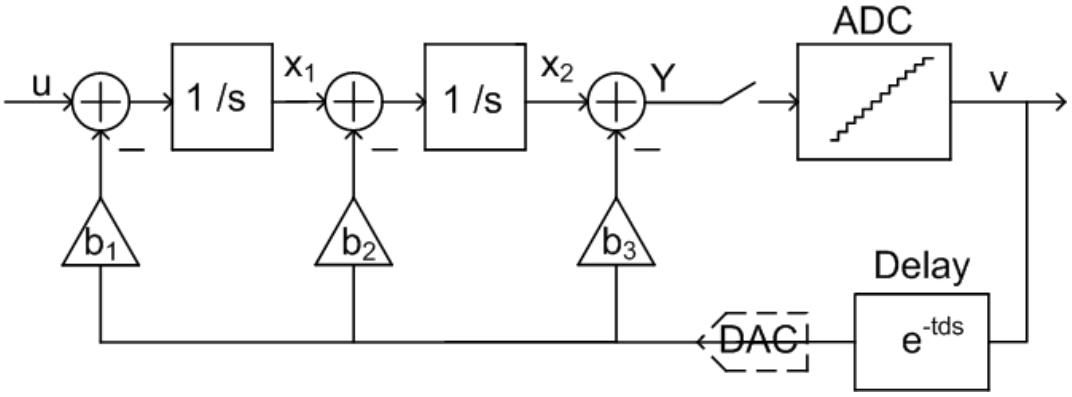


Fig. 8.4. Second order modulator with delay in feedback path

$$NTF(z) = \frac{(z-1)^2}{z^2 + a_1 z + a_0},\ \mathrm{G(z)} = \frac{1}{1 - \mathrm{NTF(z)}} \tag{8.13}$$

We chose delay = 0.5 for this example (time normalized with T). The state equation for modulator in Fig 8.4 is given by

$$A_c = \begin{bmatrix} 0 & 0 \\ 1 & 0 \end{bmatrix} \quad , \quad \mathrm{B_{c2}} = \begin{bmatrix} \mathrm{b_1} \\ \mathrm{b_2} \\ \mathrm{b_3} \end{bmatrix} \tag{8.14}$$

Evaluating equation (8.8) gives

$$\alpha_1 = \begin{bmatrix} 1 & 0 \\ 1 & 1 \end{bmatrix} \quad , \quad \beta_1 = \begin{bmatrix} -0.5b_1 \\ -0.375b_1 - 0.5b_2 \end{bmatrix}, \qquad \beta_2 = \begin{bmatrix} -0.5b_1 \\ -0.125b_1 - 0.5b_2 \end{bmatrix} \tag{8.15}$$

Substituting in equation (8.14) gives

$$A' = \begin{bmatrix} 1 & 0 & -0.5\mathrm{b_1} \\ 1 & 1 & -0.375\mathrm{b_1} - 0.5\mathrm{b_2} \\ 0 & 0 & 0 \end{bmatrix} \quad B_1' = \begin{bmatrix} -0.5b_1 \\ -0.125b_1 - 0.5b_2 \\ 1 \end{bmatrix} \quad C' = [0 \quad 1 \quad -\mathrm{b_3}] \tag{8.16}$$

Now equation (8.11) can be solved and the result equated with G(z) , which gives

$$[b_1, b_2, b_3] = \left[1 + a_1 + a_0,\ 2 + a_1, \frac{7 + 3a_1 - a_0}{8}\right] \tag{8.17}$$

The above procedure guarantees that the noise transfer function is as desired. The input signal to the modulator is pre-filtered by g_{pc} as shown in Eq (8.8). For the example above

$$G_{pc}(s) = \left[\frac{1 - z^{-1}}{s}\right]^2 \text{ where } z = e^s$$

Now we want to analyze how the delay in the feedback path affects the signal transfer function. Let us assume that there is no delay, in this case desired discrete time transfer function G(z) and the discrete equivalent of CT design H'(z) are same, thus STF is given by

$$STF = G_{pc}(s)\frac{G(z)}{1 + G(z)} \tag{8.18}$$

Now with a delay in the feedback, by the above procedure we found a new transfer function H'(z) such that $G(z) = H'(z)$. Referring to Fig 8.3(b) we note that

$$H'(z) = [1 + L(z)]e^{-st_d} = G(z) \tag{8.19}$$

The signal transfer function STF is given by

$$STF = G_{pc}(s)\frac{L(z)}{1+[1+L(z)]e^{-st_d}} = G_{pc}(s)\frac{G(z)e^{st_d}-1}{1+G(z)} = G_{pc}(s)\left[\frac{G(z)e^{st_d}}{1+G(z)} - \frac{1}{1+G(z)}\right] \tag{8.20}$$

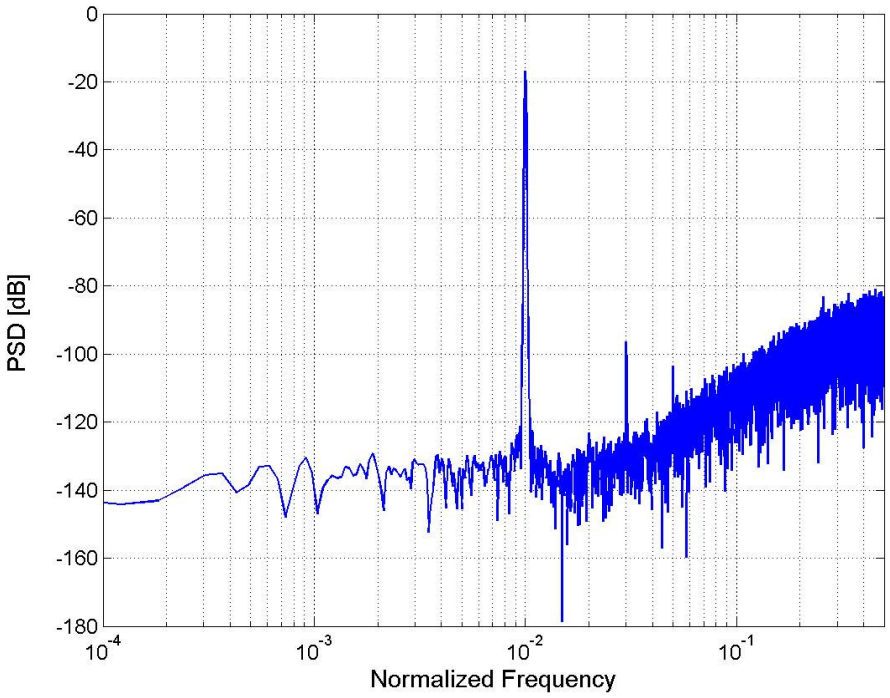
The second term in the bracket can be ignored for the baseband signal, where loop gain is large. Thus comparing equation (8.20) and equation (8.18) we observe that the STF with delay is same as without delay except for time advancement. This time advancement is absorbed by the pre-filter $G_{pc}(s)$, which has a delay of one clock period. The results are verified for the modulator in Fig 8.4 with the NTF as $(1-z^{-1})^2$. The quantizer is assumed to be 4-bit and reference voltage of one volt is assumed. The power spectral density is illustrated in Fig 8.5a and the signal transfer function is illustrated in Fig 8.5b.

The analysis presented above becomes involved for higher order systems. It is at least as complex to solve for coefficient as using modified z-transform techniques. So it becomes essential to automate the procedure using MATLAB.

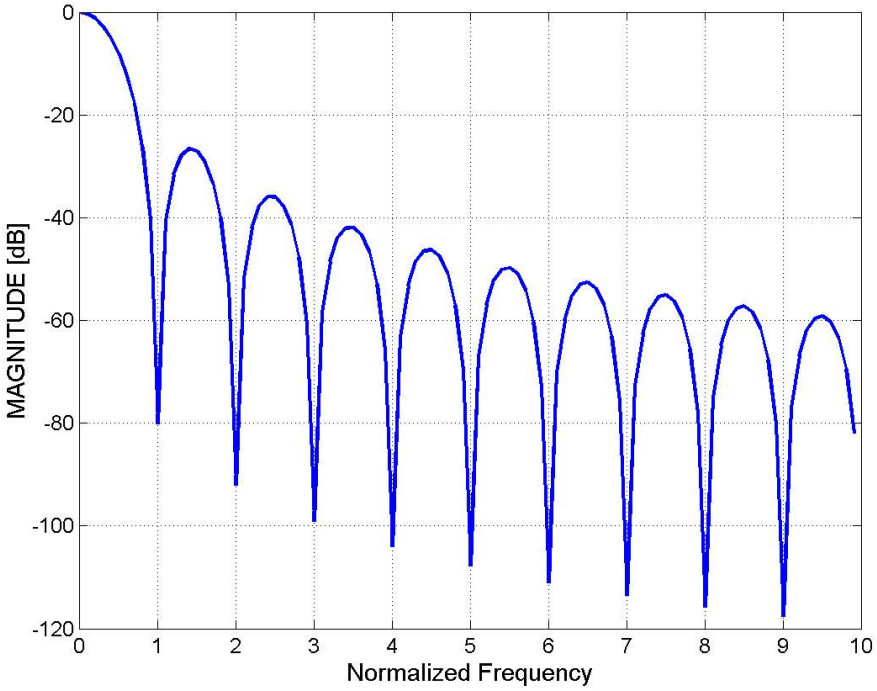
8.2.2 Loop filters with resonators

It is well known that having all the poles of the loop filter at dc doesn't give the optimal signal to quantization noise ratio (SQNR). Optimal transfer functions can be found by having some of the poles as complex conjugate, spread over the pass band [48]. Figure 8.6 shows a 3rd order modulator with such a pole pair at $s = \pm j\sqrt{g_1}$. The desired NTF obtained using Schreier's Delta Sigma toolbox [78] for a 5 bit ADC and OSR =16, is

$$NTF(z) = \frac{(z-1)(z^2-1.977z+1)}{(z-0.4009)(z^2-0.823z+0.3607)} \tag{8.21}$$



a) Output power spectral density



b) Signal Transfer function

Fig. 8.5. Second order modulator

We want to determine the coefficient [b_1, b_2, b_3, b_4, g_1]. For the CT system, the state space matrices are

$$A_c = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & -g_1 \\ 0 & 1 & 0 \end{bmatrix}, \quad B_{c2} = \begin{bmatrix} -a_1 \\ -a_2 \\ -a_3 \end{bmatrix} \tag{8.22}$$

$$C_c = [0 \;\; 0 \;\; 1] \qquad D_c = [-a_4]$$

Next we proceed to determine $\alpha_1 = e^{A_c}$;

We can expand α_1 as a series [79]

$$e^{A_c} = I + A_c + \frac{1}{2!}A_c^{\,2} + \frac{1}{3!}A_c^{\,3} + \ldots \tag{8.23}$$

This series expansion terminated in the example in Section II, but for present A_c, it gives

$$\alpha_1 = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} + \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & -g_1 \\ 0 & 1 & 0 \end{bmatrix} + \frac{1}{2}\begin{bmatrix} 0 & 0 & 0 \\ 1 & -g_1 & 0 \\ 1 & 0 & -g_1 \end{bmatrix} + \frac{1}{6}\begin{bmatrix} 0 & 0 & 0 \\ g_1 & 0 & g_1^{\,2} \\ 0 & -g_1 & 0 \end{bmatrix} + \frac{1}{24}\begin{bmatrix} 0 & 0 & 0 \\ 0 & g_1^{\,2} & 0 \\ -g_1 & 0 & g_1^{\,2} \end{bmatrix} + \ldots\ldots$$

If g_1 was known we could have solved this numerically, but since we are solving for g_1 we cannot proceed further. One way is to vary the value of g_1, solve the equations with that g_1, and select g_1, which gives the impulse response, closest to the desired DT response.We find it more efficient to use the following results from [78]

$$Z\left(\frac{\omega}{s^2+\omega^2}\right) = \frac{z\sin\omega}{z^2 + 2z\cos\omega + 1} \tag{8.24}$$

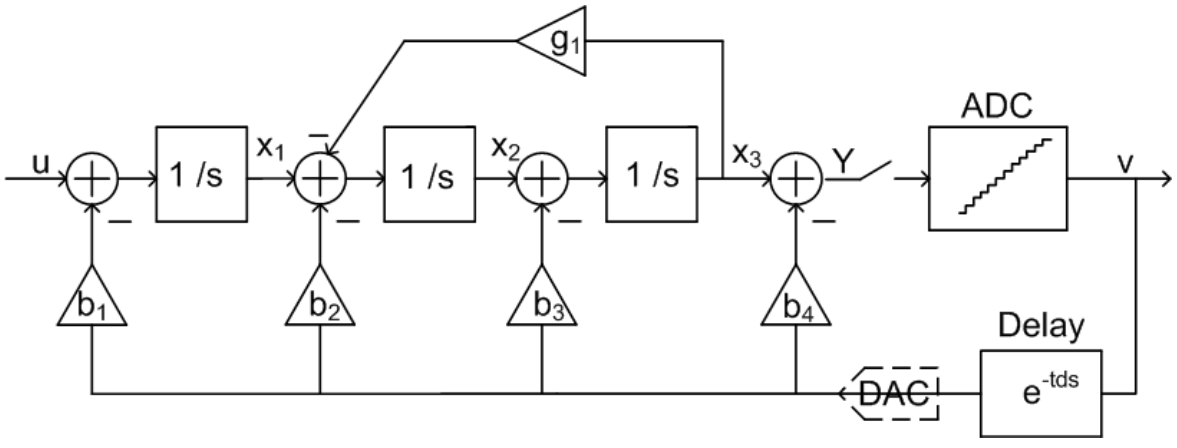


Fig. 8.6. A third order loop filter with a pole pair at s = +/-j $g_1^{1/2}$

It is easy to see that the loop filter in Fig 4 will have complex pole pair at $\pm j\sqrt{g_1}$, which gives a factor $1/s^2+g_1$. This corresponds to pole pair at $z = e^{\pm j\sqrt{g_1}}$, which gives a factor of $(z^2 - 2z\cos\sqrt{g_1} + 1)$ in the denominator of loop transfer function. Thus g_1 can be directly determined by observing the desired DT transfer function. Once g_1 is determined the analysis can proceed with state space analysis. Since this system becomes fourth order once delay is taken into account, we will not attempt to solve for coefficients manually, instead we use MATLAB for the same in next section.

8.2.3 Design examples with MATLAB

In this section we obtain the coefficients for modulator in Fig 8.6 using MATLAB. The easiest way to determine coefficient in MATLAB is to define the system as a four input, one output system. Next impulse response due to each input is computed. The desired impulse response is a weighted sum of the four individual impulse responses. The required coefficients are the weights for different inputs.

```
z = tf('z',1);
N = [(z-1)*(z^2-1.977*z+1)]/[(z-0.4009)*(z^2-0.823*z+0.3607)];
H = 1 - (1/N);                          %% Loop filter  transfer function
g1 = (acos(0.9885))^2;
y = impulse(H,10)';                     %% Desired impulse response
%% CT Loop filter  as a 4-input, 1 output system
Ac = [0 0 0 ; 1 0 -g1; 0 1 0];  Bc = [-1 0 0 0;0 -1 0 0 ;0 0 -1 0];
Cc = [0 0 1];   Dc = [0 0 0 -1];
td = 0.5;                               %% desired time delay
sys_c = ss(Ac,Bc,Cc,Dc);
set(sys_c,'InputDelay',td*[1 1 1 1]);
sys_d = c2d(sys_c,1);
yy = squeeze(impulse(sys_d,10))';
b = y/yy;                       % Solve for coefficients s.t b*yy = y
```

Fig. 8.7 Matlab code to determine the coefficient of modulator with feedback architecture

Table 8.2. Coefficients for modulator in Fig 8.5

Coefficients Delay	b_1	b_2	b_3	b_4	g_1
$t_d = 0$	0.3228	0.8994	1.2553	0.0000	0.02304
$t_d = 0.5$	0.3228	1.0436	1.7413	0.7462	0.02304
$t_d = 1$	0.3228	1.1818	2.2979	1.7531	0.02304

This procedure can be applied only if we know g_1, since then only e^{Ac} can be evaluated. We determine g_1 as discussed in section III. The MATLAB code to determine the coefficients is given in Fig 8.7. The coefficients for different value of delay are listed in Table 8.2. It should be noted the coefficients obtained above have not been scaled for dynamic range. The simulated power spectral density for the modulator is shown in Fig 8.8 with the NTF as given in (8.21) and delay of 0.5. The result is quite similar with different values of delay.

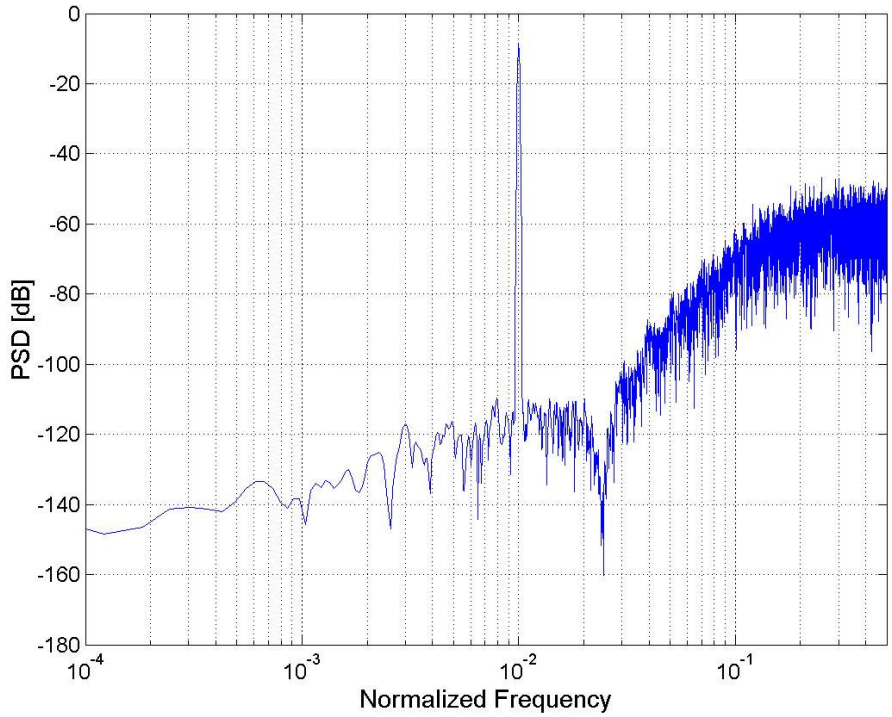
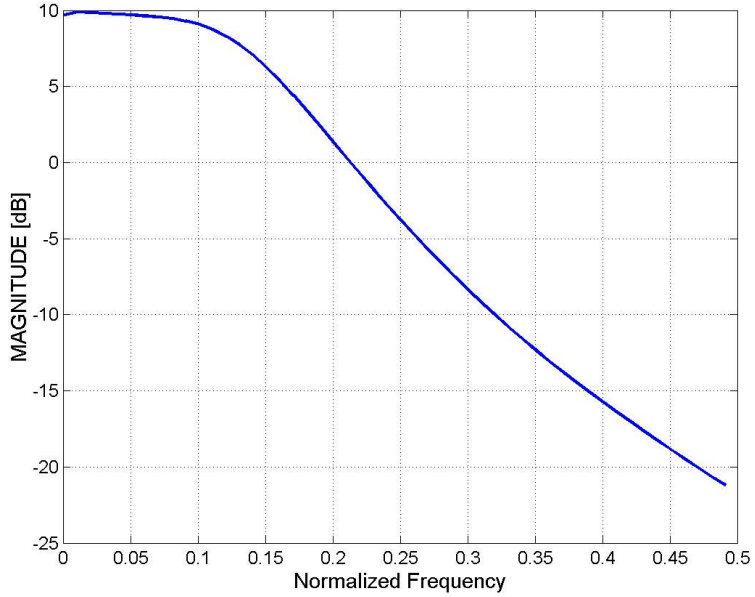
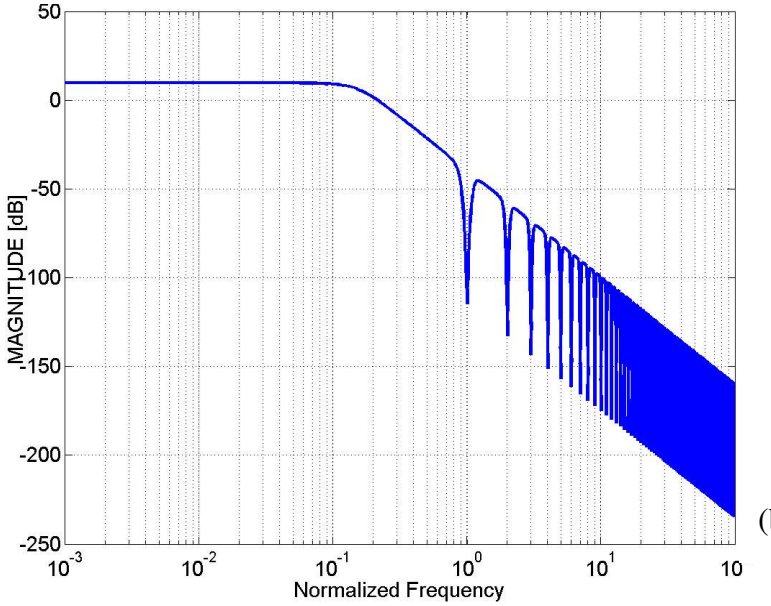


Fig. 8.8. Power spectral density for all pole third order modulator

The signal transfer function for the in-band signals is illustrated in Figure 8.9a. We observe that for OSR = 16 the signal transfer function is quite flat but it rolls-off for higher frequencies. To illustrate the anti-aliasing property the STF is plotted for frequencies greater than Fs/2 in Fig 8.9b. Since it is an all pole loop filter of order three the role-off is at 60dB per decade, which is very desirable. Also nulls at multiples of Fs help in anti-aliasing.



(a)



(b)

Fig. 8.9. Third order modulator signal transfer function a) in-band ; b) out of band

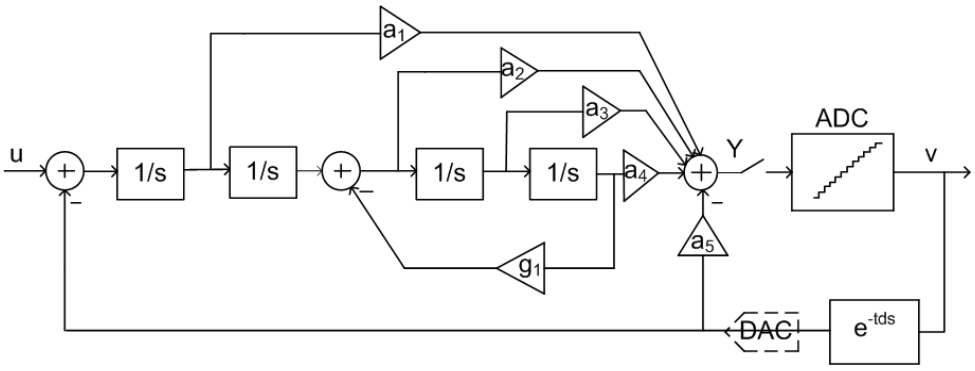


Fig. 8.10. A fourth order loop filter with feedforward architecture

Next we look into a feed-forward architecture as shown in Fig 8.10. The advantage of this architecture is that it leads to reduce signal swing at the output of integrators. The desired NTF obtained using delta sigma toolbox using OSR = 16 and 5 bit feedback DAC is as below

$$NTF(z) = \frac{(z-1)^2(z^2-1.973z+1)}{(z^2-0.9632z+0.2503)(z^2-1.118z+0.5404)} \tag{8.25}$$

```
z = tf('z',1);
N= ((z-1)*(z-1)*(z^2-1.973*z+1))/
     ((z^2-0.9632*z+0.2503)*(z^2-1.118*z+0.5404));    % NTF
H = 1 - (1/N);   g = (acos(0.9865))^2;
y = impulse(H,10)';                    %% Desired impulse response
% CT Loop filter as a 1-input, 5 output system
Ac = [0 0 0 0; 1 0 0 0; 0 1 0 -g; 0 0 1 0];
Bc = [-1 0 0 0 ]';  Dc = [0 0 0 0 -1]';
Cc = [1 0 0 0;0 1 0 0;0 0 1 0;0 0 0 1;0 0 0 0];
td = 0.5;                              %% Input delay
sys_c = ss(Ac,Bc,Cc,Dc);
set(sys_c,'InputDelay',td*[1]);
sys_d = c2d(sys_c,1);
yy = squeeze(impulse(sys_d,10))';
a = y/yy;              % Solve for coefficients s.t a*yy = y_desired
```

Fig. 8.11. Matlab code for modulator with feedforward architecture

Table 8.3. Coefficients for modulator in Fig 8.6

Delay Coefficients	$t_d = 0$	$t_d = 0.5$	$t_d = 1$
a_1	1.2992	1.8701	2.5711
a_2	1.0191	1.2683	1.5392
a_3	0.4753	0.5206	0.5624
a_4	0.0940	0.0872	0.0799
a_5	0.0000	0.7871	1.8918
g_1	0.02706	0.02706	0.02706

In this example we formulate the system as a single input, 5-output system. We compute the output impulse response for all five outputs. The desired impulse response here is the weighted sum of all five outputs and the weights are the required coefficient. The coefficient g_1 is again obtained from observation. The MATLAB code for the above procedure is as shown in Fig 8.11 and the coefficients obtained for various values of delay are compared in Table 8.3.

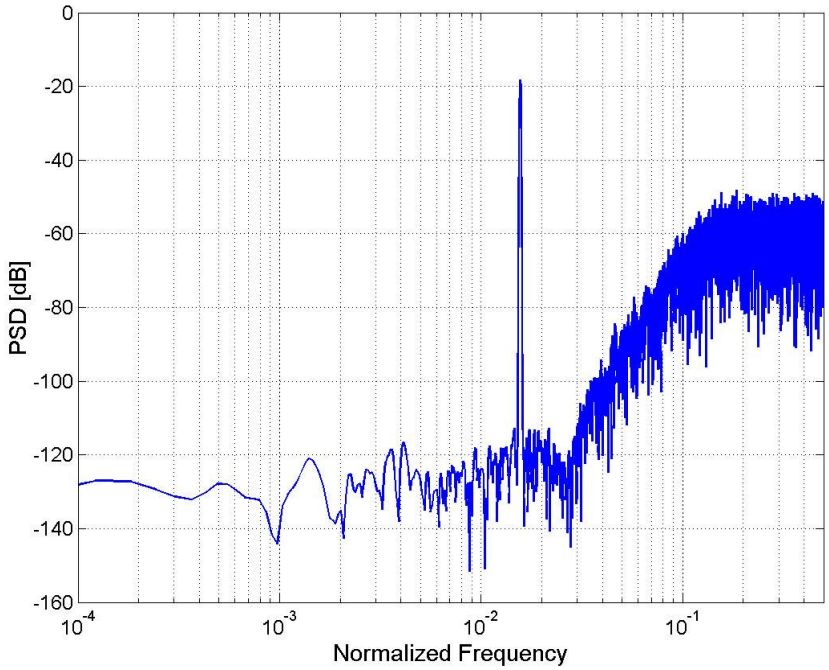


Fig. 8.12. Power spectral density for fourth order feedforward modulator

The simulated power spectral density for the modulator is shown in Fig 8.12 with the NTF as given in (8.25) and delay of 0.5. The result is quite similar with different values of delay. The signal transfer function for the in-band signals is illustrated in Figure 8.13a. We observe that for OSR = 16 the signal transfer function is flat in-band but it peaks at higher frequencies. To illustrate the anti-aliasing property the STF is plotted for frequencies greater than Fs/2 in Fig 8.13b. The roll-off at higher frequencies is only 20dB/decade because of feedforward paths.

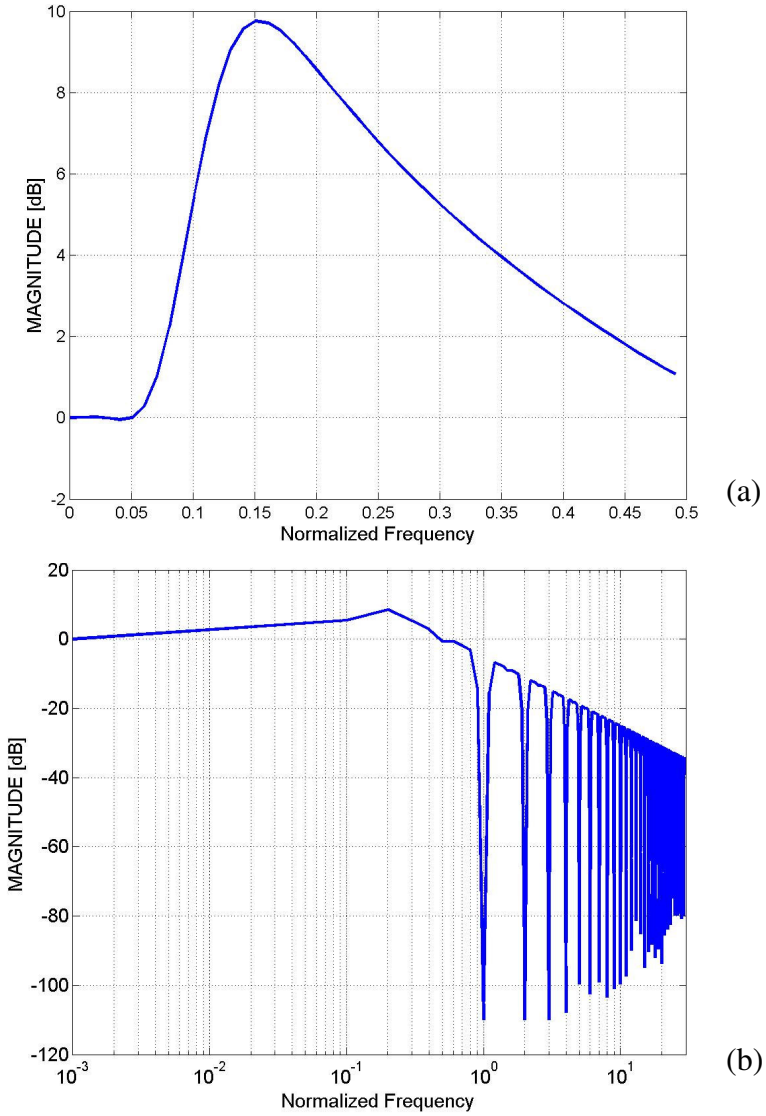


Fig. 8.13. Fourth order feedforward modulator STF a) in-band b) out of band

8.3 Conclusion

In this chapter we have analyzed the continuous time sigma delta modulator with feedback delay using state space techniques. We also analyzed the loop filters with resonators as a special case in which it is not very easy to use the state space technique. We suggest deriving the resonator loop coefficient using z-transform techniques and then proceeding with state space analysis. The techniques discussed in the paper are useful as they can be automated using MATALB and leads to a very simple design procedure.

CHAPTER IX
CONCLUSION

In this thesis we looked into design techniques for low-noise high-speed A/D converters. We discussed some applications for broadband high resolution ADC's. The high dynamic range in ADC may sometimes be required to simplify the front-end design by removing the programmable gain amplifier (PGA) or automatic gain control (AGC). We discussed the need for high-speed drivers for A/D converters and presented a novel precharge scheme to relax the requirements on the driver. We discussed the latch-up problem in two-stage amplifiers and also presented a novel multi-path common mode feedback scheme to solve the problem. We looked at various sample and hold design techniques to achieve very high linearity and presented results for one such technique. Next we looked at dynamic element matching techniques to mitigate the effects of DAC mismatch. We presented a modified second order DEM that outperforms existing DEM techniques. Next we presented some results for calibration in conjunction with DEM, which can help to reduce calibration time. Next we looked into various capacitor array layout techniques and presented measurement results from a prototype test-chip. Finally we presented a method for determining the coefficient for a continuous time sigma delta modulator using state space approach, which can be automated using MATLAB.

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