Indium Phosphide MOS Transistor

Fabrication and Characterization

by

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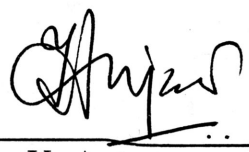

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ABSTRACT

An anodic method of forming an insulator on Indium Phosphide for use in the fabrication of MOS devices is examined. Aluminumin oxide insulating layers are produced from the oxidation of deposited aluminum films in an aqueous solution. MOS capacitors are fabricated. Experimental procedure and methods of analysis are explained. Resulting Capacitance *vs.* Voltage data is given for typical capacitors, and compared to data obtained from MOS capacitors formed from the plasma enhanced chemical vapor deposition of silicon dioxide. Reasons for the generally poor quality insulators which result are discussed.

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INTRODUCTION

The maximum speed of operation is an important characteristic of all electronic components. In the case of digital devices, 'speed' might be defined as the rate at which a pulse can be switched from on to off. Similarly, the speed of an analog device is a measure of the highest frequency at which a signal can be modulated with reasonable fidelity.

Device speed is an important technological consideration. The ever increasing clock rates of digital hardware are at the heart of the ongoing explosion in computing power and efficiency. Analog systems likewise benefit from increases in device speed. The ability to modulate signal sources at higher frequencies implies higher data rates and improved efficiency in communication systems, for example.

BACKGROUND

The semiconductor material used in the fabrication of a given solid-state device determines the ultimate speed of operation of that device. Silicon technology is well established and the vast majority of modern solid-state components are silicon based. As with all semiconductors, however, silicon has inherent limitations with respect to speed of operation. Other semiconductor materials are sought which offer the possibility of faster devices.

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Many semiconductors exhibit properties which make them attractive potential replacements for silicon in some applications. In particular, some compound semiconductors have properties which can be exploited for the fabrication of faster devices. Compound semiconductors such as Galium Arsenide, Indium Arsenide, and Indium Phosphide have been investigated with this goal in mind.

Theoretical Basis for Maximum Device Speed

Electrons in semiconductor materials experience a different 'environment' than electrons in free space. Semiconductor crystals present a very regular array of charged particles (atoms and other electrons) which interact with the conduction electrons. The resulting potential energy associated with each electron is periodic with respect to location. This periodic potential gives rise to electron behavior which cannot be accounted for by classical physics.

A treatment of the semiconductor electron using quantum mechanics is able to predict non-classical behavior. Solutions of the Schrödinger equation applied to models of the electron environment in crystals can be used to define the most pertinent electronic and optical properties of semiconductors. These properties include the electron effective mass, m^*_e, the electron mobility, as well as the band-gap energy, E_g. All of these quantities are measurable, and the Table 1 lists those properties for some semiconductors.

Table 1 quantifies the reasons why some compound semiconductors are expected to be useful in the fabrication of faster devices.

Material	E_g (eV)	m^*_e/m_{eo}	*Mobility* (cm^2/Vs)
Si	1.11	0.97	4,000
InP	1.30	0.08	8,000
GaAs	0.27	0.07	9,000
InAs	1.10	0.02	32,000

Table 1. Semiconductor Properties

The effective mass is the ratio of the force applied to the resulting acceleration of an electron; lower effective mass implies a greater reaction to an applied force. More to the point, mobility is the ratio of applied electric field to the resulting electron velocity. Higher mobility is desired for faster device operation. Both of these quantities suggest that InP, InAs, and GaAs offer large potential increases in the speed of operation of solid state devices compared to those made from Silicon. In addition, the bandgap energies associated with these materials make them valuable in electro-optical applications.

MOS Transistor Structure and Function

Figure 1 shows an idealized cross-section of a Metal Oxide Semiconductor transistor. 'Metal Insulator Semiconductor' is a more general label, since the material between the semiconductor substrate and the metal gate need not be an oxide, only a suitable insulator. The circuit associated with the transistor will cause a current (the 'drain current') to flow through the channel region.

As will be examined later, the ability of the channel to conduct current is dependent on the voltage applied between the gate electrode and the semiconductor.

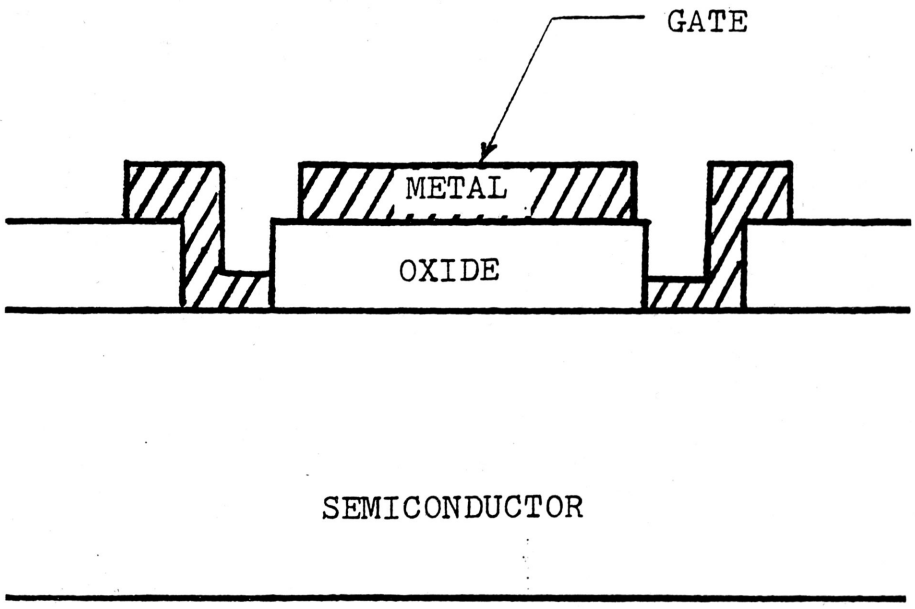

Figure 1. MOS Transistor Structure

The device is therefore a 'voltage controlled current device.' Since virtually no current flows through the insulator, modulation of the drain current is achieved with no expenditure of power – hence gain is introduced into the circuit.

As Figure 1 indicates, the drain current flows at the extreme edge of the semiconductor substrate, just at the insulator-semiconductor interface. This is necessary for the function of the transistor, yet it also means that the values of electron mobility and effective mass quoted in Table 1 may not be valid. Those properties of the material are in effect for electrons in the bulk of the material, and do not necessarily hold for electrons at the interface. However, high electron mobility at the interface must occur if the potential speed advantages of the compound semiconductors are to be realized. A gate insulator which preserves high mobility is therefore sought.

Other required qualities of the insulator can be given: a)Extremely high electrical resistivity; b)Toleration of heat, humidity, handling, and packaging; c)Feasible and economical fabrication process; d)Formation at temperatures substantially less than comparable silicon processes due to possible loss of Group V elements from diffusion.

RESEARCH SCOPE

Methods of Insulator Formation

Possibly the simplest method of forming an insulating layer on a semiconductor substrate is to cause the semiconductor material itself to oxidize. This formation of a so-called 'native' oxide is used extensively with silicon. However, researchers report little success with native oxides of compound semiconductors such as those under consideration. In particular, native oxides of Indium are generally far too conductive for use in MOS devices.[1]

A second technique of forming dielectric layers is by deposition. Silicon dioxide, Silicon nitride, aluminum oxide, as well as various organic films may be deposited on a substrate in a straightforward manner. The technology of deposited dielectrics on silicon is very mature. Compound semiconductors, however, generally require much lower temperature processes than corresponding silicon techniques. The capability of performing depositions at those lower temperatures is relatively new and the machinery required is not available on campus. Engineers at the opto-electronics

division of Honeywell Corporation in Richardson, Texas, were kind enough to perform such a deposition on two samples of InP. The suitability of those insulators will be compared to those built on-campus.

A third alternative is formation of the insulating layer by an anodic process. The sample is exposed to a solution and then biased at high voltages to cause the metal to oxidize. Researchers[2] have constructed both single and double layer insulators on InP using anodization techniques. The resulting dielectrics were generally too conductive and unstable to give meaningful results. Recent work[3] using an anodization solution previously used on GaAs claimed improved quality insulators. That solution[4] was used in this effort.

Research Goals

The original intention of this research was to continue work begun by a graduate student who was investigating the fabrication of MOS structures using anodic oxides on Indium Arsenide. Little investigation of suitable insulators on InAs has been done since the availability of quality material has been possible only very recently. However, InAs is still very expensive, and continuation of the work begun on InAs was not possible for that reason. Considering the methods of insulator formation available on campus, it was decided instead to investigate anodic oxides formed on Indium Phosphide, a very similar material. While anodic oxides on InP have been reported by many researchers, controversy still exists concerning which processes can consistently produce acceptable gate insulators. Research goals can then be stated:

1) Use anodic process to consistently produce acceptable gate insulator on InP.
2) Construct MOS capacitors.
3) Analyze/compare to samples with deposited Silicon Dioxide.
4) Analyze/compare to previously published work.

EXPERIMENTAL PROCEDURE

Appendix A contains a list of the fabrication steps of MOS capacitor structures using the anodic process on InP samples. Cleaning procedures for InP are given in Appendix B. The sequence of cross-sectional views of the process is given in Figure 2.

Insulators were deposited on InP samples by workers at the Opto-Electronics division of Honeywell Corporation in Richardson, Texas. A plasma-enhanced chemical vapor deposition of silicon dioxide was performed, yielding thicknesses of 480 and 1111 Å. Conditions of oxide deposition for these samples are given in Appendix C. From this step on, capacitors were formed from these two samples using the same steps as given in Appendix A.

After cleaning, an aluminum film is deposited on the samples by evaporation of aluminum under vacuum. Aluminum was deposited to a nominal thickness of 376 Å, which was expected to yield oxides 480 Å thick. This would allow direct comparison to the 480 Å sample produced at Honeywell.

The anodizing solution used was mixed in this way: 3 grams of tartaric acid were measured and dissolved in 100 ml of de-ionized water. To this solution was added 200 ml of propolene glycol, giving a total volume of 300 ml. This was expected

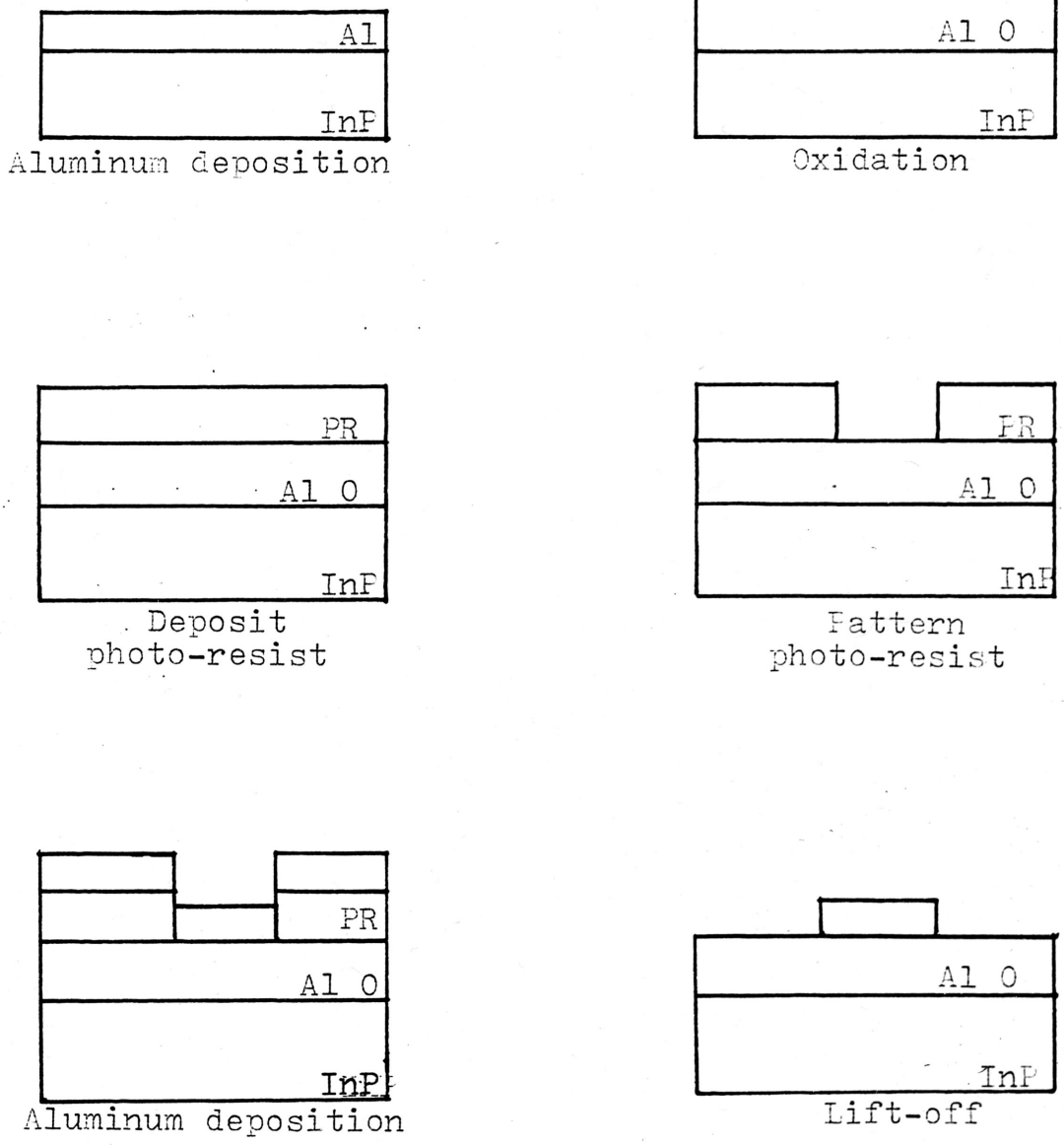

Figure 2. MOS Capacitor Fabrication.

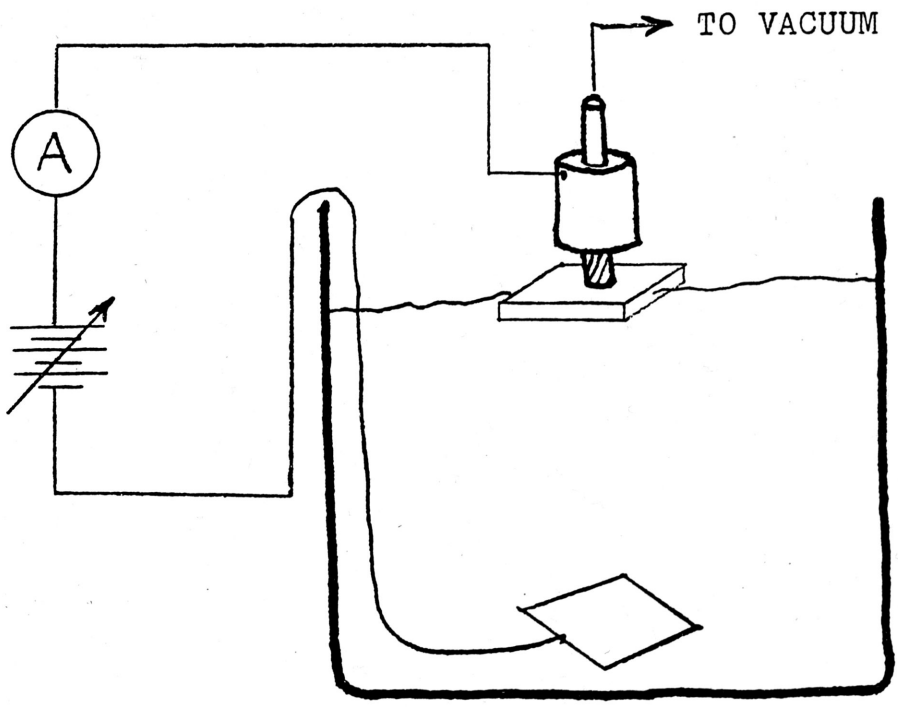

Figure 3. Anodization using vacuum chuck.

to give an acceptable value of solution pH, but this was not confirmed since no pH meter was available in the lab. This solution is the same as that used in [4].

Oxidation of the aluminum film was the least straightforward step in the fabrication. Three methods were considered and attempted:

1) Suspension of only the aluminized surface of the sample in the solution by using a vacuum chuck, as shown in Figure 3. In this way, the only current flow is that which causes the aluminum to oxidize.

2) Affixing the sample to the bottom of the anodizing beaker, making electrical contact to the back of the sample with a wire which is isolated from the solution by either an epoxy or a wax. This method also

ideally allowed the solution to contact only the aluminized surface.

3) Simply suspending the entire sample in the solution with an alligator clip. The non-aluminized back surface was isolated from the solution by coating it with black wax.

All these methods share the same goal – to pass a constant current density through the aluminum film, causing it to oxidize. As oxidation continues and the depth of the insulating aluminum oxide increases, the voltage applied to the sample must likewise be increased to maintain a constant current density. It was expected that the current would drop to zero regardless of voltage when the aluminum was completely oxidized.

After oxidation, the samples were subjected to the 'solvent' steps of the cleaning procedures to remove the viscous anodizing solution. Positive photo-resist was spun on the surface (5000 RPM for 30 seconds.) The resist was exposed and developed to form circular openings. The resist was soaked in chlorobenzene in preparation for later lift-off. A second aluminum deposition was performed, with film thicknesses anywhere from 190 Å to approximately 400 Å. The samples were then dipped in acetone and sonicated to remove the underlying photo-resist. Circular aluminum contacts were the result - forming MOS capacitors.

ANALYSIS OF MOS CAPACITORS

While exhaustive testing and characterization of the capacitors constructed was not possible, the capacitance *vs.* voltage (CV) measurements taken from all

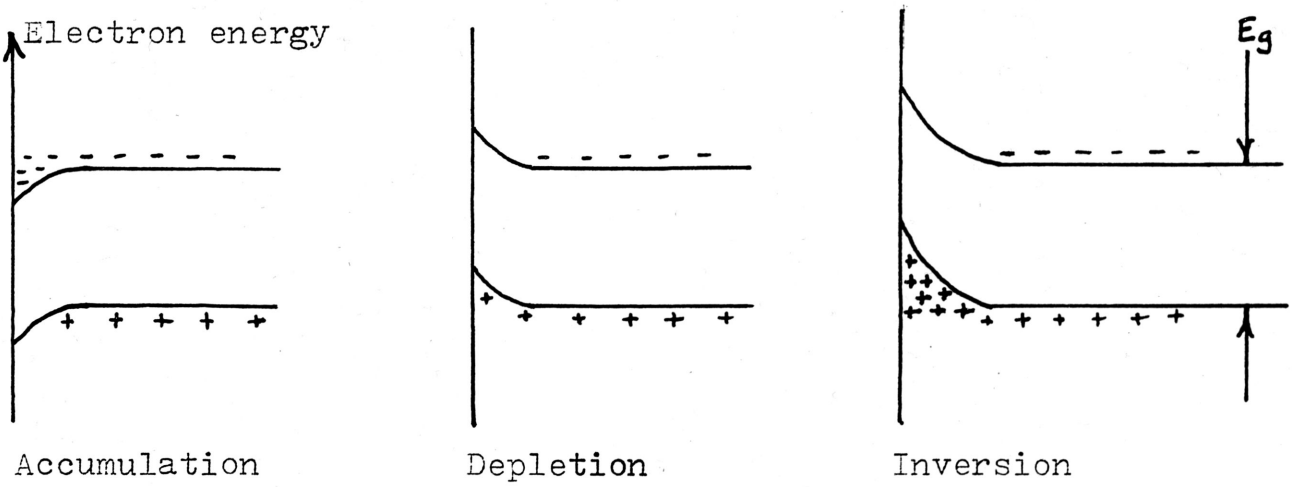

Figure 4. Energy band diagram at interface.

prepared samples were sufficient to show which of the oxidation methods holds more promise. This section outlines the physical mechanism responsible for the change in capacitance with changing gate voltage, and describes the test set-up for those measurements.

Energy Band Diagram at Dielectric Interface

The electron energy at the insulator/semiconductor interface can generally be in one of the three states shown in Figure 4, determined by the applied gate voltage V.[5] For an n-type substrate, the material is said to be in *accumulation* if an excess of conduction electrons gather at the interface area. This corresponds to the downwardly bent energy bands and a positive gate voltage as shown. As the gate voltage is made negative, electrons are forced out of the interface area, and a space-charge region is then said to exist. In this *depletion* state the region ideally

has no carriers and adds to the overall capacitance associated with the interface. If the gate voltage is made still more negative, *inversion* takes place and conduction in the channel is performed by holes rather than electrons. In summary, both the conductivity of the channel and the capacitance associated with the interface change with changing gate voltages.

Capacitances Associated with the MOS Structure

Three capacitances can be identified in the ideal MOS device.[6] The simple *geometrical capacitance*, C_i, is the capacitance of the structure if the semiconductor were replaced with a metal. In addition, the depletion of the space charge layer adjacent to the insulator interface contributes a capacitance. This effect is as differential capacitance and is defined by

$$C_{sc} = \frac{\partial Q_{sc}}{\partial V_s}$$

where C_{sc} is the *space charge differential capacitance* per unit area; Q_{sc} is the charge in the space charge region; and V_s is related to the applied gate voltage. The final capacitance is the *surface state capacitance* which is caused by the presence of charges at the insulator-semiconductor interface. It is also a differential capacitance and its definition is similar to that of the space charge capacitance. The total capacitance of the structure is then given by

$$\frac{1}{C} = \frac{1}{C_i} + \frac{1}{C_{ss} + C_{sc}}$$

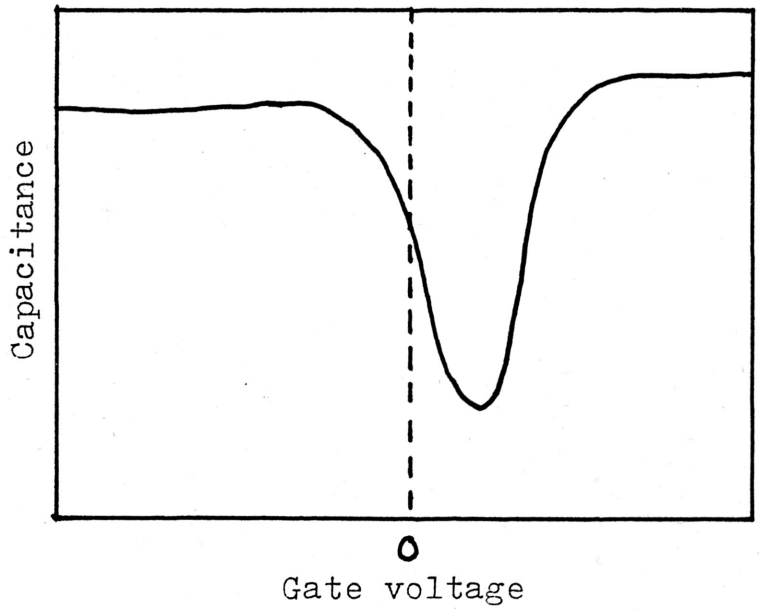

Figure 5. Ideal CV characteristic for n material.

It is clear that the maximum capacitance will occur for those values of gate voltage that cause the interface to be either in accumulation or inversion.

An ideal variation of capacitance with voltage can be derived if the following idealizations are in effect:[7] a) The insulator is free of charge; b) No surface charges exist; c) The work function difference between the metal and semiconductor is zero. In that case, the CV curve of Figure 5 is expected.

In general, the variation of capacitance with applied voltage can be exploited to determine many of the important characteristics of the MOS interface. Among these are conductivity type, impurity concentration, interface state density, and carrier mobilities. If no change in capacitance is observed, it is usually assumed that the density of surface states at the interface is so high that any variation in the space charge distribution is negated. In this case the interface is useless for the fabrication of MOS transistors.

Measurement of the CV characteristic is straightforward. A Princeton Applied Research model 410 CV plotter was used. It automatically performs all functions, including output to an X-Y plotter. Capacitance is measured at 1 MHz.

EXPERIMENTAL RESULTS

As mentioned earlier, an anodic process was used to form the gate insulator. Three different methods were used to suspend the samples in the oxidizing solution.

The vacuum chuck method was performed first. Current densities of .1 and .2 mA/cm^2 were used. In all cases, the expected voltage *vs.* time characteristic was followed for several minutes, but soon the anodizing current remained constant for any given applied voltage. (It was expected that the current should abruptly stop when all the aluminum was consumed in the oxidation process.) In addition, oxidation was not regular across the surface of the sample – some areas seemed to oxidize completely while others remained metallic. Most oxidations also produced bubbles that collected on the inverted aluminum surface, thus inhibiting oxidation. No capacitors produced by this method exhibited any change in capacitance in the CV test.

Aluminized samples were then cemented (aluminum side up) to the bottom of the beaker, with a wire making contact to the bottom side. Similar current densities were maintained in these attempts. While the problem with bubbles was lessened, oxidation was still non-uniform on the aluminum surface. As these local areas of oxidation grew in size, the current again became constant rather that decreasing

with a constant applied voltage. Additional problems with this technique include probable contamination of the anodizing solution by the epoxy, and poor contact between the sample and wire. This method again produced capacitors that did not exhibit any change in capacitance during the CV test.

Prepared samples were then suspended in the solution by simply coating the rear (non-aluminized) surface with black wax, then attaching an alligator clip to the sample and allowing it to dangle into the beaker. Oxidation again proceeded in patches, and again the current did not behave as expected. The resulting capacitors, however, were the only ones to give meaningful CV data.

Interpretation of results

CV curves for the capacitors which did exhibit changes in capacitance with applied voltage appear in Appendix D. Each sample contains dozens of individual MOS capacitors – the data presented is typical.

Referring to the ideal CV curve of Figure 5, the data shown is reasonable. The rise in capacitance for negative voltages (corresponding to the inversion state) is not seen; this is expected because the mobility of holes at the interface is very small compared to that of electrons. For this reason, the space-charge capacitance in inversion will not be measurable for a 1 MHz excitation.

The most puzzling aspect of the experimental data is the drop in capacitance as the voltage continues to rise. This is not expected, and is difficult to explain. It is suspected that the conductance of the insulator is likewise dependent on voltage, causing this effect.

Capacitors fabricated from the samples processed at Honeywell were tested. These two samples exhibited no change in capacitance over a wide range of applied voltages. It is expected that the surface state density in these structures was very high, inhibiting modulation of carrier densities at the interface.

SUMMARY AND CONCLUSIONS

If the potential advantages that some compound semiconductors offer with respect to speed of operation are to be realized, insulators must be formed that preserve the high electron mobility in those materials. Several methods exist for production of insulators on semiconductor substrates, including deposition, native oxidation, and anodic oxidation of deposited metals. This effort was an attempt to produce consistently acceptable oxides on Indium Phosphide samples using an anodic technique.

Experimental results are given for MOS capacitors constructed from the resulting oxides. The data given is from the Capacitance-Voltage method of interface characterization. Most attempts at oxidation failed to produce capacitors that showed any change in capacitance with applied voltage, indicating an oxide/semiconductor interface that is unacceptable for use in constructing MOS transistors. Those samples that did exhibit changes in capacitance gave data that is close to that typical of the ideal interface.

Many reasons can be suggested for the failure of most attempts to produce acceptable oxides. Cleanliness can be suspected, since most of the processing was

done at a time when the solid state lab was undergoing renovation and was 'unclean.' As mentioned, the pH of the anodizing solution could not be experimentally verified. Accurately maintaining the very small current densities on very small samples was difficult with the power supply used. The overiding problem, however, was the non-uniform oxidation observed on every oxidation attempt. This could have been due to a surface (either the InP substrate or the deposited aluminum) that was not sufficiently smooth, thereby causing preferred sights where oxidation proceeds rapidly. Poor electrical contact at the sample is also suspected.

Even though one attempt did give reasonable CV characteristics, the reduction of capacitance for high positive voltages is an undesired effect. The erratic variation of the oxide conductance *vs.* voltage is assumed to be the cause. In general, the goal of consistently producing an oxide/semiconductor interface suitable for use in the fabrication of an InP MOS transistor was not met.

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APPENDIX A

MOS CAPACITOR FABRICATION STEPS

1) Sample preparation/cleaning procedures

2) 390 Å layer of aluminum deposited by evaporation

3) Anneal, 20 minutes at 250 °C in forming gas

4) Anodization in aqueous solution

5) Deposit photo-resist

6) Expose/develop photo-resist

7) Aluminum evaporation

8) Remove photo-resist to form gate contacts

APPENDIX B

INDIUM PHOSPHIDE CLEANING PROCEDURE

All steps at room temperature unless otherwise stated.

Solvent Steps

1) Chlorothene, 5 minutes.

2) Acetone, 5 minutes, 70 °C.

3) Methanol, 5 minutes, 70 °C.

Acid Steps

4) DI water, 4 minutes.

5) Nitric acid, 15 minutes.

6) DI water, 2 minutes.

7) Buffered hydroflouric acid (oxide etch), 5 minutes.

8) DI water, 10 minutes.

9) Blow dry with nitrogen.

APPENDIX C

PLASMA ENHANCED CVD SPECIFICATIONS

Sample #1:

Thickness: 480 Å

Time: 2.5 minutes

Refractive index: 1.47-1.48

Stress: $2.12*10^9$ compressive

Sample #2:

Thickness: 1111 Å

Time: 5.3 minutes

Refractive index: 1.47-1.48

Stress: $5.91*10^8$ compressive

The following apply to both samples.

Pressure: 800 μtorr

RF power: 20 Watts

Temperature: 250 °C

Gas flow rates:

5 % Silane: 475 scc/minute

He: 1800 scc/minute

N_2O: 2025 scc/minute

APPENDIX D

C-V DATA FROM TYPICAL CAPACITOR