A DENSE PROGRAMMABLE READ ONLY MEMORY

by

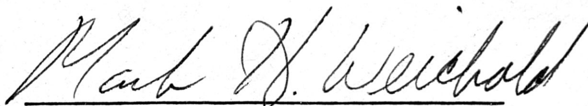
LAURA ELIZABETH MADLA

Electrical Engineering

Submitted in Partial Fulfillment of the Requirements of the University Undergraduate Fellows Program

1985-86

Approved by:



Mark Weichold

December 1986

ABSTRACT

A Dense Programmable

Read Only Memory. (April 1986)

Laura Elizabeth Madla, B.S., Texas A&M University

Faculty Advisor: Dr. Mark Weichold

The programmable read only memory (PROM) is a valuable piece of hardware in today's fast-growing microcomputer industry because of its large memory capacity and its speed. This project involves the production and testing of a high-density PROM cell which utilizes a vertical layering arrangement in an effort to decrease cell size. This cell contains a Schottky diode as a crosspoint device and a polysilicon resistor for programming. This PROM has a programming voltage of less than 40V at currents under 1mA.

ACKNOWLEDGMENTS

I would like to thank the staff of the Institute for Solid State Electronics for their help in completing this project. I would especially like to thank Robert Atkins, Vic Swenson, and Bill Gibler for all the time they spent showing me how to use the equipment and solving problems. This project would not have been possible if not for the help of my advisors, Dr. Mark Weichold and Dr. Ugur Cilingiroglu. Dr. Cilingiroglu is an excellent teacher and was invaluable to me in understanding the devices and their processing. Dr. Weichold is not only a technical advisor, but also a friend. I could not have completed this project without his encouragement, understanding, and support.

TABLE OF CONTENTS

Page

I. INTRODUCTION 1

A. Background 1

B. Description 1

C. Limitations 2

II. PROM CELL DESIGNS 3

A. Device Components 3

B. Device Designs 4

III. DEVICE FABRICATION 6

A. Overview 6

B. Fabrication Process 6

C. Device Specifications 7

IV. PROBLEMS ENCOUNTERED 9

A. Piranha Cleaning 9

B. Photoresist Process
Small Geometry Definition 9

C. Si_3N_4 Deposition 9

D. Contact Windows 9

V. RESULTS 10

A. Processing Results 10

B. Test Results 10

VI. CONCLUSIONS 17

TABLE OF CONTENTS (Continued)

	Page
REFERENCES	18
APPENDIX A	19
APPENDIX B	23
VITA	28

LIST OF FIGURES

Figure Page

1. Schottky Diode/Polysilicon Resistor 4
2. Schottky Diode/p-n Junction Shorting 5
3. Schottky Diode/Oxide Shorting 5
4. Mask Level 1 11
5. Mask Level 2 11
6. Mask Level 3 12
7. Mask Level 4 12
8. Programming Voltage Distribution – 5 μm square 13
9. Programming Voltage Distribution – 15 μm square 13
10. Programming Voltage Distribution – 50 μm square 14
11. Programming Voltage Distribution – 100 μm square 14
12. I-V Curve – 5 μm square 15
13. I-V Curve – 15 μm square 15
14. I-V Curve – 50 μm square 16
15. I-V Curve – 100 μm square 16

I. INTRODUCTION

A. Background

With the advent of large scale integration (LSI), digital system hardware has replaced software[1]. One of the most valuable pieces of LSI hardware is the programmable read only memory (PROM) which can be customized to the user's specifications. PROMs are in common use today as storage for microprograms because of their speed and large memory capacity[2].

Designers of PROM cells look for ways in which to decrease both the size of the cell and the voltage level required to program the cell. The goal is for the programming voltage to be greater than the system power supply, yet small anough to be generated by MOS (metal-oxide-semiconductor) devices on the chip itself.

B. Description

A primary goal of this project is to develop a PROM cell small in size, by using a vertical layering arrangement, with a small programming current.

Ugur Cilingiroglu, a former Visiting Assistant Professor in Texas A&M University's Electrical Engineering Department, designed several PROM cells and selected the three most likely to work. This project set out to implement one of three PROM cell designs into a memory array to be tested and evaluated. Once all three cells have been made, the test results will be compared to determine the best cell of the three. An array of cells will then be made and tested, and a final evaluation will determine the reliability and feasibility of the design. The cell designs and project proceedings will be described in later sections.

Journal model is *IEEE Transactions on Electron Devices.*

C. Limitations

Only one cell design has been fabricated to date. This report includes a description of three cell designs and specifications on device fabrication for one of these designs.

II. PROM CELL DESIGNS

A. Device Components

A PROM cell consists of a programming device and a crosspoint device. The programming device can be either short-circuited or open-circuited to produce a '1' bit or a '0' bit. The crosspoint device conducts current to the programming device so that the value of that bit may be read.

Common programming devices used in PROM cells include polysilicon fusing, p-n junction shorting and polysilicon shorting. **Polysilicon fusing** has been used in bipolar PROMs, but consumes a large area and large programming current. This scheme is primarily applied in redundancy circuitry. **Junction-shorting** has only been applied to bipolar devices. The programming and crosspoint devices are vertically connected, utilizing the n^+ and p^+ layers of a TTL transistor for programming and p-n-p transistor as the crosspoint device. The p^+ diffusion layer is common to both devices, with the transistor also utilizing the n epitaxial layer and the p^- substrate[2]. This vertical structure saves area, but the bipolar transistor is a large device. Programming currents for this scheme are also large. **Polysilicon shorting** has been used in MOS PROMs. Programming current for this scheme is relatively small so that MOSFETs can be used to change the polysilicon from a high resistive state (open circuit) to a low resistive state (short circuit)[1]. The size of this device is large.

A MOS or bipolar transistor is usually used as the crosspoint device and offers increased transition speed, but the cell size for these devices is large. A rectifying junction, either p-n or Schottky, as a crosspoint device consumes the smallest area, with speed compensation provided by regenerative sense amplifiers. Although

never used in PROM cells, a p-n junction device has been utilized as a crosspoint device in a $4F^2$ area (smallest possible area for the technology used) mask ROM cell[3].

A very small PROM cell should result from using a rectifying junction with a vertically placed programming device. Possible programming schemes include junction shorting, polysilicon shorting or oxide shorting. After analyzing possible layering arrangements combining either a Schottky diode or p-n junction diode as the crosspoint device and either junction, polysilicon, or oxide shorting as the programming device, three designs were chosen for processing and evaluation. Factors examined in selection of the three configurations to be tested included the number of polysilicon layers, NMOS process compatibility, the presence of novel features and the number of extra masks required. Also considered were the numbers of extra polysilicon depositions and polysilicon implants.

B. Device Designs

The first configuration utilizes a polysilicon resistor as the programming device and a Schottky diode as the crosspoint device. This requires a two-layer polysilicon structure, as shown in Figure 1.

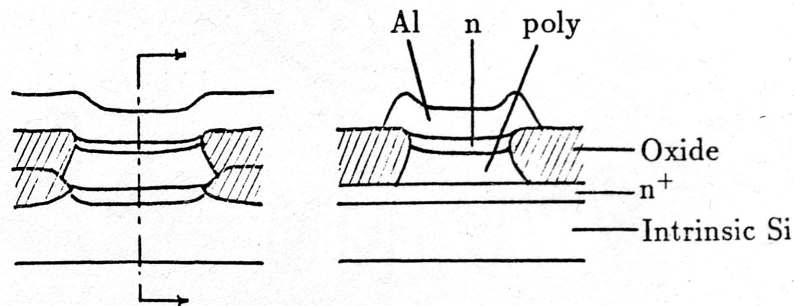


Fig. 1 Schottky Diode/Polysilicon Resistor

For the second design, A Schottky diode is again used as the crosspoint device, with p-n junction shorting for the programming scheme. As seen in Figure 2 below, only one polysilicon layer is used with a single monocrystalline diffusion.

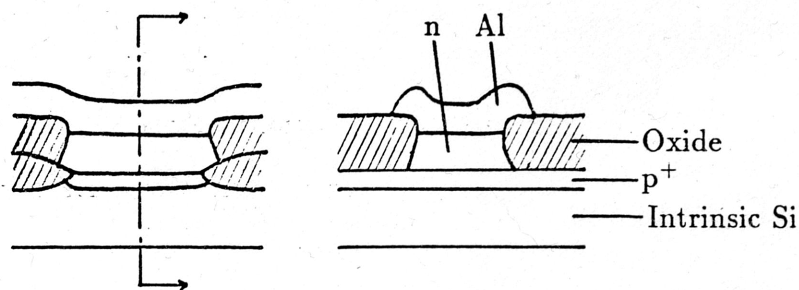


Fig. 2 Schottky Diode/p-n Junction Shorting

Oxide shorting will be used as the programming device in the third configuration along with the Schottky diode at crosspoint. This requires one polysilicon layer for one substrate interconnection diffusion. See Figure 3.

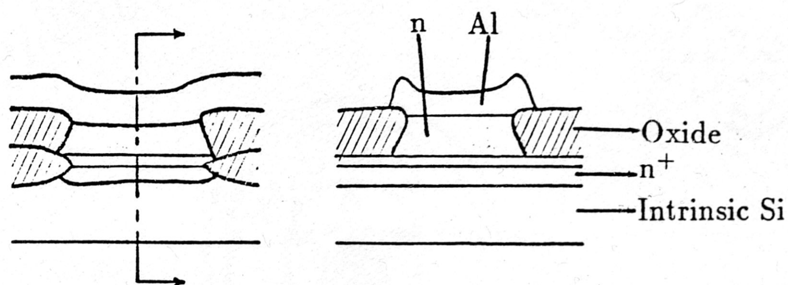


Fig. 3 Schottky Diode/Oxide Shorting

III. DEVICE FABRICATION

A. Overview

This project consists of the processing and evaluation of one cell design. This includes designing and making the masks, and doing the processing of each cell. Once the cells have been made, they will be tested to determine the characteristics of each device. The cell chosen uses polysilicon shorting as the programming device and is the most likely of the three original designs to be successful.

B. Fabrication Process

The design and preparation of the masks begins with a sketch of the masks needed. The mask acts as a photographic negative and is used to define the components of the semiconductor device. Once the mask design is complete, the mask layouts are entered into the computer and a formal mask layout is generated. The computer program and plots are located in Appendix A. This design is then photographically reduced and reproduced to create the final photolithographic mask. This process requires four masks.

Once the masks are finished, the processing can begin. The actual process is described completely in Appendix B. The first step is substrate preparation. Because of the small sizes of the components–minimum geometry of 5 microns–the cleanliness of the substrate during manufacturing is directly related to the reliability of the circuits produced. The use of clean rooms to prevent contamination by particles in the air and the use of highly refined "electronic grade" chemicals are important in achieving acceptable circuits. The monocrystalline silicon substrate is also subject to a rigorous chemical cleansing process in order to create a reproducible

and stable surface.

After the substrate has been prepared, a silicon dioxide layer is grown by oxidation of the silicon substrate. A layer of photoresist is then spun onto the oxide, and the wafer is exposed to ultra-violet light through the first mask. After developing, the exposed oxide is etched away, leaving patches of silicon exposed. This exposed silicon is then doped by ion implantation. The doped substrate layer will be the lower contact of the PROM cell.

The polysilicon is then deposited, followed by layers of silicon nitride and silicon dioxide. Mask level two is used to pattern the oxide, which acts as a mask for the nitride. The nitride is then etched away, leaving exposed polysilicon. The masking oxide is removed and the polysilicon is oxidized to provide insulation between memory cells. The masking nitride layer is etched away, leaving the polysilicon resistor islands among the oxide.

The polysilicon islands are doped by ion implant to form one end of the Schottky diode. After annealing, a third mask level is used to open contact windows at the polysilicon and n^+ contact areas. Aluminum is then deposited on the wafers and the fourth and final mask level used to define the Aluminum interconnections.

The testing and evaluation of the cells will consist of probing cells on each wafer and applying a programming voltage across each cell. By varying current and voltage, programming characteristics for each cell will be experimentally determined.

C. Device Specifications

The minimum geometry used for these devices is 5 μm. There are four cells on each die, with cell dimensions of 5 μm, 15 μm, 50 μm, and 100 μm square. There

are four mask levels for this device: n^+ diffusion, polysilicon masking, contact window definition, and contact definition.

The undoped polysilicon resistor is designed to be .4 μm thick so that a transition voltage of less than 10 volts will be needed to change the resistivity of the polysilicon to a low resistive state. The corresponding transistion current should be less than 10 mA[1]. The final polysilicon thickness was determined by calculating the amount of polysilicon necessary for the Schottky diode implant (0.15 μm) and the amount of polysilicon affected by out-diffusion of the n^+ implant for the diffusion island (0.1 μm). The total polysilicon layer is 0.65 μm thick. For our purposes, approximate polysilicon thicknesses of 0.6 μm, 0.65 μm, and 0.7 μm were used.

There are two n-type ion implants. The first is for the n^+ diffusion islands which will be the lower contact of the device. Arsenic is implanted at an energy of 90 keV with a dose of 2×10^4 cm^-2. The drive-in is at 1100°C in a 5/5/150 dry/wet/dry oxidation cycle.

The second implant forms an n-type region in the polysilicon for the Schottky diode. Arsenic is implnated at 80 keV with a dose of 5.7×10^{12} cm^-2. The drive-in is at 950°C in a 5/5/50 oxidation.

The field oxide is a standard 5000Å thick, and the aluminum contact layer 7-10Å thick. The Si_3N_4 layer used for masking the polysilicon is approximately 2000Å thick, with 1500Å of oxide used to pattern the nitride.

IV. PROBLEMS ENCOUNTERED

A. Piranha Cleaning

The initial substate cleaning resulted in a murky film on the wafers. This was remedied by introducing a wafer scrub in the first di water rinse. This helped a great deal. The problem was eliminated by using a warm (90°C) di water rinse immediately following the Piranha.

B. Photoresist Process
Small Geometry Definition

The 5 μm lines on the first mask level were lifting off during developing. Adding a 1 minute hard bake (135°C) between exposure and developing solved this problem.

C. Si_3N_4 Deposition

The initial test runs indicated that the film deposited was a mixture of SiO_2 and Si_3N_4. Purging gas lines and varying the flow rate did not help. By changin the Si_3N_4 target and using high-purity N_2 gas, a better Si_3N_4 film was obtained. Although this film is not pure Si_3N_4, it will etch off with the wet etch and will serve well as a mask.

D. Contact Windows

Because of the small geometries on this level, the mask was difficult to make. The geometries on the mask are too large, and if used, will short out the device, making it useless. The negative photoresist was overexposed to produce smaller geometries, with fair results. The smaller geometries sometimes disappeared and the 50 μm geometries were very difficult to align.

V. RESULTS

A. Processing Results

Field oxide growth. Using the ellipsometer for characterization, the oxide layer grown was between 4300Å and 5200Å. Figure 4 shows the results of the first mask level, with the 4 diffusion islands.

Polysilicon thickness. The approximate thickness of the polysilicon layer is 6500Å, as determined by the groove and stain method. The polysilicon layer is uneven, however, and varies considerably across the wafer.

Silicon nitride deposition. The nitride layer used for masking was not pure. The index of refraction was determined to be between 1.85 and 1.97 with a thickness of 1850Å to 2100Å. These results were obtained using the ellipsometer, and the nitride was satisfactory for masking purposes. Figure 5 shows the second mask level with the nitride islands used to mask the polysilicon during oxidation. Figure 6 shows the third mask level contact windows, and Figure 7 shows the final mask level – Aluminum contact pads.

B. Test Results

The devices were tested by applying voltages up to 80V in an effort to program the cells. Some devices programmed at voltages ranging from 1V to 53V. No cells programmed between 54V and 80V. 90% of all the working devices programmed with a voltage of less than 40V. The programming current could not be determined, but is less than 1mA. A breakdown of programming voltages for the devices by

device size is shown in Figures 8 – 11.

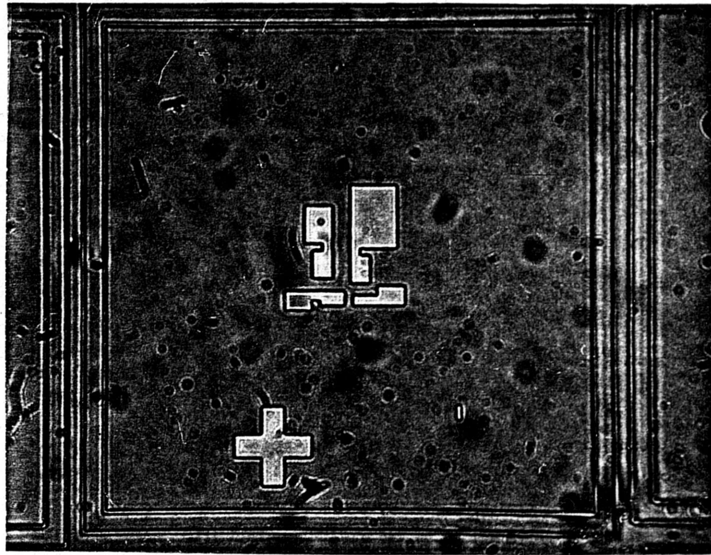


Fig. 4 Mask Level 1

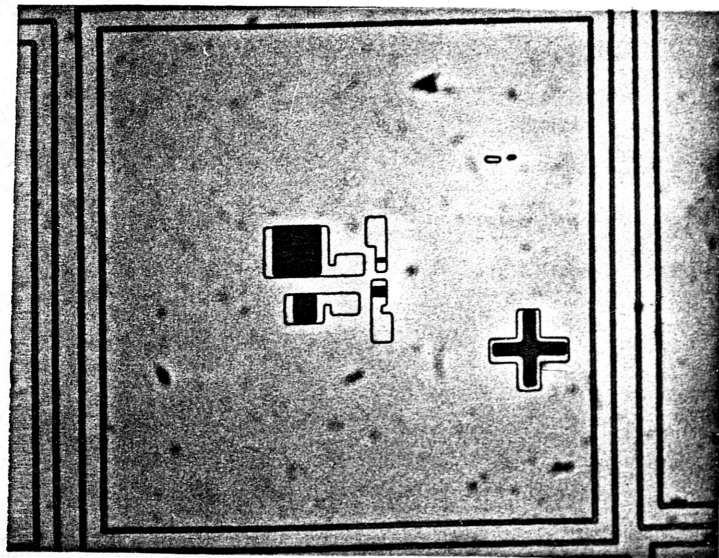


Fig. 5 Mask Level 2

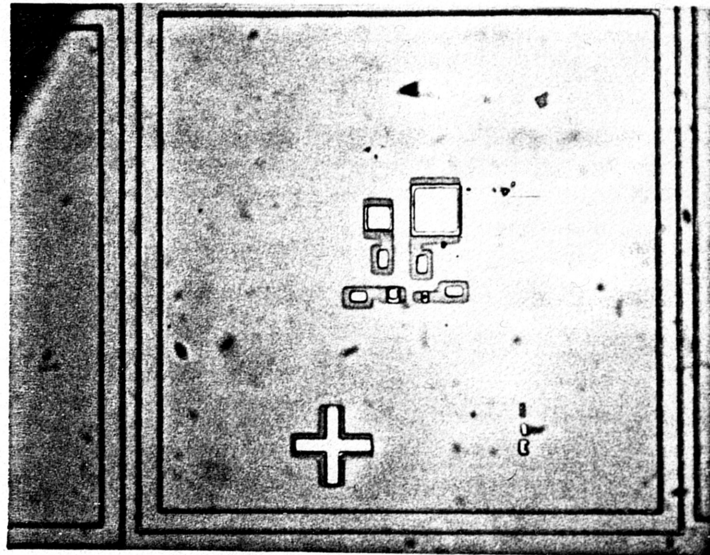


Fig. 6 Mask Level 3

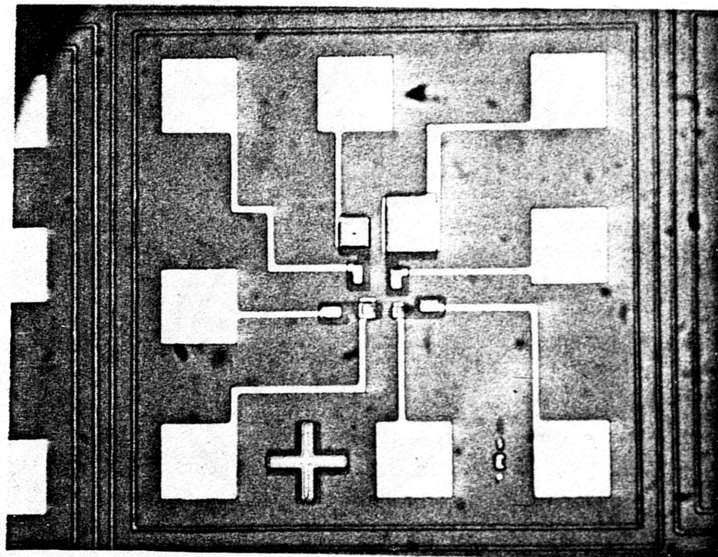


Fig. 7 Mask Level 4

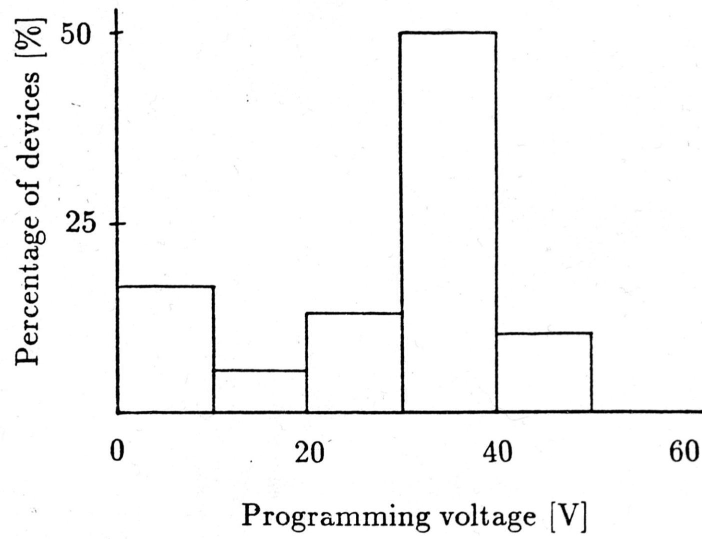


Fig. 8 Programming voltage distribution – 5 μm square

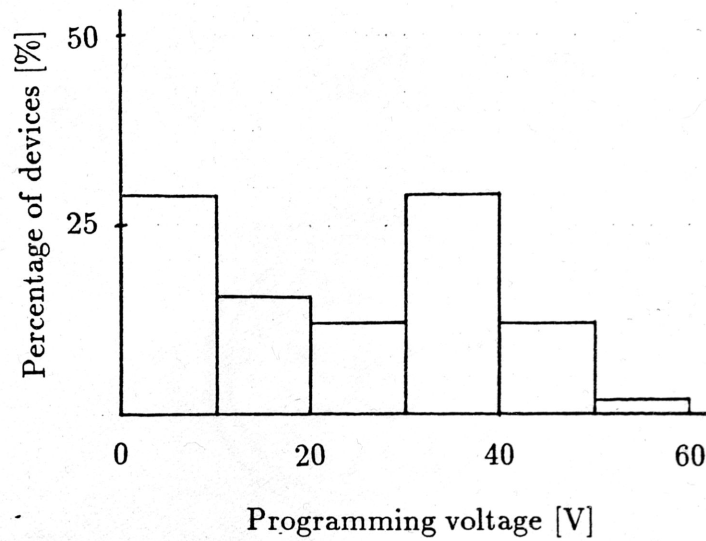


Fig. 9 Programming voltage distribution – 15 μm square

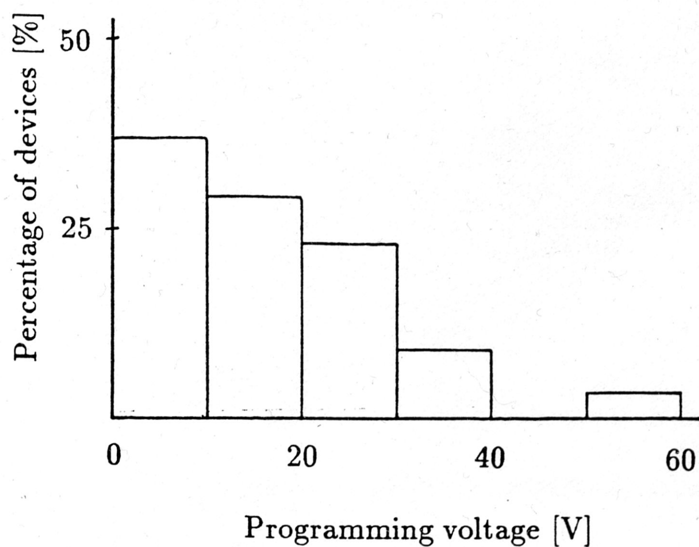


Fig. 10 Programming voltage distribution – 50 μm square

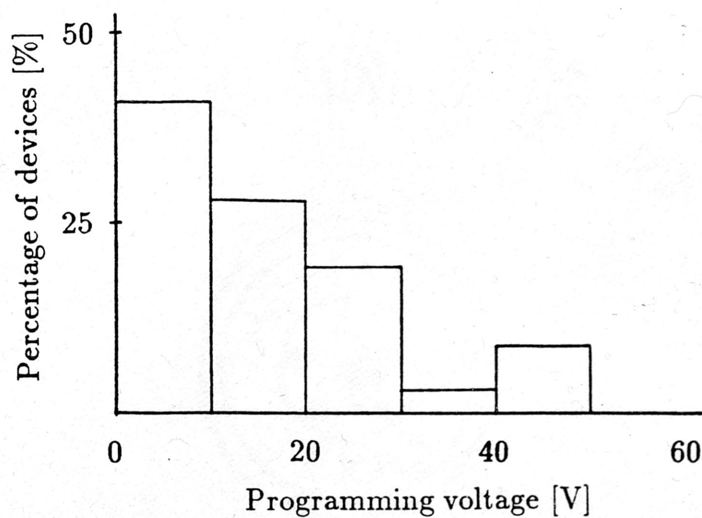


Fig. 11 Programming voltage distribution – 100 μm square

The I-V characteristics for all the devices were very similar. In the figures

below are photographs showing the I-V curves for each device size.

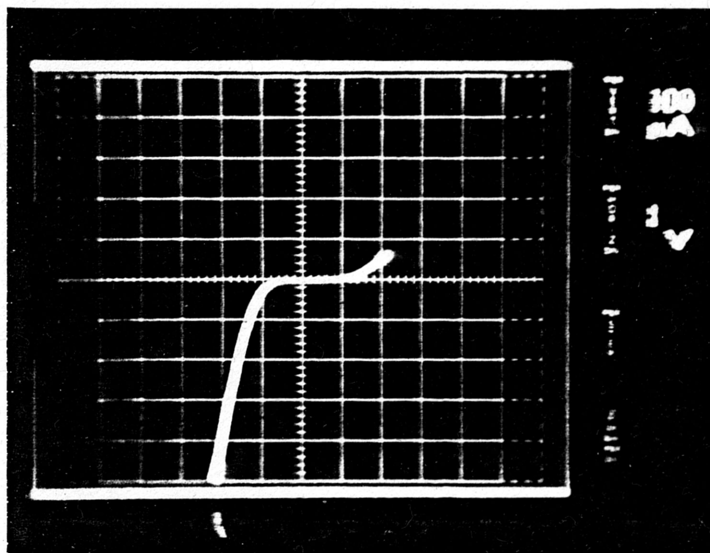


Fig. 12 I-V Curve – 5 μm square

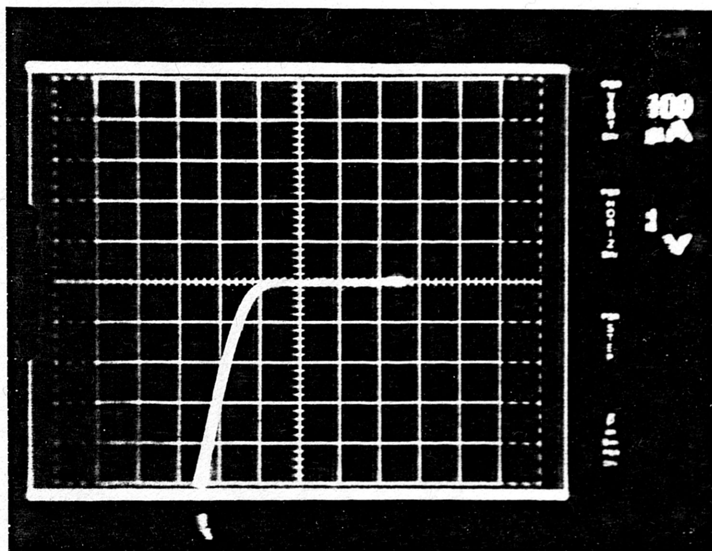


Fig. 13 I-V Curve – 15 μm square

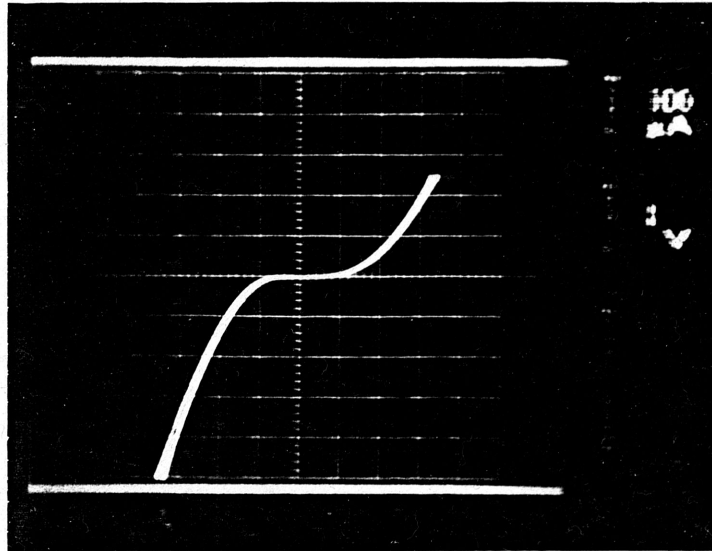


Fig. 14 I-V Curve – 50 μm square

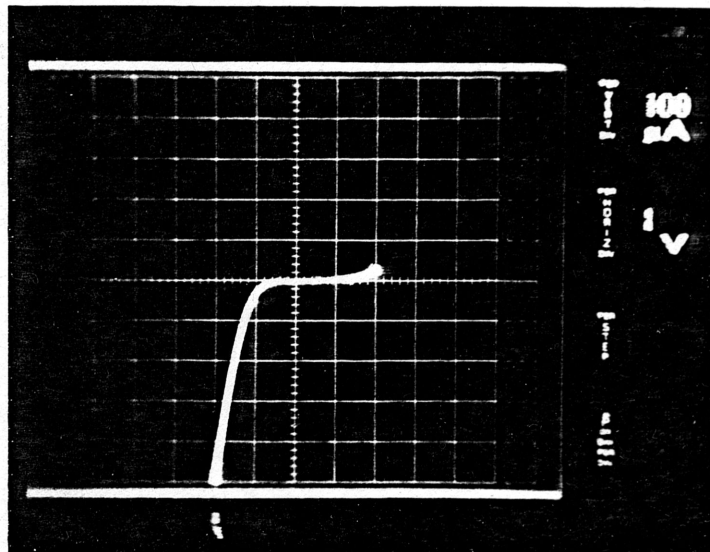


Fig. 15 I-V Curve – 100 μm square

VI. CONCLUSIONS

Although the programming voltages are higher than expected, the vertical layering scheme is a promising design for PROMs. There are many possibilities for improvement of the process and the specifications, and more testing must be done to determine what can be done to improve the devices. There is insufficient data now to make an accurate prediction of the feasibility of this design.

Areas that should be investigated include a redesign of the masks to improve alignment problems, a more even polysilicon layer, accurate measurements of layer thicknesses and characteristics, and the possibility of etching away the polysilicon instead of oxidizing to create the polysilicon islands.

REFERENCES

[1] M. Tanimoto, J. Murota, M. Wada, T. Qatanabe, K Miura, and N, Ieda, "A Novel 14 V Programmable 4 kbit MOS PROM Using a Poly-Si Resistor Applicable to On-Chip Programmable Devices," *IEEE Journal of Solid-State Circuits*, vol. SC-17, pp. 62-67, February 1982.

[2] T. Fukushima, K. Ueno, Y Matsuzaki, and K. Tanaka, "A 40 ns 64 kbit Junction-Shorting PROM," *IEEE Journal of Solid-State Circuits*, vol. SC-19, pp. 187-194, April 1984.

[3] N. Sato, T. Nawata, and K. Wada, "A New Cell for High Capacity Mask ROM by the Double Locos Technique," *IEDM Technical Digest*, pp. 581-584, 1983.

[4] Larry Metzger, "A 16K CMOS PROM with Polysilicon Fusible Links," *IEEE Journal of Solid-State Circuits*, vol. SC-18, pp. 562-567, October 1983.

[5] M. Tanimoto, J. Murota, Y.Ohmori, and N. Ieda, "A Novel MOS PROM Using a Highly Resistive Poly-Si Resistor," *IEEE Transactions on Electron Devices*, vol. ED-27, pp. 517-520, March 1980.

APPENDIX A

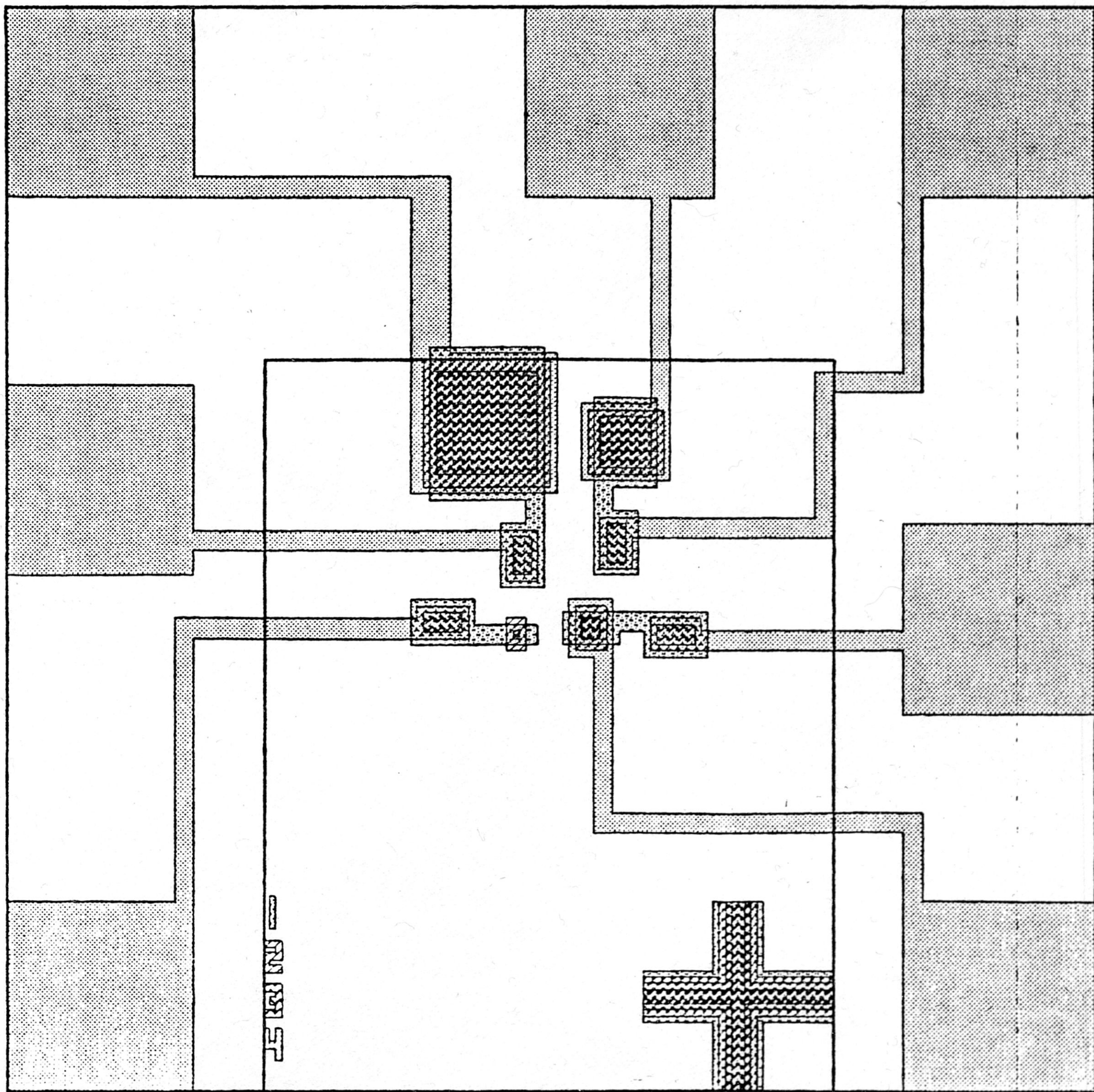
MASK LAYOUT
PROGRAM AND PLOT

```
(CONTACT WINDOWS FOR SCHOTTKY);
(N++ DIFFUSION LINES);
DS, 1;
L,ND;
 P  39000,42500 49000,42500 49000,44000 44000,44000 44000,46000 39000,46000;
 P  51000,42500 55500,42500 55500,43500 57500,43500 57500,41500 62500,41500
    62500,45000 51000,45000;
 P  49500,47000 49500,66000 40500,66000 40500,54000 48000,54000 48000,52000
    46000,52000 46000,47000;
 P  53500,48000 57000,48000 57000,53000 55000,53000 55000,55000 58500,55000
    58500,62000 53500,62000;
(ALIGNMENT MARK);
 P  63000,22000 67000,22000 67000,16500 72500,16500 72500,12500 67000,12500
    67000,7000 63000,7000 63000,12500 57500,12500 57500,16500 63000,16500;
(MASK NUMBER);
 P  28500,20000 28500,22500 28000,22500 28000,20000;
(SCRIBE LINES);
 B  96000,100,50000,2000;
 B  100,96000,2000,50000;
 B  96000,100,50000,98000;
 B  100,96000,98000,50000;
 B  104000,100,50000,-2000;
 B  100,104000,-2000,50000;
 B  104000,100,50000,104000;
 B  100,104000,104000,50000;
DF;
(POLY RESISTOR ISLANDS);
DS,2;
L,NP;
 B  10000,10000,45000,60000;
 B  6000,5000,56000,58500;
 B  2500,3500,53250,43750;
 B  1500,2500,47250,43250;
(ALIGNMENT MARK);
 P  63500,22000 66500,22000 66500,16000 72500,16000 72500,13000 66500,13000
    66500,7000 63500,7000 63500,13000 57500,13000 57500,16000 63500,16000;
(MASK NUMBER 2);
 P  29000,19000 29000,17500 28000,17500 28000,17000 29000,17000 29000,16500
    27500,16500 27500,18000 28500,18000 28500,18500 27500,18500 27500,19000;
```

```
DF;
(CONTACT WINDOWS);
DS,4;
L,NI;
(SCHOTTKY WINDOWS);
 B   8000,8000,45000,60000;
 B   4000,4000,56000,58500;
 B   1500,1500,53250,43750;
 B   500,500,47250,43250;
(N+ WINDOWS);
 B   3000,1500,41500,44250;
 B   1500,3000,47750,49500;
 B   1500,3000,55250,50500;
 B   3000,1500,60000,43250;
(ALIGNMENT MARK);
 P   64000,22000 66000,22000 66000,15500 72500,15500 72500,13500 66000,13500
     66000,7000 64000,7000 64000,13500 57500,13500 57500,15500 64000,15500;
(MASK NUMBER 3);
 P   29000,15500 29000,13000 27500,13000 27500,13500 28500,13500 28500,14000
     28000,14000 28000,14500 28500,14500 28500,15000 27500,15000 27500,15500;
(SCRIBE LINE);
 B   96000,100,50000,2000;
 B   100,96000,2000,50000;
 B   96000,100,50000,98000;
 B   100,96000,98000,50000;
 B   104000,100,50000,-2000;
 B   100,104000,-2000,50000;
 B   104000,100,50000,104000;
 B   100,104000,104000,50000; DF;
(ALUMINUM CONTACTS);
DS,5;
L,NM;
 P   7000,78000 7000,93000 22000,93000 22000,79500 42000,79500 42000,65500
     50500,65500 50500,54500 39000,54500 39000,78000;
 P   7000,63000 22000,63000 22000,51500 49000,51500 49000,47500 46500,47500
     46500,50000 22000,50000 22000,48000 7000,48000;
 P   20500,44500 39500,44500 39500,45500 43500,45500 43500,43000 22000,43000
     22000,7000 7000,7000 7000,22000 20500,22000;
(MASK NUMBER 4);
 P   29000,12000 29000,9500 28500,9500 28500,10500 27500,10500 27500,12000
     28000,12000 28000,11000 28500,11000 28500,12000;
(ALIGNMENT MARK);
 P   64500,7000 65500,7000 65500,14000 72500,14000 72500,15000 65500,15000
```

```
   65500,22000 64500,22000 64500,15000 57500,15000 57500,14000 64500,14000;
P  78000,7000 78000,27500 53500,27500 53500,41500 51500,41500 51500,46000
   55000,46000 55000,29000 79500,29000 79500,22000 93000,22000 93000,7000;
P  78000,42000 58000,42000 58000,44500 62000,44500 62000,43500 78000,43500
   78000,52000 93000,52000 93000,37000 78000,37000;
P  72500,51000 56500,51000 56500,48500 54000,48500 54000,52500 71000,52500
   71000,64000 78000,64000 78000,93000 93000,93000 93000,78000 79500,78000
   79400,62500 72500,62500;
P  59500,55500 52500,55500 52500,61500 58000,61500 58000,78000 48000,78000
   48000,93000 63000,93000 63000,78000 59500,78000;
DF;
DS,6;
C 1 T 0 0;
C 2 T 0 0;
C 4 T 0 0;
C 5 T 0 0;
DF;
C 6 T 0 0;
E;
```

Plot of Mask Layout:



APPENDIX B

PROCESS FLOW

1. Label wafers
2. Piranha clean – This self-heating mixture has a 30 minute lifetime. Add 70 parts 30% sulfuric acid; then add 30 parts unstabilized hydrogen peroxide.
   a. Piranha – 10 min.
   b. di water rinse – 5 min.
   c. buffered oxide etch – 3 sec.
   d. di water rinse – 5 min.
   e. di water rinse – 10 min.
   f. blow dry with N_2
   g. inspect visually
   h. dry @ 135° – 15 min.
3. Field oxidation – 5000Å
   a. adjust furnace to 1100°C
   b. start N_2 flow
   c. pre-heat di water for wet cycle
   d. load wafers on boat
   e. blow with N_2
   f. inspect visually
   g. place wafers in mouth of furnace – 10 min.
   h. slow push wafers to middle of furnace – 5 min.
   i. start oxygen – 5 min. (dry oxidation)
   j. start water – 60 min. (wet oxidation)
   k. stop water – 5 min. (dry oxidation)
   l. stop oxygen
   m. slow pull wafers to mouth of furnace – 5 min.
   n. leave wafers in mouth – 10 min.
   o. unload wafers
   p. inspect and note problems
4. Piranha clean – see step 2
5. PR-1 – photoresist, mask level 1, positive PR
   a. dehydration bake @ 135°
   b. cool to room temperature
   c. place wafer on chuck
   d. blow with N_2
   e. drop PR, check for air bubbles
   f. spin @ 5000 rpm – 30 sec.
   g. soft bake @ 65° – 30 min.
   h. expose – 93.5 sec.
   i. develop – 60 sec.

j. rinse in di water – 60 sec.
k. blow dry with N_2
l. inspect under microscope
m. hard bake @ 135°
n. inspect
NOTE: Smaller geometries etched off when developed. Procedure modified: added a 1 min. hard bake between exposure and developing.

6. Oxide etch – 5000Å
   a. blow with N_2
   b. buffered oxide etch – 9-12 min.
   c. rinse in di water
   d. blow dry with N_2
   e. inspect under microscope

7. n^+ implant – 2×10^4 cm^{-2}, 90 keV

8. PR strip
   a. heat nophenol to 95°
   b. place wafers in boat
   c. submerge in solution – 15 min.
   d. running di water rinse – 10 min.
   e. blow dry with N_2
   f. inspect

9. Piranha clean
   a. Piranha – 10 min.
   b. warm di water rinse – 2 min.
   c. di water rinse – 8 min.
   d. buffered oxide etch – 3 sec.
   e. running di water rinse – 10 min.
   f. blow dry with N_2
   g. inspect visually
   h. dry @ 135° – 15 min.

10. Drive in – 5/5/150, 1100°

11. Oxide etch – see step 6 – 1 min.

12. Piranha clean – see step 9

13. Polysilicon deposition – 6500Å

14. Si_3N_4 deposition – 2000Å– RF Sputterer
   a. vent system
   b. open bell jar
   c. insert wafer
   d. close bell jar
   e. open roughing valves
   f. turn on oil cooler, turbo
   g. wait for ion gauge controller reading 2 x 10^{-6}

h. turn on N_2, adjust flow to 40sccm
i. adjust vacuum to 11 microns
j. turn on water cooling valve
k. turn on RF sputtering system
l. ignite plasma
m. adjust output power to 400W, reflected power to zero
n. sputter for 20 min.
o. turn off RF sputtering system
p. turn off N_2
q. turn off water
r. turn off turbo, oil cooler
s. open bell jar
t. retrieve wafer

15. SiO_2 deposition – 2000Å
a. vent system
b. open bell jar
c. insert wafer
d. close bell jar
e. open roughing valves
f. turn on oil cooler, turbo
g. wait for ion gauge controller reading 2 x 10^{-6}
h. turn on Ar, adjust flow to 40sccm
i. adjust vacuum to 11 microns
j. turn on water cooling valve
k. turn on RF sputtering system
l. ignite plasma
m. adjust output power to 400W, reflected power to zero
n. sputter for 20 min.
o. turn off RF sputtering system
p. turn off Ar
q. turn off water
r. turn off turbo, oil cooler
s. open bell jar
t. retrieve wafer

16. Piranha clean – see step 9

17. PR-2 – photoresist, mask level 2, positive PR
a. dehydration bake @ 135°
b. cool to room temperature
c. place wafer on chuck
d. blow with N_2
e. drop PR, check for air bubbles
f. spin @ 5000 rpm – 30 sec.
g. bake @ 95° – 25 min.

h. expose – 7 sec.
i. develop – 25-35 sec.
j. rinse in di water – 30 sec.
k. blow dry with N_2
l. inspect under microscope
m. hard bake @ 135°
n. inspect

18. Oxide etch – see step 6 – 2.5 min.

19. PR strip
  a. place wafers in boat
  b. submerge in Posistrip 830 – 2 hours
  c. running di water rinse – 10 min.
  d. blow dry with N_2
  e. inspect with microscope
  f. hard bake @ 135° – 15 min.

20. Si_3N_4 etch
  a. heat Transetch N to 180°
  b. blow wafers with N_2
  c. load wafer in Teflon boat
  d. submerge in solution – 20 min.
  e. running di water rinse – 10 min.
  f. blow dry with N_2
  g. inspect with microscope

21. Polysilicon oxidation – 5 min./6 hr. 30 min./5 min., 1050 °

22. SiO_2 strip – see step 6 – 5 min.

23. Si_3N_4 strip – see step 20 – 20 min.

24. Piranha clean – see step 9

25. n implant – 5.7×10^{12} cm^{-2}, 80keV

26. Piranha clean – see step 9

27. Implant activation/drive-in –5/5/50, 950°

28. Piranha clean – see step 9

29. PR-3 – photoresist, mask level 3, negative PR
  a. dehydration bake @ 135°
  b. cool to room temperature
  c. place wafer on chuck
  d. blow with N_2
  e. drop PR, check for air bubbles
  f. spin @ 5000 rpm – 30 sec.
  g. bake @ 95° – 30 min.
  h. expose – 80 sec.
  i. develop – 90 sec.

j. resist rinse – 60 sec.
k. proponal rinse – 30 sec.
l. blow dry with N_2
m. inspect under microscope
n. hard bake @ 135°
o. inspect
NOTE: Smallest geometry sometimes disappeared. Very difficult to align 50μm contact window.

30. Contact oxide etch – see step 6 – 20-23 min.
31. PR strip – see step 8
32. Piranha clean – see step 9
33. Al evaporation – 10 kÅ
34. PR-4 – photoresist, mask level 4, positive PR
    a. dehydration bake @ 135°
    b. cool to room temperature
    c. place wafer on chuck
    d. blow with N_2
    e. drop PR, check for air bubbles
    f. spin @ 5000 rpm – 30 sec.
    g. bake @ 95° – 25 min.
    h. expose – 4 sec.
    i. develop – 25-35 sec.
    j. rinse in di water – 30 sec.
    k. blow dry with N_2
    l. inspect under microscope
    m. hard bake @ 135°
    n. inspect
35. Al etch – 10-16 min.
36. PR strip – see step 19
37. Contact sinter – 45 min., 400°