DIRECT WRITE LASER LITHOGRAPHY FOR DISCRETIONARY INTERCONNECTIONS

by

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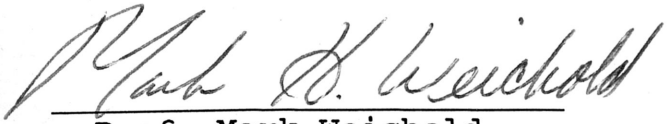
Approved by:



Prof. Mark Weichold

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ABSTRACT

A novel method for making discretionary interconnections involves direct writing on wafer using a precision laser beam and metallization using the lift off process. After experimenting with several line thicknesses, developing times (for lift off), laser power densities and speeds, I succeeded in creating arbitrary interconnections from metal to metal, metal to diffusion and metal to polysilicon on a test structure. The feasibility of step coverage was also investigated. These results are extremely encouraging from a technical standpoint and recommendations are made which would improve this work through further research.

ACKNOWLEDGEMENTS

Taking a moment to reflect upon the efforts of certain individuals who were behind the success of this project, I shall mention an enthusiastically supportive group who essentially made it all possible. First of all, I extend my appreciation to Prof. Mark Weichold of the Texas A&M University Institute for Solid State Electronics for his expertise, devotion and patience--all of which helped make this research project a success. Furthermore, I must not forget Mr. Jay Comparetto of Electro Scientific Industries who generously assisted and guided me in using the laser system and in crucial laboratory work. I would also like to thank Mr. Robert Atkins, Mr. Bill Gibler, Mr. H. C. Huang and Mr. Victor Swensen of the Institute for Solid State Electronics for their numerous contributions to my laboratory research work and Mr. Douglas Suckow of Electro Scientific Industries for his assistance in troubleshooting computer programs.

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INTRODUCTION

The advent of the integrated circuit several decades ago introduced the concept of interconnecting circuits on a silicon substrate. Wafer scale integration (WSI) extends this idea by using the full surface of a wafer for interconnections. The challenge of WSI is to increase reliability and speed while solving the problem of yield [1].

Interconnections, which play a vital role in very large scale integrated (VLSI) circuit technology, are needed primarily due to two reasons. First, pins must be provided from a packaged system to connect the internal integrated circuitry to other packaged systems. Second, the chips inside the system must be connected to perform desired functions.

Currently, fusible links and laser links are used for interconnections. The method I investigated is direct write on wafer using a precision laser followed by metallization using the lift off process [Fig. 1]. This eliminates the need for optical lithographic masks which are time consuming to prepare. The most important aspect of this method may be the ability to test or even repair faulty circuitry. Thus, a WSI circuit, which is too costly to discard unlike a chip, may be "rewired" or repaired as needed using standard integrated circuit

processing equipment. This makes the above mentioned technique very attractive economically.

In the development of new IC's one must actually test their ability to perform the desired function after fabrication in order to verify the design. The process described in this thesis uses well characterized photolithographic processes subject to selective exposure using a laser beam. Contact may be made to selected portions of an existing circuit to allow the observation of a signal, the injection of a signal or even the termination of the propagation of a signal through the removal of material.

The lift off process allows for metallization after photoresist exposure and development. The exposed wafer is soaked in chlorobenzene to provide a top layer of resist which is more resistant to developer action. This results in an undercut profile after resist development. With this undercut in the resist image, metal is evaporated over the entire surface and a discontinuity is maintained between the metal on the substrate and the metal over the resist. When the resist is removed, the metal over the resist is also removed. This provides a clear reproduction of the image in the metal. An additional advantage of the lift off process is that multilevel metal structures can be formed and any material or combination of materials that can be evaporated can be used [2].

EXPERIMENTAL WORK

A test structure was built by using three mask levels to test the feasibility and yield of the proposed process. Next, arbitrary interconnections from metal-metal, metal-N+-metal, metal-N+-polysilicon-metal, pad-N+-metal, and pad-polysilicon-metal were made by direct writing with a laser beam and then using metallization by lift off. I shall first discuss the preparation of the test structure. Then I shall describe in detail how the arbitrary interconnections were made.

(a) Test Structure

Step 1 - Grew 5000 Å of SiO_2 at 1000°C [Fig. 2].

Step 2 - Deposited 5000 Å of polysilicon at 680°C [Fig. 2].

Step 3 - Spun positive resist at 5000 rpm for 30 seconds, soft baked at 65°C for 15 minutes, patterned with mask level 1, developed for 1 minute in a 1:1 solution of DI water at MF 312 Shipley Developer and hard baked at 135°C for 1 hour [Fig. 3].

Step 4 - The polysilicon was etched in the plasma etcher. DE100 was used at a power of 100W for 10 minutes [Fig. 4].

Step 5 - The positive resist was stripped with O_2 in the plasma etcher at a power of 250W for 50 minutes [Fig. 4].

Step 6 - Spun negative resist at 5000 rpm for 30 seconds, soft baked at 90°C for 30 minutes, patterned with mask level 2, treated with negative projection developer for 90 seconds, negative resist rinse for 60 seconds, propanol for 30 seconds and hard baked at 135°C for 1 hour [Fig. 5].

Step 7 - The oxide was etched using a solution of buffered oxide etch until all the windows were clear [Fig. 6].

Step 8 - The negative resist was stripped with O_2 in the plasma etcher at a power of 250W for 50 minutes [Fig. 6].

Step 9 - A $PoCl_3$ predeposition was carried out at 900°C with an O_2 flow through $PoCl_3$ for 10 minutes [Fig. 7].

Step 10 - A drive in at 1000°C was carried out [Fig. 7].

Step 11 - 6000 Å of aluminum was deposited using a filament evaporator.

Step 12 - Positive resist was spun at 5000 rpm for 30 seconds, soft baked at 65°C for 15 minutes, patterned with mask level 3, developed for 1 minute in a 1:1 solution of DI water and MF 312

Shipley Developer and hard baked at 135°C for 1 hour.

Step 13 - Wafers were placed in a wet aluminum etch until all the unnecessary aluminum came off.

Step 14 - The positive resist was stripped with O_2 in the plasma etcher at a power of 250W for 50 minutes [Fig. 7].

This completed the preparation of the test structure [Fig. 8].

(b) Arbitrary Interconnections

I shall first describe the key steps involved in making arbitrary interconnections, which included step coverage [Fig. 9], and then discuss the problems I encountered and what I did to correct these problems.

Step 1 - Wrote CIF programs to make direct write laser patterns from metal to metal [Fig. 10], metal-N+-metal and metal-polysilicon-metal [Fig. 11], metal-N+-polysilicon-metal [Fig. 12], pad-N+-metal and pad-polysilicon-metal [Fig. 13] and finally to open contact windows [Fig. 14].

Step 2 - Spun positive laser resist at 5000 rpm for 30 seconds and soft baked at 95°C for 30 minutes.

Step 3 - Made metal-metal patterns and opened contact windows by direct writing with the laser.

Step 4 - The wafer containing metal-metal patterns was developed for the lift off process with a 2

minute chlorobenzene soak followed by a 1:1 mixture of DI water and MF312 Shipley Developer for 70 seconds [Fig. 15]. The wafer with contact window openings was developed for 45 seconds in a 1:1 mixture of DI water and MF312 Shipley Developer and hard baked at 135°C for 1 hour.

Step 5 - The wafer with contact window openings was placed in a buffered oxide etch solution until all the windows were clear.

Step 6 - The hard baked resist was stripped using a nophenol solution at 105°C for 30 minutes.

Step 7 - Positive laser resist was spun at 5000 rpm for 30 seconds over the wafer containing the contact window openings, soft baked for 30 minutes at 95°C and metal-N+-metal, metal-polysilicon-metal, metal-N+-polysilicon-metal, pad-N+-metal and pad-polysilicon-metal patterns were direct written by the laser.

Step 8 - This wafer was developed for the lift off process with a 2 minute chlorobenzene soak followed by a 1:1 mixture of DI water and MF312 Shipley Developer for 70 seconds.

Step 9 - Using the aluminum evaporator, 1800 Å of aluminum was deposited on the wafers.

Step 10 - The wafers were soaked in acetone and a sonic vibrator was used to take off the unnecessary aluminum by the lift off process [Fig. 13].

PROBLEMS ENCOUNTERED AND EXPERIMENTAL SOLUTIONS

(1) I had to experiment with several laser power densities and speeds for the metal-metal patterns. While too much laser exposure made the lines considerably wider than the theoretical width, too little exposure resulted n discontinuous lines. I varied the laser power density from 0-50 mw/cm^2 to 1-20 mw/cm^2 in steps of 0-05 mw/cm^2 and the scanning speed from 7.5 mm/s to 20 mm/s in steps of 2-5 mm/s. From this matrix, I found the best combination of power density and scanning speed. The contact window openings posed little problems and I experimented with power densities ranging from 0-30 mw/cm^2 to 0-75 mw/cm^2 and scanning speeds ranging from 10 mm/s to 20 mm/s.

(2) Centering the laser direct write pattern on the existing die was a major problem which has been only partially solved. The program I used to run these patterns is Esimask which is used for mask making. Thus, it seems to interpret the direct laser patterns in a not too predictable manner. Modifications to Esimask and automatic aligning and centering (which is significantly

more accurate than manual aligning and centering I used) should make this process much simpler.

(3) Developing a wafer for the lift off process is a crucial step because the undercut profile has to be just right. I experimented with developing times ranging from 45 seconds to 85 seconds in steps of 10 seconds.

OPTIMUM CONDITIONS AND LASER DATA

Laser Pattern Generation Mode - Raster scan

Laser Positioning Resolution - 2-5 μm

Laser Repetition Rate - 20000 HZ

Laser Wavelength - 457.9 nm

Optimum power density and scanning speed for the direct write lines - 0.85 mw/cm^2 and 12-5 mm/s.

Optimum power density and scanning speed for the contact windows - 0.50 mw/cm^2 and 20 mm/s.

Optimum developing time (for lift off preparation) - 70 seconds.

Metal-metal line width = 5 μm.

Contact window area = 6 μm x 6 μm.

RESULTS

I probed 3 different dice of metal-metal interconnections and measured the resistances of 11 different paths on each die [Fig. 10]. Then I calculated the average resistance of each path, denoted by R_{AB} through R_{EA}, and the standard deviation, denoted by S_{AB} through S_{EA}, associated with each average path resistance. All values are in ohms.

$R_{AB} = 10.29$	$S_{AO} = 3.72$
$R_{CD} = 22.60$	$S_{CD} = 2.99$
$R_{CE} = 33.59$	$S_{CE} = 7.79$
$R_{CG} = 61.05$	$S_{CG} = 36.52$
$R_{FG} = 26.61$	$S_{FG} = 6.51$
$R_{FI} = 30.70$	$S_{FI} = 0.97$
$R_{HI} = 22.49$	$S_{HI} = 3.10$
$R_{HA} = 39.39$	$S_{HA} = 19.03$
$R_{JM} = 21.51$	$S_{JM} = 4.90$
$R_{JL} = 20.11$	$S_{JL} = 6.07$
$R_{EA} = 211.37$	$S_{EA} = 69.16$

R_{EA}, which is the resistance from Pad E to Pad A, should be equal to $R_{CE} + R_{CG} + R_{FG} + R_{HZ} + R_{HA}$

$R_{EA}{}^{1} = R_{CE} + R_{CG} + R_{FG} + R_{FI} + R_{HI} + R_{HA} = 213.83$

$R_{EA} = 211.37$

This is only a 1.16% difference.

DISCUSSION

The path resistance measured directly from Pad E to Pad K differs only by a small margin from the sum of individual path resistances from Pad E to Pad K, namely the path resistances from Pads E to C, C to G, G to F, F to I, I to H and H to K. Although not conclusive, this suggests that the step resistances are very small compared to the actual line resistances.

From the results I have obtained, it is evident that direct write on laser followed by metallization with lift off is possible. The major problems I encountered were the manual centering and aligning of the pattern. However, this could be easily solved by using an automatic centering and aligning processr, i.e. beam to work alignment algorithms. In the laser system I used, the positioning resolution was 2.5 μm. I observed that this tends to increase the width of direct write lines and the area of contact windows. In fact, while the theoretical values for the line width and contact window area are 5 μm and 6 μm x 6 μm, the actual line width and contact window area are 8 μm and 9 μm x 9 μm. I predict that this problem could be corrected by using a laser with a smaller positioning resolution. Thus, although my research work is not complete, further avenues of research along these lines could lead to a satisfactory and practically applicable process.

CONCLUSIONS

The research work carried out in this work seems to indicate that direct write by laser followed by metallization with lift off holds wide applications in wafer scale integration as well as in circuit testing. This process could be used in three ways. First, interconnections for the wafer scale integrated circuit could be provided. Second, in case of a bad circuit, (which is too expensive to discard) we could "rewire" the circuit as needed. This process certainly takes advantage of a laser's precision and metal's low resistivity. Furthermore, standard integrated circuit processing equipment could be used for this process which makes it very attractive economically. Third, this technique may be used to provide arbitrary access to an IC for testing functionality.

This could be done by making contact to a selected portion of circuit. This will allow us to observe signals, inject signals or even terminate the propagation of a signal through the removal of material. Other advantages include non existence of surface charging, compatibility with current semiconductor technology, making contacts and hence measurements to circuit features too small to microprobe and incorporation of CAD layout tools to specify the arbitrary interconnections.

Wafer scale integration avoids the high costs associated with packaging individual integrated circuits

on a printed circuit board because it uses the full surface of a wafer for interconnections. Thus, fewer pins protrude from a WSI circuit than from a regular integrated circuit system. This increases system reliability and signal speed. The biggest advantage of WSI may be the replacement of a number of chips on a printed circuit board with a single wafer. This eliminates interchip connections which are a problem since they waste space, introduce noise signals and consume extra power. As such, WSI will play an important role in high technical components Thus, it would not be surprising if direct write on laser followed by metallization with lift off is the key to WSI design.

REFERENCES

(1) Jack F. McDonald, Edwin H. Rogers, Kenneth Rose Andrew J. Steckl, "The Trials of Wafer Scale Integration": IEEE Spectrum, Oct. 1984, p. 32.

(2) Gilman D. Chesley, "Main Memory Wafer Scale Integration": VLSI Design, March 1985, p. 54.

(3) H. C. Pfeiffer, "Direct Write Electron Beam Lithography": Solid State Technology, Sept. 1984, p. 223.

(4) Stephen Trimberger, "Reaching for the Million Transistor Chip": IEEE Spectrum, Nov. 1983, p. 100.

(5) R. F. W. Pease, "Fabrication Issues for Next Generation Circuits": IEEE Spectrum, Nov. 1983, p. 192.

(6) James F. Donohue, "Lasers Make IC Chips at Lower Temperatures": High Technology, Sept. 1984, p. 75.

(7) M. P. C. Watts, "Electron Beam Resist Systems-A Critical Review of Recent Developments": Solid State Technology, Feb. 1984, p. 111.

(8) Sharad C. Seth, Vishwani D. Agrawal, "Cutting Chip Testing Costs": IEEE Spectrum, April 1985, p. 38.

(9) Mark A. Fischetti, "Solid State": IEEE Spectrum, Jan. 1984, p. 58.

(10) Wilmer R. Bottoms, "Equipment Requirements for Submicron VLSI Production": Solid State Technology, Aug. 1984, p. 155.

(11) Jeff Hecht, "Outlook Brightens for Semiconductor Lasers": High Technology, Jan. 1984, p. 43.

(12) Roy A. Colclaser, "Micro Electronics-Processing and Device Design": John Wiley & Sons, Inc., 1980.

(13) M. Hatzakis, B. J. Canavello, J. M. Shaw, "Single Step Optical Lift-off Process," IBM J. Res. Develop., Vol. 34, No. 4, July 1980, p. 452.

(14) Karl L. Harris, Paul Sandland, Russell M. Singleton, "Automated Inspection of Wafer Patterns with Applications in Stepping, Projection and Direct Write Lithography": Solid State Technology, Feb. 1984, p. 159.

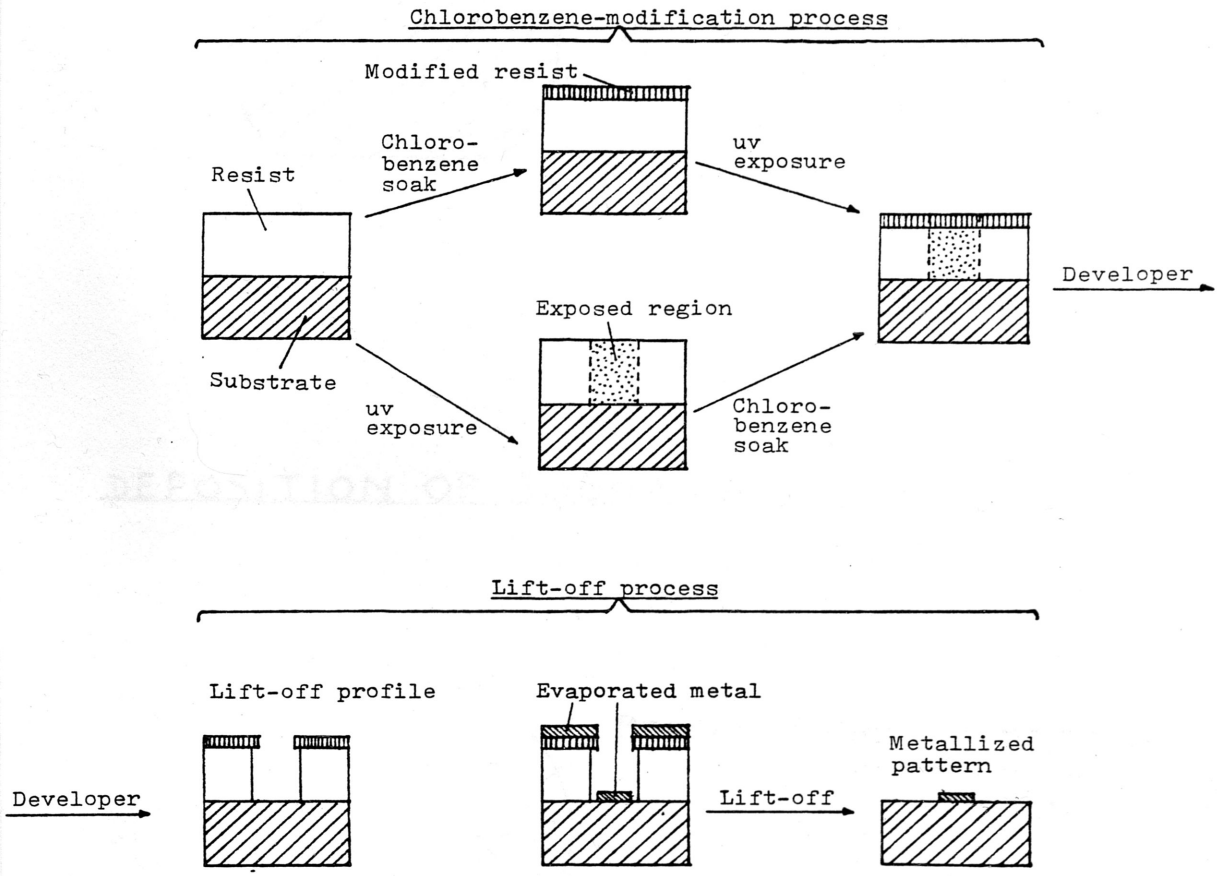
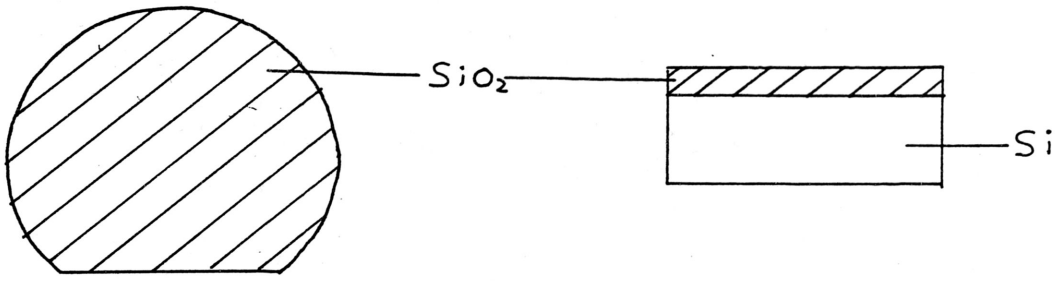


Figure 1 - Schematic of the lift-off and chlorobenzene modification process.

Figure 1

GROWTH OF 5000 Å OF SiO_2



DEPOSITION OF 5000Å OF POLYSILICON

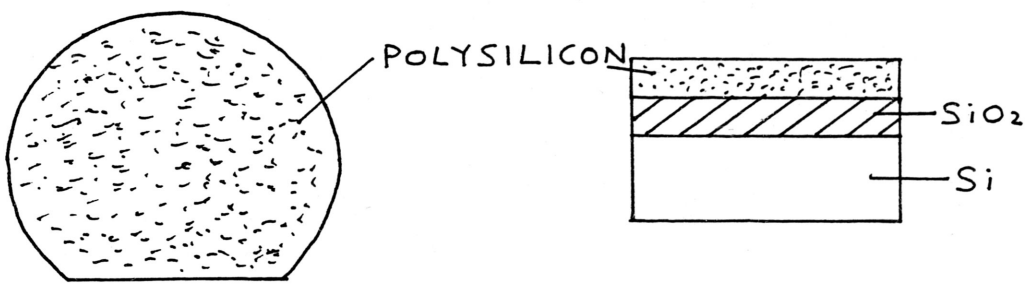
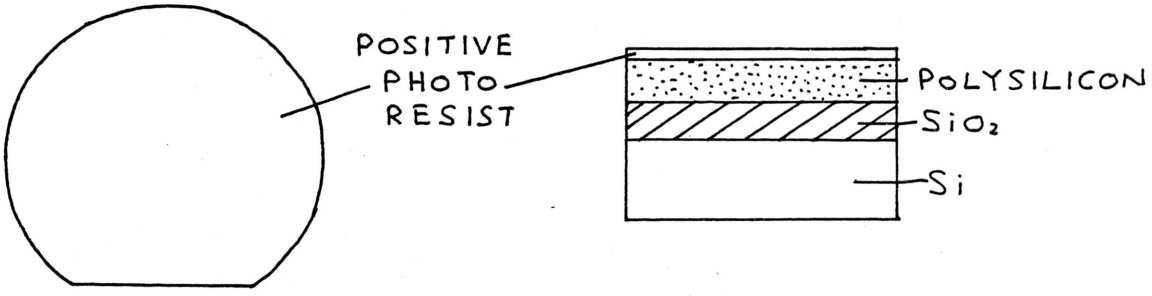


Figure 2

SPIN POSITIVE RESIST



PATTERN WITH LEVEL 1

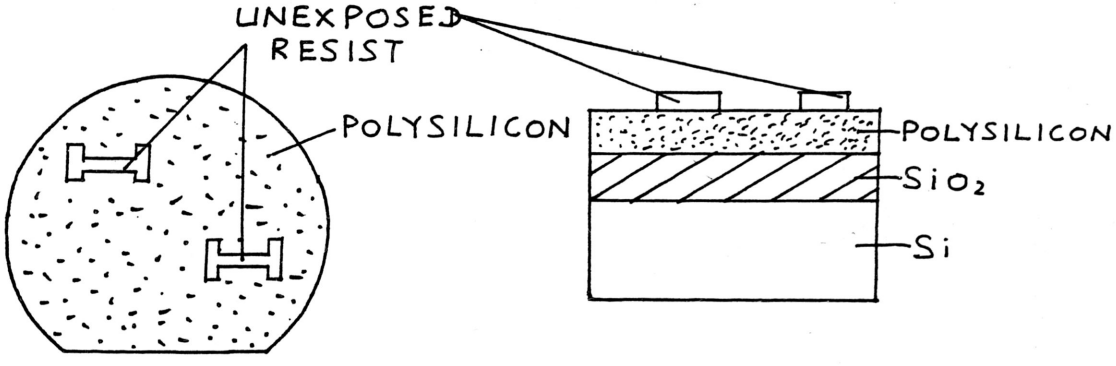
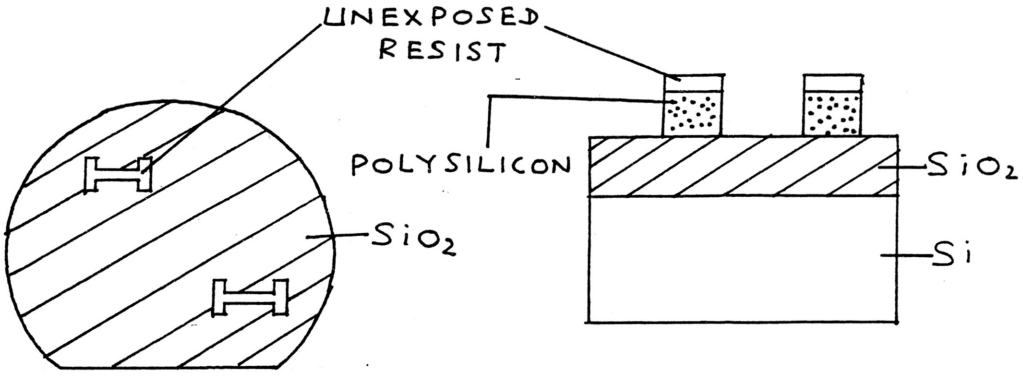


Figure 3

ETCH POLYSILICON



STRIP POSITIVE RESIST

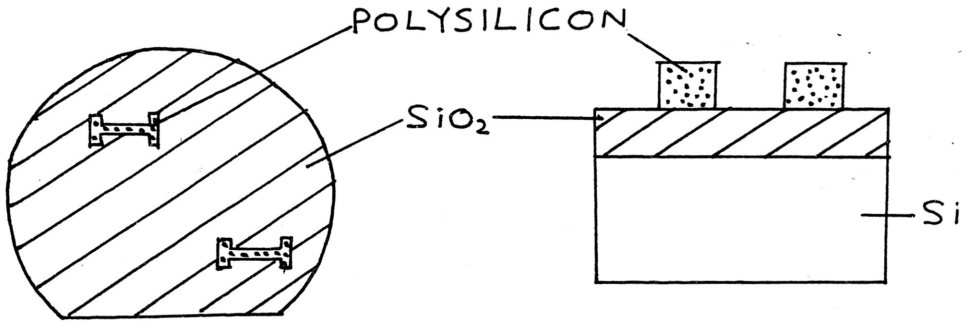
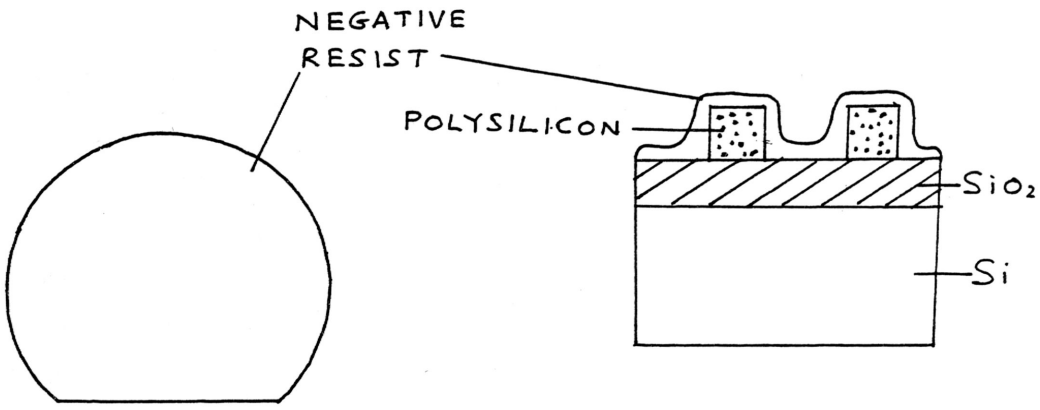


Figure 4

SPIN NEGATIVE RESIST



PATTERN WITH LEVEL 2

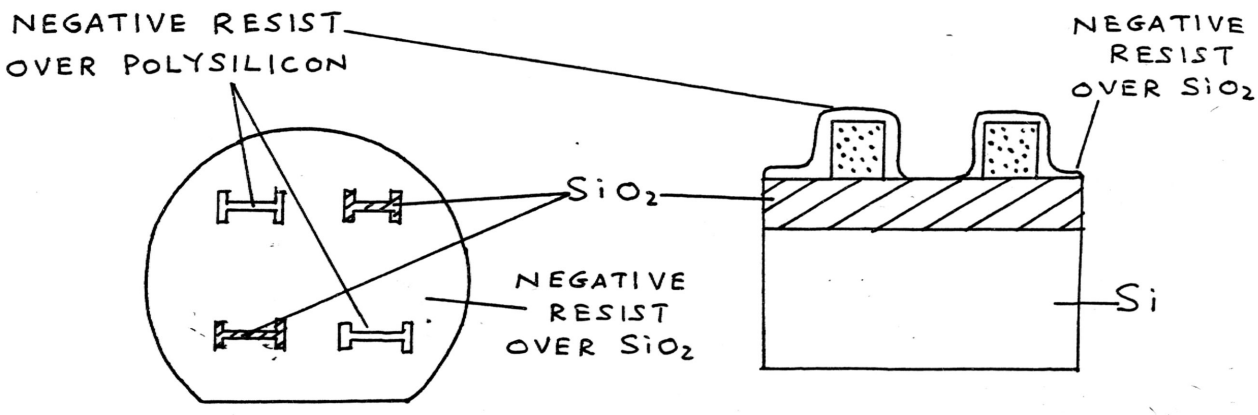
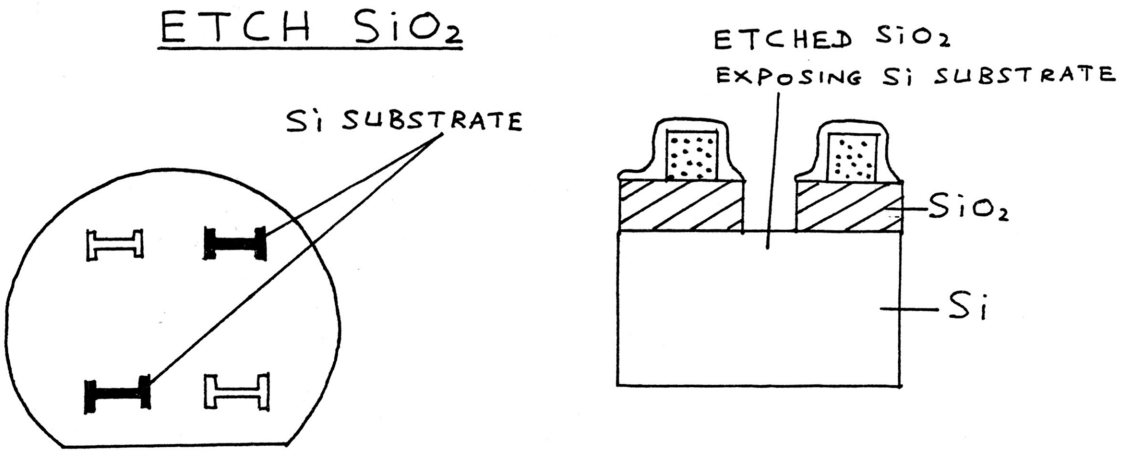


Figure 5


ETCH SiO_2
Si SUBSTRATE
ETCHED SiO_2
EXPOSING Si SUBSTRATE
SiO_2
Si

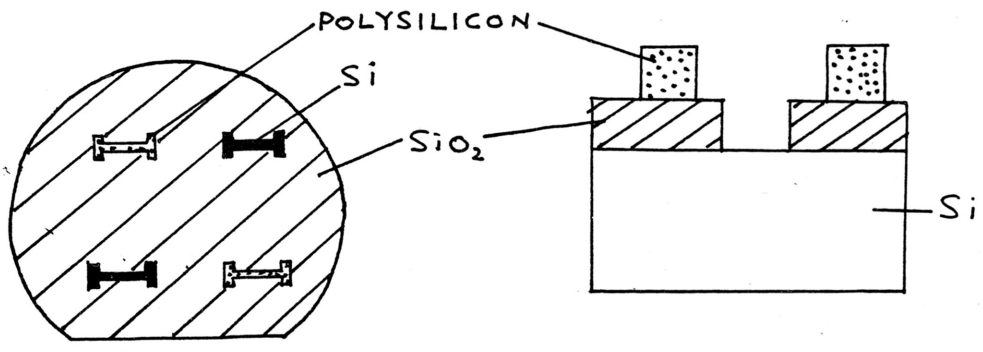
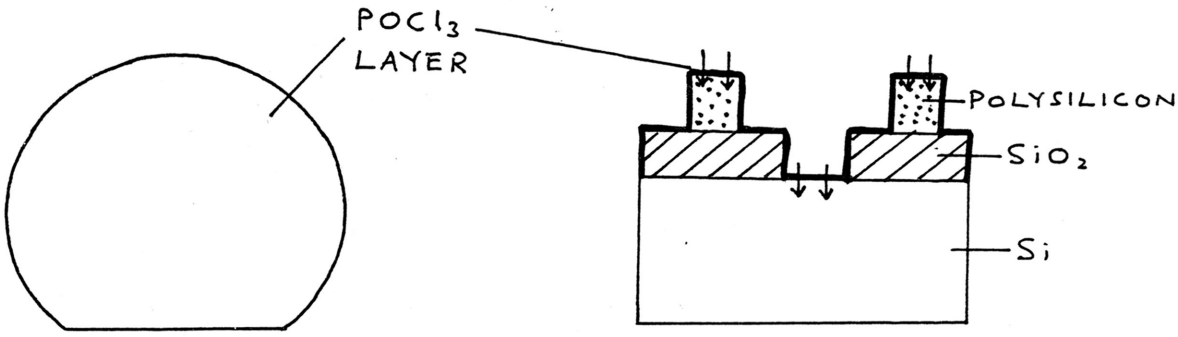

STRIP NEGATIVE RESIST
POLYSILICON
Si
SiO_2
Si

Figure 6

$POCl_3$ PREDEPOSITION & DRIVE IN



DEPOSIT 6000Å OF Al

SPIN POSITIVE RESIST; PATTERN WITH LEVEL 3

ETCH Al.

STRIP POSITIVE RESIST

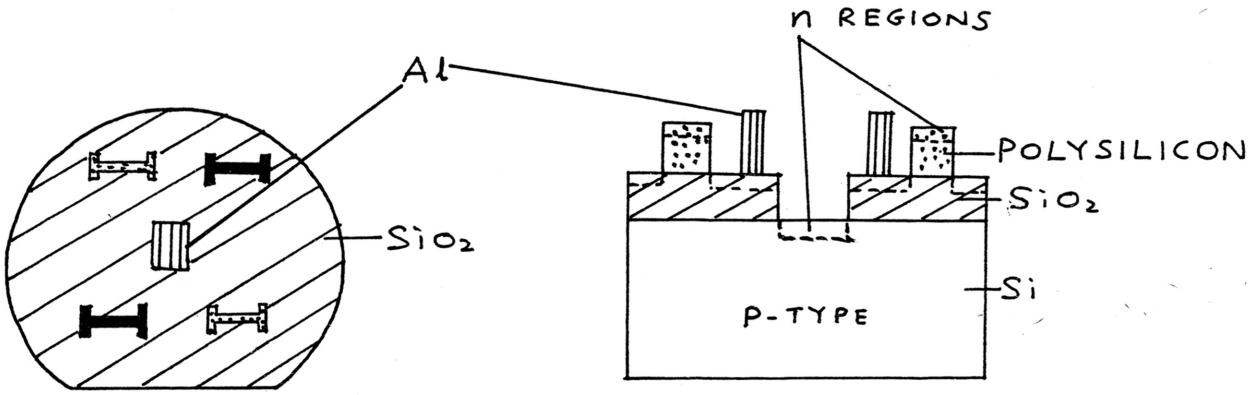


Figure 7

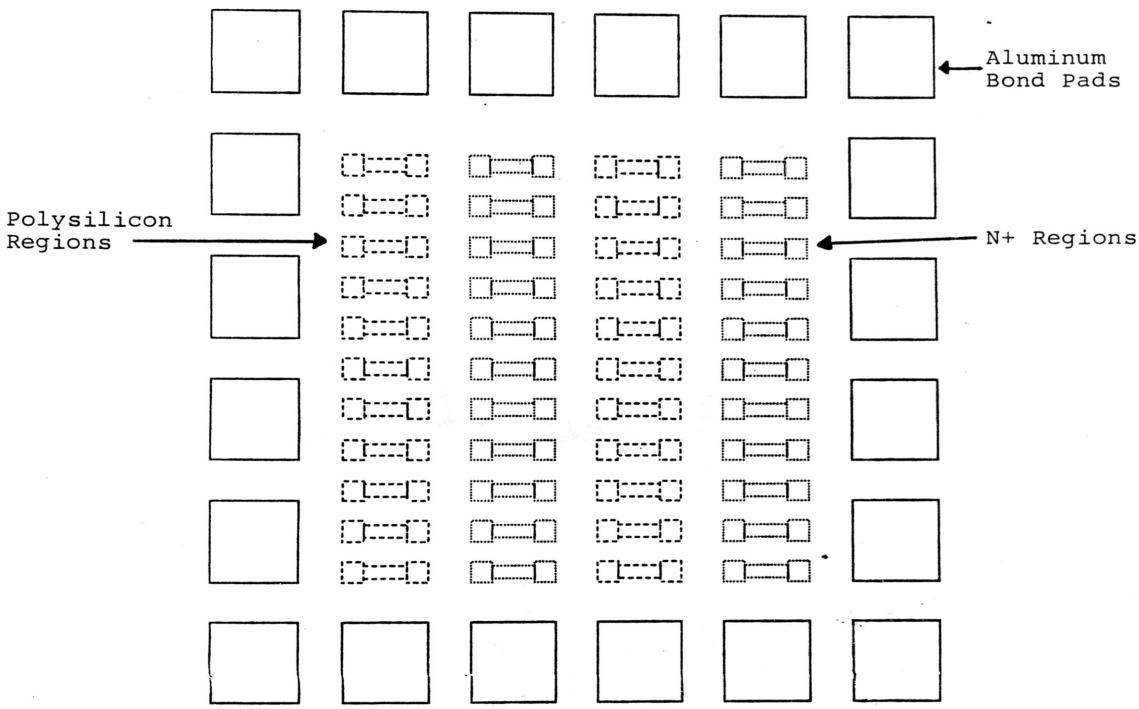
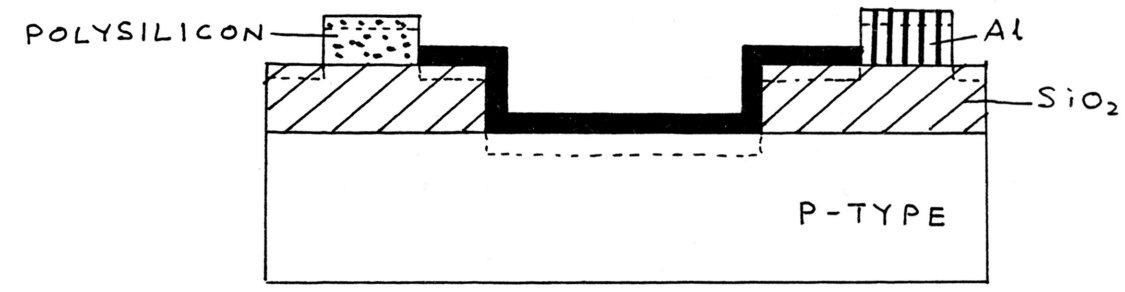
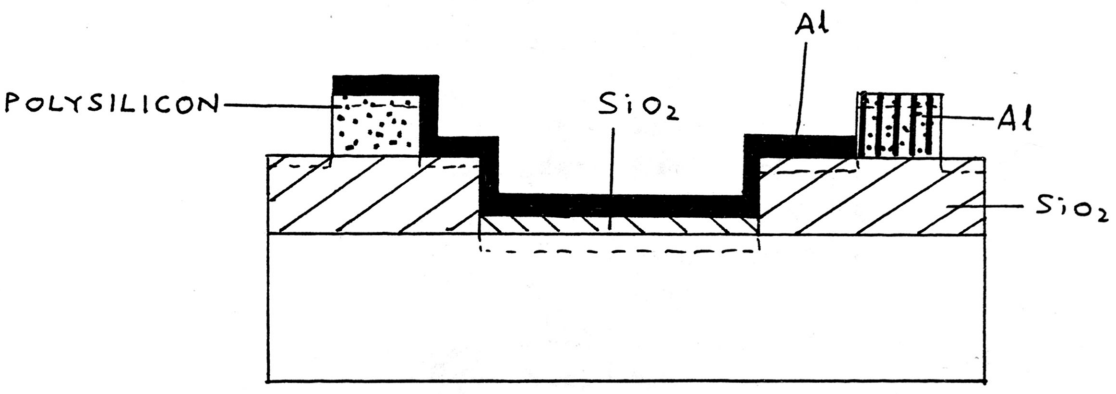


Figure 2. Mask set for yield and reliability measurements.

Figure 8 Test Structure





STEP COVERAGE.

Figure 9

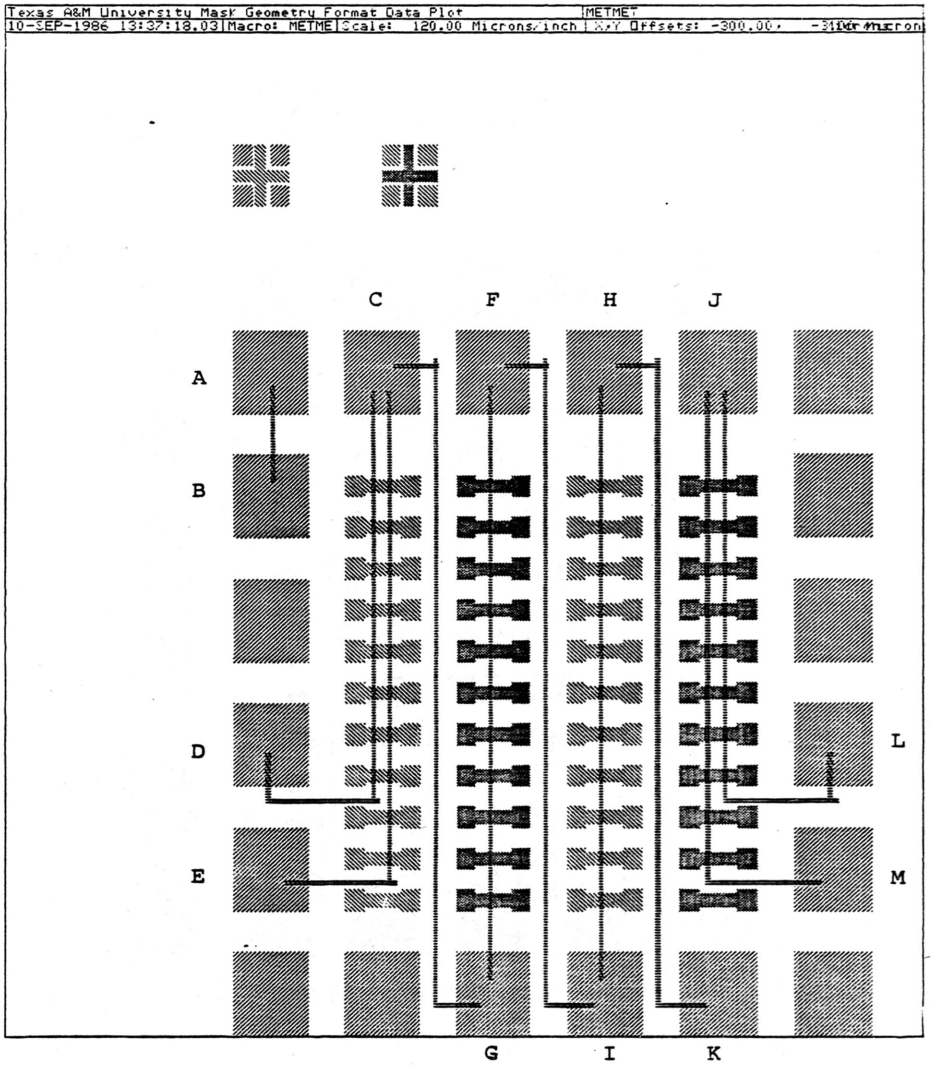


Figure 10 Metal to Metal Interconnections

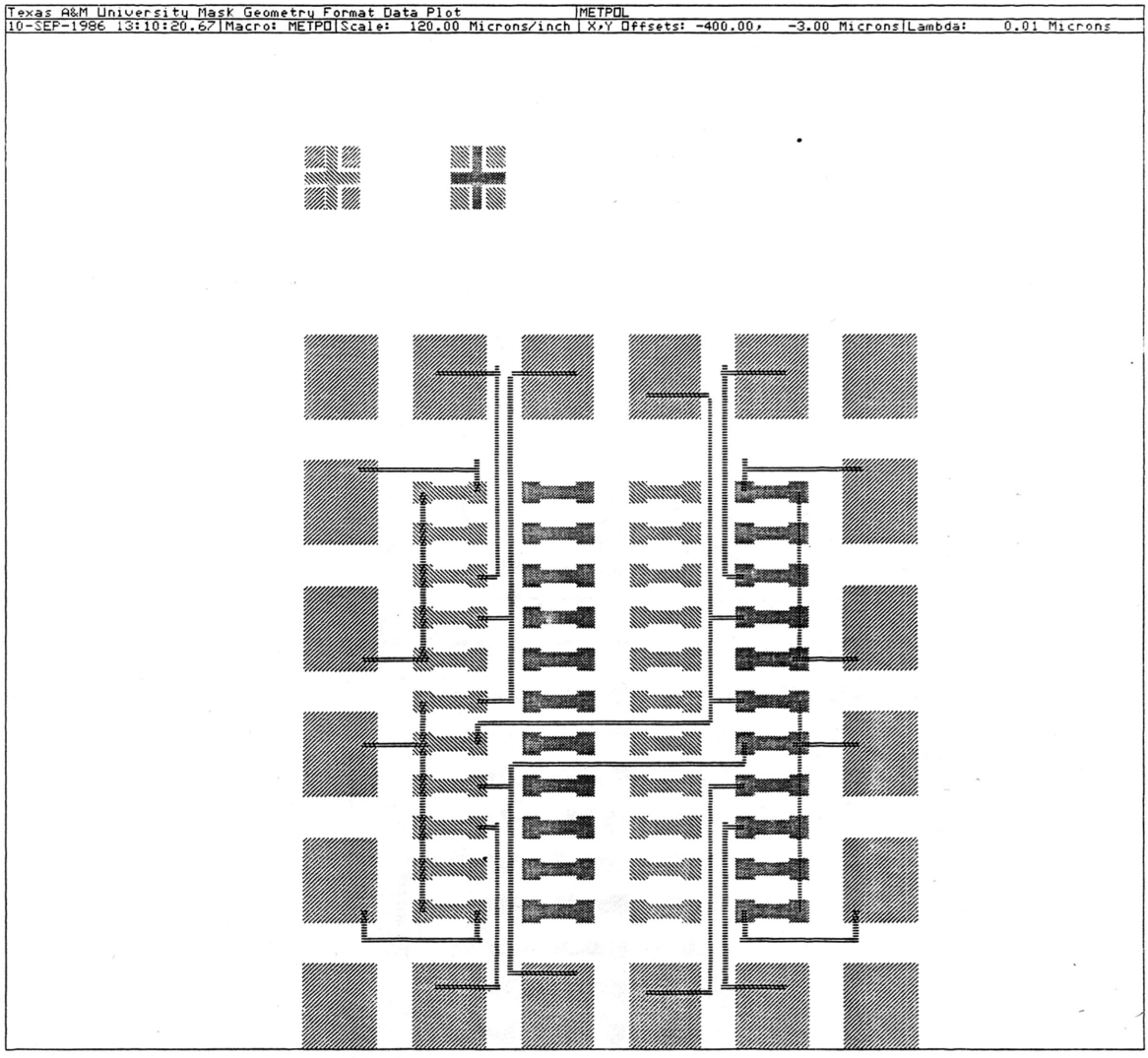


Figure 11 Metal-N+-Metal and Metal-Polysilicon-Metal Interconnections

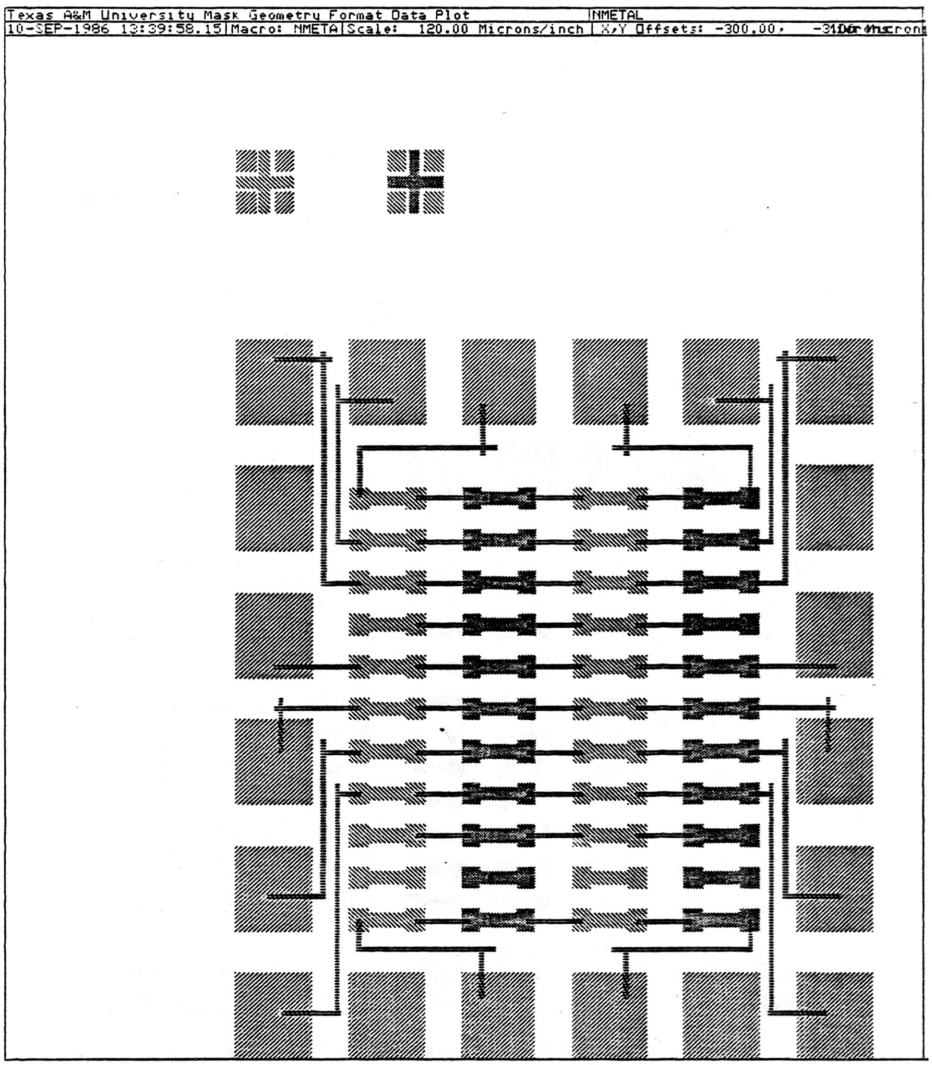


Figure 12 Metal-N+-Polysilicon-Metal Interconnections

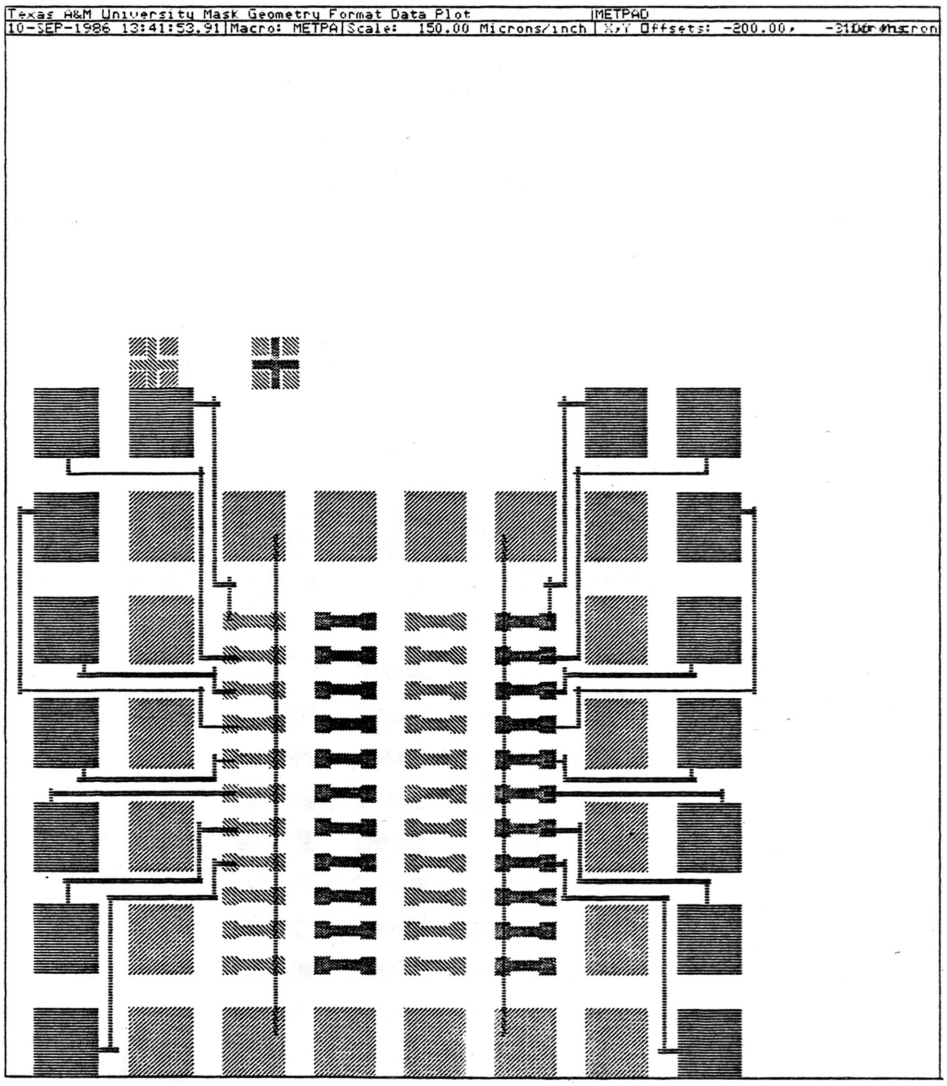


Figure 13 Pad-N+-Metal and Pad-Polysilicon-Metal Interconnections

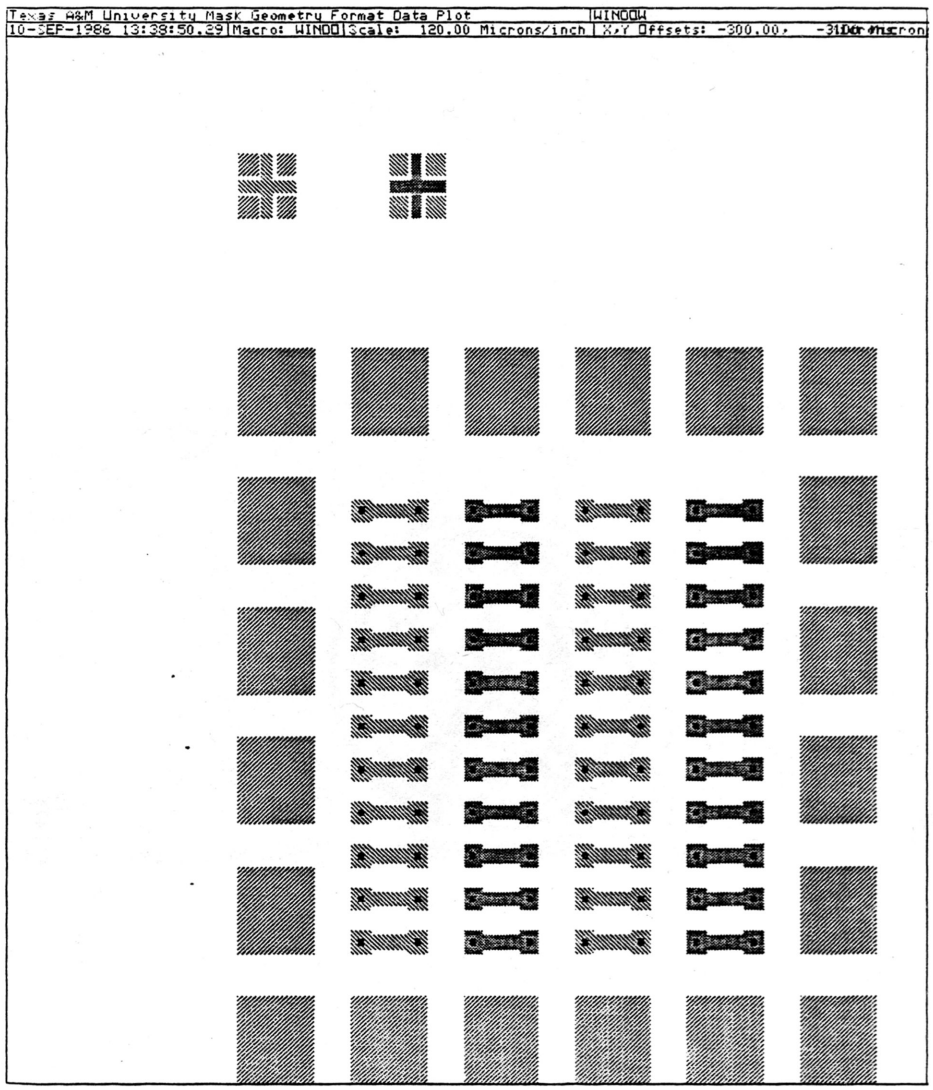
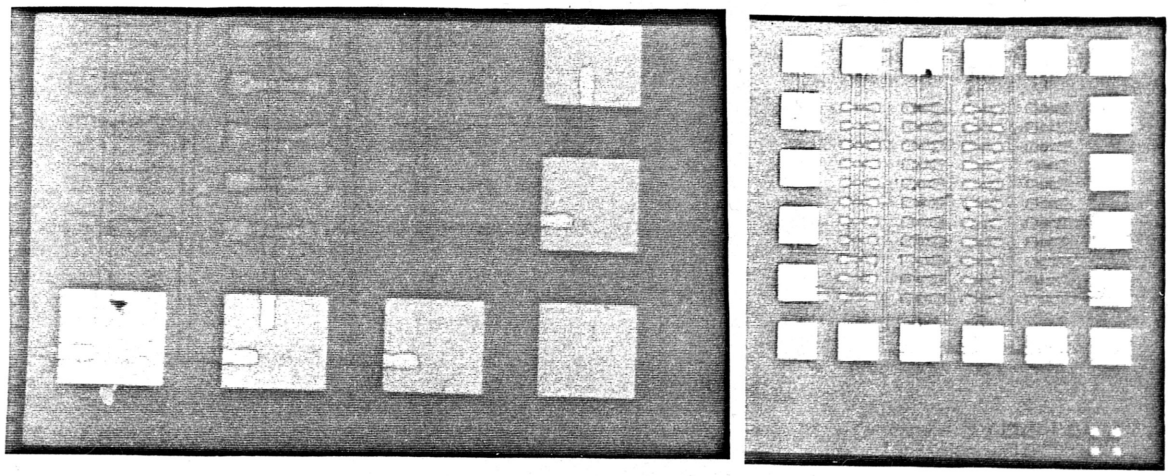


Figure 14 Contact Window Openings

Photographs after developing (for lift off)
and before depositing aluminum



Photographs after the lift off process -
these are aluminum lines

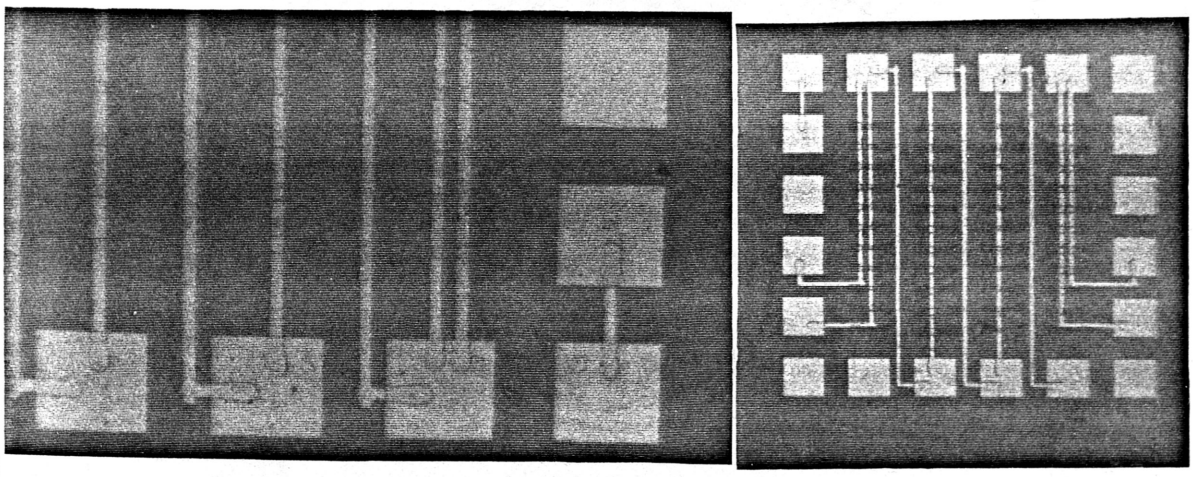


Figure 15