AUTOMATIC TESTING OF INTEGRATED CIRCUITS

by

Paul D. Bassett

Electrical Engineering Department

Submitted in Partial Fulfillment of the Requirements of the University Undergraduate Fellows Program

1981-1982

Approved by:

Randall Geiger

Dr. Randall R. Geiger

May 1982

Abstract

Two projects are discussed. First, automatic control of an SPI-C Wafer Prober via an HP 9845 computer for the purpose of testing selected die locations on an integrated circuit wafer is discussed. Included are discusions of two alternative control schemes and the documentation of the necessary alterations and software for scheme implemented.

Secondly, automated measurement of the parameters of Bipolar Junction Transistors (BJT°s) is discussed. The relationships making measurements possible and the experimental setup and algorithms used are considered. Also, some examples of the experimental results are given.

Table of Contents

Introduction 1

Literature Review 3

Automatic Control of a Wafer Prober

Introduction 4

Automatic Mode Control Scheme 4

Manual Mode Control Sheme 6

Conclusions 9

Determination of BJT Parameters

Introduction 10

Model Parameters 10

Parameter Determination Techniques 13

Experimental Setup 14

Measurement Algorithms 15

Results and Conclusions 17

References 24

List of Figures

Fig. 1. Generation of Control Signals for the Wafer Prober 7

Fig. 2(a). Ebers-Moll Equations for the Collector and Base Currents 11

(b). Inclusion of the Early Voltage and its effects of the I_C vc V_{CE} curves 11

Fig. 3(a). Injection version model 12

(b). Transport version model 12

Fig. 4. Experimental Setup 16

Fig. 5. Forward Beta vs Collector Current 18

Fig. 6. Reverse Beta vs Emitter Current 19

Fig. 7. Ln(Collector Current) vs Base-to-Emitter Voltage 20

Fig. 8. Predicted Collector Current vs Collector-to-Emitter Voltage . . 21

Introduction: IC Testing at Texas A&M University

One of the major weak points in most IC research programs, especially at the academic level, is the lack of feedback concerning the operation of the circuits on a silicon level. Due to the high cost of fabricating small batches of wafers, the delays built into the process and the time required to test a large number of circuits manually, many of the new and innovative circuits never get tested. In the case of Texas A&M°s VLSI program, an agreement between A&M and Texas Instruments Inc. (TI) to have TI fabricate two Multi-Project Chips per year has helped overcome the first problem by combining a large number of projects in a single fabrication run.

This arrangement doesn°t overcome the problem of fabrication delays or testing problems; the first of these is an integral part of the fabrication process but the second problem is currently being addressed at A&M. The efforts in this area include automatic determination of MOSFET and BJT parameters, measurement of frequency related characteristics of circuits such as group delay and transfer functions, automatic positioning of a wafer prober and interaction with the VAX computer for uploading and downloading information.

This report details efforts in two of these areas, the automatic positioning of a wafer prober to facilitate testing circuits while still in wafer form and the automatic determination of BJT paramters for characterizing fabrication processes.

Literature Review

Due to the nature of the problems addressed, very little literature related research was necessary. All of the information concerning the control of the prober was taken from the Maintenance and Operation Manual written by the manufacturer[1]. For the determination of the BJT parameters two sources are listed, the original paper concerning BJT operation by Ebers and Moll and the book by Getreu concerning BJT modeling; however, the information used could have been found in many different locations.

Automatic Control of a Wafer Prober

A. Introduction

In industrial IC manufacturing processes, it is a standard practise to test each of the dies on a wafer individually before cutting the wafer apart and bonding the circuits into their packages. This testing is performed on wafer probers which step across the face of the wafer probing each die and marking those that fail the tests which are conducted by external testers which also supply all the necessary signals for controlling the prober.

The prober in use at A&M is a Western Prober°s Model SPI-C which was given to A&M by TI; it is a standard industrial prober designed for 4 inch wafers. It has both an automatic mode fo automatic testing such as is done in industry and a manual mode which is mainly designed for initial set up and for probing a few selected die locations.

B. Automatic Mode Control Scheme

The first control scheme considered utilized the automatic mode of the prober. In this mode it would be possible to control the positioning of the prober by using the TEST COMPLETE and EDGE SENSE signals to cause the

prober to step through the rows and columns of dies to the proper locations. This scheme would minimize but not eliminate one of the major problems with utilizing the automatic mode, that of making contact with each die as the prober steps past it. Each time contact is made, the bonding pads on the circuit are damaged somewhat and this limits the number of times contact can be made. In the automatic mode, the prober raises its stage to make contact after every step and the only straightforward way to prevent this was to interrupt the power going to the stage which would mean inserting a relay inside the prober and running a signal to it from the external controller.

Two other major problems with his scheme involve the generation and timing of the EDGE SENSE (ES) signal. As with controlling the stage raising, generating the ES signal would require utilizing a relay inside the prober to open and close the ES contacts; also, there were some serious questions about how critical the timing of the ES signal would be in affecting the raising of the stage via a special feature of the pober called its Auto-Z control which controlled the exact amount the stage was raised.

All three of the problems just outlined could have been overcome, probably with a minimum of trouble, but it was decided to alter the scheme and utilize the prober°s manual mode instead of its automatic mode.

C. Manual Mode Control Scheme

When the prober is set for manual operation, the positioning of the stage is controlled by the front panel switches, four for controlling the horizontal movement directions, one for setting the type of movement (Step,Scan or Slow Scan) and one for controlling the vertical movement, also two thumbwheel switches control the sizes of the horizontal steps.

The control scheme developed for this mode utilized the fact that the action of depressing one of the directional switches or switching the Stage Up switch was manifested in the logic by the grounding of a normally HIGH input. Therfore, it was simply a matter of interrupting the switch signals and replacing them with computer generated signals of the same polarity in order to gain control of the prober.

In order to maintain manual control of the prober for use in the intial setup, the externally generated input signals were ANDed with those from the prober switches before feeding them into the control logic. The changes necessary to interrupt the switch signals and input the new signals are documented in Figure 1.

Also a program has been written for using a Digital Output Card in the HP Multiprogrammer to generate the necessary control signals for locating the dies specified by the operator. If requested, the program will draw a sample numbering diagram of a wafer as a reference for the operator. Although this program is available for use it is expected it will function mainly as a tutorial program for demonstrating the necessary control sequences to persons needing to use the prober. If the testing they plan to do is going to be automated via the HP 9845, it would be a

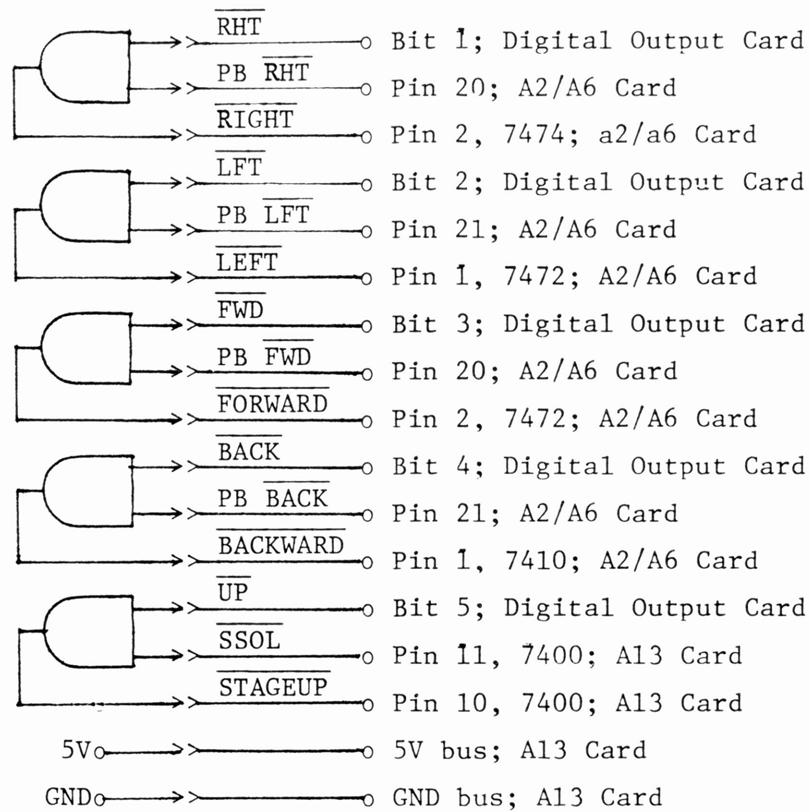

Figure 1. Generation of Control Signals for the Wafer Prober

simple matter for them to include the control sequences directly in their testing programs rather than actually use this program.

D. Conclusions

At this time, the modifications documented in Figure 1 have been made and the software written and tested. Two objectives remain however; first, it is hoped that early this summer the hardware necessary for ANDing the control signals will be put on a PC board and inserted in the cintrol box rather than being on an exterior protoboard. Secondly, it is planned o try and actually include the stepping sequences in a testing program, possibly in conjunction with a 403/404 project or with the testing program described in the next portion of this report.

Determination of BJT Parameters

A. Introduction

The design of complex electronic circuits will generally involve a fair amount of computer simulation of the circutis' performance by programs such SPICE. When utilized properly, these programs can be very useful in predicting a circuits performance; however, one source of error in such programs is in the values of the parameters used in the models for the active devices in the circuits. It was therefore desired to develop techniques and algorithms with which to determine the actual values of those parameters for MOSFETs and BJTs.

B. Model Parameters

The models used for most simulations of bipolar circuits are usually related to the model first developed in 1954 by Ebers and Moll[2]. One common form of the equations used in this model is given in Figure 2(a) along with a schematic representation of a BJT showing the currents and voltages used to specify its operation.

Figure 3 shows two different versions of the Ebers-Moll model for the BJT; Fig. 3(a) shows the original injection version model of Ebers and Moll while

Ebers-Moll Equations for Bipolar Transistors

$$I_C = I_S(e^{V_{BE}/V_T} - e^{V_{BC}/V_T}) - \frac{I_S}{\beta_R}(e^{V_{BC}/V_T} - 1)$$

$$I_B = \frac{I_S}{\beta_F}(e^{V_{BE}/V_T} - 1) + \frac{I_S}{\beta_R}(e^{V_{BC}/V_T} - 1)$$

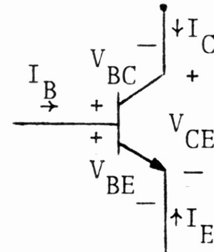

Figure 2(a). Ebers-Moll Equations for the Collector and Base Currents

In Active Region with Early Voltage Effect

$$I_C = I_S(1 + \frac{V_{CE}}{V_{AF}})\, e^{V_{BE}/V_T} \qquad V_{BE} > 0.5$$

$$I_B = \frac{I_S}{\beta_F} e^{V_{BE}/V_T} \qquad V_{BC} < 0$$

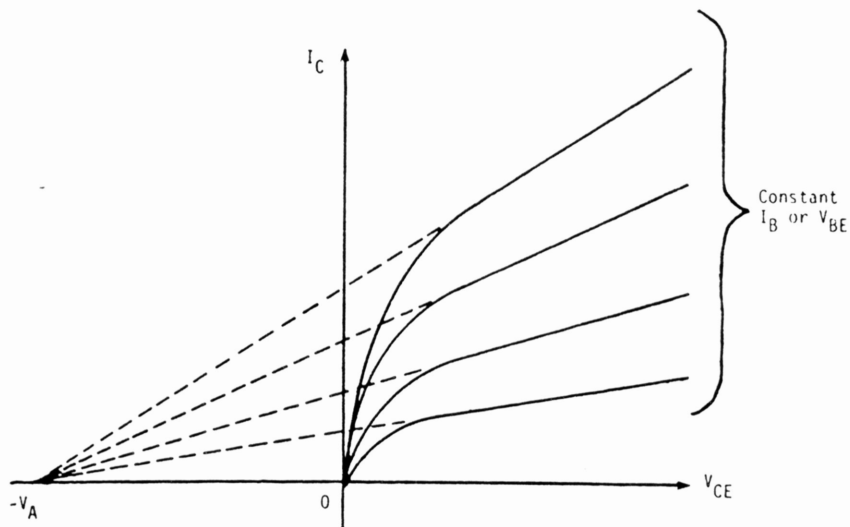

Figure 2(b). Inclusion of the Early Voltage and its Effects on the I_C vs V_{ce} curves

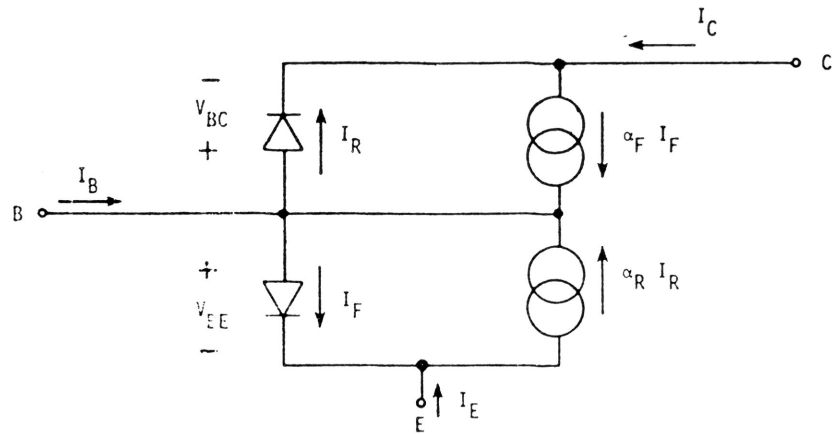

Figure 3(a). Injection version model

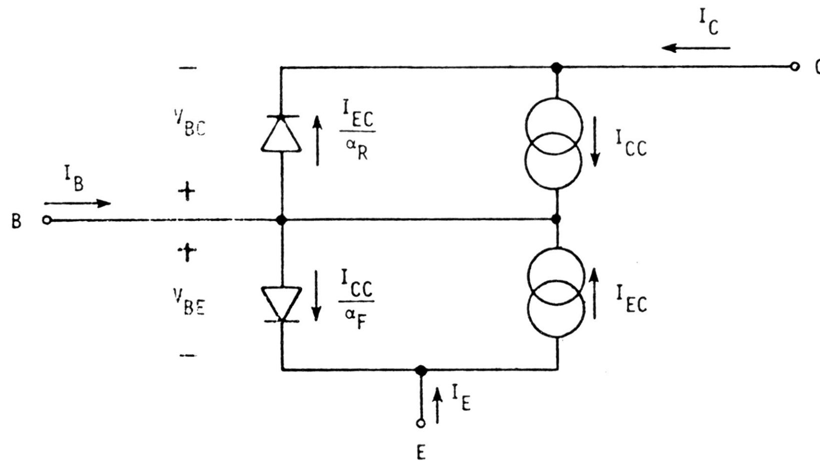

Figure 3(b). Transport version model

Fig. 3(b) shows a slight variation known as the transport version model which uses different currents as it references. The transport version simplifies the model slightly and is therefore the one generally used for computer simulatons[3]. A fairly complete discussion of both models and their parameters is given in the reference; a brief description of the model parameters and effects on interest is given here.

The parameters of interest are all shown in Figure 2; they are I_{SO}, the transistor saturation current at $V_{BC}=0$, β_F the forward current gain in the forward active region, and β_R the reverse current gain in the reverse active region all of which are shown in the equations of Fig. 2(a). Also of interest was V_A, the Early voltage which acounts for the non-zero slope of the I_C vs V_{CE} curves in the forward active region; the addition of V_A and its effects on the curves is illustrated in Fig. 2(b). Finally, the V_T term in the exponentials was to be determined although it is more a measure of the device temperature than a parameter of the BJT. Besides measuring these parameters, it was also desired to look at the variation of β_F and β_R with the current levels.

B. Parameter Determination Techniques

Of the five paramters being determined, $_F$ and $_R$ had the most straightforward measurement schemes since they were simply current ratios. Determination of $_F$ and $_R$ and their variation with current required measurements of I_C and I_B in the forward active region for $_F$ and measurements of I_E and I_B in the reverse active region for $_R$.

The determination of I_{S0}, V_A and V_T required a few more calculations. These last three parameters were all determined from plots of $\ln(I_C)$ vs V_{BE} for two different V_{BC} values, one of which was $V_{BC}=0$. At $V_{BC}=0$, the equation for $\ln(I_C)$ reduces to $I_{S0}((V_{BE}/V_T)+1)$; the $\ln(I_C)$ axis intercept and the slope of this equation plotted vs V_{BE} will be I_{S0} and $1/V_T$ respectively.

The determination of V_A required the additional $\ln(I_C)$ vs V_{BE} plot; the relationship between the saturation current at the second voltage and I_{S0} or between values of I_C for the two V_{BC} values at the same V_{BE} is dependent on V_A and is given by:

$$\frac{I_{S0}}{I_S(V_{BC2})} = \frac{I_C(0)}{I_C(V_{BC2})} = 1 + \frac{V_{BC2}}{V_A}$$

C. Experimental Setup

Figure 4 shows the experimental set up used to take the measurements needed for the parameter determination. The operation of this circuit is fairly straightforward; applying voltages V_B and V_C allowed setting I_C and V_{BC} due to the op amps' null port inputs; measurement of V_{OC} gave I_C and finally measuring V_{BE} gave the final value needed. The two transistors at the op amps' outputs served to prevent overdriving the op amps. All of the measurements for the set up shown would be in the forward active region if $V_{BC}>0$; the reverse active region measurements necessary for determining were taken by switching the positions of the collector and emitter.

D. Measurement Algorithms

In general terms, the procedure for taking the required measurements was not complicated; the major steps could be broken down as follows: set the initial values of R_C, V_B and V_C, measure V_{OC} to check for out-of-range voltages and change R_C if necessary, take final measurements of V_{OC}, V_C, V_B and V_{BE} waiting for each to settle to within one LSB of the A/D card (5mV), and finally, store the data once all the measurements have been made.

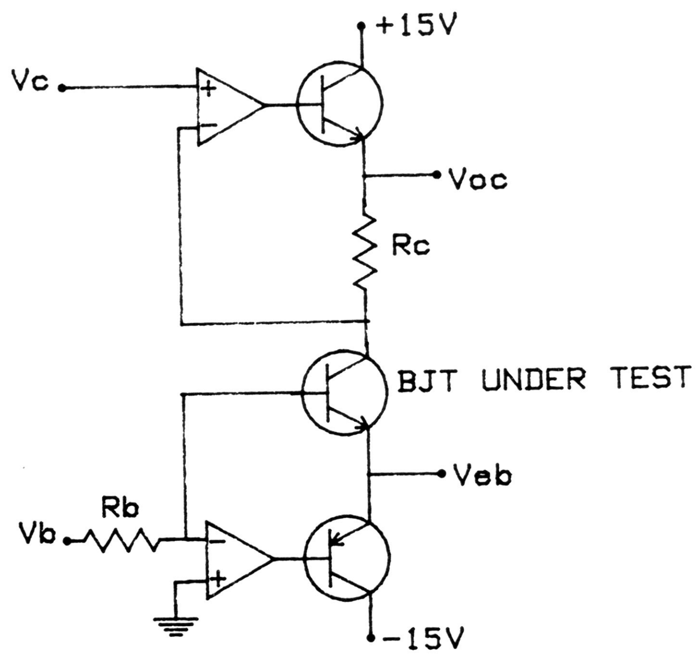

Figure 4. Experimental Setup

In line with the objective of determining the BJT parameters automatically, all the above processes were done under computer control via the HP 9845 and the HP Multiprogrammer's D/A, A/D, Relay Reedback and Resistance cards. The HP BASIC program written to set the proper voltages, make the proper connections and take the correct measurements is has been written and tested but the details of the program won't be discussed here.

E. Results and Conclusions

The results of this project up to this point are pretty well summarized by Fig. 5-8, especially Figure 8. All of these figures are based on measurements made on a 4401 transistor; Figure 5 and 6 show graphs of β_F vs I_C and β_R vs I_E respectively. Both exhibit the expected increase from an initially low value to a fairly constant value in a middle range which would then be followed by a roll off at higher values if the graphs extended that far. Figure 7 shows a plot of $\ln(I_C)$ vs V_{BE} for $V_{BC}=0$ and a linearization of this plot at low current levels; this linearization was used to find I_{SO} and V_A. A similar set of data which is not plotted was also used to calculate the V_A for this transistor. All of these measurements are summarized in Figure 8 which is a plot of I_C vs V_{CE} resulting from inserting the calculated parameters into the

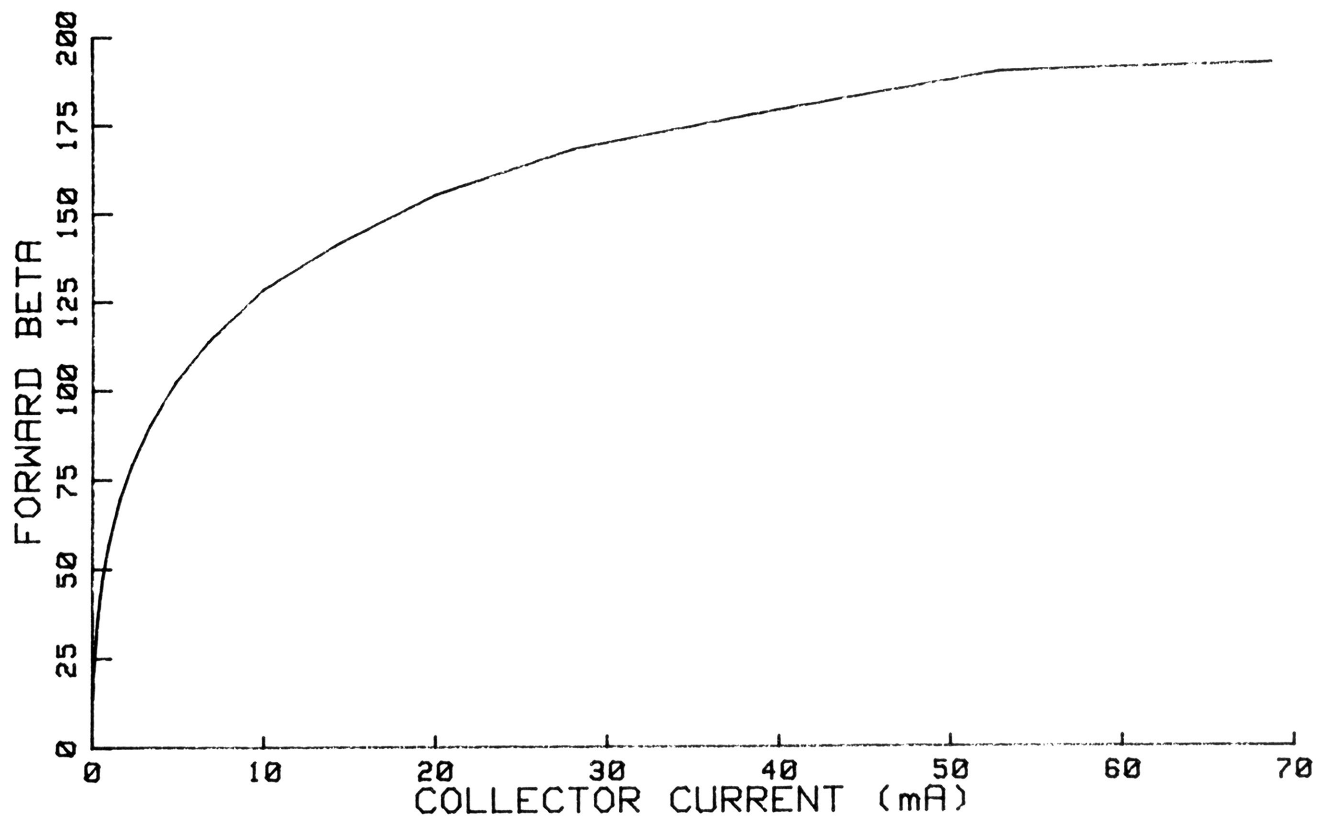

Figure 5. Forward Beta vs Collector Current measured experimentally

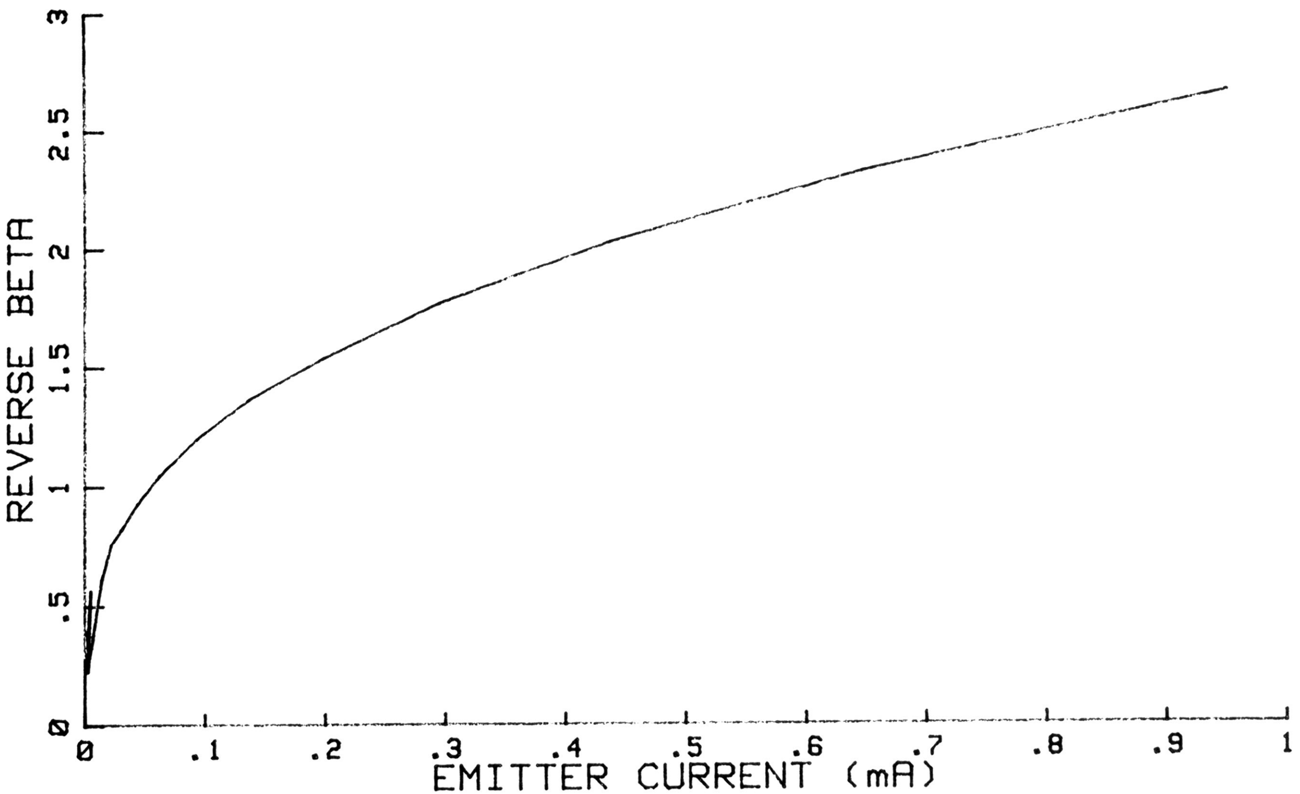

Figure 6. Reverse Beta vs Emitter Current measured experimentally

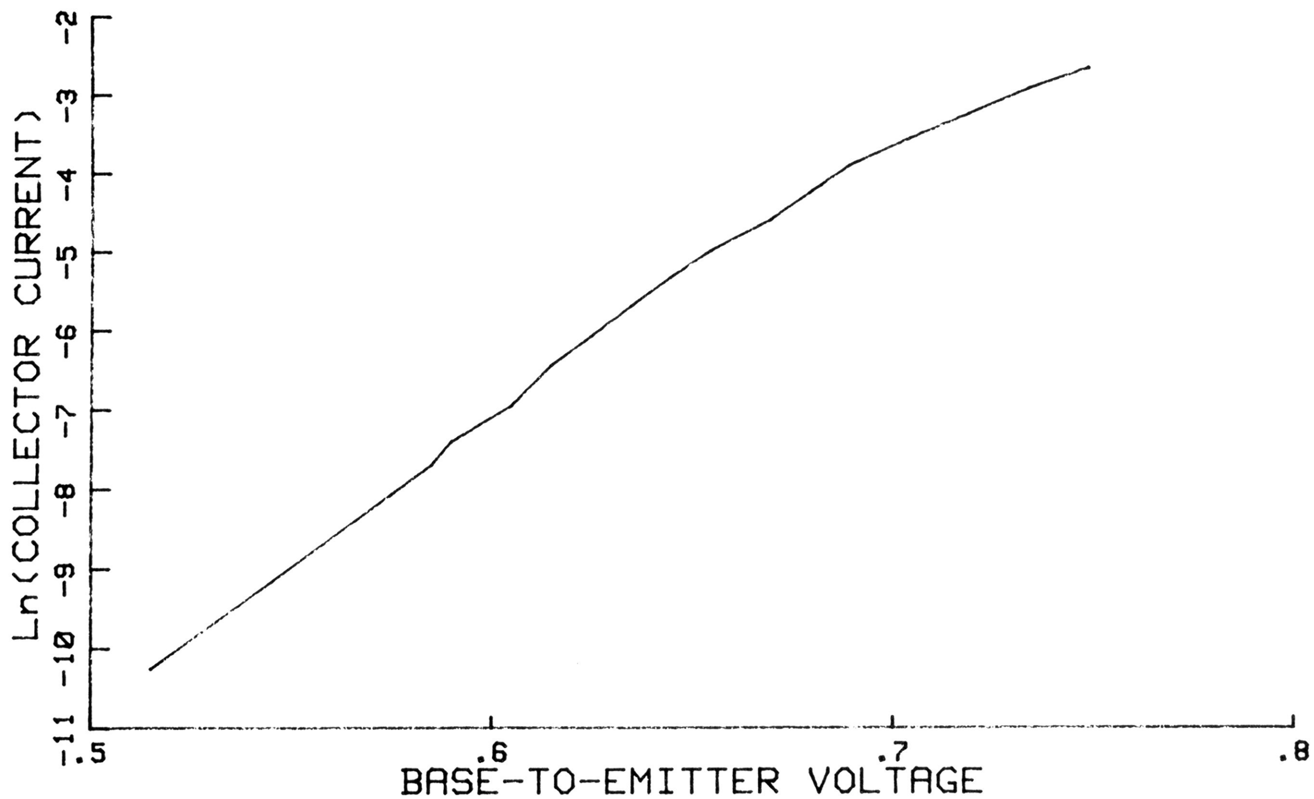

Figure 7. Ln(Collector Current) vs Base-to-Emitter Voltage measured experimentally

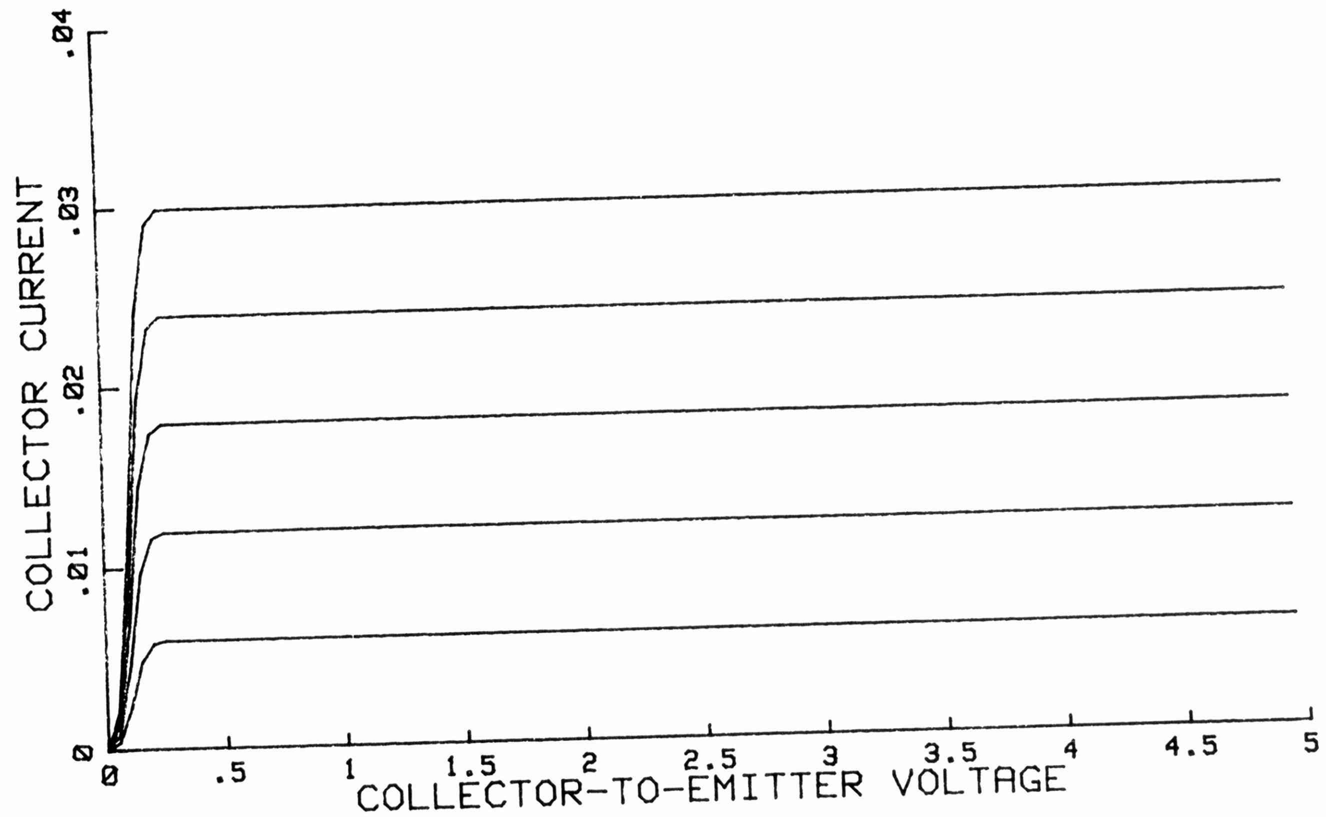

Figure 8. Predicted Collector Current vs Collector-to-Emitter Voltage based on experimentally determined parameters

Ebers-Moll equtaions. The β's which were used were found by the computer setting the transistor to a quiescient operating point specified by the operator.

While these figures illustrate how much has been accomplished, they also illustrate several things which have not been accomplished. The major objective which has not been completed is the comparison of the actual transistors performance vs it predicted perforamnce. The objective inthis area was to superimpose experimental plots of I_C vs V_{CE} over the those shown in Figure 8. A second objective was to study the high-current rolloff of ${}_F$ more closely; more specifically, if the high current portion of the $\ln(I_C)$ vs V_{BE} plot is linearized, the "knee current" of the device can be determined. This is the current where the linearizations of the low current and hogh current porions of the plot intersect; this point is a parameter in the Gummel-Poon model of the BJT which was introduced in 1970. Although the measurements have been made at the higher current levels, the linearization has not been done.

The final two unfinished objectives deal with documenting the program and standardizing its use. In process at the moment is an effort to develop a "USER" disk which will give a person who is not familiar with the programs defeloped in the IC testing area the ability to

use them with the minimum of effort. Both of the projects discussed in this report will be included in this documentation effort as it progresses. Also, since a program similar to the BJT parameter program described here has been developed for find MOSFET parameters, the final objective is to standardize any measurement, data manipulation and/or data storage techniques which the the two programs have in common in order to develop a standard format for use in any future efforts and to facilitate the future use and alteration of these programs.

References

[1] Model SP1-C High Speed Automatic Wafer Probe System, Pacific Western Systems, Inc., 1977

[2] J. J. Ebers and J. L. Moll, "Large-Signal Behavior of Junction Transistors," Proc.IRE, Vol. 42, pp. 1761-1772,December 1954.

[3] Ian Getreu,Modeling the Bipolar Transistor, Tektronix, Inc., Beaverton, Ore., 1976