INVESTIGATION OF FOUR CIRCUIT DESIGNS FOR MULTIVALUED LOGIC APPLICATIONS

A Senior Thesis

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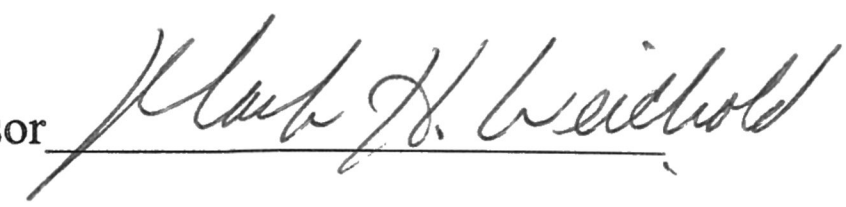
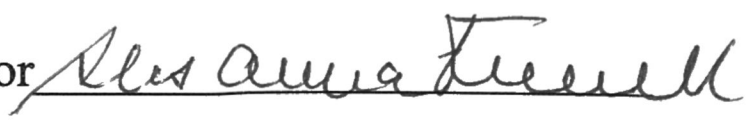
Fellows Advisor 

Honors Director 

Abstract

Investigation of Four Circuit Designs for Multivalued Logic Applications (April 1997)
Kenneth Chinchilla, Texas A&M University
Advisor: Dr. Mark H. Weichold

Multivalued logic (MVL) circuits display more than the two states (LOW and HIGH) exhibited by traditional logic circuits. A ternary logic circuit, for example, may contain states such as HIGH, MEDIUM, and LOW. The demands of low power loss and higher device speed have prompted circuit designers to consider MVL.

This thesis begins with a design that employs CMOS inverters (with different PMOS and NMOS threshold voltages) connected in parallel. The design was successfully simulated using PSPICE; the voltage transfer characteristics clearly show three states. HSPICE simulations using MOSIS parameters were not successful; three-state characteristics were not seen when using the identical circuit simulated by PSPICE. A discussion on the differences between PSPICE and HSPICE is included. Other circuit designs will also be analyzed including (1) a circuit that uses NMOS transistors to model the characteristics of switches; (2) a revised circuit that uses diode-connected transistors to replace resistors included in the previous design; and (3) a circuit that replaces two large resistances with two PMOS transistors. While the parallel-inverter design consists of four transistors (for three states), the other designs include circuits with (1) four resistors and two transistors; (2) two resistors and four transistors; and (3) six transistors. Simulations done using PSPICE and HSPICE software packages show promise for using the designs as MVL circuits.

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Background

Multivalued logic (MVL), as the name implies, exhibits more than the two states (LOW and HIGH) that are associated with the traditional binary logic. Ternary logic (three states) and quaternary (four states) logic circuits have been designed in the past ten to twelve years to execute operations that combine low power dissipation with high device speed [2]. Because of the possibility of expanding the functional complexity per unit area of silicon [5], circuit designers have paid much attention to MVL and what it offers. For one, MVL can provide accurate, higher speed arithmetic operations, greater density of information storage (by reducing the number of memory elements), and more efficient use of transmission lines [3].

To minimize the amount of power that may be lost, circuit designers can lower the supply voltage, minimize the capacitance due to wiring complexity, or reduce the quantity of active devices that perform a certain task [1]. Hanyu and Kameyama have done just that, using a multivalued MOS current-mode circuit to produce high-speed functions at a low-supply voltage. Mutoh, et al, [2] have demonstrated that it is possible to achieve a low-supply voltage, high-speed, low-power large scale integration operation using multithreshold-voltage CMOS circuit technology. Such a low-power design can find applications in cellular phones, lap top computers, and other such transportable equipment where smallness of devices and long battery life are key [2].

Research Objective

The objective of the research was to investigate parallel-connected inverters (with different threshold voltages) as a multivalued logic circuit. Specifically, the questions to be answered were:

1. What effects does changing the aspect ratios of the transistors have on the voltage transfer characteristics?
2. What is the upper bound on *n* such that *n* stable states result from *n-1* inverters?

An important first step was made by Dr. Weichold in the development of such a multivalued logic circuit, as simulated by PSPICE. The goal was to recreate the results and determine the feasibility of fabricating the circuit using MOSIS parameters. The rest of this thesis will discuss methodologies and results.

Motivation

Design 1 - Parallel Inverters

At Texas A&M, the proven benefits and advantages of multivalued logic have not gone unnoticed. Dr. Weichold has simulated an innovative circuit for obtaining multivalued logic by connecting CMOS inverters (with different PMOS and NMOS threshold voltages) in parallel.

A CMOS inverter consists of a PMOS and NMOS transistor connected as shown in Figure 1 below.

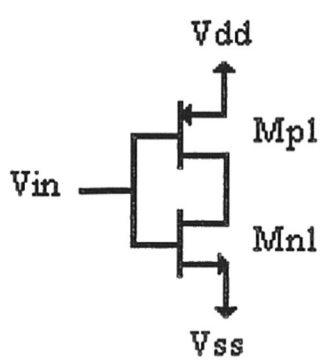

Figure 1. Basic CMOS Inverter Circuit.

If the input voltage is LOW (say 0 V) and V_{DD} is +5V, the n-channel transistor *Mn1* does not conduct since the voltage between gate and source (V_{GS}) is zero volts. (Note that ground is being referred to as V_{SS}.) The p-channel transistor *Mp1* **does** conduct since its V_{GS} is a large negative value (-5V.) Thus, *Mp1* presents only a small resistance between the power supply terminal and the output terminal, and V_{OUT} is 5V. If the input voltage is HIGH (say 5V) then *Mn1* is on since its V_{GS} is a large positive value (+5V.) Transistor *Mp1* is off since its V_{GS} is 0V. Thus, *Mn1* presents only a small resistance between the output terminal and V_{SS} ; the output voltage is 0V. The output vs. input characteristics of the basic CMOS inverter are shown in Figure A.1 in the appendix A, where the PSPICE circuit file may also be found.

Dr. Weichold has taken two basic inverters with different threshold voltages, connected the gates of the first inverter to the gates of the second, and tied the output of the first inverter to the output of the second. What results is a circuit that seems to display three state logic. The circuit is shown below in Figure 2.

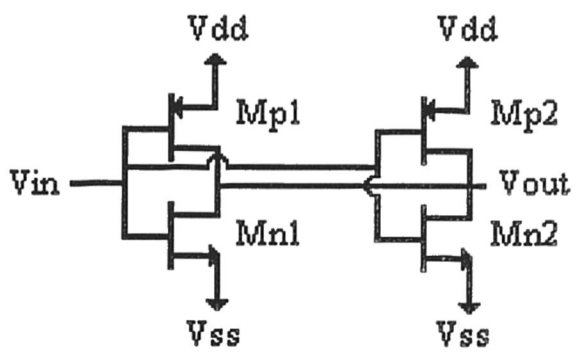

Figure 2. Three-State Logic Circuit.

This circuit was simulated using PSPICE. The plot of the voltage transfer characteristics (Appendix B) shows three distinct voltage ranges corresponding to three logic states.

According to research, such a circuit has never been used to generate multivalued logic. The motivation behind it is as follows. Figure 3 displays the IV characteristics of two n-channel enhancement-type MOSFETs with different threshold voltages.

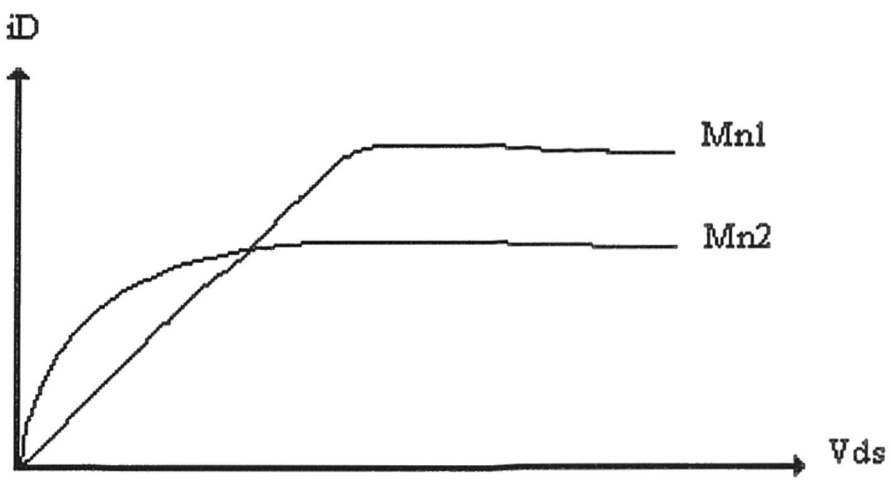

Figure 3. NMOS IV Characteristics (with different V_{Ts}).

It was thought that connecting two such transistors in parallel would result in transfer characteristics that looked like that of Figure 4 below.

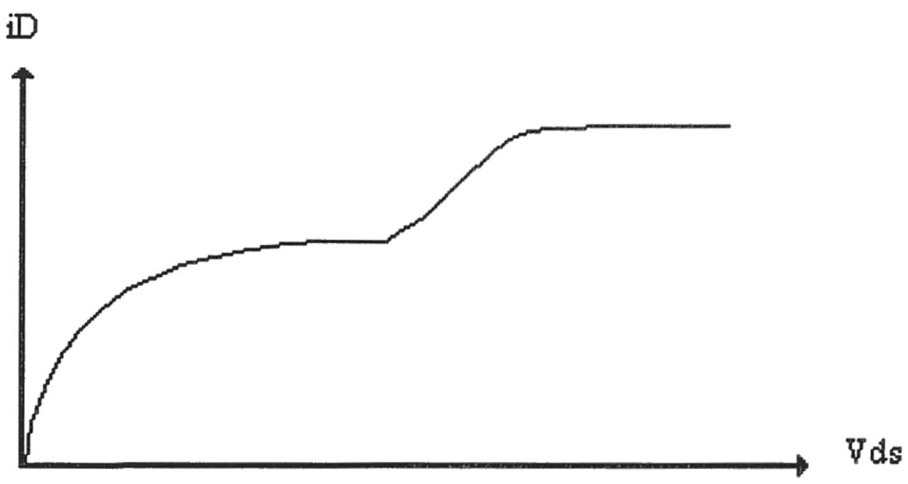

Figure 4. Combining two NMOS transistors with different V_{Ts}.

With similar reasoning applied to two p-channel enhancement-type MOSFETs, the next step was to use the NMOS transistors in conjunction with the PMOS transistors in such a way as to utilize the information given by the NMOS and PMOS IV transfer characteristics. Two basic CMOS inverters were connected in parallel with all gates and outputs tied together. What resulted was the three-state logic circuit successfully simulated by PSPICE (figure B.1 in Appendix B.)

Design 2 - Switches

The motivation for the second circuit design began with a study of the characteristics shown by switches. Figure 5 is the transfer characteristics of ideal three-state logic while Figure 6 is a circuit employing a combination of switches and resistors.

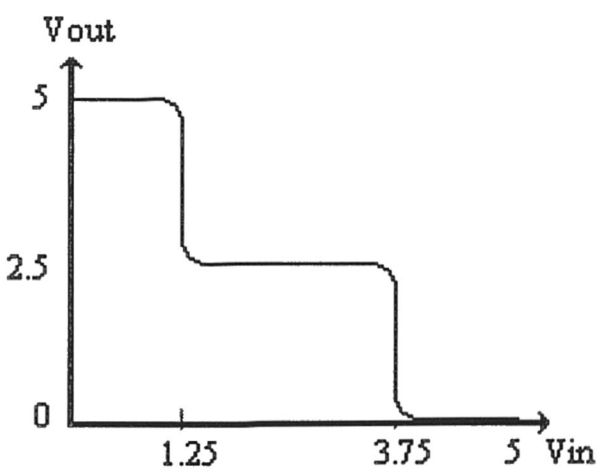

Figure 5. Transfer characteristics of ideal three-state logic.

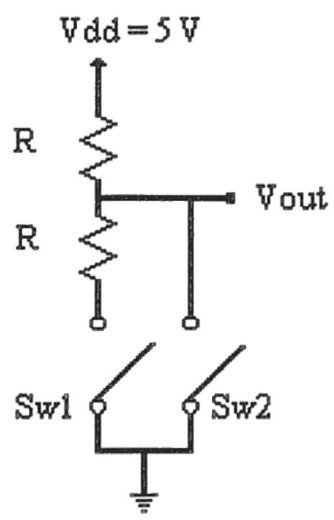

Figure 6. Switches in a circuit.

To achieve an output voltage of 5 volts for an input voltage range of 0 to 1.25 volts, both switches must be open. This way, $V_{OUT} = V_{DD}$. To achieve an output voltage range of 1.25 volts to 3.75 volts, switch 1 must be closed and switch 2 opened. This is a voltage divider:

$$V_{OUT} = R/(R+R) * V_{DD} = 1/2 * V_{DD}$$

Finally, to achieve an output voltage of 0 volts for an input voltage range of 3.5 volts to 5 volts, both switches must be closed. This creates a short circuit between V_{OUT} and ground, thus setting V_{OUT} to 0 volts.

Following the arguments of Sedra and Smith [4], switching behavior can be modeled with MOSFETs. The transistor in Figure 7 is controlled by the gate-source voltage, v_{GS}. When it is less than the threshold voltage V_T, the transistor does not conduct and the switch is open. The equivalent circuit is shown in Figure 8.

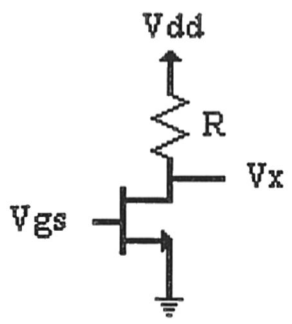

Figure 7. Circuit using NMOS transistor [4].

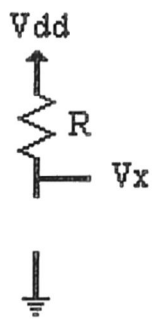

Figure 8. Equivalent circuit when switch is open [4].

When v_{GS} is greater than V_T, the transistor is on and operating in the linear region (Figure 9.) In the equivalent circuit (Figure 10), a small resistance r causes v_x to be small. This voltage is called the closure or on-voltage and the transistor can be thought of as modeling a closed switch.

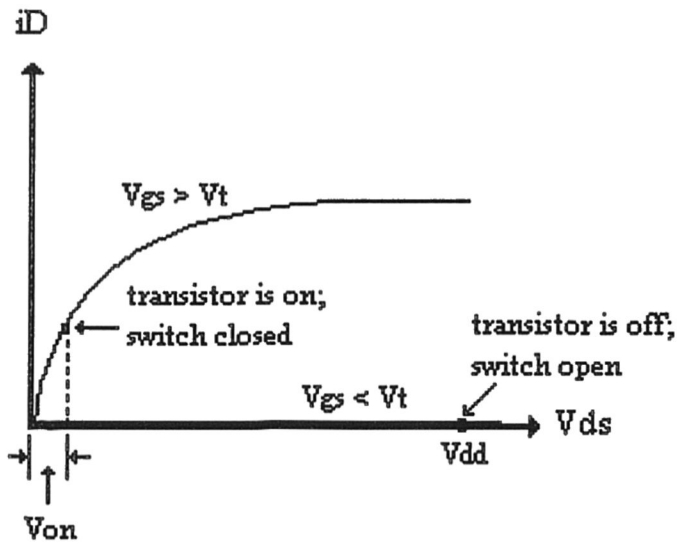

Figure 9. Operating points of the transistor [4].

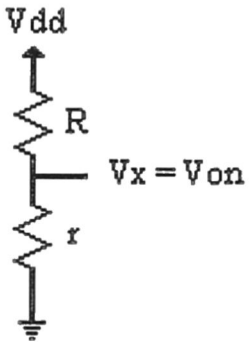

Figure 10. Equivalent circuit when switch is closed [4].

Initial Design - Parallel Inverters

After successfully demonstrating MVL with default PSPICE parameters, time was spent attempting to regenerate the three-state logic using MOSIS parameters. These are the parameter values used when the ultimate goal is the fabrication of a device. A complete substitution of MOSIS parameters for the PSPICE default parameters *did not* give us the output vs. input characteristics of MVL. MOSIS parameter values are too sensitive to their specific design constraints to be used without proper adjustments.

PSPICE parameters were then compared with MOSIS parameters and a new circuit file using a *combination* of the two sets of parameters was created. The new file consisted of all the default PSPICE parameters (which constituted the circuit displaying three-state logic) along with those parameters specific to *only* MOSIS. Running the simulation resulted in a convergence error; two or more interdependent parameters (such as substrate doping and threshold voltage) had conflicting values. Removing the substrate doping parameters solved the convergence problem but still did not demonstrate three-state logic.

Therefore, a different approach was tried. Instead of taking the default PSPICE parameters and adding them to the MOSIS parameters in the hopes of recreating MVL, the MOSIS parameters were added to the default PSPICE parameters with no duplication of values. Through much trial and error, two changes were discovered that could be made to the MOSIS parameters so as to display three-state logic. First, the zero bias threshold voltages (V_{TO}) was adjusted so that instead of

V_{TO} = -1.3970V for PMOS1 and PMOS2 and V_{TO} = -0.7698V for NMOS1 and NMOS2, the new values were -4V, 4V, -3V, 3V for PMOS1, NMOS1, PMOS2, and NMOS2 respectively. Next, a

drain-source shunt resistance (R_{DS}) of 444.4kΩ was added. Appendix C contains the output vs. input characteristics for this circuit, along with its PSPICE circuit file.

Because the source and body of all the FETs in the circuit are at the same potential ($V_{SB} = 0V$), the equation for threshold voltage

$$V_{TH} = V_{TO} + \gamma * [\ \sqrt{|-2\phi f + V_{SB}|} - \sqrt{|-2\phi f|}\ ]$$

where γ is the body-effect coefficient and ϕf is the Fermi level (a function of substrate doping) [4]

reduces to $V_{TH} = V_{TO}$. Thus, adjusting V_{TO} changes the location at which transitions occur in the output for a given input. In other words, adjusting the value of a given threshold voltage will determine at what point the transistor turns on.

The parameter R_{DS} represents the resistance seen between the drain and source of a transistor when operating in the saturation region for small drain-source voltage, v_{DS}. This resistance value is very high (about 10^{12} Ω) to prevent current conduction when v_{DS} is applied with no gate voltage present [4]. The amount of current being conducted from drain to source can thus be regulated by adjusting the R_{DS} parameter. This parameter is not part of the MOSIS model because HSPICE, a more robust software package than PSPICE, uses other parameters and their combinations to simulate the effect of drain-source shunt resistance.

It is with caution that the V_{TO} and R_{DS} changes to the MOSIS parameters are made. MOSIS is a VLSI fabrication service located at the University of Southern California's Information Sciences Institute. They have their own libraries of process parameters and generally will not modify them; uers design their circuits with MOSIS specifications in mind. Attempts to model

MVL using parallel inverters *without* making the above changes to MOSIS parameters have not been successful. Whether or not MOSIS accepts these changes remains to be seen.

HSPICE Simulation

Because HSPICE incorporates more sophisticated transistor models (more accurate, greater precision) a decision was made to simulate the parallel-inverter design with HSPICE in addition to previous PSPICE simulations. No changes were made to the circuit; it was simply run on a different software package. The results were quite different: the MVL characteristics ceased. As mentioned above, the R_{DS} parameter is not used in HSPICE. Perhaps modifying other parameters would have simulated the effect of drain-source shunt resistance and resulted in three-state logic. Already wary of making outright changes to the MOSIS model, no more parameters were modified. What *was* tried was adding finite resistors (444.4kΩ) between the source and drain of each transistor to simulate R_{DS}. The voltage transfer characteristics (Appendix D) clearly show three different states. However, fabricating such large resistances would be unrealistic. Although the exact mechanisms are not clear, it appears that the drain-source shunt resistance is the key to three-state logic using the parallel-inverters design. Further investigation needs to be made into simulating the parallel inverter MVL using MOSIS parameters and HSPICE.

Second Design - Using Switches

With transistors modeling switches, the next circuit devised was the following.

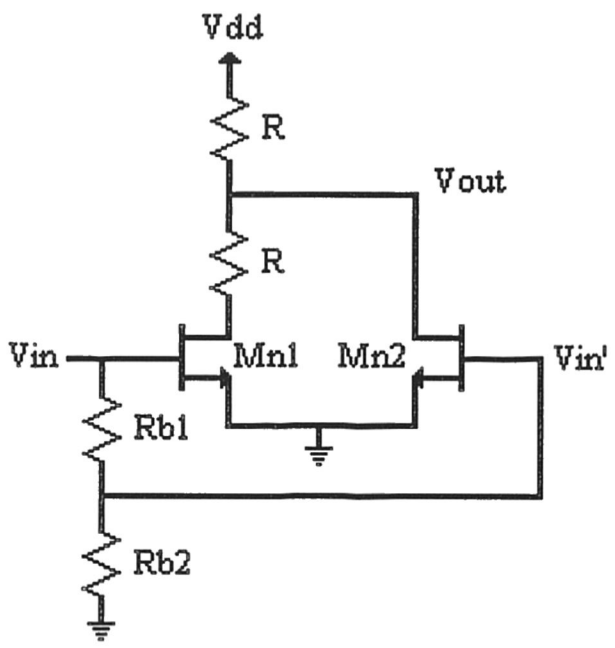

Figure 11. Circuit using transistors as switches to display three-state logic.

The elements R_{b1} and R_{b2} are resistors used to bias the transistor, constituting a voltage divider network, and ensuring that $V_{in} \neq V_{in}'$. When V_{in} is between 0V and V_t, both transistors are off and the output is HIGH. Transistor M_{n2} turns on when $V_{in} = V_t$ or $V_{in} * R_{b2}/(R_{b2} + R_{b1}) = V_t$. Thus, when the input voltage range is between V_t and $V_t * (R_{b2} + R_{b1})/ R_{b2}$, transistor M_{n1} will be on, while M_{n2} is off. We are left with a voltage divider network and an output of MIDDLE. When V_{in} is between $V_t * (R_{b2} + R_{b1})/ R_{b2}$ and V_{DD}, both transistors will be on and the output will be LOW. A summary is found in the Table 1 below.

V_{in} **Range**	M_{n1}	M_{n2}	**Output**
0 to V_t	off	off	HIGH
V_t to $V_t * (R_{b2} + R_{b1})/R_{b2}$	on	off	MIDDLE
$V_t * (R_{b2} + R_{b1})/R_{b2}$ to V_{DD}	on	on	LOW

Table 1. Summary of discussion.

Some time was spent fine tuning this circuit by varying the aspect ratios of the transistors. Drain current in both the saturation and linear regions is a function of the ratio of channel width to channel length. The transfer characteristics are shown in Figure 12 while the HSPICE circuit file can be found in Appendix E.

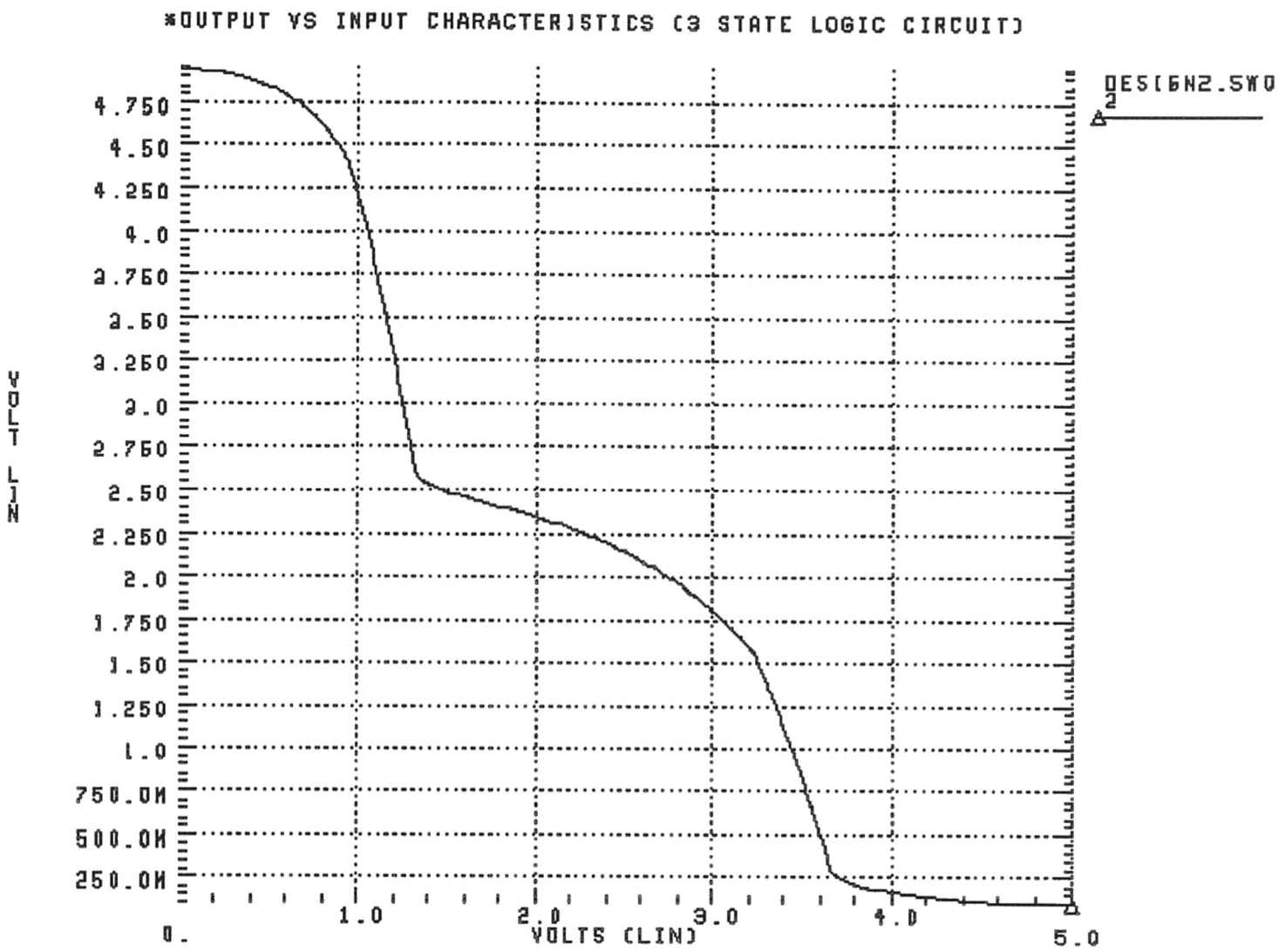

Figure 12. Three-state logic using four resistors and two transistors.

This is a good first step; the three-state logic is clearly visible. However, modifications must be made to eliminate the resistors. They take up much space on a substrate during the fabrication process.

Third Design - Two Resistors, Four Transistors

Because resistors are more costly to fabricate (in terms of size and space), the next design eliminated the biasing resistors with two diode-connected NMOS transistors. This configuration models a resistor with $r = 1/g_m$ where g_m is the MOSFET transconductance, defined as the ratio of signal current i_d to input signal v_{gs} [4]. The transconductance is also a function of the aspect ratio [$g_m = (\mu_n * C_{ox})(W/L)(V_{GS} - V_t)$] which can thus be varied to increase or decrease r. Figure 13 shows the new circuit while Figure 14 displays the transfer characteristics. The circuit file is in Appendix F.

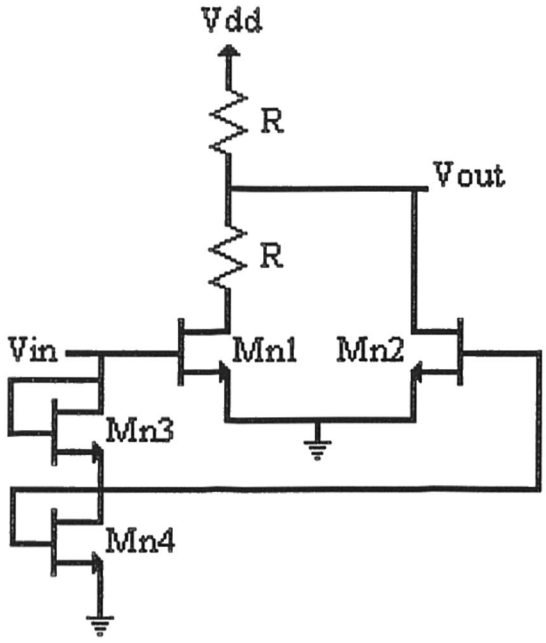

Figure 13. Modified three-state logic circuit with diode-connected transistors (M_{n3} and M_{n4}.)

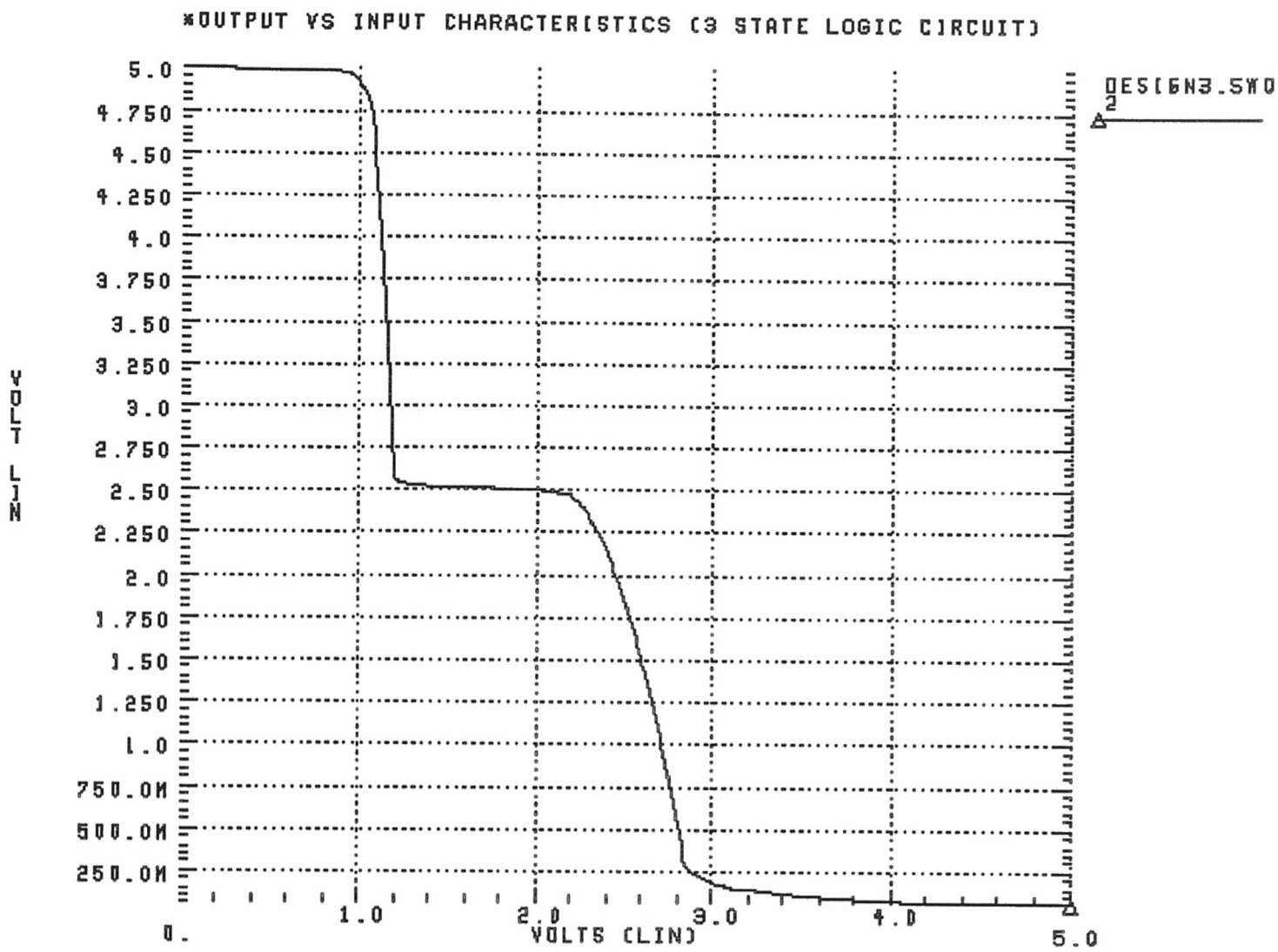

Figure 14. Three-state logic using two resistors and four transistors.

Fourth Design - Six Transistors

In the fourth design, the two remaining resistors were replaced with two PMOS transistors, properly tuned so that each models an equivalent resistance. Note the gate connections of the PMOS transistors in Figure 15 below.

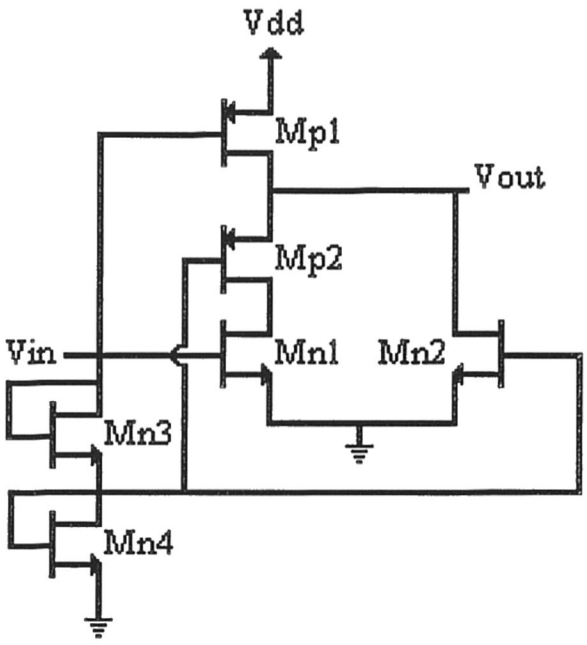

Figure 15. Modified three-state logic circuit with no resistors.

If M_{p2} and M_{p1} are both connected to V_{in}, then M_{p1} will always be in the linear region of operation in the MIDDLE region. In the MIDDLE region of operation, the circuit is reduced to that of Figure 16.

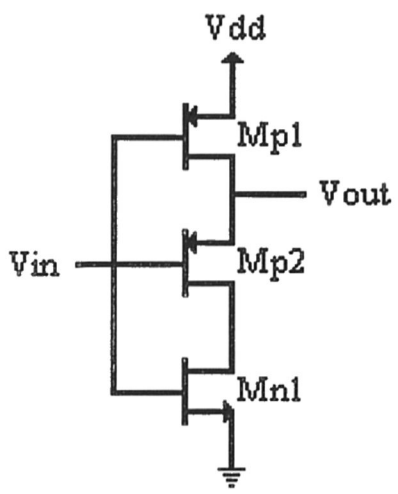

Figure 16. Equivalent circuit when in MIDDLE region of operation if V_{in} is connected to M_{p1} and M_{p2}.

With current traveling in the direction indicated, V_D will be higher than V_G. M_{p2} is in saturation because $|V_t| \geq v_{DS} - v_{GS}$. Transistor M_{p1} is in the linear region of operation because $v_{DS} - v_{GS} \geq |V_t|$ [4]. In the linear region, resistance will vary as the slope of the linear region varies (see Figure 17.) Thus, to ensure a constant response, M_{p1} should be operated in the saturation region. Figures 17 and 18 show the transfer characteristics for both cases. Note the response of the MIDDLE region when M_{p1} is operated in the saturated region (Figure 18.) The circuit files for the linear and non-linear cases are found in Appendices G and H respectively.

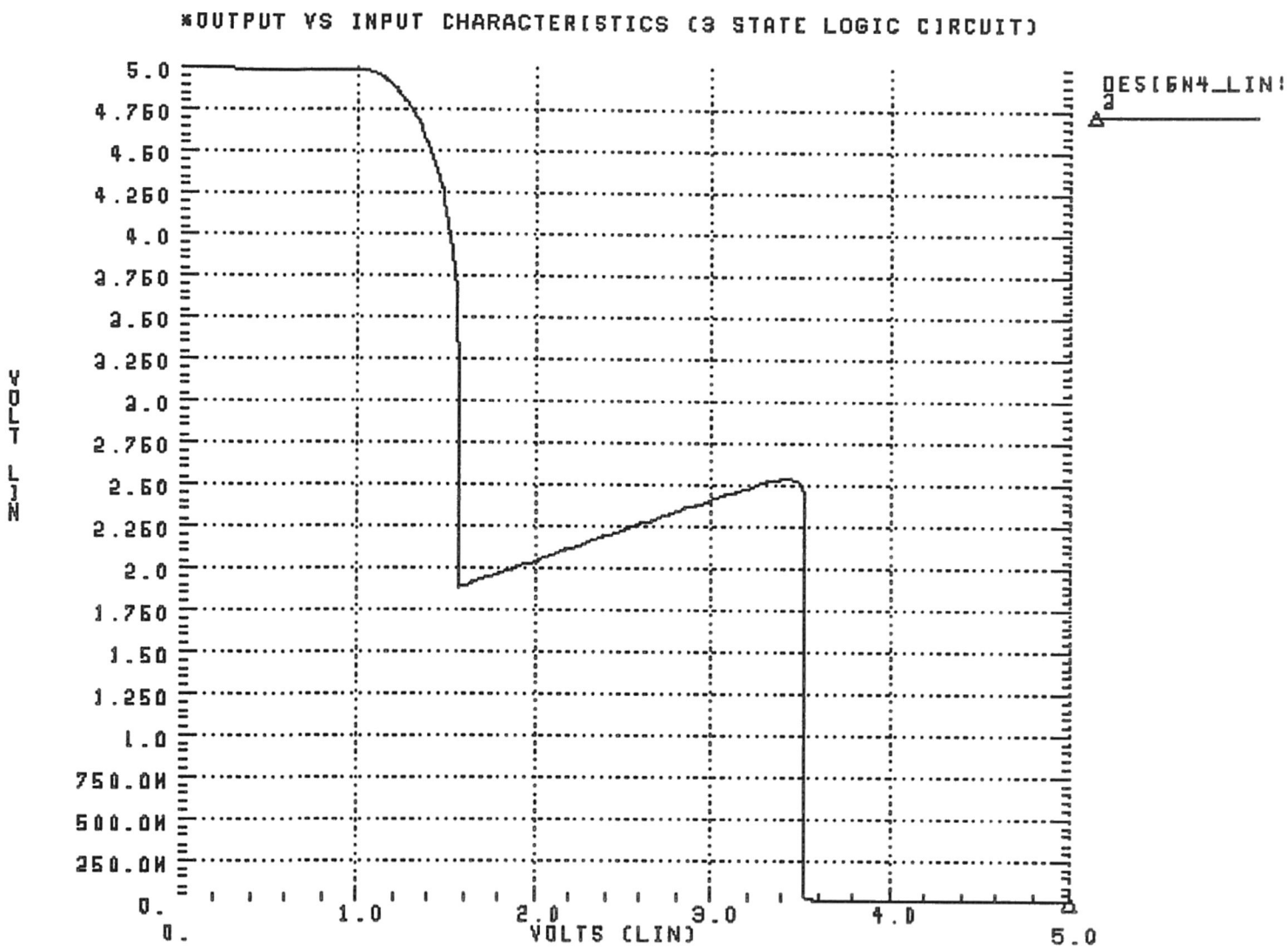

Figure 17. Linear response in the MIDDLE region.

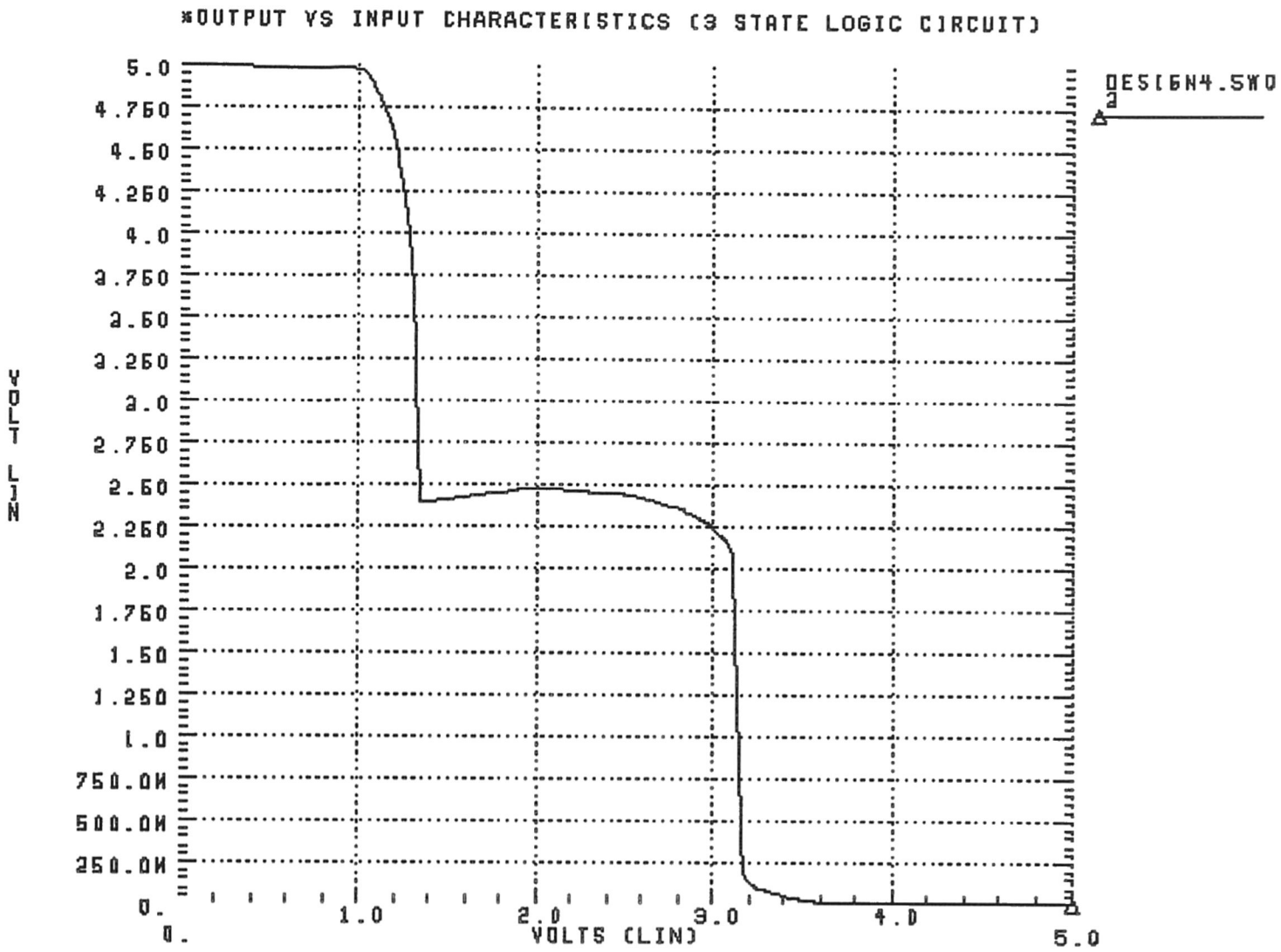

Figure 18. Three-state logic when using six transistors.

Results and Conclusions

The fourth design described above is the only one that displays MVL (as simulated by HSPICE) while containing only transistors. What's more, the Model Statement of the circuit file is made up entirely of MOSIS parameters. No modifications were made to them. This is an important result; there exists a much smaller chance of rejection of fabrication by MOSIS. An area of further study concerning this design is the diode-connected transistors (M_{n3} and M_{n4}.) This configuration uses a great deal of current and power. Future research may involve replacing these transistors with a current mirror featuring a high output resistance.

Although the parallel-inverters design exhibited MVL when simulated on PSPICE, it was only through adjusting the MOSIS parameters, and unless a strong argument can be made for changing the parameters, MOSIS generally does not allow the practice. However, it is believed that the parallel-inverters idea holds some promise as demonstrated by the PSPICE simulation. More experience is needed with HSPICE and MOSIS before further headway can be made.

It is well established that changing the aspect ratio of a transistor affects the MOSFET transconductance and the threshold voltage. This fact was employed in fine tuning the circuits of Design 2, Design 3, and Design 4. Changes were made to the aspect ratios of the transistors in the initial design, with little result. It appears that R_{DS} is the key to three-state logic in the parallel-inverters design, having more affect on the voltage transfer characteristics than the aspect ratios.

The research set out to determine the maximum number of stable states that would result from parallel inverters. However, no more than three states were studied because of the difficulty encountered in the parallel inverters design.

Ultimately, the goal of fully establishing parallel connected inverters employing transistors with different threshold voltages as a multivalued logic circuit was not met. Default PSPICE parameters gave three-state logic but MOSIS parameters did not. MOSIS does not include R_{DS} (which is not recognized by HSPICE) in its model statements while PSPICE does. However, three MVL circuits were demonstrated, the last one being the most attractive because it contained no resistors. The design was not finished early enough for fabrication but there is confidence that the circuit will be successful in displaying multivalued logic.

Acknowledgments

The author thanks Mr. Pinghai Hao, a Doctoral candidate at Texas A&M, for his contributions to the designs of the circuits containing transistors that model switches. The author further appreciates the help of Mr. Terry Mayhugh, a candidate for the Master of Science degree at Texas A&M, for his insight concerning HSPICE and PSPICE.

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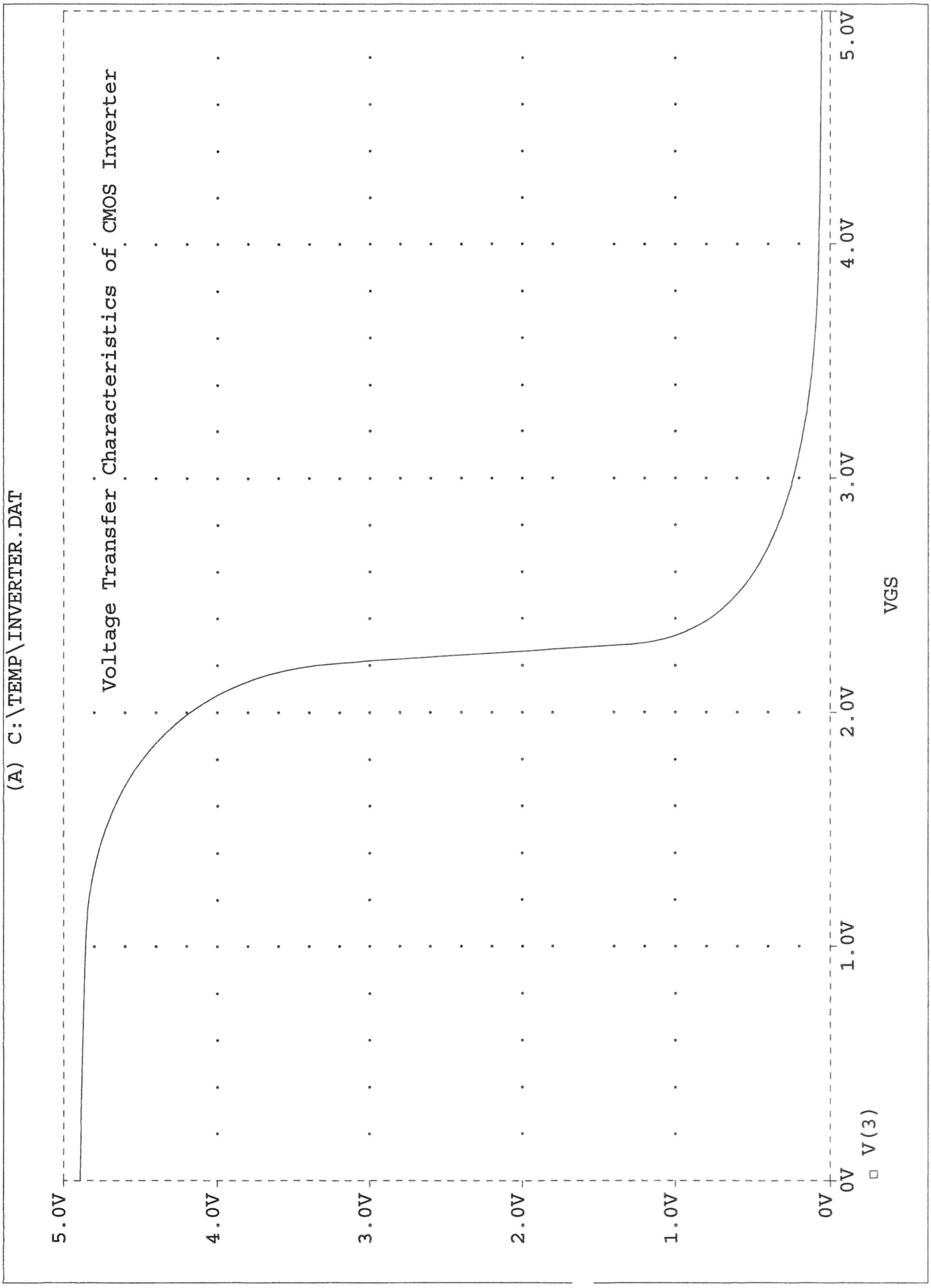
Appendix A

Figure A.1 - Output vs. Input Characteristics of CMOS Inverter

Circuit File A - PSPICE Circuit File for CMOS Inverter

Figure A.1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Voltage Transfer Characteristics of CMOS Inverter
5.0V
4.0V
3.0V
2.0V
1.0V
0V
0V
1.0V
2.0V
3.0V
4.0V
5.0V
VGS
V(3)

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*Output vs Input Characteristics (Inverter)
*Transistors
Mp 3 2 1 1 PMOS1
Mn 3 2 0 0 NMOS1

*Voltages
VDS 1 0 DC 5
VGS 2 0 DC 5

*Model Statements

.MODEL PMOS1 PMOS( Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+Vmax=0 Xj=0 Tox=100n Uo=300 Phi=.6 Rs=70.6m Kp=10.15u W=5u L=2u
+Vto=-1 Rd=60.66m Rds=444.4K Cbd=2.141n Pb=.8 Mj=.5 Fc=.5
+Cgso=877.2p Cgdo=369.3p Rg=.811 Is=52.23E-18 N=2 Tt=140n)

.MODEL NMOS1 NMOS( Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+Vmax=0 Xj=0 Tox=100n Uo=600 Phi=.6 Rs=1.624m Kp=20.53u W=5u L=2u
+Vto=1 Rd=1.031m Rds=444.4K Cbd=3.229n Pb=.8 Mj=.5 Fc=.5
+Cgso=9.027n Cgdo=1.679n Rg=13.89 Is=194E-18 N=1 Tt=288n)

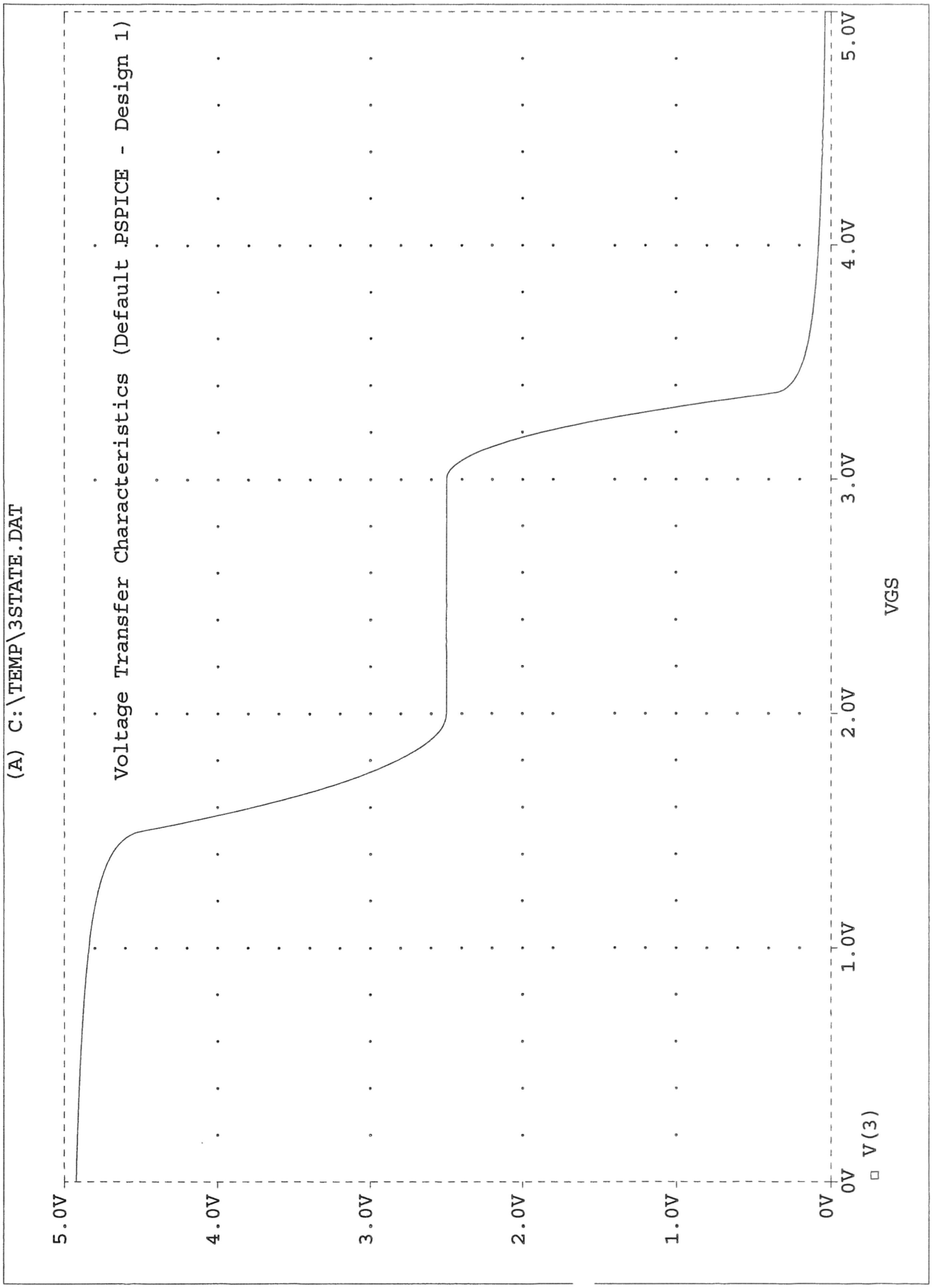
*Analysis and Output
.DC LIN VGS 0 5 0.01
.PROBE
.END
```

Appendix B

Figure B.1 - Three-State Logic Using Default PSPICE Parameters
(Initial Design)

Circuit File B - PSPICE Circuit File for Three-State Logic Circuit

Figure B.1


(A) C:\TEMP\3STATE.DAT
Voltage Transfer Characteristics (Default .PSPICE - Design 1)
5.0V
4.0V
3.0V
2.0V
1.0V
0V
0V
1.0V
2.0V
3.0V
4.0V
5.0V
VGS
V(3)

```
*Output vs Input Characteristics (3 State Logic Circuit)
*Circuit File B - Default PSPICE Parameters (Initial Design)
*Transistors
Mp1 3 2 1 1 PMOS1
Mn1 3 2 0 0 NMOS1
Mp2 3 2 1 1 PMOS2
Mn2 3 2 0 0 NMOS2


*Voltages
VDS 1 0 DC 5
VGS 2 0 DC 5

*Model Statements

.MODEL PMOS1 PMOS( Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+Vmax=0 Xj=0 Tox=100n Uo=300 Phi=.6 Rs=70.6m Kp=10.15u W=6u L=1u
+Vto=-3.0 Rd=60.66m Rds=444.4K Cbd=2.141n Pb=.8 Mj=.5 Fc=.5
+Cgso=877.2p Cgdo=369.3p Rg=.811 Is=52.23E-18 N=2 Tt=140n)

.MODEL NMOS1 NMOS( Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+Vmax=0 Xj=0 Tox=100n Uo=600 Phi=.6 Rs=1.624m Kp=20.53u W=6u L=1u
+Vto=3.0 Rd=1.031m Rds=444.4K Cbd=3.229n Pb=.8 Mj=.5 Fc=.5
+Cgso=9.027n Cgdo=1.679n Rg=13.89 Is=194E-18 N=1 Tt=288n)

.MODEL PMOS2 PMOS( Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+Vmax=0 Xj=0 Tox=100n Uo=300 Phi=.6 Rs=70.6m Kp=10.15u W=8u L=1u
+Vto=-3.0 Rd=60.66m Rds=444.4K Cbd=2.141n Pb=.8 Mj=.5 Fc=.5
+Cgso=877.2p Cgdo=369.3p Rg=.811 Is=52.23E-18 N=2 Tt=140n)

.MODEL NMOS2 NMOS( Level=3 Gamma=0 Delta=0 Eta=0 Theta=0 Kappa=0
+Vmax=0 Xj=0 Tox=100n Uo=600 Phi=.6 Rs=1.624m Kp=20.53u W=8u L=1u
+Vto=3.0 Rd=1.031m Rds=444.4K Cbd=3.229n Pb=.8 Mj=.5 Fc=.5
+Cgso=9.027n Cgdo=1.679n Rg=13.89 Is=194E-18 N=1 Tt=288n)

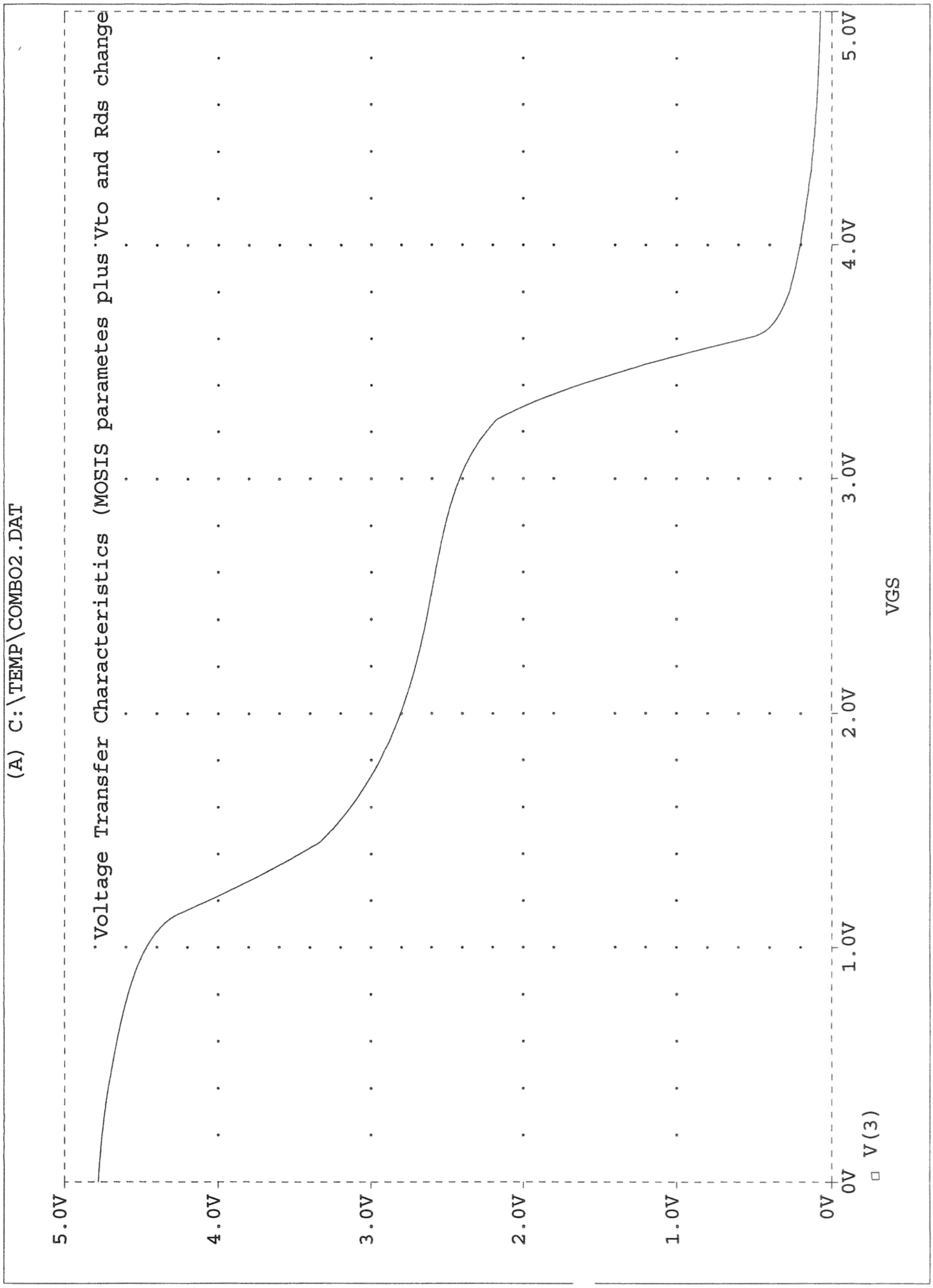

*Analysis and Output
.DC LIN VGS 0 5 0.01
.PROBE
.END
```

Appendix C

Figure C.1 - Three-State Logic Using Default PSPICE Parameters and R_{DS} and V_{TO} Changes

Circuit File C - PSPICE Circuit File for Three-State Logic Circuit

Figure C.1


(A) C:\TEMP\COMBO2.DAT
Voltage Transfer Characteristics (MOSIS parametes plus Vto and Rds change
5.0V
4.0V
3.0V
2.0V
1.0V
0V
0V
1.0V
2.0V
3.0V
4.0V
5.0V
VGS
V(3)

*Output vs Input Characteristics (3 State Logic Circuit)
*Circuit File C - Adjusting V_{TO} and R_{DS}
*Transistors
Mp1 3 2 1 1 PMOS1
Mn1 3 2 0 0 NMOS1
Mp2 3 2 1 1 PMOS2
Mn2 3 2 0 0 NMOS2

*Voltages
VDS 1 0 DC 5
VGS 2 0 DC 5

*Model Statements
.MODEL PMOS1 PMOS(Level=3 Gamma=0.4262 Delta=1.758
+Eta=0.1231 Theta=0.5125 Kappa=4.035 Vmax=1E+6 Xj=0.2u
+Tox=1.74E-08 Uo=314.2 Phi=.6 Kp=6.2355E-05
+Vto=-4 Rds=444.4K Pb=.85 Mj=.5081
+Cgso=6.0847E-12 Cgdo=6.0847E-12
+LD=2.0440E-09 RSH=9.7950E+00 NFS=2.4780E+13
+CGBO=4.8708E-10 CJ=5.5793E-04 CJSW=1.0802E-10
+MJSW=0.281913 TPG=-1 NSUB=2.1550E+16)

.MODEL NMOS1 NMOS(Level=3 Gamma=0.6022 Delta=1.104
+Eta=0.04361 Theta=0.1264 Kappa=0.1029 Vmax=1.884E+5 Xj=0.2u
+Tox=1.74E-08 Uo=629.5 Phi=.6 Kp=1.2493E-04
+Vto=4 Rds=444.4K Pb=.8 Mj=1.0432
+Cgso=2.8450E-11 Cgdo=2.8450E-11
+LD=9.5570E-09 RSH=1.1000E+01 NFS=1.0280E+13
+CGBO=4.4870E-10 CJ=2.5574E-04 CJSW=5.3595E-10
+MJSW=0.301319 TPG=1 NSUB=4.3030E+16)

.MODEL PMOS2 PMOS(Level=3 Gamma=0.4262 Delta=1.758
+Eta=0.1231 Theta=0.5125 Kappa=4.035 Vmax=1E+6 Xj=0.2u
+Tox=1.74E-08 Uo=314.2 Phi=.6 Kp=6.2355E-05
+Vto=-3 Rds=444.4K Pb=.85 Mj=.5081
+Cgso=6.0847E-12 Cgdo=6.0847E-12
+LD=2.0440E-09 RSH=9.7950E+00 NFS=2.4780E+13
+CGBO=4.8708E-10 CJ=5.5793E-04 CJSW=1.0802E-10
+MJSW=0.281913 TPG=-1 NSUB=2.1550E+16)

.MODEL NMOS2 NMOS(Level=3 Gamma=0.6022 Delta=1.104
+Eta=0.04361 Theta=0.1264 Kappa=0.1029 Vmax=1.884E+5 Xj=0.2u
+Tox=1.74E-08 Uo=629.5 Phi=.6 Kp=1.2493E-04
+Vto=3 Rds=444.4K Pb=.8 Mj=1.0432

```
+Cgso=2.8450E-11 Cgdo=2.8450E-11
+LD=9.5570E-09 RSH=1.1000E+01 NFS=1.0280E+13
+CGBO=4.4870E-10 CJ=2.5574E-04 CJSW=5.3595E-10
+MJSW=0.301319 TPG=1 NSUB=4.3030E+16)

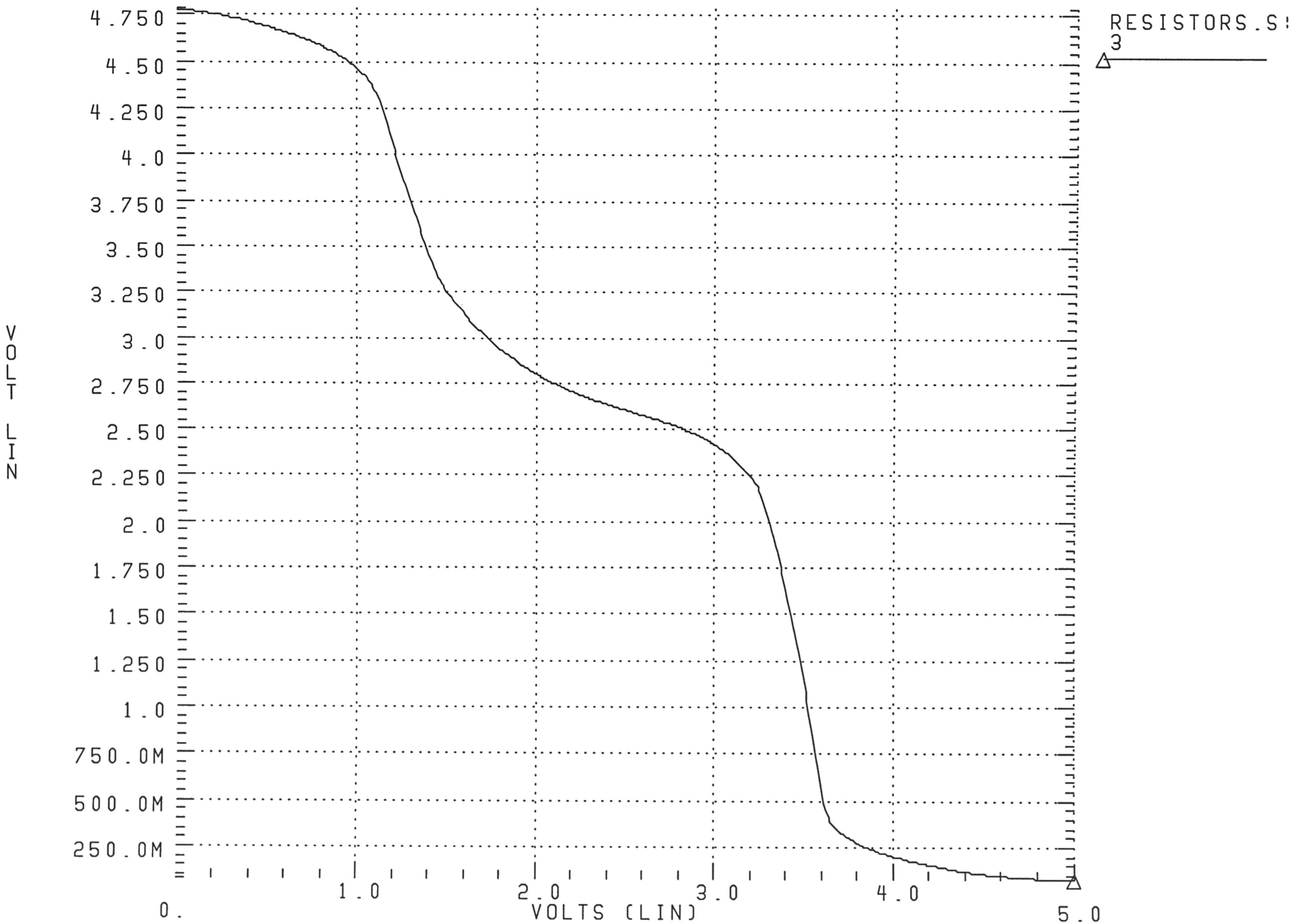
*Analysis and Output
.DC LIN VGS 0 5 0.01
.PROBE
.END
```

Appendix D

Figure D.1 - Three-State Logic (Initial Design)
Using Finite Resistors to Model R_{DS}

Circuit File D - HSPICE Circuit File for Three-State Logic Circuit

*OUTPUT VS INPUT CHARACTERISTICS (3 STATE LOGIC CIRCUIT) FIGURE D.1



```
*Output vs Input Characteristics (3 State Logic Circuit)
*Circuit File D - Using Finite Resistors to Model Rds

*Transistors
.options post

Mp1 3 2 1 1 PMOS1
Mn1 3 2 0 0 NMOS1
Mp2 3 2 1 1 PMOS2
Mn2 3 2 0 0 NMOS2

*Resistors
Rp1 1 3 444.4K
Rp2 1 3 444.4K
Rn1 3 0 444.4K
Rn2 3 0 444.4K

*Voltages
VDS 1 0 DC 5
VGS 2 0 DC 5

*Model Statements
.MODEL PMOS1 PMOS( Level=3 Gamma=0.4262 Delta=1.758
+Eta=0.1231 Theta=0.5125 Kappa=4.035 Vmax=1E+6 Xj=0.2u
+Tox=1.74E-08 Uo=314.2 Phi=.6 Kp=6.2355E-05
+Vto=-4 Pb=.85 Mj=.5081
+Cgso=6.0847E-12 Cgdo=6.0847E-12
+LD=2.0440E-09 RSH=9.7950E+00 NFS=2.4780E+13
+CGBO=4.8708E-10 CJ=5.5793E-04 CJSW=1.0802E-10
+MJSW=0.281913 TPG=-1 NSUB=2.1550E+16)

.MODEL NMOS1 NMOS( Level=3 Gamma=0.6022 Delta=1.104
+Eta=0.04361 Theta=0.1264 Kappa=0.1029 Vmax=1.884E+5 Xj=0.2u
+Tox=1.74E-08 Uo=629.5 Phi=.6 Kp=1.2493E-04
+Vto=4 Pb=.8 Mj=1.0432
+Cgso=2.8450E-11 Cgdo=2.8450E-11
+LD=9.5570E-09 RSH=1.1000E+01 NFS=1.0280E+13
+CGBO=4.4870E-10 CJ=2.5574E-04 CJSW=5.3595E-10
+MJSW=0.301319 TPG=1 NSUB=4.3030E+16)

.MODEL PMOS2 PMOS( Level=3 Gamma=0.4262 Delta=1.758
+Eta=0.1231 Theta=0.5125 Kappa=4.035 Vmax=1E+6 Xj=0.2u
+Tox=1.74E-08 Uo=314.2 Phi=.6 Kp=6.2355E-05
+Vto=-3 Pb=.85 Mj=.5081
+Cgso=6.0847E-12 Cgdo=6.0847E-12
```

```
+LD=2.0440E-09 RSH=9.7950E+00 NFS=2.4780E+13
+CGBO=4.8708E-10 CJ=5.5793E-04 CJSW=1.0802E-10
+MJSW=0.281913 TPG=-1 NSUB=2.1550E+16)

.MODEL NMOS2 NMOS( Level=3 Gamma=0.6022 Delta=1.104
+Eta=0.04361 Theta=0.1264 Kappa=0.1029 Vmax=1.884E+5 Xj=0.2u
+Tox=1.74E-08 Uo=629.5 Phi=.6 Kp=1.2493E-04
+Vto=3 Pb=.8 Mj=1.0432
+Cgso=2.8450E-11 Cgdo=2.8450E-11
+LD=9.5570E-09 RSH=1.1000E+01 NFS=1.0280E+13
+CGBO=4.4870E-10 CJ=2.5574E-04 CJSW=5.3595E-10
+MJSW=0.301319 TPG=1 NSUB=4.3030E+16)

*Analysis and Output
.DC  VGS 0 5 0.01
.probe
.END
```

Appendix E

Circuit File E - HSPICE Circuit File for Three-State Logic Circuit (Second Design)

```
*Output vs Input Characteristics (3 State Logic Circuit)
*Circuit File E - Design2.sp

*Transistors
Mn1 3 4 0 0 NMOS1 l=1u w=1u
Mn2 2 5 0 0 NMOS1 l=2.5u w=9u

*Resistors
R1 1 2 175k
R2 2 3 175k
R3 4 5 2k
R4 5 0 0.9k

*Voltages
Vin 4 0 DC 5
Vdd 1 0 DC 5

*Model Statements

.MODEL NMOS1 NMOS( Level=3 Gamma=0.6022 Delta=1.104
+Eta=0.04361 Theta=0.1264 Kappa=0.1029 Vmax=1.884E+5 Xj=0.2u
+Tox=1.74E-08 Uo=629.5 Phi=.6 Kp=1.2493E-04
+Vto=0.7698 Pb=.8 Mj=1.0432
+Cgso=2.8450E-11 Cgdo=2.8450E-11
+LD=9.5570E-09 RSH=1.1000E+01 NFS=1.0280E+13
+CGBO=4.4870E-10 CJ=2.5574E-04 CJSW=5.3595E-10
+MJSW=0.301319 TPG=1 NSUB=4.3030E+16)

*Analysis and Output
.options post
.DC Vin 0 5 0.01
.END
```

Appendix F

Circuit File F - HSPICE Circuit File for Three-State Logic Circuit (Third Design)

```
*Output vs Input Characteristics (3 State Logic Circuit)
*Circuit File F - Design3.sp

*Transistors
Mn1 3 4 0 0 NMOS1 l=8u w=1.8u
Mn2 2 5 0 0 NMOS1 l=10u w=0.8u
Mn3 4 4 5 5 NMOS1 l=4u w=1.5u
Mn4 5 5 0 0 NMOS1 l=9u w=1.5u


*Resistors
R1 1 2 10000k
R2 2 3 10000k

*Voltages
Vin 4 0 DC 5
Vdd 1 0 DC 5


*Model Statements
.MODEL NMOS1 NMOS(LEVEL=3 PHI=0.700000 TOX=2.3600E-08 XJ=0.200000U TPG=1
+ VTO=0.9596 DELTA=1.1290E+00 LD=8.4520E-08 KP=7.9349E-05
+ UO=542.3 THETA=9.6770E-02 RSH=3.1930E+01 GAMMA=0.9161
+ NSUB=5.4130E+16 NFS=6.3600E+11 VMAX=2.1470E+05 ETA=5.8910E-02
+ KAPPA=1.7800E-01 CGDO=1.8550E-10 CGSO=1.8550E-10
+ CGBO=2.6519E-10 CJ=4.970E-04 MJ=0.4580 CJSW=4.400E-10
+ MJSW=0.56800 PB=0.9900000)


*Analysis and Output
.options post
.DC Vin 0 5 0.01
.END
```

Appendix G

Circuit File G - HSPICE Circuit File for Three-State Logic Circuit
(Fourth Design with MIDDLE Region having Linear Response)

```
*Output vs Input Characteristics (3 State Logic Circuit)
*Circuit File G - Design4_lin.sp

*Transistors
Mp1 3 2 1 1 PMOS1 l=10u w=1u
Mp2 4 6 3 3 PMOS1 l=1u w=5u
Mn1 4 2 0 0 NMOS1 l=5u w=2u
Mn2 3 5 0 0 NMOS1 l=5u w=40u
Mn3 2 2 5 5 NMOS1 l=5u w=1u
Mn4 5 5 0 0 NMOS1 l=1u w=50u
Mn5 2 2 6 6 NMOS1 l=1u w=1u
Mn6 6 6 0 0 NMOS1 l=1u w=1u


*Voltages
Vin 2 0 DC 5
Vdd 1 0 DC 5


*Model Statements
.MODEL NMOS1 NMOS(LEVEL=3 PHI=0.700000 TOX=2.3600E-08 XJ=0.200000U TPG=1
+ VTO=0.9596 DELTA=1.1290E+00 LD=8.4520E-08 KP=7.9349E-05
+ UO=542.3 THETA=9.6770E-02 RSH=3.1930E+01 GAMMA=0.9161
+ NSUB=5.4130E+16 NFS=6.3600E+11 VMAX=2.1470E+05 ETA=5.8910E-02
+ KAPPA=1.7800E-01 CGDO=1.8550E-10 CGSO=1.8550E-10
+ CGBO=2.6519E-10 CJ=4.970E-04 MJ=0.4580 CJSW=4.400E-10
+ MJSW=0.56800 PB=0.9900000)

.MODEL PMOS1 PMOS(LEVEL=3 PHI=0.700000 TOX=2.3600E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8732 DELTA=2.4370E+00 LD=9.0920E-10 KP=2.2021E-05
+ UO=150.5 THETA=6.1580E-02 RSH=1.3780E+02 GAMMA=0.4539
+ NSUB=1.3290E+16 NFS=5.9090E+11 VMAX=1.1460E+05 ETA=2.8630E-02
+ KAPPA=8.0160E+00 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=2.6519E-10 CJ=4.5100E-04 MJ=0.5220 CJSW=4.2500E-10
+ MJSW=0.3210 PB=0.990000)


*Analysis and Output
.options post
.DC Vin 0 5 0.01
.END
```

Appendix H

Circuit File H - HSPICE Circuit File for Three-State Logic Circuit
(Fourth Design with MIDDLE Region having Non-Linear Response)

```
*Output vs Input Characteristics (3 State Logic Circuit)
*Circuit File H - Design4.sp

*Transistors
Mp1 3 2 1 1 PMOS1 l=1u w=1u
Mp2 4 5 3 3 PMOS1 l=1u w=5u
Mn1 4 2 0 0 NMOS1 l=5u w=50u
Mn2 3 5 0 0 NMOS1 l=10u w=40u
Mn3 2 2 5 5 NMOS1 l=5u w=10u
Mn4 5 5 0 0 NMOS1 l=1u w=10u


*Voltages
Vin 2 0 DC 5
Vdd 1 0 DC 5


*Model Statements
.MODEL NMOS1 NMOS(LEVEL=3 PHI=0.700000 TOX=2.3600E-08 XJ=0.200000U TPG=1
+ VTO=0.9596 DELTA=1.1290E+00 LD=8.4520E-08 KP=7.9349E-05
+ UO=542.3 THETA=9.6770E-02 RSH=3.1930E+01 GAMMA=0.9161
+ NSUB=5.4130E+16 NFS=6.3600E+11 VMAX=2.1470E+05 ETA=5.8910E-02
+ KAPPA=1.7800E-01 CGDO=1.8550E-10 CGSO=1.8550E-10
+ CGBO=2.6519E-10 CJ=4.970E-04 MJ=0.4580 CJSW=4.400E-10
+ MJSW=0.56800 PB=0.9900000)

.MODEL PMOS1 PMOS(LEVEL=3 PHI=0.700000 TOX=2.3600E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8732 DELTA=2.4370E+00 LD=9.0920E-10 KP=2.2021E-05
+ UO=150.5 THETA=6.1580E-02 RSH=1.3780E+02 GAMMA=0.4539
+ NSUB=1.3290E+16 NFS=5.9090E+11 VMAX=1.1460E+05 ETA=2.8630E-02
+ KAPPA=8.0160E+00 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=2.6519E-10 CJ=4.5100E-04 MJ=0.5220 CJSW=4.2500E-10
+ MJSW=0.3210 PB=0.990000)


*Analysis and Output
.options post
.DC Vin 0 5 0.01
.END
```