

**AMORPHOUS SILICON THIN FILM TRANSISTOR
AS NONVOLATILE MEMORY DEVICE**

A Dissertation

by

HELINDA NOMINANDA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

August 2008

Major Subject: Chemical Engineering

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Chair of Committee,	Yue Kuo
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ABSTRACT

Amorphous Silicon Thin Film Transistor as Nonvolatile Memory Device.

(August 2008)

Helinda Nominanda, B.S.; M.S., Texas A&M University

Chair of Advisory Committee: Dr. Yue Kuo

n-channel and p-channel amorphous-silicon thin-film transistors (a-Si:H TFTs) with copper electrodes prepared by a novel plasma etching process have been fabricated and studied. Their characteristics are similar to those of TFTs with molybdenum electrodes. The reliability was examined by extended high-temperature annealing and gate-bias stress. High-performance CMOS-type a-Si:H TFTs can be fabricated with this plasma etching method.

Electrical characteristics of a-Si:H TFTs after Co-60 irradiation and at different experimental stages have been measured. The gamma-ray irradiation damaged bulk films and interfaces and caused the shift of the transfer characteristics to the positive voltage direction. The field effect mobility, on/off current ratio, and interface state density of the TFTs were deteriorated by the irradiation process. Thermal annealing almost restored the original state's characteristics.

Floating gate n-channel a-Si:H TFT nonvolatile memory device with a thin a-Si:H layer embedded in the SiN_x gate dielectric layer has been prepared and studied. The hysteresis of the TFT's transfer characteristics has been used to demonstrate its memory

function. A steady threshold voltage change between the “0” and “1” states and a large charge retention time of > 3600 s with the “write” and “erase” gap of 0.5 V have been detected. Charge storage is related to properties of the embedded a-Si:H layer and its interfaces in the gate dielectric structure. Discharge efficiencies with various methods, i.e., thermal annealing, negative gate bias, and light exposure, separately, were investigated. The charge storage and discharge efficiency decrease with the increase of the drain voltage under a dynamic operation condition. Optimum operating temperatures are low temperature for storage and higher temperature for discharge.

a-Si:H metal insulator semiconductor (MIS) capacitor with a thin a-Si:H film embedded in the silicon nitride gate dielectric stack has been characterized for memory functions. The hysteresis of the capacitor’s current-voltage and capacitance-voltage curves showed strong charge trapping and detrapping phenomena. The 9 nm embedded a-Si:H layer had a charge storage capacity six times that of the capacitor without the embedded layer. The nonvolatile memory device has potential for low temperature circuit applications.

For my father in heaven, my mother and siblings

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CHAPTER I

INTRODUCTION

1.1. Amorphous Silicon Thin Film Transistor (a-Si:H TFT)

TFT is a type of field effect devices in which the applied voltage at one electrode, i.e., the gate, controls the electrical field by modulating the conductivity of an underlying semiconductor layer, i.e., the channel.¹ The modulation provides an electrical path for the carriers to travel about the other two electrodes, i.e., the source and drain.

a-Si:H TFT utilizes a thin film of a-Si:H as the channel for conduction. There are two types of channels depending on the majority carriers involved in the conduction: the n-type and the p-type. The n-type TFT makes use of an intrinsic a-Si:H film as the channel and relies on electrons to conduct current.² The p-type TFT uses lightly B-doped a-Si:H film as the channel to create a path for hole conduction.³ Naturally, the n-channel TFTs have higher field effect mobility, μ_{eff} , than the p-channel TFTs. The electron has a higher mobility than the hole since the effective mass of an electron is smaller than that of a hole.⁴

This dissertation follows the style and format of *Journal of the Electrochemical Society*.

The introduction of dopant in the a-Si:H film changes its conduction mechanism. However, it could also increase the defect density which affects the TFT characteristics. For instance, for the same channel dimension, an n-channel TFT requires a lower voltage to turn the transistor on, V_t , than a p-channel TFT.²

The basic structure of the gate, source, drain electrodes and the active layer for a functional a-Si:H TFT includes a top gate (staggered) and a bottom gate (inverted-staggered) arrangement.⁵ Figure 1 shows the cross-sectional schematic of the different TFT structures. Each structure has its own merits and demerits in terms of process flow and device performance. For instance, the top gate structure has several advantages over the bottom gate structure with etch stopper layer. Compared to the latter, the former requires less films deposition, needs less photolithography process for patterning, and allows for the channel to be deposited after the ohmic contact. However, the top gate structure requires that the gate dielectric to be deposited after the channel. The sequence requires a careful practice to minimize plasma damage on the channel from the gate dielectric deposition. Furthermore, the top gate structure corresponds to a higher overlapping area between source, drain, and gate electrodes, and as a result, to a high parasitic capacitance. The bottom gate structure with etch stopper layer, on the other hand, allows for a self-alignment process.⁶ The self-alignment results in a smaller overlapping area between the source, drain and gate electrodes, which in turn resulting in a comparatively smaller parasitic capacitance. Both the bottom gate and top gate structure allow for single-pump down depositions of the channel and gate dielectric to

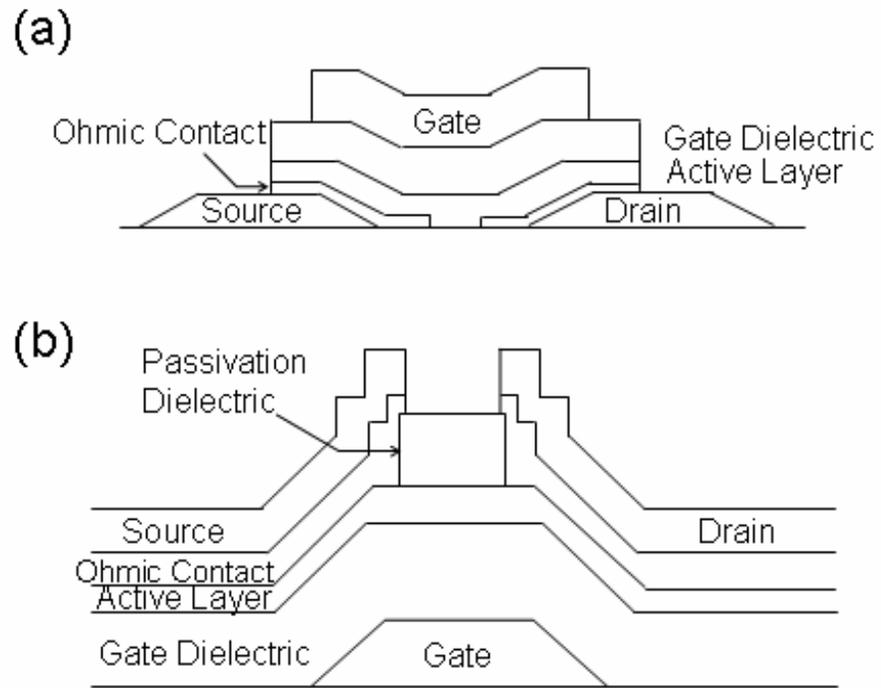


Figure 1. Cross-section schematic of the basic structure of TFT (a) staggered (top gate), (b) inverted-staggered (bottom gate) with etch stopper layer.

ensure a clean interface between the two films —an essential requirement for device performance.⁵

Historically, the concept of TFT has preceded that of the bipolar transistor and metal oxide semiconductor field effect transistor (MOSFET) with a concept patent in 1935.⁷ The milestones for a-Si:H TFT include the following points:

1. The first reported growth of amorphous silicon (a-Si) by plasma discharge⁸
2. The substitutional doping in a-Si is possible, ten orders of magnitude change in conductivity⁹
3. The experimental work on the crucial role of hydrogen in the electronic properties of high-quality a-Si¹⁰
4. The demonstration of the first functional a-Si TFT¹¹
5. The proposed model for the atomic structure of a-Si to explain many of its electrical properties, including substitutional doping¹²

The ubiquitous application of a-Si:H TFTs is as the switching device in active matrix liquid crystal display (AMLCD).¹³ The lower speed of an a-Si:H TFT is applicable to be used as the switching device in AMLCD since it only requires a refresh rate of 60 Hz.¹⁴ Other non-LCD applications includes x-ray imager,¹⁵ non-LCD flat panels,¹⁶⁻¹⁸ photo transistor,¹⁹ sensor,²⁰ and various capacity in circuits.²¹⁻²³

1.2. Preliminary Issues in a-Si:H TFT Fabrication

The two regions of operation of a TFT are the linear and the saturation regions. Figure 2 shows the channel behavior at the different operating regions for the bottom

gate structure used in this study. In the linear region, the TFT operates with ohmic conduction. Equation 1 describes the linear region from a gradual channel approximation,²⁴ i.e., (1) the drain voltage, V_d , controls the density of carrier in the active layer and thus the formation of the channel accumulation layer, and (2) the gate, the gate dielectric, and the channel are viewed as a capacitor,²⁵ i.e., the gate voltage, V_g , controls the mobile charge in the channel. The current observed at the drain, I_d ,

$$I_d = C_{SiN_x} \mu_{eff} \frac{W}{L} (V_g - V_t) V_d \quad (1)$$

where C_{SiN_x} is the SiN_x capacitance, μ_{eff} is the field effect mobility, W is the channel width, L is the channel length, V_g is the gate voltage, V_t is the threshold voltage, and V_d is the drain voltage.

In the saturation region ($V_d \geq V_{d, sat}$), the electric field between source-drain electrodes pinch off the carrier density in the channel. The I_d - V_d relationship becomes

$$I_d = C_{SiN_x} \frac{\mu_{eff}}{2} \frac{W}{L} (V_g - V_t)^2 \quad (2)$$

The μ_{eff} at the saturation region can be extracted from the linear regression of Equation 2.

Good quality a-Si:H TFTs should exhibit basic electrical performances such as a high μ_{eff} , e.g., $\sim 1 \text{ cm}^2/\text{Vs}$, for a faster switching speed,²⁶ a low V_t , e.g., $< 3 \text{ V}$, for low

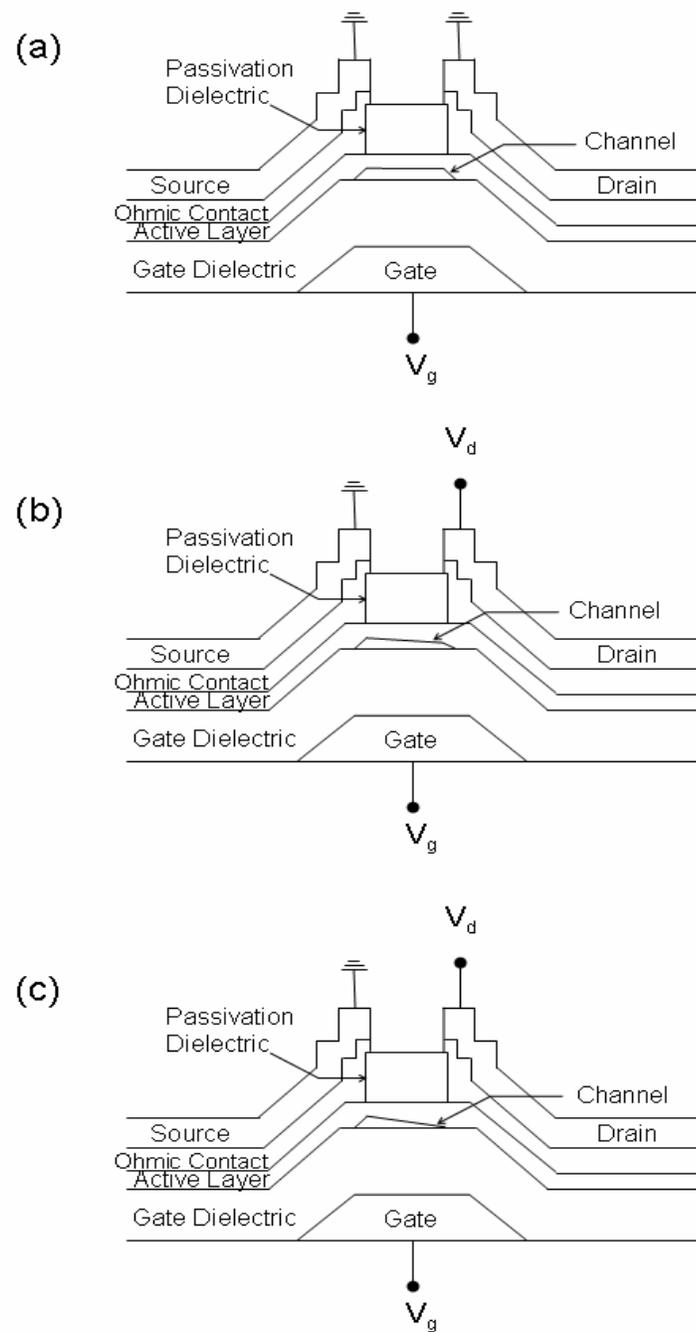


Figure 2. TFT operating regions under V_g bias (a) with $V_d = 0$, (b) at linear region, $V_d < V_{d,sat}$, and (c) at saturation region, $V_d \geq V_{d,sat}$.

power operation, a low off-current, I_{off} , for minimization of leakage current, a high on-current, I_{on} , for effective pixel driving, a high I_{on}/I_{off} ratio, e.g., 10^6 , for noise minimization,²⁷ and other dynamic requirements.²⁸

There are many aspects of the bulk and interface film properties to be assessed to achieve such performance.²⁹ First, the structural and electrical properties of the individual building block of TFT should be optimized. For instance, the Si active layer needs to have an acceptable conductivity level to accommodate a high mobility required in the channel, the SiN_x film needs to provide a high quality dielectric performance to minimize current leakage, and the contact layers needs to demonstrate a highly conductive ohmic behavior. Second, the interface between the a-Si:H/SiN_x layers should have minimum amount of interface charge trapping centers to accommodate for a high mobility requirement also. Third, the process integration to other plasma processes such as sputtering and reactive ion etching and to the lithography, wet etching, and annealing steps should be optimized.

The intrinsic a-Si:H used as the active layer for n-channel TFTs is an n-channel-type semiconductor. p-channel a-Si:H TFTs can be fabricated by doping the a-Si:H active layer with boron (B).³⁰ For example, the p-type a-Si:H layer can be deposited by plasma enhanced chemical vapor deposition (PECVD) method by using feed gas streams containing SiH₄ and B₂H₆ at 250°C.³⁰ Although the field effect mobility of a p-channel a-Si:H is low, the complimentary metal-oxide-semiconductor (CMOS)-type circuit can be manufactured with the availability of both types of TFTs. The availability of such circuit could be used in many low-speed applications such as sensors and detectors.

1.3. Cu/TiW Metal Gate for Hydrogenated Amorphous Silicon Thin Film Transistor

In its role as a pixel switching device in an active-matrix liquid-crystal display (AMLCD), the source electrode of a TFT is connected to the pixel electrode, while the drain electrode and gate electrode are connected to the data line and the address line, respectively. The time needed to reach a certain V_g is related to the RCL term of the transmission line, where R is the resistance, C is the capacitance and L is the line dimension of the conducting material.³¹

Figure 3 shows the RCL effect on time delay for MOS circuit,³² similar effect can be drawn for AMLCD circuit. RC delay can result in distortion of transmission signal or insufficient pixel charging, which deteriorates display quality. The RC delay is magnified with the long interconnect lines and close proximity of the pixels size and resolution requirement of the next generation display. The resolution, r , of a display affected by the time delays on the rise or fall time can be approximated as³³

$$r \approx \frac{1}{R_s D^3 (1 + \alpha)} \quad (3)$$

where R_s is the sheet resistance of the metal line, D is the display diagonal, and α is a function of C_s and C_{LC} capacitances of the storage capacitor.

The use of highly conductive metals such as aluminum, Al, ($2.7 \mu\Omega\text{-cm}$) and copper, Cu, ($1.67 \mu\Omega\text{-cm}$) as opposed to refractory metals (resistivity $> 15 \mu\Omega\text{-cm}$) such as molybdenum (Mo), chromium (Cr), and tantalum (Ta), etc., in both data and address

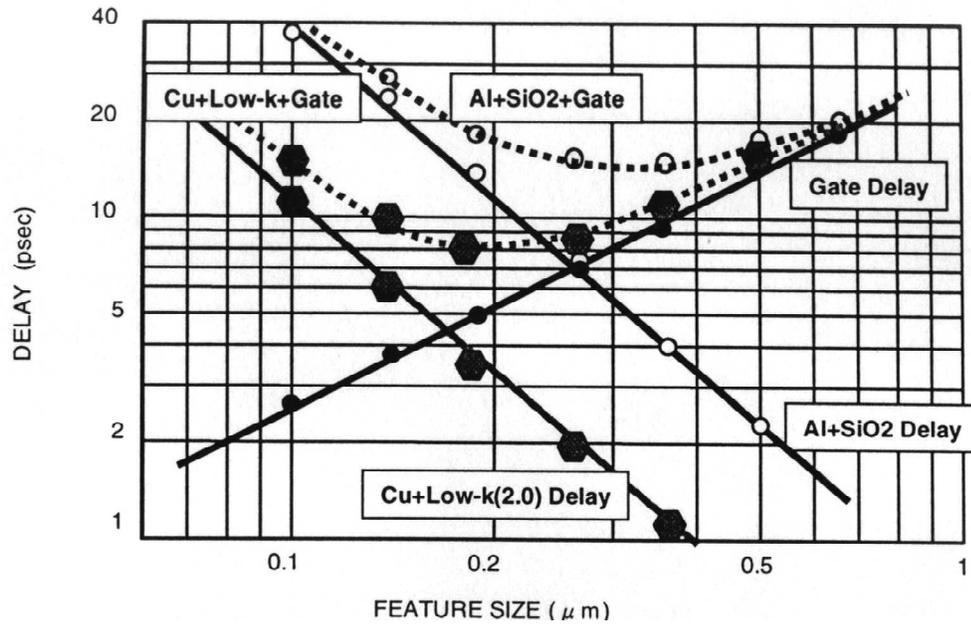


Figure 3. Gate delay and interconnect delay as a function of feature size for various metal and gate dielectric material. (After Ref. 32)

lines is required to reduce the RC delay. Compared to Al, Cu has the extra advantage of negligible hillock formation and being immune to electromigration. However, Cu has some inferior characteristics. For instance, Cu is difficult to etch into long, fine lines with a small undercut and a controlled slope profile by using a wet-etching method. Cu needs an adhesion or barrier layer underneath because it has poor adhesion to many substrates and can easily diffuse into an adjacent material at a raised temperature. Cu also has poor chemical resistance. Therefore, a passivation layer, such as Cu-Cr alloy, Cu-Mg alloy, AlN, or TiW is often deposited above it.³⁴⁻³⁷ The materials listed mostly conform to the diffusion barrier requirements: 1) conductive, 2) amorphous in nature in order to prevent Cu diffusion through grain boundaries, and 3) unreactive or form an equilibrium phase with Cu and other adjacent films such as Si and dielectric.³²

In this study, TiW is used as the barrier layer for Cu. Depending on its composition, the TiW work function, i.e., the energy difference between vacuum and the Fermi energy, is in the range of 4.3 eV (Ti) to 4.5 eV (W). Cu has a slightly higher work function of 4.65 eV. The small difference in work function between the TiW and Cu metal layers should accommodate the tunneling for electrical conduction between the two layers. The amorphous structure of the TiW film can be achieved by controlling the sputtering process parameters and the temperature of subsequent processes. Cu diffusion into the TiW diffusion barrier film can happen at temperature above the Si-Cu eutectic temperature, i.e., 555 °C.³⁵ Finally, Ti as a group III transition metal forms stable cupride with Cu, stable silicide with Si, and stable nitride with N, while W as a group V transition metal is unreactive with Cu, forms stable nitride with Si and but is unstable

with N.³⁸ Depending on the composition, transition metal alloys of TiW might have a compromised point of the advantages and disadvantages between both metals as a barrier layer for Cu.

Usually, the Cu lines is used in large area glass substrate, e.g., > 1 m by 1 m for liquid-crystal displays (LCDs). Cu lines in very large scale integrated circuit (VLSIC) are patterned by utilizing the chemical-mechanical polishing (CMP) method because it is difficult to etch Cu with a conventional plasma-etching method.^{39, 40} It is impractical to use the CMP method to prepare Cu lines on a very large substrate because it is not very flat and the process is complicated and costly. Other methods, such as jet printing, have been used to make Cu lines. This removes the need for conventional metallization, lithography, and etching.⁴¹ However, the maximum a-Si:H TFT process temperature, e.g., 300°C, limits its application in mass production. As an alternative, a novel plasma-based Cu etching process has recently been developed.⁴² The process is composed of two simple steps: (1) the exposure of the photoresist-patterned Cu film to a Cl- or Br-containing plasma, which converts the exposed Cu film into a CuCl_x or CuBr_x compound, and (2) the removal of the compound with a dilute HCl solution.⁴² Cu lines with a vertical wall profile and a high etch rate were obtained at room temperature.^{42, 43} The process is simple and only requires a conventional parallel-plate reactor. In addition, Cu/barrier dual layer could be etched with a completely dry process. This new process has been proven successful in etching complicated VLSI Cu/titanium tungsten (TiW) interconnect structure.⁴⁴

1.4. PECVD Films Optimization for a-Si:H TFT

PECVD method, a chemically reactive plasma process, has been widely used to grow the films that comprise the TFTs. For instance, a-Si:H was used as the active layer, microcrystalline n^+ Si was used for the ohmic contact, and the SiN_x was used as the gate dielectric and the top passivation layer.²⁷ The advantages include the ability for large area deposition, the convenience of gas phase doping, the economical low temperature process, and the convenience of performing single-pump down depositions to minimize contamination. Most importantly, PECVD method provides a wide window of operation for the optimization of film properties. The optimization can be performed by carefully considering the interaction among process parameters such as substrate temperature, gas phase composition, deposition pressure, and plasma power and frequency. These extrinsic plasma parameters directly affect the intrinsic parameter, e.g., the electron temperature, the dissociation efficiency, and the kinetics of the surface reaction.

Different plasma frequency should correspond to different film properties. It is important to observe the film properties deposited with each of the two plasma generator in this study, i.e., the 50 kHz and 13.56 MHz. There is bound to be less ion bombardment at the 13.56 MHz plasma compared to the 50 kHz plasma since the ionic species is less responsive to the alternating change in electric field at higher frequency plasma.⁴⁵ Self-bias decreases with the increase in frequency.⁴⁵ For instance, the ion bombardment has been observed to affect the a-Si:H properties deposited in the frequency range of 10 kHz – 50 MHz, i.e., the increase in the intrinsic compressive stress and the decrease in hydrogen content with the increase in frequency.⁴⁶ Ion

bombardment also affects film density.⁴⁷ a-Si:H structural and electronic properties such as defect density and doping potential are directly related to the film's H content.^{47, 48} The amorphous structure of a Si film corresponds to variety of Si-Si bonds, i.e., weak and strong Si-Si bonds. The weak Si-Si bonds easily break to form un-terminated dangling bonds. These defects can be passivated by bonding with H.⁴⁹ The film H content is process parameter dependent.⁵⁰⁻⁵² For the SiN_x film, the N and H contents are also process parameter dependent.^{53, 54}

A different doping behavior at different frequencies has been observed due to the different preference on the Fermi level energy shift, e.g., a shift towards the conduction band for a 400 kHz deposition and towards the midgap for a 13.56 MHz deposition.⁴⁷ The quality of the heavily doped n⁺ Si contact can be observed from the existence of the “current crowding” phenomenon on the linear region operation. The slope of Eq. 1 represents the total resistance of the parallel current path from the source to the drain electrodes via the channel. Since the resistance of the metal and the metal/contact are smaller than the channel resistance, the resistance of the former controls the total resistance. An ohmic behavior, i.e., the linear increase of I_d with V_d at a constant V_g should be observed. Non-ohmic behavior can also be attributed to the existence of parasitic resistances due to (1) the overlap of the source and drain electrodes with the gate electrode and (2) leaking of the SiN_x at the gate-source.⁵⁵

1.5. Radiation Effect on n-channel a-Si:H TFT

For MOS devices, ionizing photon radiation from sources such as x-ray and Co-60 caused the built up of trapped charges in bulk SiO₂ and at the SiO₂/Si interface, ultimately resulted in the shift the V_t of the device.⁵⁶ Similar effects have been observed on x-ray irradiated polysilicon (poly-Si) TFTs. The extent of damage is related to the exposed dosage.⁵⁷ Currently, there are few studies on the irradiation effect on a-Si:H TFT.^{58, 59} For example, it was reported that a-Si:H TFT was damaged, e.g., increase of the I_{off} and V_t , when exposed to a short wavelength light generated in a plasma etching reactor or a laser beam.^{60, 61} The damages could be repaired with a simple annealing step. For the x-ray imaging application, each pixel is composed of an a-Si:H TFT, a photodiode sensor, and a scintillation layer all of which are exposed to the radiation source during operation.⁶² Under the high dose x-ray irradiation, the TFT needs to be electrically biased or thermally annealed in order to perform the switching function effectively.⁵⁹

For the extra-terrestrial use, the gamma ray is naturally abundant in the cosmic space. Gamma-ray is more energetic than the x-ray. An x-ray has longer wavelength than a gamma ray, i.e., 10-0.1 nm vs. < 10 pm. The gamma ray irradiation can result in different photoelectron scattering, Compton scattering, and electron-hole generation effects from the x-ray irradiation.⁶³ The photoelectron scattering is associated with the emission of photoelectron from interaction of photon with a core electron.⁶⁴ The Compton scattering is associated with the decrease of photon wavelength after collision with an electron.⁶⁵ The electron-hole generation is possible by the absorption of photon

energy greater or equal to the film band gap. An electron from the valence band is transferred to the conduction band. A hole is generated from the absence of electron at the valence band. The energy difference between the photon energy and the band gap becomes the kinetic energy of the electron-hole pair. The source of gamma-ray used in this study is Co-60. The decay of Co-60 produces gamma-ray energy at 1.17 MeV and 1.33 MeV.⁶⁶

Since a-Si:H TFT is fabricated on top of an insulating substrate, such as a glass, it is a silicon-on-insulator (SOI) device. Therefore, the a-Si:H TFTs are expected to be immune to radiation damages when exposed to high-energy rays during operation, such as LCDs in space vehicles, outer space missions, or nuclear wars.

1.6. a-Si:H TFT as Nonvolatile Memory

Nonvolatile memory device has the ability to store and retrieve electrical charges at its gate/gate dielectric structure.⁶⁷ The main characteristic of a nonvolatile memory device is the high charge retention after electric field for storage has been removed. Semiconductor based nonvolatile memory devices, i.e., read-only memory (ROM) such as programmable ROM (PROM), electrically programmable ROM (EPROM), and electrically erasable programmable ROM (EEPROM) have been incorporated in modern integrated circuits.⁶⁸ Further studies on MOSFET-type memory have been focused on two techniques, namely, the choice of non-SiO₂ gate dielectric materials or varying the transistor structure. The former takes the advantage of the polarizability characteristics of ferroelectric material or metal oxides, etc.,^{69, 70} while the latter utilizes the carrier

tunneling and trapping phenomena, such as floating gate or embedded nanocrystal structures.^{71,72}

TFT based memory devices have been fabricated with similar principles of modifying gate dielectric materials such as embedding nanocrystals dot at the gate dielectric of a poly-Si TFT,⁷³ or varying the gate dielectric structure as in the poly-Si TFT with semiconductor oxide nitride oxide semiconductor (SONOS) structure.⁷⁴ The high temperature process of poly-Si TFT challenges its application on low temperature substrate such as polymer materials.

The availability of nonvolatile memory device based on a-Si:H TFT will open new areas for advanced functions or new products since the a-Si:H TFT can be fabricated at lower temperature. For instance, when static picture is stored at the memory device it requires less power to display. There are only few reports on the capability of a-Si:H TFT as a memory device with electron storage characteristics was fabricated with aluminum patterns embedded into the gate dielectric layer to form a floating gate structure.^{75,76} The fabrication process of such device is complicated and includes seven photomasks and many deposition and etching steps.

The charge stored, Q , at the floating gate memory device changes with time and is governed by the change in current density, J , as a function of electric field, ξ , of the control and gate dielectric.¹

$$Q(t) = \int J_1(\xi_1) - J_2(\xi_2) dt \quad (4)$$

In Equation 4, subscript 1 refers to the tunneling dielectric and subscript 2 refers to the control dielectric.

Non-stoichiometric a-SiN_x:H is the dielectric material used in a-Si:H TFT. It follows the Poole-Frenkel current transport

$$J = C \xi \exp [-q (\phi_B - (q \xi / \pi \epsilon)^{1/2}) / kT] \quad (5)$$

where C is a constant, ϕ is the barrier height, ϵ is the permittivity of the dielectric.

At static operation, the amount of charge stored can be quantified by the V_t shift of the TFT after charging¹

$$Q = (V_t^{\text{after charging}} - V_t^{\text{initial}}) \epsilon / d \quad (6)$$

1.7. Charge and Discharge of a-Si:H TFT Memory

It is critical to understand the charge and discharge capabilities of the floating gate a-Si:H TFT memory device in order to operate it and to achieve a high reliability. The injection and retention of charges to the a-Si:H embedded gate dielectric with respect to the gate bias condition under a grounded source and drain electrode condition can be examined. The discharge process can be taken as a combination of electron repelling and neutralization mechanisms. Discharging methods such as thermal annealing, opposite V_g bias, and light exposure might result in different discharge efficiency.

In practice, however, the drain electrode is not grounded during operation. For a conventional non-embedded TFT, the charge accumulation in the channel after the application of V_g is described by

$$Q = ew(l + 2\Delta l) \quad (7)$$

It is desirable to know the charge and discharge capability, efficiency, and mechanism under a biased drain electrode condition. The study on the effect of temperature on charging and discharging is also important for optimum operation of the memory device.

1.8. a-Si:H Metal Insulator Semiconductor Capacitor as Nonvolatile Memory

The addition of an a-Si:H embedded layer in combination with the two dielectric layers contributes to the charge trapping mechanism of the floating gate a-Si:H TFTs. Because metal insulator semiconductor (MIS) capacitor can store and remove charges with the formation of accumulation, depletion and inversion layers, it is reasonable to assume that similar type of embedded dielectric structure can enhance its charge storage capacity.

There is a lack of information on the memory function of the gate/SiN_x gate dielectric/a-Si:H MIS capacitor with an a-Si:H film embedded in the gate dielectric layer. Since flatband voltage, V_{FB} , of a capacitor is the demarkation between accumulation and depletion of charges, it can be used as a reference voltage for quantifying the stored charge Q_{ot}

$$Q_{ot} = C \cdot \Delta V_{FB} \quad (8)$$

where C is the capacitance at accumulation.

The MIS capacitor structure has been widely used to study the interface between a-Si:H and SiN_x.^{77, 78} The trap centers at the interface have been responsible to cause the

deviation from the ideal capacitor capacitance-voltage characteristic. There are two types of trap centers, i.e., donor-like and acceptor like. The former is neutral when filled with electron, the latter is charged negatively when filled with electron.¹ Since the a-Si:H embedded MIS capacitor has two extra interfaces layer, these interface charge trapping centers could affect the memory capacity.

1.9. Outline of the Dissertation

Chapter II elaborates on the materials and methods utilized in the fabrication of a-Si:H TFTs and memory devices. This includes the discussions on substrate material, cleaning procedure, plasma deposition and etching processes, lithography, and electrical characterization.

Chapter III exhibits and compares the electrical properties of the n-channel and p-channel TFTs with Cu/TiW electrodes to those with Mo electrodes. The use of highly conductive metal is important to reduce the *RC* delay from metal lines. These TFTs were prepared with 50 kHz plasma generator. The reliability issue of the Cu/TiW tungsten TFTs will be discussed.

The first and second parts of Chapter IV show the optimization process on film properties for PECVD films such as SiN_x, a-Si:H, and n⁺ Si:H for the complete fabrication of n-channel TFT. The PECVD films were deposited with 13.56 MHz plasma generator. The last part of Chapter IV shows the irradiation effect on the optimized TFTs and the recovery potential from thermal annealing.

Chapter V presents the novel nonvolatile memory based on embedding a thin a-Si:H film on the gate dielectric of the a-Si:H TFT. The film deposition conditions were chosen from the optimized films showed in Chapter IV. The feasibility, fabrication steps, and the device's basic memory characteristics such as hysteresis of transfer characteristics, programmability, and retention time will be discussed.

Chapter VI discusses in detail about the charge and discharge phenomena of the a-Si:H TFT memory device at static and dynamic operation conditions as well as a study on optimum temperature for charge and discharge. Different discharge schemes, i.e., thermal annealing, negative bias, and light exposure will be compared.

Chapter VII presents the nonvolatile memory based on embedding a thin a-Si:H film on the gate dielectric of a MIS capacitor. The chapter will discuss the structure, fabrication, interface effect, and basic memory characteristics of the device.

Chapter VIII summarize the works presented in this dissertation.

CHAPTER II

EXPERIMENTAL BACKGROUND

2.1. Introduction

This chapter describes the general fabrication and characterization methods and the background theories used in the making of a-Si:H TFTs, MIS capacitors, and memory devices in the study. The building blocks of the devices were thin films of a-Si:H, SiN_x, n⁺ μc-Si, and Mo. The thin films were deposited with plasma technologies such as plasma enhanced chemical deposition (PECVD) at elevated temperature up to 300°C and magnetron sputtering. Reactive ion etching (RIE) at room temperature was used to define the channel part of the devices. Both plasma deposition and etching techniques required clean and controlled environments which were achieved with high vacuum. For instance, a leak of oxygen into the chamber during deposition of a-Si:H film, a semiconductor material, oxidized the film to assume a property of a silicon oxide, a dielectric material. The plasma process conditions were optimized for material and electrical characteristics required on each film. Complete device was achieved with the integrations of the plasma technologies with other processes such lithography for pattern transfer, wet etching for pattern definition, and annealing at elevated temperature for damage repair. Finally, the finished devices were characterized electrically.

Section 2.2 discusses the plasma technologies used on deposition and etching and the theories behind each method. Section 2.3 elaborates on other fabrication steps used to make complete devices. Section 2.4 describes the chemical characterizations methods

used to analyze the thin films. Section 2.5 defines the electrical measurement used to characterize the completed device.

2.2. Thin Films Deposition and Etching

2.2.1. Corning 1737 Glass Substrates

Material Properties

Corning 1737 glass, a clear, alkaline-earth boroaluminosilicate type, was used as the substrate for the TFT and MIS capacitors. Table 1 shows the mechanical, thermal, optical, and electrical properties of the glass.⁷⁹

The light weight feature and the mechanical strength property of the 1737 glass contribute to its popularity with the active matrix liquid crystal display (AMLCD) industry. The thermal properties suited the highest temperature used in the fabrication process, i.e., 300°C for the plasma depositions of a-Si:H and SiN_x films. This temperature was well below the strain temperature of the glass, i.e., the extreme upper limit temperature for the glass to still retain its inherent properties after undergoing a thermal conditioning process. Furthermore, thermal expansion coefficient, TCE , of the glass is constant in the 0-300°C range. The TCE at this temperature range closely matched the TCE of the thin films deposited on top of the glass. Electrically, the high resistivity of the glass ensured minimum leakage current from the metal gate and provided isolation from the environment.

Substrate Preparation

RCA cleaning steps⁸⁰ were performed on the 1737 glass in order to minimize contamination from organic, oxide, or metallic element at the glass surface. Human and

Table 1. Material properties of Corning 1737 glass⁷⁹

Mechanical	
Density (20°C)	2.54 g/cm ³
Young's Modulus	70.9 GPa
Shear Modulus	28.9 GPa
Thickness	0.7 mm
Thermal	
Thermal Expansion (0-300°C)	37.6 x 10 ⁻⁷ /°C
Thermal Conductivity (23-300°C)	0.00217-0.00346 cal/(cm-sec-K)
Working Temperature	1312°C
Softening Temperature	975°C
Annealing Temperature	721°C
Strain Temperature	666°C
Optical	
Refractive Index	~ 1.51
Electrical	
Dielectric Constant	5.7
Log ₁₀ Volume Resistivity (250°C)	13.5 (Ω-cm)

environment during glass processing and handling were the source of organic contamination such as oil and grease. The glass also formed some native oxide on the

surface. Ionic contamination came from the glass itself since it contained boron, aluminum, and alkali elements.

The cleaning procedure was as follow. First, the glass substrate was immersed in $\text{H}_2\text{O}_2 : \text{NH}_4\text{OH} : \text{H}_2\text{O}$ solution (1:1:5 volume ratio) for 10 minutes at 85°C to remove organic contaminants. Generally, H_2O_2 acts as a strong oxidant for the organic C-chain contaminants, resulted in the increase the water solubility of the contaminants, while NH_4OH acting as the buffer in the solution. The substrate was rinsed twice in de-ionized (DI) H_2O for 1 minute each. The resistivity of the DI H_2O was $> 17.2 \text{ M}\Omega\text{-cm}$ corresponded to a high de-ionization quality. Second, the glass was immersed in $\text{HF} : \text{H}_2\text{O}$ solution (1: 50 volumetric ratio) for 15 s to remove both the oxidized organic contaminants left over from part 1 and the native oxide on the surface. This cleaning mechanism relies on the fluorination of Si that is bonded with contaminant or Si that formed native oxide to create a more water soluble fluorinated species such as SiF , NH_3AlF and NH_3SiF . No hazing was observed on the glass. Durability of the 1737 glass includes a 6.34 mg/cm^2 weight loss for a 20-minute immersion in 10 % HF solution. The weight loss from 15-s cleaning process was well below the data. The glass then underwent another two-step rinsing in DI H_2O . Third, the glass was immersed in $\text{H}_2\text{O}_2 : \text{HCl} : \text{H}_2\text{O}$ solution (1:1:6 volumetric ratio) for 10 minutes at 85°C to remove the ionic contaminants. The removal of contaminants is based on the reaction of the anion Cl^- with the ionic contaminant to form soluble inorganic complex. Another two-stage DI H_2O rinse followed. The substrate was immediately dried with N_2 air gun. Finally, the glass

was inspected under the microscope for visible particles before loaded into the deposition chamber.

2.2.2. Equipment for Plasma Processes

Plasma-Enhanced Chemical Vapor Deposition (PECVD)

Parallel plate PECVD reactor (Applied Materials, AMP Plasma I) was used to deposit a-Si:H, SiN_x, and heavily doped n⁺ μc-Si:H films. Figure 4 shows the simplified schematic of the PECVD chamber with all of its main features and control system. Gas flow into the reactor is controlled by mass flow controllers. Pressure system consists of an angle valve, a booster pump, and a mechanical pump, and pressure control logic. Temperature system consists of three-zone heater and controllers. Plasma system consists of an RF generator, a pi-type matching network, a blocking capacitor and plasma control logic. The pressure, plasma and mass flow control systems are controlled by PC with LabWindows/CVI interface (National Instrument).

The gas supply into the reactor through the mass flow controllers include: N₂ (ultra high purity, Botco, Bryan, Texas), N₂ (semiconductor, 99.9999% purity, Praxair), Ar (semiconductor, 99.9999% purity, Praxair), SiH₄ (semiconductor grade, 99.999%, Scott Specialty Gasses), B₂H₆ (2 % in H₂, 99.999% purity, Matheson Tri-Gas), PH₃ (semiconductor grade, 99.999%, Scott Specialty), NH₃ (Semiconductor, 99.999% purity, Matheson Tri-Gas), and H₂ (Semiconductor, 99.9999% purity, Praxair). Figure 5 shows the gas flow schematic as the inlet to the PECVD reactor.

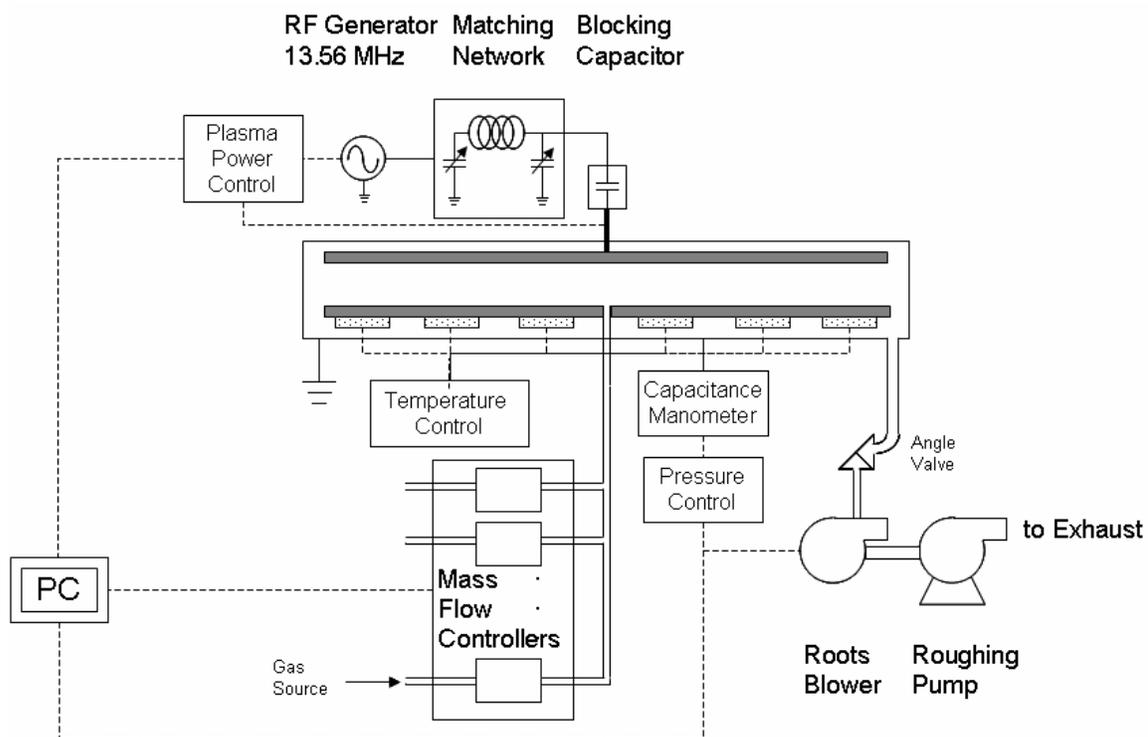


Figure 4. Schematic of plasma-enhanced chemical vapor deposition system.

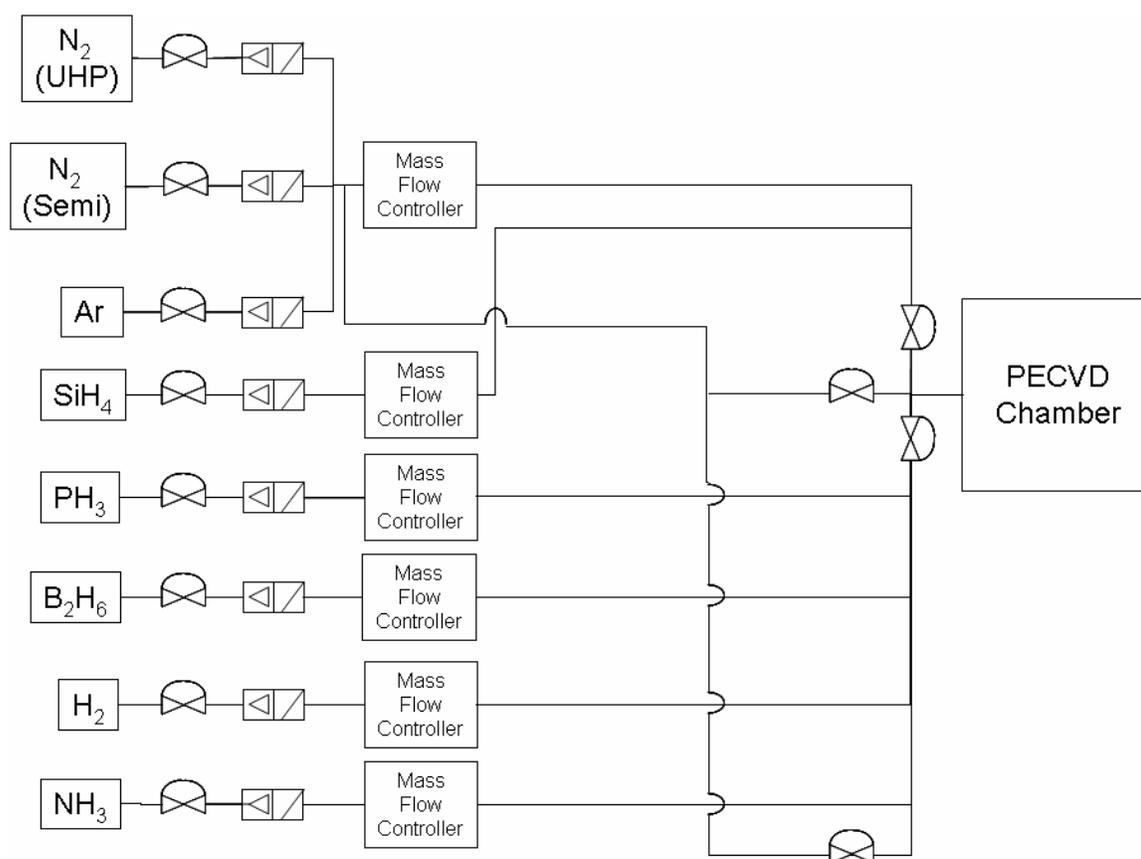


Figure 5 Gas flow schematic for plasma-enhanced chemical vapor deposition system.

Pressure range used in the plasma system is from 100 mTorr to 500 mTorr. Gas phase interaction is viscous at this condition, i.e., gas molecules interact with each other as opposed to adsorption and desorption of gas molecules at the wall chamber. The pressure range is a typical condition for acceptable molecular scale, i.e., mean free path for collision, and at the macro scale, i.e., the residence time of gas inside the chamber before being pumped out of the system. Solenoid-controlled right-angle valve acts as the gate between chamber and vacuum pump. The 90° turn of flow in the valve assisted in the pumping from atmospheric. Oil-sealed mechanical pump (Leybold, D90 AC) was used to achieve a base pressure of roughly 130 mTorr in reasonable time. A booster pump was used to provide additional constriction for the mechanical pump and to control the reactor pressure during process. Capacitance manometer (Vacuum General, CML10B) is used to monitor the chamber pressure at the chamber outlet end. The accuracy of the capacitance manometer is 1 mTorr.

The reactor is equipped with three-zone heaters. The outer, center and inner heating zone has two, five, and one heating element, respectively. The placement of the heating elements was designed to ensure uniform radial heating. Since film thickness, and subsequently film deposition rate, is a dependence of substrate temperature, enough care had to be exercised in order to achieve film uniformity. Figure 6 and Table 2 shows the variation of a-Si:H and SiN_x film deposition rates on different part on the center zone of the grounded electrode for 30 and 25 minutes depositions at 250°C, respectively. Since both films are of amorphous type, they were deposited consistently on the spots with lower deposition rate to ensure a denser morphology.

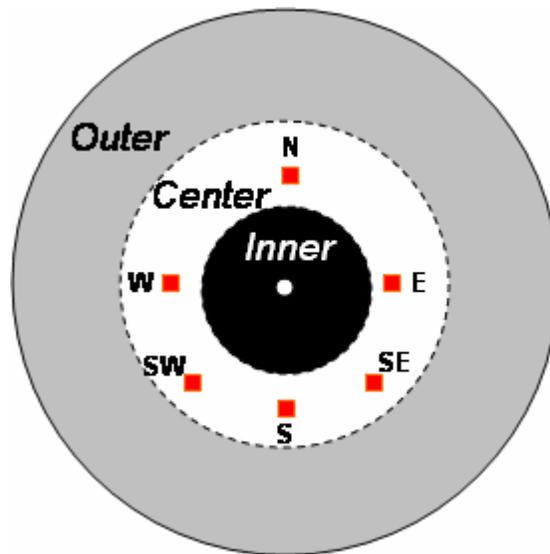


Figure 6. Heating zones and the various positions used in PECVD thickness uniformity test.

Table 2. Film deposition rates at various positions on the center zone of the PECVD electrode for 25-minute (a-Si:H) and 30-minute (SiN_x) depositions

Position	Deposition Rate ($\text{\AA}/\text{min}$)	
	a-Si:H	SiN_x
N	38	98
E	38	104
SE	42	99
S	46	103
SW	47	73
W	33	92

There are two types of RF generator used for the PECVD reactor to provide plasma at a high frequency of 13.56 MHz and a low frequency of 50 kHz, respectively. In both hi and lo -frequency cases, the top electrode of the PECVD chamber was powered and the bottom electrode and the wall were grounded and matching between load and generator output was aimed for 50 Ω .

The 13.56 MHz RF generator (OEM-12A, ENI) is connected with a pi-type matching network (MW-10, ENI). RG-393 co-axial cables were used to connect the RF generator, the matching network, and the chamber. In an ideal case where impedance of the load, i.e., the chamber and the plasma, is purely resistive and there is no loss in the transmission line, the maximum time averaged power from the RF generator to be absorbed at the load equals one quarter of peak to peak voltage of the generator squared over the resistance of the generator. In practice, the load impedance is reactive, i.e., consists of a capacitive reactance and a resistance part, while the generator is designed to be almost purely resistive. A mismatch of impedances between the generator and the load results in power loss which ultimately corresponds to the low efficiency of power absorbed at the load and the power overload at the generator from the reflected power. A pi-type matching network, in which a tuning capacitor, C2, is placed in parallel with the parallel form of resistive and capacitive reactance components of the load, is connected between the chamber and the generator. The nature of the pi-type matching network allows the complex conjugation of a wide range of load impedance.⁴⁵ A load capacitor, C1, is placed in parallel on the generator side to match the capacitance part of the load

impedance. Automatic or manual setting of the C1 and C2 capacitors controlled the degree of impedance matching. The magnitude of reverse power is < 5 W.

For the low frequency plasma, the 50 kHz RF generator (ENI, 3200 AMT, Rochester, NY) is connected with a step-up wound transformer (ENI, AM-10, Rochester, NY) as its matching network. RG-8 co-axial cables were used in the low frequency system to connect between the RF generator, the transformer, and the chamber. For this low frequency system, a step-up transformer acted as the matching network. The transformer conserves the power at each side of its two coils while transforms the voltage. Impedance matching follows the squared of the turn-ratio of the transformer.

Magnetron Sputtering

Figure 7 shows the simplified schematic of the magnetron sputtering used in the experiments. All of the high-k films were deposited by a magnetron radio frequency (13.56MHz). The reactor has three sputtering guns with two sets of RF generator/

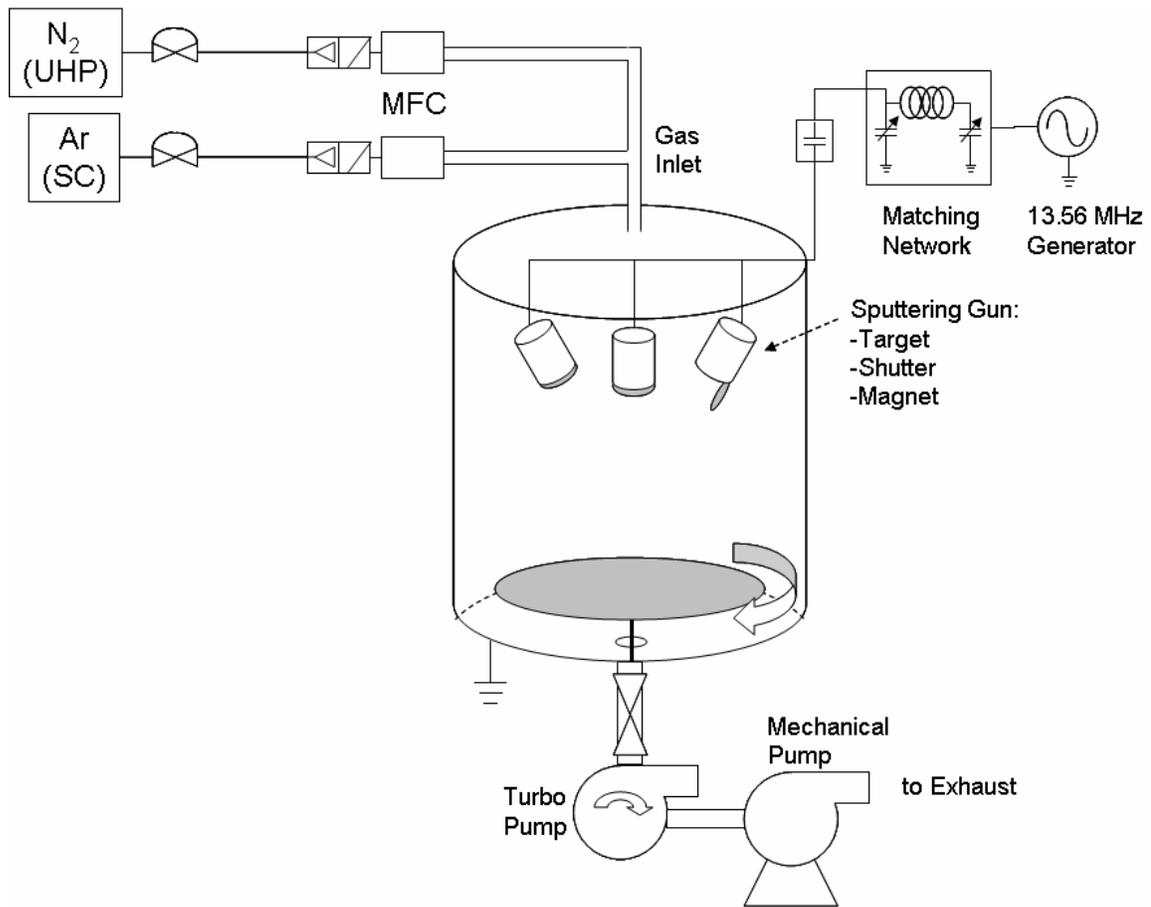


Figure 7. Schematic of magnetron sputtering system.

matching network and a DC generator. Targets used were 2 inches in diameter. The film thickness was controlled by deposition time. The working pressure for sputtering process was 5×10^{-3} Torr. Base pressure of 4×10^{-7} Torr can be achieved with a combination of turbomolecular pump and a mechanic backing pump. The substrate and chamber walls were kept at room temperature during the sputtering deposition.

Reactive Ion Etching (RIE)

A conventional diode-type reactive ion etching (RIE) chamber (700D, Plasma-Therm, St. Petersburg, FL) was used to etch a-Si:H and n^+ μ c-Si:H films. The bottom electrode is powered with a 13.56 MHz RF generator for plasma generation. The upper electrode and the reactor wall were grounded. Both the top and bottom electrodes were made of anodized aluminum and were of the same size, i.e., a diameter of 9 in, with a 2.8-in gap in between. DC sheath potential for ion bombardment was in the range of 150 V. Figure 8 shows the simplified schematic of RIE system.

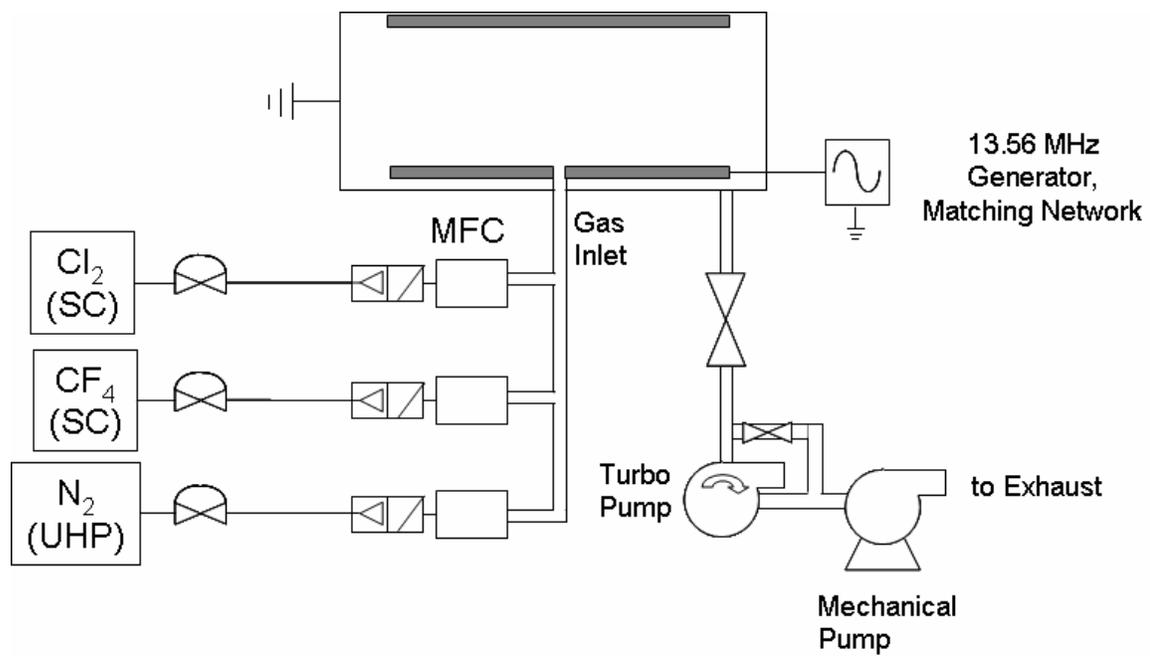


Figure 8. Schematic of reactive ion etching system.

2.2.3. Plasma Deposition and Etching of Thin Films

Low pressure plasma can be generated when currents which are supplied by the electric field from the RF generator pass through a confined gas environment. The currents partially ionize the gas into a collection of charged, neutral and radical particles. Due to the partial ionization state, the plasma is consisted mainly of neutral particles. The plasma density is quantified by the density of the charged particles, i.e., the electrons and the ions. For the low pressure plasma discharge, the plasma density is in the 10^8 - 10^{13} range cm^{-3} .⁴⁵ In general, the density of electrons equals the density of ions resulting in electrically neutral plasma. The visible glow characteristic is due to the excitation of electrons to a higher energy state followed by the relaxation to a lower energy state which is accompanied by photon emissions.

Positively charged dark spaces, or sheaths, naturally formed on a finite distance from each electrode due to charge imbalance. The mean speed velocity of ions or electrons is inversely proportional to the squared root of the mass.⁴⁵ Since the mass on an electron is about 10^5 lower than the mass of ion, it allows the electrons to be $>10^2$ times more mobile compared to the ions. At the beginning of the plasma discharge, electrons hitting the wall or electrode form negatively charged surfaces, which with time repel more electrons from coming and attract ions. The electrons head back to the bulk plasma and sustain the glow while the ions bombard the grounded region. This corresponds to DC bias profile at the sheath regions at both electrodes. With the alternating nature of the AC source, the voltage drop across the sheath and thus the thickness of the sheath at both the powered electrode and the grounded electrode sides

grows and shrinks alternatively. Sheaths formed at the low-frequency plasma generation results in higher ion bombardment than those formed during hi-frequency plasma.

Furthermore, due to the capacitive potential difference between powered and grounded area and the space charge dependence on the potential and electrode diameter, the ion bombardment at the smaller electrode is higher than that in the powered electrode.⁴⁵

Specifically,

$$\frac{V_1}{V_2} = \left(\frac{A_2}{A_1} \right)^n \quad (9)$$

where V is the applied bias at the electrode, A is the area of the electrode, and subscripts 1 and 2 refer to respective electrode. The typical experimental n -value is observed to be between 1 and 2.⁴⁵

Reactor dimension and optimization of process parameters such as gas flow rate, pressure, plasma power and frequency, and substrate temperature, can be used to collaboratively control the gas phase transport phenomena, the activity of electrons and ion of the plasma, the transport of particles to the substrate, and the kinetics of the reaction or surface phenomena at the substrate. For instance, gas residence time and consumption time are determined by factors such as chamber volume and system pressure, plasma density and potential and ion bombardment are dependence on factors such as the RF power, frequency, and the ratio of electrode areas as well as the gap between the electrodes, while temperature supplies the thermal energy needed for reaction or other surface phenomena.

Plasma Enhanced Chemical Vapor Deposition (PECVD)

In the PECVD reactor, the substrate for film deposition is positioned at the grounded electrode. Ion bombardment to the growing surface is minimized due the larger grounded area (bottom electrode + wall) compared to the powered electrode. Partial ionization of the source gasses by the energetic electrons in the plasma supplied the energy for bond breaking to generate neutral and charged particles. Electron temperature associated with plasma generation is about 20,000 K. As a result, PECVD films can be deposited at a substantially lower temperature, e.g., < 300 K, than those from a thermal deposition method, e.g., > 600 K. The transport of the particles to the surface substrate and their participation in the chemical reaction resulted in the final growth of the solid film.

Magnetron Sputtering

Magnetron sputtering powered with an RF generator was used for the depositions of Mo as the gate, source and drain electrodes of TFTs and the ground and gate electrodes of MIS capacitors. The surface growth of elemental material by physical vapor deposition such as sputtering does not involve any chemical reaction. Ion of noble gas such as Ar is used in the sputtering of target material in order to minimize contamination on the deposited film. In a simplified view, the electrons in the plasma with energy larger than 15.7 eV ionize the Ar gas. Some of the highly energized Ar^+ ions bombard the target material, while the rest collide with Ar atoms resulting in a multiple avalanche effect inside the plasma. Secondary electron is emitted when the Ar^+ collides with target to participate in plasma sustenance and in collisions with other Ar atoms. The

knocked-off atoms from the target travel down to the substrate. At the substrate, the atom can migrate along the substrate or re-enter the gas environment. Substrate temperature enhanced the mobility of the atoms on the surface. Further collisions with incoming atom forms nucleation of the atoms followed by an island growth. Continuous island growth forms a coalescence of islands and finally a continuity of film. The composition of deposited film follows the composition of the target material. To promote uniformity in film thickness, the substrate electrode was rotated at a speed of 10 rpm.

In the sputtering chamber, the substrate is also positioned at the grounded electrode while the target is positioned at the powered electrode. The powered electrode is designed to be much smaller than the grounded electrode with the purpose of minimizing ion bombardment to the substrate. A circular magnetron arrangement i.e., a circular magnet providing a magnetic field perpendicular to an electric field, is used to increase the efficiency of electron ionization around the target electrode. As a result, the plasma is sustained and the avalanche multiplication effect can be magnified.

Reactive Ion Etching (RIE)

In the reactive ion etching of a-Si:H and n⁺ μc-Si:H films, the electrons generated in the plasma partially ionize the fluorine or chlorine-based etching gasses, e.g., Cl₂ and CF₄. The transport, adsorption, and migration of the resulting neutral, charged particles, and radicals, and electrons were followed by surface reaction to generate fluorinated or chlorinated volatile Si products. The substrate with the film material to be etched is positioned at the powered electrode which is comparatively smaller than the grounded

electrode and wall. With this electrode arrangement, ion bombardments also participate in the etching of materials.

Effective etching of materials can be attained with a minimum formation of nonvolatile fluorinated reaction products, i.e., plasma polymerization, at the surface of the etched substrate. This can be achieved by controlling the chamber pressure and the etching gas. For instance, the CF_4 plasma at 100 mTorr did not result in the polymerization during the RIE of a-Si:H film.⁸¹ Once the pressure region for polymerization-free etching has been established, the next step to consider is the gas flow rates region corresponds to a compromised effect between a kinetic-limited etching and a transport-limited etching. A kinetic-limited etching is the result of limited reactants from a low flow rate condition. A transport-limited etching is the result of the low residence time of highly reactive species due to the increase of pumping speed at a constant pressure etching.

Etching selectivity greater than 1:1 between SiN_x and a-Si:H or $n^+ \mu\text{-Si:H}$ films can be achieved by the use of Cl_2 and CF_4 mixture.⁸² The etching capability of CF_4 gas on Si:H films is magnified by the Cl_2 plasma chemistry. For instance, Cl_2 plasma resulted in an ion assisted etching mechanism to form SiCl_x volatile products. The Cl^- plays a significant role in the etching of heavily doped film such as the $n^+ \mu\text{-Si:H}$.

2.3. Other Processes for Device Fabrication

2.3.1. Lithography

Lithography is a transfer of image onto a substrate. Pattern transfer process consists of a light penetration through a mask with binary pattern onto a photosensitive coating material on top of the substrate. Contact printing is achieved by an intimate contact of the mask and the coated substrate. It provides the simplest lithography with a 1:1 image transfer characteristic. The contact was achieved by vacuum. Aligner (Quintel, Q 4000, San Jose, California) with a mercury arc light source (Advanced Radiation Corporation, Q2600, Santa Clara, CA; 350 W, 56 V, 6.2 A) to deliver broad mid UV spectrum. A series of mirrors, collimator, and lenses collects, distributes, collimates, and uniformly directs the UV light onto the mask plane.⁸³ Figure 9 shows the schematic of the optical system of a typical contact aligner. Resolution, i.e., the minimum feature size, an aligner system delivers is partly attributed to the capability of its optical system in directing uniform intensity light.

The pattern to be transferred from the mask is due to the existence of the opaque part, e.g., chromium, and the transparent part, e.g., alluminosilicate, lime glasses. Resolution of the resulting image transfer then is also affected by the light diffraction in the mask. Image contrast, on the other hand, is associated with a modulation transfer function, *MTF*, which is defined as the ratio of the difference in maximum and minimum light intensity to the total intensity. For a contact printing, $MTF \sim 1$, resulting in highly contrasted pattern from the background.

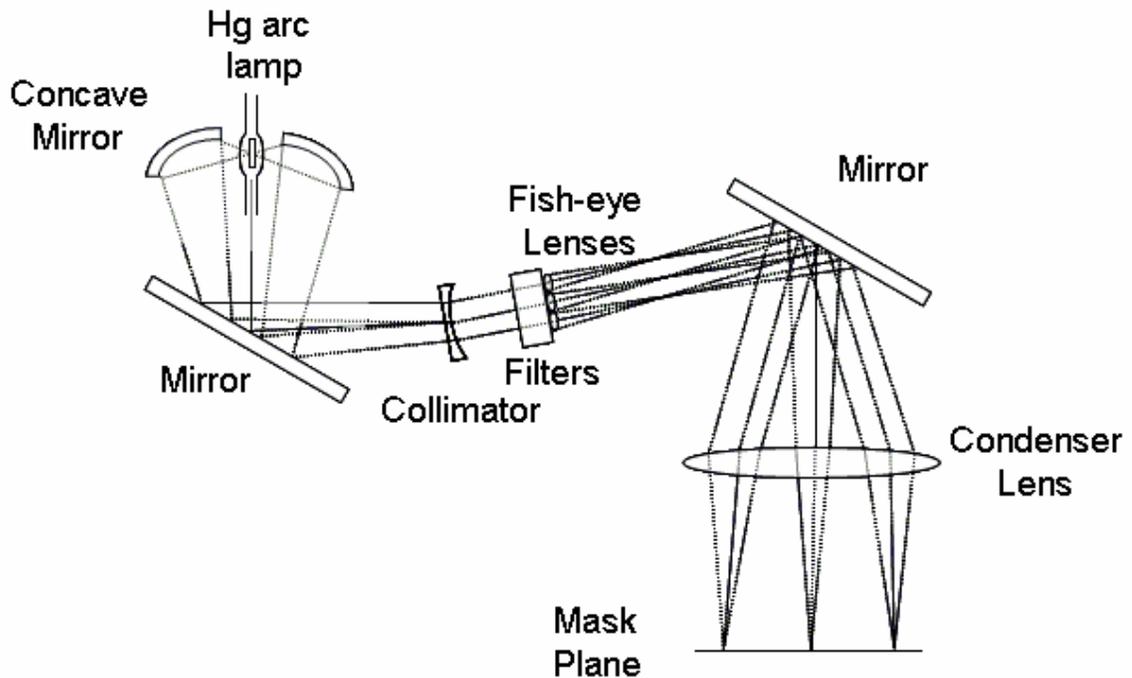


Figure 9. Optical system schematic for a typical contact aligner.⁸³

Positive photoresists with light sensitivity to g-line (435 nm), h-line (405 nm), i-line (365 nm) were used in the lithography. The photoresist consists of three materials: (1) resin as host material, (2) photoactive component that will change the dissolubility of the resin after UV exposure, i.e., enhancing dissolution for resin, and (3) solvent to control the viscosity of the photoresist for uniform spin coating operation. Both AZ 3312 and AZ 1512 (AZ Electronic Materials, Somerville, NJ) used in the study utilize cresol novolak, diazonaphthoquinonesulfonic ester, and methoxy-propanol acetate, as the resin,

the photoactive compound, and the solvent, respectively. The photoresist was applied at the surface by means of spin coating. The photoresist thickness is approximately inversely proportional to the spin rate to the half.⁸⁴ A spin rate of 4000 rpm usually corresponds to $\sim 1 \mu\text{m}$ -thick photoresist. The solvent needed to be removed from the coated substrate before it undergoes the UV exposure to increase the sensitivity of the photoresist. The practical method is to bake the coated substrate in a temperature close to the vapor temperature of the solvent for some short time. Optimization on the bake temperature and time leads to the compromising point between the sensitivity (dissolution rate) and the contrast after exposure.

Resolution of photoresist is governed by the behavior of light traveling through the resist. For instance, the light intensity decreases as it propagates down the bottom of the photoresist. Light also reflected on and off the substrate and the photoresist top. Swing curve of the photoresist accounts for the reflective behavior and relates the exposure dose needed to totally dissolve the photoresist as a function of film thickness. Based on the swing curve, the AZ 3312 requires a dose of 68 mJ/cm^2 on the exposure of $1 \mu\text{m}$ -thick photoresist on bare silicon substrate.⁸⁵ The lights reflection on glass substrate is less than the wafer substrate, which leads to a different swing curve. At $1 \mu\text{m}$ -thick and g-line exposure, AZ 3312 and AZ 1512 are projected to produce a $0.7 \mu\text{m}$ and a $0.9 \mu\text{m}$ resolution, respectively.

UV exposure results in the breaking of the weak bond between N_2 and carbon ring of the photoactive compound. The stabilization of the resulting molecule resulted in a ketene compound.

Immersion on base solution is required in dissolving the exposed part of the photoresist. The developer used was AZ 300 (AZ Electronic Materials, Somerville, NJ), which contains tetramethylammonium hydroxide. The ketene compound formed after a UV exposure reacts with water to form a carboxylic acid compound. The carboxylic acid then reacts with ammonium hydroxide of the developer to form salts. Some degree of water dilution of the developer is needed to promote the carboxylic acid generation. Stirring is needed to accommodate the N_2 release from the photoactive compound and the removal of dissolved resin and carboxylic compound from the substrate. An overall resolution of 1 μm or better was achieved in the lithography process of this study. In practice, the UV light dose used in the experiment was 11 mW/cm^2 .

2.3.2. Wet Etching

Wet etching is used to etch two types of films: the Mo (100 nm) layers for gate, source and drain electrodes and the SiN_x layer (250 nm) for top passivation layer. The three components of wet etchants materials are (1) oxidant to oxidize the materials to be etched, (2) acid or base to dissolve the oxidized materials, and (3) host solution.

Mo Etching

The wet etching used for the patterning of Mo for the gate is due to the simple procedure involved. Wet etching of a single layer material usually corresponds to a concave profile⁸⁶ which will yield a possible step coverage problem. However, since the thickness of gate dielectric to be deposited on top of the Mo is in the 300 nm range,

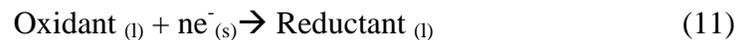
which is about three times as thick as the Mo gate, the step coverage problem will not be realized.

Plasma etching for Mo layer involved the use of CF₄ and/or Cl₂, and O₂ gasses.⁶¹ O₂ accommodates the etching process by oxidizing the nonvolatile C by-products from the CF₄-Mo reaction. The etch rate with CF₄ and 35% O₂ can be as high as 200 nm/min,⁶¹ which can easily led to over-etching and undercut. Furthermore, the use of O₂ will lower the etching selectivity to photoresist, e.g., ~ 1.4:1 etch ratio of photoresist: Mo for 20% O₂ in CF₄/O₂ etchants.⁶¹ There are two films to be etched consecutively in the source and drain area: the Mo and the n⁺ layer. Therefore, a high etching selectivity to photoresist on the Mo etching is important for the photoresist to still cover the intended area for the n⁺ layer etching. Based on the etch ratio, the photoresist selectivity, and the simplicity, the wet etching instead of the plasma etching in the patterning of Mo for source and drain electrodes.

The etching is treated as Mo corrosion⁸⁷ represented by the oxidation at the anode



and reduction at the cathode



The etch rate is the equilibrium point between the anodic and cathodic reactions.

Oxidation of Mo into Mo³⁺ can be achieved in an acidic solution. The acidic mixture called PAN solution for Mo etching consists of H₃PO₄: HNO₃: CH₃COOH:H₂O with

17:1:1:1 volumetric ratio is used to achieve the acidic. The etch rate of Mo in the PAN solution is 120 nm/min.

SiN_x Etching

The wet etching is used in the SiN_x patterning as top passivation layer. The gate metal was used as the mask for top passivation layer with the process called backlight lithography.⁸⁸ About 20% undercut is needed to open the area for source and drain contact to the a-Si:H channel. Wet etching is a good candidate to achieve the undercut profile. Diluted HF:water solution with 1:10 volumetric ratio. The etch rate is 35 nm/min. The stop layer for SiN_x etching is the a-Si:H layer which has a very low etch rate in HF solution. The etching might follow an overall reaction similar to that on stoichiometric Si₃N₄⁸⁹



2.4. Chemical Characterization

2.4.1. Electron Spectroscopy for Chemical Analysis (ESCA)

Figure 10 illustrates the principle of ESCA⁹⁰ for a Si atom. Photons from an incident monochromatic x-ray causes the ejection of a core electron to become a photoelectron. Conservation of energy yields

$$h\nu = E_B + q\theta_{SP} + E_{SP} \quad (13)$$

where $h\nu$ is the x-ray energy, E_B is the binding energy, $q\theta_{SP}$ is the work function of the spectrometer, and E_{SP} is the spectrometer energy. The ESCA equipment (Kratos Axis His 165) was equipped with a dual anode x-ray gun: Al $K\alpha$ (1486.6 eV) or Mg $K\alpha$ (1253.6 eV), a single or multiple quartz monochromator, a hemispherical analyzer, and a channel electron multiplier detector. At the x-ray gun, the filament is grounded while the choice of anode (Al $K\alpha$) was biased at 15 kV. kV.

At the analyzer, a pass energy of 80 eV was picked. Electron arrived with energy below the pass energy will be retarded, while the one arrived at energy exceeding the pass energy will be accelerated to the detector. A bias of 10 kV on the collector-anode assuring a $\sim 10^8$ secondary electrons for every electron arrived at the detector.

Qualitative and quantitative analysis of ESCA is derived from the plot of photoelectron intensity for a range of binding energy.

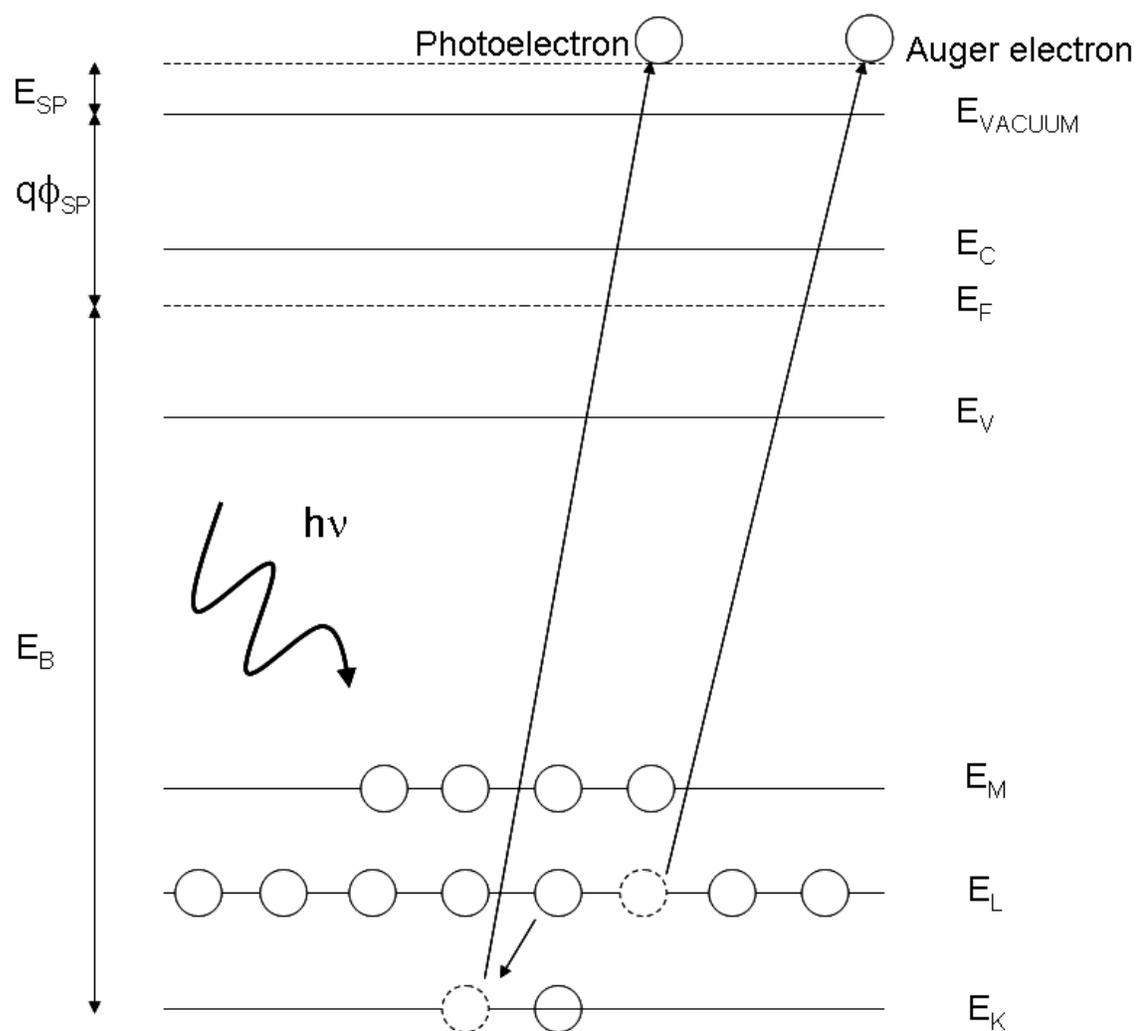


Figure 10. ESCA principle illustrated for Si atom.

The photoelectron intensity, I , is described as⁹⁰

$$I = J \rho \sigma K \lambda \quad (14)$$

where J is the flux of photon from incident x-ray, ρ is the atom or ion concentration in the surface, K is the instrument and experimental factor, and λ is the electron attenuation length. The intensity shapes to form peaks and background over the binding energy range. The peaks correspond to the excited electrons which escape as photoelectrons without suffering any energy loss. The background corresponds to the excited electrons involved in inelastic collisions. The peak is fitted with either a Gaussian or Lorentzian algorithms, or a mixture of both to quantify the area under the peak. Reduced χ^2 is used to judge the wellness of the fitting. The area ratios can be directly related to the percentage of a particular element. Energy shift of a peak compared to the peak a neutral state corresponds to the chemical change of the element. For peak deconvolution, a hypothesis on possible chemistry of the multiple peaks that form a single wider peak is needed to dictate the peak widths and the relative intensities of the peaks.

2.4.2. Raman Spectroscopy

Raman spectroscopy utilizes the scattering of photons from the incident light of a monochromatic laser onto the substrate by the lattice vibration of the substrate.⁹¹ There are three major types of photon scattering: Raleigh, Raman Stokes, and Raman Anti-Stoke. Raleigh scattering is the scattering of the excited photons back to the incident vibrational energy. The Raman Stokes is the scattering of the excited photon towards a lower vibrational energy. The Raman Anti-Stokes is the scattering of the excited photons

towards a higher vibrational energy. The Raman shift is represented by the more intense Raman Stokes scattering. The higher intensity Raman Stokes is attributed to the higher occupancy at the lower vibrational energy level. Photodetector detect the phonon wavelength shift by the Raman Stokes. A plot of phonon intensity at a range of Raman shift then can be obtained.

Raman spectroscopy can be used to quantify and qualify the amount of amorphous and crystalline phase at the Si:H films. A sharp peak at 520 cm^{-1} and a broad peak at 480 cm^{-1} correspond to the crystalline and amorphous structure, respectively. The irregularity of the amorphous phase causes the broad Raman Stokes intensity. Microcrystallinity of the Si:H then can be quantified by the ratio of the crystalline and amorphous peaks.⁹² The Raman Spectrometer used was (Renishaw System 2000, Ar ion laser Coherent Innova 70, Leica INM 200).

2.4.3. Profilometer

Profilometer utilizes a diamond stylus to horizontally scan the vertical surface profile of a wafer by intimate contact with the wafer. Diamond is suitable due to its high wear-resistant property. The height and width of a profile on the surface as well as the surface roughness can be obtained from the vertical position signal of the stylus during scanning. The scanning by the stylus is performed for a specified distance at a constant contact force. A cantilever operating with spring mechanic principle resulted in the controls the contact force. The stylus radius, the scan speed, and the scan distance control the resolution at the horizontal direction. The vertical resolution is governed by

the stylus radius, the cantilever system, and is usually in the order of 1 nm. The profilometer (Dektak³, Veeco Instrument) used in this study has a stylus radius of 5 μm .

2.4.4. Ellipsometer

Ellipsometer can be used to obtain thin film properties such as RI and thickness in a quick non-destructive manner.⁹³ The RI and absorption coefficient, k , is the imaginary and the real part of dielectric constant, ϵ , respectively

$$\epsilon = (RI - ik)^2 \quad (15)$$

The assumptions involved in ellipsometry are that film properties are uniform throughout the thickness and that the film has a sharp interface with the substrate. In ellipsometry, incident polarized light at wavelength λ is measured for amplitude and phase change corresponds to the reflection and transmission once it arrived at the film surface. Dull ellipsometer technique is based on the minimization of the reflected polarized light received at the detector.⁹⁴ The minimization is performed automatically by a computer program by adjusting the polarizer and an analyzer angle, the final setting corresponds to the angle of incident, ϕ . The ratio of the intensity and the phase difference between the detector and the polarizer is defined as the complex reflection ratio, ρ . The ellipsometry angles, ψ (0° - 90°) and Δ (0° – 360°), are related to the ρ as follows

$$\rho = \tan (\psi) e^{j\Delta} \quad (16)$$

With the optimized polarizer and analyzer angles observed before, the Δ and ψ can be solved numerically. Based on these ellipsometry angles values, the real part of RI and

the extinction coefficient of the film can be obtained through Fresnel equations. Finally, the full-cycle film thickness, d , can be calculated by the following relationship

$$d = \frac{\lambda}{2(RI^2 - \sin^2(\varphi))^{1/2}} \quad (17)$$

The actual d can be confirmed with a profilometer measurement. The RI , however, should be approximately constant throughout the film and can be taken at face value. The ellipsometer used in this study was a Rudolph i1000 with He-Ne laser.

2.5. Electrical Characterization

2.5.1. Four-Point Probe

The resistance of a semiconductor material can be obtained from a four point probe measurement.⁹⁵ The measurement allows for the assessment of material's electrical property through its physical property. The resistance of a material, R , is defined as

$$R = \rho * L / A \quad (18)$$

where ρ is the resistivity, L is the feature length, A is the area parallel to the current flow, which is the product of feature width, W , and film thickness, t . Sheet resistance, R_s , is defined as the resistivity per unit thickness. As observed from Equation 18, the R_s has a unit of Ω/square .

A popular arrangement of the four probes is on an in-line. The sheet resistance measurement is performed by an intimate contact between the probe set and the film surface. The four-point probe (Alessi Industries) has a co-linear spacing, s , of 62.5 mil

between the needles. The probe set was connected to a digital multimeter (Keithley, 196 System DMM, Cleveland, OH) that acts as a current source and voltmeter. Current flows from an outer needle into the other outer needle, while the two inner needles measure the voltage drop. There are parasitic resistances, i.e., spreading resistance and contact resistance, associated with the two current probes. The two voltage probes, on the other hand, do not result in significant parasitic resistance due to the small or negligible current flowing through these probes. The R_S measurement from a four-point probe system then is more reliable than that utilizing a two-point system. The R_S follows the relation

$$R_s = F V_{23}/I_{14} \quad (19)$$

where V_{23} is the voltage drop measured at the inner probes, I_{14} is the current flows through the outer probes, and F is the correction factor. For thin film, i.e., film thickness is less or equal than half of probe spacing, s , the differential resistance is modeled as an annular configuration and the F value approximates to 4.53. For thick films, the differential resistance is modeled as a hemispherical configuration and the F -value approximates to $2 * \pi * s$.

2.5.2. Current-Voltage Analysis

Figure 11 shows the overall measurement set up in the study. Agilent 4155C Semiconductor Analyzer was used to measure the current-voltage characteristics of the TFTs and the capacitors. The substrate holder and the probe stages are placed inside a black box and are connected to vacuum lines. The substrate holder can be heated to

250°C during measurement. The blackbox is placed on a vibration-free table and is painted black inside and outside to minimize measurement noise from environment and light radiation. The Agilent 4155 C was connected to the probe needles at the blackbox via triaxial cables, triaxial to biaxial adapters, and biaxial cables. The triaxial cables consist of an inner force/sense conductor, a guard conductor and an outer ground conductor. The triaxial-biaxial adapter connects the force/sense conductor of the triaxial cable to the center conductor of the biaxial cable, and the guard of the triaxial cable to the outer conductor of the biaxial cable. The purpose of the guard conductor is to minimize the current loss from the device under testing to the Agilent 4155C. Proper grounding is required for the blackbox and measurement device. For TFTs, the current-voltage characteristics consist of 1) the output characteristic, i.e., the I_d , as a function of V_d and 2) the transfer characteristics, i.e., the I_d as a function of V_g . The source, drain, and gate electrodes of the TFT were probed with respective needle probes to measure the TFT electrical characteristics.

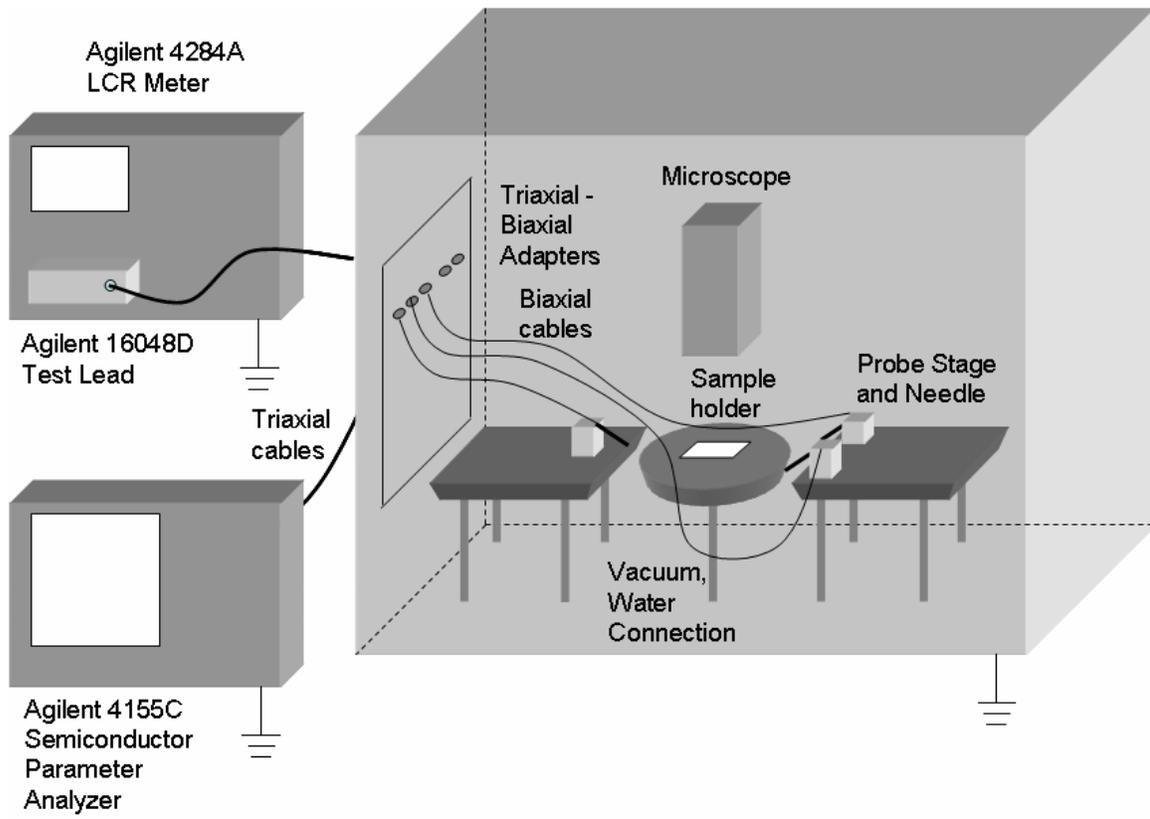


Figure 11. Measurement set-up for TFTs and capacitors.

Each measurement channel has a dual function as a voltage source and a current monitor. The linear staircase sweep measurement with 0.1 V/step which was performed at integration time of 640 μ s. The measurement was performed instantaneously, i.e., with hold time and delay time of 0 s. Hold time is defined as the time for the device to stabilize after bias while delay time is defined as the time for the device to rest after producing an output.

2.5.3. Capacitance-Voltage Analysis

Agilent 4284A was used to measure the capacitance-voltage characteristic of the capacitors. The capacitor's flatband voltage and interface state density can be extracted from the C-V characteristic. General mechanism of a C-V measurement includes a superimposition of a small sinusoidal AC signal onto a linear DC bias sweep over from the accumulation to the inversion region. The range of frequency of the AC voltage is from 10 Hz to 1 MHz. Three independent values of capacitance, conductance, and impedance can be determined by using an appropriate equivalent circuit of the capacitor in measure. A series resistance correction is performed on the fresh C-V curves.⁹⁶

CHAPTER III

N-CHANNEL AND P-CHANNEL A-SI:H THIN FILM TRANSISTORS WITH COPPER ELECTRODES

3.1. Introduction

This chapter investigated the performance of the n-channel and p-channel inverted staggered a-Si:H TFT with Cu/TiW gate, source, and drain electrodes prepared from the new plasma-based etching process. Characteristics of TFTs with Cu and Mo electrodes were compared. The reliability of the TFT was also investigated.

3.2. Experimental Method

Figure 12 shows the process flow of the fabrication of a-Si:H TFT with Cu/TiW electrodes. Plasma-enhanced chemical vapor deposition (PECVD) is a popular and reliable method in preparing high-quality a-Si:H thin films at a low temperature for a low cost. The self-aligned, inverted staggered, tri-layer TFTs were fabricated by using a 2-photomask process on Corning 7059 substrates.⁶ TiW and Cu were used for the gate, source and drain electrodes. TiW with a thickness around 150 nm was DC-sputtered to the glass substrate as a barrier and adhesion layer for Cu. The Cu film (about 50 nm) was subsequently DC-sputtered on top of the TiW layer without breaking the vacuum. The TiW/Cu gate electrode was defined by using the first mask and etched with reactive ion etching (RIE). The Cu layer was etched in a Cl₂ environment, followed by dilute HCl dipping to remove the CuCl_x compound.⁴² The TiW layer was etched with RIE by using

a CF_4/Cl_2 mixture. After the gate-metal etch, a sandwich of SiN_x/B -doped or intrinsic a-Si:H/ SiN_x tri-layer was deposited with by PECVD at 250°C without breaking the vacuum. The B-doped p-channel layer was deposited from a mixture of 50 sccm SiH_4 and 1 sccm B_2H_6 at 0.25 Torr and 85 mW/cm^2 . The intrinsic n-channel layer was deposited with 80 sccm SiH_4 at 0.20 Torr and 85 mW/cm^2 . After each layer was deposited, the chamber was purged with a series of high- and low-pressure argon (Ar) streams to remove the residue gas. After the tri-layer deposition, the top channel stop SiN_x layer was defined by a backlight exposure method by using the gate as the self-aligned mask.⁴² A heavily B-doped (p^+) or P-doped (n^+) a-Si:H layer was deposited as the source/drain ohmic contact layer by PECVD.^{3,30} The p^+ film was deposited at 0.5 Torr, 179 mW/cm^2 , 40 sccm B_2H_6 (5 % in H_2), 35 sccm SiH_4 , and 400 sccm H_2 . The n^+ film was deposited at 0.25 Torr, 179 mW/cm^2 , 35.5 sccm PH_3 (37 % in H_2), 35 sccm SiH_4 , and 400 sccm H_2 . All PECVD experiments were carried out in a parallel-plate reactor (Applied Materials AMP Plasma II) with a 50-kHz rf generator. After another set of Cu/TiW was sputter-deposited and defined with the plasma-based etch process, the p^+ layer was etched by using a mixture of CF_4 (2 sccm) and Cl_2 (8 sccm) at 100 mTorr and 300 W for about 2 minutes. All RIE experiments were performed in a parallel-plate reactor (PlasmaTherm 700) with a 13.56 MHz rf generator. The finished TFT was annealed in N_2 at 250°C for 1 hour to repair the plasma damage introduced during RIE.⁴² For electrical reliability testing, the TFT was bias-stressed with a V_g of 15 V and the source and drain electrodes were grounded. The TFT's transfer characteristics were measured with the Agilent 4155C semiconductor parameter analyzer. For the thermal-

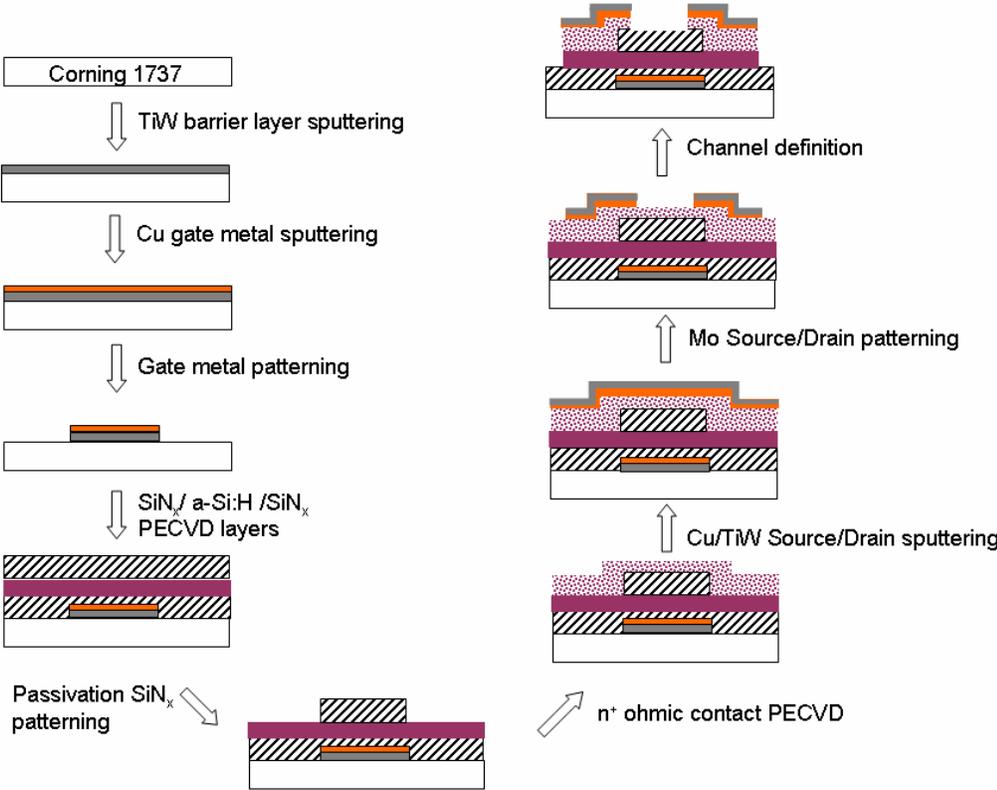


Figure 12. TFT fabrication flow.

stress tests, the TFT was annealed at 250°C in N₂. Transfer characteristics were measured before and after the thermal stress.

3.3. RIE of Cu Lines

Figure 13 shows both loosely and densely packed Cu/TiW interconnect structures successfully etched with the plasma-based process. There was no residue left after the TiW layer, which was confirmed by the SEM and EDX analysis.

3.4. Electrical Characteristics

3.4.1. Output Characteristic

Figure 14 shows the I_d vs. V_d curves of (a) a n-channel, and (b) a p-channel Cu TFT with all gate, source, and drain electrodes composed of Cu/TiW etched with by the plasma etching processes. The slight current-crowding in the low $-V_d$ region of the TFT in Fig. 14(a) is associated with the source/drain contact resistance. Since the number of electrons involved in the accumulation layer increases drastically with the increase of V_g , there should be a significant change in the I_d - V_d curve corresponding to each increase in V_g in the low $-V_d$ range. A low conductivity of the n⁺ layer or a non-ohmic contact at the source or drain region could hinder this increase.³⁰

The current crowding can be avoided by effectively removing the native oxide on the source and draining region before or during the n⁺ deposition step. Fig. 14(b) shows that ohmic contacts can be formed between the p⁺ layer and the p-type a-Si:H channel.

3.4.2. Transfer Characteristic

Figure 15 shows the transfer characteristics of p-channel and n-channel TFTs that have the same W and L dimensions. It is observed that the p-channel TFT has a lower I_{on}/I_{off} compared to the n-channel TFT. This is due to the former's low field-effect mobility (μ_{eff}), which also shows up as the low I_{on} in Fig. 15(b). There is an increase of charge scattering with the introduction of the B dopant to the active layer of the TFT. However, the above results demonstrate that both p- and n-channel TFTs with Cu/TiW electrodes prepared from by the plasma etching process have been successfully fabricated. Figure 16 shows the V_t value of a p-channel TFT at different W/L ratios. The V_t was calculated from the equation:

$$I_d^{1/2} = [1/2 * \mu * C * (W/L)]^{1/2} * (V_g - V_t) \quad (20)$$

at the saturation region. V_g needed to maintain constant drive current decreases with the increase of W/L ratio.⁹⁷ As such, in an ideal saturation condition, there should be a corresponding decrease of V_t with the an increase in W/L ratio. However, since the V_t of the TFT in Fig. 16 is high and its magnitude does not change significantly with the variation of W/L ratio, the p-channel layer's inherent characteristics, such as the high defect density, rather than the channel's physical dimensions, such as channel length, control the TFT performance. Based on the same W/L ratio, the n-channel TFT has a lower V_t than the p-channel TFT. Although the introduction of B to a-Si:H can change its conduction mechanism, it increases the defect density.

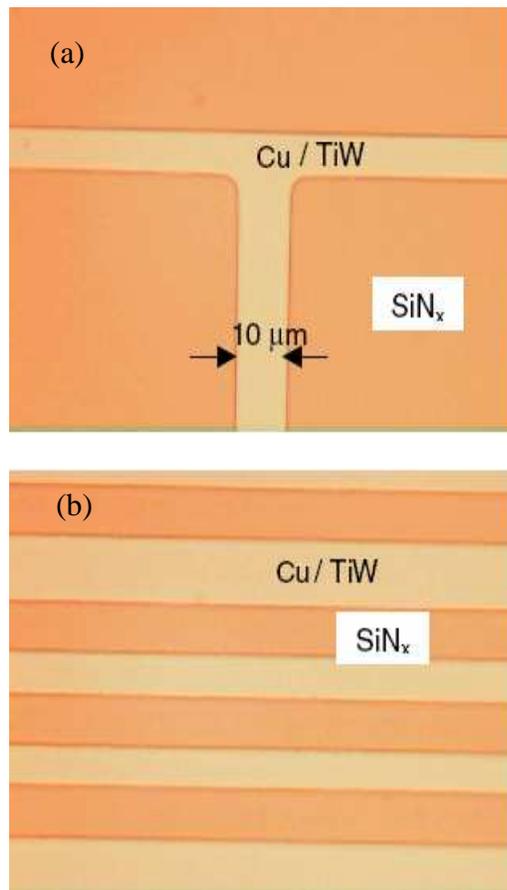


Figure 13. (a) Loosely and (b) densely packed Cu/TiW lines etched with plasma processes.

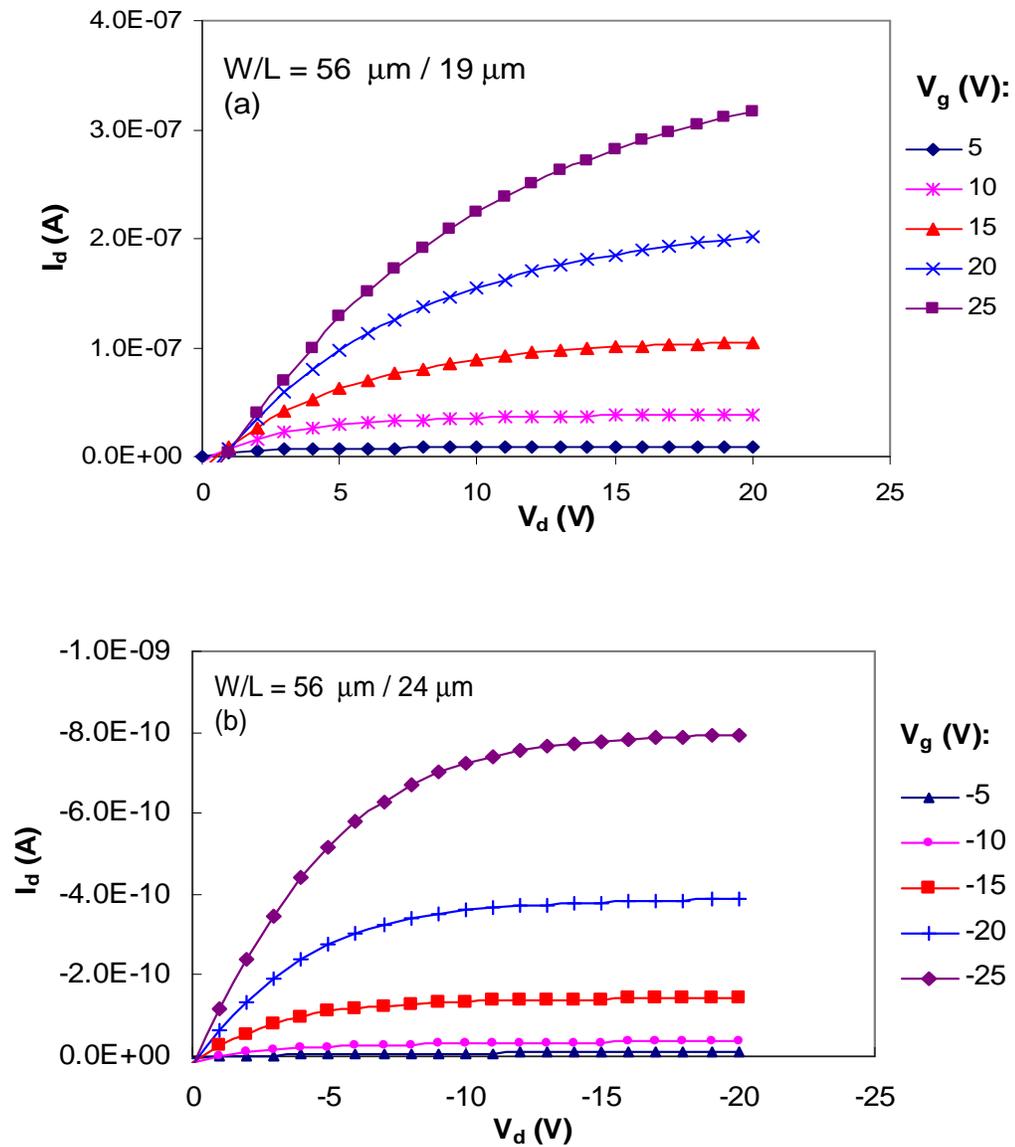


Figure 14. Output characteristics of (a) n-, and (b) p-channel TFTs with all Cu/TiW electrodes etched with plasma processes.

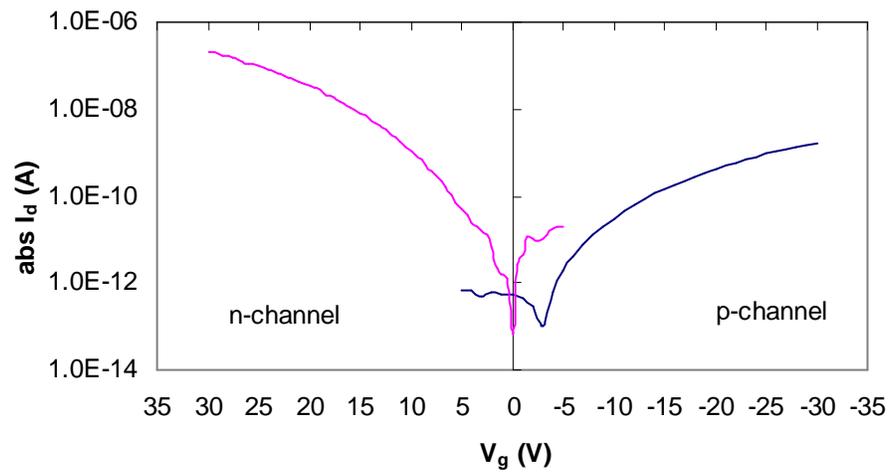


Figure 15. Transfer characteristics of n-channel and p-channel TFTs ($W = 64 \mu\text{m}$, $L = 49 \mu\text{m}$), $V_d = V_g$.

Figure 17 shows the field-effect mobility, i.e., μ_{eff} , as a function of the W/L ratio of the p-channel TFTs. The mobility decreases with the increase of the W/L ratio, which is similar to that of the conventional n-channel a-Si:H TFT. From general understanding, the increase of W/L ratio increases the electric field in the lateral direction. By assuming that carrier velocity is constant for every channel dimension, the increase of the electric field, therefore, corresponds to the decrease in carrier mobility. Gradual channel approximation assumes that the electric field in the lateral direction, i.e., along the W , is much higher than that in the longitudinal direction, i.e., along the L .⁹⁸ Channel resistance plays an important role in the case of TFTs that have similar W but different L . When the L is small, the contact resistance affects the μ_{eff} more than the channel resistance does.

Another important factor affecting the mobility is the a-Si:H channel/gate SiN_x interface quality, such as the physical sharpness, abrupt composition change, and dangling-bond concentration. They also influence other TFT characteristics, such as the V_t and the I_{on} , which are critical to the transistor's dynamic operation.⁹⁹ In this study, since the gate SiN_x /a-Si:H/top SiN_x tri-layers were deposited in the same chamber, the interface sharpness control is a critical issue. Previously, it was reported that when the gas residue from the gate SiN_x deposition step was not effectively pumped off before the p-channel layer was deposited, the resulting p-channel layer had a low conductivity and the TFT had deteriorated characteristics.⁴⁴ The gas-contamination problem was solved by applying several high-and-low-pressure Ar cycles to remove the gas residue from the gate SiN_x deposition process before the a-Si:H channel layer deposition. A distinct improvement of TFT characteristics, such as increasing μ_{eff} and decreasing V_t , was

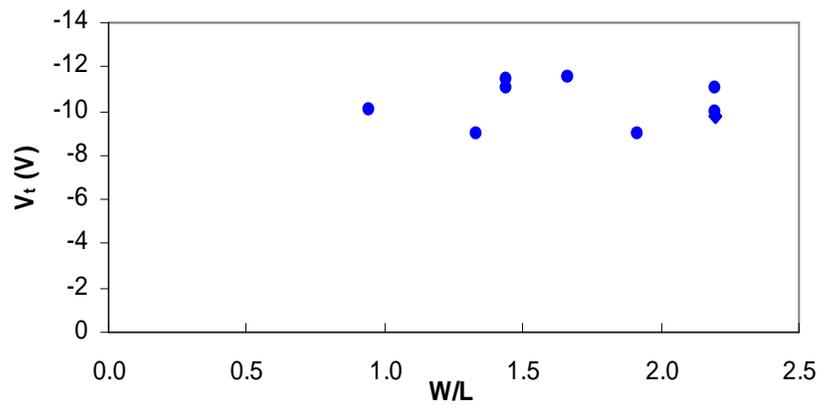


Figure 16. Threshold voltage of p-channel a-Si:H TFTs with Cu/TiW electrodes at different W/L ratios, Cu/TiW electrodes were etched with plasma processes.

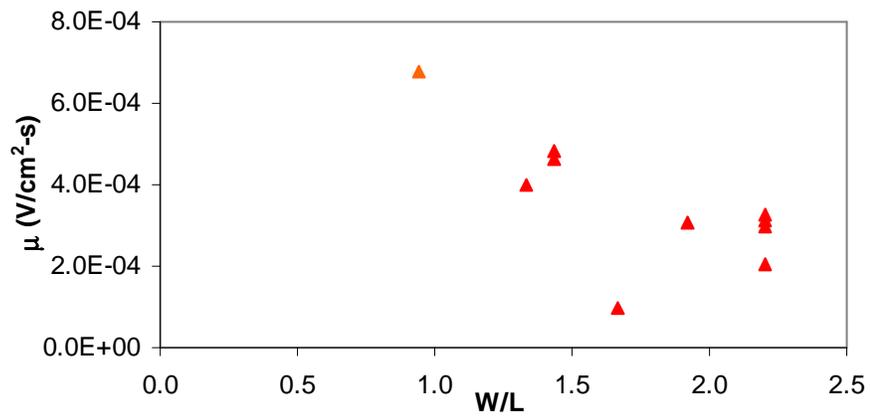


Figure 17. Field-effect mobilities of p-channel a-Si:H TFTs with Cu/TiW electrodes at different W/L ratios, Cu/TiW electrodes were etched with plasma processes.

observed with this kind of pumping method.

3.5. TiW Effectiveness

The Cu TFTs have similar performance compared to the TFTs prepared by the same fabrication process but with Mo gate, source and drain electrodes. For example, the p-channel Mo TFT with a $W/L \sim 3$ has a μ_{eff} of $2.4 \times 10^{-4} \text{ cm}^2/\text{V}\cdot\text{s}$ and V_t of -9 V .

These values are close to those of the p-channel TFT with Cu/TiW electrodes.

To observe the effectiveness of TiW as a barrier and adhesion layer of for the Cu layer, a p-channel TFT was annealed in N_2 close to the tri-layer deposition temperature, i.e., at 250°C , for more than 1 hour. Figure 18 shows that the annealing step slightly deteriorated the TFTs characteristics, e.g., shifting the transfer characteristic to a more negative V_g region. The shift increased with the annealing time. Previous investigations on stress bias suggest that the shift of the transfer characteristics corresponds to one or more of the following factors: formation of deep-gap states of the bulk a-Si:H film, increasing of a-Si:H/ SiN_x interface states, creation of charge-trapping centers, etc.¹⁰⁰

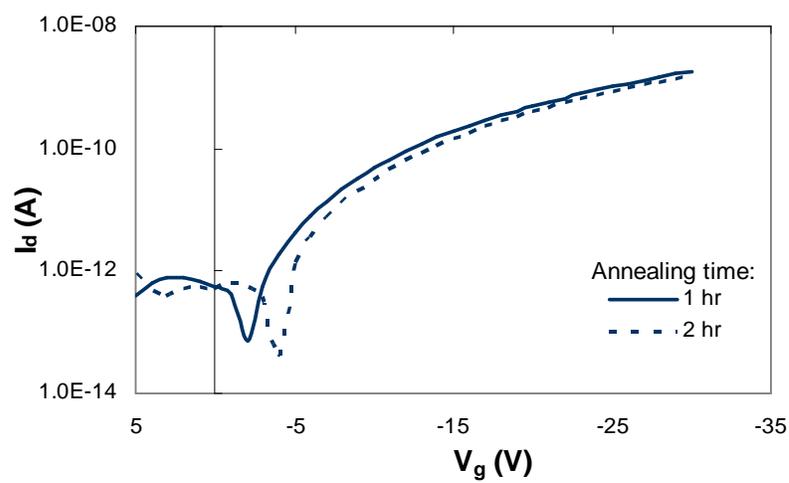


Figure 18. Transfer characteristics of a p-channel a-Si:H TFT ($W = 85 \mu\text{m}$, $L = 35 \mu\text{m}$) with Cu/TiW electrodes after 1 and 2 hours, 250°C annealing in N_2 .

Some of the loosely bounded hydrogen atoms in the original tri-layer structure, which function as passivation agents, were lost during annealing.¹⁰¹ The loss gives rise to the an increase of dangling bonds on the semiconductor layer, i.e., increasing the defect density. The I_{on}/I_{off} ratio of the TFT does not change with the annealing time. However, the onset of V_g increases with the increase of the annealing time. The TiW layer usually serves as a barrier layer hindering the Cu diffusion to its adjacent layers. Since the TiW layers were only deposited at the bottom of the Cu layers, they stopped the diffusion of Cu from the source and drain electrodes to the channel layer. However, since there is no barrier layer between the gate Cu and the SiN_x gate dielectric layer, it is possible that Cu diffuses into the SiN_x layer at a high temperature, which will be a potential reliability problem and needs to be investigated.

3.6. Reliability

The best way to investigate the reliability of the TFT is to examine its electrical characteristics with a gate bias stress method. For example, Figure 19 shows the transfer characteristics of an n-channel a-Si:H TFT with Cu/TiW gate, source, and drain electrodes at various stress times. All transistor characteristics deteriorate with the increase of stress time, which is similar to that the case of an a-Si:H TFT with Mo electrodes. This indicates that both bulk and interface properties were damaged by the stress condition. When extra defect states are created in the bulk a-Si:H, Fermi-level energy travels a longer distance to arrive at the conduction band tail. This shifts the

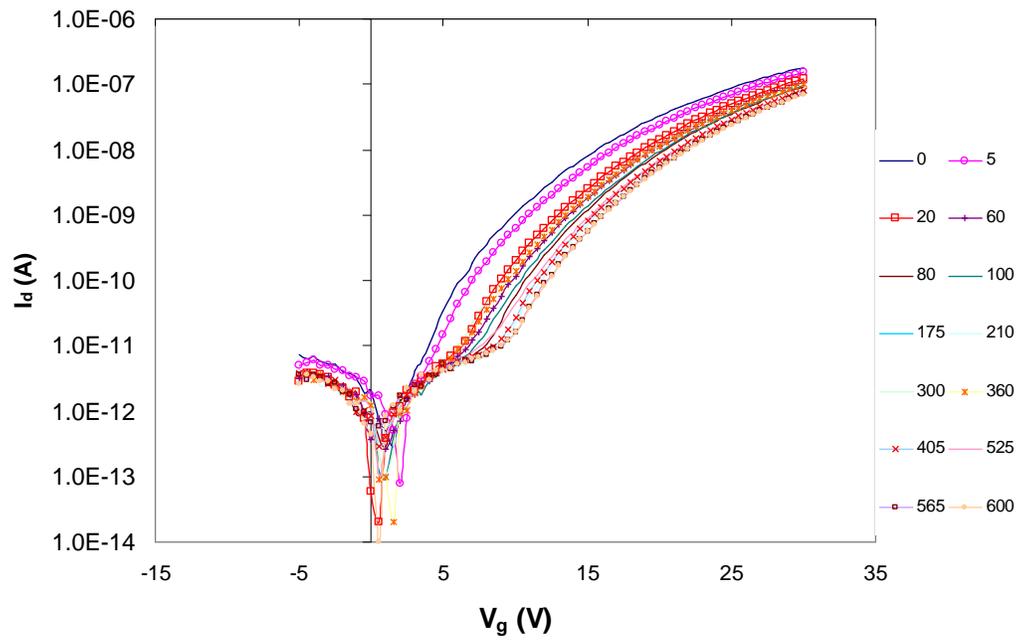


Figure 19. Transfer characteristics of an n-channel a-Si:H TFT ($W = 65 \mu\text{m}$, $L = 49 \mu\text{m}$) with Cu/TiW electrodes stressed for different times at $V_g = 15 \text{ V}$ and $V_d = V_s = 0 \text{ V}$.

transfer characteristics to the more positive direction for an n-channel TFT and to the negative direction for a p-channel TFT. The charge-trapping mechanism shifts the transfer characteristics by creating a space-charge region on the SiN_x -a-Si:H interface that inhibits the effectiveness of the V_g to accumulate electrons or holes in the channel.¹⁰⁰ If the deterioration is due to the interaction between Cu and gate SiN_x , e.g., diffusion of Cu into or through the SiN_x layer, the change is irreversible. However, if it is only due to the generation of defects in the bulk film or at the interface, the transfer characteristics should be recoverable after a thermal-annealing step. Figure 20 shows the TFT's threshold-voltage shift (ΔV_t) as a function of stress time before and after a 200°C, two-hour thermal annealing step. The curve marked "before annealing" represents the stress curve of the original TFT. The curve marked "after annealing" represents the stress curve of the TFT after being stressed for 600 minutes, followed by the thermal-annealing step. For the "original annealing" sample, the ΔV_t exhibits a power-law dependence on stress time, in which the ΔV_t drastically increased with stress time for the first 60 minutes and reached a steady value afterwards. Previous studies on stress-biased TFTs suggest that defect-states generation follows this type of time-dependence behavior.¹⁰⁰ This indicates that most defects in the TFT were generated at the early stage. If Cu was diffused into the gate SiN_x film, the increase of ΔV_t should have proceeded continuously with time until the whole SiN_x film was saturated with Cu and the diffusion stopped at the gate SiN_x /a-Si:H interface. This is unlikely because Cu is known to diffuse quickly in silicon and slowly in silicon nitride. Fig. 20 also shows that after the thermal-annealing step, the TFT's V_t returned to the same value as that of the original, unstressed TFT. In

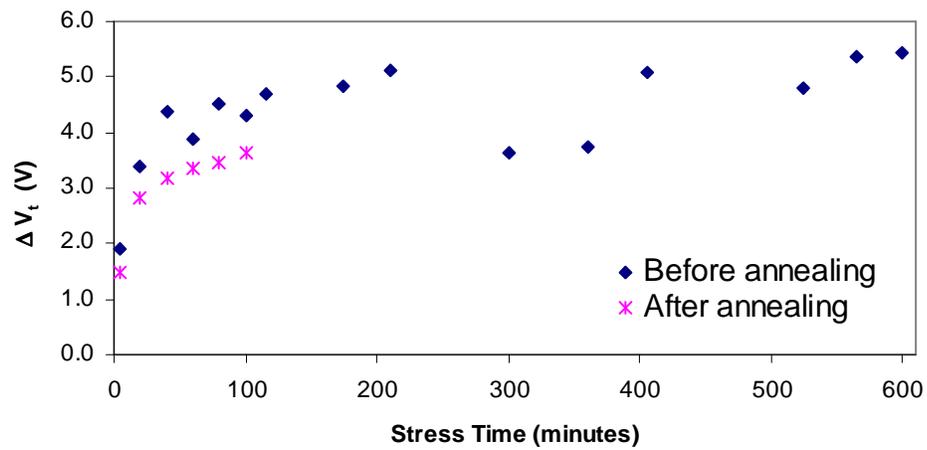


Figure 20. Threshold-voltage shift vs. stress time of an n-channel TFT ($W = 65 \mu\text{m}$, $L = 49 \mu\text{m}$) with Cu/TiW electrodes stressed at $V_g = 15 \text{ V}$ and $V_d = V_s = 0 \text{ V}$, \blacklozenge original film, $*$ film after 600-min stress followed by 200°C , 2-hour annealing.

addition, the “after annealing” curve is lower than the “before annealing” curve.

Therefore, the annealing step recovered the TFT’s transfer characteristics. This means that the Cu electrodes did not cause permanent damage to the TFT stress tests.

Therefore, the Cu/TiW electrode structure does not cause reliability concern in a-Si:H TFTs.

3.7. Summary

The p-channel and n-channel a-Si:H TFTs with Cu/TiW gate, source, and drain electrodes were successfully fabricated by utilizing a novel plasma-based Cu etching process. The bias stress result showed no reliability concern, even though the Cu gate electrode was in direct contact with the gate SiN_x film. Therefore, the new Cu etching process can be used to fabricate a large array of a-Si:H TFTs and CMOS-type circuits, which can be applied to a broad range of new products.

CHAPTER IV

OPTIMIZATION AND RADIATION EXPOSURE EFFECT ON AMORPHOUS SILICON THIN FILM TRANSISTORS

4.1 Introduction

Chapter III discusses the p-channel and n-channel a-Si:H TFTs with Mo or Cu as the electrodes. Previously, the TFTs were prepared with plasma generator with frequency of 50 kHz. In the first and second parts of this chapter, the fabrication and optimization of n-channel a-Si:H TFTs prepared with 13.56 MHz plasma generator will be discussed.

The objective for SiN_x film optimization is three-fold: 1) to achieve a RI in the range of 1.85-1.9, b) to achieve a low etch rate in buffered oxide etch (BOE) solution, c) to achieve a reasonable deposition time. The first objective follows the previous studies that correlates the SiN_x film properties such as *RI* to the electrical properties of the TFT such as V_t .⁵² The SiN_x *RI* can be correlated to the N/Si ratio of the film.¹⁰²

A low BOE etch rate corresponds to a sizeable amount of H₂ concentration in the film, which is important for film stress.⁵² Since the F atom reacts with Si to form soluble H₂SiF₆, a low BOE etch rate corresponds to a network of Si atoms being passivated with H₂. The third objective corresponds to the need to minimize particle accumulation in the plasma since particles can create paths for electron flow in the channel area from the source and drain. It will also lead to a more productive deposition scheme, which is economical.

The objective for P-doped n^+ Si film optimization is two-fold: a) to obtain a highly conductive film for ohmic contact of the Mo source and drain electrodes to the a-Si:H channel, and b) to obtain microcrystalline (μc) structure that corresponds to an even lower contact resistivity.¹⁰³

Lastly, the objective of n-channel TFT fabrication is to obtain TFT that demonstrate a high μ_{eff} , a low V_t , a high $I_{\text{on}}/I_{\text{off}}$. TFTs with the optimization of the a-Si:H channel deposited at different plasma power and pressure and with the already optimized gate dielectric and ohmic contact layers.

In the last part of the chapter, the effect of gamma-ray irradiation from a Co-60 source on the electrical characteristics of a-Si:H TFTs prepared at 13.56 MHz plasma frequency will be discussed. The possibility of recovering the damages using a thermal annealing method will also be discussed.

4.2 Film Optimization for n-channel a-Si:H TFT

4.2.1. Experimental Method

PECVD method utilizing the AMP-3300 Plasma II reactor with a capacitively coupled 13.56 MHz plasma RF frequency was used to grow independently (1) the undoped and doped a-Si:H, (2) the μc n^+ Si, and (3) the SiN_x films. The reactor underwent CF_4 and O_2 plasma cleaning and isopropanol wet cleaning after every 50 μm of the deposited film has been accumulated. Corning 1737 glass was used as the substrate for film growth and for the ESCA analysis of the films. Boron-doped silicon wafer with resistivity of 10-80 $\Omega\text{-cm}$, doping concentration of 10^{14} - 10^{15} cm^{-3} , (100)

orientation, were used for the substrates for other surface analytical methods such as Raman and FTIR. Before each PECVD deposition, the glass and the wafer substrates were dipped in HF (48%) : DI H₂O solution (1:30) for several seconds to remove the native oxides. After the substrate was loaded to the heated PECVD chamber, a pump down to 1 mTorr was performed by a combination of roughing and booster pumps. Several alternate high and low pressure purging with N₂ or Ar followed. Systematic independent depositions at 300°C were performed to observe the effect of various experimental parameters such as pressure, RF power, and gas phase composition on each film. Film thickness was obtained from the step height measured with a stylus profilometer (Dektak³, Veeco Instrument). For SiN_x films, the *RI* value was measured with ellipsometer with HeNe laser at 632.8 nm (i1000, Rudolph Incorporated). The deposition rate was measured by dividing the film thickness over deposition time. For etch rate determination, the SiN_x film was etched in a 6:1 buffered oxide (BOE, Ashland Chemical, Columbus, OH) solution for 15 s. The etch rate was measured by dividing the step height over etch time, i.e., 15 s. The resistivity of the n⁺ Si film was measured with a four-point probe. ESCA analysis (Axis Ultra, Kratos Analytical Incorporated) was performed to analyze the Si-N bonds in the film. Raman analysis (Renishaw System 2000, Ar ion laser Coherent Innova 70, Leica INM 200) were performed to observe the crystallinity of the n⁺ μc-Si contact layer.

4.2.2. Optimized SiN_x

The increase of SiH₄ flow rate at the 10-35 sccm range at constant flow rates of N₂ (720 sccm) and NH₃ (100 sccm), pressure (500 mTorr) and plasma power (350 W),

increases the SiN_x deposition rate (23.5-26.5 nm/min), etch rate (160 -340 nm/min) and RI (1.671-1.88). The increase of SiH_4 flow rate contributes to an increasing amount of Si precursors that participate in the growth process. The increase of precursors corresponds to the increase of SiN_x film deposition rate. The SiN_x films obtained from a higher deposition rate exhibit high BOE etch rate which probably corresponds to the porous structures of the film. The optimum SiN_x was found to be deposited with a 20 sccm SiH_4 by taking into account a reasonably high deposition rate (25.5 nm/min), a reasonably low etch rate (300 nm/min), and a RI in the range of 1.85-1.9.

The increase of NH_3 flow rate up to 120 sccm resulted in the increase of SiN_x deposition rate (25-27 nm/min) at fixed gas precursor flow rates (720 sccm N_2 , 20 sccm SiH_4), pressure (500 mTorr) and plasma power (350 W). Beyond this point the deposition rate decreases drastically. NH_3 is the source of the N for the growth of SiN_x . The increase of NH_3 gas phase in the system increases the N precursors for surface reaction which corresponds to the increase of deposition rate. Since NH_3 dissociates into among others NH_x and H, it also becomes a source of H in the plasma. It is possible that beyond a certain NH_3 flow rate, the decomposing H resulting in a more pronounced H etching mechanism⁵⁴ that corresponds to the drastic decrease of deposition rate. The H etching mechanism can be related to the increase of etch rate with the increase of NH_3 flow rate (160-300 nm/min). From this set of experiment, an optimum SiN_x condition (26 nm/min deposition rate, 240 nm/min etch rate, RI of 1.89) corresponds to a NH_3 flow rate of 80 sccm.

The SiN_x deposition rate increases with the increase of power up to 350 W and decreases beyond this point for a fix gas flow rates of SiH₄/N₂/ NH₃ = 20 sccm/720 sccm/80 sccm and pressure of 500 mTorr. This is the critical power that determines the dominating mechanism of the growth process, i.e., etching through hydrogenation and ion bombardment or the deposition through the surface adsorption and reaction.⁵⁴ From this set of data, the optimum SiN_x film with the *RI* at 1.89 range corresponds to a power of 300 W.

Table 3 shows the characteristics of SiN_x film deposited with different N₂ flow rate at a pressure 500 mTorr, power 300 W, and fixed gas precursors of 20 sccm SiH₄ and 80 sccm NH₃. The optimized condition is at N₂ flow of 600 sccm.

Table 3. Properties of SiN_x film deposited at different N₂ flow rate

N ₂ Flow rate (sccm)	Refractive Index	Deposition Rate (nm/min)	BOE Etch Rate (nm/min)
400	1.879	24	23
600	1.875	22	20
720	1.874	25	25
800	1.882	24.3	26
1000	1.89	24.4	19

Finally, with the fixed deposition conditions from the above optimization steps (20 sccm SiH₄, 80 sccm NH₃, 500 mTorr pressure, 300 W power) and by varying the N₂

flow rate, an optimum SiN_x film quality, i.e., a deposition rate of 0.22 kA/min, an etch rate of 2 kA/min, and an RI of 1.87 was observed for an N_2 flow rate of 600 sccm.

Figure 21 shows the ESCA analysis of SiN_x film deposited at various optimization conditions. All films show Si-O bond, possibly due to leak at the PECVD chamber.

SiN_x deposited at higher NH_3 and N_2 flow rates (Figs. 21a, 21b) show significant Si-N bonds compared to the SiN_x deposited at lower NH_3 flow rate (Figs. 21c, 21d). Furthermore, the optimized SiN_x also shows the suppression of Si-O(N) bond. This bond oxide bond might be from the formation of native oxide at the surface. The relatively low Si-N bonds could correspond to the increase of H concentration in the film, resulting in a denser film.

4.2.3. Optimized n^+ $\mu\text{c-Si}$

P-doped Si films deposited with a gas phase H_2/SiH_4 ratio < 100 showed resistivity values $> 20 \Omega\text{-cm}$. These films also exhibited amorphous structure characteristic. Highly conductive and transparent $\mu\text{c-Si:H}$ films were achieved when the H_2/SiH_4 ratio was increased to 100. Table 4 shows the change in film resistivity with the change in H_2/SiH_4 ratio. The most conductive n^+ $\mu\text{c-Si:H}$ film, i.e., with resistivity lower than $0.4 \Omega\text{-cm}$, was deposited with a gas phase composition of SiH_4 (20 sccm), H_2 (2000 sccm), PH_3 (93% in H_2 , 3 sccm) at 750 mTorr and 600 W.

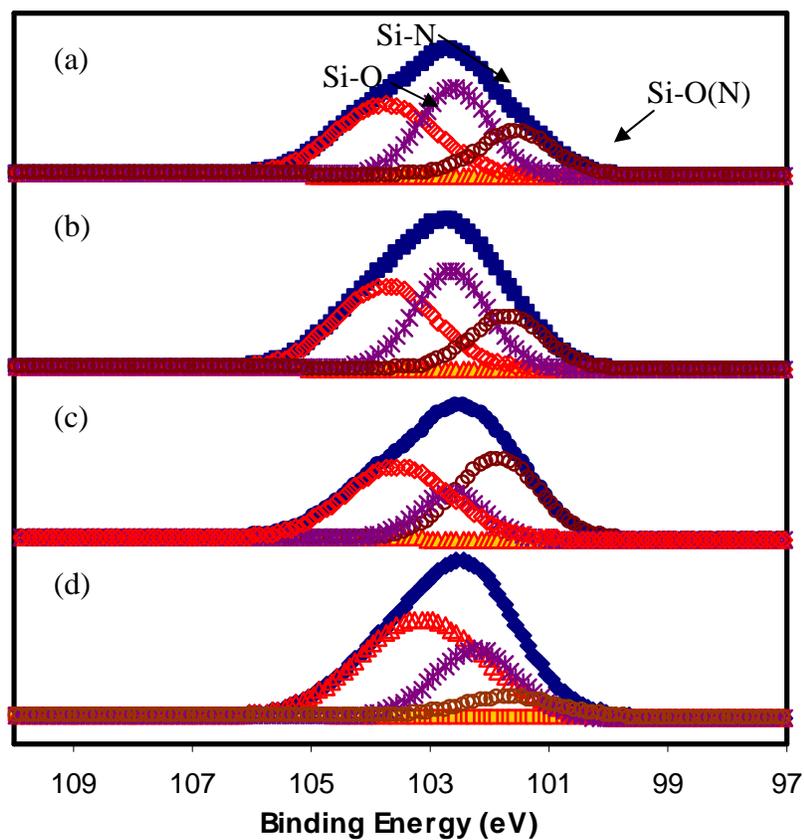


Figure 21. ESCA analysis of SiN_x film deposited with (a) SiH_4 (35 sccm)/ NH_3 (100 sccm)/ N_2 (720 sccm) at 350 W, 500mTorr, (b) SiH_4 (20 sccm)/ NH_3 (140 sccm)/ N_2 (720 sccm) at 350 W, 500mTorr, (c) SiH_4 (20 sccm)/ NH_3 (80 sccm)/ N_2 (720 sccm) at 300 W, 500mTorr, (d) SiH_4 (20 sccm)/ NH_3 (80 sccm)/ N_2 (600 sccm) at 300 W, 500mTorr.

Table 4. Resistivity value for n^+ Si film deposited at different H_2/SiH_4 ratio. Films were deposited with SiH_4 (20 sccm), H_2 (2000 sccm), PH_3 (93% in H_2 , 3 sccm) at 750 mTorr and 600 W.

H_2/SiH_4 Ratio	Resistivity (Ω -cm)
0	490
40	315
100	12

Table 5 shows that PH_3 concentration in the gas phase controls the n^+ Si film conductivity. For instance, 3 sccm of PH_3 in the gas phase corresponds to film with the highest conductivity. A +/- 33 % change to the PH_3 gas phase concentration, i.e., 1 sccm change in flow rate, resulted in increase of resistivity value of several orders of magnitude. The high gas phase PH_3 concentration possibly related to the incorporation of electrically inactive P in the film, while the low gas phase concentration simply did not supply enough dopant.

Table 5. Resistivity value for n^+ Si film deposited at different PH_3 gas phase concentration. Films were deposited at SiH_4 (20 sccm), H_2 (2000 sccm) at 750 mTorr and 600 W.

PH_3 (93 % H_2) (sccm)	Resistivity ($\Omega\text{-cm}$)
0	700
2	300
3	0.2
4	0.4
5	12

Figure 22 shows the Raman spectra of the optimized n^+ Si film feature a peak that can be deconvoluted into a minor amorphous phase peak at 480 cm^{-1} and a major crystalline phase peak at 520 cm^{-1} .

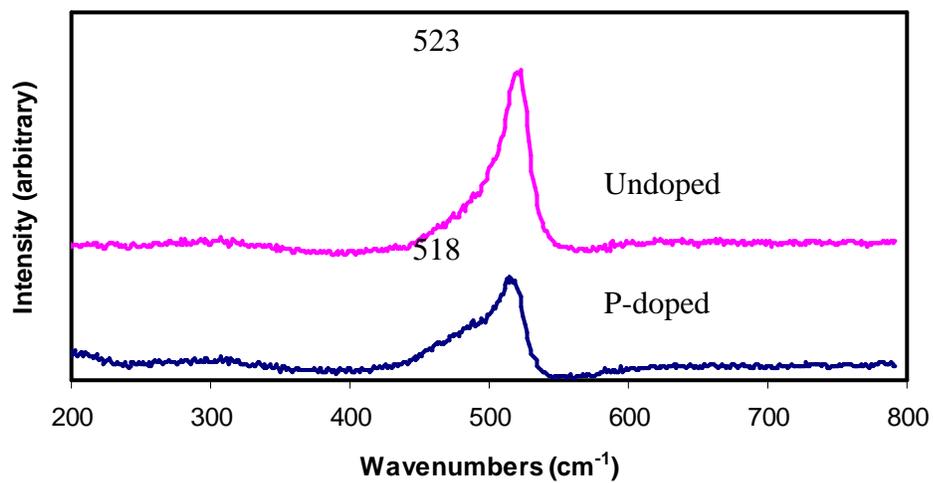


Figure 22. Raman spectra of undoped and P-doped $\mu\text{c-Si}$ films.

4.3 n-channel a-Si:H TFTs from Optimized Films

4.3.1. Experimental Method

The optimized PECVD films are used in the channel, gate dielectric, and the top passivation of the TFT. 100 nm-thick Mo films deposited with magnetron sputtering were used for gate, source and drain electrode. A DC instead of RF plasma was used to obtain a denser film at 400 W for 30 minutes. Corning 1737 was used as the substrate of the complete TFTs. Pre-sputtering for the target was performed with 13.56 MHz rf plasma for 20 min with 100 sccm Ar flow rate. To prepare the glass substrates for TFT fabrication a thorough cleaning with RCA solutions were performed.¹⁵ The first RCA solution (5:1:1 H₂O: H₂O₂: NH₄OH, 80°C) was used for the removal of insoluble organic contaminants. The second RCA solution (1:20 HF: H₂O, room temperature) was used for the removal of the native silicon oxide layer. The final RCA solution (6:1:1 H₂O: H₂O₂: HCl, 80°C) was used for the removal of ionic and metal contaminants. The TFT fabrication procedure was composed of (1) photolithography of the 100 nm Mo gate layer (Q4000 mask aligner, Quintel Corp) and wet etching (H₃PO₄:HNO₃:CH₃COOH:H₂O, 16:1:1:2) (2) deposition of 300 nm SiN_x gate dielectric/50 nm a-Si:H channel/250 nm top passivation SiN_x layers in one pump down, (3) back side lithography using the gate pattern as the self-aligned mask, followed by wet etching (HF:H₂O, 1:3) of the top SiN_x layer, (4) deposition of n⁺ and Mo layers, followed by patterning with the second mask, (5) wet etching of Mo, followed by reactive ion etching of the n⁺ layer (400 W, 100 mTorr, Cl₂:CF₄ 8 sccm:2 sccm), and (6) thermal annealing of the plate at 250°C in atmosphere for 1 h. TFTs with a-Si:H channel

deposited at 150, 200, and 250 mTorr, at either 80 or 200 W were fabricated. The SiN_x films were deposited at 300°C with a gas phase composition of 20 sccm SiH₄, 80 sccm NH₃, 600 sccm N₂, at 500 mTorr pressure, 300 W plasma power. The n⁺ ohmic contact was deposited with 20 sccm SiH₄, 3 sccm, 2000 sccm H₂ at 750 mTorr and 600 W plasma power.

Agilent 4155C semiconductor parameter analyzer with Labview 7.0 interface was used to measure the TFT's output and transfer characteristics. To shield light interference during measurement, the probe station (S-1160, Signatone Incorporated) was placed inside an Al box that was painted in black. The black box was grounded and tri-axial cables were used to minimize electrical noise.¹⁰⁴ The least-square method was used to extract the V_t and the μ_{eff} from the $I_d^{0.5}$ as a function of V_g curve at the saturation region.¹⁰⁵

4.3.2. Electrical Characteristics

Figure 23 shows the transfer and output characteristics of an n-channel TFT fabricated with a-Si:H channel deposition at 150 mTorr, 80 W and 300°C. The TFT ($W/L = 2.7$) shows a μ_{eff} of 0.46, a V_t of 3.3 V, and an I_{on}/I_{off} ratio of 6×10^8 . The I_{on}/I_{off} ratio for all TFTs was in the desirable 10^7 - 10^8 range. The high driving current and low leakage current confirm the functional characteristic of the TFT. The lack of current crowding, i.e., the significant drop of I_d at the low V_d range in Fig. 23b was due to the highly conductive μc n⁺ layer ohmic contact. Specifically, the contact resistance of the n⁺ ohmic contacts contributes to about 1% of the on-state total resistance of the a-

Si:H TFT in Fig. 23. Furthermore, since the microcrystalline n^+ film was deposited using a high hydrogen concentration and a considerably high plasma power, it etched the native oxide formed on the channel overlap region.

Figure 24 shows that the quality of the a-Si:H channel clearly affected the TFTs electrical characteristic. For instance, as shown in Fig. 24a, the TFTs with the a-Si:H channel deposited at 150 mTorr demonstrated higher μ_{eff} and lower V_t at different ratio of W to L (W/L ratio) compared to the TFTs with channel deposited at higher pressure, e.g., 200 and 250 mTorr. The a-Si:H film deposition rate was found to increase with pressure, which is expected since the increase in pressure corresponds to the increase of gas residence time. The lower deposition rate of a-Si:H deposited at 150 mTorr might correspond to a denser film in which most of the Si dangling bonds is passivated by H instead of being chemically etched. Pressure also affects the ion bombardment of the plasma since it increases collisions among dissociated species which includes ions, neutrals, and radicals.¹⁰⁶ It is possible, that the a-Si:H deposited at 150 mTorr to have less defect density due to the lower ion bombardment possibility compared to the a-Si:H deposited at higher pressure. The deposition rate of a-Si:H increases with power. This is related to the plasma power effect on the feed gas dissociations. The μ_{eff} of the TFTs did not show significant change in μ_{eff} with the increase of power from 80 W to 200 W. The plasma power at this range might correspond to a-Si:H films with similar degrees of defect density, and thus TFT with similar range of μ_{eff} . However, from Fig. 24b, it is observed that the TFTs with a-Si:H channel deposited at 80 W has lower V_t compared to the TFTs fabricated with a-Si:H channel at 200 W. A high V_t at high plasma power

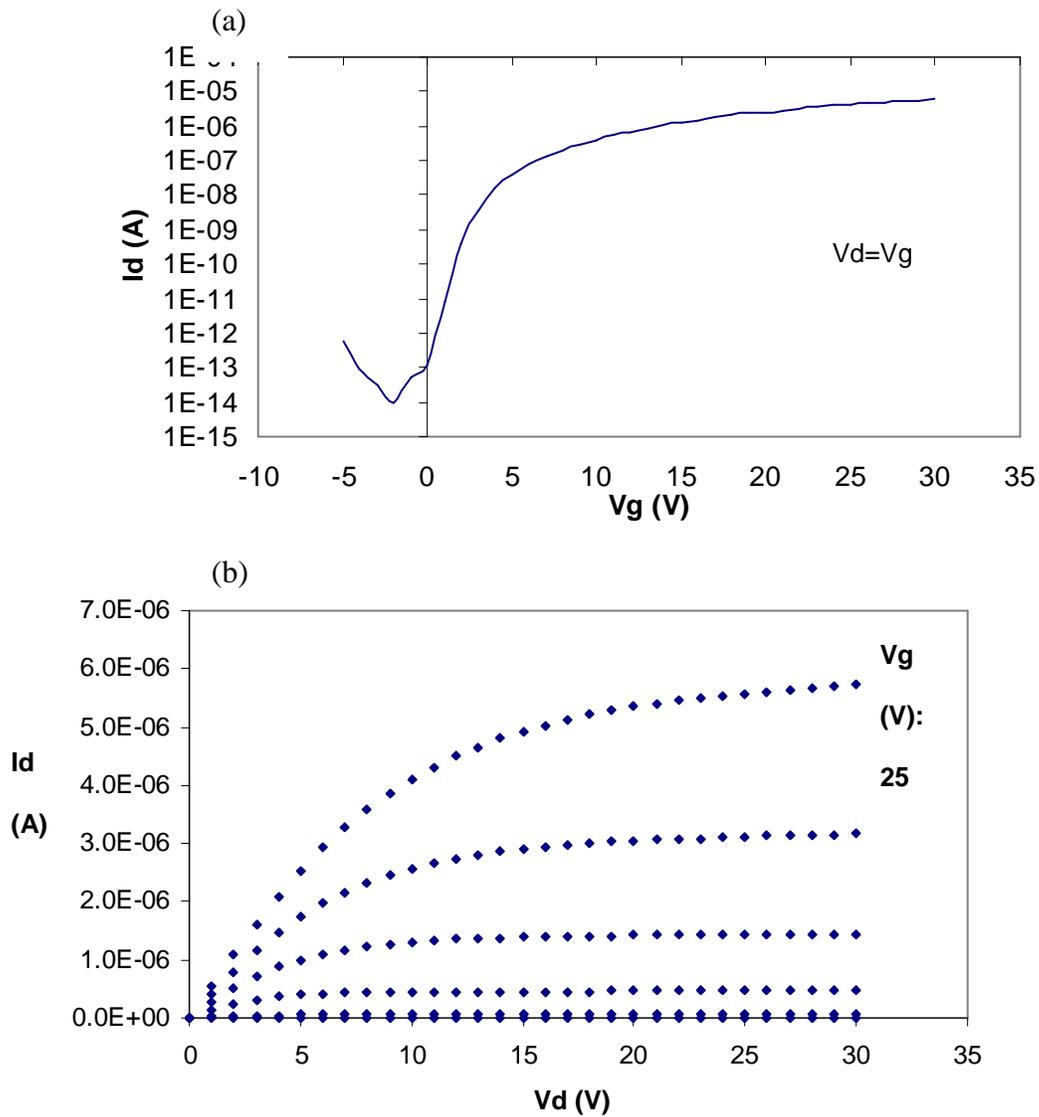


Figure 23. (a) Transfer characteristics and (b) output characteristics of an n-channel TFT. $W/L = 2.7$.

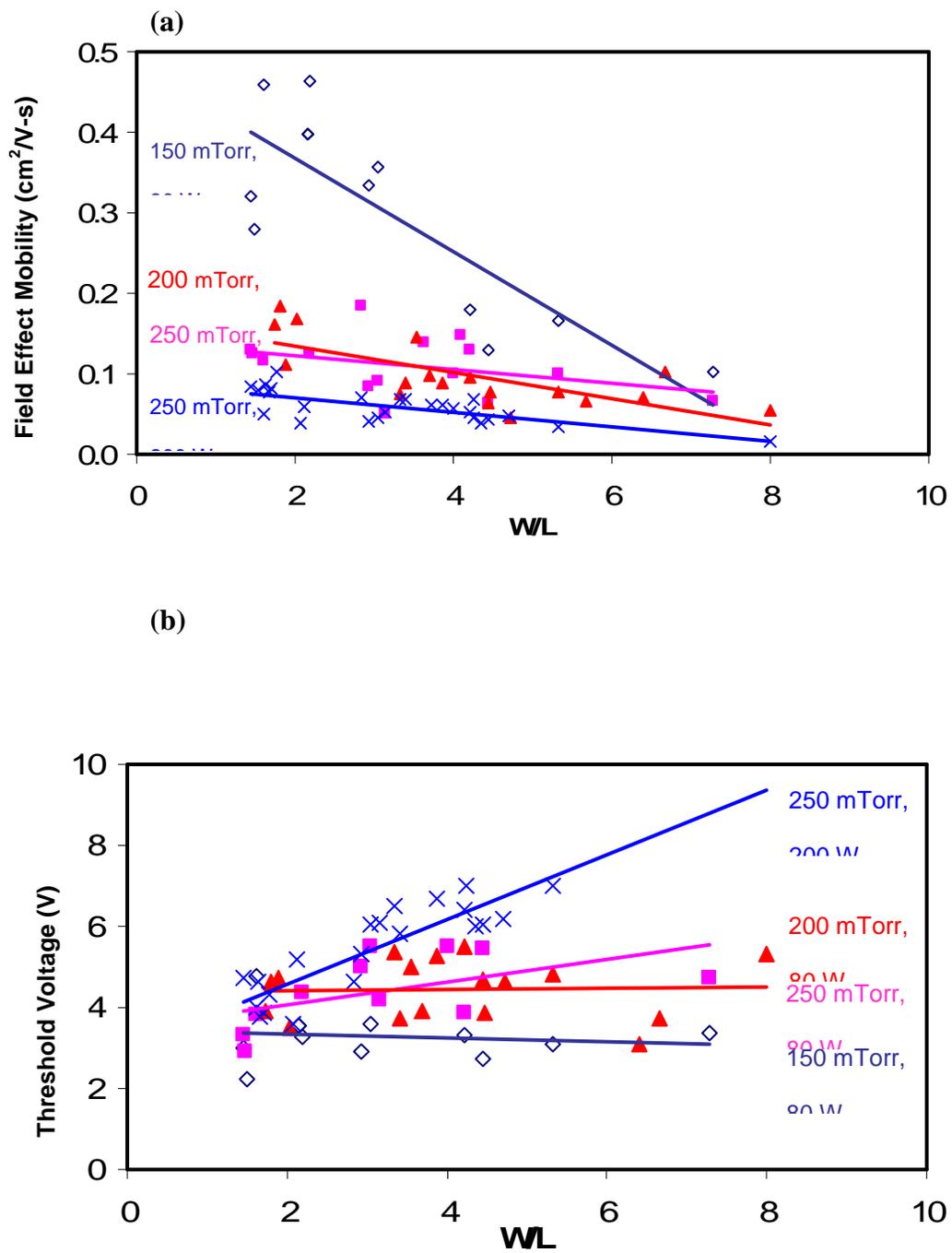


Figure 24. (a) Field effect mobility and (b) threshold voltage as a function of W/L for n-channel TFT.

condition could be contributed to the deterioration of a-Si:H-SiN_x interface properties, e.g., a rough surface and a high interface trapped charge centers.¹⁰⁷ To minimize the extrinsic contamination on film interface, the gate SiN_x/a-Si:H/top SiN_x tri-layers were deposited in the same chamber with one pump down. Even then, the interface sharpness control is still a critical issue. For instance, when the gas residue from the gate SiN_x deposition step was not effectively pumped off before a p-channel layer was deposited, the deposited p-channel layer had a low conductivity and the TFT had less desirable characteristics.²

The channel dimension affects the TFT characteristics. For instance, μ_{eff} decreases with the increase of W/L . At the same channel W , TFT with a shorter channel L , i.e., with a larger W/L ratio, experiences a higher electric field along the channel W , i.e., the lateral direction than that along the channel L , i.e., the longitudinal direction. Gradual channel approximation assumes that the change in lateral direction electric field is much higher than that in the longitudinal direction.⁹⁸ By assuming a constant carrier velocity for every channel dimension, an increase of the electric field corresponds to a decrease in carrier mobility. The V_g needed to maintain constant drive current decreases

with the increase of W/L ratio⁹⁷ which should correspond to a decrease of V_t with the increase of W/L . However, there are no significant changes in V_t observed with the change in W/L . This could be caused by the channel's inherent properties, such as defect density, rather than the physical dimension, such as channel length, controls the device performance.²

Figure 25 and Table 6 show that TFTs fabricated with the same metal electrodes but with the PECVD films deposited at 13.56 MHz exhibit higher μ_{eff} , lower V_t , and higher I_{on}/I_{off} ratio than the TFTs deposited at 50 kHz frequency. For instance, for the same W/L of 2.7, a TFT deposited with 50 kHz plasma showed a μ_{eff} of $0.2 \text{ cm}^2/\text{V}\cdot\text{s}$, V_t of 16.5 V, and I_{on}/I_{off} of 10^5 . High precursor dissociation efficiency, i.e., denser plasma, has been associated with high plasma frequency which resulted in higher film deposition rate.¹⁰⁸

Low frequency plasma, on the other hand, has been associated with high ion bombardment that contributes to the high film defect density. The improvement on the μ_{eff} , V_t , and I_{on}/I_{off} characteristic was due to the improved quality of the SiN_x , n^+ ohmic contact and the a-Si:H channel.

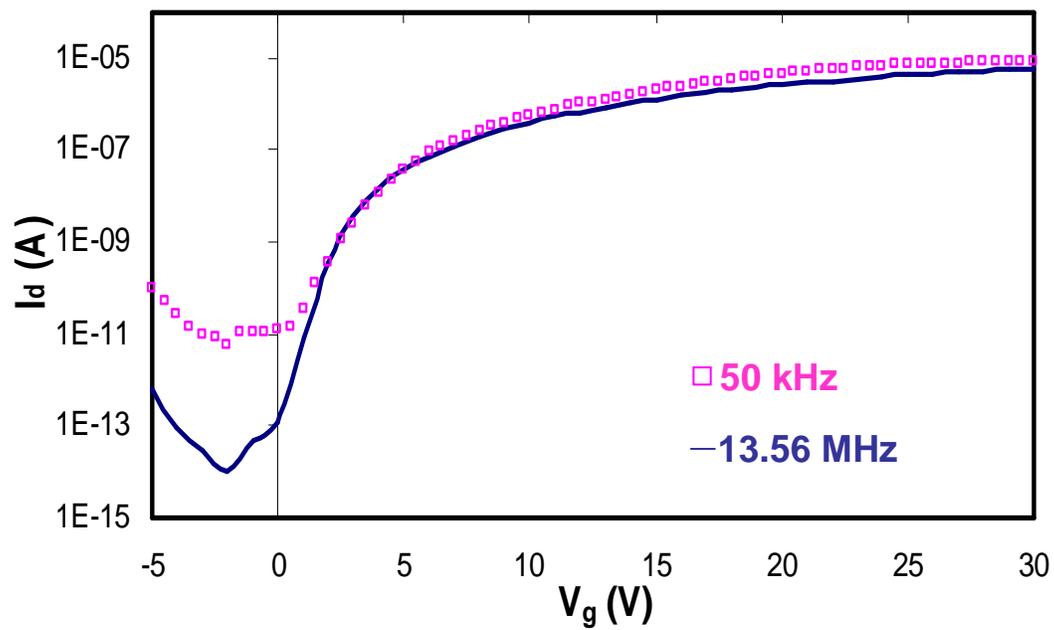


Figure 25. Comparison of the transfer characteristics of n-channel TFTs prepared from 50 kHz or 13.56 MHz plasma generator. $W/L = 2.7$.

Table 6. Comparison of the electrical properties of TFTs prepared at 50 kHz and 13.56 MHz plasma generator. $W/L = 2.7$.

	50 kHz (a-Si:H= 250 mTorr, 80 W)	13.56 MHz (a-Si:H= 150 mTorr, 80 W)
μ_{eff} ($\text{cm}^2/\text{V}\cdot\text{s}$)	0.08	0.46
V_t (V)	5	3.3
$I_{\text{on}}/I_{\text{off}}$	2×10^6	6×10^8

4.4 Co-60 Irradiation on n-channel a-Si:H TFT

4.4.1. Experimental Methods

Figure 26 shows the cross-section schematic of a self-aligned, inverted staggered, tri-layer a-Si:H TFT used. The TFTs were fabricated with a simple two-photomask process on the Corning 1737 glass.⁶ Mo metal gate (100 nm-thick) was sputter-deposited, defined with a lithography mask, and then wet etched. The SiN_x gate dielectric (300 nm-thick), a-Si:H channel (50 nm-thick), and SiN_x top passivation (250-nm thick) layers were deposited with plasma enhanced chemical vapor deposition (PECVD) in a one pump down process. Depositions were carried out in a parallel-plate

reactor at a substrate temperature of 250°C and a 13.56 MHz power supply. After the top SiN_x was defined with a backlight exposure step using the Mo gate as the mask and etched with a HF solution, a microcrystalline n^+ ($\mu\text{c-n}^+$) layer (50-nm thick) was deposited by PECVD followed with a sputtered Mo layer (100-nm thick). The source and drain areas were defined with the second lithography mask followed by wet etching of Mo and reactive ion etching of the n^+ layer. The complete TFT was annealed at 250°C for 1 hour in air to repair the plasma etch induced damages.⁶⁰ The TFT was characterized for the transfer characteristics $\log(I_d)\text{-}V_g$ and output characteristics $I_d\text{-}V_d$ using an Agilent 4155C semiconductor parameter analyzer.

The finished TFTs were irradiated with a Co-60 source at a rate of 33.2 kGy/hr continuously for a total cumulative dose of 100, 300, 400, and 600 Gy, separately. The TFT plate was located at a distance of 15 cm from the Co source. A few plates were shielded with a 1.25 cm-thick Al alloy plate (7075-T6, 90 % Al, 5.6 % Zn, 2.5 % Mg, 1.6 % Cu, and 0.23 % Cr). There was no difference on the irradiation effect between Al shielded or non shielded plates. Before and after irradiation, the TFT's electric characteristics were measured. There was a one-week time delay between sample irradiation and measurement. For the irradiated TFT plate, it was immediately annealed

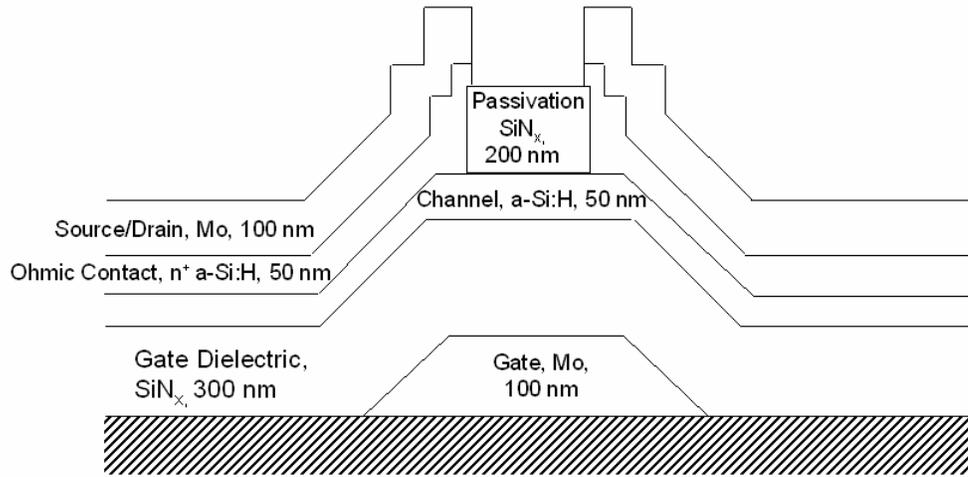


Figure 26. Schematic of the n-type a-Si:H TFT.

at 250°C in air for one hour after the measurement. The electrical characteristics were then measured to detect the post annealing effect.

4.4.2. Irradiation Effects

Figure 27 shows the transfer characteristics of TFTs before and after irradiation and after post-irradiation annealing. It is clear that the irradiation process deteriorated the transistor, e.g., lowered the I_{on} , increased the sub-threshold slope (S), and increased the V_t . During irradiation, Si-H bonds were broken, which created dangling bonds and trapped charges.⁵⁹ The shift of the transfer characteristics to the positive V_g direction indicates a delay of the electron accumulation layer formation at the positive V_g . In contrast, a previous work on Co-60 irradiation of a-Si:H TFT for the x-ray imaging application showed a different result.⁵⁹ In ref. ⁵⁹, during the irradiation process, the TFT was biased with a negative V_g . Therefore, holes were attracted to the channel a-Si:H/SiN_x gate dielectric interface. Electrons from the electron-hole pairs generated from the irradiation were easily attracted to the interface and formed neutral charges. In our work, the TFT was not biased during irradiation. After irradiation, when the measurement was started from negative V_g , holes from the electron-hole pairs were attracted to the a-Si:H/SiN_x gate dielectric interface. When the V_g changed from negative to positive, electrons attracted to the above interface were combined with holes, which delayed the formation of an electron accumulation layer and therefore, the caused a large

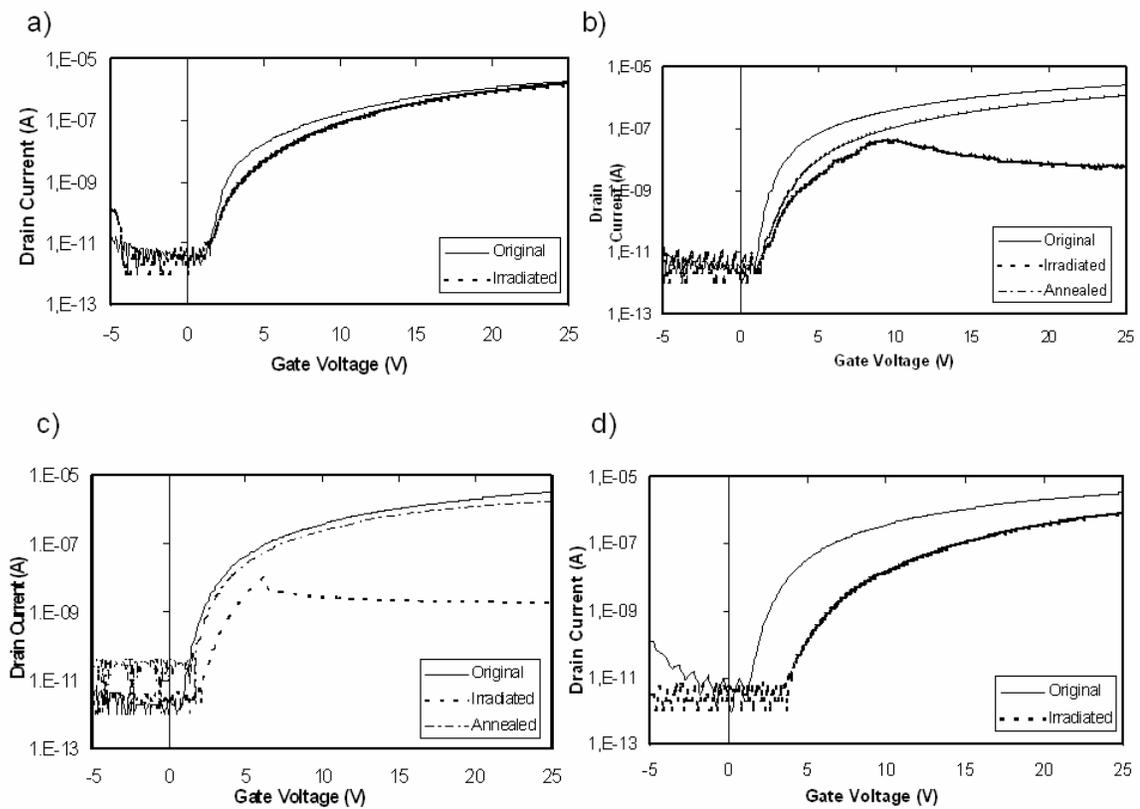


Figure 27. Transfer characteristics before and after a) 100 Gy, b) 300 Gy, c) 400 Gy and d) 600 Gy irradiation and after post-radiation annealing (for b) and c)). $W/L = 2.9$, $V_d = 10$ V.

V_t . Fig. 27 also shows that the ΔV_t , which is defined as $(V_{t,post-irradiation} - V_{t,pre-irradiation})$, increases with the increase of the radiation dosage. This indicates that the amount of electron-hole pairs generated increased with the radiation dosage due to the increase of the number of broken SiH bonds. This result also opposes the Ref. ⁵⁹4 report that ΔV_t decreased with the increase of the radiation dosage. The Ref. ⁵⁹4 sample was biased with a negative V_g during irradiation, which caused the formation of an electron accumulation layer early.

Fig. 27b) and c) shows that I_d first increases with the increase of V_g until near the saturation region and then decreases with the further increase of V_g . This only occurred at medium dosage, i.e., 300 and 400 Gy, irradiated TFTs but not at the low, i.e., 100 Gy, or high, i.e., 600 Gy, dosage irradiated TFT. It might involve a more complicated mechanism than just the electron-hole pairs generation in the bulk film. For instance, the decrease of the I_d at the high V_g might be related to the high concentration of electrons at the a-Si:H/SiN_x interface which caused the Coulomb blockade effect. The gate SiN_x film and the interface might be damaged by the irradiation process, which affected the charge transfer to the interface at the high V_g . For example, at the high dosage irradiation condition, e.g., 600 Gy, the above Coulomb blockade might disappear due to more fixed positive charges existed at the interface. However, more studies are required to verify these assumptions.

Figure 28 shows the output characteristics of TFTs irradiated under the same

conditions as Fig. 27. The irradiated TFT has an I_{on} about one order of magnitude lower than that of the non-irradiated TFT. However, the ohmic contact behavior remains. For the ohmic contact formation, the depletion width for carrier penetration between the metal and the highly doped n^+ layer is governed by the semiconductor's built in potential, dielectric constant and doping concentration.¹ Since the $\mu\text{-}n^+$ ohmic layer was highly conductive, the radiation condition did not decrease its conductivity or the quality of its interfaces with Mo or a-Si:H layer.

Figure 29 shows the contribution to the ΔV_t from charge traps at the a-Si:H/SiN_x interface (ΔV_{it}) and the gate dielectric (ΔV_{ot}), as shown below

$$\Delta V_t = \Delta V_{it} + \Delta V_{ot} \quad (21)$$

The ΔV_{it} was calculated from the difference in V_t and the voltage at the midgap state (V_{mg}) of the TFT at the pre- and post irradiation states,¹⁰⁹ i.e.,

$$\Delta V_{it} = (V_t - V_{mg})_2 - (V_t - V_{mg})_1 \quad (22)$$

where subscript 1 and 2 correspond to the pre- and post-irradiation states, respectively.

The V_{mg} is the voltage corresponded to the I_d that is approximated by a linear extrapolation of the sub-threshold I_d to the 10^{-15} A range.¹³ Once the ΔV_{it} has been extracted, the ΔV_{ot} can be calculated from Equation 21.

Fig. 29 also shows that at the high irradiation dosage range, i.e., 300 to 600 Gy, the change in ΔV_t with the increase of the irradiation dosage was mainly contributed by the increase of ΔV_{it} as opposed to ΔV_{ot} . The ΔN_{it} , which is defined as the difference in

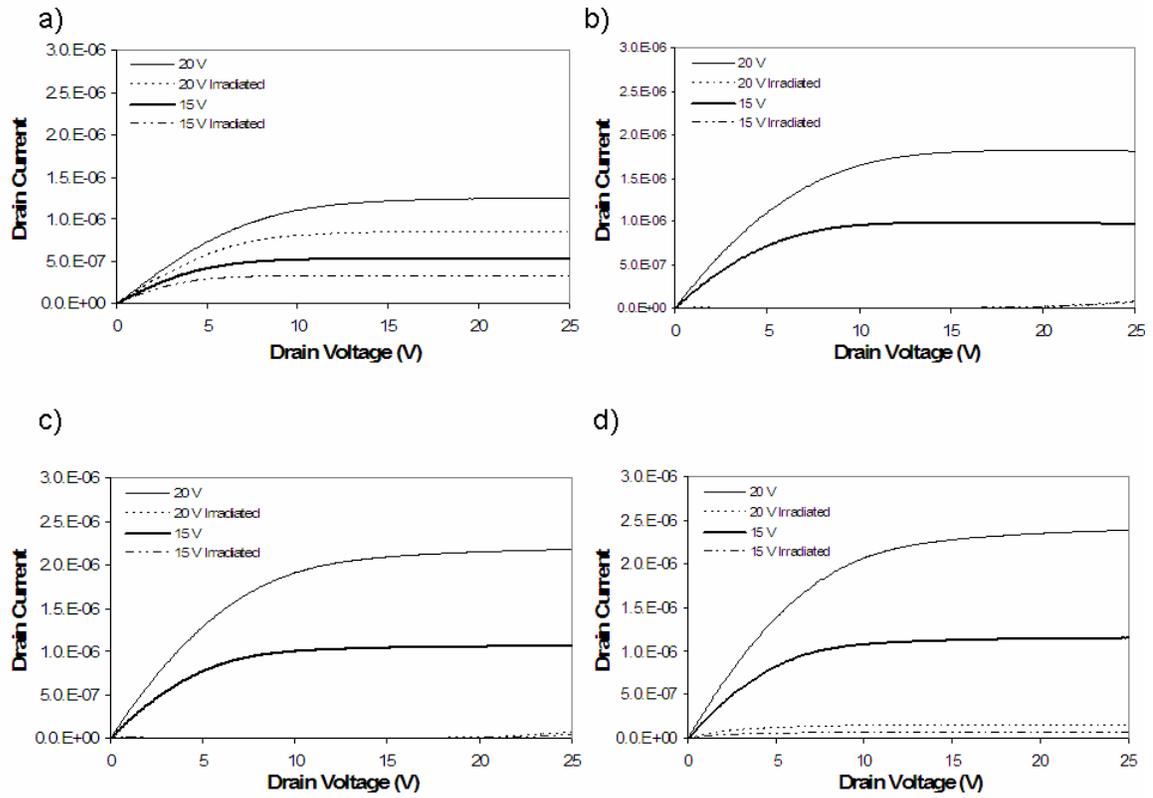


Figure 28. Output characteristics of a) 100 Gy, b) 300 Gy, c) 400 Gy and d) 600 Gy irradiated TFTs.

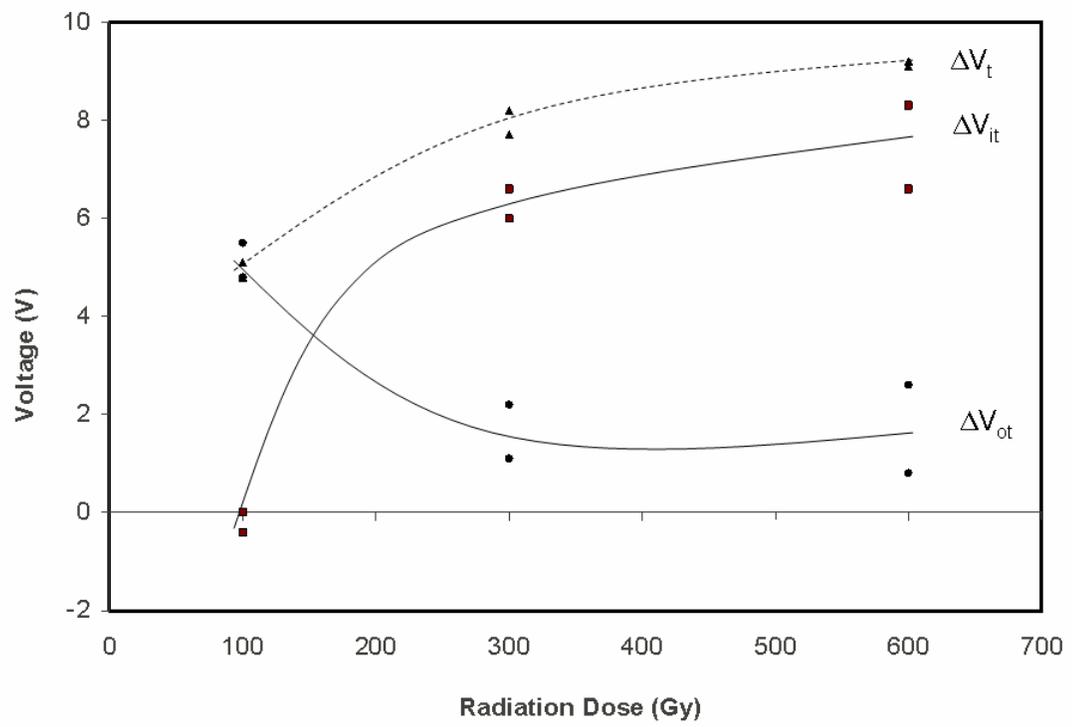


Figure 29. ΔV_t , ΔV_{it} , ΔV_{ot} as functions of the irradiation dosage. $W/L = 5.3$.

the interface state density of the postirradiation ($N_{it, post-irradiation}$) and pre-irradiation TFT ($N_{it, pre-irradiation}$), can be determined by the following relation.¹⁰⁹

$$\Delta N_{it} = \Delta V_{it} C_{ox} / q \quad (23)$$

where C_{ox} is the capacitance of the SiN_x dielectric. For instance, ΔN_{it} 's of TFTs were $3.1 \times 10^{11} \text{ cm}^{-2}$, $4.71 \times 10^{11} \text{ cm}^{-2}$, and $6.51 \times 10^{11} \text{ cm}^{-2}$ at the irradiation dosage of 100, 300, and 600 Gy, respectively.

The ΔN_{it} can also be calculated from the change of interface state density (N_{it}) before and after irradiation. The following equation can be used to estimate the N_{it} ¹¹⁰

$$S = (k T / q) \ln (10 (1 + (C_d + q N_{it})/C_{ox})) \quad (24)$$

where the S extracted is extracted from the transfer characteristics, C_d is the depletion layer capacitance, C_{ox} is gate dielectric capacitance, and q is electronic charge. ΔN_{it} 's from this calculation method were different from those calculated using Equation 23. However, they follow the same trend, i.e., the ΔN_{it} increases with the increase of the irradiation dosage.

There is a significant decrease of μ_{eff} at the post-irradiation state compared to the pre-irradiation state. For instance, μ_{eff} 's of the same TFT before and after 300 Gy irradiation were $0.117 \text{ cm}^2/\text{V}\cdot\text{s}$ and $0.014 \text{ cm}^2/\text{V}\cdot\text{s}$, respectively. The degradation of μ_{eff} is mainly due to deterioration of the interface states. After irradiation, the I_{on}/I_{off} ratio was lower than before irradiation. This is due to the decrease of I_{on} because the I_{off} 's were the same.

4.4.3. Annealing Effect

Fig. 27b) and c) also show transfer characteristics of TFTs after post-irradiation annealing at 250°C. The annealing step recovered the TFT characteristics toward the pre-irradiation condition, i.e., increases of μ_{eff} and I_{on}/I_{off} as well as decrease of V_t . Furthermore, the decrease of I_d at a high V_g was not observed. The N_{it} was also decreased to close to that before irradiation value. Other than the electron-hole pairs generation, the Co-60 irradiation at the dosage range in this study probably did not result in the loss of H. Otherwise, the electrical characteristics could not be recovered by thermal annealing.¹¹¹

4.5 Summary

SiN_x , n^+ and a-Si:H films deposited by PECVD method with 13.56 MHz plasma generator have been optimized for n-channel a-Si:H TFT application. The SiN_x film was

optimized for low etch rate, high deposition rate, and RI in the range of 1.85-1.9. The n^+ film exhibited a microcrystalline structure and prominent ohmic contact behavior. The n-channel TFTs showed significant improvements, e.g., higher μ_{eff} , lower V_t , and higher I_{on}/I_{off} ratio, over the previous TFTs fabricated with PECVD films deposited with 50 kHz plasma generator.

Co-60 irradiation and annealing effects on inverted staggered, self-aligned, tri-layer a-Si:H TFTs have been studied. Irradiation resulted in the shift of the transfer characteristics to a more positive voltage and the ΔV_t increased with the increase of the irradiation dosage. The irradiation process also increased the interface state density as well as decreased μ_{eff} and I_{on}/I_{off} ratio, but did not affect the ohmic contact behavior. These effects are due to the electron-hole pair generation in the bulk film and damages to the interface. Thermal annealing almost restored all electrical characteristics to the pre-irradiation state.

CHAPTER V

NONVOLATILE HYDROGENATED-AMORPHOUS-SILICON THIN-FILM- TRANSISTOR MEMORY DEVICES*

5.1 Introduction

The essential feature of a memory device is its ability to store and retrieve some kind of electrical entities when needed. This chapter discusses a simple method of fabricating nonvolatile a-Si:H TFTs and the preliminary observation on charge storage and erase characteristics.

5.2 Experimental Method

Figure 30(a) shows the structure of the memory device that is similar to that of a conventional inverted, trilayer TFT of Fig 30 (b), except that the gate dielectric is composed of the $\text{SiN}_x/\text{a-Si:H}/\text{SiN}_x$ structure. This is a floating gate transistor of which the a-Si:H layer in the gate dielectric layer serves as a charge retention medium. The memory function depends on the charge trapping and detrapping capabilities of this inserted layer. The TFT fabrication procedure shown in Figure 31 is composed of (1) patterning of a 100 nm Mo gate layer, (2) deposition of gate dielectric/50 nm a-Si:H

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channel/250 nm top passivation SiN_x layers in one pump down, (3) back side lithography using the gate pattern as the self-aligned mask, followed by wet etching ($\text{HF}:\text{H}_2\text{O}$, 1:3) of the top SiN_x layer, (4) deposition of n^+ and Mo layers, followed by patterning with the second mask, (5) wet etching of Mo ($\text{H}_3\text{PO}_4:\text{HNO}_3:\text{CH}_3\text{COOH}:\text{H}_2\text{O}$, 16:1:1:2), followed by reactive ion etching of the n^+ layer, and (6) thermal annealing of the plate at 250°C in atmosphere for 1 h. All SiN_x , a-Si:H, and n^+ layers were deposited by plasma enhanced chemical vapor deposition at 300°C of which the details can be found in Refs. ^{6,42}. The gate dielectric is composed of 150 nm SiN_x /4, 7, or 9 nm a-Si:H/150 nm SiN_x . For comparison purpose, the conventional a-Si:H TFT without an a-Si:H inserted in the gate dielectric layer was prepared with the same process conditions.

The TFT's transfer characteristics were measured with Agilent 4155C semiconductor parameter analyzer. The least-squares method was used to extract the parameters such as the V_t and the μ_{eff} from the $I_d^{0.5}$ as a function of V_g curve at the saturation region. Figure 32 shows the completed control and memory TFTs with $W = 85 \mu\text{m}$ and $L = 35 \mu\text{m}$.

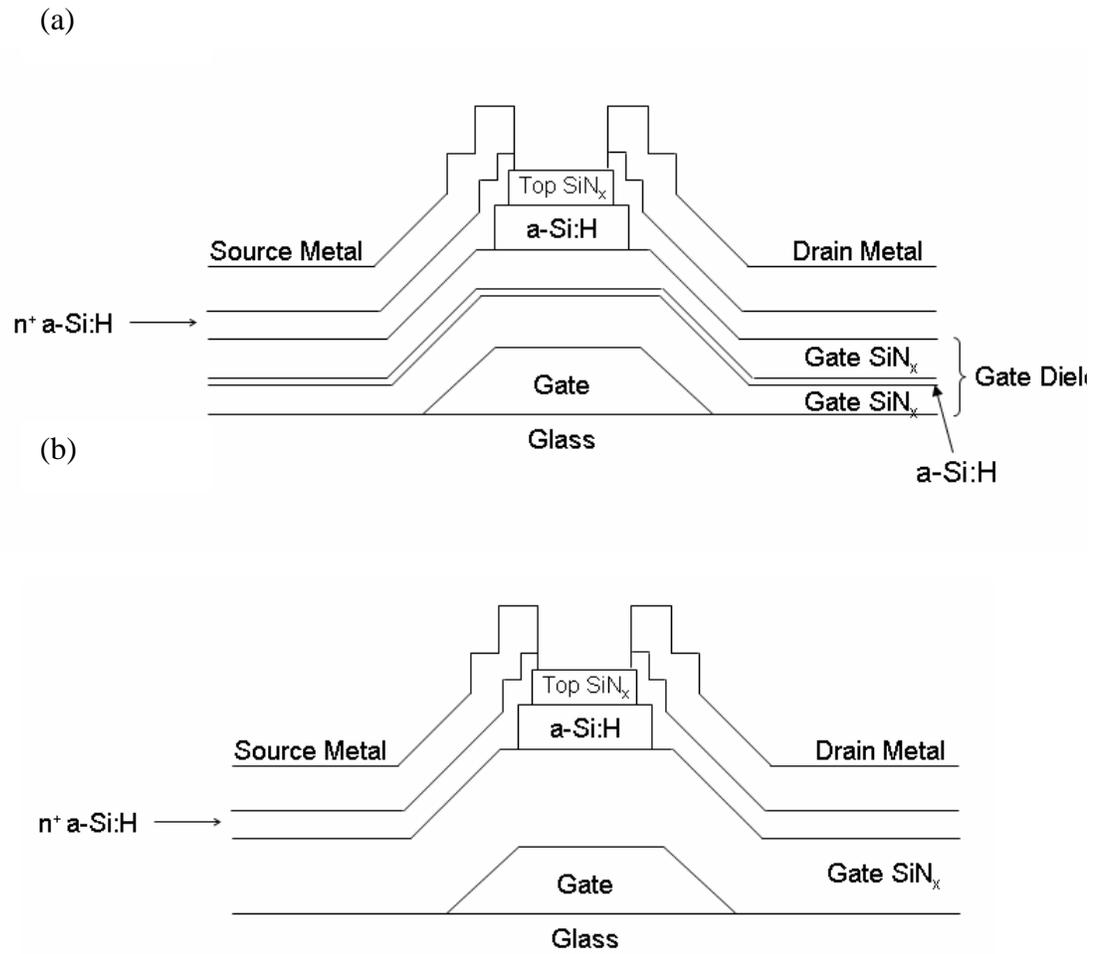


Figure 30. Cross-sectional view of an (a) a-Si:H TFT with a-Si:H layer embedded in the gate SiN_x layer, and (b) conventional a-Si:H TFT.

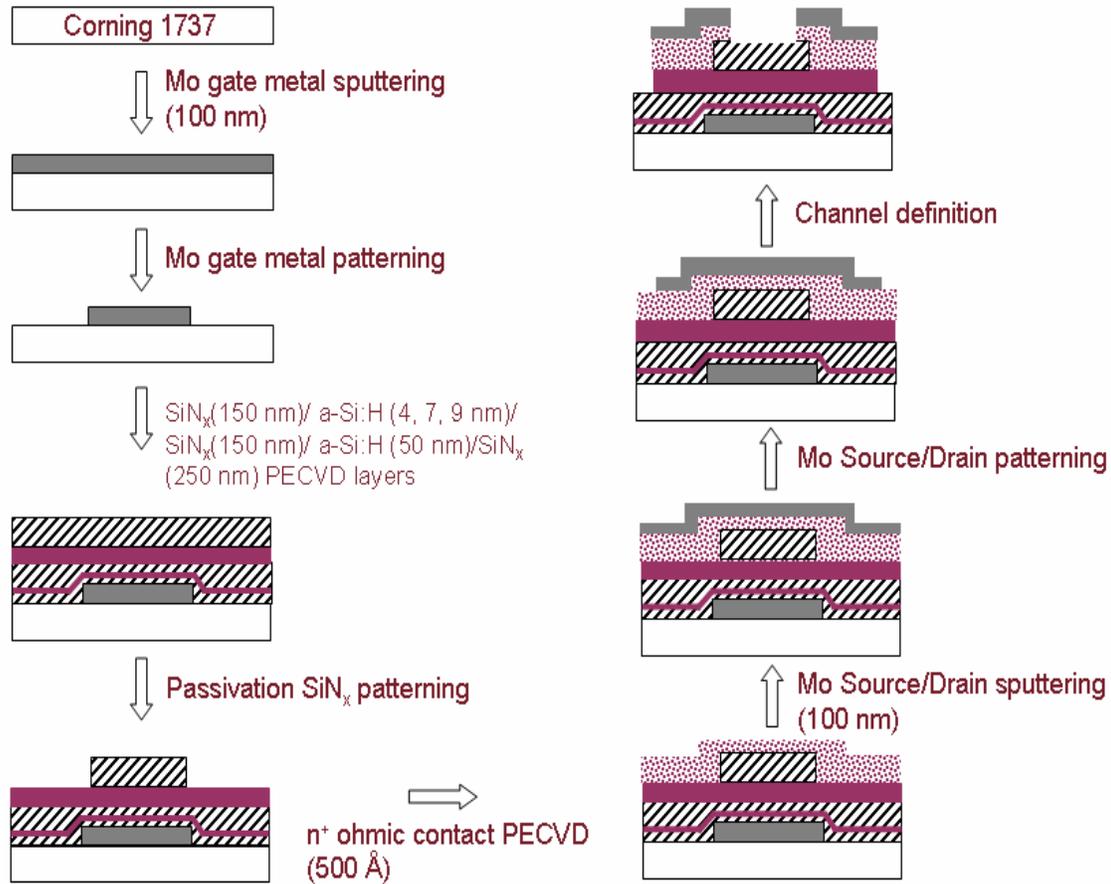


Figure 31. Fabrication flow for floating gate a-Si:H TFT.

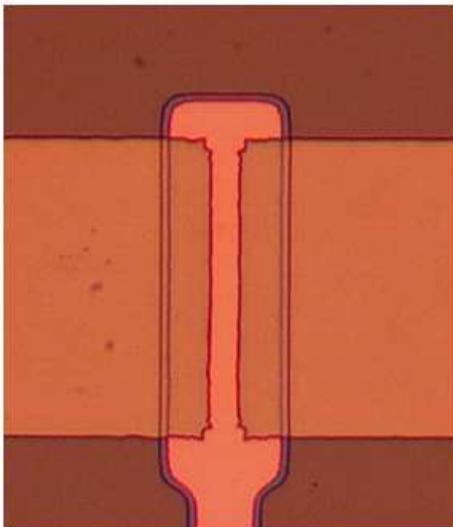
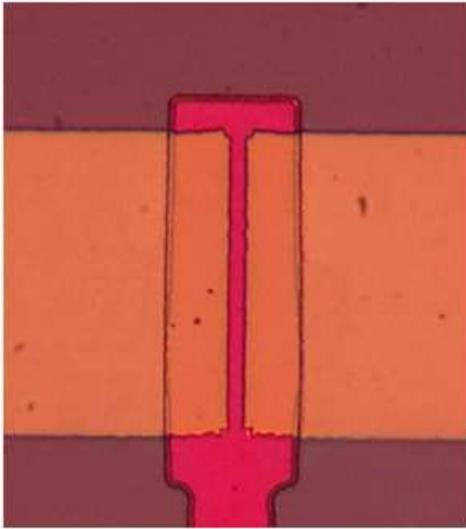


Figure 32. (a) Functional TFT with 9 nm embedded a-Si:H layer, and (b) conventional TFT.

5.3 Output and Transfer Characteristics and Thickness Effect

Initial measurements of both groups, i.e., control TFTs and TFTs with an embedded a-Si:H layer, show typical output and transfer characteristics of an enhancement mode field effect transistor. For example, high I_{on} 's and large I_{on} / I_{off} ratio ($\geq 10^6$) were observed. The difference is that the V_t increases with the increase of the embedded a-Si:H layer thickness. For instance, Figure 33 shows that at the same W/L ratio of 3.2, corresponding V_t 's of 2.8, 3.0, 3.7, and 4.9 V were observed for 0, 4, 7, and 9 nm embedded films, respectively. The S also follows the same trend with embedded film thickness, e.g., 0.1, 0.14, 0.21, and 0.47 V/decade for 0, 4, 7, and 9 nm embedded films, respectively. The a-Si:H/SiN_x interface is usually highly defective. The insertion of the a-Si:H layer to the gate SiN_x created two additional highly defective interfaces, which contributed to the increase of V_t and S .^{111, 112} The thickness effect is probably due to the increase of the interface layer thickness, otherwise the inserted a-Si:H layer can be taken as defective because the inserted layer was very thin.

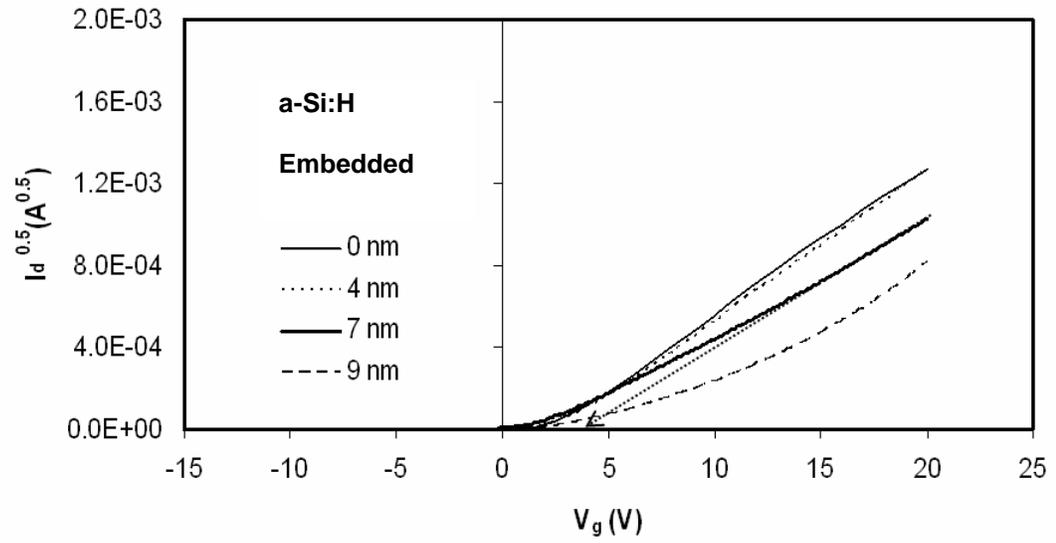


Figure 33. V_t shifts of TFTs with different a-Si:H insertion layer thickness, $V_d = 10$ V, $W/L = 3.2$. (Arrowed dashed line points to the V_t of each line)

5.4 Memory Capacity

Figure 34 shows the hysteresis of transfer characteristics of the control TFT and the TFT with a 7 nm a-Si:H layer embedded in the gate SiN_x layer. The transfer characteristic curves were obtained from the sweeping the V_g from a negative value toward a positive value and then immediately back to the starting negative value. The sweeps were performed in 0.1 V step and the V_d was fixed at 10 V. Fig. 34 (a) shows that the hysteresis of the control TFT is negligible over a large sweep voltage range. This is consistent with its desirable device quality, i.e., $V_t = 3.7$ V, $S = 0.1$ V/decade, and $\mu_{eff} = 0.38$ cm²/V-s. Fig. 34 (b) and (c) also show that the I_{off} of the reversely swept curve is higher than that of the forward swept curve. This indicates that the forward bias trapped electrons are not totally released unless a very large $-V_g$ bias voltage is applied. When the V_g is a large negative value, an inversion layer is formed at the channel a-Si:H layer adjacent to the gate SiN_x interface. For the normal TFT operation, i.e., forward gate sweep, the I_d value increases with the increase of the $-V_g$ because of hole injection. However, in the backward sweep condition, since some electrons are still trapped at the embedded a-Si:H site, they are released to the channel/gate SiN_x interface region. Therefore, the inversion layer formation is delayed. This is why at a very large $-V_g$, the leakage current of the forward sweep curve is higher than that of the backward sweep curve, as shown in Figs. 34 (b)– 34 (d).

Figure 35 shows the memory characteristic of the TFTs with different embedded a-Si:H layer thickness.¹¹³ The curves were obtained by a forward sweeping of the V_g

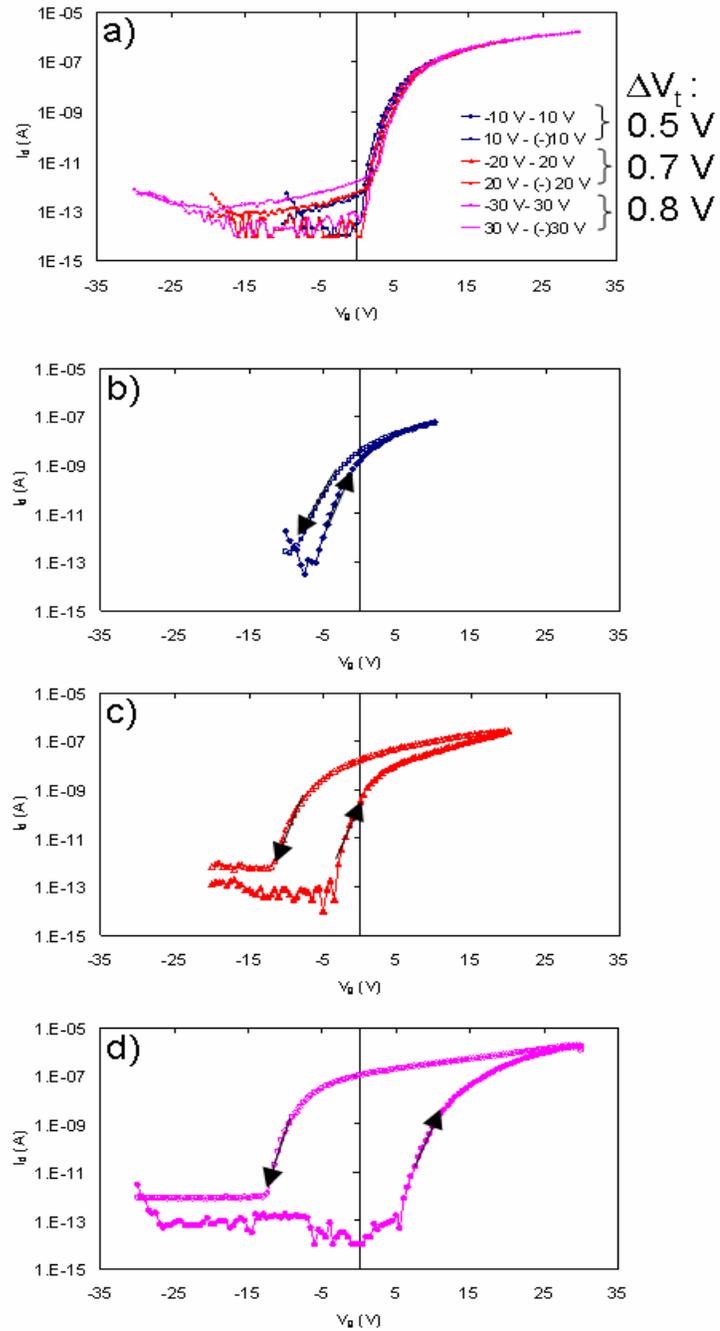


Figure 34. Hysteresis of (a) control TFT (no embedded layer), TFT with 7 nm a-Si:H embedded in the gate SiN_x layer swept at (b) -10 to +10 V, (c) -20 to +20 V, and (d) -30 to +30 V. $V_d=10$ V and $W/L=85 \mu\text{m}/35 \mu\text{m}$.

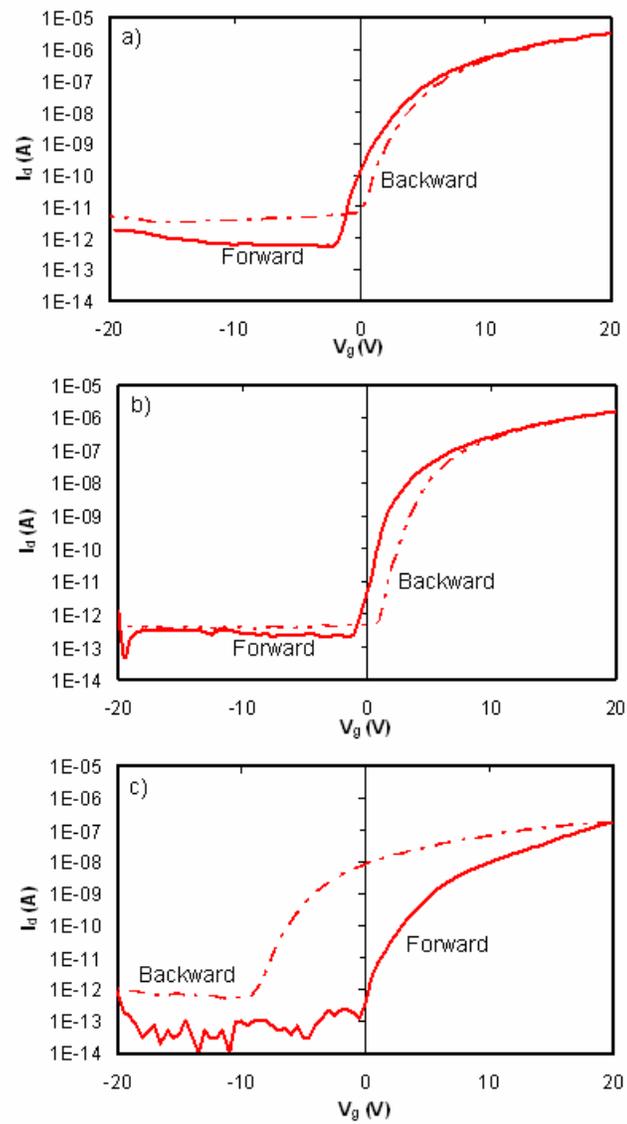


Figure 35. Hysteresis of TFT with a) no embedded layer, b) 3 nm and c) 7 nm embedded a-Si:H, $W/L = 2.4$, $V_d = 10$ V.

from -20 V to $+20$ V, which was immediately followed by a backward sweeping to -20 V. Both sweepings were performed at a 0.1 V interval with $V_d = 10$ V.

The control TFT, i.e., TFT with 0 nm embedded a-Si:H, shows a clockwise hysteresis between the forward and the backward curves with a V_t difference of 0.8 V between the two curves. The TFTs with the embedded dielectric layers show consistent increase of hysteresis gap with the increase of embedded layer thickness. The V_t difference also follows a similar trend, e.g., 1 V and 6.8 V for TFT embedded with 3 and 7 nm a-Si:H layers, respectively.

The behavior of charge accumulated at the interface is directly affected by the polarity of the starting V_g sweep. For instance, for a backward sweeping of an n-channel TFT, the highly positive V_g translates to the filling of the donor-like electron traps since the Fermi level is positioned closer to the conduction band.¹¹⁴ The increase of donor-like traps resulted in a decrease of positive charges, which translates to the shift of the transfer characteristics to a more positive side, hence the clockwise direction of the hysteresis.

The hysteresis changed direction at the 7 nm a-Si:H embedded TFT. For instance, at the positive V_g region, the backward sweep resulted in a larger I_d than that of the forward sweep. This could be related to the delay in the inversion layer formation. The release of trapped electrons at the embedded a-Si:H site to the channel/gate SiN_x interface might correspond to delay of inversion layer formation. The inversion layer was fully formed during large negative V_g value, i.e., toward the end of the backward sweep and resulted in the larger I_d .

The maximum amount of trapped charges is limited by the Coulomb blockade phenomena. Other than the barrier layer thickness, Coulomb blockade is also related to the conducting layer thickness since it directly affects the film's conductance.¹¹⁵ The conductance of the floating gate, in turn, is related to the energy level of the floating gate, which determines the possibility for electrons tunneling.

5.5 Programmability

Programmability of the nonvolatile memory can be estimated from the change of transfer characteristics after a certain amount of charges are stored; for example, the ΔV_t of a transistor before and after a period of gate bias has been used to quantify the “memory” property.¹ Figure 36 shows the channel conductance (g_d) as a function of V_g of an a-Si:H TFT with a 9 nm thick a-Si:H layer embedded in the gate SiN_x of two states. The “0” state was from the TFT before being charged and the “1” state was from the same TFT after being biased at $V_g = 20$ V for 1 s with source and drain electrodes grounded. The g_d was measured at $V_d = 10$ V. Fig. 36 shows that a $\Delta V_t = 1$ V was obtained from the two curves at the same g_d value. On the other hand, when measured at the same V_g , the channel conductance at the 1 state was lower than that at the 0 state. This is because electrons trapped in the gate SiN_x layer at 1 state hindered the accumulation layer formation at $V_g > V_t$.

According to Gauss' law, for a floating gate transistor, ΔV_t is a function of the gate dielectric layer, such as the amount of charges trapped as well as its thickness and the permittivity.¹¹⁶ The amount of charges trapped is dependent on the type of dielectric

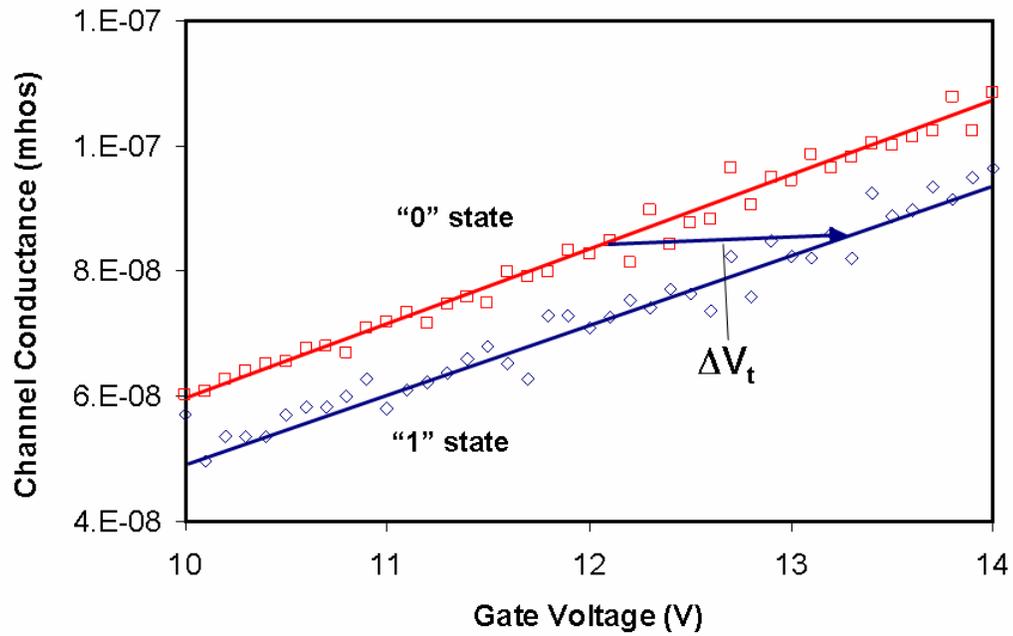


Figure 36. Channel conductance as function of gate voltage for TFT with a 9 nm embedded a-Si:H layer. $W/L = 2.7$.

material and the structure. In order to maximize the memory effect, the two gate dielectric layers sandwiching the floating gate should be of different thicknesses, i.e., the one adjacent to the channel layer needs to be thin to lower the required operation power and the one adjacent to the gate electrode needs to be thick to reduce the leakage current from the gate side.¹¹⁶ In this work, both dielectric layers are of the same thickness, which leaves room for improvement.

5.6 Charge Retention

The charge retention time is an important factor for the memory device. Figure 37 shows the V_t as a function of retention time curves of the same TFT as that of Fig. 36 at “write” and “erase” states. For the write state, the TFT was stressed at $V_g = 10$ V and $V_d = V_s = 0$ V for 1 s. The V_t was extracted every 120 s up to of 3600 s after which the erase state data were collected. For the erase state, the TFT was stressed at $V_g = -10$ V and $V_d = V_s = 0$ V for 1 s. The V_t was again extracted every 120 s up to of 3600 s. The threshold voltage difference of 0.7 V between the write and erase states was obtained originally. It decreased to 0.5 V in a short period of 240 s and remained the same until 3600 s. Switching time is related to the accumulated charge and the driving current.⁷¹ For the transistor in Fig. 34(d) ($W/L = 2.4$, $V_g = 5$ V, and $R_{max} = 1.8$ M Ω) a switching time of less than 700 μ s was estimated. Improvement of the switching time is possible through optimizing the device structure, such as the bottom SiN_x layer thickness and the embedded a-Si:H layer properties.

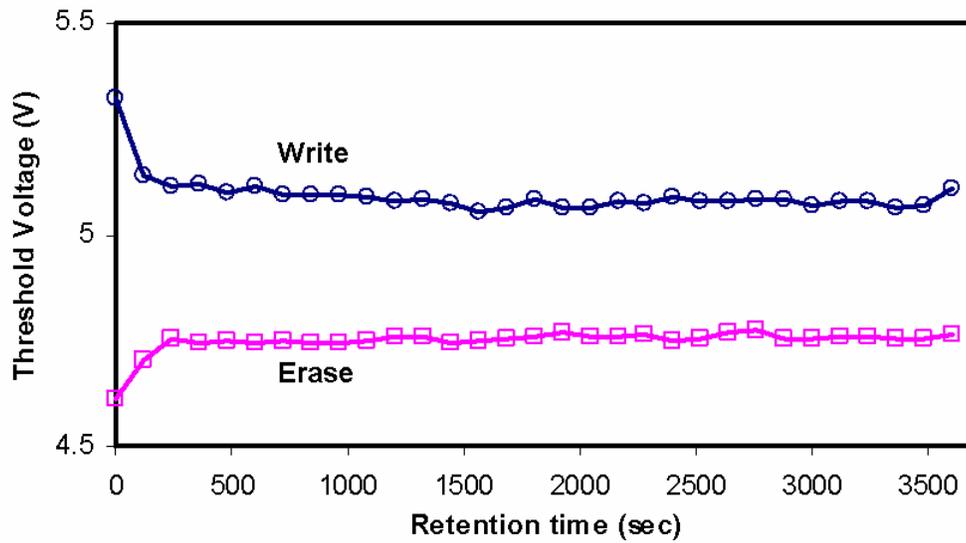


Figure 37. Change retention characteristics of Fig. 36 TFT.

This long retention time was achieved due to the low leakage current of the gate SiN_x layer. Based on the retention characteristic change, the a-Si:H TFT with the SiN_x /a-Si:H/ SiN_x gate dielectric holds charges more effectively than the TFTs with a ferroelectric or SiO_x as gate dielectric, of which the V_t decreases with time continuously for a longer period of time.^{69, 72} The steady charge holding of the a-Si:H embedded TFT may be explained with the high quality of the gate SiN_x layer, which is stable and has a low leakage current. For retention analysis at much longer time scales, there is bound to be eventual charge leaking that involves electron tunneling, hole injections, charge redistribution, etc., similar to those observed in polysilicon oxide nitride oxide silicon (SONOS) structure.¹¹⁷ The thickness of the embedded a-Si:H layer and the sandwiching SiN_x layers play significant roles in charge retention.

5.7 Summary

In summary, the a-Si:H TFT based on embedding a thin a-Si:H layer in the gate

SiN_x has been demonstrated to be an effective memory device. This kind of device is easily fabricated using two photomasks. The dielectric/channel/ top dielectric stack was deposited in one pump down and the maximum process temperature was 300 °C. The TFT's memory characteristics were proven from the hysteresis of its transfer characteristics, which increased with the increase of the sweep V_g range. The programmability and retention characteristics have also been studied. The memory window based on the channel conductance measurement is 1 V threshold voltage shift. A charge retention time greater than 3600 s was achieved. The TFT's various memory characteristics may be further improved by optimizing material properties and thickness of each composing film of the gate dielectric structure. This device is expected to be applicable to many low-temperature, large-area, flexible substrate applications.

CHAPTER VI
CHARGE AND DISCHARGE OF FLOATING GATE A-SI:H TFT
NONVOLATILE MEMORIES*

6.1 Introduction

This chapter will elaborate on the charge and discharge phenomena of the floating-gate a-Si:H TFT presented in Chapter V. The injection and retention of charges to the a-Si:H embedded gate dielectric had been investigated with respect to the gate bias condition under the grounded source and drain electrode condition. The discharge process can be taken as a combination of electron repelling and neutralization mechanisms. Three different discharging methods, namely: 1) thermal annealing, 2) negative V_g bias, and 3) light exposure, had been carried out. The discharge efficiency with respect to key parameters in each method will be discussed. The charge storage capability, the discharge efficiency, and the mechanisms under a biased drain electrode condition will be investigated. Finally, temperature effect on charging and discharging will be discussed.

6.2 Experimental Method

For the charge storage experiment on a static operation, the TFT's forward transfer characteristic from $V_g = -5$ V to a positive V_g was measured. It was then stressed

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at this V_g for a period of time with $V_d = 0$. The TFT was subsequently swept in the backward direction, i.e., from the specific V_g to -5 V. During the backward sweep, the transfer characteristics shifted to the negative direction due to the delay of the inversion layer formation associated with the negative charges being released.¹⁰⁷ The amount of charge stored at the TFT, Q , was estimated from the ΔV_t , between the forward and the backward transfer characteristics using the following equation⁶⁷

$$Q = \Delta V_t \epsilon / d \quad (25)$$

where ϵ and d are the dielectric constant and the thickness of the tunnel SiN_x , respectively.

For all discharge experiments at the static operation, the TFT's transfer characteristic in the forward direction was first measured. Then, it was stressed at a specific V_g for a period of time with the source and drain electrodes grounded. For the thermal annealing discharge, the TFT was annealed at 210°C for a period of time. For the negative V_g bias discharge, the TFT was biased at $V_g = -35$ V or -40 V for a period of time. For the light exposure discharge, the TFT was exposed to a halogen lamp (GE Quartzline EKE 35200) for a period of time. For the discharge estimation, after the TFT was discharged, its transfer characteristic was measured by sweeping V_g from -5 V to the above specified V_g . The charge remained in the TFT was estimated using Equation 25 where ΔV_t was the difference of the V_t before charge and that after discharge.

The measurement steps performed for the charge storage experiment for dynamic operation were (1) measurement of transfer characteristic from $V_g = -5$ V to 35 V at $V_d = 10$ V, (2) stress bias at $V_g = 35$ V, for 10 s at $V_d = 0, 0.1, 1, \text{ or } 10$ V with the source

electrode grounded, (3) measurement of transfer characteristic from $V_g = 35$ V to -5 V at $V_d = 10$ V. The amount of charge stored at the TFT, Q , was also estimated from the ΔV_t between the forward (in step 1) and the backward (in step 3) transfer characteristic using Eq. 25.

For discharging experiments at the dynamic operation, the TFT was first charged and then discharged. The charge step was the same as that described above: (1) measurement of the transfer characteristic from $V_g = -5$ V to 35 V at $V_d = 10$ V and (2) stress bias at $V_g = 35$ V for 10 s at $V_d = 0, 0.1, 1, \text{ or } 10$ V, separately with the source electrode grounded. For discharge with the negative gate bias method, the charged TFT was biased at $V_g = -35$ V for 10 s with V_d at $0, 0.1, 1, \text{ or } 10$ V independently. For discharge with the light exposure method, the charged TFT was exposed to the same halogen lamp (GE Quartzline EKE 35200) as the static operation at $585 \mu\text{m}/\text{cm}^2$ for 5 s with V_d at $0, 0.1, 1, \text{ or } 10$ V and $V_g = 0$ V. For discharge with the thermal annealing method, the charged TFT was annealed at 210°C for 10 min. During the annealing, $V_g = 0$ V and pulsed V_d at $0, 1, \text{ or } 10$ V was applied repeatedly for 10 1-minute cycles with each cycle including 10 s on and 50 s off. After discharge, the TFT's transfer characteristic was measured from $V_g = -5$ V to 35 V at $V_d = 10$ V. The charge remained in the TFT was also estimated using Eq. 25 where ΔV_t is defined as the difference of the V_t before charge and that after the above discharge step. The percent discharge was calculated as follows

$$\text{Percent discharge} = \left(\frac{\text{Amount of charge stored}}{\text{Amount of charge remained}} \right)_{V_d} \times 100\% \quad (26)$$

For the temperature effect on the charge capacity of the TFT, the transistor was heated to a temperature of 298, 308, 323, or 373 K. At this temperature, first, the TFT's transfer characteristic was measured. Then, the TFT was charged at $V_g = 35$ V and $V_d = 0$ V for 10 s, which was followed by transfer characteristic measurement. The TFT's charge storage capacity at each temperature was calculated.

For the annealing discharging, the TFT was first charged at room temperature and the transfer characteristic was measured. Then, it was annealed at 423, 443, 463, or 483 K with $V_g = V_d = 0$ V for 10 min. The TFT was subsequently cooled down to room temperature. The transfer characteristic was measured again. The amount of charges remained in the TFT was subsequently calculated.

All electrical measurements were performed in a black-box using an Agilent 4155C Semiconductor Parameter Analyzer. There are other methods for measuring the charge storage capacity of a dielectric film. For example, a conductive atomic force microscopy has been used to measure the electrical characteristic of a non-conductive film.¹¹⁸ The floating-gate MOS capacitor has been fabricated to characterize the charge storage capacity from the capacitance-voltage hysteresis curves.^{119, 120} The method described in this chapter is meant for the direct measurement of the TFT's memory functions.

6.3 Static Operation

6.3.1. General Charging and Discharging

Figure 38 shows charges in the floating-gate TFTs before and after discharging under various conditions for different channel dimension. The charge stored is comparable to nc-Si embedded memory capacitor ($\sim 1.5 \times 10^{12}$ charge/cm²)¹²¹ and poly-Si TFT memory ($\sim 7 \times 10^{12}$ charge/cm²).¹²²

Thermal annealing corresponds to the movement of free electrons or holes to neutralize trapped charges. The average remaining charge after annealing at 210°C for 75 minutes of TFTs with different channel sizes was 88 %. Negative V_g stress resulted in injection of holes or detrapping charges from the gate dielectric layer. The average remaining charge after a -40 V stress for 5 seconds was 89 %. Light exposure created electron-hole pairs in the a-Si:H layers and leaking them to the channel layer or gate electrode. The average remaining charge after a 5 second exposure to light at 484 $\mu\text{m}/\text{cm}^2$ was 87 %. The non-complete removal of charge is related to the deep trapping centers in embedded a-Si:H, SiN_x, and their interfaces.^{123, 124}

6.3.2. Charging Characteristic

Figure 39 shows that the amount of charge stored in the TFT increases with the increase of the bias V_g . Generally, the increase in positive V_g bias resulted in the increase of the amount of negative charge injected from the a-Si:H channel through the tunneling SiN_x into the floating gate. Fig. 39 shows a two-step charging behavior, i.e., the small amount of charge trapped under the low V_g stress condition and a large amount of charge trapped under the high V_g stress condition. The low stress V_g , e.g., 15 or 25 V, simply corresponds to smaller number electrons injected to break and occupy the weakly bonded Si-Si (bond energy of 222 kJ/mol; compared to 318 kJ/mol for H-Si and 432 kJ/mol for H-H). Saturation of charge stored and/or Coulomb blockade was not observed in the floating-gate capacitor stressed at the same high V_g of 35 V. Coulomb blockade is a phenomena resulted from insufficient voltage drop between the floating gate and the channel, i.e., across the tunneling SiN_x , to allow for more injection of charges into the floating gate.

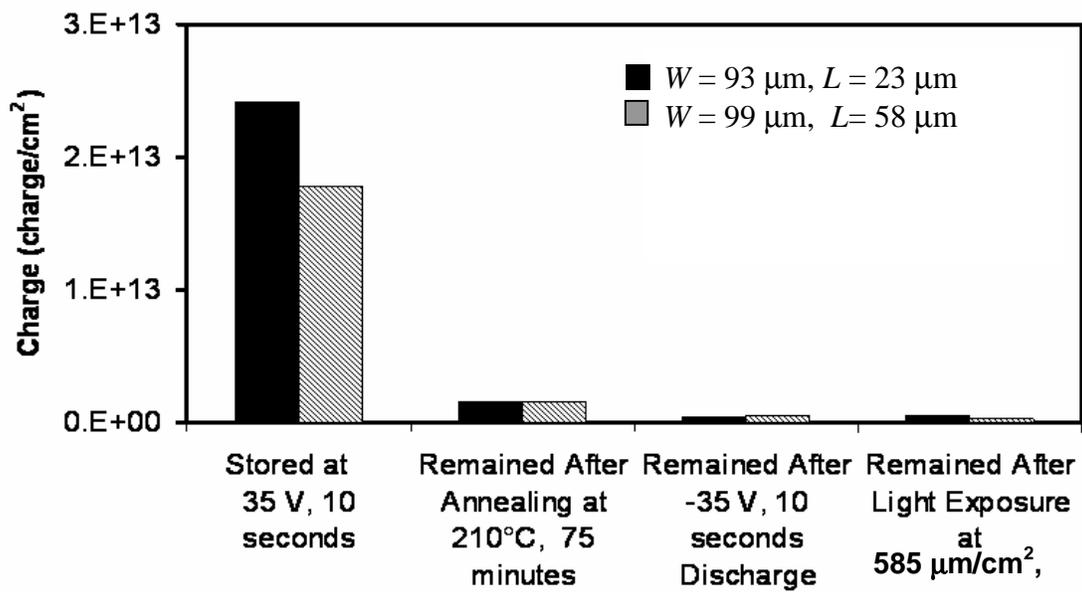


Figure 38. Comparison of various discharging methods for floating-gate a-Si:H TFTs.

Figure 40 shows the power-law time dependence charges storage relationship of $Q = Q_o t^\gamma$, where Q_o is the initial charge without V_g stress, t is the stress time, and γ is the fitted coefficient. The positive γ value means that the amount of charge storage increases with the stress time. TFTs with the shorter L , i.e., $L = 17$ and $23 \mu\text{m}$, show larger charge storage densities than that that with a longer channel length, i.e., $L = 58 \mu\text{m}$. Currently, the exact cause is not clear. It is possible due to that the short channel TFT has a smaller channel resistance than the long channel TFT, which makes it easier to attract charges to the embedded SiN_x layer.

Dangling bond formation that causes the metastability of a-Si:H layer has been observed to follow a power-law time dependence.¹²⁵ The dangling formation is attributed to the density and occupancy of band tail states and H dispersion.¹²⁵ The embedded a-Si:H layer then contributes to a magnified dangling bond effects on the TFT characteristic. The injection of negative charge corresponds to the formation of neutral and charged three-fold coordinated dangling bond formations similar to that of 8-N rule doping mechanism of a-Si:H,^{12, 123} i.e.,



Available tail states for a-Si:H for charge trapping were almost saturated when the charge time was long. The power-law time dependence was the result of self-dispersion of H atoms in the embedded a-Si:H layer, which stabilizes negatively charged dangling bonds.

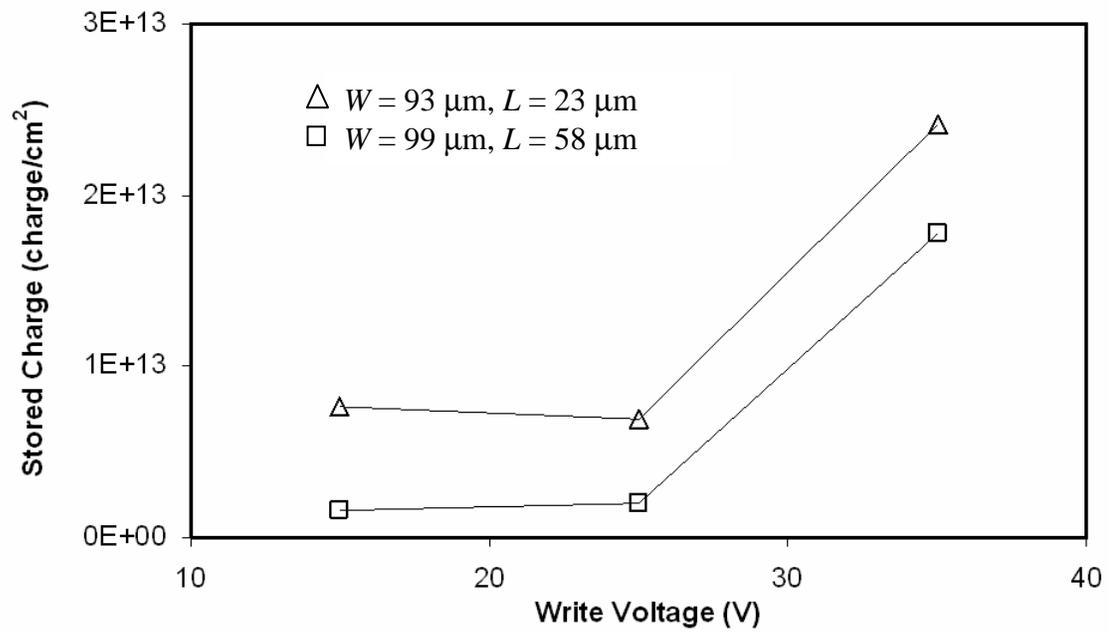


Figure 39. Charge storage density as a function of stress voltage for 10 s stress time.

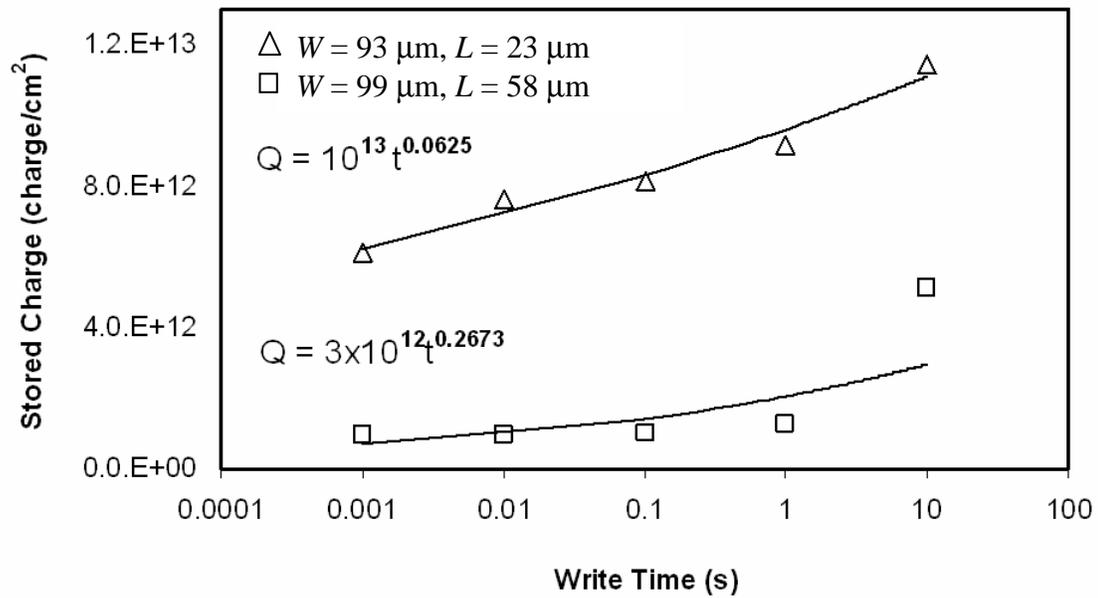


Figure 40. Charge storage density as a function of stress time at $V_g = 35$ V.

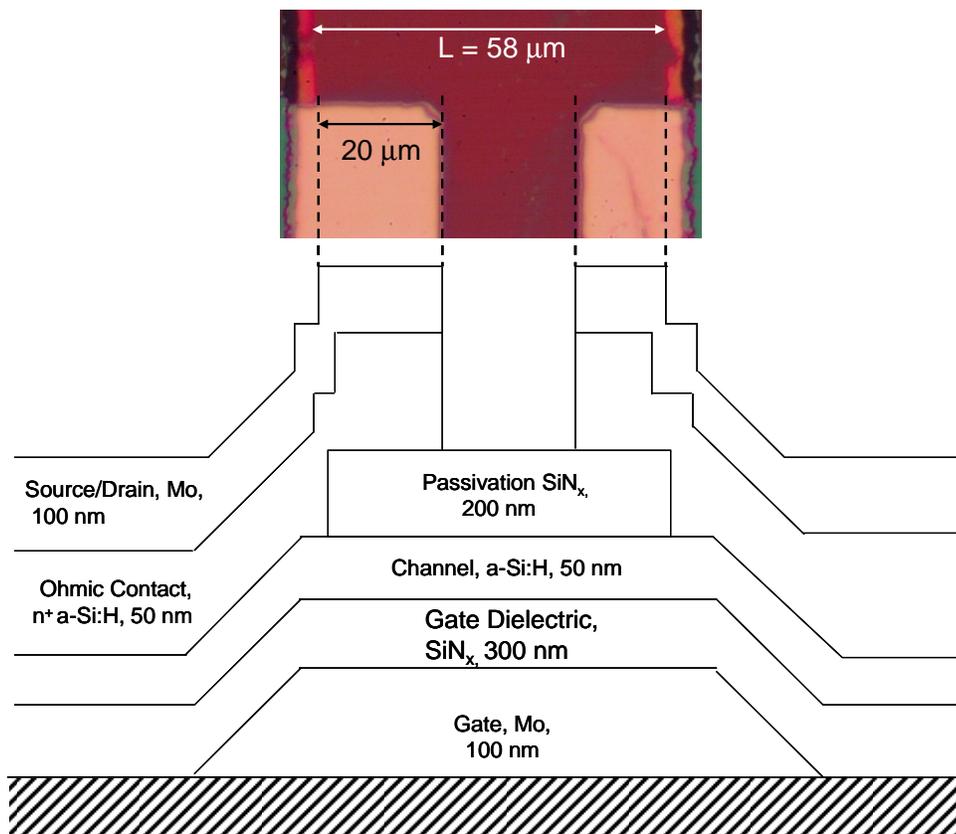


Figure 41. Source and drain overlaps with gate electrodes. $W/L = 99 \mu\text{m} / 58 \mu\text{m}$.

The overlaps of the source and drain electrodes with the gate electrode can play an important role on the charging efficiency. The charge contributed from the overlaps can be approximated by the product of the overlap region capacitance and the ΔV_t . At the overlap region, there are two metal insulator semiconductor (MIS) capacitors in series: source or drain metal/passivation SiN_x (250 nm)/a-Si:H channel capacitor and gate metal/ SiN_x /a-Si:H/ SiN_x gate dielectric (309 nm)/a-Si:H channel capacitor. The capacitance is calculated with a k -value of 6.9 for the SiN_x and with an overlap area

based on the width of the channel and the length of the respective overlap region. As an example, the TFT with a source and gate overlap of 20 μm and drain and gate overlap of 19 μm and channel width of 99 μm (Figure 41) exhibits source-gate overlap capacitance and charge of 1.9×10^{-13} F and 8.3×10^6 charge, respectively, and drain-gate overlap capacitance and charge of 1.8×10^{-13} F and 7.9×10^6 charge, respectively. The total capacitance was 5.5×10^7 charge. Therefore, about 29 % of the charge stored was from the overlap capacitance. If the overlap is small, e.g., 2 μm , the calculated contribution from the overlap is 4 %. Furthermore, the charge stored per unit area at the floating gate a-Si:H TFT after excluding the source-gate and drain-gate overlap contribution is comparable to the charge measured from a floating gate MIS capacitor with 9-nm embedded a-Si:H layer at the gate dielectric described in Chapter VII, e.g., 7.6×10^{11} charge/ cm^2 for the TFT and 2.4×10^{11} charge/ cm^2 for the MIS capacitor. Since these charges are comparable, the floating gate a-Si:H layer can consistently store charges without an apparent contribution from the overlapping regions. However, for industrial application, the overlap region between source and drain with gate electrode should be minimized.

6.3.3. Discharging by Thermal Annealing

Annealing at elevated temperature is a non-electrical method performed to neutralize injected charges. The equilibration happened throughout all hydrogenated

films, i.e., the a-Si:H and the SiN_x. High temperature a-Si:H film annealing, e.g., 350-500°C, resulted in equilibration of charged dangling bonds by mobile H atoms.¹²⁶ High temperature annealing, e.g., 900-1100°C, of SiN_x deposited at 800°C in LPCVD with SiH₂Cl₂ and NH₃ resulted in H passivation of the dangling bonds.⁴⁹ The charge equilibration by H is dependent on many factors, such as the H density in the film, the diffusivity of H, the amount dangling bonds that trap the charges, and the amount of injected charges.⁴⁹ For the floating gate memory charged at $V_g = 35$ V for 10 s, an average of 84% charge removal was obtained after annealing at 210°C for 10 minutes in air. Figure 42 shows the transfer characteristics of a 9-nm embedded TFT (W/L=99 μm/58 μm) before charging, after being biased at $V_g = 35$ V for 10 s, and after subsequent annealing in air at 210°C for 15 minutes. It is obvious that the annealed TFT shows characteristics close to that of the original TFT.

The lower temperature annealing at 210°C compared to the 350°C used in ref.¹²⁶

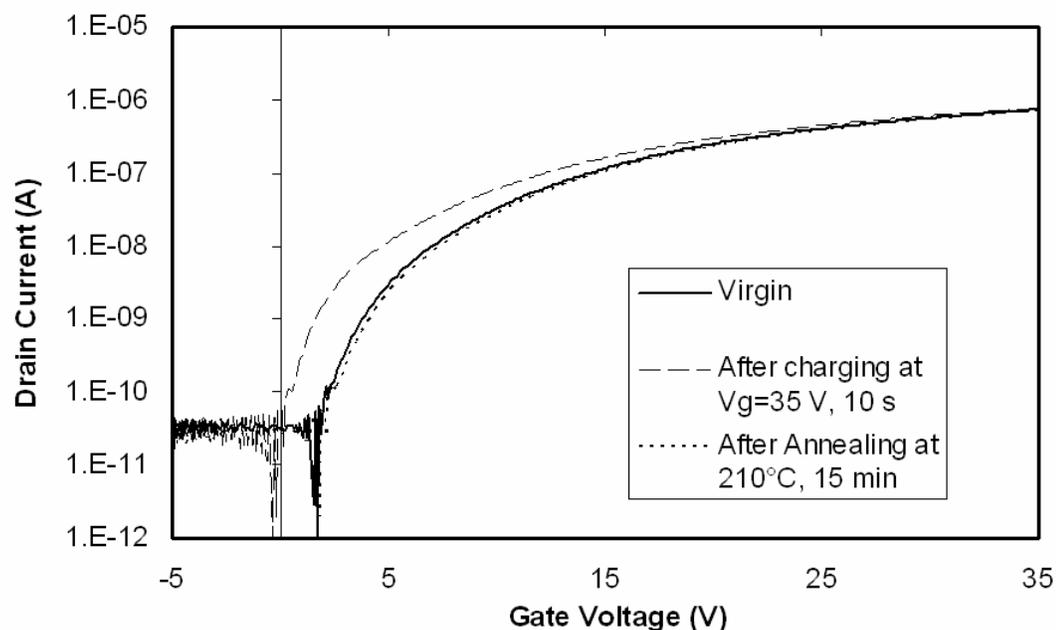


Figure 42. Transfer characteristics of virgin TFT, after charging at $V_g = 35$ V, 10 s, and after annealing at 210°C, 15 min. $W/L = 99 \mu\text{m}/58 \mu\text{m}$.

possibly produced similar equilibration mechanism of passivation of charged dangling bonds with H atoms. Since the atomic H density is fixed at the film's deposition temperature, most H atoms should not diffuse out of the films at an annealing temperature below the film's deposition temperature unless the annealing time is long. For example, annealing at the same temperature of 210°C for 75 minutes resulted in a slightly lower average charge removal, i.e., 88%. The non-complete removal of charge at a longer annealing time might be related to the removal of H atoms from the structure that induced extra dangling bonds to strongly hold trapped charges. In addition, the

existence of deep trap centers can be observed from the amount of remaining charges on TFTs that were stressed at different V_g 's although they were annealed at the same condition. For instance, an average of 80% charge removal was obtained on a TFT charged at $V_g = 15$ V for 10 s and an average of 88% charge removal was obtained on a TFT charged at $V_g = 35$ V for 10 s even both of them were annealed under the same condition of 210°C for 10 s. The smaller amount of charge stored at $V_g = 15$ V compared to $V_g = 35$ V did not translate to a higher charge removal on the former, which suggests that deep trap charges were created at both charge storage conditions and that annealing at 210°C was not enough to neutralize these charges.

6.3.4. Discharging by Negative V_g Bias

Discharging by high-temperature annealing is not a practical method to implement on devices. Instead, charges can be relieved from the floating gate electrically by applying V_g with the opposite polarity as that of the charge storage V_g . Negative V_g bias corresponds to the injection of positive charge to equilibrate the negatively charged dangling bonds on the floating gate



On the other hand, formation of new dangling bonds can also exist under negative V_g bias followed by the stabilization of these dangling bonds by mobile H.¹⁰⁰

For a floating gate TFT charged at $V_g = 35$ V for 10 s, a 10-second negative V_g stress at -35 V corresponds to an average of 87 % charge removal. A higher negative bias of -40 V at the same stress time did not improve the discharge efficiency. The

formation of new dangling bonds is a possible reason for the same discharge efficiency. The $-V_g$ may also push electrons from the floating gate to the channel region, which is equivalent to the injection of holes to the gate dielectric structure.

Figure 43 shows the power-law time dependence of the discharge process with a discharge V_g of -35 V. The removed charge density Q_d equals $Q_{od} t^\beta$, where Q_{od} is the charge removed at time 0, t is the discharge time and β is the fitted coefficient. The TFT with $L = 58 \mu\text{m}$ had a smaller amount of charge removed compared to TFTs with shorter channel length, i.e., $L = 17$ and $23 \mu\text{m}$. This is similar to the channel length effect on the charge process in which the short channel TFT has a lower channel resistance and therefore is easier to remove charges from the gate dielectric layer. The power-law time dependence of discharging can be explained by the formations of dangling bonds in the a-Si:H layer and the dangling stabilization by H atoms.¹⁰⁰ In other words, the positive charges injected at $-V_g$ were neutralized by negatively charged dangling bond. At the same time, new dangling bonds were formed and stabilized by mobile H atoms.¹⁰⁰ Therefore, if the H diffusivity is the limited mechanism, the discharging should be dependent on the H diffusion rate.¹²⁵

6.3.5. Discharging by Light Exposure

The steps performed to observe the light exposure effect were as follow: 1) charging the TFT at $V_g = 35 \text{ V}$ for 10 s with source and drain electrodes grounded, 2) removing of V_g for 10 s, 3) exposing the TFT under halogen light for 5 s at room temperature, 4) removing the light source, and 5) measuring the transfer characteristic in

the positive direction. Figure 44 shows the charge remain density as a function of the halogen light density. The remained charge density decreases with the increase of the exposure light density. Since the TFT was exposed to the light from the top side, all SiN_x and a-Si:H layers were under the influence of the light. The energy of exposure light should be higher than the barrier energy, i.e., the optical gap, in order to be absorbed by these films. The exposure light induced electron-hole pair generation in the a-Si:H layer, which neutralizes some of the trapped charges. The charge recombination process is dependent on the distribution of the trapped charges in the film.¹²³ In addition, the electric conductivity of the SiN_x layer increases with the light intensity, which leaks the mobile charges to the channel region and reduces the amount of charges remaining in the gate dielectric layer.

The channel dimension affects percentage of charge removal at all exposure intensity. For instance, the larger channel area corresponds to smaller percentage of charge removal. It has been observed that saturation of light-induced degradation on a-Si:H film was a consequence of the equal amount of defect generation and defect

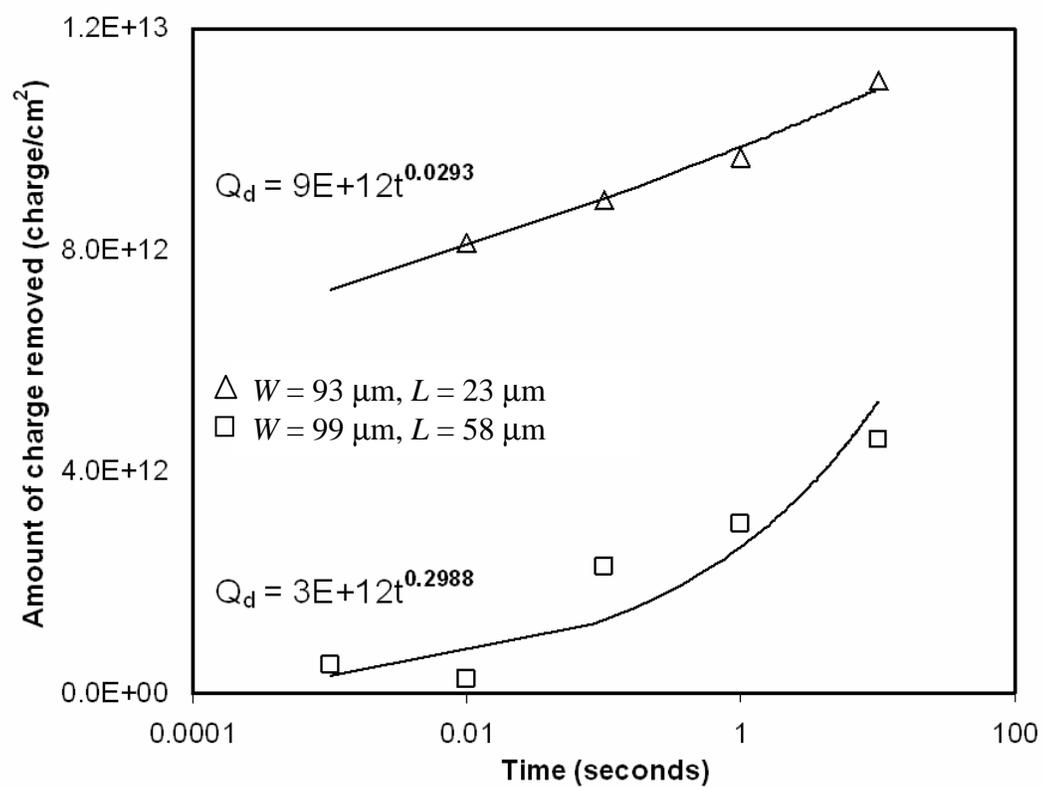


Figure 43. Removed charge density as a function of discharge time at $V_g = -35$ V.

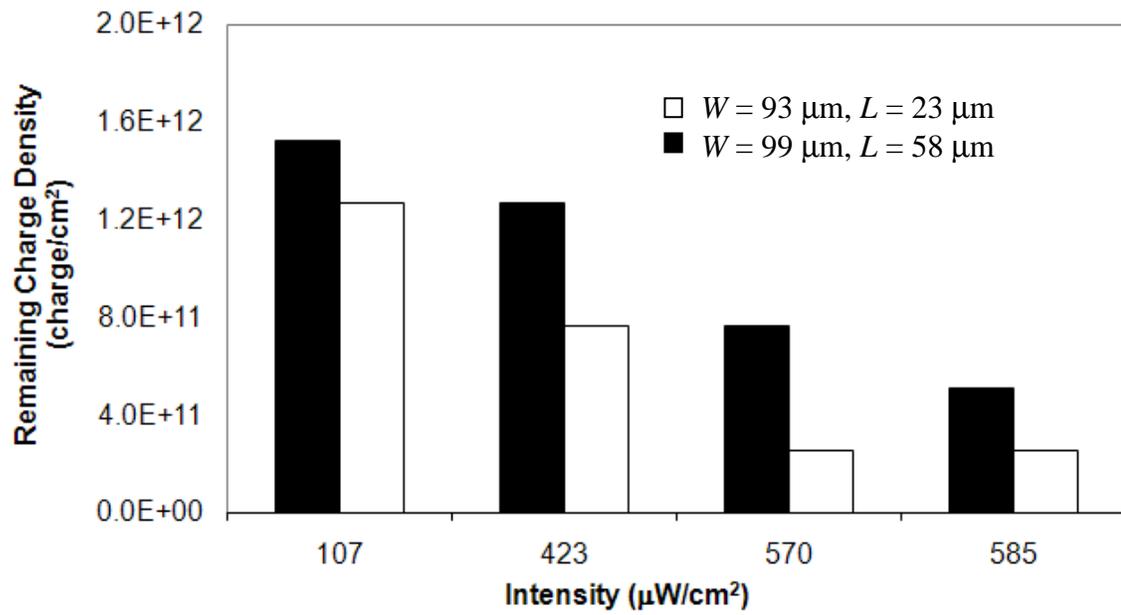


Figure 44. Remaining charge density as a function of the light exposure intensity after 5 s exposure.

annealing from light exposure.¹²⁷ Since the light intensity is constant over the whole channel region, the large amount of charge remained in the large-area TFT might be related to the number of defect creation. The channel conductivity difference between the long and short channel TFTs is another explanation for the above phenomenon.

6.4 Dynamic Operation

6.4.1. General Charging and Discharging

Figure 45 shows the transfer characteristics of a 9-nm embedded TFT with W/L of $99\ \mu\text{m} / 58\ \mu\text{m}$ at various stage of operations with $V_d = 0.1\ \text{V}$. A large hysteresis between the transfer characteristics of the TFT before and after charging was observed. After discharging by the $-V_g$ or by light exposure, the transfer characteristics shift toward the before charging transfer characteristic, which results in the smaller hysteresis between the before charging and the after discharging transfer characteristics. With the application of V_d bias during the $-V_g$ bias or light exposure discharging, the electron tunneled from the floating gate or electrons from the electron hole pairs are attracted to the drain electrode. On the forward direction sweep, the existence of such electron accumulation layer corresponds to a shift of the post discharging transfer characteristic to the right, i.e., towards the original transfer characteristic before charging. Thorough discussions on the effect of V_d on the charge and discharge process follow.

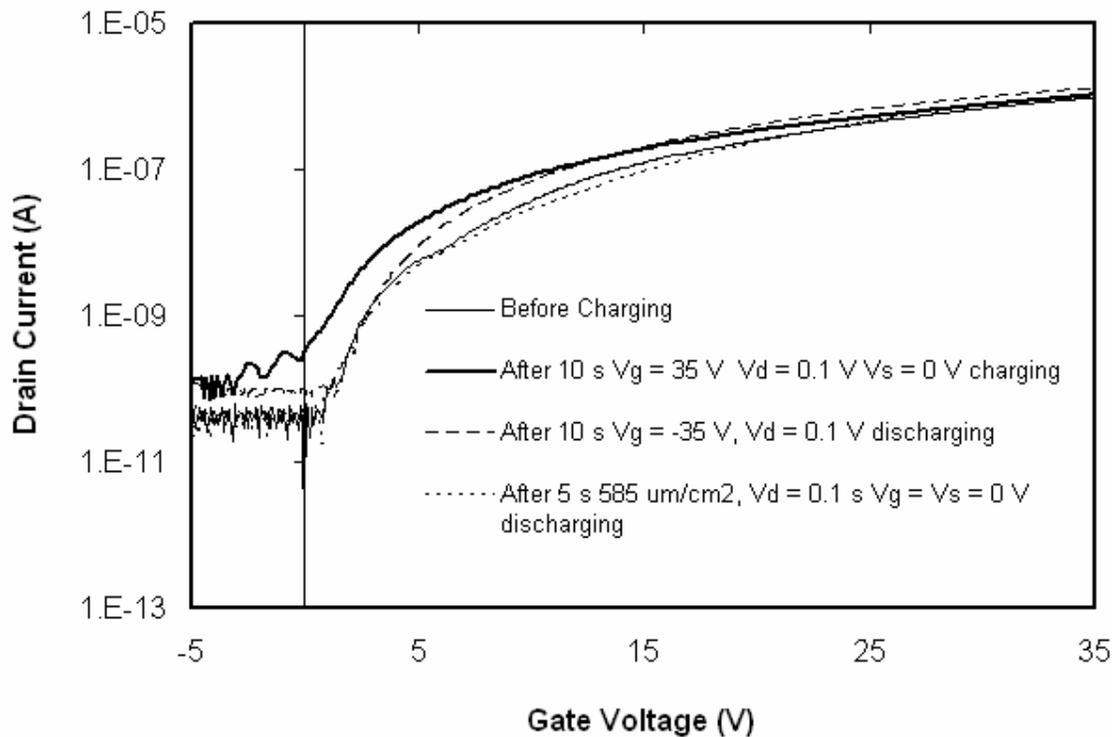


Figure 45. Transfer characteristics of a 9-nm embedded a-Si:H TFT ($W/L=99 \mu\text{m} / 58 \mu\text{m}$) before charging, after charging and after discharging with various methods.

Fig. 45 also shows that the long channel TFT has a smaller amount of stored charges than the shorter channel TFT. This may be related to the structure of the TFT. The source contact-to-gate overlap region has a MIS capacitor structure, which contributes a large portion of electrons in the accumulation layer. The long channel TFT has a higher channel resistance than the short channel TFT has. Therefore, the former has less supply of electrons for injection to the gate dielectric layer.

6.4.2. Charging Characteristic

From section 6.3.2, the charge storage capacity of the floating-gate a-Si:H was measured with the source and drain electrodes grounded. The result showed that the charge storage capacity was dependent on the stress time following the power law. It also increased with the increase of the bias V_g , which affected the electron accumulation layer formation and energy available for electrons to overcome the energy barrier between the channel a-Si:H layer and the control SiN_x layer.¹²⁸ The charge efficiency is also related to the amount of available sites for charge trapping and retention in the gate dielectric structure.¹²⁸ Figure 46 shows that amount of charges stored in the TFT decreases with the increase of the V_d value. When $V_d = 0$ V, electrons in the accumulation layer have to overcome the barrier height between the control SiN_x and channel a-Si:H layer before being injected to the gate dielectric structure. However, when a positive V_d is applied, electrons in the accumulation layer are constantly transferred to the drain electrode, which requires a lower energy than that of the energy barrier in the former case. Since in the linear region, the magnitude of I_d increases with the magnitude of V_d , the amount of electrons trapped to the gate dielectric layer decreased with the increase of V_d . The amount of charges that can be stored in the TFT may reach a saturation value if the pinch-off phenomenon occurs.¹ The pinch-off point is dependent on the magnitude of V_d .

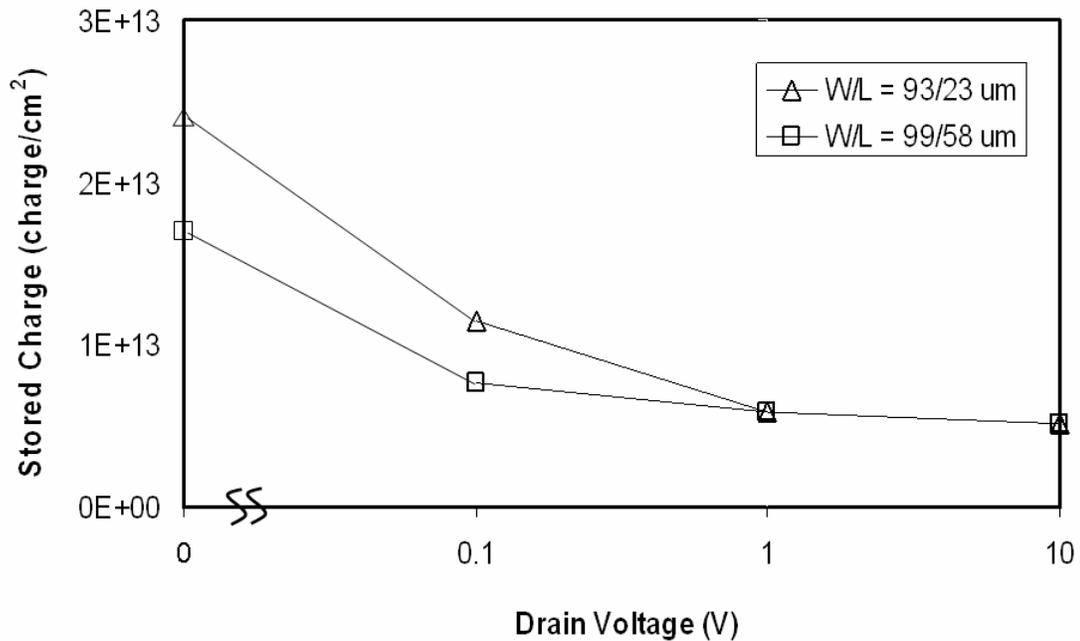


Figure 46. Stored charges of a 9-nm a-Si:H embedded TFT, biased at $V_g = 35$ V for 10s, as a function of V_d .

6.4.3. Discharging by Thermal Annealing

Figure 47 shows the amount of discharged storage as a function of V_d for 10-min thermal annealing at 210°C. Thermal annealing resulted in the energetic movement of stored charges for self-neutralization. The elevated temperature anneals the dangling bonds at the a-Si:H layers which facilitates the formation of accumulation layer. The

increase in V_d then corresponds to a delay of the inversion layer formation during post discharging transfer characteristic measurement. The hysteresis between the initial transfer characteristics and that after thermal annealing is larger. The large hysteresis corresponds to lower discharge efficiency, as observed in Fig. 47.

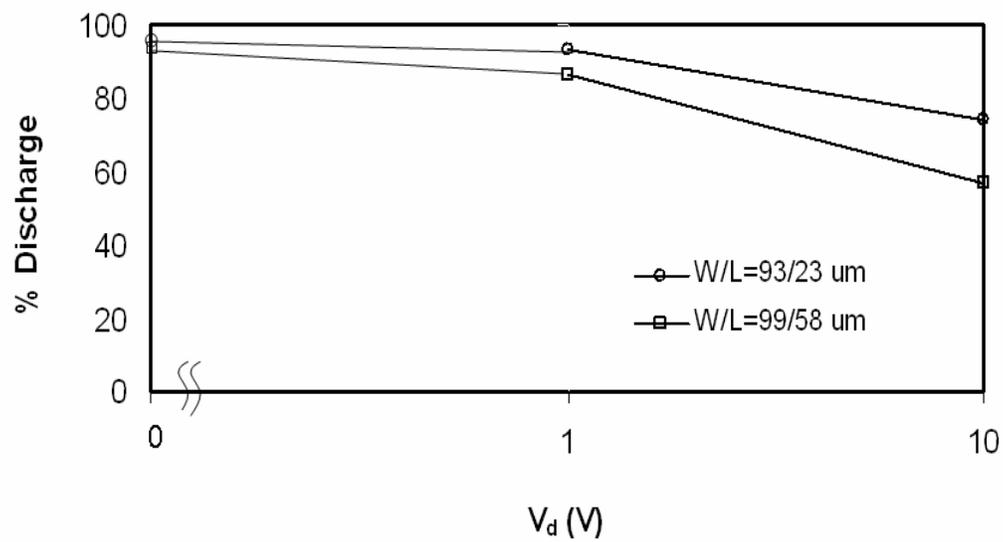


Figure 47. Percent discharge as a function of bias V_d for thermal annealing at 210°C for 10 min.

6.4.4. Discharging by Negative V_g Bias

For discharging by opposite gate polarity, the TFT was first stressed with at positive V_g for a period of time and then stressed at a $-V_g$ at various V_d 's. Figure 48 shows the percent stored discharges, i.e., charged for 10 s at $V_g = 35$ V and $V_d = 0, 0.1, 1,$ and 10 V, separately, being discharged for 10 s at $V_g = 35$ V and corresponding V_d 's. The high $-V_g$ value induced the formation of an inversion layer, which neutralized the stored electrons through injection of holes or expel of electrons from the gate dielectric layer. Fig. 48 shows that more than 80 % of the stored charges can be removed by this method. In addition, the discharge efficiency decreases with the increase of V_d . The increase of V_d corresponds to the increase of removal of holes, which is opposite of the electron flow direction, in the inversion layer to the source electrode. The smaller the V_d is, the less effective these charge carriers are removed from the inversion layer and, therefore, the higher the discharge efficiency is. The discharge efficiency may also reach a saturation value. This is also probably due to the pinch-off phenomenon that limits the transport of the charges to the drain electrode.

6.4.5. Discharging by Light Exposure

Figure 49 shows the discharge efficiency of the light exposure process, i.e., halogen at $585 \mu\text{W}/\text{cm}^2$ for 5 s. During light exposure, the applied V_d was the same as that applied during charge storage. The V_d bias effect is the same as that in Fig. 48, i.e., the discharge efficiency decrease with the increase of the V_d value. However, based on the same V_d , the light discharge is slightly more effective than that the negative gate bias

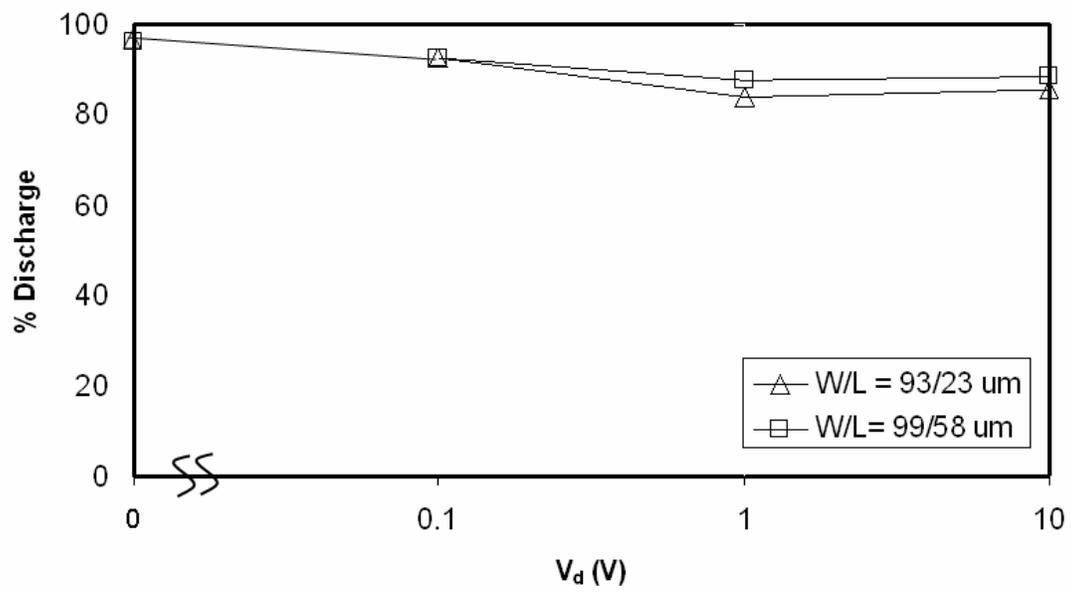


Figure 48. Discharge efficiency as a function of V_d , biased at $V_g = -35$ V for 10 s.

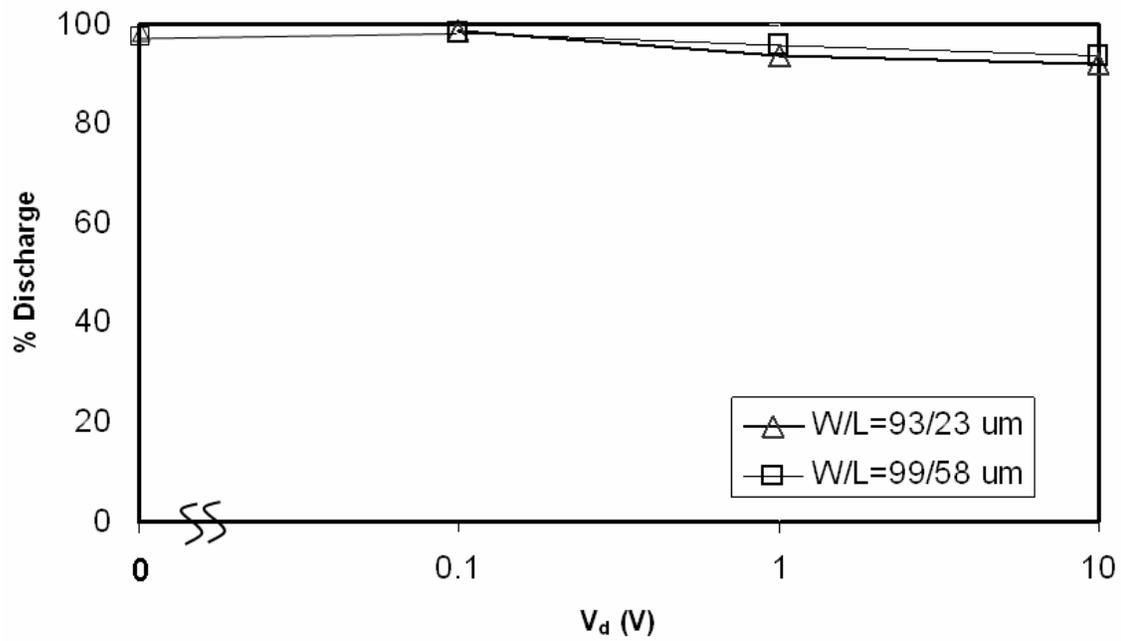


Figure 49. Percent discharge (after bias at $V_g = 35$ V for 10 s) being discharged at different V_d 's at $V_g = 0$ V under light exposure at $585 \mu\text{m}/\text{cm}^2$ for 5 s.

discharge. During light exposure, both a-Si:H and SiN_x films absorb light because the incident light has energy larger than the films' optical gaps, i.e., 1.75-1.85 eV for a-Si:H film and 1.95 eV-4.01 eV for SiN_x film.^{124, 129} Electron-hole pairs were generated in the a-Si:H film.^{130, 131} In the embedded a-Si:H film, the newly generated holes combine with the trapped electrons and leave the unbounded electrons in the film and eventually leaked through the tunnel SiN_x toward the channel a-Si:H layer.¹²⁸

6.5 Temperature Effects on Charge Capacity and Discharge Efficiency

Charge and discharge processes of the floating-gate TFT are controlled by different factors. For instance, when the TFT is charged at $V_g = 35$ V, electrons in the accumulation layer have to obtain energy higher than the barrier height between the a-Si:H channel layer and the tunnel SiN_x layer to be injected to the gate dielectric structure.¹²⁸ They are then retained by two mechanisms, i.e., the band well of the embedded a-Si:H layer or defects in the gate dielectric layers. These electrons are trapped in the deep or shallow states depending on the defect state. For example, during the injection of the high energy electrons, dangling bonds can be generated from the breakage of Si-Si or Si-H bond.¹³² Equation 29 shows an example of dangling bond formation.¹²



The dangling bond formation process is sensitive to temperature. Therefore, the charge storage capacity of the TFT is related to the temperature. Figure 50 shows the

charge storage density decreases with the increase of temperature. This is consistent with the thermal annealing discharge effect. The high temperature favors the passivation of dangling bonds, the release of trapped charges, the migration of charges, and the transportation of charges through the SiN_x dielectric layer. At the low temperature, charges have low mobilities and can be stored at the shallow state.

The discharge process is more complicated than the charge process because it is process dependent. For example, when discharge is carried out by the negative V_g bias, the process involves expelling of trapped electrons or injection of holes from the inversion layer. When discharge is done by light exposure, the process involves electron-hole pair generation and free electron transportation through the tunnel SiN_x layer. When discharge is accomplished by the thermal annealing step, the process involves hydrogen passivation and neutralization of defects and electron migration.⁴⁹

New defects or dangling bonds can be generated during discharge. For example, the Si-Si or Si-H bonds can be broken by the injected high-energy holes or the during a

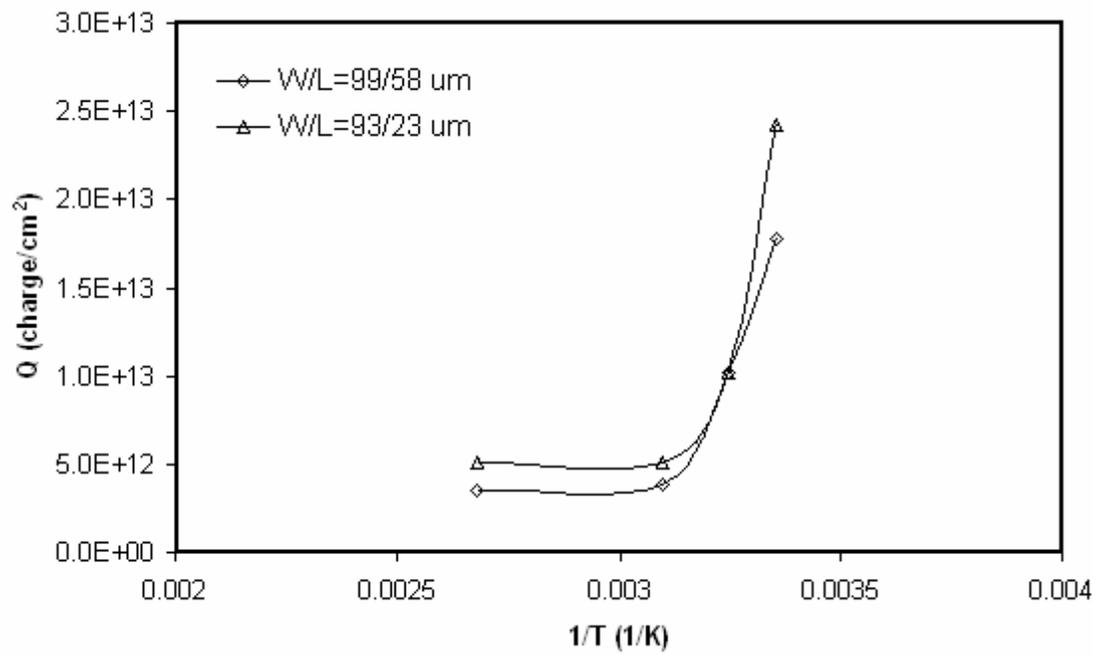


Figure 50. Temperature effect on charge storage capacity. Charged at $V_g = 35$ V, $V_d = V_s = 0$ V for 10 s.

absorption of short wavelength light. Hydrogen in the PECVD film can be released during a high annealing temperature step or a long annealing period. Therefore, it is impossible or very difficult to delineate the exact mechanism of each discharge process. However, the temperature is an important parameter for the discharge efficiency.

Figure 51 shows the discharge efficiency of thermal annealing as a function of the temperature. The TFTs were first charged at room temperature for 10 s with $V_g = 35$ V, $V_d = 0$ V before annealing at 423, 443, 463, and 483 K. The transfer characteristic after annealing then was measured at room temperature. The discharge efficiency increases with the increase of annealing temperature. This is consistent with dangling bonds passivation and charge neutralization at high temperature.

6.6 Summary

The charge and discharge phenomena of the floating-gate a-Si:H TFT have been studied under both static and dynamic operating conditions. Generally for both static and dynamic conditions, the charge storage capacity is related to the gate bias voltage and

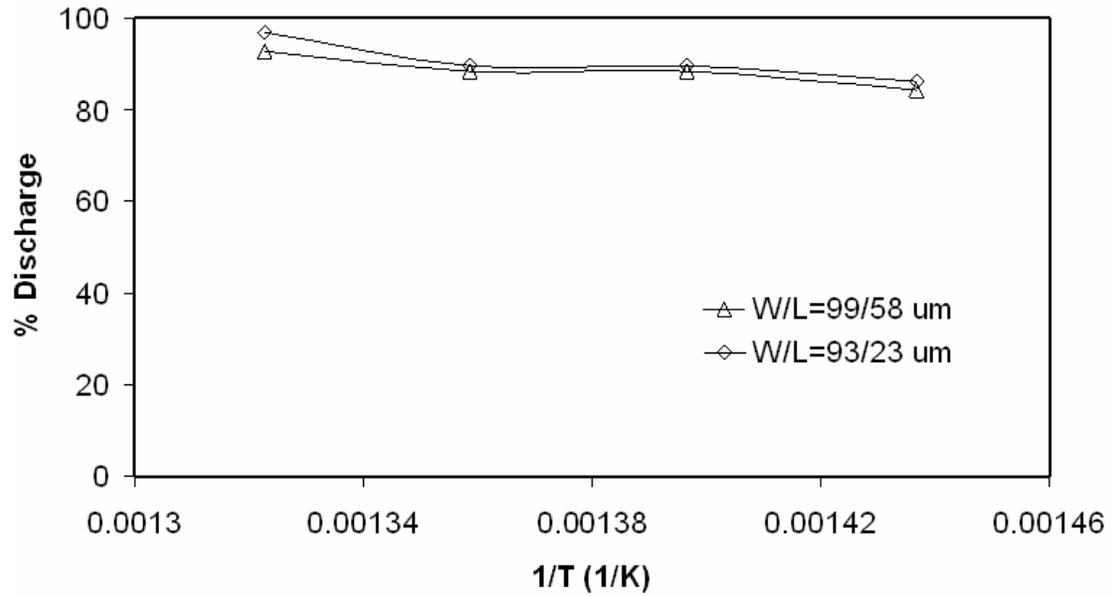


Figure 51. Temperature effect on discharge efficiency by thermal annealing. Charged at $V_g = 35$ V, $V_d = V_s = 0$ V for 10 s. Discharged by various temperature for 10 min, $V_g = V_d = V_s = 0$ V.

the stress time. Electrons were injected to the embedded gate dielectric structure when they have enough energy to overcome the barrier height between the a-Si:H channel layer and the tunnel SiN_x layer. The charge storage density increased with the stress time following the power law probably related to the defect generation mechanism in the embedded a-Si:H layer. The stored charges could be released based on difference disciplines such as electrons release by thermal activation, electron expelling and hole injection from a negative gate bias voltage, or electron-hole pairs generated from light exposure. Although most stored charges were released with the above methods, a small amount of them were strongly trapped and could not be released under the mild condition. New defects could be generated if the discharge condition is strong, such as a high annealing temperature, a very large negative gate bias voltage, or strong light exposure intensity, which hinder the charge release efficiency.

Under the dynamic operation, the charge storage decreases with the increase of

the V_d because it is easier for electrons to be transported to the drain electrode than to overcome the energy barrier between the channel a-Si:H /tunnel SiN_x gate dielectric. The discharge efficiency also decreases with the increase of the V_d in spite of the different discharge methods, i.e., the negative gate bias voltage, the exposure to light, and the high temperature thermal annealing, independently. The channel length affected the discharge efficiency, which was dependent on the discharge method. The temperature affects both the charge capacity and the discharge efficiency. The low temperature favors the charge storage but the high temperature favors the discharge.

In summary, a large number of charges can be stored and removed from the low temperature prepared floating-gate a-Si:H TFT. This is a potentially important nonvolatile memory device applicable to many products. The key parameters for the optimum operation of the low temperature fabricated nonvolatile memory device have also been revealed.

CHAPTER VII

MEMORY FUNCTIONS OF AMORPHOUS SILICON-BASED FLOATING GATE MIS CAPACITORS*

7.1 Introduction

Chapter V discusses a non volatile memory device that includes an embedded a-Si:H film in the gate dielectric of an a-Si:H TFT. This chapter will discuss the feasibility of this kind of memory device and investigated its charge trapping and detrapping mechanisms.

7.2 Experimental Method

Figure 52a shows the schematic of a floating gate MIS capacitor fabricated on Corning 1737 glass substrate. DC-sputtered Mo (100 nm thick) was used as the bottom gate and top contact electrodes. All of the embedded gate dielectric, channel (a-Si:H, 50 nm thick) and ohmic contact (n^+ μ c-Si, 50 nm thick) layers were deposited by plasma-enhanced chemical vapor deposition (PECVD) sequentially in one pump down without breaking the vacuum at 300°C with a 13.56 MHz power supply. The gate dielectric

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consisted of SiN_x (150 nm thick), a-Si:H (4, 7, or 9 nm thick), and SiN_x (150 nm thick) sandwich structure. For comparison purposes, a “control” MIS capacitor that contained SiN_x (300 nm) dielectric without the embedded a-Si:H layer was fabricated, as shown in Fig. 52b. Both types of capacitors, i.e., with 65 μm diameter, had the same channel and ohmic contact layers. The Mo layer was etched with a solution of CH₃COOH : H₃PO₄ : HNO₃ : H₂O. The PECVD n⁺, a-Si:H, and SiN_x gate dielectric layers were reactive ion etched using a mixture of Cl₂/CF₄ (8:2 sccm) at 100 mTorr and 400 W (Plasma Therm 700C). Details of the plasma conditions of the PECVD and RIE processes can be found in the literature.^{6, 42} The finished capacitor was annealed at 250°C for 1 h in air. Basic electrical and memory characteristics such as flatband voltage (V_{FB}), flatband voltage shift (ΔV_{FB}), and interface trap density (D_{it}) were extracted from the current-voltage ($C-V$) and conductance-voltage ($G-V$) curves at room temperature with Agilent 4284A LCR meter. The V_{FB} value of the $C-V$ curves was calculated from the intersection of the reciprocal of capacitance squared ($1/C^2$) vs. gate bias voltage,¹³³ where the capacitance was precorrected with the series resistance.⁹⁶ The current-voltage ($I-V$) curves were measured with Agilent 4155C semiconductor parameter analyzer.

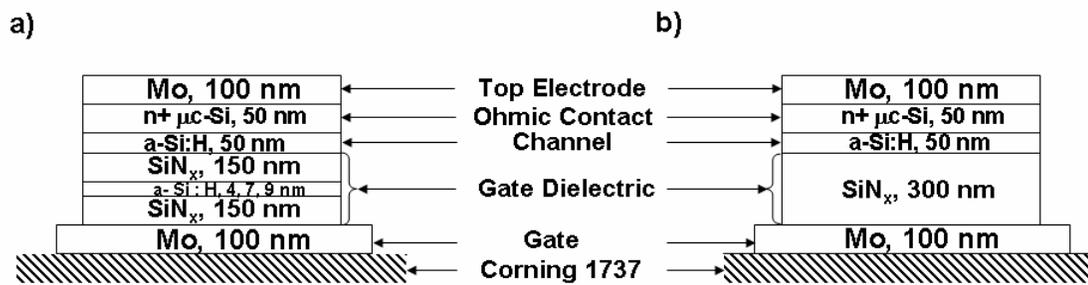


Figure 52. Structure of an MIS capacitor (a) with and (b) without embedded a-Si:H layer at the gate dielectric.

7.3 Current-Voltage Characteristic

Figures 53a and b show the J - V hysteresis curves of “control” and 9 nm embedded a-Si:H capacitors, respectively. The capacitors were swept from 20 to -20 V (forward direction) and back to 20 V (backward direction) at a rate of 0.1 V/s. For the Fig. 53a capacitor at the beginning of forward voltage sweep direction, i.e., 20 V, an accumulation layer was formed near the a-Si:H interface. Electrons were injected into the SiN_x layer, which corresponds to a high leakage current. As the voltage was reduced, the current reduced gradually, e.g., to 0 A at 4.6 V. When the voltage was less than 4.6 V, trapped electrons were released to the a-Si:H layer, which showed the opposite current flow direction as that at above 4.6 V. The magnitude of the negative current increased with the increase of negative voltage due to electrons injection from the electrode. In addition, an inversion layer was gradually formed as the magnitude of the negative V_g was increased. The current became saturated beyond -13 V because holes in the inversion region were saturated. At the high negative V_g , holes were injected from the channel a-Si:H to the SiN_x, while electrons were injected from the electrode. At the backward sweep process, e.g., from -20 to -6 V, the magnitude of the negative current dropped drastically because of the drastic reduction of holes injected from the inversion region in the a-Si:H layer and the release of trapped electron from the embedded a-Si:H layer. Above -6 V, trapped holes were back-injected to the channel a-Si:H layer. When the voltage is further increased to the positive direction, the accumulation layer was gradually formed and electrons were injected from the channel a-Si:H layer to the gate dielectric layer. Therefore, the J - V hysteresis of the device was greatly controlled by

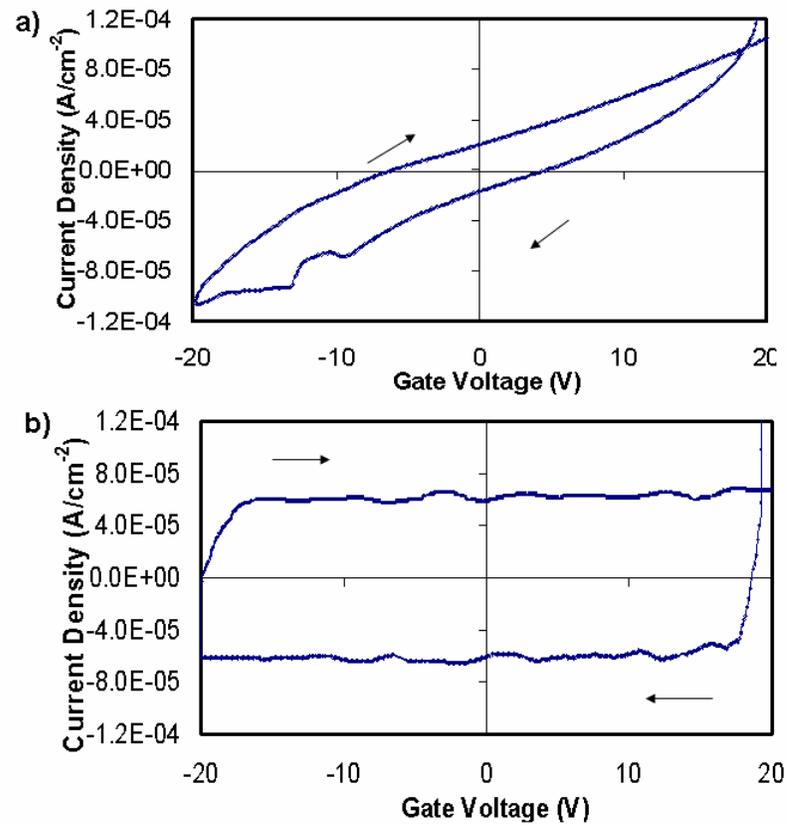


Figure 53. J - V curves for capacitor (a) without and (b) with a 9 nm embedded a-Si:H layer. Forward sweep V_g 20 to -20 V, backward sweep V_g -20 to 20 V.

trapping and detrapping of electrons and holes in the SiN_x film. This is expected because the PECVD SiN_x is a known charge trapping material.^{54, 134} Other than electron injection and trapping, hole injection and trapping have also been observed in SiN_x films when the applied voltage is high.¹³⁴

Figure 53b shows a much larger *J-V* hysteresis than that of Fig. 53a, and the current gap was greatly increased with the embedding of an a-Si:H layer. At 0 V, it had a current density of -6.5 A/cm^2 in the forward direction and 6.5 A/cm^2 in the backward direction. These two curves separated widely. For the “control” capacitor at 0 V, it had a current density of -4.5 and 4.5 A/cm^2 , respectively, in the forward and backward directions. At the high gate bias, i.e., 20 V, an electron accumulation layer was formed in the a-Si:H channel layer and electrons were injected into the gate dielectric structure. A large number of electrons were probably trapped at the interface of the embedded a-Si:H and SiN_x, which has a high defect density and a large stress mismatch. The forward current decreased rapidly when the gate bias dropped to 19 V because of the Coulomb blockade effect. When the V_g was further dropped to 17 V, the current changed the polarity due to detrapping of electrons from the embedded SiN_x layer. In addition, the current of the embedded capacitor switched polarity at a much larger positive voltage than the “control” capacitor did, i.e., 18.6 vs. 4.6 V. When the V_g was further reduced, the negative current became saturated. The embedded a-Si:H layer in the Fig. 53b capacitor accepts and releases electrons, which causes injection of electrons from the gate as well as a lag of the inversion layer formation. Because the “control” capacitor did

not have this kind of charge trapping medium, it was easier for the “control” capacitor to switch between current polarities.

The same phenomenon was observed in the backward sweep direction. For the Fig. 53b capacitor, the hole current decreased drastically from -20 to -19 V due to the decrease of the inversion region and fewer electrons were injected from the gate. Electron current then increased drastically from -19 to -15 V. From this point forward, the current started to saturate because there were more electrons available to be released from the trapping sites, i.e., the embedded a-Si:H layer. On the other hand, the “control” capacitor showed a gradual current polarity transition. The embedded layer suppressed holes injection from the a-Si:H channel layer. For example, it has a much smaller negative current than that of the “control” sample, e.g., -6×10^{-5} vs. -11×10^{-5} A/cm² at -20 V in the forward sweep direction. In other words, the embedded layer facilitated the electron injection at the high positive voltage or suppressed the hole injection at the large negative voltage from the a-Si:H channel layer.

7.4 Capacitance-Voltage Characteristic

The C-V behaviors of the “control” and the a-Si:H MIS capacitors were similar to those of a typical n-type MOS capacitor. For instance, accumulation region and depletion region of the majority carrier were observed at positive and negative gate bias, respectively. Figures 54a and b show C-V hysteresis curves of the “control” and the 9 nm a-Si:H embedded layer capacitors measured at 100 kHz, respectively.

Fig. 54a shows the C - V curve of the “control” capacitor had a ΔV_{FB} of 0.8 V. Because both V_{FB} 's were positive, i.e., 5 and 4.2 V, the “control” capacitor trapped electrons. The trapped electrons were partially released in the backward sweep direction. Fig. 54b shows the 9 nm a-Si:H embedded capacitor had a ΔV_{FB} of 2.1 V, which was 2.6 times larger than that of the Fig. 54a capacitor. Both the forward and backward C - V curves show positive V_{FB} 's, i.e., 4.3 and 2.2 V, separately. This means that the embedded a-Si:H layer enhanced the trapping of electrons compared with the “control” capacitor. The a-Si:H embedded capacitor had lower V_{FB} 's than those of the “control” capacitor in both forward and backward sweep directions. The embedded a-Si:H layer was closer to the gate electrode than the channel a-Si:H layer. Therefore, in the forward sweep direction, electrons trapped at the front side were easier to detrapp to the gate electrode than those across the SiN_x layer. In the backward sweep direction, the embedded a-Si:H attracted holes injected from the a-Si:H channel layer as well as screened the electrons injected from the electrode. The embedded a-Si:H functioned as an electron screen layer that reduced the amount of electrons trapped in the dielectric layer.

The amount of trapped charges, Q_{ot} , in an MIS capacitor can be estimated from the ΔV_{FB} measured from the C - V hysteresis and the capacitance measured at accumulation.⁹⁶ Consequently, the capacitor with embedded a-Si:H has larger storage

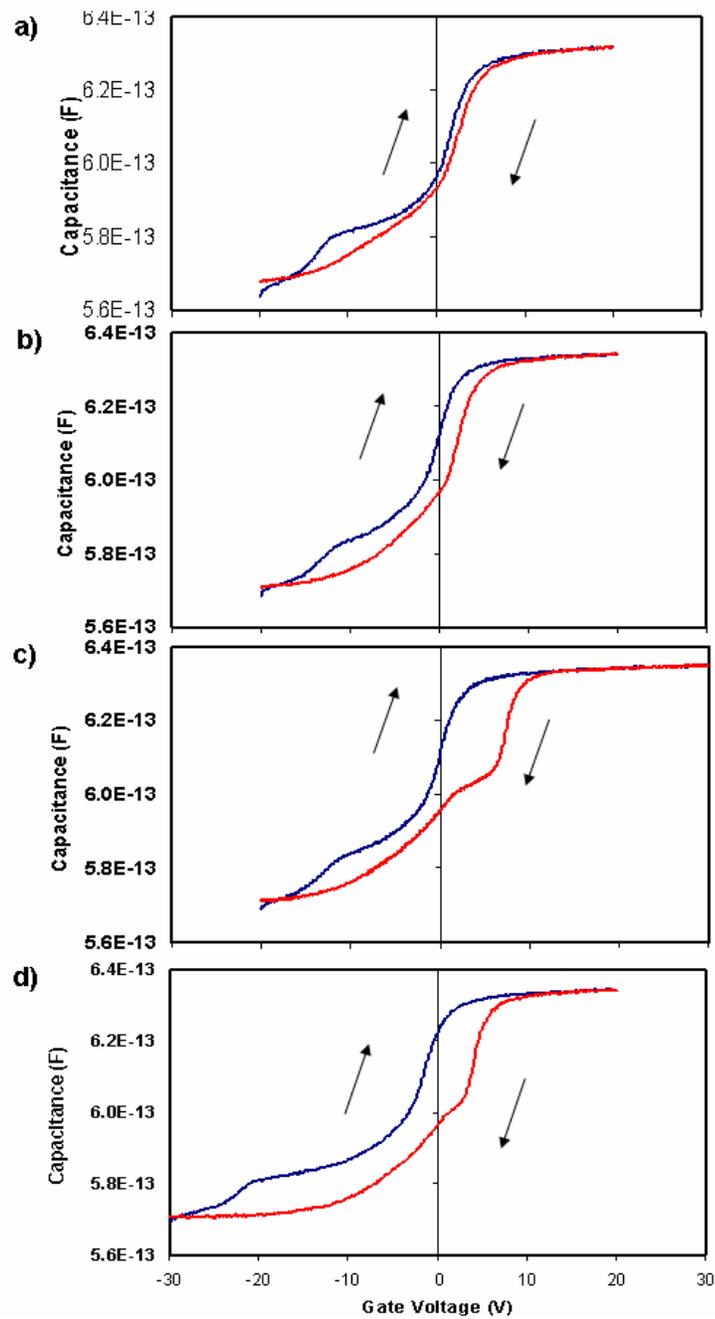


Figure 54. Hysteresis of C-V curves of capacitors (a) without the embedded layer and (b) with a 9 nm embedded capacitor at different V_g sweep ranges: (b) (+)20 V–(–)20 V–(+)20 V, (c) (+)30 V–(–)20 V–(+)30 V, and (d) (+)20 V–(–)30 V–(+)20 V. Dotted lines are the ideal C-V curves.

capacity than that of the “control” capacitors. For instance, the Q_{ot} of Fig. 54b capacitor is six times that of the Fig. 54a capacitor, i.e., 3.8×10^{-8} vs. $6.6 \times 10^{-9} \text{ C/cm}^2$.

The carrier injection mechanism of the capacitor could be verified by sweeping it through different V_g ranges.¹³⁴ Fig. 54c shows the C - V curve of the same capacitor as in Fig. 54b, except that the V_g was swept from 30 to -20 V and then back to 30 V. The V_{FB} of the backward sweep curve was independent of the range of the accumulation voltages, i.e., 2.3 V at 20 or 30 V, because the maximum amount of positive charges injected were the same at -20 V. However, the forward direction V_{FB} of Fig. 54c was much higher than that of Fig. 54b, i.e., 9.1 vs. 4.4 V, as there were more electrons injected at 30 V compared to at 20 V. Therefore, a larger ΔV_{FB} was observed in Fig. 54c compared to the one in Fig. 54b. As a result, the Q_{ot} of the Fig. 54c capacitor was three times of that of the Fig. 54a capacitor, i.e., $1.1 \times 10^{-7} \text{ C/cm}^2$ vs. $3.8 \times 10^{-8} \text{ C/cm}^2$.

Fig. 54d shows the ΔV_{FB} of the same capacitor as Fig. 54b, except that the swept was performed from 20 to -30 V (forward) and then to 20 V (backward). A lower backward direction V_{FB} than that of Fig. 54b was observed, i.e., 1.1 vs. 2.3 V. This was due to the greater number of holes injected into the floating gate because the capacitor

was biased to a larger negative bias, i.e., -30 V. Fig. 54d had a larger ΔV_{FB} than Fig. 54b had, i.e., 4.7 vs. 2.1 V and the Q_{ot} of the Fig. 54d capacitor was two times of that of Fig. 54b capacitor, i.e., 7.7×10^{-7} vs. 3.8×10^{-8} C/cm².

From the observation on the C - V characteristics of the “control” and the embedded MIS capacitors, simple energy-band diagrams at different states of operation can be constructed¹²⁰ as shown in Figure 55. When V_g of > 0 V was applied to the bottom Mo gate, electrons were injected into the a-Si:H embedded dielectric layer (Fig. 55b) and the negative charges were stored in the embedded layer (Fig. 55c), similar to the one observed in the poly-Si floating gate of the SAMOS structure [9]. As $V_g < 0$ V was applied at the gate, the trapped charges were released into the semiconductor layer (Fig. 55d) and the capacitor would return to equilibrium state (Fig. 55a). Even though both the “control” and tunneling SiN_x dielectric layers had the same thickness, the 9 nm embedded a-Si:H was thin enough to ensure the needed voltage drop across the tunneling SiN_x interface layer.

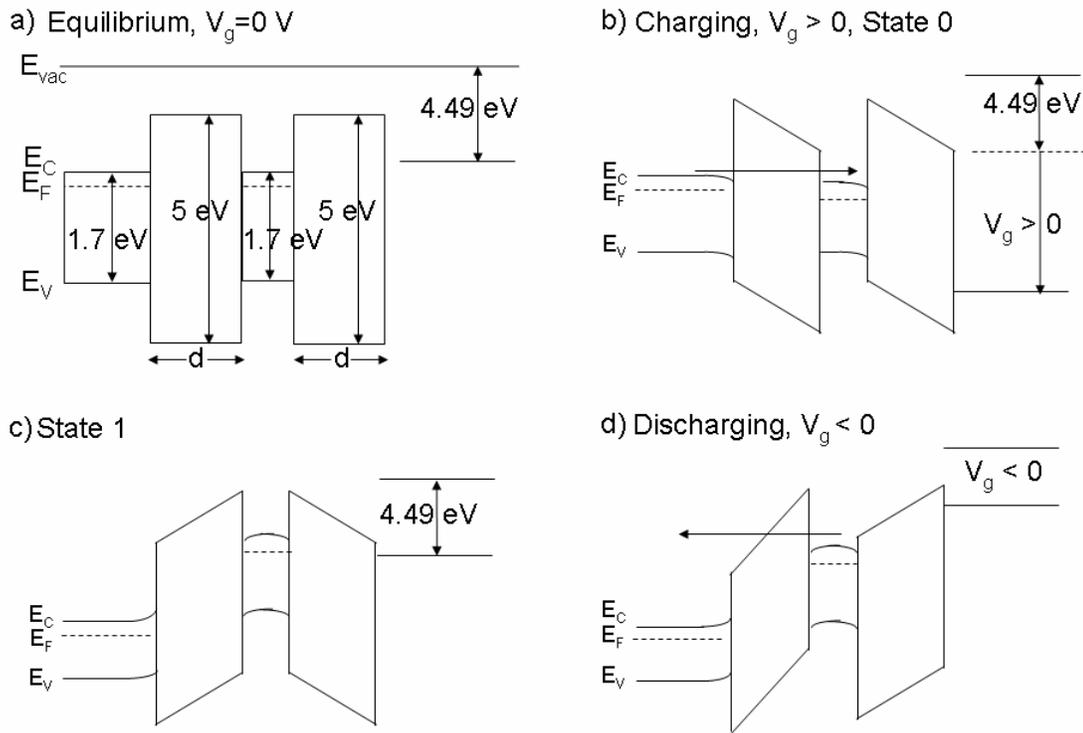


Figure 55. Energy-band diagrams for MIS capacitor with embedded a-Si:H at a) equilibrium, b) charging, state 0, c) charging, state 1, and d) discharging. (After Ref. 120)

7.5 Interface Effect

Interface effects can be qualitatively identified from the stretch out of the C - V curves when compared to an ideal C - V curve.¹³⁵ For instance, all curves in Fig. 54 show the existence of the interface state in the form of a bump at the depletion region. From Fig. 54b and c at the forward sweep, the bump was shifted to a more positive voltage with the increase of positive starting V_g . At the backward direction, the bump was shifted to a more negative voltage with the increase of negative starting V_g . Because the capacitor in Fig. 54c was biased from a higher positive V_g , the more electrons released from the embedded a-Si:H site corresponded to the increasing amount of trapped electrons at the gate dielectric channel interface. When the capacitor was biased to a higher negative bias as in Fig. 54d, there was an increasing amount of holes trapped at the same interface. This stretch out phenomenon is frequency dependent.¹²⁰ For instance, Figure 56 shows that the interface traps of both “control” and 9-nm embedded capacitors were more responsive at the low measurement frequency than that at the high frequency. The higher total capacitance at low-frequency C - V measurement compared to the high-frequency C - V was contributed by the interface capacitance (C_{it}). A similar frequency effect was also observed on the conductance-voltage (G - V) measurement. The

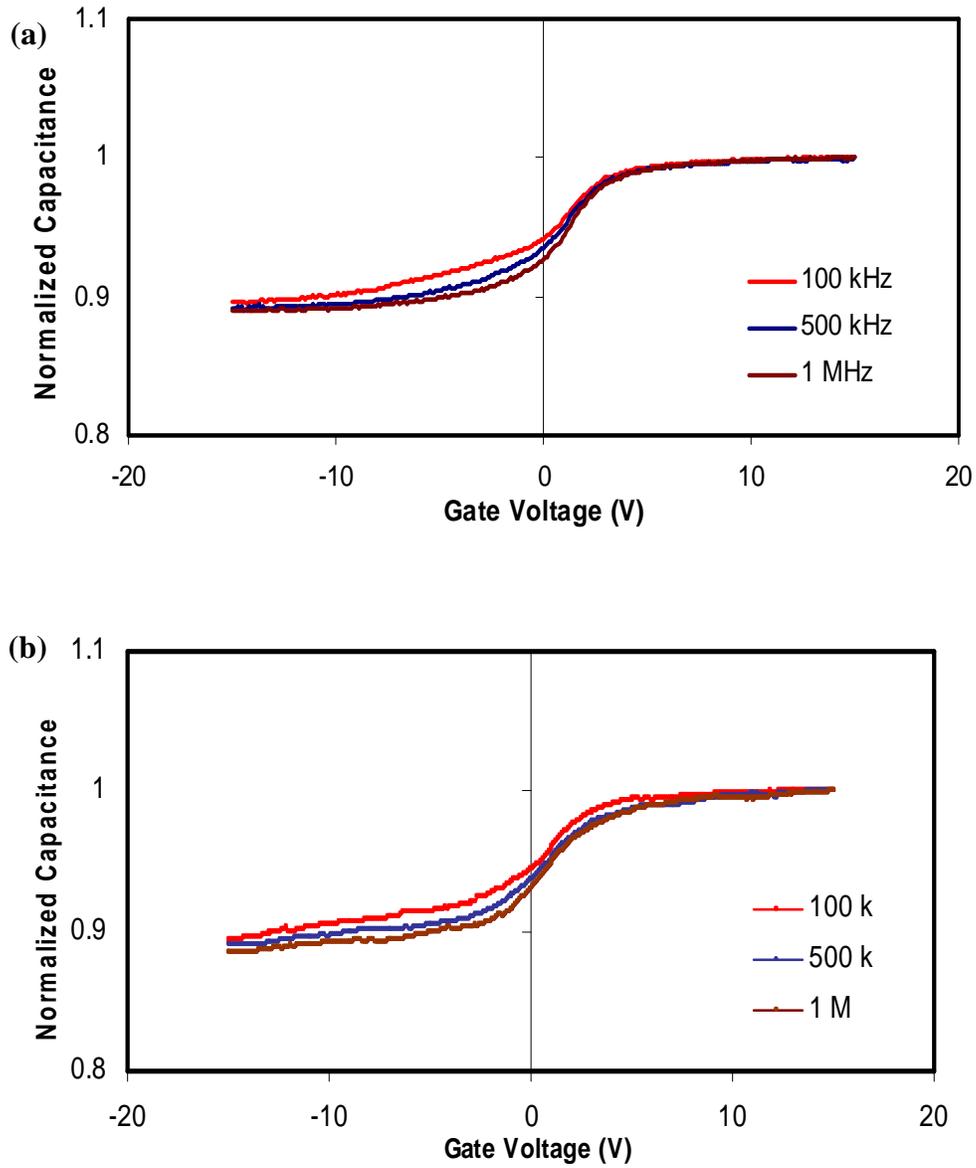


Figure 56. Normalized capacitance as a function of gate voltage for (a) 9-nm embedded and (b) control MIS capacitors.

maximum value of the G - V curves increased with measurement frequency. Because the interface traps could not synchronize in time at high frequency, the loss of energy resulted in the increase of maximum conductance.⁹⁶

7.6 Summary

In conclusion, a novel type of nonvolatile memory device, which utilizes the embedded a-Si:H layer in the gate dielectric structure to enhance the charge trapping capability of the a-Si:H-based MIS capacitor, has been fabricated and investigated. The embedded layer successfully acted as a floating gate that retained and released charges according to the polarity and magnitude of the gate bias voltage. The MIS capacitor with 9 nm embedded a-Si:H had a charge storage capacity up to six times larger than that of the capacitor without embedded layer. Properties of the embedded a-Si:H layer, such as the thickness and the composition, can influence the memory function, which requires detailed studies. This kind of memory can be applied to a wide range of low-temperature prepared solid-state circuits.

CHAPTER VIII

SUMMARY AND CONCLUSIONS

The use of highly conductive, non-refractory metal as the gate, source and drain electrodes of a TFT is required to anticipate for the RC delay and thus the detrimental effect on display quality in next generation displays. Both the p-channel and n-channel a-Si:H TFTs with Cu/TiW gate, source, and drain electrodes were successfully fabricated by utilizing a novel plasma-based Cu etching process. TiW acted as the barrier layer for Cu. The gate bias stress result showed no reliability concern, even though the Cu gate electrode was in direct contact with the gate SiN_x film. The new Cu etching process can be used to fabricate a large array of a-Si:H TFTs and CMOS-type circuits, which can be applied to a broad range of new products.

PECVD deposited SiN_x, n⁺ and a-Si:H films with 13.56 MHz plasma generator have been optimized for n-channel a-Si:H TFT application. The characteristic of the SiN_x film was optimized for comparatively low etch rate, high deposition rate, and a *RI* in the range of 1.85-1.9. The highly doped n⁺ Si film demonstrated a microcrystalline structure and prominent ohmic contact behavior. The n-channel TFTs demonstrated significant improvements, e.g., higher μ_{eff} , lower V_t , and higher I_{on}/I_{off} ratio, over the previous TFTs fabricated with PECVD films deposited with 50 kHz plasma generator.

Applications were TFTs can be potentially affected by high-energy radiation warrant the study of TFT performance under such condition. Co-60 irradiation on n-channel TFTs resulted in the shift of the transfer characteristics to a more positive V_g .

The ΔV_t increased with the increase of the irradiation dosage. The irradiation process also increased the interface state density as well as decreased the μ_{eff} and the I_{on}/I_{off} ratio; however, it did not affect the ohmic contact behavior. These effects were due to the electron-hole pairs generation in the bulk film and the damage at a-SiH/SiN_x interface. Thermal annealing of the irradiated TFTs almost restored all electrical characteristics to their pre-irradiation state.

Floating gate n-channel a-Si:H TFT with embedded a-Si:H at the SiN_x gate dielectric has been demonstrated to be an effective memory device. The fabrication process included simple two-photomask lithography. The dielectric/channel/ top dielectric stack was deposited in one pump down and the maximum process temperature was 300°C. Therefore, the device is expected to be applicable to many low-temperature, large-area, flexible substrate applications. The memory characteristics were observed and quantified from the hysteresis of the TFT's transfer characteristics, which increased with the increase of the sweep V_g range. The programmability and retention characteristics have also been studied. The memory window based on the channel

conductance measurement was at 1 V threshold voltage shift. A charge retention time greater than 3600 s was achieved. The TFT's various memory characteristics may be further improved by optimizing material properties and thickness of each composing film of the gate dielectric structure.

The charge and discharge study of the a-Si:H TFT memory under a static or dynamic operating condition is needed to improve the operation and the reliability of the device. In both operating conditions, the charge storage to the a-Si:H floating gate is related to the energy to overcome the barrier height between the a-Si:H channel layer and the tunnel SiN_x layer and the defect generation mechanism in the embedded a-Si:H layer. The stored charges could be released based on different disciplines such as electrons release by thermal activation, electron expelling and hole injection from a negative gate bias voltage, or electron-hole pairs generated from light exposure. A small amount of the stored charges were strongly trapped and could not be released under the mild condition. Under the dynamic operation, the charge storage efficiency decreases

with the increase of the drain bias. This is related to the energy barrier between the channel a-Si:H /tunnel SiN_x gate dielectric. The discharge efficiency also decreases with the increase of the V_d in spite of the different discharge methods.

A large number of charges can be stored and removed from the low temperature prepared floating-gate a-Si:H TFT. The key parameters for the optimum operation are low temperature operation for storage and higher temperature operation for discharge. Based on the charge and discharge ability, the floating gate a-Si:H device has exhibited the potential as nonvolatile memory device fabricated at low temperature which is applicable to many practical applications.

MIS capacitor with embedded a-Si:H layer in the gate dielectric structure demonstrated nonvolatile memory characteristic. The embedded layer enhanced the charge trapping capability of the a-Si:H-based capacitor by retaining and releasing charges according to the polarity and magnitude of the gate bias voltage. The capacitor with 9 nm embedded a-Si:H had a charge storage capacity up to six times larger than that of the capacitor without embedded layer. Properties of the embedded a-Si:H layer such as the thickness and the composition can influence the memory function and requires detailed studies.

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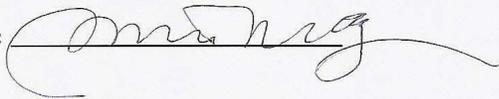
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