A CMOS 500 MHZ CONTINUOUS-TIME FOURTH ORDER 0.05° EQUIRIPPLE LINEAR PHASE FILTER WITH AUTOMATIC TUNING

A Thesis

by

PANKAJ PANDEY

Submitted to the Office of Graduate Studies of Texas A&M University in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2003

Major Subject: Electrical Engineering
A CMOS 500 MHZ CONTINUOUS-TIME FOURTH ORDER 0.05° EQUIRIPPLE LINEAR PHASE FILTER WITH AUTOMATIC TUNING

A Thesis

by

PANKAJ PANDEY

Submitted to Texas A&M University
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE

Approved as to style and content by:

Jose Silva-Martinez
(Chair of Committee)

Edgar Sanchez-Sinencio
(Member)

Aydin Karsilayan
(Member)

Mladen Kezunovic
(Member)

Cesar O. Malave
(Member)

Chanan Singh
(Head of Department)

May 2003

Major Subject: Electrical Engineering
ABSTRACT

A CMOS 500 MHz Continuous-Time Fourth Order 0.05° Equiripple Linear Phase Filter with Automatic Tuning. (May 2003)
Pankaj Pandey, B.E., Regional Engineering College, Surat, India
Chair of Advisory Committee: Dr. Jose Silva-Martinez

The growing demand of portable electronic equipment and system-on-a-chip has been pushing the industry to design circuits with very low power supply voltage and low power consumption. The Hard Disk drive industry is looking for developments in the read channel chip to push the data rates to higher speed, along with a low voltage and low cost solution. Read channel requires high-speed linear phase filters to meet these objectives. The primary objective of this project is to design, layout, and characterize a 4th-order continuous-time equiripple linear phase filter with automatic tuning system. The main requirements for design are high speed, low group delay variations, good linearity and power efficiency.

This filter features wide cut-off frequency 500MHz, which is far beyond the current state-of-the-art. The linear phase filter is based on Gm-C biquadratics. Higher speed has been achieved by minimizing the parasitics and a complementary input stage OTA. A common mode feedback (CMFB), which ensures stability at such high frequencies, has also been designed. The inaccuracies of the filter are compensated by using a simple automatic tuning system.

The design is fabricated in 0.35 μ TSMC CMOS process technology. The design was simulated in Cadence using SPICE models provided by MOSIS for the 0.35 μ TSMC process in the presence of parasitic capacitance and transistor non-idealities. Cut-off frequency of 500 MHz was achieved along with a 9% variation in the group delay.
To my parents and sister
ACKNOWLEDGMENTS

I would like to express gratitude to my advisor Dr. Jose Silva-Martinez, for his constant guidance, support and patience throughout this research work. I am deeply indebted to him for all the knowledge and help he has extended to me. I would also like to thank my committee members for their valuable suggestions and their cooperation.

I am indebted to my colleagues in the AMSC group who have helped me to enhance my knowledge through various discussions and interactions. Special mention goes to Ming Deng Chen, Husseyin Dinc and Narayan Prasad Ramachandran. Finally I am grateful to my parents and sister who inspired me to pursue my dreams.
TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>CHAPTER</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>INTRODUCTION .......................................................................................................... 1</td>
</tr>
<tr>
<td>A.</td>
<td>Architecture of Hard Disk Drive .......................................................................... 2</td>
</tr>
<tr>
<td>1.</td>
<td>Previous Work ........................................................................................................ 4</td>
</tr>
<tr>
<td>B.</td>
<td>Organization of the Thesis .................................................................................... 5</td>
</tr>
<tr>
<td>II</td>
<td>LINEAR PHASE FILTERS ........................................................................................................ 7</td>
</tr>
<tr>
<td>A.</td>
<td>Group Delay Response ............................................................................................ 7</td>
</tr>
<tr>
<td>B.</td>
<td>Transfer Function of the Filter .............................................................................. 9</td>
</tr>
<tr>
<td>C.</td>
<td>Building Blocks of the Filter ............................................................................... 11</td>
</tr>
<tr>
<td>1.</td>
<td>Two Integrator Loop ............................................................................................. 11</td>
</tr>
<tr>
<td>2.</td>
<td>Lossy Integrator .................................................................................................... 13</td>
</tr>
<tr>
<td>3.</td>
<td>Realization of a Biquad ......................................................................................... 14</td>
</tr>
<tr>
<td>4.</td>
<td>Fully Differential Implementation ....................................................................... 17</td>
</tr>
<tr>
<td>III</td>
<td>DESIGN OF SUITABLE OTA ............................................................................................. 19</td>
</tr>
<tr>
<td>A.</td>
<td>Design Considerations for High Frequency Applications ..................................... 19</td>
</tr>
<tr>
<td>1.</td>
<td>Effect of Parasitic Capacitor ................................................................................. 19</td>
</tr>
<tr>
<td>2.</td>
<td>Effect of Saturation Voltage ($V_{DSAT}$) on the OTA ........................................ 20</td>
</tr>
<tr>
<td>3.</td>
<td>Effect of Non-dominant Poles .............................................................................. 21</td>
</tr>
<tr>
<td>4.</td>
<td>Possible OTA Implementations ............................................................................ 21</td>
</tr>
<tr>
<td>B.</td>
<td>OTA Architecture .................................................................................................... 25</td>
</tr>
<tr>
<td>1.</td>
<td>Linearization Techniques ....................................................................................... 26</td>
</tr>
<tr>
<td>2.</td>
<td>Effective $g_m$ of the OTA employed ................................................................... 27</td>
</tr>
<tr>
<td>C.</td>
<td>Design Specifications and Considerations for the OTA ...................................... 29</td>
</tr>
<tr>
<td>1.</td>
<td>Minimum Requirements from the OTA ................................................................. 29</td>
</tr>
<tr>
<td>CHAPTER</td>
<td>Page</td>
</tr>
<tr>
<td>---------</td>
<td>------</td>
</tr>
<tr>
<td>2. Small Signal Model of the OTA</td>
<td>31</td>
</tr>
<tr>
<td>D. Simulation Results of the OTA</td>
<td>35</td>
</tr>
<tr>
<td>IV DESIGN OF COMMON-MODE FEEDBACK CIRCUIT</td>
<td>40</td>
</tr>
<tr>
<td>A. Design Considerations for Common-Mode Feedback Circuit</td>
<td>40</td>
</tr>
<tr>
<td>1. Why Common-Mode control is Needed</td>
<td>40</td>
</tr>
<tr>
<td>2. Sensing and Amplification Circuit</td>
<td>41</td>
</tr>
<tr>
<td>B. Possible Implementation of CMFB Circuit</td>
<td>43</td>
</tr>
<tr>
<td>1. A Simple CMFB Circuit</td>
<td>44</td>
</tr>
<tr>
<td>2. A Current Feedback Based CMFB</td>
<td>46</td>
</tr>
<tr>
<td>C. Design Considerations for the New Common-Mode Scheme</td>
<td>48</td>
</tr>
<tr>
<td>D. Simulation Results</td>
<td>50</td>
</tr>
<tr>
<td>V DESIGN OF TUNING CIRCUIT</td>
<td>55</td>
</tr>
<tr>
<td>A. Overview of Tuning Circuit</td>
<td>55</td>
</tr>
<tr>
<td>1. Why Tuning Circuit is Required</td>
<td>55</td>
</tr>
<tr>
<td>2. General Concepts in Tuning</td>
<td>55</td>
</tr>
<tr>
<td>B. Possible Tuning Implementations</td>
<td>57</td>
</tr>
<tr>
<td>1. Prominently Used Tuning Techniques</td>
<td>57</td>
</tr>
<tr>
<td>C. Implementation of a Tuning Scheme</td>
<td>59</td>
</tr>
<tr>
<td>1. Operation of the Tuning Circuit</td>
<td>61</td>
</tr>
<tr>
<td>2. Tuning Circuit Specifications and Design</td>
<td>63</td>
</tr>
<tr>
<td>D. Simulations Results of the Tuning Circuit</td>
<td>67</td>
</tr>
<tr>
<td>1. Tuning Voltage</td>
<td>67</td>
</tr>
<tr>
<td>2. Filter Output with the Tuning Voltage</td>
<td>68</td>
</tr>
<tr>
<td>3. Variation of the Tuning Voltage with Load Capacitor</td>
<td>69</td>
</tr>
<tr>
<td>4. Rectified Voltage</td>
<td>70</td>
</tr>
</tbody>
</table>
VI   SIMULATION RESULTS OF THE FILTER ............................................................... 73
    A. Schematic Level Simulation Results of Biquads Without Tuning ............. 73
       1. Estimation of the Parasitic Capacitance ......................................... 73
       2. Schematic Level Simulation Results of Biquad 1 .............................. 75
       3. Schematic Level Simulation Results of Biquad 2 .............................. 78
    B. Schematic Level Simulation Results of Overall Filter Without Tuning .... 82
    C. Schematic Level Simulation Results of Overall Filter With Tuning ........ 93
    D. Post Layout Simulation Results of the Overall Filter Without Tuning ...... 97
    E. Post Layout Simulation Results of the Filter With Tuning .................... 105

VII  SUMMARY AND CONCLUSIONS ..................................................................... 111

REFERENCES ........................................................................................................... 112

VITA .......................................................................................................................... 116
# LIST OF FIGURES

<table>
<thead>
<tr>
<th>FIGURE</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Storage system segmentation</td>
</tr>
<tr>
<td>2</td>
<td>Architecture of hard disk drive analog front end</td>
</tr>
<tr>
<td>3</td>
<td>Equiripple delay versus Bessel-Thomson delay performance</td>
</tr>
<tr>
<td>4</td>
<td>Two-integrator loop with non-ideal integrators</td>
</tr>
<tr>
<td>5</td>
<td>A transconductor loaded by an impedance Z</td>
</tr>
<tr>
<td>6</td>
<td>Lossy $g_m$-C integrator</td>
</tr>
<tr>
<td>7</td>
<td>The single-ended $g_m$-C realization of a Biquad</td>
</tr>
<tr>
<td>8</td>
<td>Fully differential Biquad with common-mode feedback circuit</td>
</tr>
<tr>
<td>9</td>
<td>Fully differential fourth-order equiripple linear phase filter</td>
</tr>
<tr>
<td>10</td>
<td>Folded-cascode and two current mirror OTA</td>
</tr>
<tr>
<td>11</td>
<td>Current mode integrator and Nauta’s transconductor</td>
</tr>
<tr>
<td>12</td>
<td>OTA architecture</td>
</tr>
<tr>
<td>13</td>
<td>$g_m$ linearization schemes using source degeneration</td>
</tr>
<tr>
<td>14</td>
<td>Parasitic capacitors in the OTA</td>
</tr>
<tr>
<td>15</td>
<td>Small signal model of the OTA</td>
</tr>
<tr>
<td>16</td>
<td>Frequency response of the OTA</td>
</tr>
<tr>
<td>17</td>
<td>DC response of the OTA</td>
</tr>
<tr>
<td>18</td>
<td>Variation of effective $G_m$ with the input</td>
</tr>
<tr>
<td>19</td>
<td>Variation of the $G_m$ with frequency</td>
</tr>
<tr>
<td>20</td>
<td>Excess phase of the OTA</td>
</tr>
<tr>
<td>FIGURE</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>21</td>
<td>Simplified model of high gain amplifier</td>
</tr>
<tr>
<td>22</td>
<td>Conceptual topology for common-mode feedback</td>
</tr>
<tr>
<td>23</td>
<td>Common mode sensing available in the OTA</td>
</tr>
<tr>
<td>24</td>
<td>Typical common-mode feedback scheme</td>
</tr>
<tr>
<td>25</td>
<td>The new current feedback CMFB</td>
</tr>
<tr>
<td>26</td>
<td>Movement of pole location</td>
</tr>
<tr>
<td>27</td>
<td>Generation of copy of reference voltage</td>
</tr>
<tr>
<td>28</td>
<td>Effect of other parasitic and introduction of zero</td>
</tr>
<tr>
<td>29</td>
<td>Previously implemented CMFB scheme</td>
</tr>
<tr>
<td>30</td>
<td>Common-mode oscillations</td>
</tr>
<tr>
<td>31</td>
<td>Test for the stability of common-mode loop</td>
</tr>
<tr>
<td>32</td>
<td>Frequency response of the open loop CMFB circuit</td>
</tr>
<tr>
<td>33</td>
<td>Step response of CMFB loop with current injection</td>
</tr>
<tr>
<td>34</td>
<td>Effect of size of Mp on the phase margin</td>
</tr>
<tr>
<td>35</td>
<td>Indirect frequency tuning by adjusting the $g_m$</td>
</tr>
<tr>
<td>36</td>
<td>Tuning scheme based on squarer</td>
</tr>
<tr>
<td>37</td>
<td>Overall tuning architecture</td>
</tr>
<tr>
<td>38</td>
<td>Frequency response of the integrator</td>
</tr>
<tr>
<td>39</td>
<td>Voltage to current converter</td>
</tr>
<tr>
<td>40</td>
<td>Current mirrors used for integrator circuit &amp; the reference circuit</td>
</tr>
<tr>
<td>41</td>
<td>Rectification and removal of ripples</td>
</tr>
<tr>
<td>FIGURE</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>-------------</td>
</tr>
<tr>
<td>42</td>
<td>Two stage high gain amplifier</td>
</tr>
<tr>
<td>43</td>
<td>Tuning voltage with a nominal load of 1pF</td>
</tr>
<tr>
<td>44</td>
<td>Transient output of the filter with the tuning voltage applied to the filter</td>
</tr>
<tr>
<td>45</td>
<td>Variation of the tuning voltage with the variation in load capacitor</td>
</tr>
<tr>
<td>46</td>
<td>Rectified voltages after the rectification operation</td>
</tr>
<tr>
<td>47</td>
<td>A zoom in view of rectified signal with the ripples</td>
</tr>
<tr>
<td>48</td>
<td>Frequency response of Biquad1 at the lowpass node</td>
</tr>
<tr>
<td>49</td>
<td>Group delay of Biquad1 at lowpass node</td>
</tr>
<tr>
<td>50</td>
<td>Transient response of Biquad1 at 500 MHz signal</td>
</tr>
<tr>
<td>51</td>
<td>Discrete Fourier Transform of the differential output of Biquad1</td>
</tr>
<tr>
<td>52</td>
<td>Frequency response of Biquad2 at the lowpass node</td>
</tr>
<tr>
<td>53</td>
<td>Magnitude response at the bandpass node of Biquad2</td>
</tr>
<tr>
<td>54</td>
<td>Transient response of Biquad2 at 500 MHz signal</td>
</tr>
<tr>
<td>55</td>
<td>Discrete Fourier Transform of the differential output of Biquad2</td>
</tr>
<tr>
<td>56</td>
<td>Overall filter architecture with the buffer at the output</td>
</tr>
<tr>
<td>57</td>
<td>Frequency response of overall filter(without buffer), Biquad1 and Biquad2</td>
</tr>
<tr>
<td>58</td>
<td>Frequency of the overall filter (without buffer)</td>
</tr>
<tr>
<td>59</td>
<td>Frequency response of the buffer along with the overall filter response</td>
</tr>
<tr>
<td>60</td>
<td>Group delay of the overall filter</td>
</tr>
<tr>
<td>61</td>
<td>Group delay at the output of the buffer</td>
</tr>
<tr>
<td>62</td>
<td>Fully differential sinusoidal output of the overall filter</td>
</tr>
<tr>
<td>FIGURE</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>------</td>
</tr>
<tr>
<td>63</td>
<td>Fully differential sinusoidal output at the buffer output</td>
</tr>
<tr>
<td>64</td>
<td>DFT of the overall filter</td>
</tr>
<tr>
<td>65</td>
<td>DFT at the output of the buffer</td>
</tr>
<tr>
<td>66</td>
<td>Differential output of the overall filter with tuning</td>
</tr>
<tr>
<td>67</td>
<td>Differential output at the buffer with tuning</td>
</tr>
<tr>
<td>68</td>
<td>DFT of the differential output of the overall filter with tuning</td>
</tr>
<tr>
<td>69</td>
<td>DFT of the differential output at the buffer output with tuning</td>
</tr>
<tr>
<td>70</td>
<td>Layout of the main OTA</td>
</tr>
<tr>
<td>71</td>
<td>Floor plan of the layout showing the individual building blocks</td>
</tr>
<tr>
<td>72</td>
<td>Layout of the filter</td>
</tr>
<tr>
<td>73</td>
<td>Post layout: frequency response of the filter and Biquads</td>
</tr>
<tr>
<td>74</td>
<td>Post layout: frequency response of the overall Filter and buffer output</td>
</tr>
<tr>
<td>75</td>
<td>Post layout: group delay of the overall filter and at the output of buffer</td>
</tr>
<tr>
<td>76</td>
<td>Post layout: DFT of the differential output of the buffer without tuning</td>
</tr>
<tr>
<td>77</td>
<td>Frequency response of the overall filter and filter + buffer with tuning</td>
</tr>
<tr>
<td>78</td>
<td>Group delay of the overall filter and filter + buffer with tuning</td>
</tr>
<tr>
<td>79</td>
<td>Post layout: magnitude of the tuning voltage</td>
</tr>
<tr>
<td>80</td>
<td>Post layout: differential output of the buffer with tuning</td>
</tr>
<tr>
<td>81</td>
<td>Post layout: Monte Carlo simulation results</td>
</tr>
</tbody>
</table>
# LIST OF TABLES

<table>
<thead>
<tr>
<th>TABLE</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>Brief summary of previously reported work</td>
<td>5</td>
</tr>
<tr>
<td>II</td>
<td>Denominator of equiripple linear phase transfer function</td>
<td>9</td>
</tr>
<tr>
<td>III</td>
<td>Values of transconductances and capacitors to be implemented</td>
<td>17</td>
</tr>
<tr>
<td>IV</td>
<td>OTA specifications</td>
<td>30</td>
</tr>
<tr>
<td>V</td>
<td>Aspect ratio of the transistors</td>
<td>34</td>
</tr>
<tr>
<td>VI</td>
<td>Summary of OTA results</td>
<td>39</td>
</tr>
<tr>
<td>VII</td>
<td>Summary of post layout simulation results of the filter</td>
<td>110</td>
</tr>
</tbody>
</table>
CHAPTER I
INTRODUCTION

Storage devices have been divided on the basis of their performance, typically specified in terms of the access time to the stored data, and cost quoted in terms of $/Mbyte. Fig. 1 shows the division of some commonly used storage devices. The cost sensitive application like data distribution and entertainment music use devices like CD-ROM, which have high access time and are low priced. Tape storage and backup systems use lower performing systems. But the Hard Disk Drive (HDD) systems are high performance systems and near real-time applications [1]. HDD systems continue to develop at a rapid and deterministic pace to meet the emerging demands of high performance computing and peripheral devices.

Fig. 1. Storage system segmentation.

This thesis follows the format of IEEE Journal of Solid State Circuits.
A. Architecture of Hard Disk Drive

Read Channel chip is very important part of the HDD system. Advances in read channel technology has lead to the increase in the areal densities of the HDD by more than 50% over last few years. Read channel is also evolving at a very fast pace to keep up with the advancements in HDD technology. Peak detection method in read channel enjoyed widespread use for more than 30 years. It was replaced by Partial response maximum Likelihood (PRML) method, which was subsequently replaced by more powerful Extended PRML. Current trend is based on combining channel coding and equalization. The magnetic media and Preamplifier stage of the HDD system can be considered as a bandwidth-limited channel. Data is recorded on the magnetic media using binary amplitude levels. The read back signal is analog. This signal is corrupted by distortion, noise and interference. The read channel involves a lot of signal processing and tries to extract reliable binary data from the magnetic media.

The corrupting noise in the signal is mostly electronic noise and media noise. But the biggest source of signal corruption is inter-symbol interference (ISI). At the higher linear densities, the linear model of the magnetic recording channel breaks down. Since the binary signal transitions are stored pretty packed due to ever increasing data density, the read back signal amplitude is difficult to decipher. This degrades the Signal to Noise ratio SNR and effectively reflects as higher Bit error rate (BER). Signal processing can only marginally compensate this effect. Hence Inter-symbol interference is by far the dominant effect of high-density recording. The PRML technique, which helps in reducing ISI, is used widely in the industry [1]. Most of them use an ADC, a FIR filter and a continuous time filter for channel equalization. Most of the equalizer architectures use a continuous time Gm-C filter, because of their higher frequency and simplicity, modularity and easy programming of the Biquads involved.

In this dissertation we would be presenting the design of a high frequency low pass equiripple linear phase Gm-C based filter used for equalization in HDD systems. As mentioned earlier PRML technique allows us to increase the data density by up to 100%
as compared to peak detect methods. However this increase is obtained at the expense of better channel equalization and detection techniques. A large number of such equalization techniques have been reported in the literature utilizing primarily analog or analog and digital methods. Some of them employ multiple chip [2] [3] or discreet external block [4] solutions. A predominantly analog design can help in reducing the cost and also avoid the noise-related issues involved with mixed mode design. One of the commonly used PRML based mixed-mode read channel path [5] has been shown in Fig.2. The above figure shows the analog front-end pulse processing with digital data detection. The preamplifier block along with noise reduction amplifies the signal from the magnetic media. This signal is then fed into the variable gain amplifier (VGA). The filter block performs some signal equalization. The signal then goes to the analog-to-digital conversion (ADC) block, typically of 6bit resolution. The digital signal processor (DSP) core can perform additional equalization, if necessary, and implements the data detector. It also controls gain and timing as well as communicates with the interface.

The equalization task involves tradeoffs between the design of analog filter and the digital finite impulse response (FIR) filter. The analog filter can be made more complex to improve the performance and this will relax the requirement on the power consumption and complexity and order of the digital FIR filter for a given silicon area. In
certain applications the analog filter performs only the task of noise anti-aliasing filter while the equalization task is done completely in the digital domain. But if a significant amount of equalization is done in the digital domain then the quantization noise produced by the ADC is enhanced by the digital FIR filter. This results in increased complexity and resolution of the ADC to reduce the quantization noise contribution. Presently in most of the designs the equalization is done mostly analog domain, as it is easier to implement high frequency designs and still reliably perform the equalization task.

The analog filter can perform some or all of the equalization required to match the pulse shape data retrieved from the magnetic media to a target pulse shape. The usual target pulse shapes are PR4, EPR4 or $E^2$PR4. Approximate pulse symmetry is usually found in incoming pulses from the magnetic media. Consequently, the group delay of the filter is required to exhibit a relatively flat characteristic in the band of interest.

1. Previous Work

In this thesis we will be designing the analog continuous time filter with a linear phase, which reflects as a flat group delay. Another role of the filter will be to minimize the incoming noise from the media, preamplifier, and VGA effectively increasing the Signal to noise ratio. In some of the approaches [5] reported in literature 7th order filters have been reported to get a real flat group delay response up to $1.75f_c$, where $f_c$ is the 3dB cutoff frequency of the filter. However instead of using a Bessel filter for a flat group delay response these approaches are mostly based on an equiripple linear phase response, which extends the range of flatness for the group delay response. In case of Bessel-type transfer function the flatness of the group delay response normally fades around $1.2f_c$. A traditional approach in defining the filter pole constellation when a flat group delay characteristic is needed is described in [6] and is based on the above mentioned equiripple approximation of the phase. In [5] such a seven-pole constellation, which yields linear phase almost up to $2f_c$, was selected. However this scheme had a two zeroes on the real axis in the seven-pole constellation thus resulting effectively in a fifth-order
roll-off. The placement of these left and right half zeroes was externally controlled and this resulted in a better correction of flat group delay response in the band of interest, thus helping to equalize somewhat asymmetrical pulses from the media.

A brief summary of some of the previously reported work has been shown in Table I. These design range over different processes. The cut-off frequency $f_c$ is in general in the range of 150MHz. There is a requirement in the hard disk industry to push this speed to even higher frequencies for higher data rates. The tuning schemes are pretty involved

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.6µ CMOS</td>
<td>0.7µ CMOS</td>
<td>0.29µ BiCMOS</td>
<td>0.35µ CMOS</td>
</tr>
<tr>
<td>$F_c$</td>
<td>50MHz</td>
<td>43MHz</td>
<td>150MHz</td>
<td>150MHz</td>
</tr>
<tr>
<td>Tuning</td>
<td>Charge comparison</td>
<td>Charge comparison</td>
<td>Not included</td>
<td>Power comparison</td>
</tr>
<tr>
<td>Group delay error</td>
<td>&lt;2%</td>
<td>&lt;2%</td>
<td>&lt;5%</td>
<td>&lt;3%</td>
</tr>
<tr>
<td>THD</td>
<td>&lt;-40 dB</td>
<td>&lt;-46 dB</td>
<td>&lt;-46 dB</td>
<td>&lt;-46 dB</td>
</tr>
<tr>
<td>DR</td>
<td>60 dB</td>
<td>----</td>
<td>48 dB</td>
<td>51 dB</td>
</tr>
<tr>
<td>Power</td>
<td>90 mW</td>
<td>120 mW</td>
<td>120 mW</td>
<td>37 mW</td>
</tr>
</tbody>
</table>

B. Organization of the Thesis

This thesis gives an overview of the design of high frequency continuous-time filter design. The concepts and design considerations have been discussed at great length. An effort has been made to deliver solution to the problems that normally plague high frequency design. A novel method has been presented for common-mode feedback,
which utilizes a current feedback. This realization also improves stability issues related to high frequency CMFB circuits and also is very robust. A novel method has been developed for the automatic tuning of the filter. Transistor level implementation of the design is realized in 0.35µm TSMC process.

Chapter II details the issues of linear phase filters. A brief overview has been provided on the applications and design considerations of equiripple linear phase filters. Also the design specifications required for the filter have been deduced in the chapter.

Chapter III presents a discussion of implementation issues in high frequency filter design. The design considerations of the integrator to be used have been discussed at length. Also the transistor level realization of the integrator has been shown. The simulation results and the performance of the OTA (Operational Transconductance Amplifier) have been discussed at length.

Chapter IV presents a discussion of common-mode feedback scheme.

Chapter V discusses the novel tuning scheme.

Chapter VI discusses the overall performance of the fourth order filter shows the post layout simulation results.

An effort will be made to discuss more of the design related issues rather than the background and history behind the concepts. This will make the dissertation more concise but will still be providing a clear insight into the design.
CHAPTER II
LINEAR PHASE FILTERS

The primary function of the linear phase filter is to lower the achievable error rates by band limiting the noise originating in the magnetic media and the preamplifier. The second role of the filter is to equalize the bit stream, i.e. to slim the data pulses, allowing higher densities. The filter tries to equalize the binary data from the media to some target data pulse such as PR4, EPR4, and E^2PR4. All these target pulses exhibit symmetry around the pulse peak. To minimize the pulse peak shifts in time, an accurate linear phase (or constant group delay) response in the signal bandwidth is essential. Pulse equalizers in read channel are normally realized as high order low pass filters. Bessel filters and 0.05° equiripple on the phase filters are mostly used.

A. Group Delay Response

One of the important specifications of the pulse equalizer is the ripple on the group delay. It should be generally smaller than 5%. The ripple on the group delay is defined as the variation of the group delay relative to the normal group delay in a certain frequency band. It is given by the following equation.

\[
\text{nominal group delay :} \\
t_{\text{g}_r\_\text{nom}} = \frac{\max [t_{\text{g}_r}(f)] - \min [t_{\text{g}_r}(f)]}{2}
\]

\[
\text{ripple on the group delay :} \\
\text{ripple} = \frac{\max [t_{\text{g}_r}(f)] + \min [t_{\text{g}_r}(f)]}{2t_{\text{g}_r\_\text{nom}}}
\]

Where \(\min\) and \(\max\) are taken over the range \(0.2f_c < f < 1.7f_c\), \(f_c\) is the filter’s cutoff frequency, and \(t_{\text{g}_r}(f)\) is the group delay.

The importance of this specification is motivated by the fact that the information content of the signal at the read head of the hard disk is held in the time at which the pulse occurs. If the group delay is not constant in the frequency band where spectral
components of the signal are located, the pulse might shift in time due to the equalizer. This means that the equalizer is affecting the information content of the signal. For this particular design a very high cutoff frequency is an important requirement. The high cutoff frequency will allow even higher data rates. As a rule of thumb for data rates up to 1Gbp/s we need a filter whose cutoff frequency is at least 500Mhz. However designing filters operating at these frequencies in pure CMOS processes is a big challenge. Selecting the correct transfer function for such a filter is an important task. We decided to use a 0.05° equiripple linear phase transfer function. Analyzing a Chebyshev approximation of a magnitude function reveals certain advantages like the distribution of permitted magnitude error uniformly over the passband rather than letting it increase monotonically toward the corner of passband as in the maximally flat response. When considering the delay approximations similar advantages are offered if we develop a filter with an equiripple delay, rather than maximally flat (Bessel-Thomson) approximation. Fig. 3. Shows the performance we hope to obtain for a desired specific delay. As the figure illustrates we achieve some combination of smaller delay error and wider bandwidth.

![Fig.3. Equiripple delay versus Bessel-Thomson delay performance.](image-url)
B. Transfer Function of the Filter

A detailed mathematical analysis of the transfer function is given in literature [6] [10]. Analyzing the generic transfer function of a equiripple linear phase transfer function

\[ T_E(s) = \frac{E(0)}{E(s)} = \frac{a_0}{s^n + a_{n-1}s^{n-1} + \ldots + a_1s + a_0} \]  

(2.2)

we can form an expression for group delay. We can impose the condition that the group delay approximates a constant value with uniform error over the desired bandwidth. Unfortunately a closed form solution for the equiripple delay transfer function has not been found. Since constant group delay reflects as linear phase we can write the equation of phase as a linear function and assume a sinusoidal ripple for ease of analysis

\[ \theta(\omega) = -D_0\omega - \Delta\theta \sin(\omega T) \]  

(2.3)

The group delay is then given by

\[ D_E(\omega) = -\frac{d\theta}{d\omega} = D_0 + \Delta\theta \times \pi / 180^\circ \times T \times \cos(\omega T) \]  

(2.4)

Where we have converted \( \Delta\theta \) into radians. \( T \) is the period of the ripple; it is approximately equal to the constant delay bandwidth divided by \( n/2 \), \( n \) being the degree of the function \( T_E(s) \). To determine the polynomial \( T_E(s) \) differential equations can be employed. The phase of Eq. 2.2 has exactly \( n \) locations where the slope equals \( D_0 \) (some constant group delay). Table II gives the normalized transfer function for \( \Delta\theta =0.05^\circ \). The table shows the transfer function for a \( 4^{th} \) and a \( 7^{th} \) order filter.

**TABLE II**

Denominator of equiripple linear phase transfer function

<table>
<thead>
<tr>
<th>N</th>
<th>( E(s) ) for ( \Delta\theta =0.05^\circ )</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>( (s^2 + 1.4894s + 2.5170)(s^2 + 1.9294s + 1.1561) )</td>
</tr>
<tr>
<td>7</td>
<td>( (s + 0.8613)(s^2 + 1.1456s + 5.3703)\times )</td>
</tr>
<tr>
<td></td>
<td>( (s^2 + 1.5420s + 2.9514)(s^2 + 1.6850s + 1.3170) )</td>
</tr>
</tbody>
</table>
The delay error is given by the following equation

$$\Delta D = 2T\Delta \theta \times \frac{\pi}{180^\circ}$$  \hspace{1cm} (2.5)

It is twice the ripple width, and is independent of n. The delay error is, of course proportional to the phase error as indicated by Eq. (2.3) and (2.5). For $\Delta \theta = 0.05^\circ$, the error is $\Delta D \approx 0.015$. However, the bandwidth $\omega_c$ over which the delay error $\Delta D$ remains constant and stays within the design specifications increases with $n$.

Based on the above discussion, we decided to implement a 4th order filter rather than a 7th order. This decision is based on certain tradeoffs. Since the primary target of this design is to reach high frequencies in the range of 500-600MHz, hence the number of poles plays a very important role. The more the number of poles in the system the more difficult it becomes to attain the proper frequency response. Also, the restriction on Biquads increases as the order of the filter increases. The required cutoff frequency of a single Biquad is really high (in the order of GHz) in case of a 7th order filter. Although the Group Delay response becomes better with the increase in the order of the filter. The Delay error is also less in case of higher order filters. High frequency prompts us to choose a 4th order filter. As shown in Table II (normalized to 1rad/sec) the transfer function of the fourth order filter is

$$E(s) = \frac{k}{(s^2 + 1.4894s + 2.5170)(s^2 + 1.9294s + 1.1561)}$$  \hspace{1cm} (2.6)

The above transfer function is a normalized function. But it gives the location of the system poles when scaled to the desired filter cutoff frequency. The subject of our interest here, a high frequency low pass filter in pure CMOS technology will be affected by lot of parasitic capacitances and high frequency poles. While calculating the individual cutoff frequencies of the two Biquads we will be targeting the final filter cutoff frequency to be around 800MHz. We know that the given low pass Biquad transfer function is of the generic form [10]

$$T(s) = \frac{\omega_0^2}{s^2 + (\omega_0 / Q)s + \omega_0^2} = \frac{N(s)}{D(s)}$$  \hspace{1cm} (2.7)
Where $\omega_0^2$ is the cutoff frequency of the Biquad, Q is the quality factor, $N(s)$ and $D(s)$ are the numerator and the denominator respectively. This Biquad transfer function can be realized by using transconductor cells, resistors and capacitors.

C. Building Blocks of the Filter

We can obtain some motivation for using transconductance-based circuits for our high-frequency active filters by recalling that individual transistors are fundamentally voltage to current converters characterized by their transconductance parameters. Here we can also compare the other options available for the implementation of the above transfer function. A widely employed practical solution uses switched-capacitor (SC) filters. The design of SC filters follows fundamentally the active-RC methods but avoids the use of resistors that are hard to implement accurately in CMOS technology. But these are low frequency circuits and the clock frequency also limits the use of very high frequencies in the range of Gigahertz. Opamp based filters are also low frequency applications as the small bandwidth of the opamps are a major hurdle. Hence the use of a $g_m$-C based filter is the optimum choice for such high frequency filter.

1. Two Integrator Loop

A Biquad transfer function can be implemented by a two-integrator loop. The basic elements in a two integrator loop being a lossy inverting integrator and a non-inverting integrator [10]. Fig 4. Shows the block diagram of a two-integrator loop with the non-idealities of the integrators included.
In the above block diagram the integrators are non-ideal where $\tau$ is the integrator time constant, normally an RC product and $q$ is the error caused by non-ideal opamps. As seen in [10], $q$ can be positive or negative, and usually is inversely proportional to the opamp gain at the frequency of interest. The above transfer function inspires us to look for an implementation of lossy and loss less integrator.

The basic component of the $g_m$-C based filter is an integrator. The fundamental circuit is obtained by loading a transconductor by an impedance $Z(s)$ as shown in Fig.5.
The circuit realizes the transfer function

\[
V_2 = g_m Z(s)(V_1^+ - V_1^-) = \frac{g_m}{Y(s)}(V_1^+ - V_1^-)
\]  

(2.8)

If we use a load capacitor and also consider non-idealities of output parasitic capacitance \(C_0\) and finite output impedance \(r_o = 1/g_o\), which appears in parallel with the integrating capacitor \(C\) the voltage gain becomes,

\[
\frac{V_2}{V_1} = \frac{g_m}{s(C + C_o) + g_o}
\]  

(2.9)

It follows that in a real \(g_m\)-\(C\) integrator the integration capacitor is increased to \(C + C_o\) by the parasitic output capacitance of the \(g_m\) cell. Also the integrator is lossy; it has a finite DC gain, \(g_m/g_o = g_m r_o\), with the 3-dB frequency equal to \(\omega_i = g_o / (C + C_o)\). We see here a reason for wishing to have as large output impedance as possible in a transconductor. Also, we note that the output parasitic capacitance \(C_o\) may not be negligible and should be accounted for in an integrator design when, as we shall see, for high frequency filters the integrating capacitors \(C\) becomes very small. Their values can be as low as 1pF or even less. Since the whole filter will be synthesized with Biquads, which are based on two integrator loops, one of which must be lossy, we need to realize a lossy integrator.

2. Lossy Integrator

If we wish to make a \(g_m\)-\(C\) integrator lossy on purpose, we need only to connect a resistor in parallel with the capacitor \(C\). A resistor can be implemented easily with another transconductor by connecting it in negative feedback. Fig. 6. shows the circuit of a lossy integrator.
When we include all the parasitic for this architecture, which includes $2C_o$ (output parasitic capacitances) and $2g_o$ from the two transconductors, as well as one $C_i$ (input parasitic capacitance) from $g_{m2}$. Hence the overall transfer function is given by

$$\frac{V_2}{V_1} = -\frac{g_{m1}}{s(C + 2C_o + C_i) + g_{m2} + 2g_o}$$

(2.10)

3. Realization of a Biquad

When we start assembling the building blocks to make a second order Biquad we start from a passive RLC circuit and then do a source transformation to get the circuit in Fig.7. As we can see in Fig. 7 it a single ended representation of the given second order transfer function; $g_{m1}$ converts the input voltage to a current, $g_{m2}$ represents the resistor R and $g_{m3}$ and $g_{m4}$ form a gyrator which together with the capacitor $C_2$ implements the inductor. The value of this inductor is given by

$$L = \frac{C_2}{(g_{m3} g_{m4})}$$

(2.11)
We can easily write the transfer function for the above Biquad in terms of the components involved. This transfer function can then be compared to the normalized transfer function given in Table II of the two Biquads. The transfer function for the above Biquad at the terminal $V_2$ gives us a Band pass response given by

$$
\frac{V_2}{V_1} = -\frac{g_{m1}}{g_{m2} + sC_1 + \frac{g_{m3}g_{m4}}{sC_2}} = -\frac{sC_2 g_{m1}}{s^2C_1 C_2 + sC_2 g_{m2} + g_{m3} g_{m4}}
$$

(2.12)

and at the terminal $V_0$ we have a lowpass response given by

$$
\frac{V_0}{V_1} = \frac{sC_2 V_2}{sC_1} = \frac{g_{m3} g_{m4}}{s^2C_1 C_2 + sC_2 g_{m2} + g_{m3} g_{m4}}
$$

(2.13)

This is the transfer function we are interested in. We will be investigating it further, by considering the effect of the parasitic on the above transfer function. $C_i$ is in parallel with the output parasitic capacitors $3C_o$ of three gm cells, two input parasitic capacitors $2C_i$ and loaded with the output impedance $3g_o$ of three gm cells. And the capacitor $C_2$ is in parallel with $g_o$, $C_o$ and $C_i$. Thus to include their effects we must replace in Eq. (2.12) and (2.13) the capacitive admittances $sC_1$ and $sC_2$ as follows

$$
sC_1 \rightarrow s(C_1 + 3C_o + 2C_i) + 3g_o = sC_{1eff} + 3g_o
$$

$$
sC_2 \rightarrow s(C_2 + C_o + C_i) + g_o = sC_{2eff} + g_o
$$

(2.14)

Inserting this modification into Eq.(2.13) results in

$$
\frac{V_o}{V_1} = \frac{g_{m3} g_{m4}}{s^2C_{1eff} C_{2eff} + s[C_{2eff} (g_{m2} + 3g_o) + C_{1eff} g_o] + g_{m3} g_{m4} + g_{m2} g_o + 3g_o^2}
$$

(2.15)
When the parasitic capacitances have been accounted for, all the transfer function
coefficients change; hence the poles and zeroes of the system are also altered. Whether \( g_o \)
should be considered in the design depends on the ratio of the output conductances to the
transconductance, \( g_o/g_m \) but \( C_o \) and \( C_i \) should always be included because circuit
 capacitance will normally be in the low Picofarad range. As we are already aware that
the above transfer function is equivalent to the Eq. (2.7). This helps us in calculating the
cutoff frequency \( \omega_0 \) and the quality factor \( Q \) of the individual Biquads in the fourth order
linear phase filter. Comparing Eq. (2.7) and Eq. (2.12) we obtain

\[
\omega_0^2 = \frac{g_{m1}g_{m4}}{C_1C_2}
\]

\[
K = \frac{g_{m1}}{g_{m4}}
\]

\[
Q = \frac{g_{m1}C_1}{g_{m2}C_2}
\]

(2.16)

Here \( K \) is the DC gain. For the simplicity of design and mathematical calculations we
make the value of \( g_{m1}, g_{m3} \) and \( g_{m4} \) same and equal to \( g_{m1} \). This will set the DC gain of the
Biquad equal to 1 and will simplify the equation for \( \omega_0 \) and \( Q \). Also let us assume that the
value of \( C_1 \) and \( C_2 \) are same. The equations simplify to

\[
\omega_0 = \frac{g_{m1}}{C_1}
\]

\[
K = 1
\]

\[
Q = \frac{g_{m1}}{g_{m2}}
\]

(2.17)

Now we pick up the normalized values of \( \omega_0 \) and \( Q \) from Table II; denormalize them to
an overall cutoff frequency of 800MHz for the overall filter and perform the
mathematical calculations using Eq.(2.17). Also here we assume the value of \( C_1 \) to be
1pF. The actual value of the load capacitors will be adjusted later in the design when we
evaluate the value of parasitic capacitances of the transconductors. We obtain the
following Table III for the value of transconductance and \( g_{m2} \) for the individual Biquads.
TABLE III
Values of transconductances and capacitors to be implemented

<table>
<thead>
<tr>
<th></th>
<th>$\omega_0$</th>
<th>$Q$</th>
<th>$g_{m1}$</th>
<th>$C$</th>
<th>$g_{m2}=I/R_{Q2}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Biquad 1</td>
<td>1.0752</td>
<td>0.5573</td>
<td>5.404 mS</td>
<td>1 pF</td>
<td>9.6977 mS</td>
</tr>
<tr>
<td>Biquad 2</td>
<td>1.5865</td>
<td>1.0652</td>
<td>5.404 mS</td>
<td>677.7 fF</td>
<td>5.0732 mS</td>
</tr>
</tbody>
</table>

The above table gives a clear indication of the design specifications that needs to be implemented for the fourth-order equiripple linear phase filter. As shown in the table above we will be using the same $g_m$ cell in both the Biquads, hence the value $C_2$ of the load capacitor has been calculated to incorporate this design simplicity. Also the parasitic capacitance of each $g_m$ cell will be evaluated later and the values of the load capacitor will changed to get the required response. A fully differential version of the Biquad has been shown in Fig.8.

![Fully Differential Biquad](image)

**Fig.8.** Fully differential Biquad with common-mode feedback circuit.

4. **Fully Differential Implementation**

In analog/mixed signal processing, fully differential structures are often being used due to their better dynamic range over single-ended structures. This is due to the properties of
any differential structure, namely, better common-mode noise rejection, better distortion performance and increased output voltage swing. For applications of lower power supply voltage and high speed, OTA architectures must generate large fully-differential transconductances for the implementation of filter poles. Fig.8. also shows the presence of Common-mode feedback (CMFB) circuits, which are an essential part of any Fully-differential circuit. Owing to the high output impedance at the output of the OTA’s the common-mode might hit the rails due to process variations. The CMFB circuit fixes the common-mode level at the output terminals of the integrators to a desired reference level and thus and we can extract meaningful signal at the output. The complexities and different schemes to implement the CMFB circuit will be discussed in later chapters. Fig.9 shows the complete circuit of the linear phase filter with both the Biquads.

Fig.9. Fully differential fourth-order equiripple linear phase filter.
CHAPTER III
DESIGN OF SUITABLE OTA

A. Design Considerations for High Frequency Applications

There are certain design rules that should be followed while designing the integrator. The OTA non-idealities affect the filter performance. The parasitic capacitors produces deviation of the -3dB frequency in the lowpass filter, while the finite output impedance affects the quality factor Q of the filter. The parasitic poles also introduce excess phase affecting the Q as well. As mentioned earlier for the high frequency applications we use small capacitors, hence the effect of parasitic capacitances become prominent. Since the junction capacitors are non-linear hence they contribute towards additional harmonic distortion [11].

1. Effect of the Parasitic Capacitor

The load capacitor in Fig 8 has three main components: the designed poly capacitor, the parasitic capacitance associated with the fabricated poly capacitor and the non-linear junction capacitors. Now let’s initially analyze the effect of only the junction capacitance contributed by the all the \( g_m \) cells at both the lowpass and the bandpass node in Fig.8. Let’s assume that the parasitic junction capacitances are included in \( C_L \). The basic equations yield the following expression for load capacitor [11]

\[
C_{\text{total}} = C_L + \frac{C_{j0}}{1 + \frac{v_0}{V_{\text{DB}}} \phi_F}
\]

(3.1)

where \( C_{j0} \) is the zero bias junction capacitor and \( V_{\text{DB}} \) (\( = V_{\text{DB}+2\phi_F} \)) is the effective junction bias voltage. \( v_0 \) is the ac voltage across the capacitor. If we consider an integrator, the OTA output current is given by \( g_mv_{\text{in}} \). Equating the injected charge
(integral of the OTA output current) with $c_{total v_0}$, and expanding the result expression it can be shown that the third order harmonic distortion can be approximated as follows.

$$HD_3 \equiv \frac{3}{32} \frac{C_L C_{j0}}{(C_L + C_{j0})^2} \left( \frac{g_m}{C_L + C_{j0}} \right)^2 \left( \frac{V_{in}}{V_{DB}'} \right)^2$$  \hspace{1cm} (3.2)

where $\omega_0$ is the frequency of the input signal, very close to $g_m/(C_L+C_{j0})$. Typical values for $V_{DB}'$ are in the range of 1-1.5 volts. For $V_{in}=200$ mV, HD3 can be as large as

$$HD_3 \leq \frac{1}{250} \frac{C_L C_{j0}}{(C_L + C_{j0})^2}$$  \hspace{1cm} (3.3)

Now if we design such that $C_L > 3C_{j0}$, HD3 is below 0.1%. For high frequency design large transistor dimensions increase junction capacitance, hence it is not an easy task to reduce the third harmonic distortion.

2. Effect of Saturation Voltage ($V_{DSAT}$) on the OTA

We know that the third harmonic distortion is approximately given by the following expression [11]

$$HD_3 \equiv \frac{1}{32} \left( \frac{V_{in}}{V_{DSAT} - V_T} \right)^2$$  \hspace{1cm} (3.4)

where $V_{in}$ is the magnitude of the input signal. Certain tradeoff’s are involved when the appropriate value of $V_{DSAT}$ is chosen. Increasing the $V_{DSAT}$ increases the small signal transconductance as well as reduces the third harmonic distortion. But a large saturation voltage leads to mobility reduction effects. This effect can be observed in the following equation [11].

$$\mu_n = \left( \frac{\mu_0}{1 + \theta (V_{GS} - V_T)} \right) \left( \frac{1}{1 + \frac{\theta V_{in}}{1 + \theta (V_{GS} - V_T)}} \right)$$  \hspace{1cm} (3.5)
where $\theta$ is a fitting parameter, which is dependent on technology. The mobility degradation puts a limit on the saturation voltage. Larger theta values in mobility degradation equation leads to more harmonic components.

3. Effect of Non-dominant Poles

Another important factor to be considered while choosing the OTA architecture for the filter is the effect of non-dominant poles. For these applications the OTA architecture chosen should be preferable a single stage with enough gain and a gain bandwidth product. In order to increase the DC gain we can use a folded-cascode or a telescopic architecture, but it includes at least one non-dominant high frequency pole. This high frequency pole limits the frequency response of the OTA. In this case the small signal transconductance is given by

$$g_m \equiv \frac{g_{m0}}{1 + \frac{s}{\omega_p}}$$  \hspace{1cm} (3.6)

where $g_{m0}$ and $\omega_p$ are the dc transconductance and the high frequency pole. For high frequency filters these non-dominant poles introduce negative excess phase on the original transconductor transfer function. To place these non-dominant poles to really high frequencies with the current CMOS technologies is a difficult task.

4. Possible OTA Implementations

Design considerations of the filter and the requirements from the transconductor lead to a very strict requirement on a high speed OTA. The OTA required should have the minimum parasitic as higher parasitic will reduce the bandwidth of the filter. It should be able to generate large $g_m$, it’s linearity should be good and should have good power supply rejection. All the specifications lead to the use of single stage fully differential OTA. Some of the possible OTA architectures like the Folded-cascode, telescopic or the
two-current mirror architecture suffer from the non-dominant pole problem. Fig. 10 shows these architectures.

Fig. 10. Folded-cascode and two current mirror OTA.

All these architectures provide us with a limited linearity, high gain and good noise rejection but they are not very suitable for high frequency design as the non-dominant pole degrades the performance of the system. Also these architectures have a single input stage and hence the $g_m$ is not very large. Though we can employ schemes to improve the $g_m$ but reducing the parasitic is a daunting task. Hence we turn our attention to certain other OTA architectures. Fig.11. represents two architectures that can be employed for high frequency design.
The above OTA are used for high frequency filter design. The first one being current mode OTA [12]. Current mode integrator has the advantage of absence of internal nodes. That means that there are no high frequency parasitic poles. This type of integrator involves a simple transistor as an integrator generating the required $g_m$. Apart from low voltage requirements this type of architecture improves the frequency response of the filter.

Nevertheless current mode filters suffer from many disadvantages. The most prominent being current conveying accuracy. The use of cascode structures to improve accuracy requires higher supply voltages. Furthermore introducing cascode structures introduces
internal nodes and hence parasitic poles. This degrades the frequency response of the system. If cascode structures are not used then these structures have low DC gain as the rout of the transistors is not that high. Also the linearity of the OTA is not very good. The absence of tail current reduces the Common-mode rejection. Also any noise on the supply voltages is directly transferred to the output signal. This again reduces the noise performance of the system.

Nauta’s architecture [13] shown in Fig 11. provides a better solution for high frequency design. It involves only the use of analog inverters. In the above integrator only six inverters are used. It’s simpler to design and also the absence of internal nodes improves the frequency response of the system. This architecture can extend the OTA response to really higher frequency and the parasitic poles appears at GHz.

But this architecture suffers from similar problems as the current mode application. In these structures the DC gain is dependent on the output impedance of a single transistor which is normally very low hence low DC gain. In Nauta’s architecture the output of the inverter is loaded with a negative resistance to increase the output impedance. This effectively increases the DC gain, but this scheme is not very accurate as it is really difficult to do the cancellation. Also the common-mode control requires a elaborate arrangement of the inverters. Also the distortion performance of this kind of architecture is affected a great deal due to mobility degradation. The noise performance is again not very satisfactory due to noise being injected directly to the output through supply voltages. But the most formidable task in using this type of architecture is the design of a very good tuning scheme to control VDD’. This requires the implementation of a very good buffer.
B. OTA Architecture

The OTA architecture used for this filter is shown in Fig. 12. This architecture is based on linearized complementary differential pairs [9]. This architecture presents several advantages, the main advantage of this being a single stage OTA. The above architecture has a complementary input with the signal being fed to both the N-type and the P-type transistor. This helps in generating a larger transconductance from the OTA thus increasing the power efficiency. This is a single pole OTA with the pole occurring at the output. Hence due to the absence of non-dominant poles the frequency response of the OTA is good. Transistors M5 and M6 are used to provide the bias current, and the same bias current IB is fed to both the differential pairs.

![OTA architecture diagram](image-url)

Fig. 12. OTA architecture.
1. Linearization Techniques

The transistors M3 and M4 used in the OTA (shown in Fig.12) are used for linearization of the OTA. The technique used in this OTA is called source degeneration. In general there are three different techniques used to linearize the OTA (a) attenuation, (b) non-linear terms cancellation and (c) source degeneration [14]. The non-linearities of the OTA stem from the use of MOS transistors, which are non-linear devices. The attenuation techniques utilize the fact that the input voltage can be reduced or attenuated by say some factor k. This attenuation yields a linear approximation for the output current and thus linearizing the OTA. But attenuation technique requires an increase in transconductance gain to compensate for attenuation, thus resulting in high power consumption and silicon area. The other technique for linearization involves certain architectures where the non-linear terms are cancelled by means of optimal algebraic sum of non-linear terms [15] [16]. However source degeneration technique is mostly employed for linearization because the above technique requires a good cancellation of non-linear terms which is difficult to achieve. Fig.13 illustrates two possible implementations.

Fig.13 a & b. $g_m$ linearization schemes using source degeneration.
Although both the topologies result in the same transconductance, they present different properties. Fig. 13b is the source degeneration technique that has been used in our OTA. The most important advantage of the architecture in Fig. 13b is higher common mode swing of the input signals as compared to Fig. 13a. The voltage drop at the resistors of Fig. 13a reduces the common-mode swing of the input signal. Also in Fig. 13a the noise contribution of the current sink is divided into both branches and appears at output as common-mode noise. While in Fig. 13b most of the noise of each current sink is injected to a single output and thus appearing as differential noise current.

2. Effective $g_m$ of the OTA employed

The relationship between output current and input voltage in an OTA is dependent upon input voltage, temperature, operating point and process variations. The OTA large signal transconductance is a non-linear function, the OTA output current can be expanded by

$$i_o = I_{DC} + \left[ \frac{\partial i_o}{\partial v_{in}} \right]_Q v_{in} + \frac{1}{2} \left[ \frac{\partial^2 i_o}{\partial v_{in}^2} \right]_Q v_{in}^2 + \frac{1}{6} \left[ \frac{\partial^3 i_o}{\partial v_{in}^3} \right]_Q v_{in}^3 \ldots \ldots \ldots \ldots (3.7)$$

Here the first term represents the output DC current of the OTA. The coefficients of $v_{in}$ represent the small signal transconductance of the OTA, and is denoted by $g_m$. If a single sinusoidal input signal is considered then the equation of output current becomes.

$$i_o = I_{DC} + \frac{1}{2} \left[ \frac{\partial^2 i_o}{\partial v_{in}^2} \right]_Q V^2 + \frac{1}{6} \left[ \frac{\partial^3 i_o}{\partial v_{in}^3} \right]_Q V^3 + \ldots \right]_Q V \sin(\omega t) +$$

$$\left[ - \frac{\partial^2 i_o}{\partial v_{in}^2} \right]_Q V^2 \sin(2\omega t) + \left[ - \frac{\partial^3 i_o}{\partial v_{in}^3} \right]_Q V^3 \sin(3\omega t) + \ldots \right.$$$$

The above equation can be used to find out the HD2 or the HD3 expressions for second and third harmonic distortions.

If we consider an ideal quadratic law for the transistors we can write the equation of output current in a much simpler manner, by using the parameters employed in circuit
design. The single side output current of the source degenerated structures shown in Fig.13a is given by [15]

$$i_o = IB \pm \left( \sqrt{\frac{2\mu_C I_B W_n}{L_n}} (1 + N) \right) v_{id} \times \sqrt{1 - \left( \frac{v_{id}}{2(1 + N)V_{DSAT}} \right)^2} \tag{3.9}$$

where $v_{id}$ is the differential input voltage, $I_B$ and $V_{DSAT}$ the bias current and the saturation voltage. The factor $N$ is the source degeneration factor where $N = g_m R$. From the above equation, the small signal transconductance and the third harmonic distortion can be found. Since the OTA architecture used (shown in Fig.12) has two complementary input pair hence the output current equation will have two components. One from the N-type input pair and the other from P-type input pair. Hence Eq.3.9 can be modified for the Fig.12 architecture to yield OTA output current as

$$i_o = g_{mn} \left( \frac{v_{id}}{1 + N_N} \right) \left[ 1 - \left( \frac{v_{id}}{2(1 + N_N)V_{DSATN}} \right)^2 \right] + g_{mp} \left( \frac{v_{id}}{1 + N_P} \right) \left[ 1 - \left( \frac{v_{id}}{2(1 + N_P)V_{DSATP}} \right)^2 \right] \tag{3.10}$$

where $g_{mn}$ and $g_{mp}$ are the transconductance of the n-type and p-type differential pair respectively; and $V_{DSATN}$ and $V_{DSATP}$ are the saturation voltages of the complementary input pair. $N_N$ and $N_P$ are the source degeneration factors given by [16]

$$N_N \equiv 2 \frac{g_{mn}}{\mu_n C_ ox \frac{W_3}{L_3} (V_{GS3} - V_{T3})}, \quad N_P \equiv 2 \frac{g_{mp}}{\mu_p C_ ox \frac{W_4}{L_4} (V_{GS4} - V_{T4})} \tag{3.11}$$

Eq.3.11 effectively shows the value of $N_N = g_{mn} R_3$ and $N_P = g_{mp} R_4$ where $R_3$ and $R_4$ are the source degeneration transistors for the N-type and P-type transistors. Eq.3.10 helps us in finding out the effective small signal transconductance [9] which is given by

$$G_m = \left[ \frac{\partial i}{\partial v} \right] = \frac{g_{mn}}{1 + N_N} + \frac{g_{mp}}{1 + N_P} \tag{3.12}$$

The OTA employed for the design is a fully differential OTA and it has the inherent property of eliminating the even-order harmonic components. Hence the total harmonic
distortion (THD) is dominated by the third order harmonic distortion (HD3). The third order harmonic distortion [9] is given by

\[
\text{HD3} = \frac{1}{32} \left( \frac{1}{1 + N_N} \right)^2 \left( \frac{V_{id}}{V_{DSATN}} \right)^2 d_1 + \frac{1}{32} \left( \frac{1}{1 + N_P} \right)^2 \left( \frac{V_{id}}{V_{DSATP}} \right)^2 d_2
\]

(3.13)

Where \( d_1 \) and \( d_2 \) are given by

\[
d_1 = \frac{g_{mn}(N_P + 1)}{g_{mn}(N_P + 1) + g_{mp}(N_N + 1)}
\]

\[
d_2 = \frac{g_{mp}(N_N + 1)}{g_{mn}(N_P + 1) + g_{mp}(N_N + 1)}
\]

(3.14)

Above equations gives us an insight into the OTA design. From the above equations we can determine where the chosen architecture meets the specification.

C. Design Specifications and Considerations for the OTA

The above architecture provides us with certain advantages as compared to the other OTA architectures. This OTA has the inherent property of providing the common-mode information. The common-mode information can be extracted either from the source of N-type or P-type input differential. We will observe later that in the Biquad the subsequent OTA will provide the output common-mode information of the previous OTA and this information will be utilized in the common-mode feedback circuit.

1. Minimum Requirements from the OTA

As discussed in Chapter II the OTA need to have a gm of at least 5.4mA/V with a 1 pF load capacitor. This does not consider the parasitic capacitance that will be loading the OTA in the Biquad. A minimum set of specifications for the OTA are shown in Table IV Since the target bandwidth for the overall filter is greater than 500Mhz it is desired that the OTA should not limit the required bandwidth. A Gain Bandwidth of 1GHz or higher for the OTA with 1pF load is desired as parasitics will increase the capacitive load once
the integrators are cascaded. Also the Gain of about 30dB is sufficient to overcome the gain error when the OTA operates in closed loop. These OTA restrictions encourages us to choose a technology that provides us with minimum amount of parasitic and which allows us to fabricate smaller transistors. As a result TSMC 0.35u technology was chosen over AMI 0.5u technology. An ever better technology of TSMC 0.25u or 0.18u would have allowed a better performance but would have increased the silicon cost. Also the supply voltages chosen for the above design is ±1.65V as some head room is required for this kind of architecture. This supply voltage will also relax the tight specification on the output swing.

Table IV
OTA specifications

<table>
<thead>
<tr>
<th>OTA Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>( G_m )</td>
<td>≥ 5.404 mS</td>
</tr>
<tr>
<td>GBW</td>
<td>≥ 1 GHz</td>
</tr>
<tr>
<td>Excess Phase</td>
<td>≤ 5° up to 1GHz</td>
</tr>
<tr>
<td>DC Gain</td>
<td>≥ 20dB</td>
</tr>
<tr>
<td>Output Swing</td>
<td>≥ 250mV peak to peak</td>
</tr>
</tbody>
</table>

Fig.12 uses two current sources, M5 is N-type current source and M6 is P-type current source. The bias voltage for the above current source has been generated through a separate bias circuit. An effort has been made to keep the \( V_{DSAT} \) less than 400mV. Good current sources require good matching and large lengths for better mirroring of current. The layout was done carefully to accommodate this design concept. But large lengths increase the device sizes and large devices increase the parasitic. Hence we have ensured that differential pair uses minimum length to reduce the parasitic. As the main design
target is to achieve highest possible speed, hence a better matching has been traded-off with speed in this design.

High speed OTA’s need a large current to increase the GBW. Since GBW is given by the ratio of $g_m/C_L$, where $C_L$ is load capacitor, the ratio can be maximized with minimum parasitic and larger $g_m$. Gm of a device is given by the following expression

$$g_m = \sqrt{\frac{2\mu C_{ox} W}{L} I_B}$$

Large $g_m$ needs a large current and a large aspect ratio of the transistor. But as discussed large aspect ratio generates more parasitics hence a better way to generate large $g_m$ is large currents. In this design current of 1.4mA has been used. This proved to be good value for the current, as increasing the current was not generating a significant increase in the GBW.

2. Small Signal Model of the OTA

Looking at the signal path shown in Fig. 14 reveals that the parasitic capacitances at the input pair dominate the frequency response of the OTA. Hence the length’s of the input pair has been kept minimum possible as allowed by the technology. Fig 14. below shows the signal path and the parasitics in the OTA.
Above figure gives us a clear representation of the parasitic capacitances in the signal path. $C_{GDN}$ and $C_{GDP}$ are the main parasitic capacitors in the signal path. These parasitics will degrade the frequency response of the OTA. These parasitics can be as large as 0.25 pF (or even larger depending on transistor size); hence they cannot be ignored. $C_{GSN}$ and $C_{GSP}$ are not in the signal path and also the source-drain and bulk-drain parasitic are grounded. An appropriate small signal model of the above architecture is given in Fig 15.
From the signal model we can derive the transfer function and the various design equations. We know that the DC gain of the OTA is given by the product of the effective Gm and the output impedance of the OTA. The output impedance of this OTA is the parallel combination of the impedance of the N-type and the P-type and is given by the following expression

\[ R_{out} \approx g_{mn} r_{on} R_N \parallel g_{mp} r_{op} R_P \]  

(3.16)

where \( r_{on} \) and \( r_{op} \) are output impedance of the input differential pair and \( R_N \) and \( R_P \) are the on resistance of the source degeneration transistors. From Eq.3.12 and Eq.3.16 we can write the expression for DC gain of the OTA

\[ A_{vo} = G_m R_{out} \approx \left( g_{mn} \frac{1}{1 + N_N} + g_{mp} \frac{1}{1 + N_P} \right) g_{mn} r_{on} R_N \parallel g_{mp} r_{op} R_P \]  

(3.17)

Also from Fig.12 we know that the output swing is limited. A boundary condition on the output swing is given by

\[ V_{IN} - V_{TN} \leq V_{OUT} \leq V_{IN} - V_{TP} \]  

(3.18)

The above condition sets a limit on the swing of the signal.

An important design consideration is the effective value of the \( g_m \). As we know that for the same current flowing through the N-type and P-type input pair and same transistor sizes, the overall Gm will be dominated by the gm of the N-type transistor. This is because of the mobility factor of the N-type transistor, which is approximately three times that of P-type. The Gain Bandwidth Product of the OTA is given by

\[ GBW = \left( g_{mn} \frac{1}{1 + N_N} + g_{mp} \frac{1}{1 + N_P} \right) \frac{1}{C_{parasitic} + C_{Load}} \]  

(3.19)

Also ideally this a single stage OTA the non-dominant pole appears at very high frequencies. Hence the phase margin of this OTA exhibits the property of an almost ideal integrator, and the phase margin is 90°. Using the all region one equation model the Aspect ratio of the transistors in the design can be determined. In this design, driver transistors are operating in the moderate inversion and all the current mirrors are operate in strong inversion. So inversion level can be chosen as \( i_f = 10 \) for input pair and \( i_f = 100 \)
for all other transistors. For the architecture shown in Fig.12, Iss can be determined by the equation below,

$$I_{SS} = n \phi g_m (1 + \sqrt{1 + i f M})$$  \hspace{1cm} (3.20)

where $\phi \approx 25.8$ mV, $n = 1.3$

$$\frac{W}{L} = \frac{G_m}{2 K_p \sqrt{\frac{I_{SS}}{2 \phi g_m n} - 1}}$$  \hspace{1cm} (3.21)

Select $i_f = 100$ for all other transistors, the sizes of the transistors can be obtained with the equation below

$$\frac{W}{L} = \frac{2 I}{i_f n K_p \phi f}$$  \hspace{1cm} (3.22)

Here $I = I_{SS}/2$

All the above equations help us in determining the aspect ratio of the transistors and they are shown in Table V.

<table>
<thead>
<tr>
<th>Transistor</th>
<th>Aspect Ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>Win $\mu$m</td>
<td>L in $\mu$m</td>
</tr>
<tr>
<td>MN</td>
<td>16*11</td>
</tr>
<tr>
<td>MP</td>
<td>20*11</td>
</tr>
<tr>
<td>M3</td>
<td>6*6</td>
</tr>
<tr>
<td>M4</td>
<td>10*15</td>
</tr>
<tr>
<td>M5</td>
<td>16*11</td>
</tr>
<tr>
<td>M6</td>
<td>16*12</td>
</tr>
</tbody>
</table>
D. Simulation Results of the OTA

Fig. 16. Frequency response of the OTA.

For the frequency response of the OTA we simulated it with a capacitive load and without the CMFB circuit. The DC offset at the output of the OTA was as low as 18mV hence the CMFB circuit was avoided. As is evident from the result (shown in Fig. 16) above the high frequency response of the OTA shows us the GBW at 1.069 GHz. This measurement was taken with a load of 1 pF at the output. We will adjust the value of load capacitor in the Biquad so that accumulated loading of load capacitor and parasitic capacitor is close to the proper value. Also it is evident that the non-dominant pole is at higher frequency. However the zero in the system because of the $C_{GD}$ capacitance between input and output is visible at around 5 Ghz. This zero plays an important role when we work at higher frequencies and cannot be neglected.
Fig. 17. DC response of the OTA.

Fig. 18. Variation of effective $G_m$ with the input.
The DC response of the OTA (shown in Fig.17) was measured with a DC sweep of the differential input. The $G_m$ variation (shown in Fig.18) simulation was made with a voltage source at the output whose value was set equal to the OTA DC offset. Then the DC sweep was done on the common-mode voltage source. The $G_m$ of the filter is pretty flat and is the sum of both N-type and P-type differential pair. The DC transconductance of the integrator is very much constant for up to a common mode variation of $\pm 300$ mV. An AC simulation (shown in Fig.19) reveals that the value of $G_m$ is constant for almost up to 1 GHz.

![Variation of the $G_m$ of OTA with frequency](image)

Fig.19 Variation of the $G_m$ with frequency.
Another important error is the transconductor’s excess phase (shown in Fig.20) due to OTA parasitic. Due to the non-ideal transfer function of the $G_m$, i.e. the presence of non-dominant poles and zeroes, the excess phase of the filter can approximated as a pure delay or a pure advance. Let’s call this delay or advance as $\tau_p$. If some mathematical analysis is done [5], then it can be proven that the filter poles and zeroes are shifted by an amount proportional to their absolute magnitudes squared multiplied by $\tau_p$. This can be a potentially hazardous situation for stability in case if any pole moves to right half plane. In this design care has been taken to reduce the excess phase and the excess phase is only 1.8° up to 1 GHz. A Table of the simulation results from the OTA has been shown below in table VI.
TABLE VI
Summary of OTA results

<table>
<thead>
<tr>
<th>OTA Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>$G_m$</td>
<td>9.606 mS</td>
</tr>
<tr>
<td>GBW</td>
<td>1.069 GHz</td>
</tr>
<tr>
<td>Excess Phase</td>
<td>1.8° at 1GHz</td>
</tr>
<tr>
<td>DC Gain</td>
<td>28 dB</td>
</tr>
<tr>
<td>Output Swing</td>
<td>400mV</td>
</tr>
</tbody>
</table>
CHAPTER IV
DESIGN OF COMMON MODE FEEDBACK CIRCUIT

A. Design Considerations for Common-Mode Feedback Circuit

Fully differential circuits have many advantages over their single ended counterparts. The main being larger output swings, avoiding mirror poles (minimizing parasitics) and thus achieving higher closed loop speed. Also the distortion is lower in these circuits. But fully differential circuits require Common-Mode Feedback circuits. Typically, when using fully differential OTA’s in feedback applications, the applied feedback is applicable to the differential signals, but does not affect the common-mode signal. It is therefore necessary to add additional circuitry to determine the output common-mode voltage and to control it to be equal to some specified voltage, usually about halfway between the power supply voltages. This circuitry is referred as the common-mode feedback (CMFB) circuitry. It is often the most difficult part of the OTA to design.

1. Why Common-Mode Control is Needed

The common-mode level at the output is important for the proper functioning of OTA. In case of fully differential circuit and also in our OTA we need a P-type current source to balance the N-type current source [17]. This situation is shown in Fig.21. The difference between IP and IN must flow through the intrinsic output impedance of the amplifier, creating an output voltage change of \( (I_P - I_N) (R_P \parallel R_N) \). Since this current error depends on the mismatches and \( R_P \parallel R_N \) is high, the voltage error maybe very large. This might drive the P-type or the N-type current source out of saturation. The output nodes of the amplifiers are very high impedance nodes, hence even a small current mismatch or process variation might make the output common-mode level to hit the rails.
The CMFB circuitry in general consists of a sensing circuit and an amplifier. The sensing circuit senses the common-mode information at the output of the OTA, and the amplifier is used to compare the output common-mode level with a reference voltage $V_{\text{ref}}$ (usually a voltage between the supply voltages). The error between the two is compared and amplified by the amplifier and an error signal is fed back to the OTA as an error control signal. This fixes the output common-mode level to the specified reference voltage $V_{\text{ref}}$.

2. Sensing and Amplification Circuit

A conceptual topology of the common-mode feedback circuit is shown in Fig.22. As discussed the task of CMFB has been divided into operations: sensing the output CM level, comparison with a reference $V_{\text{ref}}$, and returning the error to the amplifier’s bias network. The common-mode information at the output of the OTA can be extracted with the help of resistors. We recall that $V_{\text{out}_{\text{CM}}} = \frac{(V_{\text{out1}} + V_{\text{out2}})}{2}$, where $V_{\text{out1}}$ and $V_{\text{out2}}$ are the single ended output.

Fig.21. Simplified model of high gain amplifier.
Fig. 22. Conceptual topology for common-mode feedback.

Strictly speaking the following requirements must be met by Common-Mode Feedback loop [18].

(i) The DC gain of the CMFB loop must be large enough to keep an accurate control of the CM component. If the DC gain is very low then an asymmetrical swing occurs which result in the loss of Dynamic range.

(ii) The Gain Bandwidth Product of the CMFB loop (\( \text{GBW}_{\text{CM}} \)) should be at least equal to the gain-bandwidth product of the differential-mode loop (\( \text{GBW}_{\text{DM}} \)). If \( \text{GBW}_{\text{CM}} < \text{GBW}_{\text{DM}} \) the system does not perform as a fully balanced system in the range of frequencies comprised between \( \text{GBW}_{\text{CM}} \) and \( \text{GBW}_{\text{DM}} \). Henceforth common mode signals are not attenuated by CMFB.

(iii) The CMFB loop should act over CM voltage signal only, and should not affect the DM signals, otherwise harmonic distortion components due to CMFB loop are induced in the signal. In practice, differential mode linearity is one of the main constraints especially in low voltage CMFB.

The sensing circuit for our OTA is inherently embedded in the OTA architecture. However the OTA common-mode level at the output is not available directly. The information available is after a source follower stage. Hence the common-mode information available is \( V_{\text{out}} - V_{\text{GS}} \). We will be avoiding some extra circuitry for sensing by
sensing the common-mode information at the subsequent OTA i.e. the OTA following the integrator will be sensing the Common-mode information. A clear picture of common mode sensing is available in Fig.23.

As shown in Fig.23 we have the common-mode information at the node $v_{cm}$. But we have to watch carefully the effect of a parasitic pole because of the parasitic capacitor $C_{p1}$. In the actual scheme we have MOSFET resistors instead of passive resistors. Since resistance of the MOSFET transistor in triode region is dependent on $V_{GS}$ and the size of the transistor. An accurate common-mode can be obtained if the value of both resistors is same which can be achieved by closely matching the MOSFET’s. A full implementation of CMFB circuit is shown in the next section utilizing the above sensing circuit.

B. Possible Implementation of CMFB Circuit

In a Biquad we have at least four OTA’s and an ideal situation would be to have at CMFB circuits for all the OTA’s. But this not only increases a lot of extra circuitry to the whole system but adds up a lot of feedback loops to the system. Multiple loops in a Biquad are not a good sign for the stability of the system. We need to minimize the number of loops for operations at high frequencies. Also the individual parasitic poles in
the common-mode loop might cause stability problems and we might suffer from common-mode oscillations.

1. A Simple CMFB Circuit

One of the possible solutions for our system is shown in the Fig.24.

![Fig.24. Typical common-mode feedback scheme.](image)

We initially designed the above common-mode feedback circuit for our circuit. It is a typical scheme for Common-mode feedback and is discussed in [9,10]. To analyze the above circuit we can break the loop open at Vcm. The open loop transfer function of the Common-mode loop is given by [9]

\[
\frac{V_{cm}'}{V_{cm}} = \frac{g_{mMp}}{g_o} \cdot \frac{1}{1 + s \frac{C_L}{g_o} \left( 1 + s \frac{C_{p2}}{g_{m5}} \right)}
\]  

(4.1)

where \( g_{mMp} \) is the small-signal tranconductance of the transistor Mp. Although in the above transfer function another pole associated with \( C_{p1} \) is neglected, but further studies
will reveal that this parasitic pole affects the stability of the loop. We will discuss the
effect of this pole with some simulation results in the next section. The parasitic pole
associated with $C_{p3}$ can be neglected. Also in the above transfer function the value of $g_o$
will be generally low as the OTA is designed for high output impedance. Hence the value
of $g_o$ is smaller as compared to $g_{m5}$. From the above transfer function it can be easily
analyzed that the two most important poles of the system are given by

$$
\omega_{dom} = \frac{g_o}{C_L}, \quad \omega_{non-dom} = \frac{g_{m5}}{C_{p2}}
$$

Now in the above system $\omega_{dom}$ is the dominant pole of the loop and is located at the
output of the integrator. $\omega_{non-dom}$ is the non-dominant pole of the system. The Gain
Bandwidth product of the system is given by

$$
GBW_{CM} = A_o \omega_{dom} = \left( \frac{g_{mMp}}{g_o} \right) \left( \frac{g_o}{C_L} \right) = \frac{g_{mMp}}{C_L}
$$

The stability of the common-mode loop can only be ensured if the non-dominant pole of
the loop is located at higher frequency than the GBW of the loop. This condition can be
expressed as

$$
\frac{g_{m5}}{C_{p2}} > \frac{g_{mMp}}{C_L}
$$

The above condition is not easy to achieve. For high frequency design stability becomes
an important factor as it becomes really difficult to place this non-dominant pole at high
frequencies. It is evident from Fig.24. That $C_{p2}$ is dominated by the gate-source
capacitance of three transistors hence $C_{p2} \equiv 3C_{GS}$. Hence this non-dominant pole is not
located at a very high frequency. If we need the common-mode loop to operate really fast
we need to either eliminate this pole or push it to really high frequencies. Hence we
decided to explore another architecture where we can eliminate the pole $g_{m5}/C_{p2}$ and
hence increase the loop bandwidth.
2. A Current Feedback Based CMFB

As discussed in the previous section a high-speed common-mode loop is an important requirement for high frequency design. For Continuous time filter it is always difficult to design a really high speed Common-mode loop that is stable. Common Mode Oscillations are always an important issue for high frequency design. Common Mode oscillation induces unnecessary harmonic distortion components in the main signal. In this new scheme we will try to eliminate a low frequency non-dominant pole. We have used a class AB amplifier to eliminate a pole in the system. Fig.25 shows the scheme in more detail.

![Fig.25. The new current feedback CMFB.](image)

If observed closely, in the above scheme it can be noticed that the pole \( \frac{g_m}{C_{p2}} \) at node \( V_z \) in Fig.24 disappears. That was a non-dominant pole but it was the main non-dominant pole, which was degrading the frequency response. This scheme get rids of that pole, but the pole at \( V_y \) due to the parasitic capacitor \( C_{p3} \) becomes the main non-dominant pole. Parasitic at node \( V_y \) increases, other than the original parasitic capacitance \( C_{p3} \) there will
be some increment capacitor $\Delta C$ due to the drain of $M_p$ and the current source. But this $\Delta C$ will not be a big capacitor as it only coming from the drain. Hence on a frequency scale we can see the effect as shown in Fig.26. The effect of the parasitic pole at $V_{cm}$ also becomes important at this point because it is a high frequency pole, which is given by the expression

$$\omega_{V_{cm}} = \frac{g_{mM_p}}{C_{p1} + C_{GSMP}}$$

(4.5)

Fig.26. Movement of pole location.

If the size of $M_p$ is too big then the $C_{GSMP}$ will be pretty big and this pole will start dominating the frequency response of the common-mode loop. This effect has been discussed later with some simulation results. Also it is to be noticed that the transistor $M_p$ has been split into two parts. In case the output common-mode is equal to the reference no current flows in or out of first OTA into the class AB amplifier. However any difference between common-mode and reference will adjust the current flowing in first OTA and the error current will flow in the class AB amplifier. This will settle the common mode voltage equal to the reference voltage. Fig.27. shows how the copy of reference voltage ($V_{ref\_copy}$) has been generated.
C. Design Considerations for the New Common-Mode Scheme

The New common-mode scheme will be faster than the common-mode scheme described in Fig.24. as it has lesser number of poles. As discussed in the previous section there are primarily two non-dominant poles in the system. Fig.28. shows the effect of other parasitic capacitor effects.

![Diagram of Generation of Vref_copy](image1)

Fig.27. Generation of copy of reference voltage.

![Diagram of Parasitics in Class AB stage](image2)

Fig.28. Effect of other parasite and introduction of zero.
As is evident from the above Fig.28 a zero will also be introduced in the system because of the $C_{GS}$ capacitance at node $V_x$ of the class AB amplifier. Since this zero is a left half zero hence it will help in improving the phase margin of the system a little bit. Also there will be a pole at node $V_x$ which will be located at a really high frequency. But these effects are not the dominant effects of the system and will not be dominating the frequency response of the system. The current output of the class AB amplifier can be given as

$$i_{out} = g_{meff} V_{cm} \left( \frac{1 + s/\omega_z}{1 + s/\omega_p} \right)$$

(4.6)

Where $g_{meff}$ is the effective $g_m$ of $M_p$, which will be affected by the presence of upper N-type transistor. The upper N-type transistor in Fig.28 acts as a source degeneration and hence the effective $g_m$ is given by

$$g_{meff} = \frac{g_{mp} g_{mn}}{g_{mp} + g_{mn}}$$

(4.7)

Where $g_{mn}$ and $g_{mp}$ are the transconductance of $M_p$ and $M_n$ transistors shown in Fig.28.

The dominant pole in the common mode feedback loop continues to be the same one as in Fig.24 but the two non-dominant poles change. The location of poles is given by

$$\omega_{dom} = \frac{g_o}{C_L}, \quad \omega_{non-dom1} = \frac{g_{mn} \cdot C_p2 + \Delta C}{C_p1 + C_{GSMP}} \quad \omega_{non-dom2} = \frac{g_{meff}}{C_p1 + C_{GSMP}}$$

(4.8)

The above two non-dominant poles will play an important part in the frequency response of the common-mode feedback loop. Let us now analyze the DC gain of the common-mode loop. If the DC gain of the loop is low then the output common-mode will have higher offsets hence it is important to have a good DC gain. If we analyze the output impedance at the dominant pole for the common-mode loop then we realize that it is higher than the $R_{out}$ of the differential mode because the source degeneration resistors do not play any part in common-mode. The source degeneration resistors lower the $R_{out}$. The output impedance for common-mode loop is given by

$$R_{outCM} = R_{oMn} (A_{oMn}) R_{oMP} (A_{oMP})$$

(4.9)

Hence the DC gain of the common-mode loop is given by
As is evident from the above equation the DC gain of the common-mode loop is higher than the DC gain of the differential gain of the OTA.

D. Simulation Results

Initially CMFB was implemented for all the OTA’s in the system. The approach tried is shown in Fig.29.

![Fully differential Biquad](image)

Fig.29. Previously implemented CMFB scheme.

But after simulations it was realized that there were too many feedbacks in the above circuit and it was making the whole Biquad unstable. Too many loops create a lot of parasitic poles in the system. Although the above scheme is really sound for a robust CMFB circuit but too many feedback loops were inducing common-mode oscillations which are not good for the stability as well as these common-mode oscillations degrade the Total harmonic distortion of the Biquad. It was realized that the amplitude of those
oscillations was really large. Fig.30 shows the common-mode oscillations in the above circuit. These common mode oscillations are as large as 17mV and were producing lot of distortions in the circuit and were undesirable.

Because of the above effect we utilized the scheme shown in Chapter II Fig.8. This scheme has less number of feedback loops and there are no common-mode oscillations. Also this design is much more stable. We tested the stability of the Common-mode loop by breaking open the loop at the dominant pole. We used a very large inductor to maintain the DC operating point of the loop and injected the signal at the low pass node as shown in Fig.31. We measured the open loop gain of the CMFB loop and the phase margin of the loop. We realized that the phase margin of the loop was quite good (= 68°) and the DC gain of the common-mode loop was quite high, as big as 34dB, which is larger than the differential DC gain of the OTA. This was expected and has been
discussed in the previous section. Fig. 32 shows the open loop response of the CMFB loop. The common-mode was settling very close to the required 0V value.

Fig. 31 Test for the stability of common-mode loop.

Fig. 32. Frequency response of the open loop CMFB circuit.
Another important test for the stability of the common-mode loop is also shown in Fig.33. We inject a small step current at the lowpass node and see the step response to this current injection. If the output voltage settles to a proper output then the system can be defined as stable. This response has been shown in Fig.32. As discussed in the previous section the size of transistor affects the loop phase margin. The larger the size of Mp in Fig.25 the larger the gm of that transistor and larger the DC gain of the loop. But a larger Mp generates more parasitic and thus shifting the pole at Vcm in Fig.25 to lower frequency degrading the phase margin. This effect has been shown in Fig.34 where the W/L was varied from 25 to 500. We observe that a large size of Mp has the phase margin of 38°, which is not good.

![Fig.33. Step response of CMFB loop with current injection.](image-url)
Fig. 34. Effect of size of \( M_p \) on the phase margin.
CHAPTER V
DESIGN OF TUNING CIRCUIT

A. Overview of Tuning Circuit

Continuous-time integrated filters require a tuning circuitry. This requirement is a result of large time-constant fluctuations due mainly to process variations. On chip automatic tuning of filters is a very challenging task, especially at high frequencies. This section presents a brief overview of tuning.

1. Why Tuning Circuit is Required

Process variations cause a variation in the actual integrated value of components like capacitors and resistors than the intended design value. Resistors or transconductance values might vary by 20% while the capacitors might vary by 10%. Effectively the resulting RC or $g_m$-C time constant products are accurate to only 30% with process variations [19]. In addition, temperature variations further aggravate the situation because resistance and transconductance value changes substantially over temperature. A tuning circuitry is required to prevent this pole shifting. The tuning scheme modifies the transconductance values such that, the resulting time-constants are set to known values. It will be noted that, although absolute component tolerances are really high, relative accuracies can be quite good. In this design only frequency tuning has been incorporated. The Q-tuning for this design is really not important, as it is really low Q applications, with all Q being less than or equal to 1.

2. General concepts in Tuning

Most of the times Capacitors are integrated as ratio of two capacitances. It is easy to realize a pretty accurate capacitor ratio. Also the transconductance values can also be set
reasonably accurately. For example if the transconductor implementation is a CMOS differential pair with source degeneration resistor, then the effective transconductance is set by the source degenerating resistor as has been discussed in previous chapters. Similarly if other transconductors of the same type are used, their effective $g_m$ value can be set by choosing appropriate transistor sizes, bias currents, or source degeneration resistor value. All the transconductances can be written as $g_{mx}$, as an accurate constant multiplied by some basic transconductance value. This can be expressed as

$$G_{mx} = k_{mx} G_{m1}$$  \hspace{1cm} (5.1)

Here, the constant $k_{mx}$, is set reasonably accurately by appropriate transistor, resistor or bias current scaling. The tuning signal generated to correct the value of $g_m$ is then fed to the filter to be tuned. This has been shown in Fig.35.

![Fig.35 Indirect frequency tuning by adjusting the $g_m$.]
B. Possible Tuning Implementations

A review of the literature [19] [20] [21] has shown that using a standard reference frequency has been a standard method for tuning. From the filter’s response to the reference signal at this know frequency, the tuning circuitry must then detect and identify any errors, compute the appropriate corrections and apply them via a suitable control circuit to the filter. However in using this approach, it is to be remembered that the reference signal to be applied must not be allowed to interfere with the filter’s main information signal in order to avoid undesirable cross-talk or intermodulation.

1. Prominently Used Tuning Techniques

The Frequency tuning most of the time employs PLL (Phase Locked Loop) techniques for low Q applications [19]. Such techniques normally have a Master-Slave configuration. The reference signal is applied to the Master filter and the response generated by the master filter is feed to a frequency control circuit. This frequency control circuit generates the control voltage for error correction and feeds it to the Slave filter, which is the main filter.

Besides their design complexities, this tuning method is very sensitive to small phase errors as frequency and Q increase. Furthermore phase detectors needed for very high frequency applications must be really fast. This also limits PLL tuning techniques.

Another interesting tuning scheme reported [9] tries to set the value of transconductor \( g_m \) to adjust the –3dB frequency of the filter. The OTA \( g_m \) used for tuning is a replica of the transconductor used in the filter. This scheme has been shown in Fig.36 and shows the tuning control voltage being fed to all the transconductors in the main filter. The tuning integrator used is a lossless integrator, and its unity gain frequency is given by

\[
fu = \frac{G_m}{2\pi C_L}
\]  

(5.2)
By applying a reference input signal $v_{ref} = A\sin(2\pi ft)$, the integrator output voltage is given by [9]

$$v_o = v_{ref} dt = \left(\frac{f_u}{f_{ref}}\right) A\cos(2\pi f_{ref} t)$$  \hspace{1cm} (5.3)

![Diagram of tuning scheme based on squarer.](image)

The reference voltage and the integrator output are then squared which gives us the following expressions [9]

$$v_{ref}^2 = \frac{1}{2} A^2 - \frac{1}{2} A^2 \cos(4\pi f_{ref} t)$$

DC level high frequency component

$$v_o^2 = \frac{1}{2} \left(\frac{f_u}{f_{ref}}\right)^2 A^2 + \frac{1}{2} \left(\frac{f_u}{f_{ref}}\right)^2 A^2 \cos(4\pi f_{ref} t)$$  \hspace{1cm} (5.4)

As shown in Fig.36 the high frequency components are filtered out and the DC levels were compared to obtain the error. This voltage was used to control the –3dB frequency of the filter.
The above scheme utilizes the magnitude detection and the error signal generated is based on the difference of the magnitude. Magnitude detection is a good approach as the errors related to the phase error detection can easily be avoided, as well as it is simple to design. But the above scheme suffers from DC offset voltages. However the main drawback is that the above scheme uses the reference signal at the same frequency as the cutoff frequency of the filter. The use of this frequency creates tones at the cutoff frequency and creates interference with information signal to the filter. This leads to unnecessary cross talk and intermodulation at the filter output. To avoid the above problem we concentrated our attention to an alternate tuning scheme.

C. Implementation of a Tuning Scheme

It was realized that that a tuning scheme need to be implemented, where the input reference signal is N times smaller than the filter information. This helps us in not only using a low frequency input reference signal, which is easy to generate, but also it helps us in generating a cleaner output. A peak detection technique has been implemented [22] for pole correction by adjusting the $g_m$. However this implementation is not very effective as the tuning is done at the cut-off frequency of the filter. This kind of tuning is rendered ineffective for high frequency design as it will require a reference operating very high frequency. This is not a very good idea because at higher frequency a lot of noise will be injected from the substrate. The new scheme implemented in this design utilizes the same transconductor $g_m$ as used in both the Biquads of the filter. The transconductance is tuned by a correction signal and thus this will fix the filter $g_m/C_L$, i.e. the −3dB frequency. This effectively means that we need to fix the pole in one of the Biquads and then tune our $g_m$. The Biquad chosen is the one operating at lower frequency because it’s easier to design the tuning loop operating at a lower frequency. Hence Biquad1 is chosen as it operates at $1.07\omega_o$, where $\omega_o$ is the −3dB cutoff frequency of the filter. Investigation of the low pass node of Biquad1 (Fig.9.) reveals that the load capacitor at that node is 1pF and the cutoff
frequency at that node is almost 600MHz. Hence if the $g_m$ of this Biquad is adjusted then it will tune the pole at this node.

An overall view of the design of the tuning loop is shown in Fig.37. Here the integrator has the same conditions as at the integrator at the lowpass node of the Biquad1. We have used two additional dummy elements so as to replicate the parasitic capacitance as seen by the actual integrator in the lowpass node of Biquad1. This node sees the input capacitance of two $g_m$ cells and it’s own output parasitic capacitance. The load capacitor used at this node is also the same used as in the Biquad1 of filter. Hence we are able to fix the pole at the lowpass node of Biquad1 with a similar pole in the tuning integrator. This will automatically tune the other poles in the filter because of feedback loops.

![Fig.37. Overall tuning architecture.](image-url)
1. Operation of the Tuning Circuit

The tuning is based on error correction of the pole frequency of the above integrator. Essentially it detects the magnitude of the output of the integrator and compares it with a reference signal’s magnitude and then compares the error between the reference and the integrator output. The resultant of the comparison is a DC control voltage, which is then fed back to the gate of the source degeneration resistor in the integrator. As we are aware that the resistance of a transistor operating in triode region is dependent on the gate voltage, given by the following expression

\[ R_{\text{on}} = \frac{1}{g_{ds}} = \frac{1}{\mu C_{\text{ox}} \frac{W}{L} (V_{G\text{s}} - V_{th})} \]  

(5.5)

Also we are aware that the overall \( g_m \) of the transconductor is dependent on this source degeneration resistor given by the Equation (3.12). Hence the \( g_m R \) factor keeps varying because of the change in on resistance. This produces a change in the effective \( g_m \) of the transconductor and thus changing the frequency response of the integrator.

Let’s analyze the tuning loop based on the above knowledge. If a reference signal whose frequency is lower than the GBW of the integrator is applied then it produces a gain at the output of the integrator. This information is converted to current using a Voltage to current converter as shown in Fig.37 and then some current processing is done. After this processing the current is again converted to voltage and fed to a rectifier circuit. This rectifier circuit will rectify the signal and then also reduce the ripples in the signal. This will provide us with a DC information. Now the DC information from the integrator circuit and the reference circuit is compared and a DC error control signal will be generated. This DC control signal will decrease if the input reference signal is lower than GBW of the integrator and will increase the \( R_{\text{on}} \) of the resistor based on Equation (5.5). An increase in the Ron will decrease the effective Gm and hence will reduce the GBW of the integrator until and unless it becomes equal to the frequency of the applied signal. Once the pole of the tuning integrator is adjusted it will also adjust the poles in the filter and the filter –3dB frequency can then be adjusted appropriately.
As discussed earlier we decided to give a reference signal, which is $N$ times smaller than the GBW of the tuning integrator. The main advantage behind this idea is to reduce the intermodulation and the interference of the reference signal with the information signal of the filter. Fig. 38 shows the effect of choosing a reference signal, which is $N$ times smaller than the unity gain frequency of the integrator. The figure is the frequency response of the integrator. It shows that if the reference signal is $N$ times of the unity gain frequency $f_u$ of the integrator then gain of the reference signal at the output of the integrator is $N$ times.

![Frequency response of the integrator](image)

The value of the factor $N$ is chosen as 4. We are aware that the unity gain frequency is 600MHz hence the reference frequency can be chosen as 150MHz. There are several reasons behind choosing the reference frequency as $f_u/4$, the primary one being that the tones generated by reference signal will appear at 150MHz and it’s odd multiples. This will not interfere with the input signal to the filter. Also it is easy to generate a reference at 150 MHz than a 600MHz signal. We could have chosen a reference frequency that is higher than $f_u$ and still avoid interference with filter input signal. But it will force us to
design the part of tuning circuitry operating at a really high frequency. This will further complicate the design.

2. Tuning Circuit Specifications and Design

The tuning circuit shown in Fig.37 has the integrator circuit and certain dummy elements to replicate the parasitic capacitances. This part of the circuit has already been designed. If we choose a reference signal at 150 MHz then the integrator will generate the output voltage with a gain of 4. Since we are using a magnitude detection technique, this forces us to design a divider, which can attenuate the output signal by a factor 4, so that we can compare the output with the reference signal, which still has a gain of 1. Now designing a voltage divider will complicate the circuit so we decided to do the processing in terms of current. Hence the voltage output at the integrator is converted to current using a voltage to current V-I converter. We have used simple folded cascode architecture for this purpose. Fig.39 shows the architecture for this V-I converter.

![Fig.39. Voltage to current converter.](image-url)
The above voltage to current converter will deliver a current output, which will have a DC offset component and an AC signal. We are interested only in the AC signal as the information of the reference signal is preserved in it. Instead of having the lower current mirror present in the above circuit we have shown it as a separate circuit to explain the concept clearly. After we generate the current output from a signal we will need to do a current processing. This processing is the division operation, which will be performed on the current obtained from the integrator circuit. As we are already aware that a parallel processing of the input reference signal is being done using a reference circuit as shown in Fig.37, by converting it to current using the same V-I converter used above. The current output at the reference circuit is not divided at all and has the correct magnitude information already present. The division operation is only performed on current obtained at the output of the actual integrator circuit. This current division is done by using a simple current mirror circuit as shown in Fig.40.

Fig.40. Current mirrors used for integrator circuit & the reference circuit.

As is evident from Fig.40 the output of the V-I converter from the integrator circuit will generate a current equal to $I_B+4I_{ac}$ and the current output of the reference circuit is $I_B+I_{ac}$. 
Hence we put an additional current source on top of the current mirror for the integrator circuit, which will generate $3I_B$ DC current. Hence we have $4I_B+4I_{ac}$ current going to the current mirror for the integrator circuit. For the current mirror of the reference circuit no extra current source is needed, the current in this case being $I_B+I_{ac}$. The mirroring ratio for the current mirror of the integrator circuit is 4:1 hence a division operation is performed. The effective current at the output of the current mirror of the integrator circuit is now $I_B+I_{ac}$. The current mirror ratio at the output of the current mirror in the reference circuit is also $I_B+I_{ac}$. Now we have outputs, which can be compared. The current outputs of the integrator circuit and the reference circuit are then converted to voltage using a diode connected P-type transistor. This voltage is then fed to the rectifier circuit for rectification. For better division and current processing a cascode current mirror could have been used, but the cascode architecture was giving us the headroom issues, hence we decided to live with mismatches resulting from the simple current mirror. The rectifier circuit used for the rectification circuit is shown in Fig.41.

The rectifier circuit is actually an envelope detector circuit. The signal is rectified by the differential pair as shown in Fig.41. The current source M2 and the detector capacitor
$C_{\text{rectifier}}$ holds the DC information and also removes the ripples from the rectified signal thus converting it to an almost pure DC signal. The rectified signal will have a frequency that is double the input frequency. The current source discharges the output node of the detector. The current source and the capacitor determine the discharging speed of the detector. The charge and the discharge of the envelope detector can be mathematically modeled as [7]

$$v_{\text{out}} = \max(v_{\text{in}+} - V_{GS}, v_{\text{in}+} - V_{GS}) \quad \text{charging}$$

$$v_{\text{out}} = v_{\text{outchar}} - \left( \frac{I_{M2}}{C_{\text{rectifier}}} \right) t \quad \text{discharging} \quad (5.6)$$

Where max is the maximum between $v_{\text{in}+}$ and $v_{\text{in}+}$. During the charging time, the output of the envelope detector is equal to the higher differential pair input voltage, $v_{\text{in}+}$ or $v_{\text{in}+}$, level shifted by the $V_{GS}$ of M2. If the common-mode voltage of the differential pair input signal decreases rapidly, then $C_{\text{rectifier}}$ is discharged by the current source M2. After the rectification operation of both the integrator and the reference circuit the DC information obtained is compared. A high gain two stage amplifier has been used in this case. This high gain amplifier is shown in figure 42.

![Fig.42. Two stage high gain amplifier.](VDD)

$\begin{align*}
VDD & \quad M6 & \quad M6 & \quad M7 \\
\text{vin}+ & \quad Mn & \quad Mn & \quad V\text{bias} \\
& \quad M3 & \quad M5 & \quad \text{To the main OTA Gm} \\
& \quad C_{\text{compensation}} & \quad \text{Tuning Voltage} \end{align*}$
The high gain amplifier is needed, as the difference in the two DC signals is not that large. Another important consideration in choosing the two-stage amplifier was the high output swing. A folded cascode would have given us a high gain but at the cost of reduced output swing. High output swing is required for the tuning control voltage to almost swing to the VDD. We have designed the high gain amplifier such that the tuning voltage swings around the nominal value of 500mV. The tuning voltage generated from the above amplifier is fed back to the main OTA $g_m$.

D. Simulation Results of the Tuning Circuit

Simulations ran on the tuning circuit resulted in various plots which gives us an insight into the various aspects of how the tuning scheme works.

1. Tuning Voltage

Fig.43 shows the tuning voltage when we ran a transient simulating circuit. We fixed the load capacitor to the integrator as 1pF, which is the nominal load.
Fig. 43. Tuning voltage with a nominal load of 1pF.

The above simulation was performed after we set the initial condition on the output voltage of the tuning circuit to 10mV. This was done in order to save time on the transient simulation. If we don’t have an initial condition on the output voltage then the tuning voltage starts from a more negative voltage and settles to the final value in a longer time. It can be observed from the above simulation voltage settles to the final DC value to correct the pole location.

2. Filter Output with the Tuning Voltage

Fig. 44 show the filter output with the tuning voltage. As is evident from the Fig. 44 the output of the filter starts increasing with an increase in the Gm of the filter. The peak to
peak value of the output signal increases as the tuning voltage tries to settle to the final value.

3. Variation of the Tuning Voltage with Load Capacitor.

Fig. 45 shows the effect of the change in load capacitor. We know that the process variations might change the value of the load capacitor thus affecting the overall frequency response of the filter. If a fixed reference frequency of 150 MHz is applied, the tuning voltage will vary so as to set the filter \(-3\)dB frequency to the specified value. Figure 45. Shows the variation of this tuning voltage with the change in load capacitor from 600 fF to 1.4 pF. This is a transient simulation performed after running a parametric sweep on the load capacitor from 600 fF to 1.4 pF.
4. Rectified Voltage.

Fig.46 shows the rectified voltage at the output of the rectifier circuit. The AC signal after the current processing is rectified in the rectifier circuit. Only the envelope information or the DC Magnitude information is preserved after rectification. The capacitors in the rectifier circuit remove the ripples in the rectified voltage.
Fig. 46 Rectified voltages after the rectification operation.

Fig. 46 shows the rectified voltages at the output of the integrator circuit and the reference circuit and these two rectified voltages are compared with the help of a high gain amplifier. The ripples in the circuit have been reduced to a large extent and are as small as 60uV. Also the rectified signal has a frequency double of the reference signal as is shown in Fig. 47 which is a zoomed in view of above rectified signal.
Fig. 47. A zoom in view of rectified signal with the ripples.
CHAPTER VI
SIMULATION RESULTS OF THE FILTER

A. Schematic Level Simulation Results of Biquads Without Tuning

After designing the integrators, resistor and the common mode feedback circuit to be used in the Biquads an effort was made to simulate them. Several simulations were run before the specifications on the Biquads were met. The primary specifications on the Biquads were the frequency response, the linearity specification, the group delay and the noise results were met. After tweaking the circuit to meet the above mentioned specifications meaningful results were obtained. One of the very important initial tasks was to estimate the parasitic capacitances involved at each node, as they limit the filter’s frequency response. A mathematical estimation of the parasitic capacitances was done in Chapter II; we tried to estimate those values empirically through simulations in cadence as well. As mentioned previously all the simulations were performed in cadence using TSMC 0.35\(\mu\) technology and with the supply voltages \(\pm1.65V\). After the estimation of parasitic capacitances the design of the Biquads was frozen and simulations were run to estimate their performance.

1. Estimation of the Parasitic Capacitance

Calculation of parasitic capacitance involves AC simulations on the main OTA. Equation (2.13) in Chapter II shows that the parasitic capacitor at the bandpass node of the Biquad involves three output capacitance (3\(C_o\)) of the main OTA and two input parasitic capacitance (\(\Omega C_i\)) of the same OTA. Similarly for lowpass node one \(C_o\) and one \(C_i\) parasitic capacitances are present. Hence the estimation of the parasitic capacitance boils down to the calculation of input and output parasitic capacitance (\(C_o\) & \(C_i\)) of the main OTA. Instead of trying to calculate the parasitic from the DC operating points it is more
accurate to calculate it by AC simulation. AC simulations on the main OTA with two
different load capacitors will result in calculation of parasitic information.

**Calculation of Output Parasitic:** AC simulations on the OTA in open loop for two
different load capacitors result in two different unity gain frequencies for the OTA. We
know that Gain Bandwidth Product (GBW) of an OTA is given by

\[
GBW = \frac{g_m}{C_{\text{load}} + C_{\text{out, parasitic}}} \quad (6.1)
\]

In the above equation GBW of the OTA is already known from the two simulations. Also
the load capacitances for the two different loads are known. So there are two unknown
quantities and two simultaneous equations. Solving the two to obtain the output parasitic
capacitance \( C_{\text{out, parasitic}} \) of the OTA, we get

\[ C_{\text{out, parasitic}} = 0.2157 \text{ pF} \]

**Calculation of Input Parasitic:** Input parasitic can be calculated using two OTA cascaded
to each other. The second OTA will now be loading the first OTA with an additional
input parasitic capacitance \( C_{\text{in, parasitic}} \). Hence the GBW of the first OTA will now be given
by the following expression

\[
GBW = \frac{g_m}{C_{\text{load}} + C_{\text{out, parasitic}} + C_{\text{in, parasitic}}} \quad (6.2)
\]

Again AC simulations will yield two different GBW for two different load capacitance.
\( C_{\text{out, parasitic}} \) is already know from previous section and \( C_{\text{load}} \) is also known. Again solving
the two simultaneous equations yields the input parasitic capacitance as

\[ C_{\text{in, parasitic}} = 0.214 \text{ pF} \]

The input and output parasitic capacitance gives us the amount of load present at the
various nodes in Biquad. We will now scale up our design based on this information. The
cut-off frequency for Biquad2 is 1.5 times the cut-off frequency of the filter, so the
effective capacitance at the bandpass node of Biquad2 has to be minimized. Already
there is \( 3C_o \) & \( 2Ci \) at the bandpass node, which amounts to almost 1 pF. A load
 capacitance of 200 fF was chosen for this node, which makes the capacitance at this node
equal to 1.2 pF. Similarly for the lowpass node we chose 450 fF as the load capacitance
thus making the capacitance at lowpass node almost equal to 1.2pF. Similarly for Biquad1 the capacitance at bandpass and lowpass node turns out to be 1.6pF. The load capacitance at lowpass node being 1pF and at the bandpass node being 650 fF of Biquad1. Of course these values have been adjusted after a little tweaking in the simulations.

2. Schematic Level Simulation Results of Biquad1

Frequency Response of Biquad1

An AC simulation on Biquad1 resulted in the frequency response of the Biquad1. This simulation was done with a standalone Biquad with the building blocks like OTA-Gm, resistor and CMFB circuits developed in the previous section.

Fig.48 depicts the frequency response of Biquad1 at the lowpass node.

---

Fig.48. Frequency response of Biquad1 at the lowpass node.
Since the Q of Biquad1 is 0.55, the frequency response shows us a flat magnitude response. The –3dB cutoff frequency is at 562 MHz, the overall cut-off frequency will also be closer to this value as Biquad1 has a cut-off frequency of 1.075 times the cutoff frequency of the overall filter. The DC gain of Biquad1 is equal to –0.637 dB.

**Group Delay of Biquad1:**

Fig.49 shows us the group delay of Biquad1.

The Group delay information was extracted from the phase response of Biquad1. It is the derivative of phase with respect to \( \omega \). The group delay ripple of the Biquad1 is about 9%. This is expected for high frequency design, as it is very difficult to obtain a perfectly
linear phase. The phase of the filter is affected by high frequency poles, which are present at not so high frequency.

**Transient Response of Biquad1:**

Fig.50. shows the transient response of the Biquad1. This simulation was made with a sinusoidal signal input to the Biquad1. The signal employed for this purpose has magnitude of 200 mV peak-to-peak at 500 MHz.

![Graph showing transient response of Biquad1](image)

The THD of the above transient response was evaluated and it turned out to be 0.1%. The harmonic distortion was measured after a DFT analysis. Fig.51 shows the DFT analysis of the above sinusoidal signal.
Fig. 51 Discrete Fourier Transform of the differential output of Biquad1.

The DFT analysis shows the third harmonic distortion at 1.5GHz to be –66dB below the fundamental signal. This gives us a clear picture of the harmonic distortions in the filter. An HD3 of –66dB can be considered as good for the Biquad.

3. Schematic Level Simulation Results of Biquad2

Frequency Response of Biquad2

Similar AC simulation was performed on Biquad2, which resulted in the frequency response of the Biquad2. Again this simulation was done with a standalone Biquad2. Fig. 52 depicts the frequency response of Biquad2 at the lowpass node.
Fig. 52. Frequency response of Biquad2 at the lowpass node.

Since the Q of Biquad2 is 1.0652, the frequency response shows us a peak in the magnitude response of the lowpass output. For a low pass output with Q greater than 0.707 the following relation can be used [23]

$$\omega_{peak}^2 = \omega_0^2 \left(1 - \frac{1}{2Q^2}\right)$$

(6.3)

An easier way to measure the Q and \( \omega_0 \) will be to look at the bandpass node. The Frequency response at bandpass node response is shown in Fig. 53.
The $\omega_0$ of the bandpass response is located at 912MHz, which is 1.5 times the $\omega_0$ of the overall filter and the $\omega_0$ of Biquad1, which is located almost at 600MHz. Also the Q of Biquad2 is almost equal to 1. The DC gain of Biquad2 is -0.303 dB, which is closer to 0.

**Transient Response of Biquad2:**

Fig.54. shows the transient response of the Biquad2. Again this measurement was made with a sinusoidal input to Biquad2 with same magnitude of 200mV peak-to-peak and 500MHz frequency. The THD of the above transient response was measured and turned out to be 0.053%.
Fig. 54. Transient response of Biquad2 at 500 MHz signal.

The harmonic distortion was also measured after a DFT analysis. Fig. 55 shows the DFT analysis of the sinusoidal signal output.
The DFT analysis shows the third harmonic distortion at 1.5 GHz to be –65dB below the fundamental signal. An HD3 of –65dB is also a good figure of merit.

**B. Schematic Level Simulation Results of Overall Filter Without Tuning**

Frequency Response of Overall Filter:
The frequency response of the filter is a frequency domain analysis. Hence with the tuning scheme it is not possible to simulate the frequency response of the overall filter until the tuning voltage settles to the final value and the DC operating point is then calculated. However this is only a simulator level limitation and in silicon characterization it is not a problem. Hence we have done the frequency response
measurement with a fixed DC voltage being applied to the tuning node, the value of which is equal to the expected final settled value of the tuning voltage.

Another important aspect to be looked into is the presence of a buffer at the output of the overall filter. This buffer is needed, as the output of the filter cannot be directly connected to the pad frame. Pad frame, the bonding wire, components on the PCB and the measurement equipment have big parasitic capacitance. In 0.35µ TSMC process we expect these parasitic capacitance to be greater than 5pF. This will kill the frequency response of the circuit. Hence we need to put a buffer at the output of the filter. But this will alter the transfer function of the filter. Suppose the transfer function of filter is \( H_1(s) \) and the transfer function of buffer is \( H_2(s) \) then the overall measured transfer function is given by \( T(s) = H_1(s)H_2(s) \). Hence another similar buffer need to be embedded in the chip. We can extract the transfer function \( H_2(s) \) of this buffer alone and can then extract the actual transfer function of the filter by

\[
T_{\text{filter}}(s) = \frac{H_2(s)H_1(s)}{H_2(s)}
\]

(6.5)

This scheme has been shown in Fig.56. It shows a buffer at the output of overall filter and a separate buffer in the chip.
We used another OTA for the purpose as it is fast and has a good linearity. An AC simulation on the above architecture yields the frequency response of the overall filter without buffer. Fig.57 shows the Overall filter response along with the frequency response of Biquad1 and Biquad2. The –3dB cutoff frequency of the overall filter without the buffer is at 554 MHz. This is close to the –3dB cutoff frequency of Biquad1. Also the overall filter has a faster roll-off as it is a fourth order function. As is evident from Fig.57 Biquad2 does the shaping of the Frequency response of the overall filter.
Fig. 57. Frequency response of overall filter (without buffer), Biquad1 and Biquad2.

The Frequency response of the overall filter is shown alone in Fig. 58 for more clarity.
Both the above shown figures are at the output of fourth order filter. But the Frequency response that will be available to us at the time of measure is more important. We have loaded the output of buffer with $50\Omega$ termination resistance and a $2\text{pF}$ capacitive load. This load can be considered as a macro-model of the load on the filter because of the measurement equipment. An AC simulation on the overall filter along with buffer resulted in the frequency response shown in Fig.59.
The above frequency response shows that the output of the buffer is lower by –6dB than the frequency response of the overall filter. This is because of the resistive loading at the output of 50ohm. Also the –3dB frequency is reduced to 480MHz which is due to the additional pole at the output of the buffer.
Group Delay of the overall Filter:

Fig. 60. shows the overall group delay of the filter. We see that the overall filter has a nice group delay at the output of the overall filter. The overall variation in the Group Delay upto 700MHz, which is approximately 1.25 times cutoff frequency of the filter, is less than 3.8%. This is a good result considering the frequency of operation of the circuit.

![Group Delay of the Overall Filter](image)

The group Delay of the filter along with the buffer is shown in Fig.61.
The Group Delay of the filter degrades at the output of the buffer and is less than 6% at the cutoff frequency of the filter.
Transient Response of the Overall Filter:

The transient response of the overall filter was evaluated with a 200 mV peak-to-peak and 500 MHz input sinusoidal signal. Fig.62 shows the fully differential output at the output of overall filter and Fig.63 shows the fully differential output of the buffer.

Fig.62. Fully Differential sinusoidal output of the overall filter.
Fig. 63. Fully Differential sinusoidal output at the buffer output.

Distortion analysis of the above transient response reveals the HD3 performance of the filter. Fig. 64 shows the third harmonic distortion of the overall filter. The third harmonic distortion at 1.5 GHz is very low and is -76 dB below the signal.
Fig. 64 DFT of the overall filter.

Fig. 65 shows the DFT analysis of the differential output at the buffer. The third harmonic distortion at 1.5GHz in this case reduces to –73dB below the signal.
C. Schematic Level Simulation Results of the Overall Filter With Tuning

Transient Response of Overall Filter:
As mentioned before it is not possible to simulate the frequency response of the overall filter, with the tuning scheme until the tuning voltage settles to the final value. Hence we can only show the transient response of the system with the tuning scheme.

Fig. 65 DFT at the output of the buffer.
Fig. 66 shows the transient response of the overall filter with a sinusoidal input of 200 mV peak-to-peak and 500MHz signal. 

**Differential Output of the Overall Filter (Zoom-in)**

Fig. 66 Differential output of the overall filter with tuning.
Fig. 67 shows the transient response at the buffer output with the same input. The DFT analysis of the above transient response yields the third order distortion (HD3). Fig. 68 show the DFT of the Overall filter with tuning.
Fig. 68. DFT of the differential output of the overall filter with tuning.

Fig. 69 shows the DFT of the Buffer with tuning.
D. Post Layout Simulation Results of the Overall Filter Without Tuning

The Layout of the filter was done utilizing Virtuoso in Cadence. The Layout was done in a modular way and layouts of the basic building blocks were created first. These layout were tested with a design Rule checker (DRC) and after extraction a Layout Vs Schematic (LVS) was performed. After successful completion of LVS Post Layout Simulations were performed on the extracted view. This extracted view contains all the parasitic information. Great care was taken while doing the layout to minimize the parasitic capacitance as well as reduce the mismatches. An effort was made to have the same boundary condition for the elements to be matched. A layout of the main OTA is shown in Fig.70.
The Floor Plan of the Overall Layout has been shown in Fig. 71. All the building blocks have been arranged on the basis of size constraints. An effort was made to minimize the parasitics in the signal path and share the Power lines and the bias voltage.
Fig. 71. Floor plan of the layout showing the individual building blocks.

The routing of the signal path and interconnects have not been shown in the Floor Plan. The above Floor Plan is not up to the scale. Fig. 72 shows the actual layout of the filter without the padframe to give a clear picture of the size of the filter. A 64 pin package was chosen for the above design. The power lines chosen were thick and the thickness was chosen to meet the current density requirement so as to handle the amount of current absorbed by the circuit. Also the routing of the bias lines is shared by different elements. The blocks have been placed such that they have the same boundary conditions. Adding dummy elements would have increased the parasitics but reduced the mismatches.
Post Layout: Frequency Response of Overall Filter

Fig. 73 shows the Post Layout Frequency response of the Overall Filter response along with the frequency response of Biquad1 and Biquad2. This measure was made with the buffer connected to the output of the filter. We disconnected the tuning system to measure the frequency response and a DC voltage of 500 mV was given to the tuning...
node from an ideal DC source. The –3dB cutoff frequency of the overall filter is at 490 MHz. This is close to the –3dB cutoff frequency of Biquad1.

From the frequency response plot it is observed that the cutoff frequency of the filter has been reduced because of the additional parasitic in the circuit. The interconnects and routing creates this additional parasitics. We have tried to ensure the minimum parasitic in the signal path and a cutoff of 500MHz was the best that could be achieved.

Fig.74 shows the Frequency response of the overall filter along with the frequency response at the output of buffer. The additional parasitic capacitance have affected the frequency response and reduced the cut-off frequency. However the DC and other characteristics continue to remain the same. Unfortunately the simulator has the
limitation of not affecting the Post layout due to mismatches, hence the Post layout simulations differ from schematic ones.

![Post Layout: Frequency Response at output of buffer and overall filter](image)

Fig. 74. Post layout: frequency response of overall filter and buffer output.

**Post Layout: Group Delay of the overall Filter:**

Fig. 75. shows the overall group delay of the filter. The overall filter has a variation in the group delay of 9% up to the cutoff frequency of the filter.
The parasitic capacitors affect the frequency response and degrades the phase response. The degradation of the linearity of phase at high frequency in turn affects the Group delay. The additional parasitic due to the interconnect creates these high frequency poles. However this variation of the Group Delay at such high frequencies is expected.

**Transient Response of Overall Filter:**

Fig. 76 shows the DFT of the transient response of the filter at the output of buffer with a sinusoidal input of 200 mV peak-to-peak and 500MHz signal. DFT analysis was made on the fully differential output.
Post Layout measurements show the third harmonic distortion to be –57dB lower than the signal. This simulation was done with an input signal of 180MHz, hence the third harmonic distortion lies within the inband of the cut-off frequency of the filter. This gives a more realistic estimate of the distortion as the third harmonic distortion is not attenuated by the frequency response of the filter.
E. Post Layout Simulation Results of the Filter With Tuning

Post Layout: Frequency Response of Overall Filter with tuning

Fig. 77 shows the frequency response of the overall filter along with the frequency response at the output of buffer with the tuning scheme. This simulation was done with the DC tuning signal applied to the integrator. The applied tuning signal has the magnitude of 361mV. The additional parasitic capacitance have affected the frequency response and reduced the cut-off frequency.

Fig. 77. Frequency response of the overall filter and filter + buffer with tuning.
Post Layout: Group Delay of the overall Filter with tuning:

Fig. 78. shows the overall group delay of the filter. The overall filter has a variation in the group delay of 10% up to the cutoff frequency of the filter. This simulation was done with the tuning signal generated by a transient analysis of the filter.

![Group Delay Graph](image)

Fig. 78. Group delay of the overall filter and filter + buffer with tuning.

The tuning voltage generated in the post layout simulations have been shown in Fig. 79
Fig. 79 Post layout: magnitude of the tuning voltage.

Transient Response of Overall Filter with tuning

Fig.80 shows the transient response at the output of the buffer with a sinusoidal input of 200 mV peak-to-peak and 500MHz signal.
Monte Carlo Simulations:

Fig. 81 shows the Monte Carlo simulation results of the filter. These simulations were done with a 20% variation of $V_{TH}$ and $C_{ox}$ over a $3\sigma$ variation. These results indicate that the design is robust for most of the process corner variations. However, there are certain cases where the –3dB cut-off frequency lies in the 275MHz range and the DC gain goes down to –5dB. At these corners, the DC operating points of certain devices is not proper resulting in reduced performance.
Fig. 81 Post layout: Monte Carlo simulation results
A Table of simulated results of the filter has been shown in Table VII.

<table>
<thead>
<tr>
<th>Filter Parameters</th>
<th>Simulated Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3 dB Cut-off frequency</td>
<td>490 MHz</td>
</tr>
<tr>
<td>DC Gain</td>
<td>-0.9 dB</td>
</tr>
<tr>
<td>Group Delay variation</td>
<td>9 %</td>
</tr>
<tr>
<td>HD3</td>
<td>-57.39 dB</td>
</tr>
<tr>
<td>Power</td>
<td>140 mW</td>
</tr>
<tr>
<td>Area</td>
<td>1.42 mm$^2$</td>
</tr>
</tbody>
</table>

The results of the simulation prove that the filter is working at a cutoff frequency of 500MHz. The Group Delay is closer to expected results and the filter has reasonable linearity. The tuning circuit is able to tune the filter up to a cutoff frequency of 600 MHz.
CHAPTER VII
SUMMARY AND CONCLUSIONS

High Data Rates in the Hard Disk industry is the driving force towards the development of the Read Channel Filters. Hard Disk Industry is looking for pure CMOS implementations of such high frequency filters, instead of BiCMOS implementations. A CMOS solution for the above problem is presented. Several already reported filters were studied and their main drawbacks were identified. A 500MHz fourth order equiripple linear phase Filter has been designed, which can push the data rates to the range of Giga Hertz. The effects of parasitic capacitance were minimized and high-speed architectures were chosen for this design. A fast common-mode feedback circuit, which can handle these high frequencies, was designed for this purpose. A class AB amplifier was chosen instead of usual implementations to increase the common-mode speed and provide more stability for the common-mode loop.

Apart from the High frequency fully differential filter a new tuning scheme was evolved for the Filter. The $g_m$ of the integrator in the filter was adjusted with a tuning control voltage to accommodate the process variations and set the filter cutoff to the required frequency. The new tuning scheme requires a reference frequency of one-fourth the cutoff frequency. This prevents harmonics from reference signal appearing at the filter’s information signal and less noise is injected at lower reference frequencies. Simulation level performance of the filter show good GBW, group delay and distortion results. The filter operates at 500MHz in the Post Layout simulation and the Group Delay of the filter at such high frequency is less than 9%. The tuning scheme can tune the filter upto 600MHz. A well-matched printed circuit board (PCB) will be made with all the considerations for high frequency operation.

The chip was designed in TSMC 0.35µm technology. Currently the chip is queued for fabrication at MOSIS. Experimental results of the chip will be compared with the simulation results once the fabricated chip is received.
REFERENCES


VITA

Pankaj Pandey received his Bachelor of Engineering degree in Electrical Engineering from Regional Engineering College Surat, India in July 1998. He worked as a software engineer in Information Management Resources, Global India Ltd, Bangalore from August 1998 to June 2000. He joined the graduate program in electrical engineering at Texas A&M University in August 2000. He worked as a co-op in the Storage Products Group (Pre-Amp) at Texas Instruments, Dallas from January 2002 to July 2002. His main research interest is in the area of analog and mixed signal VLSI design, with emphasis on high frequency filters, tuning, signal processing, data conversion and RF circuits. Currently he is employed as an Analog designer in the Pre-Amp group of Texas Instruments, Dallas. His email address is ppandey@ee.tamu.edu. His home address is 8820 Southwestern Blvd., Apt 1115, Dallas, TX 75206.