ANALYSIS AND CHARACTERIZATION OF A PROGRAMMABLE LOW-DROPOUT REGULATOR

A Senior Scholars Thesis

by

XIAOFAN QIU

Submitted to the Office of Undergraduate Research
Texas A&M University
In partial fulfillment of the requirements for the designation as

UNDERGRADUATE RESEARCH SCHOLAR

April 2007

Major: Electrical Engineering

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Research Advisor: Jose Silva-Martinez
Associate Dean for Undergraduate Research: Robert C. Webb

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ABSTRACT

Analysis and Characterization of a Programmable Low-dropout Regulator (April 2007)

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Research Advisor: Dr. Jose Silva-Martinez
Department of Electrical and Computer Engineering

As portable electronic devices become a part of daily life, it creates a huge market for electronic components for those battery driven devices. Low-dropout (LDO) voltage regulator is an important part that provides steady DC supplies for other components. Low power, low noise and high stability are the desired features of a regulator.

Detailed analyses on CMOS LDO design and the designs of two different compensation schemes for LDO are presented in this thesis. Experimental results of the designed compensation programmable low-power low-dropout (LDO) Voltage Regulator, in comparison with an existing compensated LDO, are also presented.

The designed compensation implementation demonstrates a fast transient response and high stability in all programmable output levels. Testing chip fabricated in a standard $0.35\ \mu m$ CMOS technology provided the important parameters of the regulator, e.g. transient response, load regulation, line regulation, power supply rejection ratio (PSRR).

ACKNOWLEDGMENTS

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Second, I would also like to thank my advisor, Dr. Jose Silva-Martinez, for his time and effort in guiding me throughout the year to complete this research.

Last but not least, I would like to thank Abraham Islas, Chris Witmer, John Mincey and Vijay Dhanasekaran for helping me in the process of this research.

NOMENCLATURE

LDO	Low-Dropout
LVR	Linear voltage regulator
SMPC	Switching Mode Power Converters
EMI	Electromagnetic interference
ESR	Equivalent series resistor
DFL	Designed feedback loop
UGF	Unity gain frequency
RHP	Right-hand plane
LHP	Left-hand plane

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CHAPTER I

INTRODUCTION

A programmable voltage regulator has become an essential part of portable electronic devices, where low power dissipation, high efficiency, high stability, and low noise are desired characteristics.

Voltage regulators can be divided into two main categories: Linear Voltage Regulators (LVR) and Switching Mode Power Converters (SMPC). SMPC is restricted in the use of portable electronic devices, because of the high cost, possible electromagnetic interference (EMI), high output voltage ripple and noise [1]. On the other hand, LVR exhibits characteristics of very small output voltage ripple, compactness, and low output noise. Low-dropout Voltage (LDO) Regulator presents the lowest dropout voltage. In other words, LDO has the highest power efficiency of all the LVR. LDO is used widely in battery-powered electronics, where minimum noise is an important issue. Battery-powered devices are the intended applications of the designed LDO.

However, frequency response of the LDO system highly depends on load conditions. Load resistance significantly affects pole locations, resulting in the loss of stability due to the decrease in phase margin. Therefore, the stability issue for LDO system becomes the main challenge for LDO design. A feedback topology needs to be introduced to

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This thesis follows the style of *IEEE Transactions on Circuits and Systems*.

compensate the poles to gain high phase margin.

In this thesis, two different compensation schemes will be studied closely. One is using equivalent series resistor (ESR) of the load capacitor to gain stability. The other one is using an internal capacitor to gain stability, which is developed at Texas A&M University by the former master student, Abraham Islas. The goal of this research is to characterize, analyze and compare the performance of two schemes.

In chapter I, a general introduction on basic linear voltage regulator, CMOS LDO design concerns and two compensation schemes are provided. In chapter II, the testing parameters and the printed circuit board (PCB) design specifications are discussed. In chapter III, the experimental testing results are presented. In chapter IV, conclusions and future works are included.

Basic linear voltage regulator

A general structure of linear voltage regulator is shown in Fig. 1 [2] . A voltage-controlled current source is used to provide the regulated output voltage. A LDO needs to maintain a constant voltage at output with variations of load condition. Therefore, it requires a feedback loop in the system to monitor the output. Furthermore, in order for the system to be stable, a compensation circuitry needs to be included. For most linear regulators, a compensation scheme is part of the feedback path, while for LDOs, it requires an external load capacitor to achieve internal stability.

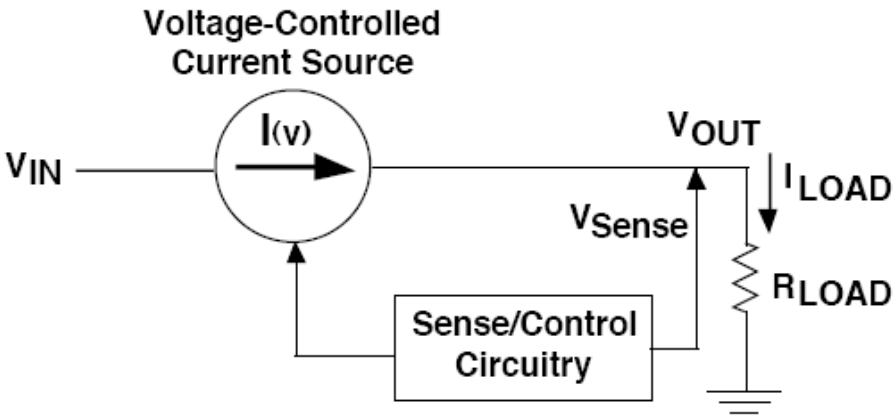

Fig. 1 Linear voltage regulator function diagram

The basic building block of the LDO circuit consists of four parts: the band gap reference, the pass element, the feedback resistor, and the error amplifier, as shown in Fig. 2 [3].

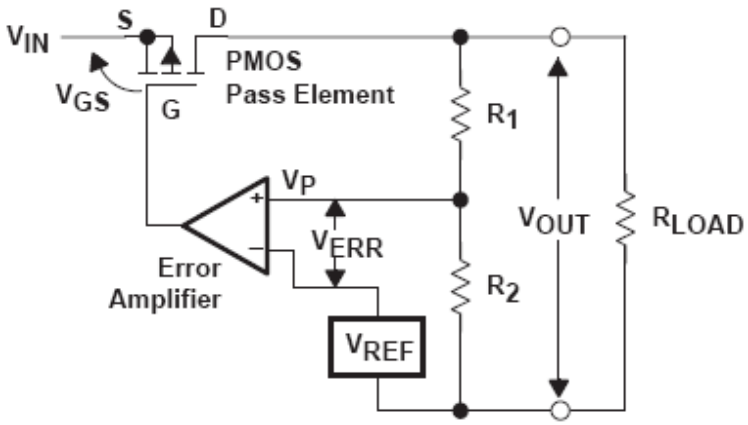

Fig. 2 Basic linear voltage regulator

Feedback path consist of R1, R2 and the error amplifier. Pass device function as the voltage-controlled current source, which is made up of NMOS, PMOS or bipolar transistors. There are three main types of regulators by replacing the pass element block with the following bipolar topologies, Fig. 3 [3]:

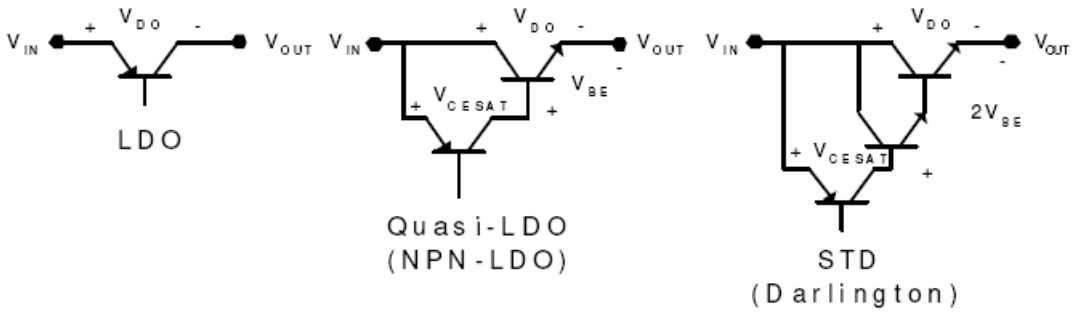

Fig. 3 Three types of pass element

The voltage drop across output and input node is called dropout voltage. To achieve higher power efficiency, a low dropout voltage is desired, especially for electronic applications. LDO has the lowest dropout voltage among three types. Therefore, LDO is best suited for battery-operated devices. A more detailed comparison of advantages and disadvantages for each topology is presented in [3].

CMOS LDO design

Steady voltage supplies to different components are highly demanded in electronic devices. It is important for a LDO to maintain a minimal voltage fluctuation while input voltage and output load condition varies. For CMOS LDO, an increase in efficiency

results in a larger pass element, in order to reduce the drop-out voltage and maintain the ability as a current source with high capacities. Terminal capacitors are proportional to transistor dimensions. Therefore, the increases in pass element size influence the frequency response of regular uncompensated LDO by jeopardizing its stability. Therefore, frequency response becomes an important characteristic of a LDO, especially of a closed-loop system.

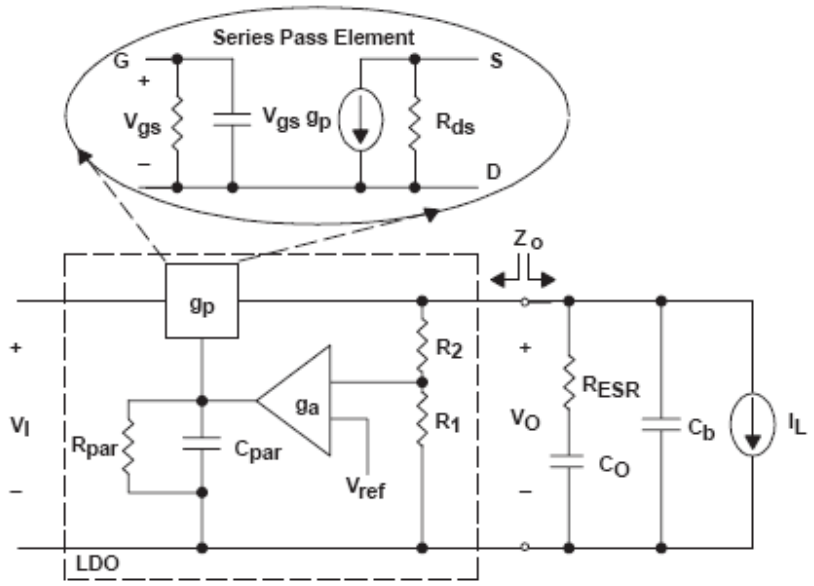

Fig. 4 AC model of a linear regulator

In this section, a typical frequency response analysis of a basic uncompensated LDO is presented [4]. Fig. 4 [4] shows a AC model of a typical LDO with essential elements. The error amplifier is modeled by a transconductor (g_a) with a load comprised of

capacitor C_{par} and resistor R_{par}. C_{par} is a function of the parasitic capacitance present at the gate of the pass element. The pass element is modeled by a small signal model with transconductance g_p. An output capacitor C_o with an equivalent series resistor (R_{ESR}) and a bypass capacitor C_b is added.

From Fig. 4, output impedance is given by

$$\begin{aligned} Z_o &= R_{12p} \,||\, (R_{ESR} + \frac{1}{SC_o}) \,||\, \frac{1}{SC_b} \\ &= \frac{R_{12p}(1 + SR_{ESR}C_o)}{S^2 R_{12p} R_{ESR} C_o C_b + S[(R_{12p} + R_{ESR})C_o + R_{12p}C_b] + 1} \end{aligned} \tag{1}$$

where $S = j\omega$, $R_{12p} = R_{ds} \,||\, (R_1 + R_2) \approx R_{ds}$, when $R_{ds} \ll (R_1 + R_2)$.

Typically, output capacitor value C_o is significantly larger than the bypass capacitor C_b. Therefore, output impedance could be approximated to

$$Z_o \approx \frac{R_{ds}(1 + SR_{ESR}C_o)}{[1 + S(R_{ds} + R_{ESR})C_o] \times [1 + S(R_{ds} \,||\, R_{ESR})C_b]} \tag{2}$$

Equation (2) carries partial frequency response information of a full open-loop gain transfer function. Zeros and poles can be found as follows:

$$P_o \approx \frac{1}{2\pi R_{ds} C_o} = \frac{I_L}{2\pi V_A C_o} \tag{3}$$

$$P_b \approx \frac{1}{2\pi R_{ESR} C_b} \tag{4}$$

$$P_a \approx \frac{1}{2\pi R_{par} C_{par}} \tag{5}$$

$$Z_{ESR} \approx \frac{1}{2\pi R_{ESR} C_o} \tag{6}$$

where $R_{ds} \approx \frac{V_A}{I_L}$, $V_A = \frac{1}{\lambda}$ for MOS devices. λ is the channel-length modulation parameter.

Fig. 5 [4] shows the typical pole-zero locations on a Bode plot.

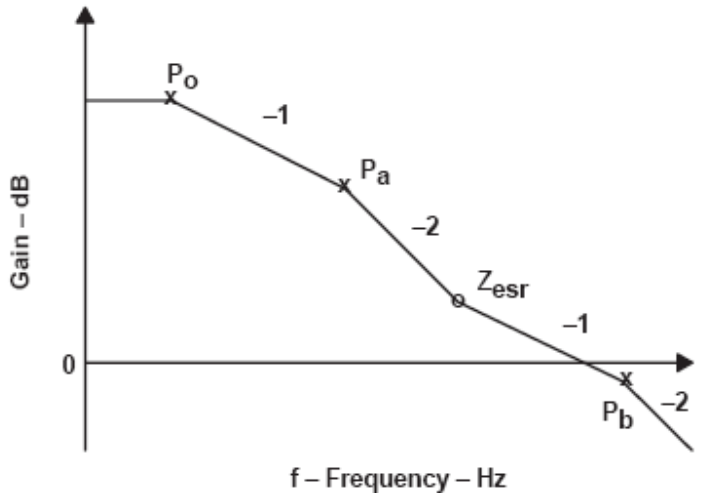

Fig. 5 Frequency response of the LDO voltage regulator

Pole P_a is an additional pole from the internal of the LDO, the input of the pass device, as opposed to other poles and zeros are from the output of the device. Pole P_o position is highly dependant on the load current condition, according to equation (3). In addition, equation (3) is derived under the assumption that $R_{ds} \ll (R_1 + R_2)$, which is true when

load current is at its relatively high level. In the tested design, the maximum current allowed is 50mA, resulting in R_{ds} at hundred ohms level. However, when load current is at its relatively low level, a few μA, $R_{12p} = R_{ds} \,||\, (R_1 + R_2) \approx R_1 + R_2$, which is $250k\Omega$ in the tested design. Therefore, the large variation in the resistance value is responsible for a large movement of the pole [5].

Pole P_a is also subjected to change according to load condition. The parasitic capacitance at the gate of the pass element is dependant of the size of the PMOS. The movement of this pole is contributed by the gate to drain capacitance (C_{GD}). Although C_{GD} is relatively small compared to gate to source capacitance, the current dependant gain variation of enormous pass element will indeed make C_{GD} a critical part of the pole movement [5].

LDO compensation schemes

From the previous section, it is shown that there are two dominant poles before unity gain frequency. The lower dominant pole is determined by load conditions, and the higher dominant pole is determined by LDO internal elements. Generally, to guarantee stability, the system must have enough phase margin, which is that, at unity gain frequency (UGF), the phase shift of the open-loop system should be less than -180 degrees. The bigger the phase margin, the more stable a system is.

One way to achieve stability is to introduce a zero before UGF. A common scheme is to use load capacitor with an equivalent series resistor (ESR) to generate the zero to gain stability. *ESR compensation* is very broadly used by the microelectronic industry in current LDOs. However, with ESR compensation, it requires a capacitor with a well defined ESR value, which is costly sometimes. Therefore, it gives the motivation for *Design Feedback Loop (DFL) compensation*, where the dependency of ESR value of output capacitor is minimized. DFL introduces a feedback signal from output node into the error amplifier to achieve stability, by splitting the existing poles apart, instead of introducing a zero to the system.

ESR scheme

ESR generated zero's location is dependant on the ESR and load capacitor value, according to equation (6). For most ESR LDO, a maximum and minimum ESR value exists:

1) ESR has to be low enough so that the third pole P_b is above UGF due to the compensation. According to equation (7), P_b is also determined by the ESR value.
2) ESR has to be high enough to compensate one pole's gain roll off so that the gain slope is -20dB/decade when crossing UGF.

Due to the ESR value limitation, most of LDO manufactures provide a graph showing the range of ESR values. Fig. 6 shows an ESR range with respect to load current [4].

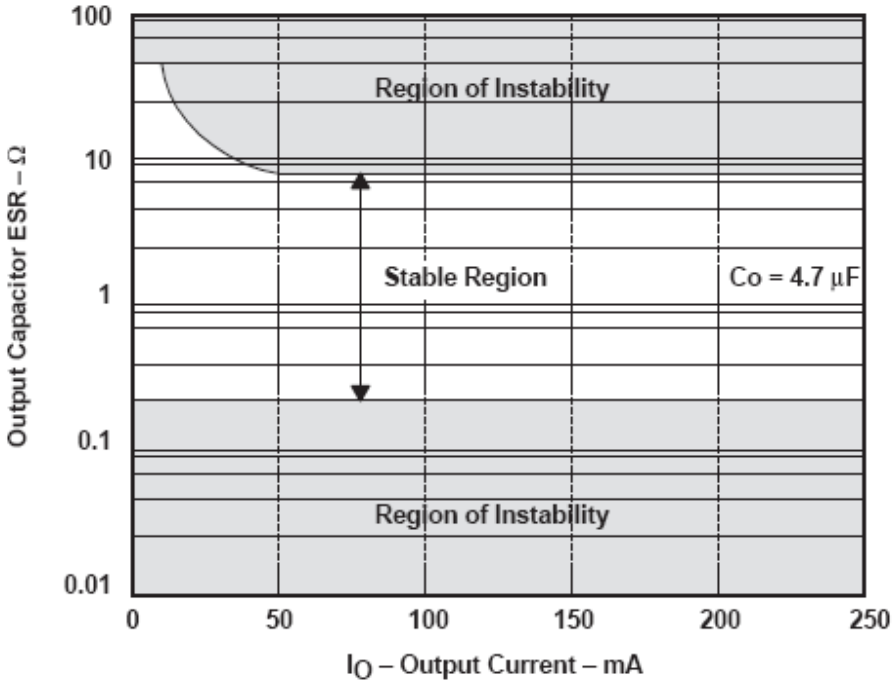

Fig. 6 Range of stable ESR values

DFL compensation scheme

This section will introduce the whole design logic and process of the DFL compensation scheme, from initial design motivations and concerns to the final design.

Design Motivation

Different from ESR compensation scheme, DFL is aiming to eliminate the pole/zero dependency on the ESR value of the output capacitor. Instead of introducing an additional zero to cancel one pole effect, design concept is to separate the existing poles further apart to gain higher phase margin, in order to get stability. Fig. 5 is used to further illustrate the concepts. Since ESR effect will be limited to minimum, the zero that is contributed by ESR will be moved up to very high frequency, outside the range of

interest. Therefore, the system is left with one dominant pole and two non-dominant poles. The goal of the compensation is to move the dominant pole to lower frequency, while moving the second non-dominant pole to higher frequency. Therefore, ideally, there will only be one pole effect on the system before it reaches unity-gain frequency (UGF).

Miller effect in compensation

In order to achieve the separation of poles, it is necessary to use a capacitor feedback. On chip capacitor values are relatively small to achieve desired pole separation, in order to save chip area. Therefore, Miller Effect provides the proper capacitance amplification that is needed. Miller Effect is the modification to the capacitor's value stems from the voltage gain across the capacitor.

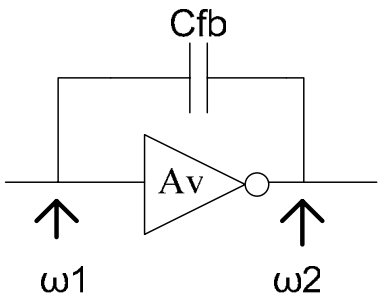

Fig. 7 Single stage amplifier with feedback capacitor

For the ease of explaining the design process, a single stage amplifier is used to represent the system, as shown in Fig. 7. The amplifier gain is Av, with a feedback

capacitor C_{fb} connected across the input and the output of the amplifier. According to Miller Effect by looking into the amplifier input, it is found that the equivalent capacitance of the circuit is $(1+A_v)C_{fb}$. The resistance value at the input node remains the same. The change in capacitance value changes the time constant, therefore, the location of the pole ω_1.

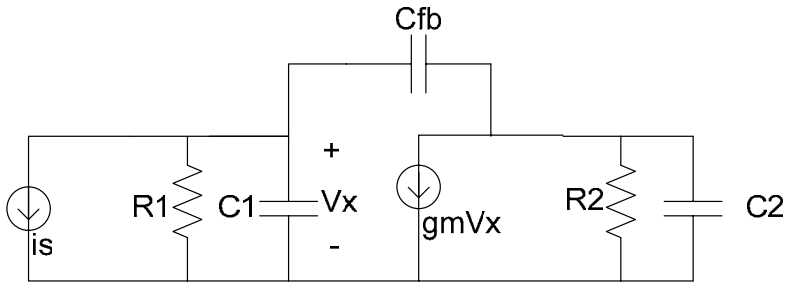

Fig. 8 Small-signal equivalent circuit o f a single stage amplifier

In order to examine the splitting of poles mathematically, small-signal equivalent circuit is used to derive the expression of the poles, Fig. 8. The dominant pole is represented as ω_1, and the non-dominant pole is shown as ω_2, Fig. 7.

Assuming reasonable parameter values, the following approximated expressions for the poles could be found:

$$\omega_1 \simeq \frac{1}{g_m R_1 R_2 C} \tag{7}$$

$$\omega_2 \simeq \frac{g_m C}{C_2 C_1 + C(C_2 + C_1)} \tag{8}$$

$$C = (1 + A_v)C_{fb} \tag{9}$$

since $C \gg C_1, C_2$, ω_2 can be further approximated:

$$\omega_2 \simeq \frac{g_m}{C_1 + C_2} \tag{10}$$

when $C_{fb} = 0$, in other words, when there is no feedback capacitor, the poles of the single stage amplifier are:

$$\omega_1 = \frac{1}{R_1 C_1} \tag{11}$$

$$\omega_2 = \frac{1}{R_2 C_2} \tag{12}$$

Pole splitting is shown by comparing (7) with (11), (10) with (12). The poles' movement is illustrated in Fig. 9.

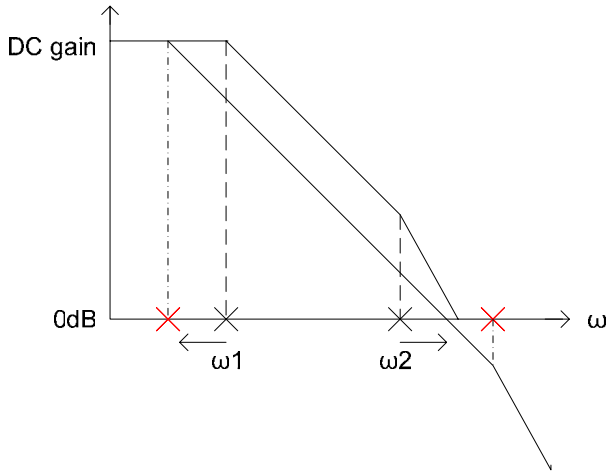

Fig. 9 Pole splitting due to miller compensation

From Fig. 9, with pole splitting, at UGF, there is only one pole effect, which ensures at least 45 degree phase margin for the system. However, the previous derivation and analysis ignores an extra zero effect, which could be detrimental to the system stability, because the zero is located at right-hand plane (RHP) of the s-plane:

$$z = \frac{g_m}{C} \tag{13}$$

Usually, the RHP zero frequency is between dominant and non-dominant pole, which will decrease the phase with the same effect of a pole. Therefore, even though when reaching UGF, there will be only one pole effect on Bode plot, and phase plot will have the effect of three poles, which could possibly result in negative phase margin.

To compensate this undesired zero effect when using capacitor feedback, a buffer amplifier is considered to be used in series with capacitor in the feedback path to

eliminate the feed-forward signal, which results in the creation of the zero. This concept leads to the DFL scheme.

DFL scheme

As shown in Fig. 10, the compensation path involves the derivative of the output state. Any transient change at the output will be fed back to the error amplifier before the A-D path, which enables DFL to exhibit a faster transient response than ESR.

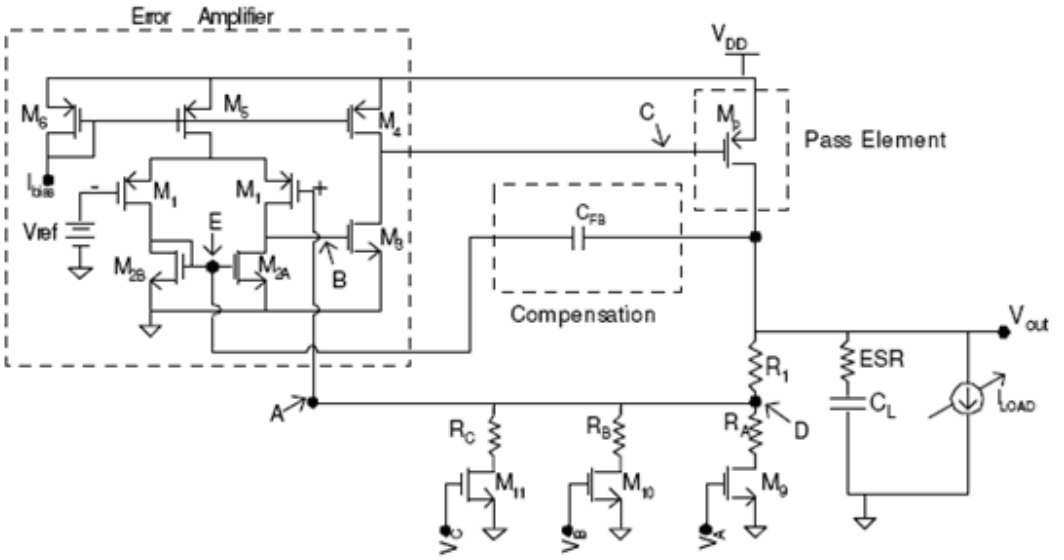

Fig. 10 Designed feedback loop schematic

It appears that a single capacitor serves as the compensation path. However, the differential pair amplifier serves as the buffer amplifier, as shown in Fig. 11. A feedback capacitor, combined with error amplifier transistors, transform output voltage signal into a current signal into the error amplifier.

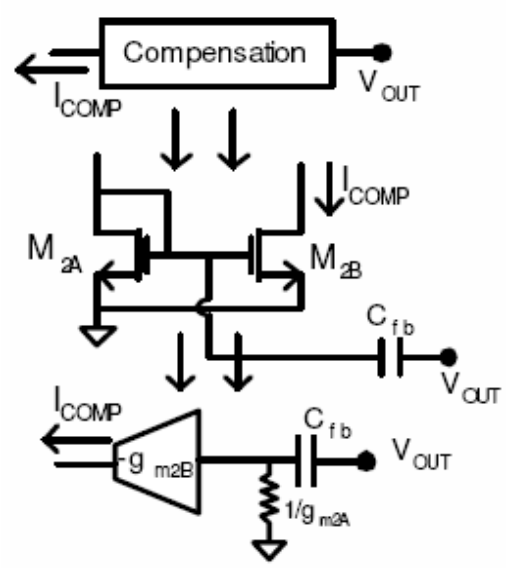

Fig. 11 Compensation path for DFL scheme

The small signal model of this compensation path can be modeled as shown in the Fig. 11. It is assumed that there is not body effect and channel length modulation, e.g. $V_A \to \infty$ and $\lambda = 0$. Diode connected nMOS, M_{2A}, can be modeled as a resistor of value $\frac{1}{g_m}$. The transfer function using small signal model could be expressed as:

$$TF_{comp} = \frac{I_{comp}}{V_{out}} = -\frac{g_m SC_{fb}}{g_m + SC_{fb}} \tag{14}$$

The compensation feedback path contributes a zero at DC frequency and a parasitic pole to the system, in addition to the changes made to the existing system. The parasitic pole is located at (8).

$$p_{fb} = \frac{g_m}{2\pi \cdot C_{fb}} \tag{15}$$

For keeping the original system stable, the added parasitic pole needs to be above a certain frequency. In the design, pole location constraint is selected to be greater than 1MHz. Thus, a minimum value for C_{fb} is required. The value for g_m could be determined in CADENCE simulation, as 67.15μ. Minimum value for C_{fb} is calculated:

$$C_{fb} \geq \frac{g_m}{2\pi \cdot p_{fb}} \Rightarrow C_{fb} \geq 10\,pF \tag{16}$$

When DFL is connected to the uncompensated LDO, the transfer function of the compensated circuit will be [5]:

$$TF_{c2} = \frac{-g_{m_1} H_{1C2} H_{2C2} H_{3C2} H_4}{1 + H_{fbC2} H_{1C2} H_{2C2} H_{3C2}} \tag{17}$$

$$H_{1C2} = \frac{R_P}{(R_P C_P)s + 1} \tag{18}$$

$$H_{2C2} = \frac{-g_{m3} R_A}{R_A (C_{GATE} + R_{PAR} g_{mp} C_{GD} + C_{GD})s + 1} \tag{19}$$

$$H_{3C2} = \frac{-g_{mp}(C_{fb}C_L(\frac{R_{ESR}R_{PAR}}{g_{m2}})s^2 + (C_L R_{PAR} R_{ESR} + \frac{C_{fb}R_{PAR}}{g_{m2}})s + R_{PAR})}{(C_{fb}C_L \frac{R_{ESR}}{g_{m2}} + C_{fb}C_L \frac{R_{PAR}}{g_{m2}} + C_{fb}C_L R_{ESR} R_{PAR})s^2 + (C_L R_{ESR} + \frac{C_{fb}}{g_{m2}} + C_L R_{PAR} + C_{fb} R_{PAR})s + 1} \tag{20}$$

$$H_4 = \frac{R_2}{R_1 + R_2} \tag{21}$$

$$H_{fbC2} = \frac{-g_{m2} C_{fb} s}{C_{fb} s + g_{m2}} \tag{22}$$

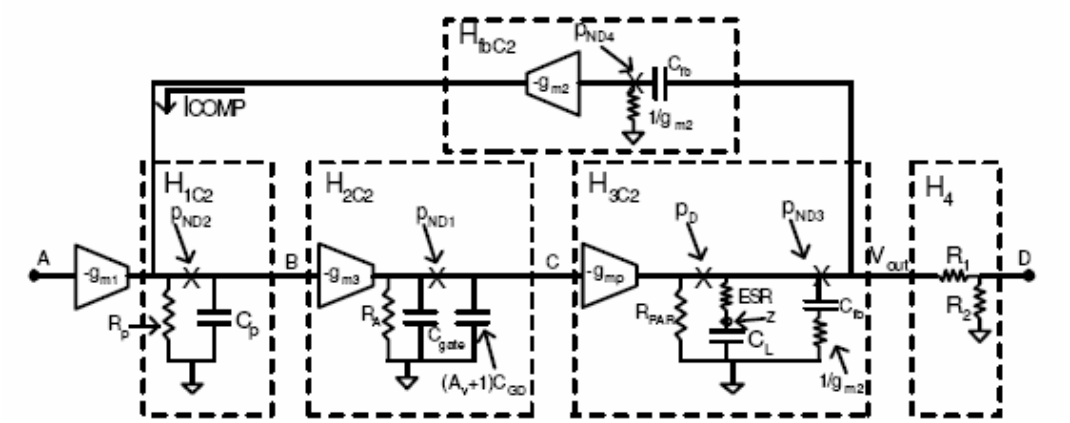

Fig. 12 Overall block diagram for DFL circuit [5]

From (20), it is shown that nominator polynomial has all positive coefficients. Therefore, for second order polynomial with all positive coefficients, real parts of the roots will be negative, which means the zeros of the system will be in left-half plane of the s-plane. System has no less than 50 degrees phase margin to ensure the stability [5]. For more simulation confirmation, please refer to [5].

CHAPTER II

METHODS

The goal of this research is to test and compare the two LDO compensation schemes described in the previous chapter, ESR and DFL schemes. The tested chip is fabricated in a standard 0.35μm CMOS technology, using a DIP40 package. There are four different LDOs on the chip, however only two were tested in this research.

The chip was tested under the same load and DC bias setup for each LDO. A detailed description of printed circuit board setup is included in this chapter. Transient response reflects a system's frequency performance. Line regulation, load regulation and power supply rejection ratio are basic LDO performance parameters regarding system's transient response. Testing parameters studied in this chapter were used in the research to test the LDOs for analysis and comparison.

Testing parameters

A list of LDO parameters are explained in detailed in this chapter. The parameters serve as the characterization guideline for testing and comparing different LDO performances. PMOS LDO will be used as an example to help explain the parameters.

Dropout voltage

Dropout voltage is the minimum voltage difference between input and output nodes when LDO is able to regulate at the designed output value. The dropout voltage will

vary slightly according to the loading conditions. A typical maximum load condition dropout voltage will be examined for comparison. Lower dropout voltage shows a better power efficiency.

Transient response

Since LDO will be subject to variation from input and load condition, transient response will show how a closed-loop system responses to those variations. There are a number of parameters need to be considered: Deflection voltage, Maximum transient voltage variation, response time, full load settling time, some of which are illustrated in Fig. 13 [5].

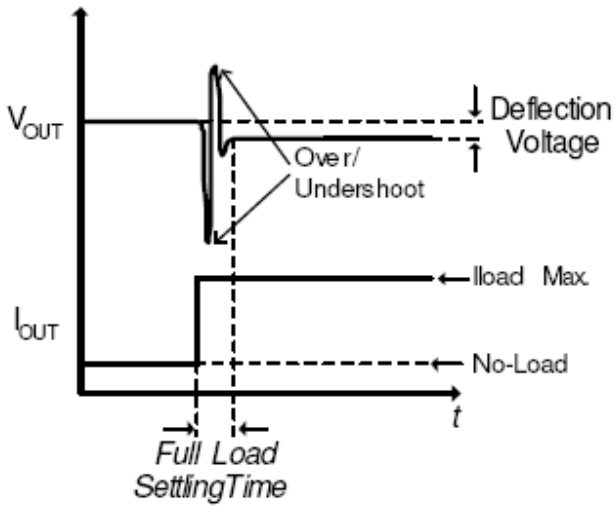

Fig. 13 Transient response characteristics

Deflection voltage is the difference of output voltages when high and low load current conditions are applied. Over/Under shoot voltage denotes the maximum transient voltage

variation. Response time is the time elapsed after output voltage reaches over/under shoot voltage till the output voltage starts to rise up, which is not indicated on the figure. Full load settling time is the time it takes for a system to reach within 1% of its designed voltage from no-load to a selected load condition.

Maximum transient voltage variation is defined as follows [6]:

$$\Delta V_{tr,\max} = \frac{I_{O,MAX}}{C_O + C_b}\Delta t_1 + \Delta V_{ESR} \tag{23}$$

where Δt_1 corresponds to the closed loop bandwidth of an LDO regulator. ΔV_{ESR} is the voltage variation resulting from the presence of the ESR of the output capacitor. The application determines how small this value should be [6].

In the experiment, a worst case scenario was considered that a change at output from zero to maximum load current was applied. A current step function was generated at the output to examine the output variations, and corresponding parameters were measured.

Line regulation

Line regulation is a measure of a system's ability to regulate the output voltage under a varying input voltage. Line regulation is defined as:

$$\text{Line Regulation} = \frac{\Delta V_O}{\Delta V_i} \tag{24}$$

In the experiment, a step change of input voltage was applied to examine the change in the output voltage. Line regulation is a steady-state parameter. Both positive and

negative variations at LDO's output will occur, because the input voltage might fluctuate around the designed value.

Load regulation

Load regulation is a measure of system's ability to regulate the output voltage under a varying load condition. Load regulation is defined as:

$$\text{Load Regulation} = \frac{\Delta V_O}{\Delta I_O} \tag{25}$$

The same experiment setup as transient response was used for load regulation. However, load regulation is a steady-state parameter like line regulation.

Power supply rejection ratio (PSRR)

PSRR, also known as ripple rejection, is a measure of a system's ability to suppress the ripple caused by the variation at the input voltage. The same expression as line regulation is applied to PSRR, except that PSRR is a frequency dependant parameter, instead of a steady-state parameter.

$$PSRR = \frac{V_{O,ripple}}{V_{i,ripple}} \tag{26}$$

A full frequency spectrum was examined with respect to PSRR value. DC/DC SMPS is the most common used supply for LDO. SMPS output noise is in the range of 100 kHz to 1 MHz, making this frequency bandwidth of special interest in testing LDOs.

Printed circuit board design

To experimentally test the LDOs, the circuit schematic shown in Fig. 14 is used for PCB board. The circuit provides the DC bias voltage and bias current that LDO needs to operate in the designed condition.

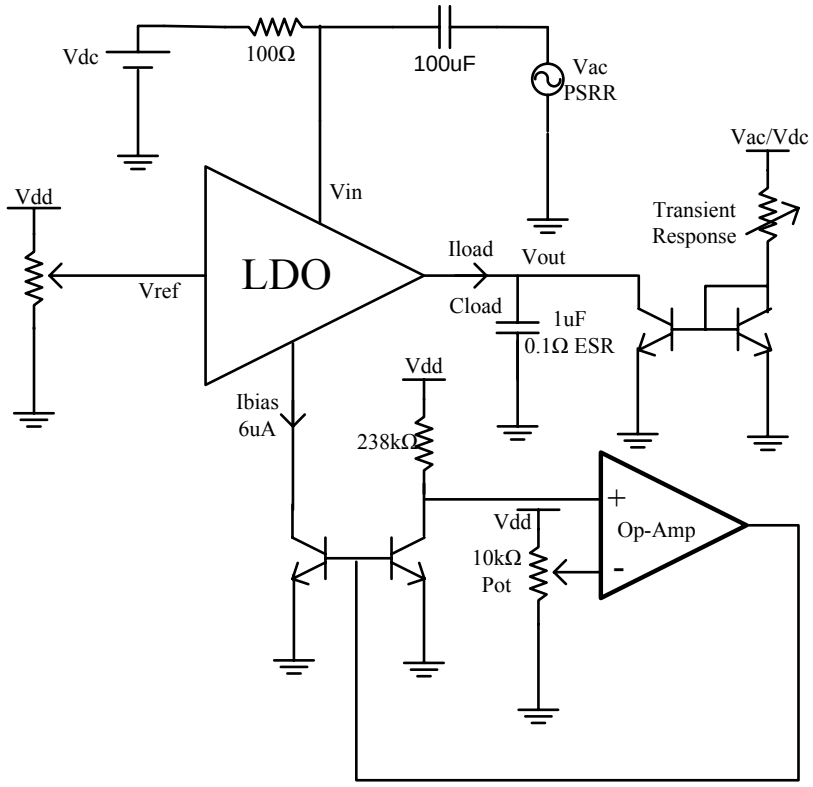

Fig. 14 Test circuit board schematic

In addition, input voltage signal path and output load path are designed to realize different parameters testing. This section consists of five parts regarding the circuit design, e.g. V_{dd}, V_{ref}, V_{in}, V_{out}, and I_{bias}.

V_{dd}

In order to provide low noise voltage signals for various circuit components, TPS79230 linear voltage regulator from Texas Instruments is used. The regulated output voltage is 3V. Input for the TPS79230 is 5V.

V_{ref}

V_{ref} is the reference voltage to the error amplifier inside LDO. Normally, V_{ref} is provided by a band-gap voltage reference, which provides low voltage, enough accuracy and thermal stability required for LDO. However, in the tested chip, V_{ref} is provided by an external voltage divider. A $10\,k\Omega$ potentiometer is connected to V_{dd}. In the experiment, potentiometer was adjusted to provide the designed V_{ref} value, 200mV.

V_{in}

V_{in} provides the power for LDO to operate. For LDO operation, a constant DC input voltage is supplied. In the experiment, V_{in} needs to be greater than 2V, since V_{out} is 1.8V and the minimum dropout voltage is 200mV. In the line regulation test, a sinusoid noise signal needs to be added at the input, while maintaining the V_{dc} supply.

V_{in} path includes both DC and AC signals. A 10 ohm resistor is put in series with the DC signal to avoid AC signal being grounded in AC mode. In DC, AC signal will be blocked by the large capacitor.

V_{out}

A bypass capacitor and loads are connected to the output of the LDO. A bypass capacitor is required for any LDO to operate. In this experiment, a low ESR value capacitor is used. The $1\mu F$ capacitor has a $0.1\,\Omega$ ESR value. In order to simulate the load condition, a current mirror XN02501 is used. A $10\,k\Omega$ potentiometer is used as the adjustable reference current, to generate the load current variation. The threshold voltage of the current mirror BJT is 0.7V. Therefore, an explicit relationship between potentiometer value and load current is:

$$I_{load} = \frac{V_{dc} - V_{th}}{R_{pot}} \tag{27}$$

where V_{dc} is 5V, and V_{th} is 0.7V in the experiment.

I_{bias}

A bias current is needed for the proper operation of the error amplifier in the LDO. In the tested chip, the bias current is 6uA. An operational amplifier and a current mirror are used to provide a steady bias current. In the design, with a resistor of value 238k, voltage value at the negative input of op-amp is calculated to be 1.57V, using Ohm's Law. Therefore, the voltage at the positive input of op-amp is 1.57V as well.

CHAPTER III

RESULTS

In this chapter, experimental results are presented along with CADENCE simulation results for both ESR and DFL compensation schemes. The test circuit board was built using the schematic mentioned in the previous chapter.

Without loss of generality, one programmable output, 1.8V, was chosen to be tested in this research. The same tests were applied under the same specifications for both ESR and DFL schemes for comparison. Both schemes were tested under the following parameters, discussed in the previous chapter: transient response, line regulation, load regulation, PSRR.

Transient response

A square-wave AC voltage signal was supplied at the output current mirror load, generating a load current variation of 0-50mA, green traces in Fig. 15 and Fig. 16. The yellow traces in Fig. 15 and Fig. 16, shows the transient response of the system. In both figures, y axis is voltage on a scale of 2.00V/div, and x axis is time on a scale of 100us/div. After some initial oscillation, the output voltage reached a steady level, which confirms that the system is stable.

Some measurements, shown in Table I, were taken for further comparison between two schemes. The absolute values of the measurements are larger than the simulation value. The discrepancy might be caused by numerous factors, including DIP package pin interference, PCB copper line interference and signal generator's noise.

TABLE I
TRANSIENT RESPONSE PARAMETERS

	ESR	DFL
Deflection Voltage (mV)	50	112
Settling Time (uS)	82	92
Undershoot (mV)	130	550

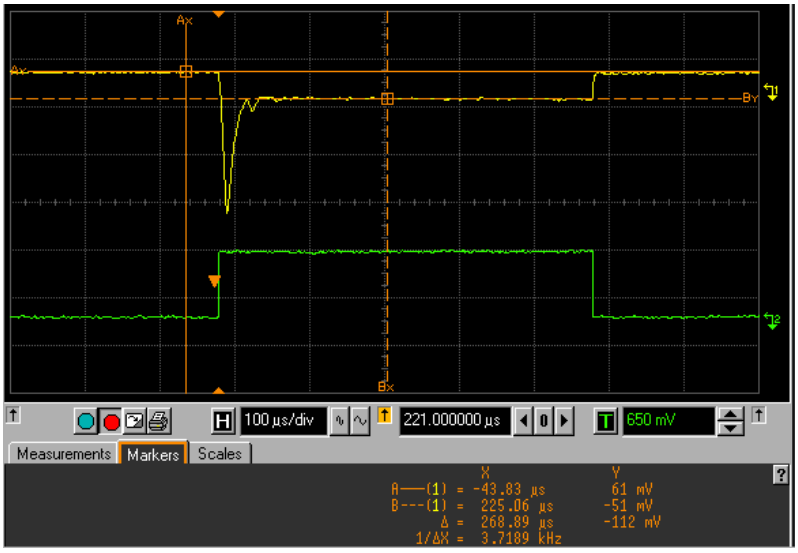

Fig. 15 Transient response of DFL scheme

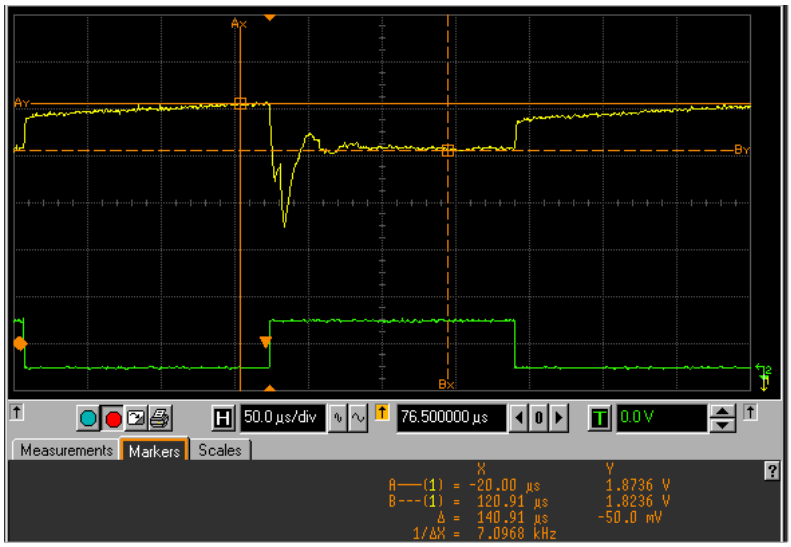

Fig. 16 Transient response of ESR scheme

Fig. 17 [5], shows the simulated transient response for ESR and DFL schemes as a reference to the experimental results.

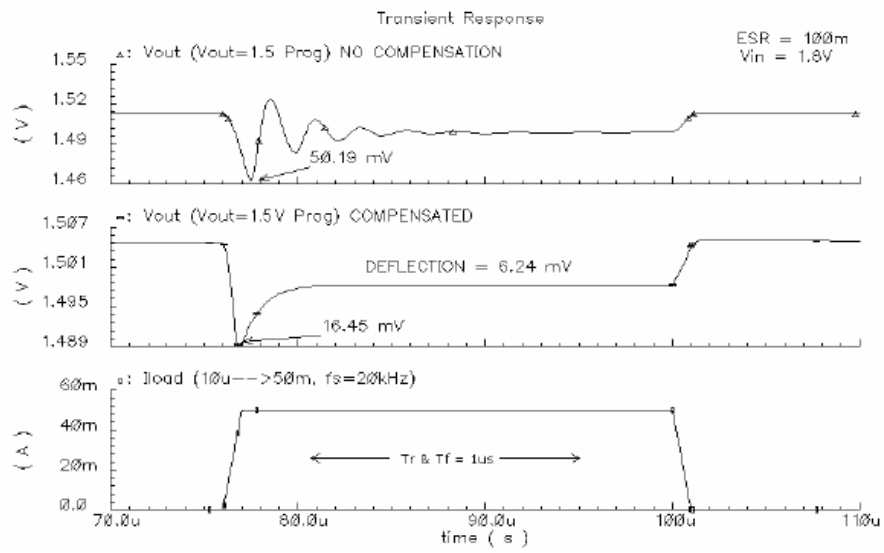

Fig. 17 Simulated transient response for ESR and DFL schemes

Line regulation

A constant-amplitude, ΔV_i, sinusoidal noise signal was generated at V_{in} AC signal path, while V_{in} DC signal was swept from 2V to 3V. The amplitude of the sinusoidal component of the output voltage signal, ΔV_o, was measured, and equation (24) was used to calculate the line regulation.

Fig. 18 and Fig. 19 show the line regulation vs. input DC voltage for DFL and ESR schemes. DFL line regulation stays in the range of 3-6mV/V when input DC voltage varies from 2V to 2.7V, which is close to the simulation value, 5.5mV/V, shown in Fig. 20 [5]. ESR scheme has a poor performance on line regulation.

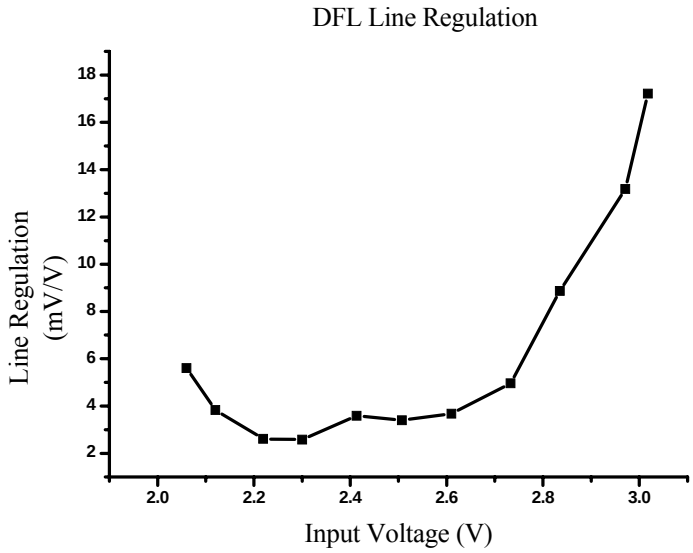

Fig. 18 Line regulation for DFL scheme

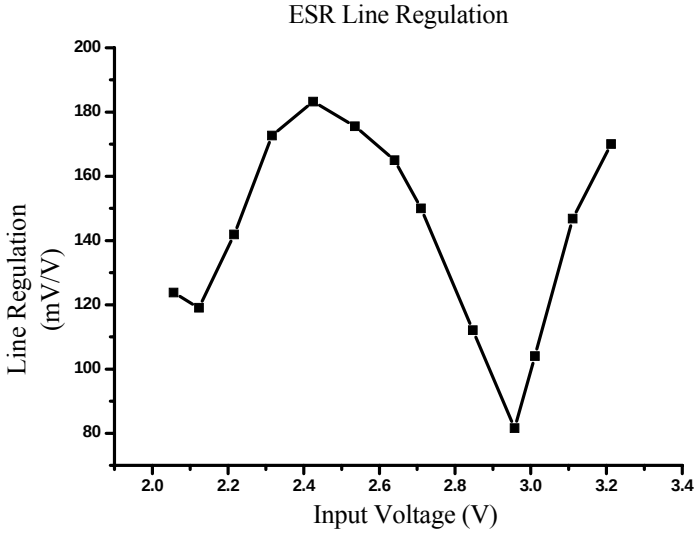

Fig. 19 Line regulation for ESR scheme

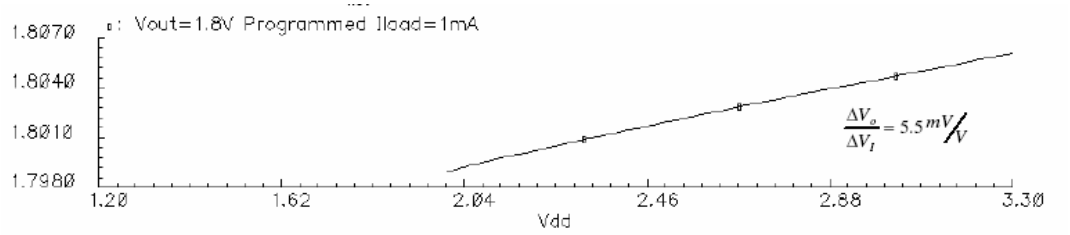

Fig. 20 Simulated line regulation DFL scheme

Load regulation

Testing setup is similar to transient response test. DC voltage was supplied at the output current mirror load. DC voltage was varied to change the load current from 0mA to 50mA. The corresponding output voltage was read when load current was at a constant value, since the load regulation is a steady-state parameter.

Fig. 21 and Fig. 22 show the load regulation vs. load current for DFL and ESR schemes. It is shown that when load current is above 20mA, the output voltage experiences a significant drop, which is undesired feature of a LDO. Fig. 23 [5] shows the simulated PSRR for DFL scheme.

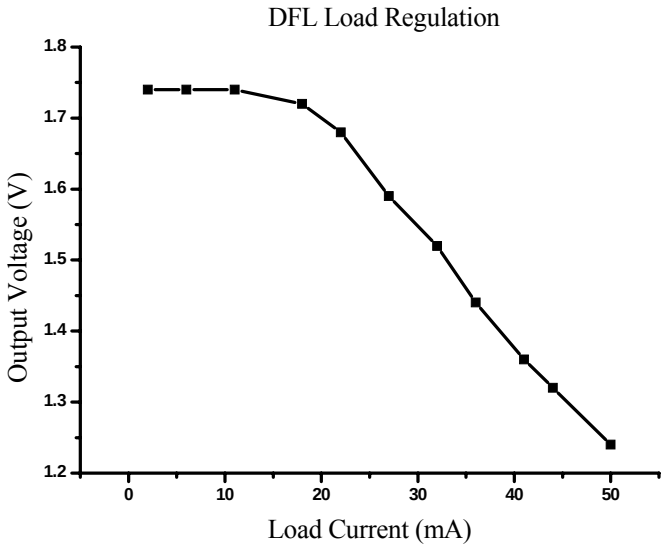

Fig. 21 Load regulation for DFL scheme

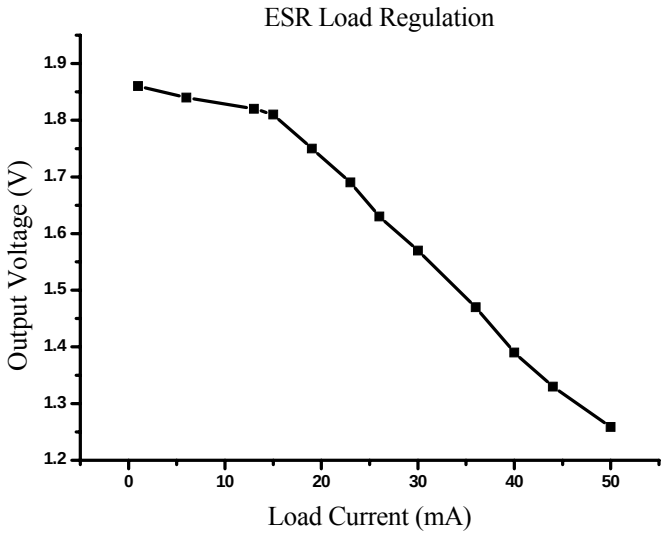

Fig. 22 Load regulation for ESR

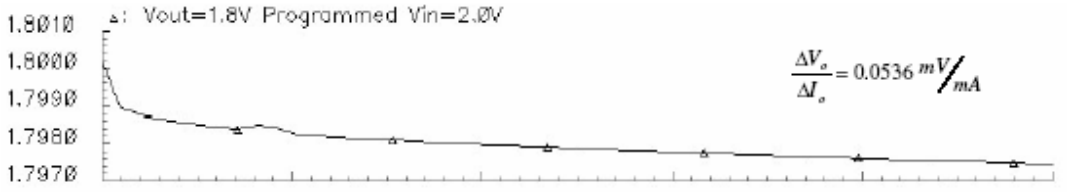

Fig. 23 Simulated load regulation for DFL scheme

PSRR

Testing setup is similar to line regulation. AC sinusoidal noise signal was generated at V_{in}. DC input voltage was kept constant through out the test. AC noise signal frequency was swept to examine the PSRR from 100Hz to 10MHz.

Fig. 24 and Fig. 25 show the PSRR vs. Frequency for DFL and ESR schemes. Both schemes exhibit lower than -20dB PSRR within the frequency range. Fig. 26 [5] shows the simulated result for DFL scheme. Under normal operation conditions, PSSR is lower than -40dB up to 100kHz frequency.

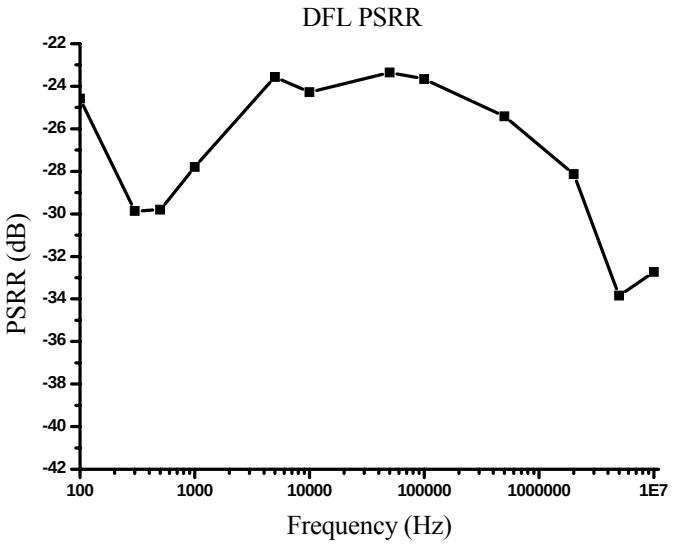

Fig. 24 PSRR for DFL scheme

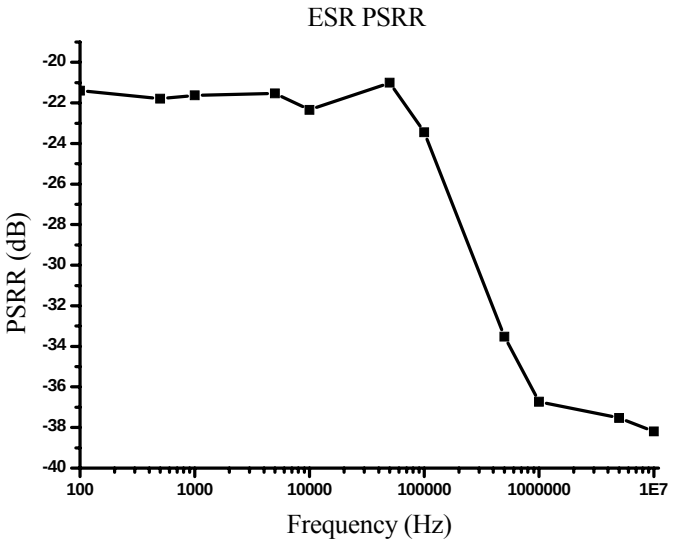

Fig. 25 PSRR for ESR scheme

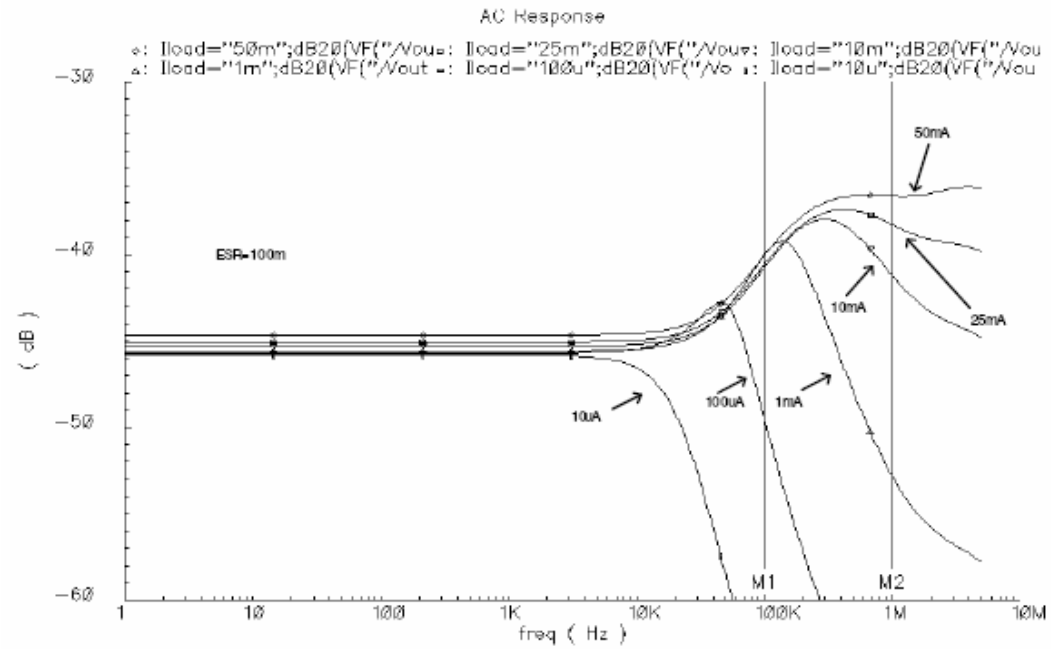

Fig. 26 Simulated PSRR for DFL scheme

CHAPTER IV

CONCLUSIONS AND FUTURE WORKS

The analysis of the DFL and ESR compensation schemes and the experimental testing results of both schemes performance are presented in this thesis. Experimental results show that DFL and ESR schemes have comparable performance. The work in this thesis serves as a complementary role to [5]. It is confirmed that DFL compensation design achieves the stability and transient performance as designed.

Some discrepancies exist between the experimental results and the simulation results. Further work could be done to test the chip with an alternative PCB schematic and re-examine the testing chip layout.

REFERENCES

[1] P. K. T. Sai Kit Lau; Ka Nang Leung; Mok, "Analysis of low-dropout regulator topologies for low-voltage regulation," *IEEE Conference on Electron Devices and Solid-State Circuits,* pp. 379- 382, 16-18 Dec. 2003.

[2] C. Simpson, "Linear and switching voltage regulator fundamentals," National Semiconductor Corporation, Santa Clara, CA, USA, 1995.

[3] Texas Instruments, "Fundamental theory of PMOS low-dropout voltage regulators," Texas Instruments Inc., SLVA068, Dallas, TX, USA, April 1999.

[4] Texas Instruments, "Technical review of low dropout voltage regulator operation and performance," Texas Instruments Inc, SLVA072, Dallas, TX, USA, August 1999.

[5] A. I. Ohlmaier, "Design of programmable, low power, low dropout regulators for portable applications," M.S. thesis, Elect. Comp. Eng. Dept., Texas A&M University, College Station, TX, 2005.

[6] Texas Instruments, "Understanding the terms and definitions of LDO voltage regulators," Texas Instrument Inc., SLVA079, Dallas, TX, USA, October 1999.

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