DESIGN OF PROGRAMMABLE, LOW POWER, LOW DROPOUT REGULATORS FOR PORTABLE APPLICATIONS

A Thesis

by

ABRAHAM ISLAS OHLMAIER

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

December 2005

Major Subject: Electrical Engineering

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Aproved by:

Chair of Committee,	Jose Silva-Martinez
Committee Members,	Aydin Karsilayan
	Karen L. Butler-Purry
	Rainer Fink
Head of Department,	Costas Georghiades

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ABSTRACT

Design of Programmable, Low Power,

Low Dropout Regulators for Portable Applications.

(December 2005)

Abraham Islas Ohlmaier, B.S., Texas A&M University

Chair of Advisory Committee: Dr. Jose Silva-Martinez

As portable electronics constantly find their way into the hands of eager consumers, the demands placed on these products and their circuits are ever increasing. More features and more performance are continuously demanded by consumers. This feature-driven market has brought with it several constraints on the type of circuits utilized in developing these portable devices. Cell-Phones, PDA's, MP3 players and various other portable electronics require different voltage levels to power different architectures that realize the many features within the device.

This work demonstrates a technique to design Programmable Low Power Low Dropout Voltage Regulators (LDO). The LDO proposed in this research utilizes a fast-transient feedback loop in order to improve transient response and guarantee stability in all the programmable output levels. Specifically, the main parameters to be improved are stability over the entire load current range, reduced overshoot and undershoot variations in transient response, reduction of LDO deflection voltage, minimization of standby current and low voltage (Vin = 1.2V) operation.

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CHAPTER I

INTRODUCTION

Voltage regulators are found in nearly every electronic device today. They provide the DC voltage, usually assumed as constant, for all the electronic circuits used in modern day applications. These applications range from high-speed microprocessors to multi-function cell phones and PDA's. Each of these applications has specific requirements of their voltage supplies. Some require very low noise, while others require very high efficiency.

Voltage regulators can be designated into two major categories: Linear Voltage Regulators (LVR) and Switching Mode Power Converters (SMPC), each of which present advantages and disadvantages over the other [1]-[3]. SMPC's present higher efficiency; however, switching noise is generated and will superimpose onto the supply voltage and pass to the control circuits causing interference problems [1]. This switching noise makes the use of SMPC's restrictive in some of today's modern electronics, especially hand-held devices with communication features like cell-phones and PDA's.

An LVR can be considered the basic building block of nearly every power supply used in micro electronics [3]. Using basic Ohms law, V = I x R, a voltage (V) can be maintained constant by implementing a resistor (R) that varies to adjust for the changes in current (I) [4]. Maintaining the V in ohm's law constant, is the basic principle behind voltage regulators. A dynamically adjusting resistor is required to regulate the voltage. Linear voltage regulators convert a noisy input voltage into a very stable and clean supply voltage by implementing the dynamically changing resistor with their 'pass element' [4]. Generally, the output noise in commercially available LVR's is lower than that obtained in SMPC's.

This thesis follows the format of *IEEE Journal of Solid State Circuits.*

The focus of this work is to design a type of LVR called a Low Dropout Regulator (LDO). The LDO should be programmable to various output levels because in modern electronic devices different voltage levels are created from one single power supply [5].

1. Types of Linear Voltage Regulators

The basic linear regulator is shown, in general form, to operate as depicted in Fig. 1 [3].

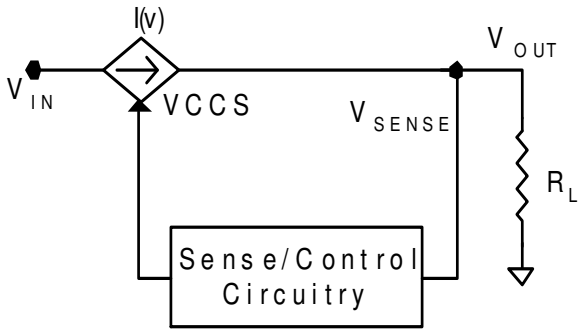


Fig. 1 Linear voltage regulator functional diagram.

The voltage controlled current source (VCCS) is adjusted according to load variations by the Sense/Control circuitry in order to maintain V_{OUT} at the programmed output level. The design limit of the current source will define the actual current the circuit can source and still maintain regulation [3]. From Fig. 1 it can be inferred that the VCCS characteristic actually resembles the operation of a transistor. How this VCCS is practically implemented is what distinguishes the different types of linear regulators in use today. V_{OUT} is controlled by the feedback loop that includes the Sense/Control block. Most linear regulators are self-compensated by this feedback path, but the LDO requires external components (i.e. a load capacitor from output node to ground) to achieve stability.

There are various kinds of linear regulator implementations, one of which is shown in Fig. 2. This type of linear regulator is called a 'Quasi-LDO Regulator' [3].

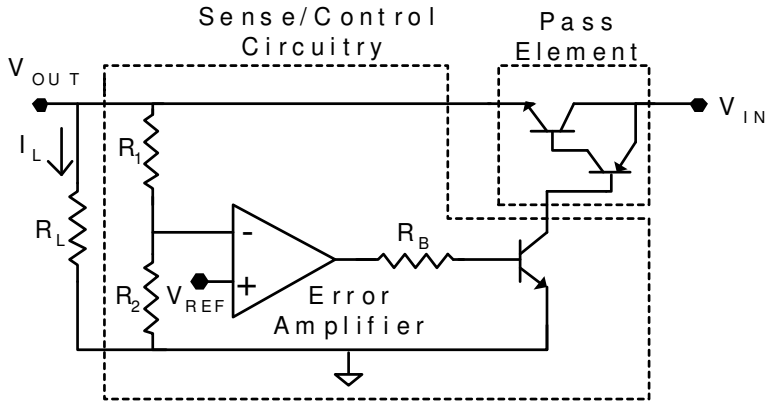


Fig. 2 Typical linear regulator.

The VCCS is now replaced by the 'pass element' as it carries out the task of sourcing current (I_L) required by the load. The pass element is controlled by the Sense/Control Circuitry. By replacing the pass element we can obtain three types of regulators as shown in Fig. 3 [3].

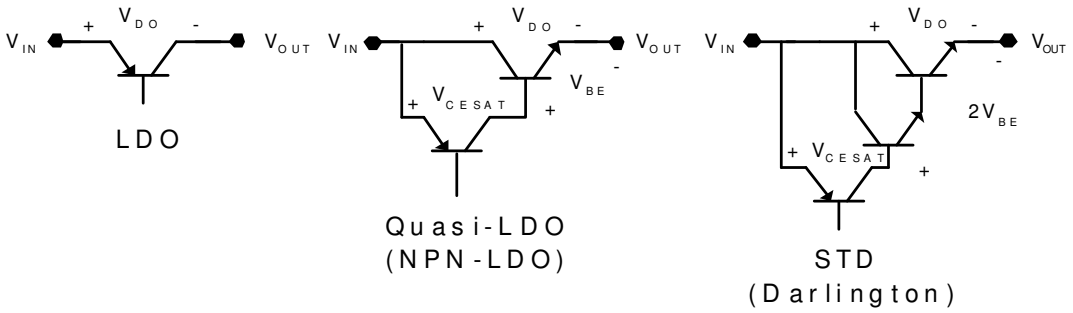


Fig. 3 Three types of pass elements.

When a simple PNP transistor is used as the pass element, the linear regulator is called an LDO (Low Dropout Regulator). The dropout refers to the voltage defined as the minimum voltage required across the LDO regulator pass element to maintain regulation. Therefore, the single PNP bi-polar transistor gives the smallest possible dropout voltage (1) of the three types of linear regulators shown in Fig. 3.

$$V_{DO} = V_{IN} - V_{OUT} = V_{CE} \tag{1}$$

Table I shows a comparison chart between the different dropout voltages in the three specific examples of regulators shown in Fig. 3.

TABLE I

LINEAR REGULATOR COMPARISON

Reg. Type	V_{DO}
LDO	V_{CESAT}
QUASI-LDO	$V_{BE}+V_{CESAT}$
STANDARD	$2V_{BE}+V_{CESAT}$

In battery operated devices, designers have continued to strive for lower supply voltages. Therefore, it is important that drop-out voltages be minimized to maximize the power efficiency within a given power supply voltage [6].

Table I shows that the LDO has the lowest drop-out voltage of the three types of linear regulators presented. This characteristic makes the LDO better suited for battery operated devices with low voltage operation.

2. CMOS LDO's

Cost and compatibility considerations, as well as power dissipation, have lead designers to look for LDO topologies that can be implemented using standard CMOS technologies. Instead of using a PNP BJT, a P-MOS device is substituted in as the 'pass element'. The sensing and control circuitry is also implemented with CMOS technology. Providing a fully CMOS solution makes the LDO compatible to implement on the actual die of larger designs. This brings further advantages to the LDO that turn out to become essential to battery-operated devices. Some of

these benefits are that lower ground current can be achieved, thus causing less current drain on the actual battery used to power the device. External LDO's are also bulky and expensive.

Quiescent, or ground current, is defined as:

$$I_Q = I_{IN} - I_{OUT} \tag{2}$$

This quiescent current consists of bias current and drive current for the series pass element [7]. Fig. 4 aids in illustrating the quiescent current advantage of using MOS devices to implement the LDO [7].

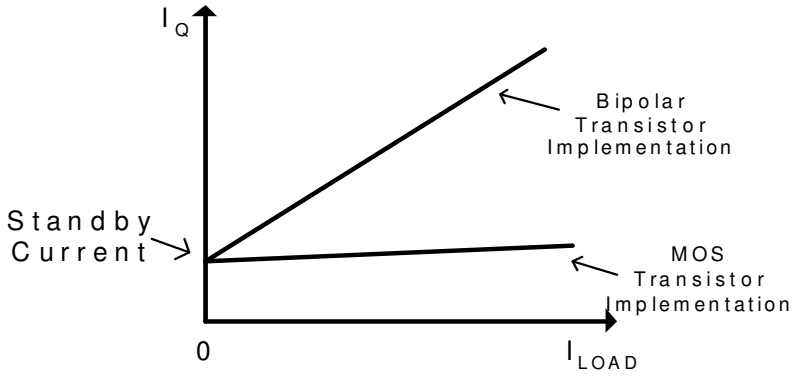


Fig. 4 Quiescent current vs. output current.

As shown in Fig. 4, the quiescent current for a MOS device shows little dependence on the load current. This is due to the fact that the MOS transistor drain-to-source current is a function of the gate to source voltage.

$$I_{DS} = \beta_{MOS}\left(V_{gs} - V_t\right)^2 \tag{3}$$

The MOS characteristic differs from the BJT because the collector current is a function of the base current, given by:

$$I_C = \beta_{BJT} I_B \rightarrow I_B = \frac{I_C}{\beta_{BJT}} \tag{4}$$

Therefore for a changing load current, essentially I_C for a BJT LDO or I_{DS} for a CMOS LDO, the BJT implementation will present an increase in base current according to (4) with respect to changing load current. The increment in base current increases the quiescent current, a very undesirable characteristic for portable applications.

Another characteristic that makes the CMOS LDO a better fit for battery-operated devices is the lower dropout voltage of around 200mV that can be achieved, as the P-MOS 'pass element' only requires a V_{DSSAT} to operate. The lower dropout voltage will maximize the efficiency as well as allowing lower voltage operation as shown in (5).

$$P = I_{LOAD} \cdot V_{DO} \tag{5}$$

3. LDO Application Examples

As previously mentioned, most of today's high end portable devices have multiple functions that range from wireless communication capabilities to larger memory. It is also known that each one of these characteristics requires different DC power levels to operate the circuits that implement these functions. For example, by looking at the typical GSM cell phone power distribution [8] shown in Table II, it is apparent that different voltages are required for the different blocks that carry out the different functions in the hand-set. In a typical GSM cell phone the LDO serves multiple purposes. Aside from their basic task of increasing battery life, they also isolate different subsystems from each other [8]. This is crucial in both the RF section and also between analog and analog/mixed signal circuits because interference can occur. The LDO provides a less costly solution, in both cost and area, when compared with the typical LC filters that are used in the supply lines of RF circuits. The LDO's PSRR is helpful in isolating the transient voltages of the battery from sensitive circuitry.

TABLE II

TYPICAL GSM 2ND GENERATION CELL PHONE POWER BUDGET [8]

	Avg. Current Consumption Talk Mode	Supply V	Avg. Current Consumption in Standby Mode
Subcircuit	**[mA]**	**[V]**	**[μA]**
Digital Base Band + Memory	19+6	1.8	300+40
Analog Baseband	9	2.5	150
SIM	1	2.8	60
RF	32	2.8	50
PA	200	Battery	770
PM(Housekeeping)	3	Battery	220
Misc. Other	5275	2.8	670
Total Current Consumption			2,260

The high current in a power amplifier, fed off the battery as shown in Table II, can cause a voltage transient of up to 0.5V due to the combined effect of the battery's ESR and protection circuitry [8]. This 0.5V transient spike can be highly detrimental to the rest of the circuits biased by this battery. In addition, lowering the voltage levels, as is the trend in todays and future portable devices, any transient spike of 0.5V would definitely cause major damage to any circuitry intended to operate with a voltage supply of 1.2V.

Another example of an application for LDO's is in hand-held products. Shown in Fig. 5 is the typical power management diagram for a 2G wireless hand-held, in the class of the Palm i705 [9].

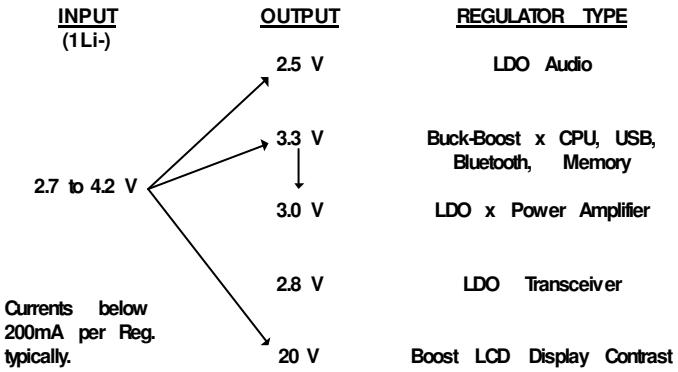


Fig. 5 Power management diagram for 2G wireless hand-held.

As shown in Table II and Fig. 5, there are different voltage levels required by the various system blocks. Different types of regulators accomplish these levels. Focusing on the number of LDO's present in the system, in this case 3, an advantage can be offered to overall system design if a single LDO offered programmability to supply the necessary voltage levels without major time consuming changes to its design.

This work concentrates on a CMOS LDO targeted for battery-powered applications. Any electronic device that has a variety of functions included in it will forcefully require various regulated DC voltage levels. With the push of many designers to increase battery life, the actual DC levels are getting lower as consumers demand more functions from their hand-held devices.

4. Thesis Organization

This thesis concentrates on the design of a CMOS Programmable LDO for use in portable applications, as has been previously stated. It is designed, simulated and laid out using a TSMC 0.35µm CMOS process available through the MOSIS service. This particular LDO addresses the issue of low voltage operation and programmability. This work presents the use of a robust compensation scheme that stabilizes the designed LDO for all 3 programmable output levels, within the specified load current range.

Chapter II shows the difficulties encountered in CMOS LDO design. The main issue concerning LDO design is stability. Various techniques are reported in the literature that solve this design concern. Two solutions, ESR compensation (most popular in industry) and a solution presented in [10] are described.

Chapter III presents the mathematical approach to the proposed phase compensation scheme. Described in this chapter are two different implementation of the proposed compensation scheme. The second of the two proposed implementations was developed after investigating possible improvements to implementation I.

Chapter IV presents the simulated results of both implementations. The results follow the performance metrics explained in Chapter II. Overall it is shown that both proposed implementations solve the stability issue, but it was found that implementation II, has lower power consumption as well as superior transient response.

Chapter V presents a detailed comparison of schematic and post-layout results for each of the performance metrics. It is shown in this chapter that schematic and post-layout results agree very closely with each other. Both proposed implementations are included in the integrated circuit that was submitted for fabrication.

Chapter VI is a compilation of the post-layout results. It presents a comparison between the performance metrics of each proposed implementation. This chapter offers further proof that implementation II is superior in post-layout simulations than implementation I of the proposed phase compensation scheme.

Chapter VII presents the experimental results obtained up to the date of development of this thesis. It proves that both implementations accomplish the main objective of increasing the phase margin and obtaining a superior transient response than an LDO without the compensation schemes.

Chapter VIII presents the concluding remarks. Two different implementation of a phase compensation scheme have been presented. The LDO's have been simulated to be stable within a 0-50mA load current range for all three programmable output levels (0.9V, 1.5V, 1.8V). These LDO implementations have all been designed to work with a 1μF ceramic load capacitor. The ability to work with a ceramic capacitor is advantageous due to cost and size considerations of bigger tantalum capacitors necessary in other solutions.

CHAPTER II

CMOS LDO

In this chapter the difficulties encountered in the design of a CMOS LDO will be explained. The performance metric definitions that are used in LDO characterization will also be presented.

1. LDO Design Concerns

The LDO has become the most popular type of linear regulator in use today. As previously discussed, different voltage levels are required by different circuits in modern electronic devices. With the various voltage supply levels required inside a single device, an LDO designed to provide them with minimal changes becomes increasingly worthwhile. By focusing on the CMOS LDO several system level necessities translate into LDO design difficulties. Particularly, the increase in efficiency translates to a larger pass element in order to reduce V_{DSSAT} (or V_{DO}) and maintain the current sourcing capability at relatively high capacities (50mA). The increase in pass element size influences the frequency response of the typical uncompensated LDO shown in Fig. 6 by jeopardizing its stability.

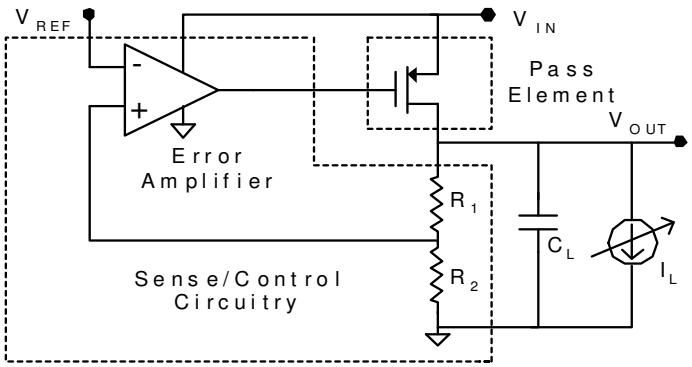


Fig. 6 Typical uncompensated CMOS LDO.

Stability is an important characteristic of any closed loop system. Therefore, in a CMOS LDO, stability is a major concern as it operates in closed loop. If the closed loop transfer function has one or more poles in the right hand plane, then any energy at these poles would cause oscillations with increasing amplitude. As the amplitude increases, then the right hand plane poles move onto the jω axis. The increase in amplitude causes the gain of the amplifying subsystems to drop due to large signal operation and a sustained oscillation will occur. Since oscillations are undesirable, it is important to make sure that there are no right hand plane poles in the system.

The root locus plot and Nyquist criteria [11] [12] show that it is possible to predict the closed loop frequency response of a system from the frequency response of the open loop transfer function. The open loop transfer function is found by breaking the loop of the system and introducing a voltage excitation in order to measure the transfer function as the excitation travels around the open loop. Fig. 7 shows the typical LDO with the loop breakpoint as well as the location of two low frequency poles.

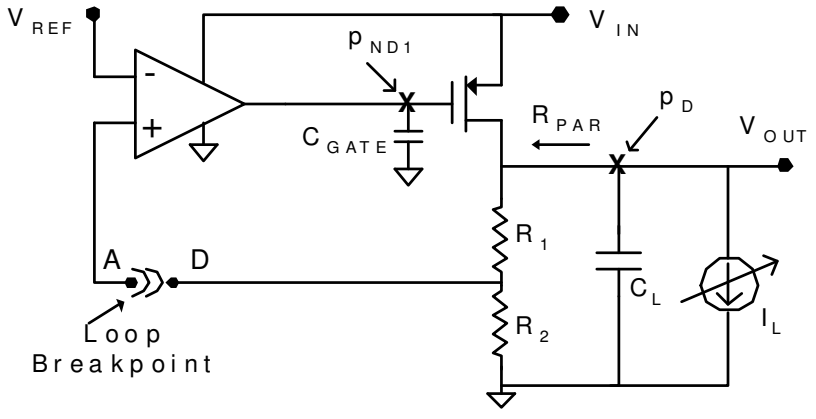


Fig. 7 Typical LDO open loop representation.

Bode analysis can then be applied to the open loop transfer function obtained from Fig. 7 to test the phase margin of the typical LDO. Phase margin is commonly defined as 180^0- $\phi(f)$ where $\phi(f)$ is the phase of the system when the magnitude of the transfer function is at 0dB gain (also recognized as the unity gain frequency, f_u). It is well known that most practical systems should have a minimum of 45º of phase margin to account for any phase degradation attributed to the non-linear nature of the gain stages within the system. Higher phase margin will result in faster settling times for transient operation.

The typical LDO open loop response can be approximated by a 2^{nd} order transfer function given as:

$$H(s) = \frac{A_0}{\left(1 + s/p_D\right)\left(1 + s/p_{ND1}\right)} \tag{6}$$

This transfer function has two poles that are directly related to the poles labeled in Fig. 7 and can be found at the output of system (p_D) and at the gate of pass transistor (p_{ND1}).

$$p_D \approx \frac{1}{2\pi \, \mathrm{R}_{\mathrm{PAR}} \, C_L} \tag{7}$$

$$p_{ND1} \approx \frac{1}{2\pi \, R_{\mathrm{A}} \left(\mathrm{C}_{\mathrm{GATE}} + R_{PAR} \, g_{mp} C_{GD} + C_{GD}\right)} \tag{8}$$

These poles follow the variations the pass element experiences when a change in load current is encountered because the output resistance of the LDO (R_{PAR}) is given by:

$$R_{PAR} = r_{DS} \| R_1 + R_2 \| R_L \tag{9}$$

The output impedance (R_{PAR}) follows variations in load because both R_L and r_{DS} are functions of the load current. The drain-to-source impedance (r_{DS}) of the PMOS pass element has a dependence on load current that is given by (10).

$$r_{DS} = \frac{1}{\lambda I_{DS}} \tag{10}$$

In (10), λ is an empirical constant and I_{DS} is the drain current of the PMOS pass device. The actual value of λ is process technology dependent but can be approximated between 0.2/V and 0.5/V in order to obtain a projection of the order of magnitude of the output impedance. The highest output impedance (R_{PAR}) is obtained when the load current is lowest, a few μA. At low current loads, R_{PAR} is dominated primarily by R_1+R_2 (R_1+R_2 = 250kΩ for the proposed designs). The lower limit for output impedance is encountered when the current load is at its highest. In the proposed design the maximum current rating is set to 50mA. Therefore, R_{PAR} is dominated by the parallel combination of R_L and r_{DS} and results in less than 10Ω for the proposed design. This large variation in output impedance is responsible for the large movement of the pole at the output of the LDO.

The variation of output impedance translates into movement of the dominant pole that is established at the output node. This movement can occur from a few hertz to the tens of kilohertz range. The 2nd low frequency pole is given by the size of the parasitic capacitance present at the gate of the pass element C_{GATE}. The movement of this pole can be attributed to a Miller effect encountered with the pass element's gate to drain capacitance. Although this C_{GD} is not physically large, the current dependant gain variation of the enormous pass element will indeed make C_{GD} a critical part of the 2nd pole movement as shown in (8). Fig. 8 shows the open loop bode plots with the general movements of both low frequency poles.

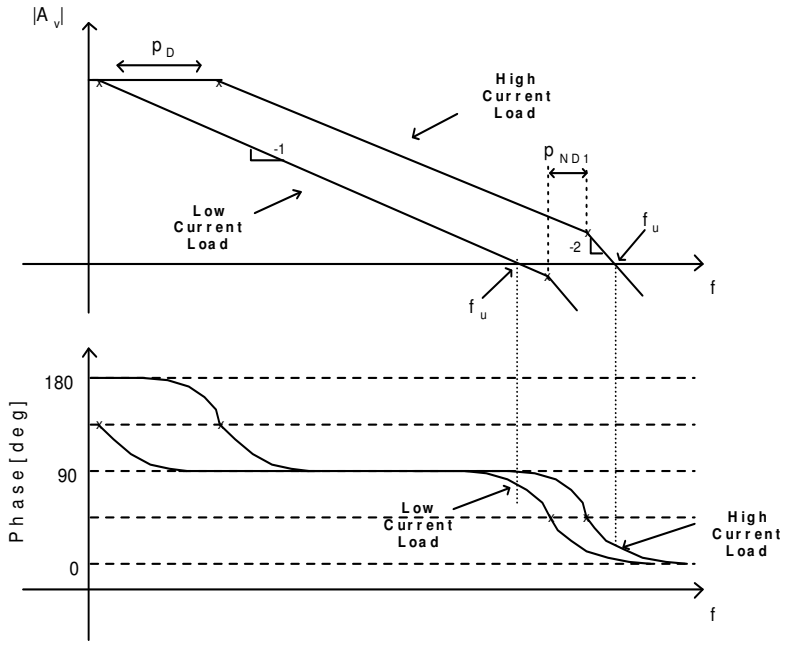


Fig. 8 Frequency response with varying load of typical LDO.

From Fig. 8 it is apparent that in the higher load current case the uncompensated typical LDO will have much less than 45º of phase margin. This problem then translates to unacceptable settling times (t_s<10μs for wireless applications) in the closed loop transient response of the system. In general, it can be concluded that the uncompensated LDO requires some modification in order to guarantee a sufficient phase margin that also improves the closed loop response.

2. LDO Compensation Techniques

Several solutions have been presented in available literature regarding the stability concern of LDO's [1], [6], [10], [13]-[17]. The majority of these solutions increase the power consumption of the LDO. For a battery operated system, with already tight power budgets, this characteristic is detrimental. Nevertheless, some examples on how to compensate for the stability issues are summarized in the following descriptions.

The most common type of LDO commercially available today is one that utilizes the ESR (Electro-Static Resistance) of the output capacitor as a zero generating element in order to

compensate the phase loss of one of the two low frequency poles encountered. Fig. 9 shows the typical LDO with the two low frequency poles, a 3rd pole (p_{ND2}) at relatively higher frequencies, and the zero used for compensation marked where they occur. The 3rd pole (pND2) is added in order to establish a more realistic system in which the gate capacitance of the error amplifier could potentially bring the pole at that node close to the band of operation of the system. By placing a zero in the open loop transfer function, the phase effect of one of the two low frequency poles will be cancelled and will effectively compensate for the phase margin loss.

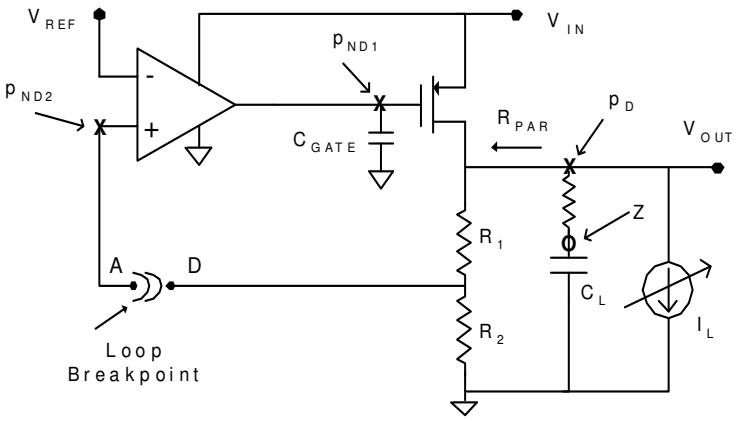


Fig. 9 Typical LDO with ESR compensation.

The magnitude response will change according to the added zero as shown in Fig. 10. The new zero will cause the magnitude plot to drop at a rate of 20dB/dec instead of at 40dB/dec after the effect of the two poles. This correlates directly to the phase plot, where the system will present a phase recovery as is shown in the phase response of Fig. 10. It is also shown that without compensation the LDO would undoubtedly drop below the 45º of phase margin which is considered the minimum.

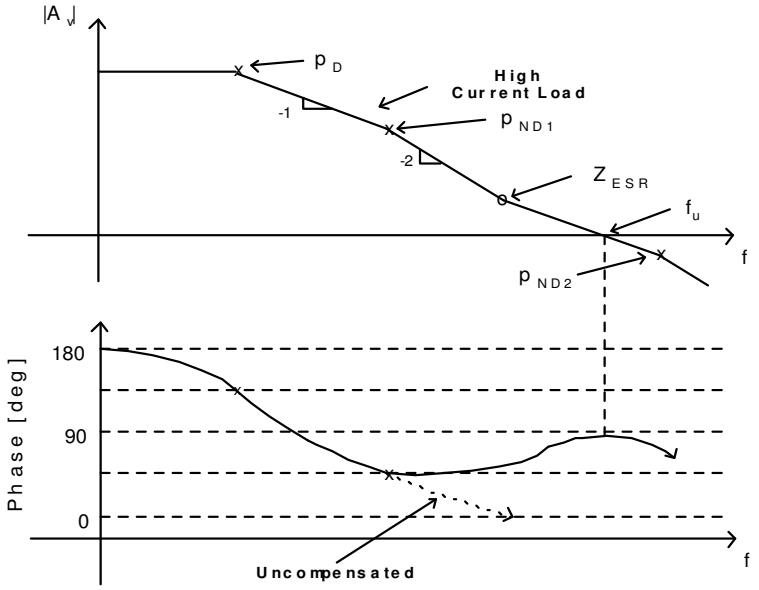


Fig. 10 Frequency response with varying load of typical LDO compensated with ESR.

The main issue with this technique is that in order to accomplish a zero at the proper frequency the load capacitor value must be large (2.2µF-4.7µF) and the ESR value must be within a given range. Manufacturers [18] [19] usually present a predetermined output capacitor value along with an ESR value for which their LDO is guaranteed stable. Fig. 11 shows the stable region characteristic for the Texas Instruments Inc. TPS763XX family of LDO's [18].

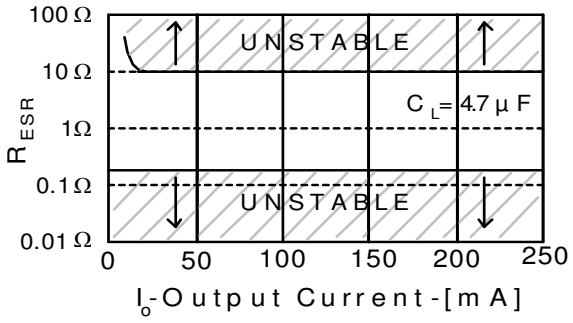


Fig. 11 Stable ESR values for TPS763XX family of LDO's.

A few important conclusions can be drawn by observing Fig. 11. First of all, the designer must have good control of the ESR value. Secondly, the only commercially available capacitors with high capacitance value (i.e 4.7μF) and relatively high ESR values are tantalum. Tantalum capacitors are more expensive when directly compared to the same value and voltage rating of a ceramic capacitor. Even though the ESR obtainable is higher than with ceramic capacitors, the actual value of the capacitance will also be higher, therefore implying larger package size, an undesirable trait for hand-held products. By observing these conclusions, it is apparent that a design with a smaller ceramic output capacitor (i.e. < 4.7μF) with lower dependence on ESR is necessary for portable applications.

A design that eliminates the dependence on ESR for compensation is presented in [10]. The LDO presented in that work uses an output capacitor of 2.2μF and presents independence from the ESR of the load capacitor. Fig. 12 shows the overall implementation of this technique.

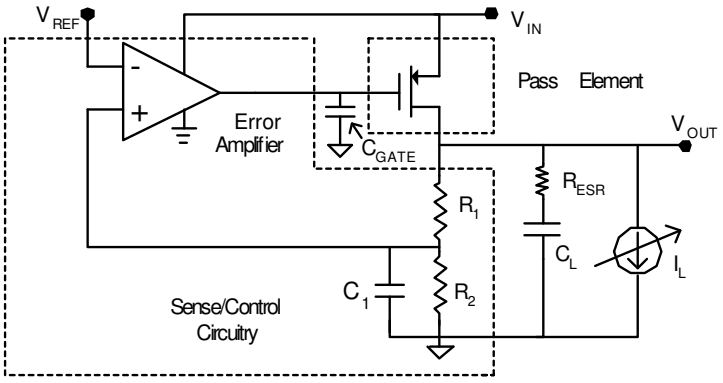


Fig. 12 LDO compensation technique presented in [10].

This implementation generates C_1 by multiplying a small on chip capacitor to a large value using a VCCS (Voltage Controlled Current Source) that will create the necessary zero and stabilize the LDO. While this technique indeed accomplishes the goal of stabilizing the LDO and eliminating

the dependence on the ESR value, the implementation of C_1 utilizes more power due to the requirement of biasing for the VCCS. Also, low voltage operation (V_{IN}=1.2V), is not attainable using this technique, therefore a direct application of this topology is not plausible to solve the low voltage and programmability concerns.

3. LDO Performance Metric Definitions.

Most of the commercial LDO's, and those reported in the literature [1], [6], [10], [13]-[17], use a specific set of performance metrics to characterize their performance. In this section each metric is explained individually. All the measurements obtained in this work follow these performance metrics.

A. AC Performance

The AC performance is mainly characterized by the phase margin test. It is required, like in most systems, that the open loop phase margin stay above 45º throughout the complete current load range. This metric will be tested by breaking the loop at a convenient point, as shown in the following chapter, and obtaining the Bode plots of the resultant transfer function.

B. Dropout Voltage

As previously explained the dropout voltage is the minimum voltage drop across the input and output terminals of the LDO with which the system is able to regulate. Some reported works show a dropout voltage anywhere from 232mV [6] to 200mV [15] measured at the maximum load current. This work will present a target dropout voltage of 200mV at its maximum load current.

C. Transient Response

In real world operation the LDO operates in closed loop with the input at the source end of the pass transistor, and one output at the drain of the pass transistor. It is required that it adapt dynamically to changes in load current and regulate the desired voltage level regardless of those

changes, just like an ideal current source. Full-load transient settling time, deflection voltage, maximum over/undershoot and startup time are all characteristics extracted from an LDO's response to stepped output loads. Fig. 13 shows the definition of each of these transient parameters except for startup time.

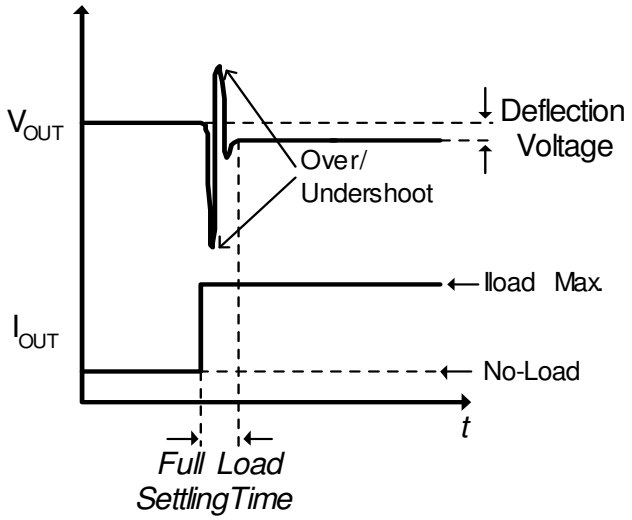


Fig. 13 Transient response characteristics.

Full load transient settling time is the measure of how fast the regulator can settle to within 1% of its steady state final value. The load is varied from no load to max load current in order to obtain this parameter. Reported in the literature is a 1% full load settling times of less than 1μs [15]. The deflection voltage is defined as the difference between the steady state final values for V_{OUT} of high and low current load cycles. The maximum over and undershoots are shown in Fig. 13 to be the maximum peak of the output waveform during the load transition phase. The startup time is defined as the time it takes the system to accurately regulate the output voltage level at a selected load current. These metrics are all measured using a known value of C_L and a given output voltage level.

D. Output Noise

The output noise voltage is usually reported as the RMS output noise voltage over a specified frequency band (10Hz to 100kHz) under the conditions of a defined output voltage, a ripple free input voltage and constant load current.

E. Load Regulation

Load regulation is the ability of the regulator to maintain the desired output voltage with any changes in load current. Load regulation can be measured by changing the load current and measuring the changes in output voltage. An expression for load regulation is shown as follows:

$$Load\ Regulation \equiv \frac{\Delta V_o}{\Delta I_o} \tag{11}$$

F. Line Regulation

Line regulation is the ability of the circuit to maintain the specified output voltage without any effects from variations in input voltage. Line regulation can be measured by giving the supply voltage a short pulse and verifying the robustness of the circuit to this pulse. Line regulation can also be expressed as:

$$Line\ Regulation \equiv \frac{\Delta V_o}{\Delta V_I} \tag{12}$$

G. PSRR

Power supply rejection ratio (PSRR), also known as ripple rejection, is the measure of the circuit's ability to maintain a regulated output voltage regardless of input voltage variations. It can be expressed by the same expression (12) that governs line regulation, except that it is a small signal parameter at a particular frequency.

When a dc/dc switch mode power supply (SMPS) is used to power the LDO, as is sometimes the case, the output ripple of the SMPS is within the frequency band of 100kHz to 1MHz, making this frequency band-interval of specific interest [18]. The switching power

supply will undoubtedly introduce variations of the input voltage with frequency content at the specified band, therefore PSRR becomes critical. An example of a PSRR reported is -26dB at 1.5Voutput [15].

H. Power Consumption/Ground Current

The ground current, also specified as quiescent, is the difference between input and output currents. Bias currents (Error-Amp, Band-Gap Reference, and Feedback Resistors) and the gate drive current of the pass element that do not contribute to the output power, constitute the ground current. Low ground current must be achieved in order to maximize the current efficiency as it is measured at no current load conditions. In this work a maximum ground current consumption of 60μA is targeted.

Overall this chapter demonstrates the main design issues encountered by LDO's. Even though programmability and low power operation are targeted, they cannot be addressed without the issue of phase degradation, as it may lead to system instability. The main performance metrics used by LDO manufacturers are defined as well in this chapter in order to establish the guidelines of how the proposed work will be characterized.

CHAPTER III

DESCRIPTION OF PHASE COMPENSATION IMPLEMENTATIONS

In this chapter, a mathematical description is carried out on a typical LDO as well as the proposed implementations that, as will be shown, improve phase margin performance. Included in this chapter are three sections that describe each one of the LDO's mathematical approximation and design.

1. Typical LDO

A. Mathematical Model and Design

A model for a typical LDO is developed in order to analyze the system mathematically and understand where changes can be made in order to accomplish a guaranteed stable system over the desired range of programmable outputs. Fig. 14 shows the conversion of the typical LDO to its mathematical approximation. Note that the error amplifier is modeled as a two-stage one-pole system. The benefits of selecting this topology will become more apparent in the following sections.

To represent the LDO in block diagram form the AC path was followed around the loop and a break-point was placed between nodes A and D in order to allow Bode analysis on this network. As shown in Fig. 14, for CADENCE simulation purposes, a large inductor was placed at the break point keeping the dc operating point of that node intact, and a large capacitor is used to inject the AC signal. The configuration for frequency analysis is now given by the loop with an input point at node A and the output point at node D.

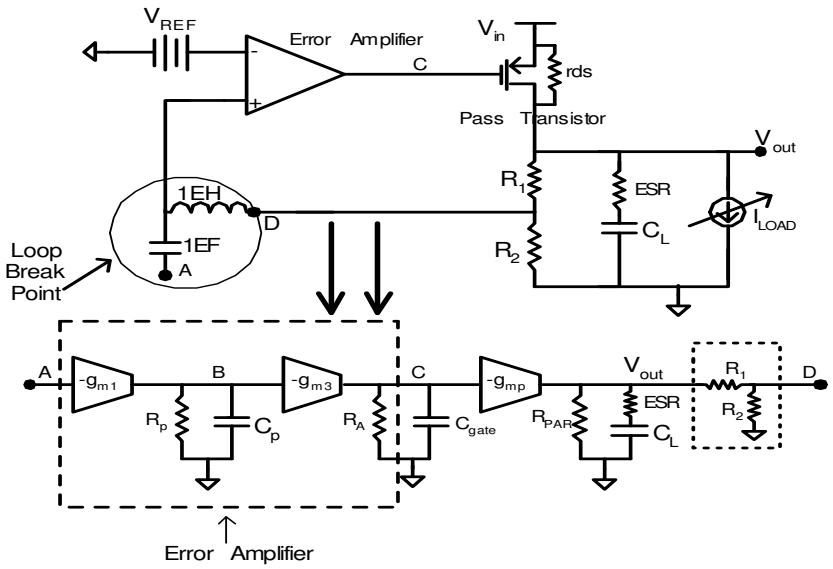


Fig. 14 Block diagram representation of typical LDO.

As previously explained, the LDO functions in a closed loop environment (i.e connecting nodes A and D together and by making $V_{IN}=V_{DD}$) but the open loop must prove to have enough phase margin (PM>45º) to guarantee stability [19]. Frequency analysis by means of bode plots will give a good initial comparison to validate the mathematical model vs. CADENCE simulations.

An important characteristic that requires careful analysis is that of the dropout voltage. As was previously discussed, this work presents a CMOS LDO with a PMOS transistor used as the pass element. This allows for lower dropout voltage, a required characteristic in LDO design. On the other hand, using a PMOS does not come without its complications. It is important to analyze the implications of targeting a $V_{DROPOUT}$ of, at most, 200mV.

In order to achieve this specification the following design procedure was carried out on the pass element. By setting $V_{DROPOUT} = V_{DSSATPass}$ and obtaining the appropriate electrical parameter values for the TSMC 0.35µm technology ($\mu_p Cox = 65.4\mu A/V^2$), as well as setting the maximum current that this transistor must supply as $I_{LOAD} = 50mA$, the following procedure is evaluated:

$$V_{DROPUT} = 200mV \Rightarrow V_{DSSATPass} \leq 200mV \tag{13}$$

Or,

$$I_D = \frac{1}{2}\mu_P Cox\left(\frac{W}{L}\right)(V_{DSATPass})^2 \Rightarrow \left(\frac{W}{L}\right) = \frac{2 \cdot I_D}{\mu_P Cox \cdot (V_{DSATPass})^2} \tag{14}$$

By using the selected technology parameters, (2) yields the following results:

$$\left(\frac{W}{L}\right) = 40{,}000 \Rightarrow W = 16mm \;\&\; L = 400nm \tag{15}$$

It is evident that with the resultant dimensions, found in (15), the capacitance of the pass transistor will play an important and limiting role in the AC response of the overall system. Fig. 15 shows the lumped elements modeled at both the input and output of the pass element.

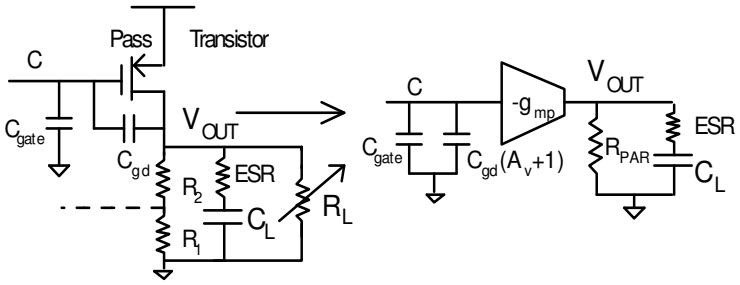


Fig. 15 Pass transistor equivalent model.

Observing Fig. 15, it is readily apparent that a Miller effect will be encountered due the large absolute value of the voltage gain ($|A_v| = g_{mp}R_{PAR}$). This gain will vary according to load condition and is shown in Table III. These values were obtained using a CADENCE simulation of the conditions stated in Table III with the dimensions stated in (15) for the pass transistor.

TABLE III

PASS TRANSISTOR GAIN WITH VARYING LOAD

I_{LOAD}	g_{mpass}[A/V^2]	R_{PAR} [Ω]	A_v [V/V]
10µA	461.7µ	59.04kΩ	27.26
1mA	22.47m	1.48kΩ	33.26
50mA	410.2m	32.9Ω	13.5

Table III indicates that the gain of the pass element will requires careful attention on the miller effect present at the gate-drain interface of the device due to the large dc gain variation.

For initial calculations of the capacitances between the terminals of the pass transistor, it is assumed as an initial approximation that the device is in saturation. As shown in Fig.15, C_{GS} and C_{GD} are considered the dominant and relevant capacitances for this device. C_{GS} can be approximated by (16):

$$C_{GS} = \frac{2}{3} \cdot W \cdot L \cdot Cox + W \cdot L_D \cdot Cox \tag{16}$$

L_D is the overlap gate to source region and its effect can be neglected as it is much smaller than length of the actual device (L = 400nm). Therefore, C_{GS} can be approximated as shown (17) for initial calculations.

$$C_{GS} \cong \frac{2}{3} \cdot W \cdot L \cdot Cox \tag{17}$$

Investigating the behavior of C_{GD}, it is found that the opposite will occur. When the device is in saturation, the drain and gate are electrically isolated due to channel pinch-off effects [20]. This could lead to an erroneous belief that C_{GD} disappears, when in fact it is dominated by the overlap capacitance between the gate and the drain. A zoomed in cross-section of a saturated p-mos transistor is shown in Fig. 16 to help illustrate this point. As can be seen, the channel is pinched off at saturation and C_{GD} can be approximated as being made up of solely the overlap capacitance shown.

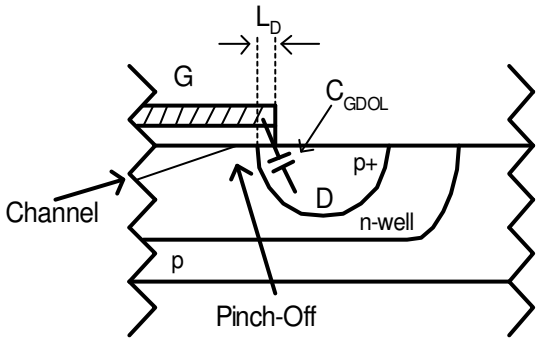


Fig. 16 Saturated p-MOS cross-section.

Therefore, C_{GD} can now be approximated, for initial calculations by (18):

$$C_{GD} \cong L_D \cdot W \cdot Cox \tag{18}$$

As can be seen in (17) and (18), these expressions do not account for changing V_G, as is the case for this application because for varying I_{LOAD}, the system will regulate the necessary V_G so that the pass transistor sources the required current. When the pass transistor is simulated in CADENCE for varying I_{LOAD} the C_{GD} varies according to V_G and the gate to drain capacitor is in the hundreds of femto-farad range. Considering this fact and the amount of gain in the pass transistor section it is impossible ignore C_{GD} and the effects on frequency response of the open loop.

For the error amplifier a two stage single ended design was used. As was mentioned before, the selection of this topology benefits the proposed implementation as will be shown in the following sections. There were some considerations taken into account when designing the error amplifier as well. The main issues related to the error amplifier are the following:

- High DC gain to guarantee high loop gain over the range of loads (A_v>60dB).
- Low output impedance for higher frequency pole created with C_{GS} of pass trans.
- Internal poles must be kept at high frequencies, preferably > f_u of the system (1MHz).
- Must operate at low input dc levels, V_{REF}=200mV.

- Must operate with a minimum V_{DD} = 1.2V.
- Low DC current consumption.
- Low Noise.

From these requirements two things are automatically established. One of them is that due to the need for the inputs to operate at low voltage, a p-mos differential pair is selected. This also benefits the noise performance as p-mos transistors have inherently less flicker noise than n-mos [21]. Secondly, by noting that the LDO is required to operate with a minimum input of 1.2V, any cascoding is ruled out. Following the requirement for low output impedance a common source stage is cascaded to output of the differential pair [22]. Also, the DC current consumption allotted for the error op-amp is a maximum of 30μA total. Using these conditions the error amplifier shown in Fig. 17 is obtained.

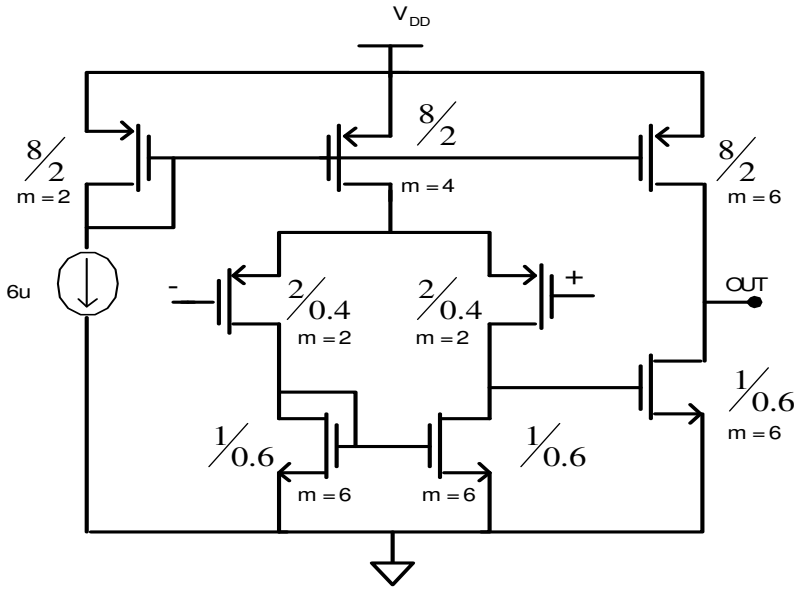


Fig. 17 Error amplifier transistor design.

Minimum lengths are used wherever possible to ensure higher frequency parasitic poles. Longer transistors are used in bias current transistors in order to ensure current matching because cascoding is not possible for low voltage operation in the chosen technology [23].

The feedback resistors R_2 and R_1 are designed according to (19) and the low power consumption constraint in mind.

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) V_{REF} \tag{19}$$

Noticing that the middle programmable level, V_{OUT} = 1.5V, leads to R_1/R_2=6.5 and that a maximum of 6μA of DC current is allotted for that branch of the circuit, then R1=195k Ω and R_2= 55kΩ. The actual value of R_2 will be programmable to obtain the different target output levels, as will be shown in the following sections. The designed error amplifier, pass transistor and feedback resistors, are kept the same throughout this work in order to better quantify the effects of the proposed phase compensation techniques.

Referring back to Fig. 14 the transfer function (TF) for the modeled ESR compensated LDO can be shown to be:

$$TF = H_1 \cdot H_2 \cdot H_3 \cdot H_4 \tag{20}$$

Where,

$$H_1 = \frac{-g_{m1} R_P}{(R_P C_P) \cdot s + 1} \tag{21}$$

$$H_2 = \frac{-g_{m3} R_A}{R_A \left(C_{GATE} + R_{PAR} g_{mp} C_{GD} + C_{GD}\right) \cdot s + 1} \tag{22}$$

$$H_3 = \frac{-g_{mp} \left((R_{PAR} R_{ESR} C_L) \cdot s + R_{PAR}\right)}{(R_{PAR} + R_{ESR}) C_L \cdot s + 1} \tag{23}$$

$$H_4 = \frac{R_2}{R_2 + R_1} \tag{24}$$

By observing (20,) and substituting (21), (22), (23) and (24) into it, the dominant pole P_D of the overall system transfer function is found as:

$$p_D = \frac{1}{2\pi\left(R_{PAR} + R_{ESR}\right)\cdot C_L} \tag{25}$$

The non-dominant poles are given by (26) and (27):

$$p_{ND1} = \frac{1}{2\pi R_A\left(C_{GATE} + R_{PAR}\, g_{mp} C_{GD} + C_{GD}\right)} \tag{26}$$

$$p_{ND2} = \frac{1}{2\pi R_P C_P} \tag{27}$$

The 2nd non-dominant pole is modeled as the pole brought along by the error amplifier as is shown in (27). The zero that is used for phase compensation, when depending on ESR, is given by (28):

$$z = \frac{1}{2\pi R_{ESR} C_L} \tag{28}$$

Knowing the location of each pole and the elements responsible for it, the mathematical model was verified by comparing MATLAB and CADENCE frequency response results. Fig. 18 shows the open loop system simulated in MATLAB with the corresponding miller effect as well as the location of each of the poles. The system was modeled with one dominant pole and two non-dominant poles as well as the zero created by the ESR of the output capacitor.

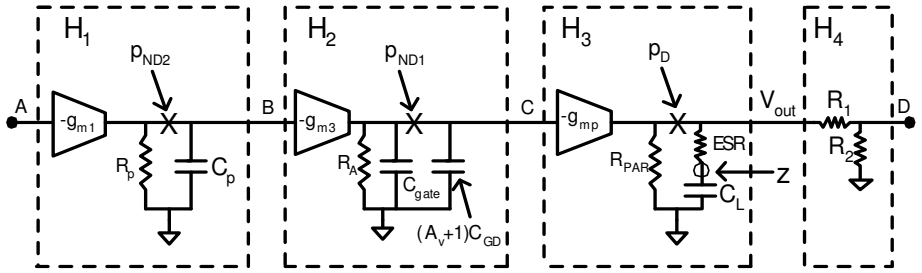
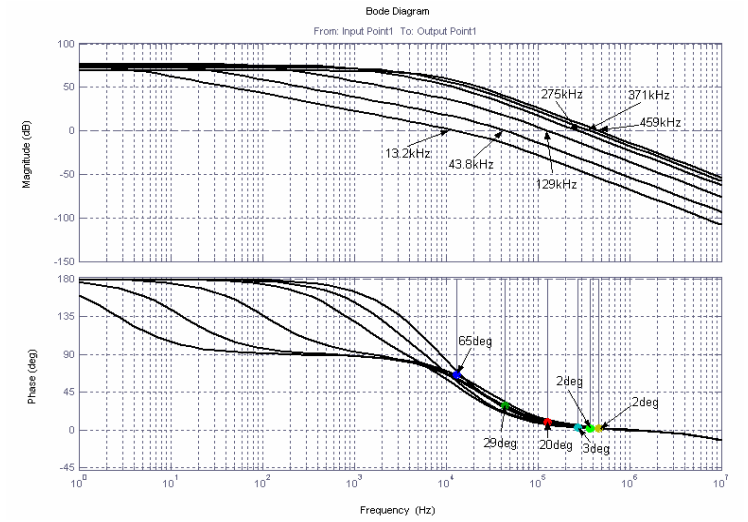
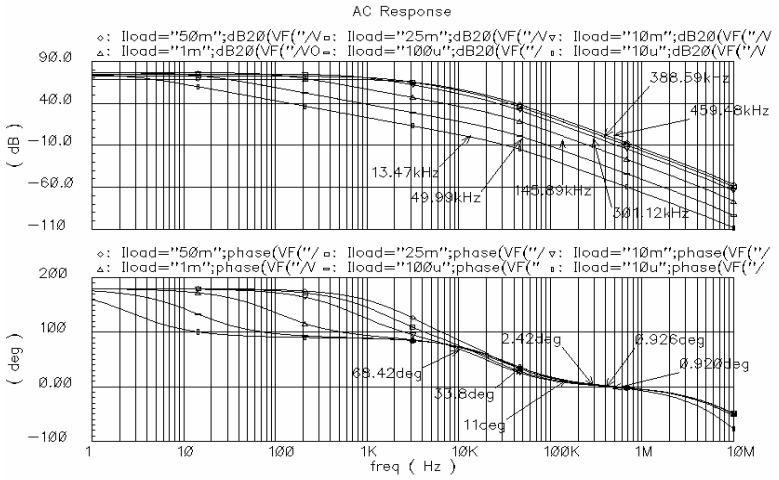


Fig. 18 Open loop typical LDO block diagram.

Fig. 19 (a) shows the open loop AC frequency response of the mathematical model simulated in MATLAB. Fig. 19 (b) shows the results of the simulation carried out on the open loop LDO system in CADENCE. For these simulations the ESR value was set to 0 in order to characterize a completely uncompensated design. It is apparent that the mathematical model predicts the performance very closely. Therefore it can be used to evaluate effects of any changes that can be made to the system in order to increase performance.



(a)



(b)

Fig. 19 AC frequency response for (a) MATLAB model and (b) CADENCE model for typical LDO without compensation.

Table IV summarizes the values obtained for each of the two methods used to characterize the open loop system. It shows that the mathematical model is a useful tool to generate predictions on the behavior of the system.

TABLE IV

AC RESPONSE FOR DIFFERENT LOADS TYPICAL LDO

	I_{LOAD} = 10µA		I_{LOAD} = 100µA		I_{LOAD} = 1mA	
	MTLB	**CDNC**	**MTLB**	**CDNC**	**MTLB**	**CDNC**
f_u	13.2k	13.47k	43.8k	49.99k	129k	145.89k
PM	65deg	68.42deg	29deg	33.8deg	20deg	11deg
	I_{LOAD} =10mA		I_{LOAD} = 25mA		I_{LOAD} = 50mA	
	MTLB	**CDNC**	**MTLB**	**CDNC**	**MTLB**	**CDNC**
f_u	275k	301.12k	371k	388.59k	459k	459.48k
PM	3deg	2.42deg	2deg	0.926deg	2deg	0.92deg

The MATLAB representation of the system is sufficiently accurate and presents a maximum of 8.6% error in unity gain frequency (f_u) compared to the results obtained in CADENCE.

An important characteristic to observe is the pole movement from low-load to high-load conditions. The pole movements are shown to be detrimental to the system's phase margin.

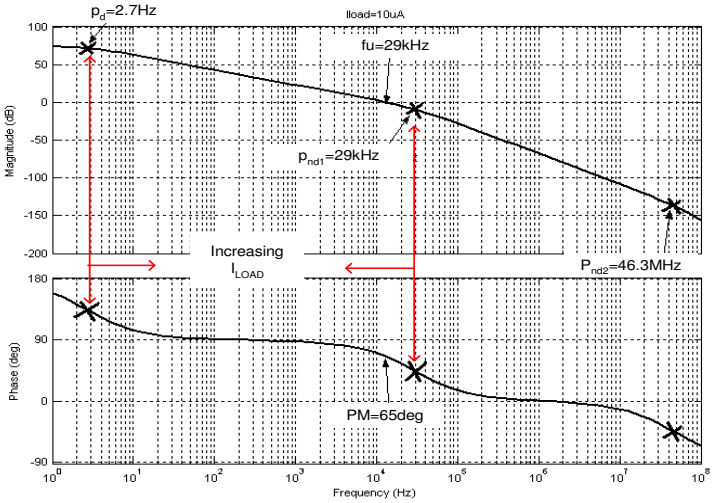
Fig. 20 (a) and (b) show the large variation in the dominant pole location and the smaller, yet no less important variation of the 1st non-dominant pole location. The dominant pole found at the output presents large variations due to the changes in load current because they translate into large variations of output impedance, $R_{PAR.}$ Also, farther compromising the stability of the system, the 1st non-dominant pole moves to lower frequencies with increasing load currents. The poles movement range is shown in Table V for the varying loads.

TABLE V

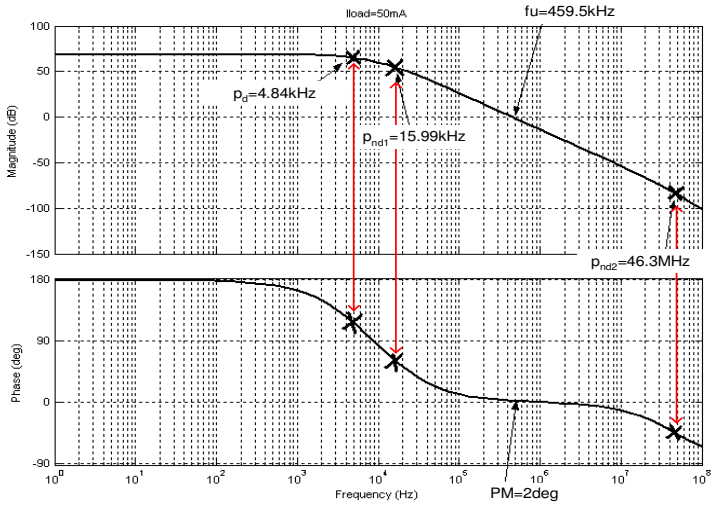
POLE LOCATION VARIATION IN TYPICAL LDO

Pole Variations (10µ-50mA Loads)	
p_d	2.7Hz - 4.84kHz
p_{nd1}	29kHz - 15.99kHz
p_{nd2}	46.1MHz - 46.28MHz

As can be seen in Fig. 20, the dominant pole and non-dominant pole variations are responsible for insufficient phase margin. Table V predicts the movement of these poles.



(a)



(b)

Fig. 20 Pole locations for I_{LOAD} (a) 10µA and (b) 50mA in a typical LDO.

The 2nd pole (i.e. p_{nd1}) will also move closer to the dominant pole when higher load currents are present causing even more deterioration of the phase margin. Therefore the critical design cases for this type of LDO are at higher current loads.

Knowing that the movement of the dominant and 1st non-dominant poles is what causes this LDO to become unstable and recognizing the elements responsible for this, it can be stated that those movements are inherent to a typical LDO. The dominant pole location moves by 270% due to the large variation in output impedance R_{PAR}, shown in (25). R_{PAR} is inversely related to the load current because it includes the output impedance r_{ds} of the pass transistor, an unavoidable effect of the topology. Another unavoidable effect is the movement of the 1st non-dominant pole due to variations in pass transistor dc gain, in turn, defined by the same R_{PAR} and g_{mp} (that also depends on I_{LOAD}) shown in (26). Both these effects lead to the development of the proposed phase compensation schemes.

2. Phase Compensation Implementation I

A. Mathematical Model and Design

Using Fig. 18 a compensation scheme was developed to improve the stability and AC performance of a typical LDO. The main objective is to obtain a guaranteed stable loop for all programmable output levels. Minimizing the dependence on the ESR of the output capacitor and limiting the pole movement will aid in accomplishing this goal. As previously discussed, the elevated cost for capacitors with a well defined low ESR value (ceramic capacitors) is a motivating factor for this design, as well as the possibility of realizing a programmable LDO that can achieve multiple output levels while exhibiting stability over the entire load range (10μ-50mA).

It was found that a feedback loop taken from the V_{OUT} node and summed back at node B will indeed stabilize the system. This idea is practical because the signal that is injected back to

node B is a current. Fig. 21 shows the compensation path attached to the typical LDO with the operational amplifier modeled as a two stage system in order to make node B readily available. It also shows the mathematical interpretation of implementation I of the compensation scheme.

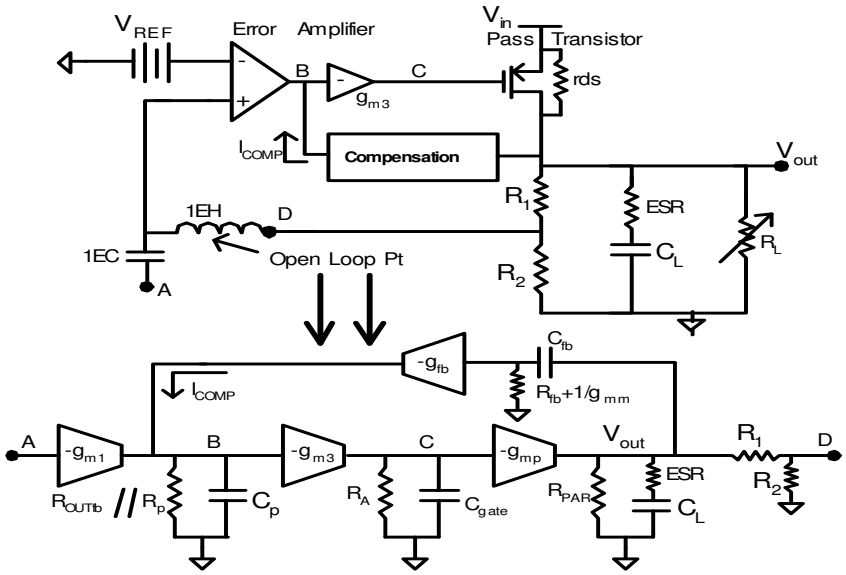


Fig. 21 Implementation I block diagram.

Implementation I, as shown, will provide a feedback path that involves the derivative of any changes created at the output of the system. Specifically, any change (transient) in the output will be detected by this feedback path before it is detected by the loop formed when the system is tied in closed loop configuration A-D. Therefore this LDO should exhibit a better transient response than one that depends on the value of ESR for its compensation as it will respond faster to changes in the output.

The feedback block is shown in more detail in Fig. 22. There are certain constraints that need to be analyzed in order to see how the addition of this feedback network interacts with the loads that are present at each of the nodes where it is connected.

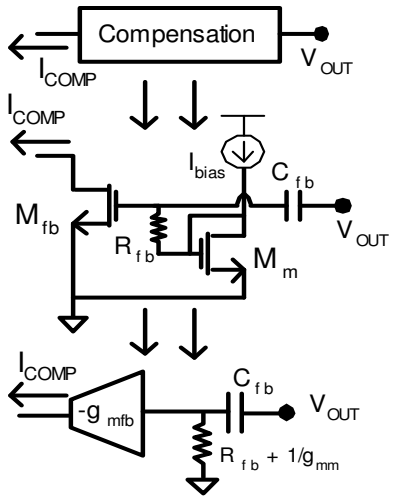


Fig. 22 Implementation I feedback circuit and block diagram.

The equation expressing the transfer function for the current injected into node B, can be derived from Fig. 22 and is given by (29):

$$\frac{I_{COMP}}{V_{OUT}} = \frac{-g_{mfb} \cdot s\left(R_{fb} + 1/g_{mm}\right) \cdot C_{fb}}{s\left(R_{fb} + 1/g_{mm}\right) \cdot C_{fb} + 1} \tag{29}$$

This circuit implements a differentiator as shown in its transfer function (29). In order to design the compensation scheme used in implementation I several factors need to be taken into account. First, a low power solution is targeted. With this in mind, expression (29) shows a pole, given by (30).

$$p_{fb} = \frac{1}{2\pi\left(R_{fb} + 1/g_{mm}\right)C_{fb}} \tag{30}$$

Noticing that this pole should be pushed to frequencies outside the band of interest (> 1MHz), (30) can be used to calculate the approximate requirement for g_{mm}. Also, taking into account that due to the nature of a low power solution, a smaller transconductance g_{mm} will be obtained, it is assumed that $1/g_{mm} >>> R_{fb}$. This will benefit the design as it will limit the dependence of the pole

location on a value that is more difficult to control in the IC (R_{fb}). Therefore, by assuming R_{fb} = 100Ω (a viable value for integration on chip) and selecting C_{fb}=8pF, the minimum value necessary to place this parasitic pole to frequencies higher than 1MHz is shown by (31):

$$p_{fb} \geq 1MHz = \frac{1}{2\pi\left(R_{fb} + 1/g_{mm}\right)C_{fb}} \Rightarrow g_{mm} \geq 50\,\mu A/V \tag{31}$$

C_{fb} was chosen at 8pF due to the fact that higher capacitance would have brought this parasitic pole to lower frequencies, deteriorating the phase margin and frequency response.

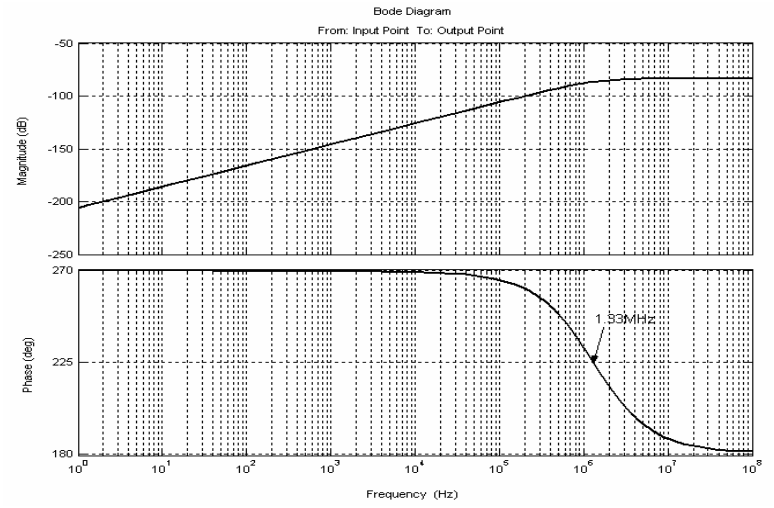
Once the transconductance g_{mm} was established, the transistor responsible for it was designed using the drain current equation for saturation. The allowed dc current was set to 12μA in order to save as much power as possible. As can be seen from Fig. 22 transistor M_m acts as a current mirror to bias the gate of transistor M_{fb} through the connected resistor R_{fb}. Now that the two transistors form a current mirror, their transconductance should, ideally, be equal and transistor M_{fb} can be designed with the drain current equation as well.

With these results a CADENCE simulation was developed for the compensation scheme used in implementation I. Table VI shows the simulated values obtained. The frequency response of the feedback block for implementation I was obtained in both CADENCE and MATLAB; they are shown in Fig. 23 (a) and (b).

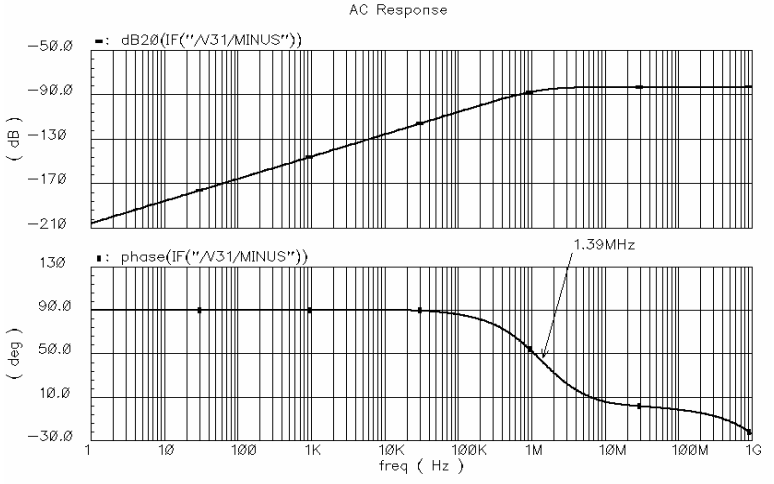
TABLE VI

SIMULATOR VALUES IMP. I

Implementation I	
g_{mfb}	66.06μ
R_{fb}	100Ω
g_{mm}	66.13μ
C_{fb}	8pF



(a)



(b)

Fig. 23 AC frequency response of feedback for implementation I (a) MATLAB, (b) CADENCE.

Clearly, the results shown in Fig. 23 that were obtained in CADENCE and MATLAB agree and both show a parasitic pole for the frequency compensation scheme at around 1.3MHz.

Once the feedback is connected into the LDO, nodes V_{OUT} and B will be loaded with the effects of implementation I. This implies that the transfer function and more specifically the pole and zero locations will change. The transfer function was found to be TF_{C1} for the system compensated with implementation I (32).

$$TF_{C1} = \frac{-g_{m1} \cdot H_{1C1} \cdot H_{2C1} \cdot H_{3C1} \cdot H_4}{1 + H_{fbC1} \cdot H_{1C1} \cdot H_{2C1} \cdot H_{3C1}} \tag{32}$$

Where,

$$H_{1C1} = \frac{R_{OUTfb} R_P}{\left(R_{OUTfb} R_P C_P\right) \cdot s + R_{OUTfb} + R_P} \tag{33}$$

$$H_{2C1} = \frac{-g_{m3} R_A}{R_A\left(C_{GATE} + R_{PAR} g_{mp} C_{GD} + C_{GD}\right) \cdot s + 1} \tag{34}$$

$$H_{3C1} = \frac{-g_{mp}\left(C_{FB} C_L R_{ESR}\left(R_{fb} + \frac{R_{PAR}}{g_{mm}}\right) \cdot s^2 + P_{PAR}\left(R_{fb} C_{fb} + \frac{C_{fb}}{g_{mm}} + R_{ESR} C_L\right) \cdot s + R_{PAR}\right)}{C_{fb} C_L\left(R_{fb} R_{PAR} + \frac{R_{PAR}}{g_{mm}} + R_{PAR} R_{ESR} + R_{fb} R_{ESR} + \frac{R_{ESR}}{g_{mm}}\right) \cdot s^2 + \left(C_L R_{PAR} + C_{fb} R_{PAR} + C_{fb} R_{fb} + \frac{C_{fb}}{g_{mm}} + C_L R_{ESR}\right) \cdot s + 1} \tag{35}$$

$$H_{fbC1} = \frac{-g_{mfb} C_{fb}\left(R_{fb} + 1/g_{mm}\right) \cdot s}{C_{fb}\left(R_{fb} + 1/g_{mm}\right) \cdot s + 1} \tag{36}$$

While H_4 and H_2 remain unchanged, overall, the system now becomes as shown in Fig. 24.

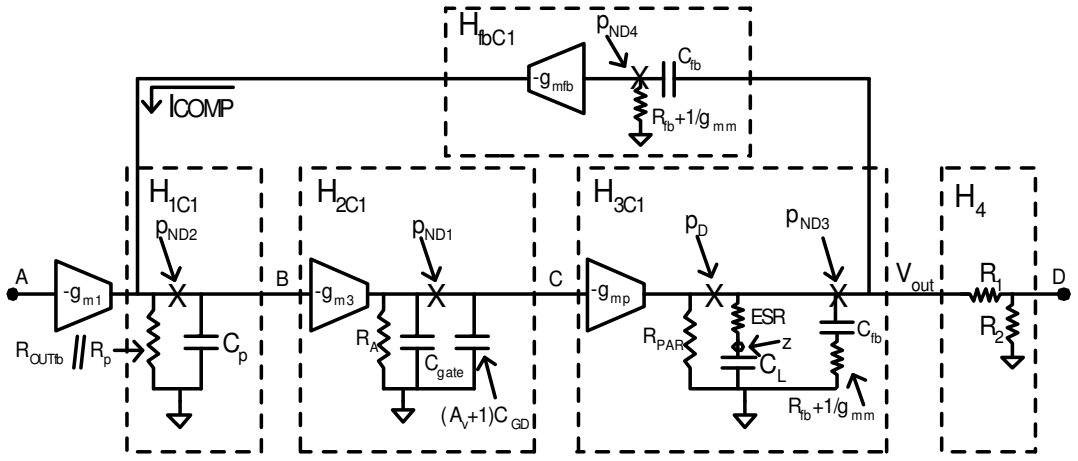
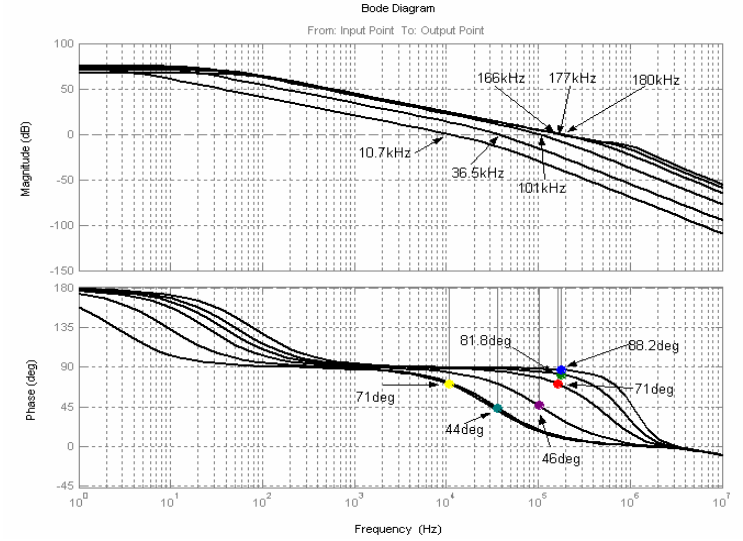
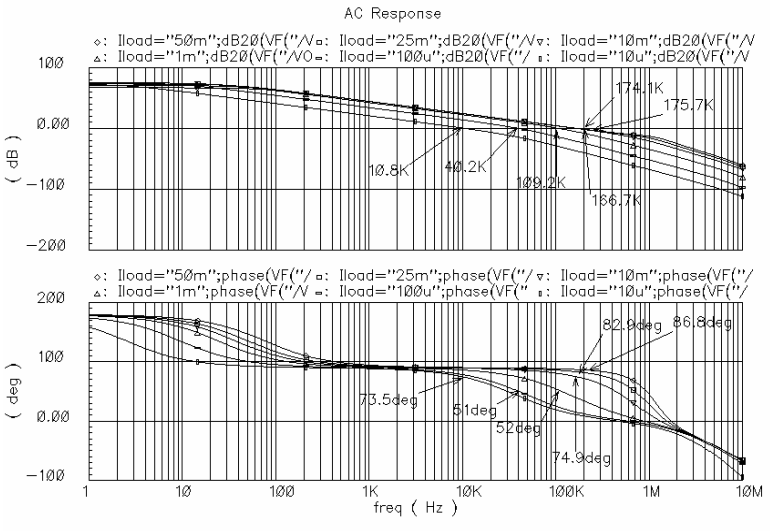


Fig. 24 Overall block diagram for implementation I.

There are now new poles and zeros for the compensated system. The system order is increased to greater than 3rd order when the feedback is applied. To identify the location of poles and zeros for the new compensated LDO, it was modeled in MATLAB. These results were also compared with results obtained in CADENCE. Fig. 25 (a) and (b) show the AC frequency simulation results.



(a)



(b)

Fig. 25 AC frequency response for (a) MATLAB model and (b) CADENCE model for implementation I.

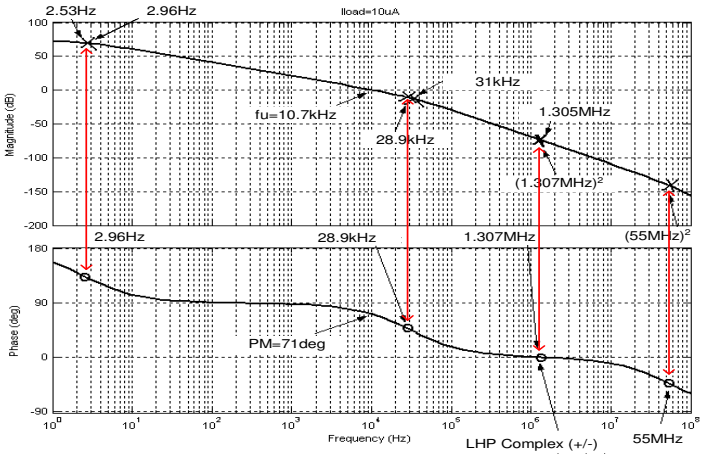
When comparing Fig. 25 to Fig. 19 it is readily apparent that there is an increase in phase margin with a decrease in f_u. Table VII shows the summary of the results predicted in MATLAB and the results obtained in CADENCE for implementation I.

TABLE VII

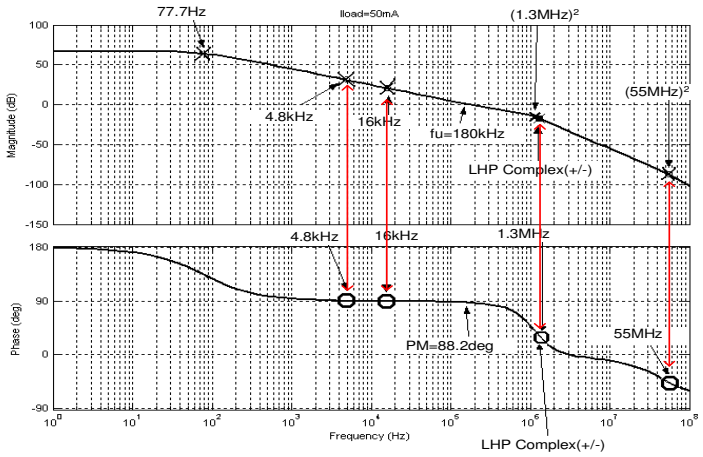
AC RESPONSE FOR DIFFERENT LOADS IMP. I

	I_{LOAD} = 10µA		I_{LOAD} = 100µA		I_{LOAD} = 1mA	
	MTLB	**CDNC**	**MTLB**	**CDNC**	**MTLB**	**CDNC**
GBW	10.7kHz	10.8kHz	36.5kHz	40.2kHz	101khZ	109.2kHz
PM	71deg	73.5deg	44deg	51deg	46deg	52deg
	I_{LOAD} =10mA		I_{LOAD} = 25mA		I_{LOAD} = 50mA	
	MTLB	**CDNC**	**MTLB**	**CDNC**	**MTLB**	**CDNC**
GBW	166kHz	166.7kHz	177kHz	174.1kHz	180kHz	175.7Khz
PM	71deg	74.9deg	81.8deg	82.9deg	88.2deg	86.8deg

In order to verify pole and zero locations for the transfer function $TF_{C1,}$ the bode plots are obtained using MATLAB. The exact pole and zero locations are obtained for the system and are shown in Fig. 26 (a) for an I_{LOAD} = 10µA. Fig. 26 (b) shows the same result for the exact pole and zero locations for an I_{LOAD} = 50mA. Both figures show the poles in the gain plot while the zeros are clearly marked in the phase margin plots. As was explained, the TF is now a 5^{th} order expression containing 5 poles and 4 zeros.



(a)



(b)

Fig. 26 Pole locations for I_{LOAD} (a) 10µA and (b) 50mA in implementation I.

The values used to evaluate the transfer function are obtained from CADENCE when the transistor implementation of the error amplifier, pass transistor and feedback resistors previously designed are used in conjunction with the design of implementation I. Clearly, there are automatic pole-zero cancellations that are inherent to the current summation node as well as the pole zero pair created at the input of the feedback network, as shown in Fig. 26.

The unity gain frequency of the system now has a maximum value of 175kHz at highest load case. It can be assumed that the effects of poles and zeros greater than 1.3MHz can be neglected for system characterization. These poles and zeros are found in higher frequencies

with respect to the BW of operation of the LDO, nonetheless it is important that they are located in the left hand plane of the Real-Imaginary axes in order to guarantee stability.

Using the previous results leads to the transistor level design of the LDO with feedback compensation implementation I, depicted in Fig. 27. The transistor level design can be directly compared to the block diagram representations shown in Fig. 21. The corresponding nodes are labeled accordingly for ease of correlation.

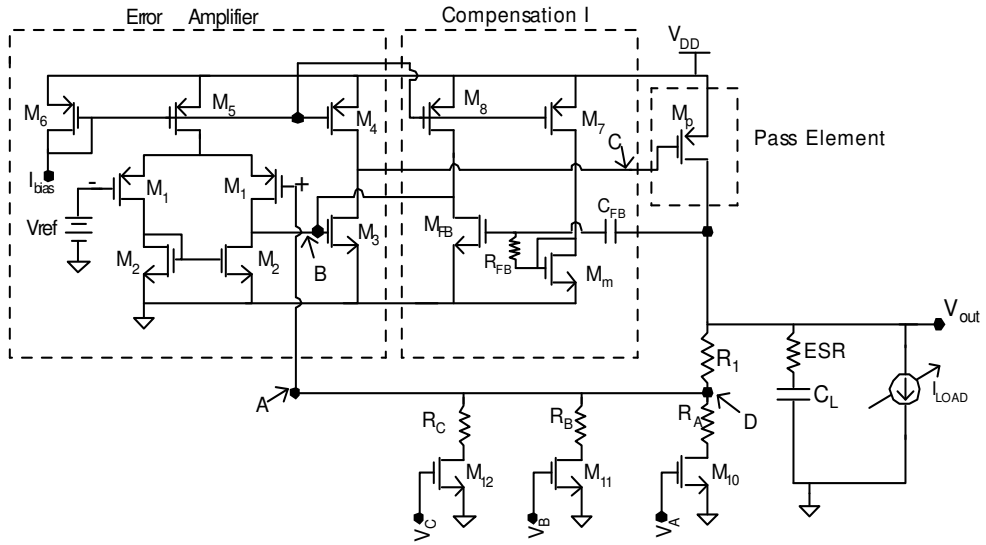


Fig. 27 Schematic for implementation I.

The programmability feature was included with different resistor values that changed the feedback factor in order to adjust the output level. N-type transistors used as switches (M_{10}, M_{11}, and M_{12}) were included to select the appropriate outputs available.

The programmability characteristic for the 3 different output levels is shown in Table VIII.

TABLE VIII

PROGRAMMABLE OUTPUT LEVELS FOR IMP. I

V_{OUT}	V_A	V_B	V_C
0.9V	1	0	0
1.5V	0	1	0
1.8V	0	0	1

In conclusion, the overall design procedure for implementation I is the following:

- Select the required dropout voltage and design the pass transistor accordingly.
- Budget DC current consumption.
- Design the error amplifier for low voltage operation (1.2V) and high gain (A_v>60dB).
- Design the feedback resistors R_1 and R_2 for minimal DC current and V_{REF}=200mV.
- Design the feedback network with parasitic pole at least 5 X f_u, when $f_u$max<200kHz.

The overall design for implementation I is summarized in Table IX. The simulated performance metrics results are discussed in the following chapter.

TABLE IX

IMP. I DESIGNED VALUES

	W	L	m
M_1	2µm	400nm	2
M_2	1µm	600nm	2
M_3	1µm	600nm	6
M_4	8µm	2µm	6
M_5	8µm	2µm	4
M_6	8µm	2µm	2
M_7	8µm	2µm	2
M_8	8µm	2µm	2
M_m	1.5µm	1µm	2
M_{fb}	1.5µm	1µm	2
M_P	50µm	400nm	320
M_9	10µm	400nm	10
M_{10}	10µm	400nm	10
M_{11}	10µm	400nm	10
R_1	195 kΩ		
R_A	55 kΩ (0.9V)		
R_B	30 kΩ (1.5V)		
R_C	24.3 kΩ (1.8V)		
C_{LOAD}	1 µF		
C_{FB}	8 pF		
R_{FB}	100 Ω		
V_{REF}	200 mV		
I_{BIAS}	6 µA		

3. Phase Compensation Implementation II

A. Mathematical Model and Design

A careful look at implementation I can lead to another implementation. Earlier in this chapter it was mentioned that the justification for the use of a two stage amplifier as the error amp would become readily apparent. By observing Fig. 27 more closely, it appears that the possibility of injecting the signal at another node inside the error amplifier would not change the loop dynamics and would also implement the feedback transfer function used for implementation I. Fig. 28 shows a clearer picture of this inherent property when using a two-stage amplifier. For

implementation II the same error amplifier, pass transistor and resistor feedback network is used in order to validate comparisons between implementations.

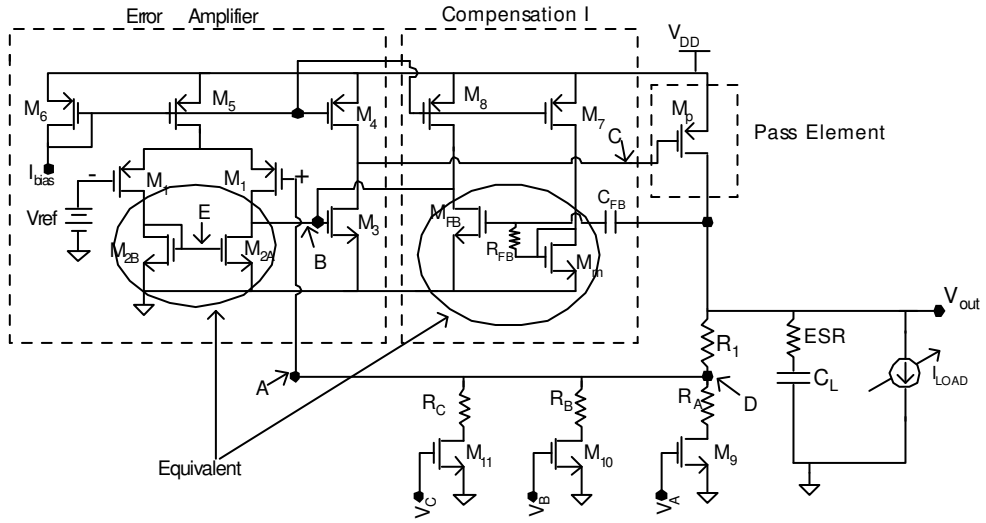


Fig. 28 Development of implementation II.

As can be seen in Fig. 28, the transistors that make up the compensation circuit ($M_{FB}$and M_m) already exist inherently in the load of the differential pair (M_2). Therefore, connecting a feedback capacitor to node E will have the same effect as implementation I. Specifically, M_{2A} will replace M_{FB} and the diode connected M_{2B} will replace M_m. This second implementation will be referred to as implementation II throughout this thesis.

Mathematically, implementation II is equivalent and can therefore be modeled as shown in Fig. 29. The compensation capacitor is connected between the V_{OUT} output node and node E; both are labeled in Fig. 28.

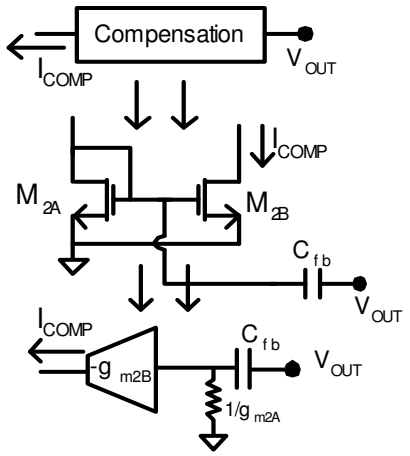


Fig. 29 Implementation II feedback block diagram.

From Fig. 29 it can be assumed that $g_{m2A} = g_{m2B} = g_{m2}$, because both transistors are connected in a current mirror configuration. Therefore, the voltage to current transfer function of implementation II is obtained (37):

$$\frac{I_{COMP}}{V_{OUT}} = \frac{-g_{m2} \cdot C_{fb} \cdot s}{C_{fb} \cdot s + g_{m2}} \tag{37}$$

Again a zero is present at DC frequency as was for implementation I. The parasitic pole location is no longer dependant on a somewhat unreliable R_{fb} (considered unreliable when integrated in the IC). The parasitic pole location is now found as shown in (38).

$$p_{fb} = \frac{g_{m2}}{2\pi \cdot C_{fb}} \tag{38}$$

Therefore, by keeping the same constraint (> 1MHz) on this parasitic pole and by using the already designed error amplifier, a minimum C_{fb} requirement can be obtained for this implementation. The 1MHz constraint is well over the anticipated fu obtained in implementation I of <200kHz; nevertheless, it is kept the same. A value for g_{m2} was extracted from the CADENCE simulations fir implementation I, as g_{m2}=67.15µA/V. It is shown in (39) that the minimum C_{fb} necessary to fulfill the 1MHz requirement is the following:

$$C_{fb} \geq \frac{g_{m2}}{2\pi \cdot p_{fb}} \Rightarrow C_{fb} \geq 10pF \tag{39}$$

Now that a minimum feedback capacitor value is obtained, a simulation in both CADENCE and MATLAB can be carried out in order to verify proper operation of implementation II. Table X shows the valued used in these two simulations for verification.

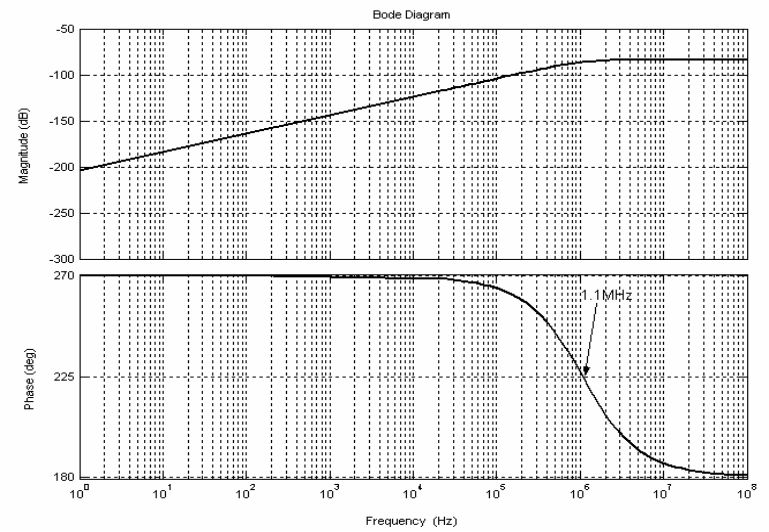
TABLE X

SIMULATOR VALUES IMP. II

Implementation II	
g_{m2}	67.15µ
C_{fb}	10 pF

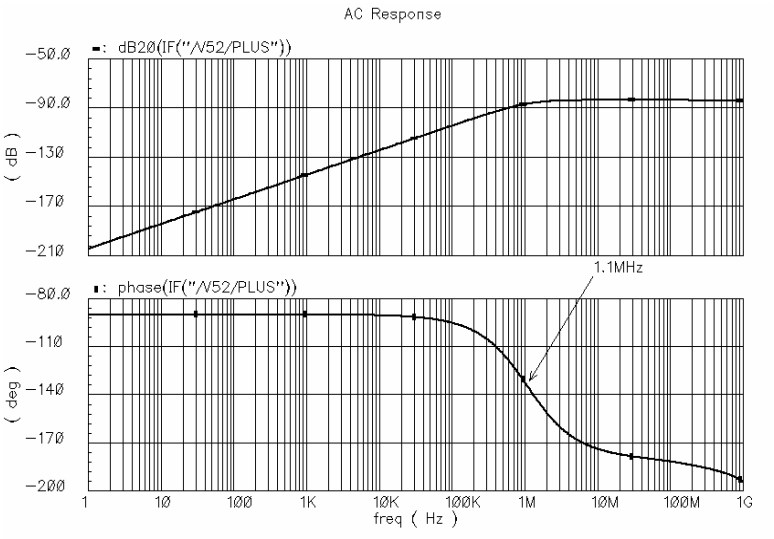
The results of the CADENCE and MATLAB simulations are shown in Fig. 30 (a) and (b) respectively. The calculated pole location for implementation II is obtained following (40).

$$p_{fb} = \frac{g_{m2}}{2\pi \cdot C_{fb}} \Rightarrow p_{fb} \approx 1.1MHz \tag{40}$$



(a)

Fig. 30 AC frequency response of feedback for implementation I (a) MATLAB, (b) CADENCE.



(b)

Fig. 30 Continued.

The two results agree well with each other. The pole calculation shown in (40) agrees with the pole location in Fig. 30. Thus, the differentiator will bring with it a zero at zero frequency (DC) and a pole at 1.1MHz as predicted by both simulations and calculation.

When implementation II is connected to the uncompensated LDO it will again interact with the elements it connects to. Like implementation I, the transfer functions will indeed change for each block the compensation is attached to. Therefore, the following expressions show these changes:

$$TF_{C2} = \frac{-g_{m1} \cdot H_{1C2} \cdot H_{2C2} \cdot H_{3C2} \cdot H_4}{1 + H_{fbC2} \cdot H_{1C2} \cdot H_{2C2} \cdot H_{3C2}} \tag{41}$$

Where,

$$H_{1C2} = \frac{R_P}{(R_P C_P) \cdot s + 1} \tag{42}$$

$$H_{2C2} = \frac{-g_{m3} R_A}{R_A \left(C_{GATE} + R_{PAR} g_{mp} C_{GD} + C_{GD}\right) \cdot s + 1} \tag{43}$$

$$H_{3C2}=\frac{-g_{mp}\left(C_{fb}C_L\left(\frac{R_{ESR}\cdot R_{PAR}}{g_{m2}}\right)\cdot s^2+\left(C_LR_{PAR}R_{ESR}+\frac{C_{fb}R_{PAR}}{g_{m2}}\right)\cdot s+R_{PAR}\right)}{\left(C_{fb}C_L\frac{R_{ESR}}{g_{m2}}+C_{fb}C_L\frac{R_{PAR}}{g_{m2}}+C_{fb}C_LR_{ESR}R_{PAR}\right)\cdot s^2+\left(C_LR_{ESR}+\frac{C_{fb}}{g_{m2}}+C_LR_{PAR}+C_{fb}R_{PAR}\right)\cdot s+1} \tag{44}$$

$$H_4=\frac{R_2}{R_2+R_1} \tag{45}$$

$$H_{fbC2}=\frac{-g_{m2}\cdot C_{fb}\cdot s}{C_{fb}\cdot s+g_{m2}} \tag{46}$$

Once again H_4 remains unchanged, as does H_2. In this implementation, H_2 is named H_{2C2}. Fig. 31 shows the mathematical representation of the LDO compensated with implementation II.

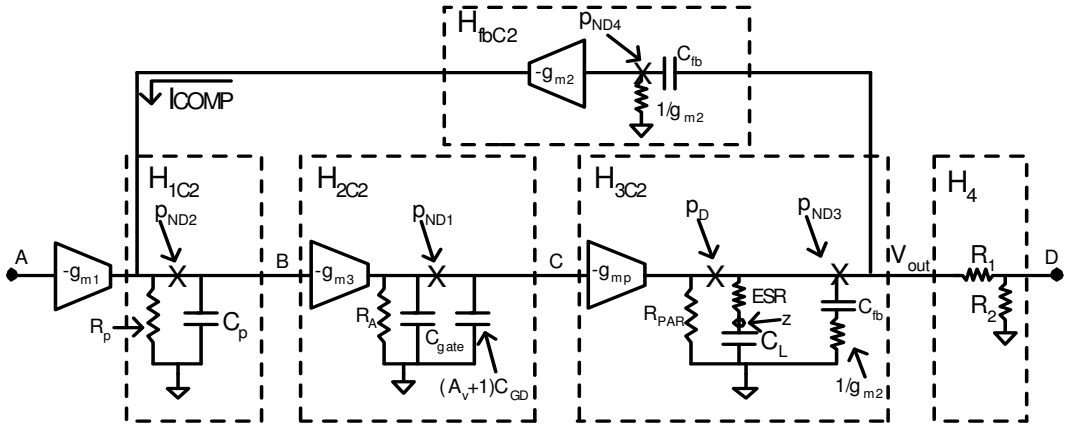


Fig. 31 Overall block diagram for implementation II.

The performance of the system was modeled in MATLAB. It was also verified and compared with results obtained in CADENCE. Fig. 32 (a) and (b) show these results.

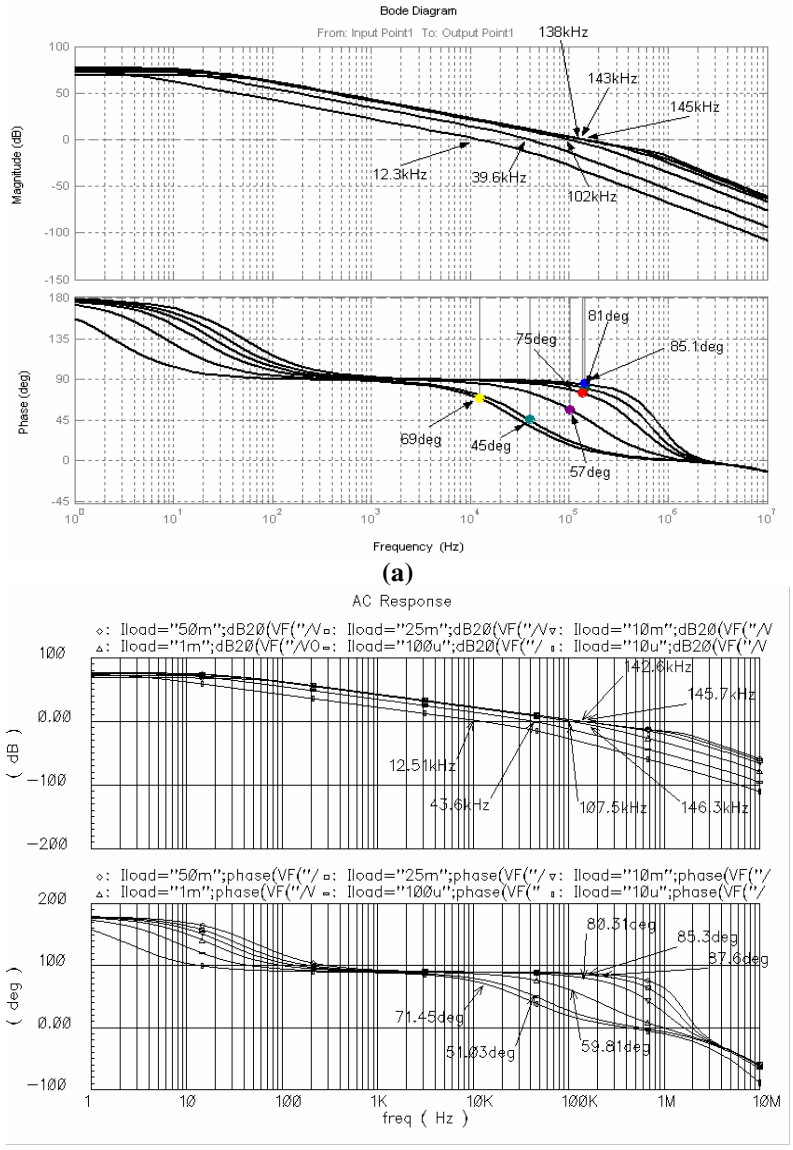


Fig. 32 AC frequency response for (a) MATLAB model and (b) CADENCE model for implementation II.

When comparing Fig. 32 to Fig. 19 it is apparent that this implementation presents an increase in phase margin with a decrease in unity gain frequency, the same results obtained for implementation I. This result is expected as the transfer function applied is the same with a different circuit implementation.

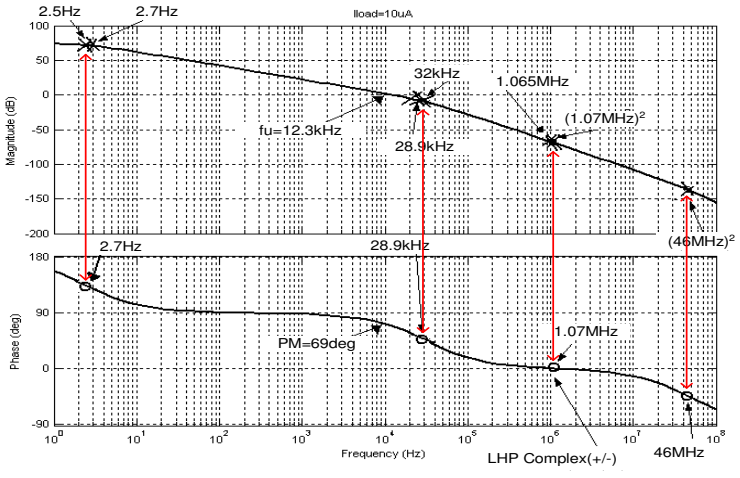
Table XI shows the summary of the results predicted in MATLAB and the results obtained in CADENCE for implementation II.

TABLE XI

AC RESPONSE FOR DIFFERENT LOADS IMP. II

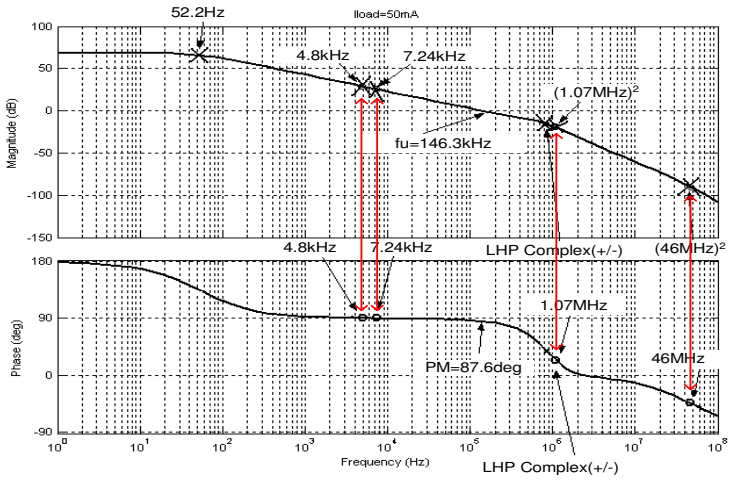
	I_{LOAD} = 10µA		I_{LOAD} = 100µA		I_{LOAD} = 1mA	
	MTLB	**CDNC**	**MTLB**	**CDNC**	**MTLB**	**CDNC**
f_u	12.3kHz	12.51kHz	39.6kHz	43.6kHz	102kHz	107.5Khz
PM	69deg	71.45deg	45deg	51.03deg	57deg	59.81deg
	I_{LOAD} =10mA		I_{LOAD} = 25mA		I_{LOAD} = 50mA	
	MTLB	**CDNC**	**MTLB**	**CDNC**	**MTLB**	**CDNC**
f_u	138kHz	142.6kHz	143kHz	145.7kHz	145kHz	146.3kHz
PM	75deg	80.31deg	81deg	85.3deg	85.1deg	87.6deg

The system in closed loop, as predicted by TF_{C2} (41), becomes a 5th order expression. Therefore, to find the exact locations and range of movement of the poles and zeros with varying load, frequency simulations are carried out and their data is plotted. MATLAB results show all of the poles and zeros of the system superimposed on the bode frequency plots. Fig. 33 (a) shows the exact locations with an I_{LOAD}=10µA. Fig. 33 (b) shows the locations with an I_{LOAD}=50mA. These results offer valuable insight into the performance of the system.



(a)

Fig. 33 Pole and zero locations for I_{LOAD} (a) 10µA and (b) 50mA in implementation II.



(b)

Fig. 33 Continued.

Once again the maximum unity gain frequency is 145.6 kHz. This result is less than for implementation I, as can be expected because implementation II has a larger value capacitor. Even so, this is a positive attribute because all the poles and zeros greater than 1.07 MHz that is ~10X the fu of the LDO compensated with implementation II. Therefore poles and zeros above 1.07 MHz can be considered higher frequency parasitics for calculation and design purposes. Nonetheless it is important to make sure that any complex poles or zeros all stay in the left hand plane of the Real-Imaginary axis.

The design procedure for implementation II follows the same procedure as implementation I except for a few changes. Once the error amplifier, pass transistor and resistor feedback network are designed, the following steps can be take in order to obtain a successful design:

- Obtain the g_{m2} value of the active load connected to the differential pair input.
- Use expression (40) to set the location of the parasitic pole introduced by implementation II; preferably >1MHz.

- Verify the location of poles and zeros of the system, if any complex pairs are present; ensure that they are located in the left hand plane of real-imaginary axis.

Using the previous assumptions and results the final design of implementation II is shown in Fig. 34. The transistor level design can be directly compared to the block diagram representations shown previously in Fig. 31. The corresponding nodes are labeled accordingly for ease of correlation.

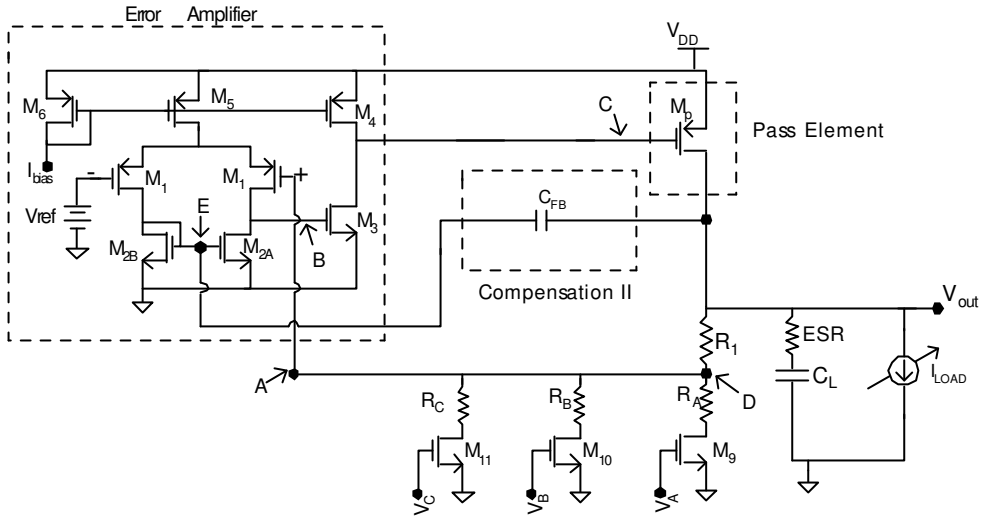


Fig. 34 Schematic for implementation II.

N-type switches (M_9, M_{10} and M_{11}) were also included to select the appropriate outputs available and their programmability is shown in Table XII.

TABLE XII

PROGRAMMABLE OUTPUT LEVELS FOR IMP. II

V_{OUT}	V_A	V_B	V_C
0.9V	1	0	0
1.5V	0	1	0
1.8V	0	0	1

The overall design for implementation II is summarized in Table XIII. The simulated results are discussed in the following chapter which includes all the performance metrics such as transient and frequency responses.

TABLE XIII

IMP. II DESIGNED VALUES

	W	L	m
M_1	2µ	400n	2
M_2	1µ	600n	2
M_3	1µ	600n	6
M_4	8µ	2µ	6
M_5	8µ	2µ	4
M_6	8µ	2µ	2
M_p	50µ	400n	320
M_9	10µ	400n	10
M_{10}	10µ	400n	10
M_{11}	10µ	400n	10
R_1	195k		
R_A	55 kΩ (0.9V)		
R_B	30 kΩ (1.5V)		
R_C	24.3 kΩ (1.8V)		
C_{LOAD}	1µF		
C_{FB}	10pF		
V_{REF}	200mV		
I_{BIAS}	6 µA		

Overall, the two implementations are shown to improve the typical LDO's phase response. Specifically, implementation I will increase the phase margin to no less than 51º according to CADENCE simulation results; implementation II will do the same to no less than 50º. The main difference between the two implementations is cost. Implementation I will require 3 more transistors, at the cost of area and power consumption; while implementation II takes advantage of transistors already present. More of the performance metrics will be evaluated in the following chapters.

CHAPTER IV

SCHEMATIC SIMULATION AND RESULTS

In this chapter, the performance metrics for each implementation's schematic are simulated using CADENCE. The results are shown for implementation I and summarized for implementation II. This is plausible because the same metrics and simulations setup was applied to both proposed implementations.

1. Phase Compensation Implementation I

A. AC Performance

For implementation I the loop is opened as shown in Fig. 35. An AC source is placed at node A and is considered the input for the open loop frequency simulations carried out in CADENCE. A large inductor is used in order to create an open circuit for higher frequencies and a short circuit for DC, thus keeping the DC voltage unchanged. The AC signal is fed through a large simulated capacitor at the break node. The input for all closed loop CADENCE simulations and practical operation is node V_{DD}.

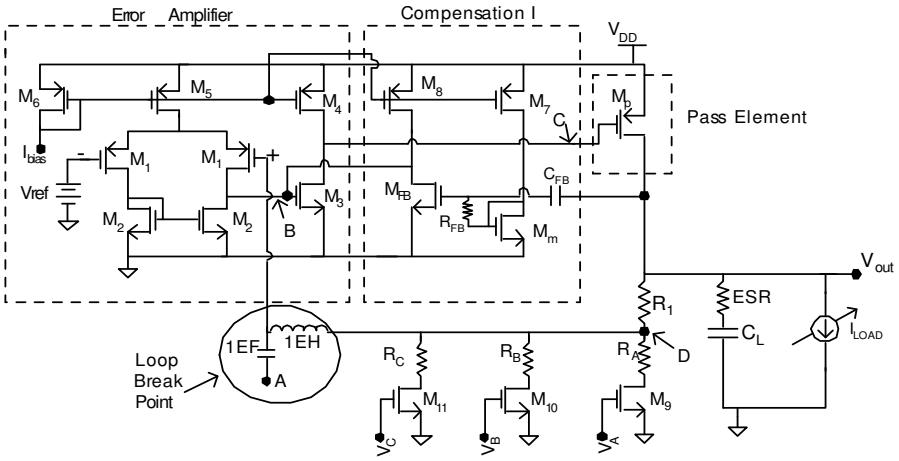


Fig. 35 Loop break point for implementation I.

The open loop frequency CADENCE simulations are obtained by sweeping through the different current load conditions while programming the output to 1.5V. C_L is made 1µF and the ESR value is set to 0. The results in Table XIV show the characteristics of various I_{LOAD} cases.

TABLE XIV

AC CHARACTERISTICS FOR IMP. I

I_{LOAD}	Av@1Hz	f_u	PM
10 µA	72.37 dB	10.8 kHz	73.5°
100 µA	74.77 dB	40.2 kHz	51.0°
1 mA	75.05 dB	109.2 kHz	52.0°
10 mA	73.19 dB	166.7 kHz	74.9°
25 mA	70.67 dB	174.1 kHz	82.9°
50 mA	67.15 dB	175.7 kHz	86.8°

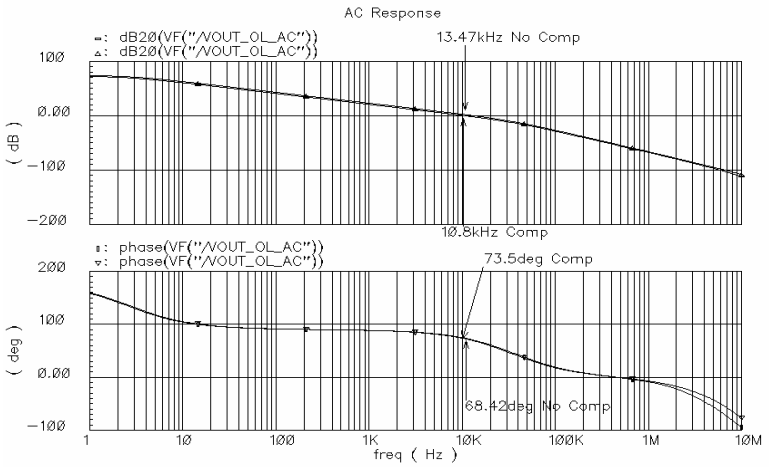


Fig. 36 AC frequency response for implementation I vs. ESR compensated w/ESR=0Ω for I_{LOAD} = 10µA, V_{IN}=1.8V, V_{OUT}=1.5V.

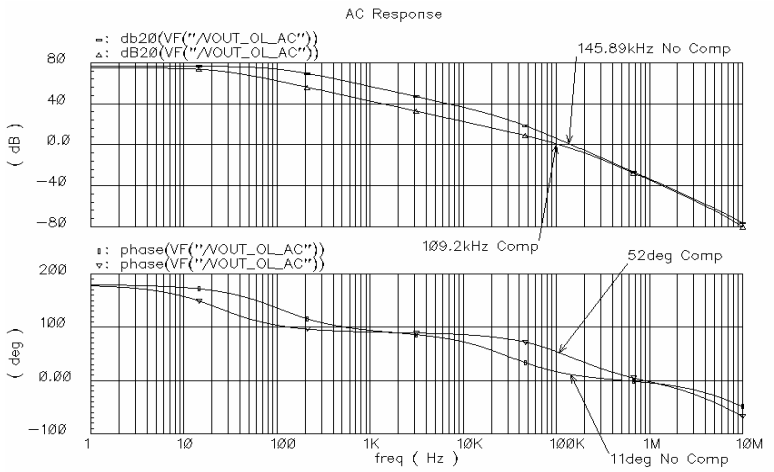


Fig. 37 AC frequency response for implementation I vs. ESR compensated w/ESR=0Ω for I_{LOAD} = 1mA, V_{IN}=1.8V, V_{OUT}=1.5V.

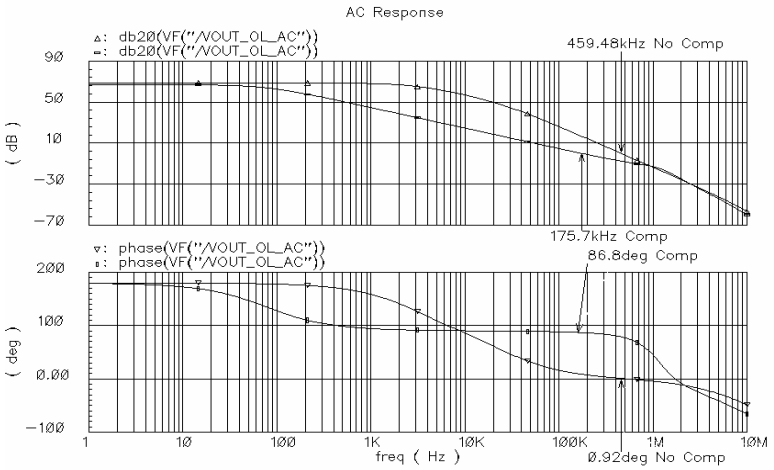


Fig. 38 AC frequency response for implementation I vs. ESR compensated w/ESR=0Ω for I_{LOAD} = 50mA, V_{IN}=1.8V, V_{OUT}=1.5V.

Implementation I, shown in Fig. 35, demonstrates suitable phase margin for the entire range of load currents as can be proven by observing Fig. 36 through Fig. 38. A graph showing the changes in output voltage, phase margin, and f_u is generated to show the trend of each parameter with changing current load. Fig. 39 shows the results of this simulation for implementation I.

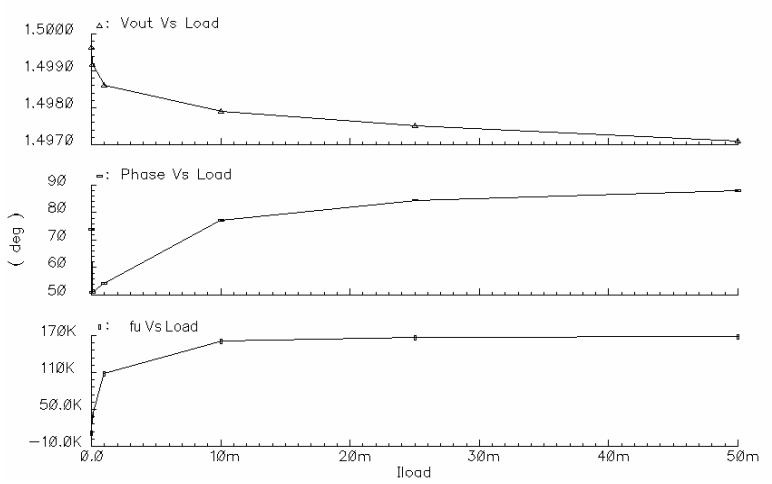


Fig. 39 Open loop V_{OUT}, phase margin and f_u vs. I_{LOAD}.

As is apparent from Fig. 39 as the load current increases the LDO becomes less accurate due to the fact that the loop gain drops with higher load currents. This will be shown in more detail in the load regulation results.

B. Transient Response

It is important to look at the response of the system to transient changes in load current when the LDO is in closed loop configuration. The results for implementation I can then be compared to implementation II and an LDO that is compensated with the ESR of the load capacitor. A square current source was set with a 1µs rise time and a period of 50µs in order to simulate the transient loads. All three programmable output voltage levels are investigated to verify the LDO's functionality with C_{LOAD} = 1µF and ESR = 0Ω. The capacitor's ESR value is set to 0Ω in order to verify the response of the LDO when implementation I of the compensation scheme is added by itself. Intermediate values of load transients were observed to ensure stable operation as well. The two important LDO parameters are extracted from these transient simulations: Deflection voltage and maximum peaking. Deflection voltage is defined as the difference between the final value of the output voltage right before a no-load to full load transition and the stabilized final value after that transition. This transition is the worst case

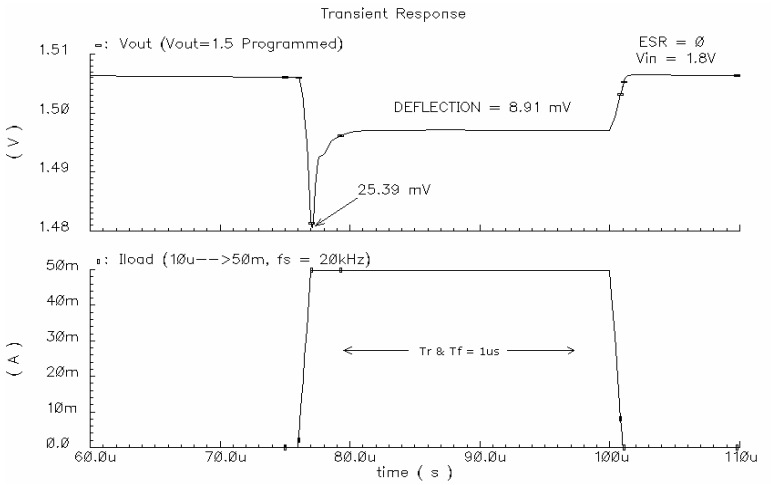
scenario of operation. Deflection voltage is also characterized by load regulation as was previously discussed in the performance metrics section of chapter II. Table XV summarizes the deflection and maximum peak results for all three programmable voltages.

TABLE XV

TRANSIENT CHARACTERISTICS FOR VARIOUS O/P LEVELS IMP. I

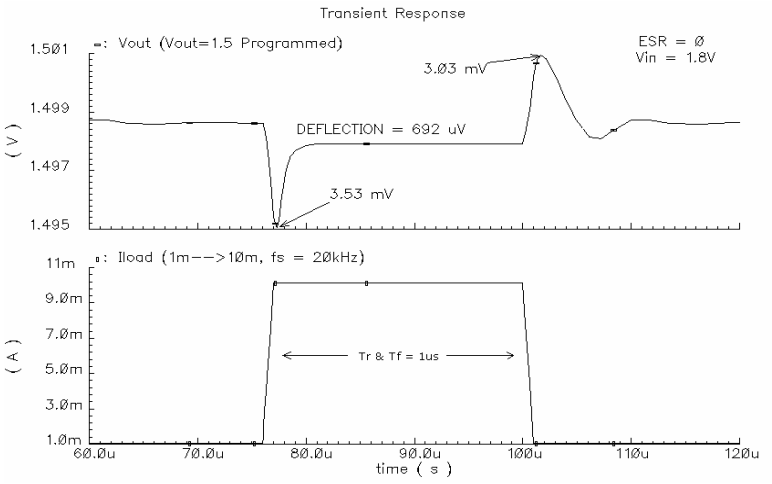
I_{LOAD}	Deflection	Max Peak
V_{OUT} = 0.9V		
10u-50mA	7.48 mV	19.67 mV
1mA-10mA	0.763 mV	2.80 mV
V_{OUT} = 1.5V		
10u-50mA	8.91 mV	25.39 mV
1mA-10mA	0.692 mV	3.53 mV
V_{OUT} = 1.8V		
10u-50mA	9.91 mV	26.41 mV
1mA-10mA	0.817 mV	3.816 mV

An example of the graphical results obtained for this transient simulation is shown in Fig. 40. These results can be extended to describe the 1.8V and 0.9V regulated cases.



(a)

Fig. 40 Transient response for implementation I w/ESR=0Ω for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} and V_{IN}=1.8V, V_{OUT}=1.5V.



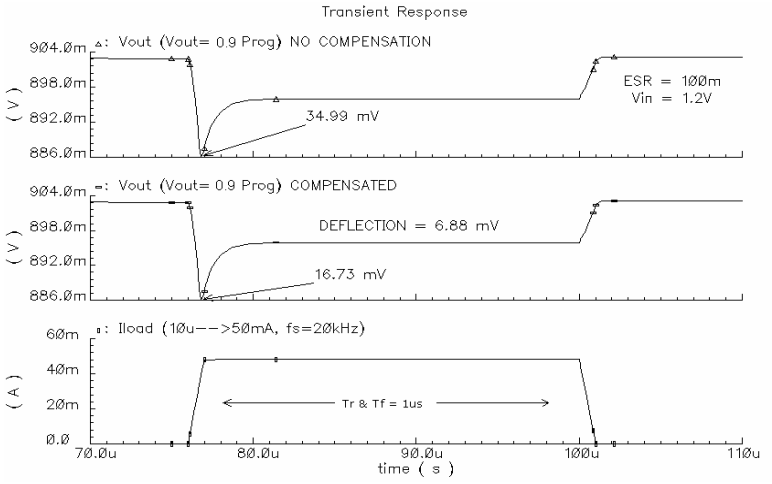
(b)

Fig. 40 Continued.

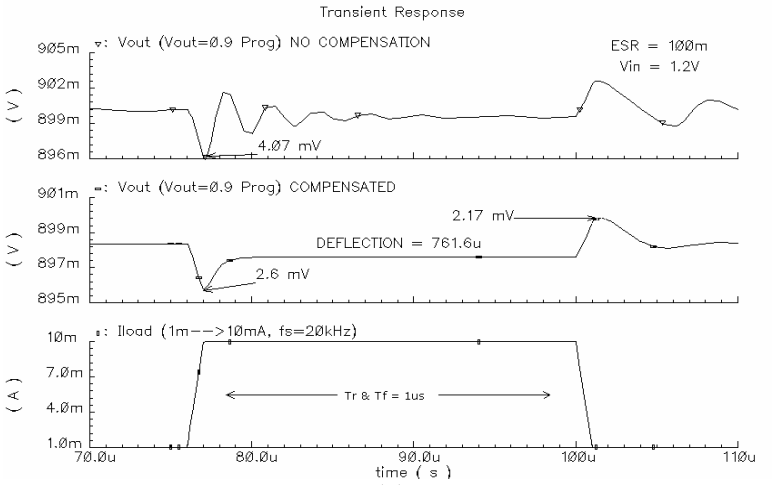
From these transient results it is clear that the LDO with the compensation implementation I can be deemed stable for the full range of load currents. If less phase margin was encountered, these plots would exhibit ringing and longer settling times. The settling time will be discussed in the following section.

C. Transient Response with ESR = 100mΩ

Transient simulations were run in order to compare the advantages of using this compensation scheme in comparison to an ESR compensated LDO. The following figures show an improvement in closed loop stability of the LDO when the proposed compensation scheme is used.



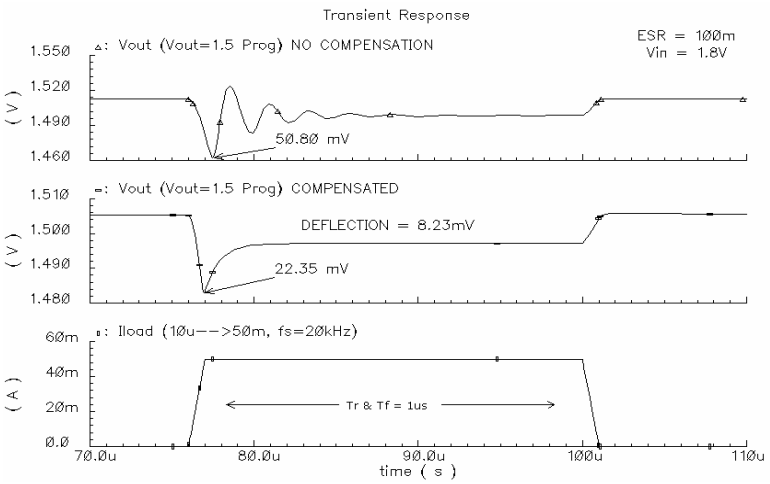
(a)



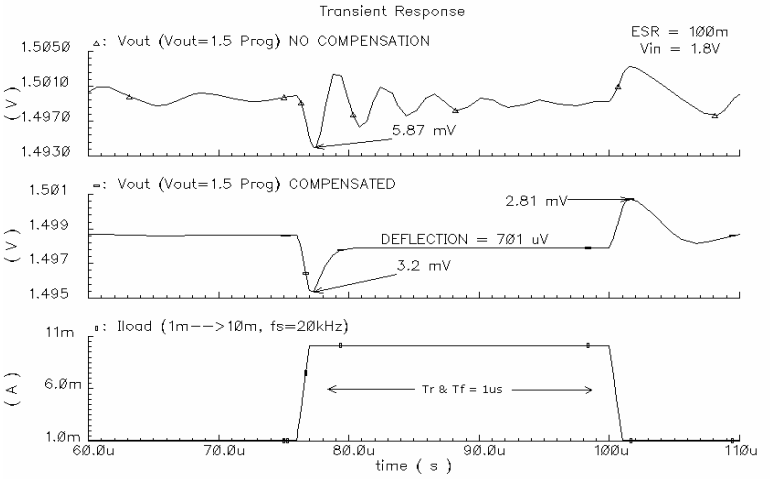
(b)

Fig. 41 Transient response for implementation I and ESR compensation w/ESR=100mΩ for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} and V_{IN}=1.2V V_{OUT}=0.9V.

The graphical interpretation of these results was deemed important to the description of the positive attributes of this topology; therefore, all three programmable voltage levels are shown in Fig. 41 through Fig. 43 respectively.

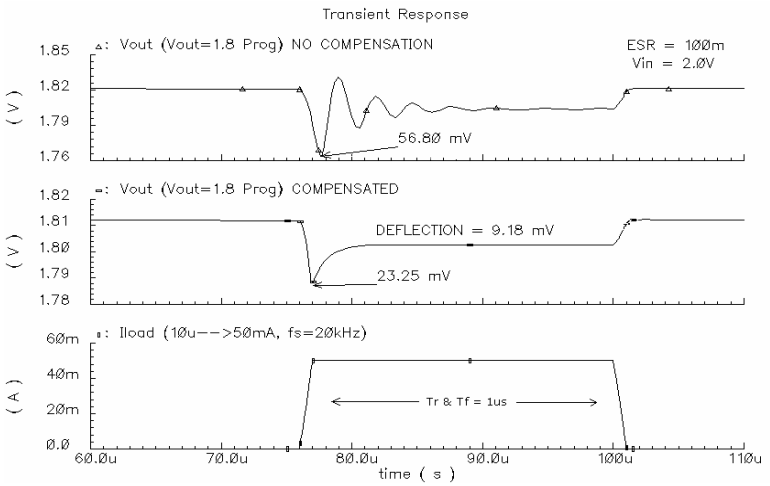


(a)

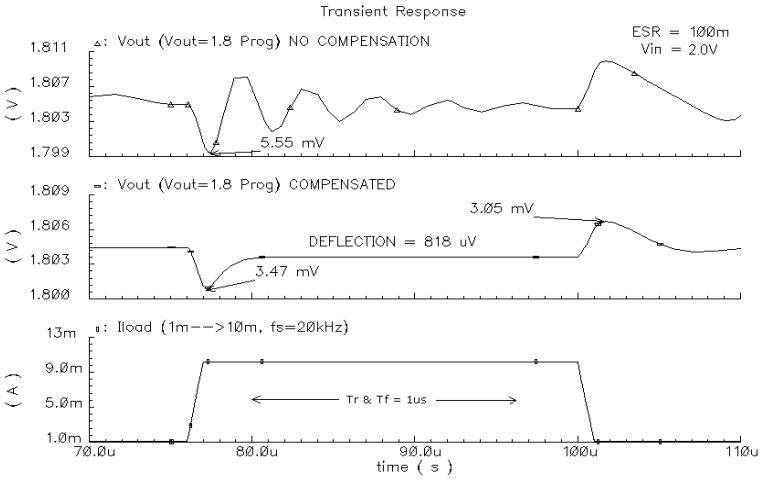


(b)

Fig. 42 Transient response for implementation I and ESR compensation w/ESR=100mΩ for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} and V_{IN}=1.8V_{OUT}=1.5V.



(a)



(b)

Fig. 43 Transient response for implementation I and ESR compensation w/ESR=100mΩ for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} and V_{IN}=2.0V, V_{OUT}=1.8V.

From the results shown in the previous figures it can be concluded that implementation I stabilizes the LDO much more accurately and much faster than an LDO compensated with just the ESR of the load capacitor. The full load settling time is the parameter that quantifies how fast the LDO actually responds. The load transient was modified to have a rise and fall time of 1ns and the step load current was set from 10µA to 50mA. The results for each programmable output are shown in Table XVI.

TABLE XVI

FULL LOAD TRANSIENT SETTLING TIME FOR IMP. I

V_{OUT}	Ts	Measured
0.9V	**1%**	< 1 µs
	0.1%	2.24 µs
1.5V	**1%**	< 1 µs
	0.1%	2.498 µs
1.8V	**1%**	< 1 µs
	0.1%	2.77 µs

The 1% settling time proved to be less than 1us for all cases. Therefore, a 0.1% settling time was measured in order to quantify the differences. These results are in line with what is expected of the faster acting differentiator path.

It can be concluded, from the transient and the full load settling time results, that the proposed implementation stabilizes the LDO and minimizes peaking. Fig. 41 through Fig. 43 demonstrate that with better phase margin response of the open loop as previously shown in the AC results section, the transient response is benefited as well. Therefore, improved transient response can be claimed when using the proposed architecture.

D. Noise Analysis

Noise simulations were performed on Implementation I of the LDO as well as an LDO compensated by using the ESR of the load capacitor. For CADENCE simulations, the reference voltage source was selected as the input noise source and the V_{OUT} node was selected as the output node. The LDO was placed in closed loop configuration. Flicker noise parameters were included in the model files for simulations. Flicker, or 1/f noise, is important because it is a frequency dependant parameter and since LDO's operate at relatively lower frequencies, flicker noise becomes relevant. The flicker coefficients used for these simulations are technology dependant and summarized in Table XVII.

TABLE XVII

TSMC 0.35µm FLICKER NOISE COEFFICIENTS

Device	K_f	A_f
P-MOS	2.1660E-28	1
N-MOS	3.9167E-28	1

Fig. 44 shows the equivalent output noise with the flicker noise coefficients from Table XVII, with respect to frequency when V_{OUT} is programmed to 1.5V with ESR compensation. The load current is swept as shown. From this simulation, the equivalent low frequency output noise is found to be 311.2µV/sqrt[Hz].

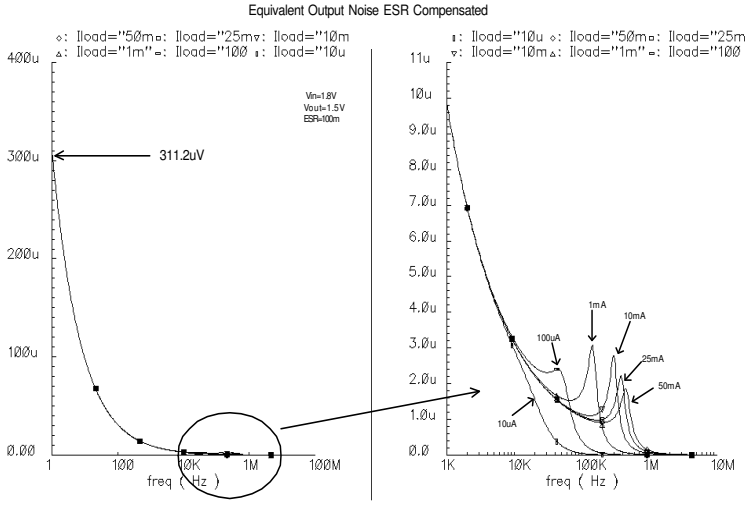


Fig. 44 Equivalent output noise for ESR compensated LDO with V_{IN}=1.8V, V_{OUT}=1.5V.

Fig. 45 shows the same result for the LDO compensated with implementation I. It shows a resultant low frequency noise of 336.8µV/sqrt[Hz]. This result shows a higher output noise density than the ESR compensated LDO. This is not surprising as 3 more transistors are used in the design of proposed implementation I. Therefore, it can be inferred that the additional noise is due to the addition of the devices in the compensation path.

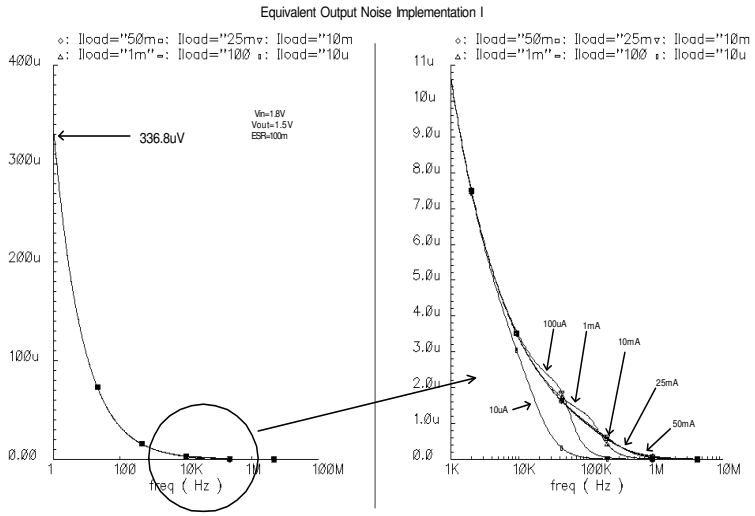


Fig. 45 Equivalent output noise for implementation I with V_{IN}=1.8V, V_{OUT}=1.5V.

The integrated output noise (including flicker coefficients) was also investigated and the results are shown in Table XVIII for V_{OUT} programmed to 1.5V. The BW for integrated noise is selected as 1-100kHz. The results demonstrate a variation of the noise with regard to load.

TABLE XVIII

IMP. I AND ESR COMPENSATED INTEGRATED NOISE V_{OUT}=1.5V

I_{LOAD}	O/P Int N. W/ Comp I	O/P Int N. ESR Comp
10µA	1.04 mV	0.978 mV
100µA	1.14 mV	1.10 mV
1mA	1.16 mV	1.092 mV
10mA	1.144 mV	1.065 mV
25mA	1.142 mV	1.063 mV
50mA	1.141 mV	1.062 mV

In conclusion, it is apparent that the overall noise is a little higher when implementation I is used vs. the ESR compensated LDO as can be seen from Fig. 45. This, as was mentioned before, can be attributed to the use of 3 more devices to generate the compensation network. If the compensation scheme was optimized for noise the area or the dc bias current would have to

be increased creating a trade-off between parasitic pole locations vs. noise or power consumption vs. noise.

Also, the main contributors to the noise of the entire system were found to be the transistors that form the differential pair and its load. Even though P-MOS devices were used for the differential pair, which inherently has less noise than N-MOS devices [21], they are at the first stage of the system. This means that whatever noise they contribute gets amplified by the following stages to appear at the output. In order to optimize for the noise of this first stage there are two options: increasing the area of those transistors (direct tradeoff with parasitic poles, but may be possible because f_u of system is low) and increasing the dc bias current (direct tradeoff with low power performance). One might be inclined to believe that the huge pass transistor would be the main noise contributor, but because the differential pair noise is amplified by all the stages in the system, these turn out to be the main noise contributors for implementation I.

E. Load Regulation

Load regulation was defined in chapter II as the measure of the circuit's ability to maintain the specified output voltage under varying load conditions [18]. This is an especially important characteristic for the programmable LDO proposed because it should be able to regulate 3 different output voltage levels. Quantifying the load regulation is done by measuring the change in output voltage level over a specified change in load current. Specifically, given by (47):

$$Load\ Regulation \equiv \frac{\Delta V_o}{\Delta I_o} \tag{47}$$

For CADENCE simulations, the output current is varied from 0-50mA in order to characterize the variation that can be expected from the system at a programmed output level. Once again, the LDO is placed in closed loop configuration and the load current is varied from 0 to 50mA.

Fig. 46 shows the resulting graph generated from this simulation with the three different available output voltages (1.8V, 1.5V and 0.9V).

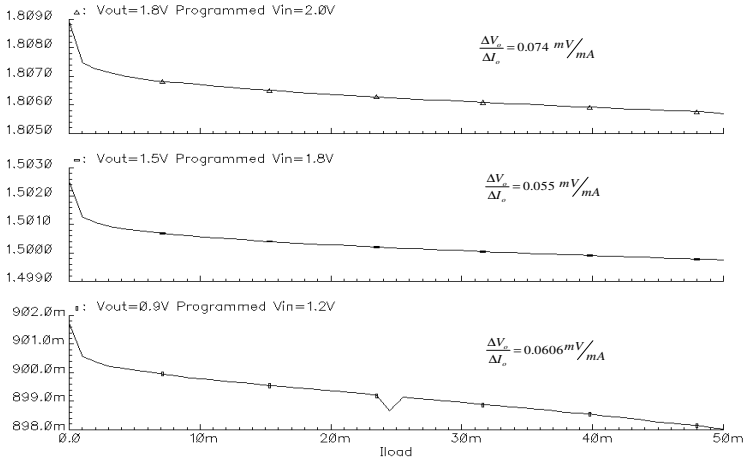


Fig. 46 Load regulation for implementation I.

The results shown in Fig. 46 demonstrate a small change in output voltage per mA change in load current. This is a positive characteristic of the proposed LDO because it presents less than 0.074mV/mA. This parameter can be improved by raising the open loop gain as was explained in chapter II.

F. Line Regulation

Line regulation was defined in chapter II as the measure of the circuit's ability to maintain the specified output voltage with a varying input voltage [18]. Line regulation is a closed loop characteristic for LDO's. To quantify line regulation, equation (48) is used:

$$Line\ Regulation \equiv \frac{\Delta V_o}{\Delta V_I} \tag{48}$$

Fig. 47 shows the results of varying the input voltage (V_{DD}) with a static I_{LOAD} = 1mA. The LDO is placed in closed loop configuration as it would be practically used. Each one of the output levels shows the respective line regulation value.

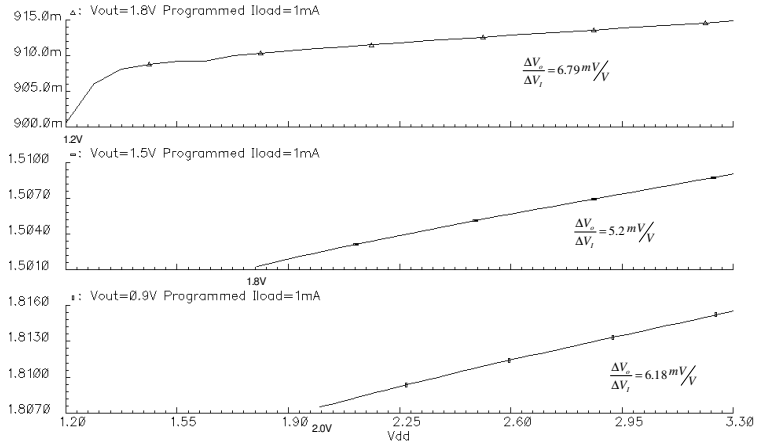
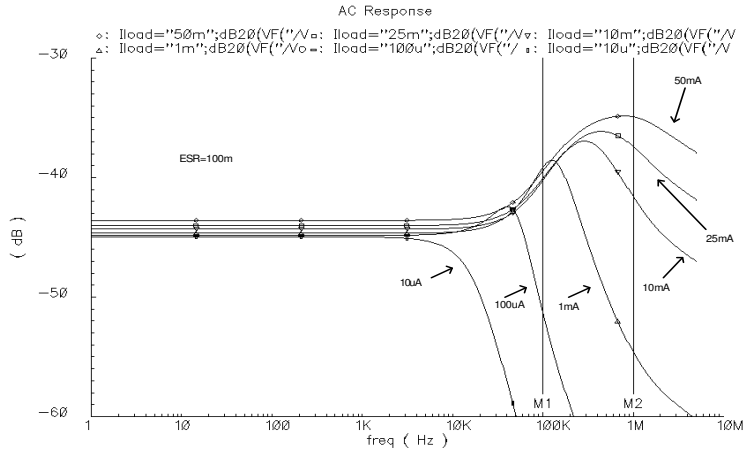


Fig. 47 Line regulation for implementation I.

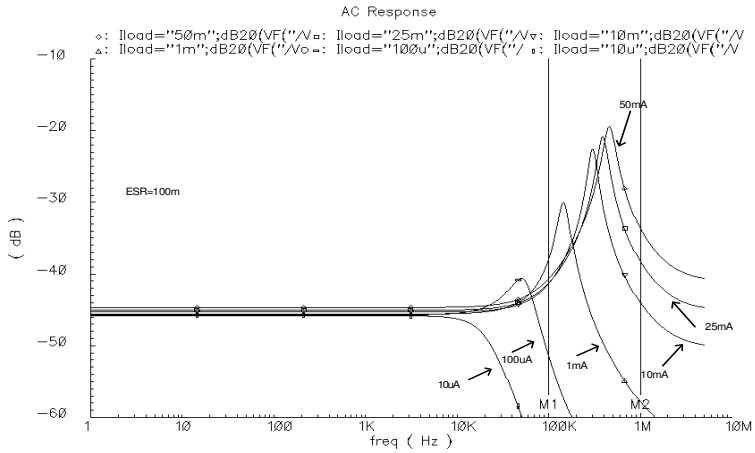
Another positive attribute found for this implementation of the LDO is that it can regulate the output voltage with a maximum deviation of 6.79mV/V to a maximum input voltage of 3.3V as shown in Fig. 47.

G. PSRR

For PSRR (Power Supply Rejection Ratio) simulations, an AC signal is introduced at the input of the regulator. PSRR is measured for the LDO with compensation implementation I and for the ESR compensated version of the LDO. The input voltage also serves as the power supply to the error amplifier, a contributor to PSRR performance of the overall system. Fig. 48 (a) shows the PSRR results for different load conditions when the LDO is compensated with implementation I. The load current is swept from 10μA to 50mA with a frequency range from 1Hz to 5MHz. Fig. 48 (b) shows the PSRR of the same LDO compensated with ESR for comparison purposes.



(a)



(b)

Fig. 48 PSRR for (a) implementation I and (b) ESR compensated.

When a dc/dc switch mode power supply (SMPS) is used to power the LDO, as is sometimes the case, the output ripple of the SMPS is within the frequency band of 100kHz to 1MHz, making this band-interval of specific interest [18]. As shown in Fig. 48 (a) and (b), there is an improvement in PSRR performance within this specific band when using the proposed implementation. The frequency domain characteristics of PSRR for compensation implementation I are summarized in Table XIX. The results for the LDO compensated with ESR are shown in Table XX.

TABLE XIX

PSRR SUMMARY FOR IMP. I

I_{LOAD}	PSRR @10Hz	PSRR @100kHz
10µA	-44.09 dB	-67.93 dB
100µA	-43.99 dB	-50.82dB
1mA	-43.82 dB	-38.96 dB
10mA	-43.52 dB	-40.08 dB
25mA	-43.26 dB	-39.92 dB
50mA	-42.88 dB	-39.36 dB

TABLE XX

PSRR SUMMARY FOR ESR COMPENSATED

I_{LOAD}	PSRR @10Hz	PSRR @100kHz
10µA	-45.81 dB	-69.51 dB
100µA	-45.73 dB	-51.24 dB
1mA	-45.59 dB	-38.22 dB
10mA	-45.31 dB	-41.46 dB
25mA	-45.06 dB	-41.37 dB
50mA	-44.68 dB	-40.76 dB

As can be seen from these two tables, the proposed implementation offers no benefits for PSRR at first glance. Now, carefully comparing Fig. 48 (a) and (b), it is obvious that there is a definite improvement in the specified band of interest. The proposed LDO has a minimum of 36dB of PSRR in that band for all current load conditions, while the ESR compensated LDO has a little as 20dB of PSRR in that band (100k-1MHz). This can be attributed to the fact that implementation I has a lower unity gain frequency.

H. Start-Up Time

In order to characterize the startup time of the circuit it is necessary to apply a step input with a fast rise time. The rise time was set to 1ns for the input (V_{DD}) and the startup time was measured to 1% settling. For a programmed output of V_{OUT} = 1.5V the startup time was found to be T_{su}~4.94µs (1% Settling) for an LDO compensated with implementation I. For an ESR

compensated system, the startup time was found as T_{su}~10.18µs (1% settling). These results are shown in Fig. 49.

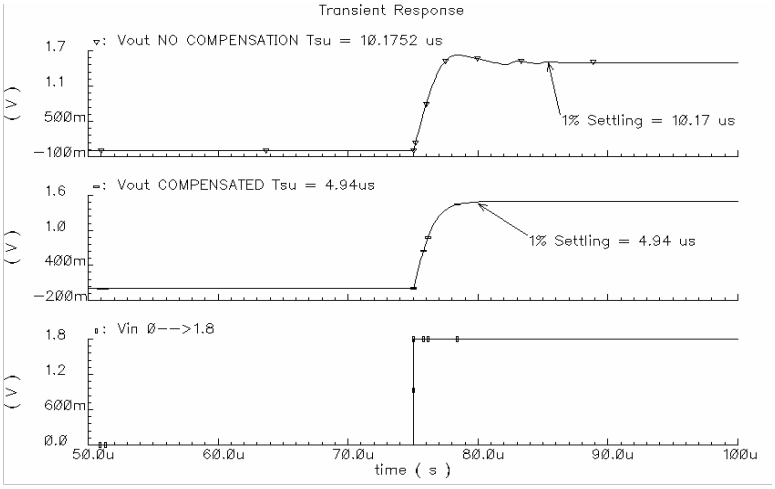


Fig. 49 Startup time for implementation I and ESR compensation w/V_{OUT}=1.5V.

Table XXI shows a summary of the startup time results for all three programmable output voltage levels. As can be seen from this table the LDO compensated with implementation I has better startup time than the ESR compensated version.

TABLE XXI

STARTUP TIME SUMMARY FOR IMP. I

V_{OUT}	1%Tsu Compensated I	1%Tsu ESR Comp.
0.9V	8.62 µs	13.44µs
1.5V	4.94 µs	10.18 µs
1.8V	5.649 µs	10.43 µs

I. Power Consumption/Ground Current

This system presents a DC current consumption of 48µA. This specification is well within the target range of <60µA. From the total 48µA consumption, 30µA are consumed by the error amplifier and 6µA are always running through the resistive feedback network for the case

when 1.5V is programmed at the output. Table XXII shows the summary of the DC current consumption for each of the programmed output levels.

TABLE XXII

DC CURRENT CONSUMPTION IMP. I

V_{OUT}	I_{DC} Amp	I_{DC} Res	I_{DC} Comp	I_{DC} Total
1.8V	30 µA	8.2 µA	12 µA	50.2 µA
1.5V	30 µA	6.66 µA	12 µA	48 µA
0.9V	30 µA	3.6 µA	12 µA	45.6 µA

There is an additional 12µA current consumption by the compensation scheme. However, this entire implementation still presents a power consumption of <60µA.

J. Process and Temperature Variations

A MonteCarlo Statistical Analysis was run on the system with implementation I. V_{THO} and μ_o were varied by 20% in order to obtain results for process parameter variations. Fig. 50 shows the results for unity gain frequency obtained.

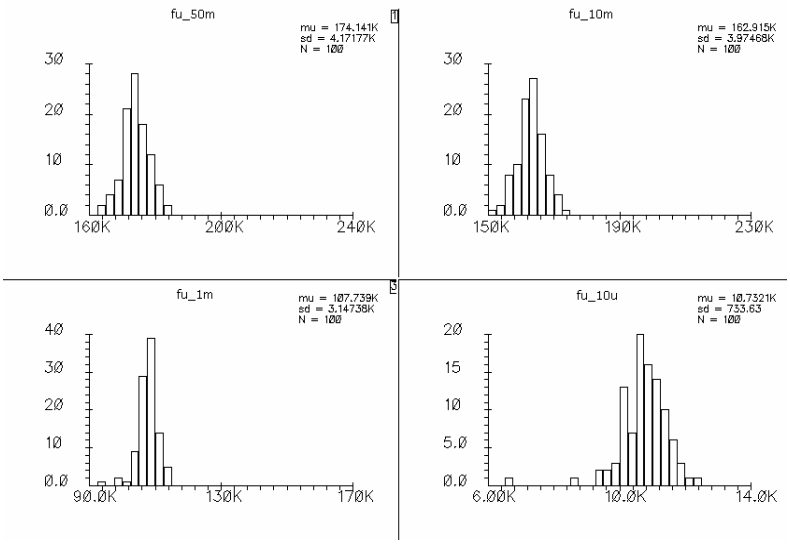


Fig. 50 Process parameter variations for f_u, implementation I.

It is evident that the unity gain frequency can be considered statistically robust for 20% parameter variation. The majority of the bins appear very close together as can be expected from a system that is not at the mercy of process parameter variations.

Fig. 51 shows that for phase margin results, even the most critical of all cases (intermediate current loads) present greater than 50° of phase margin when the before mentioned process parameters are varied by 20%. This is another positive attribute of the proposed LDO as the transient response is very much related to the amount of phase margin the LDO has in open loop operation, as was previously discussed.

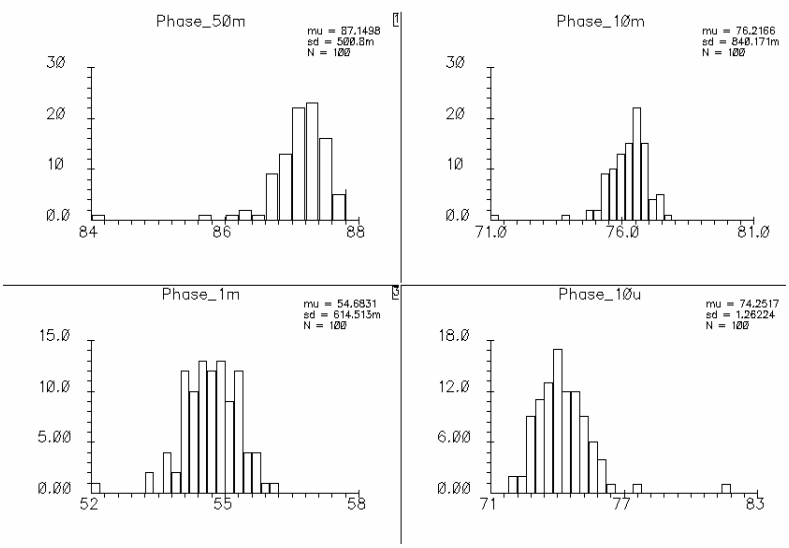


Fig. 51 Process parameter variations for phase margin, implementation I.

Fig. 52 shows the results for the DC Voltage level at the output for the variations in process parameters. Even though the ideal programmed voltage is set at 1.5V there are small variations that can be attributed to the overall offset of the system.

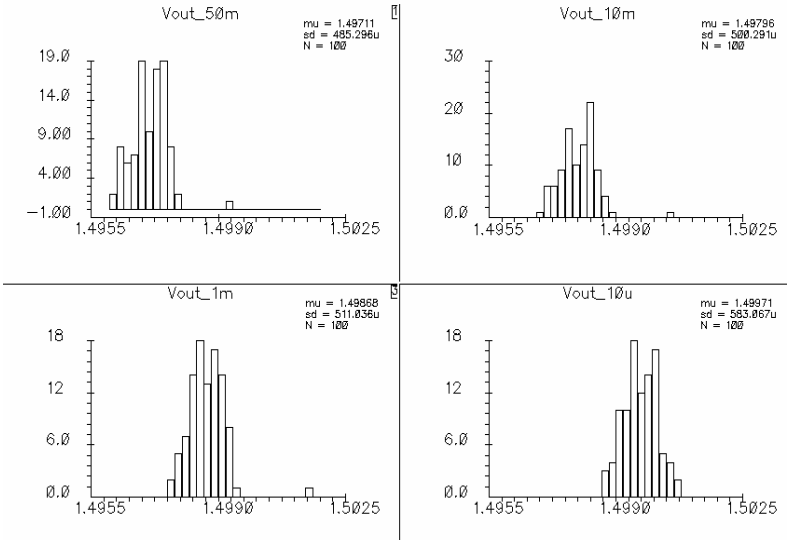


Fig. 52 Process parameter variations for V_{OUT}, implementation I.

The results obtained by running MonteCarlo simulations within CADENCE show that, statistically, the LDO is robust, as proven from Fig. 51 and Fig. 52, for the measured parameters when varying threshold voltage and carrier mobility in the technology files by 20%.

For temperature variations, the transient response was revised at three different temperatures (-40°, 27°, and 120°C). The results are shown in Fig. 53 for a V_{OUT} = 1.5V with a V_{IN} = 1.8V.

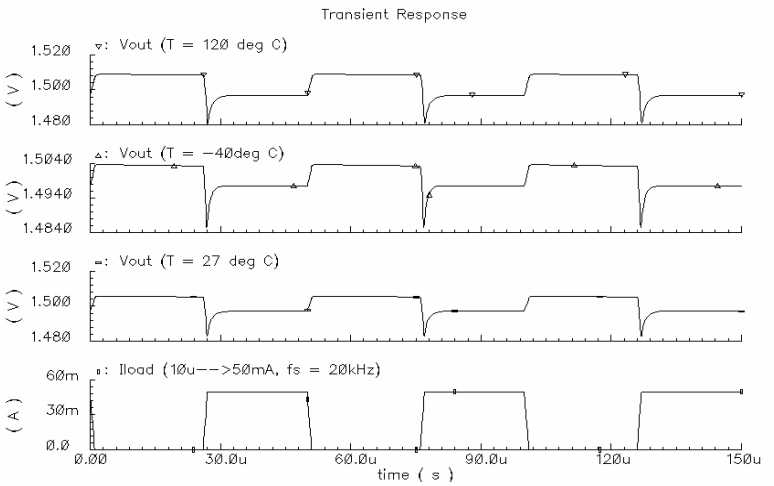


Fig. 53 Temperature variations for V_{OUT}, implementation I.

It can be seen in the previous figure that the LDO is robust to changes in temperature when it is in practical operation (i.e. closed loop transient response).

2. Phase Compensation Implementation II

A. AC Performance

In order to guarantee the stability of implementation II, the same measurements and characterization is carried out. As was stated in chapter III only the compensation scheme is different between the two topologies. The same conditions for simulations are used for implementation II as were used for implementation I in order to validate comparisons. Fig. 54 shows implementation II in its entirety. The location where the closed loop is broken and the manner in which it is broken are the same as for implementation I as well.

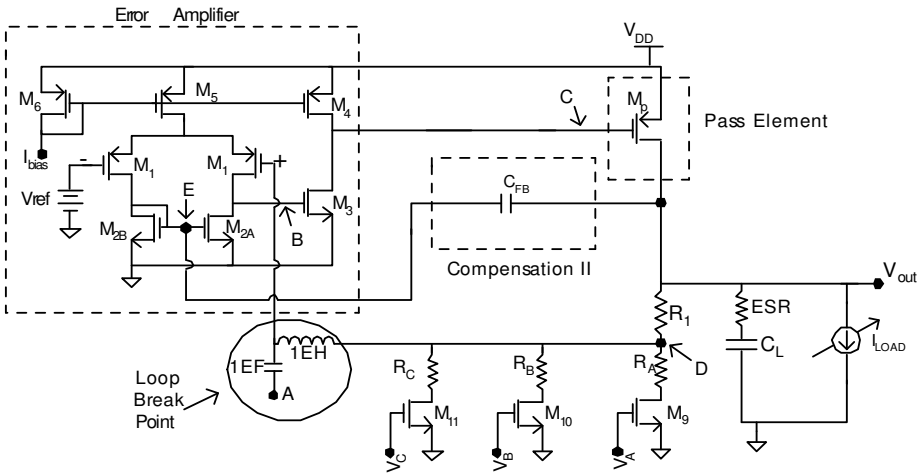


Fig. 54 Loop break point for implementation II.

AC frequency response simulations were carried out in the same manner as they were for implementation I. The same transistor level amplifier, pass transistor, feedback resistors and switch designs were used in order to make the implementation comparisons valid as was

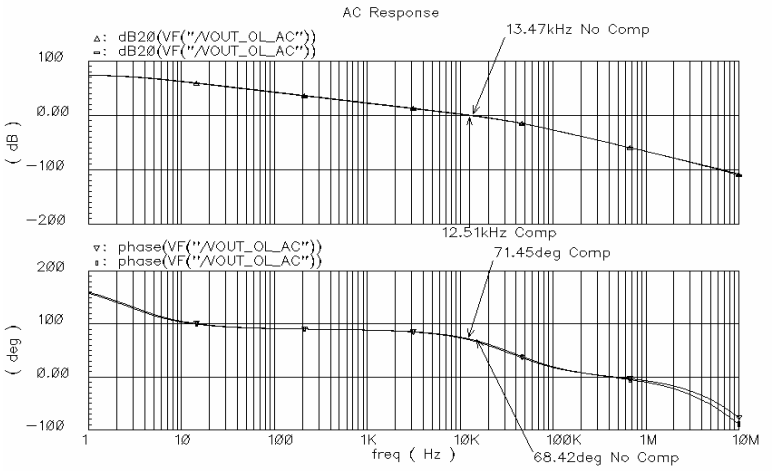
previously stated. The results for implementation II are summarized in Table XXIII. A couple of the sample simulations are presented.

TABLE XXIII

AC CHARACTERISTICS FOR IMP. II

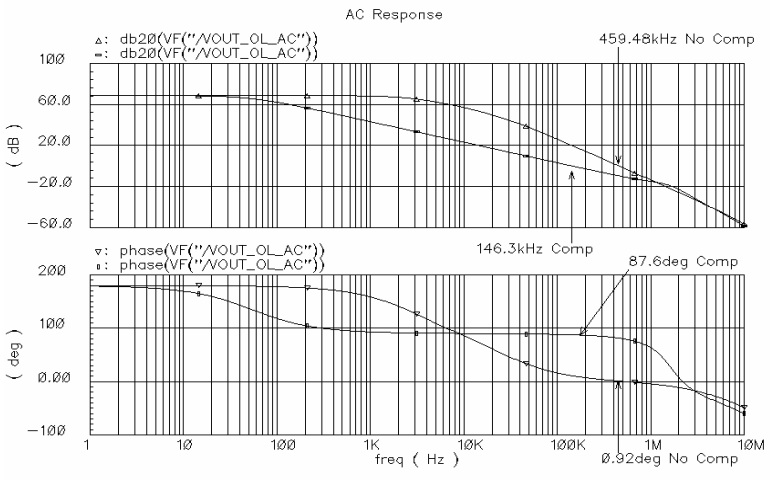
I_{LOAD}	Av@1Hz	GBW	PM
10µA	73.92 dB	12.51 kHz	71.45°
100µA	76.33 dB	43.6 kHz	51.03°
1mA	76.61 dB	107.5 kHz	59.81°
10mA	74.74 dB	142.6 kHz	80.31°
25mA	72.21 dB	145.7 kHz	85.3°
50mA	68.69 dB	146.3 kHz	87.6°

For implementation II, the two extreme load current cases are shown in Fig. 55 (a) and (b). Superimposed with these results is the AC response of the ESR compensated LDO.



(a)

Fig. 55 AC frequency response for implementation II vs. ESR compensated w/ESR=0Ω for I_{LOAD} (a) = 10µA (b) = 50mA V_{IN}=1.8V, V_{OUT}=1.5V.



(b)

Fig. 55 Continued.

It can be inferred that the system demonstrates suitable phase margin, as the LDO has more than 50° of phase margin over the entire range of load currents (10µA-50mA), shown in Table XXIII. A graph showing the changes in output voltage, phase margin, and f_u is generated to show the tendency with changing load. Fig. 56 shows that with changing load the LDO will regulate the voltage to an output of 1.5V within a deviation of 2.8mV.

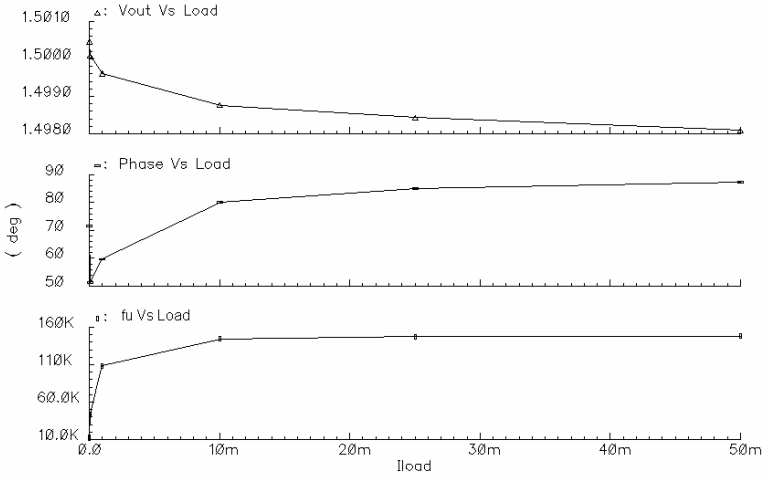


Fig. 56 Open loop V_{OUT}, phase margin and f_u Vs. I_{LOAD}.

This result is directly comparable to Fig. 39 for implementation I because with increasing load current the loop gain is dropping, which leads to less accuracy.

B. Transient Response

It is important to look at the response of the system with implementation II in order to be able to compare the results with those from an ESR compensated LDO and the system compensated with implementation I. This response was obtained under the same conditions as implementation I. The square current source was set with a 1μs rise time with a period of 50μs. All three programmable output voltage levels are investigated to verify the LDO's functionality with C_{LOAD} = 1μF and ESR = 0Ω. Deflection voltage and maximum peaking are summarized in Table XXIV for all programmable output cases. As can be seen from this table, implementation II proves to have better performance than both implementation I and the LDO compensated with ESR. A formal comparison between all the results will be carried out with post-layout simulations in chapter VI.

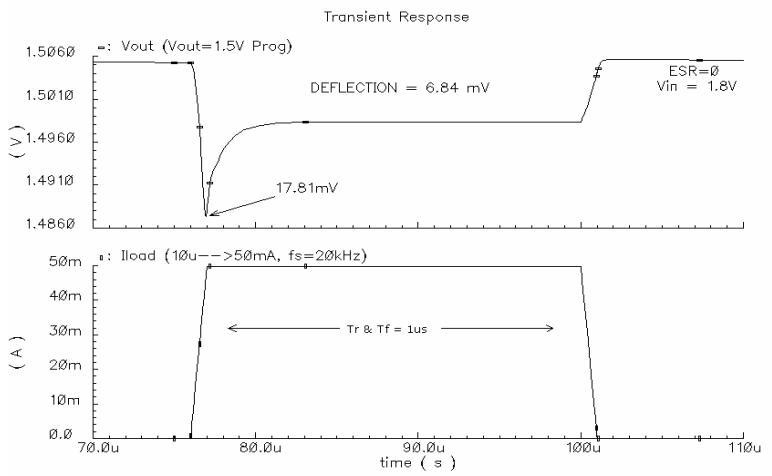
TABLE XXIV

TRANSIENT CHARACTERISTICS FOR VARIOUS O/P LEVELS IMP. II

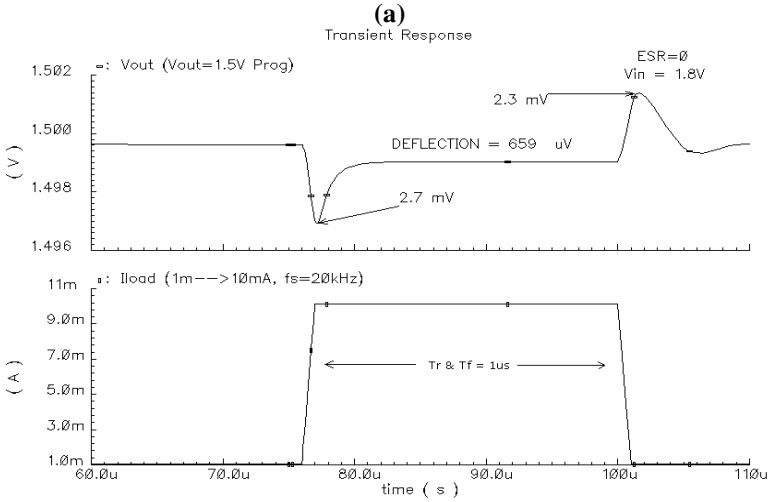
I_{LOAD}	Deflection	Max Peak
V_{OUT} = 0.9V		
10u-50mA	5.15mV	13.1mV
1mA-10mA	0.544mV	1.93mV
V_{OUT} = 1.5V		
10u-50mA	6.84mV	17.81mV
1mA-10mA	0.659mV	2.7mV
V_{OUT} = 1.8V		
10u-50mA	7.61mV	18.45mV
1mA-10mA	0.689mV	2.85mV

Once again, the results for a V_{OUT} = 1.5V are shown for implementation II in Fig. 57. It can be seen that deflection is lower for implementation II as well as lower maximum peaking is

obtained. This can be attributed to the fact that no DC signal is introduced by this compensation, thus, no DC level are changed as is the case for implementation I.



(a)



(b)

Fig. 57 Transient response for implementation II w/ESR=0Ω for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} and V_{IN}=1.8V, V_{OUT}=1.5V.

These transient results further support the stability claim proposed using the AC simulation outcome. As shown in Fig. 57, implementation II regulates the desired programmed level.

C. Transient Response with ESR = 100mΩ

Transient simulations were run in order to investigate the advantages of using this compensation scheme in comparison to an ESR compensated LDO and an LDO compensated with implementation I.

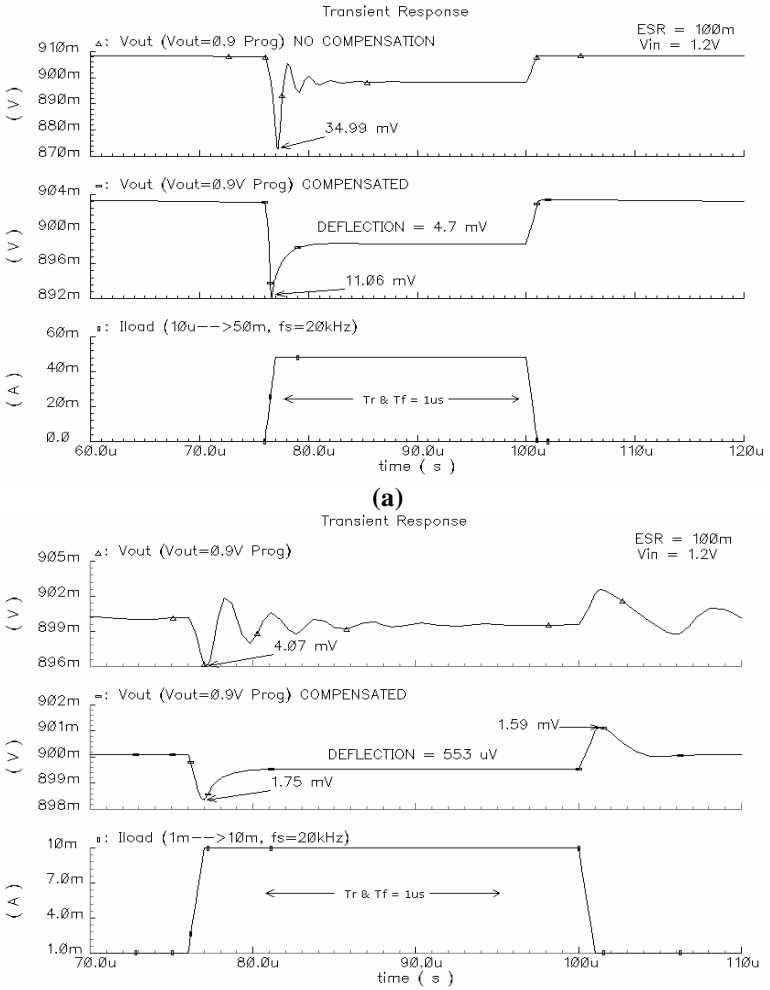
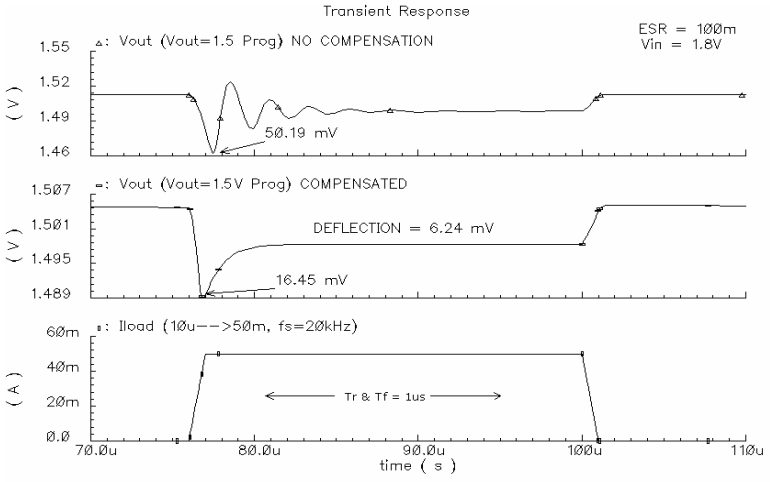
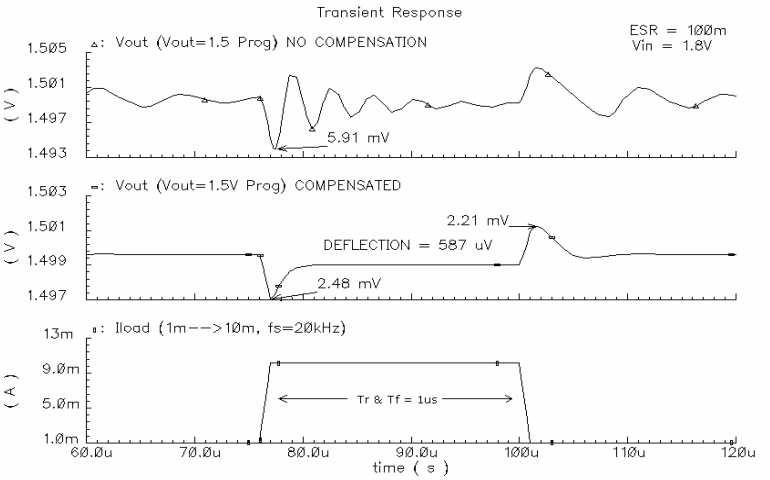


Fig. 58 Transient response for implementation II & ESR compensation w/ESR=100mΩ for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} & V_{IN}=1.2V, V_{OUT}=0.9V.



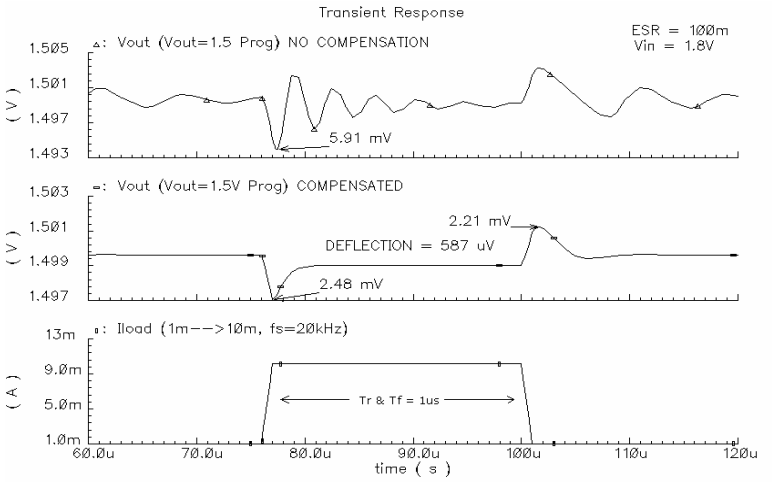
(a)



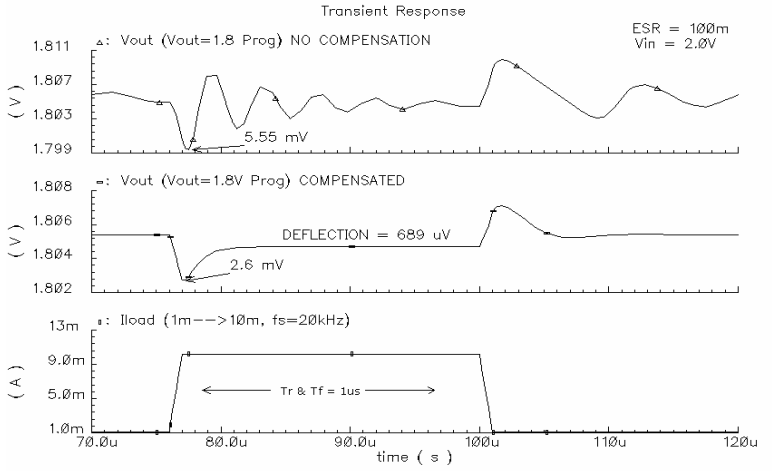
(b)

Fig. 59 Transient response for implementation II and ESR compensation w/ESR=100mΩ for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} and V_{IN}=1.8V, V_{OUT}=1.5V.

For this simulation all three programmable levels are shown because these results are considered the basis of the advantages obtained when using the proposed implementation II.



(a)



(b)

Fig. 60 Transient response for implementation II & ESR compensation w/ESR=100mΩ for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} & V_{IN}=2.0V, V_{OUT}=1.8V.

Fig. 58 through Fig. 60 are directly comparable with Fig. 41 through Fig. 43. These transient simulations were carried out with the same setup as implementation I, as previously stated. The results for implementation II are deemed superior in closed loop performance when directly comparing them to the results for transient response of implementation I.

The full load transient was also repeated on implementation II. Table XXV shows that implementation II settles faster than implementation I.

TABLE XXV

FULL LOAD TRANSIENT SETTLING TIME FOR IMP. II

V_{OUT}	Ts	Schematic
0.9V	**1%**	< 1 µs
	0.1%	1.39 µs
1.5V	**1%**	< 1 µs
	0.1%	1.907µs
1.8V	**1%**	< 1 µs
	0.1%	2.4 µs

In conclusion it has been shown that implementation II shows an improvement in transient performance over implementation I. As was previously discussed, the fact that implementation II is a purely AC feedback path contributes to better DC performance as it will not change the DC operating points of the nodes to which it is connected like implementation I.

D. Noise Analysis

Noise simulations were performed on Implementation II of the LDO as well. The same simulation setup was used as for implementation I. The flicker noise coefficients are also included in these simulations. Fig. 61 shows the equivalent output noise with respect to frequency when V_{OUT} is programmed to 1.5V with implementation II. As can be seen the equivalent output noise level is found to be 311.3µV/sqrt[Hz].

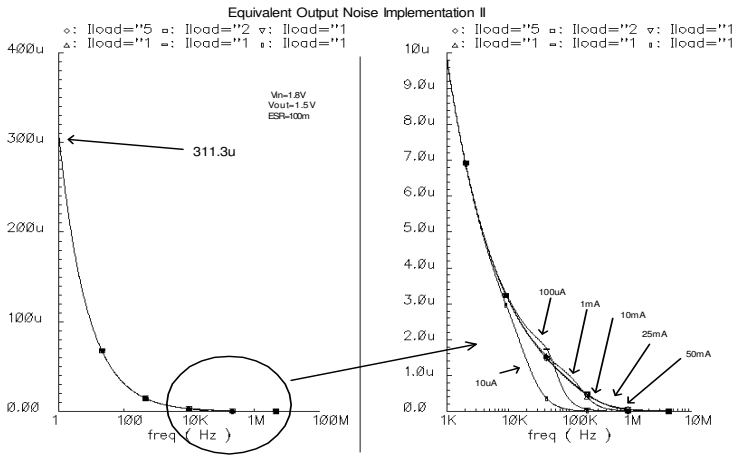


Fig. 61 Equivalent output noise for implementation II V_{IN}=1.8V, V_{OUT}=1.5V.

As was expected, the noise was lowered when compared to implementation I. This further supports the claim that the transistors used in implementation I introduced noise into the system.

The integrated output noise was also investigated and the results are shown in Table XXVI for V_{OUT} programmed to 1.5V. The integrated noise was found over the BW of 1-100kHz as well. The results demonstrate a variation of the noise with regard to load as well as slightly better performance when the LDO is compensated with Implementation II when compared to an ESR compensated LDO.

TABLE XXVI

IMP. II AND ESR COMPENSATED INTEGRATED NOISE V_{OUT}=1.5V

I_{LOAD}	O/P Int N. W/ Comp II	O/P Int N. ESR Comp
10µA	0.972 mV	0.978 mV
100µA	1.05 mV	1.10 mV
1mA	1.06 mV	1.092 mV
10mA	1.05 mV	1.065 mV
25mA	1.05 mV	1.063 mV
50mA	1.05 mV	1.062 mV

Once again the main contributors to the noise of the system are the input pair transistors. It is expected that if the only changes between implementation I and II is the compensation scheme, then everything else must remain the same. However, the noise does drop when compared to implementation I because proposed implementation II does not need extra devices in the feedback; it simply takes advantage of what is already there.

E. Load Regulation

The simulation for load regulation is conducted in the same fashion as for implementation I. The results are also presented in the same manner with expression (47) used to quantify the load regulation. Fig. 62 shows that the maximum value for load regulation occurs when the output is programmed at 1.8V.

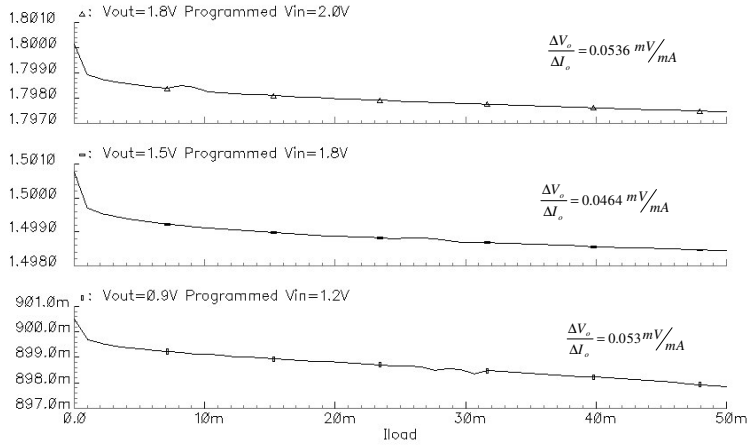


Fig. 62 Load regulation for implementation II.

Implementation II presents lower load regulation values due to the fact that it uses a purely AC feedback path. The capacitor used in the feedback connects to an already existing node in the LDO. Due to the nature of this feedback, it does not interrupt the DC biasing of that node. Implementation I, on the other hand, must have matching DC current through the feedback

branch; otherwise, a small dc offset will occur that appears at the output that will in turn degrade load regulation performance as is apparent in transient simulations as well.

F. Line Regulation

Line regulation was characterized in the same manner as it was done for implementation I. Fig. 63 shows each one of the output programmed levels and their corresponding line regulation results.

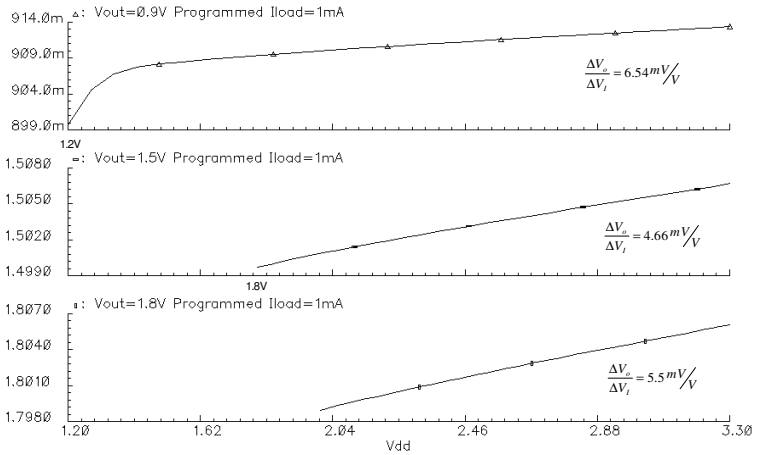


Fig. 63 Line regulation for implementation II.

Implementation II presents superior performance in line regulation than implementation II. This can be attributed once again to the fact that implementation II uses a purely AC feedback path and is not dependent on any mismatching like the feedback network in implementation I.

G. PSRR

PSRR is also verified for implementation II. The same setup is used to obtain PSRR results as was used for implementation I. Fig. 64 shows the result of the PSRR simulation for implementation II. For the important band of 100kHz-1MHz, the PSRR of implementation II has a minimum of 37dB as shown in Fig. 64.

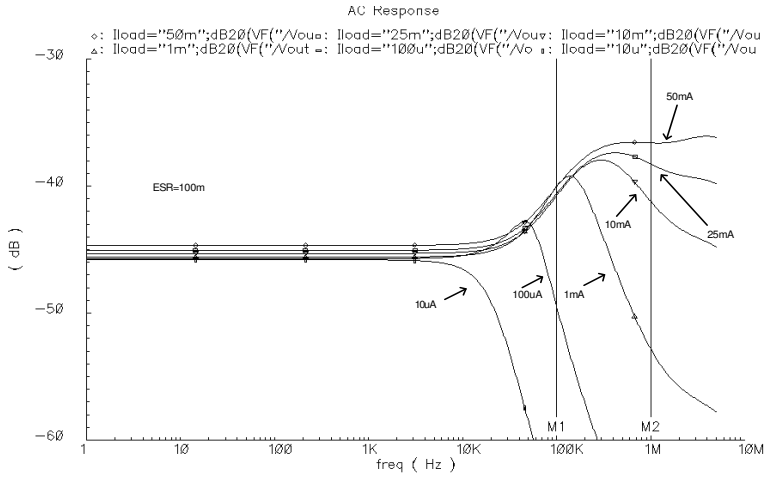


Fig. 64 PSRR for implementation II.

The frequency domain characteristics of PSRR for implementation II are summarized by load current in Table XXVII. When comparing these results to those obtained for implementation I, they are approximately equal. Although, implementation II presents a slightly better PSRR performance for the 100kHz-1MHz band.

TABLE XXVII

PSRR SUMMARY FOR IMP. II

I_{LOAD}	PSRR @10Hz	PSRR @100kHz
10µA	-45.81 dB	-66.51 dB
100µA	-45.72 dB	-49.52 dB
1mA	-45.59 dB	-40.20 dB
10mA	-45.31 dB	-40.94 dB
25mA	-45.06 dB	-40.75dB
50mA	-44.69 dB	-40.23 dB

H. Start-Up Time

In order to characterize the startup time of the circuit it is necessary to apply a step input with a fast rise time. This simulation was carried out for all three programmable output cases and

under the same conditions as for implementation I. Fig. 65 shows an example of the simulation results for the startup time measurement for implementation II.

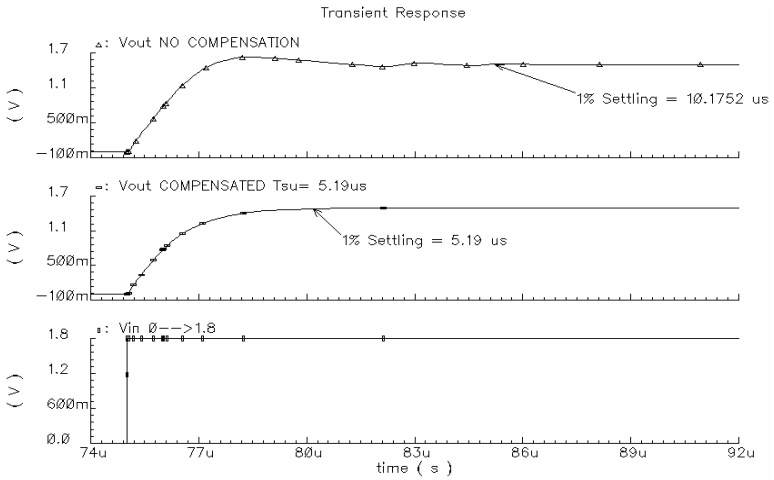


Fig. 65 Startup time for implementation II and ESR compensation w/V_{OUT}=1.5V.

The overall results for all three cases can be seen in Table XXVIII. It is apparent when comparing these results that this system presents similar startup performance than implementation I and faster than the ESR compensated version.

TABLE XXVIII

STARTUP TIME SUMMARY FOR IMP. II

V_{OUT}	1%Tsu Compensated II
0.9V	9 µs
1.5V	5.19 µs
1.8V	6.04 µs

I. Power Consumption/Ground Current

Implementation II presents a DC current consumption of 36µA, a 12µA reduction in quiescent current consumption when compared to implementation I. Table XXIX shows the amount of DC current that is consumed for each programmable output case.

TABLE XXIX

DC Current Consumption Imp. II

V_{OUT}	I_{DC} Amp	I_{DC} Res	I_{DC} Comp	I_{DC} Total
1.8V	30 µA	8.2 µA	0 µA	38.2 µA
1.5V	30 µA	6.66 µA	0 µA	36 µA
0.9V	30 µA	3.6 µA	0 µA	33.6 µA

A very positive characteristic of implementation II is that there is no additional ground current consumption in the compensation implementation meaning the compensation is carried out by a capacitor. This makes implementation II very attractive for low-power applications. This is because all the elements are already in the system to begin with.

J. Process and Temperature Variations

A MonteCarlo statistical analysis was also simulated for implementation II. The circuit presents robustness for 20% variations in V_{THO} and μ_o as can be seen in Fig. 66 through Fig. 68.

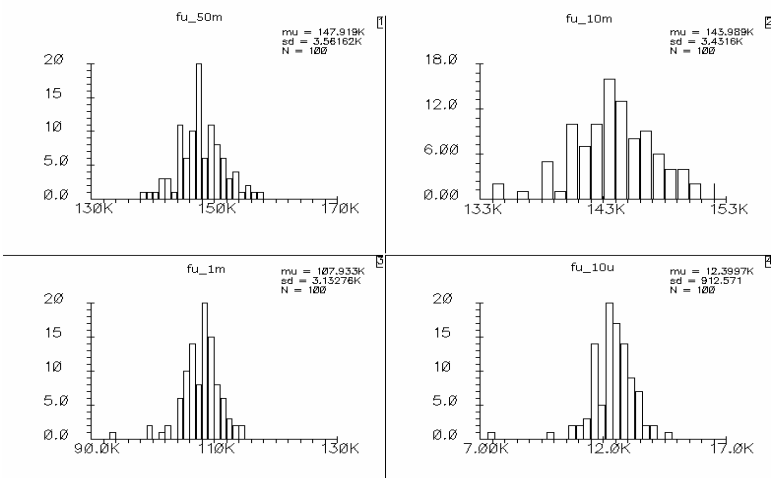


Fig. 66 Process parameter variations for f_u, implementation II.

Shown in Fig. 66 is the result for unity gain frequency. It is apparent that the entire samples lie close together, making the circuit robust for unity gain frequency to 20% variations.

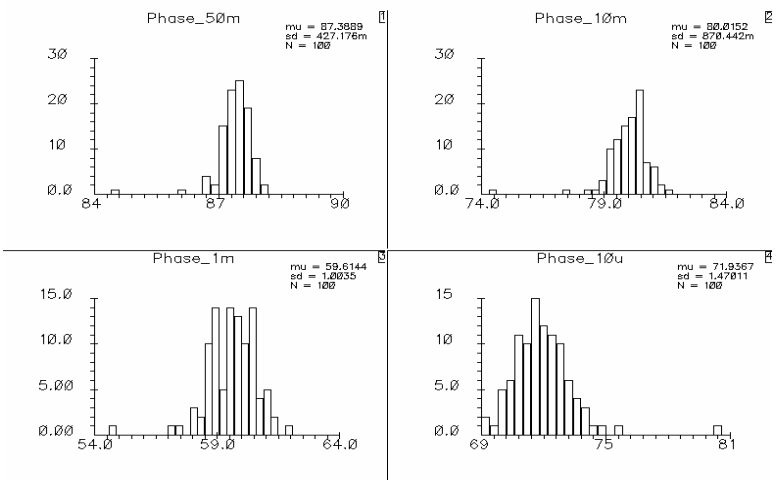


Fig. 67 Process parameter variations for phase margin, implementation II.

Fig. 67 shows all the simulated samples at >50° of phase margin. These results exhibit slightly more robustness than implementation I because there are no transistors in the compensation that can be affected by the variations introduced in the simulation.

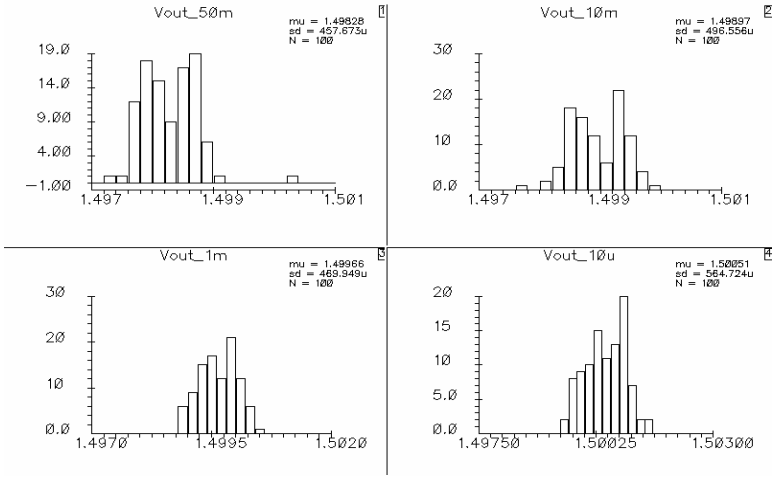


Fig. 68 Process parameter variations for V_{OUT}, implementation II.

Fig. 68 was obtained by also programming the output level to 1.5V. There is a slight deviation from 1.5V because of the changing loop gain with changing load. This effect is expected as it agrees with the load regulation results.

The temperature was also varied for implementation II and the transient results are shown in Fig. 69. This simulation was also carried out with the same variations as implementation I. The results of varying the temperature show that the system will still regulate to the programmed output voltage with changes in temperature.

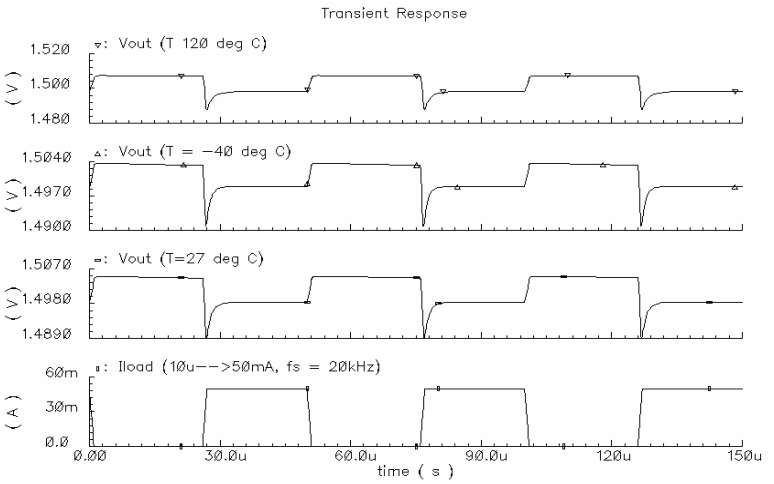


Fig. 69 Temperature variations for V_{OUT}, implementation II.

Overall, both proposed implementations can be considered to increase the phase response of an LDO, therefore an increase in transient performance should ensue. This has been proven to be precisely the case for both proposed implementations. Implementation II, however, accomplishes the required stability without a compromise in noise and DC current consumption.

CHAPTER V

POST-LAYOUT SIMULATED RESULTS

Presented throughout this chapter are the results of post-layout simulations on the proposed LDO's, implementation I and implementation II. These results are used to compare results in performance metrics between schematic and post-layout simulations in order to validate the post-layout view.

1. Phase Compensation Implementation I

A. Layout for Implementation I

The layout for implementation I is shown in Fig. 70. The layout for this implementation occupies a total die area of 0.222mm^2. Once the layout was analog extracted, the corresponding simulations were run on that view of implementation I. Analog extraction included all parasitic capacitances for more realistic results.

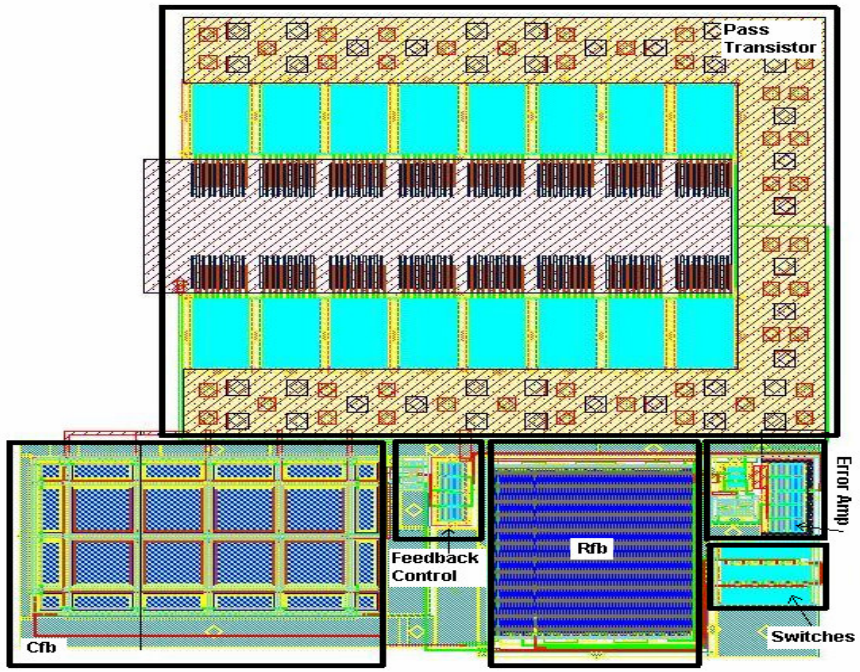


Fig. 70 Implementation I layout.

B. Post-Layout Transient Results

Post-layout simulations were carried out on the extracted version of the LDO compensated with implementation I to verify that the post-layout results match the results predicted by the schematic. The extracted version includes parasitic capacitances and thus replicates real world performance more closely and some variation is, therefore, expected. Table XXX shows the summarized results for transient operation of the circuit with a 1μF load capacitor and an ESR value set to 0Ω. It also details, in parenthesis, the percent variation from the values obtained for schematic simulations. The maximum variation in results was 3.6% while the minimum was 0.29%.

TABLE XXX

POST-LAYOUT TRANSIENT CH. FOR VARIOUS O/P LEVELS IMP. I

I_{LOAD}	Deflection	Max Peak
V_{OUT} = 0.9 V Prog.		
10μA-50mA	7.7mV (0.29%)	20.11mV (2.23%)
1mA-10mA	0.782mV (2.5%)	2.9mV (3.6%)
V_{OUT} = 1.5V Prog.		
10μA-50mA	9.13mV (2.4%)	26.1mV (2.8%)
1mA-10mA	0.709mV (2.4%)	3.64mV (3.11%)
V_{OUT} = 1.8 V Prog.		
10μA-50mA	10.1mV (1.9%)	27mV (2.23%)
1mA-10mA	0.826mV (1%)	3.9mV (2.2%)

Fig. 71 shows an example of the post-layout simulated results when the output voltage is programmed to 1.5V. The data presented in Table XXX is taken from graphs generated in the same way as shown in Fig 71.

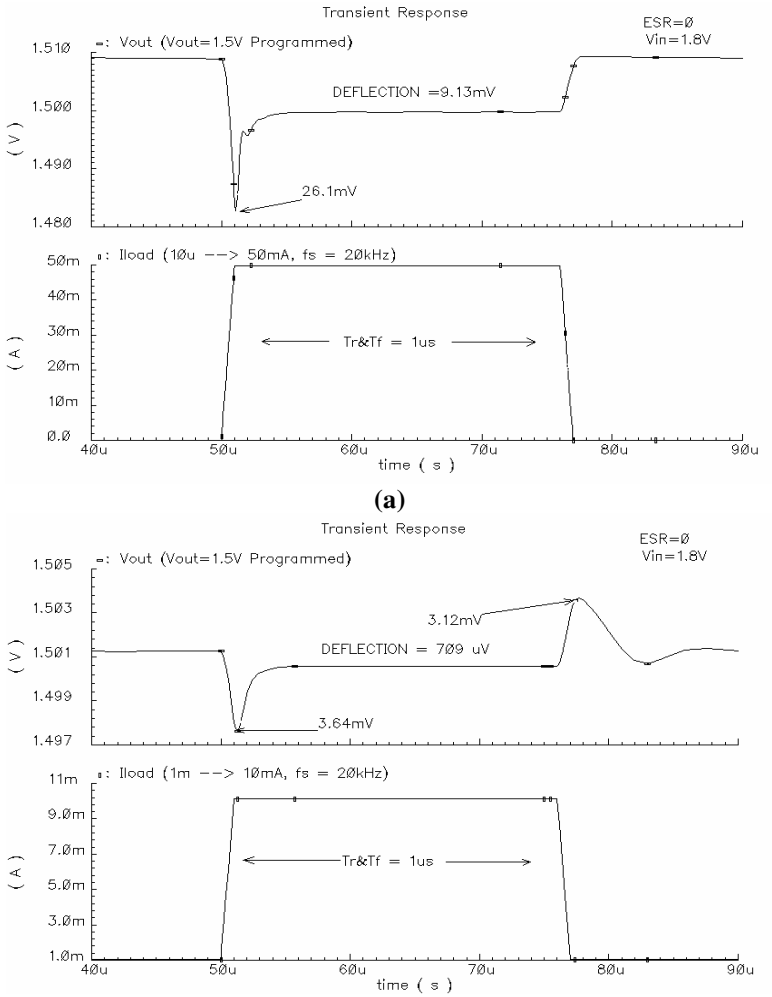


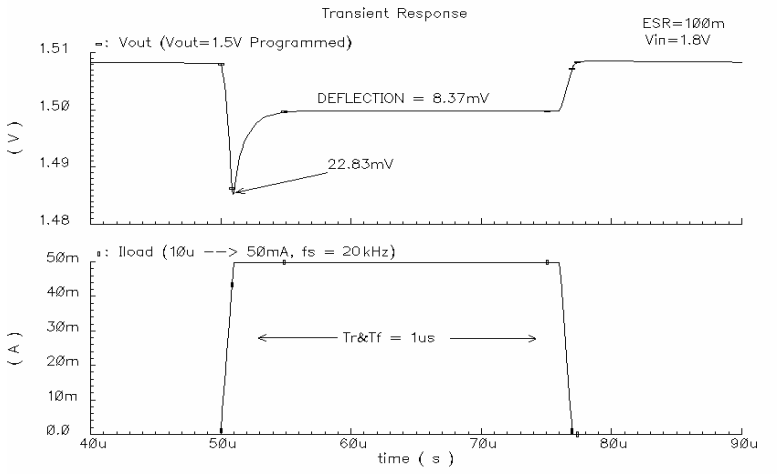
Fig. 71 Transient response for implementation I with ESR=0Ω for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} & V_{IN}=1.8V, V_{OUT}=1.5V.

The results obtained for the post-layout simulations in Fig. 71, match the results obtained from the schematic simulations closely (with a maximum of 3.6% deviation). These results show that the extracted version, including parasitic capacitances, presents variations within acceptable ranges.

C. Transient Response with ESR = 100mΩ

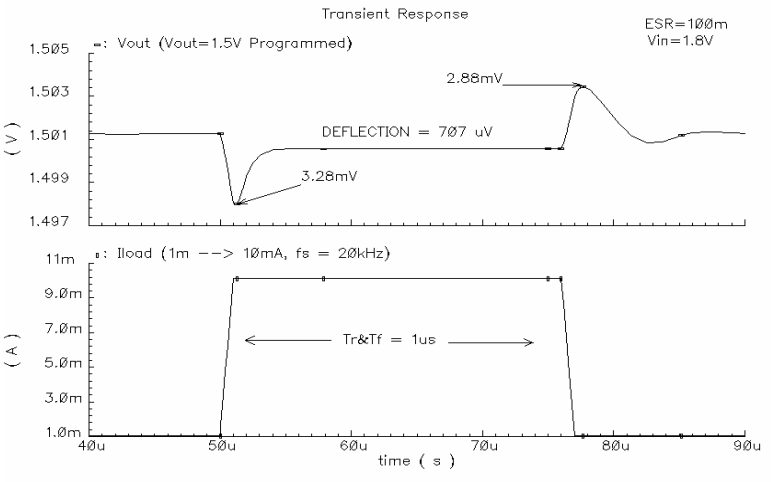
The same simulations carried out for various load conditions on the schematic are carried out on the post-layout version of implementation I. The load conditions are kept the same (C_L = 1µF and R_{ESR} = 100mΩ) in order to allow direct comparison between schematic and post-layout results. The full load transient response is also measured on the post-layout version of the circuit in the same manner it is measured in the schematic version.

Fig. 72 shows an example of the load transient performance for the case when V_{OUT} is set at 1.5V. It can be seen from these results that indeed the schematic and post-layout simulation predict similar performance.



(a)

Fig. 72 Transient response for implementation I with ESR=100mΩ for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} & V_{IN}=1.8V, V_{OUT}=1.5V.



(b)

Fig. 72 Continued.

Table XXXI shows a summary of the full load settling time for both the schematic and post-layout version of implementation I. It also demonstrates that the percent variation in this parameter between schematic and post-layout results is at a maximum of 2.5%. Therefore, it can be concluded that the post-layout view of the circuit is a valid representation of the schematic.

TABLE XXXI

POST-LAYOUT FULL LOAD TRANSIENT SETTLING TIME FOR IMP. I

V_{OUT}	Ts	Schematic	Post-Layout	% Variation
0.9V	**1%**	< 1 µs	< 1 µs	0%
	0.1%	2.24 µs	2.23 µs	0.45%
1.5V	**1%**	< 1 µs	< 1 µs	0%
	0.1%	2.498 µs	2.48 µs	0.77%
1.8V	**1%**	< 1 µs	< 1 µs	0%
	0.1%	2.77 µs	2.7 µs	2.5%

D. Post-Layout Noise Analysis Results

The same simulations for noise that are carried out for the schematic view were carried out on the analog extracted view of implementation I. The results are presented in the same order as well for ease of comparison. Fig. 73 and Table XXXII show the noise results when

programming the LDO to an output of 1.5V with an input of 1.8V. The equivalent output noise density can be seen at a level of 336.8µV/sqrt[Hz]. The integrated noise results for different loads can be seen in Table XXXII for this case. Compared to implementation II, this option presents higher equivalent output noise, as was explained in the previous chapter.

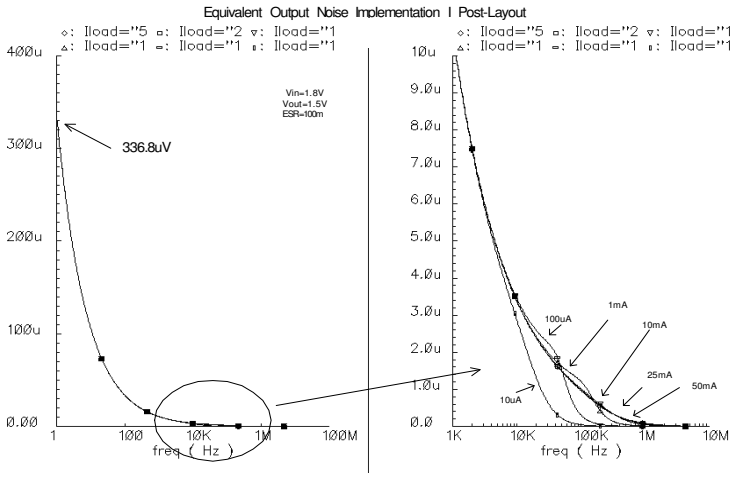


Fig. 73 Equivalent output noise for implementation I V_{IN}=1.8V, V_{OUT}=1.5V.

TABLE XXXII

IMP. I INTEGRATED NOISE V_{OUT}=1.5V

I_{LOAD}	O/P Int N. W/ Comp I
10µA	1.04 mV
100µA	1.14 mV
1mA	1.16 mV
10mA	1.14 mV
25mA	1.14 mV
50mA	1.14 mV

The results obtained for the post-layout noise simulations in Fig. 73, are very similar to those obtained for the schematic. This adds further proof that the layout is a valid interpretation of the schematic circuit.

E. Post-Layout Load Regulation

The post–layout results are very similar to the schematic simulations for load regulation. Fig. 74 shows the results of the different programmed levels when varying the current from 0-50mA.

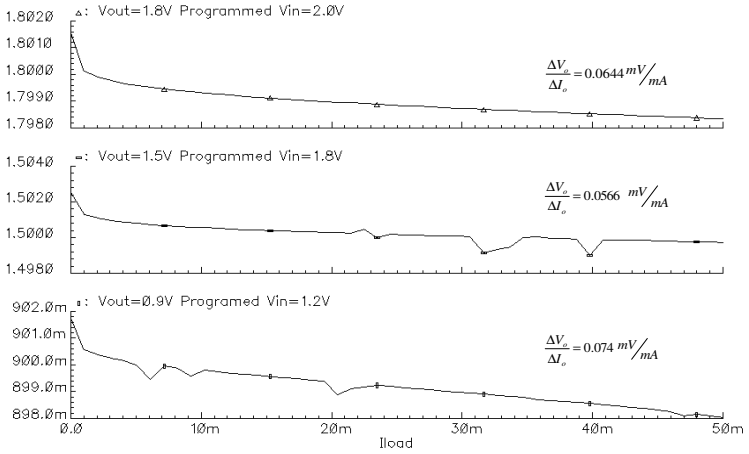


Fig. 74 Load regulation for implementation I.

A comparison between the schematic results and the post-layout simulated results is shown in Table XXXIII.

TABLE XXXIII

IMP. I LOAD REGULATION (SCHEMATIC VS. POST-LAYOUT)

V_{OUT}	Schematic	Post-Layout	% Variation
0.9V	0.074 mV/mA	0.074 mV/mA	0%
1.5V	0.055 mV/mA	0.0566 mV/mA	2.90%
1.8V	0.0606 mV/mA	0.0644 mV/mA	6.30%

It can be concluded from the previous table that the schematic and post-layout results agree with a maximum of 6.30% variation. The maximum variation occurs when the circuit is programmed for 1.8V at the output. Nevertheless, this variation is acceptable because the actual voltage change is only 40μV.

F. Post-Layout Line Regulation

All three output levels were verified by varying the input voltage up to 3.3V max as was done earlier to obtain schematic simulation results. The load current is set to 1mA as well. Fig. 75 shows the resultant graphs for the line regulation simulations.

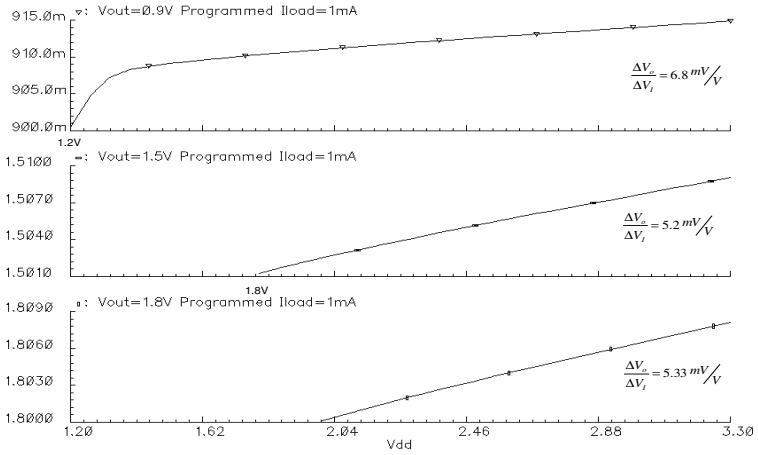


Fig. 75 Line regulation for implementation I.

These results closely follow the results obtained for the simulations run on the schematic. By direct comparison with the results in chapter IV and observing Table XXXIV, it can be concluded that the extracted circuit and the schematic predict very similar results.

TABLE XXXIV

IMP. I LINE REGULATION (SCHEMATIC VS. POST-LAYOUT)

V_{OUT}	Schematic	Post-Layout	% Variation
0.9V	6.79 mV/V	6.8 mVV	0.15%
1.5V	5.2 mV/V	5.2 mV/V	0%
1.8V	6.18 mV/V	5.33 mV/V	13.7%

Even though the maximum variation was found to be 13.7%, this only represents an actual variation of 0.85mV, which in practical terms, is acceptable.

G. Post-Layout PSRR

PSRR is measured for the extracted view of the LDO compensated with implementation I. For this simulation the output voltage was programmed to V_{OUT} = 1.5V with an input voltage set at 1.8V and the current is swept along various load levels as was done for the schematic version. The results of this simulation are shown in Fig 76.

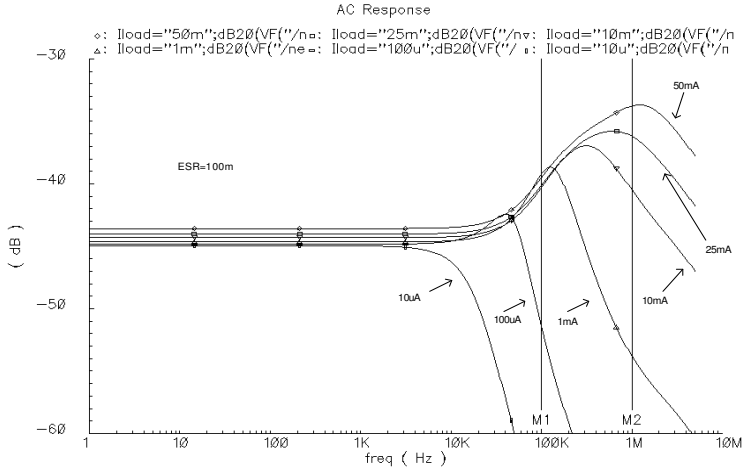


Fig. 76 Post-layout PSRR for implementation I.

It can be seen in Fig. 76 that these results agree well with the results presented in the previous chapter. The critical band of 100k to 1MHz presents a PSRR value of less than -35dB for all load cases as was the case for the schematic results. Table XXXV summarizes the PSRR performance for compensation implementation I. These results are very similar to the circuit schematic simulations.

TABLE XXXV

POST-LAYOUT PSRR SUMMARY FOR IMP. I

I_{LOAD}	PSRR @10Hz	PSRR @100kHz
10µA	-43.55 dB	-68.36dB
100µA	-43.99 dB	-51.33 dB
1mA	-44.31 dB	-39.24 dB
10mA	-44.66 dB	-40.33dB
25mA	-44.84 dB	-40.13 dB
50mA	-44.96 dB	-39.52 dB

H. Post-Layout Start-Up Time

The setup for this simulation was the same as for the schematic version. Shown in Fig. 77 is the resulting startup time for implementation I and an output programmed level of 1.5V. The other two available output levels (0.9V and 1.8V) have similar graphs and their results are summarized in Table XXXVI.

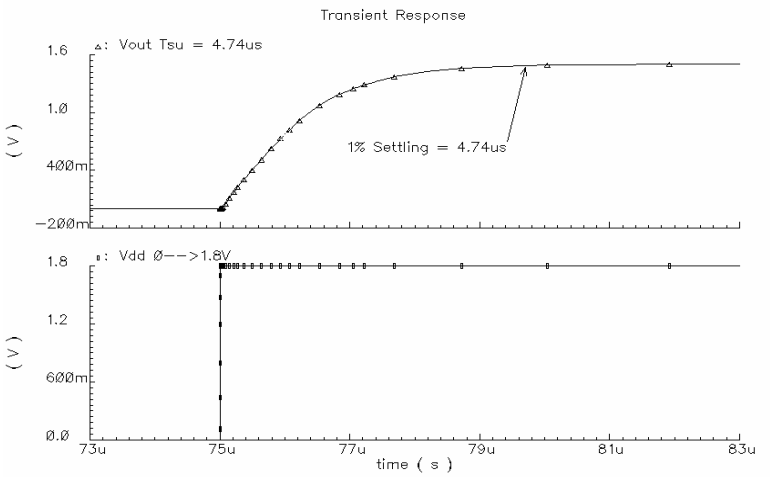


Fig. 77 Startup time for implementation I w/V_{OUT}=1.5V.

Table XXXVI also shows the comparison between schematic and post-layout results. By reviewing this comparison, it is clear that both the post-layout and schematic simulations predict very similar results with a maximum of 7% variation.

TABLE XXXVI

POST-LAYOUT STARTUP TIME SUMMARY FOR IMP. I

V_{OUT}	Schematic	Post-Layout	% Variation
0.9V	8.62 µs	8.02 µs	7%
1.5V	4.94 µs	4.74 µs	4%
1.8V	5.649 µs	5.46 µs	3.30%

As has been proven by the post-layout results obtained for implementation I, the schematic is a valid predictor of system performance. Both post-layout and schematic results agree well with each other in each of the tested performance metrics. These results lead to the conclusion that once the parasitic capacitances are included in the layout of the circuit, the results will not be degraded but will indeed agree with the schematic predictions.

2. Phase Compensation Implementation II

A. Layout for Implementation II

The layout for implementation II is shown in Fig 78; it occupies an area of 0.213 μm^2. All of the elements that make up implementation II are clearly marked as well. Once the layout was analog extracted the corresponding simulations were run on that view to verify that the simulation results of the post-layout view agree with the results predicted by the schematic simulations.

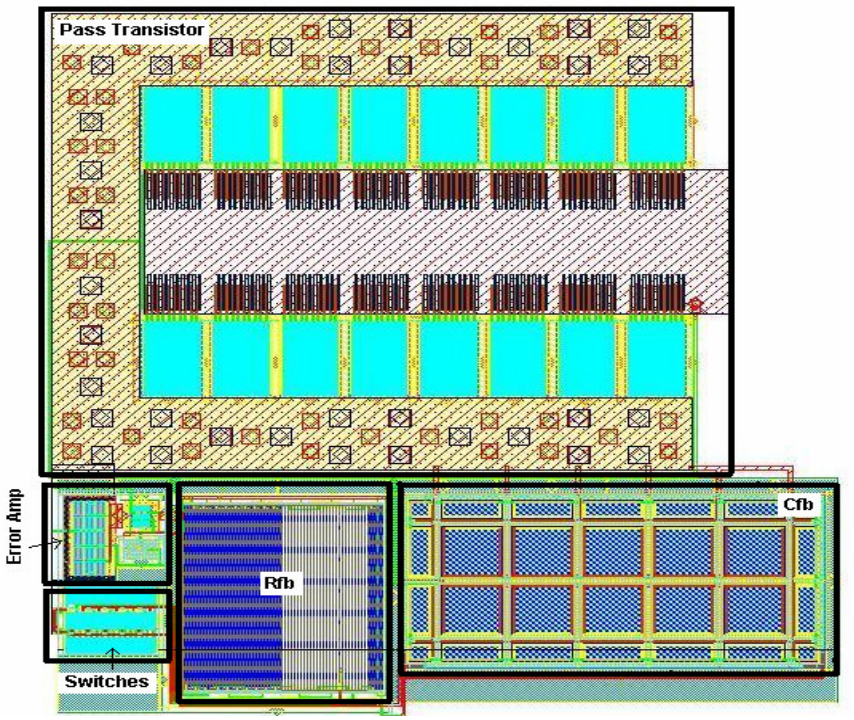


Fig. 78 Implementation II layout.

B. Post-Layout Transient Results

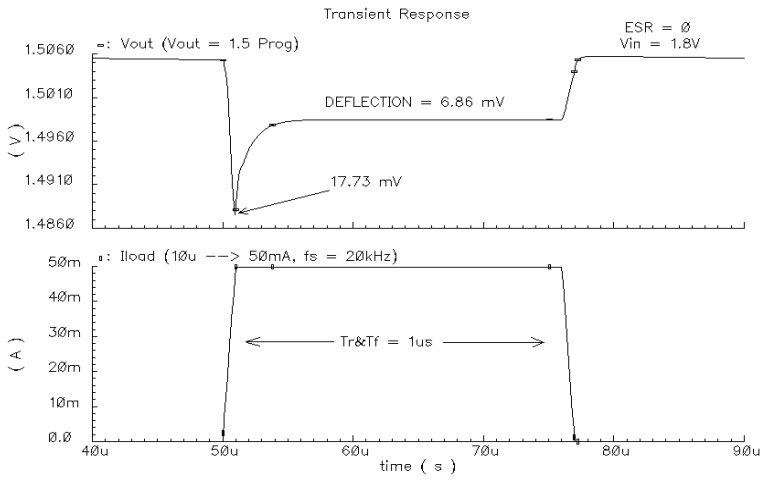
Post-layout simulations were also carried out on the extracted version of implementation II. The simulation setup was kept identical for validity of comparisons. Table XXXVII shows the load transient metrics summary for implementation II when the ESR value is set to 0. It also shows the percent deviation, in parenthesis, from the results obtained for schematic simulations.

TABLE XXXVII

POST-LAYOUT TRANSIENT CH. FOR VARIOUS O/P LEVELS FOR IMP. II

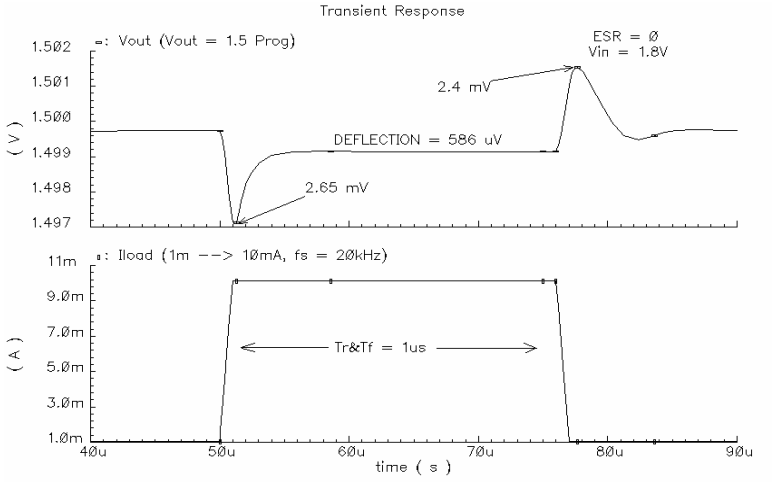
I_{LOAD}	Deflection	Max Peak
V_{OUT} = 0.9 V Prog.		
10µA-50mA	5.15mV (0%)	12.91mV (1.47%)
1mA-10mA	0.555mV (1.9%)	1.9mV (1.57%)
V_{OUT} = 1.5V Prog.		
10µA-50mA	6.86mV (0.29%)	17.73mV (0.45%)
1mA-10mA	0.586mV (12%)	2.65mV (1.8%)
V_{OUT} = 1.8 V Prog.		
10µA-50mA	7.58mV (0.39%)	18.33mV (0.7%)
1mA-10mA	0.685mV (0.58%)	2.82mV (1.6%)

It can be concluded, from the results given in Table XXXVII that the post-layout and schematic results are within acceptable ranges of deviation, therefore, the behavior of the post-layout simulations closely resembles the schematic results. The maximum percentage is actually 1.9%. All the entries in Table XXXVII are taken from simulation results like those shown in Fig. 79.



(a)

Fig. 79 Transient response for implementation II w/ESR=0Ω for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} & V_{IN}=1.8V, V_{OUT}=1.5V.

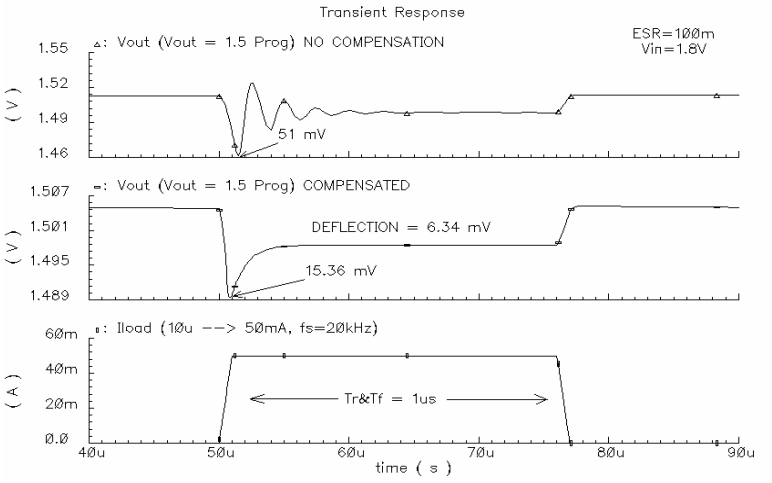


(b)

Fig. 79 Continued.

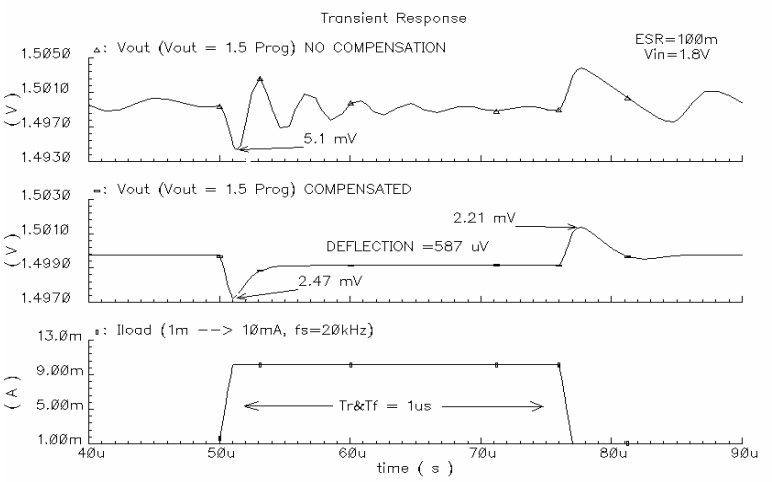
C. Transient Response with ESR = 100mΩ

Like in implementation I, an ESR value was set too 100mΩ to simulate a more practical load capacitor. Fig. 80 shows the transient results for a programmed output level of 1.5V and is used to further support the claim that both the schematic and post-layout offer very similar results.



(a)

Fig. 80 Transient response for implementation II & ESR compensation w/ESR=100mΩ for (a)10µ-50mA (b) 1mA-10mA I_{LOAD} & V_{IN}=1.8V, V_{OUT}=1.5V.



(b)

Fig. 80 Continued.

Different load transients and load levels were tested. In Table XXXVIII we can see the results of the full load transient settling time for each of the available levels. The measurements were carried out in the same manner as they were done for the schematic view of implementation II. It can be concluded that both schematic and post-layout results have a maximum of 6.47% variation; thus providing further proof that the post-layout view of the schematic is a valid representation.

TABLE XXXVIII

POST-LAYOUT FULL LOAD TRANSIENT SETTLING TIME FOR IMP. II

V_{OUT}	Ts	Schematic	Post-Layout	% Variation
0.9V	**1%**	< 1 µs	< 1 µs	N/A
	0.1%	1.39 µs	1.3 µs	6.47%
1.5V	**1%**	< 1 µs	< 1 µs	N/A
	0.1%	1.907µs	1.813 µs	4.9%
1.8V	**1%**	< 1 µs	< 1 µs	N/A
	0.1%	2.4 µs	2.312 µs	3.67%

D. Post-Layout Noise Analysis Results

The same simulations for noise that are carried out for the schematic view are carried out on the extracted view of implementation II. The results are presented in the same order for ease of comparison. The results are very similar to the data obtained from schematic simulation, as expected. Fig. 81 and Table XXXIX are the noise results when programming the LDO that is compensated with implementation II to an output of 1.5V with an input of 1.8V. The equivalent output noise is at a level of 311.33μV/sqrt[Hz] for the LDO that is compensated with implementation II.

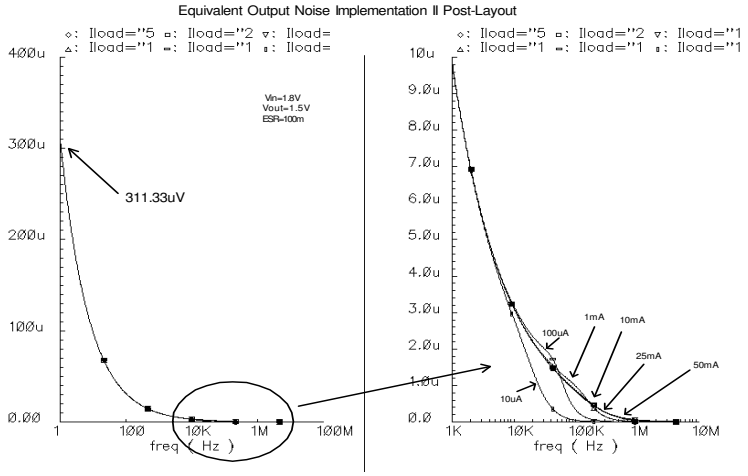


Fig. 81 Equivalent Output Noise for Implementation II & ESR Compensated V_{IN}=1.8V, V_{OUT}=1.5V.

Again, the results agree very well with those obtained from the schematic simulation. A direct comparison between results shows a very minute variation.

TABLE XXXIX

IMP. II INTEGRATED NOISE V_{OUT}=1.5V

I_{LOAD}	O/P Int N. W/ Comp II
10µA	0.971 mV
100µA	1.058 mV
1mA	1.06 mV
10mA	1.052 mV
25mA	1.051 mV
50mA	1.05 mV

E. Post-Layout Load Regulation

The post-layout load regulation results also present very similar performance to the schematic simulation predictions. Fig. 82 shows how the output programmed voltage changes with varying load current.

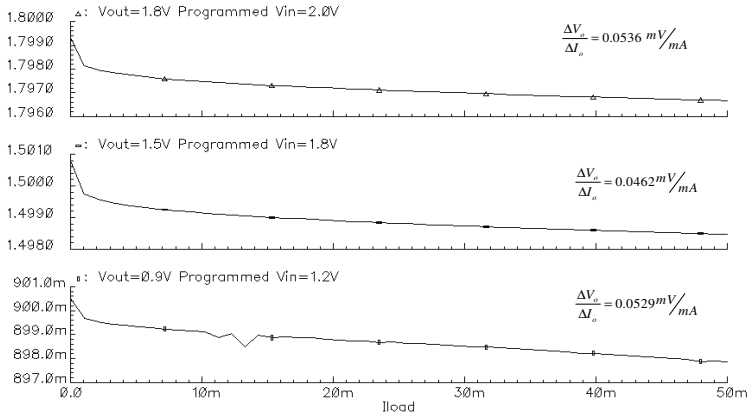


Fig. 82 Load regulation for implementation II.

The post layout results validate the schematic, because both set of results are very close. Table XL provides further proof of this conclusion. It shows that the maximum variation from schematic to pos-layout results is 0.43%. These variations further prove that the layout for implementation II is a valid representation of the performance of the overall system.

TABLE XL

IMP. II LOAD REGULATION (SCHEMATIC VS. POST-LAYOUT)

V_{OUT}	Schematic	Post-Layout	% Variation
0.9V	0.053 mV/mA	0.053 mV/mA	0%
1.5V	0.0464 mV/mA	0.0462 mV/mA	0.43%
1.8V	0.0536 mV/mA	0.0536 mV/mA	0%

F. Post-Layout Line Regulation

The line regulation is also investigated in order to quantify the variations between schematic and post-layout results for implementation II. As shown in Fig. 83 the results of line regulation for the post-layout view follow the trend obtained earlier for the schematic results.

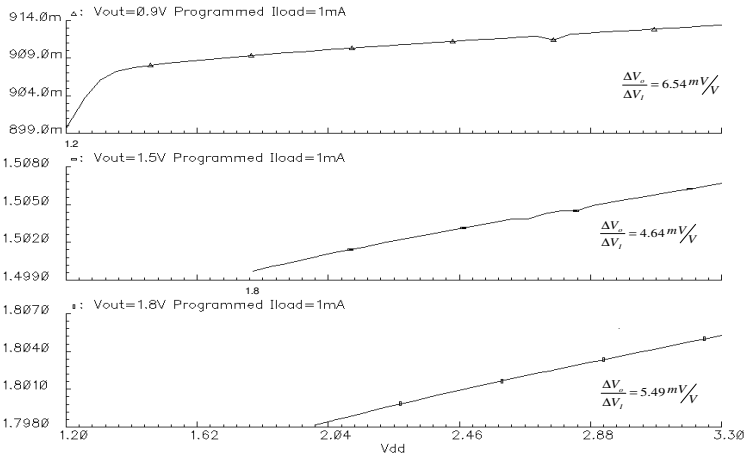


Fig. 83 Line regulation for implementation II w/V_{OUT}=1.5V.

In fact, the maximum variation between schematic and post-layout results is found to be 0.4% as shown in Table XLI. These results show that the expected performance will suffer very little degradation in post-layout results.

TABLE XLI

IMP. II LINE REGULATION (SCHEMATIC VS. POST-LAYOUT)

V_{OUT}	Schematic	Post-Layout	% Variation
0.9V	6.54 mV/V	6.54 mV/V	0%
1.5V	4.66 mV/V	4.64 mV/V	0.4%
1.8V	5.5 mV/V	5.49 mV/V	0.1%

G. Post-Layout PSRR.

PSRR is now measured on the post-layout view of implementation II. It also shows very little variation when compared to the schematic results. It can be noticed in Fig. 84 that this system exhibits the same trend in PSRR as does the schematic simulation results.

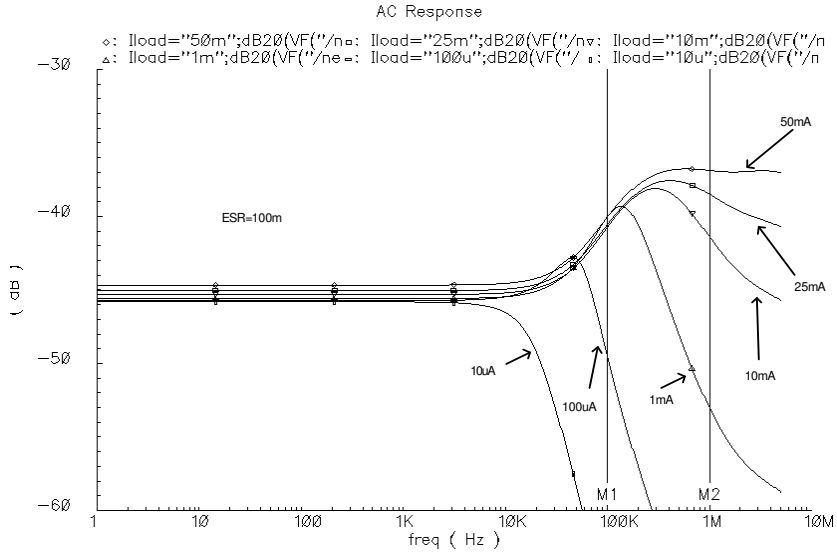


Fig. 84 PSRR for implementation II.

The results for post-layout simulations of PSRR are also summarized in Table XLII for direct comparison with the schematic results. It can be seen from both the PSRR table and the PSRR graph that indeed the schematic and post-layout results agree very well.

TABLE XLII

POST-LAYOUT PSRR SUMMARY FOR IMP. II

I_{LOAD}	PSRR @10Hz	PSRR @100kHz
10µA	-45.81 dB	-66.38 dB
100µA	-45.72 dB	-49.45 dB
1mA	-45.58 dB	-40.03 dB
10mA	-45.31 dB	-40.75 dB
25mA	-45.05 dB	-40.57 dB
50mA	-44.67 dB	-40.04 dB

H. Post-Layout Start-Up Time

The simulation was carried out with the same setup as for the schematic view. Fig. 85 shows the resulting startup time for implementation II when V_{OUT} is programmed to a level of 1.5V. All three levels were investigated and their behavior is summarized in Table XLIII.

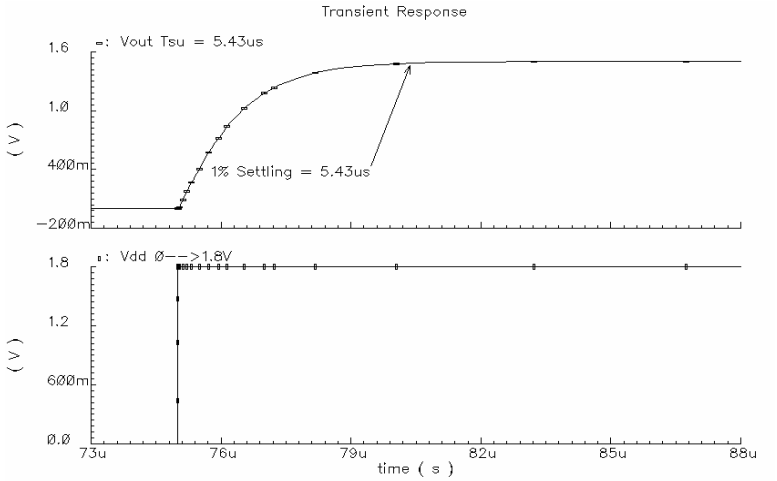


Fig. 85 Startup time for implementation II w/V_{OUT}=1.5V.

As shown in the table below, the maximum variation in startup time is found to be 6.7%. This is an acceptable result as still the pot-layout results show a sufficiently fast startup time.

TABLE XLIII

POST-LAYOUT STARTUP TIME SUMMARY FOR IMP. II

VOUT	Schematic	Post-Layout	% Variation
0.9V	9 µs	7.73 µs	6.7%
1.5V	5.19 µs	5.43 µs	4.6%
1.8V	6.04 µs	6.31 µs	4.5%

In conclusion, all the post-layout simulations agree well with the schematic results. This implies that the layout is a valid representation of the schematic circuit representations for both of the LDO implemented.

CHAPTER VI

RESULTS COMPARISON

In this chapter the post-layout results for both proposed implementations are compared in order to further characterize the performance vs. a typical ESR compensated LDO.

A. Final Chip Layout

The overall chip is laid out using the Virtuoso tool in the CADENCE software package. There are four LDO topologies placed in a DIP40 package and the overall layout is shown in Fig.86. The two implementations, the ESR compensated and a fourth LDO [10] are included in the IC for comparison in experimental results. The overall chip area is 3.46mm^2.

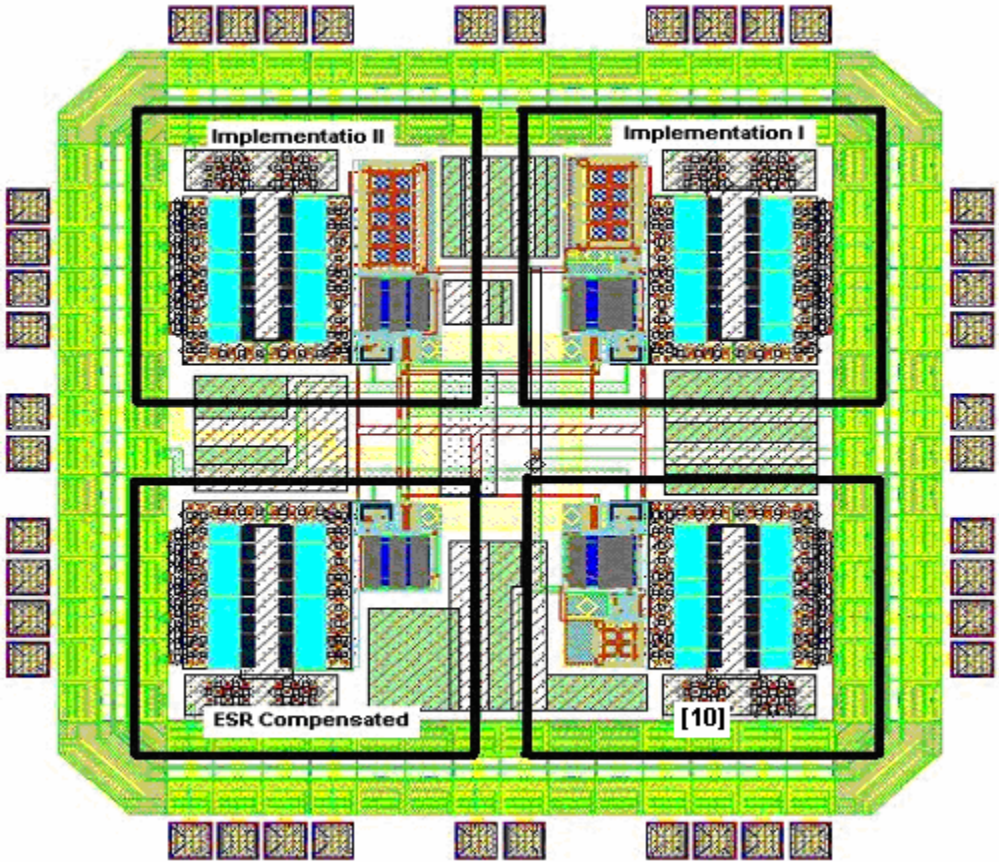


Fig. 86 Overall chip layout 3.46mm^2.

As can be seen from Fig. 86, the orientation of each LDO is kept identical, including the size and positioning of the metal routing. Also, the capacitors used for feedback are placed in a V_{DD} connected N-Well for additional noise shielding. The on chip resistors are laid out using common centroid techniques as are all of the transistors to reduce matching errors.

Four pads are used for the V_{IN} and V_{OUT} of each LDO because they will carry large currents: up to 50mA at high loads transients. For these high current lines, metal resistance is very critical; therefore, special attention was placed during layout. These connections were placed as close as possible to the pad contacts and a metal sandwich was used. The metal sandwich is made up of all four available metals stacked on top of each other. They are all contacted together making the metal resistance effectively resistors in parallel, thus reducing the Resistance.

B. Transient Comparison

Transient results are summarized in Table XLIV. These results are the compiled data from the post-layout simulations carried out on both of the proposed LDO implementations. The main characteristics that were looked at, deflection voltage, maximum peaking and full load settling time are included for the various load cases. For each programmable output voltage, two different transient load levels were simulated in order to characterize the performance of each implementation. These results are useful for comparison and evaluation of each topology vs. the others.

TABLE XLIV

TRANSIENT RESULTS COMPARISON

V_{OUT}	I_{LOAD}	Deflection	Max Peak	0.1% Settling
Compensation Implementation I				
0.9V	10µA-50mA	7.70 mV	20.11mV	2.23 µs
	1mA-10mA	0.782 mV	2.9 mV	
1.5V	10µA-50mA	9.13 mV	26.1 mV	2.48 µs
	1mA-10mA	0.709 mV	3.64 mV	
1.8V	10µA-50mA	10.1 mV	27 mV	2.7 µs
	1mA-10mA	0.826 mV	3.90 mV	
Compensation Implementation II				
0.9V	10µA-50mA	5.15 mV	12.91mV	1.3 µs
	1mA-10mA	0.555 mV	1.9 mV	
1.5V	10µA-50mA	6.86 mV	17.7 mV	1.813 µs
	1mA-10mA	0.586 mV	2.65 mV	
1.8V	10µA-50mA	7.58 mV	18.3 mV	2.312 µs
	1mA-10mA	0.685 mV	2.82 mV	
ESR Compensation				
0.9V	10µA-50mA	9.98 mV	35.6 mV	N/A
	1mA-10mA	0.899 mV	3.8 mV	
1.5V	10µA-50mA	14.1 mV	51.0 mV	N/A
	1mA-10mA	N/A	5.10 mV	
1.8V	10µA-50mA	16.9 mV	58.1 mV	N/A
	1mA-10mA	N/A	6.82 mV	

C. Noise Performance Comparison

Noise performance is also compared between implementations I and II and the ESR compensated LDO. The flicker noise coefficients are included in these results as they are obtained from post-layout simulations. Fig. 87 shows the equivalent output noise level of each LDO. Comparatively implementation II has the best noise performance. It has the same performance as that of an ESR compensated LDO. This is due to the fact that implementation II does increase the number of devices present in the typical LDO design, thus the noise remains the same. Implementation II offers a clear advantage when noise is an important consideration.

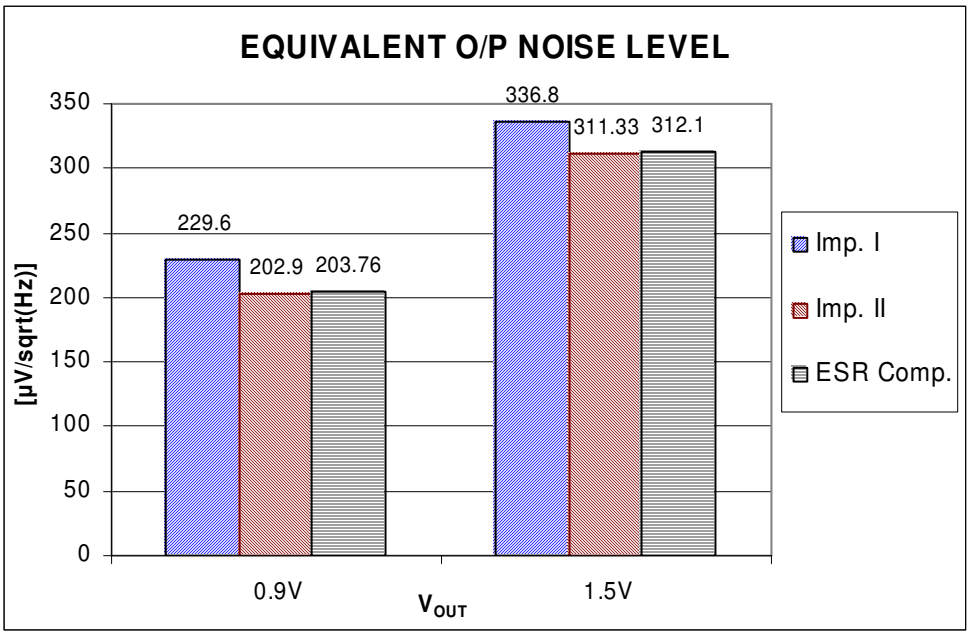


Fig. 87 Equivalent O/P noise level comparison.

The integrated noise was also investigated previously for each design; the results are summarized in Fig. 88.

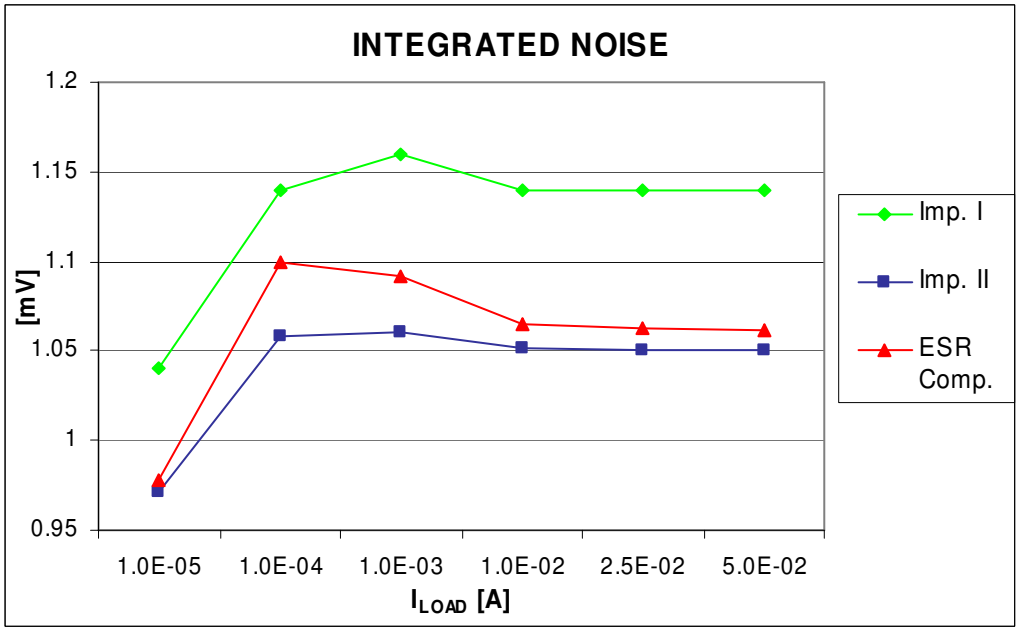


Fig. 88 Integrated noise comparison.

An interesting point to notice is that noise is higher at lower loads. As was discussed in previous chapters, the noise of the circuit shows a load current dependence. This can be attributed to the fact that the DC gain of the system increases at lower current loads due to an increase in output impedance. The decrease in gain translates into less amplification of the main noise contributors in the system, particularly the p-MOS differential pair in the error amplifier.

D. Load Regulation Comparison

After having obtained quantified values for the post-layout load regulation parameter, they are plotted in the same figure to verify that implementation II presents superior load regulation results. This comparison is done in Fig. 89.

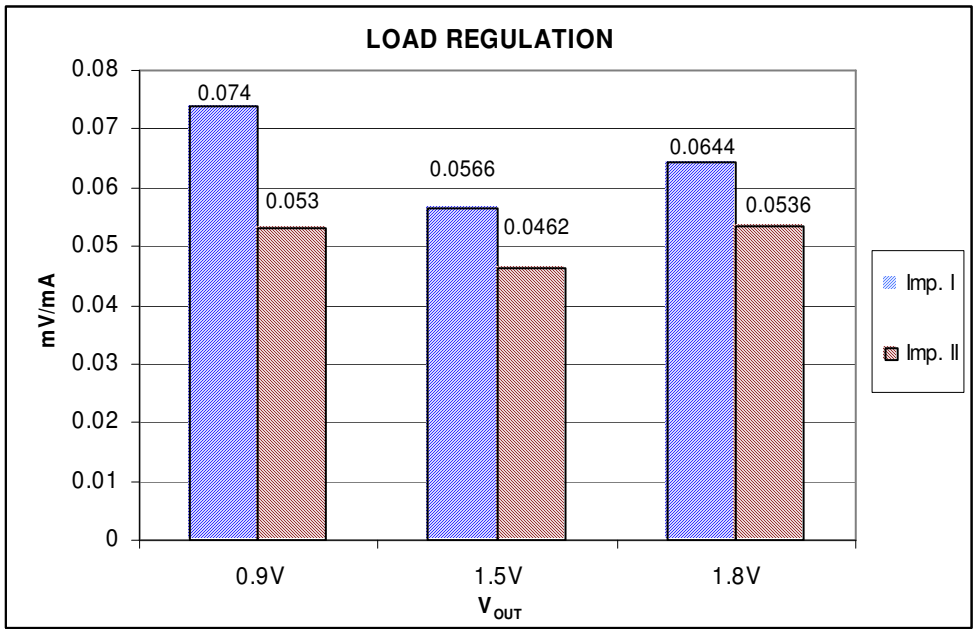


Fig. 89 Load regulation comparison

As can be seen, implementation II offers better load regulation than implementation I. This, as was discussed earlier is due to the fact that the compensation network of implementation II does

not depend on any matching between DC operating points as it will not disturb the biasing conditions at the nodes it is applied, unlike implementation I.

E. Line Regulation Comparison

Line regulation performance is also compared in the two proposed implementations. It can be seen from Fig. 90 that implementation II performs marginally better than implementation I.

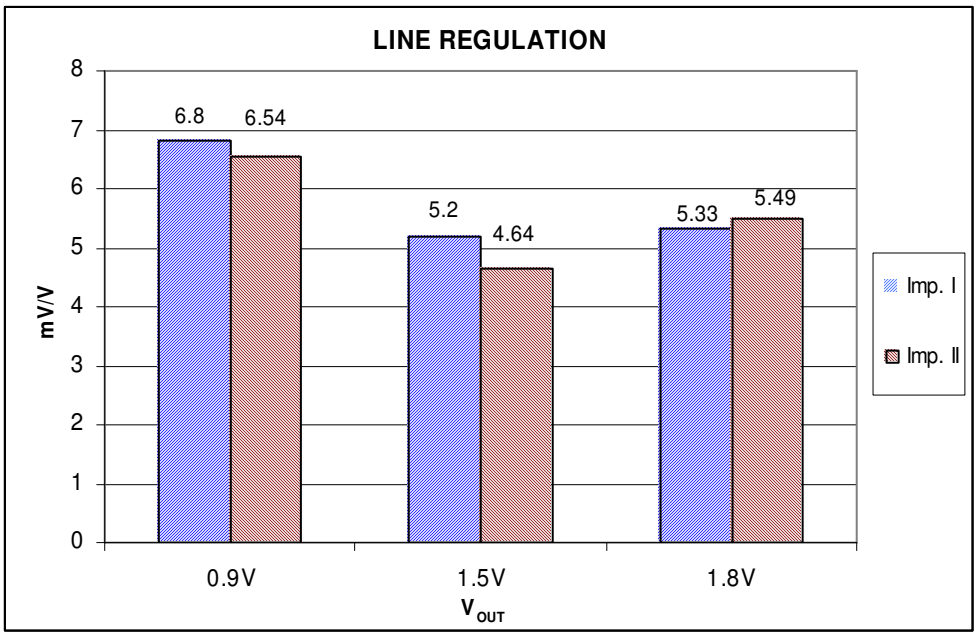


Fig. 90 Line regulation comparison.

Any differences in these implementations can once again be attributed to the open-loop DC gain of the system. For implementation I the DC gain is a lower than implementation II, this was shown in chapter IV in the *AC Performance* section. Therefore these results agree with the open loop DC gain of the system.

F. PSRR Comparison

The PSSR comparison is carried out in both Fig. 91 and Fig. 92. As can be seen from these results the PSRR performance is very much the same for all three reported cases.

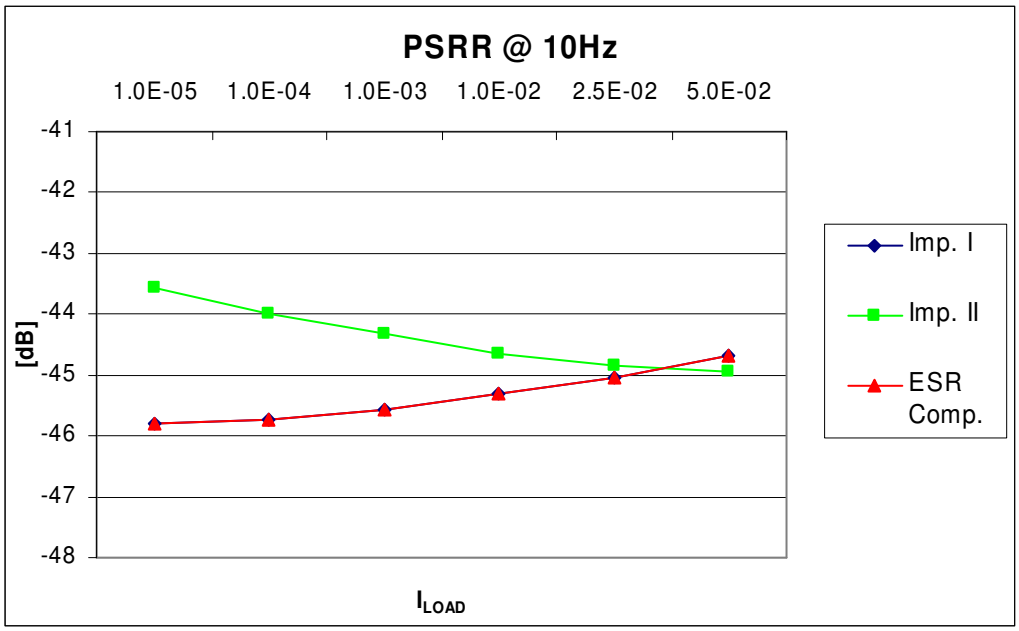


Fig. 91 PSRR @ 10Hz comparison.

The small differences apparent between implementation I and II are attributed to the fact that the implementation I uses V_{IN} (V_{DD}) powered transistors to create the feedback network. These will inject power supply noise into the feedback path and it will get amplified along the loop path, thus causing a minor deterioration of PSRR performance as is more apparent in Fig. 91.

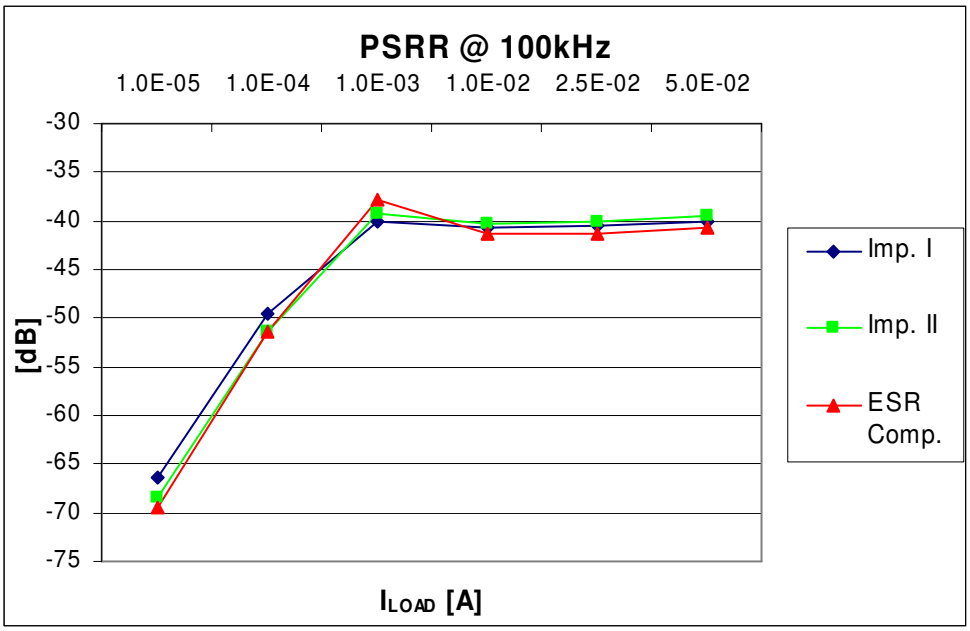


Fig. 92 PSRR @ 100kHz comparison

G. Startup Time Comparison

Startup is also an important factor in the transient response of the system. Therefore a comparative table is generated and the results indicate that implementation I and implementation II are superior in performance when compared to an LDO compensated by the ESR of the output capacitor. The startup time of each LDO is presented in graphical form in Fig. 93. The results shown in Fig. 93 further support the claim that both implementation I and II show an improved performance over the other compensations.

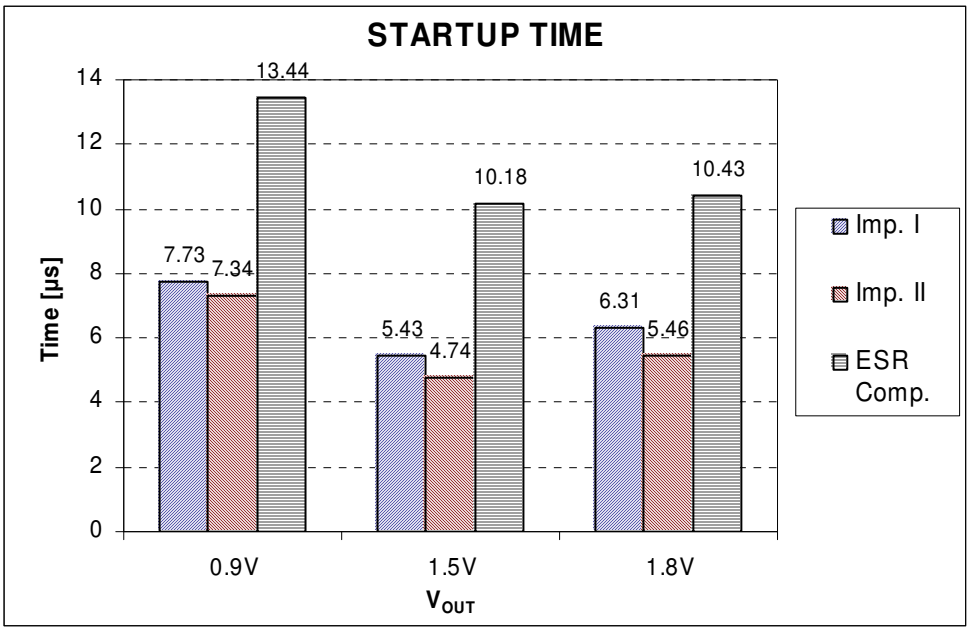


Fig. 93 Startup time comparison.

Once again, the use of a feedback path that can detect changes in the output proved beneficial as the proposed implementations prove to react with less startup time than the ESR compensated LDO.

H. Power Consumption/Ground Current Comparison

The power consumption in the form of quiescent current is summarized for all designs in Fig. 94. It is shown that Implementation II does not add any extra DC current expenditure. This is an attractive feature of implementation II for low power applications, as greater stability, programmability and faster response will be obtained without an increase in quiescent current when compared to the ESR compensated LDO.

Implementation I, on the other hand, presents an increase in quiescent current that is still within the allowable power requirements. This is due to the nature of the implemented compensation network requiring extra DC current for biasing of the additional transistors.

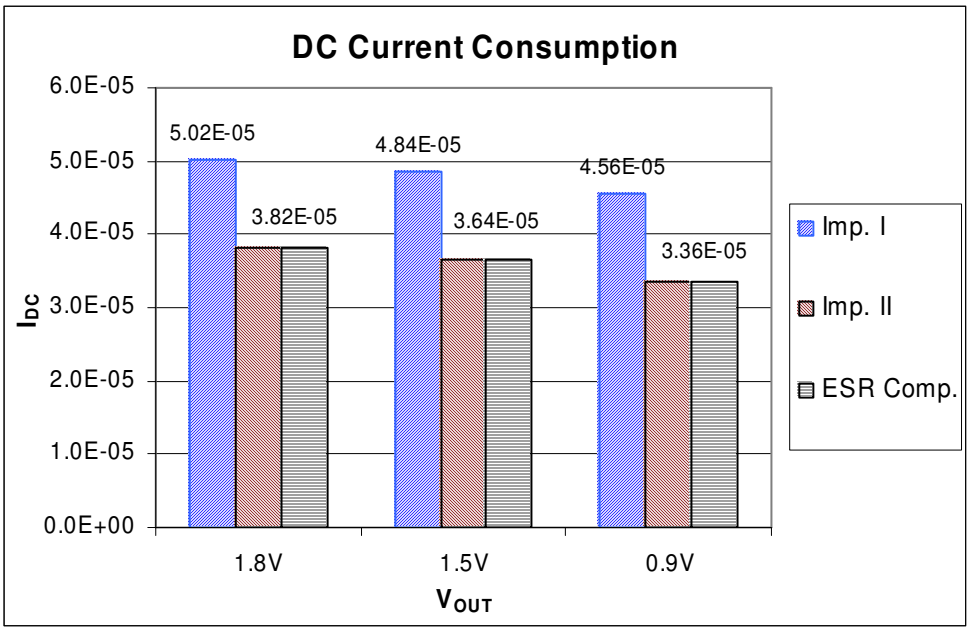


Fig. 94 DC current consumption comparison.

In conclusion, it was found that implementation II is the most beneficial of the proposed architectures that were included in the submitted chip. It is clear that better performance can be expected at low voltage operation with low power consumption if implementation II is chosen.

CHAPTER VII

EXPERIMENTAL RESULTS

In this chapter the measured results of the fabricated version of the LDO's are presented. The chip was fabricated and packaged by the MOSIS educational service in a dip-40 package. A chip micrograph shows the location of each of the LDO's included in the design. It can be seen in Fig. 95, that each LDO holds the same orientation with respect to the pins. Also, both implementation I and II are included in the same die along with two other benchmark circuits in order to make any comparison more valid.

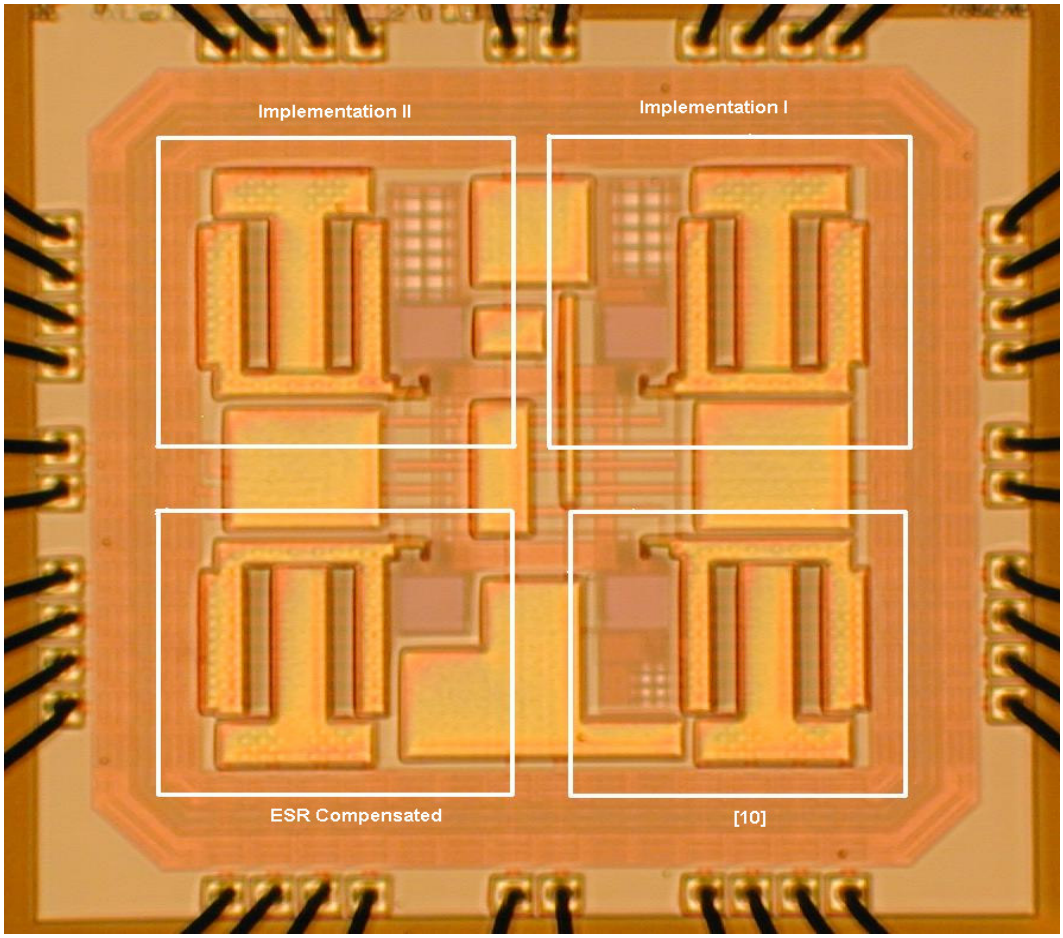


Fig. 95 Chip micrograph.

A printed circuit board (pcb) was fabricated in order to facilitate measurement of all the LDO's characteristics. Fig. 96 shows the measurement setup. All the necessary equipment (dc power supplies, pulse generator, digital multimeters, and oscilloscopes) were provided by the AMSC at Texas A&M University (Analog and Mixed Signal Center).

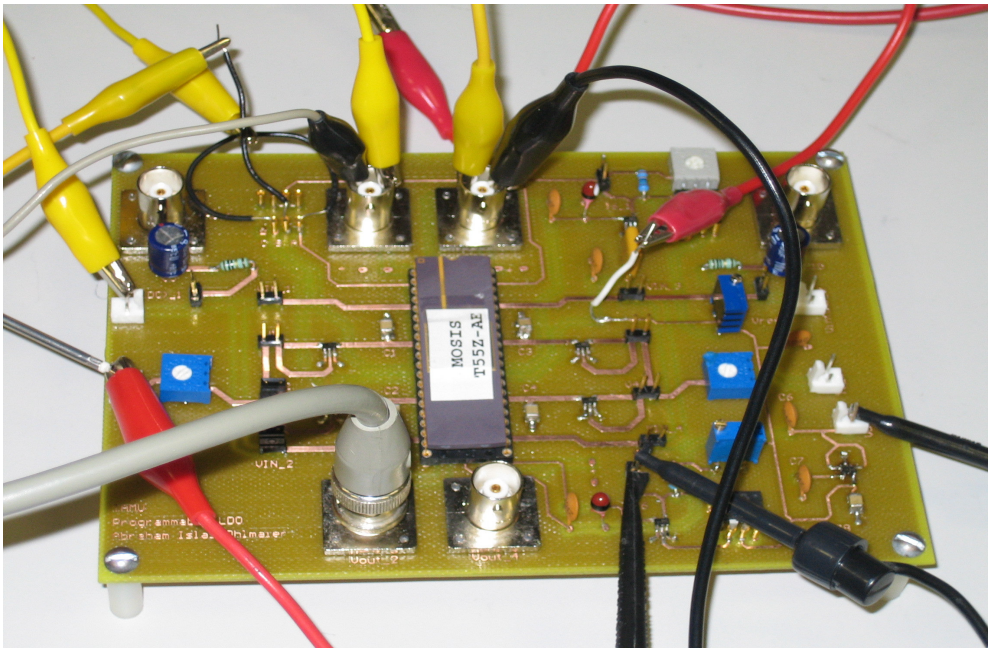


Fig. 96 PCB test setup.

The load is a 1μF multilayer ceramic surface mount capacitor. This capacitor has a low ESR of less than 0.100Ω.

The most telling test for stability of an LDO is the response to a load transient; therefore to verify basic functionality a transient load was applied at the output to simulate the effect of forcing the LDO source current. This signal was applied to the LDO compensated with the ESR of the load capacitor and to both proposed implementations. The load capacitor and PCB layout was kept exactly the same to further validate comparisons.

Fig 97 shows the result obtained for the LDO that is compensated with the ESR of the load capacitor. As can be seen in this figure, the LDO does not find a steady state value for high current loads. This characteristic matches the simulated results and it can be concluded that the LDO that depends only on the ESR of the output capacitor does not show sufficient phase margin. This test was run with a current load step of approximately 10µA to 50mA with a period of 66.67µs and a rise and fall time of 1µs. The output voltage was programmed to 1.5V with an input voltage of 1.8V. Both these conditions are kept the same for all three sets of results presented.

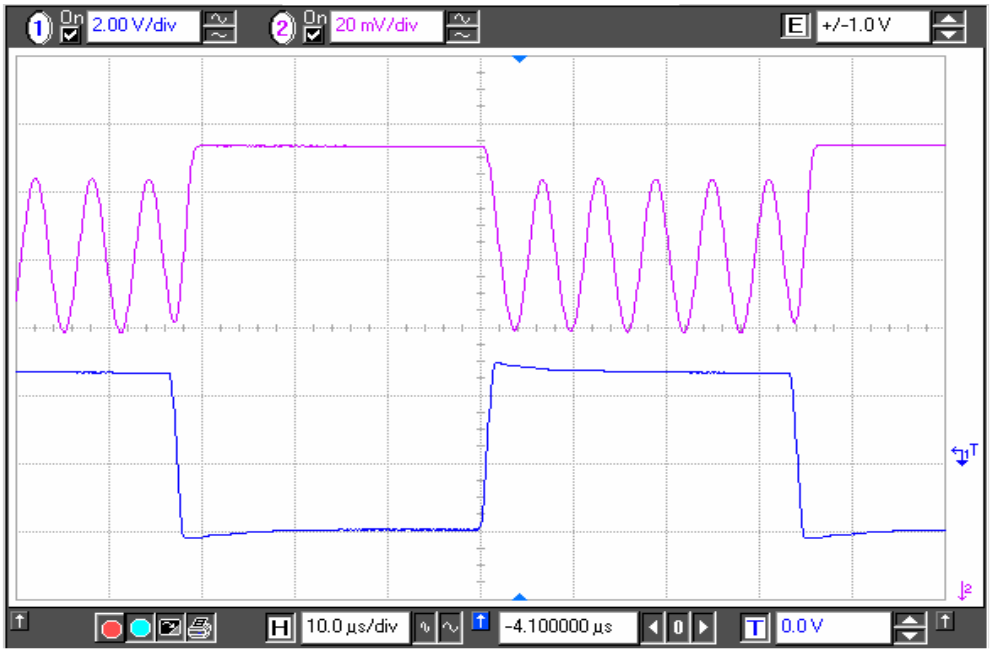


Fig. 97 ESR compensated LDO transient response.

It is obvious to see that the ESR of this load capacitor is not enough to give the LDO sufficient phase margin as the output (pink curve) does not find a steady state value with high current loads.

When the same output current step is placed at the output of implementation I, it is clear to see that indeed the LDO will find a steady state value for both transitions in the load. That is, at maximum current and at minimum load current. From Fig. 98 it can be concluded that the compensation technique used in implementation I gives the LDO sufficient phase margin as is evident from the steady state values achieved at high current loads.

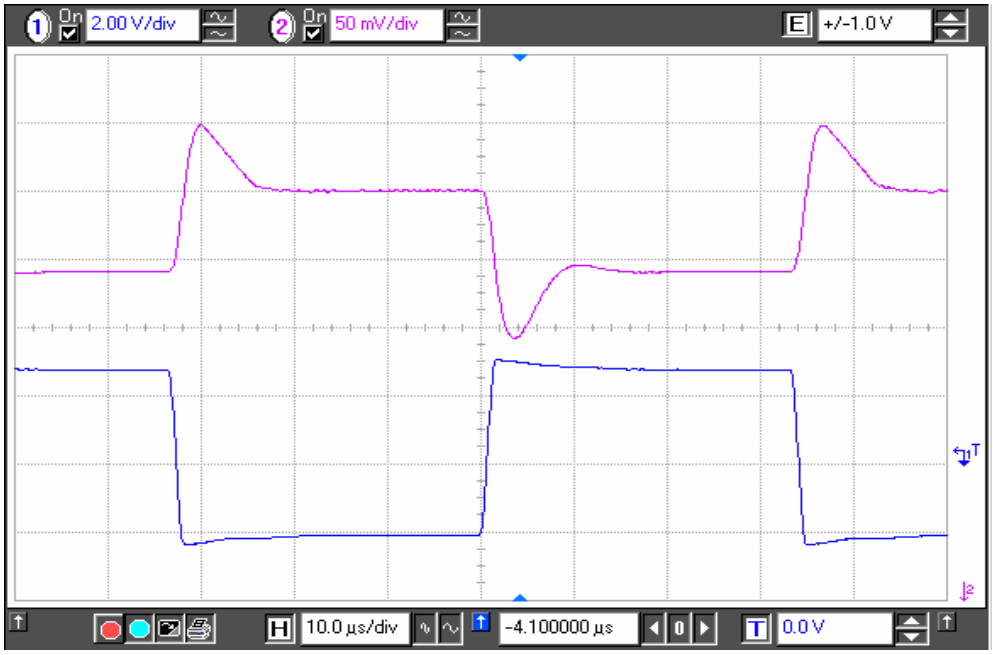


Fig. 98 Implementation I transient response.

Implementation II also gives the LDO sufficient phase margin as can be seen in Fig. 99. The difference between the two implementations is power consumption. The LDO compensated with implementation II will only consume as much as is required to properly bias the error amplifier due to the fact that the feedback is generated using only an on-board capacitor.

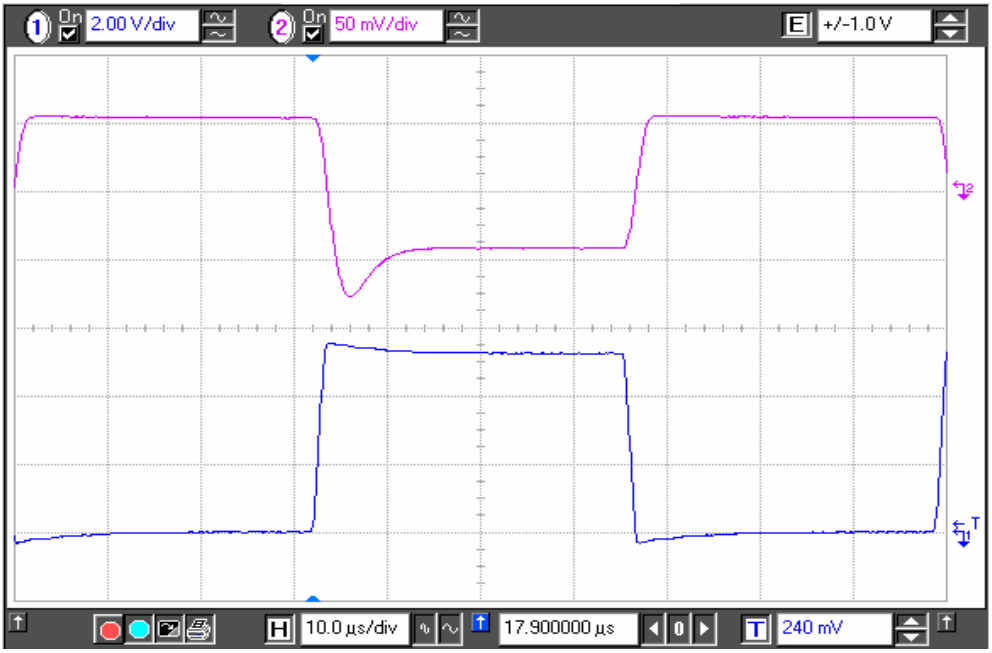


Fig. 99 Implementation II transient response.

Fig. 98 and Fig. 99 prove that both implementation I and II provide the LDO with sufficient phase margin for the systems to settle. The different specific characteristics of each regulator were still pending for characterization at the time of generation of this thesis. It can, however, be concluded that basic functionality of both techniques is achieved at the experimental level as is proven by the full load transient response of both LDO's.

CHAPTER VIII

CONCLUSIONS

The design, schematic, post layout simulations and some experimental results of two implementations of a fully stable programmable LDO for low voltage and low power operation have been presented. Both implementations have proven to provide better transient response than the typical ESR compensated LDO's as their overshoot is minimized and response times are superior. The phase compensation technique is novel and has not been reported in available literature. Also, both implementations of the proposed structure are capable of low voltage (V_{IN} = 1.2V) operation with a minimum regulated voltage at 0.9V. Two other regulated voltage levels (1.5V, 1.8V) are also available and fully stable. The power consumption (ground current) is not increased when using implementation II when compared to a typical LDO compensated with the output capacitor ESR. Implementation I presents a small increase in ground current, still staying within the required <60µA. The proposed implementations have been proven to operate in simulations and experimental tests with a low ESR small valued ceramic capacitor (1µF), ideal for real-estate and economic concerns.

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VITA

Abraham Islas Ohlmaier was born in Hermosillo, Sonora, Mexico. He received his B.S. in Electrical Engineering from Texas A&M University, College Station, TX, USA in August 2002. He received his M.S. in Electrical Engineering from Texas A&M University, College Station, TX, USA in December 2005.

He joined the Analog and Mixed Signal Center at Texas A&M University upon receiving his B.S. degree and carried out research in power management integrated circuits under the advisement of Dr. Jose Silva-Martinez. From May 2003 to August 2003 he was an IC Design Engineering Intern with California MicroDevices Inc. in Austin, TX. Also, from May 2004 to August 2004 he was an IC Design intern once again with California MicroDevices Inc. in Milpitas, CA. He currently is employed at Advanced Micro Devices (AMD) in Austin, TX. He can be contacted through the Electrical Engineering department at Texas A&M University; Department of Electrical Engineering, Texas A&M University, College Station, TX 77843.