CMOS TEMPERATURE SENSOR UTILIZING INTERFACE–TRAP CHARGE PUMPING

A Thesis

by

FEYZA BERBER

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

August 2005

Major Subject: Electrical Engineering

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ABSTRACT

CMOS Temperature Sensor Utilizing
Interface–Trap Charge Pumping. (August 2005)
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The objective of this thesis is to introduce an alternative temperature sensor in CMOS technology with small area, low power consumption, and high resolution that can be easily interfaced. A novel temperature sensor utilizing the interface–trap charge pumping phenomenon and the temperature sensitivity of generation current is proposed.

This thesis presents the design and characterization of the proposed temperature sensor fabricated in 0.18μm CMOS technology. The prototype sensor is characterized for the temperature range of 27^{o}C–120^{o}C. It has frequency output and exhibits linear transfer characteristics, high sensitivity, and high resolution. This temperature sensor is proposed for microprocessor thermal management applications.

To the memory of my father Servet Berber who always loved and encouraged me.

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I am indebted to my mother Hafize Berber for her unconditional support. Without her it would be impossible. She has always given strength to me. I would also like to thank my sister Seda Berber for her love and patience.

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INTRODUCTION

A. Temperature Sensor and Its Metrics

Built-in temperature sensors are becoming increasingly important in VLSI applications as the transistor dimensions are aggressively scaled down and more transistors are integrated on a single chip. The component density and the power dissipation of these high-performance VLSI chips necessitate alternatives to some traditional design and testing methodologies. Dynamic thermal testing and dynamic thermal management of IC's are two of these alternatives which require built-in thermal sensors [1]. Semiconductor sensors are also preferred over traditional temperature sensors in some automotive and biomedical applications due to their low–area and low–cost.

Semiconductor temperature sensors are generally based on the variation of pn–junction voltage with temperature. The temperature sensitivities of threshold voltage and direct tunnelling current are also exploited in some temperature sensor applications. The output signal of the sensor can be current, voltage, or frequency. Main performance metrics of semiconductor temperature sensors are technology compatibility, power consumption, area, operating range, linearity, accuracy, sensitivity, resolution and speed. The significance of any of these metrics depends on the application.

The main requirements for a temperature sensor to be integrated in a VLSI application for thermal management are CMOS compatibility, low silicon area, low power consumption, typical temperature range of $0 - -120^{o}$C, easy and inexpensive calibration, and preferably a digital output signal [2]. Some other applications require temperature sensors with high linearity, accuracy, sensitivity, and/or long-term

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stability.

Accuracy is the amount of uncertainty in a temperature reading, and it is usually expressed as the percentage of the input. Sensitivity gives the ratio of change in the sensor output to change in temperature. It is obtained from the slope of the calibration curve. Resolution describes the minimum amount of temperature change that can produce a detectable change at the sensor output, and it is limited by the noise level of the sensor.

The operating range of semiconductor sensors is limited to $20 - -120^{o}$C due to physical properties of silicon. A linear transfer characteristic is desired within the operating range for easy read–out. Due to the nature of sensing, transfer characteristics of semiconductor sensors are susceptible to process variations. Resulting gain, offset, and linearity errors that affect accuracy and sensitivity need to be corrected through calibration.

B. Temperature Sensor Applications

Traditional IC testing methods based on voltage and quiescent supply current (IDDQ) techniques are becoming inefficient as the threshold voltage is scaling down and leakage currents are increasing with the smaller transistor dimensions [3]. An alternative method that employs built-in temperature sensors is thermal testing [4], [5]. Thermal testing is used to detect and diagnose faults in integrated circuits based on the fact that some faults, when activated, cause an increase in power dissipation, and therefore, in temperature. Differential thermal sensors that have low sensitivity to ambient temperature changes but high sensitivity to thermal variations generated by the activated faults are employed for such applications [5].

Temperature sensors find their primary application in thermal management of

microprocessors [6], [7]. One of the limiting factors for high-performance processors with increasing transistor number and clock rate is the power dissipation. Even though the average power dissipation of a processor is typically much less than its maximum power dissipation, the thermal packaging and the cooling mechanisms are designed for the maximum dissipation, increasing the cost, area, and complexity of the design [7]. Dynamic thermal management is employed to ensure that power dissipation, and therefore, the operating temperature, does not reach the maximum limits so that the design specifications are relaxed and cost is reduced. The operating temperature is monitored by built-in thermal sensors in a thermal management system. The temperature readings are scanned by a control unit which triggers passive or active cooling actions when a threshold temperature is reached.

The Motorola PowerPC RISC microprocessor is a typical example of processor systems with a built-in temperature sensor for dynamic thermal management [8]. Thermal monitoring with a single sensor estimates the average chip temperature assuming constant temperature over the chip. As the complexity of processor functions and the integration density increase, single point temperature sensing becomes inadequate. An array of sensors is needed to monitor critical points over the chip and to ensure reliable operation of the high-performance processors. Multiple-sensor integration imposes a very important challenge to the thermal sensor design: minimum power consumption and minimum silicon area.

C. Conventional Silicon Temperature Sensors

Three devices used in CMOS technology for temperature sensing are lateral bipolar transistors, vertical bipolar transistors, and CMOS transistors operating in weak inversion [9]. These sensors usually rely on proportional-to-absolute temperature

(PTAT) principle and generate an analog output changing almost linearly with absolute temperature. Temperature sensing using vertical substrate bipolars [10], [9] is not a very feasible solution as bipolar structures are not very well characterized in most CMOS processes. Lateral bipolar transistors as temperature sensors [11], [12] can be accurate but their performance is process-dependent and, most importantly, they can only be used in special CMOS processes. Careful optimization needed to increase the current gain and minimize the leakage current to substrate also increases design complexity of sensors with lateral bipolar transistors [9]. CMOS transistors operating in weak inversion can also be configured as temperature sensors [13], but their performance is limited due to the threshold voltage dependent temperature coefficient and leakage currents at high temperatures [2]. Another problem concerning PTAT sensors in general is their analog output which needs to be digitized on-chip, increasing the overall area and power consumption of the sensor circuitry.

Some other CMOS temperature sensors that do not rely on PTAT have been reported in recent years. A current-output sensor based on temperature dependence of MOS threshold voltage and gain factor is reported in [14], but its sensitivity depends on process-dependent parameters. The same paper reports another sensor based on the previously mentioned current-output sensor and a current-frequency converter. Low power supply sensitivity and improved accuracy is obtained at the cost of area and power. A thermal feedback oscillator sensor, exploiting the temperature dependence of thermal diffusion constant of silicon, is presented in [15]. The main drawbacks are high power and strong jitter. The thermal sensor used in PowerPC RISC microprocessors is also not suitable for multiple-sensor applications due to its high power and area consumption [8].

The performance metrics of the thermal sensor used in the PowerPC RISC are summarized in Table I. The metrics of a high accuracy temperature sensor proposed

Table I. Performance comparison of some temperature sensors used in thermal management applications

Reference	Pertijs, 2005 [16]	PowerPC [8][18][19]	Szekely, 1999 [17]
Technology	0.5μm	0.35μm	1μm
Area [mm^2]	$\sim$1.25	0.2	0.018
Range [^{o}C]	-50–120	0–128	25–125
Power [W]	130μA, 2.7–5.5V	10m (max. DC)	200μ
Resolution [^{o}C]	15m (in 30ms)	4 (in 5μs)	?
Accuracy [^oC]	$\pm$0.5 (3σ,32samp,1pt)	$\pm$12 (uncalib)	$\pm$1.6 (2σ,1pt)

by Pertijs *et al.* [16] and a low–power consumption temperature sensor by Szekely *et al.* [17] are also included in the table for comparison.

D. Proposed Temperature Sensor

The general concept of the proposed temperature sensor is depicted in Fig. 1. The difference between currents i_{in} and i_{out} is converted to frequency, which in turn controls i_{out} in a feedback loop. Frequency increases with i_{error} and in turn increases i_{out} to minimize the difference. As a result, the output frequency follows i_{in} as:

$$f_{out} = \frac{K_1}{K_1 K_2 + 1} \cdot i_{in}, \tag{1.1}$$

where the linearity of the transfer characteristics is determined by the linearity of current–to–frequency and frequency–to–current conversions. For an i_{in} changing with temperature, the output frequency will change according to the relation given in (1.1).

In the proposed temperature sensor, the input current source is realized with a gate–controlled diode (GCD). The reverse current of the GCD is in the order of

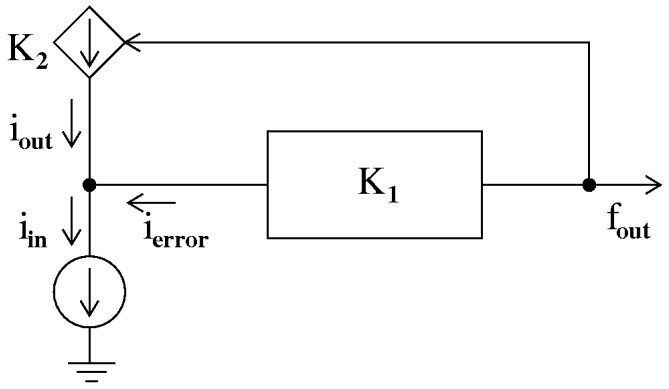


Fig. 1. Temperature sensor general presentation

pico amperes at room temperature and increases exponentially with temperature. Its high sensitivity to temperature variations promises a high resolution for the proposed temperature sensor. Its temperature sensitivity is also process–independent.

The interface–trap charge pump (ITCP) current source proposed in [20] is utilized as the frequency–controlled current source. The ITCP current source consists of two interface–trap charge pumps that translate frequency instantly to current and a cascoding transistor that produces a constant output. The output current is directly proportional to the frequency of pulse applied to the charge pump gates and changes between pA and nA depending on the input frequency. The input-output characteristic of the ITCP current source is linear for a wide range of frequencies. The temperature sensitivity of the charge pumping current is very low and the overall temperature sensitivity of the current source output can be minimized through the cascoding transistor bias. The ITCP current source, therefore, promises a linear output transfer characteristic immune to output current errors due to self–heating.

In the proposed architecture, the difference between the leakage current and the ITCP current is integrated into a voltage by a capacitor and this voltage is translated

into frequency by a voltage controlled oscillator (VCO). The feedback loop ensures that the VCO frequency is continuously adjusted to equate the leakage current and the ITCP current. The frequency output of the sensor enables easy digital interfacing.

The CMOS temperature sensor utilizing the interface–trap charge pumping phenomenon promises high resolution, linear transfer characteristics, and digital output with less area and power dissipation than conventional thermal sensors. Its small area and low power consumption makes it suitable especially for applications that require multiple sensor integration.

CHAPTER II

INTERFACE–TRAP CHARGE PUMP CURRENT SOURCE

A. Fundamentals

The ITCP current source, depicted in Fig. 2, consists of two PMOS transistors configured as interface–trap charge pumps (ITCP) and a cascoding PMOS connected to their common well. The ITCP current source was proposed by Cilingiroglu *et al.* [20] and it utilizes the interface–trap charge pumping effect [21], [22] to generate a low and constant current.

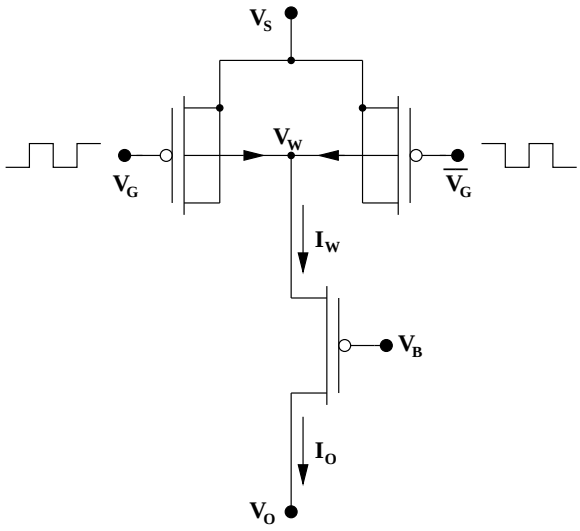
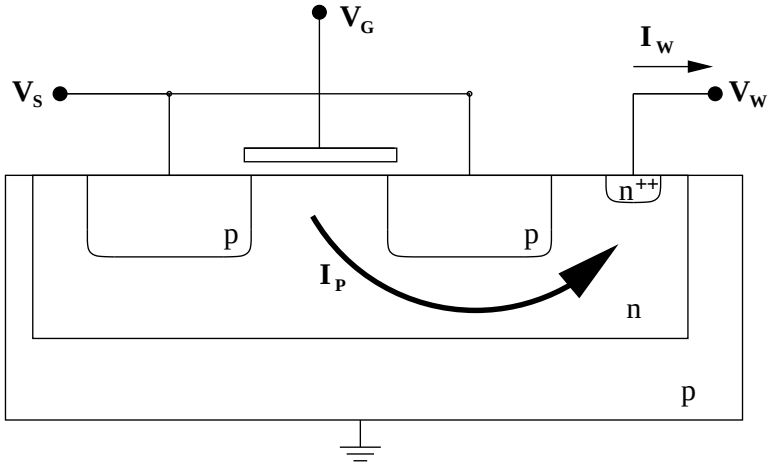


Fig. 2. Interface–trap charge pump current source schematic

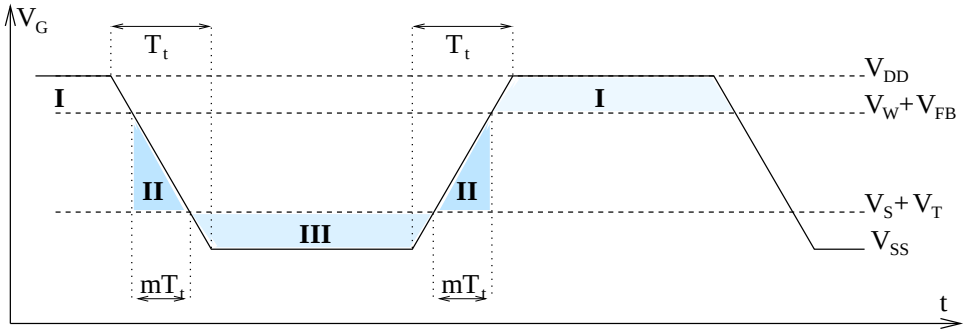
The output–terminal current of the ITCP current source changes linearly with the ITCP gate pulse frequency, and it is given by:

$$I_O = I_W \approx q \cdot A_{eff} \cdot N_{it} \cdot f, \tag{2.1}$$

where q is the electron charge, A_{eff} is the total area under the charge pump gates, N_{it} is the number of effective interface–traps per unit area, and f is the frequency of the charge pump gate pulse. Note that the cascode transistor operates under subthreshold conditions and the well current I_W is approximately equal to the total interface–trap charge pumping current, I_P, of the charge pumps.



(a)



(b)

Fig. 3. (a) PMOS transistor configured as an ITCP and (b) the applied gate voltage to induce accumulation (I), depletion (II), and inversion (III)

The ITCP current results from cycling the channel region between accumulation

and inversion conditions due to the gate pulse. It originates from the recombination of minority and majority carriers at the interface traps. PMOS transistor configured as an ITCP is depicted in Fig. 3(a) and the applied gate pulse in Fig. 3(b).

The well voltage, V_W, and the source voltage, V_S, reverse–bias the well-source junction and meet the following conditions to enable accumulation and inversion, respectively:

$$V_W < V_{DD} - V_{FB}, \tag{2.2}$$

$$V_S > V_{SS} - V_T. \tag{2.3}$$

V_{FB} is the flatband voltage and V_T is the threshold voltage of the p–channel MOSFET given by:

$$V_T = V_{FB} + 2\phi_F - \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_A(V_W - V_S + |2\phi_F|)}, \tag{2.4}$$

where C_{ox} is the oxide capacitance per unit area, and ϕ_F is the Fermi potential of the n–well.

The gate pulse periodically alternates between V_{DD} and V_{SS}. It induces inversion and accumulation conditions under the gate for $V_G < V_S + V_T$ and $V_G > V_W + V_{FB}$, respectively. Electrons moving to the surface from the n–well are captured by the interface traps in accumulation, and these traps are emptied by the captured holes moving into the channel from the source in inversion. The charge transfer due to trapped electron–hole recombination depends on the number of interface traps involved and results in a current, I_P, flowing from the source terminal to the n–well. The current magnitude is determined by the gate pulse frequency and the amount of charge transferred per unit time. I_P is given by:

$$I_P = f \cdot Q_p = f \cdot q \cdot A_{eff} \cdot N_{it}. \tag{2.5}$$

N_{it} is approximately equal to $D_{it} \cdot \Delta E$, where D_{it} is the interface trap density per unit area per unit energy and ΔE is the energy range of the charge–pumping traps. ΔE depends on the time the device spends in depletion, and it is estimated as:

$$\Delta E = 2kT \ln \frac{\tau}{mT_t}, \tag{2.6}$$

$$m \equiv \frac{V_W + V_{FB} - (V_S + V_T)}{V_{DD} - V_{SS}}, \tag{2.7}$$

where kT is the thermal energy, τ is a time constant, T_t is the transition time for the gate pulse, and m is the fraction of the transition time spent in depletion.

The shortcomings of the ITCP as a constant current source are addressed in [20] by adding a cascode transistor to the output and by complementary pumping. Complementary pumping combined with cascoding suppresses pulse feedthrough, which is an inherent problem of the bare ITCP. The cascode PMOS transistor operates in subthreshold due to the low current level, and its gate is biased to ensure $V_W > V_S$ for the ITCP. Cascoding causes the output current to be virtually independent of the output voltage. The subthreshold current for a PMOS transistor is given by:

$$I_{sub} = I_0 \cdot e^{\frac{q}{kT} V_{SG}} \left[1 - e^{-\frac{q}{kT} V_{SD}}\right], \tag{2.8}$$

where I_0, which is a function of technology parameters and W/L, is virtually independent of V_G. For $V_{SD} \gg kT/q$, subthreshold current is also assumed to be independent of V_{SD}. Therefore, the output current of the ITCP current source, I_O, is not affected by variations in the output voltage V_O. The output current is determined by the gate pulse levels, V_S, and the cascoding transistor gate voltage V_B. V_B can be used to set the accumulation level through V_W and modulate the output current. V_B also determines the disparity between I_W and I_P due to the bulk recombination current I_B. $I_W = I_P + I_B$, and I_B is expected to decrease with increasing $V_W - V_S$, therefore,

with increasing V_B.

Given the linear output current–frequency relation and the terminal voltage independent low output current, the ITCP current source is suitable to be used in the sensor application as the frequency controlled current source. Another important aspect of the cascoded pump for this application is that its temperature sensitivity can be adjusted by V_B. The overall temperature sensitivity of the ITCP current source can be, therefore, minimized or even zeroed to ensure that the temperature sensor readings are not distorted by its own temperature dependence.

B. Temperature Sensitivity

The temperature sensitivity of the ITCP current source is determined by the output current dependence on ΔE and V_W. The temperature coefficient of the output current is defined as:

$$\mathrm{TC_C} \doteq \frac{\mathrm{d}I_O}{I_O\,\mathrm{d}T} = \mathrm{TC_B} + \mathrm{VC_B} \cdot \frac{\mathrm{d}V_W}{\mathrm{d}T}, \tag{2.9}$$

where $\mathrm{TC_B}$ and $\mathrm{VC_B}$ are the temperature and voltage coefficients, respectively, defined as:

$$\mathrm{TC_B} \doteq \frac{\mathrm{d}I_W}{I_W\,\mathrm{d}T}, \tag{2.10}$$

$$\mathrm{VC_B} \doteq \frac{\mathrm{d}I_W}{I_W\,\mathrm{d}V_W}. \tag{2.11}$$

$\mathrm{d}V_W/\mathrm{d}T$ is the temperature sensitivity of the well voltage determined by the V_{GS} of the cascoding PMOS.

Considering (2.1), the temperature sensitivity of I_W is dictated by the energy dependence of N_{it}. From (2.6), ΔE of effective traps is a function of temperature

through thermal energy kT and time constant τ given by:

$$\tau = (\sigma \nu_{th} n_i)^{-1} . \tag{2.12}$$

Thermal velocity is defined as $\nu_{th} = \sqrt{3kT/m}$, where m is the effective mass. Intrinsic carrier concentration is given by:

$$n_i = n_{i0} T^{\frac{3}{2}} \exp\left(-\frac{E_g}{2kT}\right), \tag{2.13}$$

where n_{i0} is a temperature–independent constant and E_g is the silicon bandgap. Substituting (2.6), (2.7), (2.12), and (2.13) into (2.1), and ignoring the temperature sensitivity of bandgap E_g, $\mathrm{TC_B}$ is obtained as:

$$\mathrm{TC_B} \approx -\frac{1}{T}\left[\frac{E_g + 4kT}{\Delta E} - 1\right]. \tag{2.14}$$

For typical ΔE of half bandgap, $\mathrm{TC_B}$ changes between -0.4%/K and -0.3%/K for the temperature range of 300K-400K.

The expression for the voltage coefficient $\mathrm{VC_B}$ is obtained by substituting (2.6) and (2.7) into (2.1) as:

$$\mathrm{VC_B} \approx -\frac{1}{V_W + V_{FB} - (V_S + V_T)} \cdot \frac{1}{\ln\left(\frac{\tau}{mT_t}\right)}. \tag{2.15}$$

$\mathrm{VC_B}$ is determined by the gate pulse transition time and the bias voltages V_W and V_S. Depending on $\mathrm{d}V_W/\mathrm{d}T$ value for TSMC 0.18μm technology, $\mathrm{VC_B}$ can be adjusted through these two biases to set the $\mathrm{TC_C}$ value, and therefore, to obtain a minimum or zero overall temperature sensitivity for the ITCP current source. $\mathrm{d}V_W/\mathrm{d}T$ is -4mV/^{o}C for 0.5μm technology [20].

CHAPTER III

LEAKAGE CURRENT GENERATION WITH A GATE–CONTROLLED DIODE

A. Fundamentals

The so–called gate–controlled diode (GCD) is a pn–junction with an adjacent MOS gate as depicted in Fig. 4. Although very rarely utilized as a signal processing device [23], [24], it has found widespread use since the early days of solid–state development as a diagnostic tool in semiconductor surface analysis and characterization [25], [26], [27], [28], [29], [30], [31], [32].

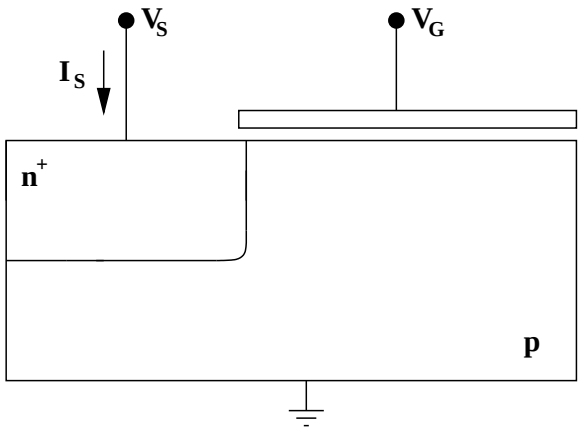


Fig. 4. n^+–p gate–controlled diode schematic

The source–terminal current I_S of a GCD reverse–biased with $V_S > 0$ has five distinct components as follows:

$$I_S = I_{dif(pn)} + I_{gen(pn)} + I_{dif(surf)} + I_{gen(surf)} + I_{gen(int)}, \tag{3.1}$$

where $I_{dif(pn)}$ is due to the electrons generated inside substrate bulk and transported to the junction by diffusion, $I_{gen(pn)}$ is due to the electrons generated inside the pn–

junction space–charge region, $I_{dif(surf)}$ is due to the electrons generated inside substrate bulk and transported to the junction by first diffusing into the surface–space charge region, $I_{gen(surf)}$ is due to the electrons generated inside the surface space–charge region, and $I_{gen(int)}$ is due to the carriers generated at the Si–SiO_2 interface of the surface space–charge region. Among the five, the first two are the conventional pn–junction leakage current components. These are independent of the gate voltage. The final three depend on the mode of the surface space–charge region, and therefore, are functions of the gate voltage. To be specific, none of the three is generated in the accumulation mode; all three are generated in the depletion mode; and, only $I_{dif(surf)}$ and $I_{gen(surf)}$ are generated in inversion. The ability of the gate voltage to modulate these three current components is the main utility of a GCD. In this work, we attempt to exploit this utility as an added degree of freedom in shaping the composition of the leakage current to be used as a temperature–sensitive variable.

The temperature sensitivity of the five components of I_S is primarily due to their dependence on the intrinsic carrier concentration n_i, which is a strongly increasing function of temperature. The relationship between these components and n_i is given by the following five expressions.

$$I_{dif(pn)} = C_{dif} A_{pn} n_i^2 \quad \text{(flows in all surface modes)}, \tag{3.2}$$

where C_{dif} is a coefficient independent of temperature and device geometry, and A_{pn} is the junction area.

$$I_{gen(pn)} = C_{gen} A_{pn} W_{pn} n_i \quad \text{(flows in all surface modes)}, \tag{3.3}$$

where C_{gen} is a coefficient independent of temperature and device geometry, and W_{pn}

is the depth of the junction space–charge region.

$$I_{dif(surf)} = C_{dif} A_s n_i^2 \quad \text{(flows in depletion and inversion)}, \tag{3.4}$$

where A_s is the gate area.

$$I_{gen(surf)} = C_{gen} A_s W_s n_i \quad \text{(flows in depletion and inversion)}, \tag{3.5}$$

where W_s is the depth of the surface space–charge region.

$$I_{gen(int)} = C_{surf} A_s n_i \quad \text{(flows in depletion)}, \tag{3.6}$$

where C_{surf} is a coefficient independent of temperature and device geometry. The depth of the space–charge regions is described by

$$W_{pn} = \sqrt{\frac{2\epsilon_s}{qN_A}(V_S + \phi_o)}, \tag{3.7}$$

where ϵ_s is the dielectric constant of silicon, q is the electronic charge, N_A is substrate doping concentration, ϕ_o is the junction built–in potential, and

$$W_s = \sqrt{\frac{2\epsilon_s}{qN_A}(V_G - V_{FB}) + \left(\frac{\epsilon_s}{C_{ox}}\right)^2} - \frac{\epsilon_s}{C_{ox}} \quad \text{(in depletion)}, \tag{3.8}$$

$$W_s = \sqrt{\frac{2\epsilon_s}{qN_A}(V_S + 2\phi_F)} \quad \text{(in inversion)}, \tag{3.9}$$

where V_{FB} is the flatband voltage, C_{ox} is the oxide capacitance per unit area, and ϕ_F is the Fermi potential of the substrate.

Based on the prediction of (3.2)–(3.7), the variation of I_S with V_G for a fixed positive V_S is plotted schematically in Fig. 5, and summarized in Table II. Note that the threshold voltage is denoted by V_T in the table, and is given by

$$V_T = V_{FB} + 2\phi_F + \frac{1}{C_{ox}}\sqrt{2q\epsilon_s N_A(V_S + 2\phi_F)}. \tag{3.10}$$

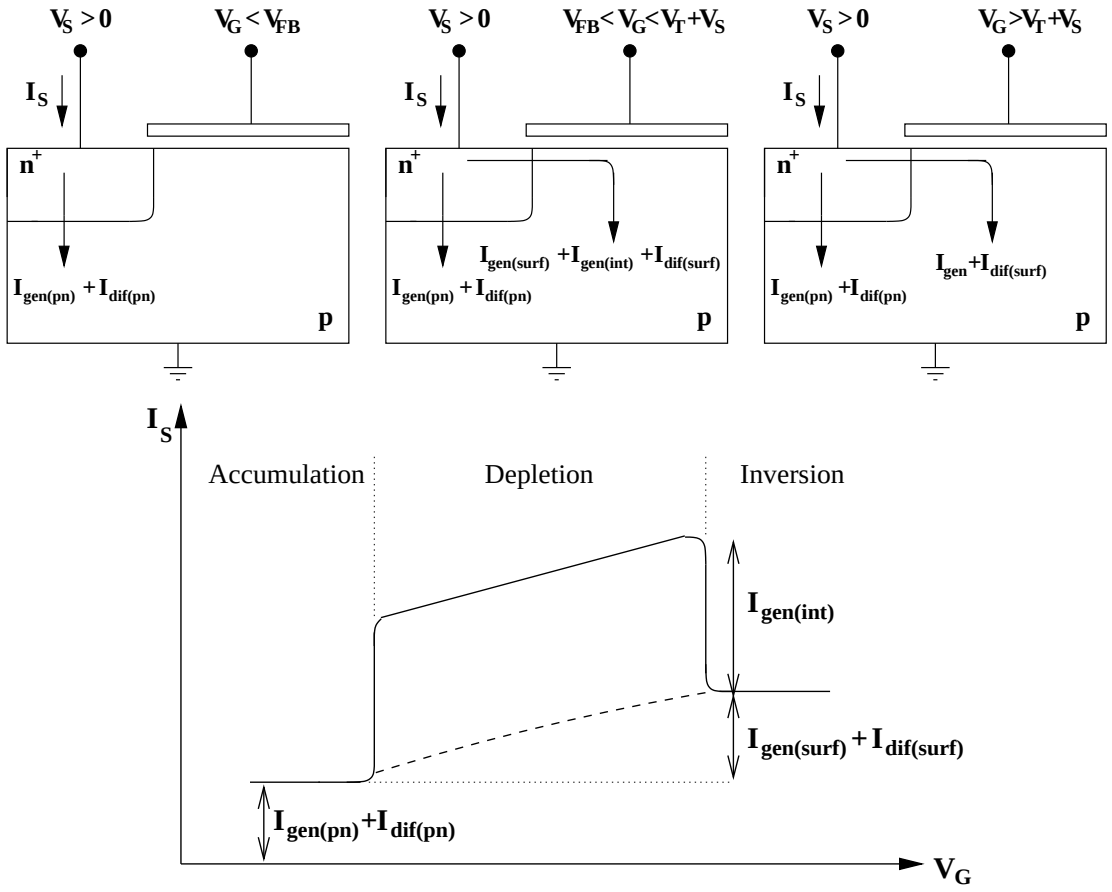


Fig. 5. Output current–gate voltage characteristics of the gate–controlled diode

The variation of I_S with V_S, on the other hand, is due to $I_{gen(pn)}$ in all modes, and to $I_{gen(surf)}$ in inversion. Both increase with V_S as a result of the increasing depth of the space–charge regions.

The model presented so far for the leakage current I_S of a GCD is valid for conservative technologies based on relatively thick gate oxides. For oxides thinner than about 4nm, the gate current must also be considered. This current communicates with the source in depletion, and with substrate in accumulation and inversion. It is known to be a very weak function of temperature [33]. Although its magnitude is minimized in depletion [34], it can easily nullify the ability of V_G to control I_S if

Table II. Variation of gate–controlled diode current components with bias conditions

Mode	Condition	$I_{dif(pn)}$	$I_{gen(pn)}$	$I_{dif(surf)}$	$I_{gen(surf)}$	$I_{gen(int)}$
Accumulation	$V_G < V_{FB}$	constant	constant	zero	zero	zero
Depletion	$V_{FB} < V_G < V_S + V_T$	constant	constant	constant	increases	constant
Inversion	$V_S + V_T < V_G$	constant	constant	constant	constant	zero

excessive. The 0.18μm technology adopted for the present work is highly prone to gate leakage as confirmed experimentally, and can be regarded as the end–of–the–road for the utility of a GCD as a controllable and temperature–sensitive leakage–current generator.

B. Temperature Sensitivity

Substituting (3.2)–(3.6) into (3.1), and combining all n_i^2–dependent diffusion terms into a single I_{dif} and all n_i–dependent generation terms into a single I_{gen}, we obtain

$$I_S = I_{dif} + I_{gen}, \tag{3.11}$$

where

$$I_{dif} \doteq C_{dif}(A_{pn} + A_s)n_i^2, \tag{3.12}$$

and

$$I_{gen} \doteq \left[C_{gen}(A_{pn}W_{pn} + A_sW_s) + C_{surf}A_s\right] n_i. \tag{3.13}$$

Next, consider

$$n_i = n_{i0}T^{\frac{3}{2}} \exp\left(-\frac{E_g}{2kT}\right), \tag{3.14}$$

where n_{i0} is a temperature–invariant coefficient, E_g is the bandgap of silicon, which is only a very weak function of temperature, k is Boltzmann's constant, and T is absolute temperature. Substituting (3.14) into (3.12) and (3.13), and using the latter two in (3.11), the relative temperature sensitivity of I_S is obtained as follows.

$$\mathrm{TC_S} \doteq \frac{\mathrm{d}I_S}{I_S\,\mathrm{d}T} = \frac{I_{gen} + 2I_{dif}}{I_{gen} + I_{dif}} \left[\frac{3}{2T} + \frac{E_g}{2kT^2}\right]. \tag{3.15}$$

For generation current components dominating the leakage current, i.e. $I_{gen} \gg 2I_{dif}$, (3.15) becomes:

$$\mathrm{TC_S} = \frac{3}{2T} + \frac{E_g}{2kT^2}. \tag{3.16}$$

The temperature coefficient changes between 7.72%/K and 4.44%/K for the temperature range of 300K-400K. If diffusion current is assumed to be the dominant current component, i.e. $I_{dif} \gg I_{gen}$, $\mathrm{TC_S}$ is calculated as:

$$\mathrm{TC_S} = \frac{3}{T} + \frac{E_g}{kT^2}, \tag{3.17}$$

and the expected temperature coefficient for the same temperature range changes between 15.4%/K and 8.88%/K.

$\mathrm{TC_S}$ variation with temperature is plotted in Fig. 6 for I_S composed of mainly generation current component and for I_S composed of mainly diffusion current component. At any temperature, $\mathrm{TC_S}$ will take a value between the two limit values, depending on the composition of I_S. At room temperature, the generation current is more dominant than the diffusion current. Therefore, a temperature coefficient around 7.72%/K is expected for the leakage current at low temperatures. However, as the temperature increases, the diffusion current will increase exponentially and $\mathrm{TC_S}$ at 400K is expected to attain a value between 4.44%/K and 8.88%/K.

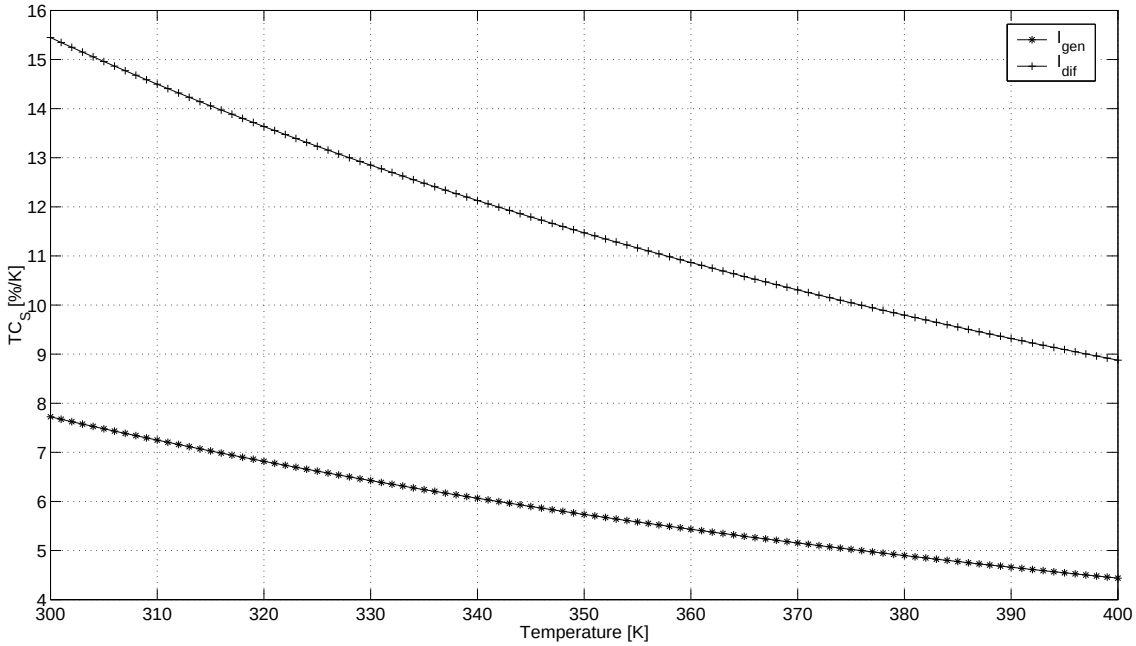


Fig. 6. TC_S variation with temperature for diffusion and generation current components

CHAPTER IV

ITCP AS A TEMPERATURE SENSOR

The temperature sensor block diagram is given in Fig. 7. The current source with output I_L is realized with an n^+–p gate–controlled diode. Two interface–trap charge pumps and the cascoding transistor of the ITCP current source described in Chapter II are illustrated in the figure. Capacitor C_p at the output of the charge pumps indicates the total parasitic capacitance associated with that node.

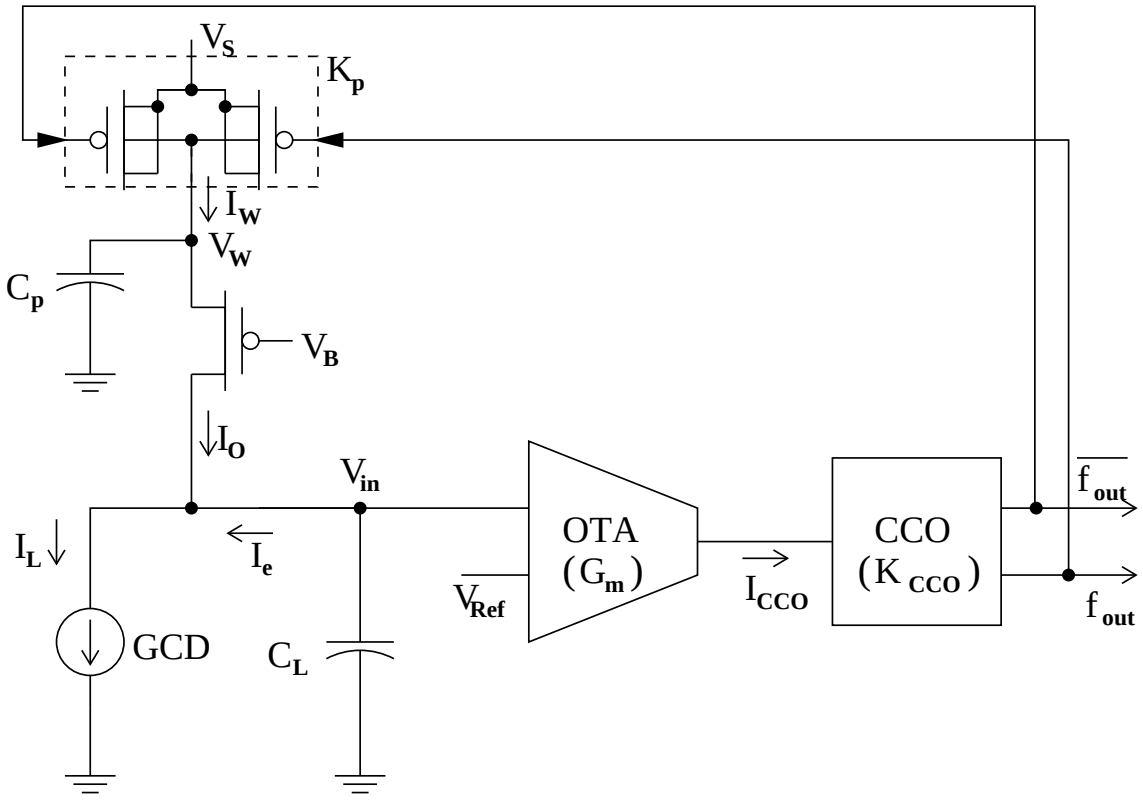


Fig. 7. Temperature sensor system blocks

I_W is approximately equal to the total interface–trap charge pumping current, I_P,

of two charge pumps with complementary gate pulse and it is given by the equation:

$$I_W = K_p \cdot f_{out}, \tag{4.1}$$

where K_p is the frequency to current conversion gain.

The output current I_O of the current source is equivalent to the difference between the charge pump current and the current flowing through the parasitic capacitance C_p:

$$I_O = I_W - sC_p \cdot V_W. \tag{4.2}$$

I_O can also be expressed in terms of the well voltage V_W and the transconductance of the cascode transistor g_m as:

$$I_O = g_m \cdot V_W. \tag{4.3}$$

The error current, I_e, is the difference between I_L and I_O and it is defined as a function of the OTA input voltage V_{in} as:

$$I_e = -V_{in} \cdot sC_L. \tag{4.4}$$

The voltage controlled oscillator consists of an OTA and a current controlled oscillator (CCO) of gain K_{CCO}. The input current to the CCO is:

$$I_{CCO} = -G_m \cdot V_{in}, \tag{4.5}$$

where G_m is the OTA transconductance. The output frequency of the CCO is given in terms of the CCO gain K_{CCO} as:

$$f_{out} = I_{CCO} \cdot K_{CCO}. \tag{4.6}$$

A. Design Considerations

The open loop diagram of the temperature sensor is given in Fig. 8. The charge pumps of the ITCP current source are replaced with a frequency–controlled current source with gain K_p in the figure.

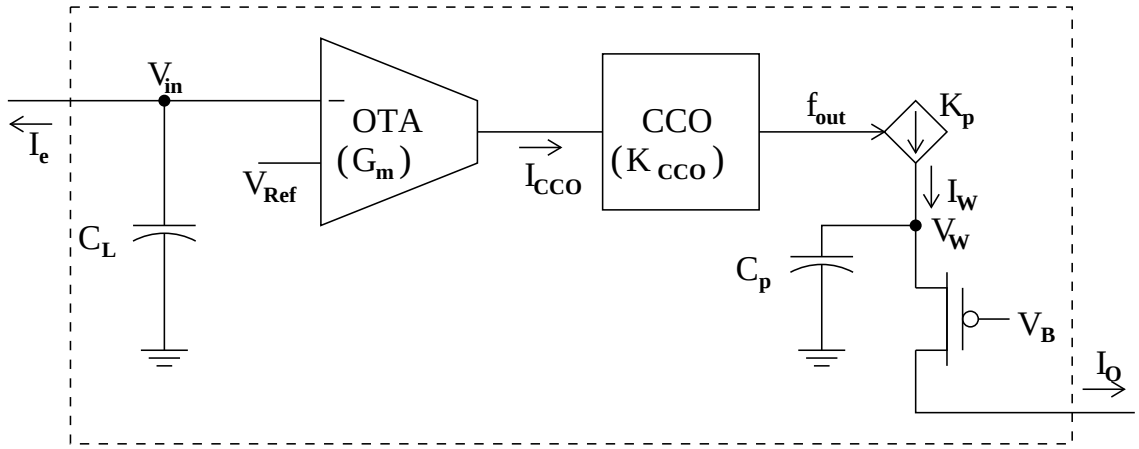


Fig. 8. Temperature sensor open loop diagram

Substituting (4.6) and (4.5) into (4.1), I_W is expressed as a function the OTA input voltage as:

$$I_W = -G_m K_{CCO} K_p V_{in}. \tag{4.7}$$

Substituting (4.7) for I_W and (4.3) for V_W, (4.2) becomes:

$$I_O = -G_m K_{CCO} K_p V_{in} - sC_p \cdot \frac{I_O}{g_m}. \tag{4.8}$$

The open loop transfer function is obtained, by substituting (4.4) for V_{in}, as:

$$A(s) = \frac{I_O}{I_e} = \frac{G_m K_{CCO} K_p}{sC_L(1 + sC_p/g_m)} = \frac{K_0}{s\,(s + g_m/C_p)}, \tag{4.9}$$

with $K_0 = G_m K_{CCO} K_p g_m / C_L C_p$ and two poles at zero and g_m/C_p.

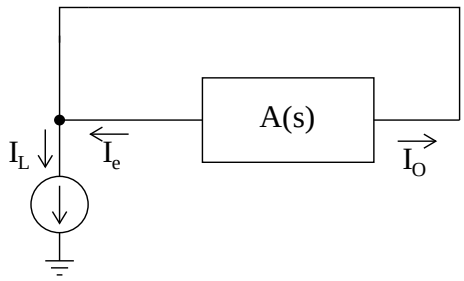


Fig. 9. Temperature sensor closed–loop diagram

Fig. 9 shows the closed-loop diagram for the temperature sensor. The closed–loop transfer function is given by:

$$\frac{I_O}{I_L}(s) = \frac{A(s)}{1 + A(s)} = \frac{K_0}{s^2 + (g_m/C_p)s + K_0}. \tag{4.10}$$

For $K_0 > (g_m/2C_p)^2$, i.e. $G_m K_{CCO} K_p / C_L > g_m/4C_p$, the roots s_1 and s_2 of $s^2 + (g_m/C_p)s + K_0$ are complex conjugate with real part $-g_m/2Cp$ and imaginary part $\pm\sqrt{K_0 - (g_m/2C_p)^2}$.

In order to determine the unity gain frequency and the phase margin, (4.9) is rearranged for s=$j\omega$ as:

$$A(\omega) = \frac{G_m K_{CCO} K_p}{\omega C_L} \cdot \frac{-\omega C_p/g_m - j}{\omega^2 (C_p/g_m)^2 + 1}, \tag{4.11}$$

and the phase and magnitude of A(ω) are obtained as:

$$\angle A(\omega) = \arctan \frac{g_m}{\omega C_p}, \tag{4.12}$$

$$|A(\omega)| = \frac{G_m K_{CCO} K_p}{\omega C_L} \frac{1}{\sqrt{\omega^2 (C_p/g_m)^2 + 1}}. \tag{4.13}$$

Rearranging (4.12), the unity gain frequency ω_1 can be expressed as:

$$\omega_1 = \frac{g_m}{C_p \tan(-180 + \varphi_m)} = \frac{g_m}{C_p \tan \varphi_m}. \tag{4.14}$$

The expression for the phase margin φ_m is derived by substituting (4.14) for ω and 1 for $|A(\omega_1)|$ into (4.13):

$$\tan\varphi_m = \frac{g_m C_L}{G_m K_{CCO} K_p C_p} \cdot \sqrt{\frac{1}{2} + \frac{G_m K_{CCO} K_p C_p}{g_m C_L}}. \tag{4.15}$$

Note that the transconductance g_m of the cascoding transistor varies with I_W as:

$$g_m = \frac{2.3}{S} I_W, \tag{4.16}$$

where the subthreshold slope S is defined as:

$$S = \left(\frac{\mathrm{d}\log(\mathrm{I}/\mathrm{I}_0)}{\mathrm{dV_{SG}}} \right)^{-1}. \tag{4.17}$$

In the sensor loop, I_W increases with temperature to equate to I_L, increasing the g_m according to (4.16) as a result. Therefore, the worst phase margin is expected at minimum I_W values in accordance with (4.15).

The $G_m K_{CCO} K_P$ product is determined by the desired temperature range and the corresponding minimum and maximum I_L. Denoting the maximum acceptable OTA input variation corresponding to this current range with ΔV_{in}, it is expressed as:

$$G_m K_{CCO} K_p = \frac{I_{max} - I_{min}}{\Delta V_{in}}. \tag{4.18}$$

As the $G_m K_{CCO} K_P$ product and g_m are mainly determined by the I_L value expected at the designed temperature range, the C_L to C_p ratio has the biggest degree of freedom to set the desired φ_m. Please note that C_p is determined by the charge pump design. Rearranging (4.15), C_L/C_p is obtained as:

$$\frac{C_L}{C_p} \cong \frac{S}{\Delta V_{in}} \cdot \frac{I_{max}}{I_{min}} \cdot \frac{\tan^2\varphi_m}{\sqrt{1 + \tan^2\varphi_m}}. \tag{4.19}$$

The output frequency of the sensor loop is determined by the OTA input voltage

and the OTA and CCO gains,

$$f_{out} = G_m K_{CCO} V_{in}. \tag{4.20}$$

Substituting (4.8) for V_{in} and (4.10) for I_O into (4.20), the output frequency is expressed as a function of the input current I_L:

$$f_{out} = \frac{1}{K_p} \cdot \frac{1 + s(C_p/g_m)}{1 + s(C_L/G_m K_{CCO} K_p) + s^2(C_L C_P/g_m G_m K_{CCO} K_p)} \cdot I_L. \tag{4.21}$$

The roots are same as those of (4.10) and there is a left–half plane zero at g_m/C_p. As indicated previously, for small values of g_m, poles are complex conjugate and peaking is expected. From (4.21), the pole frequency, ω_o, and the Q factor are:

$$\omega_o = \sqrt{\frac{G_m K_{CCO} K_p g_m}{C_L C_p}}, \tag{4.22}$$

$$Q = \sqrt{\frac{G_m K_{CCO} K_p C_p}{g_m C_L}}. \tag{4.23}$$

The overshoot expected for $Q > 0.5$, is given by [35]:

$$\%\text{overshoot} = 100 \cdot \exp\left(-\pi/\sqrt{4\mathrm{Q}^2 - 1}\right). \tag{4.24}$$

For large I_O values, for which g_m is big, single–pole behavior is assumed and the cut–off frequency is approximated as:

$$\omega_{3-dB} = \frac{G_m K_{CCO} K_p}{C_L}. \tag{4.25}$$

Considering the sensor loop given in Fig. 7, the main source of error for frequency is current error at the CCO input. Assuming that the CCO input current is $I_{CCO}+\Delta I$, and

$$f_{out} = \left[\left(I_L - (K_p f_{out} - sC_p V_W)\right) \frac{1}{sC_L} \cdot G_m + \Delta I\right] K_{CCO}, \tag{4.26}$$

the output frequency can be expressed as:

$$f_{out} = \frac{1}{K_p}\frac{1}{1+s\left(C_L/G_mK_{CCO}K_p\right)}\cdot I_L + \frac{s\left(C_L/G_mK_p\right)}{1+s\left(C_L/G_mK_{CCO}K_p\right)}\cdot \Delta i + \frac{C_pV_W/K_p}{1+s\left(C_L/G_mK_{CCO}K_p\right)}. \quad (4.27)$$

The output frequency error due to ΔI can only be minimized through low K_{CCO} according to (4.27). Note that the second error term arises because of disparity between I_W and I_O, due to leakage through the parasitic capacitance C_p.

B. Circuit Implementation

The leakage current density of a large MOS device is less than approximately 20fA/μm^2 at room temperature in TSMC 0.18μm technology. A variation of three decades is expected in I_L for the temperature range of 0^{o}C-100^{o}C. This leads to a current density of 1fA/μm^2 to 1pA/μm^2 in this temperature range. The minimum and maximum values of I_L to be processed by the sensor loop are chosen as 1pA and 1nA, considering the g_m variation according to (4.16) and its effects on circuit performance. Accordingly, the gate–controlled diode is designed with a gate area of about 1000μm^2 to obtain minimum current of 1pA.

C_L/C_p ratio is determined from (4.19). The subthreshold slope S is around 80mV/decade. Note that setting a large OTA input swing ΔV_{in}, results in a smaller C_L which moves the dominant pole away from the origin according to (4.25) and also increases the noise bandwidth $(\pi/2)f_{3-dB}$. Setting ΔV_{in} to 250mV, C_L value for a worst–case phase margin of 53^{o}C is calculated as:

$$C_L = 139\cdot C_p. \quad (4.28)$$

Given the maximum and minimum current values and the desired corresponding

V_{in} variation, the $G_m K_{CCO} K_p$ product is calculated from (4.18) as:

$$G_m K_{CCO} K_p = 4 \times 10^{-9} A/V. \tag{4.29}$$

From (4.1) and (2.1), the expression for K_p is:

$$K_p = 2qAN_{it}, \tag{4.30}$$

where A is the effective gate area for one interface–trap charge pump. The number of effective interface–traps per unit area, N_{it}, is assumed to be $2 \times 10^9 \text{cm}^2 < N_{it} < 2 \times 10^{10} \text{cm}^2$ for TSMC 0.18μm technology. Note that the charge pump area determines K_p, the cutoff frequency, and also the output frequency range, as maximum and minimum I_W values are set. The charge pumps are designed with $A \approx 3.33 \mu\text{m}^2$ yielding the minimum output frequency of 4.7kHz at 0^oC for $N_{it} = 2 \times 10^{10} \text{cm}^2$ and the maximum f_{out} of 47MHz at 100^oC for $N_{it} = 2 \times 10^9 \text{cm}^2$. The total parasitic capacitance C_p is estimated as:

$$C_p = C_{gateox} + C_J + C_{fringe} + C_{well} \cong 80fF, \tag{4.31}$$

and C_L is calculated to be around 10pF from (4.28). The corresponding cutoff frequency is 64Hz.

K_p is calculated to be $2.11 \times 10^{-17}\text{C} < K_p < 2.11 \times 10^{-16}\text{C}$ depending on N_{it}. The worst–case value is $K_p = 2.11 \times 10^{-17}$C which maximizes ΔV_{in} according to (4.18). Therefore, from (4.29),

$$G_m K_{CCO} = 1.9 \times 10^8 Hz/V, \tag{4.32}$$

is obtained for the worst–case K_p value. K_{CCO} must be minimized in order to reduce the sensitivity of the output frequency to noise in the input current of the CCO.

In order to obtain a wide tuning range of 4.5kHz - 45MHz, the current controlled

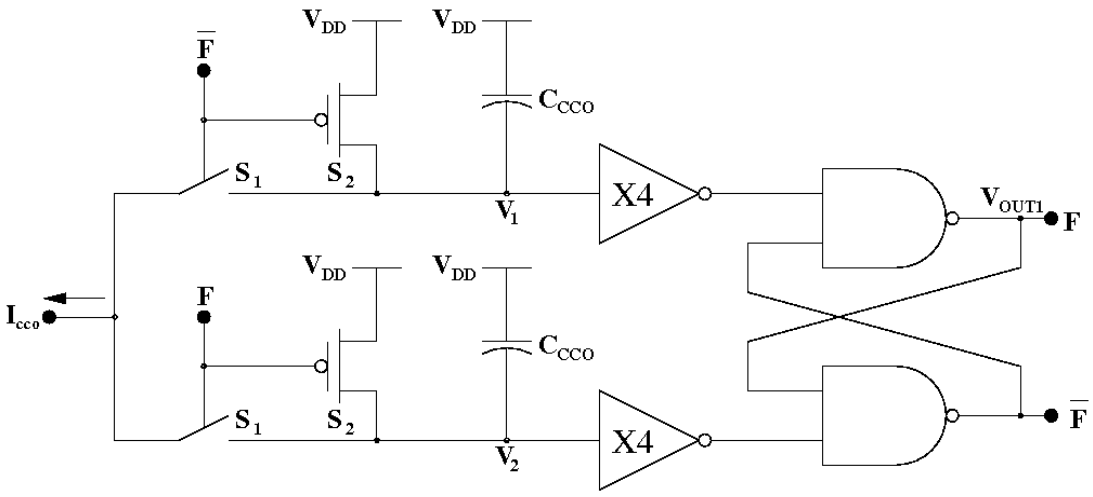


Fig. 10. Current controlled oscillator schematic

oscillator depicted in Fig. 10 is implemented [36]. The input current to the CCO is switched between the two branches by the transmission gates, denoted by S_1. PMOS switches, denoted by S_2, ensure that the two capacitors are not charged at the same time. Switches S_1 and S_2 are controlled by the outputs of the NAND gate S-R latch as shown in Fig. 10. Voltages V_1, V_2, and V_{out} are plotted in Fig. 11. Note that four inverters instead of two are used in the CCO.

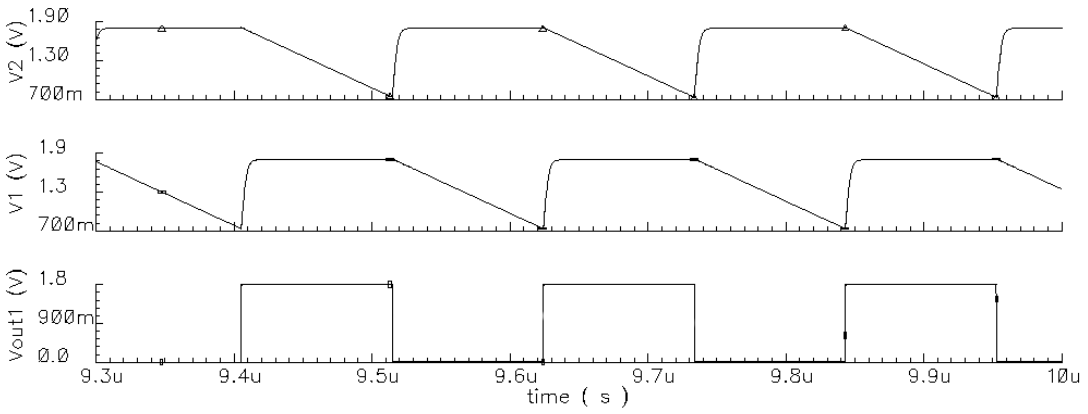


Fig. 11. Current controlled oscillator input and output waveforms

The output frequency of the CCO is determined by the input current and the capacitor C_{CCO}. K_{CCO} is:

$$K_{CCO} = \frac{F}{I_{CCO}} \cong \frac{1}{2C_{CCO}V_T}, \tag{4.33}$$

where V_T is the switching threshold of the inverters. The circuit is implemented with $C_{CCO} = 1\text{pF}$ and $V_T \approx 1\text{V}$, and K_{CCO} is around $5 \times 10^{11}\text{Hz/A}$.

The schematic of the single ended OTA used is given in Fig. 12. In order to minimize error in the output current, a very simple architecture with no current mirrors is used. Despite the noise trade–off, NMOS drivers are preferred instead of PMOS in order to isolate the input signal from the CCO input and to avoid clock feedthrough. Note that a large output swing can be achieved with this OTA.

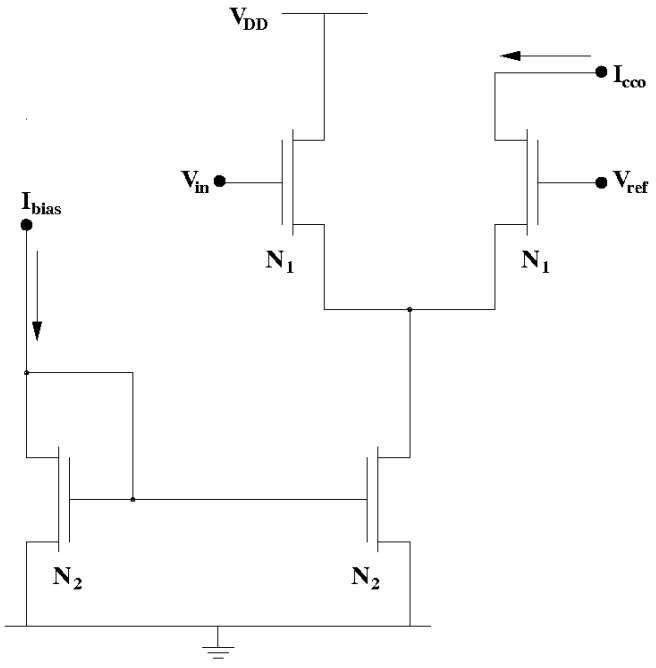


Fig. 12. Operational transconductance amplifier schematic

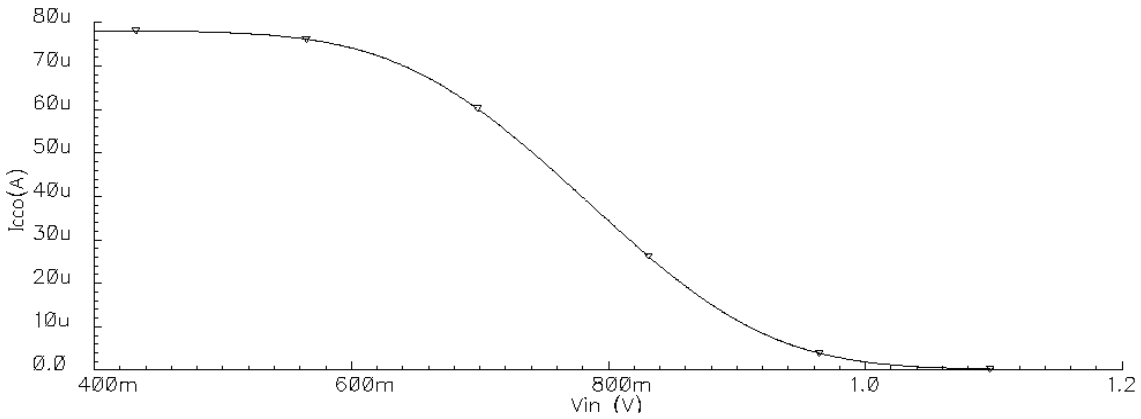


Fig. 13. Single–ended OTA transfer characteristics

The output current variation with input voltage for the single–ended OTA is plotted in Fig. 13. The bias current is 100μA and the reference voltage of the OTA is set to 770mV. G_m of 268μA/V is obtained.

CHAPTER V

TESTING AND CHARACTERIZATION

The prototype temperature sensor is fabricated using TSMC 0.18μm technology. The die photo and the prototype temperature sensor photo are given in Fig. 14. Stand–alone ITCP current source and gate–controlled diode devices are also fabricated on the same chip for characterization purposes. Important process parameters are summarized in Table III.

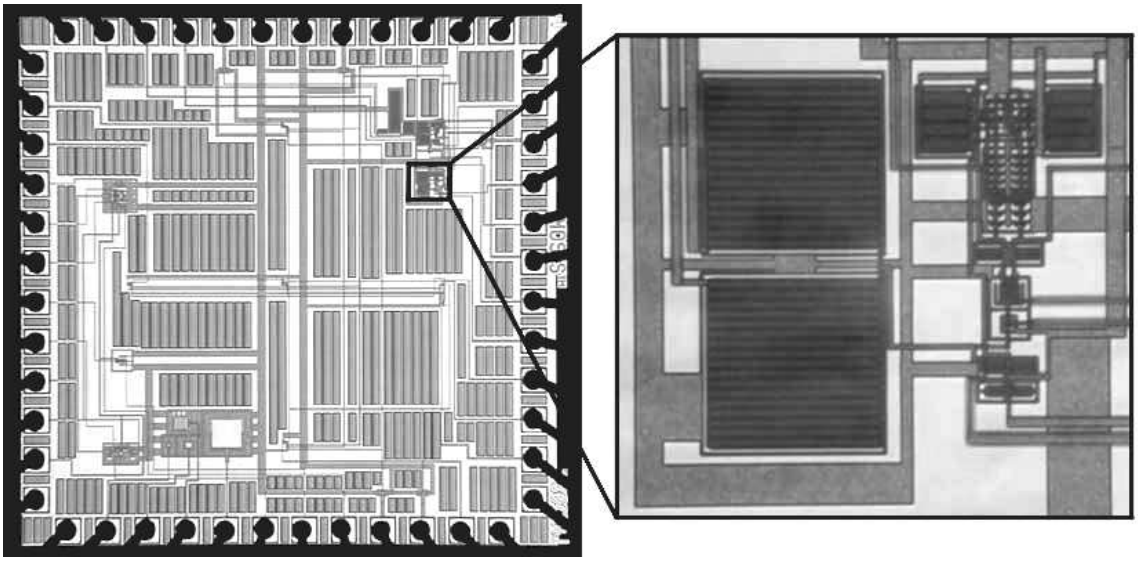


Fig. 14. Die and prototype temperature sensor photos

Table III. Process parameters for TSMC 0.18μm technology (Run:T36Q LO EPI)

Parameter	NMOS	PMOS	Units
V_{THO}	376	-404	mV
N_{CH}	2.3549×10^{17}	4.1589×10^{17}	cm^{-3}
T_{OX}	4.1	4.1	nm
C_{OX}	8.42×10^{-7}	8.42×10^{-7}	F/cm^{-2}

A. ITCP Current Source Characterization

The measurement setup and the reference current direction for the ITCP current source are given in Fig. 15. The ITCP current source consists of two source–drain shorted PMOS transistors configured as interface–trap charge pumps and a cascoding transistor. A complementary pulse is applied to the charge pump gates.

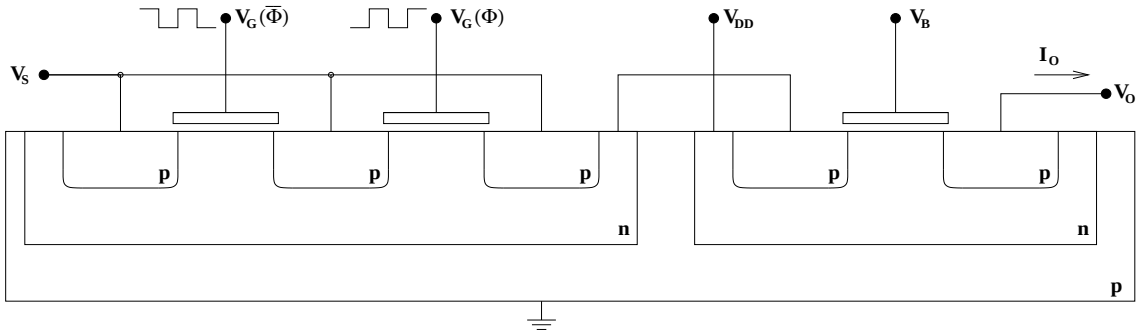


Fig. 15. ITCP current source measurement setup

There are 6 stand–alone ITCP current sources in each chip for characterization. 5 of the current sources are identical and are located at four sides and in the middle of the die to observe variation of N_{it}. The sixth charge pump has the same cascode device but the channel width, thus the gate area for interface–trap charge pumping, is increased 4 times. Note that channel length is constant and 0.54μm for all ITCP devices in order to avoid geometric current component. The dimensions for ITCP transistors and the cascoding transistor are given in Table IV.

Output characteristic of the ITCP current source, with total charge pumping area of $2 \times 3.6\mu\text{m}^2$, is plotted in Fig. 16 for different cascoding PMOS gate bias, V_B, values. Gate pulse frequency f is 500kHz, and the rise and fall times for the pulse is $T_t = 10$nsec. V_S is fixed at 600mV in order to maximize $V_W - V_S$ to minimize bulk

Table IV. Transistor dimensions for the stand–alone ITCP current sources

Device	L [μm]	W_{total} [μm]	Fingers	W_{finger} [μm]	A_{gate} [μm^2]
ITCP 1-5	0.54	6.66	2	3.33	3.5964
ITCP 6	0.54	26.64	8	3.33	14.3856
Cascode PMOS	0.9	0.9	1	0.9	-

recombination current I_B, while satisfying the inversion condition $V_S > V_{SS} - V_T$.

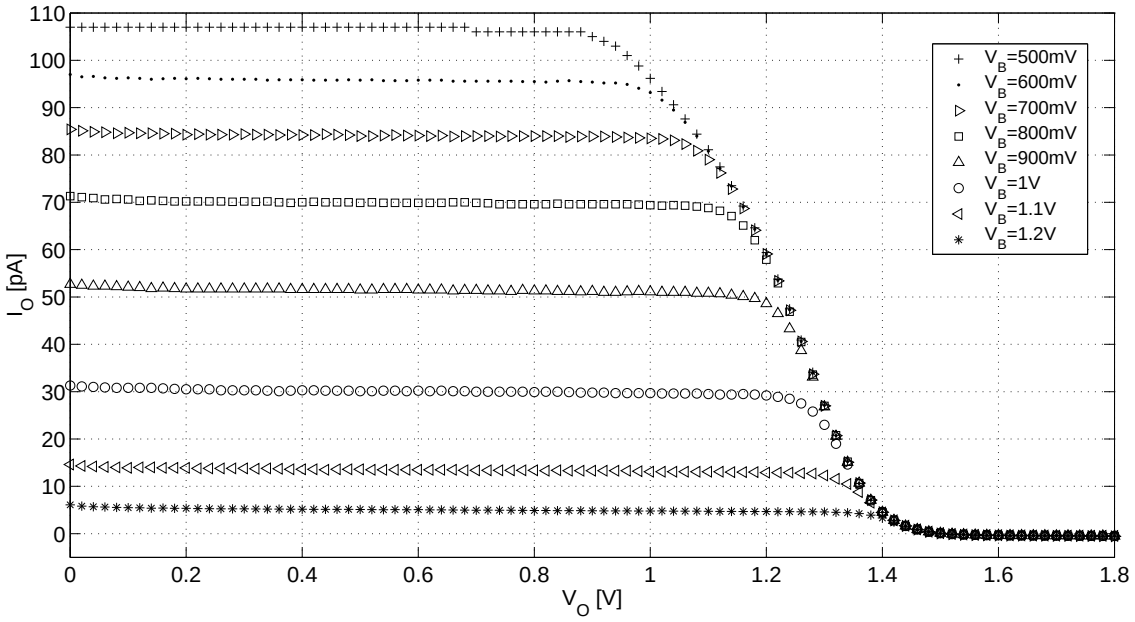


Fig. 16. Output characteristics of ITCP current source for f= 500kHz and T_t =10nsec

Fig. 16 shows that the output current is virtually insensitive to output voltage variations, and it is mainly determined by V_B for a given gate pulse. V_W increases with V_B and causes a decrease in I_P due to the bias dependence of τ [37] and m given by (2.7). For higher V_W values, the contribution of I_B to the ITCP well current also decreases. Note that for higher V_B biases, the voltage dependence of I_P is even stronger as the device deviates from strong accumulation conditions. On the other

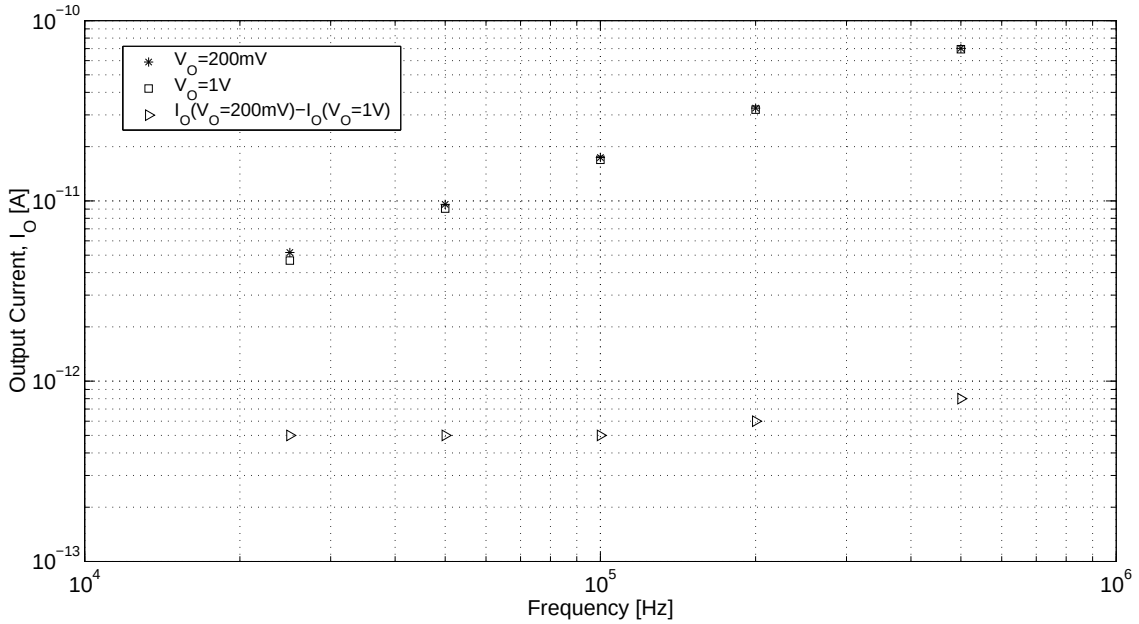
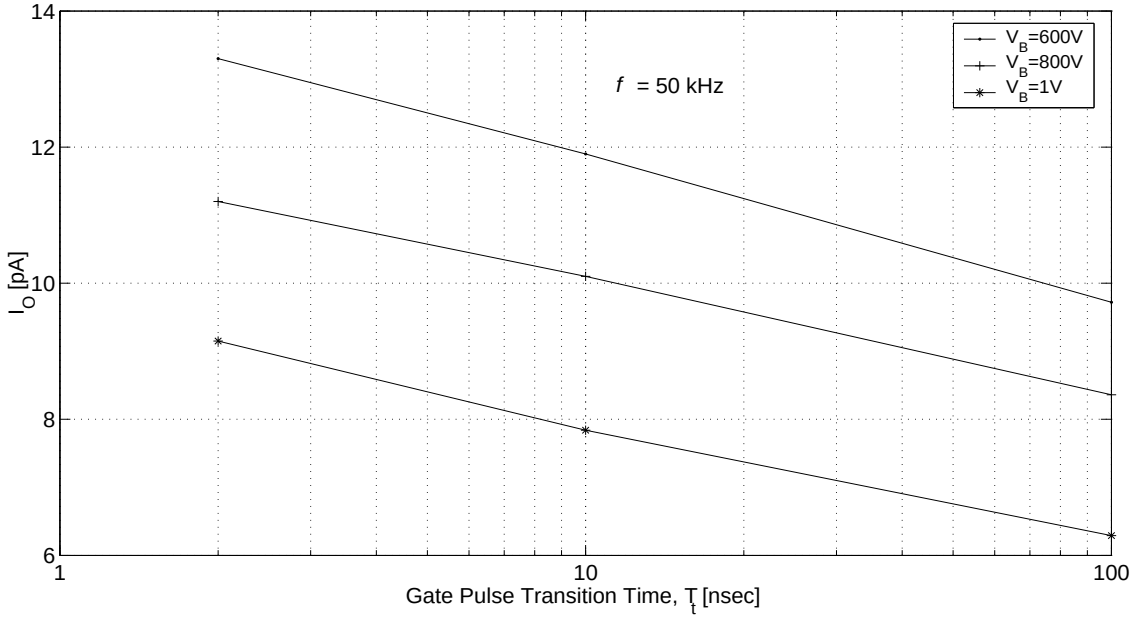


Fig. 17. Variation of output current – frequency characteristics with output voltage

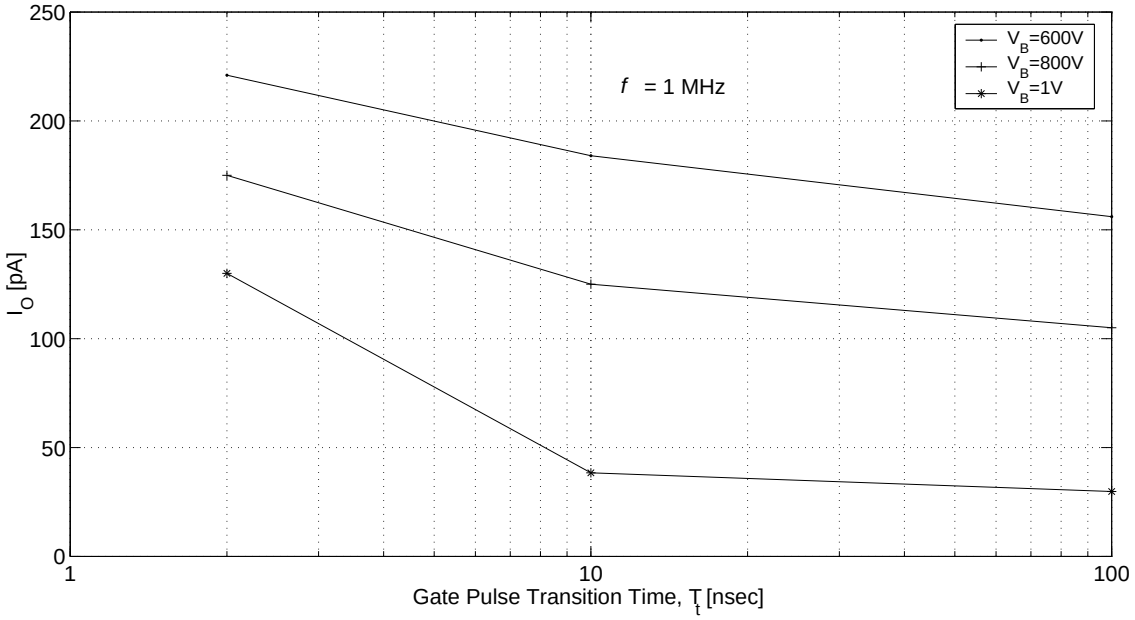
hand, with increasing V_B, the compliance voltage of the current source is minimized.

The output current variation with V_O is plotted in Fig. 17 for a gate pulse frequency range of 25kHz-500kHz. V_B and V_S are fixed at 800mV and 600mV, respectively, and T_t is 10nsec for all applied gate pulses. Note that the output current sensitivity to V_O is very small and decreases even more with increasing frequency. The highest relative variation is observed at low frequencies, where I_W and, therefore, V_{WB} is small. For small V_W values, the output voltage curtails the subthreshold current of the cascoding PMOS through its decreased source–drain voltage.

The output current variation with the gate pulse transition time is plotted for V_B at 600mV, 800mV, and 1V in Fig. 18 (a) and (b) with f= 50kHz and f= 1MHz, respectively. V_S is 600mV and V_O is 770mV. For f= 50kHz, the output current decreases almost logarithmically with T_t, as expected, for all three bias conditions. This logarithmic dependence is expressed in ΔE given by (2.6) and is explained by



(a)



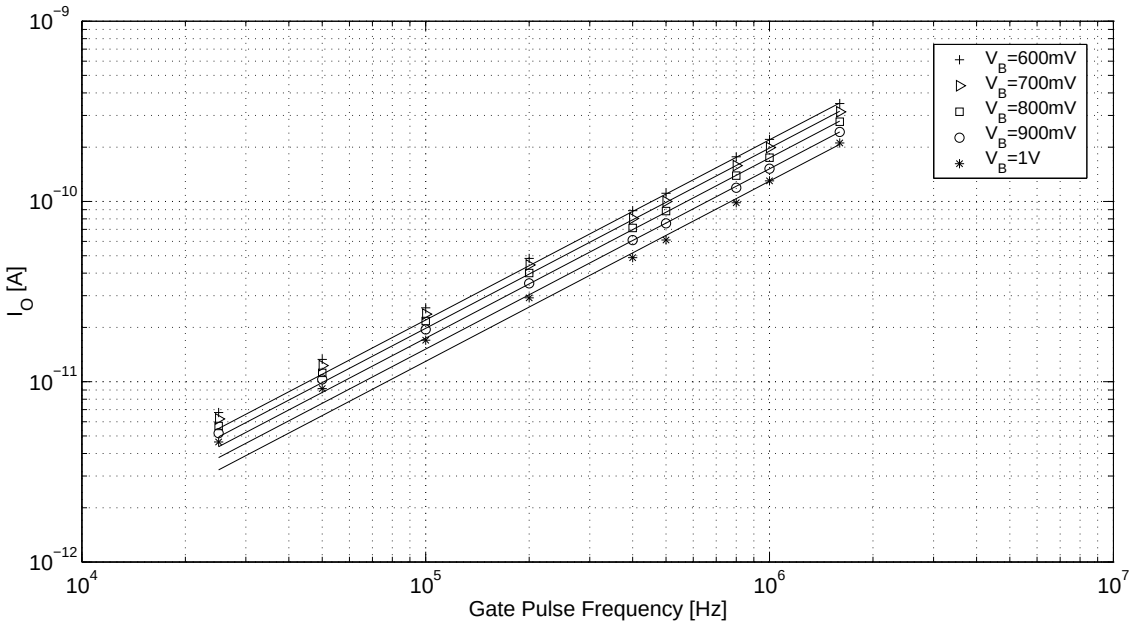
(b)

Fig. 18. Variation of output current with gate pulse transition time for clock pulse at (a) 50kHz and (b) 1MHz

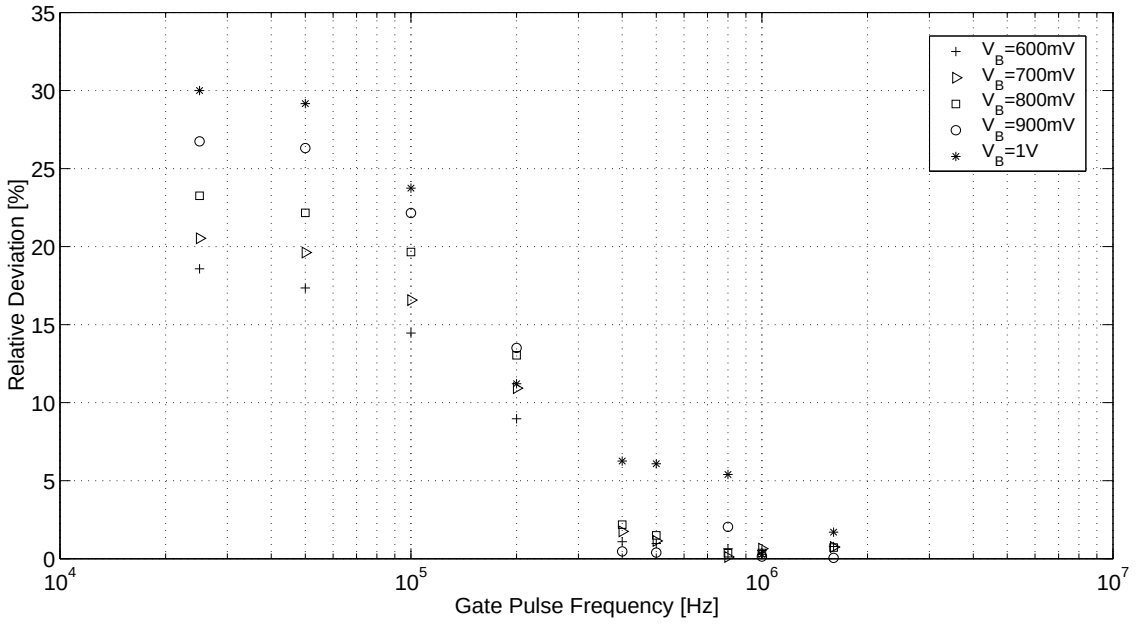
the variation of trap potential with time slowing down logarithmically with increasing T_t [38]. For f= 1MHz, the logarithmic relation does not hold especially for higher V_B values. This can be attributed to increasing trap time constant and decreasing accumulation and inversion times. The trap time constant is a strong function of the surface potential and attains its smallest values for strong accumulation and inversion conditions [21]. For increasing V_B values, V_W also increases causing weaker accumulation. As a result, the trap time constant is also expected to increase with V_B. If the accumulation and inversion times are not sufficiently long for carrier trapping to reach a steady-state limit, I_P will be nearly proportional to the pulse duration. For high frequencies, the base and peak time of the gate pulse does not accommodate steady–state occupancy of traps, especially with increasing V_W. Thus, I_P does not saturate, and it is limited by inversion and accumulation times. More detailed analysis on the effect of accumulation and inversion times on I_P can be found in [37].

In order to preserve the linear current–frequency characteristics of the ITCP current source at high frequencies, the transition time of the gate pulse should be kept short enough to avoid I_P limitation explained above. The output current variation with the gate pulse frequency is plotted in Fig. 19(a) for T_t = 2nsec. Regression lines $I_W = qA_{eff}fN_{it}$ fitted for each data set are also shown in the figure with solid lines. Fitting with relative deviation less than 5% is possible only for $f>$ 200kHz as depicted in Fig. 19(b). The deviation from linearity increases at low frequencies, especially at higher V_B biases. Bulk recombination current I_B is expected to decrease with V_B. Geometric current component which becomes effective for low transition times is expected to be negligible for $L < 1\mu$m [39]. Therefore, the observed increase in I_W can be attributed only to leakage currents.

N_{it} values obtained from the fitted regression lines are summarized in Table V. N_{it} decreases for higher V_B values due to decreasing ΔE.



(a)



(b)

Fig. 19. (a) Variation of output current with gate pulse frequency for T_t =2nsec with regression lines and (b) relative deviation from linearity

Table V. N_{it} values estimated by regression line $I_W = qA_{eff}fN_{it}$

V_B [V]	0.6	0.7	0.8	0.9	1
N_{it} [10^{10}cm^{-2}]	1.9102	1.7181	1.5151	1.3189	1.1264

1. Temperature Sensitivity

The output current variation with temperature is plotted in Fig. 20 for V_B of 800mV, 900mV and 1V. The complementary gate pulse is at 200kHz with T_t = 2nsec. V_S and V_O are fixed at 600mV and 770mV, respectively. As the temperature increases, I_P decreases, as expected, due to decreased ΔE of the charge pumping traps. However, at elevated temperatures, i.e. $T > 80^oC$, the temperature sensitivity of I_O increases rapidly. This can be attributed to the emission of trapped charges before recombination, which is eventually expected to terminate I_P [40].

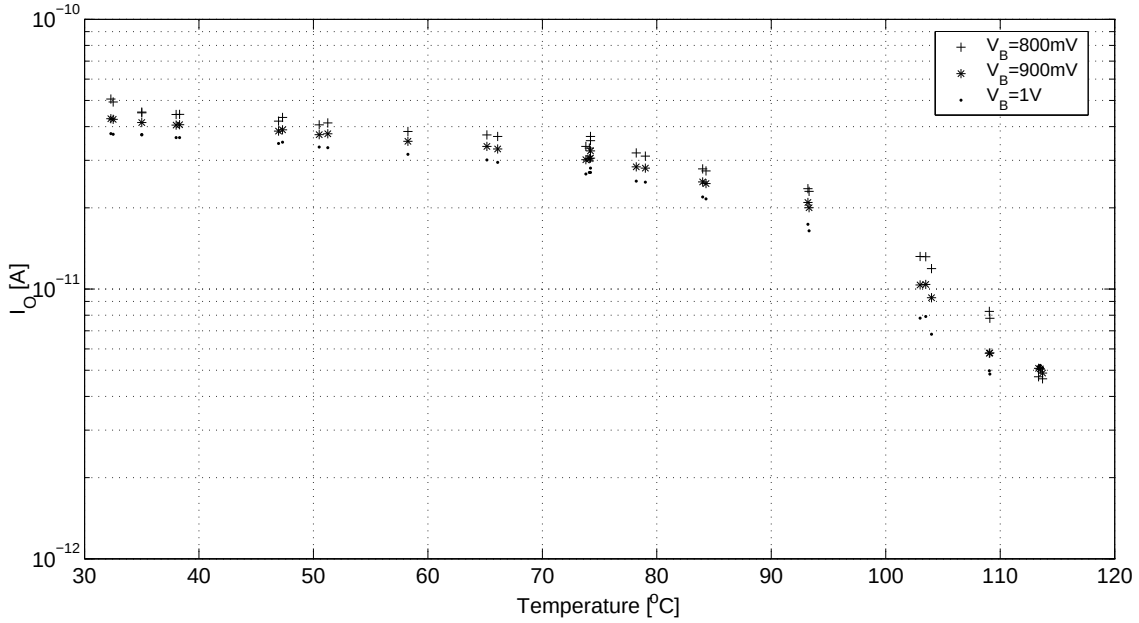


Fig. 20. Variation of output current with temperature

B. Leakage Device Characterization

The source-drain shorted NMOS transistor is used as n^+/p gate–controlled diode. There are 3 stand-alone leakage devices with scaled gate areas in each chip. The transistor dimensions for the three different devices are given in Table VI. The leakage device used in the sensor has the same dimensions with Device 1.

Table VI. Transistor dimensions for the stand–alone leakage devices

Device	L [μm]	W_{total} [μm]	Fingers	W_{finger} [μm]	A_{gate} [μm^2]
1	1.8	679.32	17	39.96	1222.776
2	1.8	2717.28	68	39.96	4891.104
3	1.8	169.825	5	33.965	305.685

The output current of the leakage device has been characterized using an Agilent 4156C Precision Semiconductor Parametric Analyzer. The device setup and the source current reference direction are given in Fig. 21.

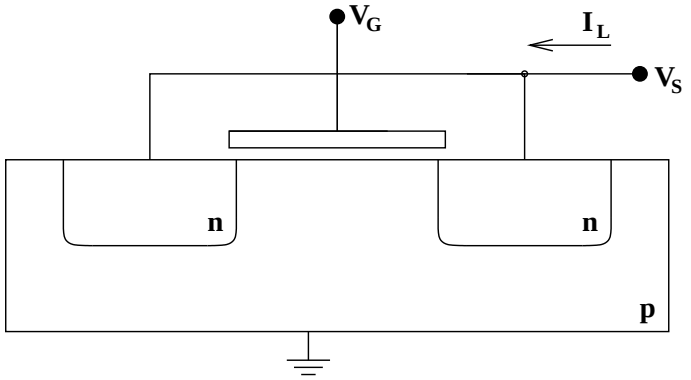
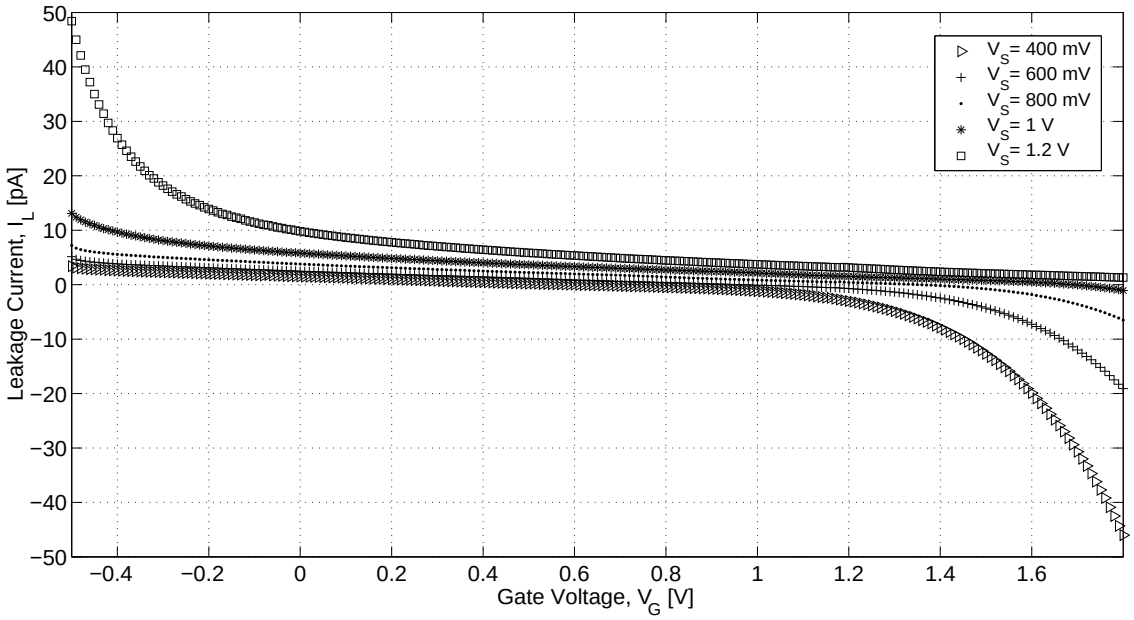
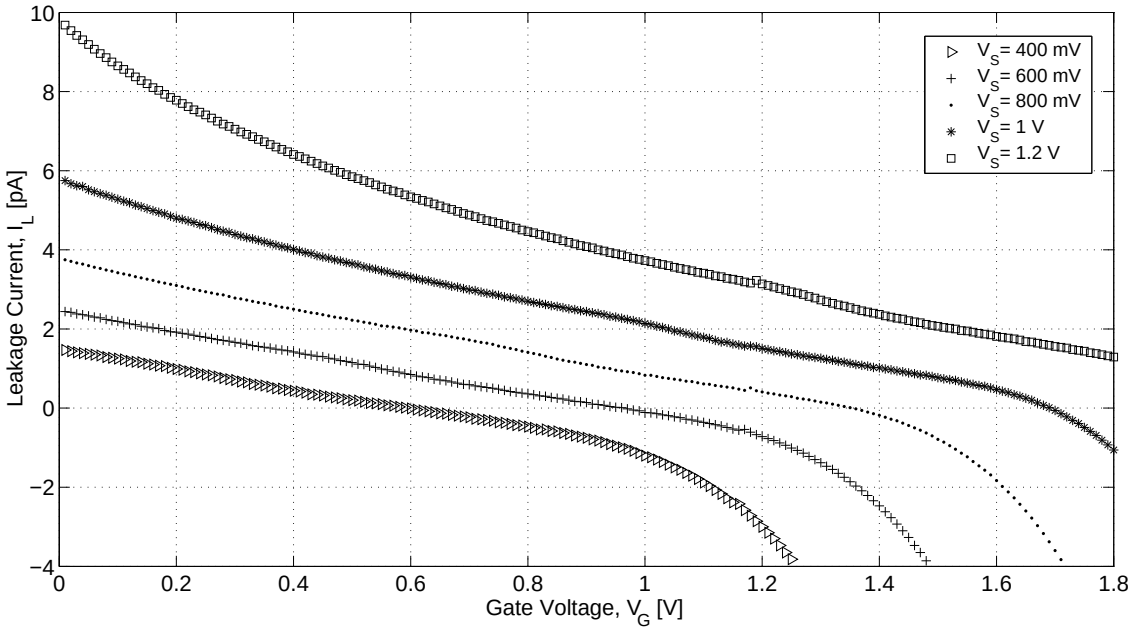


Fig. 21. Leakage device measurement setup and current reference direction

The leakage current variation with V_G for different V_S values is plotted in Fig. 22(a) for Device 1 at room temperature. Fig. 22(b) shows detail from Fig. 22(a).



(a)



(b)

Fig. 22. (a) Leakage device current variation with gate voltage and source voltage, (b) detail from (a)

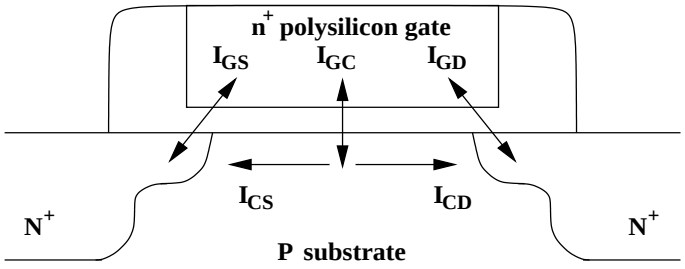


Fig. 23. Direct gate tunnelling current components

The output characteristic of the leakage device is different than the expected gate–controlled diode characteristics due to dominant direct gate tunnelling current. For high V_{GS} values, significant gate-to-source currents give rise to negative I_S. When V_{GS} increases in the negative direction, the tunnelling current flows from the source terminal to gate, causing rapid increase in I_S.

Gate tunnelling currents become significant for reduced gate oxide thicknesses and high transversal electric fields [41]. Direct gate tunnelling dominates over other tunnelling mechanisms for CMOS technologies with thin-oxide and low power supply limits [42]. Direct tunnelling current is not only between gate and substrate but also between gate and source/drain–gate overlap regions as depicted in Fig. 23. Electrons tunnelling to the gate from the channel result in a current flow between the channel and source/drain regions due to the inverted channel.

The magnitude of I_L is plotted in Fig. 24 in logarithmic scale. Note that the dips in $|I_L|$ plots correspond to I_L sign change, and current values to the right side of the dips are negative. For $V_G < 0$V, the leakage current consists of the output current of the gate–controlled diode and edge direct tunnelling currents I_{SG} and I_{DG}, due to electrons tunnelling from the accumulated n^+ polysilicon to the S/D overlap regions. There is no significant current flowing between the gate and the depleted channel for $V_{fb} < V_G < 0$V. For $V_G > 0$V, electron tunnelling from the substrate to

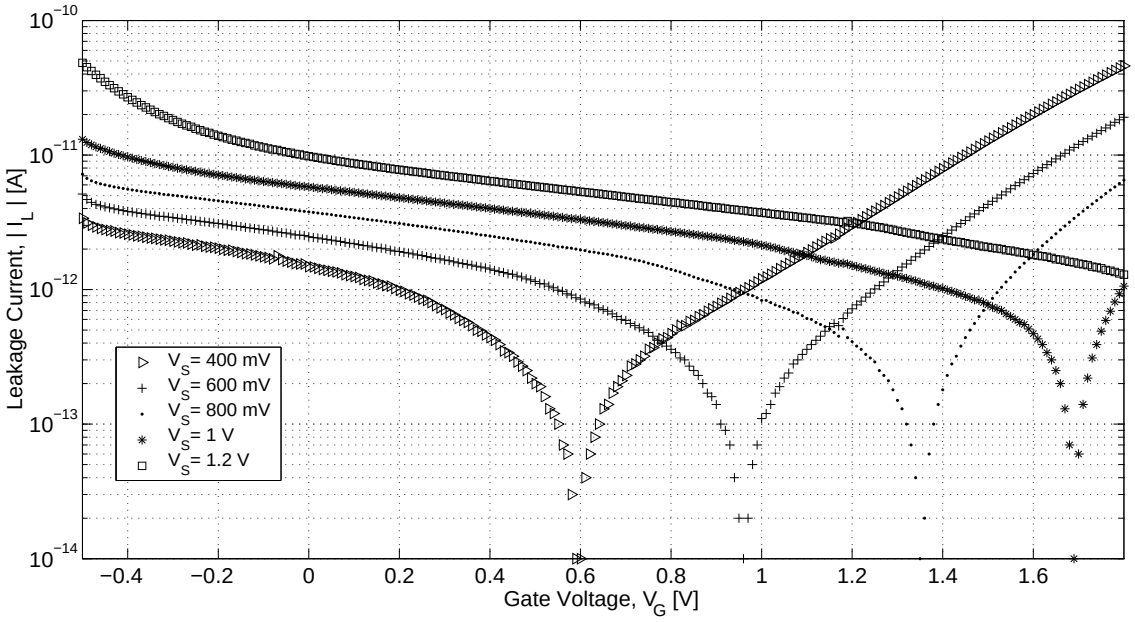


Fig. 24. Leakage current magnitude variation with gate voltage and source voltage

the gate rapidly increases with electron concentration increase in the channel area. When $V_{GS} > 0$V, edge tunnelling current flows from the gate to the S/D overlap. Both I_{GS}/I_{GD} and I_{GC} are subtracted from the conventional gate-controlled diode current, causing I_L to change sign for sufficiently high V_{GS} values. The rapid increase with V_G for negative I_L values is due to I_{GC}, which dominates over edge tunnelling currents [34].

Components of I_L for different bias conditions can be summarized as:

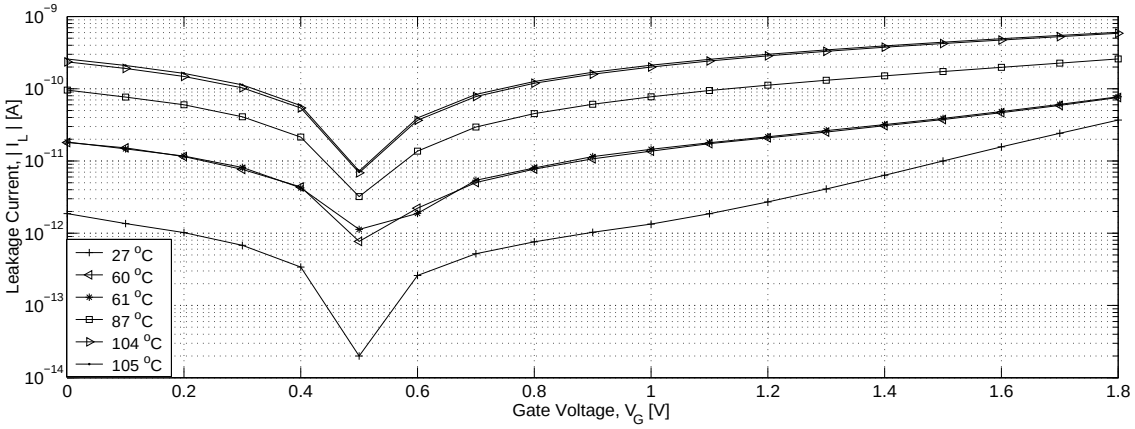
$$I_L = I_S + I_{SG} + I_{DG} \quad (\text{for } V_G < 0V \text{ and } V_{GS} < 0V), \tag{5.1}$$

$$I_L = I_S + I_{SG} + I_{DG} - I_{GC} \quad (\text{for } V_G > 0V \text{ and } V_{GS} < 0V), \tag{5.2}$$

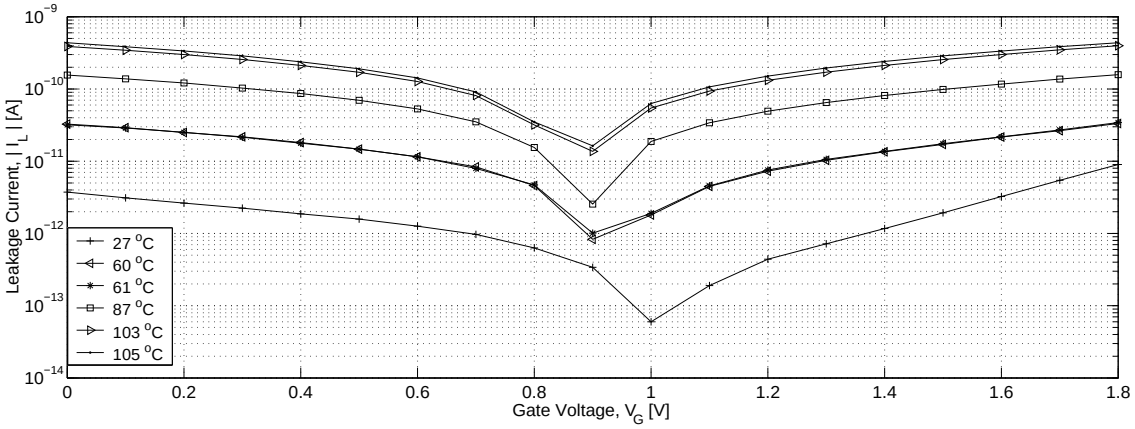
$$I_L = I_S - (I_{GS} + I_{GD} + I_{GC}) \quad (\text{for } V_G > 0V \text{ and } V_{GS} > 0V), \tag{5.3}$$

where I_S is the conventional gate–controlled diode terminal current.

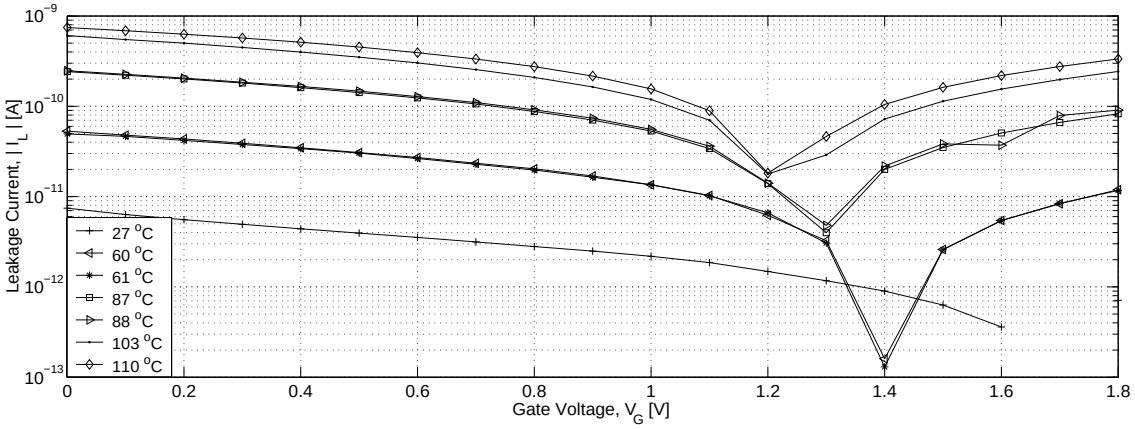
Fig. 25 (a), (b), and (c) depict I_L magnitude variation with gate voltage and



(a)



(b)



(c)

Fig. 25. Leakage current magnitude variation with temperature and gate voltage for (a) V_S =470mV (b) V_S =770mV (c) V_S =1.07V

temperature for $V_S = 470$mV, $V_S = 770$mV, and $V_S = 1.07$V, respectively. The dips in $|I_L|$ plots again correspond to I_L sign change. It is observed that for higher V_S values, the dip shifts to lower gate voltages with increasing temperature. This change can be attributed to increasing I_{GC} with temperature. Tunnelling current is generally considered to be limited only by tunnelling mechanisms, i.e. oxide thickness, oxide voltage, and to have weak or no temperature dependence. However, there are also reports of temperature–dependent direct tunnelling behavior [43], [44], [45]. It is suggested that electron concentration, which is temperature–dependent, is the limiting factor for substrate–to–gate tunnelling under depletion conditions. I_{GC} is thus enhanced with temperature due to the increase in available electrons for tunnelling. It is also observed from Fig. 25 that I_{GC} temperature dependence tends to decrease under inversion conditions.

I_L composition for $V_G > 0$V and $V_{GS} < 0$V is given by (5.2). I_L mainly consists of I_S under these bias conditions, as I_{DG}/I_{SG} and I_{GC} tend to cancel each other; former decreasing, latter increasing with V_G [34]. I_L variation with temperature in this region of operation can be attributed to the temperature dependence of diffusion and generation currents of the gate–controlled diode.

1. Temperature Sensitivity

The leakage device source voltage is determined by the OTA reference voltage in the sensor loop, and it is 770mV. The output current variation with temperature at this source voltage is plotted in Fig. 26 for V_G values between 300mV and 800mV, for which gate tunnelling component is minimum. Multiple regression model for the data is estimated as:

$$I_L = A \cdot X^2 + B \cdot X, \tag{5.4}$$

where

$$X = T^{3/2} \exp(-E_g/2kT). \tag{5.5}$$

X^2 and X are the temperature–dependent parts, and A and B are the temperature–independent parts of I_{dif} and I_{gen}, respectively. A and B are solved by least squares method. The fitted curves are given by solid lines in Fig. 26 for V_G = 300mV to V_G = 600mV. Note that fitted regression curves give bigger errors for increasing V_G values as I_{GC} starts to dominate. Especially at high temperatures, the effect of I_{GC} becomes observable as less increase in I_L with temperature. The relative error of regression is less than 10% only for V_G = 300mV and V_G = 400mV. Only under these two bias conditions I_L is close to I_S of the GCD given by (3.1).

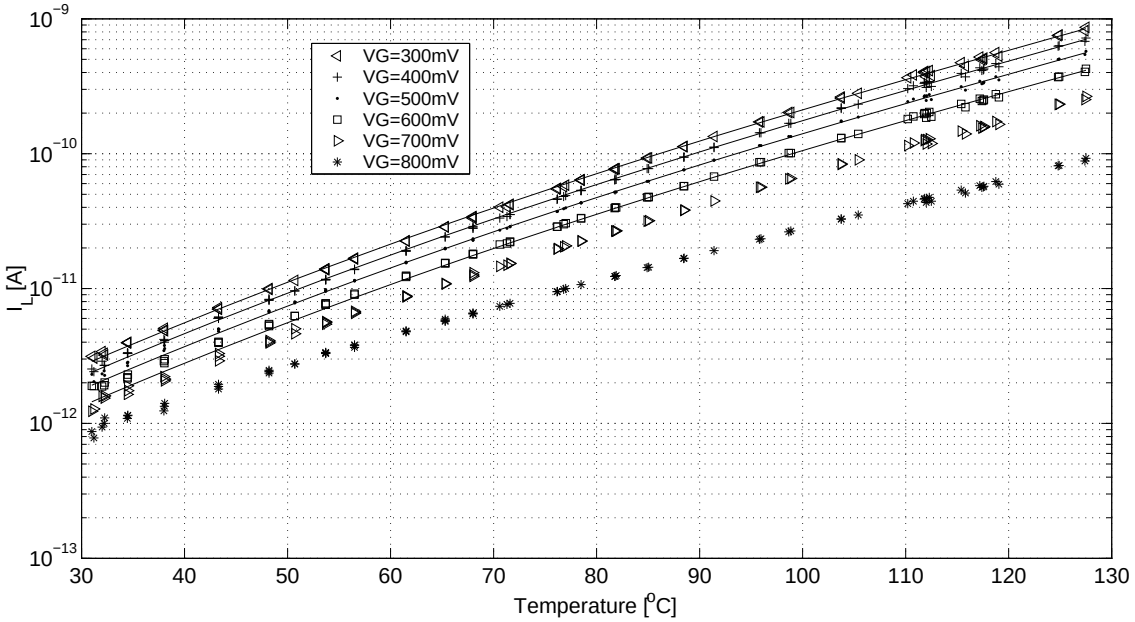


Fig. 26. Leakage current variation with temperature for 300mV$\leq$ V_G $\leq$800mV and V_S =770mV

Note from Fig. 26 that I_L decreases with increasing gate voltage under depletion

conditions. It might be due to weakly inverted parts of the surface causing a reduction in the interface generation rate [27]. However, it might also be due to I_{GC}. It is not possible to determine the exact reason for the decrease as the tunnelling currents cannot be measured with the fabricated leakage devices.

The temperature coefficients for I_L at $V_G = 300\text{mV}$ and $V_G = 400\text{mV}$ are calculated from their regression polynomials and plotted in Fig. 27. The same plot also shows the theoretical TC_S, given by (3.16) for $I_{gen} \gg I_{dif}$. Temperature sensitivity is of the output current is same as the theoretical value at low temperatures. It increases over the theoretical TC_S for $T > 70^o\text{C}$, as expected, due to diffusion current components.

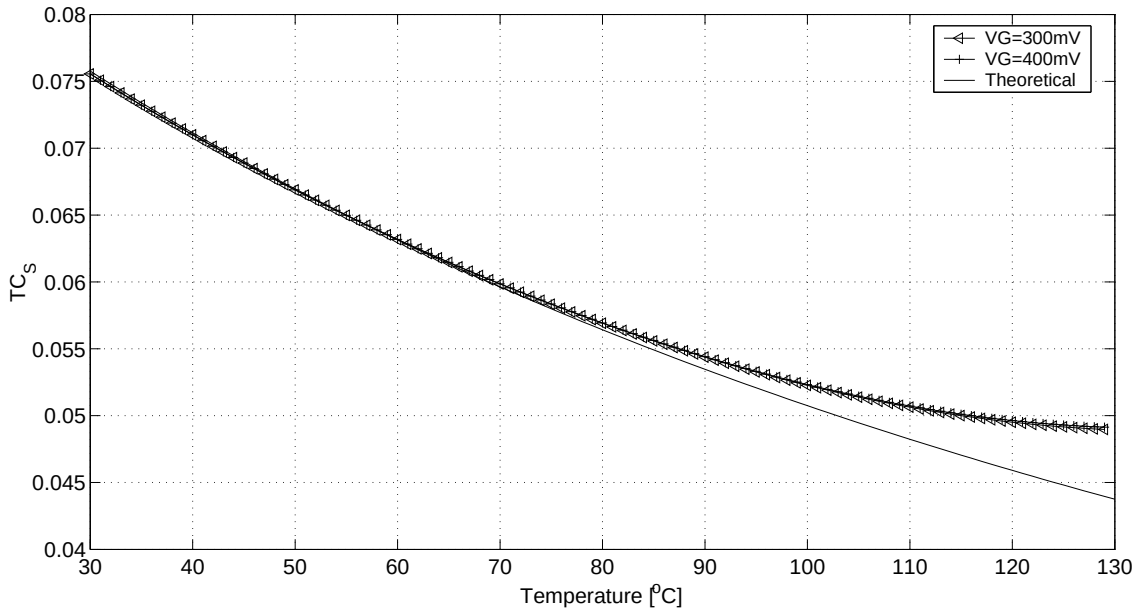


Fig. 27. Measured and theoretical leakage current temperature coefficient

C. Temperature Sensor Characterization

The schematic of the implemented temperature sensor is given in Fig. 28. The input and output pins to the chip are indicated in the figure. The detailed schematic of the current controlled oscillator with output buffers is illustrated in Fig. 29.

The bias conditions for the temperature sensor are summarized in Table VII. These values are used for all measurements unless otherwise specified.

Table VII. Temperature sensor bias conditions

$I_{bias}[\mu A]$	V_{ref}[mV]	V_S[mV]	V_B[mV]	V_L[mV]	V_{C10p}[mV]	V_{C10p}[mV]
100	770	600	800	400	600	600

The capacitors in the temperature sensor are realized with MOSCAP as poly capacitors are not available in the technology used. The capacitance of an MOS device is calculated as the gate oxide capacitance in series with the depletion layer capacitance. For accumulation conditions, only the oxide capacitance is considered. In depletion, the total capacitance decreases as the depletion layer width, x_d, increases with the gate voltage. Capacitances for MOSCAP realized with n and p–channel devices are summarized in Table VIII for different bias conditions.

Table VIII. n-MOSCAP and p-MOSCAP capacitance under different bias conditions

C_{MOSCAP}	n-MOSCAP Condition	p-MOSCAP Condition
$A_{gate} \times C_{ox}$	$V_G < V_{FB}$	$V_G > V_{FB}$
$A_{gate} \times [1/\,(1/C_{ox} + x_d/\varepsilon_s)]$	$V_{FB} < V_G < V_S + V_T$	$V_{FB} > V_G > V_S + V_T$
$A_{gate} \times C_{ox}$	$V_G > V_S + V_T$	$V_G < V_S + V_T$

Capacitor C_L is realized with an n-MOSCAP with gate area $1223\mu m^2$ and the

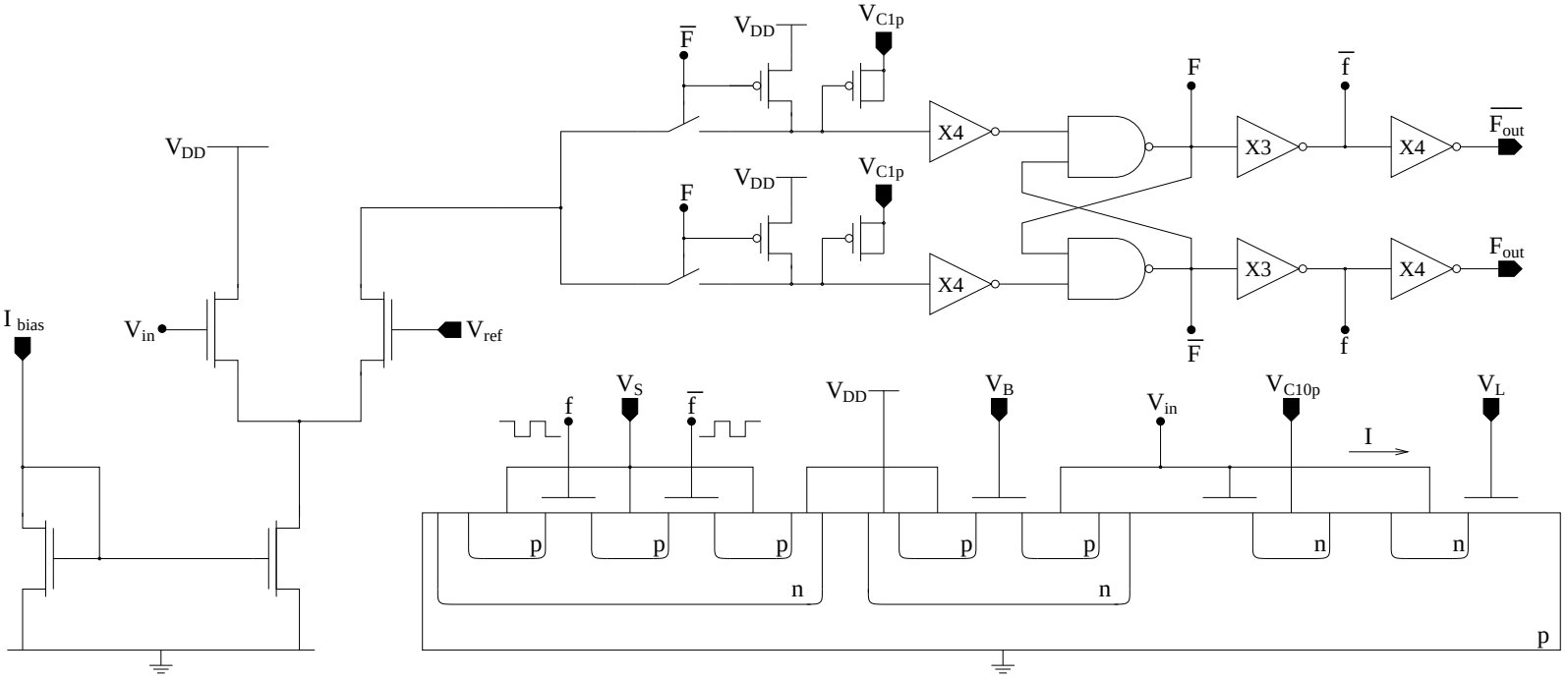


Fig. 28. Temperature sensor schematic

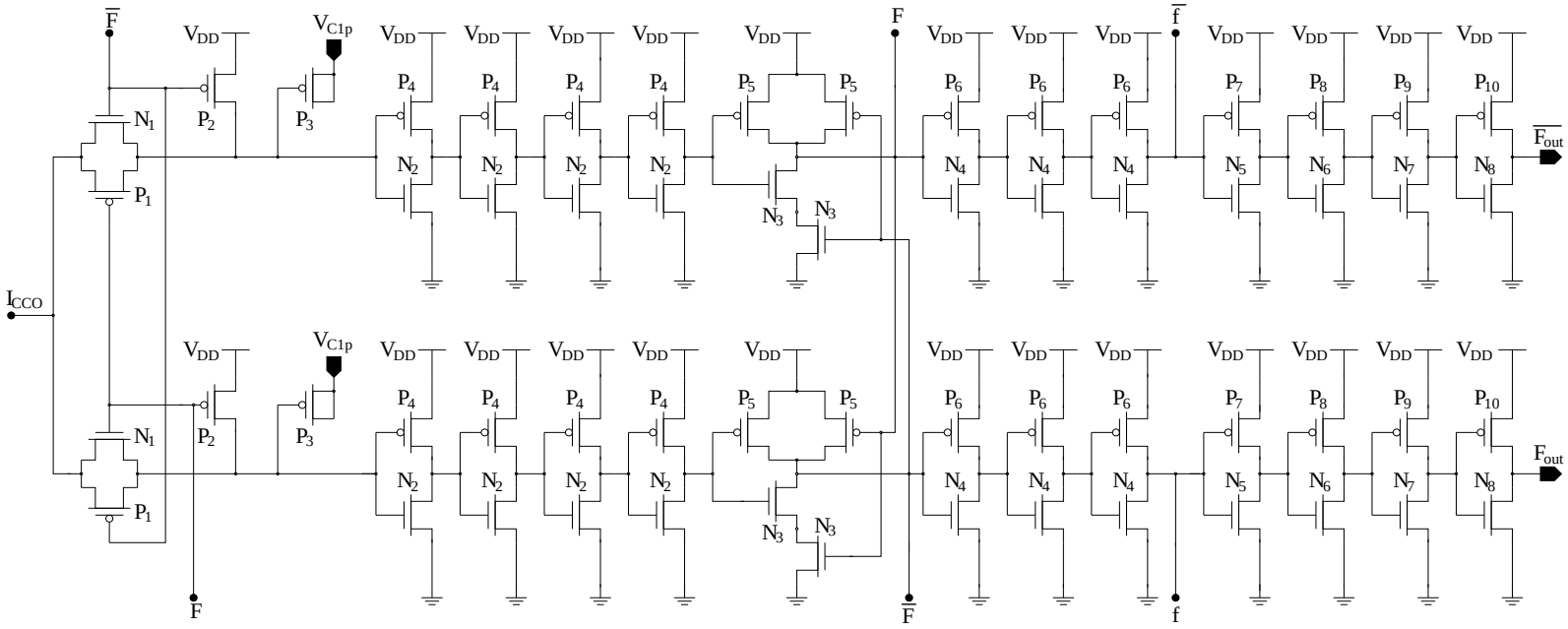


Fig. 29. Schematic of current controlled oscillator and output buffers

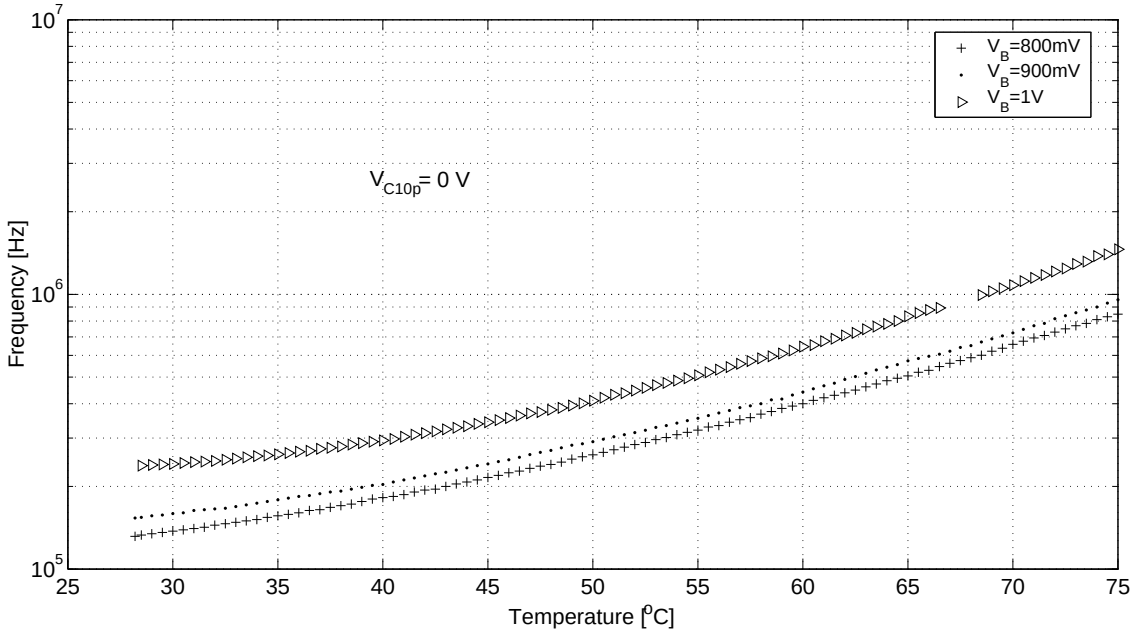
capacitors of the CCO are realized with p-MOSCAP with $A_{gate} = 120\mu\text{m}^2$. Maximum capacitance values for C_L and C_{CCO} are 10.3pF and 1pF, under inversion and accumulation conditions, respectively.

Note from Table VII that n-MOSCAP C_L is operated under depletion conditions and, therefore, its capacitance is less than $A_{gate} \times C_{ox}$, i.e. 10.3pF. V_{GS} is decreased in order to minimize tunnelling currents. Both gate–to–source and gate–to–channel tunnelling currents increase with V_{GS}, and especially for high electron concentration at the surface, gate–to–channel leakage becomes significant. Total tunnelling current I_T is not negligible under inversion conditions, given the device dimensions.

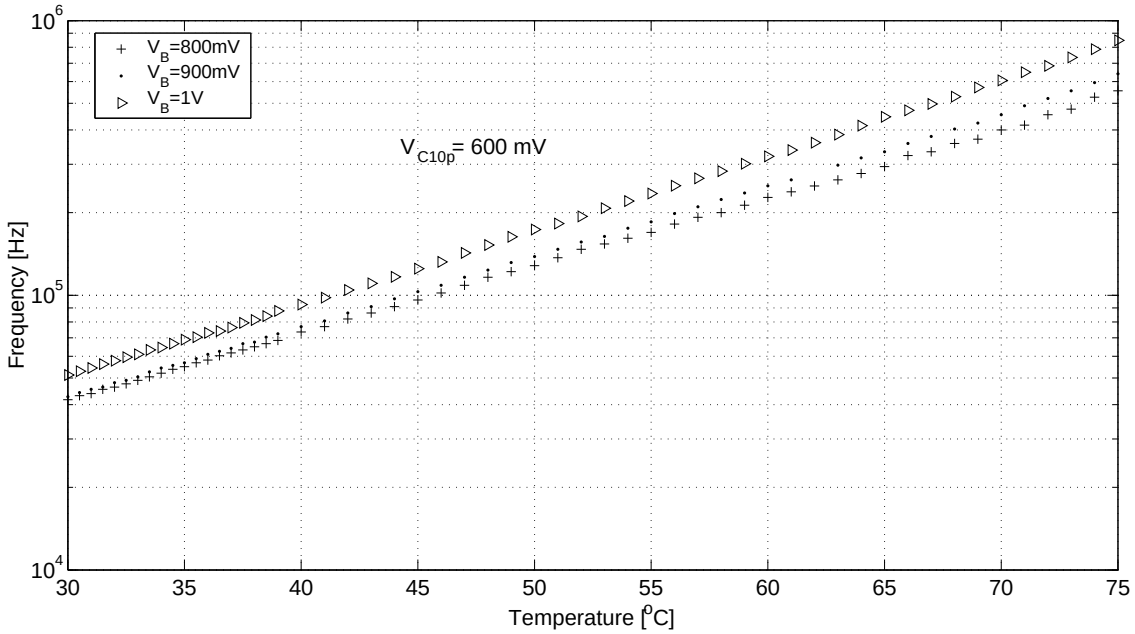
The output frequency variation with temperature is depicted in Fig. 30 (a) and (b) for V_{C10p} fixed at 0V and 600mV, respectively. The output frequency is not only higher in the whole temperature range but also less sensitive to temperature for $V_{C10p} = 0\text{V}$. Under inversion conditions, i.e. $V_{C10p} = 0\text{V}$, I_T adds to the error current and causes more increase in output frequency especially at low I_L values. For $V_{C10p} = 600\text{mV}$, both tunnelling currents are minimized as V_{GS} is reduced, and depletion prevails.

1. Output Characteristics

The output frequency variation with temperature is plotted in Fig. 31. A temperature oven was used for the measurements. The measured temperature range is 27^oC–110^oC. The frequency changes more than two decades for this range. The sensor has not yet been characterized at lower or higher temperatures. Note from Fig. 31 that V_B can be adjusted to change the output frequency range to some extent. The increase in frequency with V_B is due to the decrease in the output current of the ITCP current source.



(a)



(b)

Fig. 30. Effect of MOSCAP tunnelling current on sensor output characteristics for (a) V_{C10p}=0V and (b) V_{C10p}=600mV

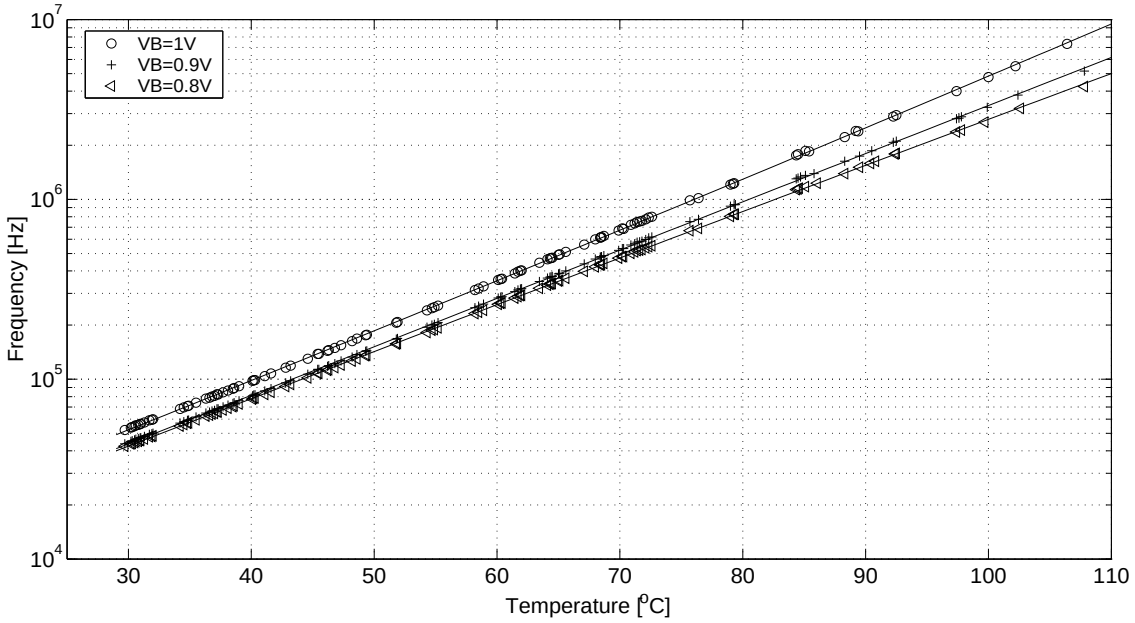


Fig. 31. Output characteristics of the temperature sensor

The temperature coefficient $\mathrm{TC_F}$ of the sensor output frequency is defined as:

$$\mathrm{TC_F} \doteq \frac{\mathrm{d}F_{out}}{F_{out}\,\mathrm{d}T}. \tag{5.6}$$

$\mathrm{TC_F}$ for the frequency curves of Fig. 31 is plotted in Fig. 32. $\mathrm{TC_F}$ plots differ with V_B bias as the temperature coefficient of the ITCP current source output depends on V_W. The temperature coefficient increases with temperature for $V_B = 1$V and decreases for $V_B = 800$mV and $V_B = 900$mV. It changes between 6.3%/^{o}C and 6.7%/^{o}C for $V_B = 1$V and between 6.1%/^{o}C and 5.85%/^{o}C for $V_B = 800$mV for the given temperature range. $\mathrm{TC_S}$ is less sensitive to temperature for $V_B = 900$mV and changes only 0.07%/^{o}C between 30^{o}C–110^{o}C. The sensor transfer characteristics show high linearity, and the linearity can be improved further through the bias voltage V_B.

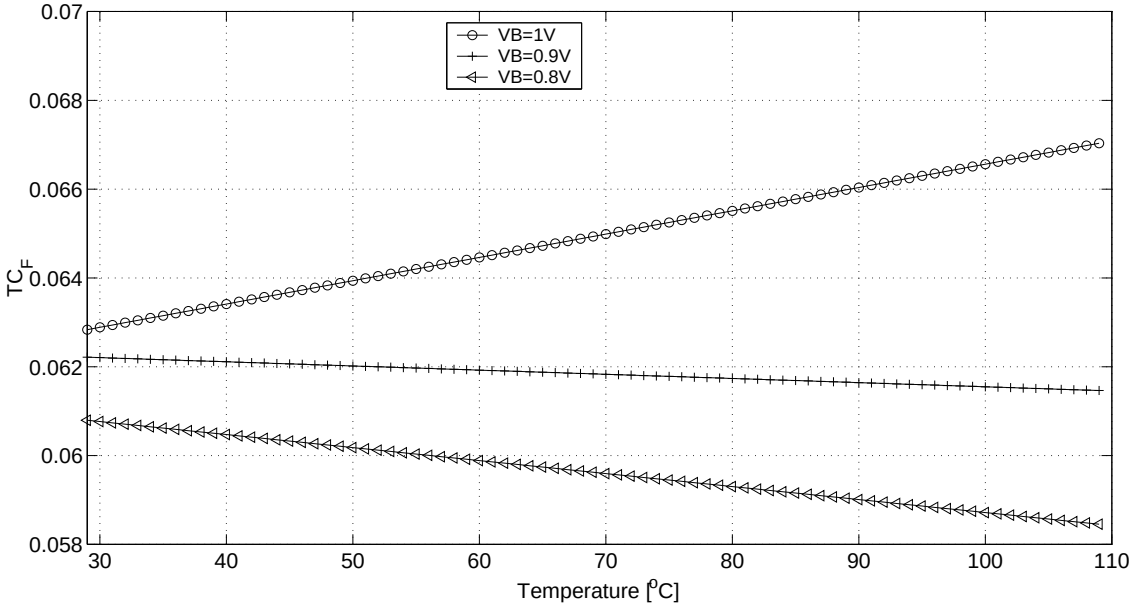
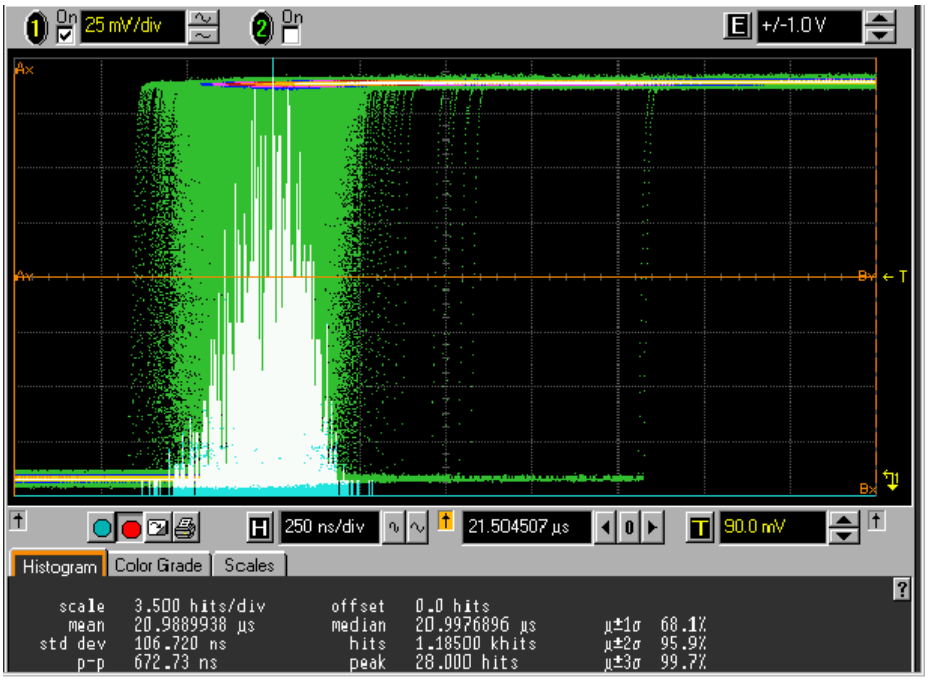


Fig. 32. Temperature coefficient of the temperature sensor

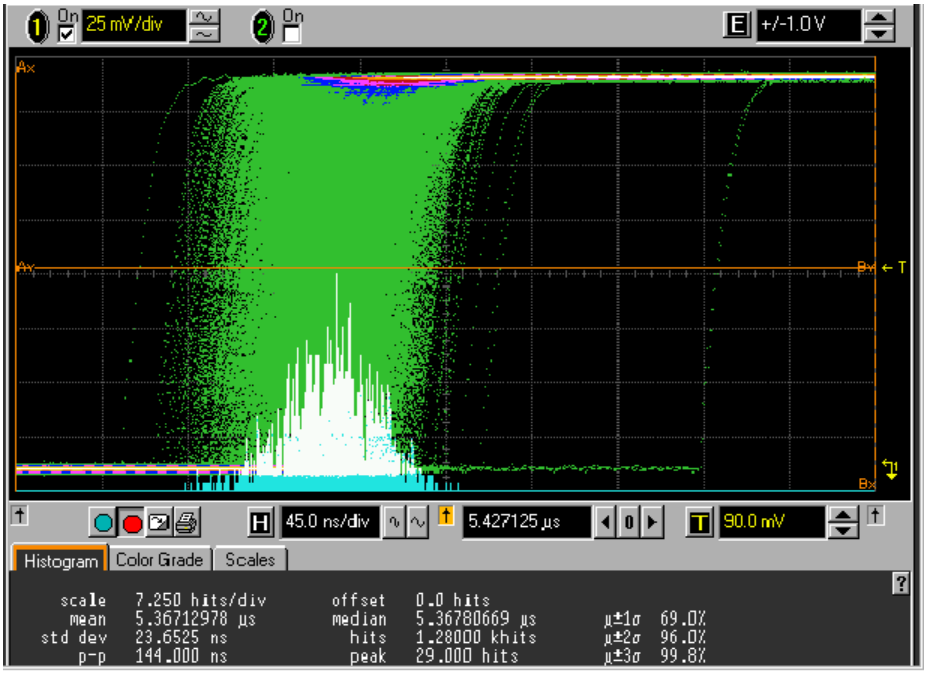
2. Jitter Distribution

The timing jitter at falling and rising edges of the sensor output is measured for V_B =[800mV,900mV,1V] at $T = 27^oC$ and $T = 50^oC$. Oscilloscope screen shots for jitter distribution at these temperatures for V_B = 800mV are given in Fig. 33 (a) and (b). Jitter has gaussian distribution; however, slight left skew is observed.

The timing jitter and skew mainly originate from the CCO. Skew arises from timing errors in the switching of S_1 and S_2. The timing jitter is attributed to the noise voltage at the inverter input of the CCO being amplified around the switching threshold and randomly modulating the switching time. Therefore, the timing jitter is determined by the noise voltage at the inverter input and the slew rate of the first inverter. The noise is mainly induced by switching and power supply. The noise current integrated by C_{CCO} also has some effect on the input voltage noise.



(a)



(b)

Fig. 33. Timing jitter for V_B=0.8V at (a) $T = 27^o$C and (b) $T = 50^o$C

The mean, standard deviation, and median values of the output signal period are summarized in Table IX for all the measurements. The number of samples used for each measurement is also indicated. Period values from each measurement is converted to frequency to obtain the corresponding mean and standard deviation in the output signal frequency. The results are summarized Table X. Note that the standard deviation is within 0.5% of the mean frequency.

Table IX. Variations in sensor output signal period

V_B [V]	Trans.	T [^{o}C]	μ [μsec]	σ [nsec]	median [μsec]	σ/μ%	Hits
0.8	rising	27.2	20.989	106.77	20.998	0.5087	1185
0.8	falling	27.2	20.961	108.73	20.966	0.5187	1189
0.8	rising	50.5	5.3671	23.662	5.3682	0.4409	1280
0.8	falling	50.35	5.448	24.014	5.45	0.4408	1334
0.9	rising	27.2	20.101	101.78	20.106	0.5063	1132
0.9	falling	27.2	20.099	105.56	20.102	0.5252	1199
0.9	rising	50.9	4.9511	21.855	4.9527	0.4414	1208
0.9	falling	50.75	4.993	21.018	4.9938	0.4210	1271
1	rising	27.2	16.37	83.421	16.375	0.5096	1233
1	falling	27.2	16.372	81.041	16.379	0.4950	1194
1	rising	50.6	3.961	17.926	3.9619	0.4526	1220
1	falling	50.9	3.902	16.462	3.9025	0.4219	1118

Table X. Variations in sensor output signal frequency

V_B [V]	Trans.	T [^{o}C]	μ [kHz]	σ [Hz]	median [kHz]	σ/μ%	Hits
0.8	rising	27.2	47.645	242.782	47.624	0.5096	1185
0.8	falling	27.2	47.708	247.611	47.697	0.5190	1189
0.8	rising	50.5	186.323	822.365	186.28	0.4414	1280
0.8	falling	50.35	183.557	810.013	183.49	0.4413	1334
0.9	rising	27.2	49.751	252.246	49.736	0.5070	1132
0.9	falling	27.2	49.755	260.433	49.747	0.5234	1199
0.9	rising	50.9	201.980	893.270	201.91	0.4423	1208
0.9	falling	50.75	200.282	843.451	200.25	0.4211	1271
1	rising	27.2	61.089	311.679	61.069	0.5102	1233
1	falling	27.2	61.080	302.875	61.052	0.4959	1194
1	rising	50.6	252.468	1143.739	252.40	0.4530	1220
1	falling	50.9	256.284	1082.398	256.24	0.4223	1118

3. Prototype Temperature Sensor Performance

a. Area

The layout of the prototype temperature sensor is illustrated in Fig. 34. The areas of individual blocks are indicated in the figure. The area of each block is calculated from the dimensions of the guard ring surrounding the block and all the necessary routing is included. Output buffers are excluded from area calculations. The total area of the prototype sensor is $5236\mu m^2$.

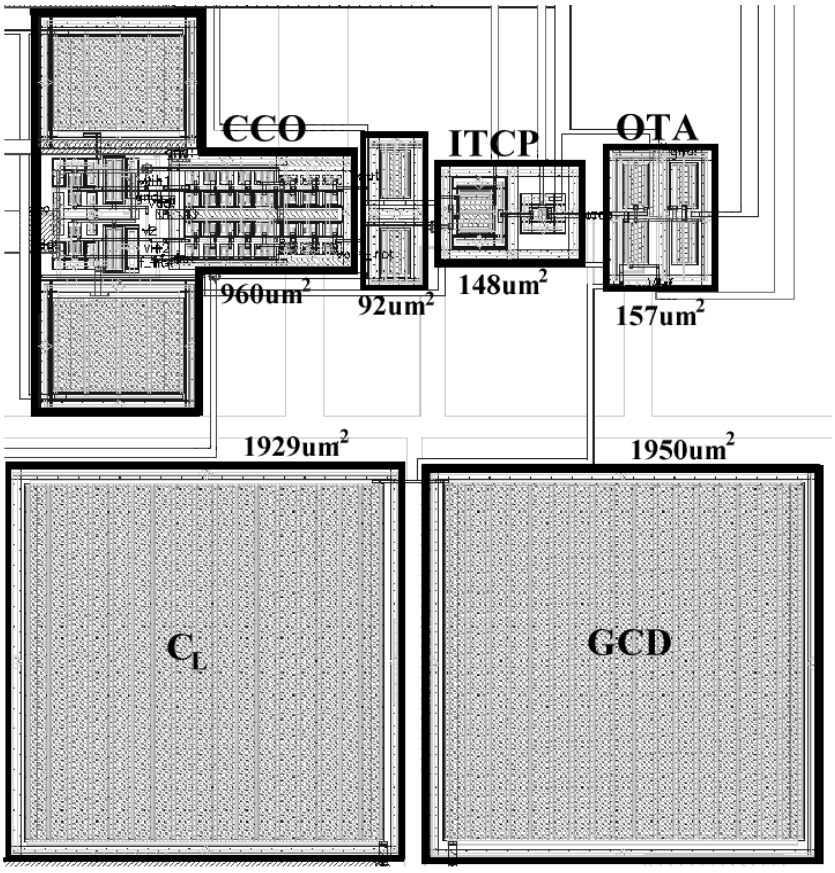


Fig. 34. Temperature sensor layout

The temperature sensing is realized with the GCD and the ITCP current source.

For multiple sensor integration, placing only these two devices at different locations over the die and using one control unit consisting of a C_L, an OTA, and a CCO to periodically read the error current I_e would suffice. Therefore, for n number of sensors integrated in a chip, the total area is $n \times 2190\mu\text{m}^2 + 3050\mu\text{m}^2$.

b. Power

The static power consumption of the sensor is simulated to be around 190μW and it is mainly due to the OTA which has a bias current of 100μA. Transient currents during the switching of the CCO also cause dynamic power consumption which increases with frequency. The average power consumption at 8MHz is obtained as 400μW.

c. Calibration

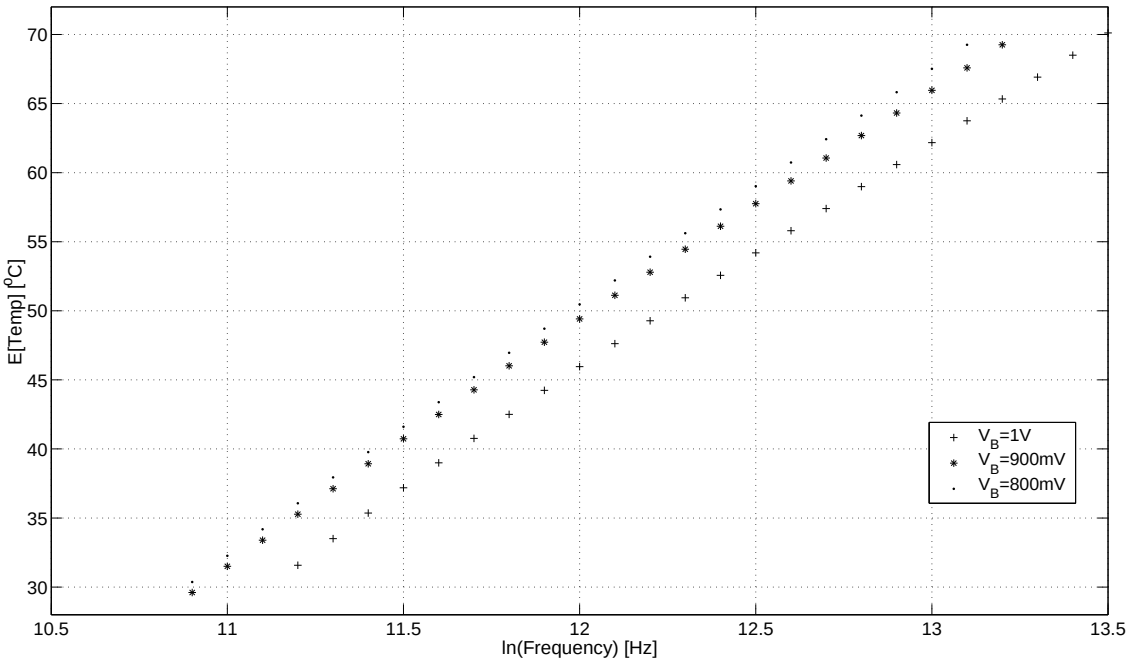
Batch calibration data for the prototype temperature sensor is obtained by measuring the output characteristics of 10 sensors from different chips. Output frequency measurements were conducted for the temperature range of 30^{o}C–70^{o}C with V_B =[800mV,900mV,1V]. Calibration lines obtained are:

$$\ln(\text{Freq}) = 0.0569 \cdot \text{Temp} + 9.1435 \quad \text{for } V_B = 0.8\text{V}, \tag{5.7}$$

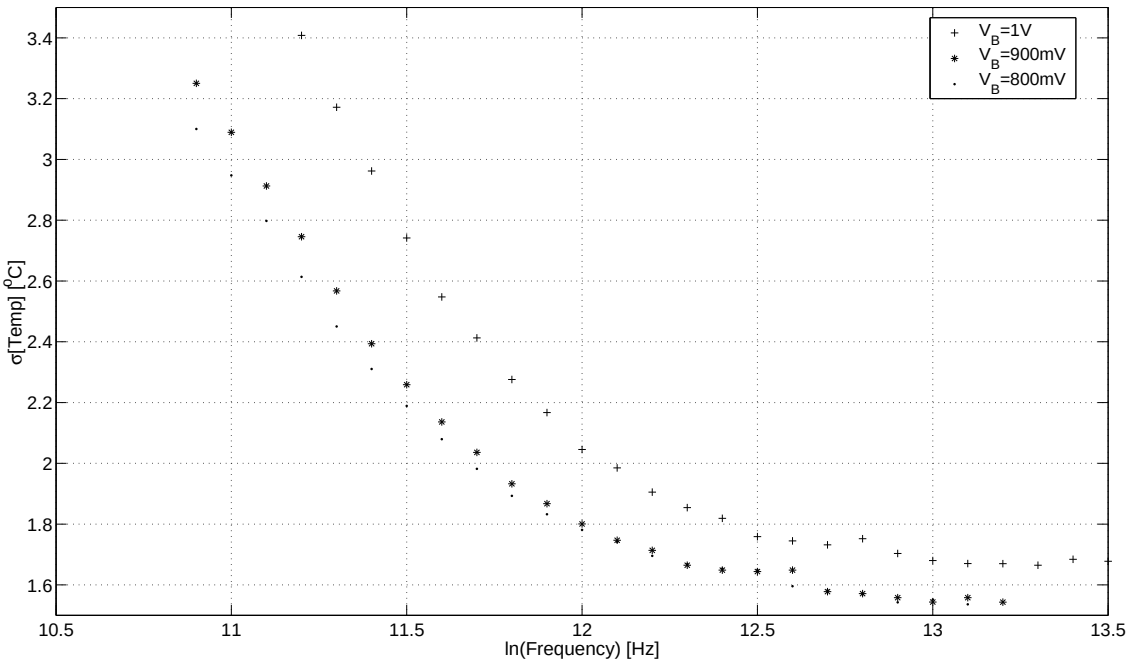
$$\ln(\text{Freq}) = 0.0584 \cdot \text{Temp} + 9.1339 \quad \text{for } V_B = 0.9\text{V}, \tag{5.8}$$

$$\ln(\text{Freq}) = 0.0602 \cdot \text{Temp} + 9.2540 \quad \text{for } V_B = 1\text{V}. \tag{5.9}$$

The expected temperature readings and the standard deviation are plotted in Fig. 35 (a) and (b), respectively. Note that the standard deviation decreases exponentially with increasing temperature. Standard deviation of $\pm 3.1^o$C at 30^{o}C and $\pm 1.5^o$C at 70^{o}C is achieved with the batch calibration line (5.7). Deviation from linearity at low



(a)



(b)

Fig. 35. (a) Expected value and (b) standard deviation (1σ) of the sensor temperature readings with batch calibration

temperatures is not an issue for thermal management applications.

d. Sensitivity

The frequency–temperature relation is exponential, as the sensor output is proportional to I_L, which changes with n_i. Therefore, its sensitivity, defined as the slope of the output characteristics, increases exponentially with temperature. TC_s, defined previously, shows the deviation from this exponential behavior. It is a more important parameter for the characterization of this sensor as it indicates how linear the output is. The sensitivity of the sensor is plotted in Fig. 36. It increases from 3×10^3Hz/^{o}C to 6×10^6Hz/^{o}C within the temperature range of 30^{o}C–110^{o}C. Even though the sensitivity is very high, the sensor resolution is limited by the jitter in the output signal.

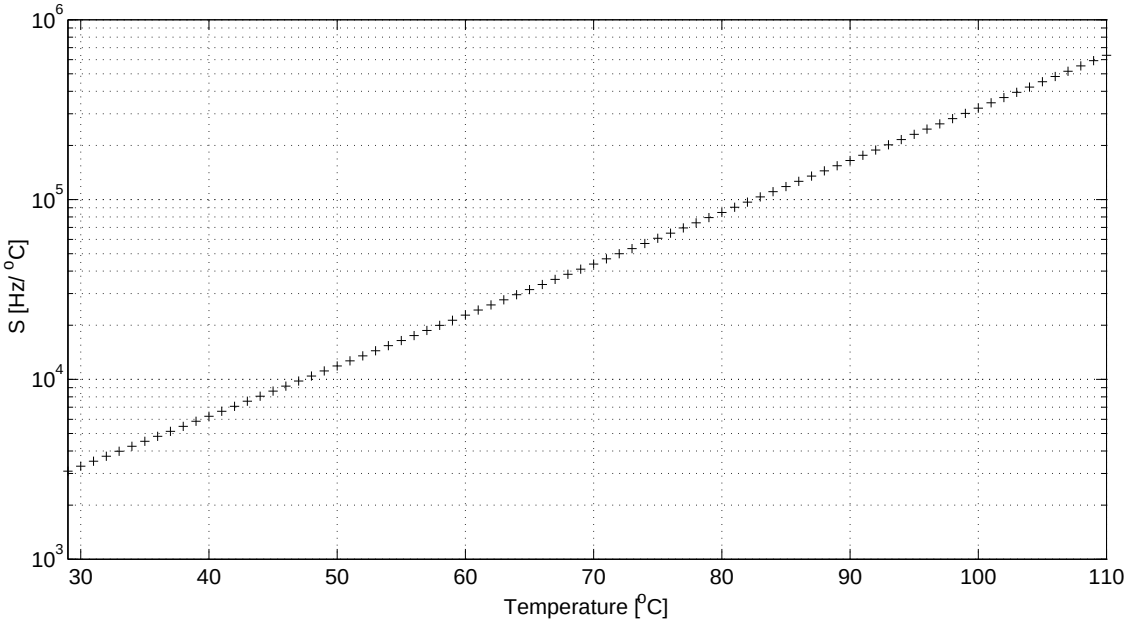


Fig. 36. Sensitivity of the temperature sensor

e. Resolution

Resolution is defined as the minimum detectable input signal that produces a change in the output. It is determined by the noise to sensitivity ratio of the temperature sensor. The resolution in this temperature sensor is limited by the jitter and the resulting standard deviation in the output frequency. Therefore, resolution can be expressed as:

$$R \doteq \frac{\sigma}{S} = \frac{\sigma/f}{1/f \cdot \mathrm{df/dT}} = \frac{\sigma/f}{\mathrm{TC_F}}. \tag{5.10}$$

Resolution is calculated using σ/f and $\mathrm{TC_F}$ values from Table X and Fig. 32, respectively. The values obtained for V_B =[800mV,900mV,1V] at $T = 27^o$C and $T = 50^o$C are summarized in Table XI. The resolution is around 0.085^oC at room temperature and it increases to 0.074^oC at $T = 50^o$C. It improves with temperature as sensitivity increases more than noise with temperature.

Table XI. Temperature sensor resolution

Resolution [^{o}C]	V_B =800 mV	V_B =900mV	V_B =1V
$T = 27^o$C	0.085	0.084	0.081
$T = 50^o$C	0.074	0.071	0.071

CHAPTER VI

SUMMARY AND CONCLUSIONS

A novel temperature sensor with an interface–trap charge pumping current source has been presented. It has linear output characteristics, high sensitivity, and high resolution. Its small area and low power consumption make it ideal for microprocessor thermal management applications. Its digital output also minimizes the cost and area for interfacing. Performance parameters of the prototype temperature sensor are summarized in Table XII. Please refer to Table I for performance comparison with three other temperature sensors proposed for thermal management applications.

The proposed sensor comprises a *sensing unit*, consisting of a gate–controlled diode and an ITCP current source, and a *control unit*, consisting of a C_L, an OTA, and a CCO, placed in a feedback loop. The prototype sensor is realized in TSMC 0.18μm technology with an area of $5236\mu\text{m}^2$ and static power consumption of 190μW. The sensor architecture enables integration of n number of sensors on-chip with a total area of $n \times 2190\mu\text{m}^2 + 3050\mu\text{m}^2$ if a single *control unit* is used.

The temperature sensor exhibits highly linear output characteristics for the temperature range of 27^oC-120^oC. Maximum and minimum operating temperatures are not yet tested. Accuracy of $\pm 3^o$C is obtained at $T = 30^o$C with batch calibration. However, the accuracy improves with temperature and it is $\pm 1.5^o$C at $T = 70^o$C. As the temperature dependence of generation current is exploited, very high sensitivity is obtained. The resolution is 0.085^oC, and it can be increased by improving the design of the current–controlled oscillator to minimize the jitter. Averaging can also be used to increase the resolution.

The sensor can be implemented in any CMOS technology. The main constraint is set by tunnelling currents which become more significant with thinner gate oxides.

Table XII. Summary of prototype temperature sensor performance

Technology	TSMC 0.18μm
Area [mm^2]	0.0052
Range [^oC]	27–120
Power [μW]	190
Resolution [^{o}C]	0.085 at 27^{o}C – 0.074 at 50^{o}C
Accuracy [^{o}C]	$\pm$3.5 at 30^{o}C – $\pm$1.5 at 70^{o}C
Sensitivity [Hz/^{o}C]	3×10^3 at 30^{o}C – 6×10^6 at 110^{o}C

The gate–controlled diode is especially susceptible to these currents. Therefore, special care must be taken to implement this temperature sensor in technologies with thinner gate oxides.

The ITCP current source is affected by N_{it} variations, but this is not an important drawback for the temperature sensor application. The variation of N_{it} causes shift in the output frequency range and limits the accuracy. However, accuracy can be improved with calibration if necessary.

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