DESIGN OF A 3.1-4.8 GHZ RF FRONT-END FOR AN ULTRA WIDEBAND RECEIVER

A Thesis

by

PUSHKAR SHARMA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

May 2005

Major Subject: Electrical Engineering

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Approved as to style and content by:

Aydin Ilker Karsilayan (Chair of Committee)	Jose Silva-Martinez (Member)
Chanan Singh (Member)	Alexander Parlos (Member)
Chanan Singh (Head of Department)	

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ABSTRACT

Design of a 3.1-4.8 GHz RF Front-end for an Ultra Wideband Receiver. (May 2005)
Pushkar Sharma, B.E. (Hons.), Panjab University, India
Chair of Advisory Committee: Dr. Aydin I. Karsilayan

IEEE 802.15 High Rate Alternative PHY task group (TG3a) is working to define a protocol for Wireless Personal Area Networks (WPANs) which makes it possible to attain data rates of greater than 110Mbps. Ultra Wideband (UWB) technology utilizing frequency band of 3.168 GHz – 10.6 GHz is an emerging solution to this with data rates of 110, 200 and 480 Mbps. Initially, UWB mode I devices using only 3.168 GHz – 4.752 GHz have been proposed.

Low Noise Amplifier (LNA) and I-Q mixers are key components constituting the RF front-end. Performance of these blocks is very critical to the overall performance of the receiver. In general, main considerations for the LNA are low noise, 50Ω broadband input matching, high gain with maximum flatness and good linearity. For the mixers, it is essential to attain low flicker noise performance coupled with good conversion gain. Proposed LNA architecture is a derivative of inductive source degenerated topology. Broadband matching at the LNA output is achieved using LC band-pass filter. To obtain high gain with maximum flatness, an LC band-pass filter is used at its output. Proposed LNA achieved a gain of 15dB, noise figure of less than 2.6dB and IIP3 of more than -7dBm.

Mixer is a modified version of double balanced Gilbert cell topology where both I and Q channel mixers are merged together. Frequency response of each sub-band is matched by using an additional inductor, which further improves the noise figure and conversion gain. Current bleeding scheme is used to further reduce the low frequency noise. Mixer achieves average conversion gain of 14.5dB, IIP3 more than 6dBm and Double Side Band (DSB) noise figure less than 9dB. Maximum variation in conversion gain is desired to be less than 1dB. Both LNA and mixers are designed to be fabricated in TSMC 0.18μm CMOS technology.

To my country, INDIA

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CHAPTER I
INTRODUCTION

With the advancement of technology, there has been a spurt in the growth of compact portable devices. These devices are divided into three main segments as Consumer Electronics (CE), Personal Computer (PC) and mobile applications as shown in Fig. 1.1. These devices communicate with each other transferring large amount of data including audio and video.

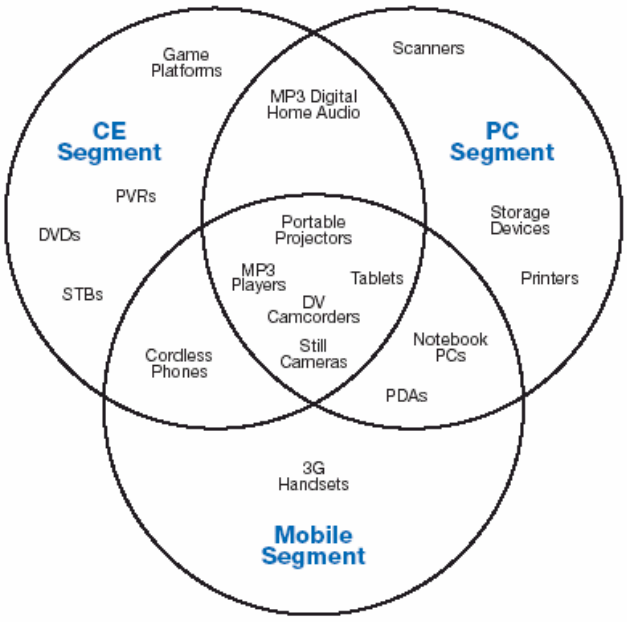

Fig. 1.1 Different segments of portable devices

With growing demand of mobility and portability, there has been a drive to eliminate bulky cables especially when many such devices are interconnected. This demands high-bandwidth short-range Wireless Personal Area Network (WPAN). Peak data rate of 1Mbps in Bluetooth technology is not enough for this purpose whereas Wi-Fi standards (IEEE 802.11(b,g)) do not meet the cost and power requirements for many

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This thesis follows the style and format of *IEEE Journal of Solid-State Circuits.*

CE devices.

1.1 Ultra Wideband (UWB) Wireless Standard

UWB is emerging as a solution for the IEEE 802.15.3a (TG3a) standard [1]. The motivation behind this standard is to provide specifications for a low complexity, low-cost, low power consumption and high data-rate wireless connectivity among devices entering the personal operating space. In February 2002, Federal Communications Commission (FCC) allocated 7.5GHz wide unlicensed band from 3.1 to 10.6 GHz for the purpose of UWB. It defines UWB signal as any signal whose bandwidth is higher than 500MHz in 3.1-10.6GHz band which follows the spectrum mask of Fig. 1.2.

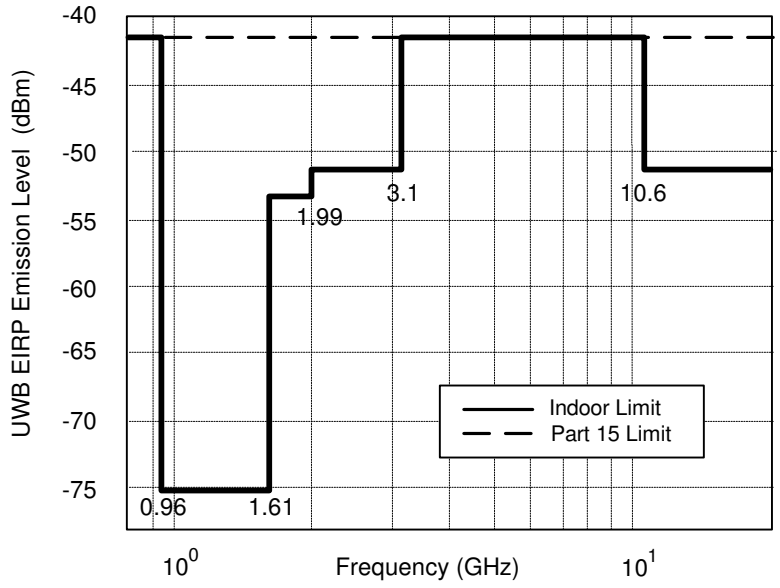


Fig. 1.2 FCC spectrum mask for UWB

High data rates attainable in UWB can be explained from the Shannon channel capacity theorem according to which, the information carrying capacity C of a channel is given by

$$C = B\log_2\left(1+\frac{SNR}{B}\right) \tag{1.1}$$

where B is the bandwidth in hertz and SNR is the signal to noise ratio. Hence with high bandwidth high data rates are attainable. The mandatory data rates of 110, 200 and 480 Mbps are required for operation up to 30ft of range. As a result of spectral power limit of -41 dBm, the required power levels are small. This means that UWB channels can co-exist with other standards in the same frequency band. Small spectral power levels also lower the transceiver power consumption. One of the two main approaches for UWB realization is a Multi-band OFDM which is spearheaded by Texas Instruments (TI). In the TI proposal [2], the whole UWB band is subdivided into multiple 528MHz widebands. For the first phase only 3.168-4.752GHz bandwidth is proposed to be used as shown in Fig. 1.3. Main advantages of using Multi-band OFDM are its exceptional spectral efficiency, resistance to RF interference and multi-path energy capture. Multi-band OFDM also offers inherent robustness vs. narrowband interference. This means a narrowband interferer at most will affect few of 128 OFDM sub-carriers, such that even if information is lost from the affected sub-carriers, it can be retrieved through error correction codes and interleaving.

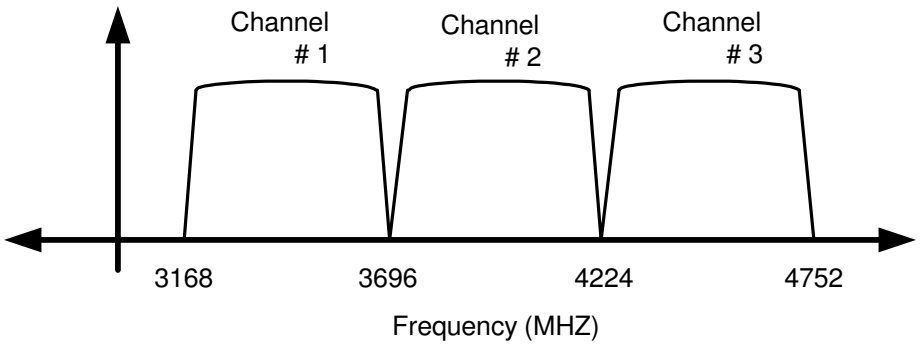


Fig. 1.3 Frequency spectrum used for UWB mode I devices

1.2 Ultra Wideband Receiver

A prototype of an Ultra Wideband receiver of which this thesis is a sub-part of, is shown in Fig. 1.4. The input signal is received from a wideband antenna and fed to an off-chip pre-select filter. The purpose of this filter is to attenuate out-of-band interferesto

avoid its modulation and intermodulation products to appear in-band and to avoid saturation in the RF front-end. Next block in the receiver chain is a $1:\sqrt{2}$ off-chip balun. The balun provides 50Ω matching to the pre-select filter and differential 100Ω matching to the on-chip RF front-end. The RF front-end for this receiver is the main objective for this thesis. It comprises of a differential Low Noise Amplifier (LNA) and I-Q mixers. The LNA is required to provide high gain to the input signal with minimum signal to noise ratio degradation (low noise figure). Further it needs wideband 100Ω input match to the balun. Being direct conversion architecture, the LNA output is directly connected to the I-Q mixers without a need for 50Ω matching. I-Q mixers are used to down convert high frequency RF signal to low frequency quadrature I and Q channel IF signal. The required quadrature LO frequencies are at 3.432, 3.96 and 4.488GHz which are generated by the frequency synthesizer.

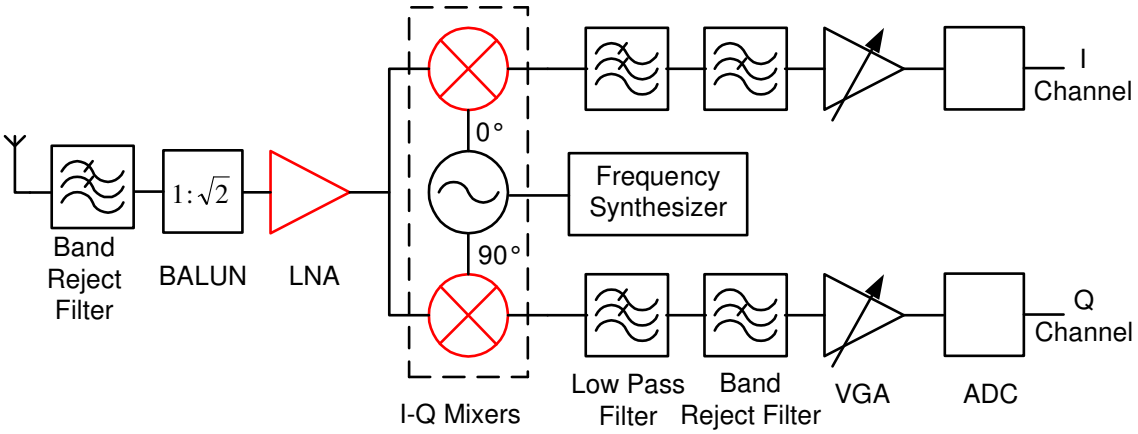


Fig. 1.4 A UWB receiver prototype

For each channel, the IF signal goes through low-pass filter to attenuate high order products of the mixer. Next, a tunable band-reject filter is used to attenuate in-band interference to avoid saturation in the base-band. Variable Gain Amplifier (VGA) conditions the amplitude of the input signal such that the ADC input is not saturated for

higher input received power levels. ADC digitizes the signal which is further processed by the DSP.

1.3 Specifications

The core of this thesis is the design of RF front-end for the UWB receiver as discussed before. The specifications for the LNA and I-Q mixers as tabulated in Tables 1.1 and 1.2 are derived from the overall system requirements.

Table 1.1 LNA Specifications

Parameter	**Specification**
S11	<-10
Gain – S21 (dB)	15/0
Max Gain Variation (dB)	1
Frequency range (GHz)	3.168-4.752
Noise Figure (dB)	<3.44
IIP3 (dBm)	>-7

.

Table 1.2 Mixer Specifications

Parameter	**Specification**
Conversion Gain (dB)	10
Maximum gain variation (dB)	1
RF Frequency range (GHz)	3.168-4.752
LO Frequencies (GHz)	3.432, 3.96, 4.488
Noise Figure (dB)	<9.3
IIP3 (dBm)	>-7

1.4 Organization of the Thesis

The thesis is organized into six chapters including the introduction. Chapter II deals with the basics of a low noise amplifier, its metrics and some popular LNA topologies with their comparison. Building upon these basics, chapter III discusses various aspects of proposed LNA architecture with simulation results. Chapter IV gives an overview of mixers in general, mixer metrics and various topologies. UWB mixers, its design, noise and linearity analysis, layout issues and simulation results are discussed in Chapter V. Chapter VI concludes the thesis and improvements are suggested for future work.

CHAPTER II
LOW NOISE AMPLIFIER

The sensitivity of a typical receiver is very low (of the order of -80dBm). At the very input of the receiver, signal to noise ratio of such a small signal level get degraded even by relatively insignificant noise sources. Hence, the initial blocks in a receiver chain need to have very small noise contribution (measured in terms of noise factor F as explained later). Further, these blocks should have high gain as well. This is done to increase the signal amplitude such that further signal to noise degradation in the receiver chain is minimal. Precisely for these two reasons, all receivers employ a Low Noise Amplifier (LNA). Mathematically, the significance of the noise factor and gain for the LNA is evident from the Friis equation as given by

$$F_{total} = F_{LNA} + \frac{F_{after} - 1}{G_{LNA}} \tag{2.1}$$

It can be seen from the above equation that the noise factor of the LNA directly adds to the overall noise factor of the receiver. Also, noise factor contribution of rest of the receiver is divided by the gain of the LNA. Hence, by reducing the noise factor and increasing the gain of the LNA, overall noise factor of the receiver is reduced.

2.1 Two Port S-Parameters

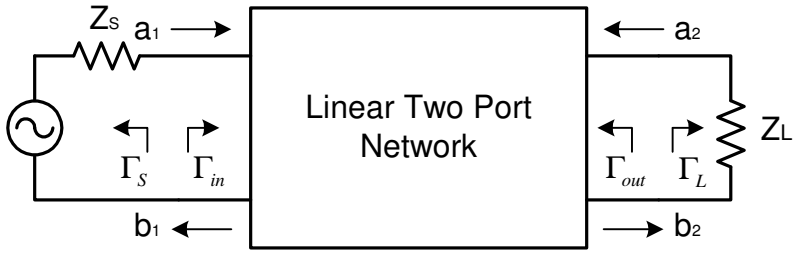


Fig. 2.1 Two port network showing incident and reflected waves

S-parameters are often used in microwave and RF circuits to characterize a multi-port linear network. For a linear two port network as shown in Fig. 2.1, the incident waves (a_1,a_2) and reflected waves (b_1,b_2) can be expressed as

$$b_1 = S_{11}a_1 + S_{12}a_2 \tag{2.2}$$

$$b_2 = S_{21}a_1 + S_{22}a_2 \tag{2.3}$$

where S11, S12,S21,S22 are the S-parameters for a two port network which can be defined as

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a2=0} \tag{2.4}$$

$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a1=0} \tag{2.5}$$

$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a2=0} \tag{2.6}$$

$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a1=0} \tag{2.7}$$

Port voltages V_1 and V_2 and port currents I_1 and I_2 can be expressed in terms of the incident and the reflected waves a_1, a_2, b_1 and b_2 as

$$a_1 = \frac{V_1 + I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{i1}}{\sqrt{Z_0}} \tag{2.8}$$

$$a_2 = \frac{V_2 + I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{i2}}{\sqrt{Z_0}} \tag{2.9}$$

$$b_1 = \frac{V_1 - I_1 Z_0}{2\sqrt{Z_0}} = \frac{V_{r1}}{\sqrt{Z_0}} \tag{2.10}$$

$$b_2 = \frac{V_2 - I_2 Z_0}{2\sqrt{Z_0}} = \frac{V_{r2}}{\sqrt{Z_0}} \tag{2.11}$$

where V_{i1},V_{r1} and V_{i2},V_{r2} are the incident and reflected voltage waves at port 1 and 2 respectively.

In general, $|a|^2$ and $|b|^2$ at any port represent the incident and the reflected power. Hence s-parameters can be written intuitively as

$$S_{11} = \frac{Power\ reflected\ from\ network\ input}{Power\ incident\ on\ network\ input} \tag{2.12}$$

$$S_{22} = \frac{Power\ reflected\ from\ network\ output}{Power\ incident\ on\ network\ output} \tag{2.13}$$

$$S_{21} = \frac{Power\ delivered\ to\ the\ load\ Z_0}{Power\ available\ from\ the\ source\ Z_o} \tag{2.14}$$

$$S_{12} = \frac{reflected\ power\ delivered\ to\ the\ source\ Z_0}{Power\ incident\ on\ the\ network\ output} \tag{2.15}$$

2.1.1 Power Matching

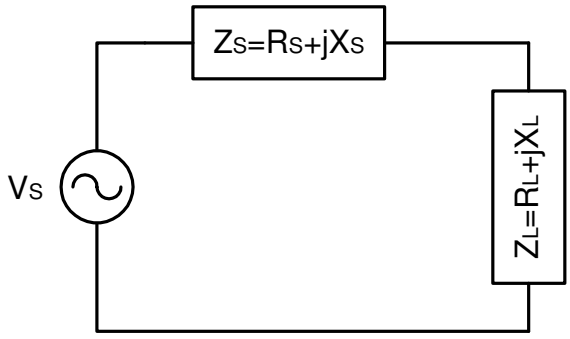


Fig. 2.2 Input port with complex source impedance terminated by a complex load

Let us consider an arrangement as shown in Fig. 2.2 where both source and load impedances are complex. It can be shown that the total power transferred to the load is

$$P_{delivered} = \frac{|V_S|^2 R_L}{(R_L + R_S)^2 + (X_L + X_S)^2} \tag{2.16}$$

To find out the condition for maximum power transfer, derivative of (2.16) with respect to R_L is made zero. Solving further leads to following conditions

$$R_L = R_S \tag{2.17}$$

$$X_L = -X_S \tag{2.18}$$

In other words, source and load impedance should be complex conjugate of each other. In general, the input and output reflection coefficient of a two port network of Fig. 2.1 can be defined as [3]

$$\Gamma_{in} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.19}$$

$$\Gamma_{out} = \frac{b_2}{a_2} = S_{22} + \frac{S_{12}S_{21}\Gamma_s}{1 - S_{11}\Gamma_s} \tag{2.20}$$

where Γ_S and Γ_L are the source and load reflection coefficients as given by

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{2.21}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.22}$$

Conditions for maximum power transfer at input and output can be expressed in terms of refection coefficients as

$$\Gamma_{in} = \Gamma_S^* \tag{2.23}$$

$$\Gamma_{out} = \Gamma_L^* \tag{2.24}$$

It can be seen that for unilateral case (S_{12}=0) or when source and load impedance equal characteristic impedance Z_0, input and output reflection coefficients simplify to S_{11} and S_{22} respectively. Hence metrics of maximum power transfer and impedance matching are S parameters S_{11} and S_{22}. Although S_{11} and S_{22} should ideally be zero, for practical purposes any value less than -10dB (0.1) is considered to be a reasonable figure.

2.1.2 Gain

There exist various definitions for gain in an RF amplifier for example transducer gain (G_T), power gain (G_P) and available power gain (G_A) which are defined as [3]

$$G_T = \frac{P_L}{P_{AVS}} = \frac{Power\ delivered\ to\ the\ load}{Power\ available\ from\ the\ source} \tag{2.25}$$

$$G_P = \frac{P_L}{P_{IN}} = \frac{Power\ delivered\ to\ the\ load}{Power\ input\ to\ the\ network} \tag{2.26}$$

$$G_A = \frac{P_{AVN}}{P_{AVS}} = \frac{Power\ available\ from\ the\ network}{Power\ available\ from\ the\ source} \tag{2.27}$$

For a unilateral case, transducer power gain can be expressed as [3]

$$G_{TU} = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2 \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2} = G_S|S_{21}|^2 G_L \tag{2.28}$$

where G_S and G_L are source and load mismatch factors. Maximum transducer gain is achieved for $\Gamma_S=S_{11}^*$ and $\Gamma_L=S_{22}^*$ and is given by

$$G_{TU,\max} = \frac{1}{1-|S_{11}|^2}|S_{21}|^2 \frac{1}{1-|S_{22}|^2} \tag{2.29}$$

For perfect impedance matching and source and load ends, $G_{TU,max}$ approaches $|S_{21}|^2$. Hence S21 is a metric for LNA gain.

2.2 MOSFET Noise Overview

2.2.1 Drain Current Noise

Due to the thermal fluctuations of channel charge, MOSFET under ON state produces thermal noise. Under saturation conditions this drain noise current is given as

$$\overline{i_{nd}^2} = 4kT\gamma g_{do}\Delta f \tag{2.30}$$

where g_{do} is the gds of the transistor when for zero drain source voltage. The parameter γ equals unity for zero Vds and roughly 2/3 for long channel mosfets. For short channel devices this values is typically between 2 and 3.

2.2.2 Gate Noise

Random fluctuations in the channel due to drain noise current induce small signal noise current fluctuations through the gate capacitance. This noise current is given by

$$\overline{i_{ng}^2} = 4kT\delta g_g \Delta f \tag{2.31}$$

where

$$g_g = \frac{\omega^2 C^2 gs}{5 g_{do}} \tag{2.32}$$

and δ is the gate noise coefficient which is typically equal to twice of drain noise coefficient γ. Being of the same origin as drain current noise, gate noise current is correlated to it by a factor *c*. For long channels, *c* is around j0.395 and for short channels it is around j0.5. Important behavior of induced gate noise is that it increases with frequency, making it one of the major concerns in high frequency design.

2.2.3 Flicker Noise

A low frequency noise is generated by the random capture and release of charge carriers by the interface traps at channel – gate oxide interface. Flicker noise can be modeled as a noise current source given by

$$\overline{i_{n,flic\,ker}^{\,2}} = \frac{K}{f} \frac{g_m^{\,2}}{WL\ Cox^2} \Delta f \tag{2.33}$$

where K is the flicker noise coefficient which is around 50 times smaller in PMOS than in NMOS. As it is seen from the above expression, flicker noise is inversely proportional to frequency hence also called as 1/f noise. A simplified noise model for a MOSFET taking all the above noise sources into account, is shown in Fig. 2.3

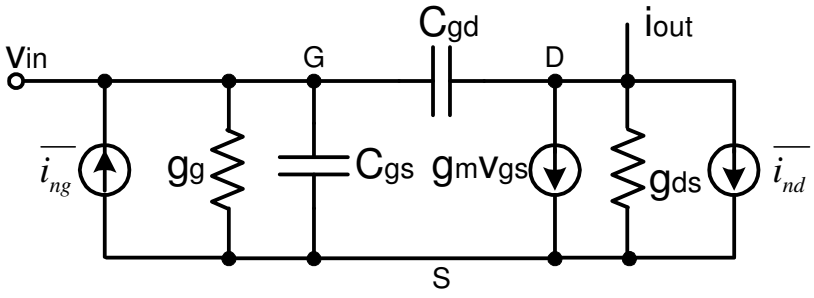


Fig. 2.3 Simplified noise model of a MOSFET

2.3 Noise Metrics

Noise of a system can be measured in two ways. One is absolute measurements where noise is measured as either input or output referred voltage spectral density (V^2/Hz). This type of measurements is usually done for baseband circuits where the input source is assumed to be noiseless. However, in RF system noise is measure relative to the noise of the input source. One such metric is the noise factor which is defined as

$$F = \frac{SNR\,at\,the\,input}{SNR\,at\,the\,output} \tag{2.34}$$

If input source has impedance Rs, then noise factor F can be expressed in terms of total input referred noise voltage spectral density of the system (v^2_n) and the noise contribution of Rs. So (2.34) can be rewritten as

$$F = 1 + \frac{v_n^{\,2}}{4kTR_S} \tag{2.35}$$

Noise factor (F) when expressed in decibels is called as noise figure (NF) as expressed as

$$NF = 10\log(F) \tag{2.36}$$

2.4 Linearity Overview

Most of the practical systems are non-linear. For a input v_{in}, a non-linear system output v_{out} can be written as

$$v_{out} = \alpha_0 + \alpha_1 v_{in} + \alpha_2 v_{in}^{\,2} + \alpha_3 v_{in}^{\,3} + ... \tag{2.37}$$

If v_{in} is a sinusoidal signal of frequency ω as given by A sin(ωt), it implies that v_{out} will contain other harmonics of input signal. Solving (2.37) results in

$$v_{out} \approx \left(\alpha_0 + \frac{\alpha_2 A^2}{2}\right) + \left(\alpha_1 A + \frac{3\alpha_3}{4}A^3\right)\sin(\omega t) + \left(\frac{\alpha_2 A^2}{2} + \frac{\alpha_4 A^4}{2}\right)\sin(2\omega t) + \left(\frac{\alpha_3 A^3}{4}\right)\sin(3\omega t) + ... \tag{2.38}$$

It can be seen from the above equation that the fundamental frequency component at the output is modified by third order harmonic component. Gain of the amplifier is going to expand or compress at higher amplitude levels depending on sign of α_3. This phenomenon is measured as a 1-dB compression point as shown in Fig. 2.4. 1-dB

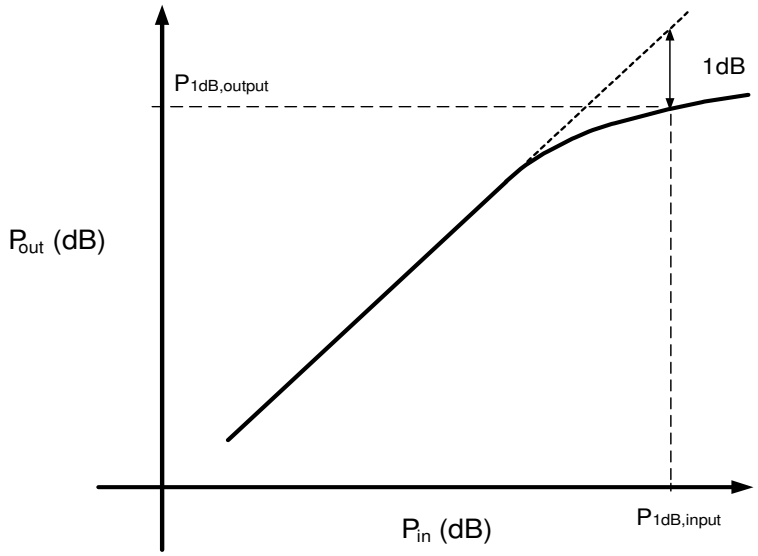


Fig. 2.4 Gain compression in a non-linear amplifier

compression point is defined as the input power for which output power is 1dB less than idea output. Mathematically, amplitude for which 1dB compression takes place is given by [4]

$$A_{1dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|} \tag{2.39}$$

2.4.1 Third Order Intercept Point

In reality in-band interferers get "mixed" with input signal and produce intermodulation products. To emulate this behavior, a two tone test is undertaken. Two signals at two closely spaced frequencies f_1 and f_2 are fed to the amplifier. Output of the amplifier contains third order intermodulation products (IM3) at $2f_1$-f_2 and $2f_2$-f_1. Amplitude of the fundamental and IM3 are shown in Fig. 2.5.

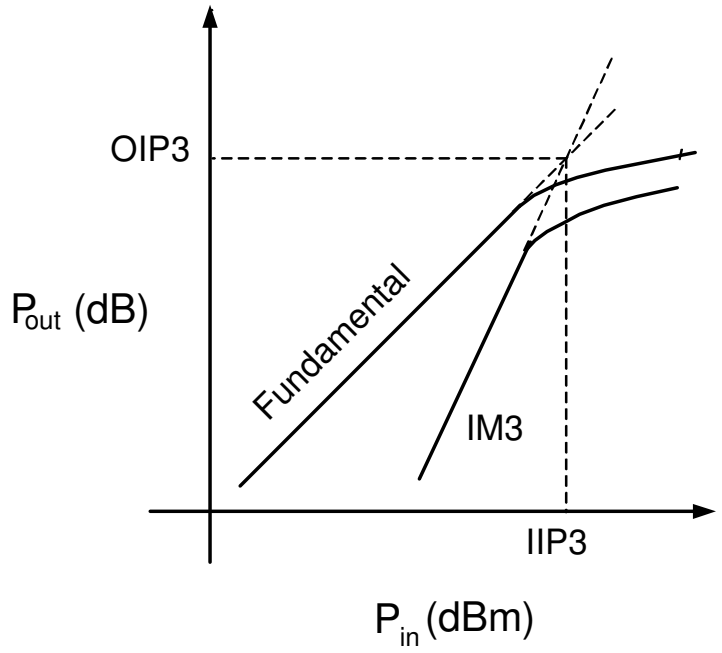


Fig. 2.5 Illustration of third order intercept point (IIP3)

which is roughly 10dB higher than the 1dB compression point.

2.5 Popular LNA Topologies

Usually LNAs are distinguished based on their matching network. Based on the specifications, different types of topologies have been proposed in the literature. In this section an overview of such topologies is highlighted.

2.5.1 Resistive Termination

Resistive termination [5] is probably the most straightforward topology as far as matching is concerned. In order to achieve impedance matching with the source impedance R_S, a simple resistor of value R_S is used in parallel to the input transistor gate. This is shown in Fig. 2.6

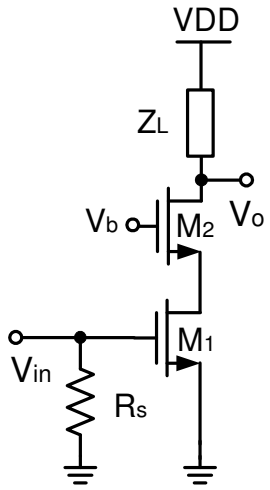


Fig. 2.6 Simple resistive termination

Obvious advantage of this topology is a simple broadband matching. Since this structure is devoid of any inductor, the total area required is small. However, the noise performance of such structure is poor. This is mainly due to the noise contribution by the termination resistor R_S and the input voltage attenuation at the gate of the transistor M1. Noise factor of this topology is shown as

$$F \geq 2 + \frac{4\gamma}{\alpha} \frac{1}{g_{m1} R_s} \tag{2.40}$$

Minimum noise figure that can be attained in this structure is 6dB. Linearity of course is improved because of attenuated input at the gate of M1, but at the cost of lower gain.

2.5.2 Common Gate Topology

Instead of using real resistor as in the previous topology, $1/g_m$ impedance seen in the source of a transistor can be used for matching purposes. This is called as common gate topology [5] as shown in Fig. 2.7 where source resistance R_S is matched to $1/g_{m2}$ of transistor M_2.

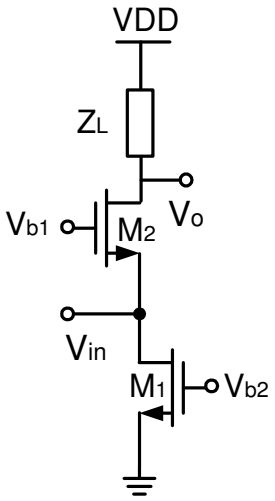


Fig. 2.7 Common gate topology

Noise factor of this topology neglecting the gate noise current is approximately given by

$$F \geq 1 + \frac{\gamma}{\alpha} \tag{2.41}$$

It can easily be calculated from above equation that the minimum achievable noise figure is 2.2dB in long channel devices and 4.8 in short channel devices. Main disadvantage in using this structure is its higher power consumption. In order to match input impedance to 50Ω, the g_m of the transistor M_2 has to be 20mA/V leading to higher power consumption. Advantages are broadband matching and smaller area.

2.5.3 Resistive Feedback Topology

Another broadband input matching LNA topology is realized by using a resistive feedback [5] as shown in Fig. 2.8. The input impedance is given by dividing feedback resistor R_f by the gain of the LNA (using miller theorem). This means that a higher R_F can be used for broadband 50Ω matching which results in lower noise figure as well. Hence it is possible to achieve low noise figures with higher gain over a broad frequency spectrum. Input impedance is given as

$$Z_{in} = \frac{R_F}{1+\left(g_m - \frac{1}{R_F}\right)\left(R_F \parallel R_L \parallel r_o\right)} \tag{2.42}$$

Approximate noise figure of this topology is given by

$$F = 1 + \frac{R_S}{R_F} \tag{2.43}$$

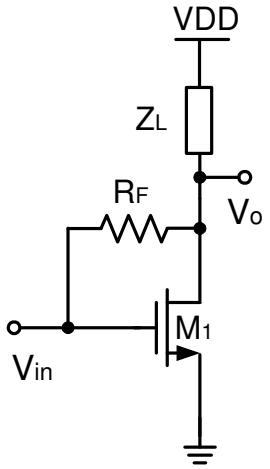


Fig. 2.8 Resistive feedback amplifier

2.5.4 Inductive Source Degeneration (ISD) Topology

Even though previously discussed topologies are broadband, most of the conventional wireless applications are narrow band only. Inductive source degeneration [5] as shown in Fig. 2.9 is used as an effective way of achieving simultaneous noise and power match. Due to source degeneration inductor L_S, a real part in input impedance (Z_{in}) appears and imaginary part is zero at the resonant frequency $\sqrt{\frac{1}{C_{gs}(L_g + L_s)}}$. Z_{in} can be written as

$$Z_{in} = j\omega\left(L_g + L_s\right) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_s \tag{2.44}$$

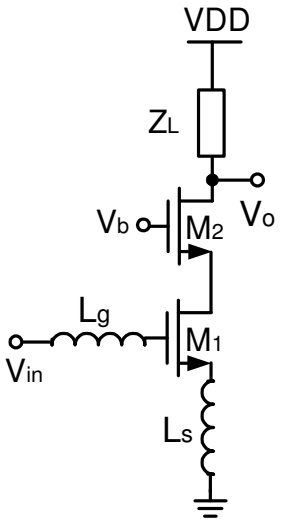


Fig. 2.9 Inductive source degenerated LNA

Noise figure expression for this topology is given approximately by

$$F \geq 1 + 2.3\left[\frac{\omega}{\omega_T}\right] \tag{2.45}$$

Hence it can be seen that attainable noise figures for this topology are very low. Being narrow band, high Q can be attained resulting in better noise figures and higher gain than broadband amplifiers.

CHAPTER III
ULTRA WIDEBAND LOW NOISE AMPLIFIER

3.1 Requirements of a UWB LNA

A general requirement for any wideband system is to maintain homogeneity in the system metrics for the whole band of interest. For LNA in particular, these metrics are input matching, noise figure, gain and linearity. Input matching is very important to transfer maximum power from the previous stage. At the same time, it should reject out of band signals. If the matching is not broadband, attaining flat gain at the output becomes tedious. Gain of the LNA should be high for desensitizing the noise effect of the following stages to the overall noise figure of the system. Besides, gain variation in the band of interest should be minimized as much as possible. Noise figure of the LNA should be as low as possible since it dominates the overall noise figure. The required specifications of a UWB LNA is given in Table 3.1

Table 3.1 LNA Specifications

Parameter	**Specification**
S11	<-10
Gain – S21 (dB)	15/0
Max Gain Variation (dB)	<1
Frequency range (GHz)	3.168-4.752
Noise Figure (dB)	<3.44
IIP3 (dBm)	>-7

3.2 Previous Work

There has been an extensive effort on applying broadband amplifier technique for low noise design. Common gate amplifiers [6], [7] are potential candidates for a broadband amplifier with low noise figures. Here matching is fairly simple and the overall LNA area is also small. However, simultaneous noise and power match in this structure is not possible. Also, power consumption increases as a tradeoff for good input matching. Resistive feedback [8], [9], [10] is another broadband amplifier topology which has been used as a low noise amplifier in broadband systems. They can achieve lower noise figures as compared to the previous structure. One of the main problems with this structure is unavailability of high quality resistors in the current fabrication technology. Negative feedback reduces the maximum available gain for the same power consumption. Isolation between input and output ports is low which can create potential instability. Distributed amplifiers [11], [12] make use of the fact that L-C ladder can be approximated as a transmission line with constant characteristic impedance over a frequency range, providing a broadband matching. Multiple transistors are used such that gate capacitance of each transistor can be absorbed into the L-C ladder. Adding output current of each transistor in phase by keeping the phase delay of both source and drain lines as same, enhances the bandwidth. High gain and low noise figures are however difficult to achieve from this methodology. Topologies discussed above have low pass behavior, whereas we need band-pass characteristic for the input matching circuit since it helps in rejecting out of band interferers. Recently, two 3.1 – 10.6 GHz UWB LNA architectures ([13] and [14]) are implemented in 0.18µm CMOS process and 0.18µm BiCMOS process respectively. They make use of a LC band-pass structure to implement input matching network. This architecture is based on inductive source degeneration technique often used in narrow band LNAs. By doing so, it is possible to achieve simultaneous noise and power matching. Both of these architectures use shunt peaking load at the output for achieving maximally flat gain. The relevant previous work is summarized in Table 3.2

Table 3.2 LNA Previous Work

Ref	Freq (GHz)	S21 (dB)	NF (dB)	PD (mW@V)	Technology	Technique
[7]	0-7.8	10.6	<4.4	6.5@1.8	0.25µm BiCMOS	Common Gate
[9]	3.1-10.6	18.5	<3.3	19@3	0.25µm BiCMOS	Resistor Feedback
[10]	0-5	12.2	<5.1	75@	0.18µm CMOS	Resistor Feedback
[12]	0.5-8.5	5.5	>13	216@3	0.6µm CMOS	Distributed Amp.
[13]	3.1-10.6	9.3	>4.2	9@1.8	0.18µm CMOS	Wideband ISD
[14]	3.1-10.6	21	>2.5	27@2.7	0.18µm BiCMOS	Wideband ISD

3.3 Proposed UWB LNA

Fig. 3.1 shows the structure of the proposed UWB LNA. It is differential in nature where each differential input is matched to 50Ω using a $1:\sqrt{2}$ balun. Advantage of using differential structure is better rejection of common mode noise coming from the digital sources or through power supply. In single ended LNA, the bondwire for signal ground comes in series with the actual circuit. This increases the source degeneration to the given LNA. Many techniques have been used to combine multiple bondwires in parallel to reduce this effect. This in fact increases the capacitance at the source of input transistor introducing negative real part in the input impedance. However in differential structures, additional small on chip source degeneration inductors can be used and bondwire inductance does not effect the differential operation. At high frequencies, this bondwire infact helps in improving the common mode performance. Differential structures have 3dB improvement in IIP3 as compared to its single ended counterpart. This improvement is essentially because input signal power is split into half.

Differential structure can be either fully or pseudo-differential. In case of pseudo-differential architecture, maximum voltage required at the gate of input transistors to keep them in saturation is $2(V_{GS}-V_T)$ where as for fully differential structures it is $\sqrt{2}(V_{GS}-V_T)$. Thus using pseudo-differential structure helps in increasing linearity and voltage headroom. For the above said advantages, pseudo-differential structure is used. Higher power consumption is traded for better robustness and performance. One

potential issue with this structure is that common mode rejection under mismatch conditions is degraded. The mismatch can be reduced with proper layout techniques for example, by symmetric layout and placing transconductor transistors close to each other.

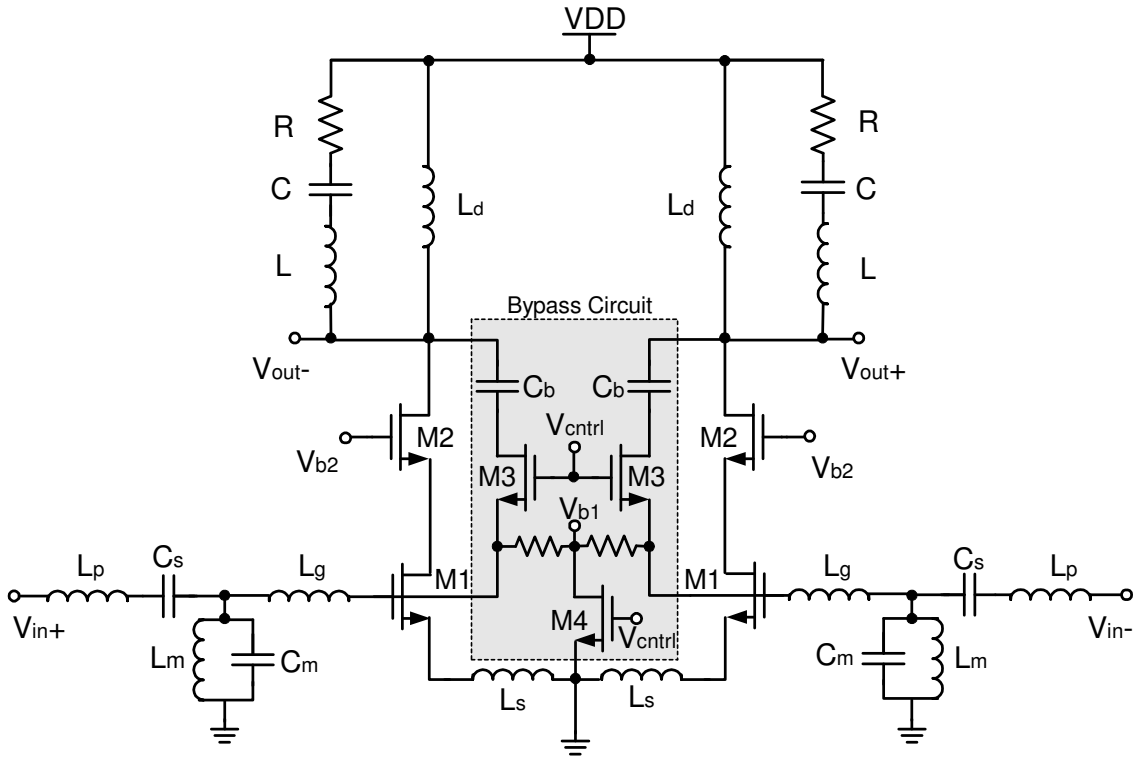


Fig. 3.1 Proposed ultra wideband LNA

As discussed before, inductive source degeneration based amplifiers achieve lower noise figures as compared to other LNA architectures. But they are inherently narrow band amplifiers. Broadband matching for inductive source degenerated topology yields low noise figures and high gains. This is achieved by using additional LC network in the input to have constant real input impedance for the whole band of interest. This is implemented by using L_p, C_s, L_m, C_m and L_g in addition to source degeneration inductor L_s as a part of input matching network in a manner shown in Fig. 3.1. Flat gain at the output with minimum ripple is achieved by band-pass behavior shown by output load consisting of L, R, C, L_d and parasitic capacitance C_{par} at the load.

For the low gain setting of LNA, a by-pass circuit is embedded in the main LNA as shown in Fig. 3.1. In the low gain mode, LNA is powered down by switching the bias voltage V_{b1} to zero with the aid of switch M_4. Output is now directly connected to the input with the help of bypass capacitor C_b by turning switch M_3 on.

3.3.1 Broadband Input Matching

A simple inductive source degenerated transistor is shown in Fig. 3.2. The input impedance of the amplifier has a real part equal to $\omega_T L_s$ as shown in the figure. Now let us examine a third order LC bandpass filter as shown in Fig. 3.3. The input impedance is R_L in the passband of the filter.

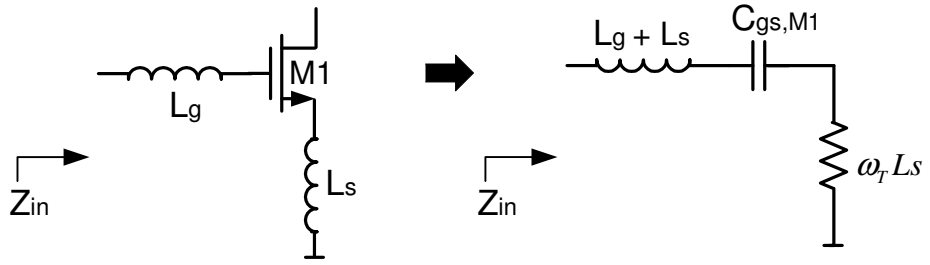


Fig. 3.2 Inductive source degeneration

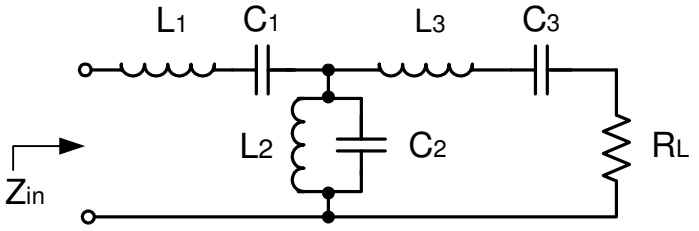


Fig. 3.3 Third order band-pass filter

By transforming the simple inductive source degeneration structure of Fig. 3.2 as a segment of the bandpass filter [13], the desired broadband matching can be achieved as shown in Fig. 3.4.

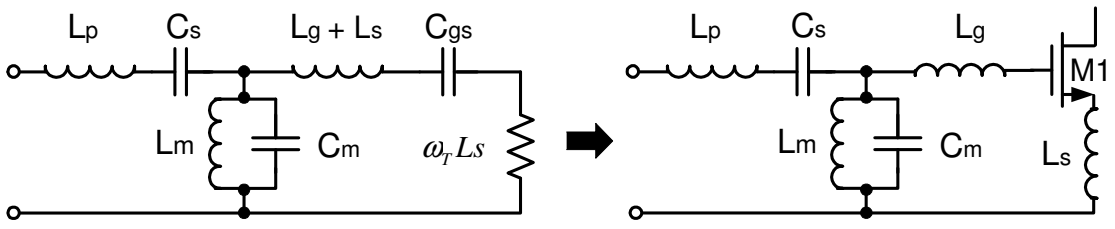


Fig. 3.4 Broadband input matching circuit

Size of the input transistor and its bias current is determined based on the noise consideration as discussed later. Based on this information rest of the matching circuit is designed. Impedance-scaled and frequency-transformed element values for centre frequency ω_0, bandwidth Δ and characteristic impedance Z_0 can be calculated as

$$L_1 = \frac{g_1 Z_o}{\omega_o \Delta} \tag{3.1}$$

$$C_1 = \frac{\Delta}{\omega_o g_1 Z_o} \tag{3.2}$$

$$L_2 = \frac{\Delta Z_o}{\omega_o g_2} \tag{3.3}$$

$$C_2 = \frac{g_2}{\omega_o \Delta Z_o} \tag{3.4}$$

$$L_3 = \frac{g_3 Z_o}{\omega_o \Delta} \tag{3.5}$$

$$C_3 = \frac{\Delta}{\omega_o g_3 Z_o} \tag{3.6}$$

where, g_1, g_2, g_3 and g_4 are elements of low-pass prototype which are chosen based on pass-band ripple specification. Chebyshev bandpass filter is chosen for improved rejection of out of band interferers because of its higher roll off.

3.3.2 Output Network

Assuming perfect input matching to the source impedance R_s in the pass-band, it can be derived that the small signal output current of the LNA for input voltage v_{in} is

$$i_{out}\big|_{pass-band} = \frac{g_m}{2s\,R_s\,C_{gs}}\,v_{in} \tag{3.7}$$

where g_m is the transconductance of the input transistor. It can be seen that the output current decreases with frequency. In order to achieve maximum gain flatness in the pass band, output load has to be modified such that a dominant zero(s) compensates for the decrease in gain. Some of the ways in which it can be done are discussed next.

3.3.2.1 Parallel R-L Load

Fig. 3.5.a. represents the small signal representation of a parallel R-L output load [5]. Here C_p includes the input capacitance of next stage and the parasitic capacitance at the output node. The output voltage (V_{out}) can be written as

$$v_{out}\big|_{pass-band} = \left(R_p \parallel s\,L_p \parallel \frac{1}{s\,C_p} \right) i_{out}\big|_{pass-band} \tag{3.8}$$

$$\begin{aligned} v_{out}\big|_{pass-band} &= \frac{g_m\,L_p}{2\,R_s\,C_{gs}\left(s^2 L_p C_p + s\frac{L_p}{R_p} + 1 \right)} v_{in} \\ &= \frac{g_m R_p}{2\,R_s\,C_{gs}\,R_p C_p\left(s^2 + s\frac{1}{R_p C_p} + \frac{1}{L_p C_p} \right)} v_{in} \end{aligned} \tag{3.9}$$

In order to get maximal flat gain, complex pole pair shown in (3.9) has to be at least a decade away from the pass-band. Also, high gain can be achieved by increasing L_p which degrades the bandwidth as it lowers the frequency of the complex pole pair. Hence there is a severe limitation in getting higher gains for broadband applications.

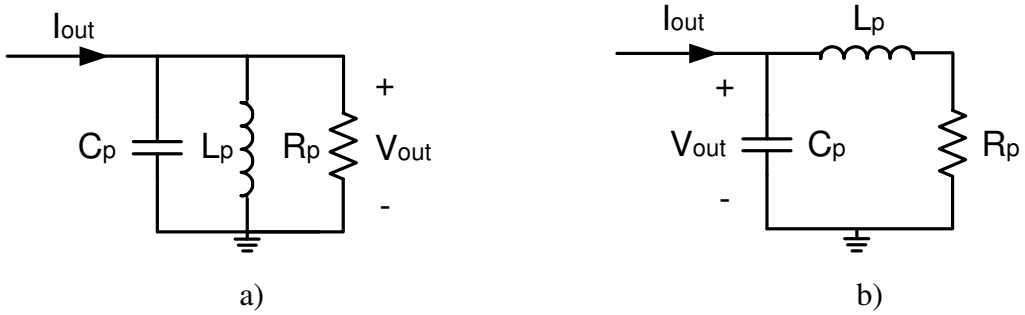


Fig. 3.5 a) Parallel R-L output load b) R-L series output load

3.3.2.2 Series R-L load

Fig. 3.5.b represents the small signal equivalent of series R-L output load [5]. Here C_p includes the input capacitance of next stage and the parasitic capacitance at the output node. Thez expression for output voltage (V_{out}) can be written as

$$v_{out}\big|_{pass-band} = \left(\left(R_p + s\,L_p\right) \| \frac{1}{s\,C_p} \right) i_{out}\big|_{pass-band} \tag{3.10}$$

which is further simplified as

$$\begin{aligned} v_{out}\big|_{pass-band} &= \frac{g_m\,R_p \left(1+\dfrac{s\,L_p}{R_p}\right) v_{in}}{2\,s\,R_s\,C_{gs}\left(s^2 L_p C_p + s\,R_p\,C_p + 1\right)} \\ &= \frac{g_m\,R_p \left(1+\dfrac{s\,L_p}{R_p}\right) v_{in}}{2\,s\,R_s\,C_{gs} L_p C_p \left(s^2 + s\dfrac{R_p}{L_p} + \dfrac{1}{L_p C_p}\right)} \end{aligned} \tag{3.11}$$

As seen from (3.11) the output voltage gain is proportional to the load resistance R_p. Left Hand Plane (LHP) zero at R_p / L_p gives a positive shift in the transfer function compensating for the negative slope introduced in (3.7). This is how gain flatness in the pass-band is achieved. For achieving larger bandwidth, complex pole pair should be at least a decade away from the pass-band. This structure can simultaneously achieve higher gain and higher bandwidth as compared to the previous structure. This is because

L_p is decoupled from gain. However, there is a severe limitation to this structure when the parasitic capacitance C_p is large such that the complex pole pair appears within the pass-band. In such cases L_p has to be decreased to very low values, R_p has to be decreased as well to maintain the same zero location, hence decreasing the gain. In addition, higher gain can be a limitation because higher R_p also leads to higher voltage drop across it forcing some of the transistors out of saturation.

3.3.2.3 Proposed Output Network

Consider the circuit of Fig.3.6. With proper choice of the circuit elements, a 4th order band-pass structure can be realized. In the pass-band, the input impedance of the circuit is R. If such structure can be realized as the load of a transconductor, the resulting output voltage gain will be constant in the pass band. This gives a good starting point for the proposed output network. Total input output impedance of the LNA is given by

$$Z_{out} = \left(R + sL + \frac{1}{sC} \right) \| \frac{1}{sC_{par}} \| sL_d \tag{3.12}$$

which after simplification can be written as

$$Z_{out} = \frac{sL_d\left(s^2LC + sRC + 1\right)}{s^4L_dC_{par}LC + s^3L_dC_{par}RC + s^2\left(L_dC_{par} + LC + L_dC\right) + sRC + 1} \tag{3.13}$$

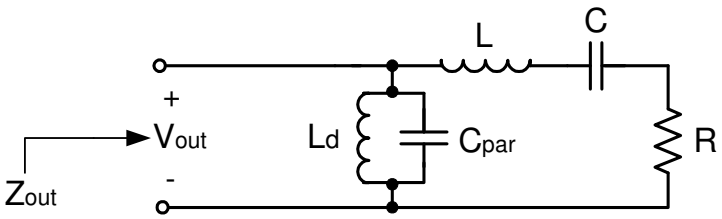


Fig.3.6. Proposed output network

In order to design the band-pass filter following equation are used

$$L = \frac{R}{\omega_o} \tag{3.14}$$

$$C = \frac{1}{L\omega_o^{\,2}} \tag{3.15}$$

$$L_d = \frac{1}{C_{par}\omega_o^{\,2}} \tag{3.16}$$

where ω_0 is the centre frequency of the pass-band and R is determined by the gain requirement of the LNA. It can be seen that the output current (i_{out}) as shown in (3.7) is not constant with frequency. The resulting output voltage in the pass band is given as

$$v_{out}\big|_{pass-band} = \frac{g_m L_d}{2R_s C_{gs}}\left[\frac{\left(s^2LC + s\,RC + 1\right)v_{in}}{s^4 L_d C_{par} LC + s^3 L_d C_{par} RC + s^2\left(L_d C_{par} + LC + L_d C\right) + s\,RC + 1}\right] \tag{3.17}$$

Constant gain in the pass-band is achieved by increasing the pole frequency by decreasing the L_d calculated in (3.16).

3.3.3 Noise Analysis

Small signal noise model for the LNA with the proposed input matching can be represented as shown in Fig. 3.7. Z_s represents the source degeneration impedance which in this case is equal to ω_TLs. i_{ng} and i_{nd} represent gate and drain noise currents respectively of transistor M_1. Z_g is the impedance of the matching network at the gate of the transistor which is given by

$$Z_g = sL_g + \left[\left(R_s + s\,L_p + \frac{1}{s\,C_s}\right) \| \frac{1}{s\,C_m} \| s\,L_m\right] \tag{3.18}$$

Noise analysis with (3.18) becomes very complicated. In order to simplify the analysis, it is assumed that the input impedance of the LNA is perfectly matched to the source impedance Rs. Under this assumption, Zg can be written as

$$Z_g = R_s - s\,L_s - \frac{1}{s\,C_{gs}} \tag{3.19}$$

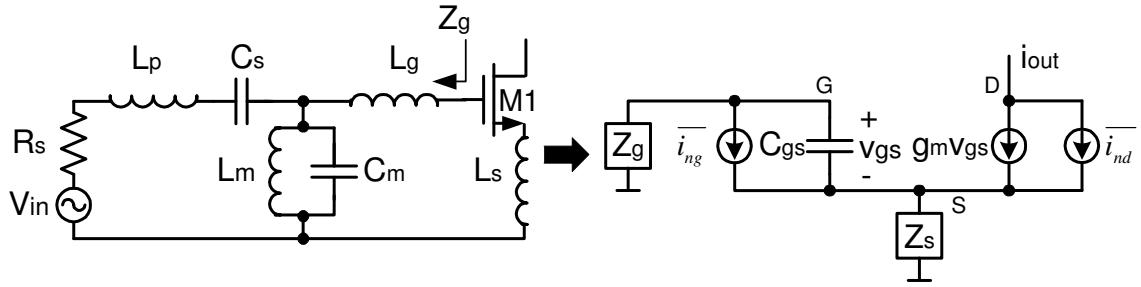


Fig. 3.7 Noise model for the LNA – step I

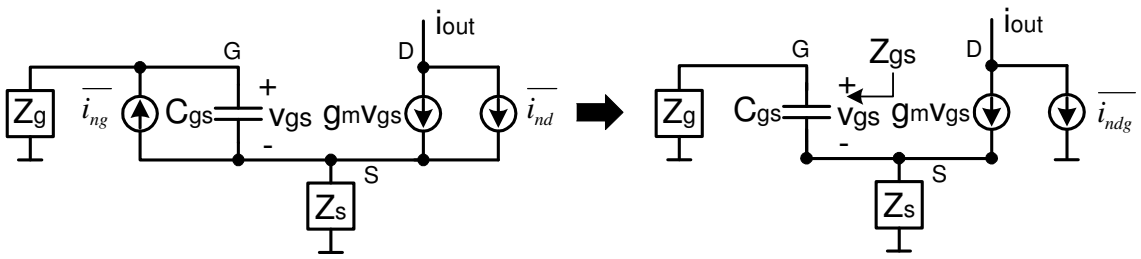


Fig. 3.8 Noise model for the LNA – step II

Cumulative noise of the LNA can be represented as i_{ng} at the drain of M1 as shown in Fig. 3.8. It can be represented mathematically as [15]

$$\overline{i_{ndg}} = \eta \overline{i_{nd}} + g_m Z_{gs} \overline{i_{ng}} \tag{3.20}$$

where η is a fraction of drain noise current appearing in i_{ng} which is given

$$\eta = 1 - \left(\frac{g_m Z_g}{Z_s + Z_g} \right) Z_{gs} \tag{3.21}$$

Z_{gs} is the total impedance between the gate and the source of the transistor given by [15]

$$Z_{gs} = sC_{gs} \parallel \frac{Z_s + Z_g}{1 + g_m Z_g} \tag{3.22}$$

The root mean square value of this current is shown as [15]

$$\overline{i_{ndg}{}^2} = \overline{i_{ndg}\, i^*{}_{ndg}} = \overline{i_{nd}{}^2}\left(|\eta|^2 + 2\,\mathrm{Re}\left\{ c\sqrt{\frac{\overline{i_{ng}{}^2}}{\overline{i_{nd}{}^2}}}\, g_m \eta^* Z_{gs} \right\} + \frac{\overline{i_{ng}{}^2}}{\overline{i_{nd}{}^2}}\, g_m{}^2 \left| Z_{gs} \right|^2 \right) \tag{3.23}$$

Here *c* is a correlation coefficient between gate noise current and the drain noise current as shown as

$$c = \frac{\overline{i^*{}_{nd}\, i_{ng}}}{\sqrt{\overline{i_{nd}{}^2}\,\overline{i_{ng}{}^2}}} \tag{3.24}$$

Substituting the expressions for noise currents i_{nd} and i_{ng}, (3.23) can be rewritten as

$$\overline{i_{ndg}{}^2} = \overline{i_{nd}{}^2}\left(|\eta|^2 + 2\,\mathrm{Re}\left\{ c\chi_d \eta^* Z_{gsw} \right\} + \chi_d{}^2 \left| Z_{gsw} \right|^2 \right) \tag{3.25}$$

where χ_d and Z_{gsw} are given by

$$\chi_d = g_m \sqrt{\frac{\overline{i_{ng}{}^2}}{\overline{i_{nd}{}^2}}} = \frac{g_m}{g_{do}} \sqrt{\frac{\delta}{5\gamma}} \tag{3.26}$$

$$Z_{gsw} = \omega C_{gs} Z_{gs} \tag{3.27}$$

Using (3.18), Z_{gs} in (3.24) can be simplified as

$$Z_{gs} = \frac{1}{sC_{gs}} \left(\frac{R_s - \dfrac{1}{sC_{gs}}}{\dfrac{g_m L_s}{C_{gs}} + R_s} \right) = \frac{1}{2\,sC_{gs}} \left(1 - \frac{1}{sC_{gs} R_s} \right) \tag{3.28}$$

This is under the assumption of perfect matching to source impedance i.e.

$$\frac{g_m L_s}{C_{gs}} = \omega_T L_s = R_s \tag{3.29}$$

Also, (3.21) and (3.27) can be simplified as follows

$$\eta = 1 - \left(\frac{\dfrac{g_m L_s}{C_{gs}}}{\dfrac{g_m L_s}{C_{gs}} + R_s} \right) Z_{gs} = \frac{1}{2} \tag{3.30}$$

$$Z_{gsw} = \frac{1}{2j}\left(1 - \frac{1}{j\omega C_{gs} R_s}\right) = \frac{1}{2} + jQ \tag{3.31}$$

where Q represents the quality factor of the input matching circuit and is given by

$$Q = \frac{1}{2\omega C_{gs} R_s} \tag{3.32}$$

Using simplified expressions of (3.30) and (3.31) in (3.25), final expression of output noise current i_{ndg} is derived as

$$\overline{i_{ndg}^{\,2}} = \frac{\overline{i_{nd}^{\,2}}}{4}\left(1 - 2|c|\chi_d + \chi_d^{\,2}\left(4Q^{\,2}+1\right)\right) \tag{3.33}$$

Noise Factor (F) can now be written as

$$F = 1 + \frac{\overline{i_{ndg}^{\,2}}}{i_{ns,out}^{\,2}} = 1 + \frac{\overline{i_{ndg}^{\,2}}}{(g_m Q)^2\ \overline{v_{ns}^{\,2}}} \tag{3.34}$$

where $\overline{v_{ns}^{\,2}}$ is the noise voltage of the source which is given by $4KTR_s\Delta f$. Using (3.33) in (3.34) noise factor can be rewritten as

$$F = 1 + \frac{\gamma g_{do}}{4(g_m Q)^2 R_s}\left(1 - 2|c|\chi_d + \chi_d^{\,2}\left(4Q^{\,2}+1\right)\right) \tag{3.35}$$

or further simplified as

$$F = 1 + \frac{\omega}{\omega_T}\frac{\gamma g_{do}}{2 g_m Q}\left(1 - 2|c|\chi_d + \chi_d^{\,2}\left(4Q^{\,2}+1\right)\right) \tag{3.36}$$

The above expression for noise factor can be minimized for Q [16]. The optimum value of Q for lowest noise factor is defined as Q_{opt} and is given by

$$Q_{opt} = \sqrt{\frac{1 - 2|c|\chi_d + \chi_d^{\,2}}{4\chi_d^{\,2}}} \tag{3.37}$$

The width of transistor M1 can be optimized based on the value of Q_{opt} as

$$W_{opt} = \frac{C_{gs,opt}}{\frac{2}{3}C_{ox}L} = \frac{3}{4\omega R_s Q_{opt} C_{ox} L} \tag{3.38}$$

This can further be rewritten using (3.37) as

$$W_{opt} = \frac{3}{4\omega_o R_s C_{ox} L}\sqrt{\frac{4\chi_d^{\,2}}{1-2|c|\chi_d+\chi_d^{\,2}}} \tag{3.39}$$

where centre frequency of the pass-band (ω_o)is used to find the optimum width.

The above analysis assumes ideal inductors. In reality, inductors have finite series resistance which contributes to the noise. In the proposed structure, in order to fine tune the noise analysis, let us assume that series resistance (r_g) of inductor L_g is the main noise contributor. In that case, the overall noise factor can be written as

$$F = 1+\frac{r_g}{R_s}+\frac{\omega}{\omega_T}\frac{\gamma g_{do}}{2g_m Q}\left(1-2|c|\chi_d+\chi_d^{\,2}\left(4Q^{\,2}+1\right)\right) \tag{3.40}$$

Assuming the finite quality factor of the inductor Q_{Lg}, second expression can be expressed as

$$\frac{r_g}{R_s} = \frac{\omega L_g}{R_s Q_{Lg}} \tag{3.41}$$

L_g+ L_s tunes out C_{gs} at centre frequency ω_0. Since L_s is much smaller than L_g, (3.41) can be rewritten as

$$\frac{r_g}{R_s} \approx \frac{1}{\omega C_{gs} R_s Q_{Lg}} = \frac{2Q}{Q_{Lg}} \tag{3.42}$$

This makes final noise factor expression as

$$F = 1+\frac{2Q}{Q_{Lg}}+\frac{\omega}{\omega_T}\frac{\gamma g_{do}}{2g_m Q}\left(1-2|c|\chi_d+\chi_d^{\,2}\left(4Q^{\,2}+1\right)\right) \tag{3.43}$$

The above expression for noise factor can be minimized for Q by equating its derivative to zero. The optimum value of Q for lowest noise factor is defined as $Q_{opt,Lg}$ and is given by (3.37).

$$Q_{opt,Lg} = \sqrt{\frac{1-2|c|\chi_d+\chi_d^{\,2}}{4\chi_d^{\,2}+\frac{4}{Q_{Lg}}\frac{g_m}{\gamma g_{do}}\frac{\omega_T}{\omega_o}}} \tag{3.44}$$

Comparing (3.44) to (3.37), it can be seen that the required quality factor decreases with lower inductor quality factor. In fact, by putting Q_{Lg} to infinity it can be seen that (3.44) turns into (3.37).

The width of transistor M1 can now be optimized based on the value of $Q_{opt,Lg}$ as

$$W_{opt} = \frac{C_{gs,opt,Lg}}{\frac{2}{3}C_{ox}L} = \frac{3}{4\omega R_s Q_{opt,Lg} C_{ox} L} \tag{3.45}$$

This can further be written using (3.44) as

$$W_{opt} = \frac{3}{4\omega_o R_s C_{ox} L}\sqrt{\frac{4\chi_d{}^2 + \frac{4}{Q_{Lg}}\frac{g_m}{\gamma g_{do}}\frac{\omega_T}{\omega_o}}{1-2|c|\chi_d+\chi_d{}^2}} \tag{3.46}$$

where centre frequency of the pass-band (ω_o) is used to find the optimum width.

3.3.4 Linearity Analysis

Even though power levels of input signal are of the order of -60dBm, linearity is still important. This is because, out of band interferers of significant power levels generate harmonic components which appear in-band and deteriorate the signal. In order to analyze the non-linear behavior, consider the small signal circuit of Fig. 3.9. This represents one half section of the LNA structure. Here Yo1 is the effective output admittance of the input transistor M1 and gm2 being the transconductance of the cascode transistor. Here it is assumed that output resistance of M2, r_{ds2} is much greater than R_{out}. Input voltage V_{in} can be written as [17]

$$V_{in} = a_1(s)V_{gs} + a_2(s)i_d \tag{3.47}$$

where

$$a_1(s) = sC_{gs}R_s \tag{3.48}$$

$$a_2(s) = sL_s\left(1+\frac{Y_{o1}}{g_{m2}}\right) \tag{3.49}$$

In the above equations it is assumed that matching is perfect within the passband.

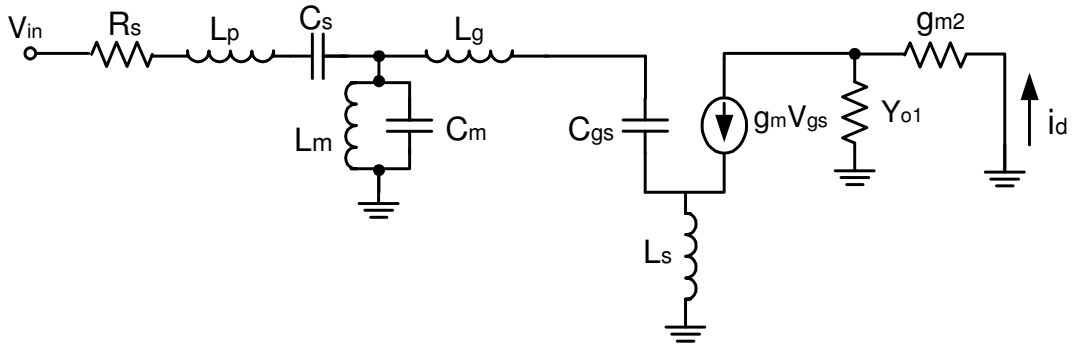


Fig. 3.9 Small signal model for linearity analysis

Output current of the LNA for the given small signal model can be written in terms of input signal V_{in} and volterra series coefficient $H_n()$ as [17]

$$i_d = H_1(s) o V_{in} + H_2(s_1, s_2) o V_{in}^{\ 2} + H_3(s_1, s_2, s_3) o V_{in}^{\ 3} \tag{3.50}$$

where operator 'o' means multiplying each frequency component of $V_{in}^{\ n}$ by $H_n()$ and shifting the phase of each frequency component in $V_{in}^{\ n}$ by the phase of $H_n()$. In order to calculate the IM3 component at $2\omega_a$-ω_b letting s_1 and s_2 be s_a and s_3 be $-s_b$. For two tone test, s_a and s_b are placed close to each other at an offset Δs which is very small.

IIM3 can be simplified as [17]

$$\left|IM3\right| = \frac{A^2}{2}\left|\frac{H_1^{\ 3}(s)}{g^{\ 3}_{m1}}\right|\left|a_1(s)\right|\left|3g_3 - 2g_2^{\ 2}M\right| \tag{3.51}$$

where

$$M = 2\Delta s L_s(\Delta s) a_2(\Delta s) H_1(s) + 2sL_s(2s) a_2(2s) H_1(2s) \tag{3.52}$$

$$H_1(s) = \frac{g_{m1}}{a_1(s) + g_{m1} a_2(s)} \tag{3.53}$$

$$g_2 = \frac{4K\mu_0 L^2 v_{sat}^{\ 2}}{\left[(V_{gs} - v_t)\mu_1 + 2Lv_{sat}\right]^3} \tag{3.54}$$

$$g_3 = \frac{4K\mu_0 L^2 v_{sat}^{\ 2}\mu_1}{\left[(V_{gs} - v_t)\mu_1 + 2Lv_{sat}\right]^4} \tag{3.55}$$

using 3.48 and 3.49, 3.50 can be further simplified as

$$\left|IM3\right| = \frac{A^2}{2}\left|\frac{1}{sC_{gs}R_s + g_{m1}sL_s(1+\frac{Y_{o1}}{g_{m2}})}\right|^3 \left|sC_{gs}R_s\right|\left|3g_3 - 2{g_2}^2 M\right| \tag{3.56}$$

or

$$\left|IM3\right| = \frac{A^2}{4}\left|\frac{1}{2sC_{gs}R_s(1+\frac{Y_{o1}}{2g_{m2}})}\right|^3 \left|2sC_{gs}R_s\right|\left|3g_3 - 2{g_2}^2 M\right| \tag{3.57}$$

or in terms of Q as

$$\left|IM3\right| = \frac{A^2 Q^2}{4}\left|\frac{1}{1+\frac{Y_{o1}}{2g_{m2}}}\right|^3 \left|3g_3 - 2{g_2}^2 M\right| \tag{3.58}$$

Observing (3.58) it can be seen that third order harmonic IM3 is proportional to the square of the quality factor Q. Thus increasing Q improves noise figure and degrades linearity. This is a direct trade-off of linearity with noise figure. The second term in (3.58) determines the size of transistor M_2. Decreasing g_{m2} improves the linearity. That is, size of transistor M_2 has to be small. However, due to miller effect and low frequency pole, very small size of the transistor M_2 is avoided. Third term in (3.58) when taking (3.54) and (3.55) into account as well, shows strong dependence on v_{dsat} of the transistor M1. Increasing the v_{dsat} of the transistor M_1 improves the linearity of the LNA due to velocity saturation. (3.58) can be represented in terms of IIP3 as

$$\left|IIP3\right| = \sqrt{\frac{4}{Q^2 R_s\left|3g_3 - 2{g_2}^2 M\right|}\left|1+\frac{Y_{o1}}{2g_{m2}}\right|^3} \tag{3.59}$$

3.4 Design Procedure

Before starting to design an LNA, it is important to know the process and characteristics of the MOSFET. Hence, the RF MOSFET in the design library is characterized for expected drain source voltage of 1V.

Analyzing Fig. 3.10, it can be seen that by increasing the overdrive voltage, transconductance g_m of the transistor starts saturating. This saturation is also evident in the f_T plot of Fig. 3.11, which saturates to around 48 GHz. In fact, f_T curve starts deviating from linear region at around 200mV overdrive. Additional overdrive does not increase the f_T but power consumption keeps increasing. Hence fixing overdrive around 200mV results in power consumption optimized noise performance. Also, higher overdrive increases noise due to hot carrier effect.

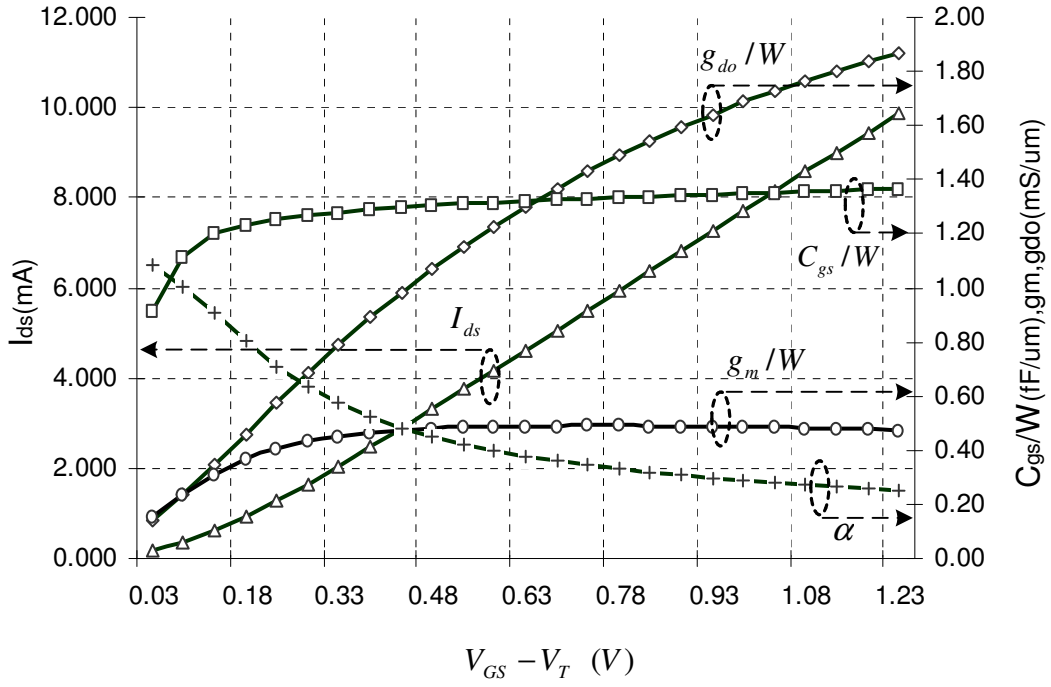


Fig. 3.10 Variation of gm, gdo, α, Ids and Cgs/W with overdrive voltage

Now the width of the transistor M_1 needs to be found which can be calculated from (3.39) or (3.44). This gives optimum width of 360μm but the required current from Fig.

3.11 comes out to be 25mA which is much above the power consumption specifications. Thus quality factor of the LNA has to be increased to optimize the LNA for power consumption.

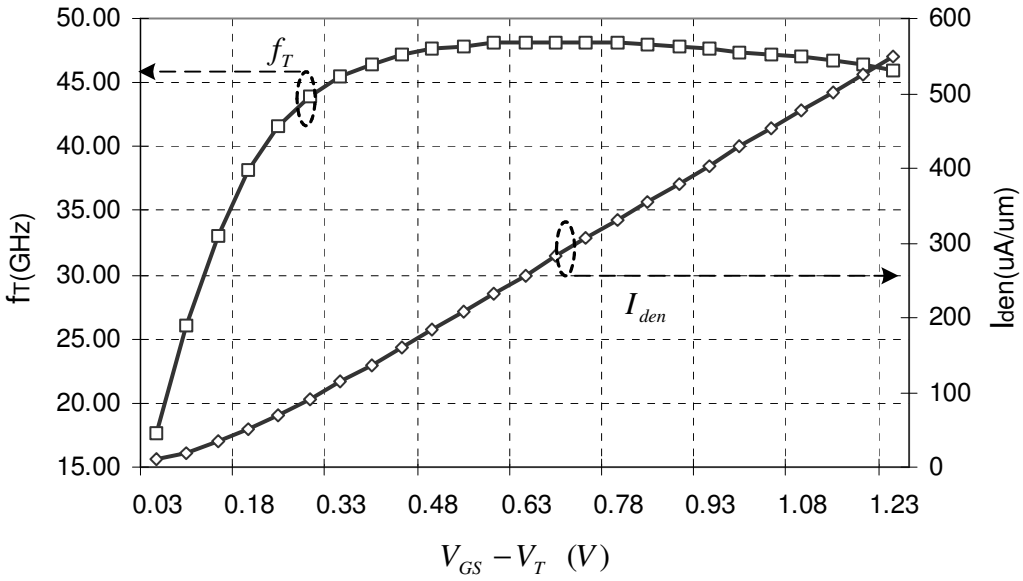


Fig. 3.11 Variation of f_T and current density with overdrive voltage

In general, quality factor of 4.5 [16] is considered to give power-consumption-optimized width. Using this value of Q, the transistor width comes out to be 160µm for 5mA bias current. Next step is to fix the width of transistor M_2. As discussed before, smaller width of M_2 improves linearity and reverse isolation but to avoid high Miller effect, M_2 was fixed at 80µm width. This gives overall capacitance at the gate Cg as 350fF which can be used in Eqs (3.1) through (3.6) to determine the input matching network.

For the design of output network, gain of 20dB is assumed. This gives value of R as 180Ω. The C_{par} is assumed to be 400fF which actually comes from the preliminary design of mixer. The design equations (3.14) to (3.16) are used to get initial values of output network parameters. Final LNA design parameters are tabulated in Table 3.3.

Table 3.3 UWB LNA Component Values

Lp	**Cs**	**Lg**	**Lm**	**Cm**	**Ls**	**M1 (W/L)**
2.5nH	530pF	2.36nH	2.36nH	130fF	500pH	142.5µm/0.18µm
Ld	**Cb**	**C**	**L**	**R**	**M2(W/L)**	**M3(W/L)**
2.36nH	250fF	110fF	8.5nH	600	80µm/0.18µm	12µm/0.18µm

3.5 Layout Considerations

In a high frequency design, the layout of a circuit plays a very important role. This is because layout determines the nature of parasitic resistances and capacitance which can alter the performance of the circuit dramatically. Signal strength at the LNA input is so small that it can easily be corrupted by the substrate noise, adjacent on-chip high power signals and interferences (clocks etc). Under these circumstances, a good layout practice becomes very essential. Having fully differential structure for the LNA rejects most of the common mode noise under the conditions of fully symmetric layout. However, due to process variation and mismatches, common mode rejection is degraded. Hence, the most critical devices are placed quite close to each other to achieve good matching and at the same time maintaining good isolation from each other. Due to better modeling for higher frequencies, only RF MOSFETs from the design library are used. Since these devices have fixed encapsulated layout, techniques such as inter-digitization become difficult to realize. Hence in order to improve matching, RF mosfets are placed closed to each other in such a way that process variations on either axis of orientation result in the lowest mismatch. Layout of the UWB LNA is shown in Fig. 3.12. As seen in the layout, transistor are laid along y axis such that process variation on x axis have little effect on the transistor and process variations on y axis will be same on both the transistors leading to better matching. Another major concern for LNAs is the series resistance of interconnects. Keeping this in mind, top metal layer is used for interconnection and multiple metal to metal contacts are used in parallel to reduce overall interconnect resistance.

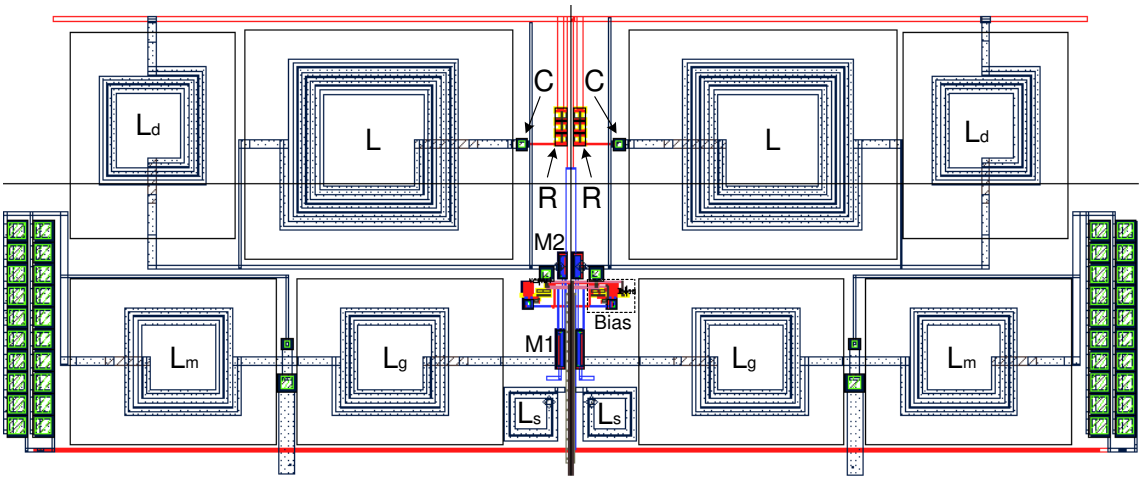


Fig. 3.12 Layout of Ultra Wideband LNA

3.6 Simulation Results

3.6.1 Input Rejection (S_{11})

S_{11} of the LNA is shown on magnitude plot and smith chart in Fig. 3.13 and

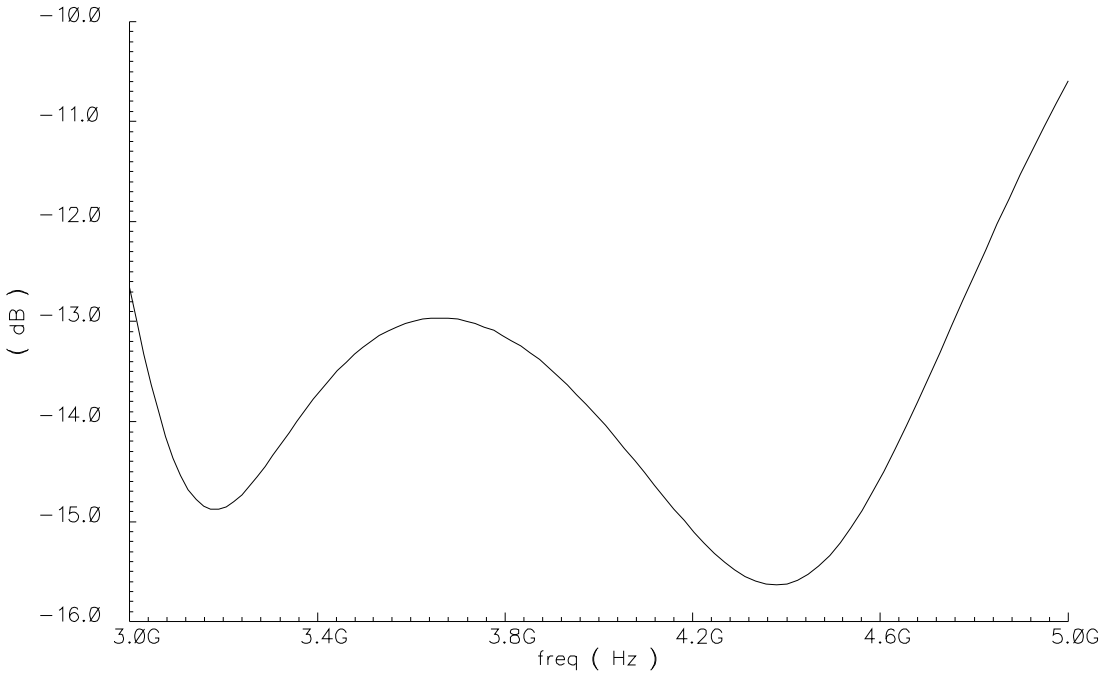


Fig. 3.13 Input rejection of LNA in magnitude vs. frequency scale

Fig. 3.14 respectively. Here it can be seen that input rejection is less than -10dB in the band of interest and increases towards 0dB mark outside the band of interest. Thus, in-band signals will pass through the matching network whereas out of band interferers will be rejected. S_{11} is plotted on a smith chart as shown in Fig. 3.14, where it can be seen as a circle around centre of the chart. In other words, real part of the input impedance is close to 50Ω and input reflection coefficient (distance from centre of the chart) is nearly constant over the desired range of frequencies.

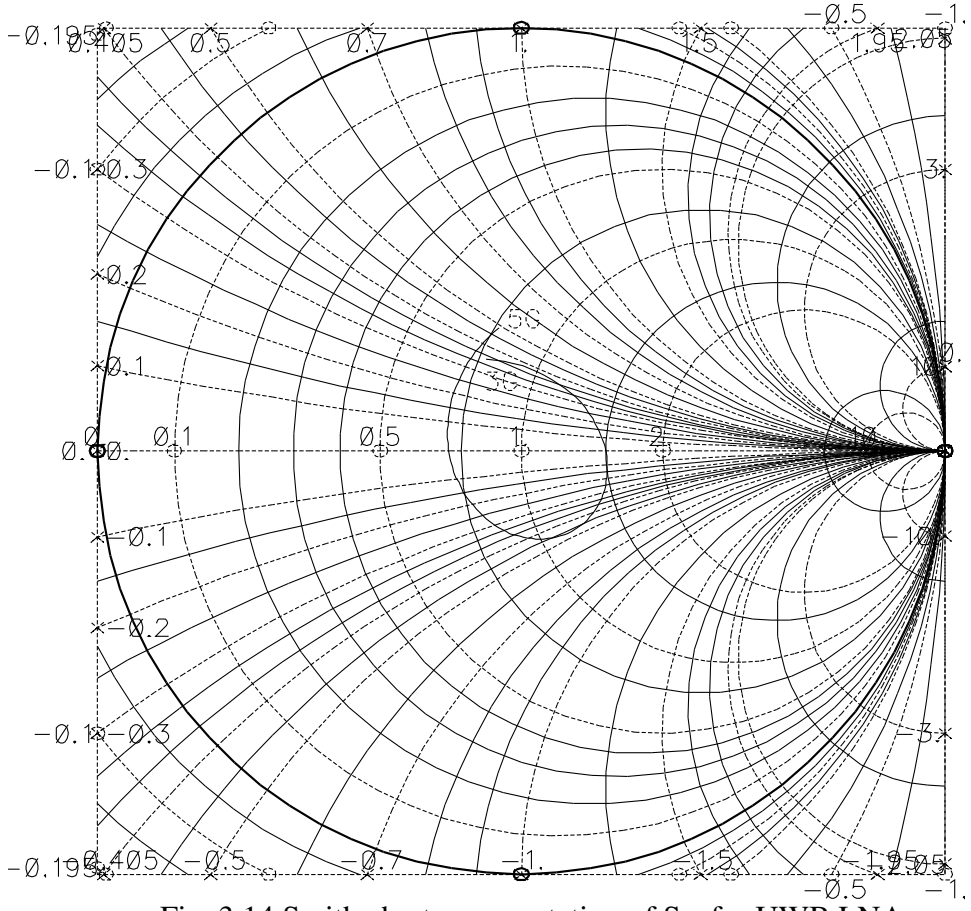


Fig. 3.14 Smith chart representation of S_{11} for UWB LNA

Of all the elements of the input matching network, the bond wire inductance (Lp) is the most prone to variation. Graphically, change in L_p shows up as a movement on a constant resistance circle. If L_p increases from the nominal value, the circle moves up

whereas it moves down if the inductance decreases from the nominal value. This can be corrected externally, by adding small series capacitance or inductances.

3.6.2 Power Gain (S_{21})

Since the UWB LNA is used in a direct conversion receiver, it is the voltage gain which is important at the input of the mixer. However, S_{21} is measured as a standard figure of merit. In order to measure S_{21}, an ideal source follower is used after LNA such that it provides 50Ω matching to the output port as well. Voltage gain of the LNA can easily be calculated by adding 6dB to S_{21}.

As shown in Fig. 3.15, average S_{21} achieved in the UWB LNA is 15.5dB. It can be seen that there is about +/- 0.35dB of ripple in the gain plot. This is essentially due to

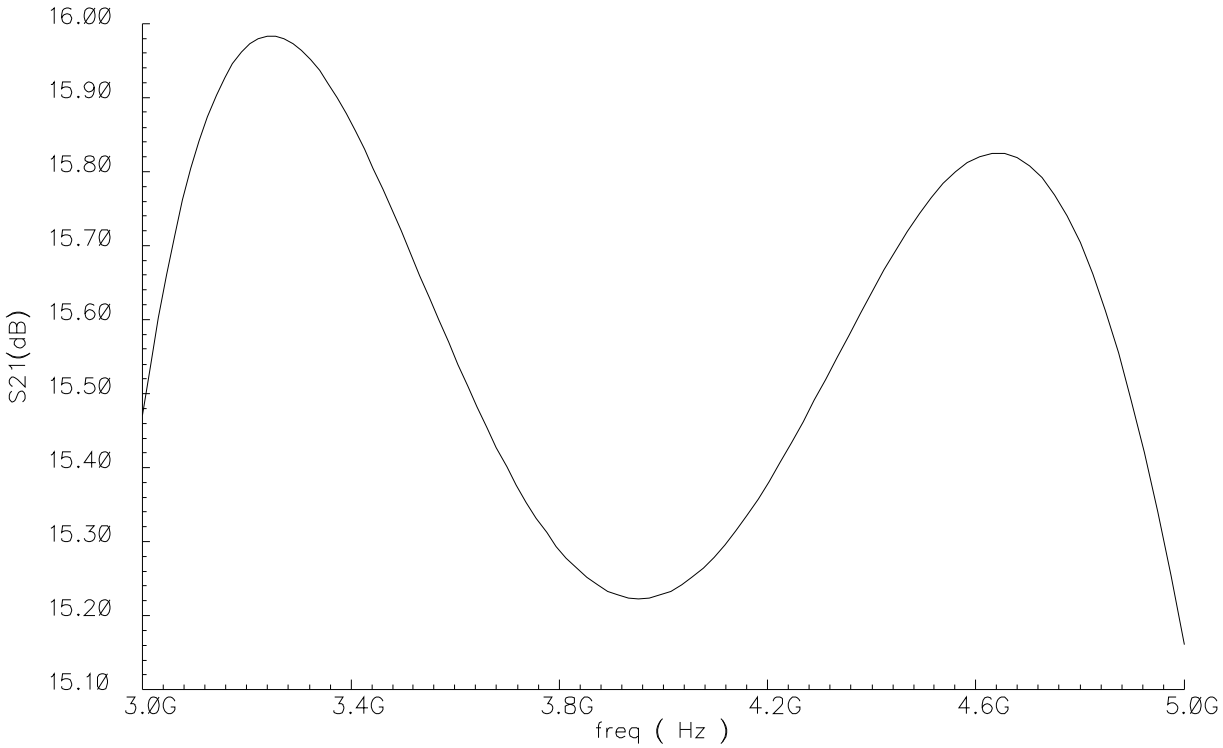


Fig. 3.15 S_{21} of the UWB LNA

Chebyshev bandpass filter implementation in the output network of the LNA. To decrease the ripple, value of R can be increased as a trade-off with a lower bandwidth. This measurement has been taken with UWB mixer loading the LNA. Due to use of inductor in the mixer, the input capacitance of the mixer is modified. Hence, based on mixer characteristics, output network of the LNA is adjusted in order to get the flat band characteristic with minimum ripple.

3.6.3 Noise Figure (NF)

Fig. 3.16 shows the noise figure of the UWB LNA. It can be seen that for the most part of the pass-band, noise figure is less than 2.5dB. It is only on the extremes of the frequency band that noise figure degrades. This is mainly due to decreasing gain of the LNA such that input referred noise of the output increases.

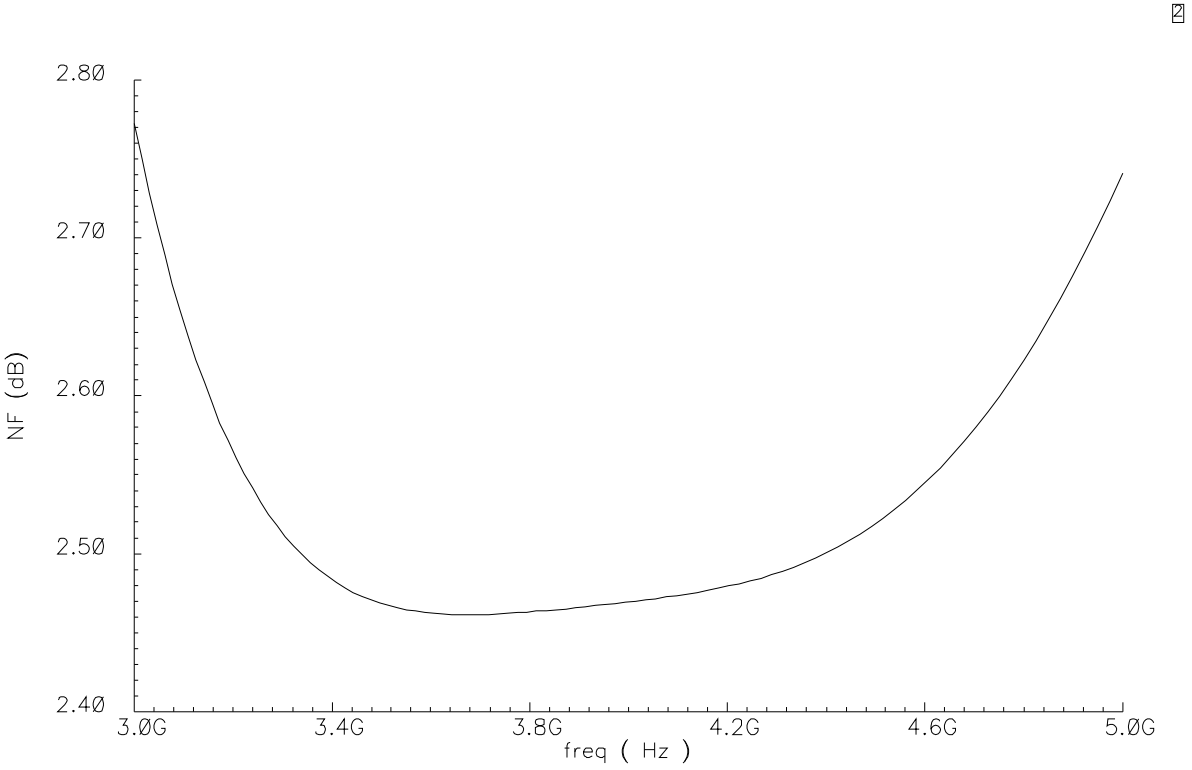


Fig. 3.16 Noise figure of the UWB LNA

3.6.4 Input Referred IP3

Input referred IP3 (IIP3) is measured by applying two-tone test to the LNA input. Frequencies of the two tones should be very close to each other and can be anywhere in the pass-band. However, since IIP3 does not vary a lot because of relative gain flatness, for the purpose of measurement, only mid band frequencies are chosen. In order to measure IIP3, one has to be sure to include mixer as the load. This is because non-linear transconductance stage produces intermodulation products which leak back to the LNA output due to finite gate drain capacitance. Also, the input capacitance of the mixer is non-linear in nature. Fig. 3.17a and 3.17b show IIP3 measurements for capacitance load and mixer load respectively. Here, considerable difference in both measurements can be seen.

3.6.5 Power Consumption

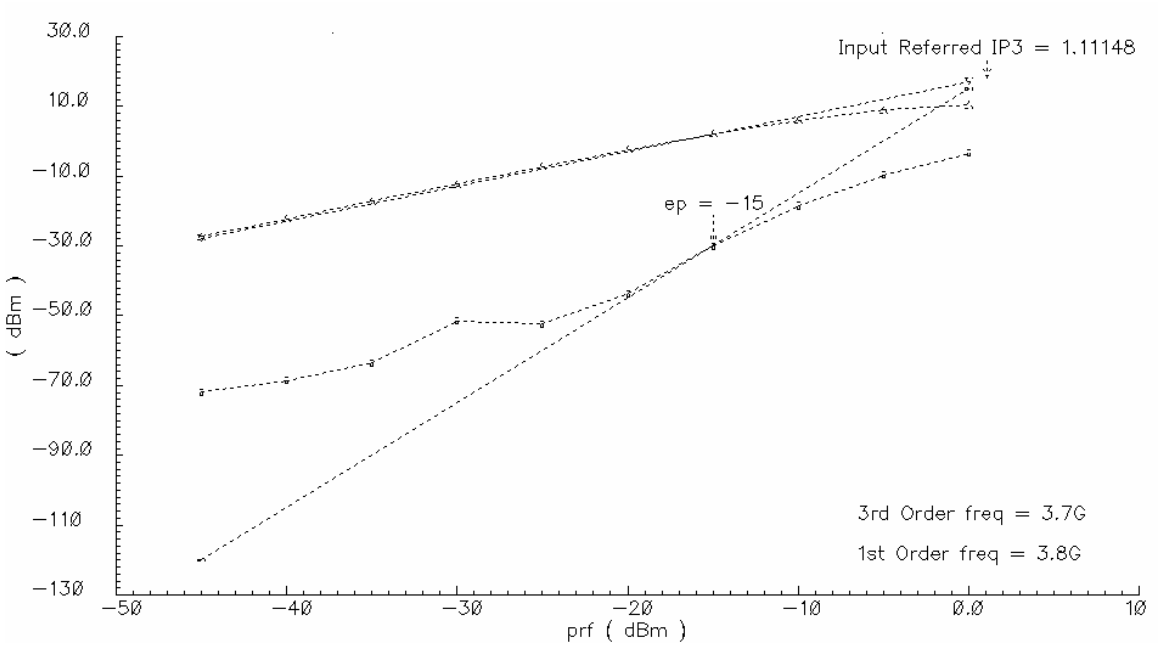
UWB LNA consumes 10.7mA of current including currents for generating bias. Equivalently, UWB LNA consumes 19.26mW of power. Core LNA however consumes 10mA of current. Higher power consumption is mainly due to fully differential structure.

3.6.6 Simulation Results Summary

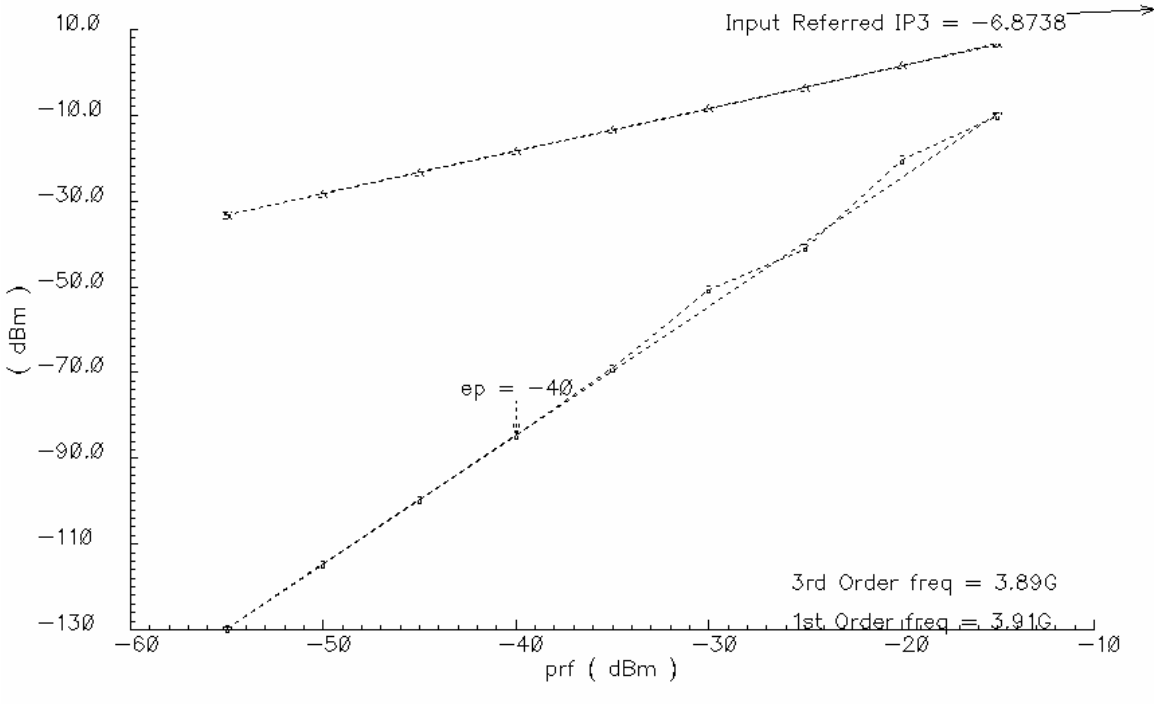
In summary UWB LNA performance can be summarized in Table 3.4

Table 3.4 UWB LNA Simulation Results

Parameter	**Results**
Gain S21(dB)	15.5 (average)
Maximum gain variation (dB)	0.35
Noise figure (dB)	2.5 (average)
Input Rejection S11 (dB)	<-12
IIP3 (dBm)	-6.8
Power consumption (mW)	19.26



a)



b)

Fig. 3.17 a) IIP3 with capacitance as a load b) IIP3 with mixer as a load

CHAPTER IV
MIXERS

Super heterodyne receiver has been the most dominant radio receiver architecture for the last 70 years. Main advantage this architecture offers is that signal at high frequency is down-converted to lower frequency. This means that quality factor (Q) requirements of the band-pass filter is relaxed. Also tuning is made easier since now only LO frequency needs to be changed rather than tuning all the band-pass filters in the receiver. This key function of down-conversion (in receivers) or up-conversion (in transmitters) is performed by mixers. If input frequency is ω_1 and LO frequency is ω_2 then, a mixer will generate difference and sum component of the input frequencies at $\omega_1+\omega_2$ and $|\omega_1-\omega_2|$. Since this is also characteristic of a multiplier, mixers can be considered as multipliers in time domain.

4.1 Mixer Fundamentals

Since linear and time invariant circuits cannot produce outputs with spectral components different from what are present in the input, mixers must be either nonlinear or time variant. As discussed before mixer operation is a multiplication in time domain. To illustrate this point consider mixer model of Fig. 4.1

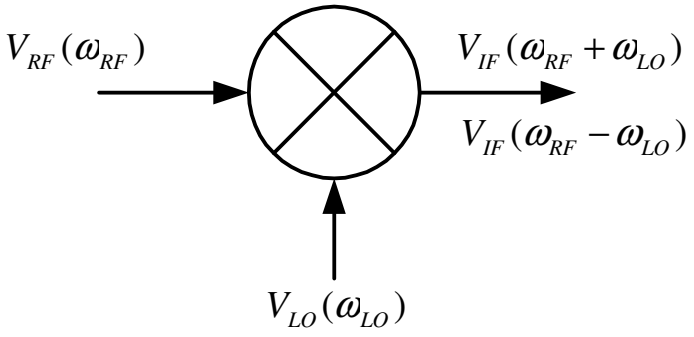


Fig. 4.1 Mixer model

The output of the mixer is given by

$$V_{IF}(t) = A_{RF}\cos(\omega_{RF}t) \times A_{RF}\cos(\omega_{RF}t) = \frac{A_{RF}A_{RF}}{2}\left[\cos(\omega_{RF} - \omega_{LO})t + \cos(\omega_{RF} + \omega_{LO})t\right] \quad (4.1)$$

For down-conversion mixers, $\cos(\omega_{RF} + \omega_{LO})t$ term is filtered out.

4.2 Active vs Passive Mixers

Mixers can be broadly classified as active and passive mixers. As the name suggests, passive mixers do not consume static power whereas active mixers have constant bias currents. Most passive mixers are realized with passive switches driven by the local oscillator. This way, multiplication is realized by each switch commutating the input RF signal. On the other hand, in active mixers, input signal voltage is converted into current by a transconductance stage, which consumes static power. This small signal RF current is either combined with LO signal and passed through non-linear device or sampled at LO frequency.

Passive mixers have the advantage of low static power consumption. However, due to lack of active current, the possible voltage gain attainable from passive mixers is less than unity or in other words, passive mixers provide loss. It can be proven that the theoretical maximum gain of a passive mixer is $2/\pi$. This loss manifests itself in terms of both linearity and noise figure. Due to attenuation, the system behaves linearly for large signals as well. This advantage of linearity is degraded because of non-linear switches in CMOS implementations. Ideally, switches do not contribute to the noise but in practice they contribute cyclostationary noise for small time intervals when they are in active region. Because of the combined effect of this noise contribution and signal attenuation, the noise figures associated with passive mixers are very high. Also, lossy elements in a receiver chain degrade the overall receiver noise figure.

Active mixers on the other hand have clear advantage that they can provide gain to the input signal from RF to IF port. This itself lowers the noise figure of the mixer and overall receiver noise figure. In current commutating architectures of active mixers, the signal swing requirement for LO is much less than that for passive mixers. Main reason

for this is that the node voltages of the switch can be fixed in an active mixer but not in the passive mixers. There exist distinct design trade-off amongst gain, noise, linearity and power consumption in active mixers as compared to passive mixers. In active mixers, although total number of noise contributions might be more than the passive mixers, noise figure is reduced due to higher gain. This is the primary reason why active mixers are used in most of the receiver as achieving high gain in LNA is difficult and mixer needs to have high gain to suppress the noise in the baseband.

4.3 Mixer Metrics

4.3.1 Conversion Gain

Conversion gain is defined as the ratio of the desired IF output to the RF input. This gain can be expressed either in terms of power or voltage such as

$$Voltage\,Conversion\,Gain = \frac{r.m.s.\ voltage\ of\ the\ IF\ signal}{r.m.s.\ voltage\ of\ the\ RF\ signal} \tag{4.2}$$

$$Power\,Conversion\,Gain = \frac{IF\ power\,delivered\,to\,the\,load}{Power\,available\,from\,the\,RF\,source} \tag{4.3}$$

For on-chip implementations usually voltage gain is specified. Active mixers are capable of providing both power and voltage gain, whereas passive mixers (except parametric converter) can only provide voltage gain.

4.3.2 Noise Figure

Noise of a mixer can be expressed in terms of input or output referred noise voltage or power spectral density. Another method is to use a noise metric which is relative to the noise contribution of the source impedance R_S. One such metric is noise figure, which for a mixer is defined as a ratio of signal to noise ratio at the RF port to the signal to noise ratio at the IF port of the mixer. There are two ways to calculate the signal to noise ratio at the output of the mixer based on the type of frequency translation.

4.3.2.1 Double Side Band (DSB) Noise Figure

Consider the diagram of Fig. 4.2. Here the mixer has a gain G, and S_i and N_i are the signal and noise power at the input, respectively. It can be seen that if there is the same signal at two frequency bands centering at RF1 and RF2, both the signal and the noise at these two bands get down converted to the IF. At the output of the mixer, the resulting signal power is $2GS_i$ and noise power is $2GN_i+N_o$ where, N_o is the noise contribution of the mixer.

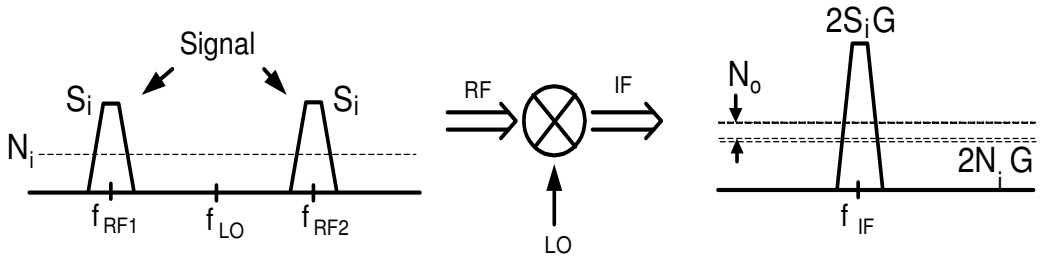


Fig. 4.2 Double side band frequency translation

Resulting noise figure is known as double side band (DSB) noise figure which can be expressed as

$$F_{DSB} = \frac{S_i / N_i}{2GS_i / (2GN_i + N_o)} = 1 + \frac{N_o}{2GN_i} \tag{4.4}$$

4.3.2.2 Single Side Band (SSB) Noise Figure

Now consider the frequency translation of Fig. 4.3. The only difference from the previous case is that there is no signal sideband at RF2. But white noise present at RF2, can get down-converted to IF. Using the same notation as for DSB case, resulting noise figure can be written as

$$F_{SSB} = \frac{S_i / N_i}{GS_i / (2GN_i + N_o)} = 2 + \frac{N_o}{GN_i} = 2F_{DSB} \tag{4.5}$$

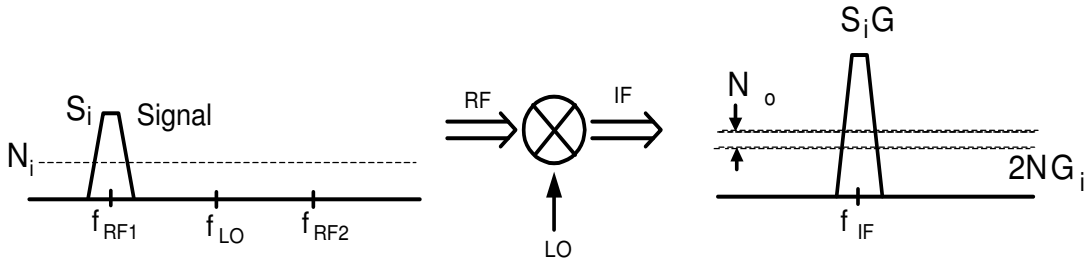


Fig. 4.3 Single side band frequency translation

Thus F_{SSB} is 3dB higher than F_{DSB}. This however is not true when image reject filter is used because the filter reduces the noise component at the image band. Nevertheless, F_{DSB} is greater than F_{SSB}.

4.3.3 Port-to-Port Isolation

Port-to-port isolation is a metric for leakage of signal from one port of the mixer to another. It is defined as the ratio of the signal power available into one port of the mixer to the measured power level of that signal at the one of the other mixer ports assuming 50Ω impedance of each port. The criticality of leakage is different from one port to another. One of the important leakage is the LO to RF leakage which is shown in Fig. 4.4. Since, LO signal is usually much higher in amplitude, it can easily leak to the RF port through substrate and parasitic capacitances of either mixer or the LNA. LO can also leak back to the antenna after leaking from LNA and get transmitted. Another effect of this LO leakage is that it can mix with LO signal inside the mixer and get down converted to DC resulting in a DC offset. This dc offset can saturate the baseband especially the VGA. The worse case can be when this DC offset is time varying.

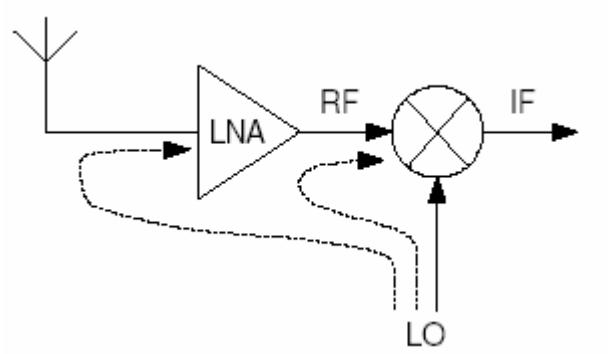


Fig. 4.4 LO to RF leakage

Another important port leakage is from LO to IF. As said before, LO power is much greater than the IF and RF power levels. If LO-IF isolation is poor, high amplitude LO signal can easily saturate the baseband. RF to LO leakage will allow the interferers and spurs present in the RF signal to interact with the LO, which can cause problems in direct conversion architecture due to the low-frequency even-order intermodulation product.

4.3.4 Linearity Metrics

It is interesting to note that mixer is essentially a non-linear device and still its linearity is important. In a real mixer, in addition to the mixing of the RF and the LO tones, their respective harmonics mix with each other producing the additional tones at the output. These additional tones can fall in the IF band and can degrade the signal. This is especially important in wide IF band mixers.

Similar to linearity metrics in RF amplifiers, linearity of the mixer is measured in terms of 1-dB compression point (P_{1dB}), second and third order intercept points (IP2 and IP3), spurious free dynamic range (SFDR) and compression free dynamic range (CFDR).

4.4 Circuit Topologies in Mixers

Mixers are essentially non-linear devices. Historically, a lot of non-linear devices such as electrolytic cells, magnetic ribbons, vacuum tubes, transistors, diodes are used for mixer implementations. These implementations can be either active or passive based on the topology. Also, for the same topology, a mixer can be single balanced or double balanced based on the symmetrical signal component cancellation requirements. Some of these architectures [5] are discussed below.

4.4.1 Diode Mixers

A diode has an exponential I-V characteristic which can be expressed as a power series. Diode mixers make use of this non-linearity to perform frequency translation. Diode mixers come under the category of passive mixers. A single-diode mixer is shown in Fig. 4.5.

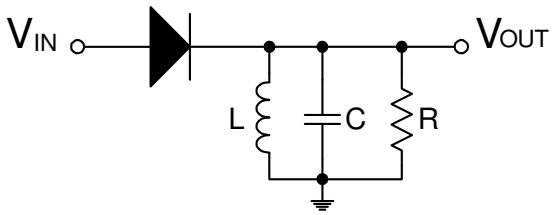


Fig. 4.5 Single diode mixer

Here sum of RF, LO and DC bias is given to the input of a mixer. The LC circuit is tuned to the desired IF frequency to filter out all unwanted frequencies. Single diode mixer has DC term and odd and even harmonics at the output of IF port. This structure has very little LO-IF isolation. To offset this problem, single balanced diode mixers are proposed as shown in Fig. 4.6. It uses two diodes such that only one is active at a time. IF-LO isolation is improved by feeding LO through a transformer. However, since IF port connects to RF when the diodes are ON, IF-RF isolation is still poor.

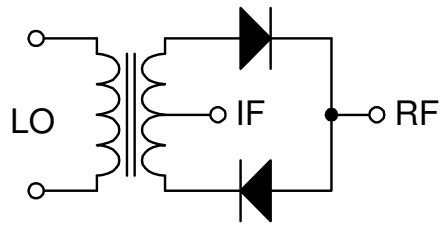


Fig. 4.6 Single balanced diode mixer

In order to solve IF-RF isolation double balanced diode mixer are proposed on the same principles as the single balanced diode mixer. As shown in Fig. 4.7, both LO and RF signals are added using transformers.

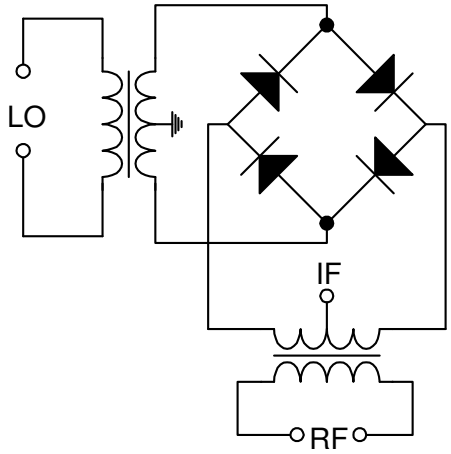


Fig. 4.7 Double balanced diode mixer

4.4.2 Double Balanced CMOS Passive Mixer

As discussed before, a simple switch driven by LO can perform the multiplier action. This can be seen as analogous to the single diode mixer where the input to the switch is a RF voltage while the IF signals is collected at the output. On the same pattern as Fig. 4.7 a double balanced CMOS passive mixer can be implemented as shown in Fig. 4.8.

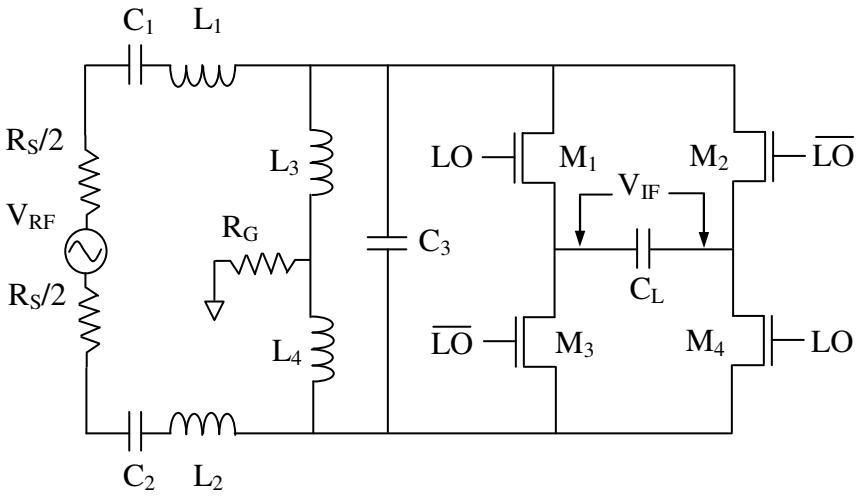


Fig. 4.8 Double balanced CMOS passive mixer

Apart from high noise figure and power conversion loss, other disadvantage of this topology is that output is a strong function of LO. Advantages are zero static power consumption, high linearity and simple implementation.

4.4.3 Square Law Mixers

In diode mixers, RF and LO signals are added and passed through a non-linear (power series transfer function) diode. Using the same concept, RF and LO signals are added and passed to a square law device for example a MOSFET in saturation. The output of a square device contains output at frequencies f_{LO}, $2f_{LO}$, f_{RF}, $2f_{RF}$, $f_{LO}+f_{RF}$ and $|f_{LO}-f_{RF}|$. The difference term is filtered out for down-conversion.

4.4.4 Gilbert Cell Mixers

Gilbert cell is probably the most popular way of implementing active multipliers. A double balanced version of Gilbert cell multiplier is shown in Fig. 4.9.

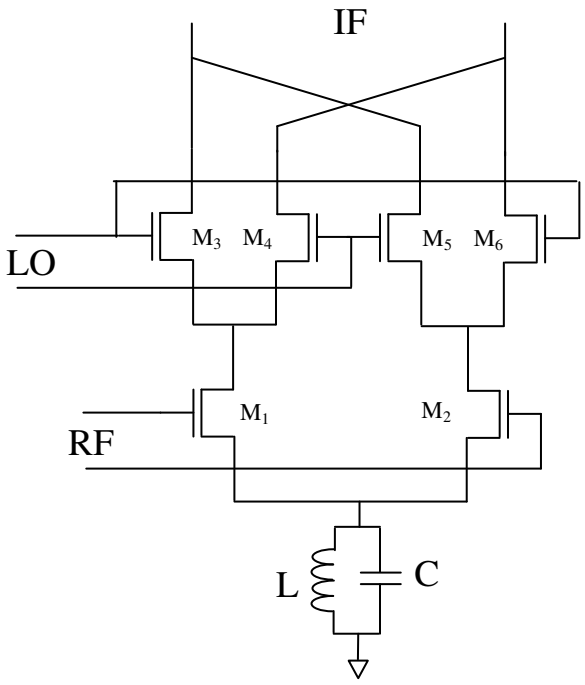


Fig. 4.9 Gilbert cell multiplier

In Gilbert cell multiplier all transistors operate in saturation region. To understand its working principle, consider M_3 and M_4 as a differential pair. The output current of this differential pair is $g_{m3,4}V_{LO}$. The transconductance of M_3 and M_4 is determined by the bias current of the differential pair, which in fact is modulated by the RF signal at the gate of transistor M_1. Thus at the IF output, multiplication of V_{RF} and V_{LO} is obtained. By using double balanced structure, components of LO and RF are subtracted, improving the LO-IF and RF-IF isolation. Since there are active devices in the signal path, the noise figure of a Gilbert cell multiplier is high. Also, the structure is not suitable for low voltage applications. Another main disadvantage is that the output is a strong function of LO voltage.

To offset these problems, LO transistors are made to work as switches by decreasing their overdrive voltage and increasing the LO amplitude. This way, the noise contribution of the switches is negligible and V_{LO} dependence on gain is reduced. This architecture is called as current commutating Gilbert cell mixer. Basically, the transistors

M_1 and M_2 are the transconductance stage which generates RF current signal $g_m V_{RF}$. This current is sampled by a square wave of amplitude V_{LO} which is nothing but multiplying the current by a signum function in time domain as shown below

$$I_{IF} = g_m V_{RF} \cos(\omega_{RF} t)\left[\frac{4}{\pi}\cos(\omega_{LO} t) + \frac{4}{3\pi}\cos(3\omega_{LO} t) + \frac{4}{5\pi}\cos(5\omega_{LO} t) + \ldots\right] \qquad (4.6)$$

Solving this further reveals that the conversion gain is $\frac{2g_m}{\pi}$. It can be seen that RF-IF and LO-IF leakage is theoretically non-existent. Hence, this is a good architecture to pursue or high gain and low noise figures.

4.4.5 Sub-Sampling Mixers

High quality CMOS switches can be used in a sample and hold circuit to act as a sub-sampling mixer. Since the information bandwidth of the modulation is much smaller than the carrier, one can sample at frequencies much smaller than carrier frequency and still satisfy the Nyquist criterion. A subsampling mixer is shown in Fig. 4.10.

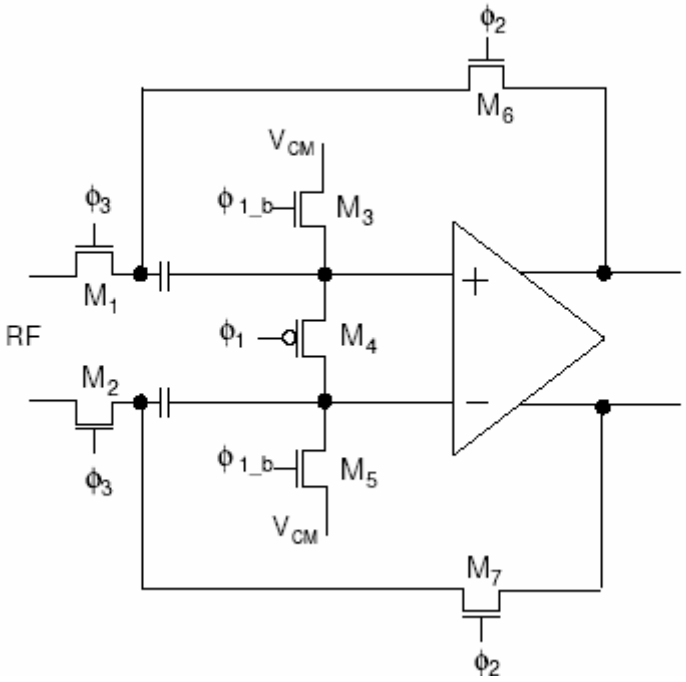


Fig. 4.10 A sub-sampling mixer.

In one half clock cycle input voltage is sampled and stored on the capacitors. On the other half cycle, it is transferred to the output. Although the sub-sampler is clocked at low frequency, it must still possess good time resolution, otherwise sampling errors occur. Sub-sampling performance is limited by the gain-bandwidth product of the operational amplifier. Another problem is the noise boost because sampled input noise at the input undergoes folding. This disadvantage offsets the advantage of high linearity of these mixers.

CHAPTER V
ULTRA WIDEBAND MIXER

5.1 Requirements of a UWB Mixer

If parasitic effects of internal nodes are ignored, mixers can be considered as broadband systems. Here, by broadband, it is meant that if LO frequency is varied over the whole band of interest, the resulting frequency characteristic of IF signal should be same throughout the band. In reality, there are parasitic capacitances associated with internal nodes, which at high frequencies become a dominant factor. In our case, the whole band of interest (3.168-4.752GHz) is divided into three 528MHz bandwidth sub-bands. Each sub-band is down-converted into IF band of 528MHz bandwidth by LO, which switches between 3.432, 3.96 and 4.488GHz. The frequency response of conversion gain for resulting three IF bands depends on two things. One is the loss of high frequency RF signal before switching due to internal parasitic capacitances. Other is the loss at the output of the mixer due to parasitic capacitance at that node. While designing a broadband mixer, the main objective is to minimize the conversion gain variation in each IF band due to both factors. Overall maximum variation in conversion gain in all IF bands combined should be less than 1dB.

Table 5.1 UWB Mixer Specifications

Parameter	**Specification**
Conversion Gain (dB)	10
Maximum gain variation (dB)	1
RF Frequency range (GHz)	3.168-4.752
LO Frequencies (GHz)	3.432, 3.96, 4.488
Noise Figure (dB)	<9.3
IIP3 (dBm)	>-7

Next main concern is the noise performance over the whole band. Being a broadband circuit, both 1/f noise and thermal noise contributions are important. For the given receiver architecture, the first two channels (each 4.125 MHz wide) are not used. Although this relaxes the 1/f noise figure requirement a little bit, corner frequency of the noise still needs to be low. Another main concern is the I-Q mismatch. For the given UWB receiver, two mixers are needed for each I and Q channels. Matching between I and Q channels affects the errors in demodulation. Hence I and Q channels mismatch needs to be reduced. Linearity requirement of the mixers is more stringent than for the LNA since the signals strength at the mixer input after being amplified is much higher than in case of the LNA. This is even more important because all the modulation and intermodulation product of interferer can easily get down-converted and appear in a 528 MHz wideband. Required specifications for UWB receiver are summarized in Table 5.1.

5.2 Previous Work

Most of the broadband mixers that have been reported in the literature are for microwave applications and very few are CMOS implementations. A micro strip mixer based on impedance mismatch concept has been reported in [18]. It is a broadband down-conversion mixer for RF frequencies 3.5-10.5GHz. Mixing operation is based on non-linear behavior of schottky barrier diode and the broadband matching is attained by the use of a micro strip hybrid tee. Although the attained noise figure of this structure is good (~6.5dB), insertion loss associated with it makes it inappropriate for the UWB application. Above all, this technique if implemented in silicon may not achieve good results in present day IC technology because of the lossy substrate. Another broadband mixer operating in 0.9 – 2.6GHz frequency range is presented in [19]. It uses double balanced diode mixers implementation in 0.3µm GaAs technology. Being a passive mixer, it has poor noise figure and conversion gain. Distributed amplification, as discussed in section 3.1, is used to extend the bandwidth of an amplifier. The same technique has been used in case of mixers as well [20]. FETs used for this purpose are dual gate FETs where each gate is connected to LO and RF port. Achievable band of

operation in this mixer is 2-18GHz. Disadvantage of this technique is higher noise figures and low conversion gain. In [21], a BiCMOS broadband mixer for 0.9 – 2.2GHz frequencies is presented. This topology is a variant of Gilbert cell mixer where input transconductors are operated in triode region to improve linearity. However, since transistors in triode region introduce more noise than in saturation, noise figures of such architectures are usually poor. A multi-gigahertz mixer implemented in 0.5µm CMOS has been reported [22]. In this architecture, RF and LO signals are applied at the front and back gates of a MOS transistor respectively. Output current is thus modulated by LO hence mixing action is attained. This technique achieves high conversion gain and uses low voltage supplies. However, its disadvantages are poor RF-LO isolation, high noise figure and high dependence of gain on LO. Comparative performance of above topologies is tabulated in Table 5.2.

Table 5.2 Mixer Previous Work

Author	**Freq (GHz)**	**CG**	**NF**	**IIP3**	**Supply**	**Technology**	**Technique**
[18]	3.5-10.5	*	6.5	*	*	Micro strip	Passive Diode mixer
[19]	0.9-2.6	*	*	*	*	0.3um GaAs	Double balanced diode mixer
[20]	2-18	0	*	*	*	0.5um GaAs	Distributed Mixer
[21]	0.9-2.2	9	*	18	3.6V	BiCMOS	Gilbert cell with transconductor in triode region
[22]	2-10	6	9.6-18	10	1V	0.5um CMOS	Dual Gate Mixer

The mixer presented in this thesis is based on current commutating Gilbert cell architecture. Broadband characteristics are attained by using an LC bandpass filter. Besides improving the bandwidth, it improves both the conversion gain and noise figure of the mixer.

5.3 Proposed UWB Mixer

Since the amount of gain achievable in the wideband LNA discussed before is limited, in order to suppress the noise degradation in base-band, conversion gain and noise figure specifications of the mixer are stringent. As discussed before, current commutating Gilbert cell mixer can achieve high conversion gain and noise figure. This is done by increasing the size of switches, reducing the bias current through switches and increasing the load. All of these steps lead to narrowing the bandwidth of the mixer. Hence a new topology is proposed which attempts attain high gain, low noise without compromising on the bandwidth. The schematic of the proposed scheme is shown in Fig. 5.1. Here it can be seen that both I and Q channel mixers are merged together by combining their transconductance stage. The main advantage of merged mixer is illustrated in Fig. 5.2. Comparing the signals at the common sources of switches for both cases of separate I-Q mixers and merged I-Q mixers, it can be seen that the waveform for merged case is one tenth in magnitude and twice the frequency of the waveform in separate mixer case. This means that LO leakage to RF is smaller and thus not of main concern. Also, being at higher frequency any leakage of this signal to IF port due to mismatch in switches will be attenuated more by the low pass filter than in the case of separate I-Q mixers.

Another feature of this structure is the use of current bleeding technique, where the amount of bias current in the switches is reduced by injecting current at the common source node of the switches. As explained in section 5.3.1, it helps in achieving both lower noise figure and higher conversion gain as compared to Gilbert cell mixer. Transistors M_3 are used to inject required bleeding current. In addition, the same transistors M_3 are reused to increase the effective input transconductance by connecting them to input. This helps in lowering its noise figure and increases the overall conversion gain.

The main disadvantage of the current bleeding technique is the increased parasitic capacitance at the switch common source node. This issue is solved by introducing a L-R series network at this node such that the overall impedance at this

node has a band- pass characteristic. In other words, parasitic capacitance is cancelled by the inductor in the pass-band. As discussed next, in addition to conditioning the conversion gain, it also helps in improving the noise figure and linearity of the mixer.

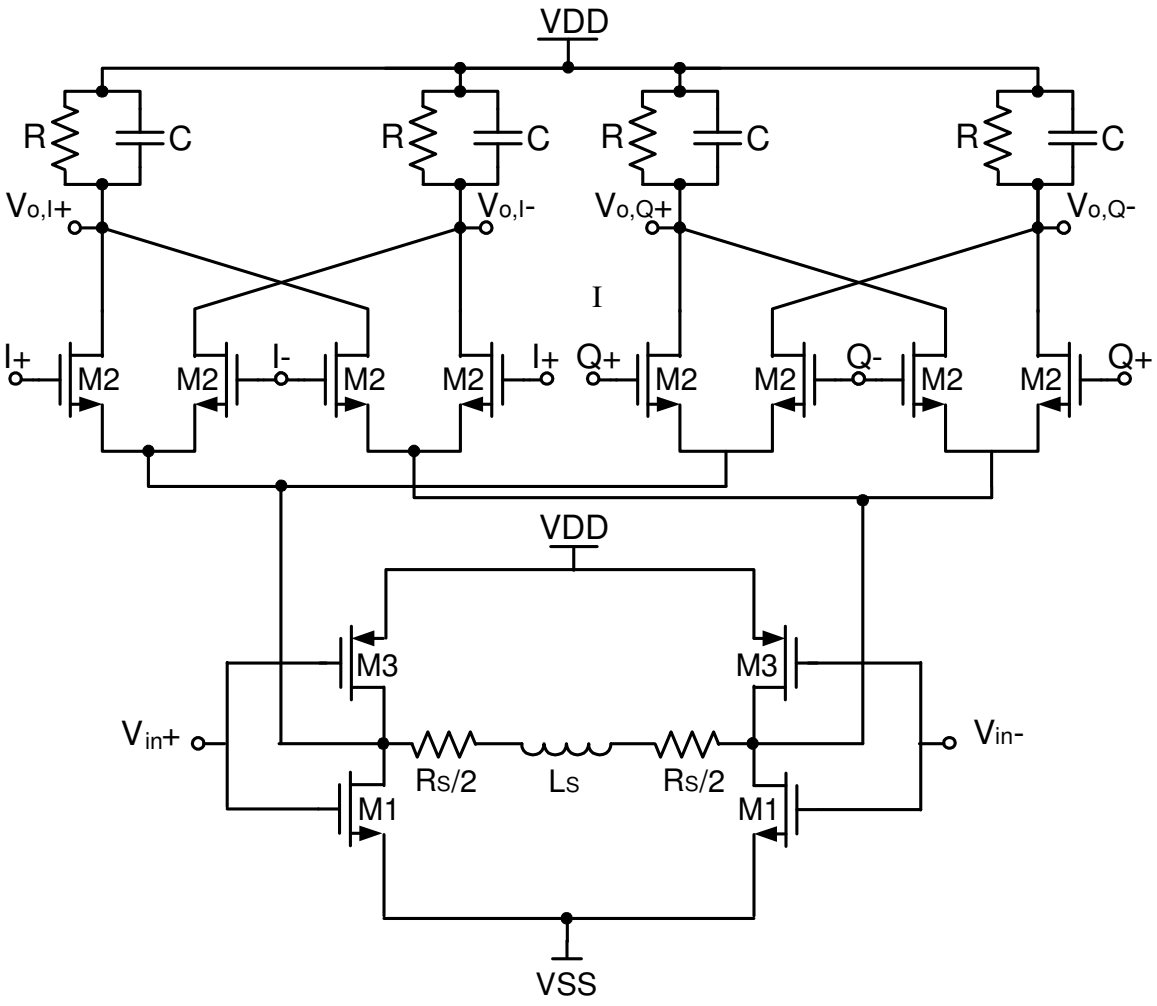


Fig. 5.1 Proposed UWB mixer

In order to improve the linearity of the transconductors, the tail currents of differential input stage are removed. This also helps in improving the voltage headroom. Its disadvantage is the degraded CMRR and PSRR, which can be reduced by reducing the mismatch in the transconductors by proper layout techniques.

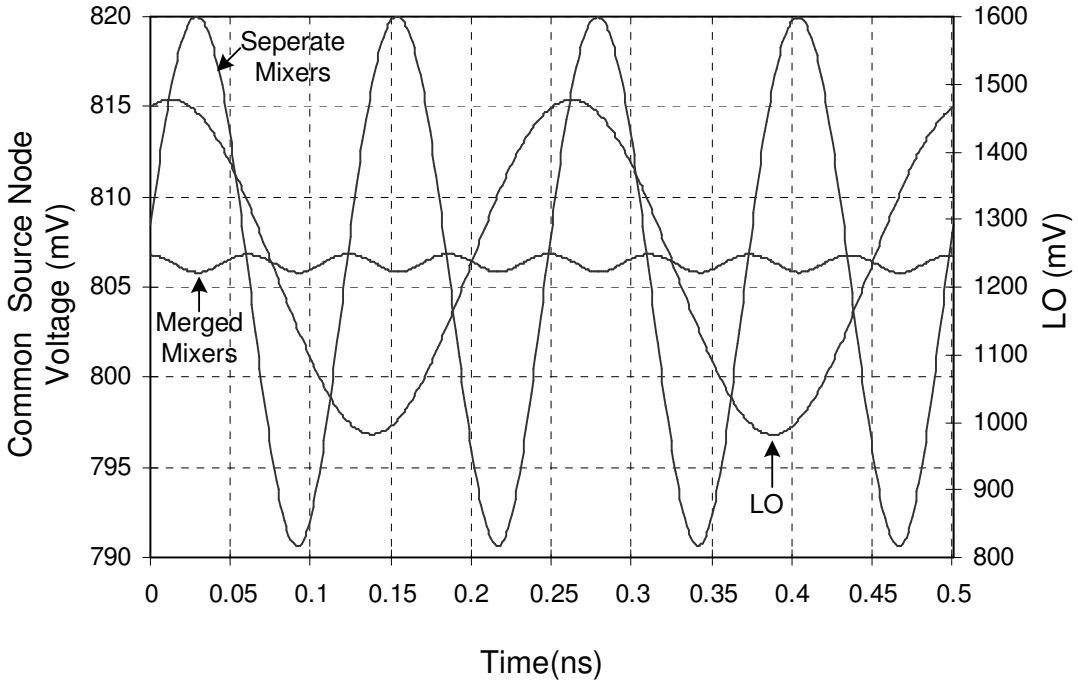


Fig. 5.2 Voltage waveform at common source node of switches

5.3.1 Current Bleeding Technique

As discussed later in section 5.5.2, it can be noticed that direct switch noise is proportional to the amount of bias current flowing through the switches. Hence, reducing the bias current in the switches results in a lower direct switch noise. However, in Gilbert cell mixer, reducing the bias current in switches inevitably reduces the bias current through the transconductance transistors as well. This puts a limitation on the maximum attainable transconductance. This is even more restricted under the constraints of linearity and power consumption requirements. In order to simultaneously improve noise figure and conversion gain, extra current required for the transconductor stage is injected at the common source of switches as shown in Fig. 5.3. This methodology is known as current bleeding technique [23]. Besides the lower noise, value of load resistance R can be increased since voltage drop across them is lower with lower bias current through them. This helps in achieving higher conversion gain. Additional

improvement in noise and conversion gain comes from the fact that lower bias current decrease the overdrive of the switches for the same transistor size

On the downside, added current sources to inject bleeding current increase the parasitic capacitance at the node of injection. If the amount of current through the switches is small, g_m of the switching transistors decreases. This increases the effective resistance at the source of switches reducing the parasitic pole location at this node, thereby decreasing the amount of current going to switches. Thus the dominant parasitic pole lowers conversion gain and induces 20dB per decade roll-off in the conversion gain hence making it inappropriate for broadband applications. Therefore the optimum bias current and switch sizes are determined by optimizing bandwidth, noise and conversion gain tradeoffs.

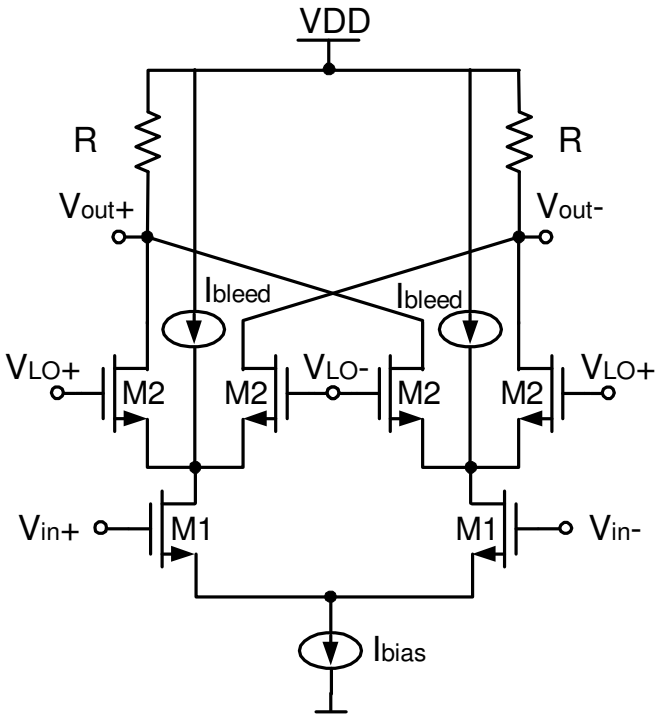


Fig. 5.3 Current bleeding technique in current commutating mixers

5.3.2 Wideband Technique

As discussed before, the main requirement for a wideband mixer is to maintain the same conversion gain and noise figure for all the RF input frequencies in the band of interest. Assuming that switch performance does not degrade with frequency, wideband mixer can be realized if the frequency degradation of transconductor output current is restricted. In reality, due to parasitic capacitances at common source nodes of a Gilbert cell mixer, the amount of RF small signal current injected into the mixer degrades at higher frequencies. This degradation in current is reflected in a 20dB/decade drop in the conversion gain. Overall conversion gain with parasitic capacitance is given as

$$CG = \frac{2}{\pi} g_{m,trans} R \frac{n\, g_{m,SW}}{n\, g_{m,SW} + sC_{par}} \tag{5.1}$$

where $g_{m,trans}$ is the transconductance of input transistors, C_{par} is the net capacitance at the common switch source node, $g_{m,SW}$ is the transconductance of the switches and n is the number of transistor switches at each node. In order to maintain the same conversion gain over the whole pass-band, an R-L series network is embedded in the mixer as shown in Fig. 5.4. Fraction of the RF current passing through switches can be derived from the

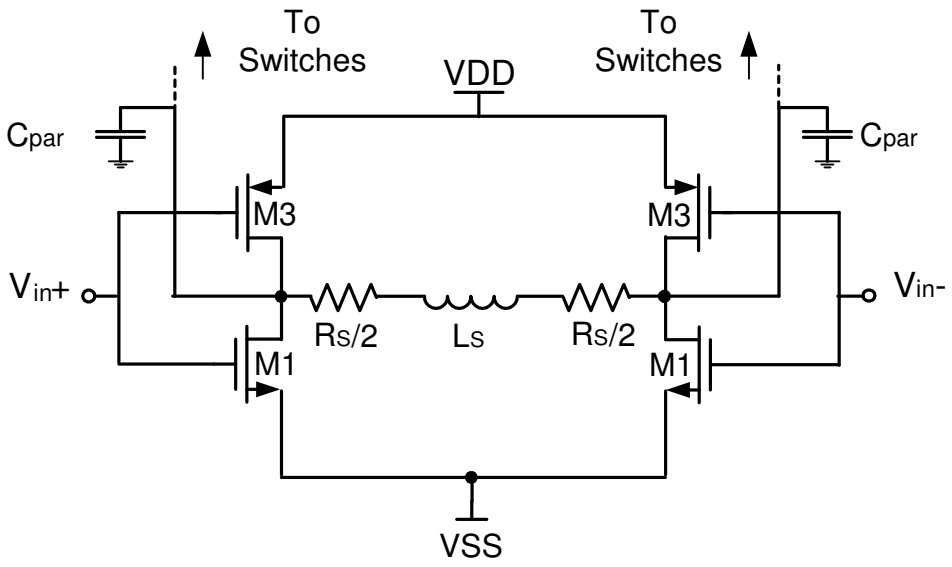


Fig. 5.4 R-L series network for wideband operation

small signal model as shown in Fig. 5.5. This modifies the conversion gain of the mixer as

$$CG = \frac{2}{\pi} g_{m,trans} R \frac{n\, g_{m,SW} (R + sL_s)}{s^2 L_s C_{par} + s(n\, g_m L_s + C_{par} R_s) + (n g_m R_s + 2)} \tag{5.2}$$

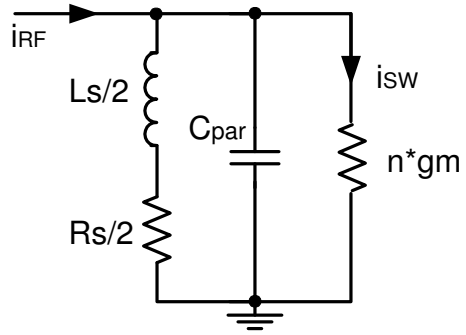


Fig. 5.5 Small signal model for Fig. 5.4

Intuitively, this can be considered as a band-pass function with centre frequency and bandwidth given as

$$\omega_o \approx \sqrt{\frac{g_m R_s + 1}{L_s C_{par}}} \tag{5.3}$$

$$BW \approx \frac{g_m}{C_{par}} + \frac{R_s}{L_s} \tag{5.4}$$

It can be seen that addition of Rs helps in widening the bandwidth and giving an extra freedom for controlling the conversion gain.

5.4 Conversion Gain of a Current Commuting Gilbert Cell Mixer

5.4.1 Ideal Case

Conceptual schematic of a current commuting active mixer can be shown in Fig. 5.6. The LO signal is assumed to be an ideal square wave and the switches are considered asideal. Because of the commuting action of the switches, output current can be seen as sampling of input current i_{RF} by a square wave. This can be represented as

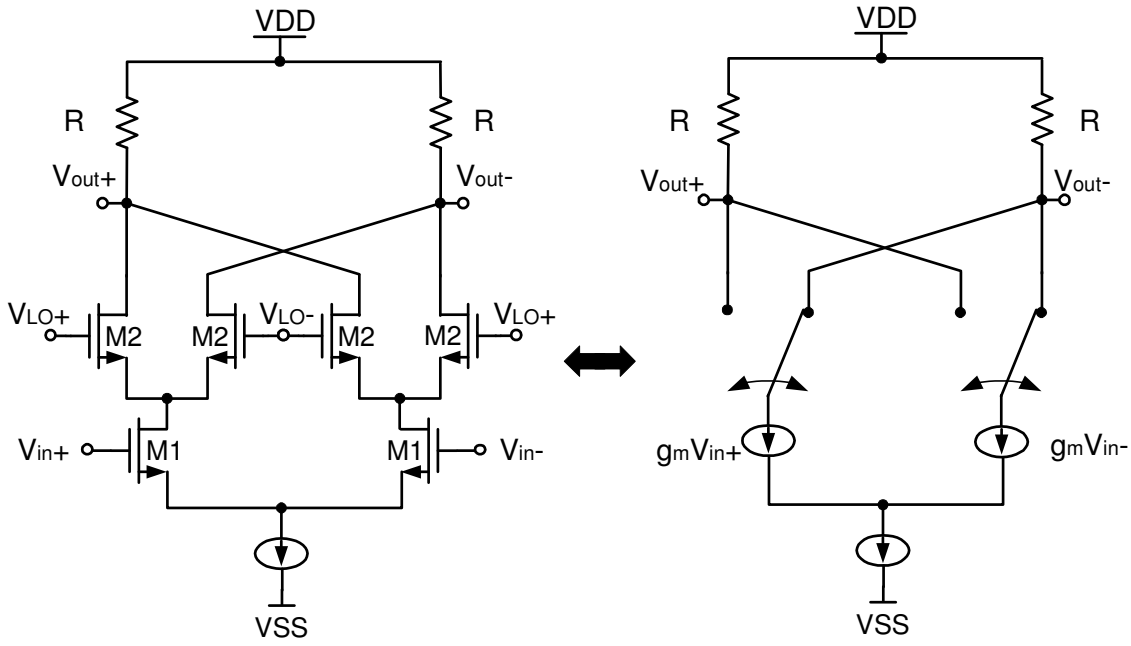


Fig. 5.6 Conceptual schematic of current commutating mixer

$$i_{LO}(t) = i_{RF}(t)\, p(t) \tag{5.5}$$

where p(t) is a pulse train of magnitude unity and frequency $\omega_{LO,}$ and $i_{RF}(t)$ is an input RF current given by

$$i_{RF}(t) = i_{RF} \sin(\omega_{RF}) \tag{5.6}$$

pulse p(t) can be written in terms of its Fourier series as [24]

$$p(t) = \frac{4}{k\pi} \sum_{k=1}^{\infty} \sin\left(\frac{k\pi}{2}\right) \cos(k\omega_{LO} t) \tag{5.7}$$

Substituting (5.2) and (5.3) into above equation gives

$$i_{IF} = \frac{4}{k\pi} i_{RF} \cos(\omega_{RF} t) \left(\sum_{k=1}^{\infty} \sin\left(\frac{k\pi}{2}\right) \cos(k\omega_{LO} t) \right) \tag{5.8}$$

Equation (5.8) consists of intermodulation products of RF signal with all the fourier components of the pulse train. Considering only the significant components, (5.8) can be further simplified as

$$i_{IF} = \frac{4}{\pi} i_{RF} \left(\frac{1}{2} \left[\cos((\omega_{LO} - \omega_{RF})t) + \cos((\omega_{LO} + \omega_{RF})t) \right] \right) - \frac{4}{3\pi} i_{RF} \left(\frac{1}{2} \left[\cos((3\omega_{LO} - \omega_{RF})t) + \cos((3\omega_{LO} + \omega_{RF})t) \right] \right) \ldots \quad (5.9)$$

For the down conversion mixers, the difference component in the first term of (5.9) is important. If i_{RF} is equal to $g_m V_{RF}$, (5.9) can be simplified as

$$i_{IF} = \frac{2}{\pi} g_m V_{RF} \cos((\omega_{LO} - \omega_{RF})t) \quad (5.10)$$

If the load resistance is R_L, output voltage is

$$V_{IF} = \left(\frac{2}{\pi} g_m R \right) V_{RF} \cos((\omega_{LO} - \omega_{RF})t) \quad (5.11)$$

Hence the conversion gain of the idealized mixer is

$$A_{CG} = \frac{2}{\pi} g_m R \quad (5.12)$$

5.4.2 Non Ideal Case

In real world, neither the switches are ideal nor the LO signal is a perfect square wave. LO signal in reality is a sine wave of large amplitude, such that current commutation still takes place. In such a case, there is a finite time where RF signal flows through both switches. Under such circumstances, it is a common mode signal at the output of mixer and the gain is low. This situation is called as the balanced state of a mixer which can be seen in Fig. 5.7, where $2t_{Bal}$ is the time for which the mixer goes into the balanced state and $(V_{GS}\text{-}V_T)_{SW}$ is the switch overdrive. The input current can be considered to be sampled by a non ideal pulse train p(t) of finite rise time as can be seen in the figure. Mathematically, p(t) is given as [24]

$$p(t) = \frac{8}{x\pi^2} \sum_{k=1}^{\infty} \frac{1}{k^2} \left[\sin\left(\frac{k\pi}{2} \right) \sin\left(\frac{k\pi}{2} x \right) \right] \cos(k\omega_{LO} t) \quad (5.13)$$

where x is defined as

$$x = \frac{4t_{Bal}}{T_{LO}} \quad (5.14)$$

Using the same analysis as before, the output voltage can be derived as [24]

$$V_{IF}(t) = \frac{8 g_m R}{x\pi^2} V_{RF} \sum_{k=1}^{\infty} \frac{1}{k^2} \left[\sin\left(\frac{k\pi}{2}\right) \sin\left(\frac{k\pi}{2} x\right) \right] \cos(k\omega_{LO} t)\ \cos(\omega_{RF} t) \qquad (5.15)$$

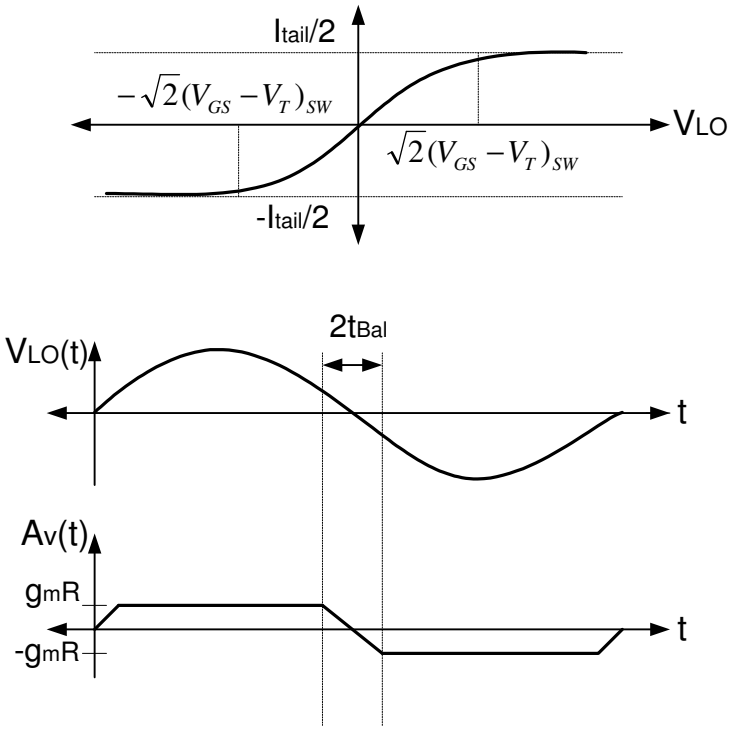


Fig. 5.7 Switching action in a differential pair with a sinusoidal LO signal

Conversion gain can be calculated by setting k=1 in the above equation as

$$A_{CG} = \frac{4 g_m R}{\pi^2 x} \sin\left(\frac{\pi}{2} x\right) \qquad (5.16)$$

It can be seen that (5.16) transforms into (5.12) for x approaching 0. Intuitively, the higher the switching transition time, the lower is the conversion gain.

In a differential pair, if the differential voltage at the gate of input transistors is greater than $\sqrt{2}(V_{gs}-V_T)_{SW}$, then one transistor will be conducting all of the tail current whereas the other transistor will go into the cut-off region. Hence t_{Bal} can be derived as the time when such condition occurs i.e.

$$V_{LO}(t_{Bal}) = V_{LO}\sin(\omega_{LO} t_{Bal}) = \sqrt{2}(V_{gs} - V_T)_{SW} \tag{5.17}$$

Assuming t_{Bal} to be very small as compared to time period T_{LO} of the LO signal, it can be approximated as

$$t_{Bal} = \frac{\sqrt{2}(V_{GS} - V_T)_{SW} T_{LO}}{2\pi V_{LO}} \tag{5.18}$$

which, when substituted in (5.14) gives

$$x = \frac{2\sqrt{2}(V_{GS} - V_T)_{SW}}{\pi V_{LO}} \tag{5.19}$$

Conversion gain of the mixer can be derived by substituting x from (5.19) in (5.16). The final expression is given by

$$A_{CG} = \frac{\sqrt{2}\, g_m R V_{LO}}{\pi (V_{GS} - V_T)_{SW}} \sin\left(\frac{\sqrt{2}(V_{GS} - V_T)_{SW}}{V_{LO}} \right) \tag{5.20}$$

By examining (5.20) carefully, it can be seen that the conversion gain is a function of the ratio of switch overdrive voltage and the LO signal amplitude. From the design point of view, this ratio has to be very small such that (5.20) can be approximated as (5.12). This can be done either by increasing the LO amplitude or lowering the overdrive of the switches. While LO amplitude is limited by the power consumption constraint, the sizes of switches are determined by both the noise and conversion gain requirements.

5.5 Noise Analysis of a Current Commutating Gilbert Cell Mixer

Main contributions to the noise of the current commutating mixer can be divided into three categories as noise from the transconductance stage, noise from the switching pair and noise from the load.

5.5.1 Noise Contribution by Transconductance Stage

Both flicker noise and thermal noise contributions of the transconductance stage can be considered as an input voltage $V_{n,i,trans}$ for the purpose of analysis. This noise voltage can be treated mathematically in the same way as the RF input signal. This noise

passes through the switches and undergoes frequency translation. In the time domain, output noise spectrum is a cyclostationary random process described by

$$i_{n,o,trans} = p(t)\, V_{n,i,trans} \tag{5.21}$$

In frequency domain, due to wide spectrum of the pulse train p(t), white noise appears as several copies of it in a wide spectrum. As is shown in Fig. 5.8, the white noise spectrum produced by the transconductance stage convolves with different harmonics of the LO signal. Mathematically, (5.21) can be expressed in frequency domain as

$$S_{n,o,trans}(\omega) = \sum_{k=1}^{\infty} |p_k|^2 . S_{n,i,trans}(\omega - k\,\omega_{LO}) \tag{5.22}$$

where $S_{n,trans,in}$ has both white noise and flicker noise components.

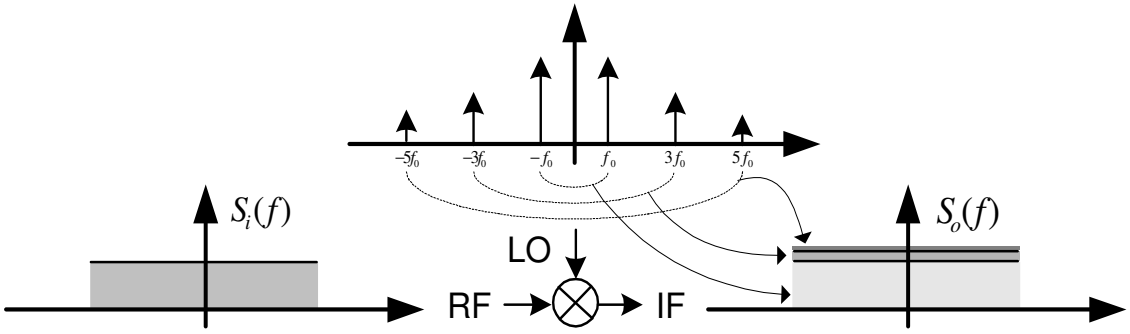


Fig. 5.8 Input transconductance noise spectrum translation by LO harmonics

After rigorous analysis [24], (5.22) can be rewritten as

$$S_{n,o,trans}(\omega) = S_{n,i,trans}(\omega)\, \xi\, A_{CG}{}^2 \tag{5.23}$$

where

$$\xi = \sum_{k=1}^{\infty} \left[\frac{\frac{1}{k^2} \sin\left(k\frac{\pi}{2}\right) \sin\left(\frac{k\sqrt{2}\,(V_{GS}-V_T)_{SW}}{V_{LO}}\right)}{\sin\left(\frac{\sqrt{2}\,(V_{GS}-V_T)_{SW}}{V_{LO}}\right)} \right]^2 \tag{5.24}$$

Equation 5.24 reveals its dependence on the ratio of switch overdrive voltage to the LO signal amplitude. Number of harmonics produced by a large amplitude LO signal is

higher. This means that output spectrum will contain many copies of input transconductance noise. Fig. 5.9 shows the variation of ζ as a function of $(V_{GS}-V_T/V_{LO})$ for different values of k.

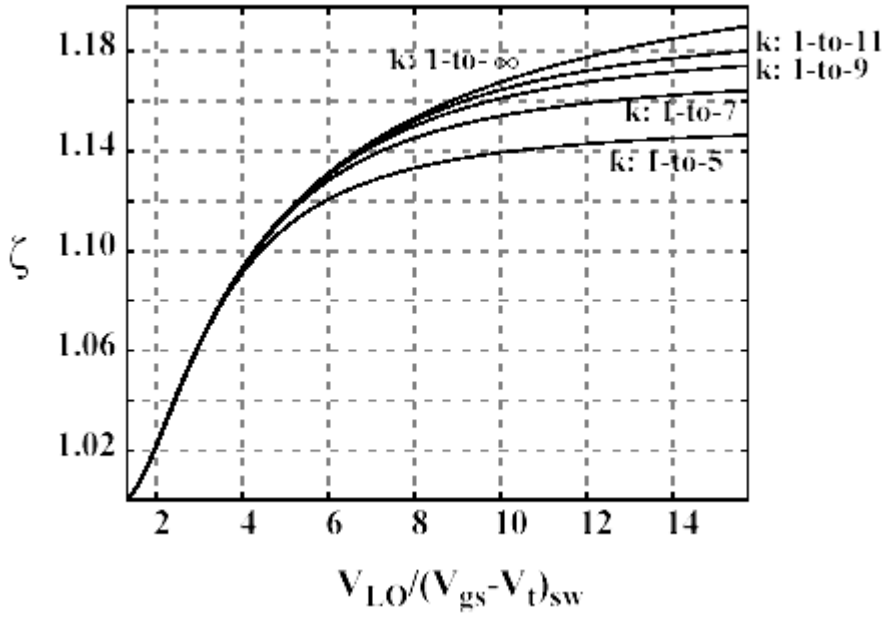


Fig. 5.9 Variation of ζ with $(V_{GS}-V_T)_{SW}/ V_{LO}$

Number of harmonics (k) which should be summed in (5.24) is dependent on the LO frequency and the bandwidth of the switches. As a rule of thumb, ratio of bandwidth of switches to LO frequency gives a good approximation for k. In most cases k is less than 10.

5.5.2 Switch Noise

Noise of switches is one of the most important noise contributors in current commutating mixers. This becomes critical in direct conversion receivers because of high flicker noise at low IF frequencies. Noise contribution of switches is divided into two subparts – direct and indirect switch noise.

5.5.2.1 Direct Switch Noise

5.5.2.1.1 Direct Switch Noise (High Frequency)

Consider a conceptual schematic of current commutating mixer of Fig. 5.6. When the mixer switches are ideal, only one of them is ON at a time. This means that noise contribution of the OFF switch is zero at that instant. Also, the mixer now behaves as a cascode amplifier with ON switch acting as a cascode transistor. Assuming that the parasitic capacitances at the source of switches are negligible, the noise contribution of this ON switch is zero. However, because of the finite time it takes for a real switch to turn ON or OFF, there is a small time interval where both the switches are ON. During this time period, the mixer acts as a differential amplifier with both switches contributing to the noise. This noise contribution is called as direct switch noise. It can be modeled as sampling of mixer input noise by a pulse train s(t) as shown in Fig. 5.10. Mathematically, output noise current can be represented as

$$\overline{i_{n,o,sw}} = s(t).\overline{v_{n,sw}} \tag{5.25}$$

In frequency domain, (5.25) can be written as

$$S_{n,o,direct}(f) = \sum_{k=-\infty}^{\infty} \left|s_k\right|^2 . S_{n,sw}(f - kf_{LO}) = \overline{v_{n,sw}}^2 \sum_{k=1}^{\infty} \left|s_k\right|^2 \tag{5.26}$$

which after mathematical simplification lead to

$$S_{n,o,direct}(f) = \frac{2I_{SW}{}^2 \overline{v_{n,sw}}^2}{\pi^2 V_{LO}{}^2} \left[1 + 4\left(\frac{V_{LO}}{(V_{GS} - V_T)_{SW}} \right)^4 \sum_{k=1}^{\infty} \left| \frac{\cos\left(k\frac{\pi}{2}\right)}{(k\pi)^2} \left(1 - \cos\left(\frac{k\pi}{\sqrt{2}} \frac{(V_{GS} - V_T)_{SW}}{V_{LO}} \right) \right) \right|^2 \right] \tag{5.27}$$

Inspection of (5.27) shows the dependence of direct switch noise with the LO amplitude. Second term in this equation is in fact dependent on fourth power of this ratio. It can be seen that the noise contribution decreases significantly with increase in ratio of LO amplitude to the switch overdrive. Another important observation from (5.27) is that the direct switch noise is directly proportional to the amount of bias current flowing through the switches. This is a major limitation in Gilbert cell architecture as reducing bias current in the switches decreases the bias current in the transconductor stage, implying

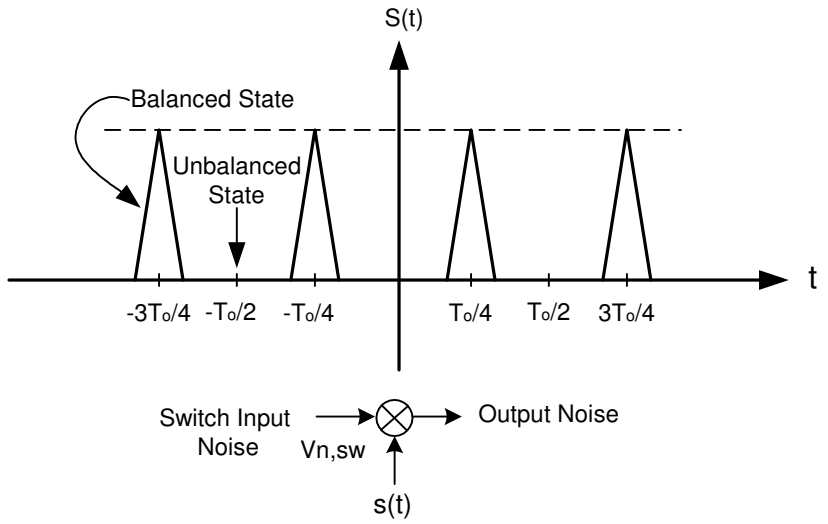


Fig. 5.10 Noise voltage transfer function from LO port to the mixer output

reduced conversion gain. By using current-bleeding architecture, amount of bias current flowing in the switches is reduced thus reducing the direct switch noise, without reducing the current flowing in the transconductors.

5.4.2.1.2 Direct Switch Noise (Low Frequency)

Treatment for low frequency direct switch noise is different from high frequency direct switch noise. Low frequency switch noise can be considered as a slow changing voltage offset at the gate of the mixer switches. For the purpose of simplicity we can assume perfect switches. This is a reasonable assumption because for low frequency noise, it is the zero crossings which are more important than the time the mixer is in the balanced state. Let us consider the waveforms shown in Fig. 5.11. Noise v_n is a slow varying voltage signal being sampled by a sinusoidal LO. The resulting output current will resemble a pulse width modulated signal as shown in the figure. Without the noise it will be an ideal square wave, but the noise voltage v_n on the gates of switches behaves as a DC offset, modulating the zero crossing of the LO. This results in a pulse width modulated signal of amplitude equal to the tail current I_{SW}. This signal can be represented as superposition of a periodic square wave of frequency ω_{LO} of amplitude

I_{SW} and random noise pulses of magnitude I_{SW} and width Δt, as shown in Fig. 5.11. Δt can be written as

$$\Delta t = \frac{V_n(t)}{S} \tag{5.28}$$

where S is the slope of LO signal at its zero crossings. For a sinusoidal LO, S is given by

$$S = \frac{d}{dt} V_{LO} \sin(\omega_{LO} t)\Big|_{t=0} = V_{LO}\omega_{LO} \tag{5.29}$$

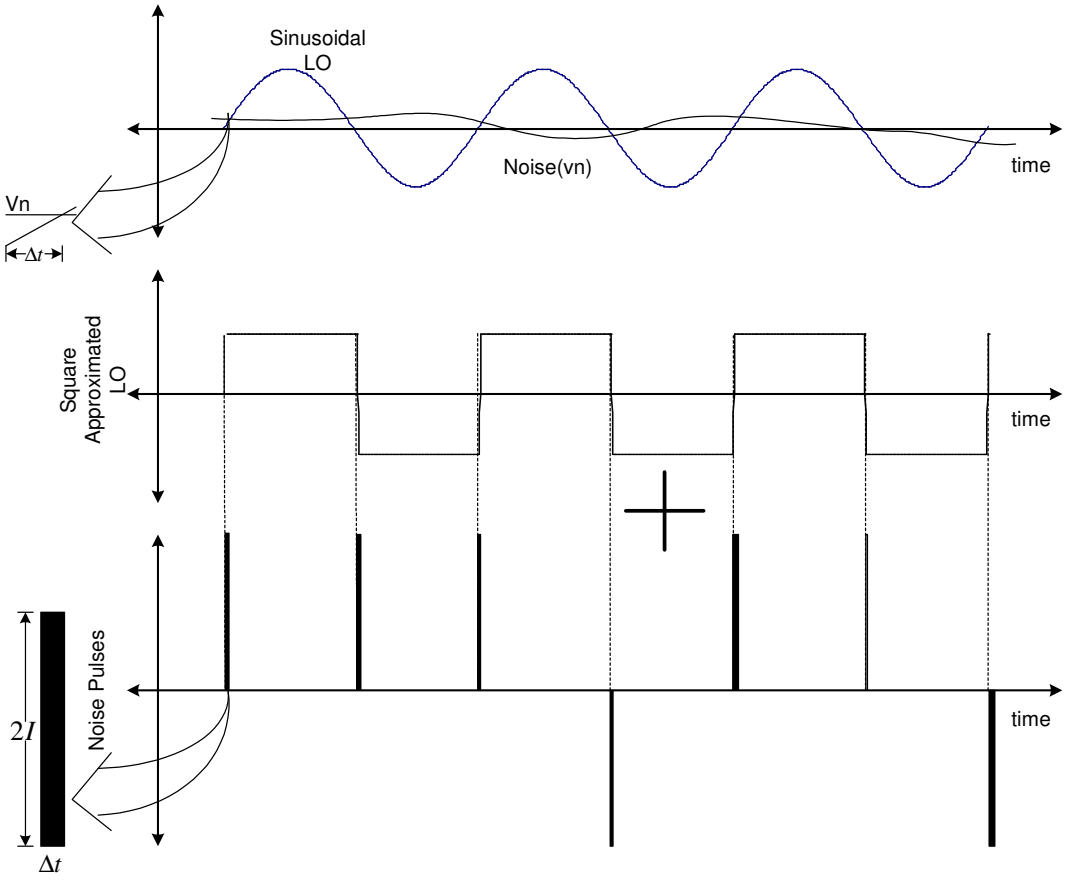


Fig. 5.11 Switch input voltage and output noise current

Taking average of the output current pulses in one period of LO leads to

$$i_{n,o} = \frac{2 \cdot 2I_{SW} \cdot \Delta t}{T} = 4I_{SW}\frac{V_n(t)}{S \cdot T} \tag{5.30}$$

When the width of pulses is much smaller than LO time period T, the output current pulses can be represented as impulses. In the frequency domain, it means that the noise spectrum will be observed in baseband and around multiples of $2\omega_{LO}$. Mathematically [25], output noise current is given as

$$S_{n,o,direct} = \overline{\left(4I_{SW}\frac{V_n(f)}{S\cdot T}\right)^2} = \left(\frac{I_{SW}}{\pi V_{LO}}\right)^2 \overline{V_n{}^2(f)} \tag{5.31}$$

Here, V_n represents differential noise and S is given by $2V_{LO}\omega_{LO}$.

5.4.2.2 Indirect Switch Noise

As it is seen in the direct noise, with increase in the LO amplitude, the time window in which both switches are ON decreases. This helps to increase conversion gain as well as minimize the direct switch noise. However, when LO amplitude is very large as compared to the overdrive of switches, indirect noise mechanism of switches becomes significant. This can happen only in the presence of parasitic capacitance at the source of switches. For simplicity of analysis, let us consider a current commutating single balanced mixer as shown in Fig. 5.12. When only one switch is ON, the mixer behaves as a source follower for the signal at its gate. Consider the noise voltage Vn of switch M_1. This noise voltage appears at the tail current node as $V_s(t)$ during the time interval when M_1 is ON. This is shown as square wave of amplitude V_n and frequency ω_{LO} in Fig. 5.12. Due to the presence of C_p at the tail current node, the voltage Vs has exponential rising and falling edges with time constant $C_{gs}/g_{m,sw}$. This is due to charging and discharging of C_p. The transient noise current in C_p at twice the LO frequency appears at the output due to the commutating action of the switches. Average output noise current over half the LO time period as given by [25]

$$i_{n,o} = \frac{2}{T}\int_0^{T/2} i_{CP}(t)dt = \frac{2}{T}\int_0^{T/2} C_p\left[\frac{d}{dt}V_s(t)\right]dt = \frac{2}{T}C_pV_n \tag{5.32}$$

Sinusoidal LO appears as a rectified sinusoidal voltage V_r at twice the LO frequency. Since the voltage V_r is not constant with time, it induces charging/discharging current in

the parasitic capacitor C_p. This current is sampled by the same noisy LO as in the case of direct noise.

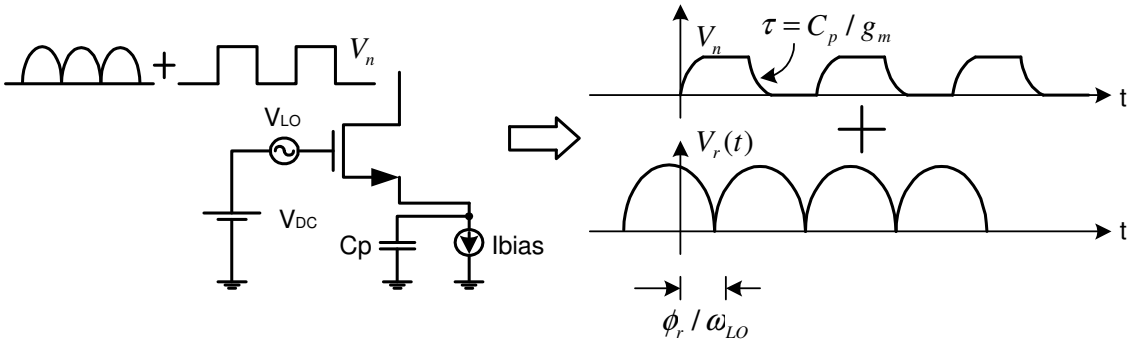


Fig. 5.12 Indirect switch noise mechanism for sinusoidal LO

The average value of the output noise current due to indirect switch noise is calculated over the time limits (-Δt/2, Δt/2) and is given by

$$i_{n,o} = \frac{2}{T} \cdot 2 \cdot \int_{-\Delta t/2}^{\Delta t/2} C_P \left[\frac{d}{dt} V_r(t) \right] dt \tag{5.33}$$

In frequency domain this can be represented as

$$i_{n,o} = -\frac{2C_P}{T} V_n(f) . \frac{g_{m,sw}^{\ 2}}{g_{m,sw}^{\ 2} + (C_P \omega_{LO})^2} \tag{5.34}$$

The total output noise density spectrum for indirect switch noise is given by adding the spectrums of (5.32) and (5.33) resulting in [25]

$$S_{n,o,indirect} = \left(\frac{2C_P}{T} \frac{(C_P \omega_{LO})^2}{g_{m,sw}^{\ 2} + (C_P \omega_{LO})^2} \right)^2 \overline{V_n^{\ 2}(f)} \tag{5.35}$$

Close examination of (5.35) reveals that indirect noise contribution is inevitable as long as there is a parasitic capacitance C_P. Further, this contribution is negligible if ω_{LO} is much less than pole ($g_{m,sw}/C_P$). Thus it can be concluded that although noise contribution by switches is reduced by sharp mixer switching, the lower bound is determined by the parasitic capacitance.

5.4.2.3 Noise Contribution by the Load

Noise contribution of load resistance R is essentially white noise and there is no flicker noise component. Current noise of the resistor adds directly to overall output noise current. Output noise current spectrum of the load noise is given by

$$S_{n,o,R} = \frac{4kT}{R} \tag{5.36}$$

5.4.2.4 Total Noise Contribution

As discussed in the previous sections white noise contribution is mainly from transconductance noise, direct noise of switches and the load resistance noise. For the flicker noise, low frequency direct and indirect noise of the switches is the major contributor. The total output current noise spectral density is given by

$$S_{n,o,total} = S_{n,o,trans} + S_{n,o,direct} + S_{n,o,indirect} + S_{n,o,R} \tag{5.37}$$

Noise figure can be calculated using (5.39) as

$$NF = 1 + \frac{S_{n,o,total} R^2}{A_{CG}{}^2 \left(4kTR_s\right)} \tag{5.38}$$

where A_{CG} is the conversion gain as calculated in (5.20), R_s is the source resistance which is standard 50Ω.

5.5 Linearity Analysis of a Current Commutating Gilbert Cell Mixer

Non-linearity in a current commutating Gilbert cell mixer is primarily dominated by the non-linearity of the transconductance stage. In a current commutating Gilbert cell, transconductance stage is essentially a differential pair. If this differential pair has tail current, the input voltage range for which both transistors are in saturation is $\sqrt{2}(V_{GS} - V_T)$. In this case, IIP3 of the mixer is approximately given by

$$V_{IIP3} \approx 4\sqrt{\frac{2}{3}}\left(V_{GS} - V_T\right) \tag{5.39}$$

However, if the differential pair does not have a tail current source (pseudo-differential) the input voltage range is increased to $2(V_{GS}-V_T)$. In other words, unlike the above case each transistor is operating independently of each other. IIP3 in this case is given by

$$V_{IIP3} \approx 4\sqrt{\frac{2}{3}(V_{GS}-V_T)E_{sat}\,L} \tag{5.40}$$

where E_{sat} is the velocity saturation electric field and L is the length of the transconductor transistor. It can be seen that by removing the current source, IIP3 of the mixer is improved by a factor of $\sqrt{\frac{E_{sat}\,L}{V_{GS}-V_T}}$. Observing both (5.39) and (5.40) it can be seen that linearity of mixer is improved by increasing the overdrive of the transconductor.

Further improvement in linearity can be achieved by proper biasing of the transconductor transistors. If the transistors are biased under high overdrive voltage, velocity saturation can be induced. Under this condition, g_m becomes more insensitive to the gate overdrive thus improves the linearity. However, high power consumption and noise contribution due to velocity saturation limit the value of overdrive that can be attained.

5.6 Design Procedure

Design of the mixer is determined by various constraints of noise, conversion gain, linearity, power consumption and LO voltage swing. Theoretically, each design variable can be found by simultaneously solving all these constraints, which in practice is a tedious exercise. For the initial estimation of design variables for the design of the UWB mixer let us begin with linearity constraint (5.41) which can be rewritten as

$$(V_{GS}-V_T)_{trans} = \left(\frac{V_{IIP3}}{4}\right)^2 \frac{3}{2E_{sat}L} \tag{5.41}$$

This gives the lower bound for transconductor overdrive. Here Esat and L are 4.7e-6 and L=0.18e-6 respectively. V_{IIP3} specification is 1V which leads to

$$(V_{GS}-V_T)_{trans} = 110mV \tag{5.42}$$

Now, let us fix the bias current in the transconductance stage to 5mA which is limited by the power consumption constraint. For short channel device it can be written as

$$I_d = W C_{ox} v_{sat} \frac{(V_{GS} - V_T)^2_{trans}}{(V_{GS} - V_T)_{trans} + L E_{sat}} \tag{5.43}$$

where v_{sat} is assumed to be 10^5 V/m. Using (5.43) width W can be found out as

$$(W)_{trans} = \frac{I_d \left((V_{GS} - V_T)_{trans} + L E_{sat}\right)}{C_{ox} v_{sat} (V_{GS} - V_T)_{trans}^2} \tag{5.44}$$

The transconductance of the input pair for short channel is given as

$$g_{m,trans} = \mu_{eff} C_{ox} \frac{W}{L} (V_{GS} - V_T)_{trans} \frac{1 + \frac{(V_{GS} - V_T)_{trans}}{L E_{sat}}}{\left(1 + \frac{(V_{GS} - V_T)_{trans}}{L E_{sat}}\right)^2} \tag{5.45}$$

Care must be taken to split the transconductance calculated in (5.46) in to two halves, since I and Q mixers share the same transconductance stage. Assuming perfect switching with a given transconductance, conversion gain is given by (5.12). For 10dB conversion gain, load R is given as

$$R = \frac{\pi CG}{g_{m,trans}} \tag{5.46}$$

Next step is to determine the size of switch transistor and amount of current flowing through them (I_{SW}). Since the IF frequency response of the mixer should be maximally flat from DC to 264MHz, the output pole (ω_p) should be at very high frequency (at least 2.64GHz). This puts limitation on the maximum parasitic capacitance at the output node of the mixer. Assuming parasitic cap of next stage as C (100fF) and neglecting the parasitic capacitance of R, the rest of the capacitor contribution comes from two cross coupled switch transistor drains. Assuming this to be from the overlap capacitance the width of each switch is given by

$$W_{SW} = \frac{1}{2 L_D C_{ox}} \left(\frac{1}{R \omega_p} - C \right) \tag{5.47}$$

Now only parameters which need to be determined is the length L of switches and the bias current Isw. To determine these, the overdrive voltage needs to be determined from the V_{LO} specs. Ratio of switch overdrive to V_{LO} is determined by noise considerations.

Fig. 5.13 shows the variation of β and ζ as function of $V_{LO}/(V_{GS}-V_T)_{SW}$. Intuitively, with increase in $V_{LO}/(V_{GS}-V_T)_{SW}$, the time in which switches are in balanced state decrease and hence the direct noise contribution of the switches at high frequencies decrease. This is represented as decreasing ζ. On the other hand, increase in $V_{LO}/(V_{GS}-V_T)_{SW}$ increase the harmonic spread of LO frequency spectrum hence more high

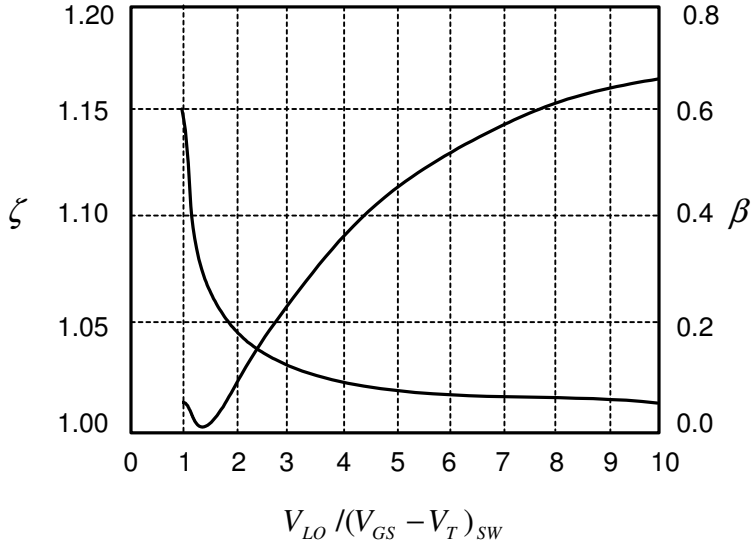


Fig. 5.13 Variation of ζ and β with $V_{LO}/(V_{GS}-V_T)_{SW}$

frequency noise of transconductor is downconverted. For $V_{LO}/(V_{GS}-V_T)_{SW}$ around 2.5, these two noise contributions are equal. Once switch overdrive is fixed, L_{SW} can be found by solving the following quadratic equation

$$\frac{4*g_{m,SW}}{C_{trans}+4*2/3C_{ox}W_{sw}L_{sw}}=B=\frac{4\mu C_{ox}W_{sw}(V_{GS}-V_T)}{L_{sw}(C_{ox}W_{trans}L_D+4*2/3C_{ox}W_{sw}L_{sw})} \quad (5.48)$$

where B is the required bandwidth of the bandpass filter embedded in the mixer.
If C_{trans} contribution is assumed to be negligible as compared to the switch capacitance, (5.48) can be simplified and L_{SW} is given by

$$L_{SW} = \sqrt{\frac{3\mu(V_{GS} - V_T)_{SW}}{2B}} \tag{5.49}$$

where B and $(V_{GS}\text{-}V_T)_{SW}$ are assumed to be 10GHz and of 50mV respectively. Final component values are listed in Table 5.3.

Table 5.3 UWB Mixer Component Values

M1(W/L)	M3(W/L)	M2(W/L)	Rs	Ls	R
160µm/0.18 µm	40µm/0.18 µm	127.5µm/0.34 µm	4.5Ω	2.36nH	500Ω

5.7 Layout Considerations

In a high frequency design, the layout of a circuit plays a very important role. This is because layout determines the nature of parasitic resistances and capacitance which can alter the performance of the circuit dramatically. Proper simulation and extraction tools can help in estimating these effects in the design process. For the UWB Mixer, considering that it operates at high frequencies, special RF mosfets, capacitors and resistors are used. Apart from better model for parasitics, these devices also have better isolation from substrate and adjacent devices. This is especially important for the mixer where LO signal can leak into RF input port. Another important layout consideration is the matching. Matching for switches is very important to lower low frequency noise and DC offsets. There is a trade off between matching and isolation. Due to very high frequency operation, inter-digitization results in poor isolation. Also, due to the fixed layout of RF mosfets used in the design, inter-digitization cannot be applied. Hence, mismatch is further reduced by keeping layout fully symmetric and placing the critical devices as close as possible. In order to reduce parasitic capacitance, metal 6 is used both as resistor Rs and as an interconnect. Layout of the I-Q mixers are shown in Fig. 5.14.

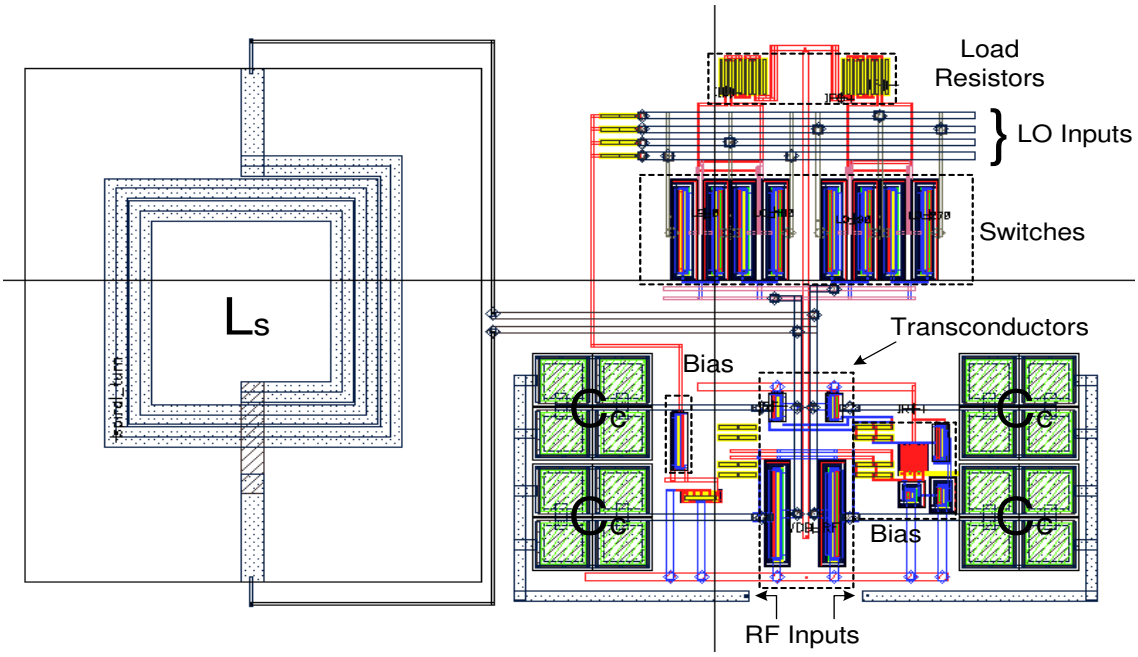


Fig. 5.14 Layout of UWB mixer

5.8 Simulation Results

The UWB mixer has been simulated with actual bond-wire model with assumed load of 100fF of next stage.

5.8.1 Conversion Gain

Conversion gain of the mixer with respect to input RF frequencies is shown in Fig. 5.15. This plot is obtained by overlapping conversion gain simulation for three sets of LO frequencies (3.432, 3.96 and 4.488 GHz) resulting in three lobes. Here x-axis represents the RF input frequency and y-axis represents the conversion gain. From the figure, it can be seen that each conversion gain lobe for each LO frequency has a band-pass characteristic with maxima lying at the LO frequency. In terms of IF frequency, this band-pass response translates into a low-pass response. The roll-off is essentially due to finite parasitic capacitance at the IF output. For a particular IF frequency, the difference

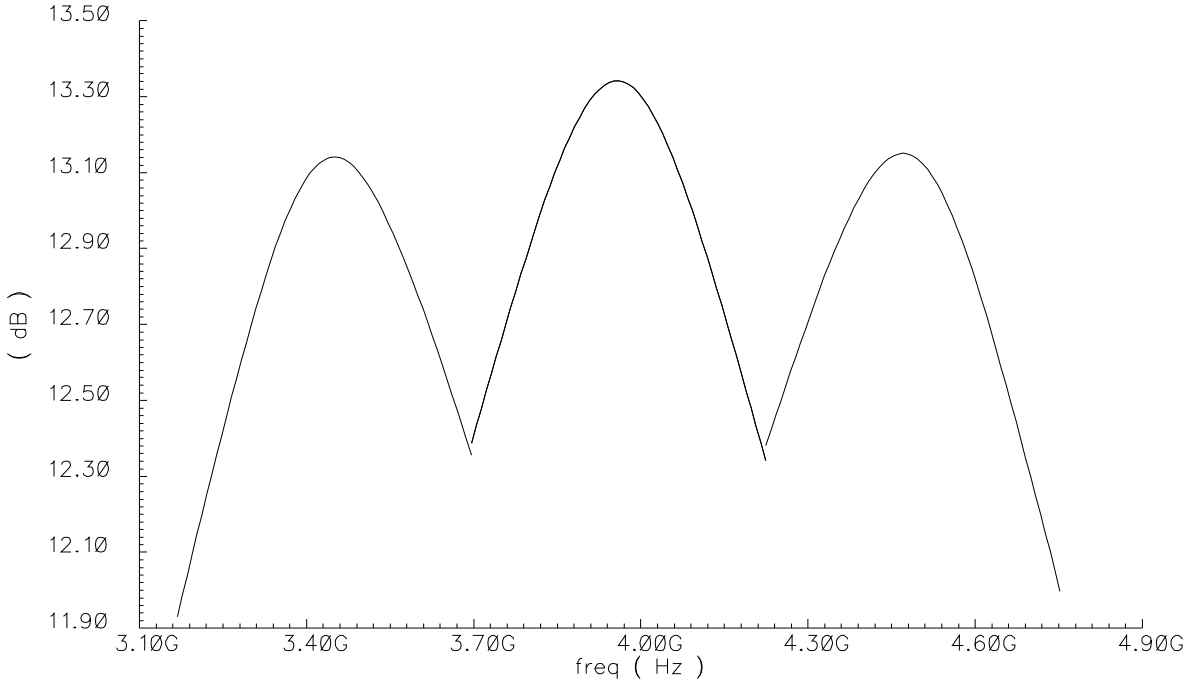


Fig. 5.15 Conversion gain of UWB mixer

in the voltage gain arises from the differences in magnitude of LO and RF signals injected into the commutating switches. Usually, this difference is due to parasitic capacitance at the common source node of the switches. This point is illustrated in Fig. 5.16, which shows the AC gain of the mixer from RF input to the sources of the mixer. Here it can be seen that without inductor, gain rolls off at the rate of 20dB/decade, causing a large conversion gain variation. Introduction of inductor creates a bandpass behavior around centre frequency of 3.96GHz while series resistor decreases the Q of this bandpass circuit, lowering the conversion gain variation. To summarize, average conversion gain of 12.8dB with less than 1dB gain variation over the whole IF range (0-264MHz) for each LO frequency is achieved. For a single IF value, the conversion gain does not change more than 0.4dB.

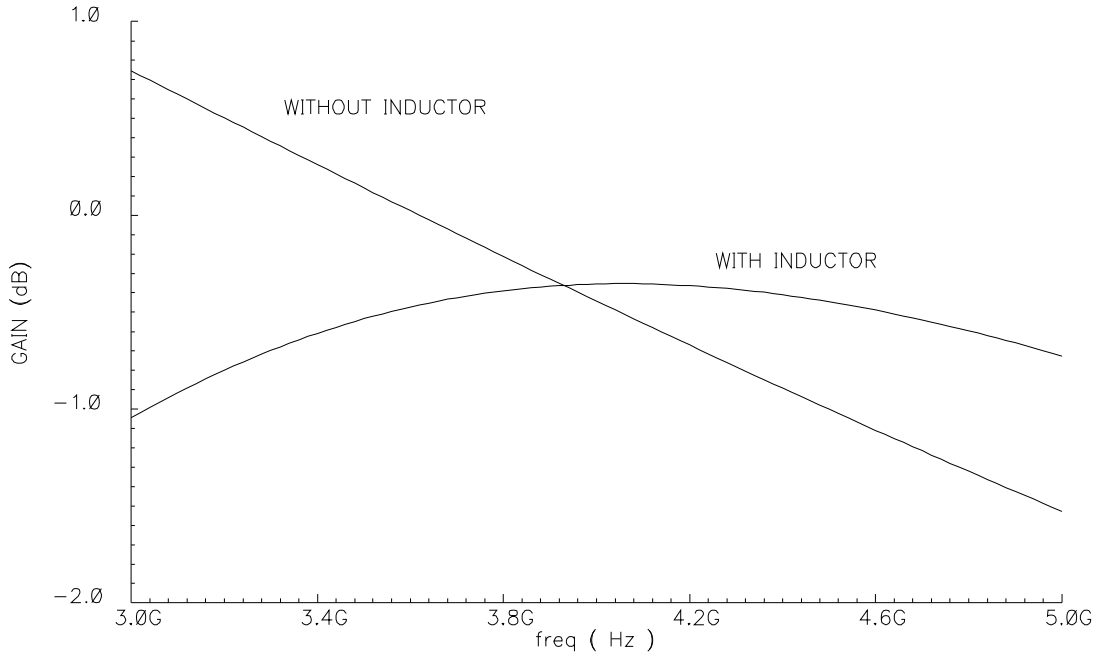


Fig. 5.16 Voltage gain from RF input port to the common source node of switches

5.8.2 Noise Figure

Since I and Q mixers are merged, noise due to the merged transconductor stage appears at the output of each mixer. Also, some part of switch noise of each mixer leaks to the output of other mixer. Hence, noise figure for each mixer is slightly higher than separate mixer case. Noise figure of the merged I-Q mixer is shown in Fig. 5.17. It can be seen that for higher IF frequencies, noise figure is almost constant around 8.5dB whereas flicker noise contribution at lower IF increases noise figure dramatically. However, this is of little concern since useful information starts at 5MHz where noise figure is 9.4dB.

5.8.3 Input Referred IP3

Third order input referred intermodulation product (IIP3) is one of the most important indicators of nonlinearity. In order to measure IIP3, two-tone test is used. For

the purpose of test, two mid band frequencies at 3.9 and 3.91GHz are applied to the input of the mixer. For LO fixed at 4GHz, output contains first order harmonics at 90 and

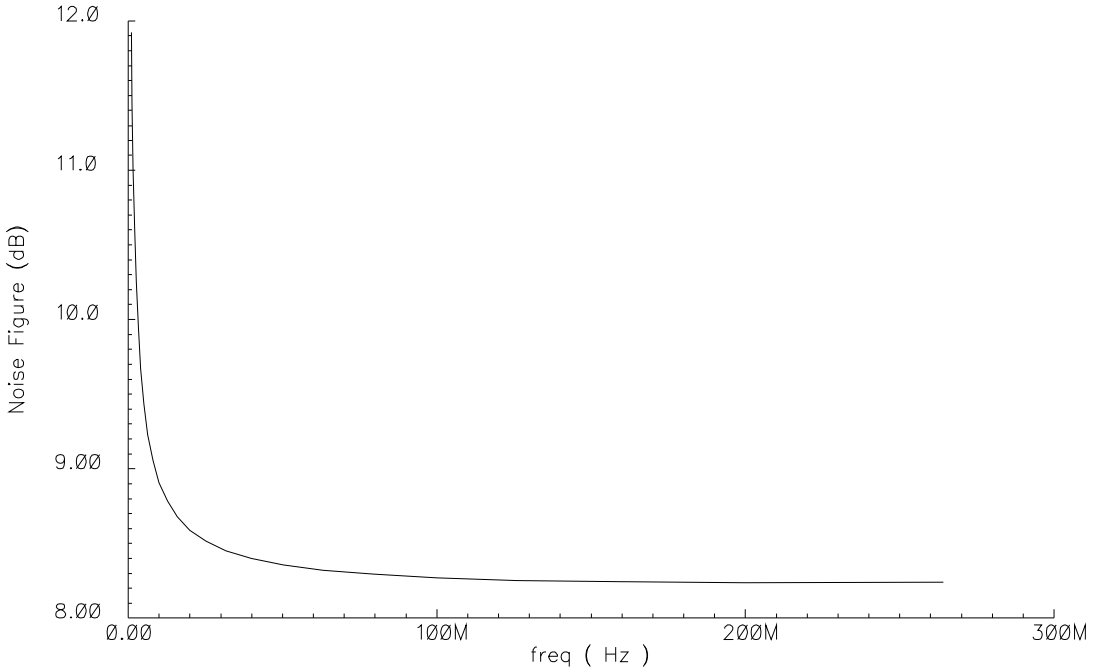


Fig. 5.17 Noise figure of UWB mixer

100MHz and third order harmonics at 80 and 110MHz. Fig. 5.18 shows the output power of first order and third order harmonics with respect to input RF power. From the figure, it can be seen that input referred IP3 comes out to be 6.04dBm. It must be mentioned that due to relatively flat conversion gain characteristic of mixer, a two tone test performed anywhere in the band yields results quite close to ones shown in Fig. 5.18.

5.8.4 Power Consumption

Overall current consumption of the I-Q mixer is 11.7mA. Equivalently, power consumption for a single mixer is 21.1mW. These figures include power consumed by the bias circuit and ignores the power consumption for test buffers as they are not part of the UWB receiver. The core mixer consumes 10.6mA at 1.8 V supply.

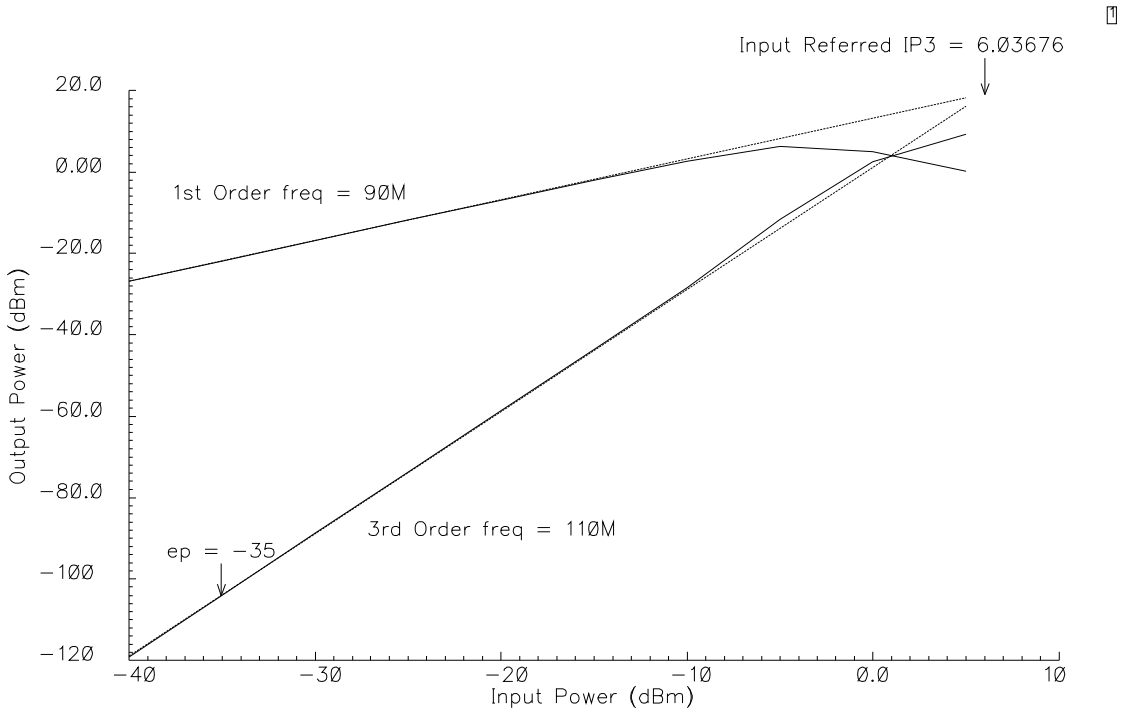


Fig. 5.18 Third order intermodulation product plot

5.8.5 Simulation Results Summary

Mixer results can be summarized in Table 5.4.

Table 5.4 UWB Mixer Simulation Results

Parameter	**Results**
Conversion gain (dB)	12.8
Maximum gain variation (dB)	1.1
Input noise (nV/sqrt Hz)	2.5@5MHz, 2 (average)
Noise figure (dB)	9.4@5MHz , 8.5 (average)
IIP3 (dBm)	6.04
Power consumption (mW)	20.34

CHAPTER VI
CONCLUSIONS

An RF front-end for an Ultra Wideband receiver is designed using TSMC 0.18 µm CMOS process. The front-end, consisting of LNA and I-Q mixers is designed to operate over a wideband of frequencies (3.168-4.752 GHz).

Various LNA architectures suited for wideband operation are investigated. Broadband input matching is achieved by using LC band-pass filters. New output network is proposed which results in high gain with maximum gain flatness. LNA is implemented as fully differential circuit with bond-wire effects taken into account.

UWB Mixer is an enhancement of a current commutating Gilbert cell mixer. In order to achieve band-pass characteristics for near flat conversion gain, inductor is used between common sources of the mixer switches. This technique helps improving both gain and noise figure.

Since RF front-end is fully differential, it helps in achieving greater robustness but at the cost of higher power consumption. Further, use of differential structures necessitates the use of broadband balun to convert single ended input signal to differential. Alternative architecture can be worked on to convert RF front-end single ended to save power. Use of on-chip inductors in the input matching network of LNA degrades the noise figure due to their low quality factors. Noise figure can be reduced by using bond-wires to replace those inductors or alternatively having off-chip matching network.

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