ANALOG-TO-DIGITAL INTERFACE DESIGN FOR WIRELESS RECEIVERS

A Dissertation

by

BO XIA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2004

Major Subject: Electrical Engineering

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Approved as to style and content by:

Edgar Sánchez-Sinencio (Chair of Committee)	José Silva-Martínez (Member)
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ABSTRACT

Analog-to-Digital Interface Design for Wireless Receivers. (December 2004)

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As one of the major building blocks in a wireless receiver, the Analog-to-Digital Interface (ADI) provides link and transition between the analog Radio Frequency (RF) frontend and the baseband Digital Signal Processing (DSP) module. The rapid development of the radio technologies raises new design challenges for the receiver ADI implementation. Requirements, such as power consumption optimization, multi-standard compatibility, fast settling capability and wide signal bandwidth capacity, are often encountered in a low voltage ADI design environment. Previous research offers ADI design schemes that emphasize individual merit. A systematic ADI design methodology is, however, not sufficiently studied. In this work, the ADI design for two receiver systems are employed as research vehicles to provide solutions for different ADI design issues.

A zero-crossing demodulator ADI is designed in the $0.35\mu m$ CMOS technology for the Bluetooth receiver to provide fast settling. Architectural level modification improves the process variation and the Local Oscillation (LO) frequency offset immunity of the demodulator. A $16.2dB$ Signal-to-Noise Ratio (SNR) at 0.1% Bit Error Rate (BER) is achieved with less than $9mW$ power dissipation in the lab measurement. For ADI in the 802.11b/Bluetooth dual-mode receiver, a configurable time-interleaved pipeline Analog-to-Digital-Converter (ADC) structure is adopted to provide the required multi-standard compatibility. An online digital calibration scheme is also proposed to compensate process variation and mismatching. The prototype chip is fabricated in the $0.25\mu m$ BiCMOS technology. Experimentally, an SNR of $60dB$ and

$64dB$ are obtained under the 802.11b and Bluetooth receiving modes, respectively. The power consumption of the ADI is $20.2mW$ under the 802.11b receiving mode and $14.8mW$ under the Bluetooth mode.

In this dissertation, each step of the receiver ADI design procedure, from system level optimization to the transistor level implementation and lab measurement, is illustrated in detail. The observations are carefully studied to provide insight on receiver ADI design issues. The ADI design for the Ultra-Wide Band (UWB) receiver is also studied at system level. Potential ADI structure is proposed to satisfy the wide signal bandwidth and high speed requirement for future applications.

To my beloved parents, brother and wife

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TABLE OF CONTENTS

CHAPTER Page

CHAPTER Page

CHAPTER Page

LIST OF TABLES

TABLE Page

LIST OF FIGURES

FIGURE Page

FIGURE Page

FIGURE Page

FIGURE Page

FIGURE Page

FIGURE Page

CHAPTER I

INTRODUCTION

As indicated by its name, Analog-to-Digital Interface (ADI) is the block that conducts the analog-to-digital conversion function in a circuit system. It is needed in almost every mixed-signal applications, from audio [1] [2] to wide band data transferring systems [3] [4]. Especially, in a wireless receiver, the ADI is an important component in the baseband. Fig. 1 shows a general model of a wireless receiver. Digital modulation formats and protocols are dominant in the modern wireless communication systems. As a result, the Medium Access Control (MAC) level baseband data process must be performed in the digital domain. However, the received Radio Frequency (RF) signal and the receiver frontend signal processing are all in the analog domain. The ADI works as a bridge in the receiver to connect the analog frontend and baseband digital processing module. We will further discuss the architectures and operation principles of the wireless receivers in Chapter II, but we can already see the importance of the ADI in a receiver through this brief description. The purpose of this research work intends to provide solution and implementation guide-lines for the ADI design in a wireless receiver environment.

A. Research Motivation and Goals

The rapid development in the wireless technology introduces new design issues and challenges, such as the low power consumption, high speed, fast settling and multi-standard programmability. These issues may result in contradictory circuit require-

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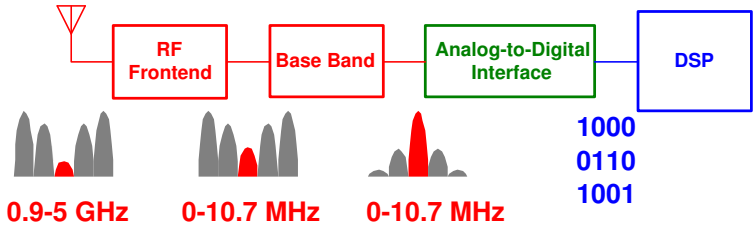

Fig. 1. The general model of a wireless receiver

ments in the implementation. In the previous research work, usually one or two ADI design merits were emphasized at a cost of sacrificing others. In this work, we try to balance the design requirements in an ADI circuit and find the optimized solution. Two design projects were carefully selected to fulfill the research purpose. They are the ADI designs for Bluetooth receiver and 802.11b/Bluetooth dual-mode receiver. Both architectural and circuit level design improvements are proposed in this dissertation for the low power ADI design in these two receivers. The ADI design for Ultra Wide Band (UWB) receiver is also discussed at system level for the completion of the topic.

The main goals of this work can be summarized as follows:

- ◇ *Identify the design methods and system level consideration for ADI circuit under different wireless standards.*
- ◇ *Explore low power consumption techniques, both at architectural and circuit level, for ADI design in a receiver environment.*
- ◇ *Investigate the solution and design techniques for ADI implementation in a fast settling system, such as the ADI for the Bluetooth receiver.*
- ◇ *Investigate the solution and design techniques for ADI implementation in a multi-standard receiver, such as the 802.11b/Bluetooth dual-mode receiver*

- ◇ *Investigate the solution and design techniques for ADI implementation in a wide-band receiver, such as the UWB receiver*

B. Organization of this Dissertation

This dissertation is divided into seven chapters.

Chapter II introduces the research background of this work. Popular ADI design approaches are briefly reviewed in this chapter.

In Chapter III, three ADI design cases are proposed. The ADI designs in the Bluetooth receiver, 802.11b/Bluetooth dual-mode receiver and UWB system are explored to provide solutions to the challenges and demands that are raised by the development in the wireless technology. The system level considerations for both cases are also revealed.

Chapter IV focuses on the ADI design for the Bluetooth receiver from ADI architecture level definition to circuit verification on the silicon.

Chapter V and VI cover the ADI design for the 802.11b/Bluetooth receiver. Chapter V discusses the system design considerations and the selection of ADI architecture. Chapter VI reveals the circuit implementation and lab measurement verification for the ADI design in detail.

Chapter VII summarizes the conclusions and observations that we have obtained during the process of this research work.

CHAPTER II

ADI DESIGN IN THE WIRELESS RECEIVER SYSTEMS

Recent years have seen the rapid expansion in the wireless communication market. Besides the tremendous development in the cell phone business [5], the wireless data communication networks [6], also experiences exponential growth. New standards and demands from end users raise design issues and challenges to the wireless receiver implementation. As an essential part of the receiver, the ADI also faces new requirements in its design.

A. The Development and Trends in the Wireless Technologies

Modern wireless technologies has evolved from the simple mobile phone services to the current high speed date data and multimedia services since the first introduction of Advanced Mobile Phone System (AMPS) in 1983. Its application provides the radio connection among personal, local, wide and metropolitan area networks (PAN, LAN, WAN, MAN). Analog telecommunication technologies has been replaced by more functional and efficient digital communication technologies. Wide band and ultra-wide band applications emerge as the new growing market in the wireless section. In this section, several developments in wireless technologies that affects the design of the ADI will be discussed.

1. Power Conscience Design

Wireless devices are intended to provide mobility for the end users. Therefore, they are usually powered by batteries, which are often the bulkiest and most expensive parts in the radio devices. How to prolong the battery lifetime or optimize the

power consumption is always the theme of the wireless system design and given first priority in all levels of the design hierarchy. ADI as one of the major block in the receiver usually contributes more than one third of the receiver power consumption. Therefore, the ADI design must be power-conscience. Any power saving in the ADI is appreciated in the power optimization of the receiver

2. Multi-Standard Compatibility

One problem that is encountered in the development of the wireless technologies is the co-existence of different communication standards. In the mobile phone and personal communication systems, the services are based on national or regional standards, such as GSM, DECT (Europe), I-54 (US), IS-95 (US). The mobile devises are able to inter-operate only within their own radio environment and geographic regions, where a specific standard is operational. In the office data communication services, the wireless LAN and PAN are both functional. Standards like IEEE802.11b (802.11b), Bluetooth and HomeRF have their own applications, and their service targets often overlap. For instance, an end user may need his laptop to communicate with his headset through Bluetooth network and have the access to the wireless LAN governed by 802.11b standard at the same time. As a result of the various wireless standards, duplicated investment and communication inconvenience become a common experience among wireless service subscribers. Multi-standard transceivers are able to provide a single device to operate under different standards and are considered as the solution to this issue. In the mobile phone services area, so-called Third-Generation (3G) telecommunication systems are developed lately. In the data network, systems integrate both 802.11b and Bluetooth technology has drawn many research interests.

From the receiver point of view, the wireless standards integrated into the multi-standard receiver often have similar RF characteristics. Therefore, the same RF

frontend with none or very limited configurability can be shared among different receiving modes. On the other end of the receiver, the DSP can easily provides the programmability in the protocol and data processing for different standards. The most of the design difficulties are placed in the baseband analog circuits, ADI is one important block among them.

Different wireless standards often adopts different data modulation formats. In term of the ADI circuit design parameters, this results in different dynamic ranges and sample rates. To provide the programmability desired in the multi-standard receiver, the ADI must be able to accommodate the difference in the design specs under different receiving modes.

3. Real-Time Decision and High Throughput Requirement

Real-time response is always desired in the wireless communication systems, especially in the voice and multi-media applications. In the data communication systems, the high throughput is required to improve the overall efficiency. Consequently, the preamble section of the data packet become shorter as the communication standards evolves. The direct impact of this change on the receiver design is the small delay and fast settling requirements.

Besides the settling in the frequency synthesizer in a receiver, the gain control loop that controls the received signal power level also needs time to settle. ADI, as we will explain later, is often located in this gain control loop. Its architecture and delay directly affect the settling of the loop. How to choose the right ADI for a certain settling requirement is also an interesting research topic.

4. Technology Scaling and SoC Requirement

The scaling of the process technology is often companied by the decreasing in supply voltage. This is because of the proportional scaling down of the gate oxide thickness. The System-on-Chip (SoC) solution requires the analog and digital parts of the receiver to be integrated on the same chip. A low supply voltage helps to reduce the power consumed by the digital circuit. Due to these two factors, the modern wireless receiver design must be conducted under low voltage supply environment. This low supply voltage also has its impact on the ADI design.

5. Wide Band Digital Modulation

In order to support data and multi-media communications, the high data rates has been adopted in the wireless systems. Wide band signal is no longer a stranger in the receiver. Ultra-wide band standard is also an area of active research. The wide signal bandwidth requires the ADI to provide a high sampling rate and high linearity, which brings new difficulties into the ADI design in a wireless receiver.

6. Challenges in the ADI Design

Summarizing the design issues revealed in the previous discussion, the challenges encountered in the receiver ADI design includes power optimization, multi-standard compatibility, fast settling, low supply voltage tolerance and high performance. In the reported research, these issues have been emphasized individually. However, a more systematical method is required to provide a guide-line in the ADI design for the wireless receiver. This research work intend to provide such a guide-line. Two ADI designs are conducted targeting at the mentioned challenges. The ADI designed for a Bluetooth receiver is used to study the ADI for receivers that require fast

settling. The ADI design for a 802.11b/Bluetooth dual-mode receiver is performed to explore the multi-standard compatibility and high speed capability in ADI. Both designs are conducted under low supply voltage and intend to achieve optimized power consumption.

B. Wireless Receiver Systems

The location of the ADI defines the separation between the analog and the digital section of the receiver. On the other hand, the receiver architecture directly affects the ADI design specs, such the sampling frequency, dynamic range and linearity requirements. Therefore, to study the ADI design in a receiver, we need to have the knowledge of the receiver architecture and its impact on ADI implementation.

1. Wireless Receiver Architectures

Depending on the location of the ADI in a receiver chain, the basic receiver architecture can be classified into 3 categories [7], as shown in Fig. 2. If we push the ADI to the RF part of the receiver, the signal is digitized at the antenna. All the signal processing including amplification, down conversion and filtering can be done in the digital domain. This results in an ideal Software Defined Radio (SDR) architecture, in which the receiving mode can be easily configurable in the DSP. Although this architecture provides maximum programmability in the receiver operation and is considered as the ultimate solution to the multi-standard communication environment, it is practically impossible to implement with current or near future technologies. The high RF sampling rates and unrealistic dynamic range and linearity requirements prevents this RF ADI receiver architecture to be used in the real wireless receiver design. Compromise in the ADI operating frequency has been made to relax ADI

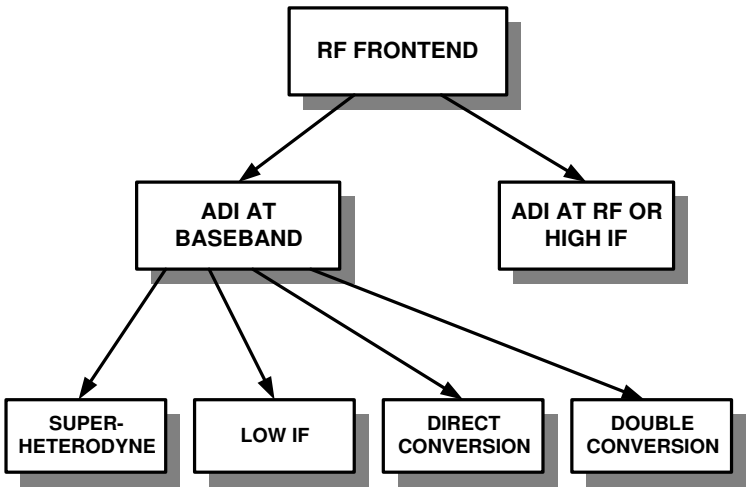

Fig. 2. Wireless receiver architectures

and DSP design specifications by moving the ADI to a high Intermediate Frequency (IF). In this architecture, Low Noise Amplifier (LNA) and mixers are needed in front of the ADI to perform signal amplification and down conversion. The channel selection and other signal processing, on the other hand, can still be conducted in the digital domain. Although this architecture is an area of active research, the design difficulties in the analog filtering and image rejection requirement in the RF section along with the tight specification for the ADI make this architecture impractical or too expensive for the receiver design.

Receivers with ADI at the baseband are the architectures currently applied in the practical wireless system design. Serval different receiver architectures belong to this category. They are super-heterodyne [8], low-IF [9], direct conversion [4] and wideband IF double conversion architecture [10]. Supper-heterodyne receiver architecture, shown in Fig. 3, usually can provide optimized selectivity and sensitivity performance. Unfortunately, it needs external IF filter and hence is not suitable for monolithic integration. The use of the wideband IF double conversion architecture is still under debate. In this architecture (Fig. 4), the received RF signal is often down-

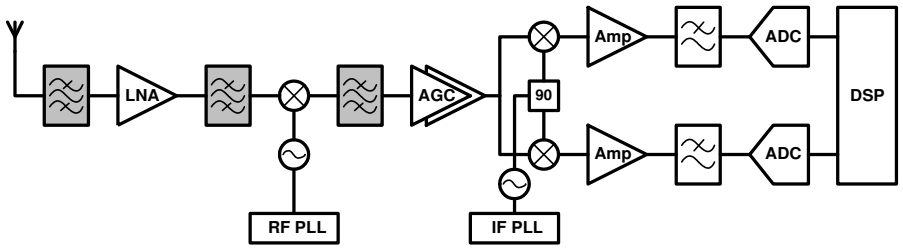

Fig. 3. Super-heterodyne receiver architecture

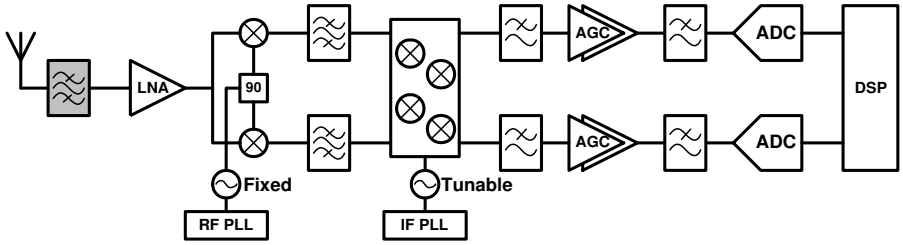

Fig. 4. Wideband IF double conversion receiver architecture

down-converted to DC by two steps. The first LO is fixed to reduce the design difficulties in high frequency PLL. The whole receiver can be integrated on a single chip by using this architecture. The wideband IF double conversion receiver claims to have good DC offset elimination and image rejection due to the two-step down-conversion. However, the need of 6 high performance mixers raises the power consumption considerably, and the frequency intermodulation products generated by the non-linearity of the mixers intends to degrade the receiver performance. Therefore, this architecture is not widely adopted in the practical receiver design either.

Direct conversion or zero-IF and low-IF are the most popular architectures applied in the monolithic receiver design lately. Fig. 5 illustrates a general model of these two architecture. The receiver front end is composed by analog circuits. A common feature of these two receiver architecture is the absence of the high-selectivity IF

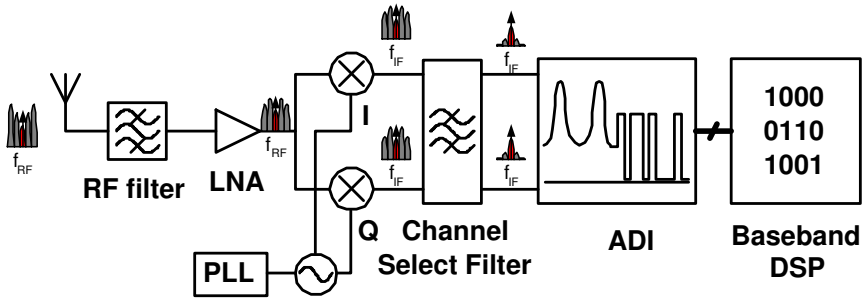

Fig. 5. General block diagram of the direct conversion and low-IF receiver architectures

stages, and thus the integration of the entire receiver becomes possible. The received RF signal is amplified and down converted to IF (low-IF architecture) or DC (Direct Conversion architecture) by the LNA and mixers, respectively. A filter is placed after the mixers to select the wanted channel and block the interferences. Until this phase in a receiver, the signal is in the analog domain. The ADI is located at low frequency baseband and performs the signal digitization. After ADI, the baseband data is processed in the digital domain. The ADI design in the low-IF and direct conversion receivers is the main scope of this research work.

Although the direct conversion and low-IF receiver architectures share many common properties, they provide different performance advantages and have different design challenges. In general, the baseband circuits in a direct conversion receiver operate at a lower frequency and thus have the potential of dissipating less power. However, since the down converted signal is located at DC, the DC offset generated by LO leakage, RF leakage, intermodulation of second order harmonics and other sources intends to corrupt the received signal. Furthermore, the flicker noise is stronger at DC and the lower frequencies. Its existence degrades the noise performance of the receiver. The low-IF receiver, on the other hand, is immune to the DC offset and flick noise issues since the received signal is placed at an IF that is away from DC. The major design concern in the low-IF receiver is the image rejection. Without proper

filtering and processing, the interferences at the image frequency will be mixed with the wanted signal during the down conversion. Comparing to the direct conversion architecture, the receiver baseband works at a higher frequency in the low-IF receiver architecture and may consume more power as a result. When conducting a receiver design, we need to consider the tradeoffs of the different receiver architectures and find the one most suitable for the target application.

2. ADI in a Wireless Receiver

In the previous subsections, we have discussed the location and functions of the ADI in a wireless receiver. However, the choice of receiver architecture also affects the ADI design. In the low-IF and direct conversion architectures, although the ADIs are located at baseband, their operation frequencies are different. Assume that the signal bandwidth is B and the IF is chosen to be f_{IF} for a certain low-IF receiver. We can have two choices for the ADI design for this low-IF receiver. We can either use a lowpass ADI that digitizes all the information within $f_{IF} + \frac{B}{2}$ or a bandpass ADI centered at f_{IF} with a pass band of B. For the lowpass ADI design, the signal bandwidth is f_{IF} larger than the one in the direct conversion ADI design. It may result in power consumption increasing depending on the ADI structure applied. For example, if an Analog-to-Digital Converter (ADC) is chosen, the wide signal bandwidth leads to an unnecessary increment in sampling rate and power dissipation. However, if an analog demodulator, such as an FM (Frequency modulation) demodulator, is used, the high frequency may even improve performance. If a bandpass approach is chosen for the ADI, it may have difficulties in the multi-standard receiver design. Usually, there exists an optimum IF in the low-IF receiver for each standard to achieve best performance. The IF may have to change when the receiving mode is switched. Thus, the bandpass ADI needs also change its center

frequency accordingly. This complicates the circuit design.

As observed in this analysis, the selection of receiver architecture affects the choice of ADI design. On the other hand, the operation frequency of the ADI defines the division of analog and digital signal processing, and hence impacts the choice of the receiver architecture. When designing the wireless receiver and its ADI, we need to take this mutual-impact into account and try to find optimized structures for both design.

C. ADI Design Approaches

In the modern wireless communication systems, the transmitted signal often modulated to improve its immunity to the channel noise and interference. The most commonly used modulation schemes can be divided into 3 large categories, amplitude modulation, frequency modulation and phase modulation. Digital domain modulation schemes are widely adopted due to its robustness, better performance and security. The ultimate goal of a receiver is to recover the transmitted signal. The ADI in a receiver is the starting point of signal processing, therefore the signal modulation format often dictates the selection of ADI structure

Since the received signal is analog, the most natural way to do so is to use an analog domain demodulator. By using such a demodulator as a receiver ADI, we are able to accomplish the digitization and bit detection in a single step. The idea sounds simple and attractive, but the implementation is not that straightforward since such a demodulator circuit has to be realized by hardware. Due to the wide adoption of advanced digital modulation formats in the wireless standards, the circuit implementation of the optimum or sub-optimum demodulators become too expensive and/or too complex to be conducted in hardware. Limited by the circuit non-ideality

and process variation, the detection performance of the analog domain hardware demodulator ADI is usually poor in the digital modulation systems except for in a handful digital FM systems, such as the Frequency Shift Keying (FSK) systems.

Another way to demodulate the received signal is to use a software demodulator, the DSP module. A DSP module can provide low cost and high performance signal demodulation in the digital domain. However, the input of this type of demodulators has to be digital, too. Consequently, an Analog-to-Digital Converter (ADC) is employed as an intermediate stage in a receiver to digitize the analog received signal first. The ADI using ADC is even more popular in the multi-standard receivers. In a multi-standard receiver, the ADI needs to accommodate several different modulation formats. Each of them may need its own demodulator for proper signal detection. It becomes unrealistic to implement each individual demodulator in hardware for the receiver. In the ADC+DSP solution, the programmability in the signal demodulation can be provided by the DSP in the digital domain. Only little configurability is required in the ADC itself. Thus, the ADC approach is dominant in the modern receiver ADI design.

The ADC ADI approach also has its limitations. First of all, the digitization in the ADC introduces quantization error and raises the overall noise floor in the received signal. In order to contain the quantization error, certain resolution requirement needs to be applied to the ADC design. Secondly, with current technology, an ADC can only provide a relatively smaller dynamic range comparing with the huge variation in signal strength seen at the receiver antenna. This dynamic range is further limited by the power consumption budget of the ADC. To satisfy the sensitivity requirement, a fine gain control processing module is needed in the wireless receiver. An Auto Gain Control (AGC) circuit often exists in the receiver that employs an ADC. This directly increases the circuit complexity and power dissipation in a wireless receiver. Another

Table I. The comparison between different receiver ADI design approaches

	Hardware Demodulator Approach	ADC Approach
Detection Performance	Poor	Good
Implementation Cost	Low	High
Power Dissipation	Low	High
Settling Delay	Small	Large
Programmability	Poor	Good
Detection Speed	High	Low

side effect of the presence of AGC circuits is the settling time required in the gain control loop. It introduces design difficulty when real-time response is required in a receiver.

As mentioned before, some hardware demodulators can still provides descent detection performance for some digital modulation formats with simple circuit implementation and consequently low power dissipation. Moreover, most of the hardware analog demodulators can accommodate large signal dynamic range, thus none or very simple gain control structure is needed and results in a fast settling for the receiver AGC loop. Because of these merits presented by the hardware demodulators, they may still worth some consideration in the receiver ADI design as long as the potential performance degradation is affordable.

Table I summarize the discussion in this section. As we can see, the ADC approach provides a better performance for the receiver while the hardware demodulators have a potential to offer low cost and fast settling solution for some modulation formats. Therefore, to choose a proper ADI solution for a wireless receiver we need to consider the impact of the signal modulation format.

D. ADI Design Procedure

Performance wise, dynamic range and sampling rate or frequency are the two most important requirements in the receiver ADI design. To sustain a reliable communication channel, a wireless standard defines the maximum allowable transmission error, often in form of Bit Error Rate (BER) or Frame Error Rate (FER). BER and FER can be calculated as

$$\begin{aligned} BER &= \frac{N_{be}}{N_{br}} \\ FER &= \frac{N_{fe}}{N_{fr}} \end{aligned} \tag{2.1}$$

where N_{be} and N_{fe} are the number of bit and frame in error, respectively; N_{br} and N_{fr} are the total number of the bit and frame received. To comply with this transmission error specification, the noise floor in the receiver must be suppressed and enough samples of the received signal need to be provided to guarantee proper demodulation performance. The dynamic range and sampling rate of the ADI can therefore be derived from the demodulation requirements. As a common practice, the ADI design often follows the procedure described below.

1 Build a demodulator model based on the wireless standard. The demodulator model developed should comply with the real circuit implementation. Its design should consider both performance and implementation complexity.

2 Model the received signal with noise and interference. Run the received signal through the demodulator. Filtering can be applied if certain filter is deployed in the receiver. Intensive simulation needs to be done in this step. Try different combination of noise power and sampling rate to find the minimum Signal-to-

Noise Ratio (SNR), SNR_{DEM}, and sampling frequency, f_S required to obtain the transmission error specs defined in the standard. SNR_{DEM} will be design base for both receiver and ADI noise performance. In ADC ADI structure, SNR_{DEM} specifies the quantization noise floor. f_S defines the sampling rate or frequency in the ADI. It satisfies not only the Nyquist criteria for signal recovery but also the sampling requirement in the demodulation.

3 The ADI dynamic range considers both the SNR_{DEM} requirement in the demodulator and the received signal dynamic range at the input of the ADI, DR_{Sig}. DR_{Sig} is determined by the receiver architecture and receiver sensitivity requirement, which specifies the minimum and maximum received signal power, $P_{Sig,MIN}$ and $P_{Sig,MAX}$, at the antenna. If the receiver stages before the ADI provides a gain from G_{MIN} to G_{MAX}, the signal dynamic range at the input of the ADI can be expressed as,

$$DR_{Sig} = |P_{Sig,MAX} \cdot G_{MIN} - P_{Sig,MIN} \cdot G_{MAX}| \tag{2.2}$$

And dynamic range of the ADI, DR_{ADI}, can be calculated by

$$DR_{ADI} = SNR_{DEM} + DR_{Sig} \tag{2.3}$$

As we can see in equation (2.2), the DR_{Sig} is largely dependent on the gain in the receiver front-end. If the a gain control system exists in the receiver, the signal dynamic range could be reduced at the input of the ADI and therefore relaxes the dynamic range required in the ADI. However, with the absence of a gain control circuit, the ADI needs to provide large dynamic range to accommodate the received signal.

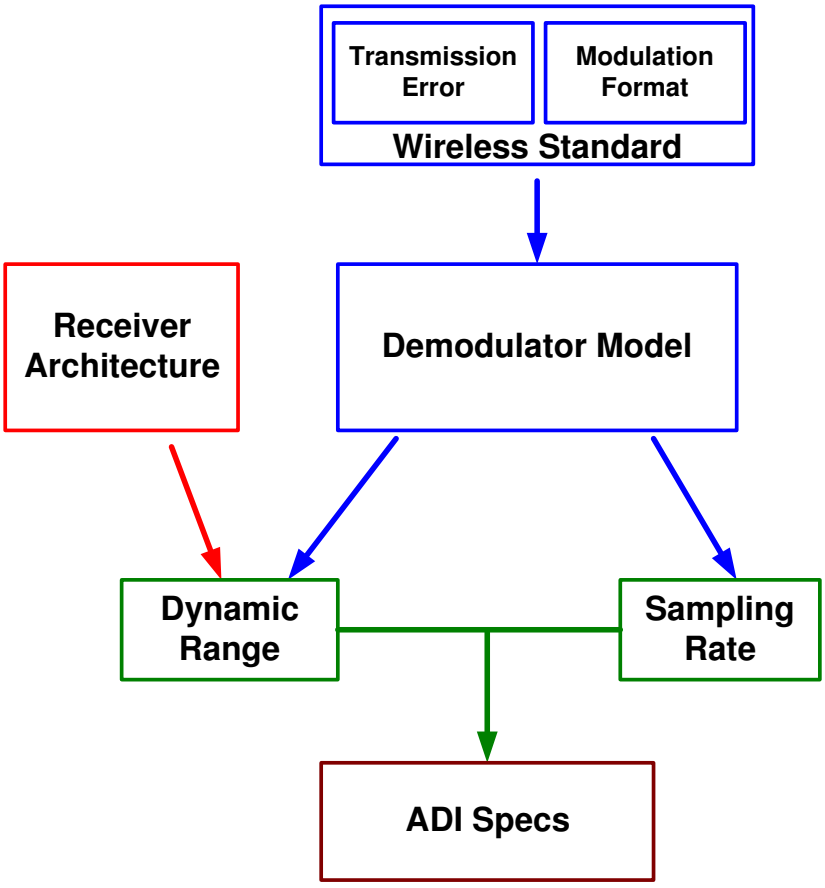

Fig. 6. Specs derivation for ADI design

After we obtain the dynamic range and sampling rate specs, we can define the ADI with a consideration of power and silicon area budget in the receiver system. Tradeoffs are made before we can reach for the ADI structure and further divide the specs for the sub-blocks in the ADI as we will discuss in the following chapters. Fig. 6 illustrates the design follow adopted in ADI specification derivation.

CHAPTER III

BLUETOOTH, 802.11B/BLUETOOTH DUAL-MODE AND ULTRA-WIDE BAND RECEIVER SYSTEMS

The Bluetooth and 802.11b/Bluetooth dual-mode receiver design were two consecutive RF system research projects that are conducted by Dr. Sánchez–Sinencio in the Analog and Mixed Signal Center of Texas A&M University. The prototypes of the Bluetooth and 802.11b/Bluetooth receivers is implemented in 0.35 μm CMOS and 0.25 μm BICEPS technology, respectively. Ahmed Emira, Chunyu Xin, Sung Tae Moon, Ari Yakov Valero-Lopez, Alberto Valdes-Garcia and the author participated in both projects. Enjoin Sheen played a leading role in the Bluetooth receiver system design and Ahmed Nadir Shielding made important contribution in 802.11b/Bluetooth receiver design. UWB as a newly introduced technology also draws many research interests lately for its applications in high speed data transferring systems. The receiver architectures and the ADI design concerns for all the three systems are described in this chapter.

A. The Wireless Standards

Over the last decade, numerous wireless standards have been developed for all kinds of applications and networks. Among them, several standards, such as the IEEE 802.11 series and the Bluetooth, dominate the current wireless market. Others, like the Ultra Wide Band (UWB) and IEEE 802.15.4 standards, will pervade soon in the future. Those wireless standards are complimentary, although huge overlaps still exist in their applications.

IEEE 802.11 series, often referred as Wi-Fi standards, are designed for enterprise

network. They have powerful data transmission capability, transferring at a rate of several mega-bit per second. As a tradeoff, the Wi-Fi systems intend to be expensive, bulky and have high power consumption. They are therefore used to build up the wireless infrastructure. Bluetooth, which has been adopted by IEEE as its 802.15.1 standard, was developed originally for Personal Area Network (PAN). It connects the devises such as hand-free headset and cell phones, printers and laptops. It also finds itself applaudable in the sensor applications. The Bluetooth chip targets for low cost and low power market. However, Bluetooth system needs to rely on other wireless network, such as the cell phone and Wi-Fi, to fully explore its functionality. UWB is a standard still under development. Its system serves as a wireless multi-media platform. UWB standard provides such a wide bandwidth that it can easily support wireless video applications. Although UWB systems are mainly used for high speed wireless applications, they also overlaps some of the Bluetooth functions, such as the connection among home appliances and peripherals with a PC. The trend in the wireless standard evolution is to pursue ever larger bandwidth. However, for some application, such as the monitoring and controlling in a warehouse, only very little information needs to be transferred but the amount of the devise needed is hundreds. The large bandwidth and its associated cost are just a waste. IEEE 802.15.4, also known as ZigBee, is to address this issue. It data rate is only 250 kbits, but its cost is so low that you can attach to almost everything. In the monitoring and controlling application, the security somehow becomes important. The ZigBee uses frequency hopping technique to enhance its security. Table II lists all the major wireless standards, their application, pros and cons. As for the system design under those different standards, each will have its own priorities and problem as we will discuss in the later sections.

Table II. Summary of existing wireless standards

Standard	Application	Cost	Pros	Cons
Wi-Fi	Enterprise Network	> $20	High data rate, Uses existing network	High cost, High power consumption, Requires Aps
Bluetooth	Personal area network	< $5	High installed base, Optimized for voice	Rely on other networks, Max of 8 nodes
UWB	Multi-media applications	> $20	Wide bandwidth, Optimized for multi-media	Still under devolvement, high cost and power consumption
ZigBee	Monitoring and Controlling	$0.5	Low cost and power consumption, No APs required	Application restricted, No processing and storage capability

B. Design of a Wireless Receiver

Noise figure and linearity are the two most important specs in the wireless receiver design. Noise figure, NF, is used to specify the noise generates by the receiver circuit, it can be expressed as,

$$NF = 10log_{10}\frac{SNR_i}{SNR_o} = SNR_{i,dB} - SNR_{o,dB} \tag{3.1}$$

Here SNR_o is the SNR at the output of the receiver and SNR_i is the SNR at the input of the receiver; $SNR_{i,dB}$ and $SNR_{o,dB}$ are input and output SNR in dB, respectively. 2^{nd} and 3^{rd} order intermodulation intercept point, IIP_2 and IIP_3, are often used in the receiver system to measure the linearity. They are the imaginary power point that the 2^{nd} or 3^{rd} order intermodulation product exceeds the signal power, respectively.

As we mentioned in Chapter II section D, the wireless receiver system design starts from the SNR required for proper demodulation performance. The wireless system transmission error is often given in the standard as Bit Error Rate (BER) or Frame Error Rate (FER). BER and FER have been defined in equation (2.1). With a right demodulator model, we can obtain the SNR requirement, SNR_{DEM}, to satisfy the BER or FER specs for the wireless system. This SNR_{DEM} is the SNR requirement for the receiver output. Usually, the wireless standard also specifies the sensitivity required in the receivers. Receiver sensitivity, $P_{si,min}$ defines the minimum power of the signal that the receiver needs to detect. The noise design for a receiver targets at this minimum detectable signal power level. The white noise floor, N_i, at the antenna is

$$N_i = 10log_{10}(kT) + 10log_{10}BW = -174 + 10log_{10}BW \tag{3.2}$$

where k is the Boltzmann's constant, T is absolute temperature and BW is the sigal

bandwidth. We can have the receiver input SNR as, $P_{si,min} - N_i$. Therefore, the system NF can be derived as considering proper design margin,

$$\begin{aligned} NF &= SNR_{i,dB} - SNR_{o,dB} \\ &= P_{si,min} + 174 - 10log_{10}BW - SNR_{DEM} - DesignMargin \end{aligned} \tag{3.3}$$

Some wireless standard defines two-tone test requirement for the system, which provides information of intermodulation product suppression. As a rule of thumb, the intermodulation product needs to be suppressed below noise floor to avoid interfering with the wanted signal. Usually, the second and third order intermodulation products dominate in the receiver system. The strength of those intermodulation , P_{IM2} and P_{IM3}, is related to the IIP2 and IIP3, as expressed below.

$$P_{IIM2} = 2P_{int} - IIP2 \tag{3.4}$$

$$P_{IIM3} = 3P_{int} - 2IIP3 \tag{3.5}$$

where P_{int} is the interferer power indicated in the two-tone test. At receiver output, the P_{IM2} and P_{IM3} have to be lower than the noise floor. Given minimum receiver output signal power $P_{so,min}$, the maximum receiver noise floor equals $P_{No} = P_{so,min} - SNR_{DEM}$. Therefore, we have

$$\begin{aligned} P_{IIM2} &< P_{No} \Rightarrow \\ IIP2 &= 2P_{int} - P_{so,min} + SNR_{DEM} + DesignMargin \\ P_{IIM3} &< P_{No} \Rightarrow \end{aligned} \tag{3.6}$$

$$IIP3 = \frac{1}{2}(3P_{int} - P_{so,min} + SNR_{DEM}) + DesignMargin \quad (3.7)$$

Once we have the overall NF, IIP2 and IIP3 for the receiver system, we can assign noise figure and linearity requirement to the individual block. In the block specification derivation, we can use the following equation to divide the receiver NF to the NF specs for each building block.

$$\begin{aligned} F &= 10^{\frac{NF}{10}} \\ F_{tot} &= 1 + (F_1 - 1) + \frac{F_2 - 1}{G_1} + ... + \frac{F_N - 1}{G_1 G_2 ... G_{N-1}} \end{aligned} \quad (3.8)$$

Here F is called noise factor, F_i is the noise factor of the i^{th} block, F_{tot} is the total noise factor of the receiver and G_i is the gain of the i^{th} block. For linearity, we can use following equations to distribute IIP2 and IIP3 into individual blocks. In the equations, A_{IIP2_i}, A_{IIP3_i} and A_i are the input referred IIP2, IIP3 (in volts) and the linear voltage gain of the i^{th} block, respectively.

$$\frac{1}{A^2_{IIP3_{tot}}} = \frac{1}{A^2_{IIP3_1}} + \frac{A_1^2}{A^2_{IIP3_2}} + \frac{A_1^2 A_2^2}{A^2_{IIP3_3}} + ... + \frac{A_1^2 A_2^2 ... A^2_{N-1}}{A^2_{IIP3_N}} \quad (3.9)$$

$$\frac{1}{A_{IIP2_{tot}}} = \frac{1}{A_{IIP2_1}} + \frac{A_1}{A_{IIP2_2}} + \frac{A_1 A_2}{A_{IIP2_3}} + ... + \frac{A_1 A_2 ... A_{N-1}}{A_{IIP2_N}} \quad (3.10)$$

Tradeoffs need to be made to optimize the overall system performance with respect to the total power consumption and implementation complexity for each block.

C. System Level Considerations in the Bluetooth Receiver Design

Bluetooth is a universal radio interface that has been developed to enable the short range wireless communication among the electronic devices through ad hoc radio

connections. It finds many applications in the PAN settings. From design point of view, Bluetooth technology offers a low power, low cost radio platform for the existing portable devices.

1. Summary of the Bluetooth Radio Specification

Blueooth system operates in the 2.4 GHz Industrial Scientific and Medical(ISM) band. Table III summarizes the Bluetooth radio specification [11], and the RSSI in the table stands for Received Signal Strength Indicator.

Low cost and single chip solution are the most attractive features of the Bluetooth technology. Comparing to the bipolar or BiCMOS technology, CMOS process is preferred in the Bluetooth system design because it provides inexpensive implementation and high integration level. Thank to the development in the process, the current CMOS technology is able to accommodate high speed RF circuit design in GHz frequency band and hence can be applied in the Bluetooth receiver design. Therefore, TSMC 0.35 μm CMOS technology is employed to realize the Bluetooth receiver system.

For the ADI design, we are more interested in the baseband definition of the Bluetooth system. The Bluetooth baseband signal has a data rate of 1Mbit/s and is modulated in Gaussian Frequency Shift Keying (GFSK) format. The product of the absolute filter bandwidth B and the symbol duration T, BT, equals 0.5 in the Bluetooth GFSK modulation. The frequency modulation index for the Bluetooth signal is between 0.28 and 0.35. Fig. 7 illustrates the power spectrum of the modulated Bluetooth baseband signal. According to the power distribution analysis, 99% of the total Bluetooth GFSK signal power is contained within DC to 430 kHz when a nominal modulation index of 0.32 is applied.

Table III. Summary of the Bluetooth radio specification

Frequency Band		2400-2483.5 MHz
Duplex		Time Division
Modulation		GFSK
Channel Space		1 MHz
Sensitivity		-70 dBm (for 0.1% BER)
Maximum Signal Level		-20 dBm
Interference Performance	$C/I_{co-channel}$	-11 dB
	C/I_{1MHz}	0 dB
	C/I_{2MHz}	-30 dB
	$C/I_{\geq 3MHz}$	-40 dB
	C/I_{image}	-9 dB
Out-of-band Blocking	30-2000 MHz	-10 dBm
	2000-2399 MHz	-27 dBm
	2498-3000 MHz	-27 dBm
	3-12.75 GHz	-10 dBm
Intermodulation Characteristics	Interference Frequency	3, 4, 5 MHz
	Interference Level	-39 dBm
	Bluetooth signal Level	6 dB above sensitivity
RSSI	Range	-60 ± 4dBm - 20 ± 6dBm
	Accuracy	$\pm$4dB
Radio Frequency Tolerance	Transmitted Frequency Accuracy	$\pm$75 kHz
	Frequency Drift	$\pm$25 kHz in one slot

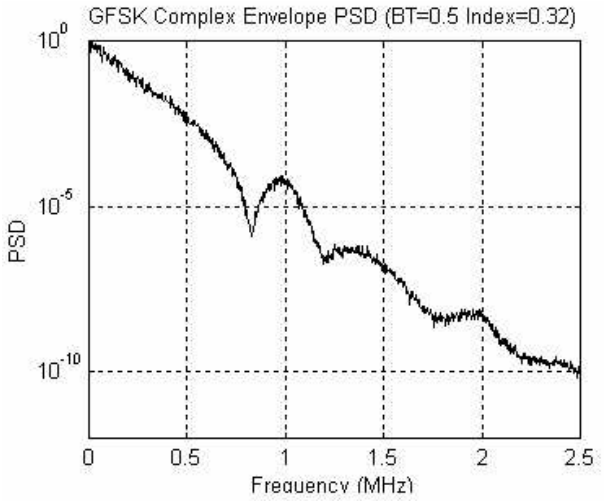

Fig. 7. Power spectrum of a Bluetooth baseband signal

2. Bluetooth Data Packets

The timing arrangement in a Bluetooth system affects the receiver design especially the ADI circuit. To understand the receiving timing, we need to have the knowledge of the Bluetooth packets [11].

Bluetooth standard defines several different types of packets to conduct various functionalities and convey data. Fig. 8 depicts the general format of a Bluetooth packets. Each packet starts with an access code and a header. They have a fixed size for all the data packets. The packet types are defined in the header. The payload length can range from 0 to a maximum of 2754 bits depends on the type of the packet. In the receiver design, we are only interested in the access code because only that part of the packet is used for the receiver settling and synchronization. Fig. 9 shows the Bluetooth access code format. The preamble and Trailer are consists of 4-bit DC offset free codes, either in the form of "0101" or "1010". The 4-bit preamble is included in all the packet while the trailer only appears in the data packet. The 64-bit sync word is used for receiver synchronization. It is formed by Pseudo Noise

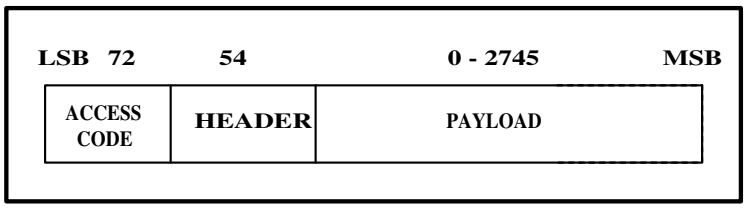

Fig. 8. Standard Bluetooth packet format

(PN) codes.

In the modern digital wireless communication systems, the signal often transmitted in data packets. A data packet consists a prefix part referred as header or access code and the data payload. The prefix includes preamble, synch word and other control signal. Among them, preamble is often used for the receiver to adjust its receiving mode, such as adjust the gain to comply to the received signal strength. Obviously, the prefix part of the data packet including the preamble is an overhead in the data communication. In order to improve throughput, short prefix is always desired in the data packet format. Short preamble, which is 4-bit in signal length or 4 μs in time, is a unique feature of the Bluetooth packet. To achieve optimal synchronization, the receiver needs to settle down within that 4 μS period before the sync word starts. The settling includes the cancellation of DC offset, the locking of frequency synthesizer and more critical the settling of the Auto-Gain-Control (AGC) circuit as commonly seen in the wireless receiver. This extremely fast settling requirement introduces difficulties to the Bluetooth receiver and especially its ADI design, as we will discuss in Chapter IV and Section D of this chapter. The PN codes that are adopted in the sync word has the same power spectrum as the white noise and therefore is DC offset free. In some design, the time for DC offset cancellation may extend into the sync word receiving phase to exploit the feature of the PN codes, but that compromises the accuracy in synchronization performance.

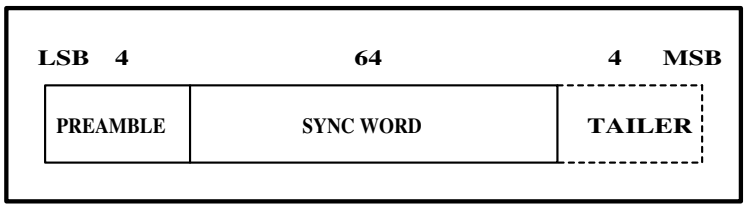

Fig. 9. Bluetooth access code format

3. The Low-IF Bluetooth Receiver Architecture

In order to support the single chip solution and reduce external components in a Bluetooth system, low-IF and direct-conversion architectures are commonly seen in the Bluetooth receiver design. Bluetooth specification is developed in favor of low-IF architecture because of the extremely short preamble and long frequency locking time provided in each time slot [12]. DC offset is a major design difficulty in the direct conversion receiver [13]. Given the short preamble in the Bluetooth data packets, it is almost impossible to detect and cancel the DC offset in such a short period. Fortunately, the redundancy in the sync word somehow relaxes the fast settling requirement for the DC offset cancellation in the direct conversion receivers. Thus, the direct conversion Bluetooth receiver can usually be implemented at the cost of the degradation in the synchronization accuracy.

Another design issue encountered in the direct conversion receiver is the strong flicker noise presented in the CMOS technology. The corner frequency of the flicker noise is somewhere between 500 kHz and 1 MHz in the TSMC 0.35 mum CMOS process. Considering almost all the Bluetooth GFSK signal power is contained within 430 kHz, the strong flicker noise and its high corner frequency degrades the SNR performance of the receiver significantly. The low-IF architecture, on the other hand, is intrinsically immune to these problem. By choosing the IF properly, the DC offset and flicker noise can be far out of the signal bandwidth and hence can be eliminated

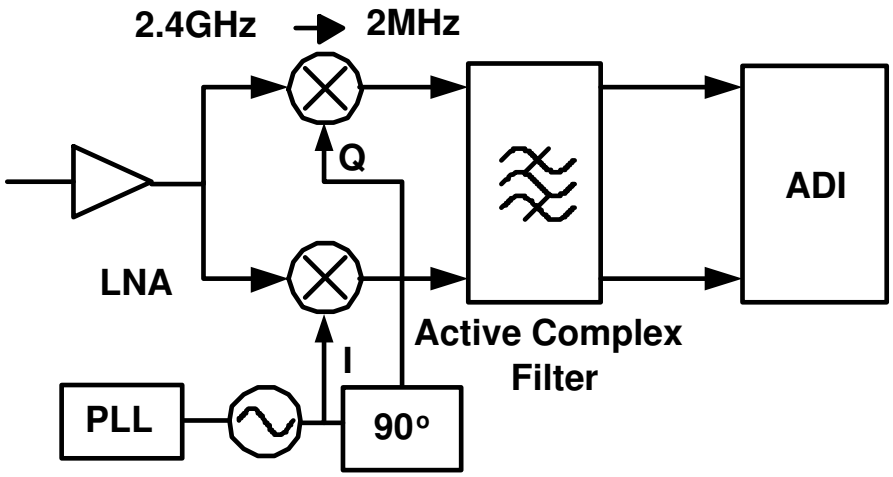

Fig. 10. The block diagram of a low-IF Bluetooth receiver

by the Band Pass Filter (BPF). In a low-IF Receiver, the main issues are to reject the image signal and folded in interferences. These issues can be solved by using a complex filter as the channel select filter [14]. Furthermore, the relaxed image rejection requirement in the Bluetooth standard also helps to alleviate the design difficulty. After examining the design tradeoffs, the low-IF architecture is chosen for the Bluetooth receiver for its high integration level and low implementation cost [15] [10]. As a result of optimization between receiver performance and circuit complexity, the IF is chosen to be 2 MHz.

Fig. 10 shows the block diagram of the Bluetooth low-IF receiver [16]. The RF signal is amplified and down-converted to IF by the front end, then channel selection is performed by an active complex filter. After the channel select filter, an ADI circuit is placed to complete the analog-to-digital conversion. Finally, the digitized signal is conveyed and processed in the baseband DSP. The specs of each individual blocks in the RF frontend is derived in the system design [13] using the method that is described in Section B. Table IV shows the major specs of each block. The input referred noise is a design parameter that is derived from NF with respect to input

Table IV. Major specs for the low-IF Bluetooth receiver

Specs	LNA	Mixer	Active Complex Filter
Voltage Gain (dB)	18	12	15
Input Referred Noise ($nV/\sqrt{Hz}$)	0.5	6	30
IIP3 (V)	0.15	0.45	3.00

and output impedance. The detail of the ADI design in the Bluetooth receiver is discussed in the Chapter IV.

D. System Level Considerations in the 802.11b/Bluetooth Dual-mode Receiver Design

The 802.11b is another wireless standard operating in the 2.4 GHz ISM band and serves as the communication platform of the Wireless Local Area Network (WLAN). Since both 802.11b and Bluetooth are standards for short range radio connection, those two often co-exist in the same office environment and their functions also overlap. From the end user point of view, the convenient switch between the two standards and avoidance of duplicated investment are desirable. The 802.11b/Bluetooth dual-mode receiver is proposed to meet these demands. To reduce the overall implementation cost, sharing the building blocks and using configurable circuits become principle in the receiver design.

1. Summary of the 802.11b Radio Specification

In the previous section, we have discussed the Bluetooth radio specification. We will focus on the 802.11b specification in this subsection. Table V is the summary of the 802.11b RF characteristics [17].

Unlike Bluetooth baseband definition, the 802.11b system includes 4 different

Table V. Summary of the 802.11b radio specification

Frequency Band		2400-2483.5 MHz
Duplex		Time Division
Modulation		DBPSK/DQPSK/CCK
Data Rate		1/2/5.5/11 Mbit/s
Channel Space		25 MHz
Sensitivity		-76 dBm (for 8% FER)
Maximum Signal Level		-10 dBm
Adjacent Channel Rejection	C/I_{25MHz}	-35 dB
Radio Frequency Tolerance		$\pm$60 kHz

data transfer rates and 3 modulation formats. Namely, the Differential Binary Phase Shift Keying (DBPSK) format is applied for the 1 Mbit/s data rate; Differential Quadrature Phase Shift Keying (DQPSK) is used for 2 Mbit/s data rate and Complementary Code Keying (CCK) is applied for 5.5 and 11 Mbit/s data rates. The receiver baseband have to support all of them, which brings challenge to the ADI design. For the RF front end, the specs are similar between 802.11b and Bluetooth, such as the operating frequency band and sensitivity requirements. IBM 0.25 μm BiCMOS technology is utilized by the 802.11b/Bluetooth dual-mode receiver design. Comparing to the CMOS process, BiCMOS process provides lower DC offset, better flicker noise performance, potential of lower power consumption and higher linearity because of the usage of the bipolar transistors. The BiCMOS process is selected in favor of the direct conversion receiver architecture. The reason of using direct conversion architecture in the 802.11b/Bluetooth dual-mode receiver is discussed in subsection 3.

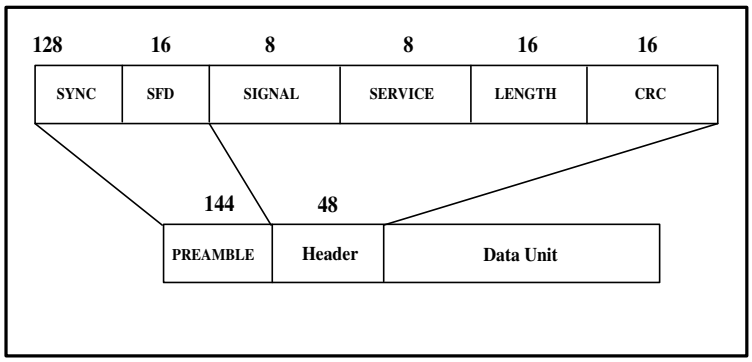

Fig. 11. The 802.11b long data packet format

2. 802.11b Data Packets

802.11b standards defines two different types of data packet formats, long and short formats. The short data packet is optional in the standard and it only adopted the high throughput applications. Fig. 11, 12 illustrate the bits arrangement in the long and short data packets, respectively [17]. Different data transfer rates are applied in the data packets. The preamble has the lowest transfer rate, 1 Mbit/s. The header has a data rate at 2 Mbit/s. And the data unit is transferred at variable rate of 1, 2, 5.5 or 11 Mbit/s in dependence of the modulation formats. Different from the Bluetooth standard, the preamble in the 802.11b data packets are much longer, 144-bit in the long data packet and 72-bit in the short data packet. This gives the receiver circuit 144/72 μS to settle. Although the fast settling is still preferred, the delay spec that can be tolerated in the AGC control loop is much relaxed.

3. The Direct Conversion Architecture for the 802.11b/Bluetooth Dual-Mode Receiver

The direct conversion architecture is more favored in the multi-standard receiver design compared to the low-IF architecture due to the different level of difficulty

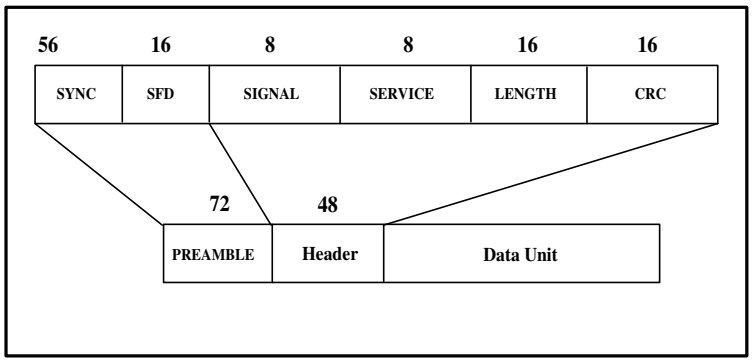

Fig. 12. The 802.11b short data packet format

encountered in their baseband design. In the low-IF architecture, the selection of the intermediate frequency is usually optimized to suite the modulation format and signal bandwidth defined in a particular standard. Therefore, the IF often varies as the receiver switches between the standards to avoid significant degradation in the receiver performance. As a consequence, the channel select filter, whose center frequency is located at the IF, becomes difficult to design. In the direct conversion receiver architecture, the channel select filter is a lowpass filter. It does not have a center frequency to be adjusted when the receiving mode is changed. Furthmore, the signal bandwidth also varies from one standard to the other. The implementation of a variable filter bandwith is more straightforward in the lowpass filter than in its bandpass counterpart.

Fig. 13 depicts a 802.11b/Bluetooth dual mode receiver using direct conversion architecture. The received RF signal first goes through the LNA. The received signal in the 802.11b standard can be 10 dBm stronger than the Bluetooth signal. To accommodate the larger dynamic range of the 802.11b received signal, the LNA provides two different gain modes. It switches between a 15 dB gain or a 15 dB attenuation in dependence of the received signal power. For a 15 dB gain mode, an LNA formed by an inductively degenerated differential pair structure is employed. In

Table VI. Major specs for the 802.11b/Bluetooth dual-mode receiver

Block	Gain(dB)		NF(dB)		IIP3(dBm)		IIP2(dBm)	
	802.11b	BT	802.11b	BT	802.11b	BT	802.11b	BT
LNA	15/-15	15	3	3	-8	-8	11	11
Mixer	16	16	15	20	5	5	48	48
Filter	6	6	32	36	23	23	64	64
VGA	62/0	24	30	30	10	10	31	31

the presence of large signals, the LNA is turned off and the signal is passed through a -15dB attenuator formed by MOS transistors in the triode region. An integer-N frequency synthesizer is employed to generate 2 times of the desired Local Oscillation (LO) frequency to avoid LO pull-in problem in a transceiver. The VCO output is divided by two to generate the LO for the I and Q channels. The received signal is down converted to the DC directly by the mixer. A programmable lowpass filter offers channel selection for both 802.11b and Bluetooth signals by varying the lowpass cutoff frequency. Then the signal goes to the gain control and ADI block before it is sent to the baseband DSP. To minimize the implementation cost. The 802.11b/Bluetooth direct conversion receiver has a shared RF front end and a configurable baseband. Following the discussion in Section B, we can derive the specs for each of the building blocks. Table VI lists the major specs for the individual blocks under both 802.11b and Bluetooth receiving modes[4]. BT in the table stands for Bluetooth. The details of the ADI design for the 802.11b/Bluetooth dual-mode receiver is discussed in the Chapter V.

Although the direct conversion receiver enjoys the high integration level and potential of low power consumption, it suffers from some inherent implementation difficulties, such as DC offset and flicker noise. The large DC offset and flick noise

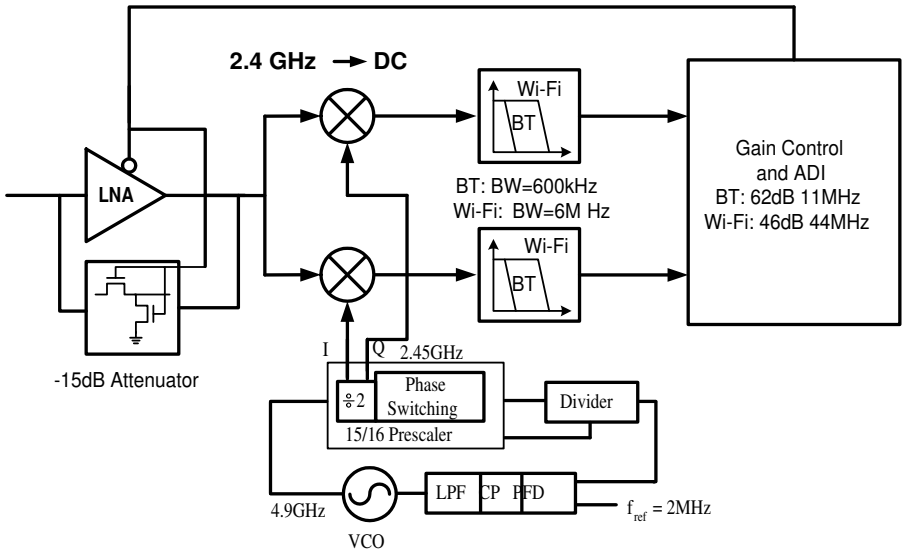

Fig. 13. The block diagram of a 802.11b/Bluetooth dual-mode receiver

make it difficult to design a direct conversion receiver in current CMOS technologies. Extra circuits and structures, such as digital calibration circuit, have to be used to alleviate the performance degradation. Those add-ins complicate the design and largely compromise the cost saving that is promised by the inexpensive CMOS process. BiCMOS technologies, on the other hand, have much lower intrinsic DC offset and flicker noise. Simple measures, like a 2^{nd} or 3^{rd} order highpass filter, can provide enough suppression to the DC offset and flick noise. Therefore, the BiCMOS process is chosen for the 802.11b/Bluetooth direct conversion receiver to relax the design complexity at an acceptable cost.

To integrate the ADI with the receiver frontend on the same chip, the ADI is also implemented in the BiCMOS process. This provides more options to the circuit design since the bipolar transistors are also available. In the transistor level design, the bipolar transistors are employed in the ADI to save power.

E. System Level Considerations in UWB Receiver Design

UWB radio is a promising new technology that is recently approved by the Federal Communication Commission (FCC). It is emerging as a solution for the IEEE 805.15.3a (TG3a) standard [18]. The purpose of this TG3a standard is to provide a specification for a low complexity, low-cost, low power consumption, and high data rate wireless connectivity among devices within the personal operating space. The data transfer rate must be high enough, for instance greater than 110 Mb/s, to satisfy the needs of consumer multimedia applications for wireless PAN communications. The TG3a standard also addresses the quality of service capabilities that is required to support certain multimedia data types. UWB products are envisioned to complement, not compete with, products compliant with IEEE 802.11 standard [19]. IEEE 802.11 is a standard for wireless LANs, while TG3a will be a standard for wireless PANs. The difference is similar to the differences between the Ethernet LAN standard and the USB or Firewire standards that connects peripheral devices.

1. Summary of the UWB Radio Specification

Strictly speaking, UWB is not a technology, but instead, is an available spectrum for unlicensed use. According to the FCC definition, any system operating at 3.1 to 10.6 GHz frequency band and having a signal spectrum more than 500 MHz can be considered as a UWB system as long as it follows the FCC emission level regulations as illustrated in Fig. 14 [20]. However, certain specifications are still needed to guide the UWB system implementation. Several industry leading companies, such as Texas Instruments Inc. (TI), have proposed their own solution for the UWB applications [21]. Those proposals are often referred as preliminary UWB specifications and are followed in the system design.

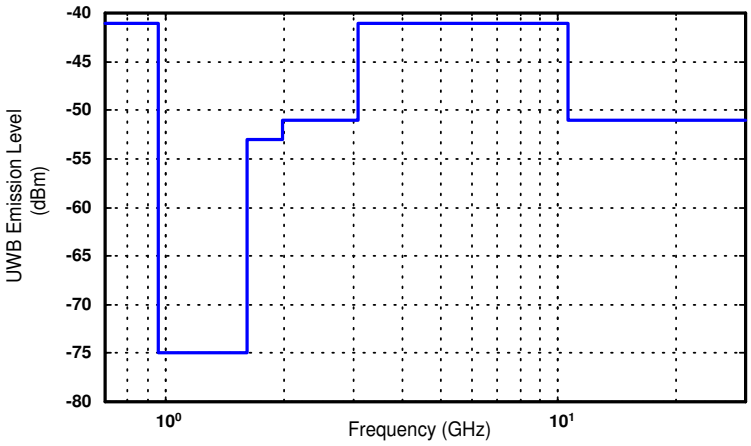

Fig. 14. Indoor UWB spectral mask

Table VII. RF specifications for the multi-band UWB

Parameters	224 Mbit/s	448 Mbit/s
Average TX Power	-10.3 dBm	-10.3 dBm
Total Path Loss	56.3 dB (@4 m)	50.2 dB (@2 m)
Average RX Power	-66.5 dBm	-60.5 dBm
Noise Power Per Bit	-91.0 dBm	-87.2 dBm
RX Noise Figure	6.6 dB	6.6 dB
Total Noise Power	-84.4 dB	-80.6 dB
RX Sensitivity Level	-77.2 dBm	-72.7 dBm
Range	7.5 m	3 m
Frequency of operation	3.1-6.6 GHz	3.1-6.6 GHz
Number of bands	5	5
Bandwidth	500 MHz	500 MHz
Hopping rate	16 MHz 3	2 MHz

A variety of UWB systems can be designed to use the 7,500 MHz available UWB spectrum. Both single-band and multi-band systems have been discussed. In the single-band system, the signal can be shaped so that its envelope occupies the full spectrum. In the multi-band system, a 500 MHz bandwidth is assigned to each signal band, allowing 15 such signals to cover the entire band. There are, of course, intermediate cases, for instance five signals of 2.5 GHz bandwidth each. These two systems also present different implementation challenges. For example, the wider signal bandwidth in the single-band systems requires very fast switching circuits and generates more severe Inter-Symbol Interference (ISI) due to the large delay spread; the multi-band systems, on the other hand, require the signal generator able to quickly switch between frequencies in different signal bands. The 7500 MHz signal bandwidth in a single-band system is simply too wide for the intergraded circuit to handle using current technology. The prototype for the multi-band system, however, is under more active research. Besides the different bandwidth allocation in the variety of UWB systems, the data rate of the UWB systems can also vary. 224 Mbit/s and 448 Mbit/s are two of the most popular data rates that are adopted by the UWB systems. Table VII summarizes the major RF characteristics of the UWB systems according to the TG3a standard.

Due to the wideband nature of the UWB systems, the description of the UWB RF characteristics is quite different from the one of the relatively narrow band Bluetooth and 802.11b systems. We can no long treat the signal as a single tone. Instead of using peak or maximum signal power, we use average power level to specify both transmitter and receiver characters. Comparing with Bluetooth and 802.11b standards, the USB systems have a much lower received signal power level even though the sensitivity specification is comparable. As a result, the required dynamic range for the UWB receivers is much smaller. According to Table VII, the average signal power at the

receiver antenna (Average RX Power, P_{RX}) is -66.5 and -60.5 dBm for the 224 Mbit/s and 448 Mbit/s data transferring modes, respectively. The Bluetooth (Table III) and 802.11b (Table V) systems have a maximum received signal at -20 dBm and -10 dBm, separately. The average UWB receiver dynamic ranges for 224 Mbit/s and 448 Mbit/s data rate can be obtained according to (3.11). Referring to the 50 dB and 66 dB dynamic range required in Bluetooth and 802.11b receiver, the 10-12 dB signal dynamic range relaxes the linearity requirement of the UWB receiver in spite of a wider signal bandwidth. However, the noise figure requirement of the UWB receiver is more strict. That is also a result of the wide signal bandwidth. More noise power is now presented in the signal bandwidth and the noise floor is high even at the receiver antenna. Therefore, the receiver needs to provide a good noise performance.

$$\begin{aligned} DR_{AVE_2 24Mbit/s} &= P_{RX} - Sensitivity = 10.7dB \\ DR_{AVE_4 48Mbit/s} &= P_{RX} - Sensitivity = 12.2dB \end{aligned} \tag{3.11}$$

2. UWB Baseband Modulation and Data Packets

For the baseband data modulation, the UWB supports various data rates as long as the signal bandwidth exceeds 500 MHz. Table VIII lists the characteristics of two most popular data transfer rates, 224 Mbit/s and 448 Mbit/s. The modulation formats adopted by the UWB systems include Pulse Position Modulation (PPM) [22], Pulse Amplitude Modulation (PAM) [23] and Phase Shift Keying (PSK) [24]. The common feature of these modulation formats is that the information is transmitted by a collection of narrow impulses with very low duty cycle (around 1%). Fig. 15 shows the UWB modulated signal in time domain.

PPM is based on the principle of encoding information with two or more positions

Table VIII. Baseband data modulation specifications for the multi-band UWB

Parameter	Value	Value
Symbol Rate	112 Mb/s	224 Mb/s
Raw bit rate	224 Mb/s	448 Mb/s
Coding rate	1/2	1/2
Bit error rate	$1e^{-5}$	$1e^{-5}$
Modulation	PPM/PSK/PAM	PPM/PSK/PAM
Required E_b/N_o	4.7 dB	4.9 dB

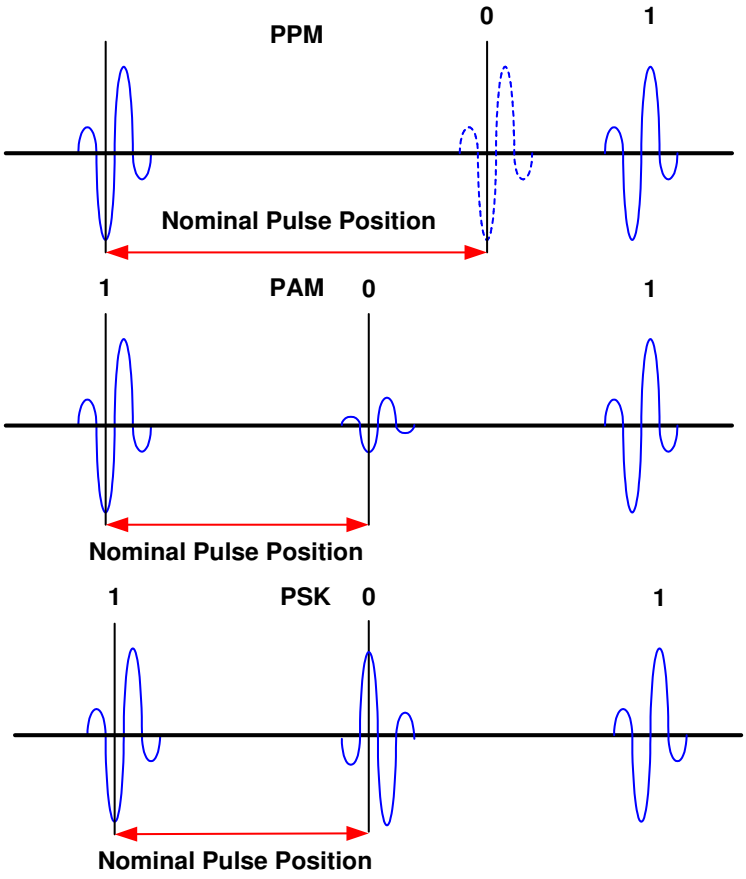

Fig. 15. UWB modulated signal in time domain

in time with respect to the nominal pulse position, as shown in the upper plot of Fig. 15. An impulse transmitted at the nominal position represents a "0", and a pulse transmitted after the nominal position represents a "1". The plot shows a two-position modulation, in which one bit is encoded in one impulse. Additional positions can be used to provide multiple bits per symbol data format. In the PPM, the time delay between positions is much shorter than the time between nominal positions to avoid interference among the impulses.

PAM is based on the principle of encoding information with the amplitude of the impulses, as shown in middle plot of Fig. 15. The plot shows a two-level modulation, "1" in higher amplitude and "0" in lower amplitude, respectively. More amplitude levels can be used to encode more than one bit per symbol data format.

In PSK modulation, information is encoded with the phase of the impulses, as shown in the lower plot of Fig. 15. If only two different phase is used, the polarity of the impulses can be switched to encode a "0" or a "1". More phase can be applied to the impulse for a multiple bit per symbol modulation.

Based on the baseband data modulation formats that we discussed above, Ti and Intel proposed to use Orthogonal Frequency Division Multiplexing (OFDM) to further modulate the transmitted signal. Using OFDM improves signal immunity to the channel interference and enhances security. However, OFDM also increases the complexity that involves in the received signal demodulation. Fortunately, the OFDM demodulation is conducted in DSP and is transparent to the receiver and its ADI design.

As we can see in Table VIII the E_b/N_o requirement for the signal demodulation is low, which means the demodulator is able to tolerate high noise level. That is a result of both the selection of the modulation formats and the process gain achieved by the proper coding.

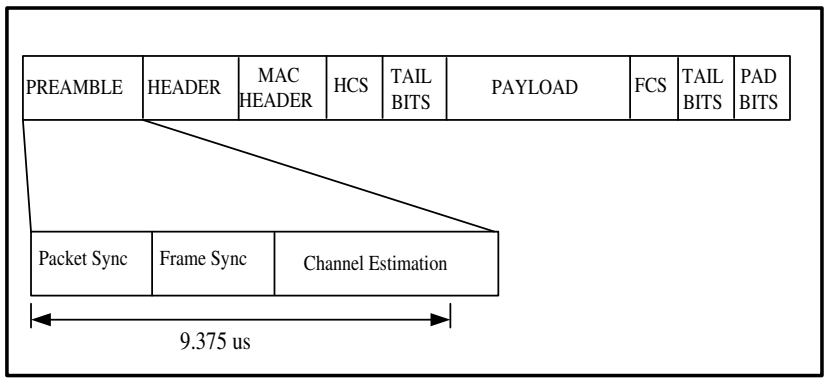

Fig. 16. UWB data packet format

The definition of the data packets for UWB is not unified. Different systems have their own formats for the data packets. Fig. 16 shows one of the proposed data packet [21]. The preamble period is 9.375 μS. Since the dynamic range of the received signal is small, the UWB receiver does not require sophisticated gain control circuit. Therefore, this period of time is enough for the whole receiver to settle.

3. Direct Conversion UWB Receiver Architecture

The UWB systems are often referred as a digital radio. The reason for that is that few baseband processing circuit blocks are actually needed in front of the ADI. The small received signal dynamic range allows the receiver to perform digitization even without AGC. Fig. 17 illustrates a block diagram for the UWB receiver. The most suitable receiver architecture is direct conversion due to the wide signal bandwidth. If a IF is applied in the receiver, the IF has to be at least higher than 250 MHz. This unnecessarily increases the circuit complexity and implementation cost by increasing baseband operating frequency. Besides, the wide signal bandwidth also relaxes the DC offset and flick noise effect in the direct conversion receiver since any interferences and noises at single frequency or small frequency band can not severely corrupt the

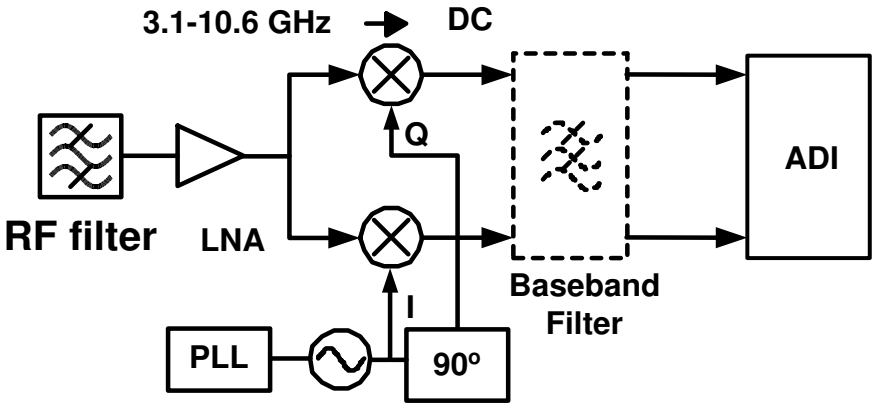

Fig. 17. The block diagram of a UWB receiver

desired signal. The ultimate goal of the UWB receiver is to place the ADI right after the antenna and LNA to form an ideal software defined radio. However, it requires the ADI to have a very high sampling rate. According to the Nyquist rules, the sampling rate of the ADC has to be at least twice of the signal bandwidth. Given a lowest carrier frequency of 3.1 GHz, the sampling rate for ADI has to be at least 6.2 GS/s. This is too high for current technology. Time-interleaved ADI structure has been considered as a solution. Even for such an ADI, the 21.2 GS/s sampling rate required for the highest 10.6 GHz carrier is also difficult to achieve. Sub-sampling technique may be applied for the ADI design, but the noise power will increase due to the aliasing caused by sub-sampling. This is not desired in a UWB system because the already stringent noise figure specs. Therefore, a down-conversion stage may still be needed in UWB receiver in the near future. An configurable RF filter is placed in front of the LNA to select the wanted band first and relax the linearity requirement for the receiver. Without the RF filter, any signal or interference in entire 7500 MHz bandwidth enters the LNA, it can easily saturate or desensitize the LNA. The baseband lowpass filter is optional depending the interference blocking performance of the RF filter.

Table IX. 802.11b and BT ADI design requirements

Specs	Bluetooth	802.11b
Modulation	GFSK	DPSK/QPSK/CCK
Data Rate	1Mbit/s	1/2/5.5/11 Mbit/s
BER	0.1%	0.001%
Preamble (Baseband Settling)	4-bit (μS)	72/144-bit (μS)
IF	2 MHz	DC
LO Offset	$\pm$100 kHz	$\pm$60 kHz

F. ADI Design in the Bluetooth and 802.11b/Bluetooth Receiver

In this research work, the ADI design for the Bluetooth and 802.11b/Bluetooth dual-mode receivers are further explored. Their implementation is conducted in transistor level and verified with the lab measurements. However, the ADI design for the UWB is discussed only at the system level. Its circuit implementation is not within the scope of this work since its standard is still under debate. The transistor level design for the UWB ADI is difficult to carry out without a clearly defined baseband specification. In the following chapters, only the ADI design for the Bluetooth and 802.11b/Bluetooth receivers will be discussed.

As discussed in the Chapter II, the ADIs in Bluetooth and 802.11b/Bluetooth receiver have different design focuses. In the Bluetooth ADI design, a fast settling is required to over come the problem introduced by the extremely short preamble. The LO frequency offset between the transmitter and receiver is another issue that needs to be addressed. For the 802.11b/Bluetooth dual-mode receiver, although the previous design concerns still exist in the ADI design for the Bluetooth receiving

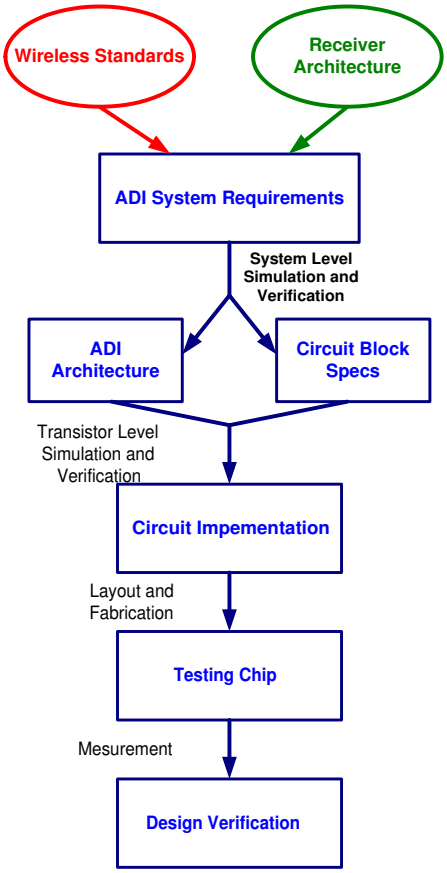

Fig. 18. The ADI design flow

mode, the compatibility issue is an more important design interest on the system level. In both cases, reducing power consumption and the silicon area of the ADI should be given priority in the system and circuit design. Table IX shows the ADI design requirement derived from the Bluetooth and 802.11b standards. The design of an ADI system follows the procedure that is illustrated in Fig. 18. In the Chapters IV and V, the entire design flow from architecture selection to the design verification for both Bluetooth and 802.11b/Bluetooth ADI will be presented.

The ADI design for Bluetooth and 802.11b receivers has been explored individually before. The ADI for a 802.11b/Bluetooth dual-mode receiver, however, is first studied in depth in this research work. ADC is often used as the ADI in the 802.11b receiver. The ADC for the 802.11b receiver is usually implemented with the baseband DSP. Few implementation has been reported in the literature. Table X shows some of the most recent reported ADI design for both Bluetooth and 802.11b receivers. The P_D and A_{Sil} are the power dissipation and silicon area for each design, respectively. The advantages and drawbacks of the proposed the ADI designs will be discussed with respect to these previous implementations. One important observation is that all the reported Bluetooth ADI implementations do not include the LO frequency offset cancellation circuitry. We need to consider this factor when calculating the overall ADI power consumption.

Table X. Reported ADI designs for Bluetooth and 802.11b receivers

References	Application	ADI Structure	ADI Performance	P_D (mW)	A_{Sil} (mm^2)
vanden2002 [25]	802.11b	Flash Interpolation ADC	8bit 200MSPS	655.00	3.36
newlogic2002 [26]	802.11b	Pipeline ADC	8bit 20MSPS	15.66	0.60
salva [27]	802.11b	Pipeline ADC	10bit 60MSPS	58.00	--
shi2002 [28]	802.11b	Pipeline ADC	8bit 20MSPS	6.00	0.33
This work	802.11b	Time-Interleaved Pipeline ADC	10bit 44MSPS	10.1	5.40
philips2003 [29]	Bluetooth	ΣΔ ADC	13bit 64MSPS	4.40	0.22
grilo2002 [30]	Bluetooth	ΣΔ ADC	13bit 32MSPS	12.00	1.00
samadian2003 [31]	Bluetooth	Phase Domain ADC	15.7dB SNR @0.1% BER	--	--
darabi2001 [32]	Bluetooth	Zero-Crossing Detector	18dB SNR @0.1% BER	8.10	--
park2003 [33]	Bluetooth	Delay Line Discriminator	20dB SNR @0.1% BER	3.60	2.40
huang2001 [34]	Bluetooth	Delay Line Discriminator	16.5dB SNR @0.1% BER	5.00	0.22
This work	Bluetooth	Zero-Cross Detector	16.3dB SNR @0.1% BER	9.00	0.70
This work	Bluetooth	Pipeline ADC	11bit 11MSPS	7.40	2.70

G. ADI Design in the UWB Receiver

One problem encountered in the wideband systems design is the large noise power presented in the system. The noise power at a receiver antenna matching to a 50 Ω resistance can be calculated as

$$P_N = -174dBm + 10log_{10}(BW) \tag{3.12}$$

where BW is the bandwidth of the signal. For the 500 MHz UWB signal, the noise power obtained from (3.12) is -87 dBm. This high noise floor at the antenna results in a low SNR in the demodulator even after a very careful noise design in the receiver. Referring to Table VII and using the 224 Mbit/s data receiving mode as an example, the sensitivity requirement in that case is -77.2 dBm, which gives us a minimum input SNR_i ($Sensitivity - P_N$) of 9.8 dB at the receiver antenna. Given a receiver Noise Figure (NF) of 6.6 dB, the The minimum SNR at the output of the receiver (SNR_{RX}) can be derived as

$$SNR_{RX} = SNR_i - NF = 9.8 - 6.6 = 3.2dB \tag{3.13}$$

At this small SNR level, the random noise power at some frequency or time points can easily exceed the signal power. To overcome this hurdle, robust modulation formats, such as PPM, PSK and PAM, are applied in UWB systems. Furthermore, sophisticated coding schemes are also used in the UWB systems to provide processing gain in the baseband data processing. As a result, the received data detection is preferred to be performed in digital domain and an ADC is used as the ADI for the receiver.

Unlike in the narrow band receiver, the quantization noise of the ADC does not limit the overall receiver noise performance. The SNR of an ADC due to the

quantization error can be formulated as [35]

$$SNR_{ADC} = 6.02N + 1.76 \quad dB \tag{3.14}$$

where N is the number of bits used by the ADC. Comparing to the 3.2 dB SNR at the output of the receiver, even a 1-bit resolution ADC can provide a quantization noise power below the receiver noise floor. The dynamic range of the ADC, DR_{ADC} is determined not only by the quantization error requirement but also by the signal dynamic range in front of the ADC. If the quantization noise floor is required to be $S/N_{quan.}$ dB lower than the signal power, the ADC dynamic range specs can be derived as

$$DR_{ADC} = S/N_{quan.} + DR_{sig} + Design\ Margin \tag{3.15}$$

According to (3.11), the average dynamic range of the received signal is around 10 or 12 dB. Even without gain control module in the receiver, a 6-bit ADC is able to provide big enough dynamic range [19] to include design margin and possible peak in the received signal power level. This requirement can be further relaxed to 4-bit or even less by employing simple gain control schemes [36]. The resolution and dynamic range specification is not a problem for the ADC design, however, the sampling rate requirement for the ADC is tough. The UWB baseband signal has a bandwidth of 250 MHz. According to the Nyquist rule, the sampling rate of the ADC needs to be at least 500 MHz. The state of art ADC design in CMOS technology is able to provide a 6-bit resolution at a sampling rate over 1.1 GS/s [37]. Therefore, the 500 MS/s sample rate is achievable in the ADC design. However, the power consumption in those ADCs is usually around several hundred mW and is unaffordable in the portable devices. Table XI summarize the requirements for the UWB ADC, where ENOB stands for the effective number of bits.

Table XI. ADC specification for a UWB receiver

Parameter	Value
Dynamic Range	20-30 dB
ENOB	4-6-bit
Sampling Rate	500 MS/s
Signal bandwidth	250 MHz
Power Consumption	Minimum

To implement the ADC with such high speed, the flash/flash interpolation ADC architecture is the best choice. A flash/flash interpolation ADC is able to achieve high speed due to the parallel comparison and distributed sampling mechanism. The principle of these tow ADCs will be introduced in Chapter V Section C. Other ADC structure has also be proposed for the UWB systems, such as the time-interleaved ADC [38]. Fig. 19 shows the block diagram of such an ADC. The ADC consists M identical ADC branches. Each ADC branch is an individual ADC and can use any available ADC structures, such as flash or pipeline. All the ADC branches has a sampling rate of f_S/M and operate in a time-interleaved fashion. This gives an overall sample rate of f_S for the time-interleaved ADC. Since each ADC branch works at only a fraction of the required sampling rate, the specs for those ADC branches can be much relaxed. Unfortunately, the time-interleaved ADC suffers from the performance degradation caused by mismatching, phase skewing and coupling among the branches. Special measures need to be taken in the circuit level design to suppress those negative effects. Therefore, in the relatively low speed multi-band UWB systems, the flash/flash interpolation ADC is preferred for the ADI design because of its straightforward implementation. The time-interleaved ADC structure, however, has a potential of achieving even higher speed and can be a good candidate

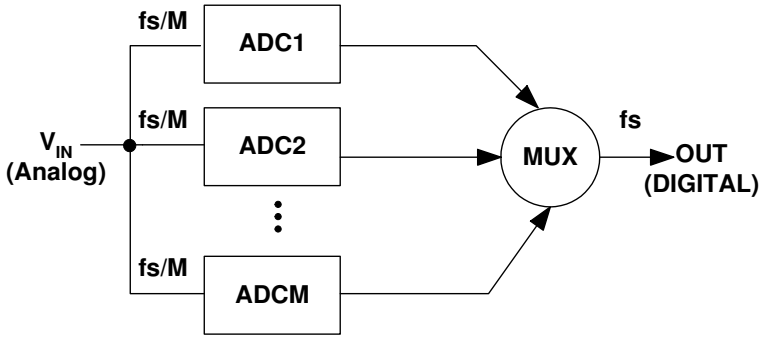

Fig. 19. The block diagram of a time-interleaved ADC

for the single-band UWB receiver ADI design.

Another new wide band ADC architecture that is currently under active research is the frequency channelized ADC. Its structure is illustrated in Fig. 20. The frequency channelized ADC also adopted parallel processing principle to accommodate wide input signal bandwidth. Instead of perform parallel mechanism in time domain, as implemented in the time-interleaved ADC, it channelizes the input signal and processes signal at different frequency at the same time. As shown in Fig. 20, the input signal is mixed with Local Oscillation (LO) signal at different frequencies. This mixing operation shifts different band of input signal to DC. Lowpass filters follow the mixers to channelized the frequency shifted input signal. Only one band of the input signal goes to the ADC. ADCs then only need to process a portion of the input signal. Fig. 21 shows the processing of the frequency channelized ADC in frequency domain. If the input signal, f_{SIG}, is divided into M channels, each ADC only needs to process a signal with bandwidth of $\frac{1}{f_{SIG}}$. Therefore, the specs for each individual ADC is relaxed. At the ADC system level, the power consumption can be largely reduced. However, the frequency channelized ADC also has its problems. Firstly, a set of mixers and filters are added into the ADC. Although the mixers and filters can be realized by passive components and therefore consume little power, they

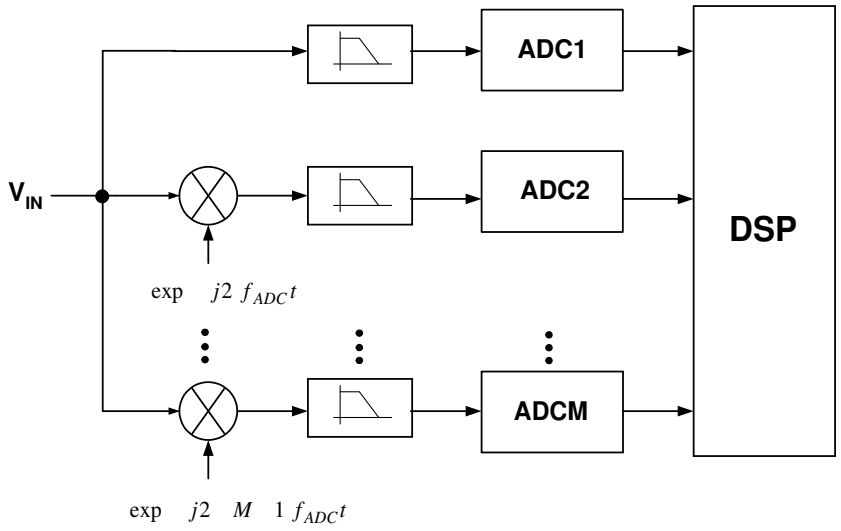

Fig. 20. The block diagram of a frequency channelized ADC

still increases design complexity and silicon area of the ADC. Secondly, signal swing usually is large at the input of the ADC, the linearity requirement for the mixer and filter is high since they need to provide better linearity than the ADC. Thirdly, the phase noise in the LOs may raise the noise floor of the ADC. Lastly, there could be folded-in noise and jitter issues because of the mixing. Fortunately, all those issues only become performance constrains when designing for high resolution ADCs. For the UWB system, the ADC dynamic range requirement is usually only 4-6 bit. The frequency channelized ADC provides an attractive solution for the UWB ADI design.

Power consumption optimization is always a major concern in the high speed ADC design. As mentioned before, currently the ADC with a speed high than 500 MS/s usually consumes several hundred mW in power. How to lower the ADC power dissipation becomes a major research interest in the ADI design for the UWB receivers.

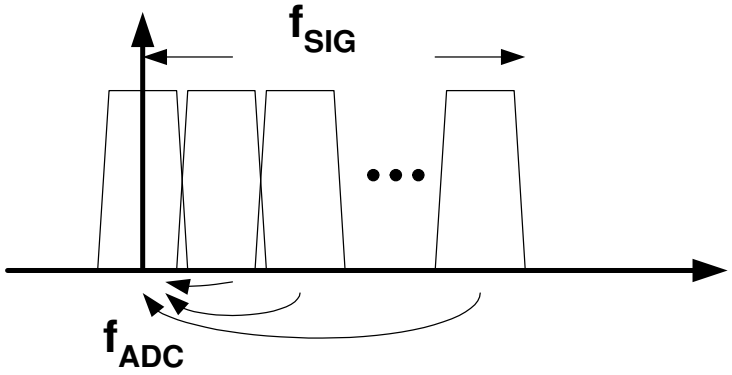

Fig. 21. Frequency domain explanation for the frequency channelized ADC

CHAPTER IV

ADI DESIGN FOR THE LOW-IF BLUETOOTH RECEIVER

The ADI design for the low-IF Bluetooth receiver is an example of the ADI implementation in a short-preamble wireless system. The system consideration, ADI design approach and circuit implementation for this particular type of system are discussed in this chapter.

A. The Characteristics of Bluetooth GFSK Modulation and Its Detection

System level simulation is conducted in the matlab to determine the specs and the best architecture for the ADI in the Bluetooth receiver. The summary of the baseband detection requirements are listed in Table IX.

1. Bluetooth GFSK Signal

The Bluetooth system adopts Gaussian Frequency Shift Keying (GFSK) modulation format with a data transfer rate of 1 Mbit/s and a nominal frequency modulation index of 0.32 [11]. The Bluetooth baseband data packet is in the form of bit streams. Its square pulses are first shaped by the Gaussian filter to limit the bandwidth and then applied to a Frequency Modulation (FM) circuit to generate the GFSK modulated signal. Fig. 22 illustrates the block diagram of one implementation for the

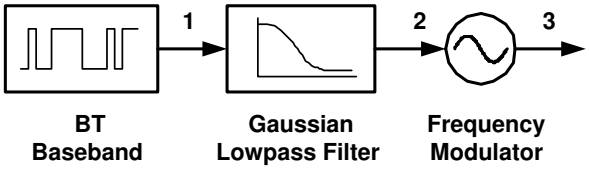

Fig. 22. The block diagram of a GFSK modulator

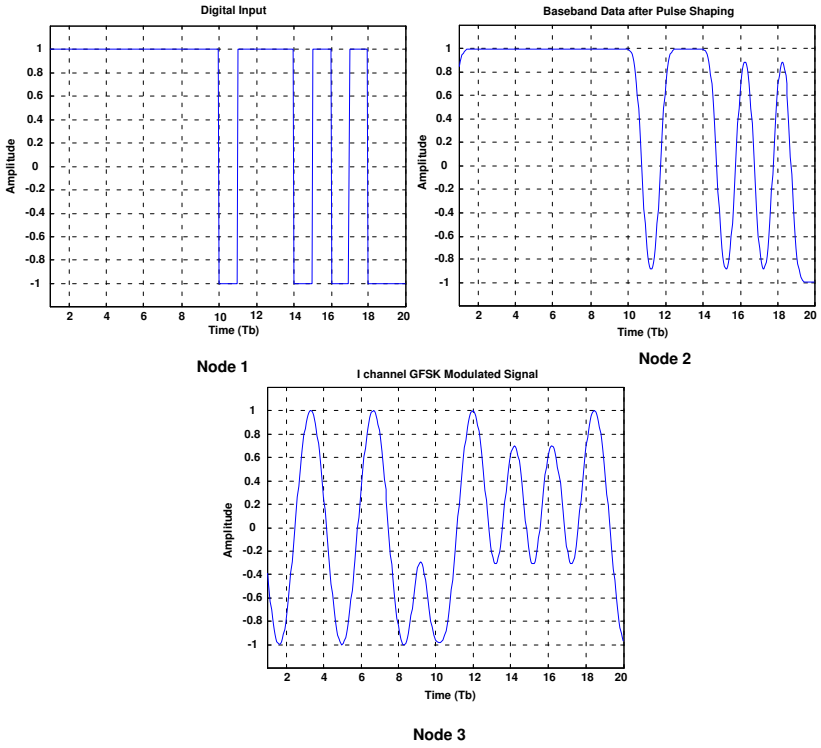

Fig. 23. The time domain signal waveform at internal nodes of a typical GFSK modulator

Bluetooth GFSK modulator. In the receiver and ADI design, we are only interested in the received signal detection. However, we need the knowledge of the Bluetooth GFSK modulated signal in order to provide correct signal demodulation. Equations in (4.1) show the mathematical expression of a Bluetooth GFSK baseband complex envelope [39] [40]. In those equations, $\boldsymbol{b}$ is the vector of the unmodulated baseband data bit stream, $[b_0, b_1, ..., b_i, ...]$; $g(t)$ is the time domain output pulse function of a Gaussian lowpass filter when a square pulse is applied to its input, its property is determined by the product of the absolute filter bandwidth B and the symbol duration T; $q(t)$ is the corresponding phase function of $g(t)$, it is obtained by integrating $g(t)$; $\varphi(t, \mathbf{b})$ is the phase of the modulated GFSK signal, the frequency modulation depth is controlled by the modulation index ρ, which is from 0.28 to 0.35 according to the Bluetooth standard; $S(t, \mathbf{b})$ is the transmitted signal. Fig. 23 shows the time domain signal waveform at each node in the GFSK modulator.

$$
\begin{aligned}
S(t,\mathbf{b}) &= exp(j\varphi(t,\mathbf{b}) \\
\varphi(t,\mathbf{b}) &= 2\rho\pi \sum_{i=-\infty}^{\infty} b_i q(t-(i-1)T) \\
q(t) &= \int_{i=-\infty}^{t} g(\tau)d\tau \\
g(t) &= \frac{1}{2T}\left\{Q\left(\frac{2\pi BT}{\sqrt{\ln(2)}}\left(\frac{t-T/2}{T}\right)\right) - Q\left(\frac{2\pi BT}{\sqrt{\ln(2)}}\left(\frac{t+T/2}{T}\right)\right)\right\} \\
Q(x) &= \int_{x}^{\infty} \frac{1}{\sqrt{2\pi}} exp\left(-\frac{u^2}{2}\right) du
\end{aligned}
\tag{4.1}
$$

From its mathematical expression, we can see several interesting properties of the Bluetooth GFSK signal. Firstly, Bluetooth GFSK signal has a constant envelop in magnitude and its phase is continuous in time domain. The continuous-phase

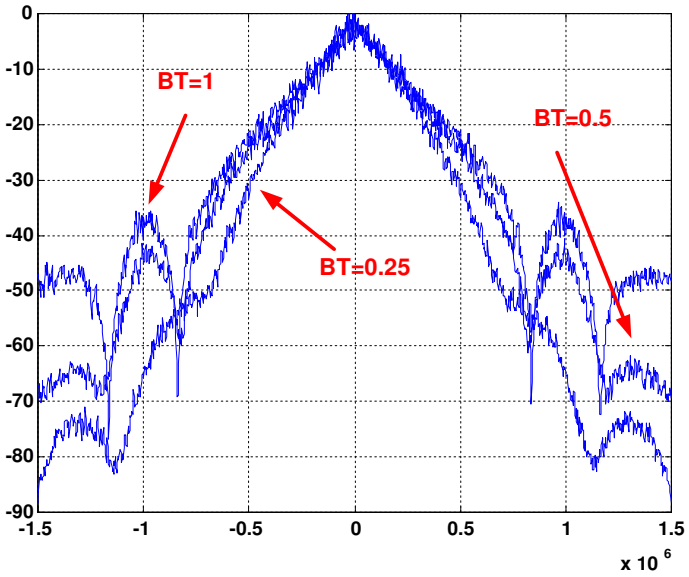

Fig. 24. The power spectrum density of the GFSK signal with different BTs

frequency modulation character of the Bluetooth GFSK signal allows the usage of FM demodulator in the received signal detection. In the frequency domain, the bandwidth of the Bluetooth GFSK modulated signal is limited by the Gaussian pulse shaping to assure minimum signal power spilling among adjacent channels. As we have seen in Fig. 7, 99% of the total Bluetooth GFSK signal power is contained within a 430 kHz bandwidth. Unfortunately, the Gaussian shaping expands the symbol duration in the time domain. The power of the adjacent bits extends into the current bit duration and thus introduce the Inter-Symbol Interference (ISI) . To achieve an optimal signal detection, sequence detectors are needed to process the adjacent bits together. Symbol-by-symbol detectors simply disregard the existence of the ISI and hence degrade the receiver performance. How much degradation that the ISI can cause in the symbol-by-symbol detectors is still a research interest because of the low implementation cost of those detectors. If the degradation is not severe, the simple symbol-by-symbol demodulator will be preferred in the Bluetooth receiver design.

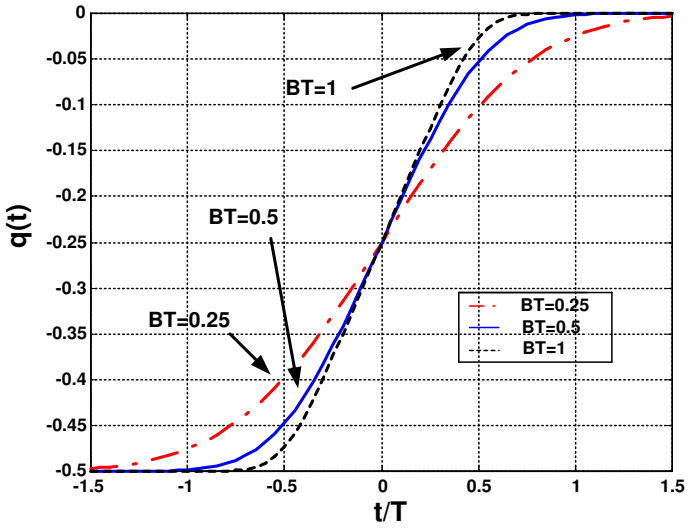

Fig. 25. The $q(t)$ of the GFSK signal with different BTs

The level of the ISI in a GFSK signal is determined by the product of BT in the phase function, $q(t)$. As the value of BT varies from 0 to 1, the frequency bandwidth of the corresponding GFSK signal expands while the time domain duration decreases. Fig. 24 and 25 shows the power spectrum density and $q(t)$ of the GFSK signals with different BTs, respectively. As we can see in Fig. 25, $q(t)$ becomes constant as it moves away from the current bit duration. The ISI caused by the current bit is generated by the transition part of the $q(t)$ that enters the adjacent bits durations. The larger the BT value is, the steeper the slope of $q(t)$ is and the less interference power is ejected into the neighboring bits. However, the increased signal bandwidth due to larger BT raises the power level of the adjacent channel interference, as illustrated in Fig. 24. The Bluetooth standard carefully select the BT to be 0.5 such that it provides a good compromise between frequency bandwidth and symbol duration. The $q(t)$ of $BT = 0.5$ only extends to the closest two bits. Therefore, the ISI in the Bluetooth signal is not too severe. The expected performance degradation that is caused by a symbol-by-symbol (bit-by-bit) Bluetooth detector can be around 1 or 2 dB.

2. The Detection of the Bluetooth GFSK Signal

A Bluetooth GFSK signal can be demodulated either in the digital [40]-[42] or analog domain [43]-[53]. The selection of the demodulation scheme dictates the ADI design in the low-IF Bluetooth receiver. In this subsection, we will discuss the implementation and performance of different GFSK demodulators. Their effects on the ADI design will be analyzed in the next section. The demodulation circuits that are examined here include the optimum no-coherent detector and other analog FM demodulator. The received signal is modelled by transmitting the Bluetooth GFSK modulated signal through an Additive Gaussian White Noise (AGWN)channel.

◇ *Optimum non-coherent detector*

Due to the existence of the ISI, a viterbi detector can be employed to provide optimal data detection performance. Fortunately, the ISI of the Bluetooth GFSK signal is limited in the most adjacent two bits, the complex viterbi detector can be approximated by a sequence detector as illustrated in Fig. 26. The received signal is first correlated with a bank of correlators (match filters). The match filters are formed by the complex conjugates of all the possible combination a 3-bit modulated data sequence. Then the sequence detector will choose in favor of the data sequence $\boldsymbol{b}$ that maximizes the metric given below [40] as the detected data sequence. In equation (4.2), $R(t)$ is the received signal, and $S^*(t, \mathbf{b})$ is the complex conjugate of the transmitted signal that is defined in (4.1).

$$\Lambda(\boldsymbol{b}) = |\frac{1}{T}\int R(t)S^*(t, \boldsymbol{b})dt|^2 \tag{4.2}$$

Since there are in total 8 possible combinations for a 3-bit sequence, 8 match fil-

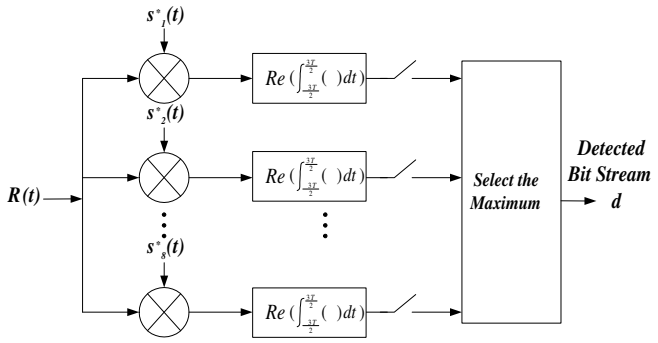

Fig. 26. The block diagram of an optimum non-coherent GFSK detector

ters are needed in the optimum non-coherent detector. Obviously, the optimum non-coherent GFSK detector is preferred to be realized in the digital domain due to the cost and complexity involved in its circuit implementation. In addition, the optimum non-coherent detector can only process baseband signals. A second downconversion is needed in the low-IF Bluetooth receiver to convert the received signal from IF to DC, which increases the circuit complexity in the receiver.

◇ *Frequency discriminator*

Frequency discriminators are widely used in the demodulation of FM signals [43]-[45]. By nature, it is a symbol-by-symbol detector. In a frequency discriminator, a resonant circuit provides a linear amplitude versus frequency response to convert the frequency information into voltage variation. Fig. 27 shows the block diagram of a frequency discriminator. The frequency discriminator is preferred to be used in those deep modulated FM systems. Unfortunately, the modulation index of the Bluetooth GFSK signal is only 0.28-0.35, which results in a small frequency variation in the modulated signal. To assure the demodulation performance, a high quality factor (Q) is required in the resonant

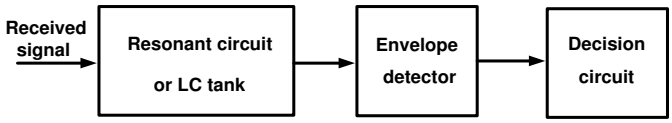

Fig. 27. The block diagram of a frequency discriminator

circuit to provide adequate sensitivity. This high Q ($Q > 10$) requirement make it difficult to integrate the inductor of the resonant circuit on chip. Furthermore, the 2 MHz IF of the Bluetooth receiver results in large inductance and capacitance for the resonant circuit, which consumes large silicon area in the circuit implementation.

◇ *Phase Lock Loop (PLL) based FM demodulator*

The core of this demodulator is a PLL, as shown in Fig. 28 [43] [46] [47]. In the PLL circuit, the phase detector detects the frequency variation in the received signal through the phase difference between the incoming signal and output of the Voltage Control Oscillator (VCO). After proper amplification and filtering, a control voltage at output of the lowpass filter is applied to the VCO to adjust its oscillation frequency until the VCO frequency locks to the received signal frequency. Therefore, the control voltage of the VCO is related to the frequency of the received signal. PLL based demodulators are also symbol-by-symbol detectors. Several factors limit the detection performance of this type of GFSK demodulators. Firstly, PLLs require certain amount of time to settle to the desired frequency, which is called settling time in the PLLs. For a quickly changing FM signal, the detection performance of a PLL based demodulator is poor since the PLL is not fast enough to follow the input signal. Another factor that degrades the detection performance of this demodulator is the VCO phase noise. This phase noise directly raises noise floor of the received signal

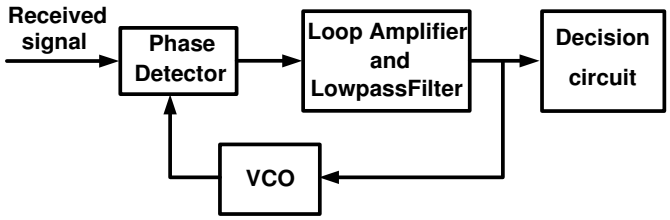

Fig. 28. The block diagram of a PLL based demodulator

and affects the data detection. $\Sigma\Delta$ modulator has been introduced into the PLL circuit to improve the detection performance [46] [47]. As a consequence, the implementation cost and power consumption significantly increases.

◇ *Differential or delay line discriminator*

The Differential or delay line discriminators are also symbol-by-symbol GFSK demodulators. There are several different implementations for the differential or delay line discriminators [48]-[32], such as one symbol delayed [48], two symbol delayed [50] and quadrature differential demodulator [32]. The principle behind all of them is the same, the received signal is multiplied with a delayed version of itself to detect the phase difference that is accumulated during the time interval equalling to the delay. The phase difference, which contains the frequency variation information in the delay period, is used to determine the received bit. A quadrature (I,Q) structure, as shown in Fig. 29, is often used in the delay line discriminators to improve the detection performance since it utilizes the information in both signal channels. Using the notation in equation (4.1), we can define the quadrature outputs of the channel select filter as

$$I(t) = A\cos(\omega_C t + \varphi(t, \mathbf{b}) \tag{4.3}$$

$$Q(t) = A\sin(\omega_C t + \varphi(t, \mathbf{b}) \tag{4.4}$$

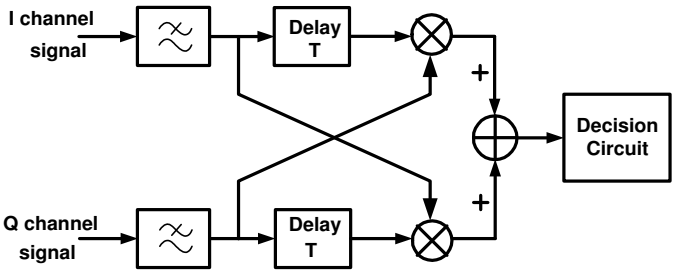

Fig. 29. The block diagram of a delay line discriminator

where *I(t)* and *Q(t)* are the received signal in I and Q channels, respectively. By delaying both branches by 1 bit interval and multiplying with the opposite channel, the output of the discriminator yields

$$\begin{aligned} V_{out}(t) &= I(t)Q(t-T) - I(t-T)Q(t) \\ &= A^2 \sin(\Delta\varphi) \qquad (4.5) \\ \Delta\varphi &= \varphi(t-T, \mathbf{b}) - \varphi(t, \mathbf{b}) \qquad (4.6) \end{aligned}$$

Since $\Delta\varphi$ contains information about the phase variation in one bit interval, we can detect each bit based on that information. The main difficulty for this structure is to achieve accurate and matched time delays in both I and Q channels. On-chip tuning may be needed for the delay circuit design.

◇ *Zero-crossing detector*

Fig. 30 illustrates a conventional zero-crossing detector [51]-[53]. For an FM signal, the change of frequency results in the variation in the number of the zero-crossing points in a certain period time. The zero-crossing detector detects GFSK modulated signal by using this principle. A limiter first amplifies and clips the received signal turning it into a frequency-modulated square wave. Then the square wave is differentiated and each zero-crossing point generates

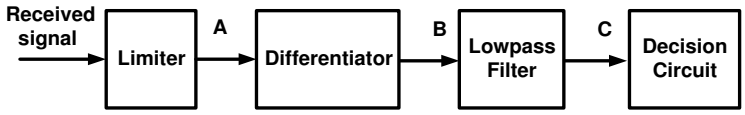

Fig. 30. The block diagram of a zero-crossing detector

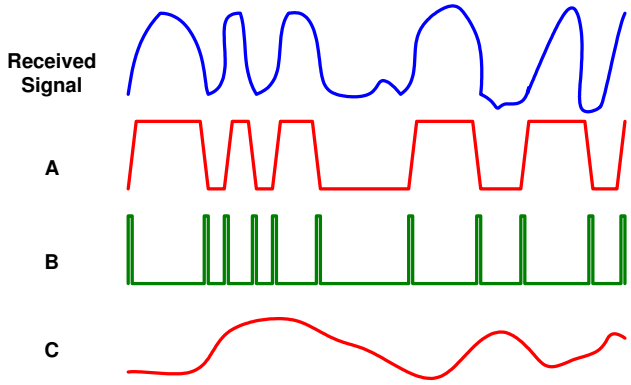

Fig. 31. The transient voltage changes in the zero-crossing detector

a pulse at the output of the differentiator. A lowpass filter finally averages the energy power of the pulse train. Thus, the pulse density, which carries the frequency modulation information, is converted into a voltage variation. Fig. 31 shows the voltage waveforms at each nodes in the zero-crossing detector.

In some zero-crossing detectors, the lowpass filter is replaced by a counter. The counter counts the number of the pulses in each symbol durations and hence detects the frequency variation in the received signal. This type of zero-crossing detector usually provides better performance for the deep modulated FM signal and is not suitable for the Bluetooth application. The frquency modulation index used in the Bluetooth GFSK signal is small. Considering an IF of 2 MHz, the frequency of a Bluetooth GFSK modulated signal varies between 1.825 MHz to 2.175 MHz. In term of the number of the zero-crossing points in one symbol

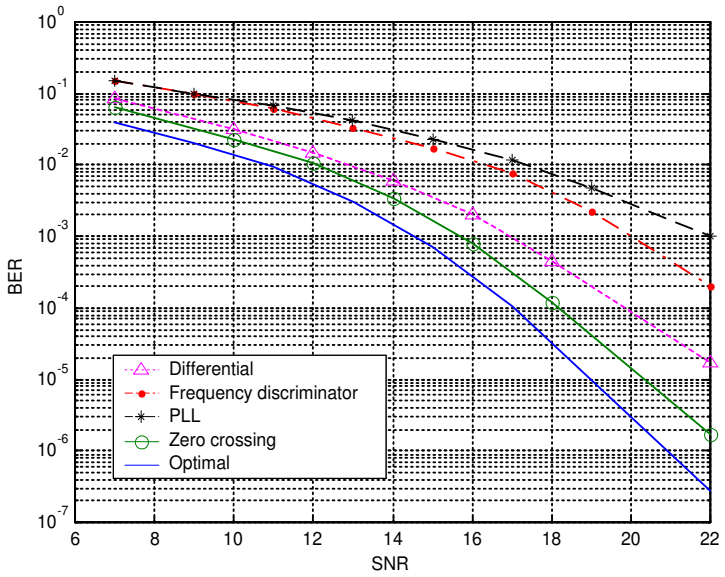

Fig. 32. Matlab simulated BER performances of different demodulators

duration (1 μs) the difference is smaller than 1. Therefore, the counter cannot tell the difference between the high and low frequencies of the GFSK signal. Lowpass filter, on the other hand, averages the energy power in the pulse train and is still able to show the frequency differences in the received signal in the form of voltage changes.

Five GFSK demodulators are examined in this subsection. The optimum non-coherent demodulator is a sequence detector and all the other four demodulators are symbol-by-symbol detectors. Their detection behaviors are simulated in matlab. The matlab code for each GFSK demodulator is included in Appendix A. Fig. 32 shows the Bit Error Rate (BER) vs Signal-to-Noise Ratio (SNR) performance of each demodulator. Although the performance of the symbol-by-symbol demodulators degrade from the optimum non-coherent demodulator, they provides inexpensive implementations that are desirable in the Bluetooth receiver. The BER performances of the PLL based demodulators, the frequency discriminator and the delay line dis-

criminator are relatively poor. The zero-crossing detector, however provides the best BER performance among the symbol-by-symbol demodulators and only has less than 0.8 dB degradation in comparison with the optimum case. This is a factor that needs to be considered in the ADI design for the low-IF Bluetooth receiver.

B. ADI Design Approach for the Low-IF Bluetooth Receiver

In a Bluetooth GFSK optimum non-coherent detector, a bank of matching filters and a viterbi decision circuit are needed. Those circuits must be realized in hardware in the analog demodulator approach. The cost of implementation and circuit complexity are too high for the practical design. On the contrary, the digital domain implementation of the optimal non-coherent GFSK detector appears to be much cheaper and easier, although an ADC has to be placed in front of the digital demodulator to digitize the received analog signal. Therefore, in the Bluetooth ADI design, the ADC approach is associated with the optimum non-coherent demodulator. In this section, three possible ADI architectures for Bluetooth receiver are discussed considering both the receiver performance and implementation cost.

1. ADC+AGC Approach for the low-IF Bluetooth Receiver

In a conventional receiver architecture, a combination of AGC and ADC circuits (AGC+ADC) are used in the baseband signal processing and digitization [54]. Fig. 33 shows the block diagram of a typical receiver that adopts this type of baseband design. The function of the AGC is to provide programmable signal amplification for different received signal power levels. Hence the signal dynamic range in front of

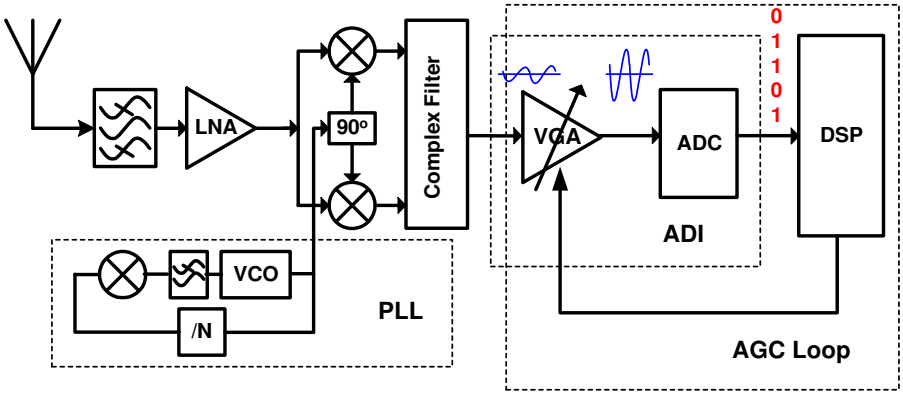

Fig. 33. The block diagram of a Bluetooth receiver using AGC+ADC ADI structure

the ADC is limited to such an extent that the signal power will not be too small for the ADC to detect, nor will it be too big and saturate the ADC. For instance, when the received signal is strong, the AGC provides lower gain; when the received signal power is small, higher gain is used in the ADC. The AGC circuit usually contains a Variable Gain Amplifier (VGA) and a gain control loop. The AGC gain control loop is used to detect the received signal strength and control the gain in the VGA.

The AGC+ADC structure is welcomed by many ADI designers because of the relatively relaxed circuit specs and flexibility in design. By carefully distributing the specs between AGC and ADC, both circuits can be realized with simple designs. Furthermore, the severe LO frequency offset that presents in the Bluetooth system can be accurately compensated in the digital domain before the data detection. However, one prominent feature of the Bluetooth data packets is its short preamble (4 bits) [11], which leads to an extremely short settling time requirement (4 μS) for the AGC gain control loop. In the receiver of Fig. 33, an ADC and a DSP are also located in the AGC gain control loop besides the VGA. The gain adjustment in the VGA is controlled by a digital word that is generated in the baseband signal processing module in the DSP. Therefore, the total delay in the AGC gain control loop is consist

of the delay in the VGA, ADC and DSP. Considering the clock cycles that is needed for the DSP to process signal power level detection and gain control word generation, a very high speed DSP must be applied in the Bluetooth receiver. The corresponding cost is not desired in the Bluetooth system design.

The gain control loop in a AGC circuit can also be implemented in the analog domain. The same delay issue, however, still exists. Some attempts have been made to provide fast settling for the Bluetooth AGC, such as distributing the gain control in several stages [54] and/or using feedforward algorithm [55]. Unfortunately, these approaches either complicate the system or introduce significant power consumption.

Although the AGC+ADC ADI structure has performance advantages, such as potential of using the optimum non-coherent demodulator and the precise LO frequency offset cancellation in the digital domain, it suffers the from design difficulties caused by the extremely fast settling requirement in the AGC. High implementation cost including both circuit complexity and power consumption may be involved in the circuit level design.

2. Single ADC Approach for the low-IF Bluetooth Receiver

Since the settling time requirement is so difficult to achieve in the AGC design, the entire AGC circuit is taken out in some previously reported Bluetooth receivers [56] and results in a receiver architecture that is shown in Fig. 34.

In this single ADC ADI structure, the absence of the AGC assures the fast settling in the baseband. However, the ADC dynamic range requirement is tightened as a result. Without the gain adjustment in the AGC, the ADC will directly see the large variation in the received signal power. The Bluetooth standard specify a maximum received signal power of -10 dBm, and a -80 dBm sensitivity specification

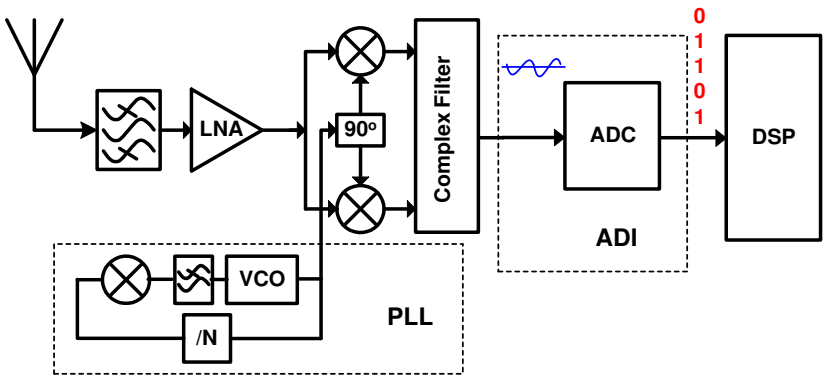

Fig. 34. The block diagram of a Bluetooth receiver using single ADC ADI structure

is often applied in the practical Bluetooth receiver design. That gives us a 70 dB signal dynamic range. The ADC must provide a dynamic ranger larger than this 70 dB requirement to assure the sensitivity and linearity performance of the receiver. As in the reference [56], an ADC with 80 dB dynamic range is designed for the receiver. Consequently, the ADC consumes nearly 40% of the total receiver power dissipation and occupies an area twice as the RF frontend.

As the AGC+ADC ADI structure, the signal ADC ADI design enjoys the performance superiority since it can also be used with the optimum non-coherent demodulator and digital domain LO offset cancellation. The avoidance of the AGC brings both advantage and drawbacks. The receiver and ADI architecture is simplified and the difficult settling time specs is avoided in the design while the implementation complexity and power consumption of the ADC increases significantly.

3. Hardware Demodulator of the ADI for the low-IF Bluetooth Receiver

Hardware demodulator can also be used in the Bluetooth ADI design [43]-[53]. The block diagram of a Bluetooth receiver that uses analog demodulator ADI structure are illustrated in Fig. 35. The hardware implementation cost of an analog optimum non-

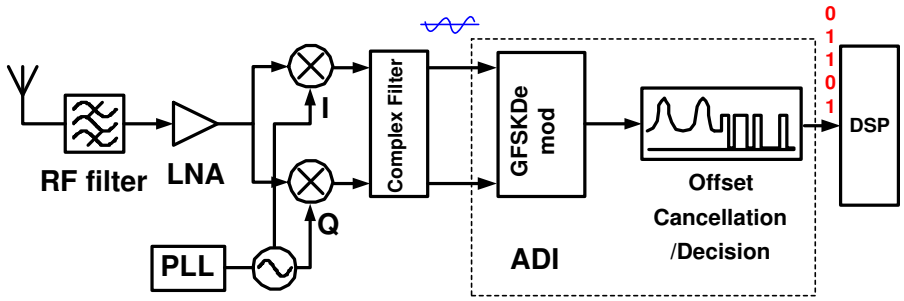

Fig. 35. The block diagram of a Bluetooth receiver using single analog demodulator ADI structure

coherent GFSK demodulator is too high. Moreover, the process variation will also degrade and ultimately limit the detection performance of an optimum non-coherent demodulator. Therefore, we only consider the symbol-by-symbol detectors that we have discussed in the subsection 2 of the section A.

Although the symbol-by-symbol hardware demodulator often provides inexpensive and straightforward implementation for ADI in a receiver system, they are generally ignored in the digital communication systems design due to their relatively poor detection performance. Fortunately, the small ISI in the Bluetooth GFSK modulated signal limited the performance degradation caused by the symbol-by-symbol detection scheme. As revealed by the matlab simulation (Fig. 32), the zero-crossing detector only has 0.8 dB degradation in the BER performance comparing to the optimum non-coherent demodulator. In the receiver design, the Noise Figure (NF) requirement of the RF frontend has to be 0.8 dB smaller to compensate this raise in the demodulator SNR specs. Considering the fast settling performance and the power and silicon saving gained by skipping the AGC and ADC, we may even reduce overall implementation cost for the receiver. Therefore, the analog hardware demodulators can still be candidates for the the Bluetooth ADI design as long as the price for achieving a smaller NF RF frontend is affordable in the design.

4. The Selection of the ADI Structure for the low-IF Bluetooth Receiver

Three ADI design approaches have been presented in the previous subsections. The AGC+ADC and single ADC approaches provides better detection performance and LO offset cancellation property since both the data detection and offset cancellation can be conducted in the digital domain. However, these two approaches suffers from a high implementation cost and power consumption in the circuit design. The AGC+ADC ADI structure faces the design difficulties and cost issues caused by the fast settling requirement of the AGC. The single ADC approach avoids the AGC settling problem by complicates the ADC design. Although the optimum non-coherent GFSK demodulator is too expensive to be implemented in the analog domain, other hardware demodulators, such as the simple symbol-by-symbol demodulators, demonstrate reasonable detection performance compared to the optimum non-coherent detection. Their simple circuit implementation and low power consumption is desired in the Bluetooth receiver design. Therefore, the analog demodulator approach, specifically, the zero-crossing detector, is chosen for the ADI design in the low-IF GFSK receiver as a good balance between performance and implementation cost.

Besides the digitization of the received signal, the Bluetooth ADI also need to compensate the LO frequency offset between the transmitter and receiver. The entire ADI for the Bluetooth low-IF receiver is depicted in Fig. 36. It is consist of three parts, the zero-crossing detector, the DC offset cancellation circuit and the the decision circuit. Using the zero-crossing detector, the large LO frequency between transmitter and receiver in the Bluetooth systems is converted into a DC offset voltage. Since this DC offset voltage varies from time to time, it must be cancelled before the bit detection. In section C, the circuit implementation of the zero-crossing detector is presented, the circuit of the demodulator lowpass filter is discussed in section D,

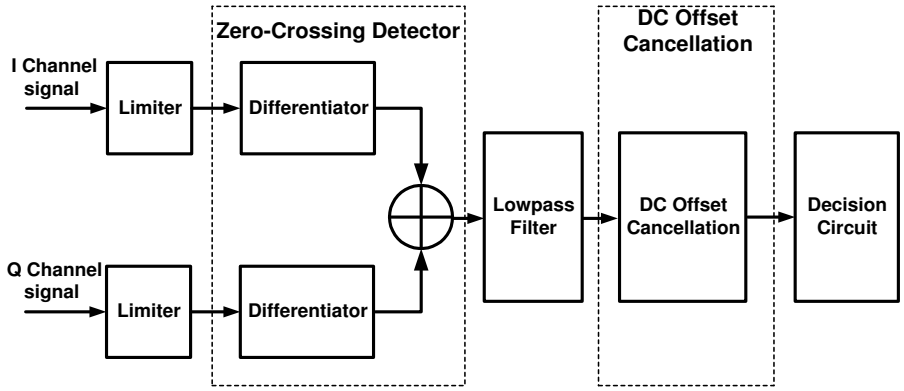

Fig. 36. The ADI architecture for the Bluetooth low-IF receiver

the DC offset cancellation structure is described in section E and finally the decision circuit is depicted in section F.

C. Zero-Crossing Detector Circuit Design

The conventional zero-crossing detector is illustrated in Fig. 30. In the matlab simulation for the zero-crossing detector, both I and Q channels are used to improve the detection performance with respect to the single channel detection. The quadrature zero-crossing detector is depicted in Fig. 37. In the Bluetooth low-IF receiver (Fig. 35), I and Q channels have independent signal and noise path. It is reasonable to assume the noise in the I and Q channels are uncorrelated. Using both I and Q channels in the signal detection does not improve the SNR. However, the the number of zero-crossing point is doubled comparing to the single channel signal detection due to the the 90 degree phase delay between I and Q channels. In the matlab simulation, the performance of the quadrature zero-crossing detector is around 2 dB better than the single channel zero-crossing detector. In this section, we will introduce a modified GFSK zero-crossing detector and its circuit implementation. The zero-crossing detector of the Bluetooth ADI is formed by a bank of edge detectors, a shape keeping

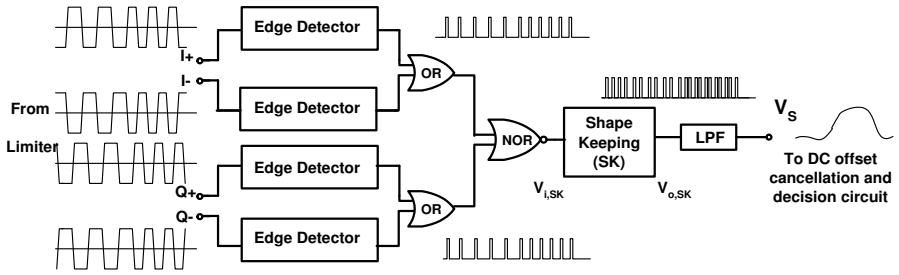

Fig. 37. The proposed zero-crossing detector for Bluetooth GFSK signal

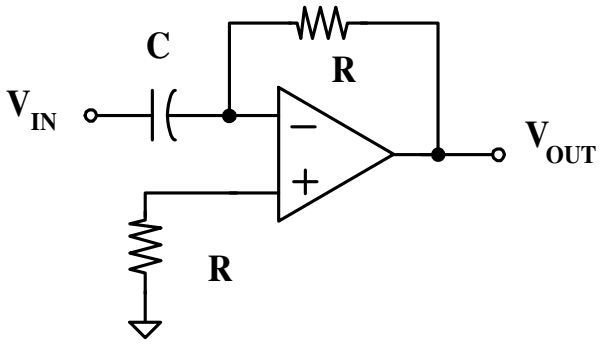

Fig. 38. Analog differentiator

one-shot and other auxiliary logic circuits. Its schematic is shown in Fig. 37. Structural level improvement has been made to over come the non-ideality and process variation suffered by the conventional zero-crossing detector.

1. Architectural Improvement in the Zero-Crossing Detector

Although the matlab simulation of the quadrature zero-crossing detector shows close performance in comparison with the optimum non-coherent GFSK demodulator, the non-ideality in the practical circuit design will introduce performance degradation. Conventional analog differentiator as shown in Fig. 38, which is consist of a resistor, a capacitor and an OpAmp, is not suitable for the demodulator. The reason is

that analog differentiator gives positive and negative pulse at the rising and falling edge of the square wave signal, respectively. Thus, the different polarity pulses will cancel each other during the energy averaging in the lowpass filter and the frequency modulation information is lost. Since the zero-crossing point in a square wave signal is associated with the rising edge and falling edge, we can use the edge detector to perform the zero-crossing detection. The circuits shown in Fig. 39 are one-shot edge detectors. They generate square pulses when the rising or falling edges occur in the input signal and thus detect the zero-crossing points. The one-shot circuit on the upper half is used to detect the rising edges and can be denoted as the rising edge detector. The one in the lower half is used to detect the falling edges and can be denoted as the falling edge detector. Their detailed operation principles will be discussed in subsection 2. The width of the pulse generated by the edge detectors is determined by the absolute values of the R, C and the logic threshold voltage in the detectors. In the 0.35 μm TMSC CMOS technology, the R and C can change widely due to large process variation. Therefore, the pulse width generates in I and Q channels can be quite different. As previously explained, the accurate data detection is based on the averaged energy of the pulse train that is generated by the zero-crossing detector. Both pulse width and pulse density affects the averaged pulse train energy. Unequal pulse width in the detector desensitizes the demodulator's response to the pulse density, and hence degrades the detection performance. Matlab simulation shows that we can tolerate $\pm 10\%$ variation in the absolute value of the pulse width if it occurs uniformly to both I and Q channels, but the unequal pulse width in different channels kills the detection performance. In the Bluetooth low-IF receiver, the baseband adopts fully differential architecture. As illustrated in Fig. 37, the positive and negative signal paths for both I and Q channels involves 4 edge detectors in their operation. It is difficult to provide good matching performance

among all the 4 edge detectors in the layout.

To solve this design issue, a shape keeping one-shot is added into the zero-crossing detector, as shown in Fig. 37. It re-shapes the pulses generated by the edge detectors and forces them into the same width. The circuit implementation of this shape keeping one-shot will be explained in subsection 2.

In the circuit operation, the edge detectors generates a narrow pulse at each zero-crossing point of the input. Then the pulses from I and Q channels are combined together via 2 OR gates and 1 NOR gate. The pulse width generated by the one-shot edge detectors may vary because of the process variation and mismatching. The shape keeping one-shot re-generate the pulse from the combined uneven pulse train. Process variation may still affect the pulse width of the shape keeping one-shot output, but it affects all the pulses in the same direction and no mismatching among pulse widths exists. Therefore, it eliminates the negative effect of unequal pulse width on the demodulator performance.

2. Circuit Implementation of the Zero-Crossing Detector

In this subsection, we will discuss the circuit implementation and operation principle of the edge detectors and shape keeping one-shot.

- ◇ *Edge detectors*

  We will use the rising edge detector to explain the principle and operation of the one-shot edge detectors. The rising edge detector (upper half of Fig. 39 is consisted of an inverter, a NOR gate and an RC network. Due to the presence of the RC network, the voltage at node B is a function of V_X and time following the equation (4.7).

$$V_B(t) = V_X(1 - e^{-\frac{t}{RC}}) \tag{4.7}$$

During the steady state ($t >> RC$), the voltage at B is equal to the voltage at node X. As the voltage level at X is low, the voltage at node A and B stay at logic "1" and "0", respectively. Hence the output of the one-shot is "0" at node Y. When the rising edge occurs, the voltage at node A changes from logic "1" to "0". The voltage at node B, however, cannot change to "1"instantly but stays at logic "0". The output of the one-shot becomes "1". The voltage at node B increase with time as described in (4.7). Once the voltage crosses over certain threshold voltage V_{TH}, the NOR gate will treat it as logic "1" and the output of the one-shot falls back to "0" again. In that way, a pulse is generated at the rising edge of the input square wave. The width of the pulse is determined by the R, C and the logic threshold voltage V_{TH}. When $t << RC$, equation (4.7) can be approximated as

$$V_B(t) = \frac{t}{RC}V_X \tag{4.8}$$

Therefore, the pulse width or the time that the voltage at node B reaches the logic threshold can be calculated as

$$T = RC\frac{V_{TH}}{V_X} \tag{4.9}$$

Then when the falling edge occurs, the voltage at A switches from "0" to "1". For the same reason, the voltage at B cannot change to "0" instantly. Therefore, no pulse is generated in this case. The pulse generation principle for the falling edge detector (lower half of Fig. 39) is the same, only this time the pulse is

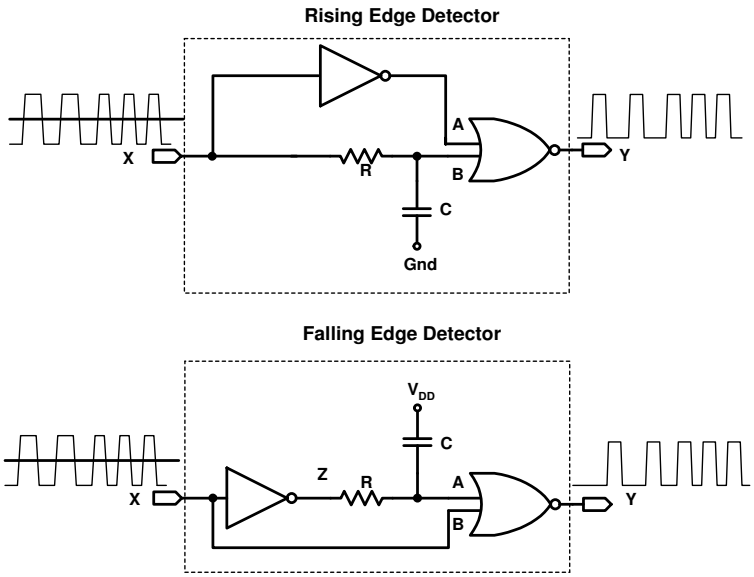

Fig. 39. One-shot zero-crossing detectors

generated at the falling edge. As shown in (4.9), the pulse width is proportional to the product of R and C since the logic threshold V_{TH} is usually fixed in a certain process.

In the circuit implementation, only the falling edge detector is used in the zero-crossing detector because of the fully differential architecture adopted in the ADI design. The R is chosen to be 1 kΩ and the C to be 7 pF. That gives a pulse width of about 13 ns. Fig. 40 shows the transient response of the edge detector.

◇ *Shape keeping one-shot*

Fig. 41 depicts the schematic of the shape keeping one-shot circuit. The resistor ladder in the left provides voltage references, $VDD > V_{REFH} > V_{REFL} > 0$, for the circuit operation. The SR latch in the middle, which is formed by two NOR gates, has a characteristics as shown in the Table XII. C_{n-1} and C_n in the truth table are the current and the next state at node C, respectively. A start-up

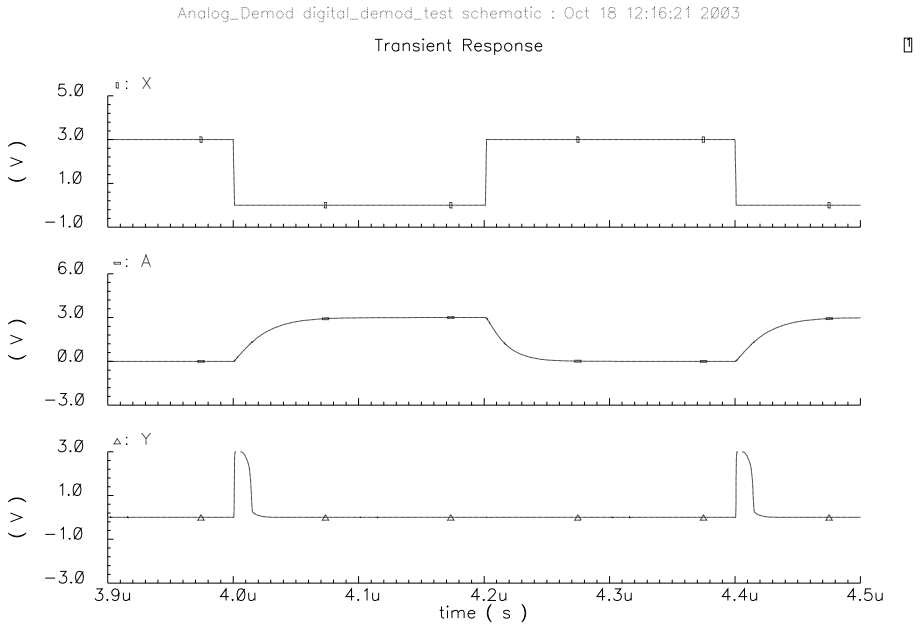

Fig. 40. Internal node voltage transient response of the edge detector

Table XII. The truth table of the SR latch

A	B	E	C_n
0	0	0	C_{n-1}
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	X
1	1	0	1
1	1	1	X

circuit is connected to node A to provide initial state to the SR latch. Since the voltage at the node A is always "0", the logic uncertainty (both $A+B=1$ and $E=1$) in the SR latch is avoided when it is powered on. The two OpAmps, A1 and A2, operate as comparators. When the input $V_{i,SK}$ is low ($V_{i,SK} < V_{REFL}$), the voltage at node E is logic "1" and the output of the shape keeping one-shot, $V_{o,SK}$ is "0". The voltage at F is high too, and it switches on the transistor M. Thus, voltage at G becomes low. Since $V_G < V_{REFH}$, B becomes logic "0". As the input, $V_{i,SK}$, changes from low to high, $V_{i,SK} > V_{REFL}$ and the logic voltage at E changes from "1" to "0". The voltage at B is still "0", the output of SR latch and the shape keeping one-shot, C and $V_{o,SK}$ remain in the previous state, which is "1" and "0", respectively. When $V_{i,SK}$ falls from high to low, $V_{i,SK} < V_{REFL}$ and E becomes "1" again. The output of the SR latch changes to "0" at C and F becomes low, too. The transistor M is switched off and the current starts to charge the capacitor C_2. The output of the one-shot becomes "1". The voltage change over the capacitor at node G can be expressed as

$$V_G(t) = V_{DD}(1 - e^{-\frac{t}{R_5 C_2}}) \tag{4.10}$$

Once the voltage at G excess the V_{REFH}, the voltage at B changes to logic "1" and the SR latch output becomes "1" again. Hence, the output of the shape keeping one-shot returns to "0" and a pulse is generated at the falling edge of the input waveform. The transistor M is switched on and the node voltage at B turns to "0". Therefore, each falling edge in the $V_{i,SK}$ maps to a pulse in $V_{o,SK}$. The width of the pulse in $V_{o,SK}$ is defined by the time for the voltage over the capacitor C_2 to exceed V_{REFH}. Using the linear approximation, the

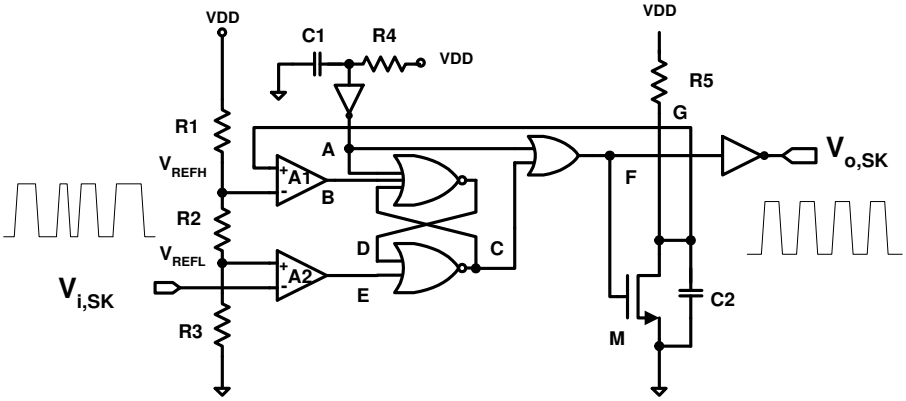

Fig. 41. Shape keeping one-shot circuit

pulse width, T, can be calculated as

$$T = R_5 C_2 \frac{V_{REFH}}{VDD} \tag{4.11}$$

There are certain requirements for the pulse width of the shape keeping one-shot output. Firstly, the pulse width of the shape keeping one-shot needs to be wider than any of the widths of the pulses generated by the edge detectors. This is to avoid the state that both inputs of the SR latch becomes "1". Secondly, the pulse generated in the shape keeping one-shot cannot overlap each other to avoid miss-count in the number of the pulses. These two requirements set the upper and lower boundary for the shape keeping one-shot pulse width. In the circuit design, we set the $R_5 = 4k\Omega$ and the $C_2 = 16p$ to generate a pulse width of 85 nS. Fig. 42 shows the transient response of the shape keeping one-shot.

The proposed zero-crossing detector is simulated at the transistor level in the cadence design environment. Fig. 43 shows the transient response of the circuit. Each zero-crossing point of the input square wave in both the I and Q channels are mapped into a pulse in the output of the zero-crossing detector.

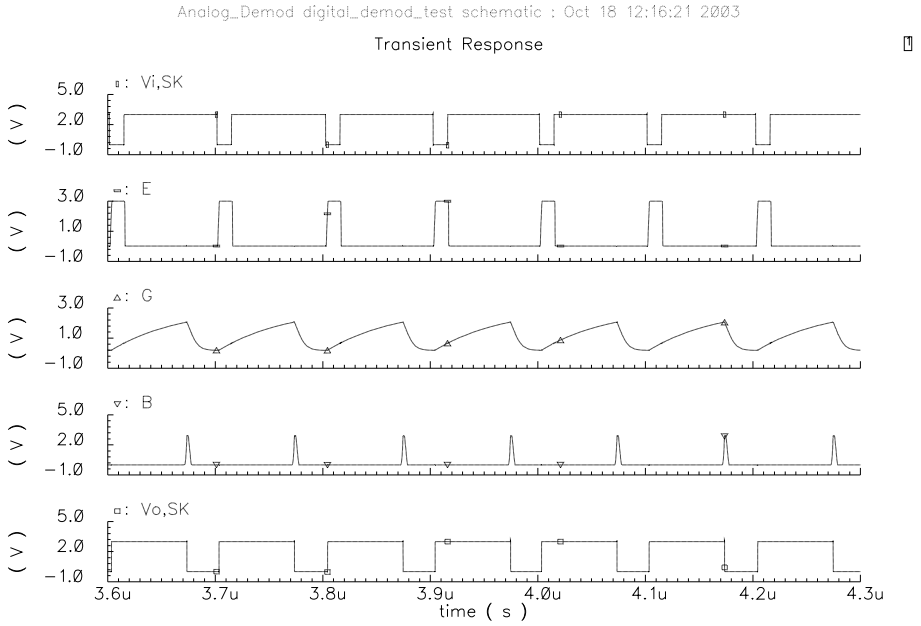

Fig. 42. The internal node voltage transient response of the shape keeping one-shot

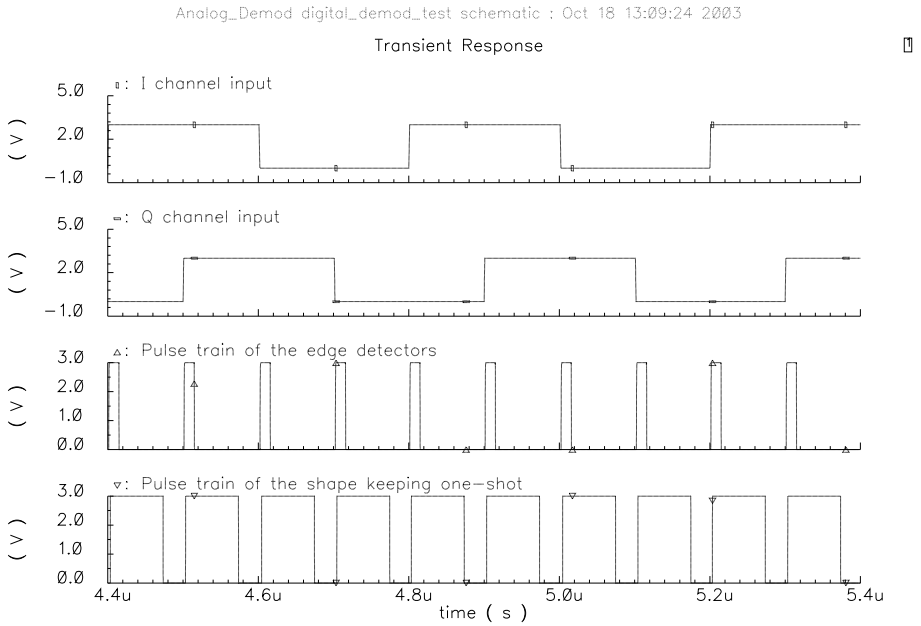

Fig. 43. Transient response of the zero-crossing detector

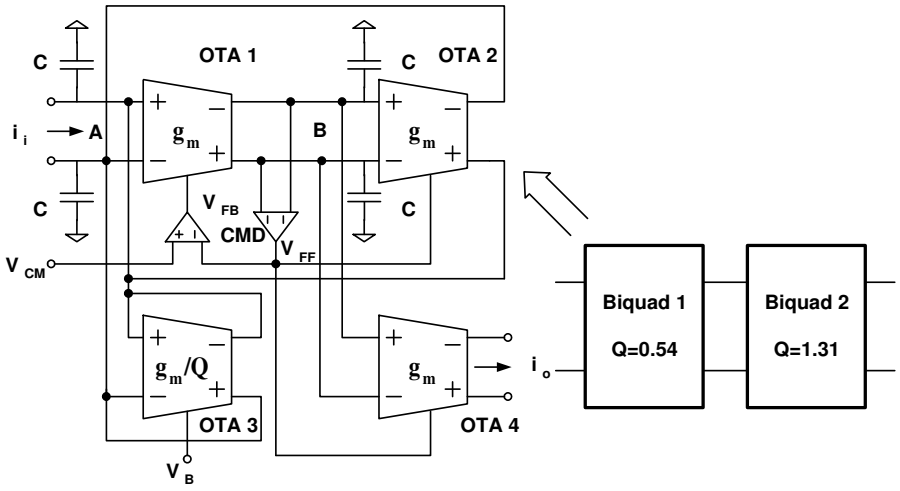

Fig. 44. The demodulator lowpass filter and the schematic of the biquads

D. Demodulator Lowpass Filter

The lowpass filter used in the Bluetooth GFSK demodulator is a 4^{th}-order butter worth filter. It has a cutoff frequency at 605 kHz. As shown in Fig. 44, the filter is consist of two similar Biquads that adopt operational transconductance amplifier-capacitor (OTA-C) techniques.

The output of the zero-crossing detector is a rail-to-rail square wave. Pseudo differential OTA, as depicted in Fig. 45, is applied in the filter to provide a large input swing in the low supply voltage design environment (3.3 V). Its transconductance, g_m depends on the input common mode voltage, $V_{i,CM}$, and can be expressed as,

$$g_m = K_{pn}\frac{W}{L}(V_{i,CM} - V_{TH}) \tag{4.12}$$

The pseudo differential OTA has same differential mode and common mode gain. Therefore, Common Mode Feed-Back (CMFB) and/or Common Mode Feed-Forward (CMFF) circuits are needed to enhance the Common Mode Rejection Ratio (CMRR) of the filter. If the output common mode impedance is high, then CMFB is needed to

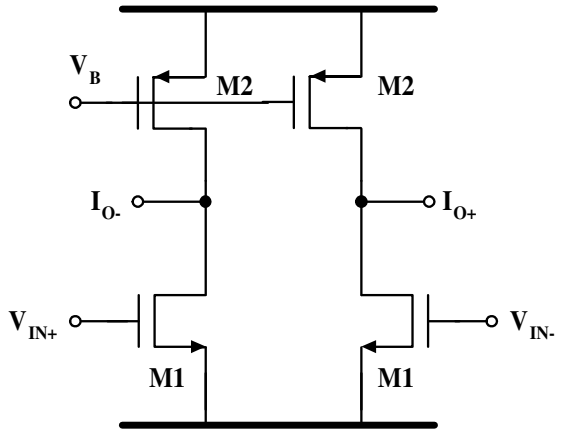

Fig. 45. The schematic of the pseudo differential OTA

lower this impedance. This is illustrated in Fig. 46, where the output CM impedance becomes $1/g_{mfb}$ and g_{mfb} is the transconductance of the CMFB loop. In the figure, the Common Mode Detector (CMD) senses the common mode signal at the output nodes and feeds the correction signal to the bias voltage V_B of the OTA. Since the CMD circuit is inverting, another inverting stage is added to make the CMFB loop gain negative. On the other hand, if the output common mode impedance is sufficiently small, CMFB is not needed and CMFF is used to isolate the input and output common mode signals of the OTA. This is illustrated in Fig. 47. Note that the polarity of the OTA indicated in Fig. 47 is only in the differential mode sense. The common mode transconductance of the OTA in Fig. 47 is always negative. The CMD circuit and the inverting circuit are shown in Fig. 48.

Fig. 44 shows the circuit of one of the filter biquads. OTA1 and OTA2 form a negative differential mode feedback loop, but a positive common mode feedback loop. The output node of OTA2, node A, is a low impedance ($1/Qg_m$) node due to the resistive-connected OTA3. Hence, no CMFB is needed at this node and only CMFF is used in all the OTAs that feed this node, excluding OTA3. If CMFF is used in

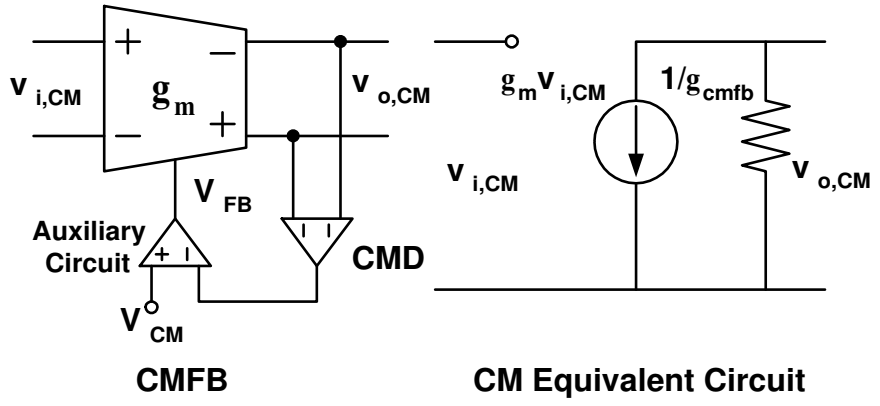

Fig. 46. CMFB circuit

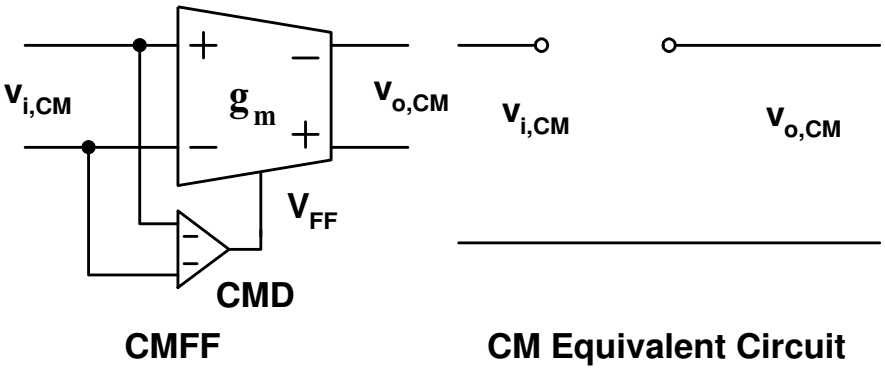

Fig. 47. CMFF circuit

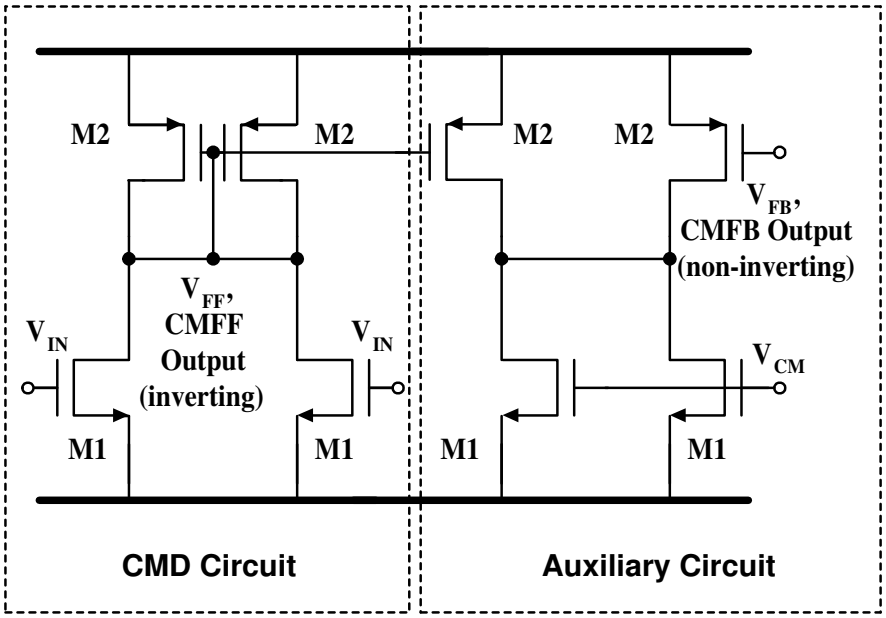

Fig. 48. The CMD and its auxiliary circuits

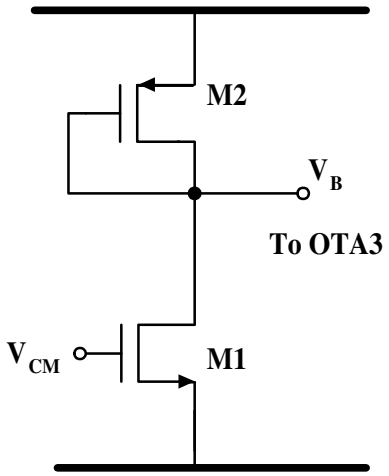

Fig. 49. The biasing circuit for OTA3

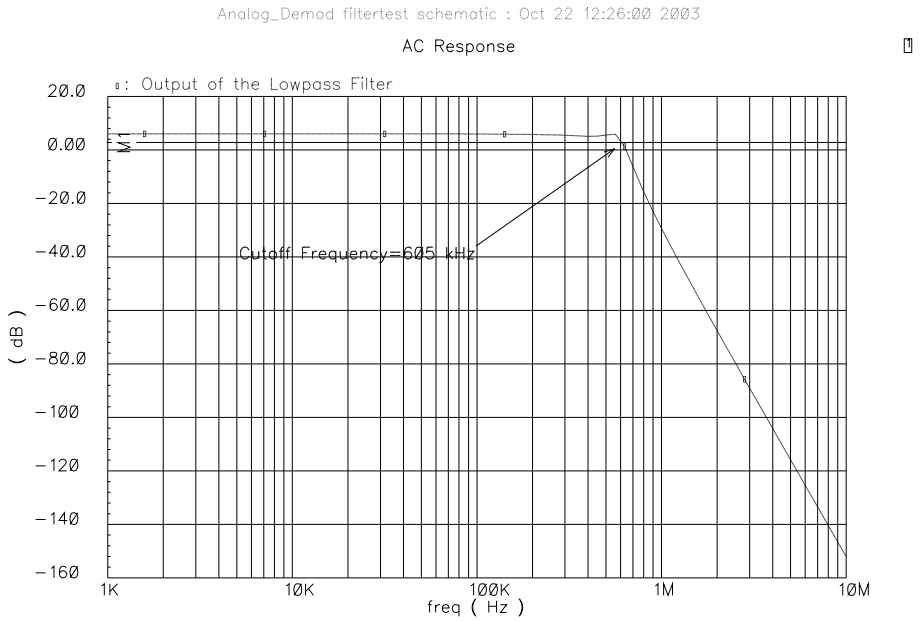

Fig. 50. The frequency response of the demodulator lowpass filter

OTA3, the common mode impedance at node A will be very high. Instead, the bias voltage of OTA3 is obtained from the on-chip biasing circuit in Fig. 49. Note that the input to this biasing circuit is connected to common mode reference voltage, V_{CM}, not to the input or output nodes of the OTA. Therefore, OTA3 in the two biquads can be biased using a single biasing circuit. The use of CMFF in OTA2 breaks the common mode loop formed by OTA1 and OTA2. Node B is a common mode high impedance node, and hence, needs CMFB to stabilize it. CMFB loop is formed in OTA1 through the same CMD that provides CMFF for OTA2 and OTA4. CMFF is also used in OTA4 to isolate the common mode signals in this biquad stage from the next biquad. Only 1 common mode detector are needed to form the common mode control circuit in this biquad stage with 4 OTAs. By using the minimum number of common mode control circuits, this efficient scheme saves considerable power and silicon area, and contributes less noise than using a common mode control circuit for each OTA.

Long channel transistors are used in the lowpass filter to enhance the output resistance, improve matching, and reduce flicker noise. The transistor sizes for M1 and M2 are $2\mu m/6\mu m$ and $1\mu m/6\mu m$, respectively. The capacitor, C, in the lowpass filter is chosen to be 7.3 pF. Fig. 50 shows the frequency response of the filter, the cutoff frequency is at 605 kHz and the filter has a passband gain of 6 dB. Since the lowpass filter is used for power averaging, its cutoff frequency does not need to be very precise. The specs of filter does not require high quality factor (Q) in the filter implementation either. Therefore, tuning circuit is not necessary for the demodulator lowpass filter. The group delay for the filter is 0.96 μs.

E. LO Frequency Offset Cancellation

As we have discussed in the previous chapter, the Bluetooth system has an LO frequency offset up to $\pm$100 kHz between the transmitter and receiver. Comparing to $\pm$175 kHz maximum frequency modulation depth of the Bluetooth, LO frequency offset can be as large as 60% of the maximum frequency modulation deviation. This frequency offset affects the number of the zero-crossing points detected by the zero-crossing detector. After averaging in the demodulator lowpass filter, it is converted into a DC offset voltage. Hence, the frequency offset cancellation becomes DC offset cancellation in the proposed demodulator. Matlab simulations show that the DC offset has to be less than 10% of the peak-to-peak voltage of the lowpass filter output to avoid significant degradation in the signal detection performance.

1. Proposed Frequency Offset Cancellation Structure

Several potential DC offset cancellation circuit approaches were studied. Fig. 51 shows a digital cancellation approach [57]. An ADC is used to digitize the output

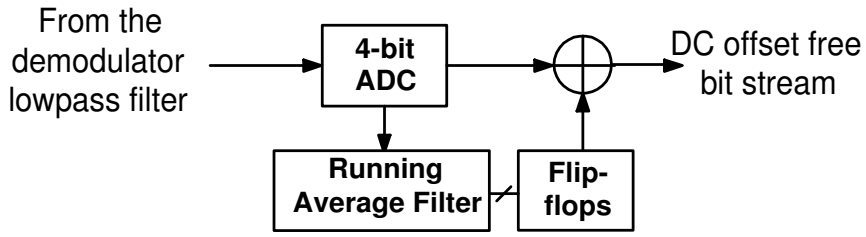

Fig. 51. Digital domain DC offset cancellation circuit

of the demodulator lowpass filter. The DC offset is detected by an averaging circuit in the digital domain and stored in a set of flip-flops. A digital adder is employed to cancel the offset. Unfortunately, to reduce the remainder of the DC offset to be less than 10% of the peak-to-peak voltage of the demodulated signal, at least a 4-bit ADC is needed, this increases the complexity of the demodulator circuitry. Fig. 52 illustrates an adaptive DC offset cancellation structure [58]. The principle of this structure is based on the assumption that the the received signal is DC offset free over a long period of time. Since the transferred data is whitened at baseband in the transmitter this assumption is valid for the Bluetooth system. The received signal is integrated in the adaptive circuit. The integral is regarded as the DC offset voltage and subtracted from the output of the lowpass filter. For long enough period of time, the adaptive circuit is able to provide an relatively accurate estimation of the DC offset. The advantage of this scheme is that the estimation is obtained without previous knowledge of the data packets, but the control of the circuit is relatively complicated.

Given the knowledge of the access code, we can avoid using the complex systems in Fig. 51 and 52. We proposed a DC offset cancellation circuit design for its simplicity and flexibility in operation mode. A complete block diagram of the DC cancellation and decision circuit is shown in Fig. 53. In each Bluetooth data packet, there are 4-bit DC free preamble and trailer in the access code, either in form of ”0101” or ”1010”

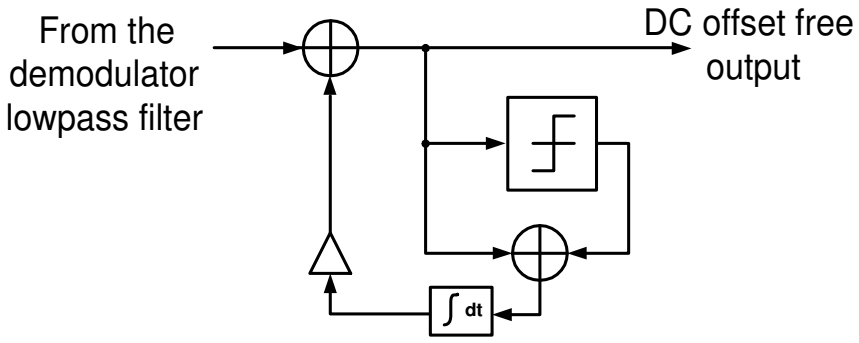

Fig. 52. Adaptive DC offset cancellation circuit

[11], as illustrated in Fig. 9. By integrating either the preamble or the trailer, we can get an estimation of the existing DC offset and subtract it from the received signal. Since a maximum frequency drifting of $\pm 25kHz$ is likely to occur in one time slot, the DC offset cancellation circuit should be able to track and compensate this variation as well. In order to do so, we change the operation mode of the DC offset estimator by using switched-capacitor techniques. The DC offset estimator works as an integrator during the reception of the access code, but as a very-low cutoff frequency lowpass filter during the data packets transmission to track the possible frequency drifting. A sample and hold circuit stores the offset voltage and feeds it back to the voltage subtractor to cancel the DC offset before the signal goes into the decision circuit. The control signal, Ctrl1, is used to enable and disable the Integrator/LPF circuit that works as a DC offset estimator. Ctrl3 and Ctrl5 are used to control the sample and hold circuit and the DC offset voltage feedback path , respectively. Ctrl2 and Ctrl4 are applied to the decision circuit. Fig. 54 shows the voltage changes at each stage of the DC offset cancellation and decision circuit. The left half of the figure illustrates the signal waveforms during DC offset integration phase, and right half illustrates the waveforms during the DC offset tracking phase when the DC offset estimator works as a lowpass filter.

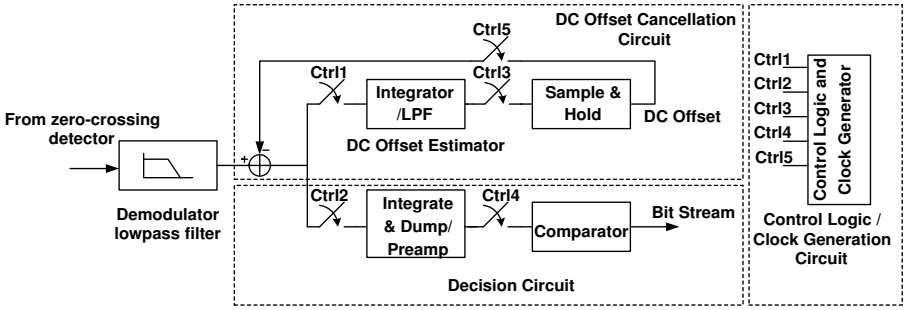

Fig. 53. Proposed DC offset cancellation and decision circuit

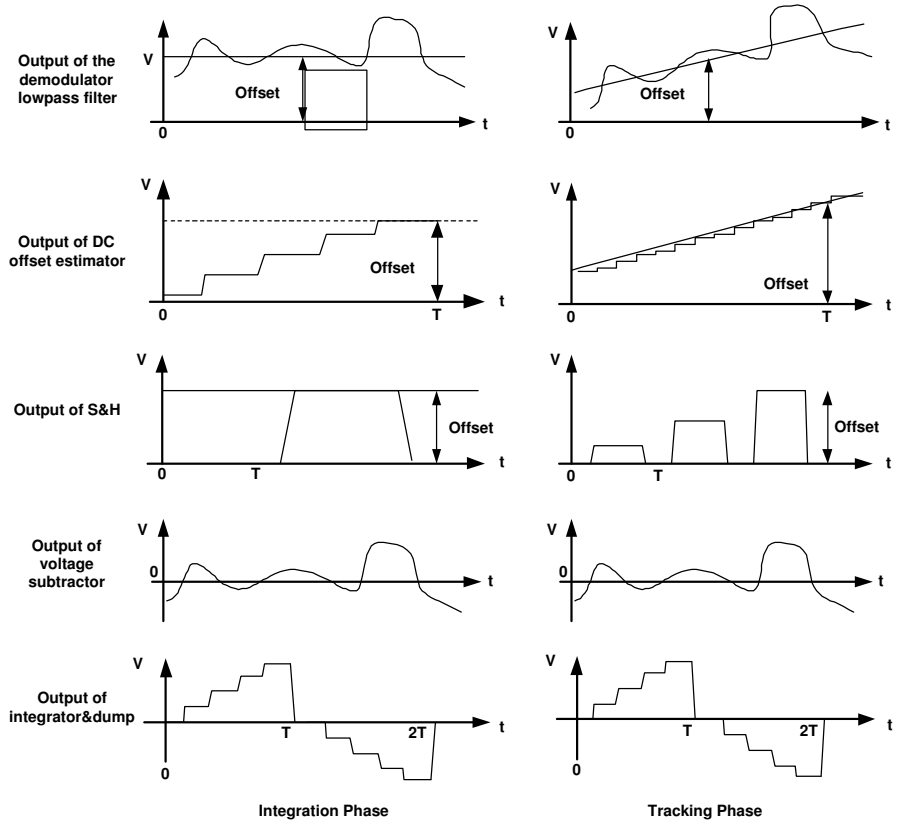

Fig. 54. The time domain waveform at each node of the DC offset cancellation and decision circuit

Timing is one critical issue in the circuit design. Since the access code is at the beginning of the data packet, the DC cancellation circuit starts to integrate the incoming signal whenever the RF frontend detects a power burst in the received signal. Signal synchronization at this stage is not very accurate, hence the DC offset estimation is not accurate either. Fine synchronization is achieved by calculating the auto-correlation of the sync word. Once the receiver clock is perfectly synchronized to the transmitter clock, the trailer in the access code of a data packet is integrated to yield an accurate DC offset estimation. A control logic/clock generation circuit is employed to provide clock and control signals for the DC offset cancellation circuit.

2. Circuit Implementation of the DC Offset Cancellation Structure

As introduced in the previous subsection, the LO frequency offset or DC offset cancellation circuit contains a voltage subtractor, a DC offset estimator operating as either integrator or lowpass filter, a sample and hold and the control logic/clock generator. Their transistor level implementation is explained in this subsection.

- ◇ *Voltage subtractor*

  The voltage subtractor used in the DC Offset cancellation circuit is a continuous time circuit, its circuit schematic is showed in Fig. 55. The voltage at the output can be expressed as,

$$(V_{cp} - V_{cm}) = \frac{R_f}{R_i}(V_{inp} - V_{inm}) - \frac{R_f}{R_{off}}(V_{offp} - V_{offm}) \tag{4.13}$$

  where $V_{cp} - V_{cm}$ is the differential output of the subtractor, $(V_{inp} - V_{inm})$ is the differential input from the demodulator lowpass filter, and $(V_{offp} - V_{offm})$ is the estimated DC offset voltage.

  Since the load of the OpAmp is resistive, the output stage of the OpAmp must

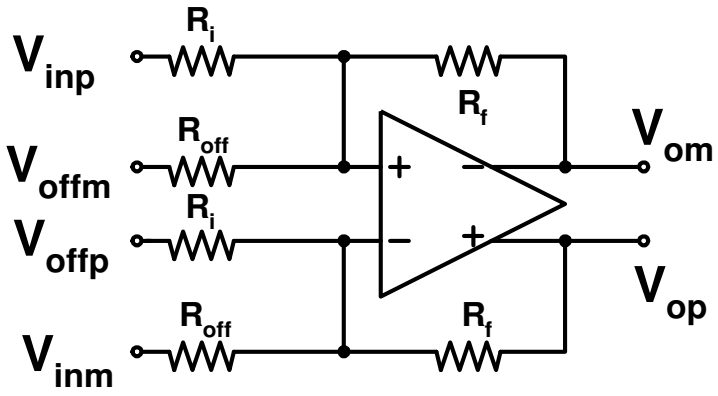

Fig. 55. Adaptive DC offset cancellation circuit

Table XIII. The specs and simulation results for the voltage subtractor OpAmp

Parameters	Specifications	Simulation Results
DC Gain	$> 60dB$	$64.2dB$
Slew Rate	$> 5V/\mu S$	$6.3V/\mu S$
GBW	$> 30MHz$	$34.5MHz$
Output Resistance	$< 200\Omega$	152Ω
Phase Margin	$> 60degree$	$78degree$
$V_{DD}/V-SS$	$+1.65/-1.65V$	$+1.65/-1.65V$
Current Consumption	Minimum	$240uA$

have a low impedance to make the circuit work properly. Table XIII shows the Specs for the OpAmp used in the voltage subtractor.

Based on the specs of the OpAmp, a two stage OpAmp is designed. The schematic is shown in Fig. 3.7. The left part of the OpAmp, M1-M7, M10 and M11 are a fully differential two-stage-OpAmp. The right part, transistors M12-M19 are the common mode feedback circuit, which is used to control the common mode voltage at the output. To split the poles of the OpAmp, capac-

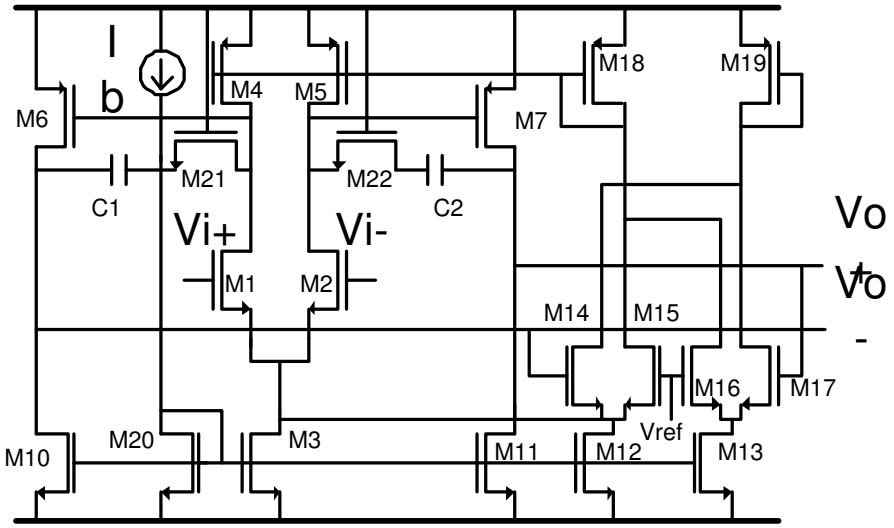

Fig. 56. Two-stage-OpAmp used in the voltage subtractor

itors, C1, C2, and transistors M21, M22, are connected between two stages to assured the stability of the system. The schematic of the OpAmp is shown in Fig. 56. The simulation results for the OpAmp is also included in Table XIII. Table XIV lists the transistor size used in the OpAmp and the resistor values in the voltage subtractor.

◇ *DC offset estimator and clock generator*

Table XIV. The transistor size and capacitor, resistor value used in the voltage substractor

M1,2	$24\mu m/0.6\mu m$	M4,5,18,19	$48\mu m/0.8\mu m$
M3,20	$72\mu m/1\mu m$	M6,7	$32\mu m/0.6\mu m$
M10,11	$16\mu m/0.6\mu m$	M21,22	$1.6\mu m/0.6\mu m$
M12,13	$36\mu m/1\mu m$	C1,2	$2pF$
M14-17	$36\mu m/0.9\mu m$	R_i, R_f	$2k\Omega$
R_{off}	$8k\Omega$		

As introduced in previous subsection, the DC offset estimator operates in two different mode. It works as an integrator during the transmission of the access code, integrate the preamble or trailer to get the DC offset estimation. After that it works as a very low frequency low pass filter to tracking the DC voltage changing. Switched-capacitor circuit is used in the DC offset estimator circuit to provides flexibility in programming the operating mode. The schematic of the circuit is showed in Fig. 57. During the access code transmission, Clk4 is always low and the switches S6, S9, S15, S18 are off. The circuit works as an integrator. The circuit transfer function under this mode can be expressed as,

$$H(z) = \frac{C1}{C2}\frac{z^{-1}}{1 - z^{-1}} \tag{4.14}$$

After the transmission of the access code, Clk4 is high and the switches S6, S9, S15, S18 are on. The circuit works as a lowpass filter and its transfer function is derived as,

$$H(z) = \frac{\frac{C1}{C2}z}{\left(1 + \frac{C3}{C2}\right)z - 1} \tag{4.15}$$

When Clk3 is high, the switch S5, S14 are on and the DC voltage accumulated on C2s is reset. This reset phase occurs before and after the preamble and trailer receiving period. The different circuit operating modes are showed in Fig. 58. The proper operation of the DC offset estimator is based correct clock arrangement. A clock generation circuit is also included in the DC offset cancellation circuit to create a clock sequence as shown in Fig. 59. The core of the clock generator is a counter, which divides the a 16 MHz main clock and arrange the clock sequence with the assistance of other logic circuits.

A clock frequency of 4 MHz and 600 kHz are applied to the DC offset estimator under integration mode and lowpass filter mode, respectively. In the lowpass

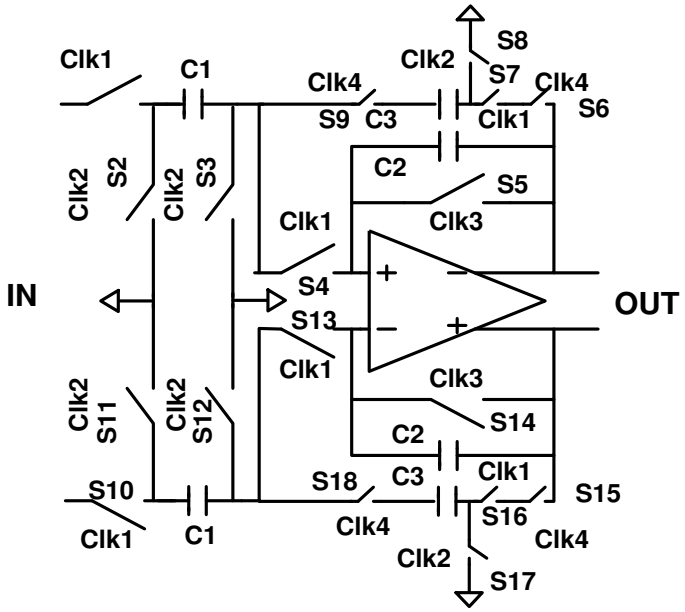

Fig. 57. DC offset estimator

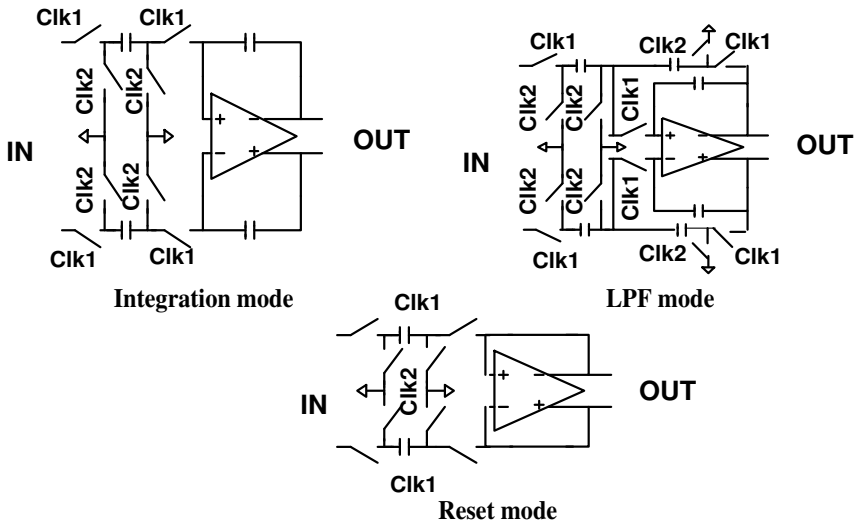

Fig. 58. The operating modes of the DC offset estimator

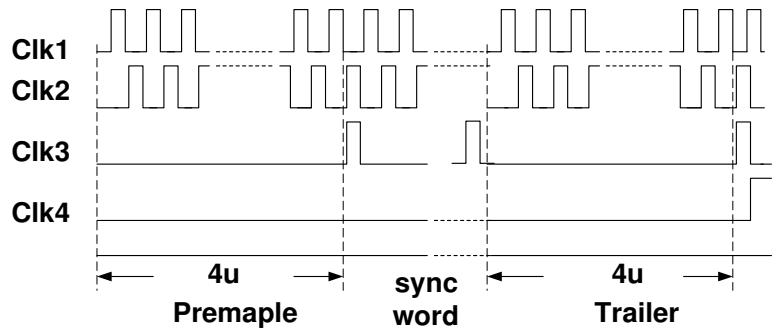

Fig. 59. Clock phases in the DC offset estimator

Table XV. The transistor size for the folded-cascode OpAmp

M1,2	$24\mu m/0.6\mu m$	M4,5	$64\mu m/0.6\mu m$
M3,20	$60\mu m/0.6\mu m$	M6,7	$72\mu m/0.6\mu m$
M10,11	$36\mu m/0.6\mu m$	M21	$6\mu m/0.6\mu m$
M8,9	$48\mu m/0.6\mu m$	M22	$16\mu m/0.6\mu m$

filter mode, according to (4.15), the pole of the filter is at approximately $\omega_p = -\frac{C3}{C2} f_s$ if $\frac{C3}{C2} >> 1$, where f_s is the sampling frequency. We fixed ratio of $\frac{C2}{C3}$ to be 16, given a 600 kHz sampling frequency, the cutoff frequency of the lowpass filter is at around 6 kHz.

The OpAmp used for the switched capacitor circuit in the DC offset estimator is a folded-cascode OpAmp, as illustrated in Fig. 60. A switched capacitor common mode feedback circuit is employed to fix the common mode voltage of the fully differential OpAmp. The advantage of using switched capacitor CMFB circuit is that it does not limit the swing of the output signal. The transistor size used in the folded-cascode OpAmp is listed in Table XV, and Table XVI summarizes the specification and simulation results for the OpAmp.

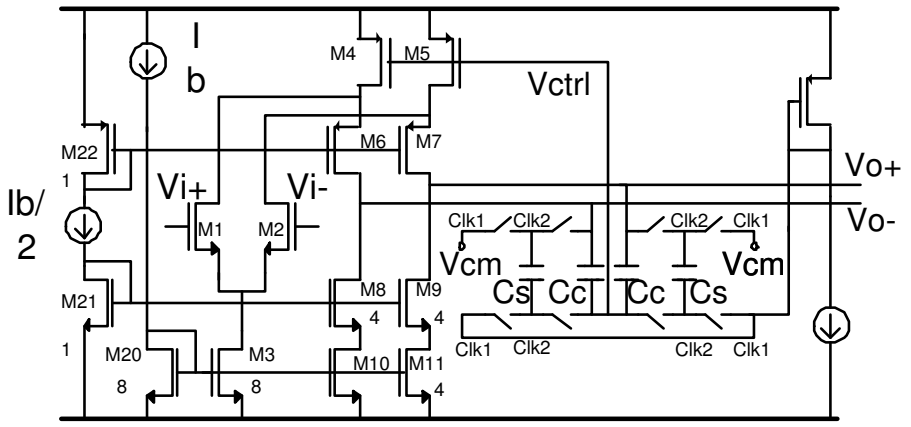

Fig. 60. The folded-cascode OpAmp used in the DC offset estimator

Table XVI. The specs and simulation results for the folded cascode OpAmp

Parameters	Specifications	Simulation Results
DC Gain	$> 60dB$	$72.4dB$
Slew Rate	$> 16V/\mu S$	$18.2V/\mu S$
GBW	$> 30MHz$	$44.2MHz$
Phase Margin	$> 60degree$	$74degree$
V_{DD}/V_{SS}	$+1.65/-1.65V$	$+1.65/-1.65V$
Current Consumption	Minimum	$180uA$

◇ *Sample and hold*

The voltage hold circuit follows the DC offset estimator. It samples and holds the DC voltage obtained in the DC offset estimator. Then feeds back it back to the voltage subtractor to cancel the DC offset in the received signal waveform. The leakage current in the CMOS process is small. The transmission time of a Bluetooth data packet is less than 300 μS, according to the simulation, the leakage of the designed circuit in 400 μS is less than 0.5 mV. Since the demodulator can tolerate 10% offset voltage, no extra voltage leakage compensation circuit is required. Fig. 61 shows the schematic of the sample and hold circuit. Clk3SH is used to reset the holding voltage. The clock applied in the Sample and Hold (S&H) circuit is 4 MHz. That requires the circuit to settle with half of the clock period, which is 125 nS. The maximum voltage that can appears at the input of the S&H circuit, V_{max}, is 800 mV. To assure the S&H output is in steady state before the voltage subtraction, we decide that the voltage should be able to settle to 800 mV within $T_{set} = 50nS$ during the holding phase. Therefore, the slew rate requirement for S&H OpAmp, SR, can be calculated as,

$$SR = \frac{V_{max}}{T_{set}} = \frac{800mV}{50ns} = 16V/\mu S \tag{4.16}$$

In the S&H circuit, we have $C_{SH1} = C_{SH2}$, which gives a feedback factor, β, of 0.5. To make the settling error, e_{set}, less than 1% within 50 nS, the S&H OpAmp needs to have a GBW of . This can be calculated from 4.17

$$GBW = -\frac{ln(e_{set})}{2\beta\pi T_{set}} = 14.7MHz \tag{4.17}$$

The folded-cascode OpAmp as illustrated in Fig. 60 meets all the above re-

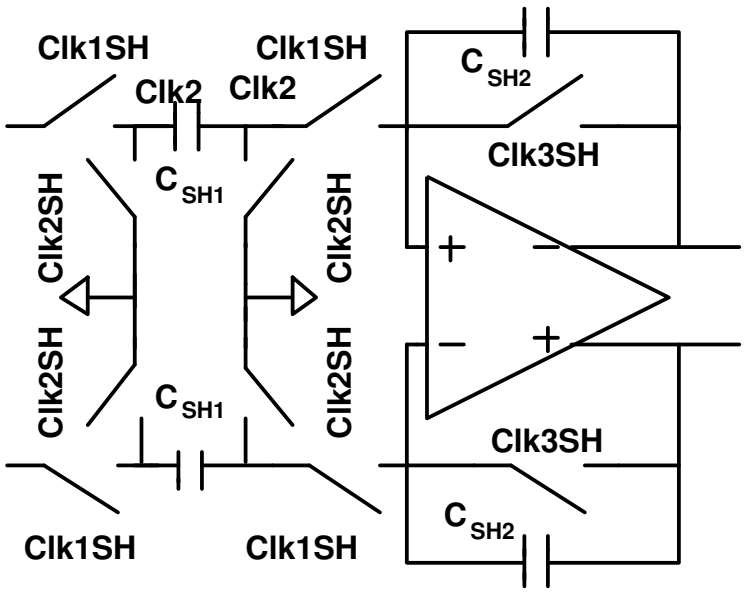

Fig. 61. The sample and hold circuit

quirement, therefor the same OpAmp can also be used in the S&H circuit.

F. Decision Circuit

The decision circuit contains an integrate-and-dump circuit, a comparator and a output buffer. The integrate-and-dump circuit integrates the voltage in each bit duration. The polarity of the integral is used for bit detection. Compared to the simple sample and decide circuit, the proposed decision circuit has better immunity to the timing error and thus has an improved performance. Fig. 62 depicts the decision circuit. A 4 MHz clock is applied to the integrator and dump circuit and the sampling frequency for the comparator is 1 MHz. The OpAmp used in the integrate-and-dump circuit is a folded-cascode OpAmp as shown in Fig. 60. Since the integrator and dump circuit provides a 12 dB gain, no pre-amplifier is needed for the comparator. The bit detection is conducted by the latch comparator. An RS latch circuit works as a digital output buffer to drive the following DSP modules.

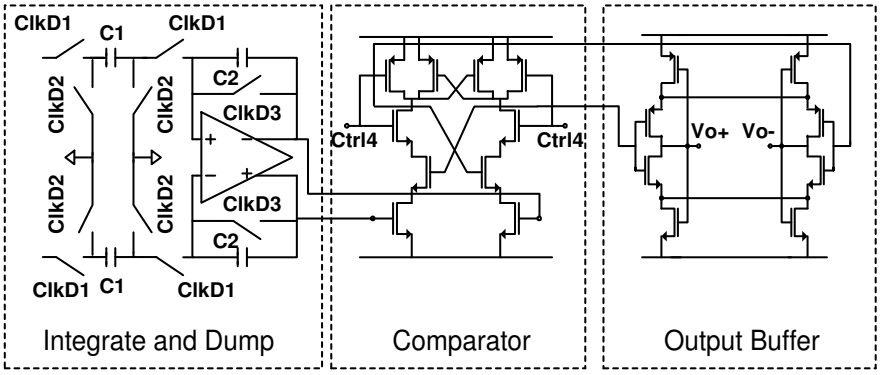

Fig. 62. The decision circuit

G. Bluetooth ADI Design Testing and Verification

The demodulator chip was fabricated in the TSMC 0.35 μm CMOS process through MOSIS. Fig. 63 shows the die microphotograph. It takes 0.7 mm^2 silicon area.

1. Testing Setup

The data detection performance of the proposed GFSK demodulator is tested in the LabView environment. A Print Circuit Board (PCB) is fabricated with an I/O interface to the National Instruments (NI) board (NI Px1-1000R) that is configured by the LabView testing software. Fig. 64 shows the testing setup for the GFSK demodulator and its DC offset cancellation circuit. The received signal sequence is generated by passing the Bluetooth GFSK modulated signal through an Additive White Gaussian Noise (AWGN) channel. This part is conducted in matlab on a computer. The signal sequences for both I and Q channels are then applied to the demodulator inputs through the interface between the testing board and the NI board. The bit stream at the output of the demodulator is feedback to the NI board and captured in the LabView. The raw data, which is the detected bit stream, is finally is compared with the transmitted data sequence to obtained the BER.

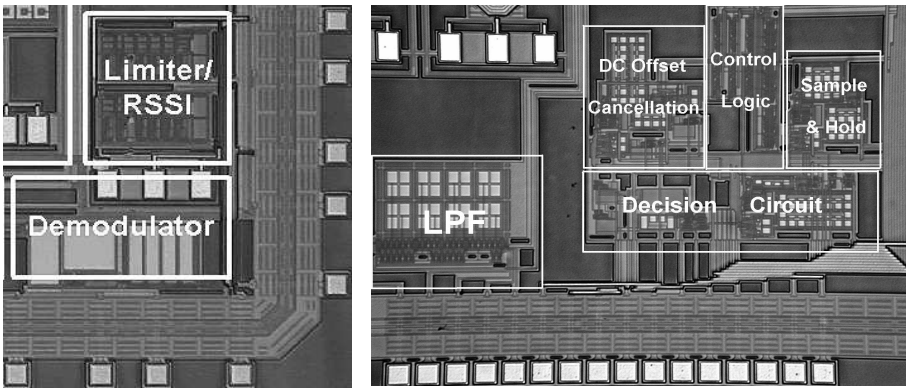

Fig. 63. The die microphotograph of GFSK demodulator and LO frequency offset cancellation circuit

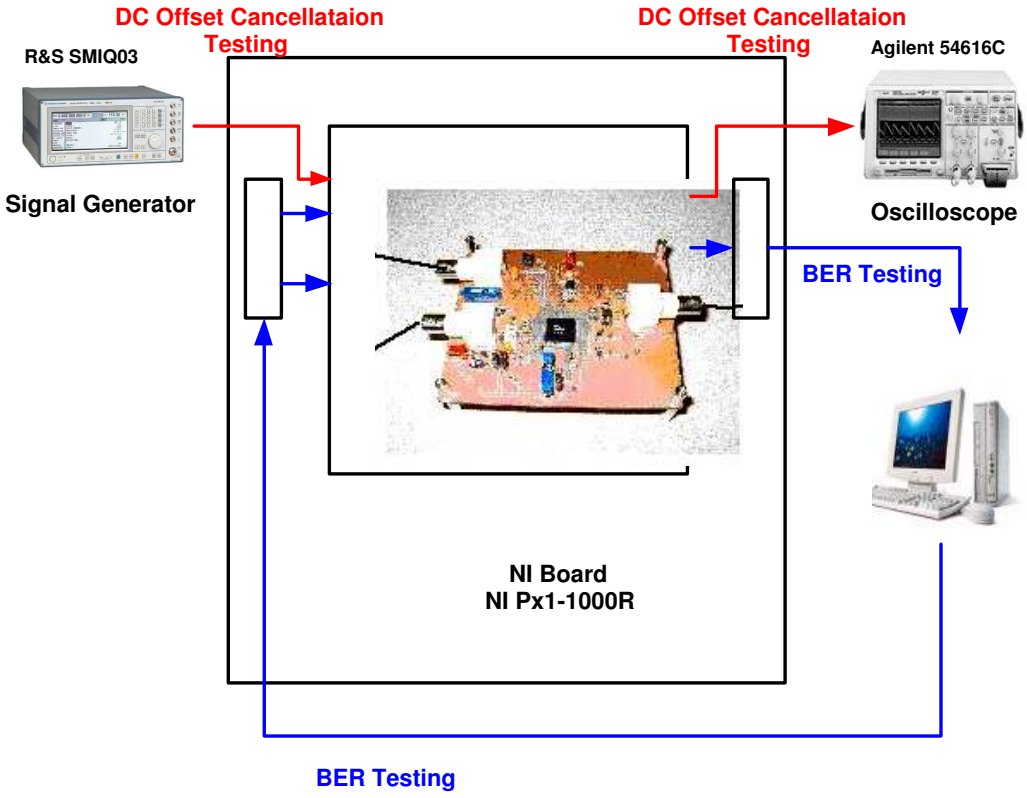

Fig. 64. Testing setup for the proposed GFSK demodulator and its DC offset cancellation circuit

The DC offset cancellation circuit is tested by applying a sinusoidal signal with a DC offset to the input. The waveform at the output of the voltage subtractor is taken to the oscilloscope to examine the effectiveness of the DC offset cancellation circuit. The signal generator used in the DC offset cancellation testing is Rohde&Schwarz SMIQ03 and the oscilloscope used is Agilent 54616C.

2. Experimental Results

The active complex filter before the demodulator limits the noise bandwidth to 1.04 MHz. Fig. 65 shows the measured BER versus SNR for the input signal with a nominal modulation index of 0.32. For 0.1% BER, as specified in Bluetooth standard, only 16.2 dB of input SNR are required. When a Bluetooth modulated co-channel interference, which is 11.2 dB lower than the desired signal, is added to the signal, 0.1% BER is achieved with only 0.2 dB degradation in the SNR. No calibration is required for this demodulator. The demodulator drains 3 mA from a 3 V power supply and occupies 0.7 mm^2 silicon area. Table XVII summarizes the simulation and measurement results. The simulated result in Table XVII is the circuit level simulation done in Spectre, it matches the Matlab simulation within 0.3dB deviation in the BER performance. Monte Carlo simulation was also carried out to examine the robustness of the design. Even with 20% variation in process, the degradation of BER performance is less than 0.5 dB. Due to the limited silicon area and consideration of testing flexibility, the zero crossing detector and the DC offset cancellation and decision circuits were fabricated on separate chips. The loading effect of the pins adds distortion to the output of the zero crossing detector, this caused performance degradation in the measurement result. Better buffering can be used to eliminate this problem. Moreover, this degradation in detection performance can be avoided in the single chip receiver solution. Previous research on the demodulation of continuous

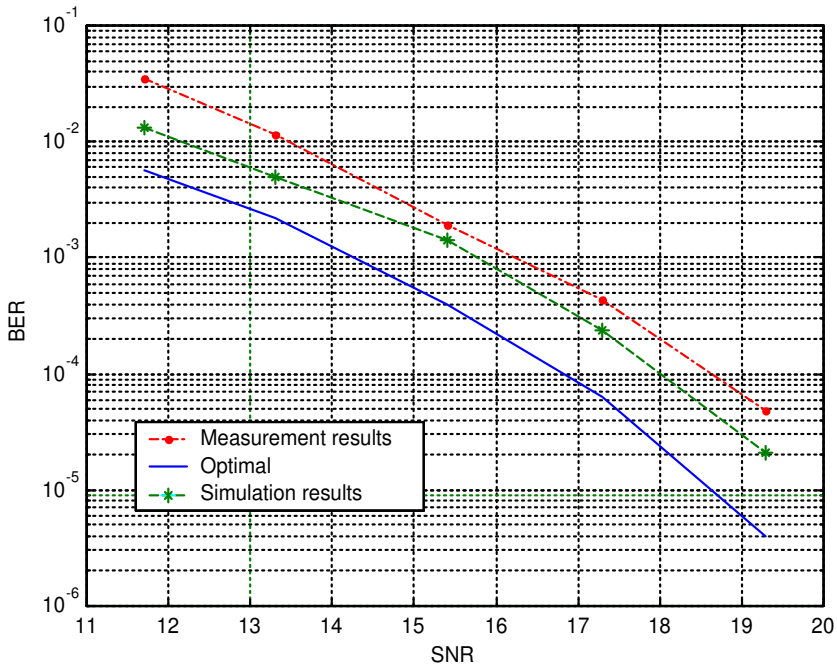

Fig. 65. The measured BER performance of the zero-crossing demodulator

phase frequency-modulation signals mainly focuses on the demodulation of FSK and GMSK signals, which is used in pager and GSM systems. Considering the difference in the modulation index and the BT, it is difficult to make a direct comparison in performance with those demodulators. The proposed demodulator achieves 0.1% BER with an input SNR of 16.2 dB. In comparison with other reported approaches [32] [34], the same BER is archived with 18 and 16.5 dB input SNR, respectively.

The DC (LO frequency) offset cancellation circuit are also tested. Fig. 66 shows the measurement result of the DC offset cancellation circuit. A sinusoidal wave with DC offset is employed to test the DC offset circuit. The upper trace is the input with DC offset, the lower trace the signal at the output of the DC offset cancellation circuit. The maximum frequency offset allowed Bluetooth specification is converted to around 60 mV DC offset at the output at the demodulator. In Fig. 66, a 110 mV offset is applied to the input signal, the offset residue in the output is only -4 mV.

Table XVII. The simulation and measurement results for the Bluetooth GFSK Demodulator

SNR (dB)		11.5	13.1	15.2	7.2	19.2
BER	Optimum performance	0.82	0.43	0.06	0.007	0.0004
	Simulated Results	1.90	0.76	0.24	0.048	0.004
(%)	Experimental Results	5.09	1.68	0.28	0.06	0.007

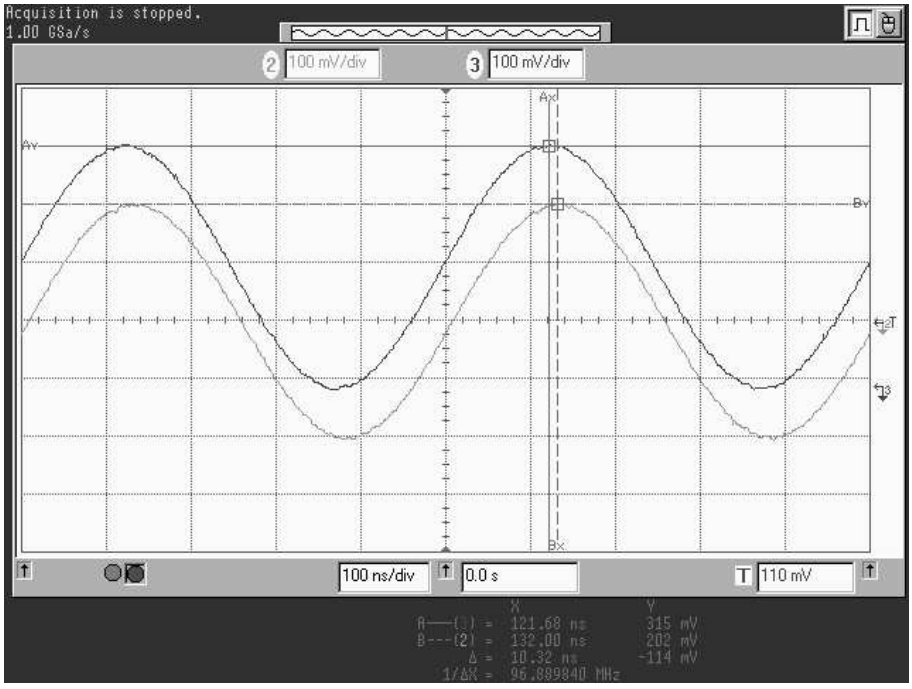

Fig. 66. The performance testing for the DC offset cancellation circuit

The circuit is able to detect and cancel a DC offset as large as 140mV limiting the offset residue within 5% of the original DC offset.

CHAPTER V

ADI DESIGN FOR THE DIRECT CONVERSION 802.11B/BLUETOOTH DUAL-MODE RECEIVER

The ADI design for the 802.11b/Bluetooth dual-mode receiver is an example of the ADI implementation in a multi-standard compatible wireless system. The system consideration, ADI design approach and circuit implementation for this particular type of system are discussed in this chapter.

A. The Characteristics of 802.11b Modulation Formats and Their Detection

In the 802.11b/Bluetooth dual-mode receiver, we need to provide proper demodulation for both 802.11b and Bluetooth signals. The demodulation of the Bluetooth GFSK signal has be discussed thoroughly in the previous chapter. Here we will focus on the demodulation of the 802.11b signalling formats.

1. 802.11b Baseband Signal

Four baseband modulation formats are employed by the 802.11b standard [17] to provide different data transfer rate. The Differential Phase Shift Keying (DPSK) and Differential Quadrature Phase Shift Keying (DQPSK) formats are used in the low data transfer rate modes, which have a data rate of 1 Mbit/s and 2 Mbit/s, respectively. The Complimentary Code Keying (CCK) format is adopted for higher date transfer rates at 5.5 and 11 Mbit/s.

- ◇ *DPSK and DQPSK modulation formats*

  The modulation of the DPSK and DQPSK follows the rules shown in Table. XVIII and XIX. In the DPSK modulation, each bit introduces a certain phase

Table XVIII. DPSK encoding table

Dibit pattern (d0)	phase change φ
0	0
1	π

Table XIX. DQPSK encoding table

Dibit pattern (d0, d1)	phase change φ
00	0
01	$\frac{\pi}{2}$
11	π
10	$\frac{3\pi}{2}$

shift in the baseband sinusoid signal. In the DQPSK modulation format, the combination of two bits modulates the phase of the baseband signal. Therefore, both modulation formats are achieved by phase shifting as expressed in (5.1). Fig. 67 depicts the phase placement of the DPSK and DQPSK modulated signal.

$$s = exp(j\varphi) \tag{5.1}$$

◇ *CCK modulation format*

The 802.11b standards adopts CCK modulation scheme for its 5.5Mbit/s and 11Mbit/s data transmission modes. For the CCK modulation mode, the spreading code length is 8 and is based on complementary codes. The chipping rate is 11 Mchip/s. The symbol duration shall be exactly 8 complex chips long, which gives a symbol rate of $\frac{11}{8} = 1.38MSymbol/s$. Equation (5.2) is used to derive the CCK code words. The terms, φ_1, φ_2, φ_3 and φ_4, will be defined later for

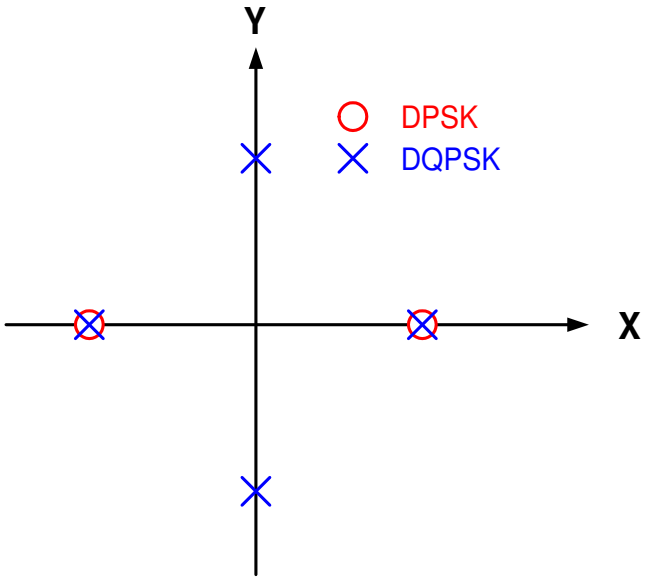

Fig. 67. Phase of the DPSK and DQPSK modulated signal

5.5Mbit/s and 11Mbit/s transmission modes separately. The 5.5Mbit/s data rate is achieved by transmitting 4-bit per symbol while the 11Mbit/s data rate is obtained by transmitting 8-bit per symbol. The fourth and seventh chips have a minus sign as shown in (5.2). This is the result of the 180° rotation created by the cover sequence to optimize the sequence correlation properties and minimize DC offsets in the codes.

$$\begin{aligned} \boldsymbol{c} \;=\; & \{e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{(j\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)}, -e^{j(\varphi_1+\varphi_4)}, \\ & e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j\varphi_1}\} \end{aligned} \tag{5.2}$$

where $\boldsymbol{c}$ is the CCK code word,

$\boldsymbol{c} = \{c_0, c_1, \cdots, c_7\}$ $\quad$ c_0 is always transmitted first in time.

Table XX. 5.5 Mbit/s CCK encoding table

Dibit pattern (d0, d1)	Even symbols	Odd symbols
00	0	π
01	$\frac{\pi}{2}$	$\frac{3\pi}{2}$
11	π	0
10	$\frac{3\pi}{2}$	$\frac{\pi}{2}$

For the CCK signal at 5.5 Mbit/s, 4 bits {d0, d1, d2, d3} (d0 first in time) are transmitted per symbol. The data bits d0 and d1 encode φ_1 based on DQPSK as shown in Table XX. The phase change for φ_1 is relative to the phase φ_1 of the preceding symbol. All odd-numbered symbols is given an extra 180° rotation, in addition to the standard DQPSK modulation as specified in Table XX. The first symbol is numbered "0" for the purposes of determining odd and even symbols. The data dibits d2 and d3 CCK encode the basic symbol by setting φ_2, φ_3 and φ_4 according to (5.3).

$$\begin{aligned} \varphi_2 &= (d2 \times \pi) + \frac{\pi}{2} \\ \varphi_3 &= 0 \\ \varphi_4 &= d3 \times \pi \end{aligned} \tag{5.3}$$

For CCK signal at 11 Mbit/s, 8 bits {d0, d1, $\cdots$, d7} (d0 first in time) are transmitted per symbol. The process of (d0, d1) is the same as in the 5.5Mbit/s

Table XXI. 11 Mbit/s CCK encoding table

Dibit pattern [di, d(i+1)]	Phase
00	0
01	$\frac{\pi}{2}$
10	π
11	$\frac{3\pi}{2}$

modulation. The dibit (d0, d1) encode φ_1 based on DQPSK as shown in Table XX. The phase change for φ_1 is relative to the phase φ_1 of the preceding symbol. All odd-numbered symbols is given an extra 180° rotation, in addition to the standard DQPSK modulation as specified in Table XX. The first symbol is numbered "0" for the purposes of determining odd and even symbols. The data dibits (d2, d3), (d4, d5), and (d6, d7) encode φ_2, φ_3, and φ_4, respectively, based on QPSK specified in Table XXI. Fig. 68 shows the 11 Mbits CCK pulse sequence. The 5 Mbits CCK has similar pulse sequence but at a low frequency.

2. The Detection of the 802.11b Baseband Signal

The detection of the can be conducted in a the optimum non-coherent demodulator. In the Additive White Gaussian Noise (AWGN) channel, the Maximum Likelihood (ML) receiver is the optimum receiver, given that both "0" and "1" are transmitted with equal priori probability. In a AWGN channel, the received signal has a normal distribution. To maximize the probability $p(r|s_m)$ is equivalent to find the s_m that minimizes the Euclidean distance

$$D(r, s_m) = \|r - s_m\|^2 \tag{5.4}$$

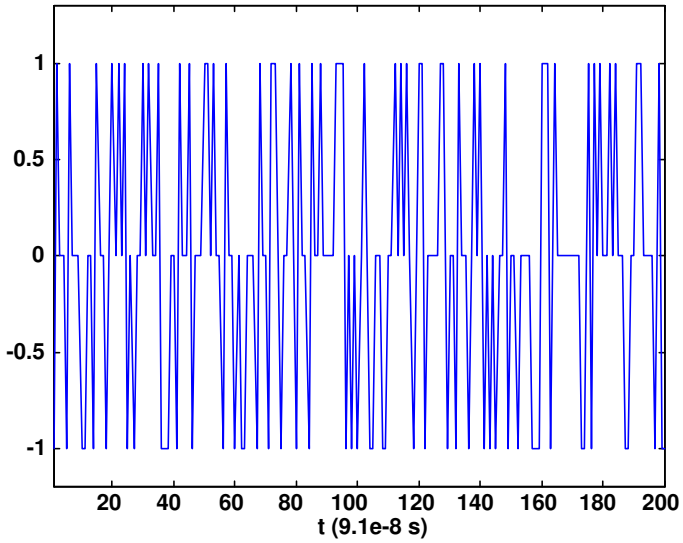

Fig. 68. The pulse sequence of 11 Mbits CCK modulated signal

where r is the received signal and s_m is the transmitted CCK code word, $m = 1, 2, \ldots, 16$.

By expanding (5.4), we have

$$\begin{aligned} D(r, s_m) &= \int_0^T (r(t) - s_m(t))(r(t) - s_m(t))^* dt \\ &= \|r\|^2 + \|s_m\|^2 - 2Re\Big(\int_0^T r(t) s_m^*(t) dt \Big) \\ C(r, s_m) &= 2Re\Big(\int_0^T r(t) s_m^*(t) dt \Big). \end{aligned} \tag{5.5}$$

Therefore, to minimize $D(r, s_m)$ is equivalent to maximize $C(r, s_m)$. We will build the optimum receiver based on the metrics, $C(r, s_m)$. The optimum receiver is illustrated in Figure 69.

The performance of the optimum non-coherent detector is simulated in the SystemView design environment. Fig. 70 illustrates the BER performance of the optimum non-coherent demodulator for each of the modulation format adopted in the

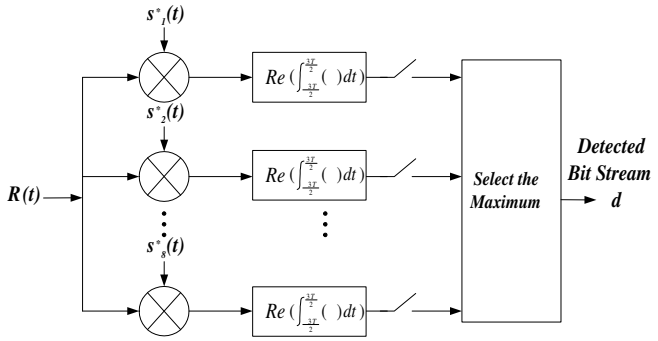

Fig. 69. The general block diagram of an optimum non-coherent detectors for the 802.11b baseband signal

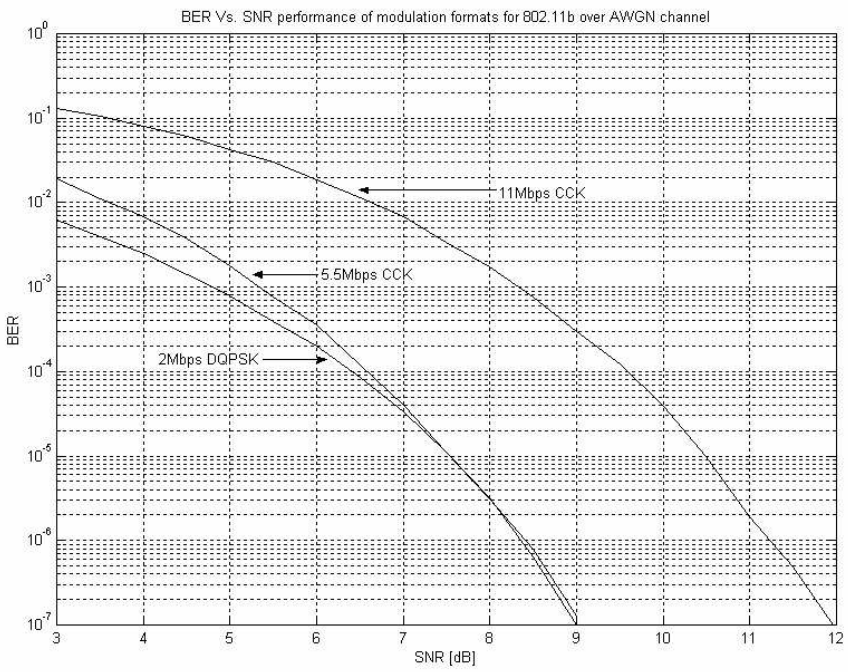

Fig. 70. SystemView simulated BER performances of optimum non-coherent demodulator

802.11b standard. The simulation setup in the SystemView is discussed in Appendix B. Since the complexity and implementation cost of the optimum non-coherent demodulator is high due to the number of the matching filters needed, especially in the CCK receiving mode, the demodulator is preferred to be implemented in the digital domain. Other simplified analog demodulators can also be used with an expectation of degradation in the detection performance.

B. ADI Design Approach for the Direct Conversion 802.11b/Bluetooth Dual-Mode Receiver

As we have mentioned the in Chapter II, both analog demodulator and ADC approaches can be used in the ADI design. For the 802.11b/Bluetooth dual-mode receiver, five different modulation formats co-exist in the baseband. If the analog demodulator approach is employed, five individual demodulators is required for each of the modulation formats. This results in significant increment in implementation cost and circuit complexity. In addition, the complexity involved in the 802.11b optimum non-coherent demodulators design makes it desirable to implement the demodulators in the digital domain. Therefore, the analog demodulator ADI approach becomes unrealistic for the dual-mode receiver, and ADC is the only candidate for the 802.11b/Bluetooth receiver.

The same fast settling requirement still exists in the 802.11b/Bluetooth receiver under the Bluetooth receiving mode as it is required in the Bluetooth receiver. Among the three ADI design approach that we analyzed in the chapter IV, besides the analog demodulator approach, the single ADC ADI approach is also able to provide a fast settling by skipping the VGA and AGC loop. The fast settling in this approach is achieved at a cost of increasing ADC dynamic range requirement. The Bluetooth

received signal has a dynamic range of 60 dB at the antenna [11]. With a single step gain control in the LNA as shown in Fig. 13, we reduced the signal dynamic range in front of the ADC to 30 dB. This greatly relaxes the ADC specs and makes the single ADC ADI design approach favorable in the 802.11b/Bluetooth dual-mode receiver.

Dynamic range and sampling rate are two major design specs for the ADC implementation. Both specs are governed by the modulation formats that are adopted in the wireless system. Several factors need to be considered when deriving the dynamic range of the ADC. Firstly, the continuous-to-discrete digitization process in an ADC inevitably generate error that is referred as quantization noise. Depending on the baseband data modulation format, the ADC quantization noise power needs to be suppressed to guarantee the proper detection of the received signal. Secondly, the ADC also needs to accommodate the power variation of the received signal in front of the ADC. This is determined by the receiver architecture. In Chapter III, we derived the formula for the ADC dynamic range, DR_{ADC}, as shown in (3.15). For convenience, we re-write the equation here.

$$DR_{ADC} = S/N_{quan.} + DR_{sig} + Design\ Margin \tag{5.6}$$

Where $S/N_{quan.}$ is the quantization noise floor in the ADC that is determined by the SNR requirement of demodulator; DR_{sig} is the signal dynamic range in front of the ADC. A design margin of 4 to 10 dB is also applied as a common practice in the ADC design to accommodate the possible peaking of the received signal. The sampling rate that is applied in the ADC should not only excess the Nyquist rate with respect to the largest signal bandwidth in the system, but also satisfy the synchronization requirement of the data detector. The multi-standard receiver environment usually complicates the ADC design because more modulation formats are involved.

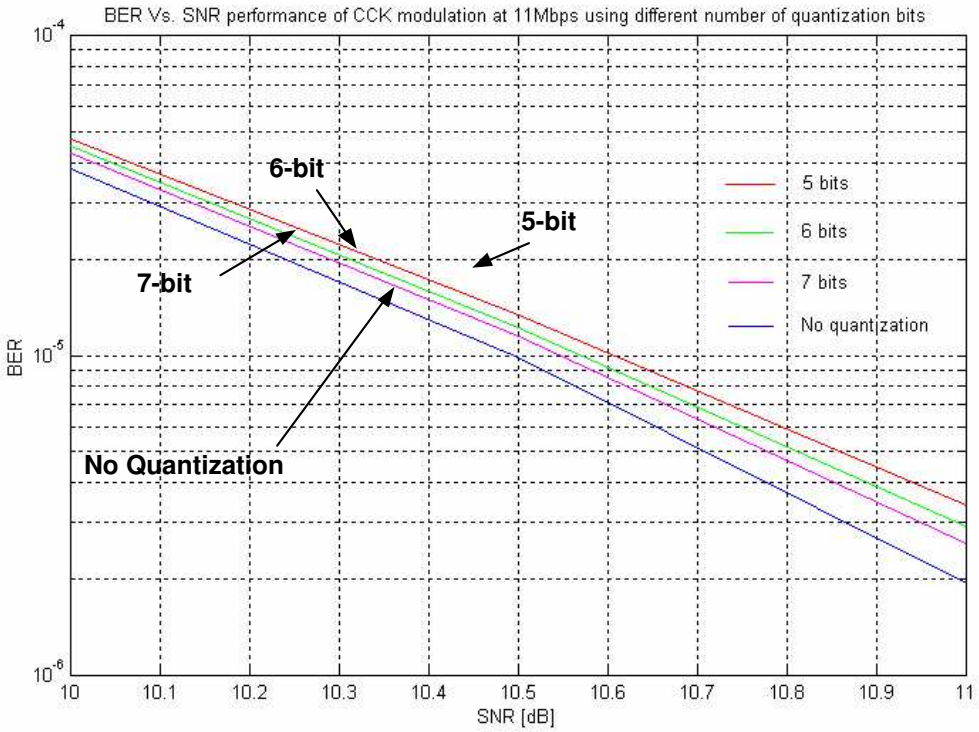

Fig. 71. The effect of ADC quantization noise on the 802.11b 11Mbit/s CCK signal demodulation

The 802.11b standard includes 3 modulation formats for 4 different data transfer rates. Bluetooth standard adopts a 1 Mbit/s GFSK signal. Table IX in Chapter III summarizes the characteristics of the 802.11b and Bluetooth modulated signals. Matlab and SystemView programs are developed to build non-coherent demodulators for the Bluetooth and 802.11b systems. Through the simulation conducted in those demodulator models, we can obtain the $S/N_{quan.}$ and minimum sampling rate for each of the modulation formats.

Fig. 71 and 72 show the effect of quantization noise on the BER performance of the 802.11b CCK and Bluetooth GFSK demodulators, respectively. These two plots determine the maximum tolerable quantization noise level in the demodulators or quantization noise floor $S/N_{quan.}$ in the ADC. 5-bit ADC can provide enough resolution for both the 802.11b and Bluetooth receiver system. The received signal

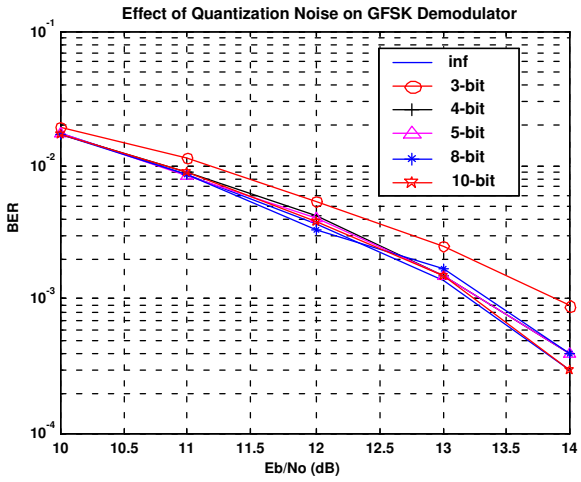

Fig. 72. The effect of ADC quantization noise on the Bluetooth GFSK signal demodulation

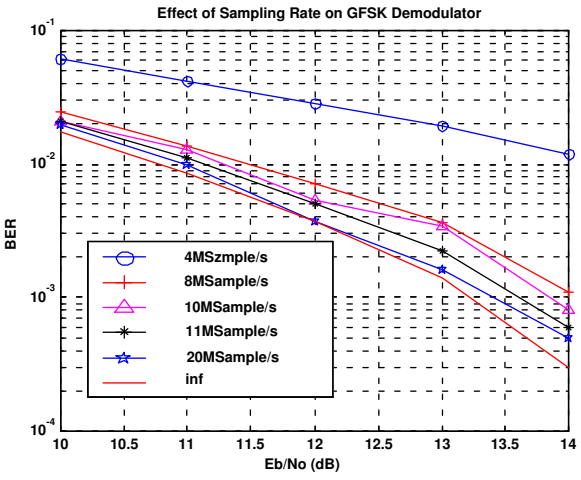

Fig. 73. The effect of sampling rate on the Bluetooth signal demodulation

dynamic range at the antenna is -80 dBm to -20 dBm for the Bluetotoh system and -80 dBm to -10 dBm for the 802.11b system. As we mentioned before, A single step gain control in the LNA provides a 30 dB reduction in the signal dynamic and results a DR_{sig} of 30 dB during the Bluetooth receiving mode. In the 802.11b receiving mode, the AGC settling requirement is much relaxed. Fine gain control steps are applied in the VGA to reduce the received signal dynamic range to 6 dB in front of the ADC. Using equation (5.6), the ADC dynamic range specs for 802.11b and Bluetooth receiving mode are 46 dB and 64 dB, respectively. In a direct-conversion receiver, the received signal is converted to DC directly. The maximum bandwidth of the received 802.11b and Bluetooth signals are 5.5MHz and 550kHz accordingly. However, in the system simulation, the required sampling rates for both standards are higher than the Nyquist rates in order to provide the synchronization accuracy needed in the demodulator. For 802.11b receiver, the synchronization requirement is simple, since its baseband signal is in form of square wave. To avoid detection error, 4 samples per bit is enough. As a result, a 44 MSamples sampling rate is applied for the 802.11b receiving mode to satisfy the highest data rate of 11 Mbit/s. The deriving of the sampling rate specs for the Bluetooth receiving mode is not that straightforward. Simulation in the Matlab demodulator model is performed to get this requirement. As illustrated in Fig. 73, an 11MSamples sampling rate is needed for the Bluetooth signal to prevent severe degradation in the BER performance. Furthermore, low power consumption is always a priority for an ADC embedded in a receiver. Table XXII summarizes the ADC specifications for the 802.11bBluetooth ADI design.

A multi-standard receiver is not a simple combination of individual receivers that operate under each standard. To optimize implementation cost for the multi-standard receiver, maximum circuit block sharing is required. Therefore, configurability is another important aspect in the multi-standard ADC design. Configurability allows

Table XXII. ADC specs

Specs	802.11b	Bluetooth
SNR	46 dB	66 dB
ENOB	8-bit	11-bit
Sample Frequency	44 MHz	11 MHz
Signal Bandwidth	5.5 MHz	550 kHz
Input Voltage Swing	$2V_{pp}$	$2V_{pp}$
DNL	<0.25 LSB	<0.25 LSB
INL	<1 LSB	<1 LSB
Supply Voltage	2.5 V	2.5 V
Current Consumption	minimum	minimum

the ADC minimizing the extra silicon area and power dissipation that are required to digitize different data formats. How to configure the ADC to share circuit blocks in 802.11bBluetooth dual-mode receiver is an interesting topic to be addressed in this research work.

C. ADC Architectures

According to the ratio between sampling rate, also known as sampling frequency, and input signal bandwidth, ADCs can be classified into two categories, the Nyquist rate ADCs and over-sampling ADCs. The Nyquist rate ADCs comply with the Nyquist laws. Their sampling rate is at or slightly higher than the Nyquist rate (F_{Ny}), which is twice of the signal bandwidth. In an over-sampling ADC, the sampling rate (F_S) is usually much high than the Nyquist rate. Over-Sampling Ratio (OSR) in such an ADC is defined as $M = \frac{Fs}{F_{Ny}}$ and usually is between 8 to 256. Several important

ADC architectures will be discussed in this section as a background knowledge for the selection of proper ADC structure for the 802.11b/Bluetooth dual-mode receiver.

1. Flash/Flash Interpolation ADC

A flash/flash interpolation ADC is able to achieve high speed due to the parallel comparison and distributed sampling mechanism.[35] Fig. 74 shows the schematic of a N-bit flash ADC. It consists of a resistor ladder, a decoder, $2^N - 1$ preamps and comparators. The resistor ladder comprises $2^N - 1$ equal segments, which divide the full scale reference voltage into 2^N equally spaced reference voltage nodes. The preamps amplify the voltage difference between the input signal and the corresponding reference voltage before the comparators make the comparison. For example if the analog input is between reference voltage V_{Ri} and $V_{R(i+1)}$, comparator A_1 through A_i produce "1" while the rest generate "0". More comparators can be placed between the preamps and transfer the ADC structure to a flash interpolation architecture. As a result, the number of the preamps and ADC power consumption is reduced at a cost of linearity.

The number of the preamps and comparators that are required in an N-bit flash ADC is $2^N - 1$. Thus the power consumption and silicon area used by flash ADC increases exponentially with the number of bits produced by the ADC. Using interpolation in the flash ADC can help to reduce the number of the preamps, but the power and silicon area cost still increases rapidly as the ADC number of bits grows up. The resolution and linearity of the flash/flash interpolation ADC are usually limited to 6 or 8-bit due to the non-ideality in the circuits. The most significant factors are the DC and AC bowing. The non-ideality of the comparators and mismatching among the resistors can introduce substantial errors in reference voltage generated by the resistor ladder and cause bowing in the DC voltage. The capacitive feedthrough at

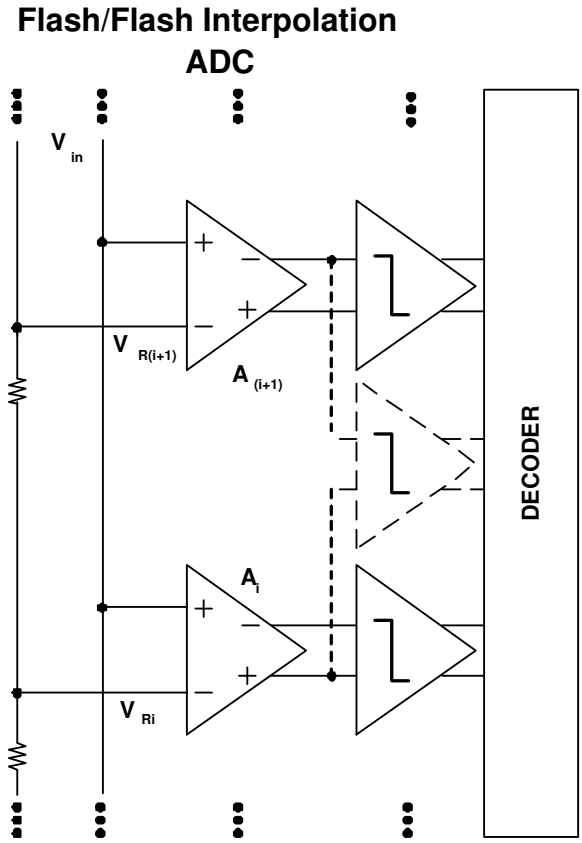

Fig. 74. The schematic of a flash/flash interpolation ADC

the inputs of the comparators causes transient error that can be seen as AC voltage bowing. Therefore, the flash/flash interpolation ADCs are often used in those applications that require high speed but low resolution or small dynamic range.

2. Two-step ADC

As the resolution requirement increases, the implementation cost of a flash ADC, in term of power and silicon area, grows exponentially. In practical design, the flash ADC is hardly used for resolutions above 8-bit. Other alternatives are needed for the high resolution applications. Two-step ADC is one of these alternatives. It trades speed for low power consumption and small silicon area [35].

Fig. 75 shows the conceptual schematic and timing diagram of a typical two-step ADC. It consists of a coarse and a fine sub-ADC that operate subsequently in time. First, the course sub-ADC digitizes the analog input and yields the Most Significant Bits (MSBs) of the entire ADC. Then the quantization error of the coarse sub-ADC, also known as "residue", is further digitized by the fine sub-ADC to obtained the Least Significant Bits (LSBs). Together the two sub-ADCs generates the required resolution. Since the AD conversion is completed in two separated stage, this type of ADCs are called two-step ADCs.

In a two-step ADC, the residue is generated by subtracting the coarse sub-ADC output from the analog input. A Digital to Analog Converter (DAC) is used to convert the coarse sub-ADC output, MSBs, into analog voltage. Flash ADC structure is usually used to implement the sub-ADCs. The bits division between the coarse sub-ADC and fine sub-ADC can be any combination. As a common practise, the bits are divided equally between the two sub-ADCs, such that the same sub-ADC design can be re-used in both stages. A Sample-and-Hold (S&H) circuit is placed in front of the two sub-ADCs stages. It plays a critical role in the ADC. The S&H circuit

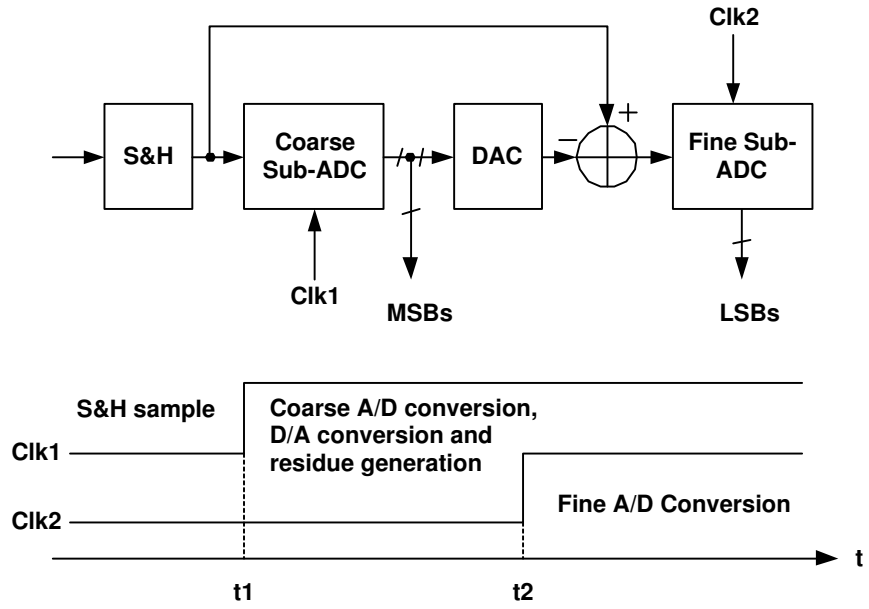

Fig. 75. Block diagram of a two-stage ADC ADC

assures that the voltage sensed by the residue subtractor equals to the one digitized by the coarse sub-ADC. That relaxes the maximum allowable slew rate of the input signal. Other variations of the two-step ADC also appear in the ADC design, such as the two-step recycling ADC and two-step subranging ADC. However, the operation principles are the same.

The two-step architecture allows ADCs to achieve high resolution with low implementation cost, but this is achieved by sacrificing speed. To obtain certain sampling rate, the circuit has to work at twice of the sampling frequency. This type of ADC fits best in those moderate resolution and low speed applications.

3. Pipeline ADC

Pipeline mechanism has been widely used in the digital system to improve the throughput. The same concept can be applied in the ADC design as well [35].

By examining the operation of the two-step ADC, we can find that both of the

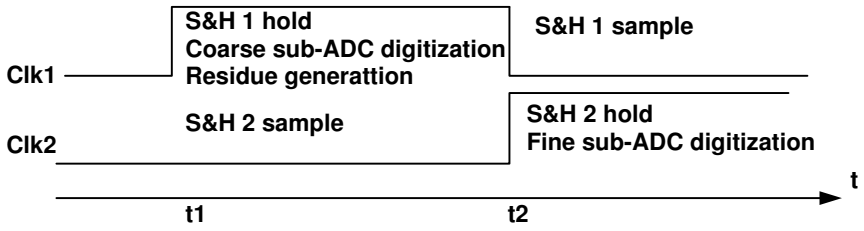

Fig. 76. Clock diagram of a two-step pipelined ADC

two sub-ADC operates for only half of the clock cycle. The first coarse sub-ADC stage is idle when the second fine sub-ADC stage is processing the residue and the second sub-ADC stage is idle when the first stage is producing the residue. The efficiency of the two-step ADC can be improved by pipelining the operation in the two stages. Fig. 76 illustrates the clock diagram of the pipelined two-step ADC. Now, the first stage coarse sub-ADC is sampling the input while the second stage fine sub-ADC is digitizing the residue that is generated in the previous clock cycle. The two sub-ADC stages are now operating in a pipelined fashion and the sampling rate of the ADC is therefore doubled comparing to the simple two-step ADC. In this two-stage pipeline ADC, the throughput rate of the ADC is limited only by the speed of each stage. Since both of the sub-ADC stage can be implemented with flash structure, the speed of a pipeline ADC can be comparable to the flash ADC. In order to implement the pipeline ADC, another S&H circuit is needed in the second fine sub-ADC to hold the residue generated by the first stage in the previous clock cycle. Fig. 77 shows the schematic of the two-stage pipeline ADC. A delay circuit is applied to output of the coarse sub-ADC to synchronize the MSBs and LSBs.

More sub-ADC stages can be added in the pipeline ADC to achieve high resolution. Fig. 78 shows a conceptual schematic of a multi-stage pipeline ADC. Each of its stage except for the last stage, which contains only a sub-ADC, consists of a sub-ADC, a S&H, a DAC, a subtractor that detects the residue and a gain stage.

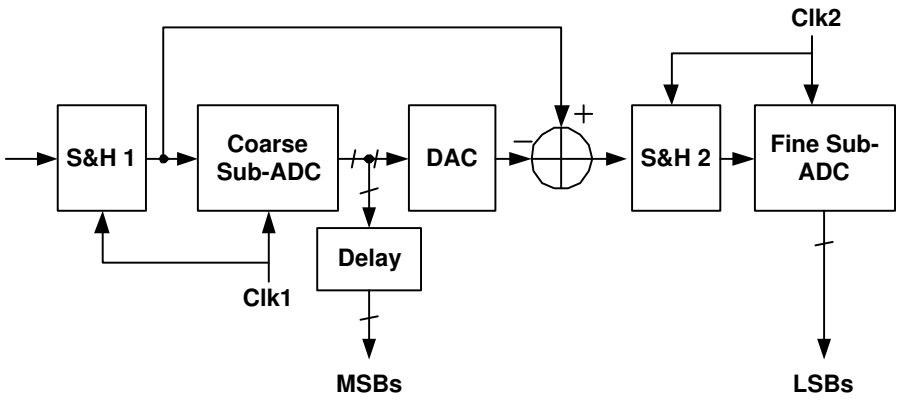

Fig. 77. Schematic of a two-step pipelined ADC

Usually the same reference voltage is applied throughout all the stages. The gain stage in each pipeline stage is also called residue amplifier. It is used to amplify the residue in order to utilize the full swing of the sub-ADC in the following stage. Thus, for a n-bit stage, the gain in the residue amplifier should be 2^n. In the many circuit implementations, the function of S&H, DAC, residue detector and amplifier is performed by a single circuit called Multiplying DAC (MDAC), as we will explain in Chapter VI

The adjacent stages in a pipeline ADC often have overlap in their output bits. The redundancy between two neighboring stage makes the amplified residue of the previous stage occupies only part of the sub-ADC swing in the later stage. Therefore, the sub-ADC in the previous stage can tolerate bigger offset without saturating the later stages. Together with the digital correction techniques, the pipeline ADC structure with redundant bits suppresses the error caused by the non-ideality of the sub-ADCs [59]. Considering the bit overlap between the adjacent sub-stages, the gain of the residue amplifier in a n-bit stage becomes 2^{n-x}, where x is the number of bits overlapped. $n - x$ is also referred as effective number of bits of the pipeline stage.

Pipeline ADC provides comparable speed as the flash ADC. However, its power

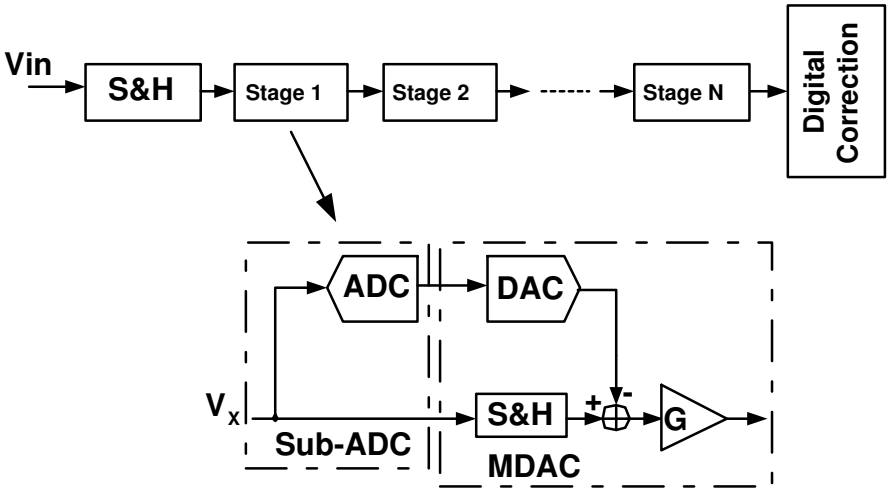

Fig. 78. Schematic of a multi-stage pipelined ADC

consumption grows almost linearly instead of exponentially as the resolution requirement increases. This is because that the higher resolution in a pipeline ADC is achieved by adding more stages. For a resolution higher than 10-bit, usually calibration is needed in the pipeline ADC due to process technology limitation. Thus, the pipeline ADCs are often used in the applications requires moderate speed and high speed.

4. ΣΔ ADC

Over-sampling ADCs often appear in the applications that require high resolution. By natural, the over-sampling in the ADC lowers the noise floor and the SNR is improved. The SNR of an over-sampling ADC without noise shape can be expressed as,

$$SNR = 6.02N + 1.76 + 10log_{10}\frac{F_S}{F_{Ny}} \tag{5.7}$$

Where N is the number of the bits of the ADC, and $\frac{F_S}{F_{Ny}}$ is the OSR. Referring to

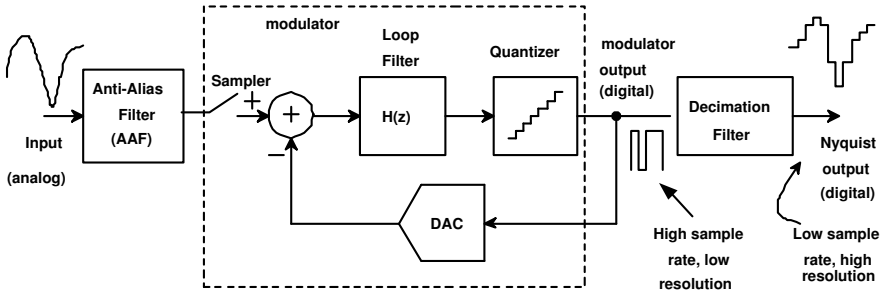

Fig. 79. Block diagram of a ΣΔ ADC

(3.14), the SNR increases by a factor of $10log_{10}\frac{F_S}{F_{Ny}}$ comparing to Nyquist rate ADC. According to (5.7), the SNR improves 3 dB as the OSR doubles in an over-sampling ADC. However, the high OSR and the resulted high power consumption are not affordable in many applications that require high resolution. ΣΔ is one type of over-sampling ADCs that further improves the SNR with noise shaping and hence reduces OSR. Fig. 79 illustrates the block diagram of a ΣΔ ADC.

A ΣΔ ADC usually consists three parts, a frontend anti-aliasing filter, a ΣΔ modulator and a digital decimation filter. The frontend anti-aliasing filter is used to suppress the high frequency noise that will be folded into the signal bandwidth by the sampling in the ADC. Its cutoff frequency is usually set to be half of the sampling frequency. The over-sampling ΣΔ ADC often has high sampling frequency. Thus the anti-aliasing filter can be quite simple. The core of the ΣΔ ADC is the ΣΔ modulator, which performs noise shaping in the ADC and converts the analog signal into low resolution noise shaped digital signal. The third part, digital decimation filter, is deployed to filter out the out band noise in the digital domain. It converts the low resolution digital signal from the ΣΔ modulator into high resolution digital signal at a low sampling rate usually equal to twice of the signal bandwidth.

The operation of a ΣΔ modulator is a nonlinear phenomenon because of the strong non-linearity of the quantizer. Rigorous analytical treatment has proven diffi-

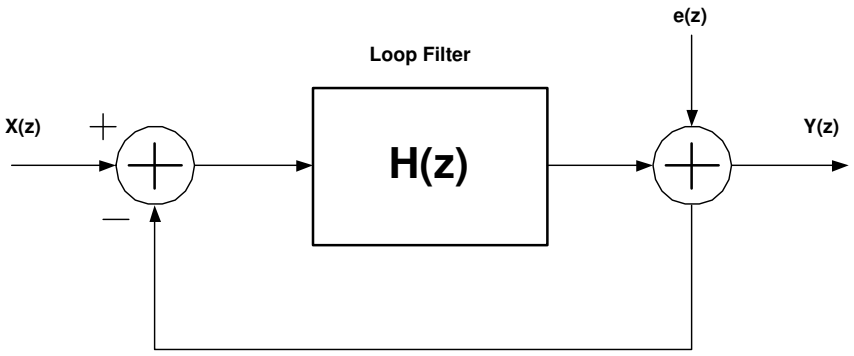

Fig. 80. Linear model of a ΣΔ modulator

cult or even impossible. The linearized model shown in Fig.80 is simple approximation to provide some insights to the noise shaping function of a ΣΔ modulator. In the linear model, the quantization noise of the ADC is modelled as e(z). If the input and output of the ΣΔ modulator are X(z) and Y(z), respectively, Y(z) can be expressed as

$$Y(z) = \frac{H(z)}{1 + H(z)} X(z) + \frac{1}{1 + H(z)} e(z) \tag{5.8}$$

The gain factor, $\frac{H(z)}{1+H(z)}$, for the input signal X(z), is the Signal Transfer Function (STF). Whereas the gain factor, $\frac{1}{1+H(z)}$, for the quantization noise e(z), is the Noise Transfer Function (NTF). We may observe that, if $|H(z)|$ has a lowpass response and is very large within the frequency band of interest, the gain of $e(z)$, $|NTF| = |\frac{1}{1+H(z)}|$, would be nearly zero and suppress the quantization noise at the frequency band of interest.

With the over-sampling and noise shaping, the ΣΔ ADC is able to provide very high resolution. However, the operation frequency of the circuit now will be at 2OSR times of the signal frequency. Because of the speed limitation of the current process technology and power dissipation constraint in the system, the ΣΔ cannot be used

Table XXIII. ADC architectures and their targeting applications

ADC Structure	Signal bandwidth	Resoltion
Flash and Flash Based	High, several hundred MHz to GHz	Low, <8-bit
Pipeline and Parallel Pipeline	High, up to several hundred MHz	Media/High, Up to 12, 14-bit
Two-step	Media, Up to several tens MHz	Media, <12-bit
Sigma Delta	Low, Up to several MHz	High, >14-bit

in some wideband applications.

The ADC structures discussed in this section have different features in their performance and limitation. The selection of the ADC for certain receiver system largely depends on the data format in the application. Table XXIII gives a general guideline for the ADC selection in the system design.

D. Configurable Time-Interleaved Pipeline ADC Structure

In order to reduce power consumption and silicon area in a multi-standard receiver, the circuit blocks are preferred to be shared among different standards. One most straightforward way of implementing a multi-standard ADC is to design an ADC that meets all the toughest requirements. That is to design for the fastest speed and largest dynamic range requirements. However, the extra power dissipation and possible increment in silicon area can not be justified for the low speed or low dynamic range receiving mode. As an alternative, individual ADC is used in different receiving mode as appearing in some reported multi-standard receiver design. That approach

needs more silicon area since no circuit blocks can be shared among the ADCs. As mentioned in section B, the power and silicon area optimization in a multi-standard receiver requires maximum sharing of circuit blocks in the ADC part. Therefore, in the ADC design for the 802.11b/Bluetooth dual-mode receiver, we need to not only satisfied the ADC specifications for each of the receiving mode, but also provide the desired programmability if possible.

1. Selection of Proper ADC Architecture for 802.11b/Bluetooth Dual-Mode Receiver

Previously, only ΣΔ ADCs with adjustable Over-Sampling-Ratio (OSR) have been reported in multi-standard applications [60]. As shown in Fig. 79, a ΣΔ ADC consists of a ΣΔ modulator and a digital decimation filter. The bandwidth of the ADC can be easily configured by adjusting the cutoff frequency of the digital decimation filter. The dynamic range of a ΣΔ ADC, however, can not be altered conveniently. The noise transfer function of a ΣΔ ADC modulator is illustrated in Fig. 81. For wideband signal, more noise power is presented with the signal bandwidth and results in a reduced ADC SNR or dynamic range performance. When the signal bandwidth is small, less noise power appears in the signal bandwidth, which leads to a higher SNR or dynamic ranger for the ADC. Due to the noise shaping, the changes in the ADC dynamic range between narrow band and wide band signals are large. Therefore, a ΣΔ ADC can be configured conveniently for wider bandwidth with smaller dynamic range, or narrower bandwidth with higher dynamic range, by programming or reconfiguring the digital decimation filter. Thus ΣΔ ADCs can be deployed in multi-standard wireless receivers.

Two factors ultimately limit the usage of the ΣΔ ADCs in some multi-standard receivers. Firstly, the the over-sampling nature of the ΣΔ ADC prevents it to be used

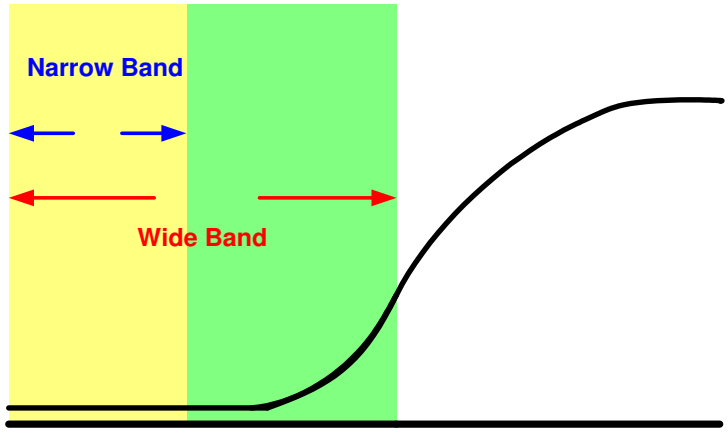

Fig. 81. Noise transfer function of a ΣΔ modulator

in wide-band applications. The OSR of a ΣΔ ADC is usually more than 8 times of the Nyquist sampling frequency. The ADC circuit has to operate at a much higher frequency than the signal bandwidth. As a result, most ΣΔ ADC implementations are seen in those systems with a signal bandwidth that is less than 1 MHz. Secondly, the drastic changes in the ADC dynamic range as the ΣΔ ADC switches among standards complicates the design of the ADC and other blocks in the receiver. In some cases, due to the large performance difference between various communication standards, the ΣΔ modulator noise shaping filter coefficients and sampling frequency may have to be adjusted as well. This will inevitably increases the design complexity. In other cases, a fine received signal power level control is required to satisfy the dynamic range that can be provided by the ΣΔ ADC.

For our specific case of the 802.11b/Bluetooth dual-mode receiver, the 5.5 MHz 802.11b signal has a too wide bandwidth for the ΣΔ ADC to handle. Equation (5.9)calculates the SNR or dynamic range of an L-th-order n-bit ΣΔ ADC with an OSR=M. To achieve a 46 dB SNR required for the 5.5 MHz 802.11b CCK signal. A minimum OSR of 9 is required for a $3^n d$ order one-bit ΣΔ ADC. The corresponding

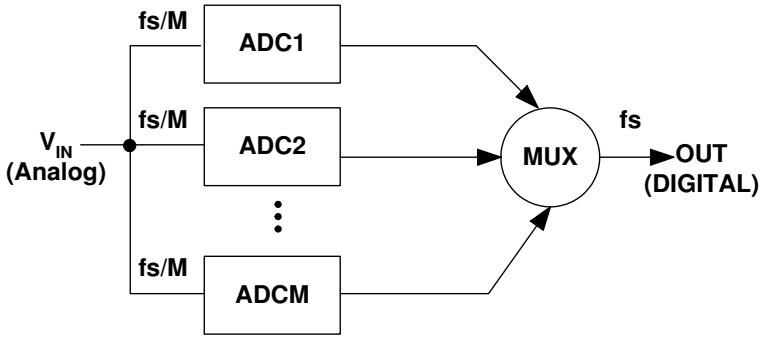

Fig. 82. The block diagram of a time-interleaved ADC

sampling rate needed in the ADC is 99 MHz. To design such a high speed ADC, the power consumption involved is not affordable in a 802.11b/Bluetooth receiver. Other solutions are desired to solve the programmability issue in the ADC design.

$$DR_{\Sigma\Delta ADC} = \frac{2}{3}\frac{2L+1}{\pi^{2L}}M^{2L+1}(2^n - 1)^2 \tag{5.9}$$

The ADC proposed for the 802.11b/Bluetooth dual-mode receiver in this research work is a configurable time-interleaved pipeline ADC. Time-interleaved ADC structure has been used in the high speed AD conversion applications [61]- [65]. Fig. 82 shows the structure of a time-interleaved ADC. It consists of multiple identical ADC branches that operate in a time-interleaved fashion. As a result, the power consumption of the entire ADC is lowered by reducing the sampling rate of each ADC branch to only a fractional of the overall sampling frequency, $\frac{F_S}{N}$, where F_S is the overall sampling rate and N is the total number of the identical ADC branches. Note that the overall sampling rate of the time-interleaved ADC, F_S, can also be interpolated as $N\frac{F_S}{N}$, the sampling rate of each ADC branch times the number of the ADC branches. This observation indicates that the overall sampling rate of a time-interleaved ADC can be programmed by deploying different number of the ADC branches in operation. The ADC structure for the 802.11b/Bluetooth dual-mode receiver is proposed based

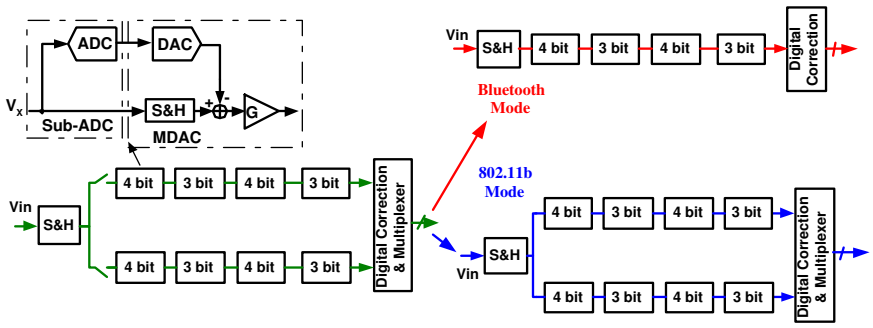

Fig. 83. Configurable time-interleaved pipeline ADC for 802.11b/ Bluetooth dual-mode receiver

on this new perspective. The configurable time-interleaved ADC is illustrated in Fig. 83. It consists of two identical 11-bit pipelined ADC branches that are designed to working at 22 MSample/s. Both of them operate during the 802.11b receiving mode to provide an overall 44MSample/s sampling rate. Only one pipeline branch is activated in the BT receiving mode and the sampling rate can be easily scaled down to 11MSample/s since both branches are designed for 22MSample/s. To save power in the 802.11b mode, the last stage in each pipeline branch can be disabled while still providing the required dynamic range. With the programmability in the ADC, we can share the same circuit blocks for both receiving modes. In high speed 802.11b receiving mode, we benefit from the time-interleaved structure to bring down the ADC power dissipation. Silicon area wise, the time-interleaved ADC trades off area for power dissipation. However, the overall silicon area used by the proposed ADC is less comparing to the two individual ADCs solution.

2. Pipeline ADC Branch in the Configurable Time-Interleaved ADC

We already mentioned in the previous subsection that pipeline ADC structure is used for the ADC branches in the time-interleaved ADC. The reason for this se-

lection is that pipeline structure is suitable for the implementation of the ADC branches because of the moderate A/D conversion resolution and speed required by the 802.11b/Bluetooth dual-mode receiver. To provide the required resolution, the pipeline ADC branch can have many different combination in the stage arrangement. We can use either multiple-bit stage or the 1.5-bit stage. In the 1.5-bit stage pipeline ADC, each stage provides 2-bit output. Since there is 1 bit overlap between adjacent sub-stages, the effective resolution of each stage is 1.5-bit. The multi-bit stage pipeline ADC refers to the pipeline whose stage has more than 2-bit output. Considering the receiver environment, power optimization should be the first priority in the ADC design and will be the guideline in choosing the pipeline branch structure.

In the pipeline ADC branch, each stage except for the last one has a gain for the residue, which is the input signal of the next stage. We can consider the pipeline ADC branch as a cascade system and use (5.10) to calculate its overall input referred error. In (5.10) e_{TOT} is the total input referred error of the pipeline ADC; e_i $(i = 1, 2, ..., m)$ is the error in stage i and G^k is the residue gain in the k^{th} stage. From the equation, we find that the error in each stage is attenuated by the gain in the previous stages when mapping to the input. Therefore, bigger error including offset, components mismatch and noise can be tolerated in the later stages in the pipeline ADC branch.

$$e_{TOT} = e_1 + \sum_{i=1}^{m-1} \frac{e_{i+1}}{\prod_{k=1}^{i} G^k} \tag{5.10}$$

Referring to subsection C.3, the residue gain of each stage in a pipeline ADC equals 2^{n-x}, where $n - x$ is the effective number of bits in that stage. By deploying high bits MSB sub-stages, we will have higher gain in those sub-stages. This can relax the design requirements in the LSB sub-stages, such as gain of the amplifier, kT/C noise and mismatching requirement among capacitors when switched-capacitor

circuit is applied. As a result, we can deploy smaller capacitors in the LSB sub-stages, and hence amplifiers with low speed can be used. The implementation cost in term of power dissipation and silicon area can be reduced. The multi-bit stage pipeline ADC has been adopted widely in high resolution applications for power efficiency [66] [67]. However, using high bits sub-stages increases the load seen by the previous sub-stages. Especially the high bits first stage will load the frontend S&H circuit. Since the S&H has to provide a better accuracy and linearity than the overall ADC resolution, the large load demands extremely high speed in the S&H and usually will result in large power dissipation. As a good compromise, the bits per stage is often limited to 3 and 4 in the practical circuit design. In the proposed configurable time-interleaved pipeline ADC design, 4-bit first stage is employed to explore the power saving advantage of the high bits MSB sub-stages.

Further analysis at the circuit level is necessary to define the rest of the sub-stages in the pipeline. In circuit implementation, more preamps and comparators are used in the sub-ADCs of the multi-bit sub-stages pipeline while the number of MDACs is reduced in comparison to the 1.5-bit sub-stages structure. The MDACs are usually the major contributor in power consumption. We will provide more analysis and proof for this argument in Chapter VI. Even though the OpAmp for the MDAC in a 1.5-bit stage has smaller load than the one in a multi-bit stage does, the GBW requirements are the same. Therefore, the power consumed in the MDAC is not directly proportional to the load. As a result, although each MDAC in the multi-bit stage pipeline consumes more power, the overall power dissipation can still be lowered because of the drastically reduction in the total number of the MDACs. Furthermore, due to low residue gain in the 1.5-bit sub-stages, the MSB sub-stages require high-gain OpAmps and large capacitors to meet the matching requirement. Consequently, more current is needed in the circuit design. Other things also favor the deployment

of multi-bit sub-stages. The BiCMOS process provide low power, high gain and high speed implementation for the OpAmp in MDAC. The input sampling circuit in the sub-ADCs is specially designed to avoid loading the previous MDAC, which helps to relax the slew rate and speed specs for the MDAC OpAmp. 2X flash interpolation sub-ADC is employed to minimize the additional preamps required by the multi-bit stage. Those circuit design measures will be discussed in detail in Chapter VI. Based on these observations, we decide to use multi-bit stage for the rest part of the pipeline ADC to explore the potential of power saving. A bonus we obtain by using multi-bit stage pipeline ADC branches is that we reduce the intrinsic delay in the ADC, which is applauded in real-time response receiver systems. As illustrated in Fig. 83, the pipeline ADC branches in the time-interleaved ADC is formed by an interweaved 4-bit and 3-bit stage. Noticing that the 4-bit stage is loaded by a lower bit stage, and therefore less driving capacity is required in the 4-bit substage. This arrangement allows us taking advantage of the power saving in the higher bit stage, the 4-bit stages, without the disadvantage of the associated excessive load. The 3-bit sub-ADC employs a flash architecture. The 4-bit ADC adopts 2X flash interpolation structure.

E. Non-Idealities in the Time-Interleaved Pipeline ADC

Besides the common design challenges faced by the pipeline ADC, the time-interleaved structure brings new issues to the ADC design. In this section, we will discuss the non-idealities in the time-interleaved pipeline ADC and derive the requirements for each circuit block.

1. Design Concerns in the Time-Interleaved ADC

The mismatch between the pipeline ADC branches causes different offset, residue gain and skew in the sampling time. These non-idealities introduce the offset error, gain error and timing skewing into the time-interleaved ADC. Timing skewing is also known as phase skewing in some literatures. Notice the errors discussed here are relative errors that are caused by mismatch specifically in the time-interleaved ADC. The absolute errors due to the process and design imperfection are not included here since they are general issues encountered in any ADC design. Those errors will be discussed in the next two sub-section.

To analyze the effect of those error, we developed a simplified time domain transfer function of the ADC as expressed below

$$\begin{aligned} Y(t) &= X(t) \sum_{n=-\infty}^{\infty} (A_1\delta(t-(2n-1)T_s) + A_2\delta(t-2nT_s)) + \\ &\quad \sum_{n=-\infty}^{\infty} ((B_1+\Delta_1)\delta(t-(2n-1)T_s) + (B_2+\Delta_2)\delta(t-2nT_s)) \end{aligned} \quad (5.11)$$

T_s is the sampling interval of the ADC, which equals to $1/44MSample/s = 22.7ns$. $Y(t)$ are the ADC output, which is produced by sampling and digitizing the continuous input of X(t) in the two pipeline ADC branches. $\delta(t)$ is the impulse response of the sampling function. A_1, A_2 are the gain in branch 1 and 2; B_1, B_2 are the offset of branch 1 and 2. Δ_1, Δ_2 are the quantization error generated in branch 1 and 2. If only gain mismatch exists between the two branches, we have $\delta_A = A_1 - A_2$ and $B_1 = B_2 = B$. Given a sinusoidal input $X(t) = sin(2\pi f_{IN}t)$, the transfer function of the ADC can be re-written as

$$Y(t) = (A_1 sint(2\pi f_{IN} t) + B + \Delta) \sum_{n=-\infty}^{\infty} \delta(t - nT_s) + \delta_A sint(2\pi f_{IN} t) \sum_{m=-\infty}^{\infty} \delta(t - (2m-1)T_s) \quad (5.12)$$

Here Δ is the quantization error of the entire ADC. Now we have a second term of $\sum_{m=-\infty}^{\infty} \delta_A X(t)\delta(t - (2m-1)T_s)$ in the transfer function. By applying the discrete Fourier transform to (5.12), we can have a power spectrum of the ADC output as shown in Fig. 84. We have a second harmonic tone and a tone at frequency of $f_S/2 + f_{IN}/2$, where f_S is the sampling frequency of the time-interleaved ADC and f_{IN} is the input signal frequency. To achieve 11-bit dynamic range, we need to suppress that tone under the quantization noise floor. Therefore, the δ_A needs to be smaller than $\frac{1}{2^{11}}$. Notice that the error power in Fig. 84 is a result of gain mismatch. The absolute gain error in each stage and the S&H circuit needs also be suppressed. However, it is an design issue for pipeline ADCs in general not specifically for the time-interleaved pipeline.

From (5.11), we can also derive the transfer function of the ADC with only offset error as in (5.12). Here we assume that the $A_1 = A_2 = A$, $\delta_B = B_1 - B_2$.

$$Y(t) = (A_1 sint(2\pi f_{IN} t) + B + \Delta) \sum_{n=-\infty}^{\infty} \delta(t - nT_s) + \delta_B \sum_{m=-\infty}^{\infty} \delta(t - (2m-1)T_s) \quad (5.13)$$

In the power spectrum, the term caused by the offset mismatch results in a tone at $f_S/2$, as shown in Fig. 85. The δ_B needs to be smaller than $\frac{LSB}{2}$ to achieve the required resolution. Same as in the gain error analysis, this offset error is a relative error caused by mismatch in the two pipeline ADC branches.

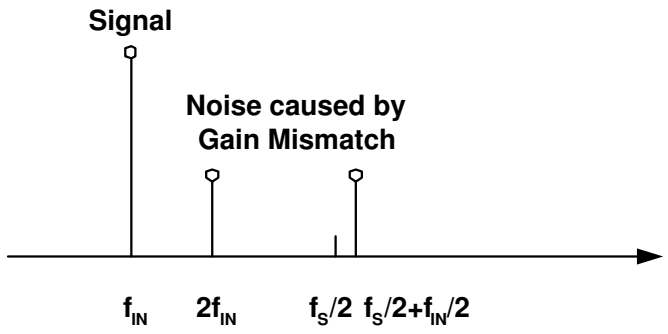

Fig. 84. Spectrum of a 2-branch time-interleaved ADC output with a sinusoidal input and gain mismatch between the branches

The timing skew in the time-interleaved ADC is caused by different timing in the two branches when the S&Hs change between sampling phase and hold phase. The transfer function of the ADC with timing skew can be expressed as

$$\begin{aligned} Y(t) &= (Asint(2\pi f_{IN}t) + B + \Delta) \sum_{n=-\infty}^{\infty} (\delta(t - (2n-1)T_s) + \\ &\quad \delta(t - 2nT_s - \Delta t)) \end{aligned} \tag{5.14}$$

In (5.14), we assume that the two branches have identical gain, A, and offset, B; the timing skew between the two branches is Δt. The different timing skew introduces two imaging tones around $f_S/2$ in the output power spectrum, as shown in Fig. 86. The power of the tones reduces as the skew becomes smaller. In ideal case, when $\Delta T = 0$, the two tones cancels each other and the error introduced by timing skew equals to zero. Again the error here is a result of mismatch.

A frontend S&H circuit is deployed in the time-interleaved ADC and shared by both pipeline ADC branches to minimize the error caused by mismatch. This arrangement is indicated in Fig. 83. Double sampling techniques are applied to this frontend S&H circuit such that the same OpAmp can be re-used for both pipeline

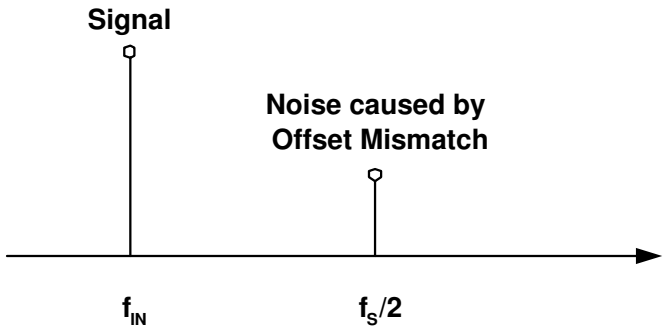

Fig. 85. Spectrum of a 2-branch time-interleaved ADC output with a sinusoidal input and offset mismatch between the branches

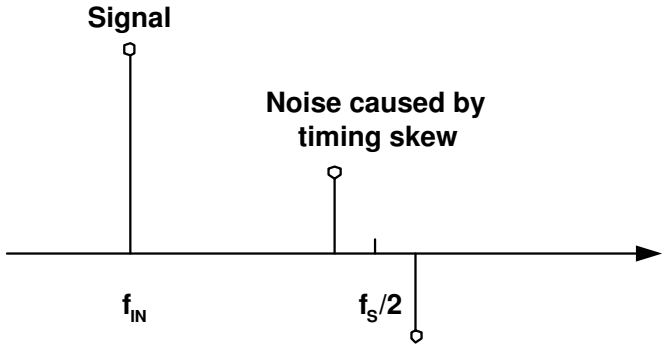

Fig. 86. Spectrum of a 2-branch time-interleaved ADC output with a sinusoidal input and timing skew between the branches

branches. The detail of the doubling sampling mechanism and circuit implementation will be discussed in Chapter VI. By doing that, the switching between sample and hold phases is identical for both branches. Therefore, the timing skew is eliminated. The offset mismatch performance also improves due to the OpAmp re-use. The gain mismatch now only comes from the capacitor mismatch in the S&H. In this ADC design, we rely on careful layout to suppress the gain mismatch. Larger capacitor size is used in the S&H to achieve better matching. An on-line digital calibration scheme is also implemented to further compensate the mismatch errors.

2. Design Requirement for the Frontend S&H Circuit

The frontend S&H circuit improves the immunity to the mismatch between the pipeline ADC branches for the time-interleaved ADC. To guarantee 11-bit overall resolution of the ADC, the absolute error performance in the S&H itself needs to be better than 11-bit. That means the error power of absolute gain error, offset and noise in the S&H should be at least 66 dB lower than the maximum signal strength. The ideal gain in an S&H is 1. Assuming that we have a gain error of $\delta_{GS\&H}$ in the S&H circuit, the maximum error power caused by this gain error occurs when the input signal is at its highest power level. This gives $V_{in} = V_{FS}/2$ and the error voltage caused by gain error is $V_{err} = \delta_{GS\&H}\frac{V_{FS}}{2}$, where V_{FS} is the full scale of the reference voltage of the ADC. To achieve 11-bit resolution, (5.15) needs to be satisfied.

$$\begin{aligned} V_{err} &= \delta_{GS\&H}\frac{V_{FS}}{2} < \frac{LSB_{11bit}}{2} = \frac{V_{FS}}{2^{12}} \\ \delta_{GS\&H} &< \frac{1}{2^{11}} = 0.05\% \end{aligned} \tag{5.15}$$

For the same reason the offset in the S&H circuit, $V_{offS\&H}$ should also be less

than half of the LSB. Since the the full scale of the ADC is $V_{FS} = 2V$, we have

$$V_{offS\&H} < \frac{LSB_{11bit}}{2} = \frac{V_{FS}}{2^{11}} = 2mV \tag{5.16}$$

The SNR of the ADC is 66 dB during the Bluetooth receiving mode. Therefore, the total in band noise power of the ADC should be less than -66 dBc with respect to the full scale input. The input referred noise of the S&H circuit needs to be 6 dB lower than -66 dBc to avoid raising the noise floor in the ADC.

Another critical error source in the ADC is the clock jitter. Clock jitter is the timing uncertainty of the rising and falling edge in the clock signal. It translates to a timing error in the S&H circuit as it switches between sampling phase and holding phase, and introduces a voltage variation. The effect of clock jitter will be seen as a random noise at the output of the ADC [35]. Apparently, the smaller the jitter is, the lower the noise power is. The effect of the clock jitter on the overall ADC SNR can be ignored if analog input varies by less than half of the LSB during jitter induced time deviation of the sampling point. Assuming that the clock has a jitter of Δt and input analog signal is a full scale sin wave $V_{in} = \frac{V_{FS}}{2} sin 2\pi f t$, whose maximum rate of variation is $2\pi f \frac{V_{FS}}{2}$. The voltage error caused by jitter need to satisfy the following condition,

$$\begin{aligned} 2\pi f \frac{V_{FS}}{2} \Delta t &< \frac{LSB_{11bit}}{2} = \frac{V_{FS}}{2^1 2} \\ \Delta t &< \frac{1}{2\pi 2^1 2} = 1.76ps \end{aligned} \tag{5.17}$$

Equation (5.17) is only an estimation for the maximum tolerable jitter in the ADC. However, it still provides us guideline in the clock circuit design.

We have derived gain error, offset, noise and clock jitter specs for the frontend

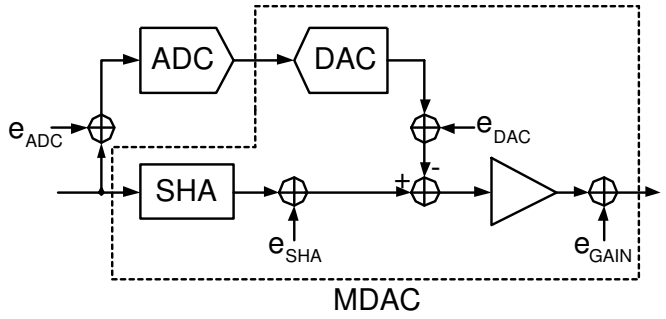

Fig. 87. Error model of a stage in the pipeline ADC

S&H circuit in this sub-section. All these specs are summarized in Table XXIV.

3. Design Challenges in the Pipeline ADC and Requirements for the Sub-Stages

Both the frontend S&H circuit and sub-stages in the pipeline ADC branches introduce errors. Due to the error scaling in the pipeline ADC, the most critical blocks are the S&H and the first 4-bit stage.

Fig. 87 illustrates the error model of a stage in the pipeline ADC branch. Four types of error exist in the model. The non-ideality in the sub-ADC introduces e_{ADC}. It appears as ADC offset and non-linearity. Since we use MDAC in the pipeline stage, e_{DAC}, e_{SHA} and e_{Gain} are all caused by the non-idealities in the MDAC circuit. Among them, the e_{DAC} is the DAC error; e_{SHA} is the S&H error and e_{Gain} is the residue amplifier gain error. Besides the errors included in this error model, in band noise created by the stage circuit should also be considered in design.

The redundant bits between the adjacent sub-stages in the pipeline ADC along with the digital correction relax the maximum tolerable ADC error in each stage. As long as this ADC error, e_{ADC}, is smaller than the half of the LSB in the next stage, its effect is negligible in the overall ADC SNR performance. From this analysis we get

$$G_i e_{ADC} < \frac{LSB_{i+1}}{2} \tag{5.18}$$

Here G_i is the residue gain of current stage and LSB_{i+1} is the LSB of next stage. From (5.18), we get the sub-ADC requirements for the first 3 sub-stages in the pipeline ADC branch are 6-bit. Since no load is seen by the last stage, the sub-ADC in it only needs to provide a resolution of 3-bit. The current analog process is usually good enough to provide better than 6-bit resolution in the sub-ADC with careful circuit design and layout. Therefore, we can consider the sub-ADC in the pipeline branch ideal

As shown in (5.10), the error in current stage of the pipeline ADC gets scaled down by the gain in the previous sub-stages. In other word, each stage needs only to provide a better resolution than the remaining bits after current stage. For instance, in our 11-bit pipeline ADC, the S&H circuit needs to provide a 11-bit resolution, while the first 4-bit stage needs have an accuracy of 8-bit and the second 3-bit stage only needs to provide an 6-bit resolution. This will be the guideline for the analysis of e_{Gain}, e_{DAC}, e_{SHA} and noise.

As long as the maximum error voltage caused by the gain error is smaller than the half of the LSB of the remaining bits, this error will not degrade the overall SNR performance of the ADC. This gives us,

$$\delta_{G_i} \frac{V_{FS}}{2} < \frac{LSB_{rem}}{2} = \frac{V_{FS}}{2^{rem+1}} \tag{5.19}$$

Where δ_{G_i} is the gain error in the current stage, rem is the remaining bits in the pipeline ADC and LSB_{rem} is the LSB of the remaining bits after current stage. From (5.19), we can get the gain error requirements for the first 3 sub-stages are 0.4%, 1.6% and 12.5%. When a MDAC is applied in the pipeline stage, the gain error is

determined by the mismatch in the capacitors. In the ADC design, we used IBM BiCMOS process, which has a good matching performance for capacitors. By careful layout, we can suppress the gain error below the specs.

As MDACs are used in the pipeline sub-stages to perform the function of DAC, S&H, residue detection and amplification, the DAC error, e_{DAC}, and S&H error, e_{SHA}, can be modelled together as DAC non-linearity. Since the non-linearity of the DAC affects the accuracy of the residue before the residue amplification, it will not be attenuated by the gain of the current stage when referred to the input. Therefore, the effect of DAC non-linearity on overall ADC SNR is negligible only if the DAC in each stage has a better linearity than the remaining bits in the pipeline ADC branch including the bits generated by the current stage. That means the DAC in the first 4-bit stage should have a linearity of 11-bit; the second 3-bit stage should have a linearity of 8-bit; and the third 4-bit stage should have a linearity of 3-bit. Current analog process technology is able to provide better than 10-bit linearity. Therefore, after the first 4-bit stage, we can rely on careful circuit design and layout to achieve the required linearity for the rest of the ADC. A digital calibration scheme is applied to improve the linearity if the DAC in the fist 4-bit stage. We will discuss its implementation in Chapter VI.

The same principle can be applied to the input referred noise analysis for each stage. The noise referred to the input of each stage need to provide a 6 dB better SNR required by the remaining bits in the pipeline ADC branch including the bits generated by the current stage. For the 4 sub-stages in the pipeline ADC branch, the in band input referred noise requirements are -72 dBc, -54 dBc, -42 dBc and -24 dBc.

The circuit block requirements for the time-interleaved pipeline ADC are summarized in Table XXIV. The sub-stages in the table is in sequence from MSB to LSB. The offset requirements for the sub-stages are derived from sub-ADC require-

Table XXIV. Circuit block requirements for the time-interleaved pipeline ADC

Specs	Frontend S&H	4-bit	3-bit	4-bit	3-bit
Gain Error (%)	0.05	0.4	1.5	12.5	–
Offset (mV)	2	31	31	31	125
ADC Error (bits)	–	6	6	6	3
DAC linearity (bits)	–	11	8	6	–
Noise (dBc)	-72	-72	-54	-42	-24
Clock jitter (ps)	1.76				

ment with a $V_{FS} = 2V$. Here all the analysis is based on the 11-bit dynamic range or resolution requirement in the Bluetooth receiving mode. The 8-bit 802.11b receiving mode can have more relaxed specs. However, the ADC needs to accommodate both receiving modes. Therefore, we need to shoot for the tougher specs in the circuit design.

F. System Level Modelling and Simulation of the ADC

Although theoretical derivation provides a good explanation and specification for the ADC, system level simulation is still needed to verify the system design. A simulink model was developed for the pipeline ADC. Fig. 88 shows the model. It contains 4 sub-stages. Each sub-stage is a sub-model. The main non-ideality in each sub-stage comes from the MDAC as we have discussed. In the model, we use a matlab function to describe the MDAC. Its parameters include DC gain. slew rate and GBW of the OpAmp, the capacitor ratio and mismatching factor, sampling period. The detailed code of the MDAC is attached in the Appendix C.

Another important block in the pipeline ADC is the S&H circuit. Fig. 89 illustrates the simulink model that is used in the system level verification. In that

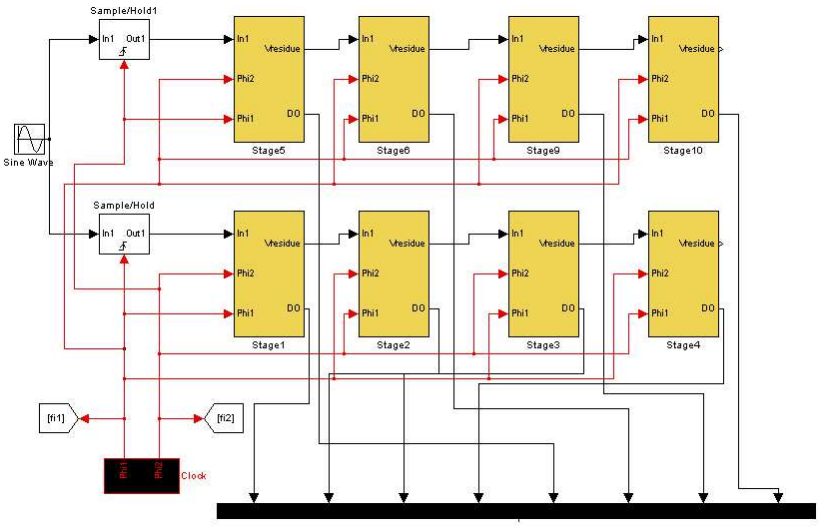

Fig. 88. Simulink model for pipeline ADC system level verification

that model, we include KT/C noise and clock jitter parameters. Those non-ideality sources are highlighted in the Fig. 89 with dotted box.

The purpose of developing these models is to verify the specs we derived for each circuit block. We added those specs as non-ideal parameter in the model to check the ADC system performance. In the matlab simulation, we achieved an SNR of 68 dB and SFDR of 71 dB with the circuit specs included in Table XXIV and Chapter VI.

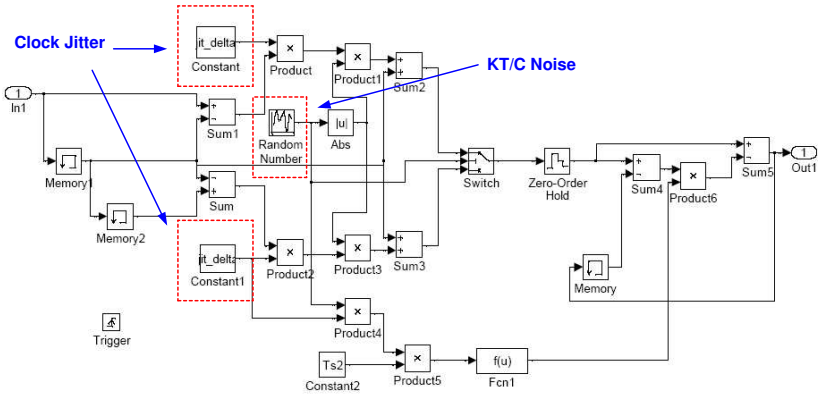

Fig. 89. Simulink model for the S&H circuit

CHAPTER VI

CIRCUIT IMPLEMENTATION AND VERIFICATION FOR THE ADC DESIGN IN THE 802.11B/BLUETOOTH DUAL-MODE RECEIVER

In this chapter, we will discuss the circuit implementation and lab verification of the time-interleaved pipeline ADC. To improve circuit performance, fully-differential architecture is applied to the entire ADC.

A. Sample and Hold Circuit

OpAmps are power consuming parts of the ADC. As we mentioned in Chapter V. OpAmp sharing technique is used in the S&H circuit to reduce the number of OpAmps used in the ADC. The schematic and clock arrangement for the S&H circuit is illustrated in Fig. 90. Two sets of sampling capacitor C_{S1} and C_{S2} are deployed to sample the input data to the two parallel pipeline ADC branches, respectively. When $Clk1$ is high and $Clk2$ is low, the input signal is sampled onto C_{S1}; the output of the S&H reads the voltage from C_{S2} and feeds to the ADC branch 2. When $Clk1$ is low and $Clk2$ is high, the input signal is sampled onto C_{S2}; the output of the S&H reads the voltage from C_{S1} and feeds to the ADC branch 1. In this way, the two pipeline ADC branches get their inputs from independent capacitor sets, however only one OpAmp is employed in the S&H circuit.

1. Specs Derivation

DC gain, Unit-Gain-Frequency (UGF), Slew Rate (SR) and phase margin of the amplifier are among the most important circuit specs for the S&H circuit. The DC gain and UGF define the settling error of the S&H output while UGF and SR decide

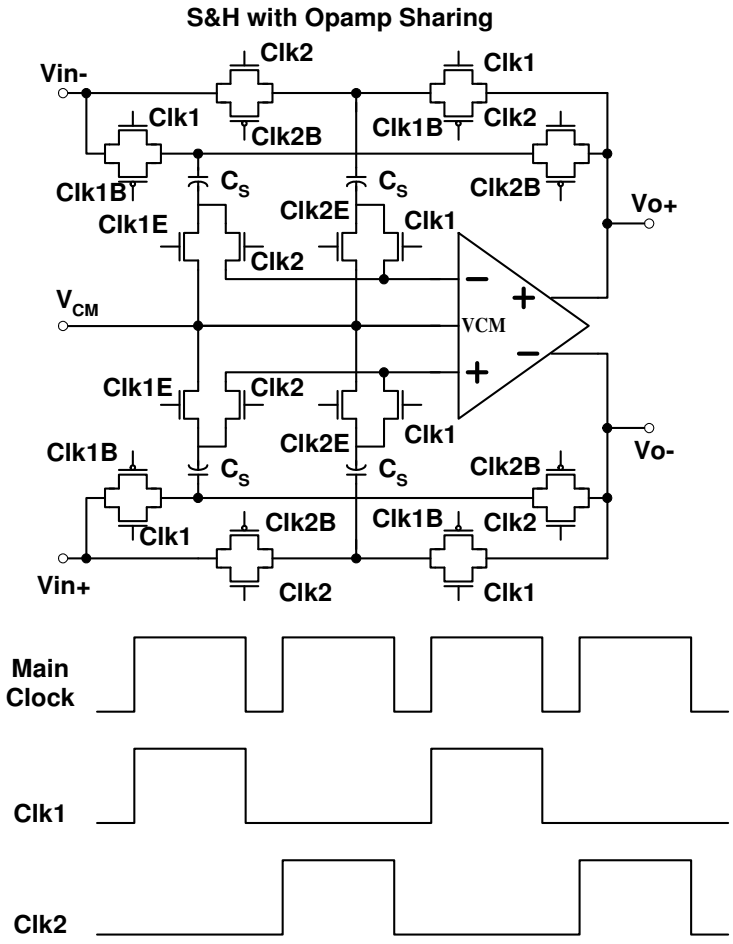

Fig. 90. The schematic and clock arrangement for the S&H circuit

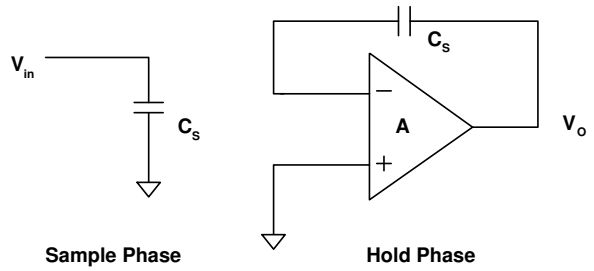

Fig. 91. The schematic of the S&H circuit in different phase

the settling speed of the S&H. The phase margin is important for the stability of the circuit. Before, we start to derive the specs for those circuit parameters, we need to first determine the capacitor size used the in the S&H circuit and the ones involved in the MDAC that follows, since those capacitors are the load seen by the S&H. The capacitor size is chosen as a compromise among matching performance, noise performance, silicon area and power dissipation. The bigger the capacitance are, the better matching and lower noise we can achieve. However, we will pay more in the silicon area and also as the capacitance load increases, the power consumption for the OpAmps go up as well. In our design, we choose $C_{S1} = C_{S2} = 1pF$ to provide low enough kT/C noise and good enough matching in the S&H. The capacitor banks used in the MDACs has a unit capacitance of 200 fF. This gives us a total capacitance of 1.6 pF (3.2 pF differentially) as the load the S& H circuit. We will analyze the MDAC in detail in the next section, we simply use this capacitor value for the specs derivation here.

Fig. 91 illustrates the circuit topology for each branch in the two phases operation of the S&H. For simplicity, we use a single-ended OpAMp in the specs development. In the sample phase, the charge stored on the capacitor becomes,

$$Q_S = C_S \cdot V_{in} \tag{6.1}$$

In the hold phase, given the DC gain of the OpAmp is A, the charge across the capacitor becomes,

$$Q_H = C_S \cdot \left(V_O + \frac{V_O}{A}\right) + C_P \cdot \frac{V_O}{A} \tag{6.2}$$

where C_P is parasitic capacitance seeing at the input of the OpAmp. Since no current charge or discharge happens in the hold phase, Q_H should equal to Q_S, which gives us,

$$\begin{aligned} C_S \cdot V_{in} &= C_S \cdot \left(V_O + \frac{V_O}{A}\right) + C_P \cdot \frac{V_O}{A} \\ V_O &= \frac{C_S \cdot V_{in}}{C_S \cdot \left(1 + \frac{1}{A}\right) + C_P \cdot \frac{1}{A}} \end{aligned} \tag{6.3}$$

C_P usually is much smaller than C_S, (6.3) can be approximated by

$$V_O = \frac{V_{in}}{1 + \frac{1}{A}} \tag{6.4}$$

From (6.4), we can see that the error of the S&H circuit is determined by its amplifier gain. To achieve a resolution of 11-bit, $1 - \frac{1}{1+\frac{1}{A}} = \frac{1}{1+A}$ needs to be less than 0.024%, which leads to a amplifier gain larger than 72.2 dB. To assure stability of the S&H circuit and provide fast settling (no over-shoot in the step response), the phase margin requirement of the OpAmp will be 60° at the unit gain frequency.

Equation (6.4) provide a way to calculate the S&H error in the steady state. Considering the cutoff frequency of the OpAmp is not infinite, the output voltage of the S&H needs to settle to its steady state value. If the OpAmp has a single pole at p, equation (6.4) can be re-write as,

$$V_O = \frac{V_{in}}{1 + \frac{1+\frac{s}{p}}{A_0}} \approx V_{in} \frac{1}{1 + \frac{1}{pA_0}} \tag{6.5}$$

where A_0 is the DC gain of the OpAmp. Notice in (6.5), pA_0 is gain bandwidth product and it also equal to $\omega_u = 2\pi f_u$, where f_u is the unit gain frequency. Applying inverse Laplace transformation to (6.5), we can have the time domain transfer function of V_O as,

$$V_O = V_{in} e^{-\omega_u t} \tag{6.6}$$

Thus, the error due to the settling of the S&H output is

$$error = 1 - e^{-\omega_u t} \tag{6.7}$$

where t is the required settling time. The S&H is operating at a frequency of 44 MHz. This settling error of the S&H should be lower than half of the LSB within the holding period. To guarantee the sub-ADC and MDAC in the first stage has enough time to sample the S&H output, we decide the settling time t to be 4ns, which gives a f_u requirement for the OpAmp larger than 330 MHz. For an OpAmp, $f_u = \frac{g_m}{C_L}$, where C_L is the load to the OpAmp. The load of the S&H is the capacitor bank of the MDAC, which is 1.6 pF. Thus, we can obtain the g_m requirement for the OpAmp from the f_u specs and design the input differential pair accordingly.

The OpAmp slew rate also affects the settling of the S&H output. The maximum slew rate required is related to the maximum swing of the output voltage and settling time. If we still require a settling time of $t = 4ns$, given a $V_{pp} = 2V$ swing at the output, the required SR is

$$SR = \frac{V_{pp}}{t} = 500V/\mu s \tag{6.8}$$

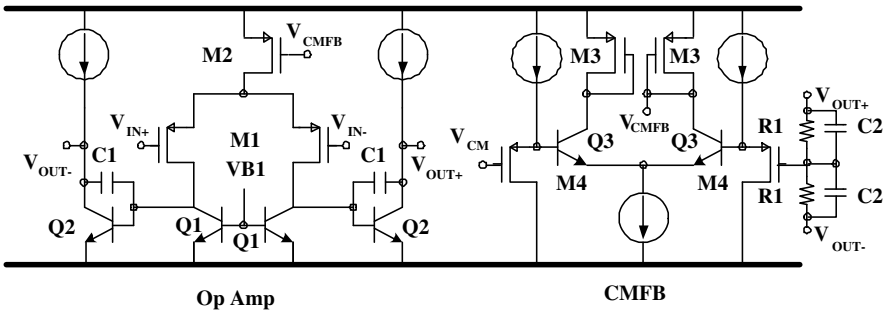

Fig. 92. The schematic of the OpAmp used in S&H and MDACs

In the OpAmp design, $SR = \frac{I_O}{C_L}$, where I_O is the current driving out from the output stage of the OpAmp. Knowing $C_L = 1.6pF$, we can calculate the current drive capability required for the OpAmp.

2. Circuit Implementation

Now we have derived major specs for the S&H OpAmp. Those specs are summarized in Table XXVI. As we have discovered, the S&H OpAmp requires high gain, large swing, large current driving capability and fast settling at the output. Single stage OpAmp usually cannot provide large enough gain and swing. Compensation in the multi-stage (more than 2 stages) OpAmps slows down the OpAmps. Therefore, 2-stage OpAmp is the best choice for the S&H circuit design. Fig. 92 shows the OpAmp schematic along with its common mode feedback circuit.

In the 2-stage OpAmp, the input differential pair is implemented with PMOS transistor to achieve better noise performance in comparison with the NMOS transistor. Bipolar transistors are not suitable for input pair because the current leakage through the base of the transistors can discharge the sampling capacitor and introduce errors. The size of the input differential pair and its tail current is decided by the UGF specs. Bipolar current sources are used as the load of the differential pair.

In the IBM 0.25 μm BiCMOS process, for the same current, the bipolar transistor demonstrates higher output impedance than the CMOS transistors do. Using bipolar transistor as the load can improve the gain of the first stage. Even more important, the small parasitic capacitance of the bipolar transistor helps to push the second non-dominant pole at node VB1 to high frequency and improves AC response of the OpAmp. In the second stage, the high g_m and r_O of the bipolar transistor provides significant gain boost for the OpAmp. In the S&H OpAmp circuit, the SR is limited by the charging of capacitive load at the output. The SR specs determines the current needed in the output stage.

In detail, we first determine the bias current needed for the first and second stage based on the slew rate requirement. Hence, we have

$$I_1 > C_C \cdot SR \tag{6.9}$$

$$I_2 > C_L \cdot SR \tag{6.10}$$

where $I-1$ and I_2 are the tail current of the differential pair and the DC bias current of the output stage; C_C and C_L are the values of the compensation capacitor and load capacitor, respectively, SR is the slew rate specs for the S&H OmAmp. To guarantee the OpAmp DC gain and speed, we need to have

$$\frac{g_{m1}}{C_C} > GBW \tag{6.11}$$

$$\frac{R_{o2}}{C_L} > 4 \cdot GBW \tag{6.12}$$

$$g_{m1}R_{o1}g_{m2}R_{o2} > A_o \tag{6.13}$$

where g_{m1}, R_{o1}, g_{m2} and R_{o2} are the transconductance and output impedance of the first and second stages, respectively. With this equations, we can obtain the

Table XXV. The circuit design parameters of the S&H OpAmp

M1	$96\mu m/0.24\mu m$	M2	$20\mu m/0.24\mu m$
M3	$20\mu m/0.24\mu m$	M4	$20\mu m/0.24\mu m$
Q1	$0.8\mu m$	Q2	$6\mu m/0.6\mu m$
Q3	$1.2\mu m$	R1	$100k\Omega$
C1	$1.6pF$	C2	$0.5pF$

transistor size for the S&H OpAmp.

Two identical resistors are connected in serial between the two output node as a common mode voltage detector. Unfortunately, those resistors also load the OpAmp and lower its output impedance. To avoid degrading the gain of the OpAmp too much, those resistors have to be large, 100 $k\Omega$ in our case. This creates an high impedance node in the common mode feedback loop. In order to assure the stability of the CMFB loop, 2 capacitors are connected in parallel with the resistors to reduce the node impedance at higher frequency. We want to use bipolar transistors in the CMFB circuit to achieve a high gain and good frequency response. However, the base current leakage of the bipolar transistors is not desired in the CMFB. Therefore, we place a paire of PMOS source followers before the CMFB amplifier bipolar input pair. In this way, we are able to enjoy the large gain provided by the bipolar transistor without suffering from its current leakage. Table XXV summarizes the circuit design parameters of the S&H OpAmp.

3. Simulation Results

The S&H circuit is simulated in the Cadence by Spectre. The S&H OpAmp is first examined for its frequency response. Fig. 93 shows the OpAmp output AC magnitude and phase. In the simulation, we obtained a DC gain of 85.8 dB, UGF of 420 MHz

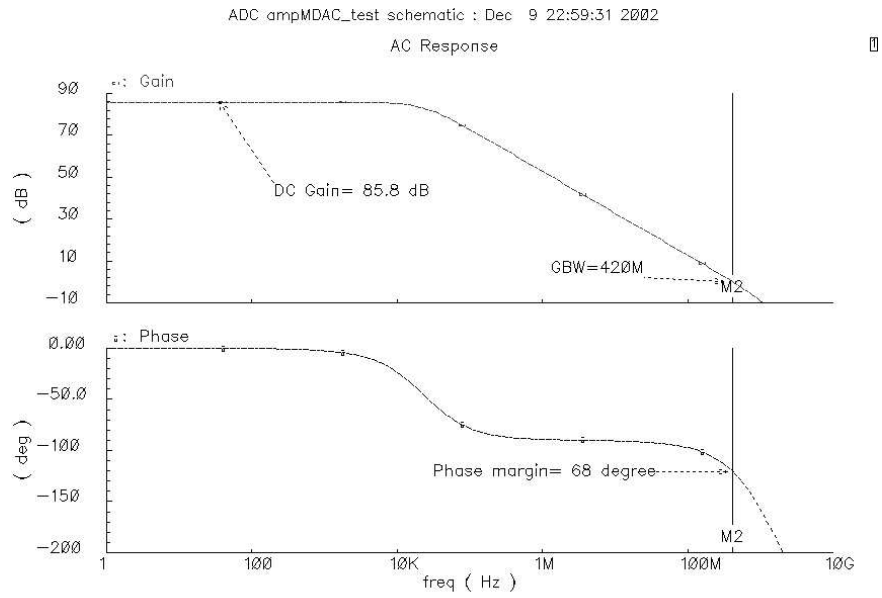

Fig. 93. The AC response of the S&H OpAmp

and phase margin of 68 degree. All specs are met as shown in Table XXVI. We also check the settling behavior of the S&H circuit by applying a 6 MHz, 2 V peak-peak sinusoidal signal to the S&H input. As depicted in Fig. 94, the output tracks the input correctly and the S&H settles much faster than the required 4 ns. Finally, the linearity of the S&H circuit is also tested by applying FFT to the S&H output. A SFDR of 68.3 dB is achieved, as illustrated in Fig. 95.

B. MDACs

The MDACs in the pipeline ADC branches use charge re-distribution techniques to perform the function of S&H, residue detector and amplifier in each sub-ADC stage. Fig. 96 shows the operating modes of the MDACs.

The MDAC is formed by MDAC OpAmp and a capacitor bank. To achieve better linearity the capacitor bank uses thermometer control code, and therefore

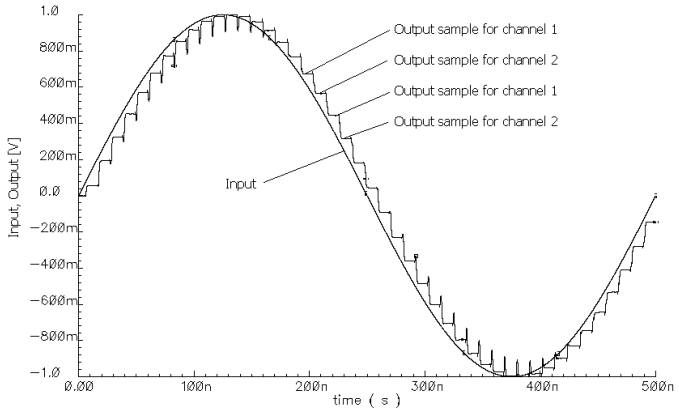

Fig. 94. The settling of the S&H circuit

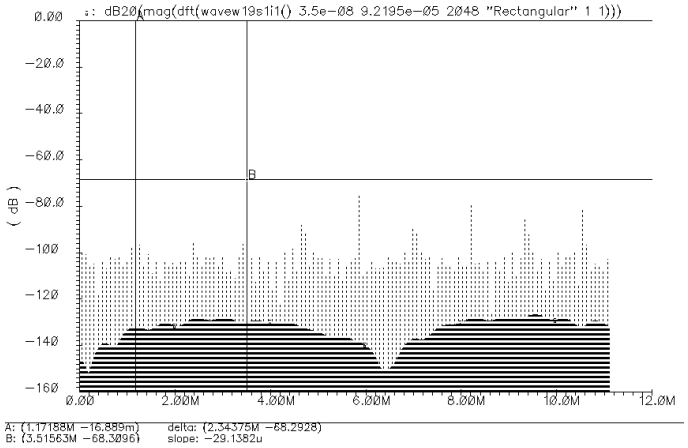

Fig. 95. The linearity of the S&H circuit

Table XXVI. The summary of specs and simulated results for the S&H OpAmp

	Specs	Simulated Results
DC Gain	72.2 dB	85.8 MHz
Unite Gain Frequency	330 MHz	420 MHz
Phase Margin	60 degree	68 degree
Slew Rate	500V/μs	723V/μs
Linearity	66 dB	68.3 dB
Supply Voltage	2.5 V	2.5 V
Power Consumption	Min	1.2 mA

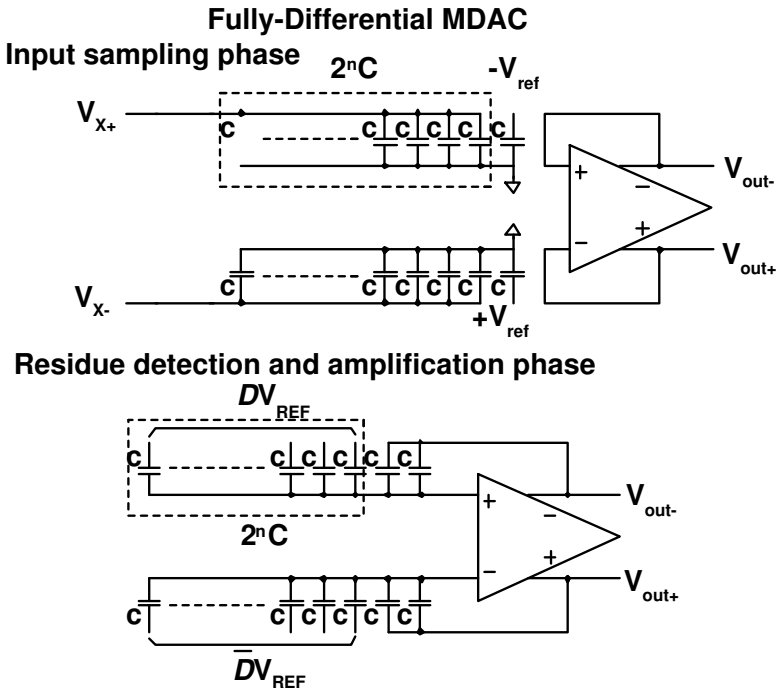

Fig. 96. The schematic and operating modes of the MDACs

consists $2^n + 1$ unit capacitors, where n is the number of bit in the MDAC. For a 3-bit MDAC, its capacitor bank has 9 unit capacitors and a 4-bit MDAC has 17 unit capacitors. Considering both area and matching performance, a unit capacitance, C_u of 200 fF is chosen. Also, the 200 fF unit capacitance brings down the kT/C noise below the quantization noise floor [68]. Thus, the total capacitance in a 3-bit MDAC capacitor bank is 1.8 pF and a 4-bit MDAC capacitor bank has a capacitance of 3.4 pF.

During the input sampling phase, the input voltage is sampled on to 2^n capacitors. The one capacitor left is connected to the reference, V_{ref}. The reason that we connect the last capacitor to the V_{ref} is to create a half LSB shift in the residue, as we will see in the derivation later. That half LSB shift is needed in the pipeline structure [59]. The charge on the capacitors in this phase is

$$Q_S = V_{in} \cdot 2^n C_u - V_{ref} C_u \tag{6.14}$$

During the residue detection and amplification phase, all the capacitors in the MDAC capacitor bank except for 2 is connected to the reference voltage $\pm V_{ref}$ depending on the output of the sub-ADC. The other 2 capacitor is connected across the MDAC OpAmp. Assuming the sub-ADC output is $D = [d_{N-1}, ..., d_0], N = 2^n$ in form of the thermometer code and the OpAmp gain is A, we have

$$Q_D = \left(V_{out} + \frac{V_{out}}{A}\right) \cdot 2C_u + \left(V_{ref} d_{N-1} - \frac{V_{out}}{A}\right) \cdot C_u + ... + \left(V_{ref} d_0 - \frac{V_{out}}{A}\right) \cdot C_u \tag{6.15}$$

Here we ignore the parasitic capacitance because comparing to the capacitance in the MDAC capacitor bank, the parasitic capacitance are negligible. Since no current goes in or out the capacitor bank during the sampling and residue detection amplification

phase, the charge in the two equation (6.14) and (6.15) should be equal.

$$\begin{aligned} Q_D &= Q_S \\ V_{out} &= 2^{n-1}\Big(V_{in} - \frac{V_{ref}}{2^n+1} - V_{ref}\cdot\frac{D}{2^n}\Big)\Big(\frac{1}{1+\frac{2^n+1}{2A}}\Big) \end{aligned} \tag{6.16}$$

In ideal case, the OpAmp gain is infinity, this leads to

$$V_{out} = 2^{n-1}\Big(V_{in} - \frac{V_{ref}}{2^n+1} - V_{ref}\cdot\frac{D}{2^n}\Big) \tag{6.17}$$

Equation (6.17) shows that the MDAC output provide an amplified residue with a gain of 2^{n-1} for the next stage.

With finite gain in the OpAmp, the output will have error. Comparing (6.17) and (6.16), we can see the error term is

$$error = 1 - \Big(\frac{1}{1+\frac{2^n+1}{2A}}\Big) \approx \frac{2^{n-1}}{A} \tag{6.18}$$

This error will appear as gain error for the pipeline. To suppress it under the half of the LSB of the current stage, we will require A to be big. The first stage MDAC OpAmp needs to have more than 60 dB gain to provide a sufficiently small gain error. The phase margin for the MDAC OpAmp however should be checked not at the unit gain frequency but the close loop gain frequency. The close loop gain is equal to $\frac{1}{\beta}$, where β is the feedback factor that is given by (6.19), which is $\frac{2}{17}$ for the 4-bit MDAC and $\frac{2}{9}$ for the 3-bit MDAC. To guarantee the stability and avoid over-shoot at the output of the MDAC, the phase margin needs to be higher than 70 degree.

$$\beta = \frac{2C_u}{(2^n+1)C_u} \tag{6.19}$$

The UGF of the OpAmp also affects the performance of the MDAC. We can use

Table XXVII. The summary of specs for the MDAC OpAmp

	Specs (4-bit)	Specs (3-bit)
DC Gain	60 dB	48 MHz
Unite Gain Frequency	384 MHz	174 MHz
Phase Margin	70 degree	70 degree
Slew Rate	500V/μs	723V/μs
Supply Voltage	2.5 V	2.5 V
Power Consumption	0.8mA	0.6 mA

the single pole approximation to model the MDAC OpAmp. If the pole is at p, the settling error of the MDAC can be written as

$$error = 1 - e^{-pt} \tag{6.20}$$

With a feedback factor of β, we have

$$p = 2\pi f_u \cdot \beta \tag{6.21}$$

wheref_u is the unit gain frequency. Combining (6.20) and (6.21), if we want the MDAC output to settle within 4 ns to an error less than half of the LSB, we get the UGF specs for the MDAC OpAmp, which is 384 MHz for the 4-bit MDAC and 174 MHz for the 3-bit MDAC. /par

Now we have derived major specs for the MDAC as summarized in Table XXVII. Since the S&H OpAmp meets all the specs here, we re-used it in the MDAC circuit implementation. The only change we made is to scale down the current in the 3-bit MDAC OpAmp to save power.

The MDAC circuits are simulated in the Cadence design environment. Fig. 97

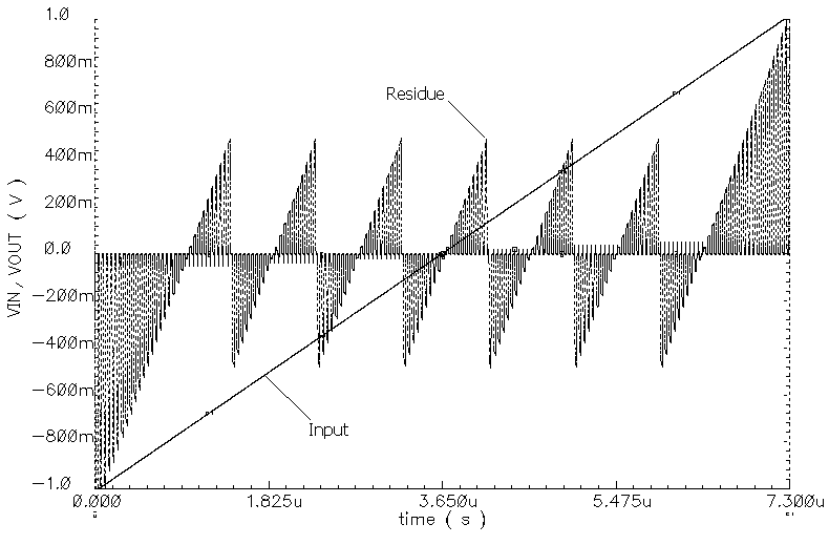

Fig. 97. The residue waveform of the 3-bit MDAC

and Fig. 98 show the residue waveform of the 3-bit and 4-bit MDAC, respectively.

C. Sub-ADCs

The pipeline stages consist of 3-bit and 4-bit sub-ADCs. The 3-bit sub-ADC employs a flash architecture. The 4-bit ADC adopts 2X flash interpolation structure to reduce the number of the preamps and corresponding power consumption. Resistor ladders are deployed to generate the reference voltages that is needed in the sub-ADcs.

The schematic of the 3-bit and 4-bit sub-ADCs are shown in Fig. 99. The sub-ADC is formed by input sampling section, preamps and comparators. The difference between the 3-bit flash sub-ADC and the 4-bit 2X flash interpolation sub-ADC is that the 4-bit sub-ADC has an extra comparator inserted between the adjacent preamps. Preamps are used in the sub-ADC to amplify the difference between the input signal and reference voltage to improve the sensitivity of the comparators. It also provides isolation to the kick back noise from the comparator follows. Furthermore, the offset

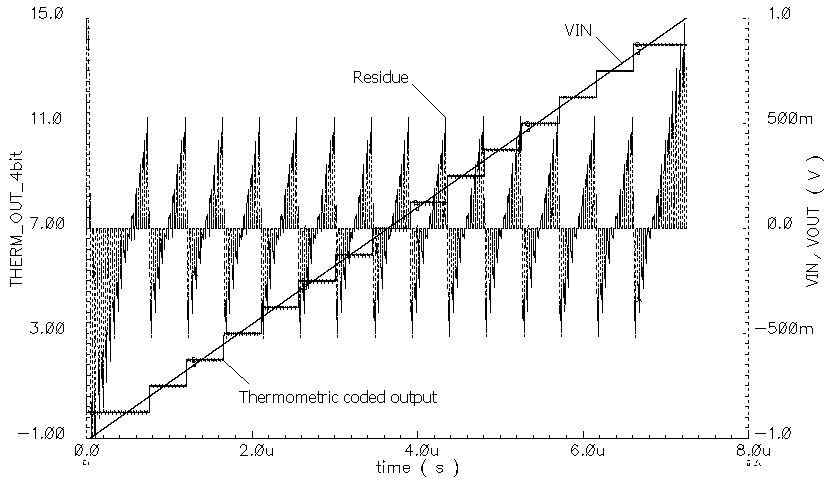

Fig. 98. The residue waveform of the 4-bit MDAC

of the comparator gets to be divided by the gain of the preamp and hence the sub-ADC is less sensitive to the comparator offset. This makes the comparator easier to design. The sampling timing arrangement at the input of the preamps is designed to avoid loading the previous stage. In each sampling cycle, Clk_{2e} is turned to high first to connect the bottom plates of capacitor $C0$ and $C1$ to the common mode voltage (virtual ground). The input referred offset of the preamp, V_{off}, is sampled to $C1$ as Clk_3 turns high. Meanwhile the reference voltage, V_{Ri}, where i is the i^th reference voltage node of the sub-ADC, is sampled onto a separated capacitor $C0$. Then, the input voltage (the output voltage from the previous stage), V_X, is connected to the capacitors and resulting a voltage of $V_X - V_{Ri} - V_{off}$ at the input of the preamps. This action causes a shift in the voltage at the input of the preamp but does not involve any current flow into the input capacitors since there is no current path for the capacitors in the input sampling phase. In this way, the sub-ADCs do not represent as a load to the previous stage. It should be noted that except for the first time the input capacitors are charged to the reference voltage, the reference sampling action is just

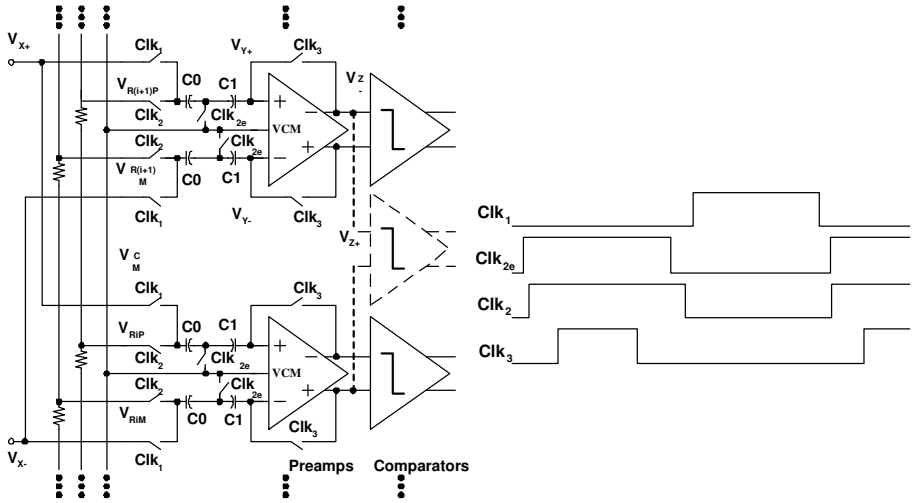

Fig. 99. The schematic of sub-ADCs

to compensate for possible charge leakage and does not involved a significant current flow as well. Smaller load resulted from this innovation allows us to relax the specs of the amplifiers used in the S& H and MDACs circuits.

Fig. 100 shows the schematic of the preamp. NMOS transistors are preferred for the input of the preamp instead of bipolars to avoid the discharge of the input capacitors. To minimize the offset of the preamps their input transistors are biased in the weak inversion region. The same preamp circuit is re-used in both of the 4-bit and 3-bit sub-ADCs. The gain of the preamp is determined by the 4-bit 2X flash interpolation sub-ADC. To avoid the dead-zone in the interpolation structure, where the transition slope of the preamp is narrower than the steps in the sub-ADC, the gain of the preamp is decided to be less than 8 [35]. The transistor sizes used in the preamp are $MP = 1.2\mu m/0.3\mu m$ and $MN = 3\mu m/0.24\mu m$. In the simulation the preamp exhibits a gain of 5 and consumes 0.03 mA current. Fig. 101 shows the preamp output voltage waveform at different reference nodes. As we can see the linear slop of the preamps at each reference voltage node overlaps to avoid dead-zone

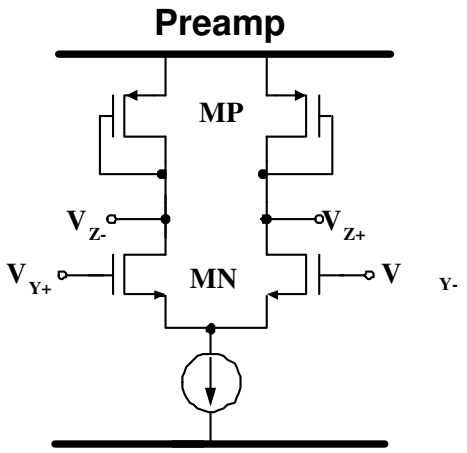

Fig. 100. The schematic of the preamps in the sub-ADCs

in the flash interpolation sub-ADC.

The pipeline ADC branches work at a frequency of 22MHz. In the operation of each stage, the quantization in the sub-ADC needs to be performed at twice of that frequency to leave time for the MDAC to detect and amplify the residue. Therefore, the sub-ADCs operate at 44MHz, which is 22.7ns in time. Half of it has assigned to the sampling at the input of the preamp, hence the comparator needs to finish the digitalization within 11ns. In the circuit design, we set the speed requirement for the comparator to be 5ns. As we discussed before, the offset requirement of comparator is relaxed by the preamp gain. However, in the comparator design, we designed for the 0 dB preamp gain, which gives us a offset specs less than 1 mV.

Fig. 102 illustrates the schematic of the comparator. It can be divided into 3 portion, the input stage, the regenerative comparator and a S-R latch. The input stage of the comparator further amplifies the input signal and isolate the kick back noise. The regenerative comparator is chosen for its fast and reliable overdrive (from full sale input) recovery. The S-R latch is used to safely hold the digital decision through the latch signal. For the comparator, bipolar transistors can be employed in

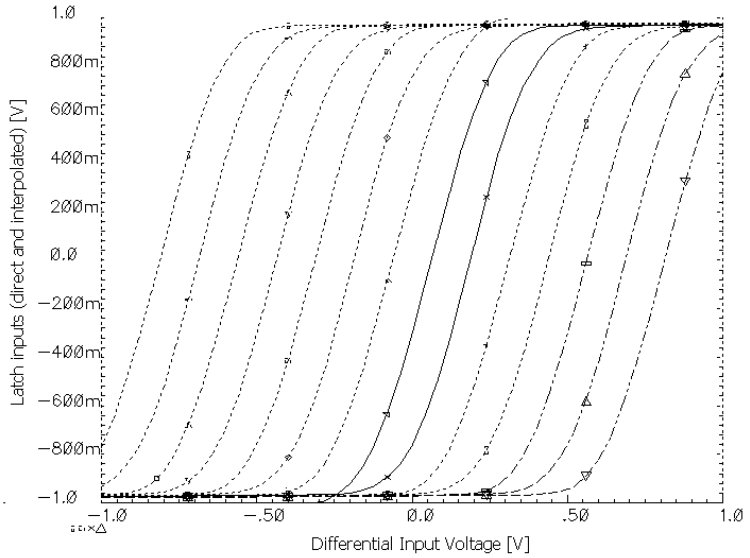

Fig. 101. The simulated preamp output waveform at different reference nodes

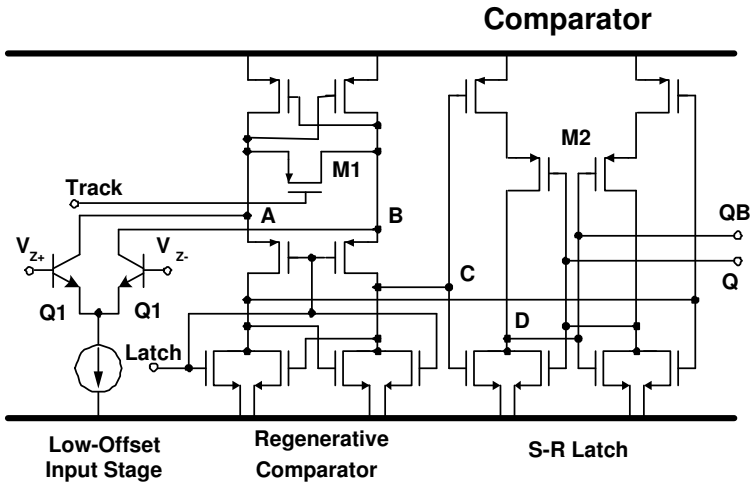

Fig. 102. The schematic of the comparator in the sub-ADCs

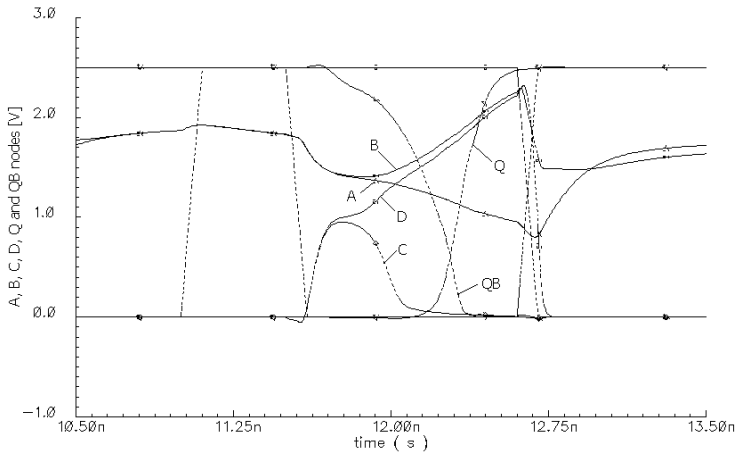

Fig. 103. The output and internal node waveform of the comparator

the input stage since their base current is provided by the preamp without altering the voltage to be compared. To use bipolars for the comparator has a number of advantages; there are low offset, better kick-back noise isolation and high speed with very-low bias current. The bipolar transistors used in the input stage has an emitter length of $2.5\mu m$. At the regenerative comparator stage, all the transistors have the same size, which is $M1 = 0.3\mu m/0.24\mu m$. The same transistors $M2 = 0.6\mu m/0.24\mu m$ are used in the S-R latch. Fig. 103 shows the simulation result for the comparator. Waveform A, B, C and D show the voltage transition at the internal nodes of the comparator. The simulation indicates that the comparator is able to resolve a $400\mu V$ input within 1.5ns. The input referred offset measured for the comparator is $34\mu V$. When standby, the comparator dissipates 0.025mA quiescent current. Table XXVIII summarizes the specs and simulation results for the sub-ADC

D. Digital Calibration and Correction

In the configurable time-interleaved pipeline ADC, an on-line digital calibration scheme is applied to cancel the non-linearity of the MDAC in the first stage and reduce er-

Table XXVIII. The summary of specs and simulated results for the sub-ADC circuit

	Specs	Simulated Results
Preamp Gain	3-8 (V/V)	5 (V/V)
Preamp Offset	<1 mV	94 μV
Preamp Power	Min	0.03 mA
Comparator Settling time	<5 nS	1.5 nS
Comparator offset	<1 mV	34 μV
Comparator Power	Min	0.025 mA

rors caused by mismatch. Logic and delay circuit also used to implement the digital correction mechanism of the pipeline ADC branches.

1. Digital Calibration

As we have discussed in the previous chapter, the MDAC in the first 4-bit stage need to provide a linearity of 11-bit to maintain the overall ADC performance in the Bluetooth receiving mode. The linearity of the MDAC is limited to about 10 to 12 bits by component matching. Although thermometer code is applied in the MDAC capacitor array to improve DNL in the circuit implementation, it is still risky to rely only on careful layout to achieve the 11-bit linearity. Both analog [69] and digital [70] [71] calibration techniques have been introduced before to reduce the effect of DAC errors. The pure digital techniques are usually preferred since almost no additional analog hardware is needed. Furthermore, the speed of the ADC will not be sacrificed because of the calibration. Based on the already reported digital calibration scheme, we extend it to an on-line calibration scheme. With this improvement, we can use this scheme to compensate the mismatch between parallel pipeline branches and the mismatch between I and Q channels in the receiver as well.

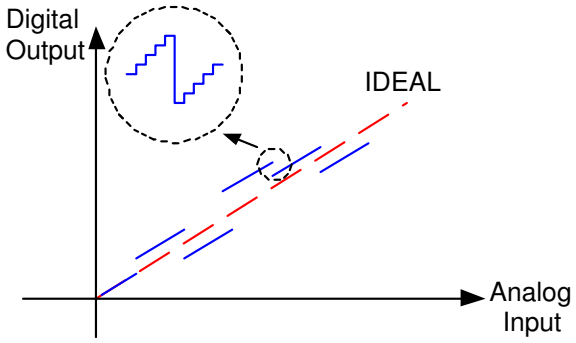

Fig. 104. Non-linearity of the ADC

To describe the implementation of this on-line digital calibration mechanism, we will briefly introduce the principle of the conventional digital calibration [59] technique.

As we have discussed in the previous chapter, the first 4-bit stage relaxes the requirement for the lower bits sub-stages in the pipeline ADC branch. It is reasonable to assume that except for the errors in the first stage MDAC, all the following stages in the pipeline are error-free. Therefore, the non-linearity error only occurs when the output of the first stage MDAC changes. Fig. 104 illustrates this non-linearity in ADC output. The segment for the same first stage output is linear and the displacements only happen when the output of the first stage changes. The displacements caused by the MDAC non-linearities can be corrected in the digital domain if we know their sizes. For our 11-bit pipeline setup, the residue gain factor of the first stage is 8 and the remaining stages of the pipeline has a total resolution of 8 bits. Ideally, with a fixed analog input, we can see that the first stage residue will decrease by $V_{FS}/2$ as increasing the MDAC digital input by 1 bit, where V_{FS} is the full scale reference voltage of the ADC. This corresponds to a change of 2^7 in the 8-bit converter output of the following stages. However, the non-linearity in the MDAC will cause the output of the 8-bit following stage changes to some other value Y(k), where k is the input

code to the first stage MDAC or the output of the first stage sub-ADC output. The error $\delta(k) = Y(k-1) - Y(k) - 2^7$ causes the displacement happens in the total ADC transfer function. The shift size when the first stage digital output is k equals $CORR(k) = \sum_{i=1}^{k} \delta(k)$. Now we have the estimate of the size of the shift caused by the first stage MDAC non-linearity. We can compensate it by adding it back, as illustrated in Fig 105. The $CORR(k)$ only corresponds to the error when the first stage output bits are k. Therefore, we need to sweep through all the combination of the first stage output to get the individual error code for each of them. Those error codes can be stored in memory and used to correct the ADC output with respective to MSBs generated in the first stage. The calibration process can be described as following.

1. Turn the input of the first stage MDAC to calibrate and force it input bits to be 0. Apply an input offset such that the output ends up in the upper part of the range. Measure the digital output code from the following stages.

2. Change the input bits to the first stage MDAC to 1. Measure the corresponding digital output of the following stage and calculate the difference from the previous measurement. This gives us the error $\delta(1) = Y(1) - Y(0) - 2^7$

3. Repeat the above procedure when changing the code from 1 to 15. This gives $\delta(k)$ for each output of the first stage.

4. Assume $\delta(0) = 0$ and calculate $CORR(k)$ by using $CORR(k) = \sum_{i=1}^{k} \delta(k)$. Store the correction codes in a memory

In this way DAC errors and linear gain errors in the first stage MDAC can be corrected.

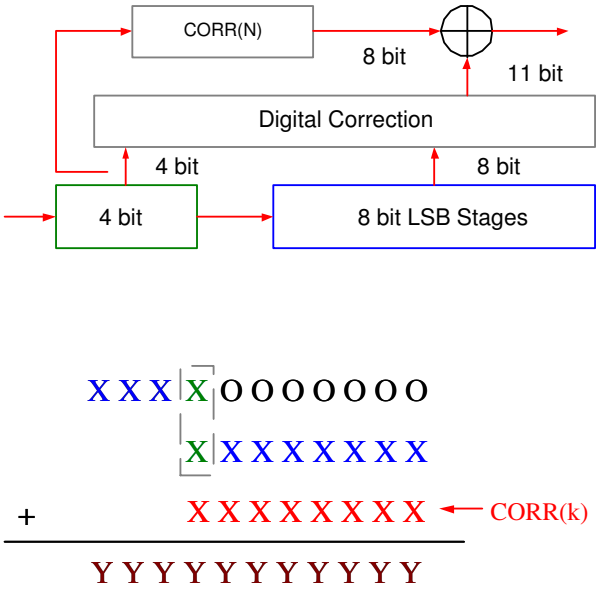

Fig. 105. Digital calibration in the pipeline ADC

2. On-line Digital Calibration Scheme

The digital calibration scheme presented in the previous subsection is able to correct the non-linearity in the pipeline ADC. However, it must be performed off-line. This may not be desired in a lot of real-time system applications, such as in the wireless receivers. The real-time response requirement in the receiver demands minimum down time of the ADC. To tackle this problem, we propose a modification of the existing digital calibration scheme to extend it to on-line calibration.

In order to do that, an identical pipeline ADC branch is introduced. Considering that each of the I and Q channel need an ADC, which consists of 2 parallel pipeline branches, there are in total 5 pipeline branches in the ADC, as illustrated in Fig. 106. The first stage MDACs are calibrated one by one in rotation. The same digital calibration mechanism as introduced in previous subsection is applied with respect to the lower bits stage in the additional pipeline ADC branch. The first stage of the extra branch substitutes and functions as the stage in calibration. Thus, there

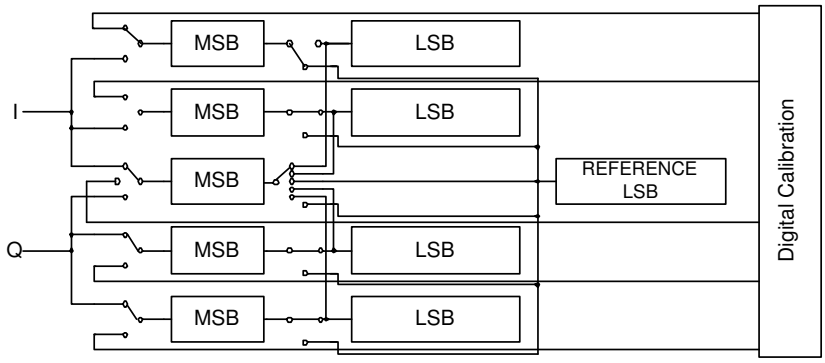

Fig. 106. The proposed on-line digital calibration structure

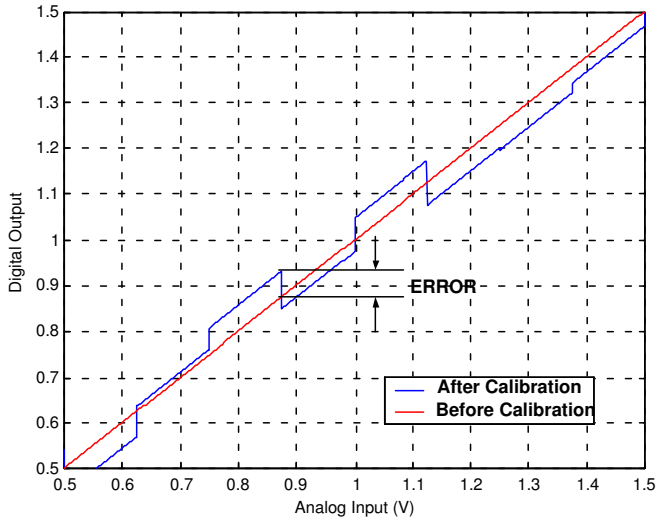

Fig. 107. Simulated ADC output before and after the calibration

are always 4 pipeline ADC branches operating in the receiver and the calibration is transparent to the circuit outside the ADC. All the first stage MDACs are calibrated using the same lower bits stages in the extra pipeline branch, hence their performance becomes identical. This helps to compensate the offset mismatch among the branches. System wise, the I/Q mismatch can also be alleviated through this scheme. Since the calibration can be conducted at a much lower frequency, once every msec in our case, the overhead in power consumption is insignificant. The silicon area overhead of the on-line digital calibration scheme is around 20% since all the 5 ADC branches are identical.

We simulate the on-line digital calibration scheme in matlab. First, we intensionally added some non-linearity in the first stage MDAC of the pipeline ADC branches. The resulted output of the ADC has error as the MSBs changes. After turn on the calibration process, the output curve is moved back to ideal straight line. The non-linearity of the first stage MDAC is therefore compensated. Fig. 107 shows the ADC output before and after the calibration with added-on non-linearity in the first stage MDAC.

3. Thermometer Code to Binary Decoder

The sub-ADC in the pipeline generates thermometer code output. It needs to be converted into binary digits. One problem need to solve in the conversion is the possible sparkles in the thermometer code. The sparkles are referred to as the missing code in the thermometer code due to the fast changing input and timing mismatch among the comparators in the flash ADC. If we convert the thermometer code directly to the binary digits, the sparkles could cause big error. Usually, an intermediate stage is placed to reduce this error. We first convert the thermometer code to Gray code and then convert the Gray code to binary digits.

Since 3-bit and 4-bit sub-ADC is involved in the pipeline branch, we need to design thermometer-Gray-binary decoder for each case. The logic we used in the decoder is list below. In those equations, $T_i(i = 1, ..., 7 \quad or \quad 15)$ stands for thermometer code; $G_i(i = 1, ..., 3 \quad or \quad 4)$ is Gray code and $B_i(i = 1, ..., 3 \quad or \quad 4)$ is binary code, where B_1 is the least significant bit.

1. 3-bit thermometer code to Gray code decoder

$$\begin{aligned} G_1 &= \overline{(T_1\overline{T_3})(T_5\overline{T_7})} \\ G_2 &= \overline{\overline{T_2} + T_6} \\ G_3 &= T_4 \end{aligned} \tag{6.22}$$

2. 3-bit Gray code to binary decoder

$$\begin{aligned} B_3 &= G_3 \\ B_2 &= G_2 \oplus G_3 \\ B_1 &= G_1 \oplus G_2 \oplus G_3 \end{aligned} \tag{6.23}$$

3. 4-bit thermometer code to Gray code decoder

$$\begin{aligned} G_1 &= \overline{(T_1\overline{T_3})(T_5\overline{T_7})(T_9\overline{T_{11}})(T_{13}\overline{T_{15}})} \\ G_2 &= \overline{(T_2\overline{T_6})(T_{10}\overline{T_{14}})} \\ G_3 &= \overline{\overline{T_4} + T_{12}} \\ G_4 &= T_8 \end{aligned} \tag{6.24}$$

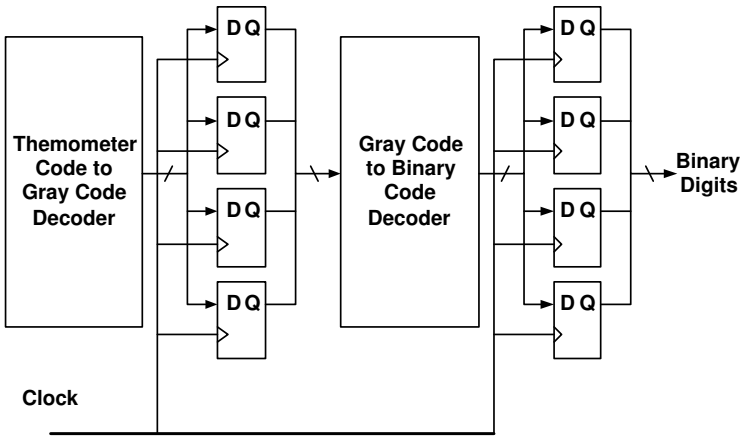

Fig. 108. Schematic of the thermometer code to binary decoder

4. 4-bit Gray code to binary decoder

$$\begin{aligned} B_4 &= G_4 \\ B_3 &= G_4 \oplus G_3 \\ B_2 &= G_4 \oplus G_3 \oplus G_2 \\ B_1 &= G_4 \oplus G_3 \oplus G_2 \oplus G_1 \end{aligned} \tag{6.25}$$

Fig. 108 shows the schematic of the decoder. The 2 D flip-flop is added at the output of the thermometer code to Gray code decoder and the output of the Gray code to binary decoder to synchronize the decoder output.

E. Low Jitter Clock Re-Generation Circuit

From the analysis in the previous chapter, we reached a conclusion that the clock jitter needs to be less than 1.76 ps. Although in the lab, we can find signal generators that provide low jitter clock for our measurement, it will be too expensive to have such a low jitter clock source on a wireless receiver chip. The jitter of a clock signal can be estimated by

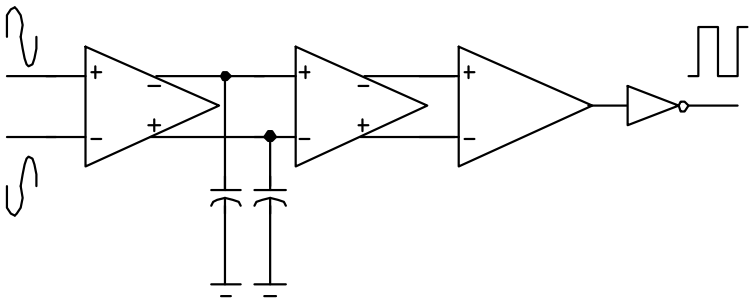

Fig. 109. The schematic of the clock re-generation circuit

$$\Delta t = \frac{V_n}{\Delta} \tag{6.26}$$

where V_n is the total in band noise voltage of the clock signal, and the Δ is the slope of the rising or falling edge of the clock. This is a pessimistic estimation since jitter is not the only components of the noise in the clock signal. However, equation (6.26) suggests ways to reduce the clock jitter. Firstly, clock jitter is proportional to the noise of the clock signal. We can have low jitter clock signal by using low noise clock. Secondly, by increasing the slope of the rising and falling edge of the clock, we can suppress the clock jitter. Usually, the clock circuit in a wireless receiver cannot meet the low noise requirement to assure a clock jitter less than 1.76 ps. On-chip clock re-generation circuit is needed for the ADC. The clock re-generation circuit utilizes the second observation we conclude from (6.26). It creates fast switching edge for the clock signal to suppress jitter.

One way to increase the slope of the rising and falling edge of the clock signal is to amplify the signal. The clock re-generation circuit that we designed for time-interleaved pipeline ADC has 3 amplification stages as shown in Fig. 109. The frequency response of the 3 amplifiers are illustrated in Fig. 110. We can choose to have either square or sinusoidal signal as the input. The sine wave input is preferred

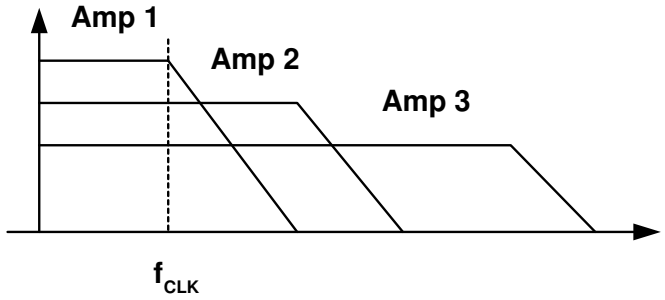

Fig. 110. Frequency response of the three amplifiers in the clock re-generation circuit

since it will have a tone at a single frequency and introduces minimum interference to the rest part of the system through the substrate in the frequency domain. In the design, fully differential 88 MHz sine wave is used as the input of the clock re-generation circuit. 88 MHz is 4 times of the main 22 MHz clock frequency. This gives us freedom in the control signal design. By dividing the 88 MHz clock signal, we can have more options in delay generation, which is essential in the timing control. The 3 amplifies have different requirements. The main purpose of the circuit is to fasten the edges of the clock signal, however the add-in noise of the amplifiers itself should be minimized. As a cascade system, the first amplifier is the most critical stage in the noise design. Besides the low noise requirement, the first amplifier should have lowest 3 dB cutoff frequency and highest gain among the 3 amplifiers to suppress the noise power in the following stages. The 3 dB bandwidth of the first amplifier only needs to be larger than the clock frequency to allow the clock signal passing. A pair of loading capacitor is applied between the first and second amplifiers to adjust the bandwidth of the first stage. The last stage is used to clip the signal into a square wave and convert the differential signal into single-ended output. Its bandwidth needs to be large to satisfy the abundant frequency information of the square wave. The second stage is used to provide more gain to the clock signal before it is clipped in the third stage. It can have a lower gain than the first stage but a larger bandwidth

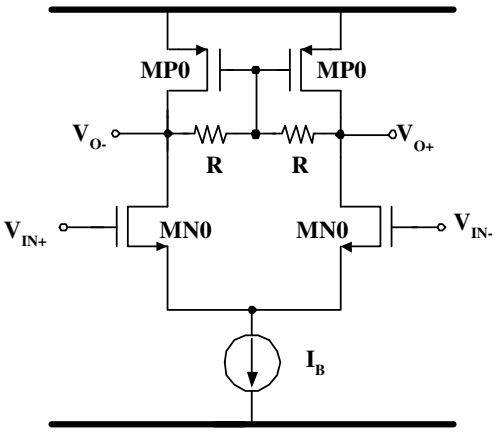

Fig. 111. The schematic of the first two amplification stages in the clock re-generation circuit

to accommodate the steeper slope.

The first and second amplifiers shares the same circuit architecture as shown in Fig. 111. Their gain can be calculated as,

$$Gain = g_{m1} \cdot g_{m2} R_{o2} R \tag{6.27}$$

where g_{m1} and g_{m2} are the transconductance of MN0 and MP0, R_{o2} is the output impedance of MP0. As shown in (6.27) resistors are used to provide common mode feedback and boost the gain as well. Smaller resistors are used in the first amplifier for noise consideration. The loading capacitors put between the first and second amplifiers are 0.4 pF to provide a 90 MHz 3 dB bandwidth for the first amplifier. Large size transistors are used in the input differential pair in the first two amplifier to provide gain and limit noise. The third stage is a two-stage OTA as illustrated in Fig. 112. Both stages provide some gain to finally clip the signal into square wave and the signal is converted to single ended clock sequence. The circuit parameters for the three amplifiers are listed in Table XXIX. Fig. 113 shows the output signal waveform of the clock re-generation circuit. The jitter of the output clock can be calculated

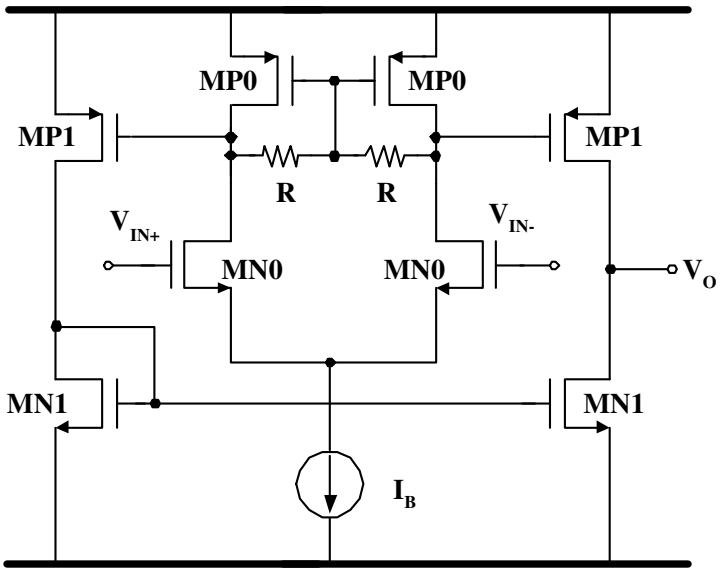

Fig. 112. The schematic of the third amplification stage in the clock re-generation circuit

from (6.26) and is 0.7 ps, which is much smaller than the 1.76 ps requirement.

The main clock signal applies to the ADC is a pair of non-overlap clock signal at 22 MHz. Fig. 114 shows the circuit used to generate these non-overlap clock signal, and Fig. 115 illustrates the counter used to divide the 88 MHz output of the clock re-generation circuit.

F. 802.11b/Bluetooth ADI Design Testing and Verification

The prototype of the time-interleaved pipeline ADC was fabricated in IBM 0.25 μm BiCMOS process through MOSIS. The ADC is integrated with the entire 802.11b/Bluetooth dual-mode receiver. Fig. 116 shows the chip microphotograph. The silicon area, for both I and Q channels, pads and the calibration circuit, is 10.92 mm^2. The ADCs and their auxiliary circuits occupy approximately half of the total die area.

Table XXIX. The circuit parameters for the clock re-generation circuit.

Devises	Amplifier 1	Amplifier 2	Amplifier 3
MN0 ($\mu m/\mu m$)	38.4/0.48	28.8/.48	28.8/0.48
MN1 ($\mu m/\mu m$)	—	—	28.8/0.48
MP0 ($\mu m/\mu m$)	64/0.8	32/0.8	32/0.8
MP1 ($\mu m/\mu m$)	—	—	32/0.8
R ($k\Omega$)	3.6	2.4	2.4
I_B (μA)	600	400	400

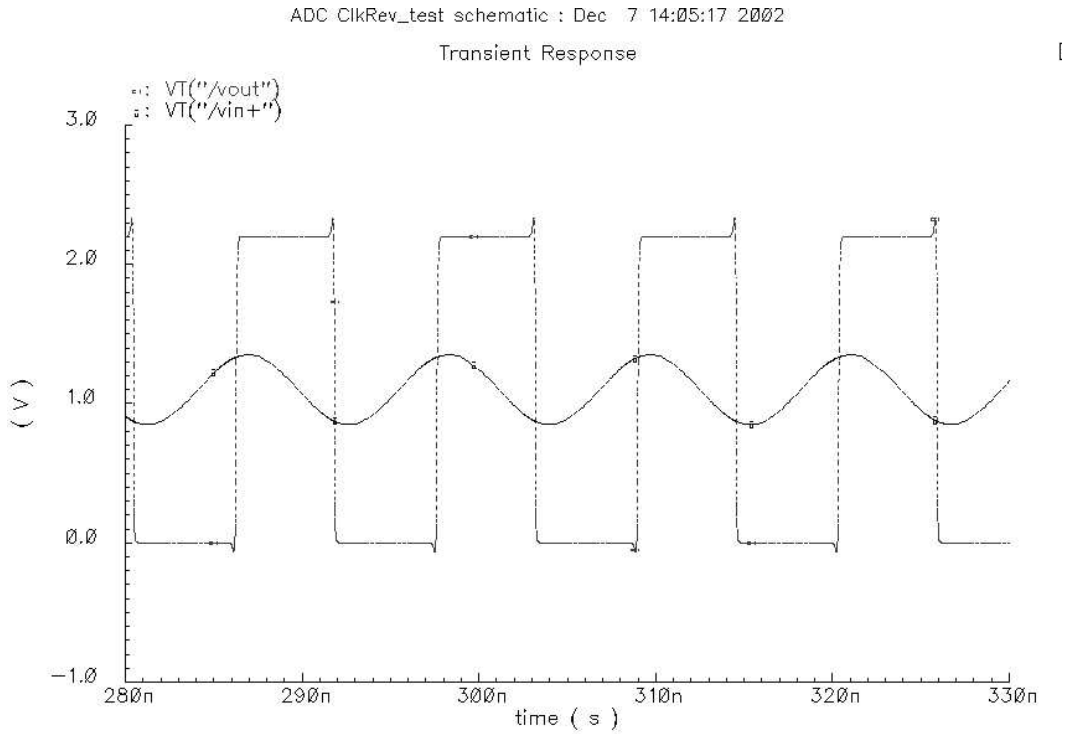

Fig. 113. The output of the clock re-generation circuit vs. its input

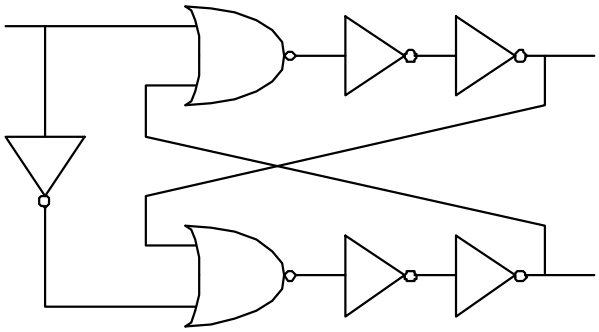

Fig. 114. The schematic of the non-overlap clock generator

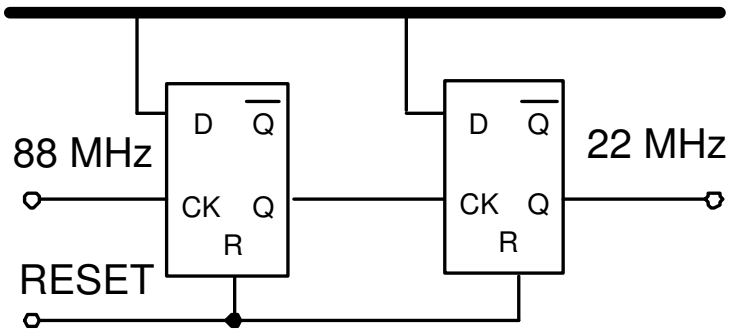

Fig. 115. The schematic of clock divider

1. ADC Layout Design and Consideration

The implementation of the circuit design on the silicon ultimately determines the performance of the ADC. As we have discussed in the previous chapter, the matching among the pipeline ADC branches affects offset, gain error and linearity specs of the ADC. Locally, the matching among transistors in circuit blocks, such as OpAmps and current mirrors, also has impact on the overall ADC performance. Substrate and supply noise is another serious issue in the circuit layout design. All the circuits on the same chip share the same substrate. Usually the substrate is connected to the ground to prevent latch-up. All sorts of noise, especially the ones generated by the switching of the digital and switched-capacitor circuits, gets to broadcast through the substrate and causes fluctuation in the ground voltage. Analog circuits are sensitive to this fluctuation. The unstable ground voltage will appears as noise in the analog circuit. For the same reason, noisy supply voltage is not desired in the analog circuit design, either. The drop in the supply voltage is caused by the current burst in the digital circuit. Therefore, layout techniques are needed to improve matching property of the ADC and lower noise.

A common way to improve matching is to use fully symmetric floor plan in the layout design. In our ADC design, we placed critical circuit block, such as the input differential pair of the OpAmps, resistors in the reference ladder and capacitor bank of the MDACs etc., in a common-centroid way. At system level, we arrange the pipeline ADC branches in a symmetrical way, as illustrated in Fig. 116. We first layout one single branch of the ADC, then copy and mirror it to get the other branch. Next we copy and mirror the whole ADC to obtain the ADC in the other channel.

Three major methods are used in to suppress the substrate and supply noise. Firstly, the digital supply and analog supply are separated. The digital ground and

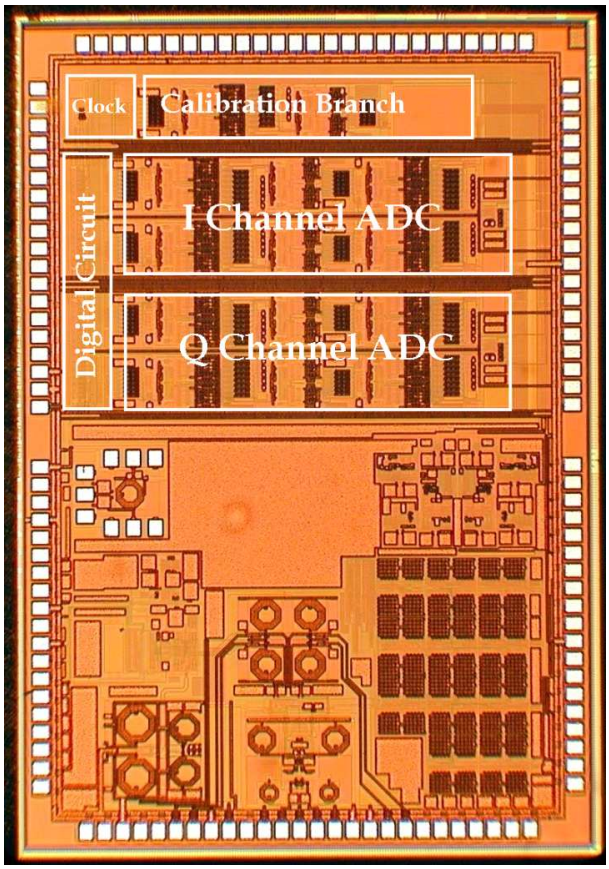

Fig. 116. The die microphotograph of the time-interleaved pipeline ADC on the 802.11b/Bluetooth receiver chip

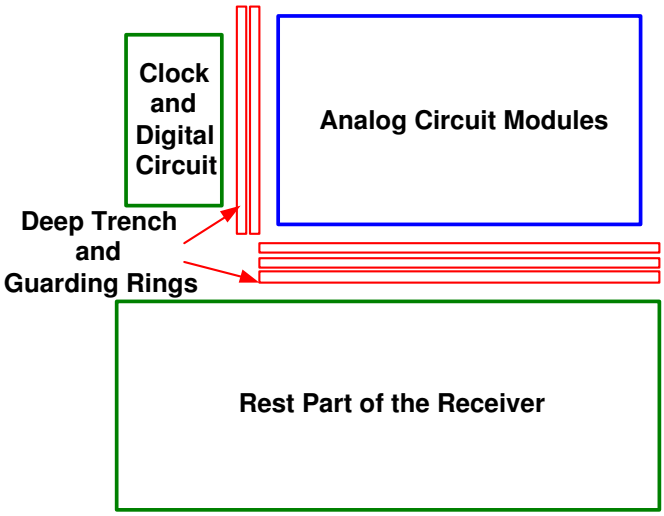

Fig. 117. Deep trench and guarding ring placement on layout

analog ground only connected though narrow traces. By doing that, we limited the noise broadcast in the supply. Secondly, we applied deep trenches and guarding rings between analog and digital circuits also between the ADC and rest part of the receiver to isolate substrate noise. Fig. 117 shows the principle of deep trench and guarding ring deployment. Thirdly, we put capacitor in empty space on the chip to decoupling the supply and ground. Those capacitor along with the off-chip decoupling capacitor helps to filter out noise and stabilize the supply voltage.

2. Testing Setup and Print Circuit Boards (PCBs) Design

Fig. 118 depicts the testing plan for the ADC. Two PCBs have been designed for the purpose of testing. One board has the ADC chip, or so-called Devise Under Testing (DUT) on it. The other board is called supply and DAC board, which provides supply voltage and data processing functionalities. The input sinusoidal signal to the ADC is generated from Agilent Signal Generator E4432B while the clock to the ADC is generated from Agilent Signal Generator 33250A. E4432B and 33250A are able to

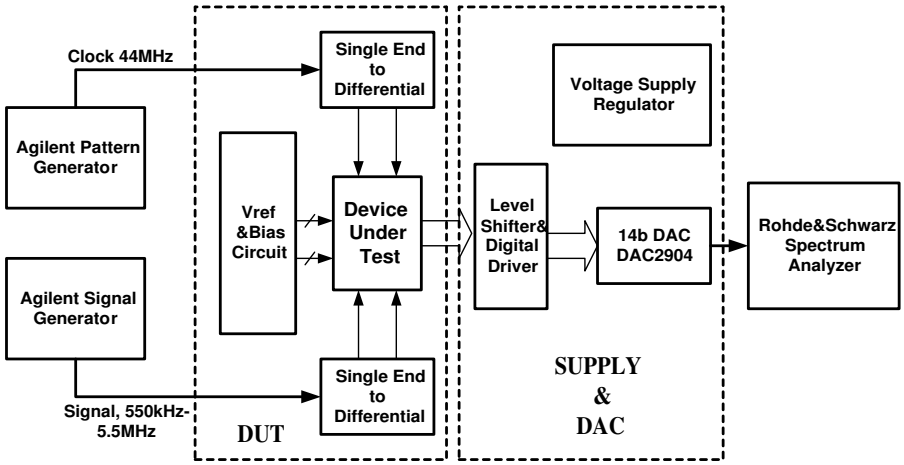

Fig. 118. The testing setup for the time-interleaved pipeline ADC

output signal with an SNR of 140 db and 120 dB, respectively. The noise floor from both instruments are much lower than the quantization noise floor we are interested in the testing. The digital outputs of the ADC is buffered and re-shaped to get rid of the distortion caused by transmission before applied to a 14-bit DAC. The DAC used is Texas Instruments DAC2904. Since the DAC has a resolution of 14-bit, it is ideal to the 11-bit ADC testing chip. We can use a spectrum analyzer, Rohde& Schwarz spectrum analyzer FSEB, to examine SNR of the ADC directly through the DAC output.

Besides the ADC testing chip, the DUT board also has biasing, reference and single-ended-to-differential conversion circuits on it. The biasing circuits are used to provide current bias for the OpAmps and comparators in the ADC. Fig. 119 illustrates the current biasing circuit on the DUT board. A potentiometer is used to adjust the bias current that goes into the circuit. The bias current is measured through the voltage across the resistor R1. The two capacitors in the circuit is to filter out the noise in the bias current. The full-scale reference voltage is applied to the DUT from outside. Fig. 120 shows the buffer circuit that supplies the reference voltage to the ADC. The

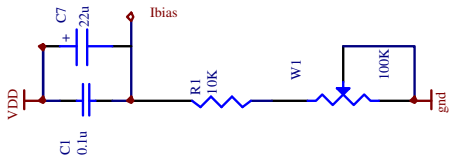

Fig. 119. The biasing circuit setup for the ADC testing

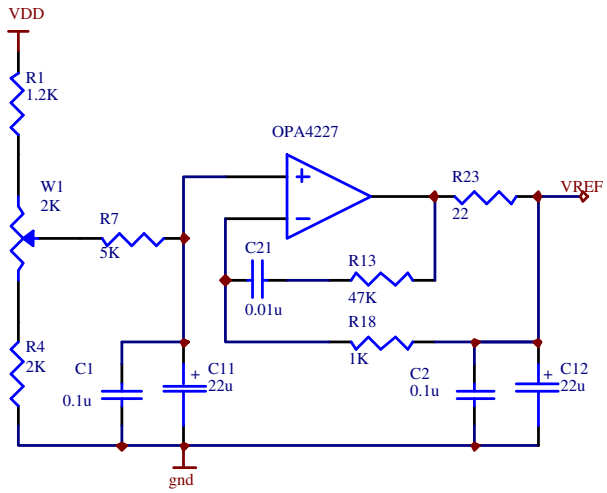

Fig. 120. The reference voltage circuit for the ADC testing

OpAmp in the circuit is OPA4227 (Texas Instruments). It is a low noise, low offset amplifier and has a bandwidth of 8MHz. The full-differential architecture of the ADC requires differential signal and clock input. The signal generators available however only have single-ended output. To solve this issue, a single-ended-to-differential conversion circuit is designed for the DUT board as shown in Fig. 121. A balun is used to re-generate the differential signal from the single-ended input. The balun used in the design is coilcraft TTWB2010, which has a 3 dB bandwidth from 0.3 to 250 MHz.

The ADC is supplied with a 2.5 V VDD voltage. That voltage is obtained from 5 V supply generator. On the supply and DAC board, we have a regulator circuit to filter out fluctuation in the voltage generator output and provide a clean supply voltage for the ADC. The core of the regulator circuit is the National semiconductor

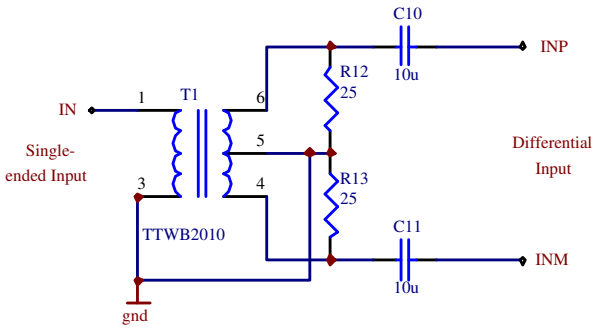

Fig. 121. The single-ended-to-differential V-V conversion circuit for the ADC testing

3-terminal adjustable regulator LM317, as shown in Fig. 122. The DAC2904 used in the testing is a fully-differential current steering DAC. We need to convert its output to single-ended voltage before connect to the spectrum analyzer. Fig. 123 illustrates the schematic of the conversion circuit. Since the output of the DAC has a frequency of 44 MHz, we need a high speed OpAmp in the conversion circuit. The OpAmp used in the circuit is Texas Instruments OPA2653, which has a unit gain frequency of 700 MHz. OPA2653 also has large current drive capability, 140 mA maximum, which is big enough to drive the 50 Ω resistance load from the measurement instrument.

Besides the SNR measurement directly obtained from the PCBs, we also captured the digital output of the ADC and processed it in the computer to get other specs of the ADC, such as DNL and INL. The digital output of the ADC is captured by Agilent 54622D Mixed-Signal Oscilloscope.

3. Measurement Results

In the testing, 550 kHz and 5.5 MHz sinusoidal signals are applied to the DUT to measure the ADC performance under the Bluetooth and 802.11b receiving mode, respectively. The sampling rates used are 11 MSample/s for the Bluetooth mode and 44 MSample/s for the 802.11b mode. A 0 dB input power level is corresponds to

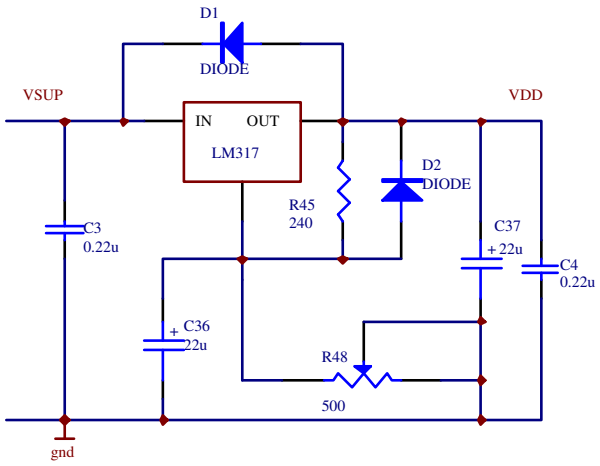

Fig. 122. The voltage regulator circuit for the ADC testing

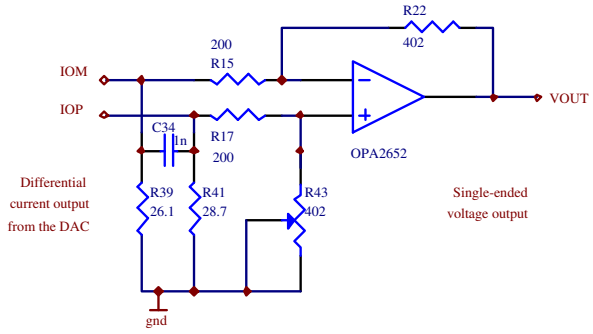

Fig. 123. The differential-to-single-ended I-V conversion circuit for the ADC testing

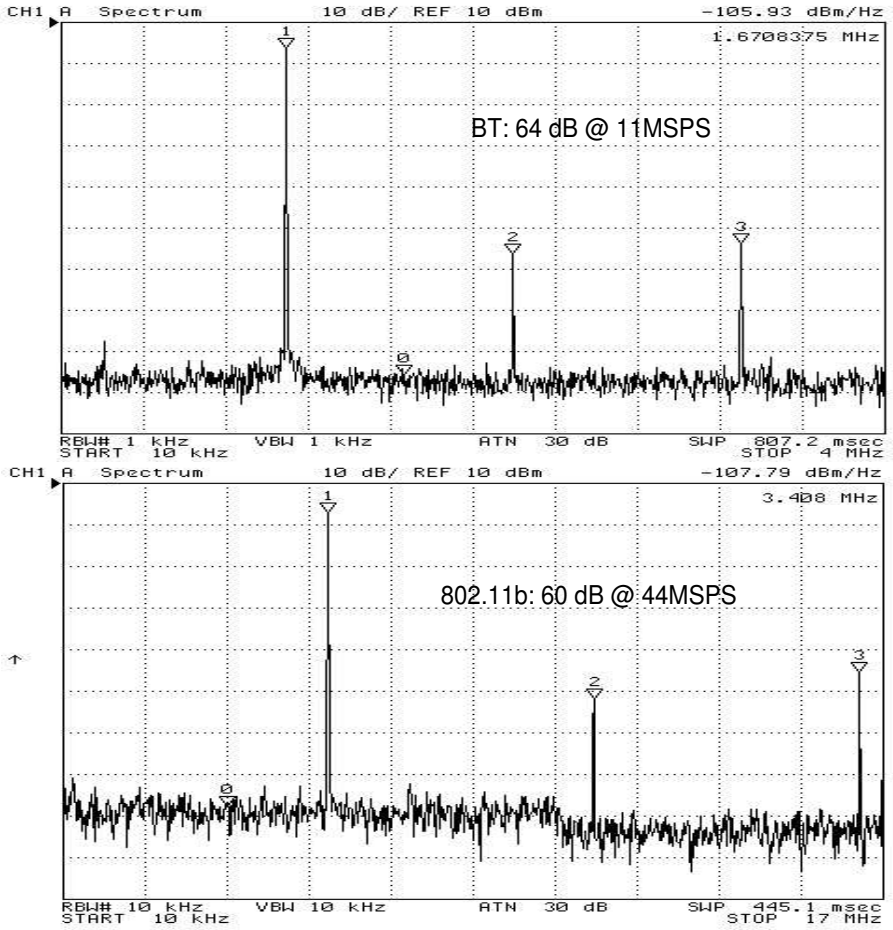

Fig. 124. The measured SNR for the time-interleaved pipeline ADC

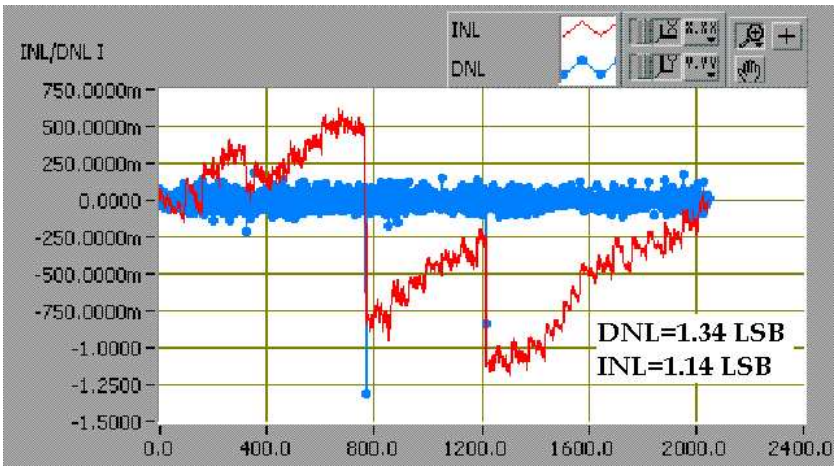

Fig. 125. DNL and INL performance of the time-interleaved pipeline ADC with calibration off

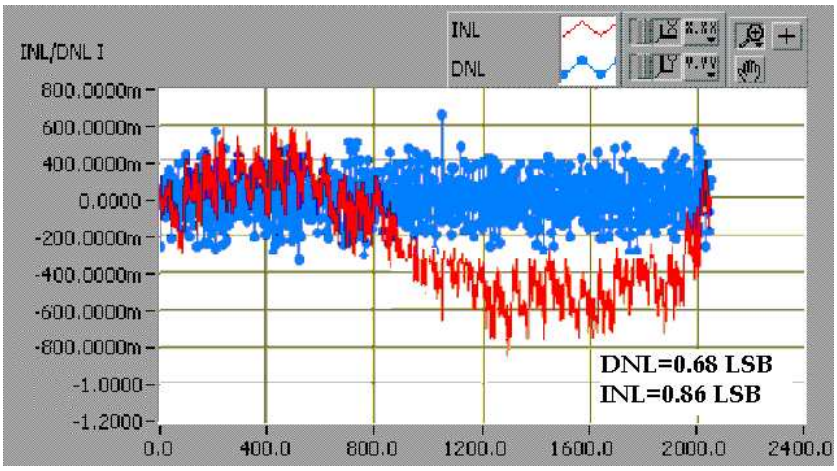

Fig. 126. DNL and INL performance of the time-interleaved pipeline ADC with calibration on

a 2.0 Vp-p sinusoidal signal. Fig. 124 shows the measured SNR in both receiving modes, which is directly captured from the spectrum analyzer. The ADC achieves a 60dB SNR for the 802.11b signal sampling at 44 MSample/s without disabling the last pipeline stage, and a 64dB SNR for the Bluetooth signal at a sampling rate of 11 MSample/s. The ADC power consumption are 20.2 mW for the 801.11b mode and 14.8 mW for the Bluetooth receiving modes. In the DNL and INL measurement. Triangular waveform is applied to the input of the ADC. The corresponding output digital codes are processed by software to get the averaged DNL and INL. The on-line digital calibration structure is also tested during the DNL and INL measurement. Fig. 125 and Fig. 126 depict the DNL, INL plot when the calibration is off and on, respectively. As we can see, the DNL improves from 1.31 LSB to 0.48 LSB; and INL improves from 1.18 LSB to 0.86 LSB. The measurement shows that the on-line calibration is helpful in improving the linearity of the ADC. Especially in the DNL measurement, the on-line calibration prevents the missing code as it appears in the calibration off DNL measurement. The performance of this ADC is summarized in Table XXX.

Many previously reported ADCs have similar specification. We made a comparison based on the measured performance of other pipeline ADCs implementations with similar specs. The Figure Of Merit (FOM) used here is,

$$FOM = \frac{ENOB \cdot SamplingRate}{Power} \tag{6.28}$$

where ENOB is effective number of bits. The comparison is illustrated in Fig. 127 and Table XXXI. As we can see, the time-interleaved ADC has the best power consumption performance.

Table XXX. The summary of the experimental results of the time-interleaved pipeline ADC

Standards	Bluetooth	802.11b
Signal Bandwidth	550 kHz	5.5 MHz
Sample Frequency	11 MHz	44 MHz
SNR	64 dB	60 dB
Power Consumption	14.8 mW	20.2 mW
Supply Voltage	2.5 V	
Process	0.25 μm BiCMOS	
Area	10.92 mm^2	

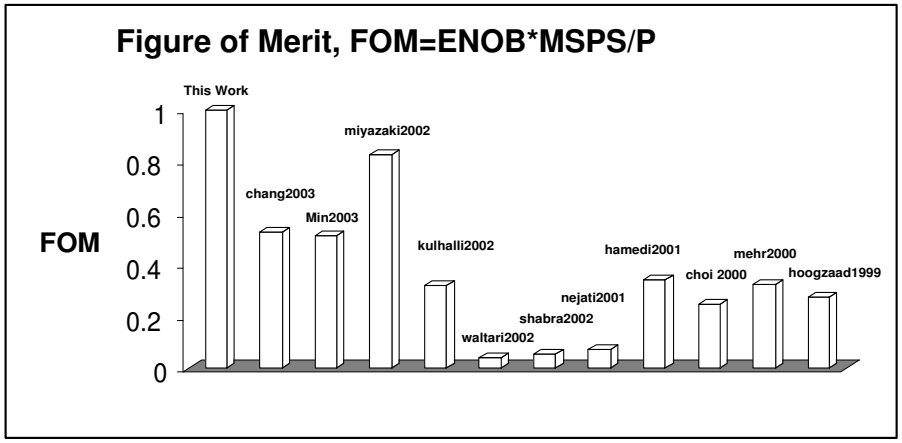

Fig. 127. The performance comparison with similar implementations

Table XXXI. The comparison of power FOM

Implementations	ENOB (bit)	Sampling Rate (MSPS)	Process (μm)	Supply (V)	Power (mW)	Area (mm^2)	FOM
This work	10	44	0.25BiCMOS	2.5	20.2	4.37	1
chang2003 [72]	10	25	0.35CMOS	1.4	21.0	2.24	0.53
min2003 [73]	10	80	0.18CMOS	3.0	69.0	1.85	0.51
miyazaki2002 [74]	10	30	0.3CMOS	2.0	16.0	3.12	0.83
kulhalli2002 [66]	12	21	0.18CMOS	2.7	35.0	0.82	0.32
waltari2002 [67]	13	50	0.35BiCMOS	2.9	715	6.00	0.04
shabra2002 [75]	12	61	0.35CMOS	3.4	600	--	0.05
nejati2001 [76]	10	40	0.6CMOS	2.5	240	--	0.07
hamedi2001 [77]	10	50	0.25CMOS	2.5	65.0	3.20	0.34
choi2000 [78]	10	25	0.25CMOS	1.5	45.0	2.21	0.24
mehr2000 [79]	10	40	0.35CMOS	3.0	55.0	2.60	0.32
hoogzaad1999 [80]	10	40	0.6BiCMOS	5.0	65.0	0.80	0.27

CHAPTER VII

CONCLUSION

As explained in the first chapter, the purpose of this research work is to seek solutions to the design issues that exists in the wireless receiver ADI implementation. In order to do so, the ADI designs for two different wireless receivers are carefully studied. The Bluetooth receiver features with fast settling requirement and the 802.11b/Bluetooth dual-mode receiver requires the ADI to operate under different communication standards without significantly increasing the implementation cost. Both ADI designs are aimed to achieve power consumption optimization under the low supply voltage environment. In this chapter, we will summarize the contribution of this research work and provide insights based on the observation obtained in the course of the research.

A. Summary

A GFSK demodulator based on zero-crossing detection scheme is designed for the low-IF Bluetooth receiver. By skipping the VGA and the AGC loop, the demodulator provides real-time response in the received signal digitization. An additional shape keeping one-shot is added to reshape the pulse width of the output of the zero-crossing detection one-shots. As a result, the proposed demodulator has a better immunity to the process variation and mismatching. The demodulator design is fabricated in the 0.35 μm CMOS technology. The large LO frequency offset between the transmitter and the receiver is converted into DC offset by the zero-crossing detector. Utilizing DC offset free segment of the Bluetooth data packets, a DC offset cancellation circuit is employed to compensate the DC level shift caused by the LO frequency offset. In the lab measurement, the proposed GFSK demodulator achieves an SNR of 16.2 dB

at 0.1% BER and a co-channel interference rejection ratio of 11 dB. The DC offset cancellation circuit is able to remove an equivalent LO frequency offset of ±120 kHz. The zero-crossing demodulator offers best detection performance and LO frequency offset immunity with a comparable power dissipation in comparison with the reported implementations [32]-[34].

Although it has been introduced before in the high speed ADC design, the time-interleaved pipeline ADC structure is proposed for the multi-standard receiver ADI design for the first time. Comparing with the popular $\Sigma\Delta$ ADC approach, the time-interleaved ADC structure is more suitable for the wide band applications. The large dynamic range of the ADC eliminate the need for the received signal power level control circuit, and hence assures the fast settling of the baseband. The prototype chip is fabricated in 0.25 μm BiCMOS technology. An on-line digital calibration scheme is also introduced to reduce the negative effect caused by the non-ideality in the circuit and compensate the mismatching caused by the process variation. An SNR of 60 dB and 64 dB SNR are obtained under 802.11b and Bluetooth receiving modes in the testing, respectively. The power consumption of the ADI is 20.2 mW under 802.11b receiving mode and 14.8 mW under the Bluetooth mode. The proposed ADI design for the dual-mode receiver achieves the best power figure of merit with respect to the previously reported work.

B. Insights on the Receiver ADI Design

As discussed in Chapter II, multi-standard compatibility, real-time decision capability, power consumption optimization and high speed requirement become design concerns in the wireless receiver ADI design. What are the insights that we can gain through this research?

1. *Multi-standard compatibility*

   The baseband part of a multi-standard wireless receiver usually needs to accommodate different dynamic ranges and data rates. The data detection is preferred to be done in digital domain utilizing the flexibility of the DSP modules. Analog demodulators and multiple ADCs approaches become unrealistic for the ADI design because of the huge hardware cost and high implementation complexity. Therefore, configurable ADCs become desirable solution for multi-standard ADI design.

   A $\Sigma\Delta$ ADC consists of a $\Sigma\Delta$ modulator and a subsequent digital decimation filter. By programming or reconfiguring the digital decimation filter, $\Sigma\Delta$ ADCs can easily achieve different dynamic ranges over different signal bands. Naturally, $\Sigma\Delta$ ADCs are the first to be used in multi-standard applications. However, the over-sampling nature of the $\Sigma\Delta$ ADC prevents it to be used in wide-band applications, and the changes in the OSR bring drastic variations in the ADC dynamic range as it switches between standards. In general, $\Sigma\Delta$ ADCs are more suitable for narrow-band multi-standard ADI design. Time-interleaved Nyquist-rate ADCs, on the other hand, are able to provide consistent dynamic range over a wide frequency band, and hence are more attractive for multi-standard receivers that involves wide band signals. Since wide band and high speed are the development trends in the wireless technologies, the configurable time-interleaved ADC structure may find more applications in the multi-standard ADI design.

2. *Real time response*

   To achieve real-time response, minimum delay is required in the receiver baseband circuit. Usually, the settling time in the baseband can be reduced by

relaxing the received signal power control requirement. As as direct result, the dynamic range of the ADI increases accordingly. However, using coarse gain control or even skipping the VGA is desirable in a receiver design as we push towards the software defined radio. Therefore, using high resolution ADI is one way to reduce the signal processing delay in the wireless receiver.

High dynamic range ADC is not the only solution for this problem. For some modulation formats, such as FSK and other continuous phase FM modulated signal, can be detected directly by simple hardware demodulators. In spite of slight degradation in the detection performance, the hardware demodulator ADI is usually able to provide fast baseband settling with reduced circuit complexity, as proved by the ADI design for the low-IF Bluetooth receiver.

3. *Power consumption optimization*

   ADI is one of the major contributors in the total receiver power consumption. As shown in the 802.11b/Bluetooth dual-mode receiver design, the ADC dissipates more than one third of the receiver power consumption budget. Power consumption optimization needs to be conducted at every level of the ADI design. As proved in the 802.11b/Bluetooth ADI design, the adoption of time-interleaved ADC architecture at system design level, the use of the multi-bit stage pipeline ADC branch at the sub-block design level and OpAmp design at the transistor level all help to save power dissipation in the ADI.

4. *Wide signal bandwidth and high speed requirement*

   Wide band and high speed are the ultimate goal of the development in the wireless technologies. However, the high speed in the ADI is usually achieved at a cost of the dynamic range. Fortunately, the modulation formats adopted

by the wide band systems often have large Euclidean distance in their symbol coordinate. The relaxed resolution requirement allow the use of simple structure in the ADI design, such as flash ADC. Currently, ADI structure like pipeline ADC is already able to operate under moderately high speed. By using time-interleaved structure, those ADCs are able to provide the fast sampling rate that is required in the UWB systems. The larger dynamic range provided by the ADC branches is able to relax the specs of the gain control blocks in the receiver. As a consequence, the pursuing of high resolution, high speed ADI designs will eventually lead to the implementation of the ideal software defined radio.

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APPENDIX A

THE MATLAB AND SIMULINK MODELS FOR THE BLUETOOTH GFSK DEMODULATORS

A.1 Optimal Non-coherent Demodulator

```
clear all;
j=sqrt(-1);
% Generate random data

Num_data=240000;
% Num_data=21; % The sync word is 21 bit long
data=2*round(rand(1, Num_data))-1;
samp=20;
smpl_sp=Num_data*samp;
% This data array is used for synchronization.
% data=[1 -1 1 1 1 1 1 1 -1 -1 1 1 -1 1 -1 1 1 1 -1 -1];
sp_data=zeros(1, Num_data*samp);
for i=1 : Num_data
   sp_data((i-1)*samp+1:i*samp)=data(i);
end

% Add Guassian pulse shape
BT=.5;
t=[-samp:1:samp];
ht=sqrt(pi*2/log(2))*BT/samp*exp(-
(pi^2*2*(BT/samp)^2/log(2))*power(t,2));
psh_sig=conv(sp_data, ht);


% BT/samp=B, the Guassin filter cause 1 bit delay
% Define complex envelope of the GFSK signal
ind=0.32; % using norminal value, modulation index for BT
is 0.28-0.35
phi=0;
gfsk=zeros(1, smpl_sp-2*samp);
for i=1 : smpl_sp-2*samp,
   phi=phi+psh_sig(i+2*samp); % Get rid of the first 2 bits
to obtain better synchronization
   gfsk(i)=exp(j*ind*pi*phi/samp);
end
```

```
% Match filters
d00=ones(1, 4*samp);
d01=[ones(1, 3*samp) (-1)*ones(1,samp)];
d10=[ones(1, 3*samp)*(-1) ones(1,samp)];
d11=ones(1, 4*samp)*(-1);
for i=1:samp,
   d00(i+samp)=-1;
   d00(i+samp*2)=-1;
   d01(i+samp)=-1;
   d01(i+samp*2)=1;
   d10(i+samp)=1;
   d10(i+samp*2)=-1;
  d11(i+samp)=1;
   d11(i+samp*2)=1;
end
sd00=conv(d00, ht);
sd01=conv(d01, ht);
sd10=conv(d10, ht);
sd11=conv(d11, ht);
s00=sd00(2*samp+1: samp*4);
s01=sd01(2*samp+1: samp*4);
s10=sd10(2*samp+1: samp*4);
s11=sd11(2*samp+1: samp*4);
phi00=0;
phi01=0;
phi10=0;
phi11=0;
for i=1 : 2*samp,
   phi00=phi00+s00(i);
   mf00(i)=((exp(j*ind*pi*phi00/samp))').';
   phi01=phi01+s01(i);
   mf01(i)=((exp(j*ind*pi*phi01/samp))').';
   phi10=phi10+s10(i);
   mf10(i)=((exp(j*ind*pi*phi10/samp))').';
   phi11=phi11+s11(i);
   mf11(i)=((exp(j*ind*pi*phi11/samp))').';
end
d000=[ones(1, samp) -1*ones(1, 3*samp) ones(1, samp)];
d001=[ones(1, samp) -1*ones(1, 2*samp) ones(1, samp) -
1*ones(1, samp)];
d010=[ones(1, samp) -1*ones(1, samp) ones(1, samp) -
1*ones(1, samp) ones(1, samp)];
d011=[ones(1, samp) -1*ones(1, samp) ones(1, 2*samp) ];
d100=[-1*ones(1, samp) ones(1, samp) -1*ones(1, samp) -
1*ones(1, samp) ones(1, samp)];
```

```
d101=[-1*ones(1, samp) ones(1, samp) -1*ones(1, samp)
ones(1, samp) -1*ones(1, samp)];
d110=[-1*ones(1, samp) ones(1, 2*samp) -1*ones(1, samp)
ones(1, samp)];
d111=[-1*ones(1, samp) ones(1, 3*samp) -1*ones(1, samp)];
sd000=conv(d000, ht);
sd001=conv(d001, ht);
sd010=conv(d010, ht);
sd011=conv(d011, ht);
sd100=conv(d100, ht);
sd101=conv(d101, ht);
sd110=conv(d110, ht);
sd111=conv(d111, ht);
s000=sd000(2*samp+1: samp*5);
s001=sd001(2*samp+1: samp*5);
s010=sd010(2*samp+1: samp*5);
s011=sd011(2*samp+1: samp*5);
s100=sd100(2*samp+1: samp*5);
s101=sd101(2*samp+1: samp*5);
s110=sd110(2*samp+1: samp*5);
s111=sd111(2*samp+1: samp*5);
phi000=0;
phi001=0;
phi010=0;
phi011=0;
phi100=0;
phi101=0;
phi110=0;
phi111=0;
for i=1 : 3*samp,
   phi000=phi000+s000(i);
   mf000(i)=((exp(j*ind*pi*phi000/samp))').';
   phi001=phi001+s001(i);
   mf001(i)=((exp(j*ind*pi*phi001/samp))').';
   phi010=phi010+s010(i);
   mf010(i)=((exp(j*ind*pi*phi010/samp))').';
   phi011=phi101+s011(i);
   mf011(i)=((exp(j*ind*pi*phi011/samp))').';
   phi100=phi100+s100(i);
   mf100(i)=((exp(j*ind*pi*phi100/samp))').';
   phi101=phi101+s101(i);
   mf101(i)=((exp(j*ind*pi*phi101/samp))').';
   phi110=phi110+s110(i);
   mf110(i)=((exp(j*ind*pi*phi110/samp))').';
   phi111=phi111+s111(i);
```

```
   mf111(i)=((exp(j*ind*pi*phi111/samp))').';
end


% Add white noise, define Eb/N
EbN=[8 10 11 12 13 14 16];
for k=1:length(EbN),
   sigma=sqrt(samp/2/power(10,(EbN(k)/10)));
   %sigma=0;
   Nn=length(gfsk);
   No_I=randn(1, Nn)*sigma;
   No_Q=randn(1, Nn)*sigma;

% LPF filters the noise
   order=5;
   bwlp=2/samp;
    [BBS,ABS]=butter(order, bwlp);

% Let the noise go through the filter
   Nk_I=filter(BBS,ABS,No_I);
   Nk_Q=filter(BBS,ABS,No_Q);

% Received signal
   rx_sig=gfsk+(Nk_I+j*Nk_Q);


% Run the received signal through match filter bank
% Calculate the first bit
   lambda(1)=abs(sum(rx_sig(1:2*samp).*mf00));
    lambda(2)=abs(sum(rx_sig(1:2*samp).*mf01));
    lambda(3)=abs(sum(rx_sig(1:2*samp).*mf10));
    lambda(4)=abs(sum(rx_sig(1:2*samp).*mf11));
    [mxl, ix]=max(lambda);
    Dr(1)=floor(ix/3)*2-1;

   for i=2:(length(rx_sig)/20-1)
     icur=samp*(i-2);
     pSt=icur+1;
      pEd=icur+samp*3;
      if Dr(i-1)==1
        lambda(1)=abs(sum(rx_sig(pSt:pEd).*mf100));
        lambda(2)=abs(sum(rx_sig(pSt:pEd).*mf101));
        lambda(3)=abs(sum(rx_sig(pSt:pEd).*mf110));
          lambda(4)=abs(sum(rx_sig(pSt:pEd).*mf111));
      else
```

```
          lambda(1)=abs(sum(rx_sig(pSt:pEd).*mf000));
        lambda(2)=abs(sum(rx_sig(pSt:pEd).*mf001));
        lambda(3)=abs(sum(rx_sig(pSt:pEd).*mf010));
          lambda(4)=abs(sum(rx_sig(pSt:pEd).*mf011));
      end
      [mxl, ix]=max(lambda);
      Dr(i)=floor(ix/3)*2-1;
   end
      Ds=data(2:Num_data-2);
      De=Dr-Ds;
      err=find(De);
      BER(k)=(length(err))/length(Ds)*100;
      %[np f]=psd(Nk_I, 8192, samp*fIF);
      %[sp f]=psd(gfsk_I, 8192, samp*fIF);
       %snr(k)=10*log10(sum(sp)/sum(np));
    end
BER
semilogy(EbN, BER/100);
grid on;
ylabel ('BER');
xlabel ('Eb/No');
title ('BER Performance of Optimal Non-coherent GFSK
Demodulator');
```

A.2 Delay line demodulator

```
clear all;

% Generate random data
Num_data = 30000;
data = 2*round(rand(1, Num_data))-1;
%data=ones(1, Num_data);
%for i=1:Num_data-1,
%   data(i+1)=-data(i);
%end
samp = 80;
samp2 = 20;
stp = samp/samp2;
sp_data = zeros(1, Num_data*samp);
for i = 1 : Num_data
   sp_data((i-1)*samp+1:i*samp) = data(i);
end

BT = .5;
```

```
t=[-samp:1:samp];
ht = sqrt(pi*2/log(2))*BT/samp*exp(-
(pi^2*2*(BT/samp)^2/log(2))*power(t,2));
psh_sig = conv(sp_data, ht);
% BT/samp=B, the filter 1 bit delay

% Define modulation index, IF frequency and bit duration
ind=0.35;
fIF=1.0e6;
Ts=1e-6;

% Define Eb/N
EbN=15.4;
sigma=sqrt(samp/2/power(10,(EbN/10)));
%sigma=0;

gfsk_I = zeros(1, Num_data*samp-2*samp);
gfsk_Q = zeros(1, Num_data*samp-2*samp);
phi = 0;
for i = 1 : Num_data*samp-2*samp,
  phi = phi + psh_sig(i+2*samp);
  gfsk_I(i) =
cos(2*pi*fIF*rem(i,samp)/samp*Ts+ind*pi*phi/samp);
  gfsk_Q(i) =
sin(2*pi*fIF*rem(i,samp)/samp*Ts+ind*pi*phi/samp);
  %No_I(i)=sqrt(2)*cos(2*pi*fIF*rem(i,samp)/samp*Ts);
  %No_Q(i)=sqrt(2)*sin(2*pi*fIF*rem(i,samp)/samp*Ts);
end
T=linspace(0, 1e-6*(Num_data-2), Num_data*samp-2*samp)';

%Generate white noise
Nn=length(gfsk_I);
%Nseed=randn(1, Nn)*sigma;
%No_I=Nseed.*No_I;
%No_Q=Nseed.*No_Q;
No_I=randn(1, Nn)*sigma;
No_Q=randn(1, Nn)*sigma;

% IF bandpass filter, and filtering the noise
DataIn=[(gfsk_I)' -(gfsk_Q)'];
FilterOut;
r_I=DataOut(:,1)';
r_Q=DataOut(:,2)';
clear DataIn DataOut;
DataIn=[(No_I)' -(No_Q)'];
```

```
FilterOut;
Nk_I=DataOut(:,1)';
Nk_Q=DataOut(:,2)';
clear DataIn DataOut;
rk_I=sign(r_I+Nk_I);
rk_Q=sign(r_Q+Nk_Q);
%rk_I=rkg_I(1:stp:length(rkg_I));
%rk_Q=rkg_Q(1:stp:length(rkg_Q));

Nr=length(rk_I);
rkt_QI=zeros(1,Nr);
rkt_IQ=zeros(1,Nr);

BD=0.718*[1 -1]; %sample rate is 80M
AD=[1 -0.436];
%BD=0.39*[1 -1]; % sample rate is 20M
%AD=[1 0.2];

d_I=(filter(BD, AD, rk_I));
d_Q=(filter(BD, AD, rk_Q));
rkt_QI=rk_Q.*d_I;
rkt_IQ=rk_I.*d_Q;
skto=-rkt_QI+rkt_IQ;

% Lowpass filter
wlp=(620e3)/(samp/2/Ts);
[BL,AL]=butter(3,wlp);
skto=filter(BL,AL,skto);
%skt=-skto-0.12727;
skt=-skto(1:stp:length(skto))-0.12727;%-0.12727;%-0.129933;
syn=118;%119
for i=1:Num_data-11,
   ns=syn+(i-1)*samp2;
   nd=syn+i*samp2;
   if sum((skt(ns:nd)))>0
       Dr(i)=1;
   else Dr(i)=-1;
   end
end

Ds=data(6:Num_data-6);
De=Dr-Ds;
err=find(De);
BER=(length(err))/(Num_data-11)*100
[np f]=psd(Nk_I, 8192, samp*fIF);
```

```
[sp f]=psd(r_I, 8192, samp*fIF);
snr=10*log10(sum(sp)/sum(np))
```

A.2 Zero-crossing demodulator

```
clear all;

% Generate random data

Num_data = 100;
data = 2*round(rand(1, Num_data))-1;
%data=ones(1, Num_data);
%for i=1:Num_data-1,
%   data(i+1)=-data(i);
%end
samp = 20;
sp_data = zeros(1, Num_data*samp);
for i = 1 : Num_data
   sp_data((i-1)*samp+1:i*samp) = data(i);
end

BT = .5;
t=[-samp:1:samp];
ht = sqrt(pi*2/log(2))*BT/samp*exp(-
(pi^2*2*(BT/samp)^2/log(2))*power(t,2));
psh_sig = conv(sp_data, ht);

% BT/samp=B, the filter 1 bit delay
% Define modulation index, IF frequency and bit duration
ind=0.35;
fIF=2e6;
Ts=1e-6;

gfsk_I = zeros(1, Num_data*samp-2*samp);
gfsk_Q = zeros(1, Num_data*samp-2*samp);
phi = 0;
for i = 1 : Num_data*samp-2*samp,
  phi = phi + psh_sig(i+2*samp);
  gfsk_I(i) =
sqrt(2)*cos(2*pi*fIF*rem(i,samp)/samp*Ts+ind*pi*phi/samp);
  gfsk_Q(i) =
sqrt(2)*sin(2*pi*fIF*rem(i,samp)/samp*Ts+ind*pi*phi/samp);
end

% Add white noise, define Eb/N
EbN=15;
```

```
sigma=sqrt(samp/2/power(10,(EbN/10)));
sigma=0;
Nn=length(gfsk_I);
No_I=randn(1, Nn)*sigma;
No_Q=randn(1, Nn)*sigma;

% IF bandpass filter, and filtering the noise
order=8;
rip=0.5;
BW_s=600e3;
wbp=[(fIF-BW_s)/(samp/2/Ts),(fIF+BW_s)/(samp/2/Ts)];
%wbp=BW_s/(samp/2/Ts);
%[BB,AB]=cheby1(order,0.3,wbp);
%wbp_s=[(fIF-
720e3)/(samp/2/Ts),(fIF+520e3)/(samp/2/Ts)];%for chebyshev
[BBS,ABS]=butter(order,wbp);
%[BBS,ABS]=cheby1(order,rip,wbp_s);

% Let the noise go through the filter
Nk_I=filter(BBS,ABS,No_I);
Nk_Q=filter(BBS,ABS,No_Q);

% Let the signal go through the filter
%rk_I=filter(BBS,ABS,gfsk_I+No_I);
%rk_Q=filter(BBS,ABS,gfsk_Q+No_Q);
r_I=6*filter(BBS,ABS,gfsk_I+No_I);
r_Q=6*filter(BBS,ABS,gfsk_Q+No_Q);

%Nppp=length(rk_I);
%for k=1:Nppp,
%   if rk_I(k)>1
%      r_I(k)=1;
%   elseif rk_I(k)<-1
%     r_I(k)=-1;
%   else r_I(k)=rk_I(k);
%   end
%   if rk_Q(k)>1
%      r_Q(k)=1;
%   elseif rk_Q(k)<-1
%      r_Q(k)=-1;
%   else r_Q(k)=rk_Q(k);
%   end
%end
ind_I=find(r_I>1);
r_I(ind_I)=1;
```

```
ind_I=find(r_I<-1);
r_I(ind_I)=-1;
ind_Q=find(r_Q>1);
r_Q(ind_Q)=1;
ind_Q=find(r_Q<-1);
r_Q(ind_Q)=-1;


%r_I=sign(Nk_I+gfsk_I);
%r_Q=sign(Nk_Q+gfsk_Q);

%r_I=sign(rk_I);
%r_Q=sign(rk_Q);

Nr=length(r_I);
%rk_IQ=zeros(1,Nr-1);
%rk_QI=zeros(1,Nr-1);
rkt_QI=zeros(1,Nr);
rkt_IQ=zeros(1,Nr);

%rk_QI=r_Q(1:(Nr-1)).*diff(r_I);
%rk_IQ=r_I(1:(Nr-1)).*diff(r_Q);

BD=0.39*[1 -1];
AD=[1 0.2];

d_I=(filter(BD, AD, r_I));
d_Q=(filter(BD, AD, r_Q));
rkt_QI=r_Q.*d_I;
rkt_IQ=r_I.*d_Q;

%sko=-rk_QI+rk_IQ;
skto=-rkt_QI+rkt_IQ;
% Lowpass filter
wlp=(600e3)/(samp/2/Ts);%(600e3)/(samp/2/Ts);
[BL,AL]=butter(4,wlp);
skt=filter(BL,AL,skto)-0.12998;%0.095195;%-0.032448;%-
0.12993;
%skt=filter(BL,AL,skto)-0.2517;
syn=120;%4th order%118;%89;%2nd order%93;%3rd order%111;
%syn=108;

for i=1:Num_data-11,
   ns=syn+(i-1)*20;
   nd=syn+i*samp;
```

```
   if sum(skt(ns+2:3:nd))>0
   %if skt(nd)>0
     Dr(i)=1;
   else Dr(i)=-1;
   end
end

Ds=data(6:Num_data-6);
De=Dr-Ds;
err=find(De);
BER=(length(err))/(Num_data-11)*100
[np f]=psd(Nk_I, 8192, samp/Ts);
[sp f]=psd(gfsk_I, 8192, samp/Ts);
snr=10*log10(sum(sp)/sum(np))
```

APPENDIX B

SYSTEMVIEW SIMULATION SETUP FOR THE 802.11B RECEIVER

Fig. B.1 shows the SystemView simulation setup for the 802.11b non-coherent detector. The functionality of each block is described in Table B.1.

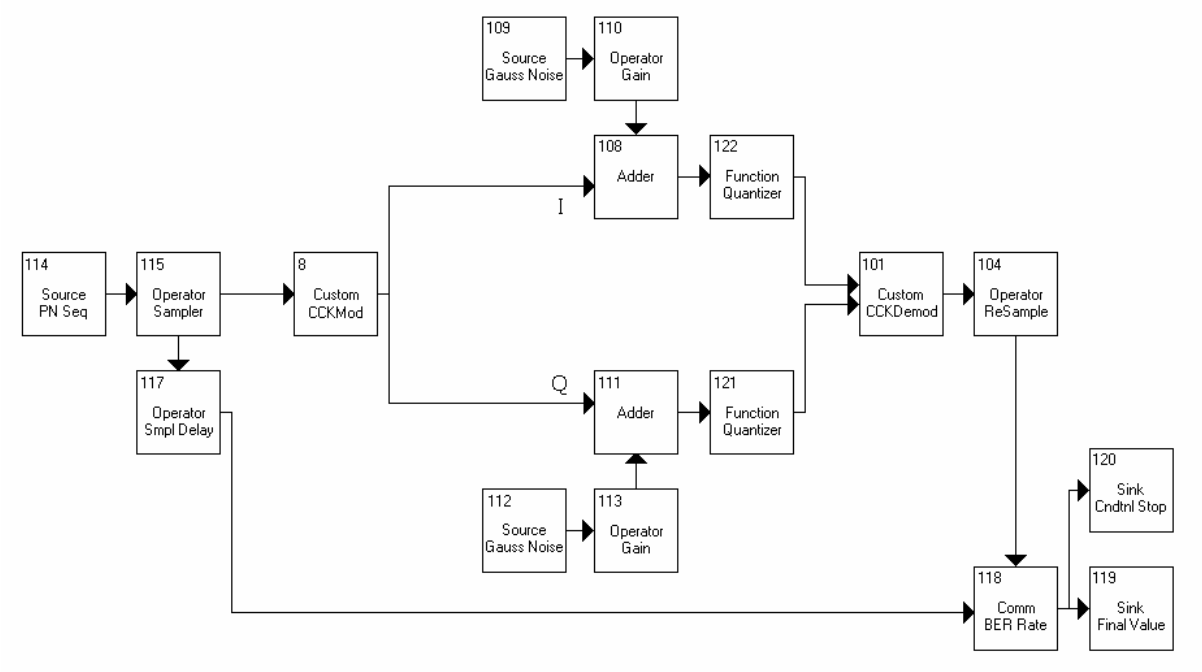

Figure B.1

Token #	Description
114	Random bit sequence generator.
115, 104	Samplers of the input an output bit sequences (respectively) at the specified data rate for each modulation format (1, 2, 5.5 and 11 Mbps).
8	Modulator. Each modulation format has its own modulator block which takes the input bit stream at the specified rate (1, 2, 5.5 or 11Mbps) and creates an 11Mbps modulated output according to the coding and modulation described in table 1.
101	Demodulator. Each modulation format has its own demodulator block which takes an input sample stream at 11Msps and converts it into an output bit stream at the specified bit rate (1, 2, 5.5 or 11Mbps).

109,112	Gaussian uncorrelated noise sources with fixed standard deviation of 1.
110, 113	Variable gain blocks used to change the SNR at every loop of the simulation program (by attenuating the noise).
108, 111	Simple adders
117	Delay for input/output bit stream synchronization.
118	BER computation (compares input and output bit streams)
119	Keeps record of the final BER after each loop of the program
120	Makes the program jump to the next loop after a specified quantity of bit errors has been found.

Table 1.B

Since the amplitude of the signal at each branch (I and Q) is normalized to 1 and the standard deviation of each of the uncorrelated Gaussian noise sources is fixed to 1, then the Eb/No (SNR) is given directly by the attenuation factor applied to the noise by the variable gain blocks (tokens 110 and 113).

During each loop of the program the attenuation factor of tokens 110 and 113 is kept constant. After the specified number of bits has gone through or a specified number of errors has occurred (whatever happens first) the program stops, reports the computed BER and jumps to the next loop in which a different (usually larger) attenuation factor is used.

For the plot shown in Fig B.2, points were taken every 0.5 dB of SNR. To optimize speed and accuracy, for every group of 3 or 4 points, different settings for the number of bits and expected bit errors were used. For a relatively accurate estimation of the BER below 1E-5 simulations using streams of more than 1E7 random bits were required.

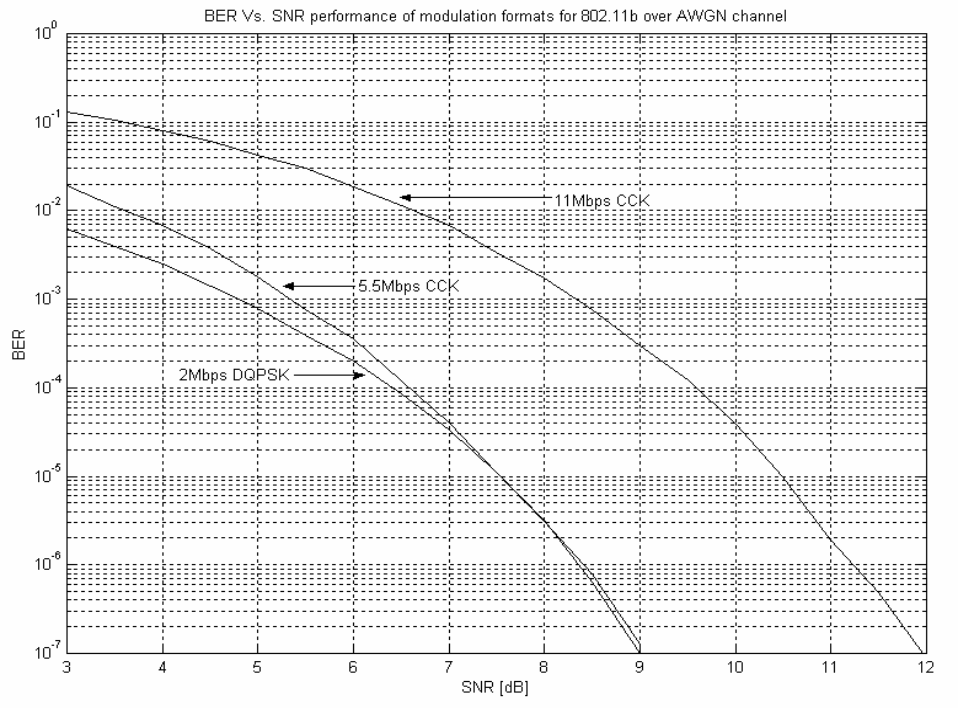

Figure 2

According to these results, an SNR of 10.5 is required to achieve 10E-5 BER at 11Mbps which translates to a FER of 8E-2 (802.11b specification) for frames comprising 1000 octets.

Fig B.3 shows a BER plot to observe the effect of adding a 6 bits quantization (number of bits proposed for our 802.11b system design) before the demodulator.

Fig B.4 shows a more detailed plot showing the specific SNR degradation involved in the addition of 5, 6 or 7 bits of quantization around the required BER (1E-5).

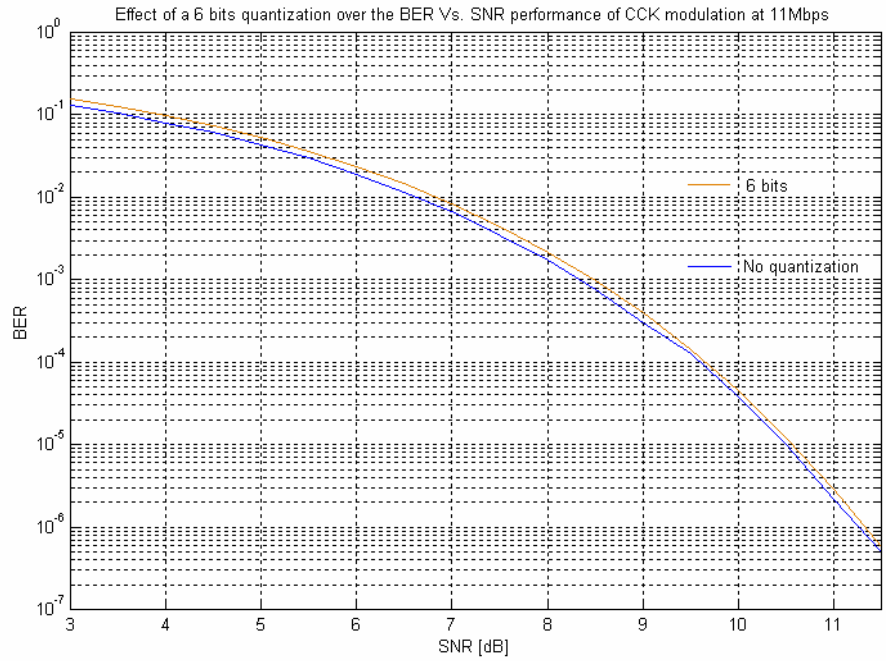

Figure B.3 BER performance of the 802.11b data detector with and without quantization

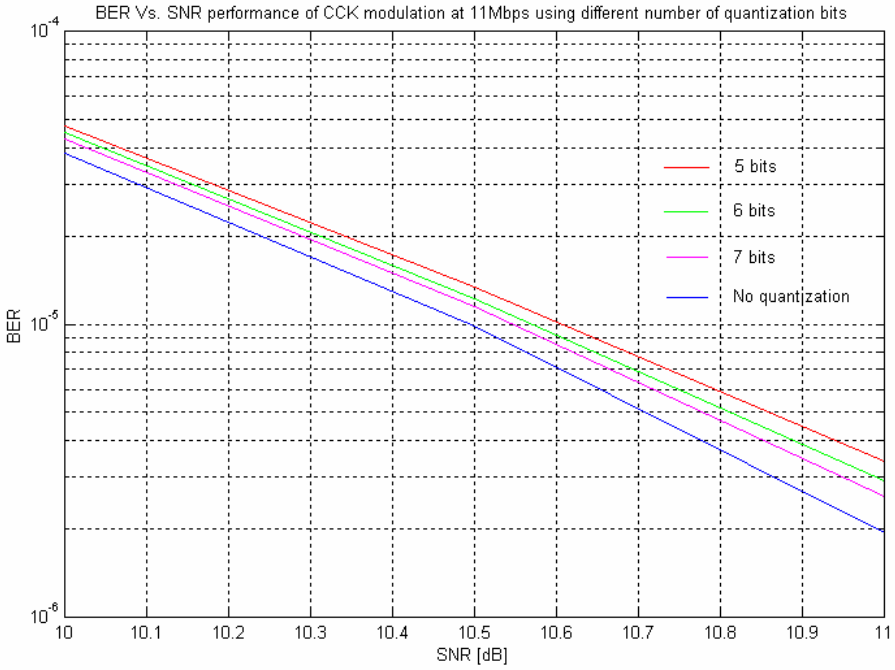

Figure B.4 The effect of quantization on 802.11b data detector BER performance

APPENDIX C

MDAC MODEL FOR ADC SYSTEM SIMULATION

```
function out = funcslew(u)
%
% Models the op-amp slew rate for a discrete time integrator
%
% in:   input signal amplitude
% alfa: effect of finite gain (ideal op-amp alfa=1)
% sr:   slew rate in V/s
% GBW:  gain-bandwidth product of the integrator in Hz
% Ts:   sample time
%
% out:  output signal amplitude
Vin=u(1);
dcode=u(2);
Vref=u(3);
A=u(4);
GBW=u(5);
Ts=u(6);
mserr=u(7); %mismatch error
sr=u(8);
f=u(9);


tau=1/(2*pi*GBW);% Time constant of the integrator
Tmax = Ts/2;
alfa=(1+(A*f)^-1)^-1;
if (dcode==0)
   in=(2+mserr)*Vin+(1+mserr)*Vref;
elseif(dcode==1)
   in=(2+mserr)*Vin;
else
  in=(2+mserr)*Vin-(1+mserr)*Vref;
end

slope=alfa*abs(in)/tau;
if slope > sr        % Op-amp in slewing
   tsl = abs(in)*alfa/sr - tau;  % Slewing time
   if tsl >= Tmax
  error = abs(in) - sr*Tmax;
   else
      texp = Tmax - tsl;
      error = abs(in)*(1-alfa) + (alfa*abs(in) - sr*tsl) * exp(-
texp/tau);
   end

else              % Op-amp in linear region
   texp = Tmax;
   error = abs(in)*(1-alfa) + alfa*abs(in) * exp(-texp/tau);
end
```

VITA

Bo Xia received his bachelor degree in electrical engineering from Shanghai Jiao Tong University in July, 1997. Between September 1997 to August 1998, Mr. Xia worked as an engineer at Hewlett Packard Co., Ltd., China. Since September 1998, Mr. Xia has been studying towards his Ph.D. under the advisory of Dr. Edgar Sánchez-Sinencio in the Analog and Mixed-Signal Center, Texas A&M University. His major research interests focuses on the wireless receiver system and baseband circuitry design. In the past a few years, Mr. Xia has played an important role in many research projects, such as the Bluetooth receiver and 02.11b/Bluetooth dual- mode receiver design, continuous-time Sigma-Delta modulator design for the ADSL system. During the summer of 2002, Mr. Xia took his internship in Agere Systems, Inc, Allentown, Pennsylvania. He worked on the frequency synthesizer for the 802.11b receiver with Agere's radio frequency integrated circuit group there. Mr. Xia is also a co-recipient of the Best Student Paper Award on IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, 2002.

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The typist for this thesis was Bo Xia.