INVESTIGATION OF ANTI-ISLANDING SCHEMES FOR UTILITY INTERCONNECTION OF DISTRIBUTED FUEL CELL POWERED GENERATIONS

A Dissertation

by

CHUTTCHAVAL JERAPUTRA

Submitted to the Office of Graduate Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

December 2004

Major Subject: Electrical Engineering

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ABSTRACT

Investigation of Anti-Islanding Schemes for Utility Interconnection of Distributed Fuel Cell Powered Generations.

(December 2004)

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The rapid emergence of distributed fuel cell powered generations (DFPGs) operating in parallel with utility has brought a number of technical concerns as more DFPGs are connected to utility grid. One of the most challenging problems is known as islanding phenomenon. This situation occurs when a network is disconnected from utility grid and is energized by local DFPGs. It can possibly result in injury to utility personnel arriving to service isolated feeders, equipment damage, and system malfunction.

In response to the concern, this dissertation aims to develop a robust anti-islanding algorithm for utility interconnection of DFPGs. In the first part, digital signal processor (DSP) controlled power electronic converters for utility interconnection of DFPGs are developed. Current control in a direct-quadrature (dq) synchronous frame is proposed. The real and reactive power is controlled by

regulating inverter currents. The proposed digital current control in a synchronous frame significantly enhances the performance of DFPGs.

In the second part, the robust anti-islanding algorithm for utility interconnection of a DFPG is developed. The power control algorithm is proposed based on analysis of a real and reactive power mismatch. It continuously perturbs (±5%) the reactive power supplied by the DFPG while monitoring the voltage and frequency. If islanding were to occur, a measurable frequency deviation would take place, upon which the real power of the DFPG is further reduced to 80%; a drop in voltage positively confirms islanding. This method is shown to be robust and reliable.

In the third part, an improved anti-islanding algorithm for utility interconnection of multiple DFPGs is presented. The cross correlation method is proposed and implemented in conjunction with the power control algorithm. It calculates the cross correlation index of a rate of change of the frequency deviation and (±5%) the reactive power. If this index increases above 50%, the chance of islanding is high. The algorithm initiates (±10%) the reactive power and continues to calculate the correlation index. If the index exceeds 80%, islanding is now confirmed. The proposed method is robust and capable of detecting islanding in the presence of several DFPGs independently operating.

Analysis, simulation and experimental results are presented and discussed.

To My Family

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CHAPTER I

INTRODUCTION

1.1 Introduction

Recent developments in fuel technology have contributed to lower cost and better performance of fuel cell stacks [1]. With these positive gains and deregulation as a driving force, the result has been a rapidly increasing number of non utility owned distributed fuel cell powered generations (DFPGs) operating in parallel with utility. Fig. 1.1 shows the typical configuration of a DFPG connected to utility grid [2]. Fuel cells typically generate low output voltage (current). They can be interfaced to utility grid by means of power electronic converters. Use of DFPGs integrated to utility can provide numerous benefits to both utilities as well as customers [3-5]. In utility perspectives, some of the apparent advantages include distribution and transmission capacity relief, load peak shaving, deferral of high cost transmission and distribution (T&D) system upgrades, etc. Utility customers also gain benefits from efficient use of energy from combined heat and power (CHP), enhanced power quality and reliability, tax incentives, etc.

Despite the benefits gained as described, synchronization of DFPGs with utility can cause many serious technical issues that are currently discussed and addressed in the IEEE Std 929-2000 [6] and the IEEE Std. 1547 [7-8]. One of the most serious issues

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The journal model for this dissertation is *IEEE Transactions on Power Electronics.*

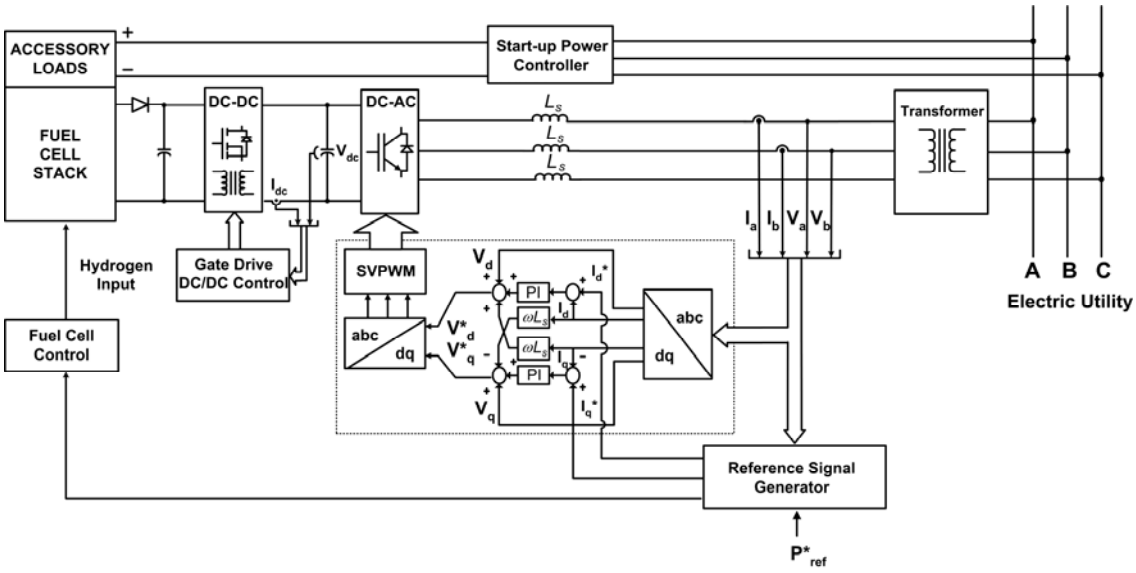


Fig. 1.1 Fuel cell power conditioner control system for supplying power to the utility (utility interface)

is islanding phenomenon. Islanding phenomenon is a situation in which a portion of the distribution system is intentionally or accidentally isolated from the utility grid. It is energized by local power generations without control and/or supervision of utility. This phenomenon can result in a number of potential hazards [9-11].

- Maintenance personnel may be harmed when arriving to service the energized isolated feeder.
- Utility customer equipment may be damaged due to uncontrolled voltage and frequency excursion.
- Switching and measuring devices may be damaged due to unsynchronized reclosure.
- Automatic reclosing devices may malfunction.

As a result, this dissertation proposes a robust anti-islanding algorithm for utility interconnection of DFPGs. The proposed algorithm is highly effective in detecting islanding in the presence of a number of DFPGs which are independently operating. Furthermore, it is capable of eliminating a so called "non-detection zone" (NDZ) without causing significant implications to utility.

1.2 Review of Islanding Detection

Several islanding detection methods have been developed [9-21]. They can be organized into three major categories such as passive, active, and other methods. Their principles, strengths and weaknesses are detailed in the following sections.

1.2.1 Passive Method

The principle of the passive method is to monitor selected system variables such as the voltage at inverter (DFPG) terminal, the frequency of inverter (DFPG) terminal voltage, and other characteristics. The Passive method does not have influences upon utility grid. If observed parameters are out of set limits, an occurrence of islanding can be confirmed.

1.2.1.1 Over/Under Voltage and Frequency Detection

The principle of the over/under voltage and frequency detection is to monitor the voltage at the inverter (DFPG) terminal and the frequency of the inverter (DFPG) terminal voltage [9-13]. A DFPG must be disconnected to prevent equipment damage

when the voltage or the frequency are out of recommended thresholds ($0.88 \leq V \leq 1.10$ per-unit and $59.3 \leq f \leq 60.5$ Hz) specified by the IEEE Std. 929-2000 [6] or the IEEE Std. 1547-2003 [7].

As the basic over/under voltage and frequency protection described, an occurrence of islanding can be detected concurrently. Fig. 1.2 shows real and reactive power mismatch at the instant utility disconnected. Real and reactive power mismatch is the difference between real and reactive power supplied by the inverter (DFPG) and consumed by the load before utility disconnection expressed as,

$$\Delta P = P_I - P_{Load} \tag{1.1}$$

$$\Delta Q = Q_I - Q_{Load} \tag{1.2}$$

Real and reactive power supplied by the inverter (DFPG) can be expressed as,

$$P_I = V_i I_i \cos(\phi) \tag{1.3}$$

$$Q_I = V_i I_i \sin(\phi) \tag{1.4}$$

where V_i and I_i are root mean square (RMS) values of the voltage at inverter (DFPG) terminal and the inverter (DFPG) current and $\cos(\phi)$ denotes displacement power factor.

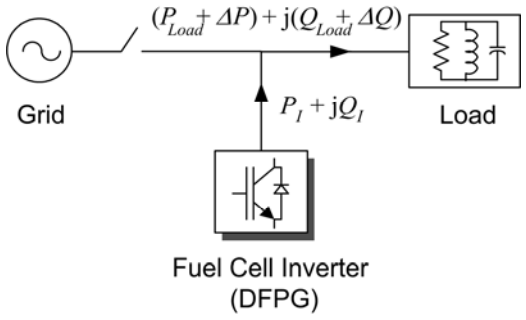


Fig. 1.2 Real and reactive power mismatch at the instant utility disconnected

The load is modeled as parallel RLC components. It is assumed that real power is absorbed by the resistor R and reactive power is consumed by the parallel LC. Real and reactive power of the load can be expressed in a function of voltage and frequency as,

$$P_{Load} = \frac{V_i^2}{R} \tag{1.5}$$

$$Q_{Load} = V_i^2 \left(\frac{1}{\omega \cdot L} - \omega \cdot C \right) \tag{1.6}$$

In the absence of utility, the voltage and the frequency are uncontrolled. Their new operating points must satisfy balances of real and reactive power between the inverter (DFPG) and the load. From (1.1)-(1.6), the following can be concluded.

- If real power mismatch ΔP is positive ($\Delta P > 0$), the inverter (DFPG) terminal voltage will be higher than the system voltage. But, if real power mismatch ΔP is negative ($\Delta P < 0$), the inverter (DFPG) terminal voltage will be lower than the system voltage for vice versa.
- If reactive power mismatch is positive ($\Delta Q > 0$), the frequency will be increased until reactive power supplied by the capacitor C balances with that consumed by the inductor L. However, if reactive power mismatch is negative ($\Delta Q < 0$), the frequency will be decreased for vice versa.

In most cases, real and reactive power mismatch is relatively large ($\Delta P > \pm 20\%$ or $\Delta Q > \pm 5\%$). After utility disconnected, the voltage and the frequency are immediately out of the thresholds confirming islanding.

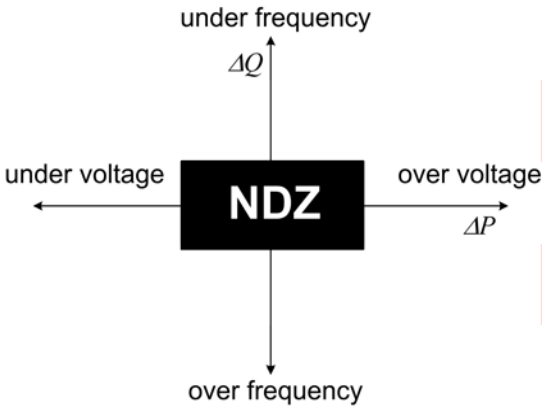


Fig. 1.3 A non-detection zone (NDZ) of over/under voltage and frequency detection method

This method of detection is shown to be simple. However, its principle relies on real and reactive power mismatch at the instant utility disconnected. If both real and reactive power mismatch (ΔP and ΔQ) is small, the voltage and the frequency remain in the thresholds and escape the detection. It is commonly known as a non-detection zone (NDZ) shown in Fig. 1.3. Thus, it is concluded that the over/under voltage and frequency detection method is insufficient for islanding detection.

1.2.1.2 Phase Jump Detection

The principle of the phase jump detection is to monitor the phase difference (sudden phase jump) between phase of the utility voltage and the inverter (DFPG) current [9-13]. In the presence of utility, utility can be assumed as a stiff voltage source providing sinusoidal voltage at system voltage and frequency. While operating as power conditioning, an inverter (DFPG) regulates sinusoidal waveform current

impressed into utility grid. Phase of the inverter (DFPG) current is synchronized with phase of the utility voltage via phase lock loop circuitry (PLL). However, at the instant the utility disconnected, if real and reactive power mismatch is large, phase of the voltage at inverter (DFPG) terminal is instantaneously shifted so as to balance real and reactive power between the inverter (DFPG) and the load. Fig. 1.4 shows lagging phase error ϕ_{err} occurred due to the presence of an inductive load after utility disconnected. If this phase error exceeds the phase threshold ($\phi_{err} > \phi_{th}$), islanding is now confirmed.

This method of detection is shown to be simple. Phase lock loop (PLL) can be implemented by analog circuitry or software using a digital signal processor (DSP). Size of a non-detection zone (NDZ) can be reduced by setting small phase threshold ϕ_{th}. However, too small phase threshold ϕ_{th} can result in nuisance tripping during startup of large induction motors or switching of power factor correction capacitors. The method also fails when power factor of the load is near unity.

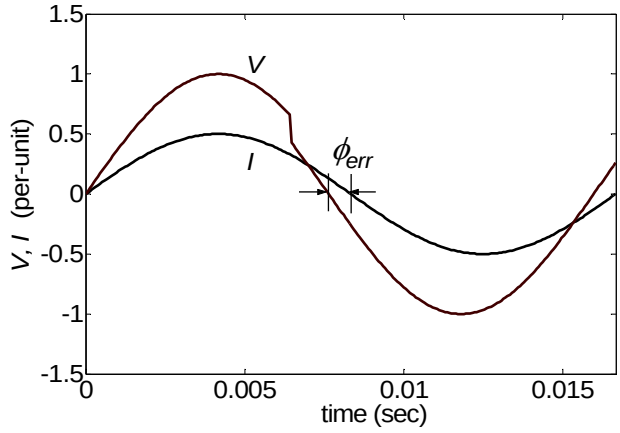


Fig. 1.4 Voltage phase jump after utility is disconnected

1.2.1.3 Voltage Harmonic Detection

The principle of the voltage harmonic distortion detection is to detect total harmonic distortion (THD) of the voltage at inverter (DFPG) terminal [9-13]. In the presence of utility, utility can be considered as a stiff voltage source providing essentially sinusoidal waveform voltage. However, after utility disconnected, voltage harmonic distortion at the point of common coupling (PCC) becomes significant due to interaction between high impedance of islanding loads and harmonic currents from various sources such as inverter (DFPG) itself, nonlinear power electronic load, and nonlinear excitation current of distribution power transformer etc as shown in Fig. 1.5. If the total harmonic distortion (THD) is higher than the threshold, an occurrence of islanding can be confirmed.

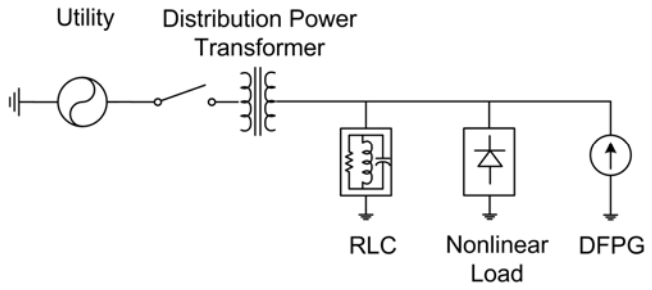


Fig. 1.5 Islanding contains RLC load, nonlinear load, and distribution power transformer

This method of detection is effective to detect islanding because it does not rely on real or reactive power mismatch at the instant utility disconnected. However, the method is more computational involved than other methods. In addition, if a formed islanding load has a high quality load factor ($q = R\sqrt{C/L}$), it could serve as a low pass filter having very low impedance for a wide range of frequency. Thus, it results in low total harmonic distortion (THD < 5%) to appear and it possibly leads to failure of the detection. Furthermore, appropriate harmonic threshold is hard to find, hence rendering this method as impractical [14].

1.2.2 Active Method

The principle of active method is to slightly perturb system variables such as the voltage at inverter (DFPG) terminal and/or the frequency of inverter (DFPG) terminal voltage and simultaneously observing their impacts. Islanding is detected if observed variables are forced out of thresholds.

1.2.2.1 Output Power Variation

The principle of the output power variation method is to periodically vary real power output supplied by an inverter (DFPG) to utility [9, 11, 15]. Islanding is detected, if a change in the voltage at inverter (DFPG) terminal escapes the threshold ($0.88 < V < 1.10$ (per-unit)). Let real power output be expressed in average real power P^0 and real power variation ΔP as,

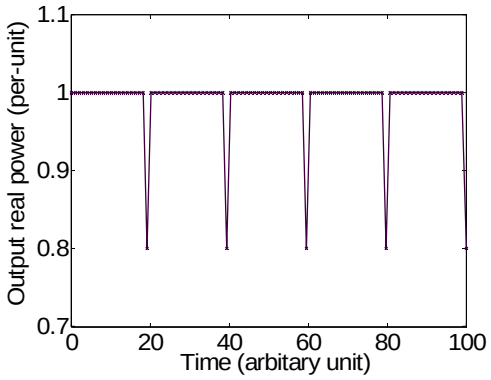
$$P = P^0 + \Delta P \tag{1.7}$$

Voltage variation ΔV is expressed in a function of real power variation ΔP and load real power P_{Load} (see (1.5)) as,

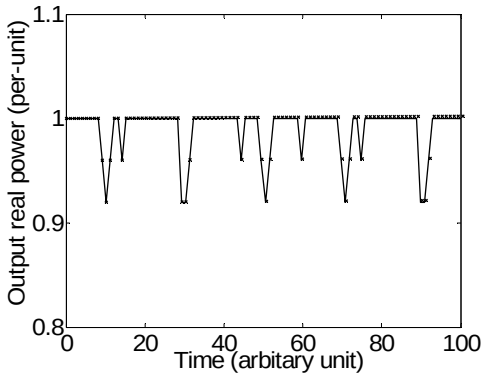
$$\Delta V = \sqrt{\frac{\Delta P}{P_{Load}} + 1} - 1 \tag{1.8}$$

From (1.8), the real power variation ΔP must be set at least ±0.20 (per-unit) so that a change in the voltage at inverter (DFPG) terminal is out of the threshold ($0.88 < V <$ 1.10 (per-unit)) after disconnection of utility, hence confirming an occurrence of islanding.

This method of detection is shown to be robust and capable of reducing size of a non-detection zone (NDZ) to zero when a single inverter (DFPG) is connected to utility. Fig. 1.6 (a) shows the real power output of the inverter (DFPG) while supplying the load. The real power variation ΔP = -0.20 (per-unit) is periodically changed. After utility disconnected, the voltage at inverter (DFPG) terminal is dropped below 0.88 per-unit and islanding is confirmed. But it possibly fails to detect the occurrence of islanding, if multiple inverters (DFPGs) connected to utility are operating independently due to unsynchronized output power variations [9, 11, 15]. Fig. 1.6 (b) shows the real power output from multiple inverters (DFPGs) which are independently operating. It results in inadequate real power mismatch ($\Delta P <$ ±0.20 per-unit) and the voltage at inverter (DFPG) terminals remains within the threshold. This method therefore fails to detect islanding. In addition, large real power variation ΔP by this method causes poor power quality such as voltage flicker and grid instability.



(a) Output real power from a single DFPG



(b) Net real power output from multiple DFPGs while operating independently

Fig. 1.6 Output power variation method

1.2.2.2 Impedance Measurement

The principle of the impedance measurement method is similar to the output power variation method. Real power output is periodically varied while simultaneously determining grid impedance by calculating a rate of change of the voltage at inverter (DFPG) terminal with respect to the inverter (DFPG) current given by (1.9) [9, 11]. Islanding is confirmed, if a significant increase in grid impedance above the threshold is observed.

$$Z = \frac{\Delta V}{\Delta I} \tag{1.9}$$

This method has advantages and disadvantages similar to the output power variation method. However, it requires a precise value of grid impedance which may not be known and available, hence causing this method as impractical.

1.2.2.3 Sliding Mode Frequency Shift

The principle of the sliding mode frequency shift method is to force the frequency of inverter (DFPG) output up/down by controlling the starting phase angle of the inverter (DFPG) current [16-18]. Islanding can be confirmed, if the frequency is out of the threshold ($59.3 \leq f \leq 60.5$ Hz). It is suggested that a sinusoidal function should be used to provide phase information for the current which is expressed as,

$$\theta = \theta_{max}\ sin\left(\frac{\pi(f - f_0)}{2(f_{max} - f_0)}\right) \tag{1.10}$$

where θ_{max} is the maximum phase shift corresponding to the maximum frequency f_{max}.

The system frequency is represented by f_0. The function of phase angle (1.10) is plotted associated with various load lines shown in Fig. 1.7. In the presence of utility, it is assumed that the inverter (DFPG) supplies constant real power output and zero reactive power output. After utility disconnected, for an inductive load (load line #1, $I_{l(\phi,1)}$), the frequency is immediately increasing while simultaneously phase of the inverter (DFPG) current is controlled in advanced with respect to the load phase angle. It results to further accelerate the frequency moving out of the unstable region (see Fig. 1.7). When the frequency is higher than the maximum frequency f_{max}, the starting phase

angle is controlled in the opposite direction. It is gradually decreased while the frequency is increasing to seek a new operating frequency. The new operating frequency is found where the starting phase angle equals the load phase angle. At this equilibrium point, the reactive power supplied by the inverter (DFPG) is evenly absorbed by the load. This process occurs in the opposite manner with a capacitive load (load line #2, $I_{l(\phi,2)}$). That is, the frequency and the starting phase angle are decreasing until the starting phase angle matches with the load phase angle.

This method is shown to be highly effective to detect islanding and capable of reducing size of a non-detection zone (NDZ) near to zero. It provides good compromise between effectiveness and output power quality. However, it possibly fails to detect islanding, if the starting phase angle matches with the load phase angle at frequency located within the threshold. It also fails, if a rate of change of the starting phase angle with respect to the frequency is less than that of the load line as shown by $I_{l(\phi,3)}$.

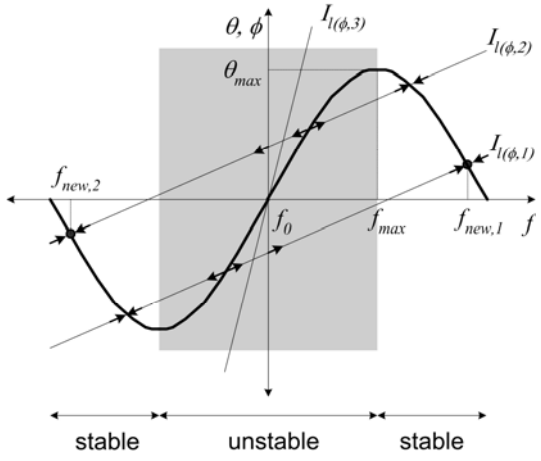


Fig. 1.7 A sinusoidal function of phase angle and load lines

1.2.2.4 Active Frequency Drift

The principle of the active frequency drift method is to force the frequency of inverter (DFPG) output up/down by using positive feedback to accelerate the frequency of the inverter (DFPG) current [9, 11, 19]. Islanding can be confirmed, if the frequency is out of the frequency threshold ($59.3 \leq f \leq 60.5$ Hz). Fig. 1.8 shows the current waveform that implements upward active frequency drift along with its fundamental waveform and utility voltage. With upward active frequency drift, the current waveform is sinusoidal with frequency slightly higher that of a previous positive half cycle. When the inverter (DFPG) current reaches zero, it is held at zero for a chopping fraction T_{cf} until the next zero crossing of utility voltage occurs. Similarly, during a negative half cycle, the current waveform has a negative half of a sinusoidal waveform with frequency higher than that of a previous cycle. When the current waveform approaches zero, it is again held constant at zero for a chopping fraction T_{cf} until the next zero crossing of utility voltage occurs.

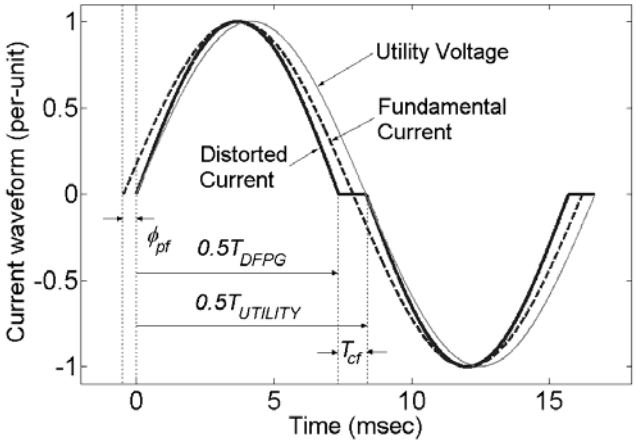


Fig. 1.8 Output current waveform implementing upward active frequency drift

While utility is connected, reactive power output is constantly supplied to utility expressed as,

$$Q_I = V_i I_i \sin(\phi_{pf}) \tag{1.11}$$

where V_i and I_i are RMS values of the voltage at inverter (DFPG) terminal and the inverter (DFPG) current respectively and ϕ_{pf} represents the phase offset due to perturbing the frequency. It is assumed that the load is represented by parallel RLC elements. Reactive power of the load Q_{Load} and reactive power mismatch ΔQ at instant the utility disconnected (see Fig. 1.1) can be expressed as,

$$Q_{Load} = V_i^2 \left(\frac{1}{\omega \cdot L} - \omega \cdot C \right) \tag{1.12}$$

$$\Delta Q = Q_I - Q_{Load} \tag{1.13}$$

From (1.11-1.13), it can be concluded in the following.

- If reactive power mismatch is positive ($\Delta Q > 0$), the frequency will be increasing so that the load can supply more reactive power and eventually the reactive power supplied by the inverter (DFPG) balances with reactive power of the load ($\Delta Q = 0$).
- If reactive power mismatch is negative ($\Delta Q < 0$), the frequency will be decreasing so that the load produces less reactive power and eventually the reactive power supplied by the inverter (DFPG) balances with reactive power of the load ($\Delta Q = 0$).

As a result, if the frequency is drifted up/down out of the frequency threshold ($59.3 < f < 60.5$ Hz), the occurrence of islanding is confirmed. This method of detection

is shown to be highly effective to detect islanding and it can eliminate a non-detection zone (NDZ) near to zero. However, the method fails to detect islanding, if the phase offset generated by perturbing the frequency matches with the load phase angle at frequency within the threshold. In addition, if its use is to be widespread, interventions among them lead to detection failure, unless all inverters (DFPGs) must adopt the same drifting direction.

1.2.2.5 Main Monitoring Units with Allocated All-Pole Switching Devices Connected in Series (MSD)

The principle of the main monitoring units with allocated all-pole switching devices is to employ two separate MSD (Mains Monitoring with Allocated Switching Devices) in cascade to perform self test to ensure reliability of both islanding detection devices [10]. Fig. 1.9 shows a block diagram of design of automatic disconnection devices according to VDE 126 [11]. Allocated all pole switches (SW2) in Fig. 1.9 must be electromechanical devices with load break rating such as relays or magnetic contactors.

Multiple islanding detection methods can be used in both of MSD1 and MSD2 such as the over/under voltage and frequency detection method and the grid impedance measurement method. For the grid impedance measurement method, islanding is confirmed, if there is a sudden change in grid impedance larger than 0.5 ohm ($\Delta Z \geq 0.5\ \Omega$) or grid impedance is higher than 1.25 ohm ($Z > 1.25\Omega$).

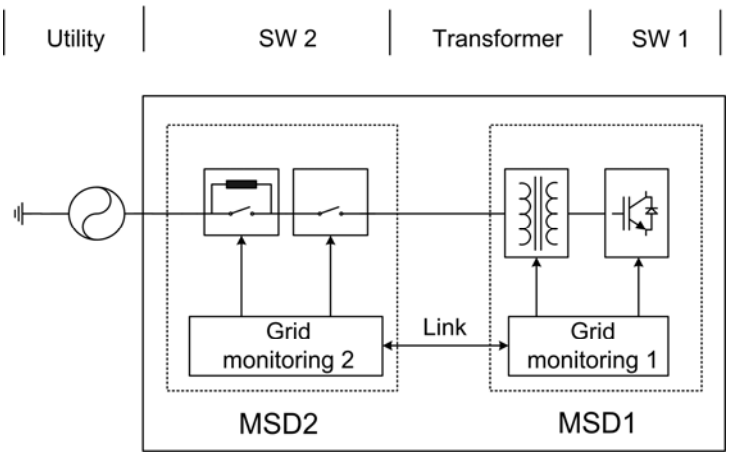


Fig. 1.9 Design of automatic disconnection switch in accordance to VDE 126

This method basically has advantages and disadvantage similar to impedance measurement method. Moreover, with the redundant design and automatic self test capability, reliability of the detection is improved and periodic approval of inverters (DFPGs) requested by DNO (Distributed Network Operator) is not required. But dispensable switches (SW2) in the redundant design add additional cost to inverters (DFPGs).

1.2.3 Other Method

Other method employs different detection techniques than passive or active method as described. They are often implemented at utility level. These detection methods include reactance insertion, power line carrier communication (PLCC) and supervisory control and data acquisition (SCADA).

1.2.3.1 Reactance Insertion

The principle of the reactance insertion is to connect a low-value impedance such as a capacitor bank to a distribution feeder within a short delay time after utility is disconnected as shown in Fig. 1.10 [9, 11]. The capacitor bank supplies additional reactive power to the load and unbalances reactive power between the inverter (DFPG) and the load. If the frequency is below the frequency threshold ($59.3 \leq f \leq 60.5$ Hz), an occurrence of islanding is confirmed.

Other types of impedances such as a low-value resistance can be used to unbalance real power between the inverter (DFPG) and the load during the occurrence of islanding. If a drop in the voltage occurred is below the voltage threshold ($0.88 < V <$ 1.10 per-unit), islanding is positively confirmed.

This method is highly effective to prevent islanding. A non-detection zone (NDZ) can be eliminated, if a capacitor bank is properly installed and coordinated (with additional time delay). But it has a slow response compared to active method. Furthermore, cost of implementation is expensive because every disconnection switch must be equipped with a switchable capacitor bank.

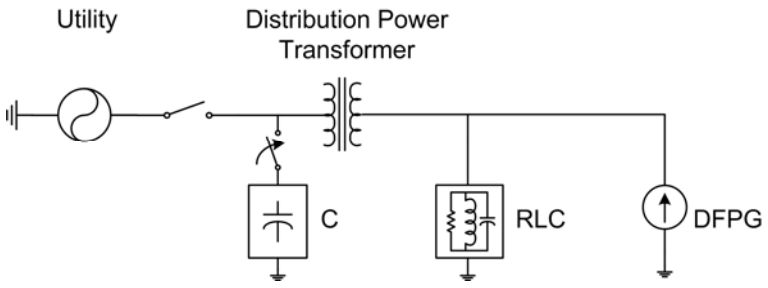


Fig. 1.10 System configuration of reactance insertion method

1.2.3.2 Power Line Carrier Communication

The principle of the power line carrier communication (PLCC) is to use a low energy communication signal sent by a transmitter at utility side throughout power distribution network shown in Fig. 1.11 [9, 21]. Line discontinuity is acknowledged and an occurrence of islanding can be confirmed, if a signal cannot be received by a receiver installed at the inverter (DFPG).

A continuous communication signal is preferred since it is more reliable and simpler than an intermittent signal (discrete or digital signal) for continuity test. With an intermittent signal, loss of the signal due to discontinuity or cessation of the transmission cannot be distinguished without encoding and decoding a signal. In addition, the signal should be low frequency signal (i.e., less than 500 Hz) so that it can propagate well in power line without having troubles with line inductance. A sub-harmonic signal is also preferable because it is not mistakenly produced by customer loads.

Use of power line carrier communication has several advantages. It does not degrade power quality. A non-detection zone (NDZ) can be eliminated. It is unaffected by a number of inverters (DFPGs) connected to utility (high penetration level). Furthermore, with existing automatic meter reading (AMR) system, it is possible to use its signal for this purpose in conjunction with an inexpensive receiver. However, such transmitter is uncommon and expensive. It is economical only in high-density distributed generation areas.

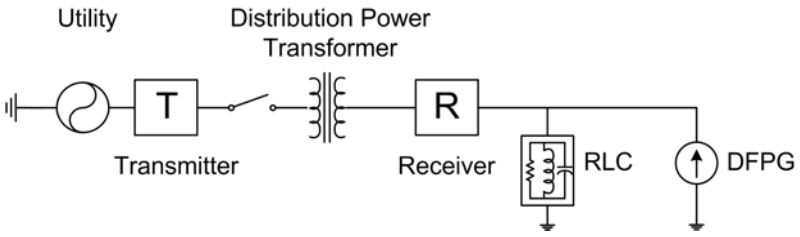


Fig. 1.11 System configuration of power line carrier communication method

1.2.3.3 Supervisory Control and Data Acquisition

The principle of the supervisory control and data acquisition (SCADA) is to monitor states of entire distribution system such as voltage, frequency and other characteristics and enable rapid response to eliminate islanding [9, 11]. When an inverter (DFPG) is installed, a voltage-sensing device must be installed in the local part of utility. Voltage information is sent through communication links to a central station. After utility disconnected, if the voltage can be detected from the disconnected area, the occurrence of islanding is confirmed. Corrective measures must be done to eliminate islanding so that utility personnel are not injured while servicing isolated feeders and out of phase reclosure can be avoided.

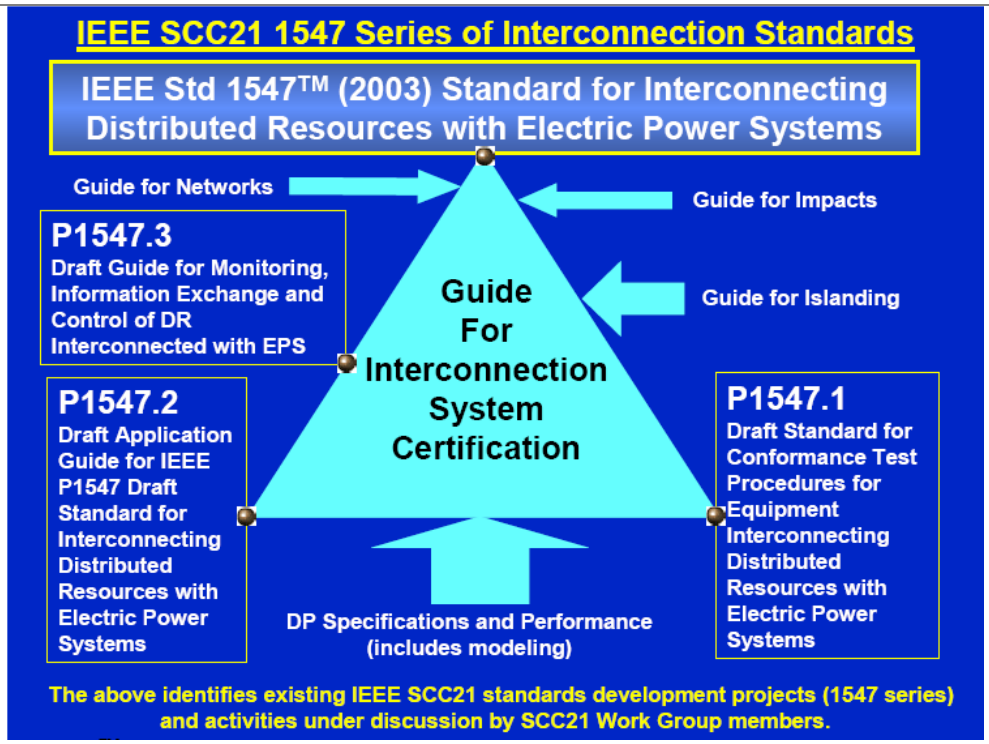
This method is highly effective to detect islanding and a non-detection zone (NDZ) is eliminated, if the system is properly instrumented and controlled. However, cost of implementation is highly expensive because each inverter (DFPG) installed needs separate instrumentation and communication to send necessary information to a central station.

1.3 IEEE Standard 1547

As the interest of use of distributed resources (DR) such as fuel cell (DFPGs) photovoltaic cells, microturbines, energy storages etc operating in parallel to utility is rapidly escalated. It has raised the concerns of having a uniform technical standard for the following reasons – prevent hazards possibly occurred to utility personnel, minimize their impacts on power quality, and avoid conforming to numerous local practices and guidelines.

In response to these concerns, Standard for Interconnecting Distributed Resources (DR) with Electric Power Systems (EPS), IEEE Std. 1547-2003 has been developed by IEEE Standards Coordinating Committee 21 (SCC21). It is the primary interconnection standard that provides system-level technical requirements and specifications needed to interconnect DR with EPS. Other ancillary standards for testing, applications, and communications are now being developed by IEEE work groups as shown in series of interconnection standard in Fig. 1.12.

IEEE Std. 1547-2003 is a uniform standard for interconnection of distributed resources (with aggregate capacity of 10 MVA or less at point of common coupling (PCC)) with EPS as shown in interconnection configuration and definition in Fig. 1.13. It provides requirements relevant to performance, operation, safety consideration, testing, and maintenance of interconnection. Summary of essential interconnection technical specifications and requirements is given in Table 1.1.



IEEE 1547™ (2003) – This standard establishes criteria and requirements for utility interconnection of distributed resources (DR) with electric power systems (EPS)

P1547.1 – This standard specifies the type, production, and commissioning tests that shall be performed to demonstrate that interconnection functions and equipment of a DR conform to IEEE 1547.

P1547.2 – This guide provides technical background and application details to support the understanding of IEEE 1547 Standard for Interconnecting DR with EPS.

P1547.3 – This document provides guidelines for monitoring, information exchange, and control for DR interconnected with EPS

Fig. 1.12 Series of Interconnection Standard IEEE 1547 [20]

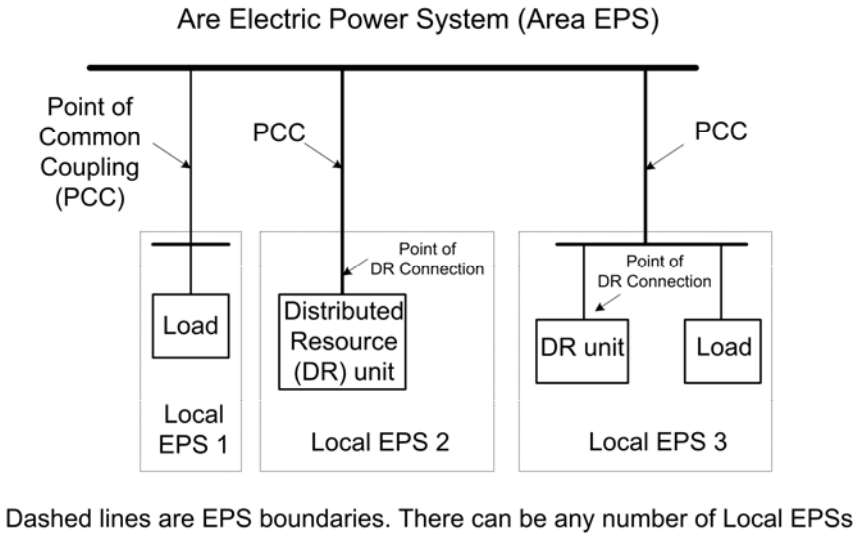


Fig. 1.13 Interconnection configuration and definition

Table 1.1 Technical specifications of IEEE Std. 1547

Specifications	**Descriptions**
Voltage	0.88 – 1.10 per-unit
Frequency	59.3 – 60.5 Hz
Voltage Flicker	Imperceptible, IEEE 519 – 1992 [B5]
DC Injection	Less than 0.5%
Harmonics	TDD < 5% (see Table 1.2)
Islanding	Must be detected within 2 sec.
Synchronization	Must cause voltage fluctuation < 5%
Isolation Device	Upon request of the area EPS
Parallel Device Voltage Rating	Capable of withstanding up to 220% of system rated voltage

Table 1.2 Maximum harmonic current distortion

Individual harmonic order h (odd harmonics)	**h <11**	**11≤ h <17**	**17≤ h <23**	**23≤ h <35**	**h > 35**	**Total demand distortion (TDD)**
Percent (%)	4.0	2.0	1.5	0.6	0.3	5.0

1.4 Research Objective

As discussed in the introduction, safety of utility personnel and equipment is one of the most serious issues associated with islanding phenomenon. Thus, a robust and reliable anti-islanding algorithm is necessary when more and more DFPGs are connected to utility. In response to this concern, this research is focused on investigation and development of a robust anti-islanding algorithm for utility interconnection of DFPGs.

In the first study, DSP controlled power electronic converters for utility interconnection of distributed fuel cell powered generations (DFPGs) are developed. Current control in a synchronous reference frame (dq-frame) utilizing proportional-integral (PI) controllers is proposed. The pulse width modulation (PWM) inverters are fully digitally controlled employing a commercially available digital signal processor (DSP). With a high speed DSP, real time control of digital current control in a synchronous frame, phase lock (PLL), and space vector PWM is realizable by implementing via software. Advantages of the proposed current control are capable of achieving zero steady state error, fast dynamic, and supplying high quality output power to utility. Simulation and experimental results of the three-phase PWM inverter

rated at 10 kW, 208V/60Hz and the single-phase PWM inverter prototype rated at 0.5 kW, 120V/60Hz show excellent performance.

In the second study, the development of the robust anti-islanding algorithm is explored. The power control algorithm is proposed following the analysis of real and reactive power mismatch. The proposed algorithm continuously perturbs ±5% the reactive power supplied by the DFPG while monitoring the utility voltage and frequency. If islanding were to occur, noticeable frequency deviation ($> \pm 1\%$) is observed. To further confirm islanding, the output real power is reduced to 80%. Now, if a drop in voltage is below 0.9 per-unit, islanding is positively confirmed and the DFPG is safely disconnected. This method of detection is shown to be robust, fast acting (operable in one cycle) and significantly reduces the non-detection zone (NDZ) compared to all other detection methods. Several possible islanding conditions are simulated and verified with analysis. Experimental results confirm effectiveness of the proposed algorithm.

In the third study, an improved anti-islanding algorithm for utility interconnection of multiple DFPGs is presented. As shown via analysis, multiple DFPGs independently operating in parallel to utility possibly result the power control algorithm failed to detect islanding due to (±5%) the reactive power average out. Thus, the cross correlation method is proposed and implemented in conjunction with the power control algorithm. While the power control algorithm continuously perturbs (±5%) the reactive power supplied by the DFPG, the cross correlation index of a rate of change of the frequency deviation $\Delta\omega$ with respect to the (±5%) reactive power is

calculated to confirm an occurrence of islanding. If islanding were to occur, the cross-correlation index is higher than 50%, the proposed algorithm further initiates (±10%) reactive power increase and continues to calculate the correlation index. If the cross correlation index exceeds 80%, the occurrence of islanding is positively confirmed. The proposed method is shown to be robust and capable of detecting the occurrence of islanding in the presence of several DFPGs independently operating in parallel to the same utility grid. The viability of the cross-correlation method is demonstrated by the simulation of multiple inverters (DFPGs) under the worst case islanding condition and the results confirm effectiveness of the proposed method.

1.5 Dissertation Outline

The content of this dissertation is organized in five chapters in the following manner. Chapter I, islanding phenomenon and its associated potential hazards are introduced and presented. Review of islanding detection methods is discussed and provided as a background. Standard related to interconnection of distributed resources (DR) with area of electric power system (EPS) is also presented along with some important specifications and requirements related to this research. Finally, research objectives are presented and discussed.

Chapter II, DSP controlled power electronic converters are developed for utility interconnection of DFPGs. Current control in a synchronous frame (dq-frame) utilizing proportional-integral (PI) controllers is proposed. Analysis and design of the synchronous frame current controller are detailed. DSP implementation combines space

vector pulse width modulation (PWM), phase lock, synchronous frame current control etc. Simulation and experimental results are presented and discussed.

Chapter III, the development of a robust anti islanding algorithm is explored. Analysis of islanding voltage and frequency is shown. The power control anti-islanding algorithm is proposed following the analysis. Several possible islanding conditions are simulated and verified with analysis and experimental results are presented and discussed.

Chapter IV, an improved anti-islanding algorithm for utility interconnection of multiple DFPGs is presented. Analysis of islanding voltage and frequency is shown. The cross correlation method is proposed and used in conjunction with the power control algorithm. Simulation results of multiple DFPGs independently operating in parallel with utility under the worst case islanding condition are presented and discussed.

Chapter V, the contributions of this research in the area of islanding detection is concluded. Finally, some suggestions are also provided for future work.

CHAPTER II

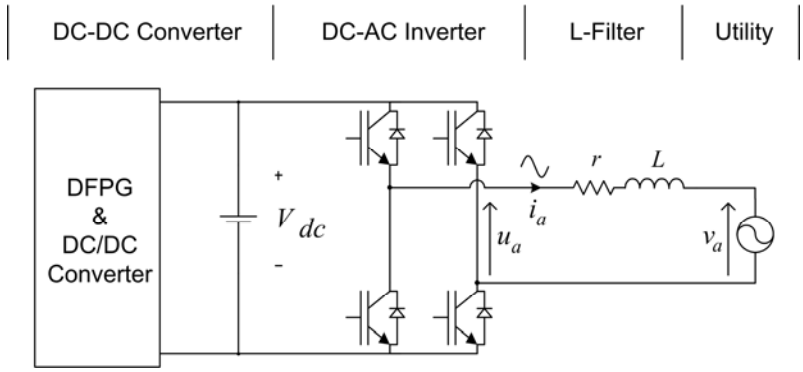
DSP CONTROLLED POWER ELECTRONIC CONVERTERS FOR UTILITY INTERCONNECTION OF DISTRIBUTED FUEL CELL POWERED GENERATIONS

2.1 Introduction

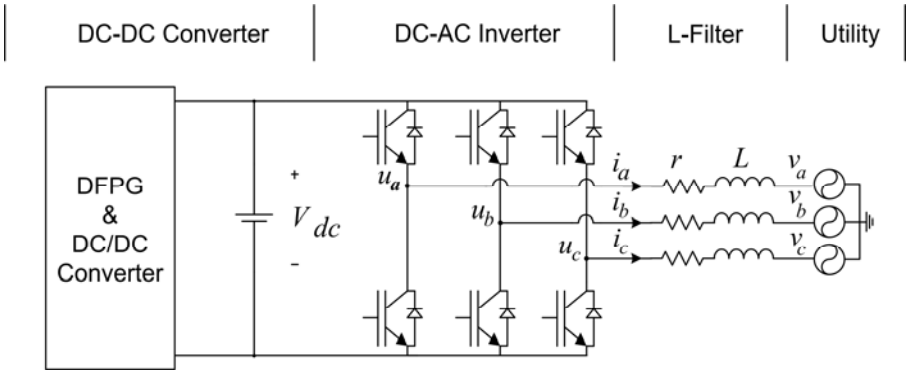
Due to the present high electricity demand, utility deregulation, and market uncertainty, distributed fuel cell powered generations (DFPGs) are considered as a technology of choice providing electricity economically, efficiently and environmentally safely. With their clean performance, high power density and modularity, they are allowed to be sited near to electricity users and supply electricity through existing public utility grid. DFPGs operating in parallel with utility can provide numerous potential benefits such as augmenting capacities of distribution systems, deferring capital investments on distribution and transmission (T&D) systems, and improving power quality and system reliability.

Fuel cells are electrochemical energy conversion devices similar to batteries. They generate variable and low output voltage (current). Thus, they are unable to connect to utility directly. However, they can be interfaced and supply power to utility by means of power electronic converters [22]. Fig. 2.1 show system integration of fuel cell power conditioning system which comprising of a fuel cell stack associated with a dc-dc converter and a widely used DC-AC pulse width modulation (PWM) inverter connected to utility grid. A single phase fuel cell power conditioning system is often

selected for low power applications (< 3 kW) i.e., residential applications. For higher power applications i.e., commercial or industrial applications, a three-phase fuel cell power condition system is preferable.



(a) System integration of single phase fuel cell power conditioning system



(b) System integration of three-phase fuel cell power conditioning system

Fig. 2.1 System integration of fuel cell power conditioning systems

While cost of digital signal processor (DSP) has been drastically decreased since its introduction in 1980's, use of DSP based control of power electronic converters has been gaining popularity [23]. With commercially available high speed DSP core processors, real time control of power electronic converters formerly processed by analog circuitry is now realizable by implementing in software. The advantages of successfully performing these functions are in the followings.

- Performance of power electronic converters is significantly enhanced and less dependent on device technology and environmental variations.
- Cost of power electronic converters is less expensive by mass-production of switching devices embedded with DSP controllers.
- Flexibility and ability to implement advance control algorithms are realizable via programmability.
- High power quality and system reliability can be obtained.

In this chapter, DSP controlled power electronic converters for utility interconnection of DFPGs using commercial DSP are developed. The PWM inverters are controlled in current mode and able to supply high quality output real and reactive power to utility. Current control in a synchronous frame (dq-frame) utilizing proportional-integral (PI) controllers is proposed to ensure sinusoidal waveform current impressed to utility grid. Analysis and design of the PI-controller are discussed. DSP implementation combines space vector pulse width modulation (PWM), phase lock (PLL), closed loop current control etc. Advantages of the proposed current control are capable to achieve zero steady state error, fast dynamic response, and high

quality output power with low current distortion. Simulation and experimental results of the fuel cell based single-phase and three-phase power conditioning systems, employing commercial Texas Instrument DSP TMS320-F243 shows excellent performance.

2.2 DSP Based Control

Implementation of power electronic converters traditionally employs analog control. Lower cost compared to DSP based control is seen as a major advantage in the past. Despite the cost competitiveness, analog control has many drawbacks such as a number of component counts and connections, long-term component instability (aging) and thermal drift. These adverse effects directly degrade performance of converters and cost expensive routine maintenance. In addition, analog control typically is designed specifically for a single converter model. As a result, converter upgrade and scalability are impossible without replacing new hardware.

Currently, price of a single DSP chip is drastically dropped to a few dollars but its performance and capability of executing millions of instructions (MIPS) is significantly increased. Fig. 2.2 shows a block diagram of a DSP controller TMS320-F243 from Texas Instrument. It has a 16 bit fixed-point DSP core which is integrated with several specific peripherals on-chip including – 2 general purpose timers and 8 PWM generators, 3 capture units, 16 channels 10 bit ADC, CAN Interface, SPI, SCI etc. Integration of a high speed DSP core with specific peripherals does not only simplify design process but also offers flexibility via programmability. Thus, advance

control algorithms can be implemented and upgraded by a short period of development time.

With all advantages mentioned above, the DSP based control now becomes preferable to analog counterpart so that higher-performance and lower cost of power electronic converters for utility interconnection application could be realized.

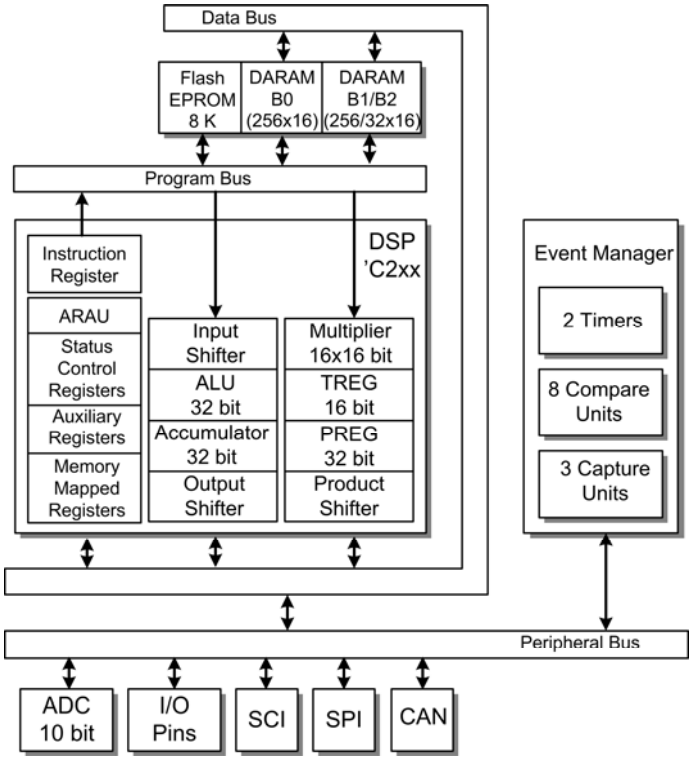
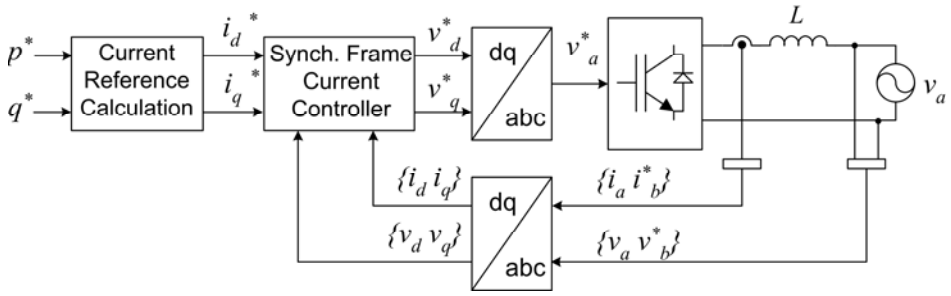


Fig. 2.2 A simplified block diagram of a digital signal processor TMS320-F243

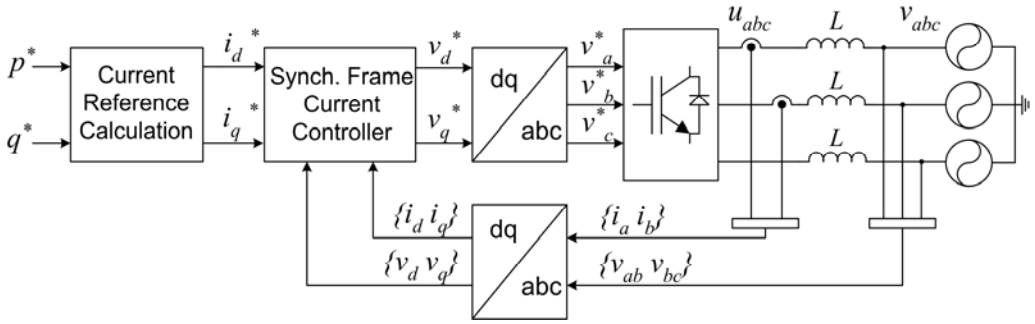
2.3 Control Topology

The objective of power electronic converters for utility interconnection of DFPGs is to supply high quality power output to utility grid. In compliance with the IEEE Std. 929-2000 [6] and the IEEE Std. 1547-2003 [7], the real power output is maintained constant to minimize current and/or voltage harmonic distortion at the point of interconnection and the reactive power output is regulated to zero to achieve power factor near unity. Fig. 2.3 shows the control topology employing synchronous frame current control. DC-AC PWM inverters are operated in current mode. The inverter currents are transformed into a synchronous frame by Park's transformation and regulated in dc-quantity corresponding to the current references $i^*_{\{d,q\}}$. In the following stage, the voltage references in dc-quantities $v^*_{\{d,q\}}$ which being processed by PI controllers are transformed into a stationary frame by the inverse of Park's transformation and utilized as command voltages for generating high frequency pulse width modulated (PWM) voltage ensuring high quality power with low current harmonic distortion supplied to utility.

With the control topology described, fuel cell power conditioning system is capable of supplying sinusoidal waveform current into utility grid. Zero steady state error of inverter current can be achieved [24]. In addition, real and reactive output power can be independently controlled [25], hence resulting power conditioning system furthering capable of providing other ancillary services such as reactive power compensation (voltage support).



(a) Control topology of a single phase PWM inverter



(b) Control topology of a three-phase PWM inverter

Fig. 2.3 Control topology

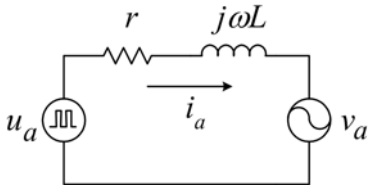
2.4 Proposed Digital Current Control in a Synchronous Frame

In this section, modeling of a single phase and a three-phase PWM inverter and design of synchronous frame current control in discrete time domain based on Root Locus method are detailed.

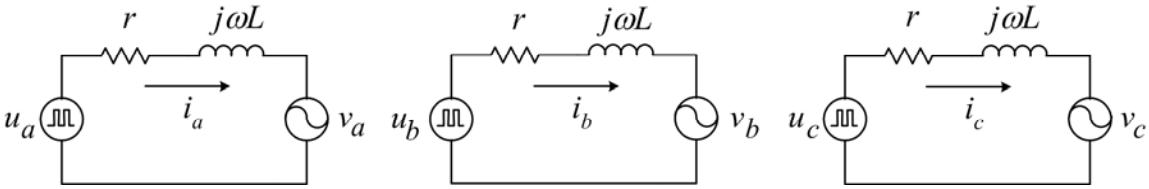
2.4.1 Modeling of PWM Inverters

Fig. 2.4 shows per-phase equivalent circuits of a single-phase and a three-phase PWM inverter. By neglecting high switching frequency components, a DC-AC

PWM inverter can be represented as a sinusoidal voltage source which connects to utility through a L filter [26]. With this configuration, the PWM inverter can be modeled as the first-order system in frequency domain. An input-output transfer function of the PWM inverter in a synchronous frame can be derived by choosing inductor current as a state variable and voltage generated by the PWM inverter as a control input.



(a) Equivalent circuit of a single phase PWM inverter



(b) Equivalent circuit of a three-phase PWM inverter

Fig. 2.4 Per-phase equivalent circuits of DC-AC PWM inverters

2.4.1.1 A Single Phase PWM Inverter

From Fig. 2.4 (a), let the utility voltage v_a and the inverter current i_a be expressed as,

$$v_a = \sqrt{2} \cdot V_{rms} \cdot sin(\omega \cdot t) \tag{2.1}$$

$$i_a = \sqrt{2} \cdot I^*_{rms} \cdot sin(\omega \cdot t + \phi) \tag{2.2}$$

where V_{rms} is a root-mean-square (RMS) value of the utility voltage and I^*_{rms} is a RMS value of the current reference.

The inverter voltage u_a is derived in a function of the inverter current i_a and the utility voltage v_a expressed as,

$$u_a = r \cdot i_a + L\frac{di_a}{dt} + v_a \tag{2.3}$$

In addition to an actual circuit (phase A) of the inverter, a virtual circuit (phase B) operating 90°out of phase with respect to the actual circuit (phase A) is introduced and expressed as,

$$u_b^* = r \cdot i_b^* + L\frac{di_b^*}{dt} + v_b^* \tag{2.4}$$

where

$$v_b^* = \sqrt{2} \cdot V_{rms} \cdot sin(\omega \cdot t + \frac{\pi}{2}) \tag{2.5}$$

$$i_b^* = \sqrt{2} \cdot I^*_{rms} \cdot sin(\omega \cdot t + \frac{\pi}{2} + \phi) \tag{2.6}$$

From (2.1) and (2.2), they are formed into two-phase system and expressed as,

$$\begin{bmatrix} u_a \\ u_b^* \end{bmatrix} = r \cdot \begin{bmatrix} i_a \\ i_b^* \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b^* \end{bmatrix} + \begin{bmatrix} v_a \\ v_b^* \end{bmatrix} \tag{2.7}$$

To find an input-output transfer function (2.7) in a synchronous frame, the system equation (2.7) must be transformed by two-phase Park's transformation $\boldsymbol{S}_{dq}$ expressed as,

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} cos(\omega \cdot t) & -sin(\omega \cdot t) \\ sin(\omega \cdot t) & cos(\omega \cdot t) \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \end{bmatrix} \tag{2.8}$$

or

$$\boldsymbol{v}_{dq} = \boldsymbol{S}_{dq} \cdot \boldsymbol{v}_{ab} \tag{2.9}$$

and its inverse also holds

$$\boldsymbol{v}_{ab} = \boldsymbol{S}_{dq}{}^{-1} \cdot \boldsymbol{v}_{dq} \tag{2.10}$$

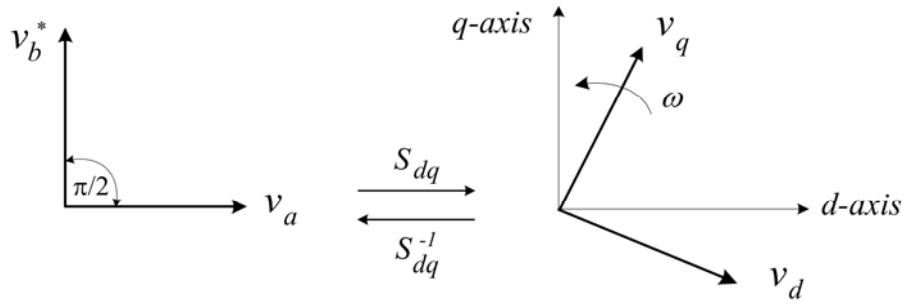


Fig. 2.5 A transformation diagram using two-phase Park's transformation

Fig. 2.5 shows a transformation diagram between a stationary frame and a synchronous frame using two-phase Park's transformation. In a synchronous frame, a direct axis (d-axis) is lagged a quadrature axis (q-axis) by 90°. Since the dq-axis rotates in counter clockwise at the system frequency, voltage and current variables transformed into a synchronous frame become dc-quantity.

Let the system equation (2.7) be transformed to a synchronous frame by two-phase Park's transformation (2.8) expressed as,

$$\boldsymbol{S}_{dq}\begin{bmatrix} u_a \\ u_b \end{bmatrix} = r \cdot \boldsymbol{S}_{dq}\begin{bmatrix} i_a \\ i_b \end{bmatrix} + L\frac{d}{dt}\left(\boldsymbol{S}_{dq}\begin{bmatrix} i_a \\ i_b \end{bmatrix}\right) + \boldsymbol{S}_{dq}\begin{bmatrix} v_a \\ v_b \end{bmatrix} \tag{2.11}$$

Differentiation of the product of Park's transformation and the inverter currents $i_{\{a,b\}}$ is derived by calculus rules as,

$$\boldsymbol{S}_{\boldsymbol{dq}}\begin{bmatrix} u_a \\ u_b \end{bmatrix} = r \cdot \boldsymbol{S}_{\boldsymbol{dq}}\begin{bmatrix} i_a \\ i_b \end{bmatrix} + L \cdot \left(\frac{d\boldsymbol{S}_{\boldsymbol{dq}}}{dt}\begin{bmatrix} i_a \\ i_b \end{bmatrix} + \boldsymbol{S}_{\boldsymbol{dq}}\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \end{bmatrix}\right) + \boldsymbol{S}_{\boldsymbol{dq}}\begin{bmatrix} v_a \\ v_b \end{bmatrix} \tag{2.12}$$

Special care must be used when two-phase Park's transformation is differentiated with respect to time. It further introduces cross coupling voltage between dq-axis. The system equation (2.7) derived in a synchronous frame is expressed as,

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = r \cdot \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \omega L \cdot \begin{bmatrix} -i_q \\ i_d \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} v_d \\ v_q \end{bmatrix} \tag{2.13}$$

By taking Laplace transform both sides of (2.13), it can be represented in frequency domain as

$$\begin{bmatrix} U_d(s) \\ U_q(s) \end{bmatrix} = (sL + r) \cdot \begin{bmatrix} I_d(s) \\ I_q(s) \end{bmatrix} + \omega L \begin{bmatrix} -I_q(s) \\ I_d(s) \end{bmatrix} + \begin{bmatrix} V_d(s) \\ V_q(s) \end{bmatrix} \tag{2.14}$$

The input-output transfer function block diagram of a single phase PWM inverter in a synchronous frame derived in (2.14) is shown in Fig 2.6. It is shown that the inverter model is the first order system as represented by *G(s)* (2.15). Furthermore, cross coupling terms $-\omega L i_d$ and $\omega L i_q$ resulting from the differentiation of Park's transformation form feedback loop between dq-axis.

$$G(s) = \frac{1}{sL + r} \tag{2.15}$$

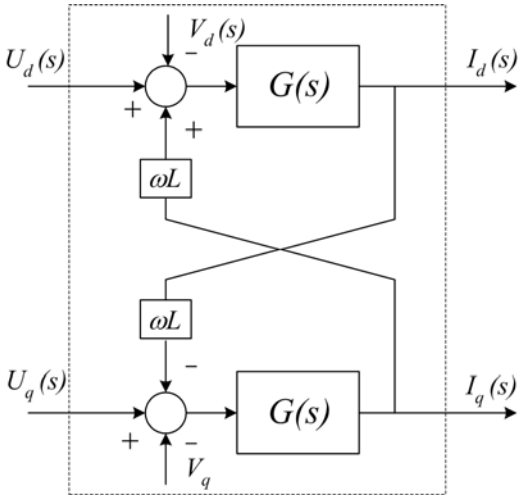


Fig. 2.6 A transfer function block diagram of a single phase PWM inverter in a synchronous frame

2.4.1.2 A Three-Phase PWM Inverter

From Fig. 2.4 (b), let the utility voltage $v_{\{a,b,c\}}$ and the inverter current $i_{\{a,b,c\}}$ be expressed as,

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \sqrt{2} \cdot V_{rms} \cdot \begin{bmatrix} sin(\omega \cdot t) \\ sin(\omega \cdot t + \frac{2\pi}{3}) \\ sin(\omega \cdot t - \frac{2\pi}{3}) \end{bmatrix} \tag{2.16}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \sqrt{2} \cdot I^*_{rms} \cdot \begin{bmatrix} sin(\omega \cdot t + \phi) \\ sin(\omega \cdot t + \frac{2\pi}{3} + \phi) \\ sin(\omega \cdot t - \frac{2\pi}{3} + \phi) \end{bmatrix} \tag{2.17}$$

where V_{rms} is a RMS value of the utility voltage and I^*_{rms} is a RMS value of the current reference.

Under balance three-phase voltage condition, a three-phase PWM inverter circuit can be simplified into three per-phase circuits expressed as,

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = r \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.18}$$

The system equation (2.18) is transformed into a synchronous frame by Park transformation $\boldsymbol{T}_{dq0}$ expressed as,

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3} \cdot \begin{bmatrix} cos(\omega \cdot t) & cos(\omega \cdot t + \frac{2\pi}{3}) & cos(\omega \cdot t - \frac{2\pi}{3}) \\ sin(\omega \cdot t) & sin(\omega \cdot t + \frac{2\pi}{3}) & sin(\omega \cdot t - \frac{2\pi}{3}) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.19}$$

or

$$\boldsymbol{v}_{dq0} = \boldsymbol{T}_{dqo} \cdot \boldsymbol{v}_{abc} \tag{2.20}$$

and its inverse also holds

$$\boldsymbol{v}_{abc} = \boldsymbol{T}_{dqo}{}^{-1} \cdot \boldsymbol{v}_{dq0} \tag{2.21}$$

Fig. 2.7 shows a transformation diagram between a stationary frame and a synchronous frame. Balance three-phase voltage and current variables transformed to a synchronous frame rotating at the same frequency as the system frequency becomes dc-quantity. Zero-sequence is zero and it can be neglected.

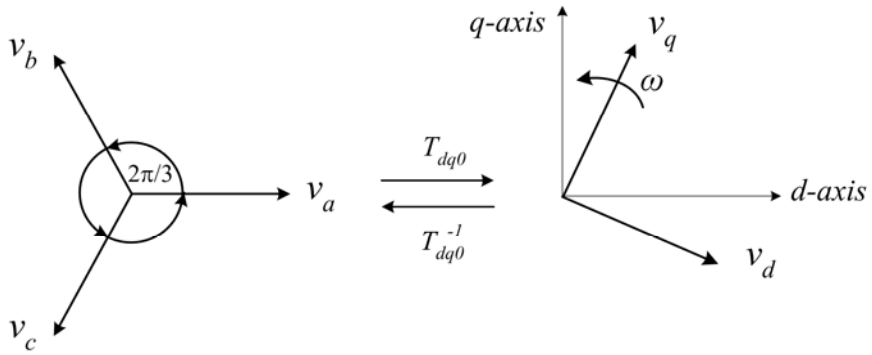


Fig. 2.7 A transformation diagram between a stationary frame and a synchronous frame

Let the system equation (2.18) be transformed to a synchronous frame by Park's transformation and expressed as,

$$\boldsymbol{T}_{dqo}\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = r \cdot \boldsymbol{T}_{dqo}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L\frac{d}{dt}\left(\boldsymbol{T}_{dqo}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}\right) + \boldsymbol{T}_{dqo}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.22}$$

Differentiation of the product of Park's transformation and the inverter currents can be derived in the same manner as (2.11) and {2.12). Thus, the system equation (2.18) is expressed in a synchronous frame as,

$$\begin{bmatrix} u_d \\ u_q \\ u_0 \end{bmatrix} = r\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \omega L\begin{bmatrix} -i_q \\ i_d \\ i_0 \end{bmatrix} + L\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} + \begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} \tag{2.23}$$

By taking Laplace transform both sides of (2.23), the system equation in a synchronous frame (2.23) is derived as,

$$\begin{bmatrix} U_d(s) \\ U_q(s) \\ U_0(s) \end{bmatrix} = (sL + r)\cdot\begin{bmatrix} I_d(s) \\ I_q(s) \\ I_0(s) \end{bmatrix} + \omega L\begin{bmatrix} -I_q(s) \\ I_d(s) \\ I_0(s) \end{bmatrix} + \begin{bmatrix} V_d(s) \\ V_q(s) \\ V_0(s) \end{bmatrix} \tag{2.24}$$

By neglecting zero-sequence, the transfer function of a three-phase PWM inverter (2.24) is identical to that of a single-phase PWM inverter (2.14) which shown in Fig. 2.6.

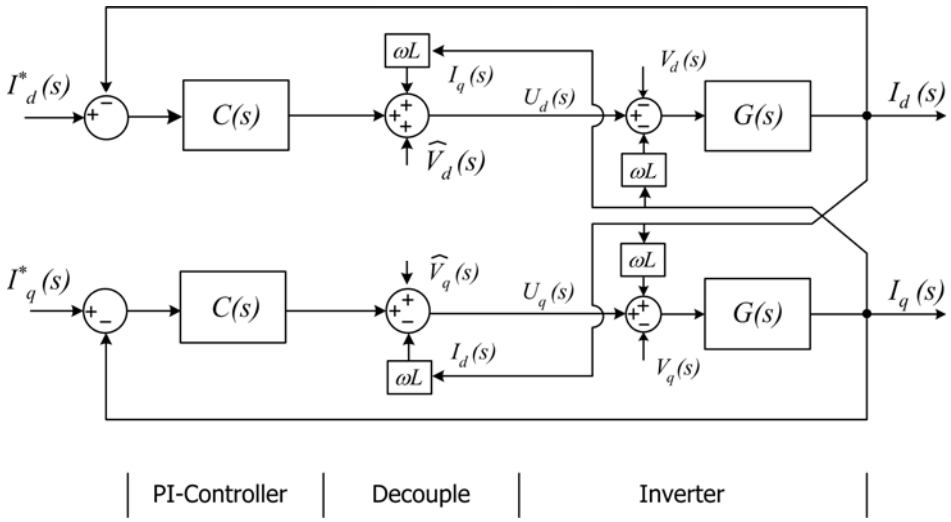
2.4.2 Synchronous Frame Current Control

Fig. 2.8 (a) shows a block diagram of closed loop synchronous frame current control. The inverter currents transformed to a synchronous frame $i_{\{d,q\}}$ are compared

to the current references $i^*_{\{d,q\}}$. The resulting errors are regulated by proportional-integral (PI) controllers. Let the PI controller be expressed as,

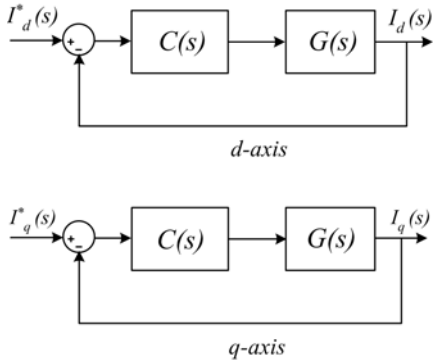
$$C(s) = K_P + \frac{K_I}{s} \tag{2.25}$$

Utility voltage $\hat{v}_{\{d,q\}}$ and decoupled terms $-\omega L i_d$ and $\omega L i_q$ are added in a forward path to cancel effect of the utility and the cross-coupling voltage. Fig. 2.8 (b) shows a simplified block diagram of synchronous frame current control. It is shown that the transfer function of closed loop synchronous frame current control is decoupled and it is identical to both dq-axis.



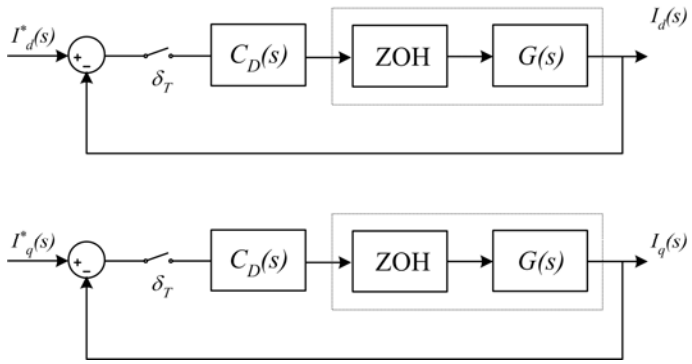
(a) A block diagram of closed loop current control

Fig. 2.8 Synchronous frame current control in frequency domain

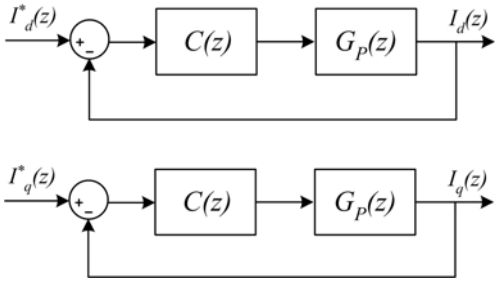


(b) Simplified block diagrams

Fig. 2.8 Continued



(a) A block diagram of closed loop current control in discrete-time domain



(b) An equivalent block diagram

Fig. 2.9 Synchronous frame current control in discrete-time domain

Fig. 2.9 (a) shows discrete-time realization of closed loop current control. The transfer function of a PI controller *C(s)* is transformed to a pulse transfer function $C_D(s)$ and expressed as,

$$C(z) = (K_P + K_I)\left(\frac{z - \frac{K_P}{K_P + K_I}}{z-1}\right) \tag{2.26}$$

Zero order hold (ZOH) is used to represent pulse width modulation (PWM) character of the inverter output voltage. Thus, the transfer function of a DC-AC PWM inverter can be represented by a cascade of the zero order hold (ZOH) and the inverter model (2.15) expressed as,

$$G_P(z) = (1 - z^{-1})Z\left(\frac{G(s)}{s}\right) = \left(\frac{1 - e^{\frac{-rT}{L}}}{r}\right) \cdot \left(\frac{1}{z - e^{\frac{-rT}{L}}}\right) \tag{2.27}$$

The equivalent block diagram of closed loop current control in discrete-time domain is shown in Fig. 2.9(b).

Gain selection of the PI controller can be design and selected based on Root Locus design method. Let the opened loop transfer function of synchronous frame current control be expressed as,

$$C(z) \cdot G_p(z) = (K_P + K_I) \cdot \left(\frac{1 - e^{\frac{-rT}{L}}}{r}\right) \cdot \left(\frac{z - \left(\frac{K_P}{K_P + K_I}\right)}{z^2 - (1 + e^{\frac{-rT}{L}})z + (e^{\frac{-rT}{L}})}\right) \tag{2.28}$$

Let complex closed loop poles in z-plane be selected based on given performance specifications such as settling time T_s and maximum overshoot M_p expressed as,

$$z^* = e^{(-\sigma \pm j\omega_d)\cdot T} \tag{2.29}$$

where damped frequency ω_d and σ are expressed as,

$$\omega_d = \omega_n \sqrt{1-\varsigma^2} \tag{2.30}$$

$$\sigma = \varsigma \cdot \omega_n \tag{2.31}$$

and

$$\omega_n = \frac{4.6}{\varsigma \cdot T_s} \tag{2.32}$$

Fig. 2.10 shows locations of uncompensated poles ($e^{\frac{-rT}{L}}$), zero (z_0) and desirable closed loop pole (z^*). Based on angle condition, the closed loop pole z^* must satisfy the following condition.

$$\angle C(z)\cdot G_p(z) = \pm 180\cdot(2k+1), \quad k = 0,1,2,... \tag{2.33}$$

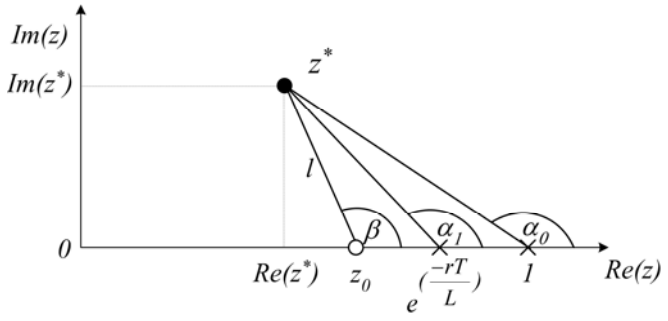


Fig. 2.10 Opened loop poles (×), zero (o), and desirable closed loop pole (z^*)

or (in Fig. 2.10)

$$\beta - (\alpha_0 + \alpha_1) = \pm 180 \cdot (2k+1), \quad k = 0, 1, 2, \ldots \tag{2.34}$$

Thus, zero of the PI controller *C(z)* can be calculated by

$$z_0 = Re\{z^*\} - l\cos(\beta) \tag{2.35}$$

where

$$l = \frac{Im\{z^*\}}{\sin(\beta)} \tag{2.36}$$

β is expressed as,

$$\beta = \alpha_0 + \alpha_1 - \pi \tag{2.37}$$

and

$$\alpha_0 = \pi - \tan^{-1}\left\{\frac{Im(z^*)}{1 - Re(z^*)}\right\} \tag{2.38}$$

$$\alpha_1 = \pi - \tan^{-1}\left\{\frac{Im(z^*)}{e^{(\frac{-rT}{L})} - Re(z^*)}\right\} \tag{2.39}$$

Proportional gain K_P of the PI controller *C(z)* is calculated based on magnitude condition expressed as,

$$\left|C(z) \cdot G_p(z)\right|_{z=z^*} = 1 \tag{2.40}$$

From (2.40), the proportional gain K_P of the PI controller *C(z)* can be selected by

$$K_P = \frac{z_0 \cdot r}{\left(1 - e^{\left(\frac{-rT}{L}\right)}\right)} \cdot \left| \frac{(z-1)\left(z - e^{\left(\frac{-rT}{L}\right)}\right)}{(z - z_0)} \right|_{z=z^*} \tag{2.41}$$

From (2.28) and (2.41), the integral gain of the PI controller is selected by

$$K_I = \frac{(1 - z_0)K_P}{z_0} \tag{2.42}$$

Given system parameters and specifications in Table 2.1, controller gains are selected based on (2.41) and (2.42). Fig. 2.11 shows root locus of the closed loop synchronous frame current control. It is shown that all desirable closed loop poles are located inside a unit circle $\{0.78 \pm j0.18\}$ ensuring stability of the closed loop system. Step response of the closed loop current control is shown in Fig. 2.12. It is shown that the output current reaches the reference with zero steady state error in the specified settling time (20 sampling periods).

Table 2.1 System parameters and selected gains

Parameter	**Value**
Resistance (r)	0.05 Ω
Inductance (L)	1.2 mH
Switching frequency	10.8 kHz
Settling time, T_s	2 ms
Maximum overshoot M_p	20%
Damping ratio ζ	0.707
K_P	7.17
K_I	1.65

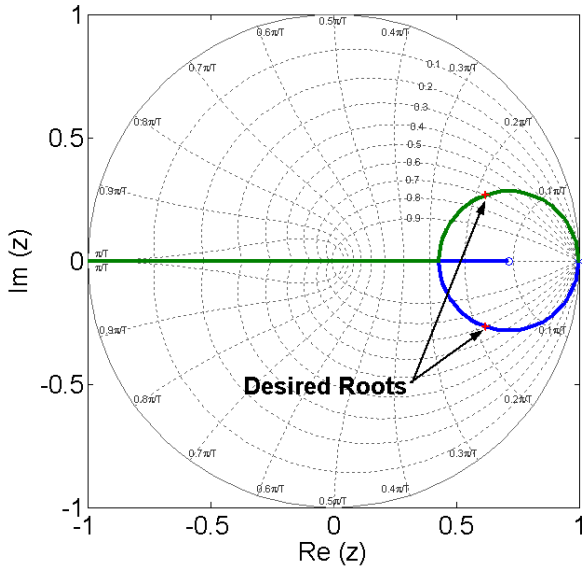


Fig. 2.11 Root locus of closed loop current control

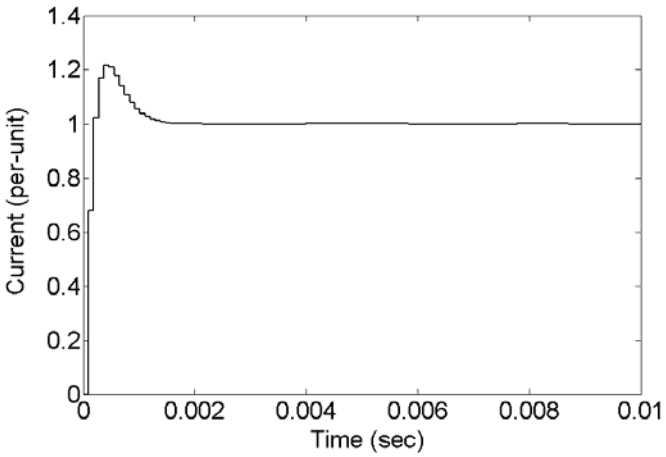


Fig. 2.12 Step response of closed loop current control

2.5 Current Reference Calculation

The function of current reference calculation is to compute the current references corresponding to real and reactive power references. While functioning as

power conditioners, the inverters control constant real power output and zero reactive power output supplied to utility grid. The current references in a synchronous frame $i^*_{\{d,q\}}$ can be expressed in a function of real and reactive power references and utility voltage in a synchronous frame as,

$$\begin{bmatrix} i^*_d \\ i^*_q \end{bmatrix} = k \cdot \begin{bmatrix} v_d & v_q \\ -v_q & v_d \end{bmatrix}^{-1} \cdot \begin{bmatrix} p^* \\ q^* \end{bmatrix} \tag{2.43}$$

where $k = 2$ for a single phase system and $k = 1$ for a three-phase system [25].

From (2.43), under sinusoidal or balance three-phase voltage, the current reference i^*_d is always set to zero to achieve unity power factor. The current reference i^*_q determines real power output supplied to utility. In the presence of distortion or unbalance voltage, a low pass filter is recommended to filter out voltage harmonic before calculating the current references $i^*_{\{d,q\}}$ to further improve power quality.

2.6 Space Vector PWM

Space-vector pulse width modulation (SVPWM) concept is based on space vector representation of PWM inverter output voltage generated from all possible switching states [27]. It is shown to have performance superior to conventional sinusoidal pulse width modulation (SPWM) in many aspects such as better dc-link voltage utilization, lower switching loss, and less switching ripple current. Fundamental and implementations of space vector PWM for both single-phase and three-phase PWM schemes are detailed in the following sections.

2.6.1 Single Phase Space Vector PWM

A single phase PWM inverter consists of two half bridges poles (phase A and B). It typically provides four possible switching states. Of theses, two active states form two active vectors equal in same magnitude to dc-link voltage V_{dc}. The other two states are zero vectors contributing zero output voltage. All four switching states are shown in Fig. 2.13 and their vector representations are mathematically expressed as,

$$\begin{aligned} u_k &= V_{dc}\, exp(jk\pi) \quad ; \text{for } k = 1, 2 \\ u_0 &= 0 \quad ; \text{zero vector} \\ u_3 &= 0 \quad ; \text{zero vector} \end{aligned} \tag{2.44}$$

Let the reference voltage u^* be expressed as,

$$u^* = Re\left\{ \left| u^* \right| exp(j\omega \cdot t) \right\} \tag{2.45}$$

To synthesize the reference voltage u^* from active and zero states, time intervals in active states T_k can be expressed as,

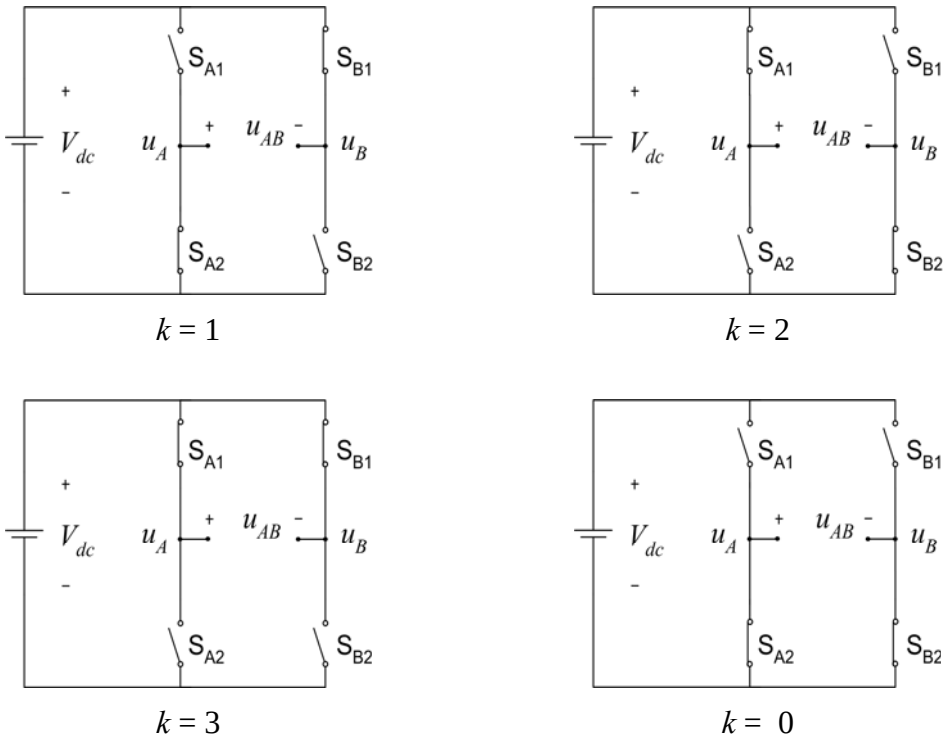
$$T_k = \frac{\left| u^* \right|}{V_{dc}} T \tag{2.46}$$

and the rest of a period is evenly divided to zero states T_0 and T_3

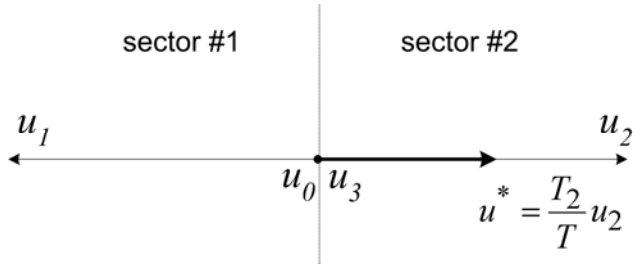
$$T_0 = T_3 = \frac{T - T_k}{2} \tag{2.47}$$

Fig. 2.14 shows switching sequences of symmetrical space vector PWM. For the reference voltage u^* residing in sector #1 (Fig. 2.14 (a)), the sequence starts with the zero state u_0 for $T_0/2$ and transitions to the active state u_1 for the next interval $T_1/2$. After the active state u_1 is completed, the other zero vector is utilized for $T_3/2$ to

complete modulation in a half period. The pattern is reversed to complete the rest of a modulation cycle.

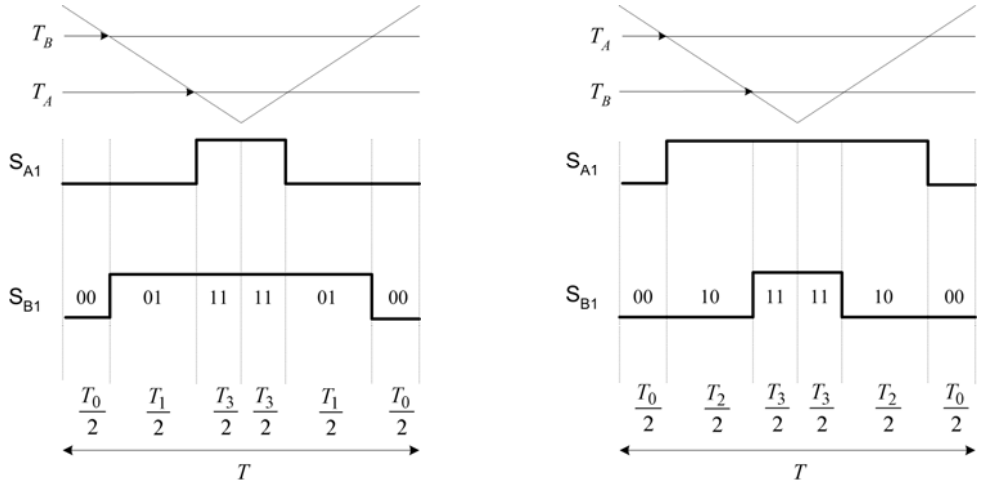


(a) Four switching states of a single phase PWM inverter



(b) Space vector representations of four switching output voltages

Fig. 2.13 Single phase space vector PWM



(a) $k = 1$ (b) $k = 2$

Fig. 2.14 Switching pattern of symmetrical space vector PWM for a single phase PWM inverter

Generation of symmetrical space vector PWM waveform as described can be easily implemented by software using a digital signal processor i.e., TMS320-F243. By configuring a timer counting up/down, appropriate time intervals T_A and T_B are programmed into compare registers and symmetrical space vector PWM outputs can be generated (see section 2.7). Values of compare registers for both sectors are derived and shown in Table 2.2

Table 2.2 Phase/sector compare value settings (single phase space vector PWM)

Phase/Sector	**1**	**2**
Phase A (T_A)	$\frac{(T_0 + T_1)}{2}$	$\frac{T_0}{2}$
Phase B (T_B)	$\frac{T_0}{2}$	$\frac{(T_0 + T_2)}{2}$

2.6.2 Three-Phase Space Vector PWM

A three-phase PWM inverter consists of three half bridge poles (phase *A*, *B* and *C*). This configuration has eight possible switching states (shown in Fig. 2.16) all of which divide a complex plane into equal 6 sectors inscribed by a hexagon as shown in Fig. 2.15. Of these, six of them are active vectors and other two are zero vectors. The active vectors are equal in magnitude ($2/3 \cdot V_{dc}$) but geometrically phase displaced by 60°. On the other hand, zero vectors are located at the center of the hexagon and produce zero output voltage. Mathematical representations of all states are expressed as,

$$\begin{aligned} u_k &= \frac{2}{3} V_{dc}\, exp(\, j(k-1)\frac{\pi}{3}) \quad ; \text{for } k = \{1,\ 2, \ldots, 6\} \\ u_k &= 0 \qquad\qquad\qquad\qquad\quad ; \text{for } k = \{0, 7\} \end{aligned} \tag{2.48}$$

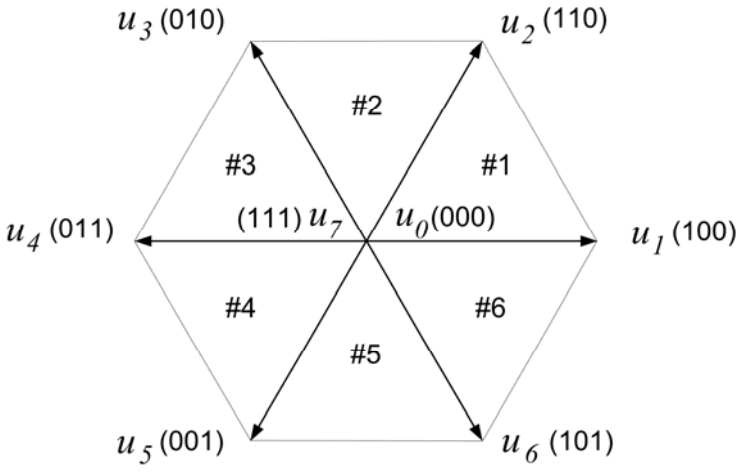
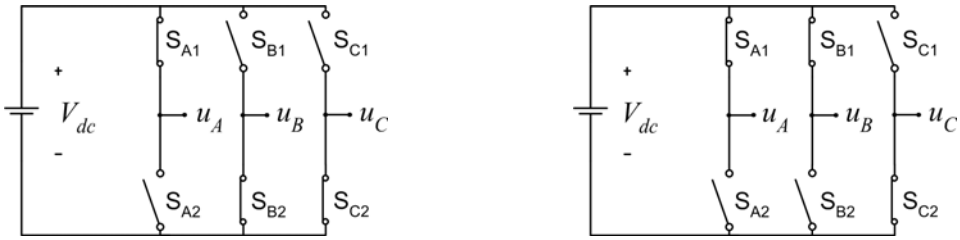
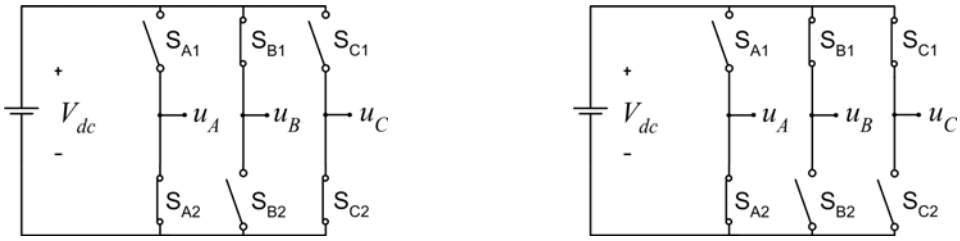


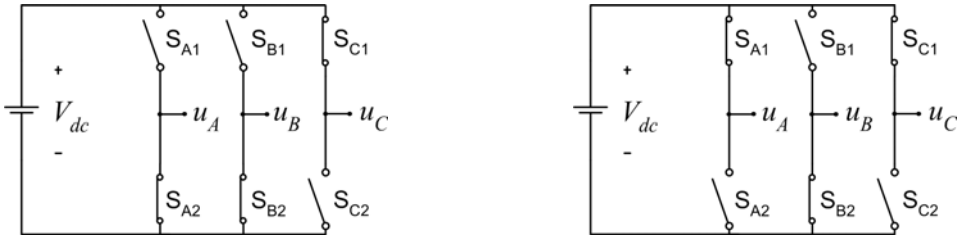
Fig. 2.15 Eight possible switching states form 6 active vectors and two zero vectors



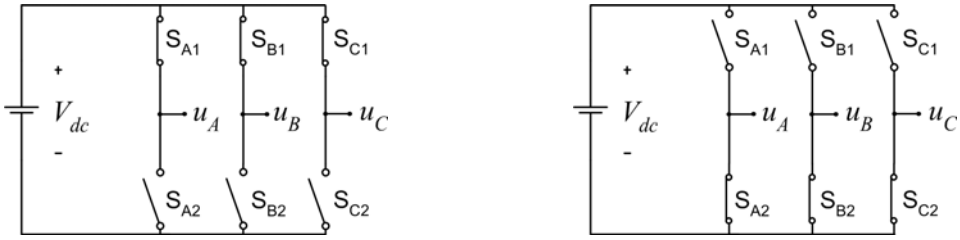
$k = 1$ $k = 2$



$k = 3$ $k = 4$



$k = 5$ $k = 6$



$k = 7$ $k = 0$

Fig. 2.16 Eight switching states of a three-phase PWM inverter

Let balance three-phase voltage reference u^* be transformed to a synchronous frame by Park's Transformation and moves along a circular trajectory expressed as,

$$u^* = \left| u^* \right| \cdot exp(j\omega \cdot t) \tag{2.49}$$

where ω is the system frequency and $\left| u^* \right|$ is expressed as,

$$\left| u^* \right| = \frac{2}{3} \cdot \left[sin(\omega \cdot t) \quad sin(\omega \cdot t + \frac{2\pi}{3}) \quad sin(\omega \cdot t - \frac{2\pi}{3}) \right] \cdot \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{2.50}$$

By means of space-vector PWM, the reference voltage u^* obtained from (2.49) can be synthesized by vector sum of two adjacent active vectors shown in Fig. 2.17. For the voltage reference residing in sector #1, the vector sum of two adjacent active vectors within one switching period can be expressed mathematically as,

$$\bar{u}^* = \frac{T_1}{T} u_1 + \frac{T_2}{T} u_2 \tag{2.51}$$

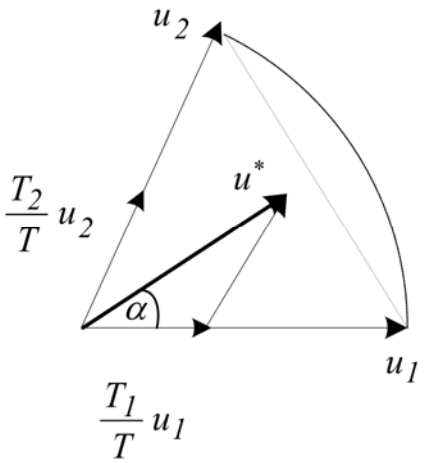


Fig. 2.17 Reference vector and its adjacent vectors

In one switching period T, T_1 and T_2 are time intervals during which vector #1 and #2 are selected respectively. However, if a total time interval ($T_1 + T_2$) is less than switching period T, zero vectors will be utilized. Calculation of time intervals for each vector can be derived by reforming (2.51) into Cartesian coordinate as,

$$\left|\bar{u}^*\right| \cdot \left(\cos\alpha + j\sin\alpha\right) = \frac{T_1}{T}\left|u_1\right| + \frac{T_2}{T}\left|u_2\right| \cdot \left(\cos\frac{\pi}{3} + j\sin\frac{\pi}{3}\right) \tag{2.52}$$

Equating real and imaginary components yield the solutions of

$$T_1 = M \cdot \frac{\sin(\frac{\pi}{3} - \alpha)}{\sin(\frac{\pi}{3})} \cdot T \tag{2.53}$$

$$T_2 = M \cdot \frac{\sin(\alpha)}{\sin(\frac{\pi}{3})} \cdot T \tag{2.54}$$

$$T_0 = T - T_1 - T_2 \tag{2.55}$$

and

$$M = \frac{\left|\bar{u}^*\right|}{\left|u_k\right|} \tag{2.56}$$

Commonly used symmetrical space vector PWM centers active vectors in the first half cycle. Zero vectors are divided evenly between u_0 and u_7 and placed at the beginning and at the end of two consecutive active vectors u_1 and u_2 as shown in Fig. 2.18. The pulse pattern is then reversed for the rest of a switching period until the modulation process is completed. For the voltage reference u^* residing in other sectors, switching time intervals (T_k, and T_{k+1}) corresponding to their adjacent vectors (u_k and

u_{k+1}) can be calculated in the same manner as (2.53)-(2.55). Fig. 2.19 shows switching patterns of symmetrical space vector PWM for all other sectors. To implement symmetrical space vector PWM waveforms by using a DSP such as TMS320-F243, a timer counter is configured up/down counting. Appropriate time intervals T_A, T_B and T_C are programmed into compare registers (see section 2.7). Values of those compare registers for all sectors are derived and shown in Table 2.3

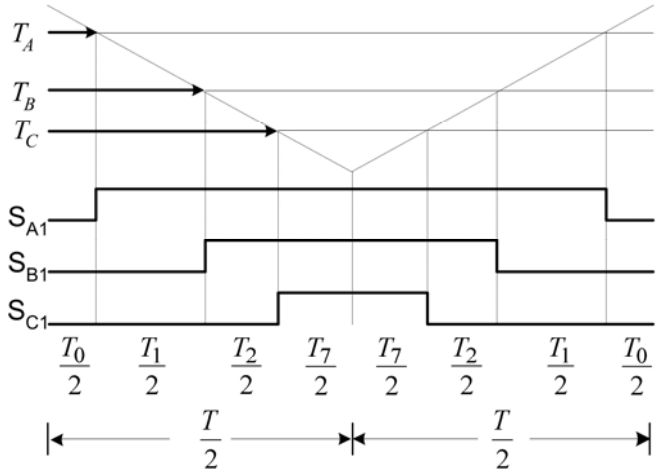
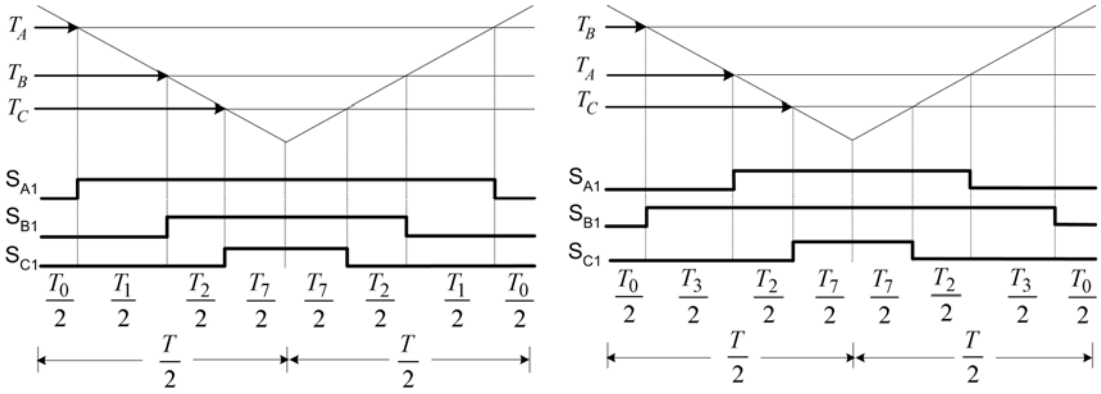


Fig. 2.18 Switching pattern of a symmetrical space vector PWM (k = 1)

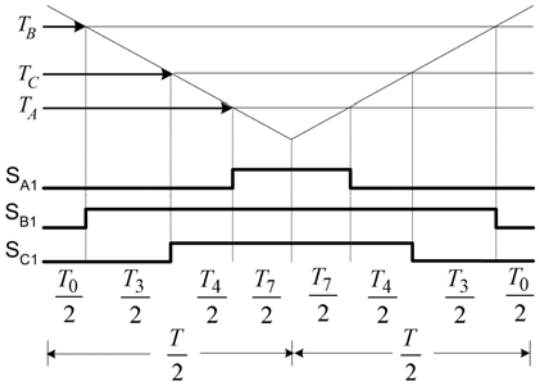
Table 2.3 Phase/sector compare value settings (three-phase space vector PWM)

Phase/Sector	**1**	**2**	**3**	**4**	**5**	**6**
Phase A (T_A)	$\frac{T_0}{2}$	$\frac{(T_0+T_3)}{2}$	$\frac{(T-T_0)}{2}$	$\frac{(T-T_0)}{2}$	$\frac{(T_0+T_5)}{2}$	$\frac{T_0}{2}$
Phase B (T_B)	$\frac{(T_0+T_1)}{2}$	$\frac{T_0}{2}$	$\frac{T_0}{2}$	$\frac{(T_0+T_5)}{2}$	$\frac{(T-T_0)}{2}$	$\frac{(T-T_0)}{2}$
Phase C (T_C)	$\frac{(T-T_0)}{2}$	$\frac{(T-T_0)}{2}$	$\frac{(T_0+T_3)}{2}$	$\frac{T_0}{2}$	$\frac{T_0}{2}$	$\frac{(T_0+T_1)}{2}$

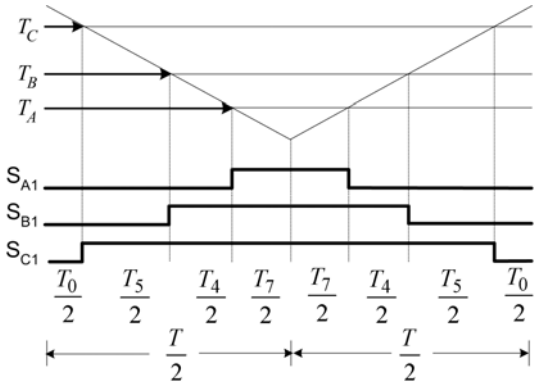


$k = 1$

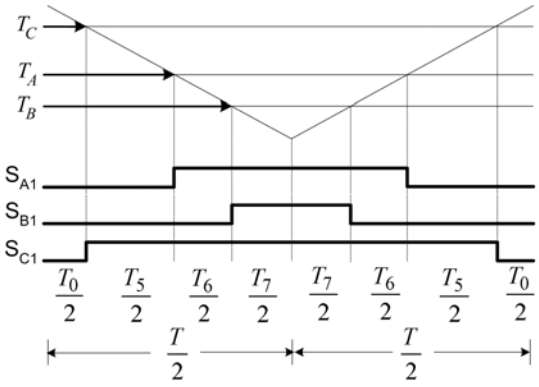
$k = 2$



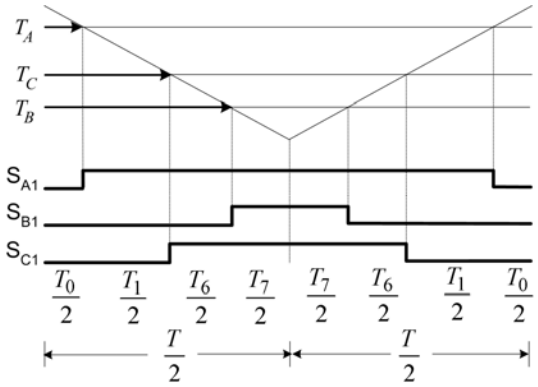
$k = 3$



$k = 4$



$k = 5$



$k = 6$

Fig. 2.19 Switching patterns of symmetrical space vector PWM

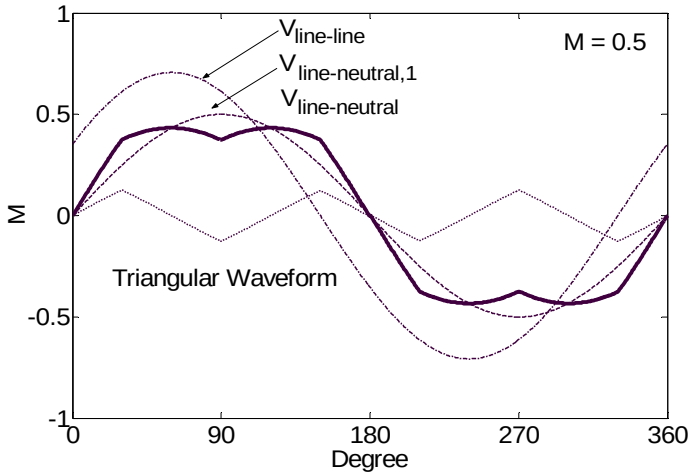


Fig. 2.20 Line to load-neutral and line to line voltage

As zero vectors evenly divided, the third harmonic triangular waveform is inherently added to a fundamental sinusoidal modulating signal. It results in flattening top of a space vector modulation function. The maximum continuous modulation index increases up to $M = 0.866$ which is similar to those obtained from conventional sinusoidal PWM with third harmonic injection. Thus, DC voltage utilization is 15% better than sinusoidal PWM. Fig. 2.20 shows line to load-neutral voltage that can be though of as consisting of the fundamental sinusoidal waveform and the triangular waveform of tripplen harmonic. Only the fundamental sinusoidal waveform appears in line to line voltage because common mode third harmonic is cancelled.

2.7 Implementation of DSP Based Control

Fig. 2.21 shows flow control diagram of the program implemented on the DSP [28]. Two interrupts such as period-interrupt and capture-interrupt are used to call

specific subroutines upon request performing several functions i.e., sampling, phase lock, generation of PWM output, current reference calculation, and synchronous frame current control. The period-interrupt is repeatedly called every switching period to sample the utility voltage and the inverter current, generate fundamental sinusoidal waveform, reference current calculation, and process current control algorithm. The capture-interrupt is repeatedly called every half period of the utility voltage to synchronize phase of fundamental sinusoidal waveform and calculate frequency of utility.

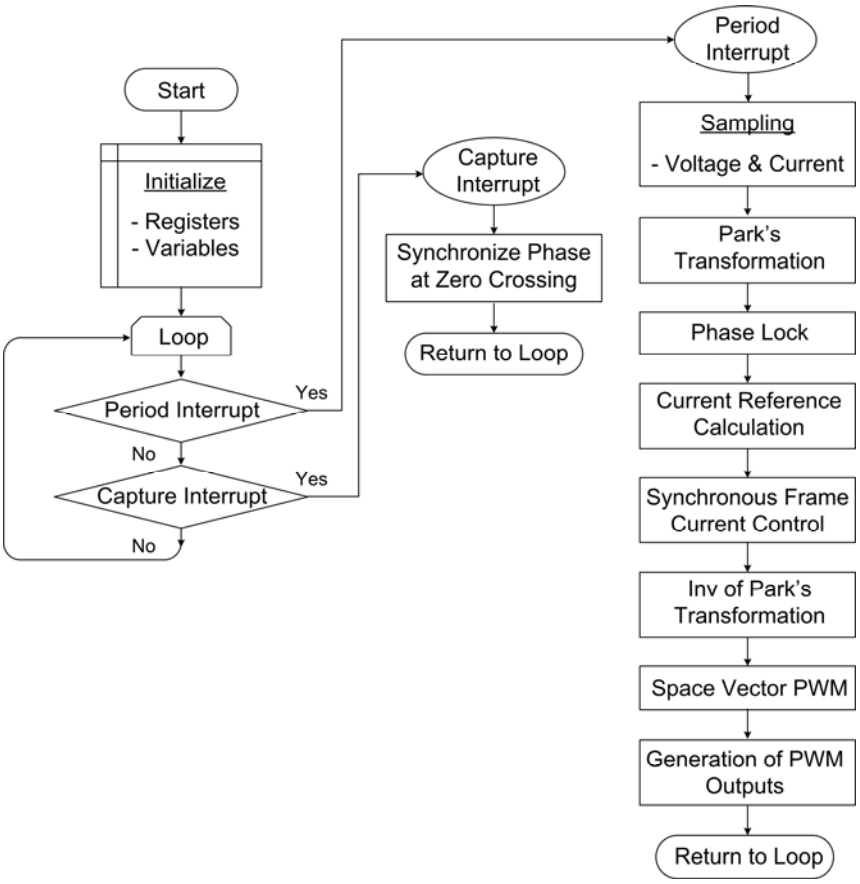


Fig. 2.21 Flow control of the program implemented by software

2.7.1 Sampling

Analog-to-digital converter (ADC) converts analog signals such as utility voltage and inverter current into 10-bit binary digits suitable for fixed-point arithmetic operations. It takes up to 1 μs for a single conversion. Since, the conversion of the ADC can be started by software. The period-interrupt is used to repeatedly call a subroutine to initiate a sampling process. After the conversion completed, voltage and current information in binary format (Q-format) are sent through 16-bit data bus to a DSP core for processing of the synchronous frame current control algorithm.

2.7.2 PI Controller

The control output signal of the PI controller (2.26) is expressed in difference equation as,

$$y_{[n]} = K_P \cdot e_{[n]} + K_I \cdot e_{[n]} + y_{[n-1]} - K_P \cdot e_{[n-1]} \tag{2.57}$$

where K_P and K_I are gains of the proportional and integral controller respectively. Discrete time realization of the PI controller is shown in Fig 2.22.

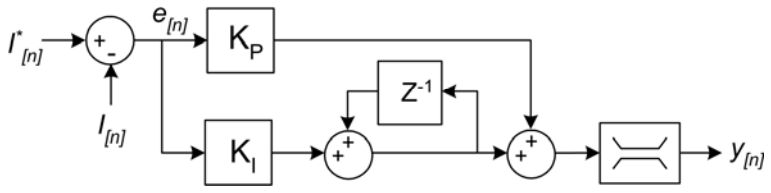


Fig. 2.22 Discrete time realization of the PI controller

2.7.3 Phase Lock

Fundamental sinusoidal waveforms such as $sin(\omega t)$ and $cos(\omega t)$ are needed by Park's Transformation. These waveforms can be easily generated from a table lookup which their values are pre-calculated and stored in allocated program memory. Fig. 2.23 shows generation of a fundamental sinusoidal waveform $sin(\omega t)$. To properly track the phase of utility voltage, a phase pointer is developed. Its value is increased by one every the period interrupt occurred. This value represents the phase of utility voltage and it is used as a pointer to retrieve sinusoidal values from a table lookup.

Phase of fundamental sinusoidal waveform must be synchronized with utility at every zero crossing to avoid phase shifting problem. The capture interrupt is employed to detect a transition (zero-crossing) of utility voltage. If a transition occurs, the capture interrupt calls a subroutine to reset a phase counter to zero. In addition to phase synchronization, the frequency of utility voltage is needed to be calculated every half cycle. In conjunction with a general purpose timer (GPT2), the capture unit (CAP) stores a counter value (T2CNT) from a selected timer on memory stacks (FIFO) when the capture interrupt occurs. The period of utility voltage can be calculated from a time interval during the occurrences of two consecutive interrupts. Fig. 2.23 shows calculation of the frequency of utility voltage. A 20 MHz clock signal is pre-scaled by 64. Within a half period, a phase counter accumulates up to 2604 which the utility period is calculated by $2\times2064\times64\times50$ nsec (60 Hz).

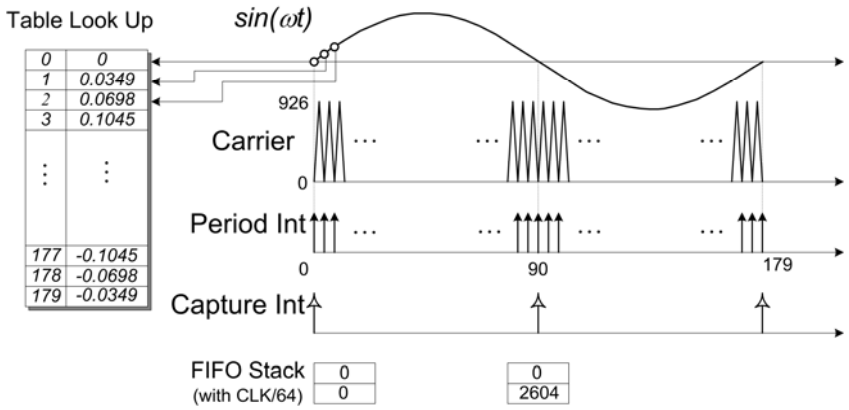


Fig. 2.23 Generation of a fundamental sinusoidal waveform

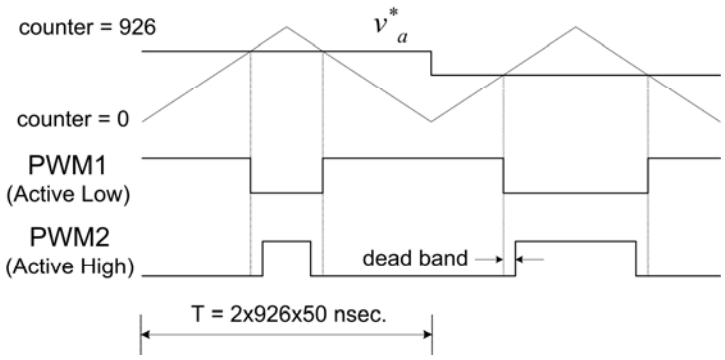


Fig. 2.24 Generation of PWM outputs

2.7.4 Generation of PWM Output

Generation of PWM output corresponding to the voltage references $v^*_{\{a,b,c\}}$ can be done easily with the available PWM peripheral. The PWM peripheral consists of three (full) compare units and can generate up to three PWM outputs grouped in pairs (PWM_X and PWM_{X+1}, x = {1, 2, 3}). One general purpose timer (GPT1) associated with a timer counter (T1CNT) is used to repeat up/down counting and store in a counter (T1CNT). Fig. 2.24 shows generation of PWM signals. With a 20 MHz clock

signal, a timer counter starts up/down counting from 0 to 926 generating a periodic triangular waveform at 10.8 kHz switching frequency. The modulation periods (see Table 2.2 and Table 2.3) stored in compare registers (CMPR1-3) are constantly compared to the value of a counter (T1CNT). When the value matches, a transition (low to high or high to low) occurs on the associated outputs. This process is repeated every period interrupt with different modulation periods in compare registers. To avoid shoot-through faults, blanking time is inserted by programmable dead band logics as shown in Fig. 2.24. Its value typically ranges from 1-4 μsec.

2.8 Simulation Results

To demonstrate viability of the proposed control topology, a single phase and a three-phase PWM inverter operating in parallel with utility are simulated. The single phase PWM inverter constantly supplies 0.5 kW output power with unity power factor to utility. The inverter output current is digitally controlled using the synchronous frame current controller (developed in section 2.5.2). In another simulation, the three-phase PWM inverter supplies 10 kW output power with unity power factor to balance three-phase utility 208V/60Hz. The three-phase inverter output currents are also digitally controlled by the synchronous frame current controller. Gain selection of the PI controllers is calculated from (2.41) and (2.42). System specification and simulation parameters are given in Table 2.4 and Table 2.5.

Table 2.4 System parameters and gain selection of a single phase PWM inverter

Parameter	Value
DC voltage	240 V_{dc}
Resistance	0.1 Ω
Inductance	2.4 mH
Switching frequency	10.8 kHz
Settling time, T_s	2 ms
Maximum overshoot M_p	20%
Damping ratio ζ	0.707
K_P	14.35
K_I	3.31

Table 2.5 System parameters and selected gains of a three-phase PWM inverter

Parameter	Value
DC voltage	360 V_{dc}
Resistance	0.05 Ω
Inductance	1.2 mH
Switching frequency	10.8 kHz
Settling time, T_s	2 ms
Maximum overshoot M_p	20%
Damping ratio ζ	0.707
K_P	7.17
K_I	1.65

Fig. 2.25 shows the output inverter current of the single phase PWM inverter i_a, while delivering 0.5 kW real power output to utility. The inverter current waveform is essentially sinusoidal waveform. It has low total harmonic distortion (THD) < 3%. Phase of the inverter current is controlled in phase with the utility voltage to maintain unity power factor.

Fig. 2.26 (a) and (b) shows step response of the output inverter current under 50% the real power reduction. The inverter current is effectively controlled under the sudden change of the real power reference. It reaches the steady state in 2 msec with acceptable 20% overshoot.

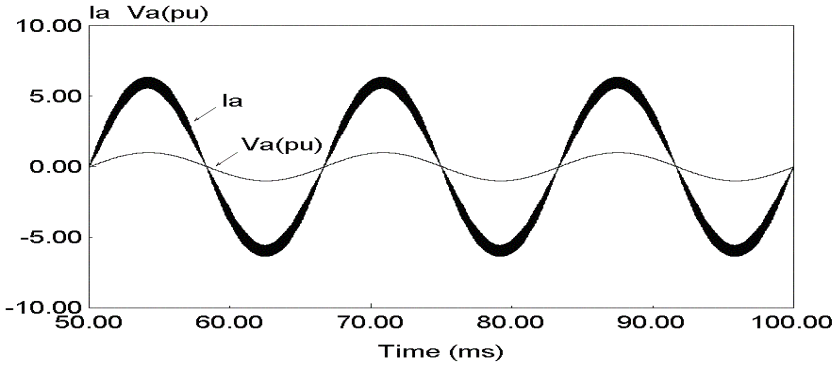
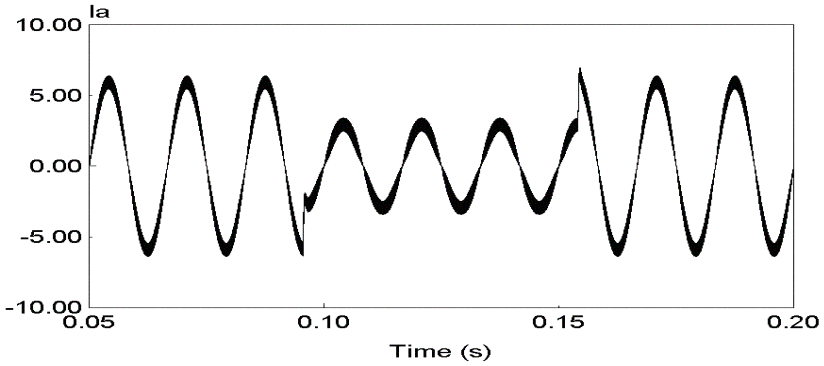
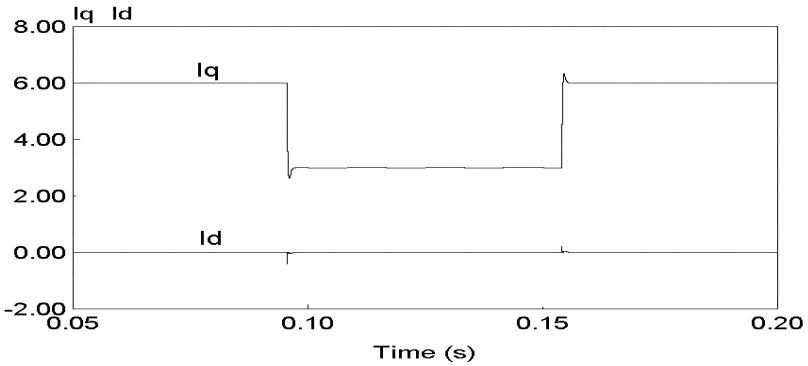


Fig. 2.25 Simulation result of the single phase PWM inverter supplying 0.5 kW, the inverter current i_a and utility voltage v_a



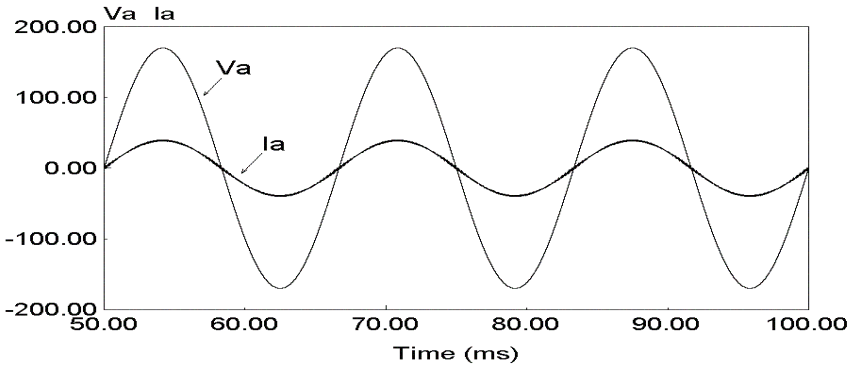
(a) Output inverter current i_a



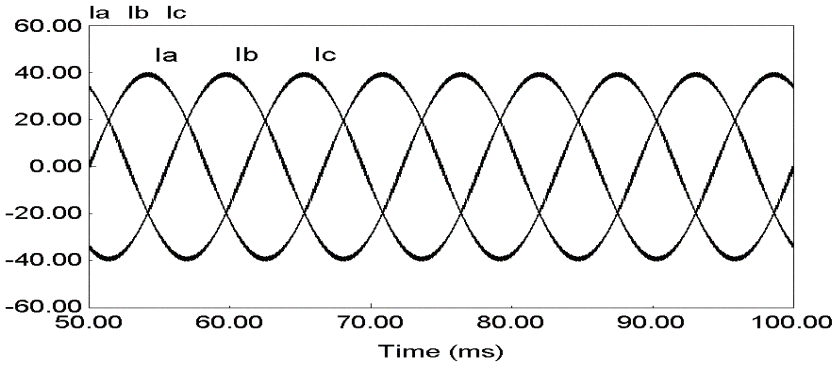
(b) Output inverter current in a synchronous frame $i_{\{d,q\}}$

Fig. 2.26 Step response of the single phase PWM inverter current under 50% real power reduction

Fig. 2.27 (a) shows the output inverter current i_a of the three-phase PWM inverter while delivering 10 kW to utility. Phase of the inverter current is regulated in phase with the utility voltage. Fig. 2.27 (b) shows the balance three-phase inverter current.



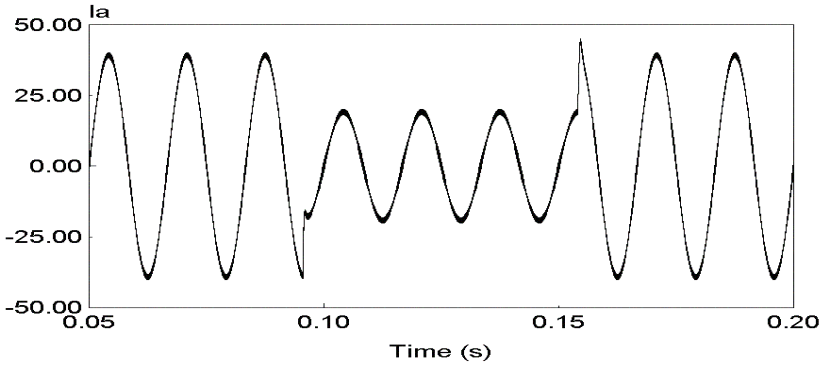
(a) Output inverter current i_a and utility voltage v_a



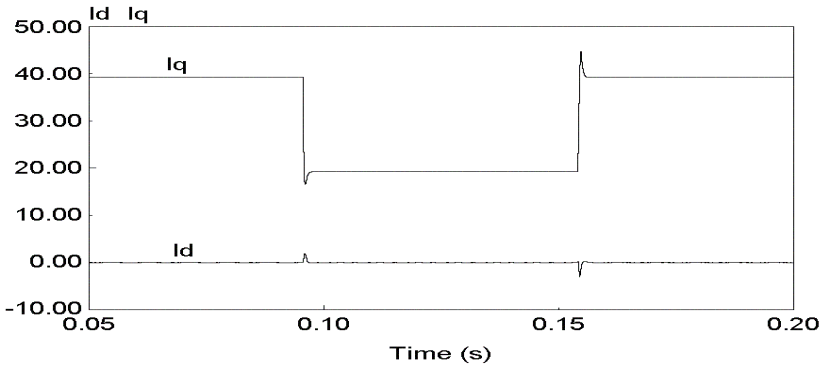
(b) Balance three-phase inverter current

Fig. 2.27 Simulation results of the output current of the three-phase PWM inverter supplying 10 kW

Fig. 2.28 shows step response of the output inverter currents i_a and $i_{\{d,q\}}$ under 50% the real power reduction. It is shown that the output inverter currents i_a and $i_{\{d,q\}}$ are well regulated and reach the steady state in 2 msec with moderate overshoot 20%.



(a) Output inverter current i_a



(b) Output inverter current in a synchronous frame $i_{\{d,q\}}$

Fig. 2.28 Step response of the three-phase PWM inverter current under 50% real power reduction

2.9 Experimental Results

A single-phase fuel cell inverter prototype rated at 0.5 kW, 120V, 60Hz is built for a laboratory test. Experimental setup and DSP control implementation are shown in Fig. 2.29. The proposed control topology associated with the power calculator, the synchronous frame current controller and the space vector PWM

scheme are implemented via software using a digital signal processor TMS 320-F243. System parameters and gain selection of the PI controller are shown in Table 2.4.

Fig. 3.30 (a) shows generation of a fundamental sinusoidal waveform. In every period-interrupt, the phase counter is constantly added by one. It is synchronized with utility by resetting to zero in half period of utility. Its value ranges from 0 to 89 representing phase of utility in a half period. A normalized value of the sinusoidal waveform is properly picked from the table lookup in the program memory by taking into account of the value of the phase counter and the polarity of utility voltage. Fig. 3.30 (b) shows period and magnitude measurement of utility voltage. These values are needed for monitoring conditions of utility. The inverter is required to disconnect from utility, if the frequency is out of a range 59.3-60.5 Hz and the voltage is out of a range 105.6-132 V as recommended by the standards [6],[7].

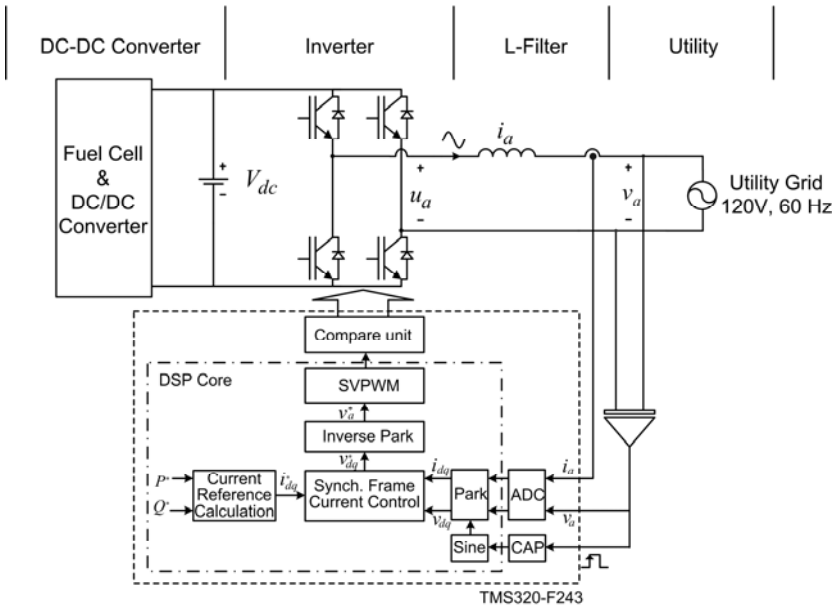
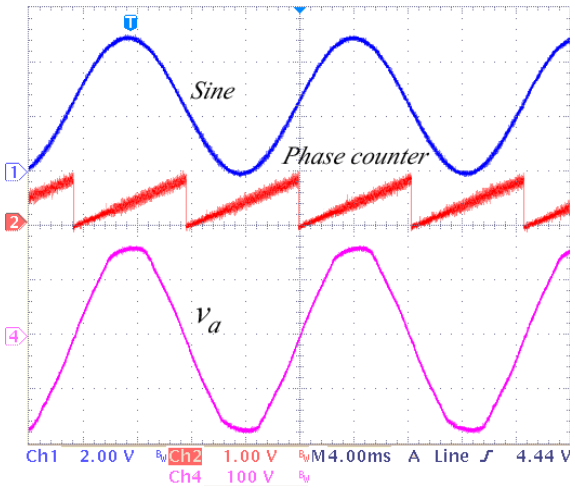
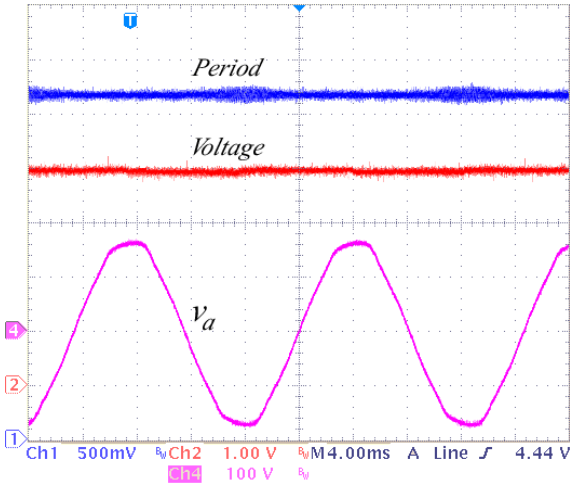


Fig. 2.29 DSP control implementation of a single phase fuel cell based inverter

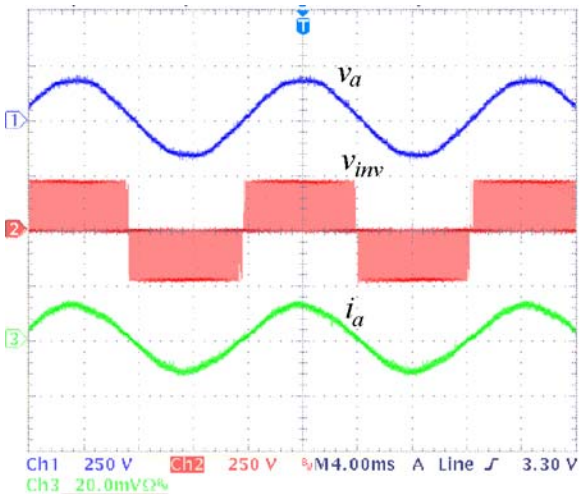


(a) A fundamental sinusoidal waveform generation, Ch1: a normalized sinusoidal waveform and Ch2: phase counter, Ch3: utility voltage (v_a) 100V/div

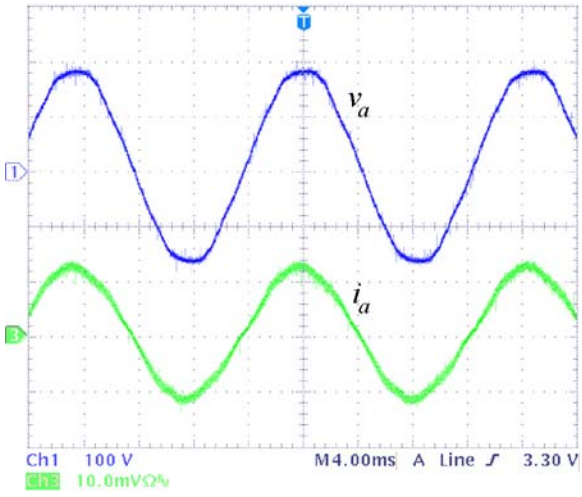


(b) Ch1: period of utility voltage 2.625 ms/div, Ch2: the inverter terminal peak voltage (utility) 42.5 V/div and Ch4 utility (v_a) 100V/div

Fig. 2.30 Phase Lock and sinusoidal waveform generation



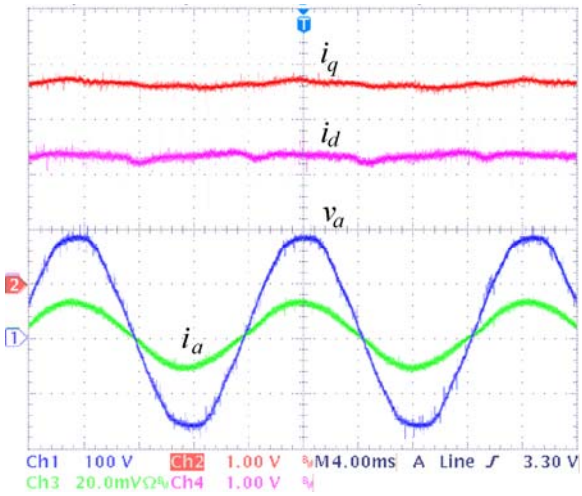
(a) Ch1: utility voltage (v_a) 250 V/div, Ch2: the inverter switching voltage (v_{inv}) 250 V/div, and Ch3: the inverter current (i_a) 10A/div



(b) Ch1 utility voltage (v_a) 100 V/div and Ch3: inverter current (i_a) 5A/div

Fig. 2.31 Steady state operation of the single phase PWM inverter supplying 0.5 kW

Fig. 2.31 shows steady state operation of the inverter while delivering 0.5 kW output power with unity power factor. The inverter output current is digitally controlled in a synchronous frame. It has essentially sinusoidal waveform in phase with the utility voltage. In compliance to the IEEE Std. 929-2000 [6] and the IEEE Std. 1547 [7], the total harmonic distortion (THD) is suppressed below 3.5%. Switching voltage at the inverter terminal is shown to illustrate the operation of single phase space vector PWM. High frequency switching ripple current is satisfactorily attenuated by the inductor filter.



Ch1: utility voltage (v_a) 250 V/div, Ch2: the inverter output current in a q-axis (i_q), Ch3: the inverter current (i_a) 10A/div, and Ch4: the inverter current in a d-axis (i_d)

Fig. 2.32 Transformed inverter output currents in a synchronous frame i_d and i_q while the single phase PWM inverter supplies 0.5 kW

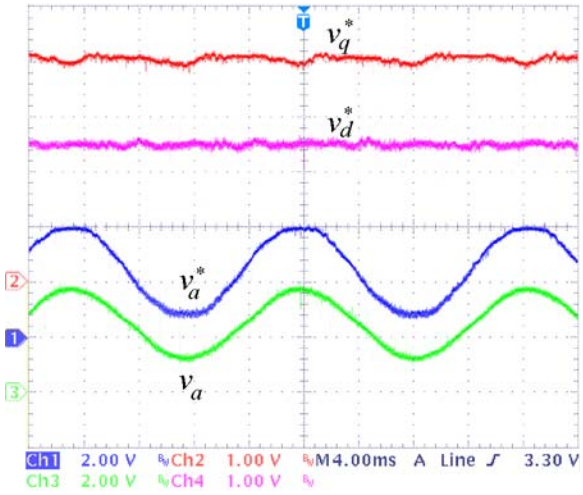


Fig. 2.33 Control voltage reference in a synchronous frame v_d and v_q, the transformed voltage reference v^*_a and utility voltage v_a

Fig. 2.32 shows the inverter output currents i_d and i_q transformed to a synchronous frame rotating at the system frequency. The transformed current is well regulated in dc-quantity by PI controllers. Slightly distortion at zero crossing is observed and it can be further improved by reducing dead band and increasing resolution of the sampled inverter currents.

Fig. 2.33 shows the voltage references in a synchronous frame v^*_d and v^*_q computed by synchronous frame current controllers. These voltages are transformed to a stationary frame or v^*_a by the inverse of Park's transformation ($\boldsymbol{S_{dq}}$). It is later used to generate high frequency PWM output voltage which ensures sinusoidal inverter current supplied to utility grid.

2.10 Summary

In this chapter, digitally controlled DC-AC PWM inverters have been developed for utility interconnection of the DFPG. Current control in a synchronous reference frame (dq-frame) utilizing proportional-integral (PI) controllers has been proposed. With a high speed digital signal processor (DSP), real time control of digital current control in a synchronous frame, phase lock function (PLL), space vector pulse width modulation (PWM) etc is realizable by implementing via software. The DSP based control significantly enhances performance and flexibility of the inverters. Simulation and experimental results of the single-phase PWM inverter 0.5kW, 120V/60Hz and the three-phase PWM inverter rated 10kW, 120V/60Hz show excellent performance.

CHAPTER III

DEVELOPMENT OF A ROBUST ANTI-ISLANDING ALGORITHM FOR UTILITY INTERCONNECTION OF A DISTRIBUTED FUEL CELL POWERED GENERATION

3.1 Introduction

As discussed in Chapter I, a number of islanding detection methods have been developed in the past decade [8-17]. However, the passive method is shown to have a non-detection zone (NDZ) leading to failure of the detection. The active method is capable of reducing a non-detection zone (NDZ). But it also fails under particular circumstances as discussed. In other method, it is shown to be an ideal solution but high cost of implementation renders the method as virtually impossible.

In response to this concern, this chapter explores the development of a robust anti-islanding algorithm. The proposed algorithm continuously perturbs (±5%) the reactive power supplied by a DFPG while monitoring the utility voltage and frequency. It is shown that perturbing the DFPG reactive power by ±5% results in observable frequency (> ±1%) when islanding occurs. To further positively confirm islanding, the proposed algorithm reduces the DFPG real power output to 80%. If the inverter (DFPG) terminal voltage drops below 0.9 per-unit, the occurrence of

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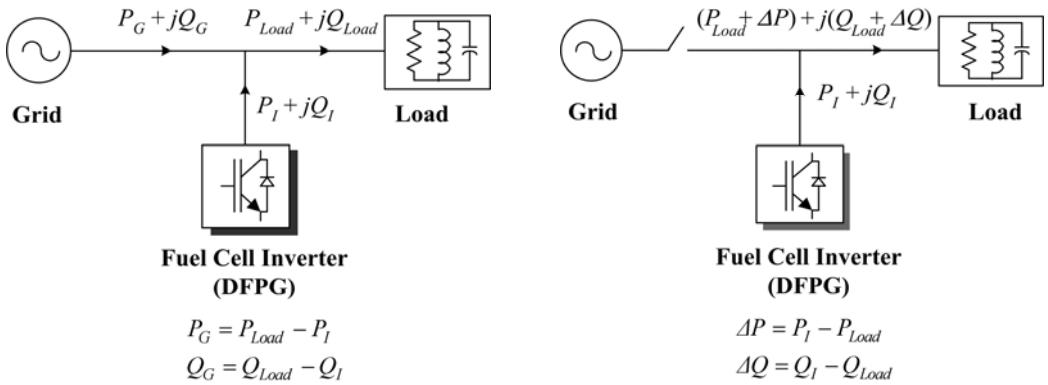
*Reprinted with permission from "Development of a Robust Anti-Islanding Algorithm for Utility Interconnection of Distributed Fuel Cell Powered Generation" by C. Jeraputra and P. N. Enjeti, *IEEE Transactions on Power Electronics,* Vol.19, No. 5, pp. 1163-1170, September 2004.

islanding is confirmed and the DFPG is safely disconnected. This method of detection is shown to be robust and fast acting (operable in a cycle) and it significantly reduces the non-detection zone (NDZ) compared to all other detection methods. Several possible islanding conditions are simulated and verified with analysis. Experimental results on the fuel cell inverter (0.5 kW) connected to 120V/60Hz utility are presented.

3.2 Analysis of Real and Reactive Power Mismatch

Islanding voltage and frequency can be calculated analytically based on real and reactive power mismatch at the instant the utility disconnected. Fig. 3.1 (a) shows power flow diagram of a DFPG and a load in the presence of utility. Fig. 3.1 (b) shows disconnection of utility. ΔP and ΔQ are defined as real and reactive power mismatch at the instant of disconnection. For the purpose of analysis, the DFPG is modeled as a current source and the load is represented by equivalent parallel RLC elements. Fig. 3.2 shows per phase equivalent circuit of the system for this condition.



(a) Normal condition (b) Islanding condition

Fig. 3.1 Interconnection of a DFPG source to utility and a load

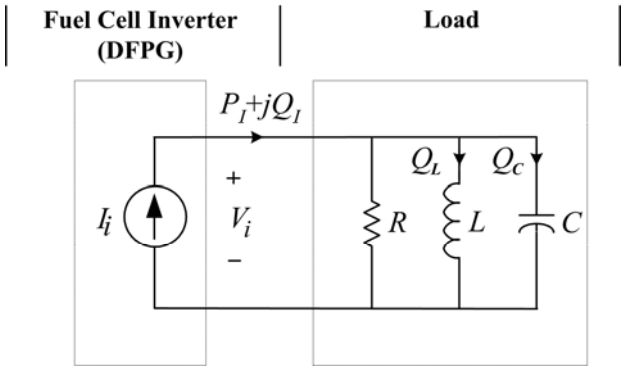


Fig. 3.2 Equivalent circuit of a DFPG and a RLC load at the instant the utility disconnected

For clarity, the term "islanding voltage V_i" is defined as the voltage at inverter (DFPG) terminal and the load terminal. The term "islanding frequency ω_i" is defined as the frequency of inverter (DFPG) output when the utility is disconnected.

Let:

P_I : Real power output of the DFPG

Q_I : Reactive power output of the DFPG

P_G : Real power output of the utility

Q_G : Reactive power output of the utility

Q_C : Capacitive reactive power (of the load)

Q_L : Inductive reactive power (of the load)

ΔP: Real power mismatch between DFPG and utility

ΔQ: Reactive power mismatch between DFPG and utility

V_i : Islanding voltage

V_n : Nominal system voltage

Since the load is represented by equivalent RLC elements, which connected in parallel, islanding voltage across R and parallel LC is the same. The impedance of the parallel LC (Fig. 3.3) is expressed as,

$$Im\{Z_{LC}\} = \frac{\omega_i L}{1-\omega_i{}^2 LC} \tag{3.1}$$

where ω_i is the islanding frequency. Furthermore, Z^*_{LC} is expressed in terms of P_I and Q_I variables as,

$$Im\left\{Z^*_{LC}\right\} = \frac{R \cdot P_I}{Q_I} \tag{3.2}$$

Equating (3.1) and (3.2) we obtain,

$$\omega_i{}^2 - \frac{Q_I}{RCP_I}\omega_i - \left(\frac{1}{\sqrt{LC}}\right)^2 = 0 \tag{3.3}$$

The quality factor q of the connected load is defined as,

$$q = \frac{\sqrt{|Q_L| \cdot |Q_C|}}{P} = R\sqrt{\frac{C}{L}} \tag{3.4}$$

Equation (3.3) can be expressed in term of q as,

$$\omega_i{}^2 - \frac{R}{q^2 L}\frac{Q_I}{P_I}\omega_i - \left(\frac{R}{qL}\right)^2 = 0 \tag{3.5}$$

From (3.5), the islanding frequency ω_i can be computed,

$$\omega_i \approx \frac{1}{\sqrt{LC}} \cdot \left(1 + \frac{1}{2}\frac{Q_I}{qP_I}\right) \tag{3.6}$$

Voltage at the instant utility disconnected (islanding voltage) can be calculated from the following equation.

$$\frac{V_i}{V_n} = \sqrt{\frac{P_I}{P_{Load}}} \tag{3.7}$$

The islanding voltage V_i can be expressed as,

$$V_i = \sqrt{k} \cdot V_n \tag{3.8}$$

where

$$k = \frac{P_I}{P_{Load}} \tag{3.9}$$

From the above analysis the following can be concluded:

- The islanding frequency ω_i is a function of the DFPG real power P_I, reactive power Q_I and resonant frequency of the load ($1/\sqrt{LC}$) (in (3.6)).
- The inverter (DFPG) terminal voltage at the instant utility disconnected is a function of the ratio of real power of the DFPG and the load (in (3.8)).
- The worst case islanding condition occurs in the following scenario: when the real power of the DFPG is equal to the real power of the load i.e., $P_I = P_{Load}$, and the corresponding reactive power is also equal i.e., $Q_I = Q_{Load}$. For this condition, the voltage and the frequency at the inverter terminal continues to be the same as when utility was connected. Under this condition, the DFPG fails to notice the disconnection of utility and continues to operate, hence causing islanding. When the above described conditions are nearly met, the variations in the voltage and the frequency may be small and may escape the detection. This zone is called a non-detect zone (NDZ).

3.3 A Robust Anti-Islanding Algorithm Development

Three major islanding scenarios are explored and the robust anti-islanding algorithm is developed and presented in this section.

Case # 1: ΔP is large:

When the real power of the DFPG and that of the load are not equal, ΔP is large. Under this condition, if the utility is disconnected, then from (3.8), it is clear that the inverter (DFPG) terminal voltage will vary widely. Fig. 3.3 shows the variation of the islanding voltage V_i as a function of ΔP. According to the IEEE Std. 929-2000 [6] or the IEEE Std 1547-2003 [7], the inverter (DFPG) operating voltage should be within the range of $0.88 \leq V_i \leq 1.10$ per-unit. If these operating limits are chosen, islanding condition can be detected effectively only if $\Delta P > \pm 20\%$ (see Fig. 3.3).

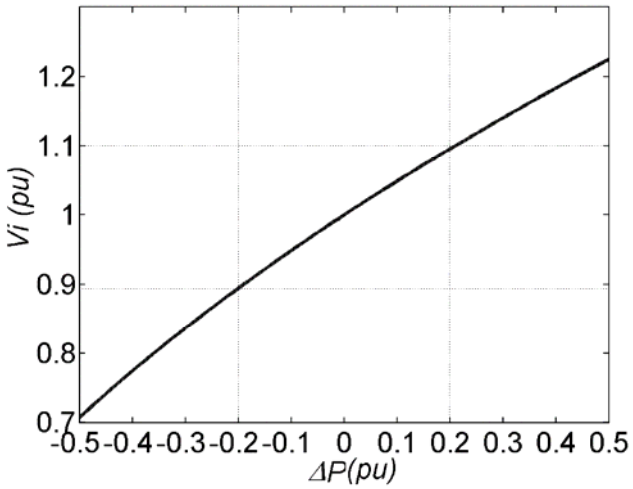
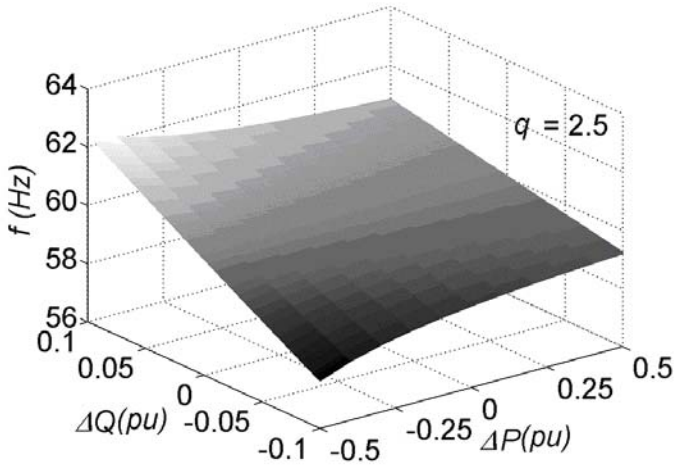


Fig. 3.3 Variation of islanding voltage V_i (in Fig. 3.2) versus ΔP

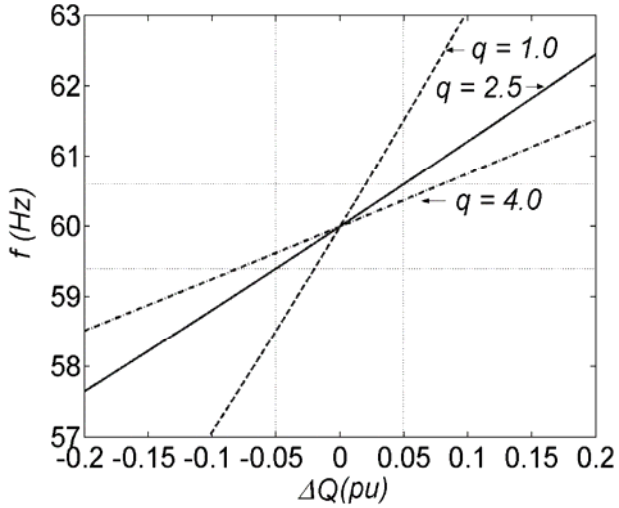
Case # 2: ΔP is small and ΔQ is large:

In the case, the real power of the DFPG and the load are nearly equal (i.e., ΔP is small); however, the reactive power of the DFPG and the load differ (ΔQ difference is larger). Upon disconnection of the utility, the relationship derived in (3.6) confirms that a change in frequency occurs. Fig. 3.4 (a) shows variation of the islanding frequency as a function of ΔP and ΔQ. Fig.3.4 (b) shows islanding frequency variation as a function of ΔQ when ΔP is zero. It is noted that the variation is also a function of the quality factor q of the load (see (3.6)). According to the IEEE Std. 929-2000 [6] or the IEEE Std. 929-2000 [7], the DFPG operating frequency should be within the range of 59.3Hz to 60.5 Hz. Therefore, the DFPG must be disconnected when the frequency is out of these limits. However, if this condition is chosen for islanding protection, the DFPG will fail to disconnect when the load has $q \geq 2.5$, $\Delta P = 0$, and $\Delta Q < \pm 5\%$.



(a) Variation of Islanding frequency as a function of ΔP and ΔQ variables for $q = 2.5$

Fig. 3.4 Islanding frequency



(b) Frequency vs. ΔQ as a function of q when $\Delta P \approx 0$

Fig. 3.4 Continued

Case # 3: ΔP and ΔQ are small:

It is clear from case # 1 and # 2 analysis that a small ΔP (< ±20%) results in an insufficient change in the voltage V_i (Fig. 3.3) and small ΔQ (< ±5%) results in inadequate change in the frequency (Fig. 3.4) to effectively disconnect the DFPG and prevent islanding. This zone is commonly known as a non-detection zone (NDZ) for the passive method to detect islanding and is shown in Fig. 3.5. Thus, the focus of the proposed power control algorithm in this paper is to nearly reduce the NDZ to zero and is detailed in the next section.

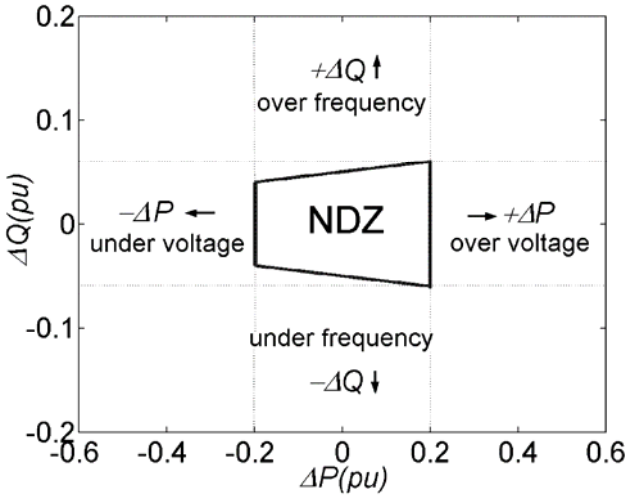


Fig. 3.5 Exist of a non-detection zone (NDZ) of over/under voltage and frequency method

3.4 Proposed Power Control Algorithm

The focus of the proposed power control algorithm is to reduce the NDZ to near zero. The algorithm consists of two steps. In step #1, the reactive power (Q_I) of the DFPG is continuously perturbed by ±5%, while maintaining the real power (P_I) constant. Both the voltage and frequency simultaneously are monitored. The ratio of the reactive power Q_I to the real power P_I supplied by the DFPG is expressed as,

$$\frac{Q_I}{P_I} = K \cdot sgn(V_i) \tag{3.10}$$

where K denotes the reactive power perturbation and is set to 5% (or 0.05 per-unit). For this setting a noticeable frequency deviation can be observed when the load $q <$ 2.5 (see Fig. 3.4). From (3.5), the islanding frequency for this perturbation can be calculated as,

$$\omega_i = \frac{1}{\sqrt{LC}}\left(\frac{K \cdot sgn(V_i)}{2q} + 1\right) \tag{3.11}$$

The frequency deviation ($\Delta\omega_i$) is defined as.

$$\Delta\omega_i = \omega_{i[k]} - \omega_{i[k-1]} \tag{3.12}$$

When utility is connected, the frequency deviation $\Delta\omega_i$ is small or nearly zero. However, when the instant utility disconnected, a change in the frequency deviation $\Delta\omega_i$ is noticeable due to ±5% perturbation in the reactive power Q_f. When the frequency deviation confines in $\pm 1\% \leq \Delta\omega_i \leq \pm 2\%$, the possibility of islanding is considered to be somewhat higher since it is within the specified limit of the IEEE Std. 929-2000 [6] or the IEEE Std. 1547 [7], (59.3Hz to 60.5Hz). This change is observed for at least for four consecutive cycles. If during this period the frequency change increases rapidly, then islanding is confirmed and the DFPG is disconnected. However, if the frequency deviation $\Delta\omega_i$ continues to be within the above specified limits, the proposed algorithm reduces the DFPG real power to 80% (i.e., 0.8 per-unit) for another 10 cycles as a part of step #2. Now if the magnitude of the voltage V_i falls below 0.9 per-unit, the occurrence of islanding is confirmed and the DFPG is disconnected. In case, the magnitude of the voltage V_i is normal. The DFPG is allowed to continue its operation. The proposed two step approach, (described above), is robust and fast acting. Fig. 3.6 shows a flowchart of the proposed robust anti-islanding algorithm.

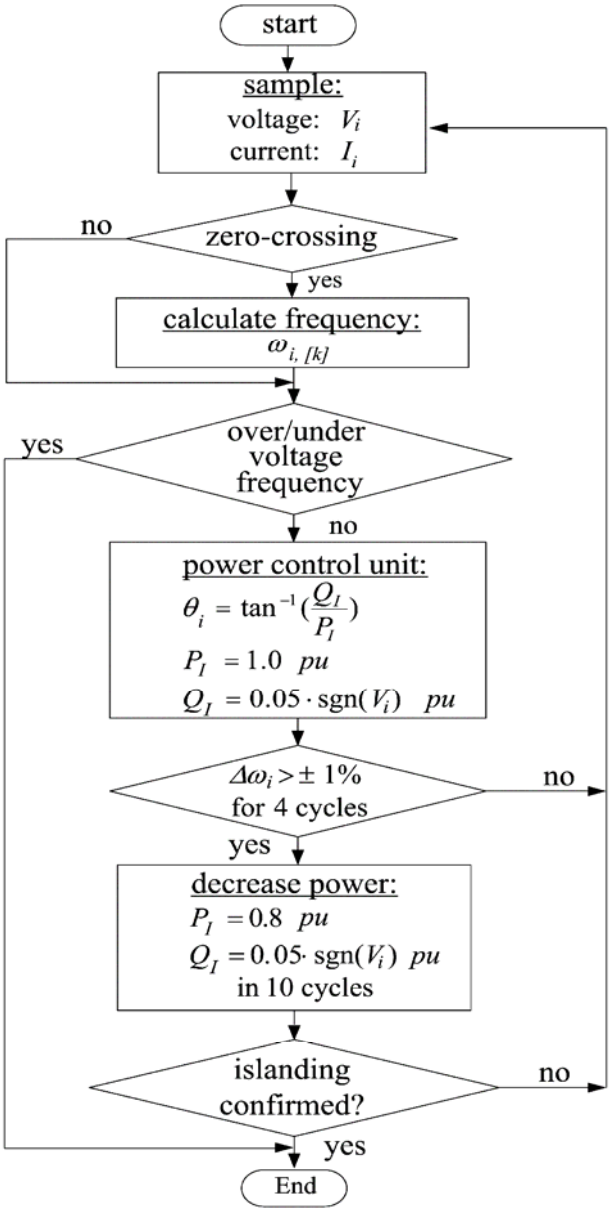


Fig. 3.6 Flow chart of the robust anti-islanding detection algorithm

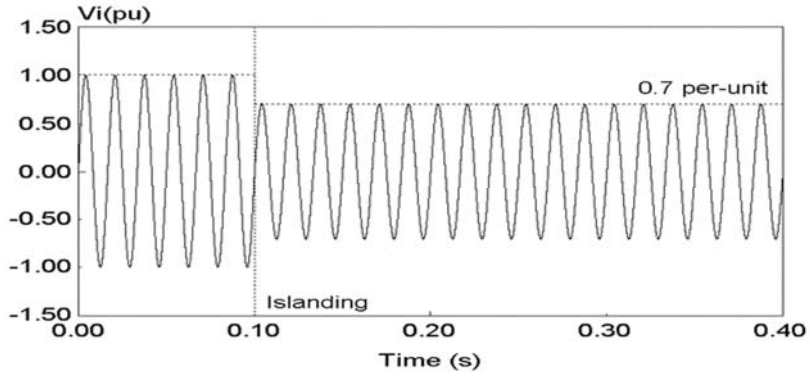
3.5 Simulation Results

In this section simulation results are presented to illustrate the effectiveness of the proposed anti-islanding algorithm. Three possible islanding cases are simulated. The DFPG is represented by a voltage controlled current source and its frequency is monitored every half cycle by a resetable integrator. Table 3.1 shows the parameters used in the simulation of the system.

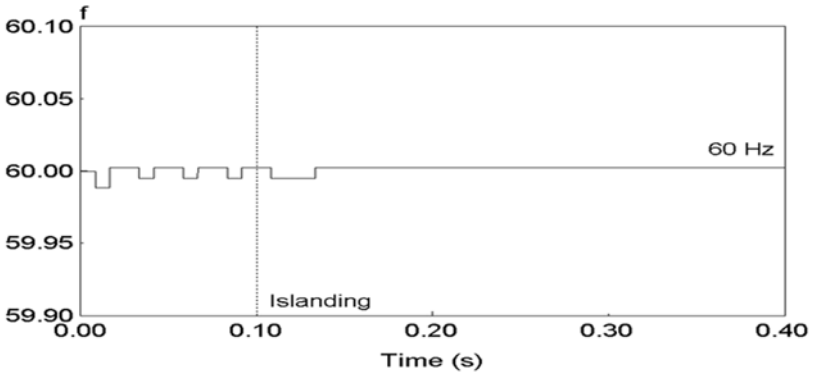
In Fig. 3.7, for case # 1: real power mismatch between the DFPG and the load is large (ΔP = -0.5 per-unit and ΔQ = 0 per-unit). Under normal condition, the DFPG continuously supplies the constant real power (P_I = 0.5 per-unit, Q_I = 0 per-unit) to the load. At instant the utility disconnected, the magnitude of the voltage *Vi* immediately drops to 0.70 per-unit (Fig. 3.7 (a)) due to insufficient real power supplied from the DFPG (see (3.7)). The occurrence of islanding can be easily detected by monitoring the under voltage. It is noted that the frequency does not alter significantly since reactive power mismatch ΔQ is zero.

Table 3.1 Simulation parameters

Parameters	Value
Voltage	120 V
Frequency	60 Hz
P_{Load}	0.5 kW, 28.80 Ω
Q_L	1.25 kVAR, 30.56mH
Q_C	1.25 kVAR, 230.25μF



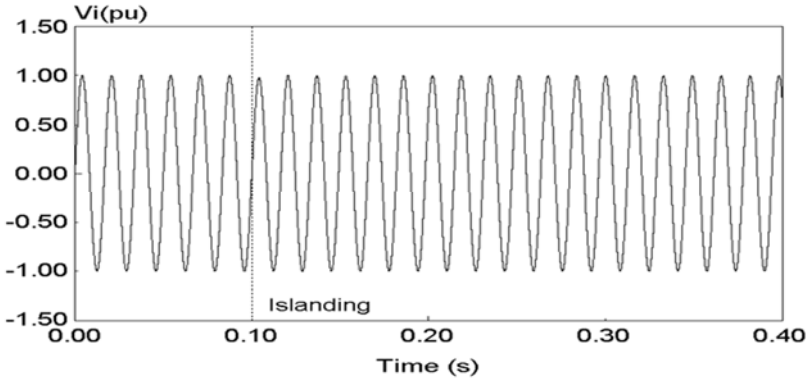
(a) Islanding voltage of ΔP = -0.5 and ΔQ = 0



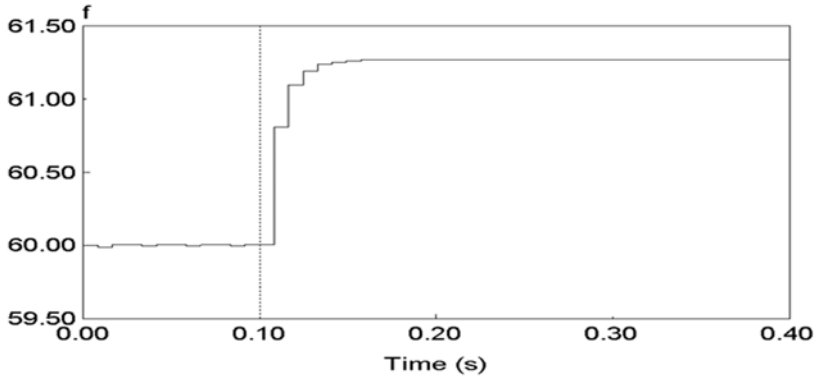
(b) Islanding frequency of ΔP = -0.5 and ΔQ = 0

Fig. 3.7 Simulation results for Case # 1: ΔP is large

Fig. 3.8 shows the simulation results for case # 2: real power mismatch is near zero and reactive power mismatch is larger ($\Delta P \approx 0$ and ΔQ = 0.1 per-unit). In this case, the DFPG real power P_I is essentially the same as the load P_{Load}, however the DFPG reactive power Q_{Load} exceeds Q_I by 0.1 per-unit. At the instant the utility disconnected, the magnitude of V_i is unaltered; however, the frequency increases to 61.25 Hz. This new operating frequency results from a larger reactive power mismatch (see (4.6)). Since this exceeds the threshold (59.3Hz to 60.5Hz) [6],[7]. The occurrence of islanding is positively confirmed.



(a) Islanding voltage

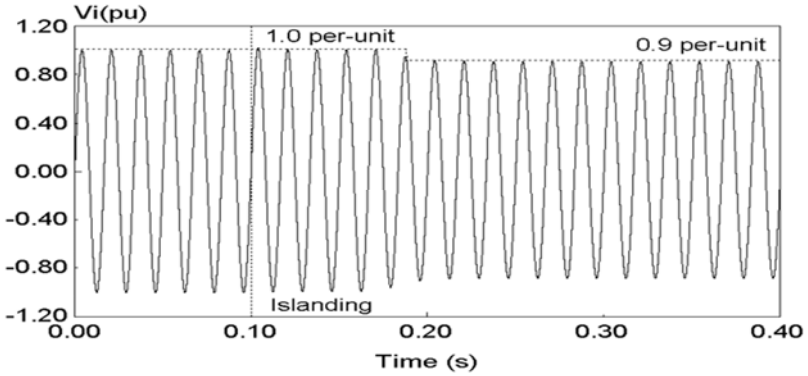


(b) Islanding frequency of $\Delta P = 0$ and $\Delta Q = 0.1$

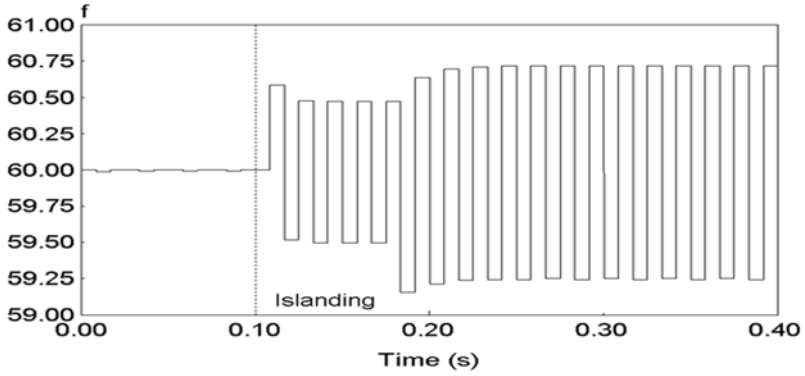
Fig. 3.8 Simulation results for case #2: ΔP is small and ΔQ is larger

Fig. 3.9 shows the simulation results for case # 3: both the real and reactive power mismatch is small ($\Delta P \approx 0$ per-unit and $\Delta Q \approx 0$). For this condition to exist, the DFPG real and reactive power must match the connected load. That is $P_I \approx P_{Load}$ and $Q_I \approx Q_{Load}$). From the previous analysis it is clear that this is the most difficult scenario to detect islanding. The proposed power control algorithm is employed. In this case the DFPG real power is maintained constant and its reactive power is perturbed by ±5%. At the instant the utility disconnected, from Fig. 3.9 (b) it is noted

that the frequency deviation is observed ($\Delta\omega$ = ± 0.5Hz). According to the proposed algorithm, the DFPG is allowed to continue its operation as long as the frequency variation is within the specified limit (59.3Hz to 60.5Hz). In the mean time, the algorithm recognizes the frequency variation for over four consecutive cycles and the DFPG real power P_I is then reduced to 80% for the next 10 cycles. It is noted in Fig. 3.9 (a) that the inverter terminal voltage V_i is reduced to 0.9 per-unit thus positively confirming islanding.



(a) Islanding voltage



(b) Islanding frequency of $\Delta P \approx 0$ and $\Delta Q \approx 0$.

Fig. 3.9 Simulation results for case #3: ΔP and ΔQ are small and the proposed power control algorithm is applied

3.6 Experimental Results

Fig. 3.10 shows the experimental setup of the single phase fuel cell inverter rated at 0.5kW, 120V, 60Hz connected to the utility. The inverter (DFPG) developed in the previous chapter is controlled in current control mode employing a TMS-320-F243 digital signal processor (DSP). The proposed robust anti-islanding algorithm is implemented in DSP via software. Under normal condition, the inverter (DFPG) is programmed to continuously supply the available fuel cell power to the utility. The reactive power of the inverter (DFPG) is constantly perturbed by ±5% as described in the previous sections. Both real and reactive power supplied by the inverter (DPFG) can be controlled by altering the phase shift between the utility voltage and the inverter current.

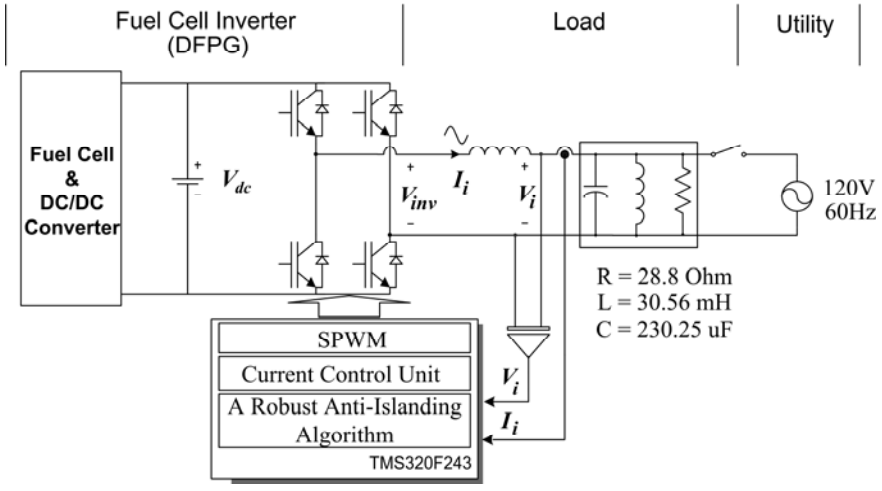


Fig. 3.10 Experimental set up

Fig. 3.11 shows the normal operation of the inverter (DFPG) when connected to utility. Fig. 3.12 shows significant the inverter (DFPG) terminal voltage drop to 0.70 per-unit due to large real power mismatch ΔP = -0.50 per-unit which is described in islanding case #1. It is noticed that inverter (DFPG) current is increased after reduction of terminal voltage to maintain constant output the real power. Fig. 3.13 shows the noticeable frequency change when islanding occurs for case #2. The frequency is increased to 61.3 Hz due to reactive power mismatch ΔQ = 0.1. But the inverter (DFPG) terminal voltage remains the same as utility was connected because of zero real power mismatch.

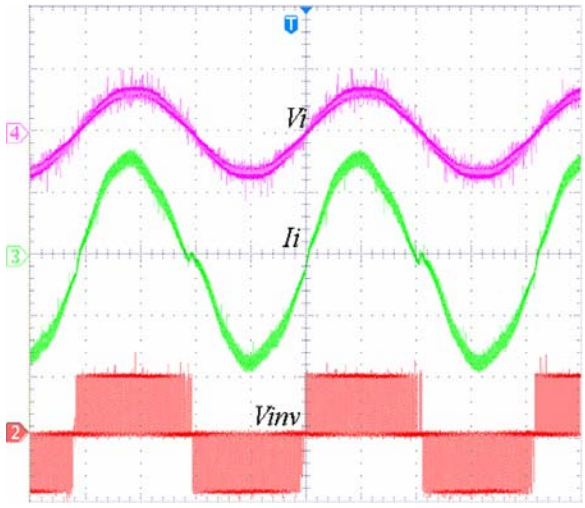


Fig. 3.11 Experimental result of normal operation of the DFPG connected to the utility, CH2: fuel cell inverter voltage (V_{inv}) 250V/div, CH3: fuel cell inverter current (I_i) 4A/div, CH4 terminal voltage (utility voltage V_i) 250V/div

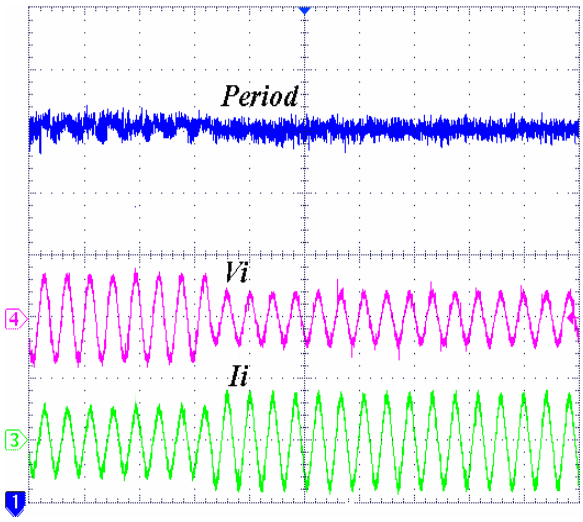


Fig. 3.12 Experimental result of islanding case #1, CH1: period of terminal voltage 2.60 ms/div, CH3: fuel cell inverter current (I_i) 10 A/div CH4: terminal voltage (islanding, voltage V_i) 250V/div

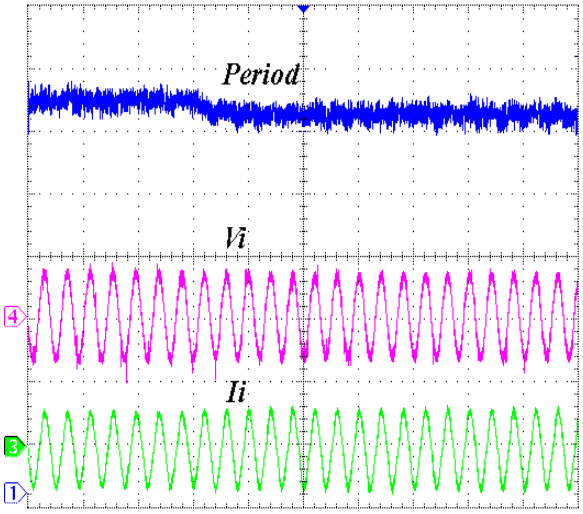


Fig. 3.13 Experimental result of islanding case#2, CH1: period of terminal voltage 2.60 ms/div, CH3: fuel cell inverter current (I_i) 10 A/div CH4: terminal voltage (islanding, voltage V_i) 250V/div

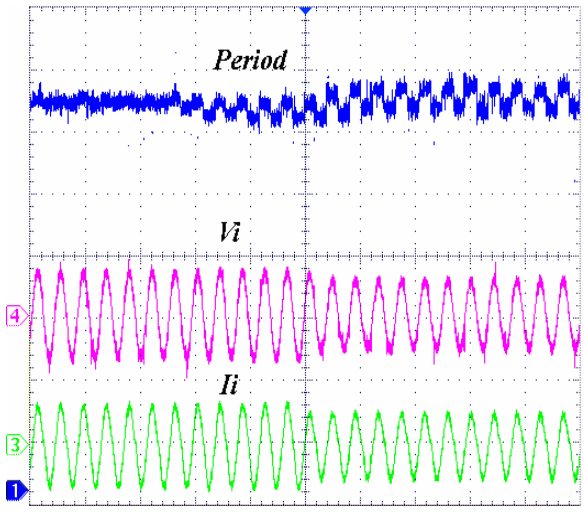


Fig. 3.14 Experimental result of islanding detection by the developed robust anti-islanding algorithm, CH1: period 2.67ms/div, CH3: fuel cell inverter current (I_i) 10A/div., CH4: terminal voltage (islanding voltage V_i) 250V/div

Fig. 3.14 shows the noticeable frequency deviation ($\Delta\omega_i$ = ±0.60 Hz) when islanding occurs for case # 3. The inverter (DFPG) continues to operate (Fig. 3.14) for four cycles and initiates the real power reduction to 0.8 per-unit, upon which the voltage (V_i) is shown to reduce confirming islanding. Experimental results of all three cases are compared to simulation results and analytical equations in Table 3.2.

Table 3.2 Summary of calculation, simulation and experimental results

Case	ΔP (pu)	ΔQ (pu)	Calculation		Simulation		Experiment	
			V_i (pu)	Hz	V_i (pu)	Hz	V_i (pu)	Hz
1	-0.5	0	0.71	60	0.7	60	0.7	60
2	0	0.1	1.0	61.26	1.0	61.25	1.0	61.30
3	0	0	0.89	60±0.75	0.90	60±0.75	0.89	60±0.80

3.7 Summary

In this chapter, the robust anti-islanding algorithm for utility interconnection of a distributed fuel cell power generation (DFPG) has been presented. It has been shown via analysis that the islanding voltage depends on real power mismatch alone and the islanding frequency is a function of both real and reactive power. Following the analysis, the robust anti-islanding algorithm has been fully analyzed and developed. The algorithm consists of two steps. In the first step, it perturbs (±5%) the reactive power while continuously monitoring voltage and frequency. Islanding phenomenon is noticed when frequency deviation is observed. To positively confirm islanding, the output real power is reduced to 80% as a part of the second step. Islanding is confirmed when under voltage is observed. This method of detection has been shown to be robust and fast acting (operable in a cycle) and it significantly reduces the non-detection zone. Simulation and experimental results confirm the effectiveness of the proposed method.

CHAPTER IV

AN IMPROVED ANTI-ISLANDING ALGORITHM FOR UTILITY INTERCONNECTION OF MULTIPLE DISTRIBUTED FUEL CELL POWERED GENERATIONS

4.1 Introduction

Detecting the occurrence of islanding when a number of distributed fuel cell power generations connected to utility has always been a challenge. In the previous chapter, the robust anti-islanding algorithm for utility interconnection of a distributed fuel cell powered generation (DFPGs) has been developed. This method of detection has been shown to be robust and capable of reducing size of a non-detection zone (NDZ) to zero. However, it possibly fails to detect the occurrence of islanding when multiple DFPGs are connected to utility grid as the configuration shown in Fig. 4.1. The root cause of the failure results from dilution of the ±5% reactive power perturbation supplied from the DFPG while each of DFPGs independently operating in parallel to the same utility grid.

As a result, this chapter presents an improved anti-islanding algorithm for utility interconnection of multiple DFPGs. Islanding voltage and frequency are analyzed based on real and reactive power mismatches. The analysis shows that sizes of non-detection zones (NDZ) are larger when several DFPGs are independently operating in parallel to the same utility grid, hence elevating a chance of islanding to occur. Following the analysis, the cross correlation method is proposed and

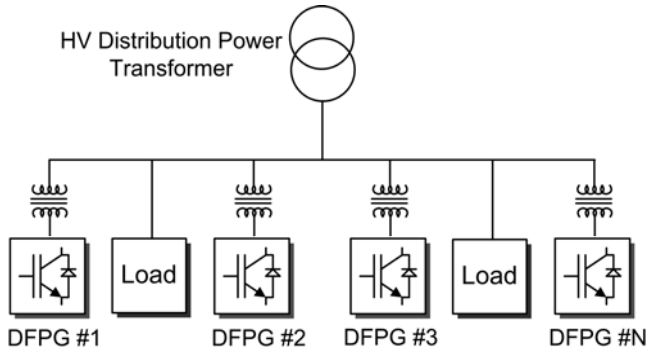


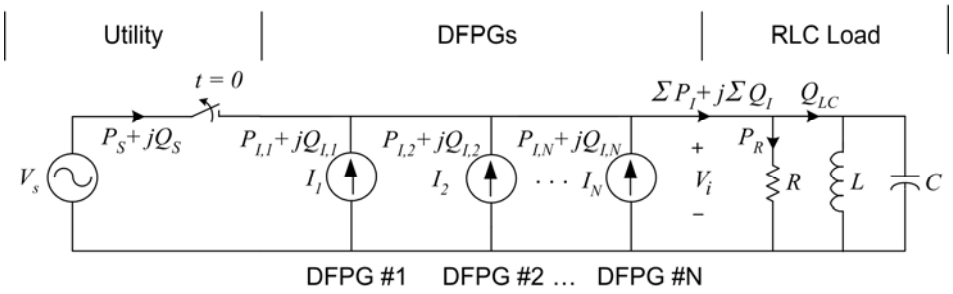
Fig. 4.1 Multiple DFPGs independently operate in parallel to utility

implemented in conjunction with the power control algorithm developed in the previous chapter. The power control algorithm continuously supplies (100%) the output real power and perturbs (±5%) the reactive power supplied by the DFPG while simultaneously monitoring the terminal voltage and the frequency. In parallel, the proposed method calculates the cross-correlation index of a rate of change of the frequency deviation with respect to (±5%) the reactive power. This index is used to confirm the occurrence of islanding. That is, in the presence of utility, the voltage at DFPG terminal and the frequency reside in the thresholds ($0.88 < V_i < 1.10$ per-unit and $59.3 < f < 60.5$ Hz) [6], [7]. Furthermore, the cross correlation index is relatively low (< 20%). If islanding were to occur, the cross correlation index rapidly increases above 50%. To further confirm the occurrence of islanding, the proposed method initiates ±10% the reactive power and continues to calculate the cross correlation index. If the cross correlation index exceeds 80%, islanding can be positively confirmed. The proposed method is shown to be robust and capable of detecting islanding in the presence of several DFPGs independently operating in parallel with

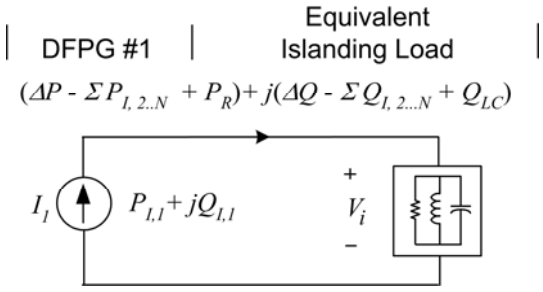
utility. The viability of the cross correlation method is demonstrated by the simulation of multiple DFPGs independently operating in parallel with utility under the worst case islanding condition and the results are discussed.

4.2 Analysis of Islanding Voltage and Frequency

Fig. 4.2(a) shows an equivalent circuit of DFPGs connected to a RLC load and utility. The DFPG #1 and other DFPGs supply sinusoidal waveform current to utility grid. They can be represented as ideal current sources. Real and reactive power consumed by the RLC load is supplied either from DFPGs or utility.



(a) Full description of an equivalent circuit of islanding



(b) A simplified equivalent circuit of the DFPG and the load

Fig. 4.2 Equivalent circuit of islanding load

Fig. 4.2(b) shows a simplified equivalent circuit. Real and reactive power supplied by the DFPGs #2 to #N and absorbed by the RLC load are combined and formed as an equivalent islanding load. This arrangement allows the DFPG #1 to be realized as a single inverter (DFPG) connected to the equivalent islanding load. Thus, the analysis of islanding voltage and frequency based on real and reactive power mismatches ΔP and ΔQ in Chapter III can be applied.

Let:

ΣP_I : Sum of real power from all DFPGs

ΣQ_I : Sum of reactive power from all DFPGs

$P_{I,\, i...N}$: Real power supplied from DFPGs unit $i...N$

$Q_{I,\, i...N}$: Reactive power supplied from DFPGs unit $i...N$

P_S : Real power supplied by utility before islanding

Q_S : Reactive power supplied by utility before islanding

P_R : Lumped load real power

Q_{LC} : Lumped load reactive power

ΔP : Real power mismatch at instant utility disconnected

ΔQ : Reactive power mismatch at instant utility disconnected

V_i : Inverter terminal voltage

V_n : Nominal system voltage

ω_i : Frequency of inverter terminal voltage

ω_n : Nominal system frequency

q : Quality factor ($q = R\sqrt{C / L}$)

Assumptions of the worst case islanding conditions:

- Real and reactive power mismatches are zero, $\Delta P = 0$ and $\Delta Q = 0$
- Resonant frequency of the RLC load is the same as the system frequency $\omega_n = 1/\sqrt{LC}$
- Reactive power of the RLC load is zero, $Q_{LC} = 0$

The islanding voltage can be derived in a function of a ratio of sum of the real power supplied from all DFPGs (ΣP_I) and the load real power (P_R) as,

$$V_i = \sqrt{\frac{\Sigma P_I}{P_R}} \cdot V_n \tag{4.1}$$

Voltage variation ΔV is defined as the voltage difference between islanding voltage and system voltage expressed as,

$$\Delta V = V_i - V_n \tag{4.2}$$

From (4.1) and (4.2), ΔV is derived in per-unit by

$$\frac{\Delta V}{V_n} = \sqrt{\frac{\Sigma P_I}{P_R}} - 1 \tag{4.3}$$

Let the real power supplied from the DFPG #1 be expressed as sum of real power $P^0_{I,1}$ and real power perturbation $\Delta P_{I,1}$. Also the reactive power supplied from DFPG #1 is expressed as sum of reactive power $Q^0_{I,1}$ and reactive power perturbation $\Delta Q_{I,1}$ as,

$$P_{I,1} = P^0{}_{I,1} + \Delta P_{I,1} \tag{4.4}$$

$$Q_{I,1} = Q^0{}_{I,1} + \Delta Q_{I,1} \tag{4.5}$$

From (4.4) and (4.5), $\Delta V/V_n$ in (4.3) can be expressed as,

$$\frac{\Delta V}{V_n} = \sqrt{\frac{P^0{}_{I,1} + \Delta P_{I,1} + \sum_{n=2}^{N} P_{I,n} - P_R}{P_R} + 1} - 1 \tag{4.6}$$

If real and reactive power perturbations supplied from the DFPG #1 were zero, real and reactive power mismatches are expressed as,

$$\Delta P = P^0{}_{I,1} + \sum_{n=2}^{N} P_{I,n} - P_R \tag{4.7}$$

$$\Delta Q = Q^0{}_{I,1} + \sum_{n=2}^{N} Q_{I,n} - Q_{LC} \tag{4.8}$$

Under the worst case islanding condition, real and reactive power mismatches are zero. From (4.7) and (4.8), $\Delta V/V_n$ in (4.6) is expressed in a function of real power perturbation supplied from DFPG #1 as,

$$\frac{\Delta V}{V_n} = \sqrt{\frac{\Delta P_{I,1}}{P_R} + 1} - 1 \tag{4.9}$$

Let a capacity ratio k_c be defined as a ratio of the real power supplied from the DFPG #1 to the load real power P_R expressed in per-unit as,

$$k_c = \frac{P^0{}_{I,1}}{P_R} \tag{4.10}$$

Voltage variation in (4.9) can be written in a function of a capacity ratio k_c as,

$$\frac{\Delta V}{V_n} = \sqrt{k_c \cdot \frac{\Delta P_{I,1}}{P^0{}_{I,1}} + 1} - 1 \tag{4.11}$$

The islanding frequency ω_i can be derived in a function of sum of real and reactive power (see (3.6)) as,

$$\omega_i \approx \frac{1}{\sqrt{LC}} \cdot \left(1 + \frac{\sum Q_I}{2q \sum P_I}\right) \tag{4.12}$$

Let frequency deviation $\Delta\omega$ be defined as the difference between islanding frequency and system frequency.

$$\Delta\omega = \omega_i - \omega_n \tag{4.13}$$

Due to assumptions, resonant frequency of the load is the same as system frequency $\omega_n = 1/\sqrt{LC}$. Thus, frequency deviation $\Delta\omega$ in (4.13) is derived and expressed as,

$$\Delta\omega = \frac{\omega_n}{2q} \cdot \frac{\sum Q_I}{\sum P_I} \tag{4.14}$$

From (4.7) and (4.8), frequency deviation $\Delta\omega$ in (4.14) can be expressed in a function of real and reactive power mismatches as,

$$\Delta\omega = \frac{\omega_n}{2q} \cdot \frac{\Delta Q_{I,1} + Q^0{}_{I,1} + \sum_{n=2}^{N} Q_{I,n}}{\Delta P_{I,1} + P^0{}_{I,1} + \sum_{n=2}^{N} P_{I,n}} \tag{4.15}$$

or

$$\Delta\omega = \frac{\omega_n}{2q} \cdot \frac{\Delta Q_{I,1} + \Delta Q + Q_{LC}}{\Delta P_{I,1} + \Delta P + P_R} \tag{4.16}$$

Following assumptions of the worst case islanding condition, real and reactive power mismatches are zero (ΔP = 0 and ΔQ = 0) and the RLC load reactive power is also zero (Q_{LC} = 0). Frequency deviation $\Delta\omega$ in (4.16) can be further simplified as,

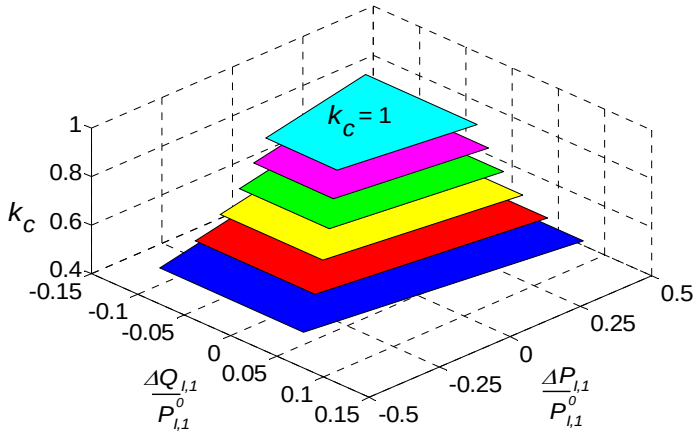
$$\Delta\omega = \frac{\omega_n}{2q} \cdot \frac{\Delta Q_{I,1}}{\Delta P_{I,1} + P_R} \tag{4.17}$$

Frequency deviation $\Delta\omega$ in (4.17) is expressed in a function of a capacity ratio k_c as,

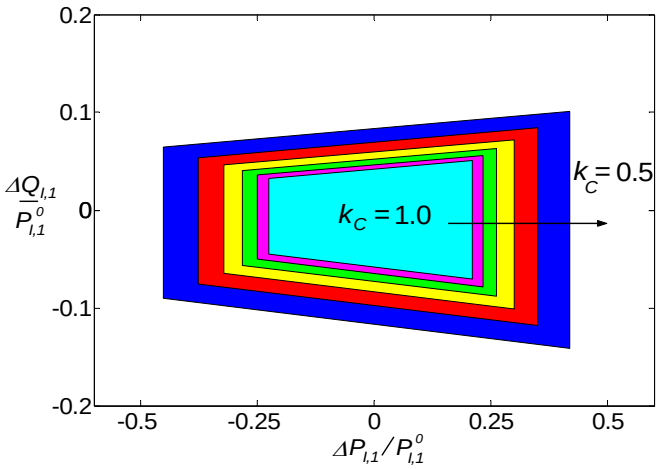
$$\Delta\omega = \frac{\omega_n}{2q} \cdot \frac{\frac{\Delta Q_{I,1}}{P^0{}_{I,1}}}{\frac{\Delta P_{I,1}}{P^0{}_{I,1}} + \frac{1}{k_c}} \tag{4.18}$$

Following the analysis, a small scale DFPG with $k_c << 1.0$ has been shown to have less potential to deviate the voltage or the frequency out of the thresholds after utility disconnected. Non-detection zones (NDZ) of the DFPG #1 under the worst case islanding condition with different values of a capacity ratio k_c are shown in Fig 4.3. It is noticed that non-detection zones (NDZ) expand from top to bottom while a capacity k_c is decreasing. Thus, it is concluded that the DFPG #1 with a small capacity ration k_c independently operating in parallel with other DFPGs has a higher chance of islanding to occur due to a larger non-detection zone.

To detect the occurrence of islanding effectively, the DFPG #1 and other DFPGs connected to utility should have been synchronized. Real and reactive power exported from each unit could have been controlled in the same direction allowing at least 20% real power mismatch and/or ±5% reactive power mismatch to be present. However, this ideal solution could not be happen. Thus, the cross correlation method is proposed to enhance reliability of the robust anti-islanding algorithm developed in Chapter III and detailed in the following sections.



(a) Various NDZ with different k_c



(b) Top-view of non detection zone (NDZ)

Fig. 4.3 Non-detection zones (NDZ) of the DFPG #1 under the worst case islanding condition

4.3 A Cross Correlation Function

Mathematical expression of a cross correlation function in discrete-time is expressed as,

$$c_{f\,[n]} = \frac{1}{K_{norm}}\left[\frac{1}{M}\sum_{k=0}^{M}\Delta\omega_{[k]}\cdot\frac{1}{\Delta Q_{I,1[n+k]}}\right] \tag{4.19}$$

and

$$K_{norm} = \frac{k_c\cdot\omega_0}{2q} \tag{4.20}$$

where M is a computation order (filter length) and K_{norm} is a normalized constant.

The expression in (4.18) is also known as a moving average of a rate of change of the frequency deviation $\Delta\omega$ with respect to ±5% the reactive power perturbation $\Delta Q_{I,1}$. If frequency deviation $\Delta\omega$ strongly depends on ±5% the reactive power perturbation $\Delta Q_{I,1}$, the cross correlation index c_f will rapidly increase in positive direction. However, if those two variables have no relationship, the cross correlation index c_f will vary near zero. This condition can occur only when the DFPG is connected to utility.

Fig 4.4 shows calculation of the cross correlation index. It is noticed that at lagging time $n = 6$, the frequency deviation $\Delta\omega$ and the reactive power perturbation $1/\Delta Q_{I,1}$ are perfectly correlated. It results in a significant increase of the cross correlation index $c_{f[6]} = 100\%$. Discrete-time realization of the cross correlation function (4.19) can be implemented similarly to a finite impulse response filter (FIR) as shown in Fig. 4.5.

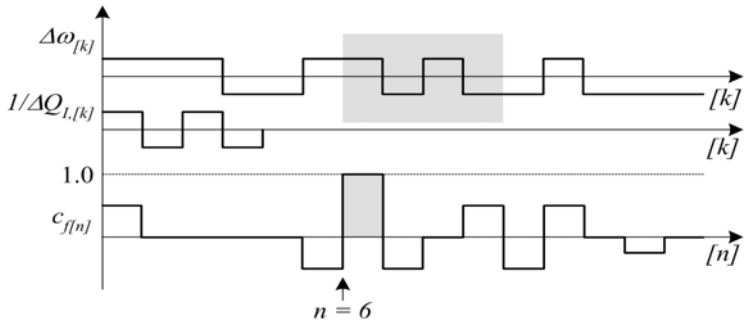


Fig. 4.4 Illustration of cross correlation index calculation

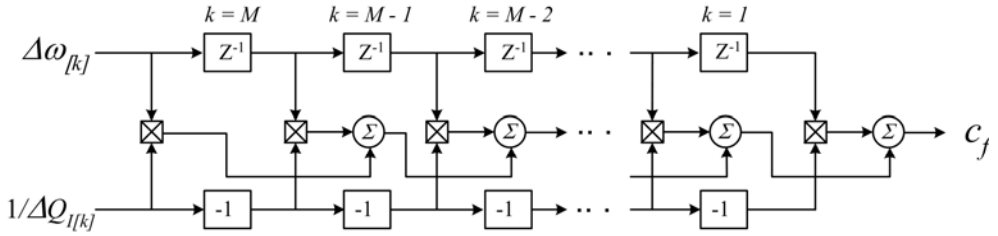


Fig. 4.5 Discrete-time realization of a cross correlation function

4.4 Proposed Cross Correlation Method

The proposed cross-correlation method is implemented in conjunction with the power control algorithm. That is, the power control algorithm constantly supplies (100%) the real power and (±5%) the reactive power given by (4.21) and (4.22) while simultaneously monitoring the voltage at inverter (DFPG) terminal and the frequency. Furthermore, the proposed correlation method calculates the cross correlation index of a rate of change of frequency deviation $\Delta\omega$ with respect to (±5%) the reactive power $\Delta Q_{I,1}$ supplied by the DFPG (see Fig. 4.2).

$$P^0{}_{I,1} = 1.0 \text{ (per-unit)} \tag{4.21}$$

$$\frac{\Delta Q_{I,1}}{P^0{}_{I,1}} = 0.05 \cdot sgn(V_i) \text{ (per-unit)} \tag{4.22}$$

The occurrence of islanding can be confirmed from the following three distinct situations.

1. If the voltage at inverter (DFPG) terminal or the frequency is out of the thresholds ($0.88 \le V \le 1.10$ per-unit and $59.3 \le f \le 60.5$ Hz) respectively as specified by IEEE Std 929-2000 [6] or IEEE Std 1547-2003 [7], the occurrence of islanding is immediately confirmed.
2. If the voltage and the frequency remain in the thresholds but the frequency deviation is greater than 1% ($\Delta\omega > 1\%$) by four consecutive cycles, the power control algorithm developed in Chapter III initiates (80%) the real power reduction. If the voltage falls below 0.90 per-unit, the occurrence of islanding can be confirmed.
3. If the voltage and the frequency reside in the thresholds and the frequency deviation is less than 1% ($\Delta\omega < 1\%$) but the cross-correlation index of a rate of change of frequency deviation with respect to (±5%) the reactive power is higher than 50% ($c_f > 0.50$), the proposed cross correlation method initiates (±10%) the reactive power increase and continues to calculate the cross-correlation index. If the cross-correlation index continues to increase above 80% ($c_f > 0.80$), the occurrence of islanding can be positively confirmed.

The proposed cross correlation method implemented in conjunction with the power control algorithm significantly enhances reliability of islanding detection. Flow chart of the proposed algorithm is shown in Fig. 4.6.

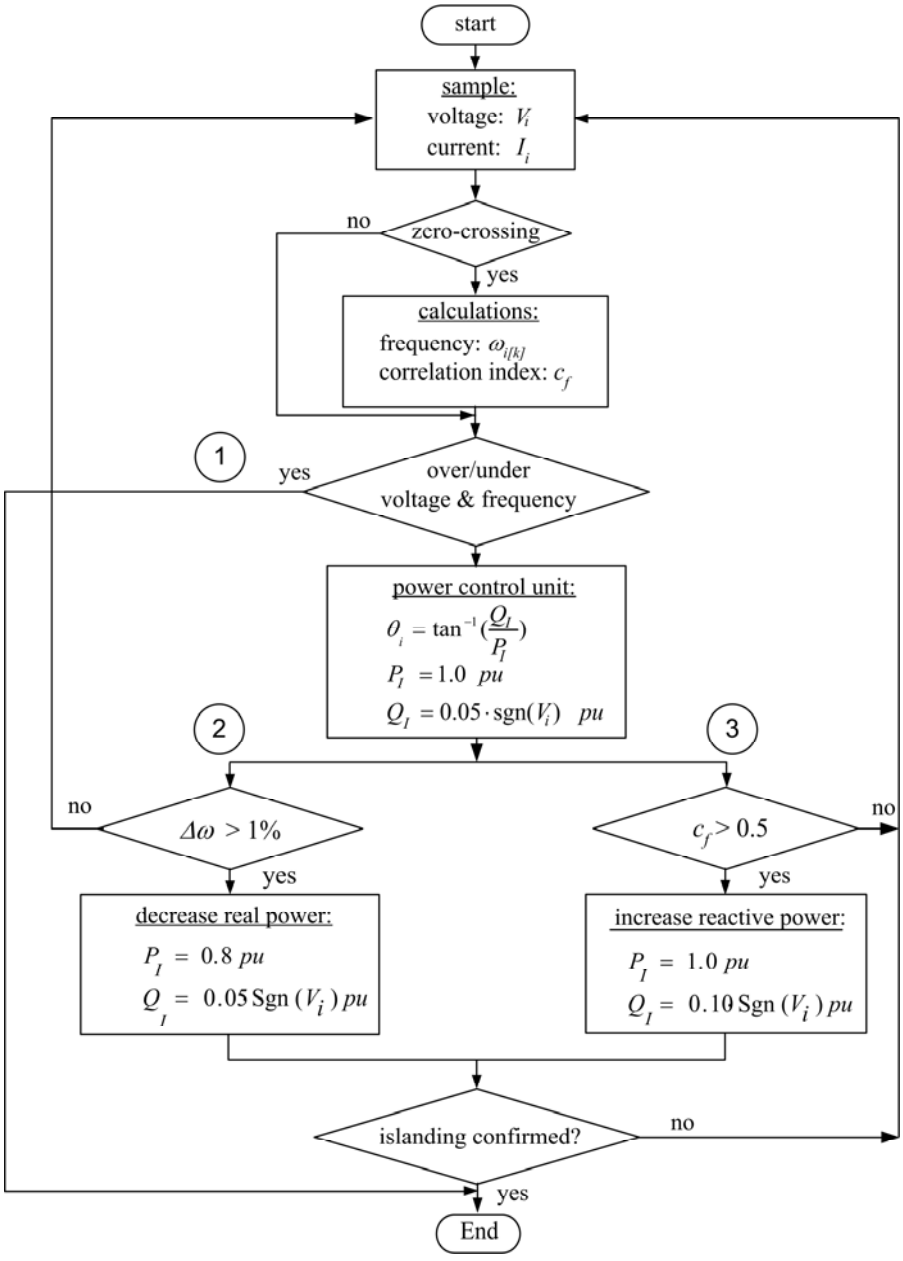


Fig. 4.6 A flow chart of the proposed cross correlation method

4.5 Simulation Results

To demonstrate viability of the proposed cross correlation method, multiple DFPGs independently operating in parallel to the utility grid and the RLC load is simulated under the worst case islanding condition. Fig. 4.7 shows a circuit diagram of the simulation. Simulation parameters and specification of DFPGs are shown in Table 4.1 and Table 4.2. Utility grid impedance is represented by a series resistor and inductor. DFPGs are operating in current mode control which they can be modeled as ideal current sources in the simulation. The proposed cross correlation method is implemented by the DFPG #1. Other DFPGs are assumed having over/under voltage and frequency detection method. The RLC load has load capacity of 5kW, load quality factor q = 2.5, and resonant frequency ω_n = 60Hz. The cross correlation function has a computation order of sixty ($M = 60$). At the instant utility disconnected, it is assumed that that real and reactive power mismatches are essentially zero $\Delta P \approx 0$, $\Delta Q \approx 0$.

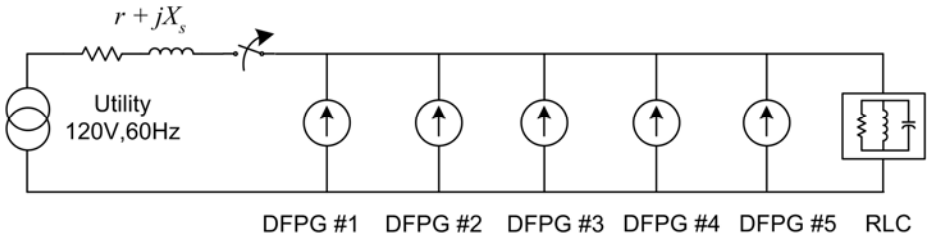


Fig. 4.7 A circuit diagram of simulation

Table 4.1 Simulation parameters

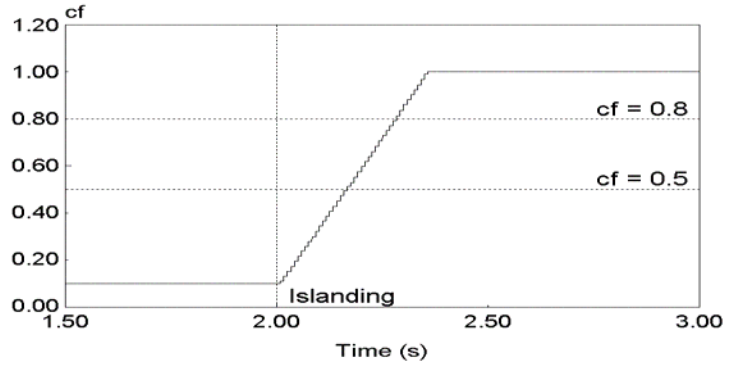
Parameters	Values
R	2.88 Ω
L	3.055 mH
C	2.303 mF
$r + jX_s$	0.05 + j0.01885 Ω

Table 4.2 Specifications of DFPGs

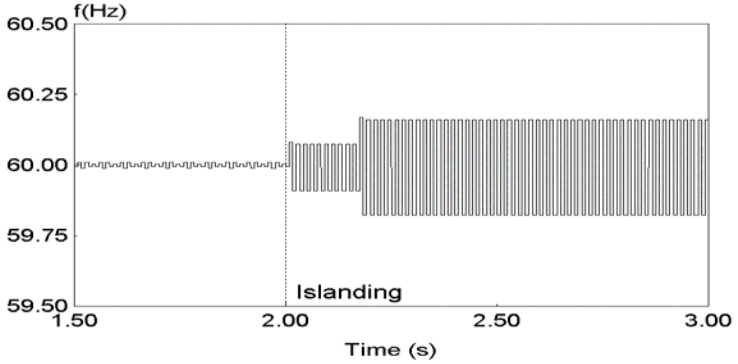
Specifications	DFPG #1	DFPG #2-5
Output power capacity	1 kW	1 kW
Voltage	120 ± 10%	120 ± 10%
Frequency	60.5 ~ 59.3 Hz	60.5 ~ 59.3 Hz
Islanding detection method	Proposed cross correlation method	Over/under voltage and frequency detection

Fig.4.8 shows simulation results of the proposed cross correlation method while each DFPG evenly supplies 0.20 per-unit real power output to utility (5×0.20 per-unit). In the presence of utility, the cross correlation index is relatively low ($c_f <$ 0.20) because (±5%) the reactive power supplied by the DFPG #1 is mostly absorbed by utility. Thus, frequency deviation $\Delta\omega$ becomes unnoticeable ($\Delta\omega <$ 1%). At the instant utility disconnected; the voltage at DFPG terminal and the frequency remain within the thresholds. It is shown that the power control algorithm developed in Chapter III fails to detect the occurrence of islanding. Nevertheless, the cross

correlation index c_f apparently increases as the frequency deviation occurred strongly depends on the (±5%) the reactive power perturbation. Until the cross correlation index is higher than 50% ($c_f > 0.5$), a chance of islanding is considered highly possible. Then, the algorithm initiates (±10%) the reactive power perturbation supplied by the DFPG #1 and continues to calculate the cross correlation index. Larger frequency deviation $\Delta\omega$ is suddenly observed. The cross correlation index exceeds 80% ($c_f > 0.80$) and the occurrence of islanding is now confirmed.

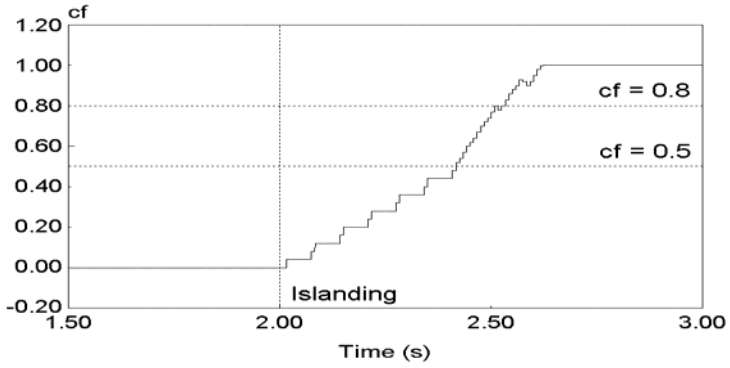


(a) The cross correlation index (c_f)

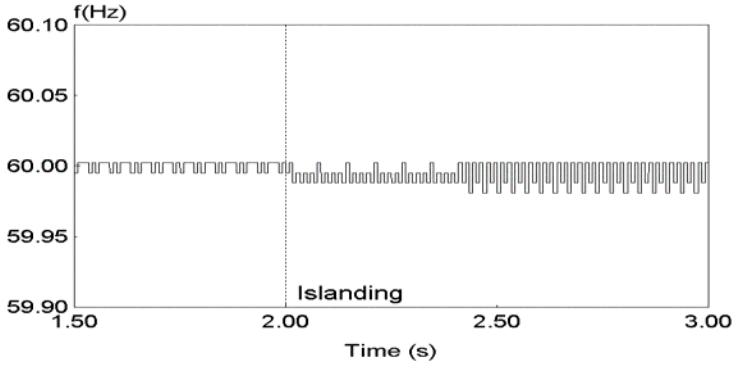


(b) Frequency of the terminal voltage

Fig. 4.8 Simulation results of the proposed cross correlation method ($k_c = 0.2$)



(a) The cross correlation index (c_f)



(b) Frequency of the inverter terminal voltage

Fig. 4.9 Simulation results of the proposed cross correlation method (k_c = 0.01)

Fig.4.9 shows another simulation to validate effectiveness of the cross correlation method while the DFPG #1 is connected to relatively large islanding load. The DFPG #1 is configured to supply 0.01 per-unit real power output while other DFPGs supplying 0.99 per-unit real power output. In the presence of utility, frequency deviation is very small ($\Delta\omega \approx 0.01$ Hz) and it varies randomly. It results the cross correlation index nearly equal to zero ($c_f \approx 0$). At the instant utility disconnected, the noticeable frequency deviation is observed. Its pattern follows that of (±5%) the

reactive power perturbation supplied from the DFPG #1. Thus, the cross correlation index c_f is gradually increasing. Until it is higher than 50% ($c_f > 0.5$), a chance of islanding is highly possible. To further confirm the occurrence of islanding, the algorithm initiates (±10%) the reactive power supplied from the DFPG #1. Larger frequency deviation is instantaneously observed and the cross-correlation index continues to increase. Islanding is positively confirmed when the cross-correlation index exceeds 80% ($c_f > 0.8$).

4.6 Summary

In this chapter, an improved anti-islanding algorithm for utility interconnection of multiple distributed fuel cell powered generations (DFPGs) has been presented. The cross correlation method has been proposed and implemented in conjunction with the power control algorithm developed in Chapter III. While the power control algorithm constantly supplied 100% the real power and ±5% the reactive power, the proposed method calculates the cross-correlation index to confirm the occurrence of islanding. If the cross-correlation is increasing above 50%, the proposed method initiates (±10%) the reactive power and continues to calculate the cross correlation index. If the index exceeds 80%, islanding can be confirmed. The viability of the proposed cross correlation method has been demonstrated by simulation. The results have been shown that the proposed method is robust and capable of detecting islanding in the presence of several DFPGs which are independently operating in parallel to utility.

CHAPTER V

CONCLUSION

5.1 Conclusion

Safety of utility personnel, equipment damage and system malfunction are major concerns possibly occurred due to islanding phenomenon. Several islanding detection methods have been discussed in Chapter I, however, each of them has been shown to fail. Thus, this dissertation has proposed a robust anti-islanding algorithm for utility interconnection of distributed fuel cell powered generations (DFPGs).

In the first study, DSP controlled power electronic converters for utility interconnection of DFPGs have been developed and they have been used to demonstrate viability of the proposed robust anti-islanding algorithm. Current control in a synchronous frame (dq-frame) utilizing PI controllers has been proposed. Real time control of digital current control in a synchronous frame, phase lock, and space vector PWM has been implemented by software using a commercially available DSP. The DSP based control has been shown to significantly enhance performance and flexibility of DFPGs. Simulation and experimental results show excellent performance.

In the second study, the development of a robust anti-islanding algorithm for utility interconnection of a DFPG has been explored. The power control algorithm has been proposed to eliminate a non-detection zone based on real and reactive power mismatch. The algorithm constantly supplies 100% the real power and ±5% the reactive power supplied by the DFPG. If islanding were to occur, frequency deviation takes place, upon which the real power is reduced to 80%. A drop in voltage confirms

the occurrence of islanding. This method of control has been shown to be robust and fast acting (operable in a cycle). Simulation and experimental results confirm effectiveness of the proposed algorithm.

In the third study, an improved anti-islanding algorithm for utility interconnection of multiple DFPGs has been presented. The cross correlation method has been proposed and implemented in conjunction with the power control algorithm. The proposed method calculates the cross correlation index of a rate of change of frequency deviation with respect to (±5%) the reactive power perturbation. If this index increases above 50%, chance of islanding is considerably high. To further confirm the occurrence of islanding, the algorithm initiates (±10%) the reactive power perturbation and continues to calculate the correlation index. If the cross correlation index exceeds 80%, islanding is confirmed. The proposed method has been shown to be robust and capable of detecting islanding in the presence of several DFPGs independently operating in parallel to utility. The viability of the proposed method has been demonstrated by the simulation.

5.2 Suggestion of Future Work

Continuation of the work in this dissertation could be focus on experiments to confirm viability and effectiveness of the proposed cross-correlation method. Further investigation could be focused on impacts of the proposed algorithm upon power quality when a large number of DFPGs connected to utility grid.

REFERENCES

[1] US Department of Energy, "Fuel Cells," [Online] Available: http://www.netl.doe.gov/publications/brochures/pdfs/fuel_cell.pdf, 1999.

[2] P. N. Enjeti, Chapter 8, "Power Conditioning Systems for Fuel Cell Systems," in *Fuel Cell Handbook*, 6th Edition, Morgantown, WV: U.S. Department of Energy, Office of Fossil Energy, National Energy Technology Laboratory, 2002.

[3] H. B. Puttgen, P. R. Macgregor, F. C. Lambert, "Distributed Generation: Semantic Hype or the Dawn of a New Era ?" *IEEE Power & Energy Magazine*, pp. 22-29, January/February 2003.

[4] T. E. McDermott, R. C. Dugan, "PQ, Reliability, and DG," *IEEE Industry Applications Magazine*, pp. 17-23, September/October 2003.

[5] Electric Power Research Institute, "Electricity Technology Roadmap: 2003 Summary and Synthesis", Tech. Rep. EPRI, Inc., Palo Alto, CA, November 2003.

[6] IEEE Standard 929-2000, *Recommended Practice for Utility Interface of Photovoltaic (PV) Systems*, IEEE, Inc., New York, NY, January 2000.

[7] IEEE Standard 1547-2003, *Standard for Interconnecting Distributed Resources with Electric Power Systems*, IEEE, Inc., New York, NY, July 2003.

[8] T. Basso, R. Deblasio, “IEEE 1547 Series of Standards: Interconnection Issues,” Tech Rep., National Renewable Energy Laboratory, Golden, CO, September 2003.

[9] M. E. Ropp, “Design Issues for Grid-Connected Photovoltaic Systems,” Ph.D. dissertation, Georgia Institute of Technology, Atlanta, GA, 1998.

[10] J. Stevens, R. Bonn, J. Ginn, S. Gonzalez, G. Kern, “Development and Testing of an Approach to Anti-Islanding in Utility-Interconnected Photovoltaic Systems,” Tech Rep., Sandia National Laboratories, Albuquerque, NM, August 2000.

[11] W. Bower and M. E. Ropp, “Evaluation of Islanding Detection Methods for Photovoltaic Utility-Interactive Power Systems,” Tech Rep. IEA PVPS T5-09:2002, [Online] Available: http://www.iea-pvps.org, 2002.

[12] H. Kobayashi, K.Takigawa, E. Hashimoto, “Method for Preventing Phenomenon of Utility Grid with a Number of Small Scale PV Systems,” in *Proc. 22nd IEEE Photovoltaic Specialists Conf*, 1991, pp. 695-700.

[13] H. Kobayashi, K. Takigawa, E. Hashimoto, A. Kitamura, H. Matsuda, “Problems and Countermeasures on Safety of Utility Grid with a Number of Small-Scale PV Systems,” in *Proc. Photovoltaic Specialists Conference*, Vol. 2, May 1990, pp. 850-855.

[14] A. Kitamura, M. Okamoto, F. Yamamoto, K. Nakaji, H. Matsuda, K. Hotta, “Islanding Phenomenon Elimination Study at Rokko Test Center,” in *Proc. 1st*

IEEE World Conference on Photovoltaic Energy Conversion, Part 1, 1994, pp. 759-762.

[15] G. A. Kern, "Sunsine300 Utility Interactive AC Module Anti-Islanding Test Results," in *Proc. 26th IEEE Photovoltaic Systems*, 1997, pp. 1265-1268.

[16] G. A. Smith, P. A. Onions, D. G. Infield, "Predicting Islanding Operation of Grid Connected PV Inverters," in *Proc. IEE Electrical Power Application*, Vol.147, No.1, pp. 1-6, January 2000.

[17] S. Yuyuma, T. Ichinose, K. Kimoto, T. Itami, T. Ambo, C. Okado, K. Nakajima, S. Hojo, S. Shinohara, S. Ioka, M. Kuniyoshi, "A High Speed Frequency Shift Method as a Protection for Islanding Phenomena of Utility Interactive PV Systems", *Sol. Energy Materials, Sol. Cells*, Vol. 35, Issue 1-4, 1994, pp. 477-486.

[18] G. K. Hung, C. C. Chang, C. L. Chen, "Automatic Phase-Shift Method for Islanding Detection of Grid-Connected Photovoltaic Inverters," *IEEE Transaction on Energy Conversion*, Vol.18, No.1, March 2003, pp. 169-173.

[19] M. E. Ropp, M. Begovic, A. Rohatgi, "Analysis and Performance Assessment of the Active Frequency Drift Method of Islanding Prevention," *IEEE Transactions on Energy Conversion*, Vol. 14, No.3, pp. 810-816, September 1999.

[20] Draft DIN VDE 0126:1999, *Automatic Disconnection Facility for Photovoltaic Installations with a Nominal Output < 4.6 kVA and a Single-Phase Parallel Feed by Means of an Inverter into the Public Grid* (*German*

National Standard for Utility Interconnection of Photovoltaic Systems), DKE German Commission for Electrical, Electronics & Information Technologies of DIN and VDE, Frankfurt am Main, Germany, 1999.

[21] M. E. Ropp, K. Aaker, J. Haigh, N. Sabbah, "Using Power Line Carrier to Prevent Islanding," in *Proc. Photovoltaic Specialist Conference*, September 2000, pp. 1675-1678.

[22] M. Prodanovic, T. C. Green, "Control and Filter Design of Three-Phase Inverters for High Power Quality Grid Connection," *IEEE Trans on Power Electronics,* Vol.8, No.1, pp. 373-380, January 2003.

[23] A. Von Juanne, P. N. Enjeti, D. J. Lucas, "DSP Control of High-Power UPS Systems Feeding Nonlinear Loads," *IEEE Transactions on Industrial Electronics*, Vol. 43, No.1, pp. 121-125, February 1996.

[24] M. Cichowlas, M. P. Kazmierkowski, "Comparison of Current Control Techniques for PWM Rectifiers," *in Proc. IEEE International Symposium on Industrial Electronics*, Vol. 4, 2002, pp. 1259-1263.

[25] J. Ching Liao, S Nian Yeh, "A Novel Instantaneous Power Control Strategy and Analytic Model for Integrated Rectifier/Inverter Systems," *IEEE Transactions on Power Electronics*, Vol. 15, No.6, pp. 996-1006, November 2000.

[26] V. Blasko, V. Kaura, "A New Mathematical Model and Control of a Three-Phase AC-DC Voltage Source Converter," *IEEE Transactions on Power Electonics*, Vol. 12, No. 1, pp. 116-123, January 1997.

[27] H. Willi Van Der Broeck, H. Christoph Skudelny, “Analysis and Realization of a Pulsewidth Modulator Based on Voltage Space Vectors,” *IEEE Transactions on Industry Applications*, Vol. 24, No. 1, pp. 142-150, January-February 1998.

[28] Texas Instruments, *TMS320 F/C24X DSP Controllers CPU and Instruction Set Reference Guide*, Houston, TX, March 1999.

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