MODIFICATION OF TRACK AND HOLD NETWORKS FOR IMPROVED BANDWIDTH AND SAMPLING ACCURACY IN HIGH-Q ANTENNA SYSTEMS

A Thesis

by

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MASTER OF SCIENCE

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ABSTRACT

Increased interest in mixer-first receiver architectures has been primarily driven by the need for compact receivers capable of operating across a wide range of frequencies, particularly in edge devices and software-defined radios (SDR). Matching between a receiving antenna and subsequent RF components is inherently poor but can be improved through narrowband matching networks. These networks limit the antenna's bandwidth, distorting short-duration pulsed signals, and may not offer significantly reduced loss. The design proposed in this paper is a modification of existing sample and hold circuits, such as those applied in mixer-first receivers, to provide a reflectionless match without the need for additional matching networks between an antenna and the direct sampling stage. This was done using circuit-level simulations in Keysight Pathwave ADS with ideal components. Results from the current work indicated that the modified sampling network could nullify ringing after very short duration pulses, provides a reflectionless match to a wide range of source impedances, accurately sample monocycle signals from highly reactive sources, and sample with low loss.

DEDICATION

To my parents, for all the love and support they have given me. Without that support, I could not have made it so far. Thank you to everyone who has helped me along the way.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supervised by a thesis committee consisting of Professor Katehi (advisor), Professor Wright, Professor Entesari of the Department of Electrical Engineering, and Professor Howard of the Department of Mathematics.

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1. INTRODUCTION

Modern wireless devices must access and employ an ever-increasing number of communication bands. For example, Long-Term Evolution (LTE) has discrete bands from 400 MHz to nearly 6000MHz, even without including more recent developments such as 5G frequency range which extends to double-digit GHz bands. This has led to significant interest in low-power RF front ends with very wideband operation, such as mixer-first and direct sampling receivers. These designs introduce new challenges and constraints when compared to conventional receivers.

Mixer-first designs are implemented to increase bandwidth by reducing the number of RF components [1]. By immediately mixing the signal received by the antenna down to an intermediate frequency (IF), amplification, filtering, and digitization are performed at a much lower frequency. Thus, the only component which needs to function at RF will be the front-end mixer. As a result, the specifications of amplifiers, filters, and other RF components in the signal path may be reduced. Passive mixer-first receivers are a specific implementation of mixer-first receivers, using direct sampling at the antenna to implement sampled mixers [2].

Direct sampling receivers (DSR) are of interest for similar reasons. Sampling directly at RF frequencies typically reduces the complexity of the design. For this thesis, the interest is primarily in DSRs and passive mixer-first receivers that directly sample the received signal. As in passive mixer-first designs, the sampling network modification presented in this thesis are most valuable when connected to an inductive antenna because of greater distortion during the transient period. When electrically small antennas are used, such as in most edge devices, the impedance presented by the antenna tends to be complex with a significant reactive component [3]. This direct antenna-receiver interface results in distortions caused by an impedance mismatch, such as

reflections and transient ringing, mainly when presented with short-duration signals. More significant impedance mismatches result in worse effects on the signal and conventionally require an antenna-receiver co-design to achieve acceptable performance. Signals composed of very short pulses, such as monocycle sinusoids, result in significant ringing, which distorts future signals [4, 5]. The design proposed in this thesis aims to reduce reflections between the antenna and to remove ringing without introducing additional filters, matching networks, or other bandwidth-limited components in front of the sampling network. This allows the receiver to maintain its wideband performance and reduces the need for matching elements that may limit bandwidth. Further, with inductive antennas, the circuit topology is similar to that of a switched-mode boost converter and may introduce an intrinsic voltage gain. This is particularly useful since direct sampling prohibits the implementation of a preamplification stage.

This thesis is divided into six chapters described below. Chapter 2, "Background", explains in detail the fundamental concepts, including an overview of sampling theory, sample and hold circuits, passive mixers, and transient distortion effects existing encoding schemes and communication standards. Chapter 3, "Literature Review", summarizes relevant research in several papers, which were used as a basis for the proposed design in this thesis. The literature presented herein establishes common elements in early-sampling designs and demonstrates that there is a known problem regarding transient performance. Chapter 4, "Theory and Design" covers the mathematical model for the proposed design as well as a detailed description of the circuit. Chapter 5, "Test Setup", is split into two sections. Section one covers the setup and goals for tests on distortion removal, primarily shown in the time domain. Section two covers the design and goals for tests on sampled voltage amplitude and other factors best shown in the frequency domain. Chapter 6, "Results", provides the analysis and reviews the results obtained from those tests.

Additionally, it compares the performance of this new design to an unmodified sampling network. Chapter 7, "Conclusions", concludes the presented data and discusses potential applications and future work.

2. IDENTIFICATION OF PROBLEM STATEMENT, BACKGROUND, AND LITERATURE REVIEW

2.1 Problem Statement

When receiving a signal, best practice dictates minimizing reflections/distortions and maximizing power transferred to the sampling network. This is typically achieved by matching the characteristic impedances of the source and load. Conventional time-invariant matching networks are often used which can come in various implementations, from transmission line designs to lumped element networks. These networks typically have limited bandwidth due to wavelength-dependent designs or resonances at specific frequencies and can incur significant power loss when a considerable mismatch occurs [6]. Bandwidth limitations are rarely a concern when receiving a long signal under the Nyquist cut-off frequency. Still, pulsed transmissions and very short duration symbol periods can create very wide frequency responses, as short pulses in the time domain result in wide signals in the frequency domain. Thus, the bandwidth of a sampling network can be limited by the preceding matching network due to the impedance and reflection of frequencies outside its design frequency band and the often-narrow width of the passband.

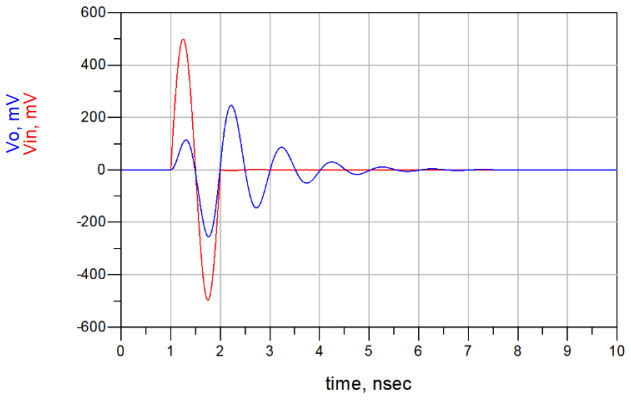

Figure 2.1: Ringing example
Pulse input (red) and resulting ringing on load (blue)

Figure 2.1 shows the transient result of a short pulse transmitted to a load matched for maximum transmitted power. Although the phase on the output signal matches the source phase during the pulse period, significant energy is stored between the capacitive and inductive elements of the matching network and the source. This energy storage results in resonance, appearing as a ringing distortion of the signal, and is a result of the multiplication of the transmitted sine wave and a 1ns wide rectangular pulse introduced by the 1ns transmission window. Typically, the desired part of the signal is the sine wave's phase, amplitude, and frequency [7]. Transforming the signal (on the load) in the frequency domain would result in the sine wave convoluted with the rectangular pulse function and the exponential decay after that. This would distort the amplitude and phase of the interpreted signal. If phase shift keying (PSK) or some similar encoding method is used, this could introduce an error when decoding the symbol. There are computational methods for removing the unwanted effect of the transmission window. However, they require information on the transmission duration and can decrease the data rate if the processing duration exceeds the symbol duration. The computational requirements grow as more symbols are transmitted, especially if the conditions vary. Sequential symbols may be affected by stored energy from the previous signal, changing the measured amplitude and phase of differing symbols.

A Binary Phase Shift Keying (BPSK) modulation is used as an example during the modified sampling network's testing. This modulation applies a 0-degree or 180-degree phase shift to the carrier frequency to convey a "0" or "1" symbol. If the signal is sufficiently distorted that the waveform cannot be read as 0 or 1 or is read as the opposite, this will form an error during data recovery from the signal. In transmissions with very long symbol lengths relative to the carrier frequency's period, the risk of error is low because a given symbol will be transmitted long enough

for any transient-state inter-symbol interference (ISI) to fade. This ISI duration limits how short a signal can be, and with the constantly increasing demand for faster transmission rates, it can be a significant design constraint. Sampling networks undergo similar distortions despite being significantly different from simple, complex loads. The primary goal of the design in this thesis was to remove the distortion of non-continuous signals and improve bandwidth for a wide range of complex impedances. Further, since development began with mixer-first receivers in mind, the design's ability to function in a parallel configuration was also investigated. Implementation focused on mixer-first and direct sampling receiver architectures to identify improvements for impedance matching, bandwidth, and short-duration signal sampling.

2.2 Background

A basic sample and hold network consists of a switch to control current flow, a capacitor to hold the sampled voltage, and a buffer with high input impedance to prevent current leakage while providing the capacitor's voltage for further use in the receiver.

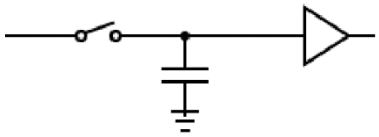

Figure 2.2 Basic sample and hold circuit

These circuits (Figure 2.2) can be set up in parallel and are typically controlled through non-overlapping clock signals (Figure 2.3). The lack of overlap ensures that only one capacitor receives current at any given time. Thus the input "sees" only one capacitor for the entire operational duration. This is important for consistent sampling since every branch's circuit should be identical during the sampling state. Meanwhile, charge on a given capacitor at the start of the

track state may vary, and is dependent on the voltage when the preceding hold state began minus any parasitic losses.

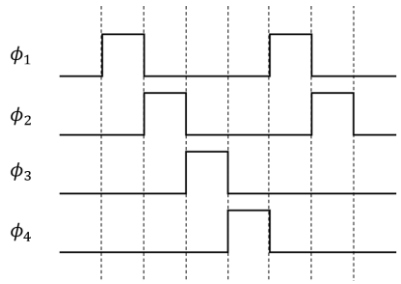

Figure 2.3 Non-overlapping clock example

Parallelized sample-and-hold networks can increase sampling or function as a mixer. If a 0/180 phase shift is present between two paths, and they are recombined to form one sample, then mixing occurs. Figure 2.7 and the following paragraph cover this mixing method. If each path is used to record separate samples at independent points in time, then the available sampling rate increases such that an N-path sampling network has an effective sampling rate of Nf_s where f_s is the sampling frequency of a single branch.

With a purely real source and a capacitor with a sufficiently short time constant RC, a sampling capacitor's voltage will track the input signal accurately. When the switch opens, the capacitor maintains its charge, and the voltage is constant. (Figure 2.4)

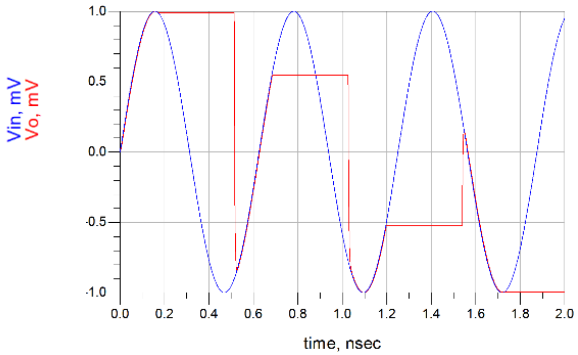

Figure 2.4 Sampling example
The input signal voltage (blue) and sampling capacitor voltage (red) as a function of time

Adding reactive components, however, can lead to significant distortions during the track state. In the time domain, these are primarily due to overshoot, delay, and ringing (Figure 2.5) and can affect the accuracy of future samples and create spurious tones in the frequency domain. The hold state's performance remains unchanged since the source is disconnected from the capacitor during this time due to the resonance between the sampling network and the source.

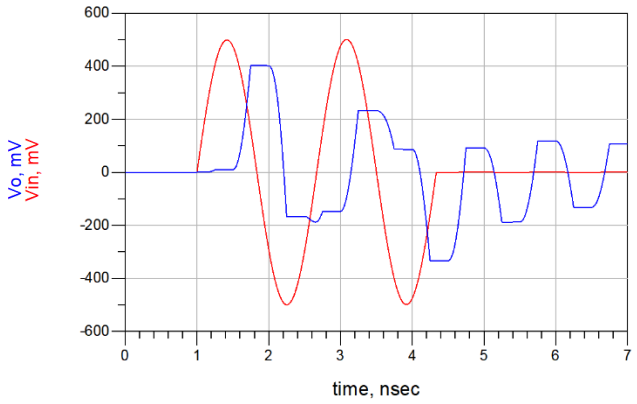

Figure 2.5 Sample and hold transient plot for an inductive source
The input signal (red) and the resulting ringing on load (blue)as shown as a function of time

This error also translates to the frequency domain, as seen in Figure 2.6. There is significant distortion compared to the ideal frequency transform of the above input signal (red). The ideal result was obtained by directly sampling the input signal in MATLAB at the same frequency as the sampling network. The information which may have been held in that two-cycle pulse was irrecoverable, with no clear evidence of the original 0.6 GHz signal.

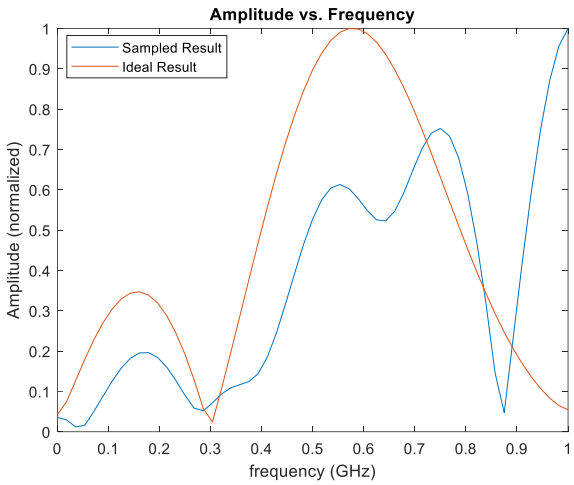

Figure 2.6 Sample and hold frequency domain plot for an inductive source

Mixers can be implemented using switched circuits. In its simplest form (Figure 2.7), the switched mixer consists of a 0/180^{o} split, with a switching rate equal to the LO frequency between the two phase-offset channels. This results in the formation of IF frequencies such that IF=|RF ± LO|. Other tones are also generated, especially if multiple RF frequencies are present at the output, but these are existing methods for removing these.

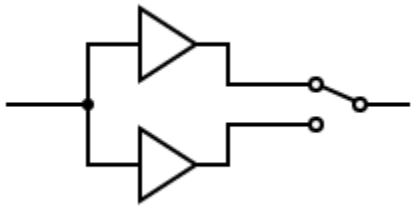

Figure 2.7 Basic switching mixer

Mixer-first receivers take advantage of this property [8-10] and implement 0/180 switched paths directly or as part of a front-end sampling network. The latter is prevalent in Software Defined Radio (SDR) receivers. There are various specific implementations [11, 12], which perform direct sampling at the antenna.

2.3 Literature Review

Sample and Hold circuits have been a vital component of RF receivers since the need for signal digitization first appeared. Early designs were applied at the very tail end of a receiver architecture immediately before the digitization of the signal using an Analog Digital Converter (ADC). Transistor technologies severely limited the possible switching rate, preventing sampling at RF. Signal reconstruction requires sampling at no less than twice the maximum frequency of interest, as per Nyquist Theorem, and early transistors did not sample in the GHz range. As CMOS technology has improved, so has the switching rate [13], and thus the application of switched networks has migrated toward the front of the receiver path. The ability to sample at GHz frequencies has permitted the application of switched mixer-first receivers [1] and N-path filters [9] for applications such as Wi-Fi and LTE. Figure 2.9, taken from[10], shows the basic model for a (single-ended) I/Q passive mixer.

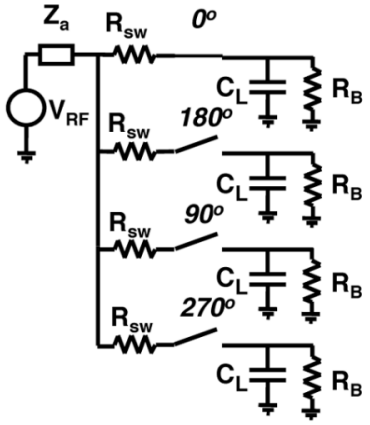

Figure 2.8 Model of 4-phase passive mixer with sampling capacitor C_L and variable load resistor R_B
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It is important to note that the variable resistor R_B is chosen to be sufficiently large such that the voltage across the sampling capacitor C_L does not change significantly during one sampling cycle ($\tau_{RC} \gg \tau_s$). The network is directly connected to the source (with V_{RF} as the signal and Z_a as the impedance of the antenna) and has no preceding amplifiers or matching networks. The buffers or any following circuits are not shown, as the paper focuses on an 8-phase passive mixer design. Figure 2.10 shows the complete block diagram for the 8-phase design, in which the signals are sampled, buffered, and combined to form the differential I and Q signals.

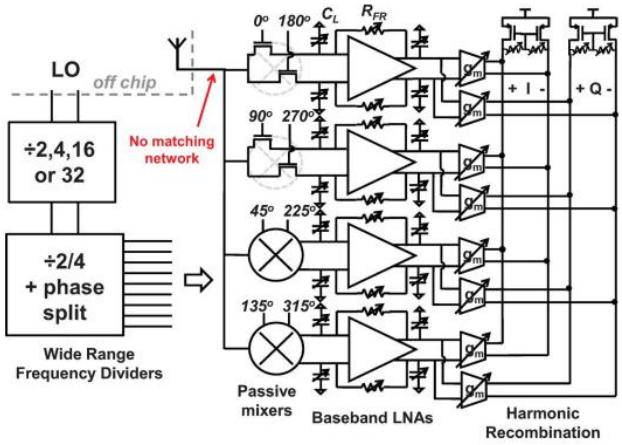

Figure 2.9 The block diagram of a receiver, including frequency dividers, passive mixers, baseband LNAs, and recombination buffers

Of interest is that the antenna is assumed to be a 50Ω impedance with little reactive deviation for the frequency band of interest, and the authors note that their constant Z_a model is, therefore, limited. This problem is encountered by other papers using similar methods, such as [8], which focused on reconfigurable passive mixers. In that design, the matching problem was solved by having tunable elements in the front end, which shifts its impedance to better match the antenna at the frequency of interest. Generally, these receivers are designed with naturally well-matched antennas in mind. Without additional matching networks, their effectiveness with electrically small

antennas (ESA) would be limited. ESAs typically have low resistance and high reactance in the band used and see significant mismatch when connected to a 50Ω network.

A paper on matching schemes for time-varying matching networks [5] provided insight into time-domain techniques for improving matching and bandwidth, particularly in enhancing the reception of pulsed signals. That design requires knowledge of when the signal arrives and sets the initial conditions for the reactive components such that the load maximally absorbs the incoming signal. Figure 2.10 shows a network designed to receive a sinusoidal monocycle and match some input and a 50Ω load.

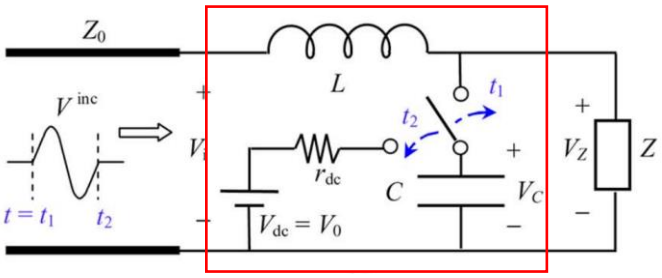

Figure 2.10 time-varying matching network for a sinusoidal monocycle signal
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The section within the red box replaces a conventional matching network. The extended work [14] is for a design that optimizes the power received from an antenna and achieves a significant bandwidth increase. This allows the time-variant matching network to not only remove the ringing present when using conventional matching networks (Figure 2.11, top (b) graph), but it can also increase the voltage swing seen by the load.

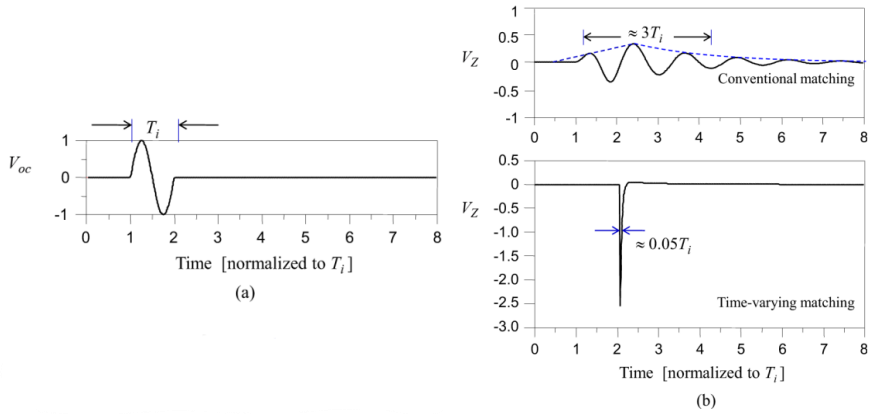

Figure 2.11 An incoming monocycle signal (a) and load voltages for conventional and time-varying matching (b)
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This was observed when the modified network was fed via a loop antenna, which is generally inductive [3]. In a passive mixer-first receiver, achieving increased voltage swing in the sampling stage would effectively provide "gain" and help counteract some disadvantages of not using a preamplifier.

The simulation setup of [14] used the loop antenna lumped element model found in [15]for simulations and validated the results with measurements. That paper's lumped element model proved to be invaluable for the tests performed in this thesis as well. Finding a lumped element dipole model proved straightforward, [16] presented a simple model with reasonable accuracy at frequencies such that the dipole half-length is below one-tenth of a wavelength.

3. THEORY AND DESIGN

3.1 Design Basis

Due to the periodic time-varying nature of sampling networks, design, and analysis were primarily focused in the time domain. This allows taking advantage of unique properties in the switched capacitor network that would not have been feasible in time-invariant designs. In particular, it is also easier to investigate transient effects such as short-duration transmissions or the resulting distortion in encoded symbols.

The key mechanism in the design presented in this work is the complete discharge of the sampling capacitor before reconnection with the source. This resets each sampling branch to zero voltage shortly before the track state, removing any state memory carrying over between sampling cycles (Figure 3.1). Without that previously held charge being released back into the network, sampling at any given time will be identical to the initial samples taken. There is no transient charge-up period as the sampling capacitor stored energy reaches a steady state with the reactive elements of the source antenna. The initial charge on a capacitor is maintained throughout the sampling and ensures that energy stored from previous sample cycles is not re-introduced into the system and distorts future samples. Equations (3.1) through (3.4) show this principle mathematically. Since sample and hold networks drive high impedance buffers, the energy lost by discharging sampling capacitors to ground does not result in additional losses. However, the total voltage swing for a given signal may be reduced if a conventional sampling network establishes a resonance with the complex source and boosts the received voltage. Similar architectures have been investigated in the past [17-19] for error compensation and offset calibration.

A B

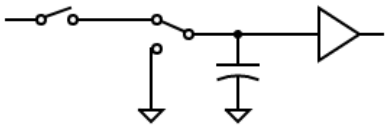

Figure 3.1 Modified sampling network

3.2 Modified Sample and Hold

The leftmost switch is Switch A, and the rightmost changeover switch is Switch B. Switch A is open on Low and closed on High. B connects between the left switch and capacitor (position 1) when High and between the capacitor and ground (position 2) on Low.

Figure 3.2 is a graph depicting the switch control signals with two full sampling periods, 0.5 nanoseconds each. State 3 is where both signals are high, 0-0.25nS. State 2 is low A, and high B, 0.25-0.45nS, and state 1 are both A and B low, 0.45-0.50ns.

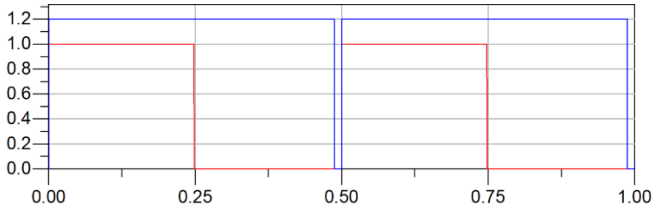

Figure 3.2 Clock signals for a single sampling branch.
Switch A Control Line signal (red) and Switch B Control Line signal (blue)

The switched capacitor branch occupies one of three states. Starting in State 1, Switch A closes, and Switch B switches to position 1, allowing the capacitor to "track" the incoming voltage by gaining a charge q such that $V = q/C$. The accuracy of the tracking is dependent on the same principles as a conventional track-and-hold network. In state 2, Switch A opens, where it "holds" the voltage across the capacitor constant. Switch B remains in the same position. The right-hand side of the network would connect to a buffer, typically consisting of an amplifier, with a very high input impedance. In a typical CMOS-implemented system, a small amount of current will

leak through parasitic effects, and extra capacitance from the transistors will be present. However, a good design will minimize these effects. During this time, the voltage along the capacitor can be converted by an ADC or otherwise read by the next stage in the receiver. State 3 has Switch B move to the bottom position and is very short, and "resets" the voltage on the capacitor to 0, draining all charge by shorting it to ground. Switch B is then moved back to the top position to reconnect the capacitor with Switch A and allow sampling to occur. Even if switch A closes with switch B in the "down" position, there will be no connection between switch A and B.

For the modified circuit, these three states can be represented in Figure 3.3, showing both the circuit as a whole and as a simplified circuit diagram.

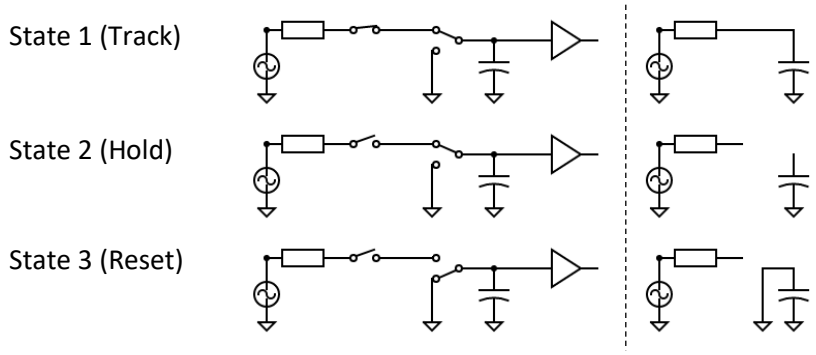

Figure 3.3 Modified sampling network states (left) and simplified circuit diagrams (Right)

This modified design results in two important mechanics; firstly the switched capacitor is now a memoryless device preventing the previous sample's information from contaminating the next information, as the modification stops the stored charge from reflecting into the system and disrupting the incoming signal. Equations (3.2) and (3.3) represent the generalized form of the voltage across the sampling capacitor at a time *t*, for a conventional sampling network and modified sampling network respectively. The current through sampling network *I(t)* and charge

across the capacitor *Q(t)* are left time-dependent to keep the equations short. Equation (3.1) simply shows that the term $R_{source}(t)$ is derived from the impedance of the source.

$$(3.1)\ R_{source}(t) = \mathcal{F}^{-1}(Z_{source}(f))$$

$$(3.2)\ V_s(t) = \begin{cases} \mathrm{V_{in}}(t) - I(t)R_{source}(t) + \frac{Q(kt_{start})}{C_s} e^{-\frac{t}{R_{total}C_s}}, & t_{start} \le t \le t_{hold} \\ \frac{Q(t_{hold})}{C_s}, & t_{hold} < t \le t_{period} \end{cases}$$

As (3.2) shows, the voltage for a given sampling period is intrinsically dependent on the previous value. The charge held during a previous sampling period affects the voltage during the following period. For a purely resistive source and small sampling capacitor, *I(t)* and *Q(t)* work out such that any charge is dissipated through losses in the network. In the case where the reactance is sufficiently large, and resistance is small, V_s may be affected by the previously stored charge. R_s is the parasitic resistance of the sampling capacitor.

$$(3.3)\ V_s(t) = \begin{cases} \mathrm{V_{in}}(t) - I(t)R_{source}(t) + \frac{Q(t_{start})}{C_s} e^{-\frac{t}{R_{total}C_s}}, & t_{start} \le t \le t_{hold} \\ \frac{Q(t_{hold})}{C_s} e^{-\frac{t}{R_s C_s}}, & t_{hold} < t \le t_{reset} \\ \frac{Q(t_{reset})}{C_s} e^{-\frac{t}{R_{drain}C_s}}, & t_{reset} < t \le t_{period} \end{cases}$$

Since the RC constant of the path to ground in State 3 should be as short as possible, the sampling capacitor voltage can be approximated as 0, and thus the charge presented at the start of any sampling period would also be 0, and the sampled voltage loses any dependency on previous states.

$$(3.4)\ V_s(t) = \begin{cases} \mathrm{V_{in}}(t) - I(t)R_{source}(t), & t_{start} \le t \le t_{hold} \\ \frac{Q(t_{hold})}{C_s} e^{-\frac{t}{R_s C_s}}, & t_{hold} < t \le t_{reset} \\ 0, & t_{reset} < t \le t_{period} \end{cases}$$

This effectively improves the sampling network bandwidth in regard to sharp pulse boundaries. The shorting of the capacitor before sampling prevents lingering reflections between the reactive elements in the input and the sampling network. Antennas, in particular, can store significant amounts of energy. Reflections can "ring" between the sampling network and an

antenna and last long enough to affect future samples. This effect becomes cumulative, potentially altering the phase and amplitude seen by the sampler, and the resulting intersymbol interference may introduce errors when decoding the received data. The modification presented removes this nonlinearity and, by immediately functioning in a steady state, allows for a more accurate reconstruction of the incoming signal.

The modified sample and hold network can be parallelized for configurations such as the front-end sampling in [10]. This circuit is set up as in Figure 3.4, with each sampling capacitor branch connected in parallel. The change in timing is that the duration t_1, the track duration, becomes $t_1 = \frac{1}{Nf_s}$, where N is the number of sampling branches.

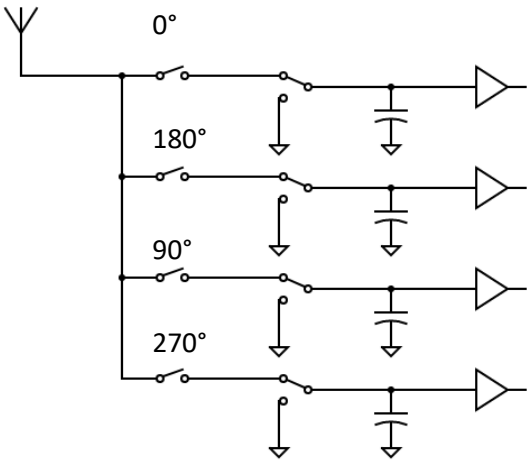

Figure 3.4 A 4-phase sampling network

The tests performed in Chapter 5 use the network in Figure 3.4 to better observe the impact of the modification in an I/Q passive mixer-first receiver. After confirming that it worked in both single and quadrature configurations, results were measured for the quadrature design.

4. METHODS

4.1 Simulation Environment

The simulation environment used is the PathWave Advanced Design System (ADS), and tests were performed primarily using the Transient simulation, a time domain circuit analysis, with data exported as tables in .csv format for processing. Although the performance of RF networks is typically measured in the frequency domain and directly simulated, that is not possible when the transient performance of the circuits is the primary focus. Investigating transient effects must be done with a time domain analysis because classic S-parameter or AC simulations may not adequately capture that behavior. When steady-state results are required, the same transient analysis setup can be used by running the simulation long enough for the steady-state performance to comprise almost all the data taken. Fourier transforms then convert the time-domain results into the frequency-domain. Frequency-domain data were obtained by exporting the time-domain data in tables and processing them in MATLAB. Direct sampling followed by post-processing in MATLAB was chosen in order to remove any complications that may have arisen from implementing more of the receiver and analog-to-digital conversion in hardware. Sources of error are minimized by keeping to ideal mathematical implementations outside of the network under test.

Results for the modified sampling network are mostly shown alongside results from the conventional sampling network, directly sampled input, or both. This provides two baselines to compare the modified network's performance. It should exceed the performance of the conventional network and approach the results of the directly sampled data as much as possible.

4.2 MATLAB Processing Environment

MATLAB was chosen for data processing because it is well-suited for handling large amounts of data, has built-in functions for nearly every operation needed, and familiarity with its common usage in academia. It is primarily used to extract the frequency domain information from the data sampled by the sample-and-hold network under test. By saving both the clock voltage (for Switch A) "Vsw" and the sampling capacitor voltage "Vo," it is simple to extract the value of Vo during the hold phase as it is constant for the duration, excluding the square wave rise/fall time. Therefore the sample for a given sample-and-hold cycle is taken from a single value ten timesteps after the capacitor is isolated. Using a single value was observed to be sufficient for accurate results, and inspecting the transient data showed that the values during the "hold" portion were all identical outside of the short rise and fall. The rise and fall period each only registered for several datapoints in the data file. This is due to the capacitor being ideal and without any shunt resistance for current leakage. In several tests, the input signal "Vin" is sampled at the same points in time as the Vo signal to provide a directly-sampled benchmark, where the signal is perfectly measured and sampled. This is used to compare against the conventional and modified networks, setting an upper limit to the accuracy and fidelity that can be achieved with a small number of samples for a given signal. These sampled voltages were then input into a Fast Fourier Transform (FFT) and combined with sampling rate information, thus providing a frequency domain representation of the sampled data. Due to its extensive math graphics libraries, MATLAB was also used for additional plotting and graphing purposes. Figure 4.1 is a graphic demonstration of the process for obtaining the directly sampled data. The input waveform is generated in ADS, then sampled and converted to individual data points in MATLAB. Both steps 1 and 2 are performed in ADS for the sampling network data.

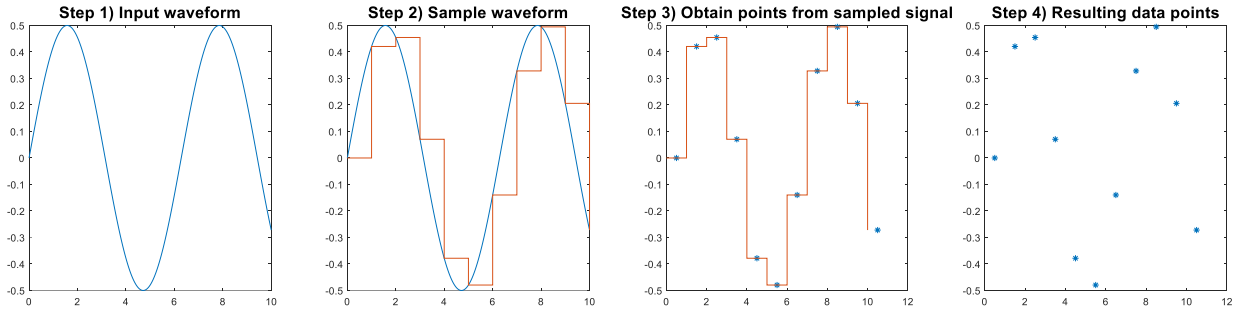

Figure 4.1 MATLAB process for converting continuous signals into sampled data

4.3 Sampling Network Configuration

Two network configurations were used for simulation experiments. The modified sampling network is the novel design presented in this paper, while the conventional sampling network is the basic sample-and-hold design. Comparison is made to the basic version because the modifications in the novel design could theoretically be applied to more advanced versions, such as feedback sampling networks, as there is no modification to previous or later stages. Since several mixer-first designs with quadrature approaches initially inspired this design, the sampling network contains four branches, arranged as in Figure 3.4, with clock offsets of $0°, 180°, 90°, \text{and } 270°$. This forms the 4-phase configuration. Information and samples from branches 2-4 were discarded after confirming that sampling on all branches demonstrated equivalent effects and had no functional difference. Since this thesis is focused on the sampling modification rather than the passive mixer in general, data collection was focused on the impact seen by a given sampling branch.

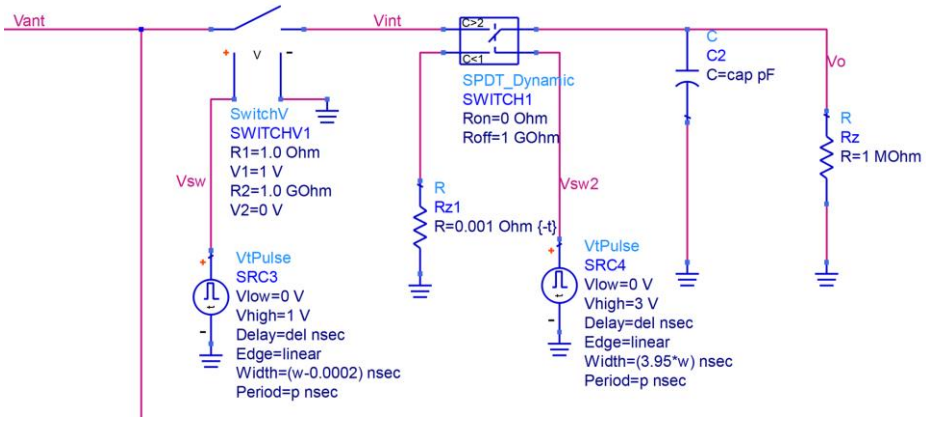

Figure 4.2 Modified network implementation in Keysight ADS

The modified network introduced in Figure 3.1 is realized in ADS using the network in Figure 4.1. The input has been left out of this schematic as it will depend on the specific test being performed as presented in the upcoming sections. The sampling buffer has been replaced with a 1MΩ resistor, and the sampling capacitor voltage is sampled directly at the node labeled "Vo." The source voltage is recorded at the node labeled "Vin." In some of the tests, a small resistor is placed between Vin and the voltage sources for simulation purposes. Without that resistor, ADS will automatically introduce a resistor after the voltage sources to separate what node they are on, as the simulation cannot drive the same node at two different voltages. Placing the resistor ensures that it is a known value. Since some tests involve multiple sources, it is important to ensure that they sum equally prior to entering the system under test. The net labeled "Vsw" on the diagram is the same Vsw used for timing the sampling reconstruction in MATLAB, while "Vsw2" is specifically for the timing of the changeover switch and does not get used in any post-processing. The SPDT switch control is 0-3V, as that is the standard control value for a SPDT_Dynamic element in Pathwave ADS, and a 0-1V signal similarly controls SwitchV by default.

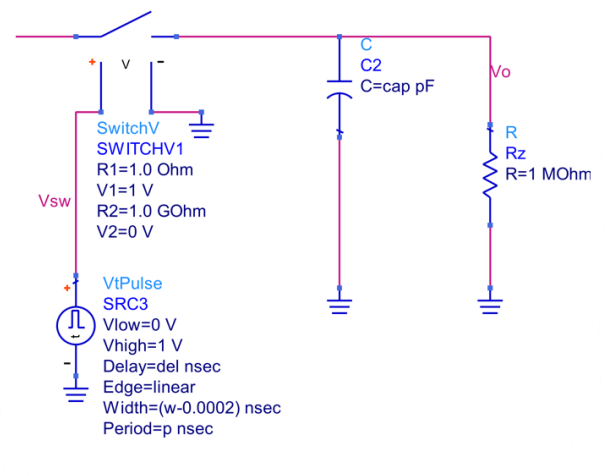

Figure 4.3 Conventional network implementation in Keysight ADS

The conventional network (Figure 4.2) was implemented in ADS in the same manner as the modified network, except without the components representing the changeover switch. Data were recorded on nets Vsw and Vo, and Vsw2 was not present as there is only one switch per sampling branch.

4.4 Ringing Cancellation

The modified sampling network is designed to reduce transient nonlinearities in the sampled signal for networks connected to an unmatched source, particularly ones such as a short antenna or another high-reactance element. This typically exhibits ringing and may distort reconstructed signals and frequency domain conversion. This section focuses on observing ringing cancellation in the modified sampling network, as compared to the conventional sampling network. The first two tests are preliminary tests of this function, while the third and fourth tests examine network behavior with realistic antenna models. Tests five and six examine the behavior of the sampling networks in data transmission and intermodulation effects, respectively.

4.4.1 Resistive Source Impedance

Figure 4.4 Resistive source impedance model in Keysight ADS

The resistive source impedance is demonstrated as a control test to show that the sampling modification does not cause any adverse effects when sampling from a purely resistive source. F_s is the frequency of the sine-wave voltage source providing the input signal, R_s is the source resistance, and $Z_s(f)$ is the impedance for the given frequency.

Table 4.1 Resistive source lumped element model values

Variable	Value
R_s	50 Ω
F_1	500 MHz
$Z_s(F_1)$	50 Ω
F_2	1000 MHz
$Z_s(F_2)$	50 Ω

4.4.2 Capacitive Source Impedance

Figure 4.5 Capacitive source impedance in Keysight ADS

The capacitive source impedance is shown in Figure.4.5, with values as per Table.4.2. C_s and R_s are chosen to induce as much ringing as possible in a conventional sampling network to clearly represent the effect. Since the source is capacitive, there is only a low potential for resonance, and C_s will need to form a very large mismatch to see ringing. The value used for C_s is not practical in real systems but is just used to obtain preliminary measurements. The dipole and

loop antenna models described later in this section are more accurate for real-world applications. F_s is the frequency of the sine-wave voltage source providing the input signal. This test was run as a preliminary assessment to determine the modified network's ability to reduce ringing for capacitive sources with a signal duration of two full-wave periods. Since only a single frequency is being tested, the impedance listed is accurate for that specific configuration. If other input frequencies were present, then the source impedance would vary based on the R_s and C_s values.

Table 4.2 Capacitive source lumped element model values

Variable	Value
C_s	0.05 pF
R_s	5 Ω
F_1	500 MHz
$Z_s(F_1)$	5-j6366 Ω
F_2	1000 MHz
$Z_s(F_2)$	5-j3183 Ω

4.4.3 Inductive Source Impedance

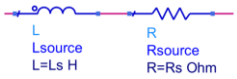

Figure 4.6 Inductive source impedance in Keysight ADS

The inductive source impedance is shown in Figure.4.6, with values as per Table.4.3. L_s and R_s were chosen to induce significant ringing in a conventional sampling network to represent the effect. F_s is still the frequency of the sine-wave voltage source providing the input signal. This test was run as a preliminary assessment to determine the modified network's ability to reduce ringing for inductive sources with a signal duration of two full-wave periods. Since only a single frequency is being tested, the impedance listed is accurate for that specific configuration. If other input

frequencies were present, then the source impedance would vary based on the R_s and L_s values.

Table 4.3 Inductive source lumped element model values

Variable	Value
L_s	200 nH
R_s	5 Ω
F_1	500 MHz
$Z_s(F_1)$	5+j628 Ω
F_2	1000 MHz
$Z_s(F_2)$	5+j1256 Ω

4.4.4 Dipole Antenna Lumped Element Model

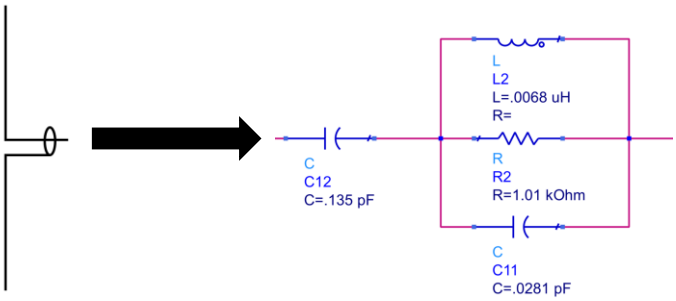

Figure 4.7 Short Dipole Lumped Element Equivalent

A lumped element model for dipole antennas, as shown in Figure.4.7, provides a more accurate model for the type of source this sampling network is likely to interface with. Drawn from [16], this model is accurate for thin wire antennas and exhibits less than 10% reactance error and 0.5% radiation resistance error for frequencies where the antenna half-length is under 25% of the corresponding wavelength. Since testing occurred under 1GHz, a dipole half-length of 3cm was chosen. The 10% error cut-off is thus at 2.5GHz, well above the frequencies being tested. The calculations for the lumped element values and followed the equations (4.1) through (4.4). Short dipoles are capacitive, and so the results from this model were predicted to be similar to that of the capacitive source impedance test.

(4.1) $C_1 = \frac{12.0674h}{loglog\,(2h/a) - 0.7245} pF$

(4.2) $C_2 = 2h\left\{\frac{0.89075}{[loglog\,(2h/a)\,]^{0.8006} - 0.861} - 0.02541\right\} pF$

(4.3) $L_1 = 0.2h\{[(2h/a)\,]^{1.012} - 0.6188\} \mu H$

(4.4) $R_1 = 0.41288[log\ log\ (2h/a)\,]^2 + 7.40754(2h/a)^{-0.02389} - 7.27408\ k\Omega$

4.4.5 Loop Antenna Lumped Element Model

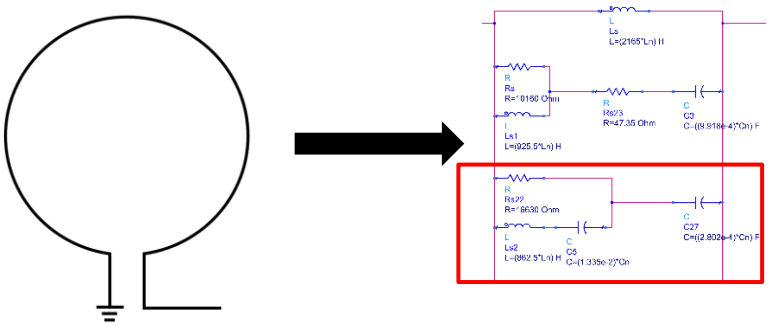

Figure 4.8 Coil antenna lumped element equivalent (partial)

Lumped element modeling for coil antennas, which were chosen for testing due to being naturally inductive, was more complicated than for short dipoles. As such, only part of the antenna model is pictured. The top two parallel branches are unique, while the third (boxed in red) through tenth maintain the same topology but with different values for the resistors, capacitors, and inductors. The specific model used for testing was the Type-1 equivalent circuit from [15], with the parameters as a circular loop antenna with a radius of 1cm. This model is also used for tests 4.5, 4.6, and 4.7. A better image of the lumped element model is available in Appendix A.

4.5 Sampled Voltage Amplitude

This test is the sampling network equivalent to measuring the power transmission and losses in an RF circuit. Unlike in a filter or conventional matching network, power does not get relayed to the output of the sampling network. Instead, the voltage stored on the capacitor is the critical metric for determining the degree of loss. The high-impedance buffer amplifier sees this voltage and transfers it further along the receiver path.

It is important to note that any gain is voltage gain, not power gain, similar to the effect seen in [14]. The loop antenna lumped element model is inductive at the frequencies tested and thus can result in increased voltage swing at the sampling capacitor. This is covered more in section 5.1.2.

The P_1Tone source in Keysight ADS is used, which generates a sine wave set to 32mW and a variable frequency to sweep from 10MHz to 990MHz. The test is performed with a 100ns Transient analysis for each frequency individually, with the data processed in MATLAB to obtain the frequency domain representation. Test frequency peaks are recorded and then plotted to get the frequency response chart. The loss is obtained by dividing the output signal amplitude by the input signal amplitude for a given frequency. A 50Ω load, without a matching network, is used for comparison as well. To ensure that the comparison is as accurate as possible, the load voltage is sampled at the same points in time as the data from the sampling networks. This follows the same method as demonstrated in Figure 4.1.

4.6 BPSK Modulation Transmission

This test consists of a Binary Phase Shift Key (BPSK) modulated signal at 500MHz input into the sampling network through the loop antenna lumped element model. BPSK was chosen to

simplify the test by switching between binary phase states. The 0°/180° shift also presents the most significant change in signal possible from phase-only encoding. The loop antenna model was chosen because of the strong ringing seen on the conventional network, much greater than that from the dipole antenna model. Since the conventional sampling network has shown the worst performance on a loop antenna out of the four options tested, it would also be the most rigorous test for determining the ability of the modified network to rectify the distortion that could otherwise reduce symbol interpretation accuracy. A series of 5 symbols are transmitted as in Figure 4.9 to test the degree of error encountered by the conventional and modified sampling networks. Ideally, there should be 180 degrees of separation between a 0-encoded symbol and 1-encoded symbol, so the symbol 1 was determined as a phase within 90 degrees of separation between the N^{th} symbol's phase and the first symbol's phase. Over 90 degrees separation indicates a 0.

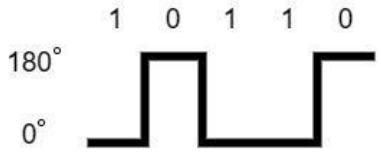

Figure 4.9 BPSK encoded binary signal, five bits long

These symbols are transmitted for different durations or frequencies depending on the test performed. Three sets of data were derived from each test, consisting of ideal sampled data, conventional sampling network data, and modified sampling network data. The first set is taken directly from the input signal, as described earlier in the test setup section, while the latter two sets are taken from their respective sampling networks. Results are then shown as a comparison of magnitude and phase plots in the frequency domain for each symbol at the frequency of interest.

Amplitude plots are normalized with respect to their maximum value because the main interest is to observe whether or not the peak amplitude shifts in frequency for either sampling network.

The symbols are encoded on a 500MHz sine wave for one cycle each, resulting in 2 ns per symbol and a total transmission length of 10 ns. With such short symbol durations, this is a transient test, and the conventional sampling network could not reach a steady state. The accuracy of the results will be dependent on the amount of distortion seen by each network during their transient period.

4.7 Multiple Frequency Test

This series of tests is to ensure that no unwanted intermodulation is presented by the input of multiple frequencies into the modified network. For both the long and short sampling window tests, the input signal consists of a 400MHz and 600MHz sine wave at equal amplitude. Comparison to ideal sampling now requires frequency-based normalization due to multiple input frequencies and was performed by multiplying the input signal frequency response by the (linear) S21 response of the loop antenna model.

4.7.1 Long Sampling Window

The long sampling window test was run for 100 ns and, as with the previous test, formed a steady-state baseline for both sampling networks. By comparing these results against the short sampling window results, the modified network's improved performance in very short sampling windows should be clear.

4.7.2 Short Sampling Window

The short sampling window test was run for 5ns and formed the transient dataset. Compared to the long sampling window results, the resolution should be significantly decreased, and zero-padding is necessary to improve readability. The modified network was expected to perform roughly as well as during the long sampling period test, while the conventional sampling network would have very poor performance.

4.7.3 Directly Sampled Data Normalization

The S21 magnitude response of the antenna was taken in ADS using an S-Param simulation over the region of interest (10MHz-1GHz). The Equation $F_{norm}(\omega) = F(\omega) * \sqrt{S21_{mag}(\omega)}$ was used to normalize the response of only the ideal sampling data since the network-sampled data was from the voltage across the sampling capacitor and thus already accounts for the antenna response. Figure 4.8 shows the S21 used for these calculations.

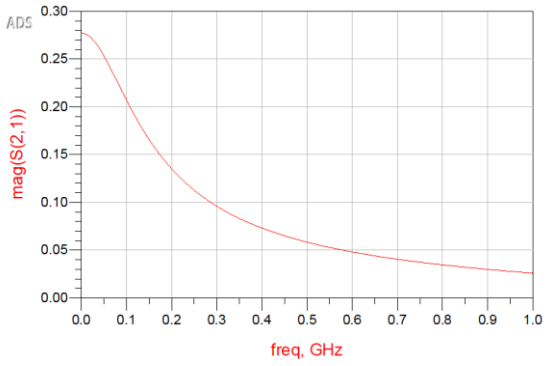

Figure 4.10 Loop antenna S21 response

5. RESULTS

5.1 Ringing Cancellation Tests

These tests were performed at both 500MHz and 1000MHz to demonstrate results from both the Nyquist frequency and a frequency solidly within the sampling network's frequency range. Both sampling networks operate at a 2GHz sampling rate for all tests in this section.

5.1.1 Resistive Source Impedance

The first Resistive Source Impedance test (R= 50Ω) was performed at 500 MHz, resulting in a source impedance of $Z_s = 50\Omega$. No ringing was expected in this case, as the source has no reactive elements.

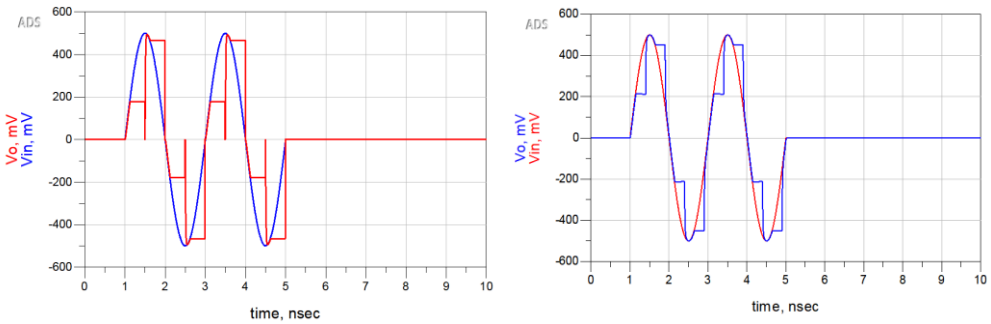

Figure 5.1 Resistive source transient analysis with 500MHz sinusoidal signal Modified Network (Left), Conventional network (Right)

The second resistive source impedance test was performed with the same lumped elements for the source but at 1000 MHz.

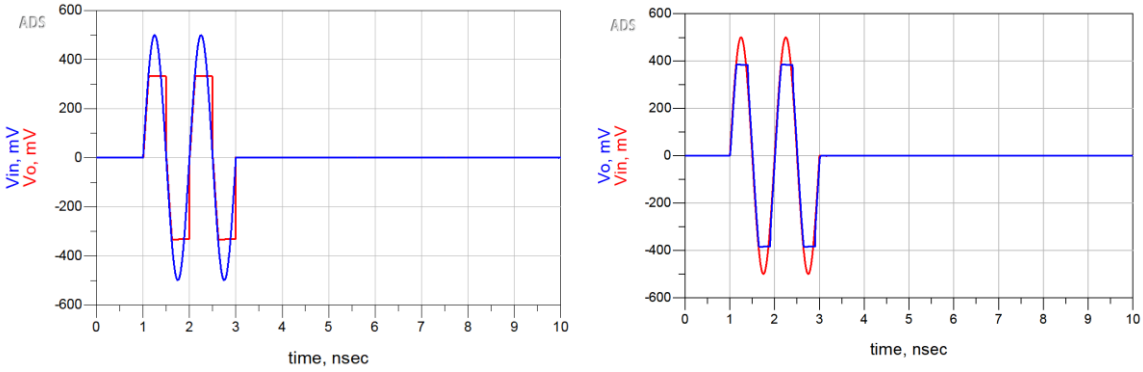

Figure 5.2 Resistive source transient analysis with 1000MHz sinusoidal signal
Modified Network (Left), Conventional network (Right)

In both cases (Figure 5.1, 5.2), the networks perform near-identically and track the input signal accurately. The sampling network modification does not impede performance in conventional use cases with purely resistive sources.

5.1.2 Capacitive Source Impedance

The first Capacitive Source Impedance test (R_{source}= 5Ω, C_{source}= 0.05 pF) was performed at 500 MHz, resulting in a source impedance of $Z_s = 5 - j6366\Omega$. Results are limited to the first 10ns to improve readability. However, the conventional sampling network did have further ringing, which eventually decayed. Ringing was more evident in the inductive source tests.

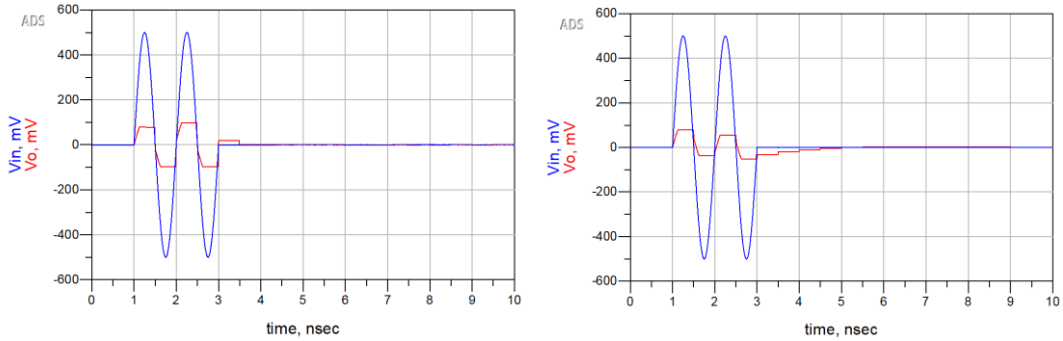

Figure 5.3 Capacitive source transient analysis with 500MHz sinusoidal signal
Modified Network (Left), Conventional network (Right)

The purely capacitive source impedance did not show much ringing even on the conventional network, but the modified network removes this ringing nonetheless. This is expected due to the low degree of possible resonance in purely capacitive circuits. The low voltage swing on the sampling capacitors can be attributed to the source impedance capacitance storing part of the incoming energy and forming a series capacitance. Thus, for a source capacitance C_{source} and sampling capacitor C_S, an incoming voltage V_{in} results in sampled voltage V_s, as shown by Equation (5.1), where Q is the charge stored on the capacitors. The source capacitance reduces the voltage seen across the sampling capacitor. The current is very low as the only DC path to ground is through the megaohm resistor R_Z in Fig. 4.2, which represents the buffer input impedance, and thus the voltage drop across the resistor R_{source} and R_Z may be negligible.

$$(5.1)\ V_s(t) = V_{in}(t) - \frac{Q(t)}{C_{source}} - R_{source}I(t) - R_zI(t) \cong V_{in}(t) - \frac{Q(t)}{C_1}$$

The second capacitive source impedance test was performed with the same lumped elements for the source but at 1000 MHz for a source impedance of $Z_s = 5 - j3183\Omega$.

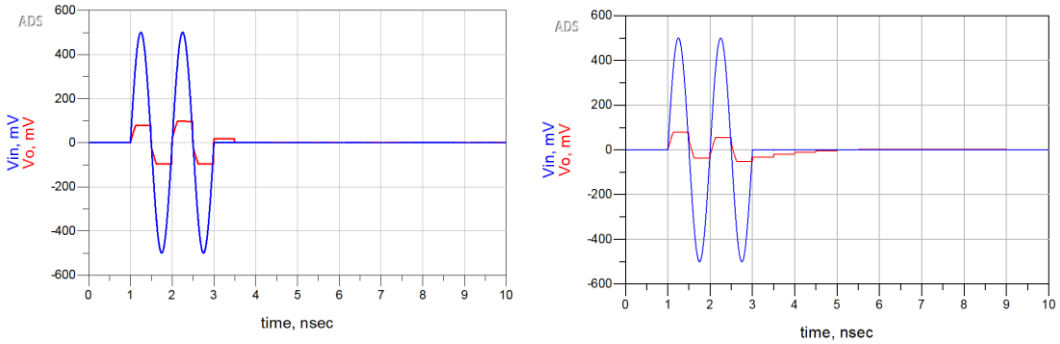

Figure 5.4 Capacitive source transient analysis with 1000MHz sinusoidal signal Modified Network (Left), Conventional network (Right)

Slightly more ringing was observed at 1000 MHz on the conventional sampling network, and as with 500MHz, no resonance was observed on the modified sampling network. In both cases, the output voltage swing was significantly reduced.

5.1.3 Inductive Source Impedance

Ringing was significantly more visible on the inductive source impedance (R_{source}= 5Ω, L_{source}= 200 nH) test for both 500 MHz and 1000 MHz. Figure 5.5 demonstrates both the severe ringing on the conventional network (right) and the lack of ringing in the modified network (left). The source impedance for the 500 MHz test was $Z_s = 5 + j628\Omega$.

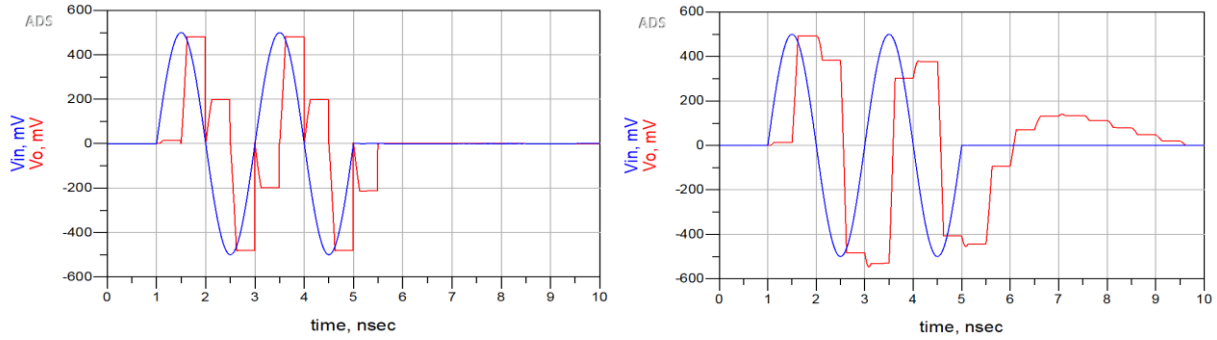

Figure 5.5 Inductive source transient analysis with 500MHz sinusoidal signal Modified Network (Left), Conventional network (Right)

Unlike a capacitive source, the inductive source may cause a marginal increase in the sampled voltage instead of a decrease. There is also a significant delay between the input voltage and the voltage across the capacitor, again due to the nature of an inductor. The voltage across the sampling capacitor can be expressed with Equation (5.2), and as with the previous setup, the voltage drop across the resistor can be considered negligible. Likewise, t_1 is the time at which the sampling switch opens and the sampler enters the 'hold' state. As the sampling capacitor charges, current decreases and $\frac{di}{dt}$ becomes negative. This results in $-L_{source}\frac{di}{dt}$ becoming a positive value

and increasing the voltage seen across the sampling capacitor. It is important to note that although the voltage swing may increase, power is conserved as current reduces accordingly. The sampling buffer then passes the capacitor's stored value to the next stage, preserving the high voltage without drawing current.

(5.2) $V_s(t) = V_{in}(t) - L_{source}\frac{di}{dt} - R_{source}I(t) - R_zI(t) \cong V_{in}(t) - L_{source}\frac{di}{dt}, t \leq t_1$

Figure 5.6 shows the results for the same test performed at 1000 MHz as well. In this case, the sampled voltage swing does not exceed the input voltage due to the points at which it was sampled since the timing of the sample-and-hold network is such that it does not switch to "hold" at the peak of the input signal. Shifting the start of sampling in time would show the expected increase in voltage. Ringing on the conventional network is more subdued but still clearly present.

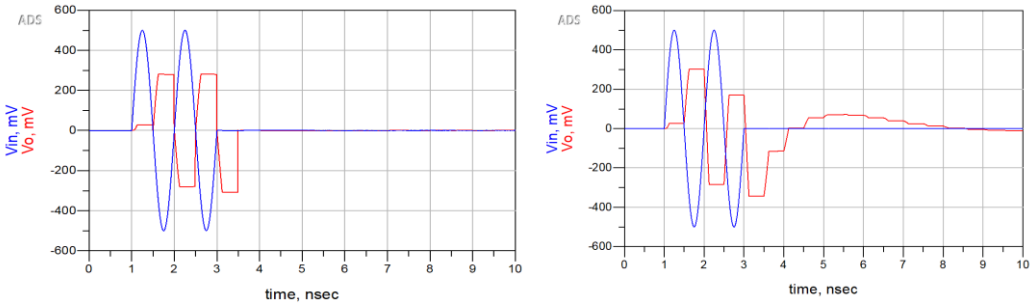

Figure 5.6 Inductive source transient analysis with 1000MHz sinusoidal signal Modified Network (Left), Conventional network (Right)

5.1.4 Dipole Antenna Model

Both tests for the dipole antenna performed very similarly to the capacitive source test, with low amounts of ringing even on the conventional network and no ringing on the modified network. For reference, the lumped element model and test were described in Section 4.4.3.

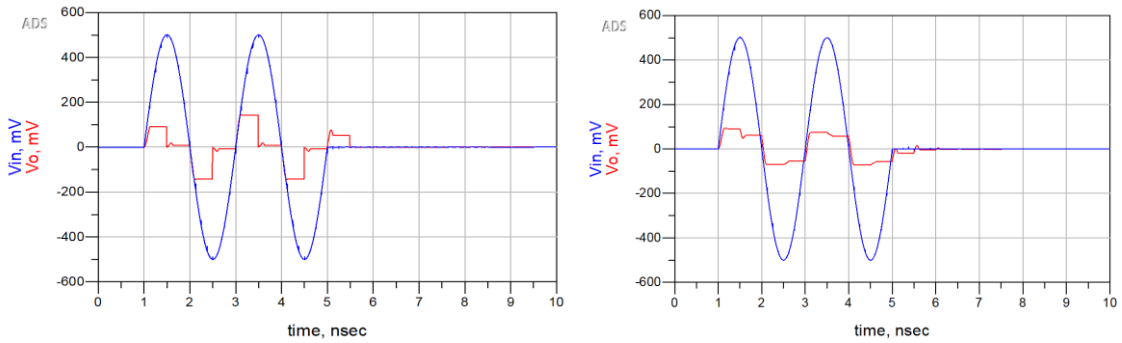

Figure 5.7 Dipole model transient analysis with 500MHz sinusoidal signal
Modified Network (Left), Conventional network (Right)

Although the expression for the sampling capacitor voltage can be expressed in terms of the lumped elements as in previous tests, it is not as helpful for determining time-variant effects due to the complexity of the circuit. Dipole antennas are known to be capacitive, however, and this was seen during impedance analysis of the lumped element model, so it can be inferred that the dipole-fed network undergoes similar effects as the network in Section 5.1.1.

Slightly more ringing was observed on the conventional network at 1000MHz, which was likewise not present on the modified network sampling capacitor.

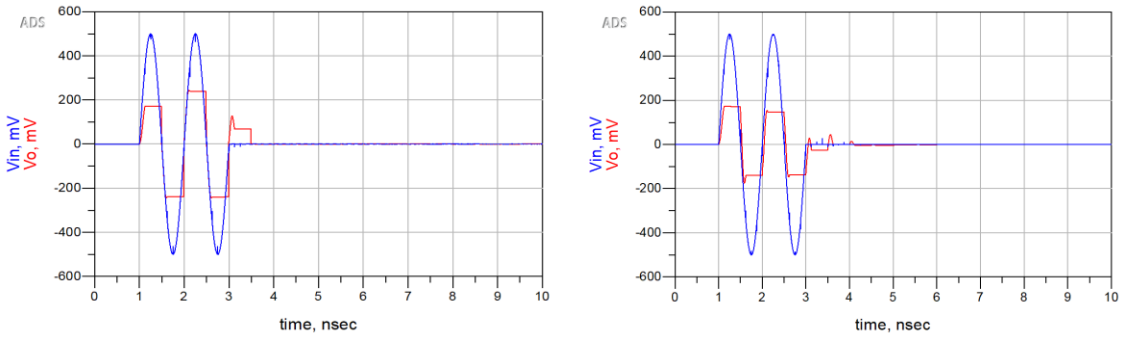

Figure 5.8 Dipole model transient analysis with 1000MHz sinusoidal signal
Modified Network (Left), Conventional network (Right)

5.1.5 Loop Antenna Model

The loop antenna model performed similarly to the inductive source impedance but with much greater ringing. At both 500MHz and 1000MHz, the ringing extends past 10ns on the conventional network, and the modified network fully eliminates ringing on the output.

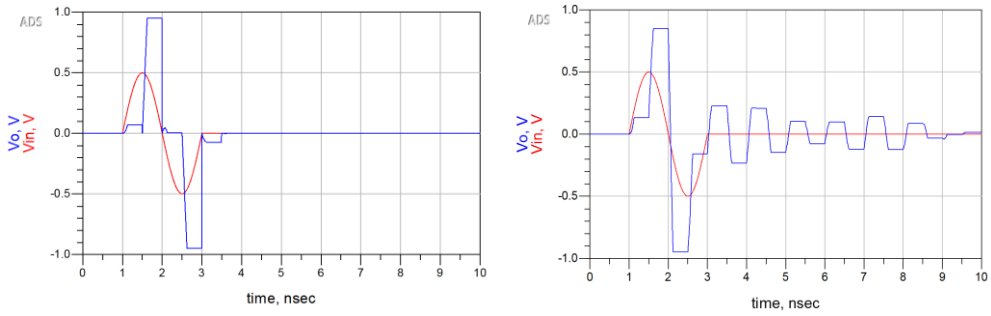

Figure 5.9 Loop antenna model transient analysis with 500MHz sinusoidal signal
Modified Network (Left), Conventional network (Right)

The 1000MHz test in Figure 5.10 demonstrates this improvement even more than the 500MHz test, with significant ringing that extends past 10 ns on the conventional sampling network's output but not on the modified network's output. For reference, the lumped element model and test were described in Section 4.4.4.

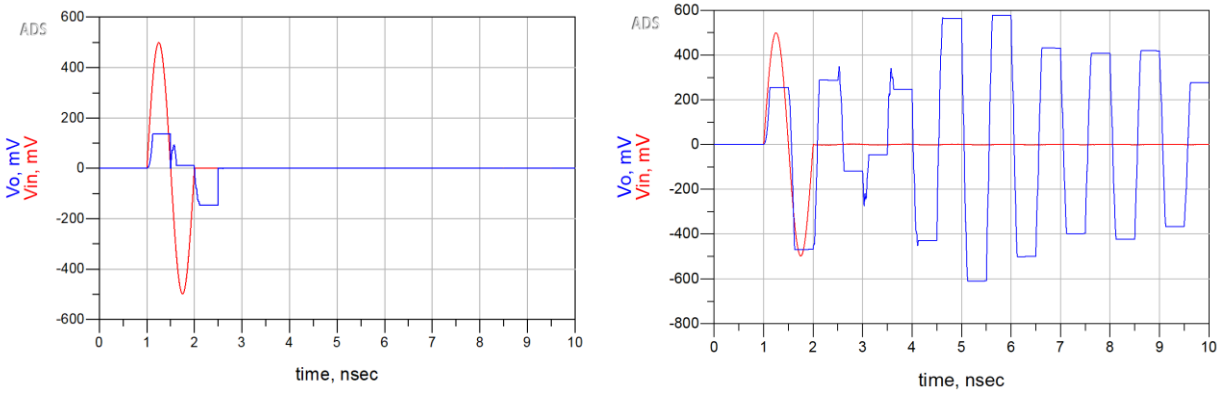

Figure 5.10 Loop antenna model transient analysis with 1000MHz sinusoidal signal
Modified Network (Left), Conventional network (Right)

Sustaining the signal for 7 cycles results in Figure 5.11 and demonstrates that the conventional network's distortion is also present in short signals at high frequencies (relative to the Nyquist frequency). A dip in amplitude is visible between 6-14 ns and generally appears erratic, while the modified network's response is identical for all cycles.

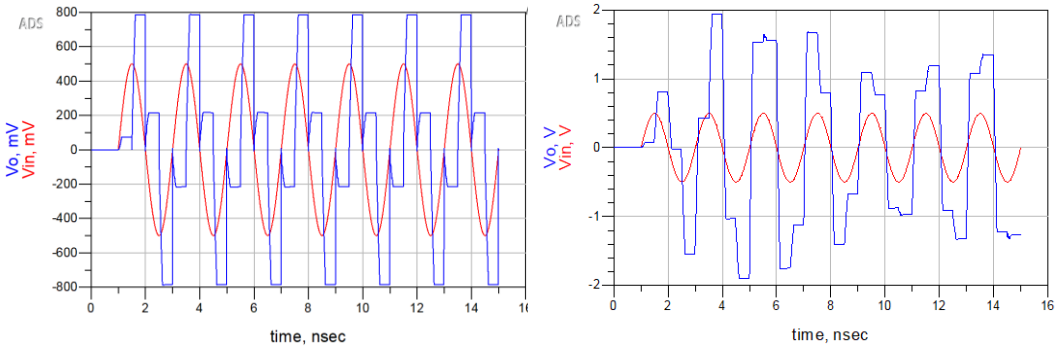

Figure 5.11 Transient analysis of 10ns sinusoidal signal at 500MHz
Modified Network (Left), Conventional network (Right)

Comparing the frequency domain responses from the direct sampled data, modified network data, and conventional network data shows how the modified network can almost perfectly match the results from directly sampling the input waveform. In contrast, the conventional network has a false peak 100MHz away from the 500MHz input. (Figure 5.12)

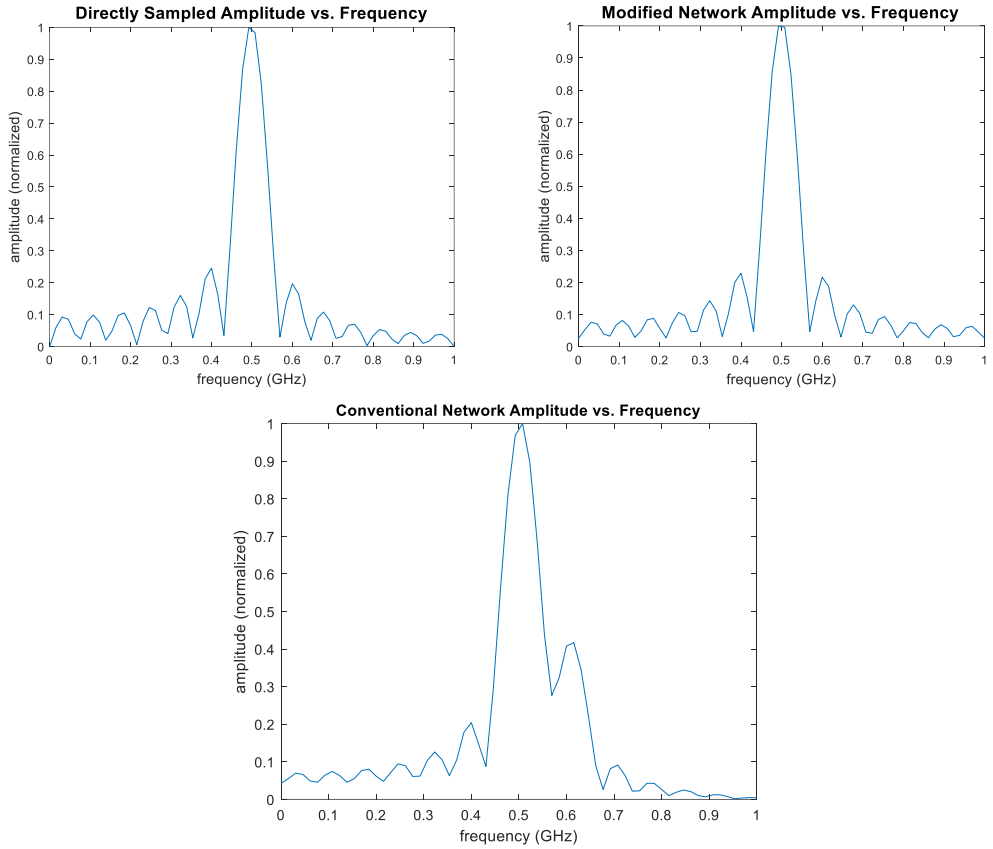

Figure 5.12 Frequency domain analysis of 10ns sinusoidal signal at 500MHz
Directly Sampled Input (Left), Modified Network (Middle), Conventional network (Right)

Since transmission durations may not always be known, and sampling may continue past the point at which transmission has ceased, another test was performed in which the signal was transmitted for 15 ns while sampling continued for another 35 ns. Ringing in the conventional network was near zero at this point, so data beyond that point were not plotted (Figure 5.13). The conventional approach performed worse in this situation, while there was no impact on the modified circuit. Significant distortion was observed in the conventional network during the transmission duration, followed by steadily decaying ringing.

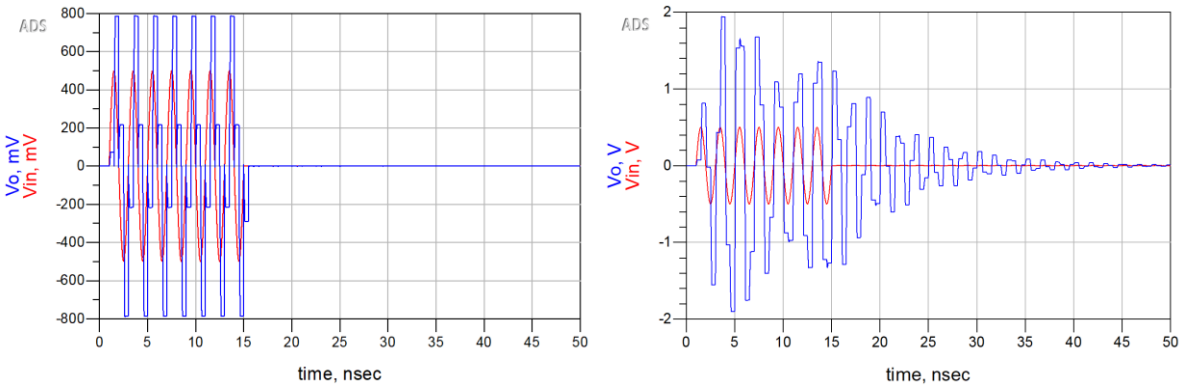

Figure 5.13 Transient analysis of 10ns signal with continued sampling past signal cutoff
Modified Network (Left), Conventional network (Right)

The false peak is even stronger in the frequency domain than in the previous test, at only 30% down from the true peak. Time domain data in Figure 5.13 is true to the actual voltages on the circuit, while the frequency domain results in Figure 5.14 were normalized to a peak of 1 for easier comparison.

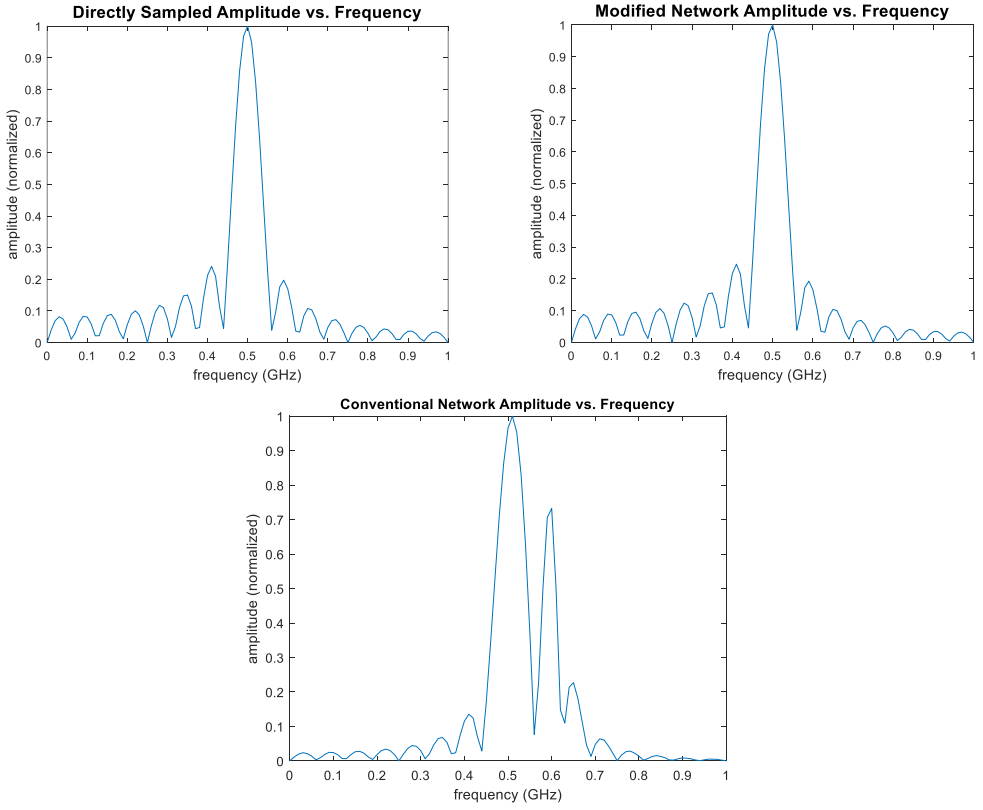

Figure 5.14 Frequency spectrum of 10ns signal with continued sampling past signal cutoff
Modified Network (Left), Conventional network (Right)

Overlapping the directly sampled and modified network frequency domain charts shows very good agreement between the two. (Figure 5.15)

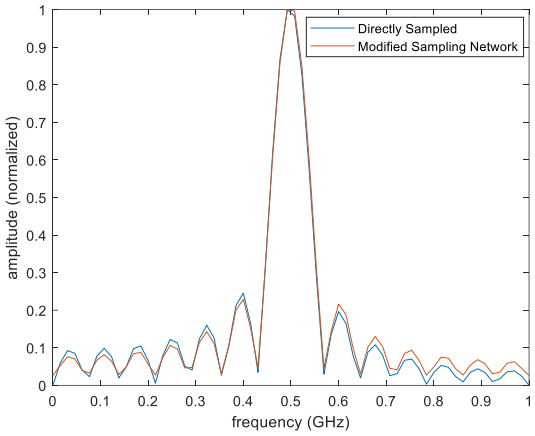

Figure 5.15 Overlapped frequency response of directly sampled data and modified sampling network data from figure 5.14

5.2 Sampled Voltage Amplitude Test

In this test, the modified network did not outperform the conventional sampling network. While the modified network does not achieve as high voltage peaks as the conventional sampling network, the response is much more flat. Figure 5.16 demonstrates the voltage amplitude seen by both networks, where the input voltage for all test frequencies was a sinusoidal wave of 1V peak-to-peak.

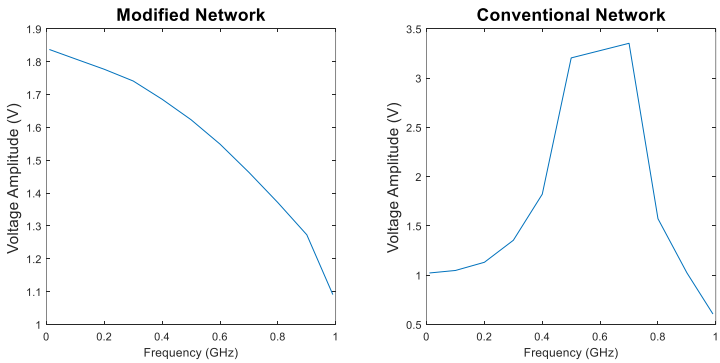

Figure 5.16 Sampled voltage amplitude response vs. frequency

The conventional sampling network exhibits higher peak gain, nearly 3.5x at 0.7 GHz, but this is sharp and only covers a small portion of the frequency range. Further, as seen in Figure 5.24 from the multiple-frequency test (Section 5.4), this only occurs after the sampling network has reached a steady state. The initial voltage gain is low similar to the modified network. The modified sampling network has a much smoother gain curve but only reaches a maximum of 1.85x. Gain could most likely be optimized in both cases, as it was not a consideration when initially designing the sampling networks. In general, decreasing the sampling capacitance appears to increase the voltage swing on the output but that comes with the usual low capacitor value tradeoffs in CMOS implementations. One concern with this test is that the results may be less accurate due to model limitations. The inductors and capacitors that make up the loop antenna model may store more energy than the fields of the actual antenna or react differently to changes in current or voltage and result in a greater voltage increase than would be seen. Definitively confirming these sampling amplitude results would likely require real hardware testing and thus was outside the scope of this thesis. However, these preliminary results are promising and warrant further investigation.

5.3 Multiple Symbol Test

Data was taken with one sampling branch at a 2GHz sampling rate for a monocycle BPSK signal at 0.5GHz. 5 Symbols were transmitted with the pattern 10110, resulting in the input signal shown below in Figure 5.16.

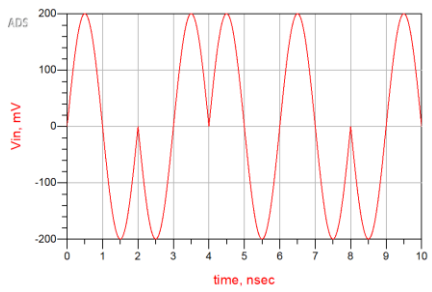

Figure 5.17 BPSK input signal in Keysight ADS

The directly sampled data were taken directly from the input signal in Figure 5.15, while the modified and conventional network data were obtained through their respective sampled signals (Figure 5.18, blue).

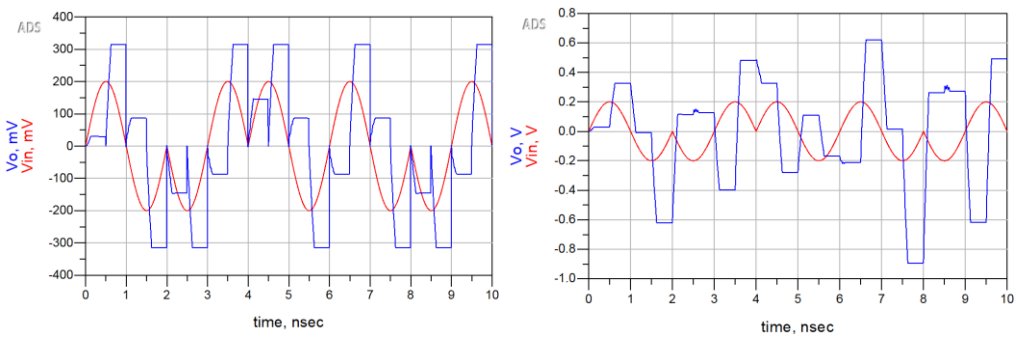

Figure 5.18 BPSK transient analysis for a Modified Network (Left) and a Conventional network (Right)

As in Figure 5.11, the conventional sampling network's transient response is irregular and does not clearly respond to the changes in incoming signal. The modified network's response is much clearer, with consistent response to changes in the incoming signal. These transient responses were converted to the frequency domain, to look at both the amplitude and phase response at the frequency of interest (0.5GHz). Figures 5.19 through 5.21, along with Tables 5.1 through 5.3, demonstrate the phase at 0.5GHz for both networks, as well as for the directly sampled input. Figure 5.22 compares the amplitude response for each symbol between the three sampling methods.

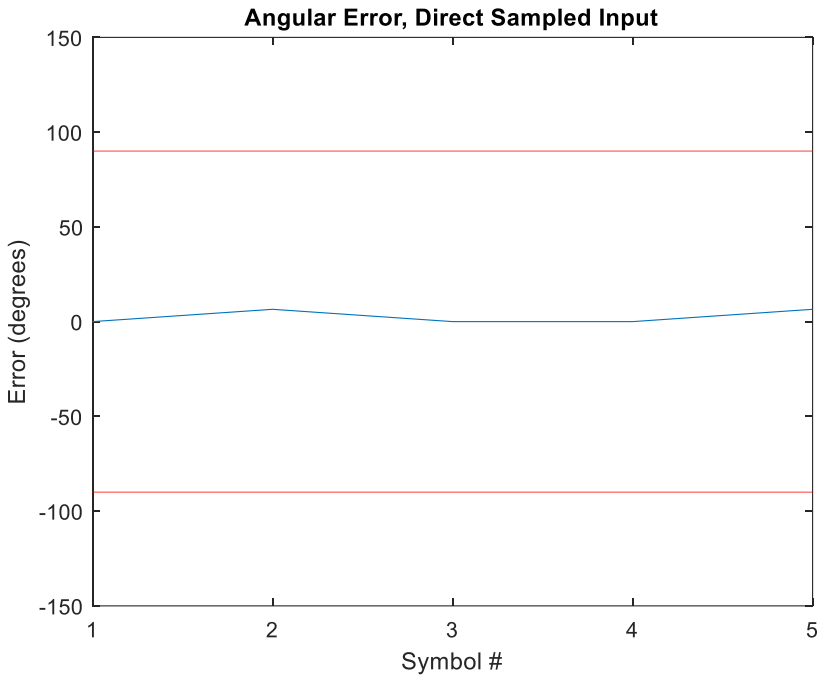

Figure 5.19 Angular error on multi-bit test (Directly Sampled)

Figure 5.19 and Table 5.1 are for the control case, in which the input signal was directly sampled at the voltage source at the same points in time as the conventional and modified networks. The horizontal orange lines represent the error boundaries outside of which the decoded symbol would switch from 1 to 0 or vice versa. The error in Figure 5.17 is relative to the ideal angle, 0° or 180°, and is likely present due to the very short sampling window. Only four samples per symbol were used to reconstruct these results, much shorter than conventionally used symbol durations.

Table 5.1 Multi-bit Test Results for the Direct Sampled Data

Symbol #	Ideal Angle*	Encoded Symbol	Actual Angle*	Decoded Symbol
1	0°	1	0°	1
2	180°	0	173.5°	0
3	0°	1	0°	1
4	0°	1	0°	1
5	180°	0	173.5°	0

**relative to the first symbol angle*

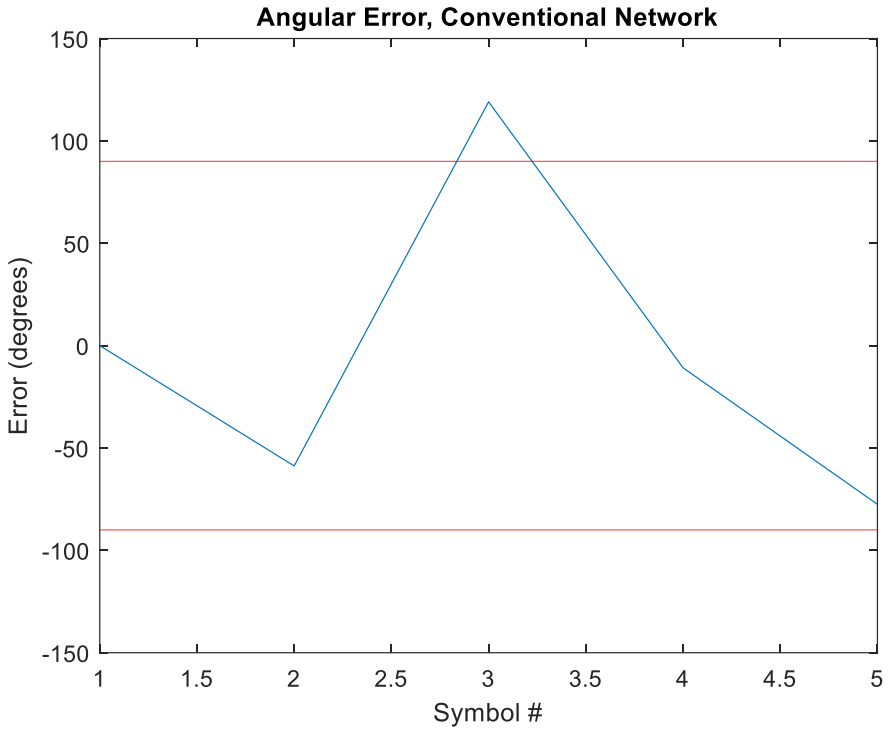

Figure 5.20 Angular error on multi-bit test (Conventional Network)

The conventional sampling network performed poorly in this test, with one incorrect and one questionable phase result. Symbol 3 was well beyond the error boundaries (orange), as seen in Figure 5.20. Note that the phase for symbol 5 is very close to the cut-off point for symbol value as well, though it does not exceed the error boundary. While the decoded symbol is still correct, in a real system any added noise or other irregularity could easily result in the phase shifting below the cut-off at -90 degrees.

Table 5.2 Multi-bit Test Results for the Conventional Network

Symbol #	Ideal angle*	Encoded Symbol	Actual angle*	Decoded Symbol
1	0°	1	0°	1
2	180°	0	115°	0
3	0°	1	119°	0
4	0°	1	−10.8°	1
5	180°	0	96°	0

**relative to the first symbol angle*

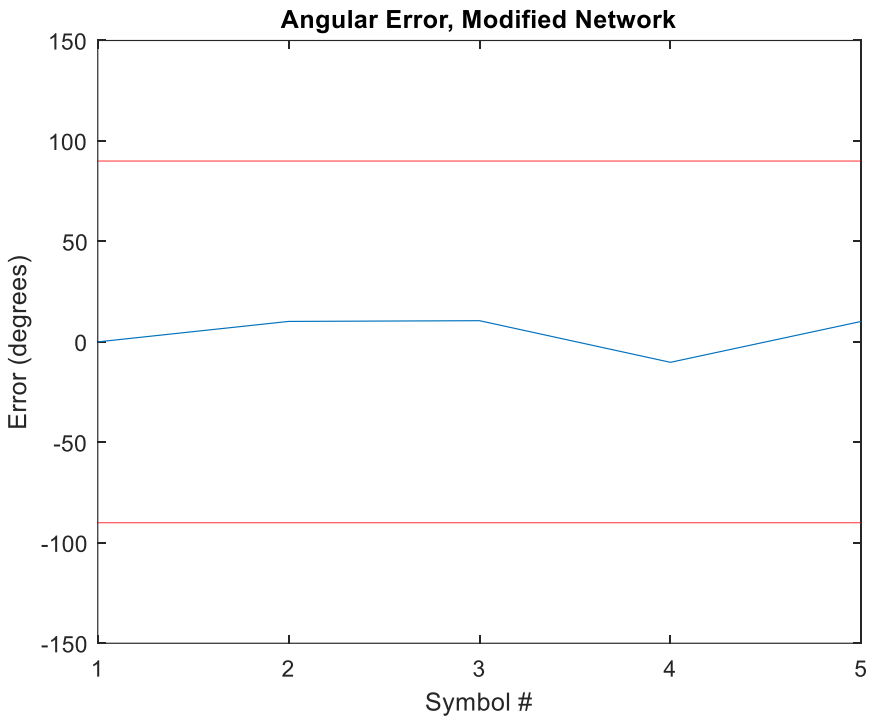

Figure 5.21 Angular error on multi-bit test (Modified Network)

The modified network performed significantly better, with results more comparable to the directly sampled data than the data from the conventional sampling network. The mean phase error was found to be 8.2°, as compared to a 3.3° mean error for the directly sampled results and 69.7° for the conventional sampling network. This is a 92% reduction in error compared to the conventional network for monocycle BPSK transmissions at half the sampling network's Nyquist rate.

Table 5.3 Multi-bit Test Results for the Modified Network

Symbol #	Ideal Phase*	Encoded Symbol	Actual Phase*	Decoded Symbol
1	0°	1	0°	1
2	180°	0	184°	0
3	0°	1	10.6°	1
4	0°	1	−10.2°	1
5	180°	0	184°	0

**relative to the first symbol angle*

Figure 5.22 below compares the amplitude results for the three sets of data (left to right) for the five symbols transmitted (top to bottom).

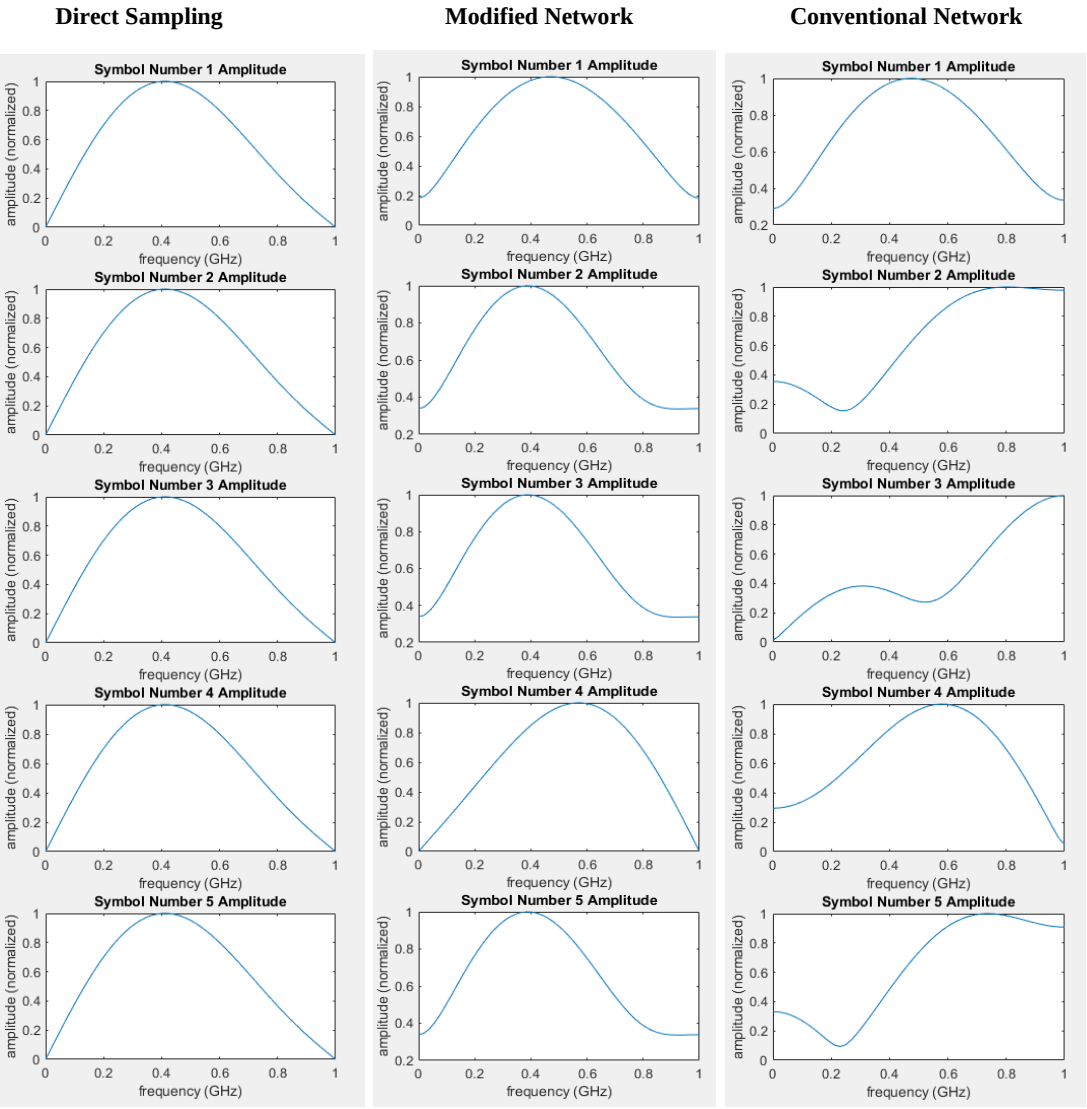

Figure 5.22 Frequency responses for each symbol in the BPSK test, for the direct-sampled data (left), modified network data (middle), and conventional network (right)

Direct sampling, as the control case, has identical amplitude for all symbols. The modified network did see shifts in the peak, with symbols 2,3 and 5 reaching their maximum at 0.4GHz and symbol 4 close to 0.6GHz. Although this did not perfectly match the directly sampled case, it was significantly better than the recovered amplitudes from the conventional network. For the

conventional network the first symbol is still close, symbols 2,3, and 5 are entirely distorted, and only symbol 4 has a curve similar to the direct sampling results.

5.4 Multiple Frequency Test

The modified network sampling resulted in a nearly identical frequency domain amplitude as the directly sampled input, with just a slight reduction in amplitude at 0.6GHz in both long and short cases. Even in the long-symbol (100ns) test (Figure 5.23), the conventional network fails to recover the frequency domain information accurately. The ratio of the 400 MHz signal over the 600MHz signal should be 1:0.9 but is instead 1:10, a very significant degree of error.

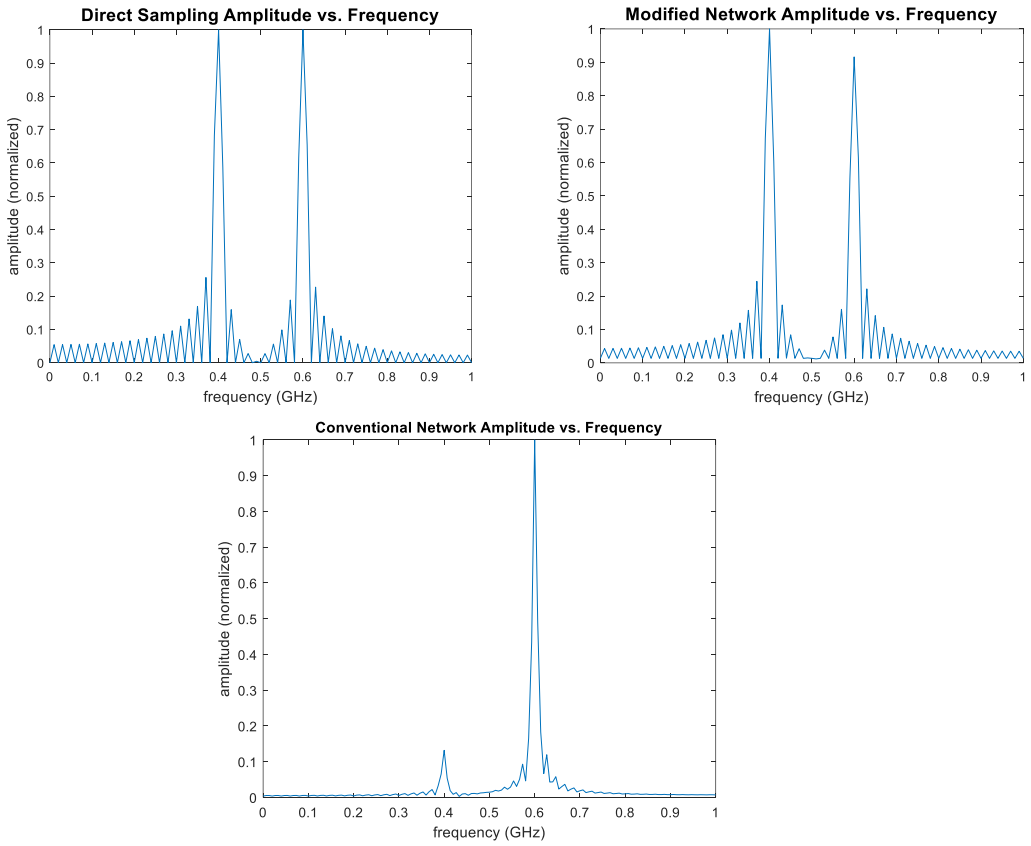

Figure 5.23 Frequency response for two-frequency input, 0.4GHz and 0.6GHz, for 100ns

In the short-symbol test (5ns), the conventional network continues to perform poorly, while the modified sampling network remains fairly accurate. Figure 5.24 compares the three tests, as in

Figure 5.23, while Figure 5.25 overlaps the directly sampled signal results over the modified sampling network results for easier comparison. As can be seen, the two datasets' primary peaks are identically spaced and match in amplitude, though there is increasing error at the upper and lower frequency bounds of the graph. This is in part due to the method used to normalize the directly sampled data, as the frequencies outside 400MHz and 600MHz result from the short sampling period and would not be affected by the antenna's frequency response.

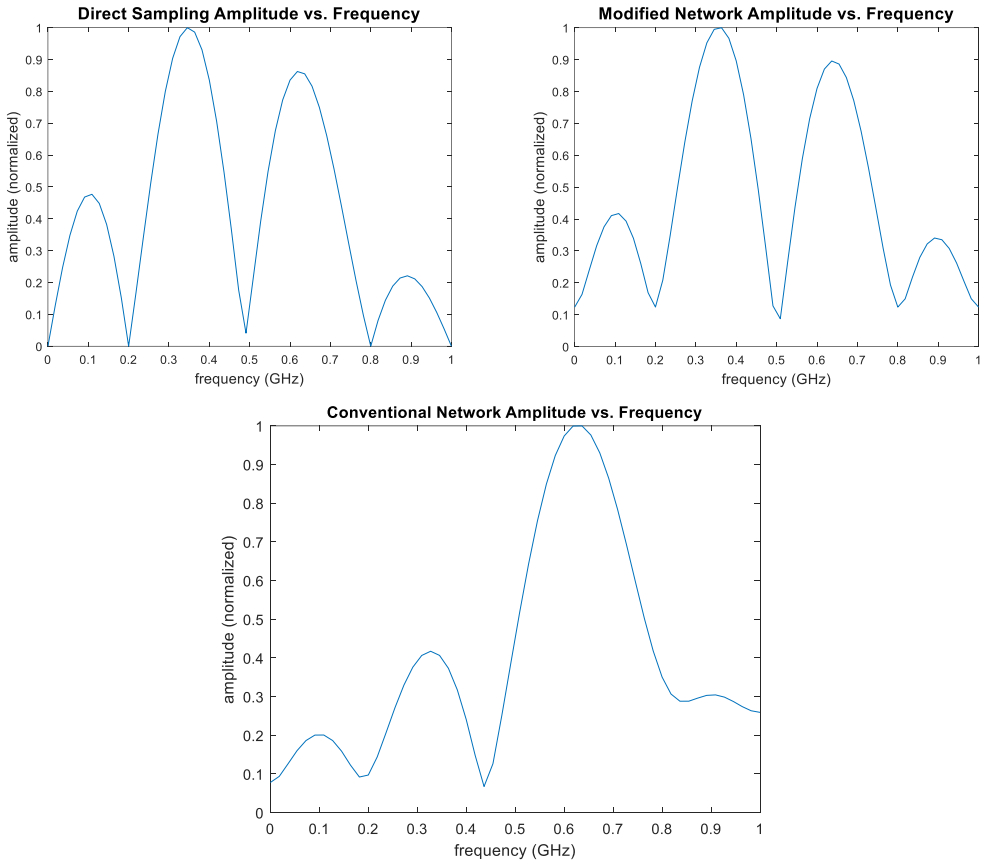

Figure 5.24 Frequency response for two-frequency input, 0.4GHz and 0.6GHz, for 5ns

As in the long-duration signal, the modified network frequency domain amplitude closely matched that of the directly sampled input. The directly-sampled result is in orange, and the modified network result is in blue (Figure 5.25).

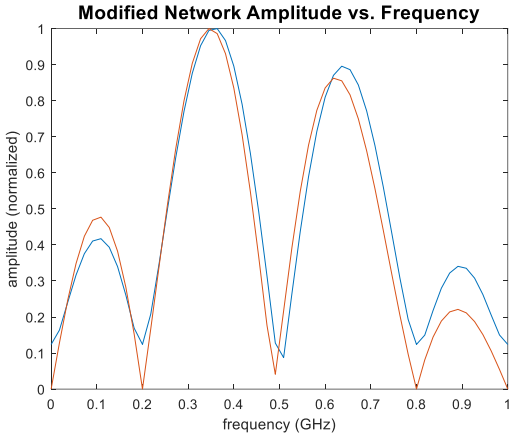

Figure 5.25 modified sampling network and directly sampled input overlap for the 5ns two-frequency test

In addition to accurate sampling, these results further demonstrate the modified sampling network does not suffer signal degradation in very short sampling windows. Figure 5.26 shows the time domain data from both networks, and it is clear that the conventional network takes time to reach steady state sampling even for a continuous signal. If the incoming signal is of comparable duration, then the samples from that transient period further distort the frequency domain reconstruction.

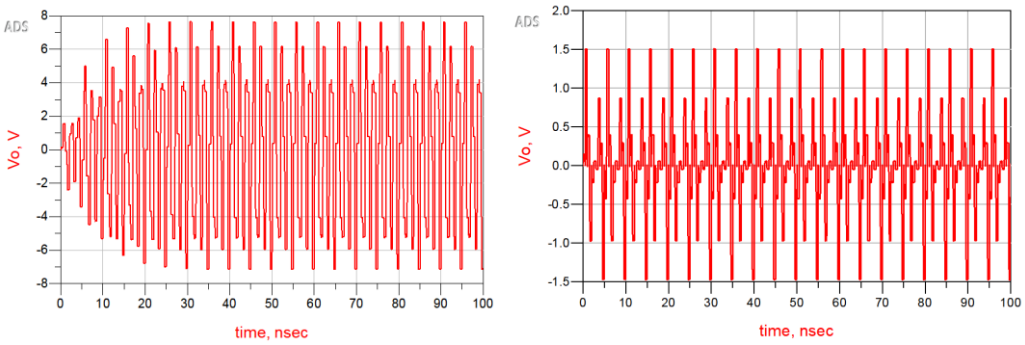

Figure 5.26 Time analysis from 100ns two-frequency test
Conventional Sampling Network (left), Modified Sampling Network (right)

6. CONCLUSIONS AND FUTURE WORK

The modified network presented in this paper has shown considerable improvements toward removing unwanted signal distortions, particularly for very short signals and signals received through inductive sources. By interrupting the release of stored energy from previous sampling states, the changeover switch effectively interrupts the resonance condition created by non-continuous signals propagating between unmatched circuit elements. This removes all mismatch-related distortions from the sampled signal, resulting in a reconstruction nearly identical to an equivalent ideally sampled input signal. Since impedance matching is sometimes ineffective at improving SNR for highly reactive antennas [6], the lack of improvement in power transfer for capacitive sources is not a unique drawback in the primary use cases for the modified sampling network.

The primary benefits of the modified design are for designs involving direct sampling of a signal from a strongly reactive antenna, where matching may not be possible. This is most directly applicable in passive mixer first receivers such as [2, 8, 10]. Although capacitive antennas provide relatively little distortion, inductive antennas result in significant resonance when feeding a conventional sampling network. The modified network entirely removed the impact of that mismatch in both the capacitive and inductive antennas and had similar degrees of loss as the conventional network in both cases.

The primary downside to the modified sampling network is the minor increase in area usage, as its voltage transfer and signal quality were equivalent to or better than that of the conventional sampling network. The added design complexity and area usage are for two additional transistors for the changeover switch and the control pulse generator for that changeover

switch. Only the changeover switch count scales with the number of sampling units, resulting in an area increase of $A_{mod} = 2N * A_{switch} + A_{rectgen}$ where N is the number of sampling units, A_{switch} is the area of a switching transistor, and $A_{rectgen}$ is the area needed for the rectangular pulse generator used to control the changeover switch. Another potential drawback to the modified network is sudden voltage spikes from the sampling capacitors draining to ground, especially if the device ground is poorly implemented. This can be mitigated by increasing the drain switch's resistance to ground if necessary and is not a previously unseen issue regardless, so ultimately is not a major issue. Further, a good ground would likely be required due to the clock circuits to prevent clock signals from flowing through the ground to the sampling capacitor.

Future work should be focused on transistor-level design, fabrication, and testing. Significant evidence supports the modified sampling network's performance with ideal circuit components, but more testing is required to confirm that it works in the real world. The first step would be the design and simulation of the circuit using real transistor models and non-ideal lumped elements. Once the transistor-level simulation demonstrates the appropriate results, the project can move toward fabrication and measurement. Hardware-based testing would allow for observing how well the system samples from real antennas and fully confirm that the modified sampling network's behavior is not due to limitations in the simulation or models used. Hardware testing would be particularly important for confirming the sampled amplitude measurements since the voltage gain improvement would be very significant for receivers sampling at the antenna.

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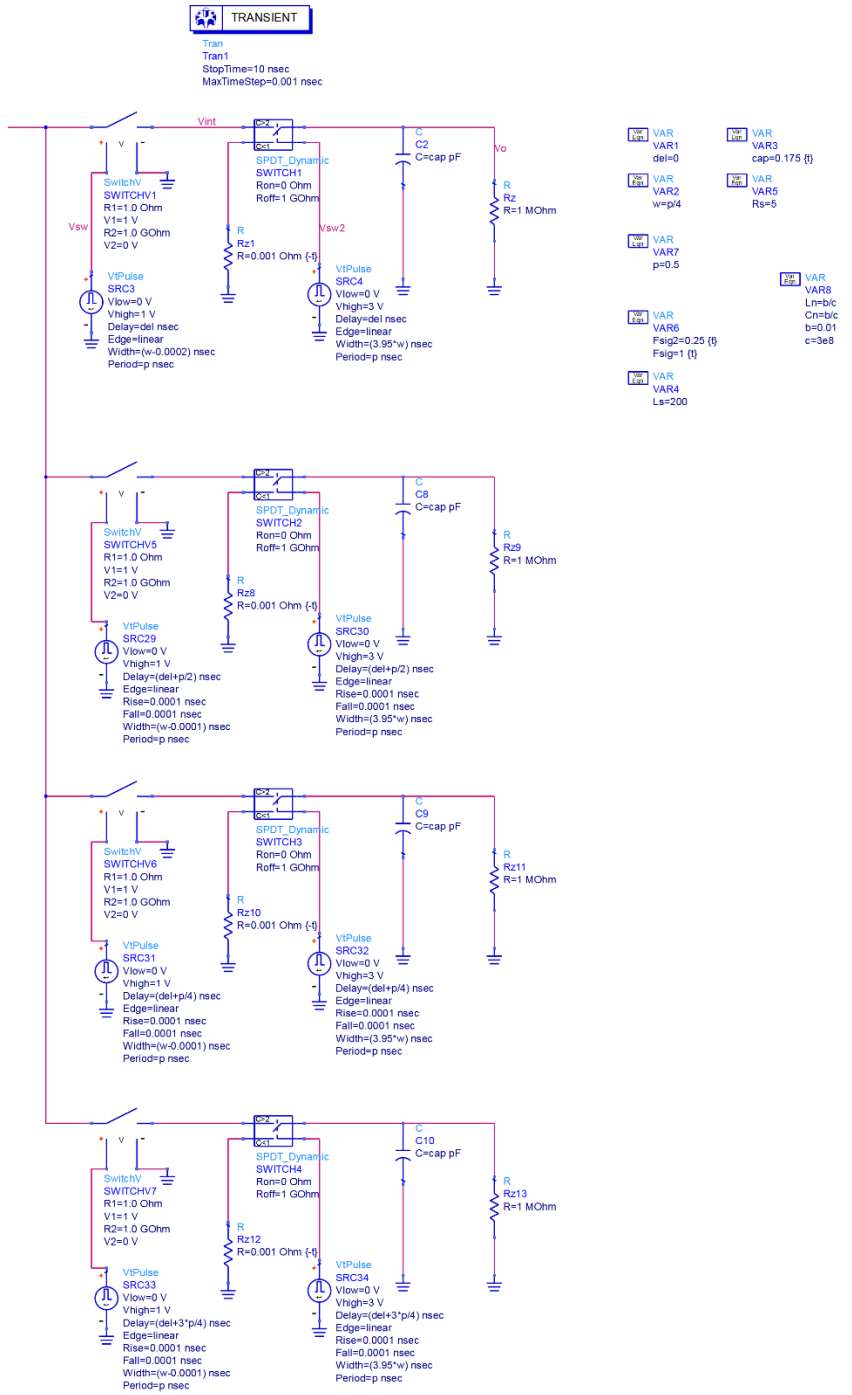
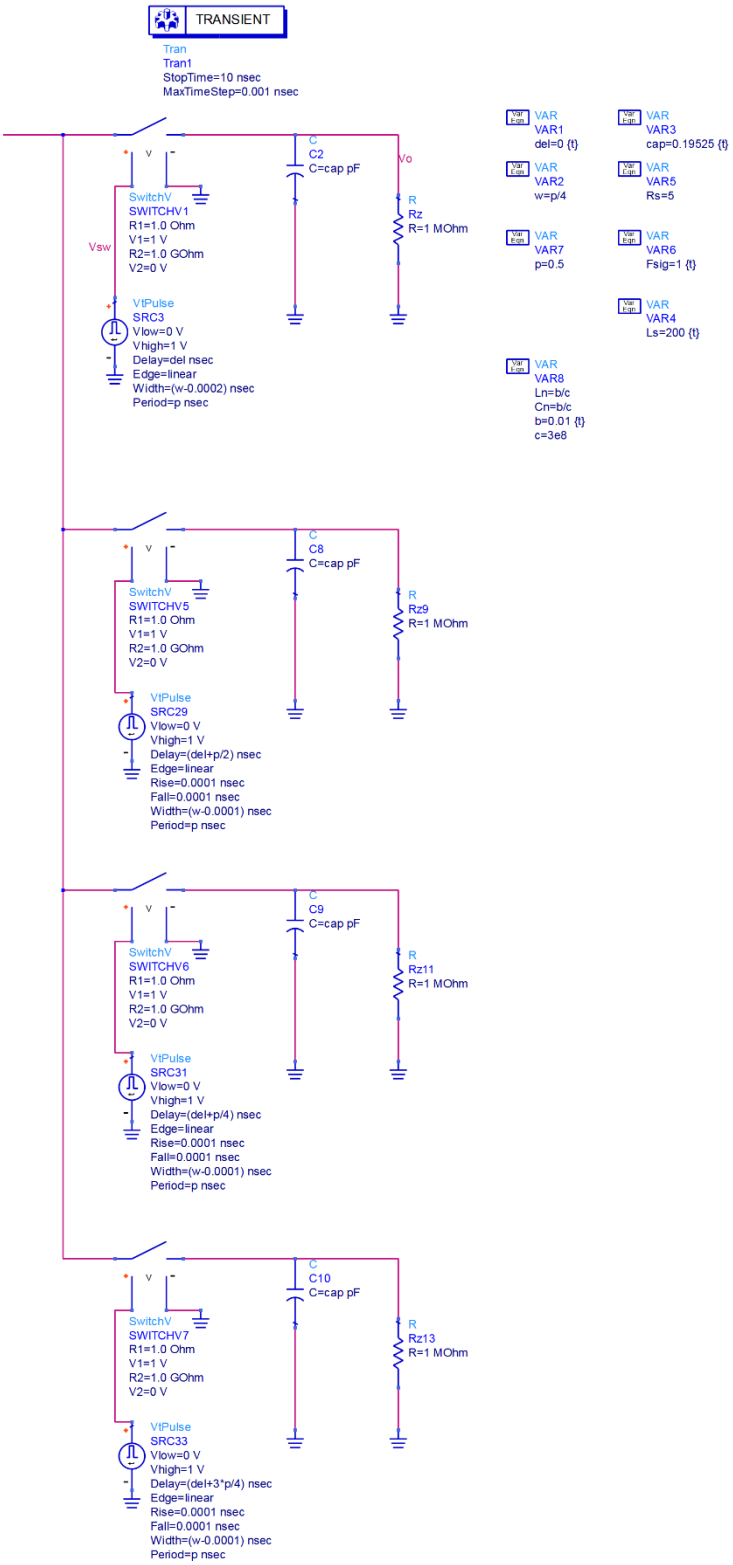
APPENDIX A: PATHWAVE ADS SCHEMATICS

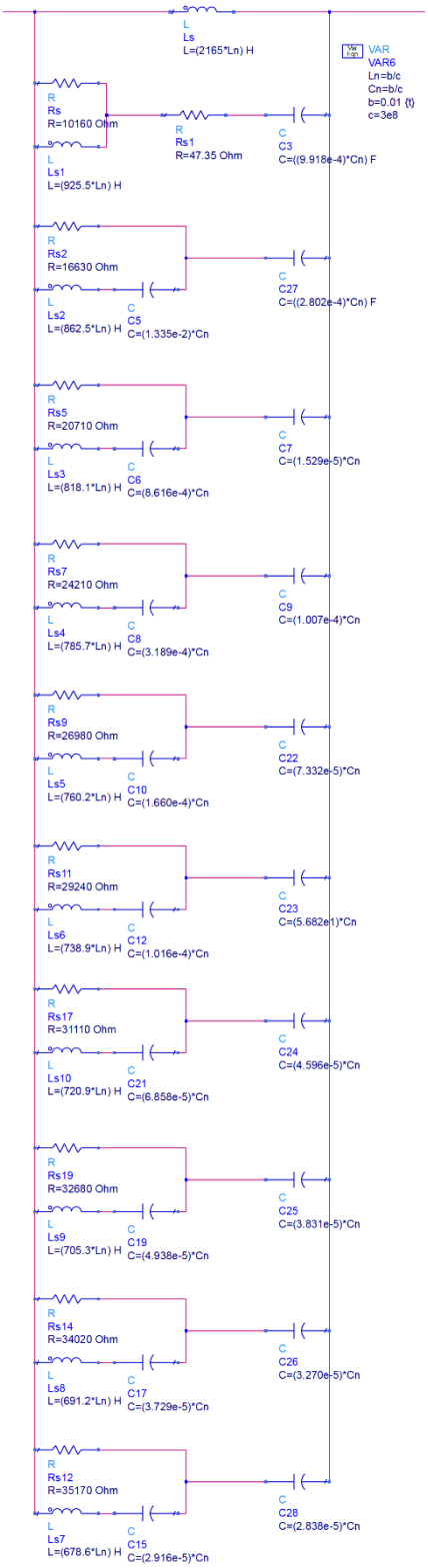
A.1 Modified sampling network, 4-phase configuration



A.2 Conventional sampling network, 4-phase configuration.



A.3 Loop Antenna Model, full schematic



Dipole Antenna Model