COMPARISON OF VARIOUS PERFORMANCE CHARACTERISTICS OF NEW TO AGED

MICROCHIPS

A Thesis

by

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ABSTRACT

In our ever-modern society, semiconductor devices are becoming increasingly common throughout the average person's daily life. These ordinary people go along with their days not thinking about the effect of how their lives might change if one of these devices were not designed in their original format but instead tampered with by bad actors who either refurbished used chips and labeled them as new or installed hardware trojans that can render the device inoperational. This research aims to find and eliminate these dangerous devices from the supply by detecting their abnormal behavior. The research is set up to perform DOE or Design of Experiments analysis to characterize the effects four input factors have on the operation of MSP430 microcontrollers in six different types of responses. The four input factors that are considered in this paper are Voltage Common Collector (Vcc, also known as Supply Voltage), Temperature, Humidity, and Age. The measured output responses are VIL, VIH, VOL, VOH, and two types of power consumption. A set of chips were accelerated at approximately 10 and 20 years old through increased temperature and Supply voltage. Overall, this research determined that Supply Voltage was the most significant of the four input factors, with temperature coming in second place. Throughout the course of this research, it was also determined that output load might be an important factor that was not integrated into the DOE analysis.

DEDICATION

This paper is dedicated to my late grandfather, Jim Jackson. Throughout my childhood and teen years, he was always there for me when I needed him. He taught me many of the skills and life lessons that I hold dear to this day. Although it has been nearly 5 years since his passing, I know he is up there in heaven, smiling down upon all my accomplishments to this point. I plan to continue his legacy throughout the next chapter of my life and one day become as good of a man as he was.

ACKNOWLEDGEMENTS

I would like to thank my committee chair, Dr. Rainer Fink, for allowing me to work on this project. I would also like to thank my committee members Dr. Wei Zhan and Dr. Jeyavijayan Rajendran, for assisting me throughout the process of this project.

Thanks also go out to members of the ETID department for guiding me through processes I didn't fully understand and making things work as intended. Special thanks to Dr. Logan Porter for allowing me to be the Graduate Assistant Teaching his course ESET 219, enabling me to attend graduate school. Thanks also go out to Professor Thomas Munns; without him selecting me to become an undergraduate teaching assistant for his class ESET 352, I would not have never known the opportunity to attend graduate school in the first place.

Finally, thanks to my parents, Becky, and Neal Schneider, for providing me with every possible opportunity to be successful in my academic career.

NOMENCLATURE

Vcc   Voltage Common Collector

GAT   Graduate Assistant Teaching

PC   Power Consumption

VIL   Voltage Input Low

VIH   Voltage Input High

VOL   Voltage Output Low

VOH   Voltage Output High

SNR   Signal to Noise Ratio

P   Power

I   Current

V   Voltage

CSV   Comma Separated Variable

DUT   Device Under Test

GPIO   General Purpose Input Output

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1. INTRODUCTION

Over the last several years, cyber security has become one of the hottest topics worldwide. A new breach seems to be publicized every single week. Bad actors will stop at nothing to get their hands on people's private information or disrupt operations. One of the ways that bad actors attack is to infiltrate the chip manufacturers themselves to either add a hardware trojan to a microchip or rebrand used or old chips as new chips. This not only harms the customer, who is not getting the product they purchased, but also damages the company's reputation that makes the real version of the chip that was sold. That is where this research comes into the equation.

This research aims to find the effects of different inputs on the outputs of an MSP430 using Design of Experiment or DOE analysis. The different inputs that were originally posed to be tested are Age, Humidity, Temperature, Common Collector Voltage (Vcc), and Chip-to-Chip Variation. The outputs that were posed to be tested are Voltage Input Low (VIL), Voltage Input High (VIH), Voltage Output Low (VOL), Voltage Output High (VOH), and Power Consumption. By applying these conditions and measuring the outputs, it is assumed that chips that are tampered with will have different responses than what is anticipated with normal versions of the chips.
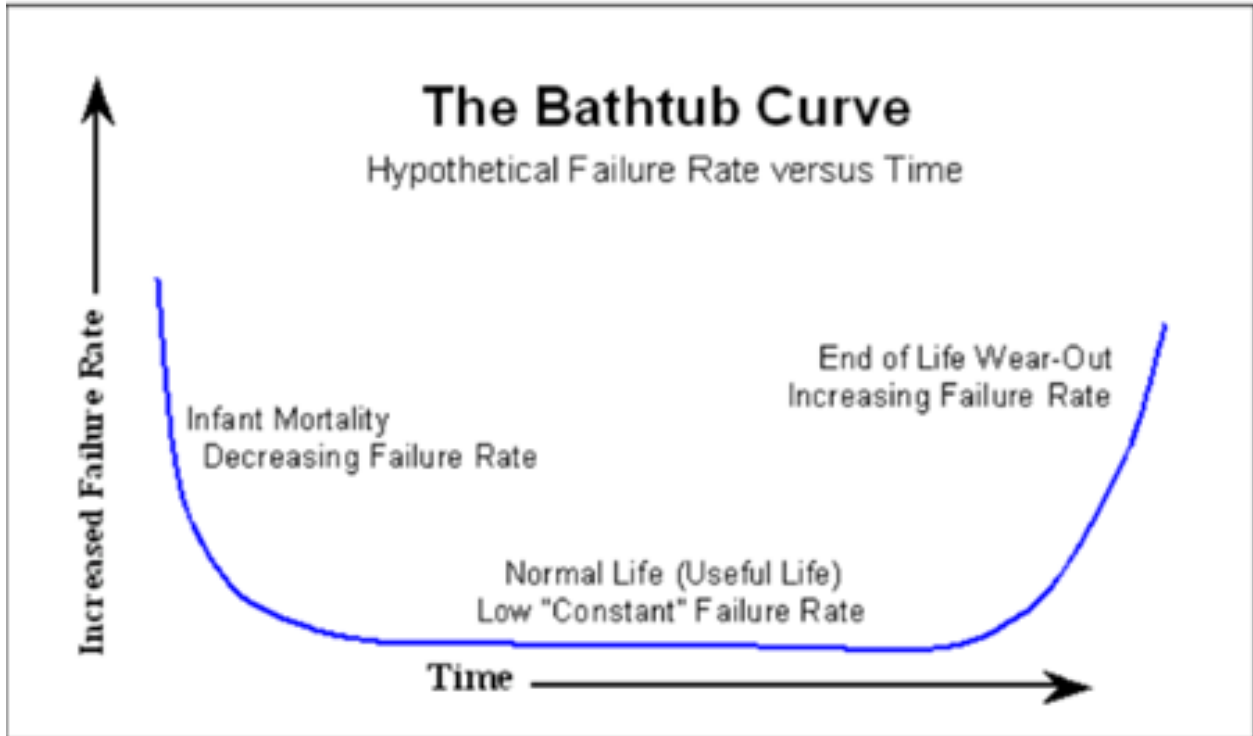
Figure 1. Bathtub Curve – Image Credit [1]

Ultimately, the result of this project is to offer a new way to test microchips for defects and counterfeits rather than the traditional method of Burn-in testing, which is used throughout the industry currently, and to view the bathtub effect of microchips as they increase in age. Burn-in testing is an extreme stress test on a component that operates at a condition such as voltage, current, temperature, and frequency at or above its maximum limit [1]. The bathtub effect is the hypothetical failure rate of a population compared to time [1][2]. The effect contains three sections: Infant Mortality, Normal Life, and End of Life Wear-Out, and can be observed in Figure 1. Infant Mortality is where the failure rate decreases, and defects usually cause the failures. During Normal Life, failures are extremely unlikely to occur.[2] When a chip reaches the end of life, the failure rate increases as the chips become worn out as materials used inside the chip begin to fail. This project primarily focuses on the beginning of life for a chip to detect defects and the end of life to see where the chips wear out over time through accelerated aging. It

is theorized that if a chip contains a hardware trojan or is a counterfeit, it will wear out faster

than an Original Equipment Manufacturer (OEM) component.

2. BACKGROUND RESEARCH

The aging of microchips is a very important part of the semiconductor industry. In the semiconductor industry, it is known as HALT or Highly Accelerated Life Test. It is a method to apply the chip under a high amount of stress in a short amount of time "to discover weak links of a product. Utilizing the two most common testing stimuli, temperature and vibration, it can precipitate failure modes faster than traditional testing approaches."[3] It is not meant to characterize the performance of a chip but to find the weak links within the design or material or the chip. It essentially breaks the weakest link in the chain. Another characteristic of an older chip compared to a new chip is that the performance of the chip will degrade over time. "One of the impacts of aging is a rise in the device's leakage current, which leads to a decrease in transmission quality and a rise in energy consumption. The decrease in threshold voltage caused by aging impacts the device's switching properties, such as turn-on and turn-off timings.".[4] This is due to a change in the chip's capacitance values and an increased failure rate as the chip ages, thus showing us the wear-out phase of the bathtub curve.

Another used for high temperatures in the semiconductor industry is Burn-in Testing. "A burn-in test is a special type of stress test conducted on electronic devices prior to their public release which uses some combination of high temperature and/or high electrical voltage to determine whether the device being tested or any part of it, is likely to fail or malfunction in the early stages of its product life."[5] Burn-in tests typically run at or beyond the publicized maximum operating temperature that the chip is rated for to bring out failures in the bathtub curve's infant mortality phase. This process better optimizes manufacturing to reduce the number of chips that fail early in their lifespan. A burn-in test typically occurs within an oven capable of stacking multiple PCB on top of each other with sockets that hold the chip being tested. "The

sockets are equipped with features such as heat sinks, temperature sensors, fans, and heaters to help individual DUTs achieve a more uniform burn-in temperature. A feedback loop is set up between the heater, fan, and sensor to allow more individual temperature control over each DUT in the oven. "[6]. These sockets are used repeatedly to test different DUT and to keep the line moving. Overall, Burn-in Testing is an important part of the semiconductor industry that ensures the products are top-notch.

As stated in the introduction, one of the main motivations for this project is to find potential counterfeit chips. One of the main features of a counterfeit chip is that they are more likely to experience failures than a new Original Equipment Manufacturer chip. "Counterfeits are often "harvested" from electronic waste using crude and poorly controlled processes that result in counterfeit semiconductors having far higher failure rates than the genuine articles. Some of these 'harvested' chips will fail immediately when electrically tested or first used, while others will fail after days, months, or years in the field." [7]. If a counterfeit chip were to be integrated into a system whose operation is critical, it could lead to disastrous effects like property damage or even death. This risk only increases yearly as society increasingly relies on electronics for our everyday lives. Therefore, finding and eliminating these dangerous chips from the supply chain is more important than ever to ensure a positive future for everyone.

3. RELATED RESEARCH

3.1 A Clock Sweeping Technique for Detecting Hardware Trojans Impacting Circuits Delay

In this paper, the researchers set out to implement and prove that a delay-based technique could be used to detect hardware trojans. This was done by looking at the propagation delay between different nodes, which is an output of a logic gate. The researchers theorized that adding a hardware trojan at the node would increase the load capacitance, thus increasing the delay time it takes for a signal to go from one point to another inside the chip. The researchers also added a clock sweep to their test patterns to increase the likelihood of a hardware trojan being detected. The trojan would be detected by the logic failing at a particular frequency. This method worked well for a long path since the amount of delay between the two nodes is longer than the period of any of the tested frequency ranges. However, it only worked when in paths that were considered short due to the delay time being less than the period of the clock cycle being tested. This was of less concern to the researchers as it is noted that trojans close to a node tend to consume more power as the gates within the system are more likely to activate, thus meaning other trojan detection methods, such as looking at power consumption, are likely to detect the difference between a clean and modified chip. In their tests, they tested 300 chips, with 200 not having hardware trojans and 100 a trojan. This test was completed for 6 different types of trojans with different levels of complexity. They successfully detected all the hardware trojans in 5 out of the 6 tests. In the single test that did not have a 100 percent success rate, they discovered 64 percent of compromised chips. This was theorized to be the case because the Trojan was extremely simple, with only a single path. A big takeaway from this research is that the larger the hardware trojan, the larger the frequency step size needs to be to detect the trojan due to the increased

amount of points from which the digital logic can be triggered. Overall, this paper gives an interesting insight into how to detect hardware trojans without modifying a chip in any way and can be easily implemented by manufacturers worldwide with their current test equipment.

3.2 Thermally Accelerated Aging of Semiconductor Components

In this experiment from nearly 50 years ago, the author Frederick Reynolds set out to prove the importance of using temperature to accelerate the aging process within semiconductors. This process was originally proposed in the 1960s but was not widely accepted as possible at the time. Throughout his testing process, he looked at the failure rate induced by testing. The components he tested were all simple in nature since all the ideas he was testing at the time were purely theoretical. It was found that as the temperature at the components being tested increased, the rate of failures that were observed also increased in a straight line, indicating a correlation between the test condition and the rate of failures. After the test was complete, it was also proved that the components could not be returned to their original state before the test. He also noted, there were a lot of areas within his tested mechanism that could have led to the increasing failure rates that were observed. This would not be a problem if the parameters were measurable and separate from each other, but problems arise when they are connected. To solve this problem, the author recommends having a large sample size of at least 20 through the use of statistics. The paper ended with the quote, "History will very likely show that the thermal acceleration technique is neither valueless nor faultless [9]". I find it interesting that the author was accurate in his analysis. This research was extremely valuable to the semiconductor industry's future.

3.3 A Sensitivity Analysis of Power Signal Methods for Detecting Hardware Trojans Under Real Process and Environmental Conditions

This paper analyzes power signals on the multiple individual power ports of a chip to detect hardware trojans. This works by using statistics to find anomalies within a data set. The process implemented by the researchers involved calibration circuits that are implemented into the chip to allow for the amount of noise in the system during the test to be reduced. The calibration circuits also deter potential bad actors, as any changes to the calibration setup are easily detectable. For the actual experiment, the researchers tested 15 models, 10 with trojans of increasing size and 5 that were trojan free. These models were tested under several different environmental conditions from 0 to 30 decibels of SNR and four levels of background stimulus on the chip. It was discovered that extremely simple trojans with a single gate could be detected in an environment with no noise. However, it became more difficult to detect trojans with up to 3 gates when increasing the amount of noise. When the number of gates reached 4, the trojans became easily detectable. The other condition tested in this experiment was the 4 different types of stimulus applied to the chip to add background switching activity to the chip. The trend discovered by this test was that it became more difficult to detect the trojan with more background switching activity within the chip. It was found that the magic number for gates in a trojan for it to be detectable with the increased background switching to be 5 gates. Overall this paper follows the general trend that the larger the hardware trojan, the easier it is to detect in a test environment.

4. THE AGING PROCESS

4.1 What Is Accelerated Aging

Accelerated aging is the process of running a microchip at conditions beyond its normal operating conditions to increase the amount of wear on the chip. The amount of wear produced on the chip is equivalent to its age; therefore, an older chip has much more wear on it. The most important factor when aging a chip is how much the environmental conditions increase the rate at which the chip is aging. To complete the aging process in this project, we found a formula that calculates the acceleration factor, which is the rate of increased aging of a microchip from Tom Resh [11]. The formula, which can be found in Figure 2, has 8 inputs that we had to account for to calculate the AF or acceleration factor. V2 is the test voltage or voltage the chip runs at while aged. V1 is the normal operating voltage of the chip. n is the voltage constant of the chip. eV is the activation energy which is a default 0.7. k is Boltzmann's constant which is 8.62 x 10^-5 eV/k. T1 is the normal operating temperature of the chip in Celsius. T2 is the test temperature of the chip or the temperature the chip is run at while being aged in Celsius. Using this formula, we produced an acceleration factor of 226.3453 or 16.1258 days to age the chips 10 years based on the conditions that were able to apply to the Environmental Chamber that was used throughout the project. The condition we used for testing was a V2 of 3.6 volts, a V1 of 3 volts, an n of 3 volts, a T1 of 25 degrees Celsius, and a T2 of 90 degrees Celsius. The V2 value of 3.6 volts was chosen as it is the absolute maximum Vcc voltage of the MSP430. V1 and n were selected as 3 Volts since that was the standard voltage under which we were testing the chip. The T1 temperature of 25 degrees C was selected because that is the standard ambient temperature used throughout the industry. The T2 temperature of 90 degrees C was selected because that is the highest temperature the Environmental Chamber could sustain during aging. The chips were

aged for 10 years twice, with data being collected at 10 years old and 20 years old, meaning that the chip was run at 90 degrees Celsius and 3.6 volts for 32.25 days.

$$AF = \left(\frac{V2}{V1}\right)^n * e^{\frac{eV}{k}\left(\frac{1}{T1+273.15} - \frac{1}{T2+273.15}\right)}$$

Figure 2. Formula to Aging Microchips Faster using Temperature and Voltage

4.2 Hardware Development

Since it takes 16 days to age the chips 10 years, we needed an automated system that ensured that the chips were running at the correct temperature and voltage level without anyone present. The functional block diagram for the system that was used can be seen in Figure 3. The centerpiece was the polycarbonate environmental chamber. Inside the chamber were two heating elements. One of these heating elements was constantly connected to 120V AC power from the wall. Therefore, remained permanently on. An AC plug relay from the Arduino controlled the other heating element. The Arduino received the internal temperature of the environmental chamber through an SHT40 temperature sensor and then turned the heater on and off based on that information. Due to the voltage difference between the AC plug relay and the Arduino, we had to connect an Arduino relay to the system. The Arduino powers this relay. This relay takes a GPIO high or low from the Arduino. If the signal from the Arduino is high, it closes the relay, and if it is low, it opens the relay. When the Arduino relay is closed, it closes the circuit starting at the 5-volt power supply output that goes through the Arduino relay to the AC plug relay and then back to ground at the power supply. A second channel on the power supply also provides

the 3.6 volts that are needed by the MSP430s. The MSP430s are attached to the outside of the

environmental chamber so that only the chip and its socket are exposed to the increased

temperature. This means that only the chip is aging, not the entire board. This setup can be seen

in Figure 4.
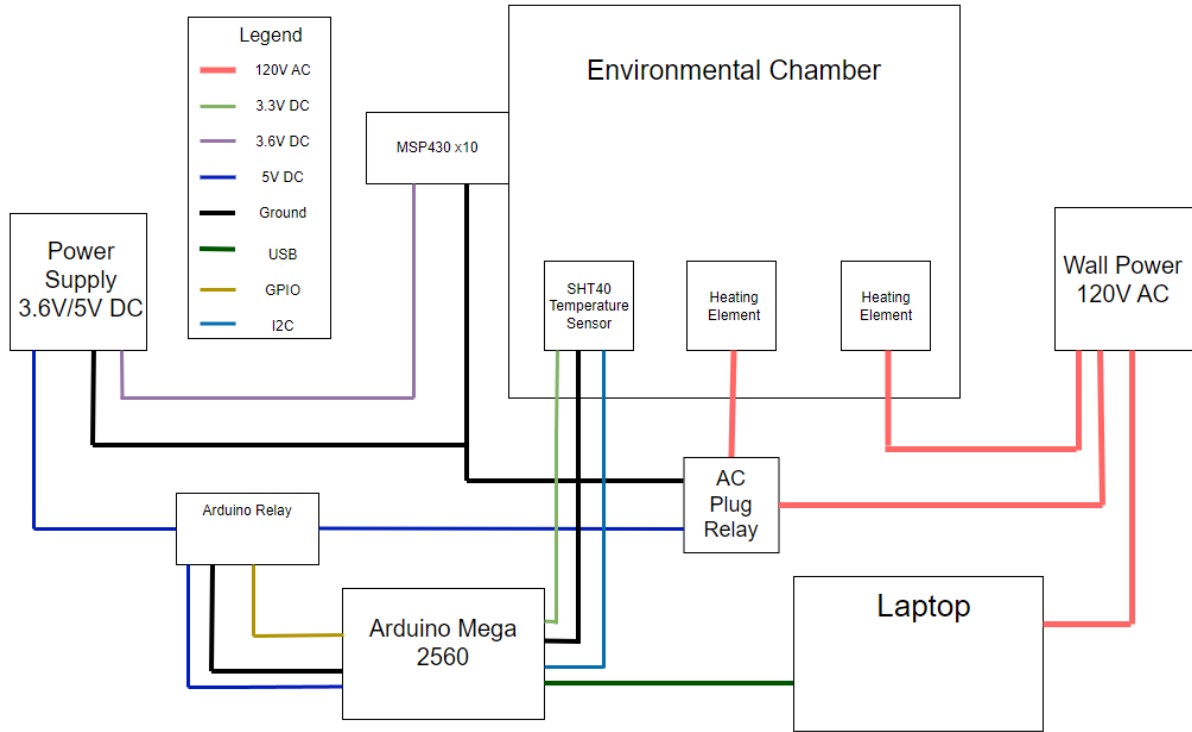
Figure 3. Aging Functional Block Diagram
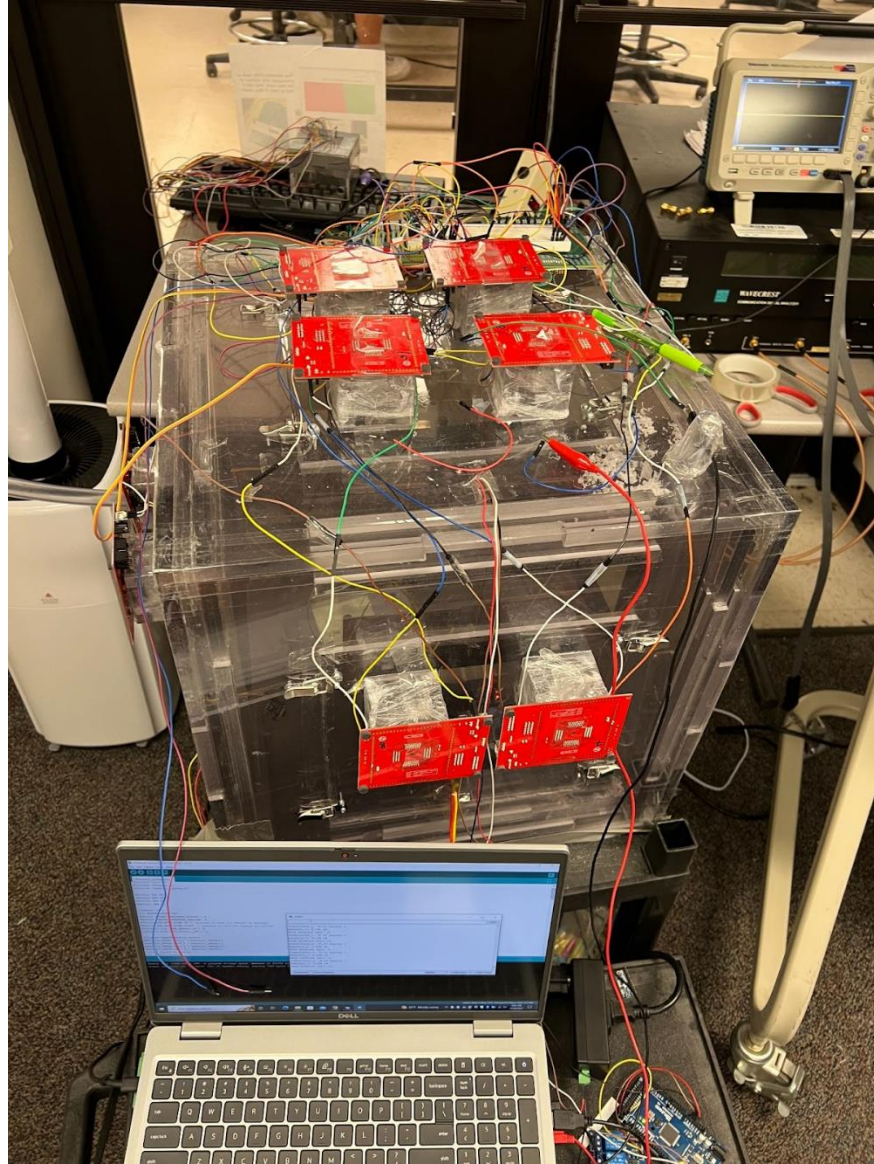
Figure 4. Hardware Setup for the Aging Process

4.3 Software Development

Two different pieces of software were used during the aging process. The first is the code

created for the Arduino for use in the aging and testing process. This program took a single input

from the user: the desired temperature. The user would input the desired temperature, and the

Arduino would open and close the relay to maintain the desired temperature. To better control

the internal temperature, dead bands were used to maintain the temperature range to a minimum.

The dead bands that were used were -0.2 for when the temperature was falling and 0.2 for rising. For aging purposes, when the internal temperature fell below 89.8 degrees Celsius, the relay would close to increase the system's temperature, then open when the temperature reached 90.2 degrees, allowing the system to cool down. This setup leads to a range of plus or minus 0.5 degrees Celsius during aging. This program was provided by previous researchers working on this project.

The second piece of software that was created was for the MSP430s. This code was an infinite loop that turned all the GPIO pins of the MSP430s on and off again through exclusive ORing the logic at its current state. This means that all of the GPIO pins were set to outputs and turned off and on again for the same amount of time for the entire duration of the aging process. One benefit of this code is that an LED on the board that the MSP430s were socketed in would turn on and off when the chip was powered, indicating that the board was operational. This ensured that everything was working as intended in a short amount of time.

4.4 Problems Encountered During the Aging Process

The project process of accelerating aging came with its issues. The first major issue that was encountered was that the environmental chamber began fogging up, and what looked like mold was growing inside the chamber. An example of this can be seen in Figure 5. The decision was made to pause the aging process and clean the chamber out with a degree of caution. When the chamber was opened, plastic flakes were found throughout every crevasse in the MSP430s socket, as seen in Figure 6. The chips were cleaned off with isopropyl alcohol, and the entire chamber was disinfected before restarting the aging process.
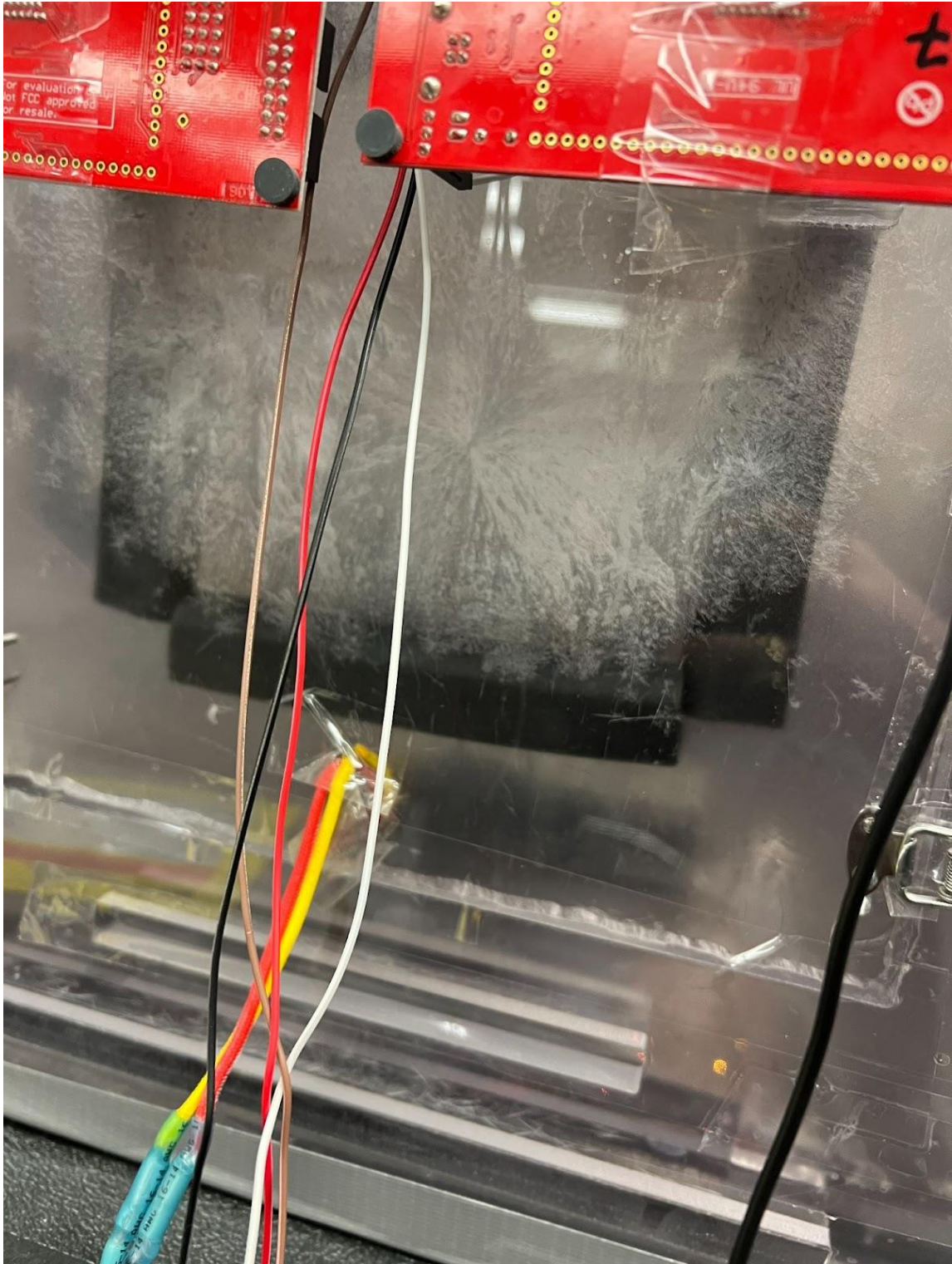
Figure 5. Fogging of the Environmental Chamber
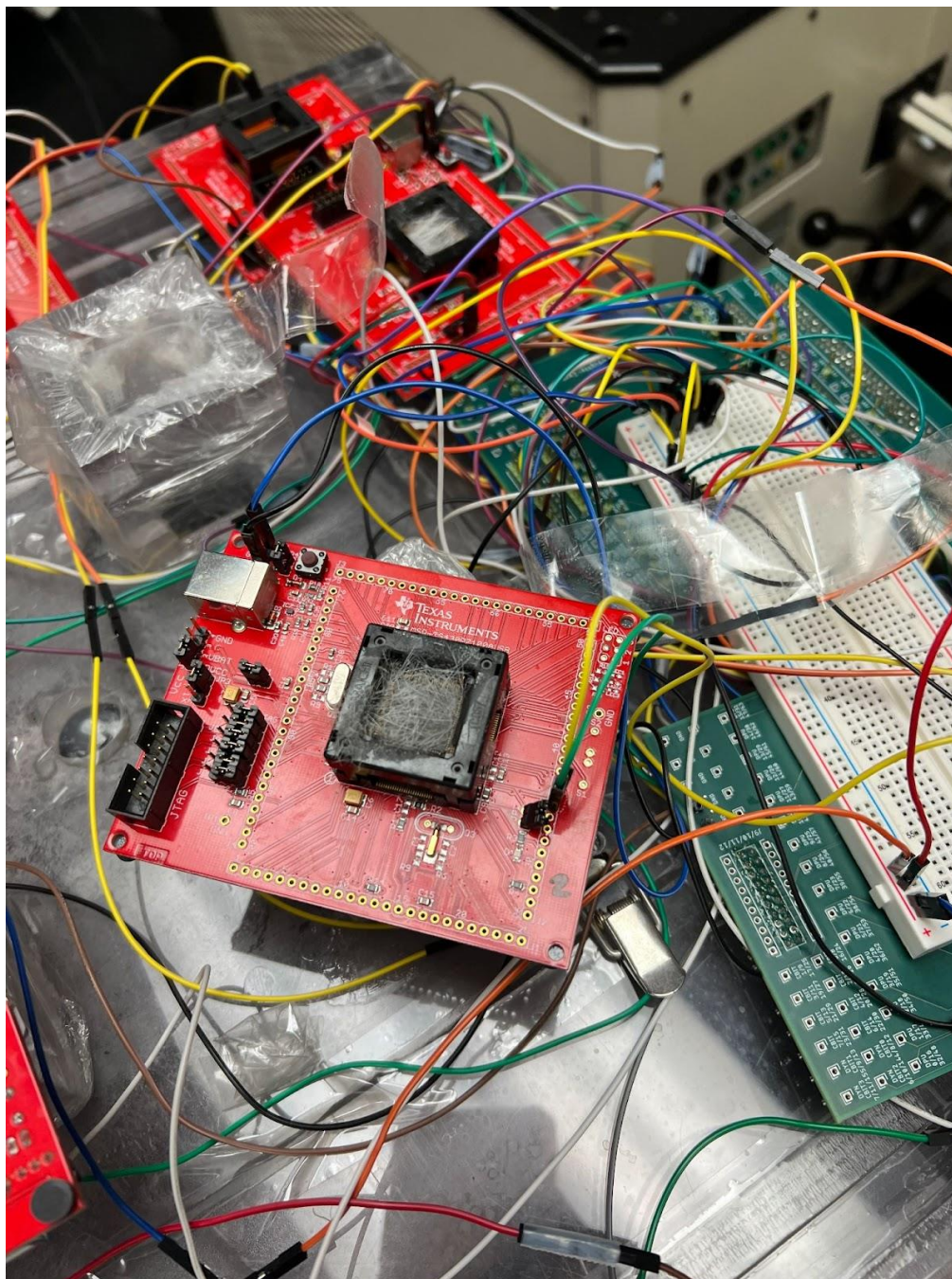
Figure 6. Plastic Flakes Located on MSP430s

After the plastic shard issue, there were no additional problems that arose with the first 10 years of aging. During the 10 to 20-year aging process, there were 2 mild complications. One morning when checking the status of the chamber, the internal temperature had dropped to 78 degrees Celsius due to the AC plug relay becoming disconnected. It was estimated that the relay

was disconnected for approximately 3 hours. Therefore, dropping the temperature by 12 degrees Celsius. The test was extended by that amount of time when the chamber reached 90 degrees Celsius again. The second of these minor issues was that the LED on chip 4 needed to be fixed upon checking it. It was found that the shunt[12] that controls whether the LED is enabled had fallen off, but the chip was still operating as intended; therefore, no adjustments were made due to this problem.

The final and largest issue that was encountered during the aging process was found once the chips had reached 20 years old. Due to the chamber's seal being faulty, the chamber had to be disassembled. When opened, the area below the main heating element was completely melted through. This led to a giant hole in the bottom of the environmental chamber. The aftermath of the melted polycarbonate can be seen in Figure 7. With the significant damage caused to the environmental chamber, the decision was made to scrap it and build a new chamber that would handle the heat produced by the heating elements. Upon further investigation, the environmental chamber melted due to the area around the heating element reaching up to 350 degrees Fahrenheit. The ½ inch of polycarbonate used in constructing the environmental chamber can only handle around 200 degrees Fahrenheit. The flaking of the chamber during the first 10 years of aging should have been a red flag that the materials used were not designed to be put under the conditions they were for an extended period of time. The damage was not visible until the box was taken apart because it was located on the bottom of the box and underneath the heating element. The cart that the environmental chamber had also sustained damage by permanently attaching the melted polycarbonate to it, as seen in Figure 8.
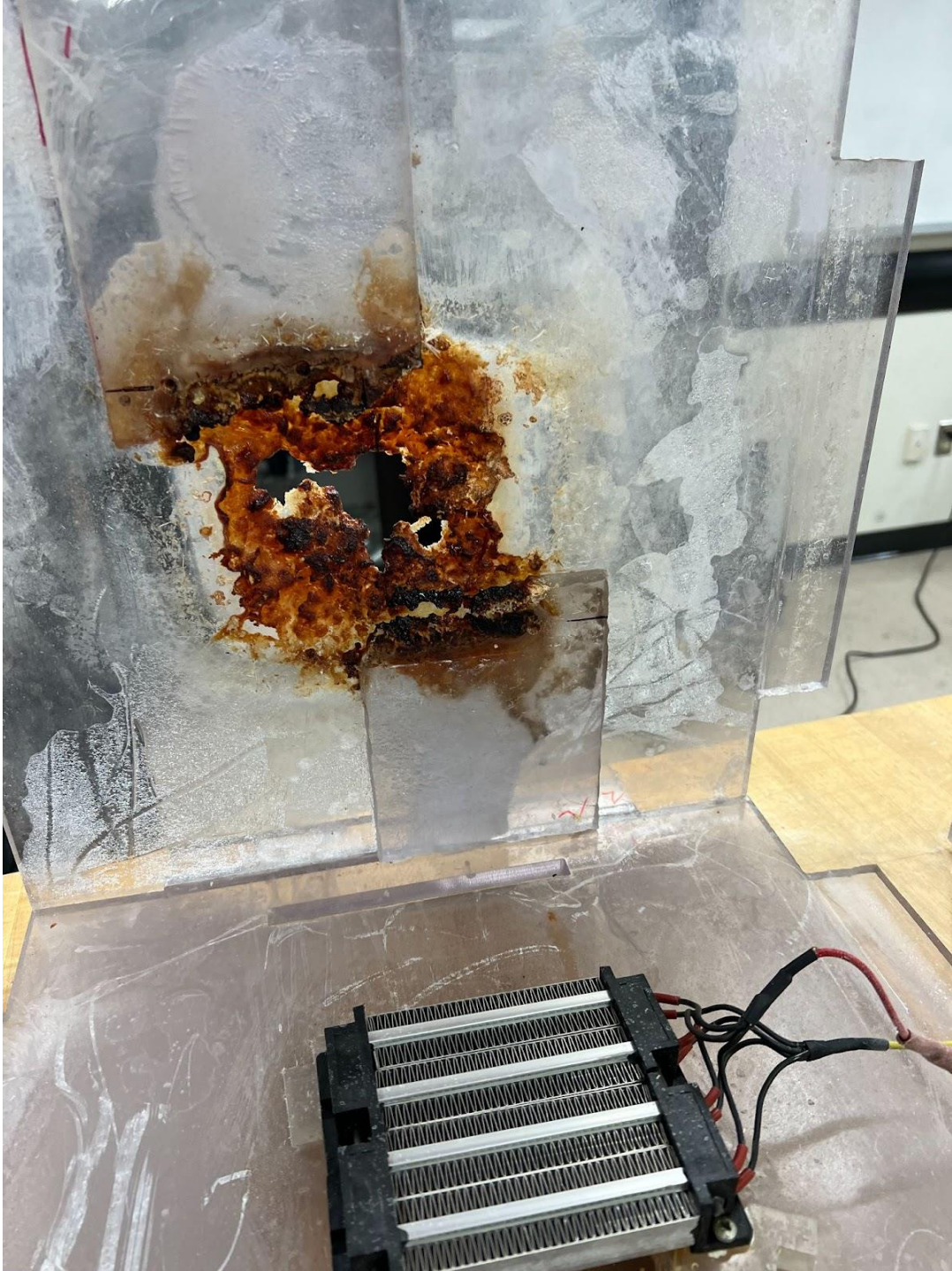
Figure 7. Melted Polycarbonate on the Bottom of the Environmental Chamber

Figure 8. Melted Polycarbonate on the Cart that Held the Environmental Chamber

5. TESTING SETUP

5.1 A New Environmental Chamber

As mentioned in the previous chapter, the environmental chamber that previous researchers on this project designed had to be discarded because it melted under high-temperature conditions for extended periods. A new chamber needed to be constructed to collect the data for this project and future research within the Mixed Signals Test Lab at Texas A&M University. Many of the lessons learned during this complication were considered in the design of the new Environmental chamber. The running joke in the lab was that the old environmental chamber was a box with a box; while that was not the case to keep the new design as simple and effective as possible, a box within a box was created. In the new chamber, the inside box in Figure 9 was made out of 304 Stainless Steel to handle the high temperature. The box is made out of six 18-inch by 18-inch ⅛ inch thick stainless steel sheets that are welded together. ¾ inch threaded stainless steel pipes are fitted at the top and bottom of the box for an inlet for humidity and a drain for any condensation that could form inside the box. Inside the Stainless steel box are the two heating elements used to control the chamber's temperature. In the old environmental chamber, a 1500-watt and 1000-watt heating element was used, while two 1500-watt heaters of the same type were used in the new chamber. To connect the inside box to the outside box, ⅝ inch high-temperature rubber was used.
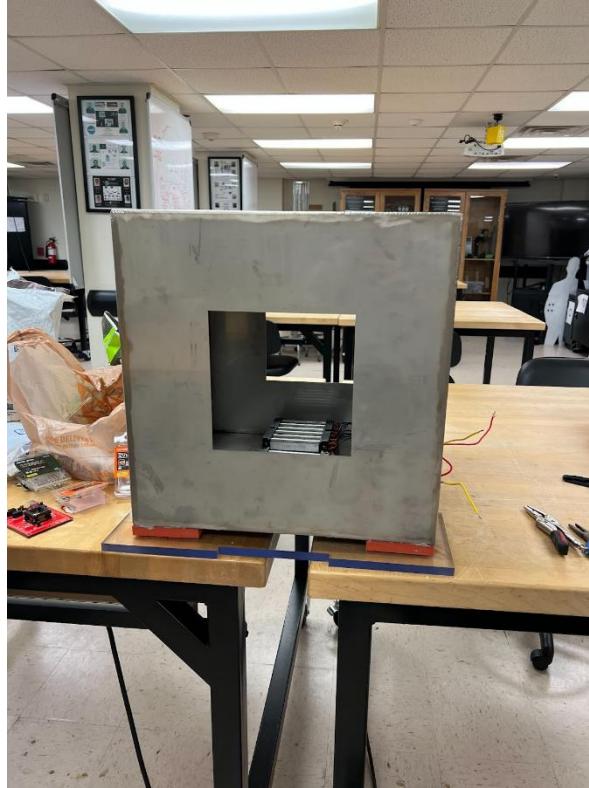
Figure 9. Stainless Steel Box with Heating Elements Inside

The rubber was connected to the stainless steel with high-temperature JB weld putty, which provided a strong bond between the two materials. In the area between the two boxes, there was a layer of ½ inch melamine foam that was attached, using nuts and bolts, to the stainless steel box to provide insulation in order to maintain the temperature within the environmental chamber better. The outside box was constructed with the same ½ inch polycarbonate as the previous generation of the environmental chamber. The polycarbonate box has dimensions of 20.5 by 20.5 by 20.5. This allowed the 18 by 18 by 18 stainless steel box and ⅝ inch rubber pieces to fit nicely with approximately 0.1 inches of tolerance. A high-temperature silicone caulk was used to completely seal the two boxes together, thus only allowing pressure to escape where the chip holders were located to ensure no leaks between the inside and outside boxes. Figure 10 shows the chip holder connected to the Box.
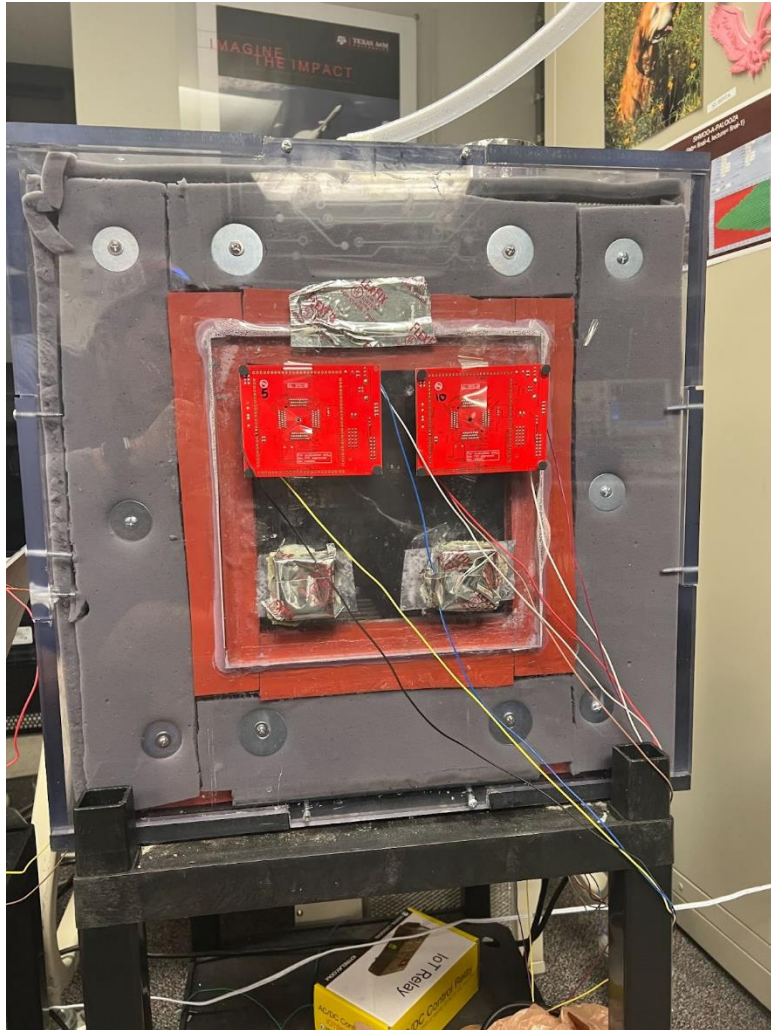
Figure 10. Chip Holder Connected to the Environmental Chamber

The chip holder is made out of ½ inch polycarbonate and allows for the chip to be

connected to the inside of the environmental chamber. It also allows the rest of the board to be

under ambient conditions. The chip holders have gaps just large enough to fit the socket of the

MSP430 inside. The chip holder Socket also extrudes out to cover the entire socket to have the

best seal between the chamber and the chip so that less pressure can escape. This extrusion is

made out of ¼ inch polycarbonate and is significantly smaller than the previous generation of the

environmental chamber. The difference in size can be seen in Figure 11. The smaller stature

allows the conditions the chip is experiencing to be much closer to what the temperature sensor is reading inside the chamber.
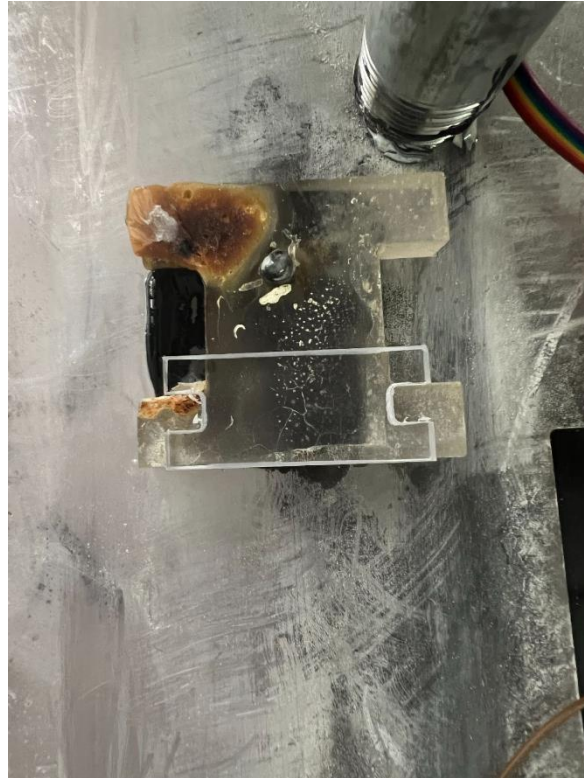
Figure 11. The Size Difference Between New and Old Chip Holder Socket

Overall the new environmental chamber provides better sustained performance for maximum temperature and humidity. The old chamber could only maintain 70 degrees Celsius and 50% relative humidity, while the new chamber can easily maintain 70 degrees Celsius and 65% relative humidity. This allows future researchers to test larger variations of environmental conditions than was previously possible for this research. Several improvements can also be made to increase the possible variation of environmental conditions. One potential change, would be adding a dehumidifier to the system to lower the humidity at lower temperatures, as the humidity at lower temperatures is currently dependent on the condition on the test floor. A

second Potential change would be to add a pump between the humidifier and the inlet of the environmental chamber. As pressure escapes through the inlet as the pressure is higher inside the box than coming out of the humidifier. A final potential change would be to use a thinner variant of the high-temperature rubber in the areas of the chip holder where a socket hole is not located, as that area is where most of the heat escaping the system is coming from.

5.2 Hardware Setup

The hardware setup used for the testing process can be seen in Figure12. The same code and setup were used to control the internal temperature of the environmental chamber as the aging process, as the dead bands produced a temperature range of plus or minus 1 degree Celsius at the testing temperature of 70 degrees Celsius. The SHT40 was also used to show the relative humidity of the environmental chamber. This enables the researchers to manually control the humidifier and adjust the internal relative humidity of the chamber. The MSP430 was attached to the Environmental chamber in the same way as the aging process. However, instead of being powered by a power supply, they were connected to the Eagle ETS-364 mixed-signal semiconductor tester. For each of the ten chips, the Vcc pin and two GPIO pins were connected to individual channels of the APU10, and each chip was grounded to the tester's ground. The connection was made to the test through jumper wires between the male pins on the tester and the male pins on the MSP430s. The connection to the APU10 allowed the researchers to control and measure the MSP430s to get the desired data.
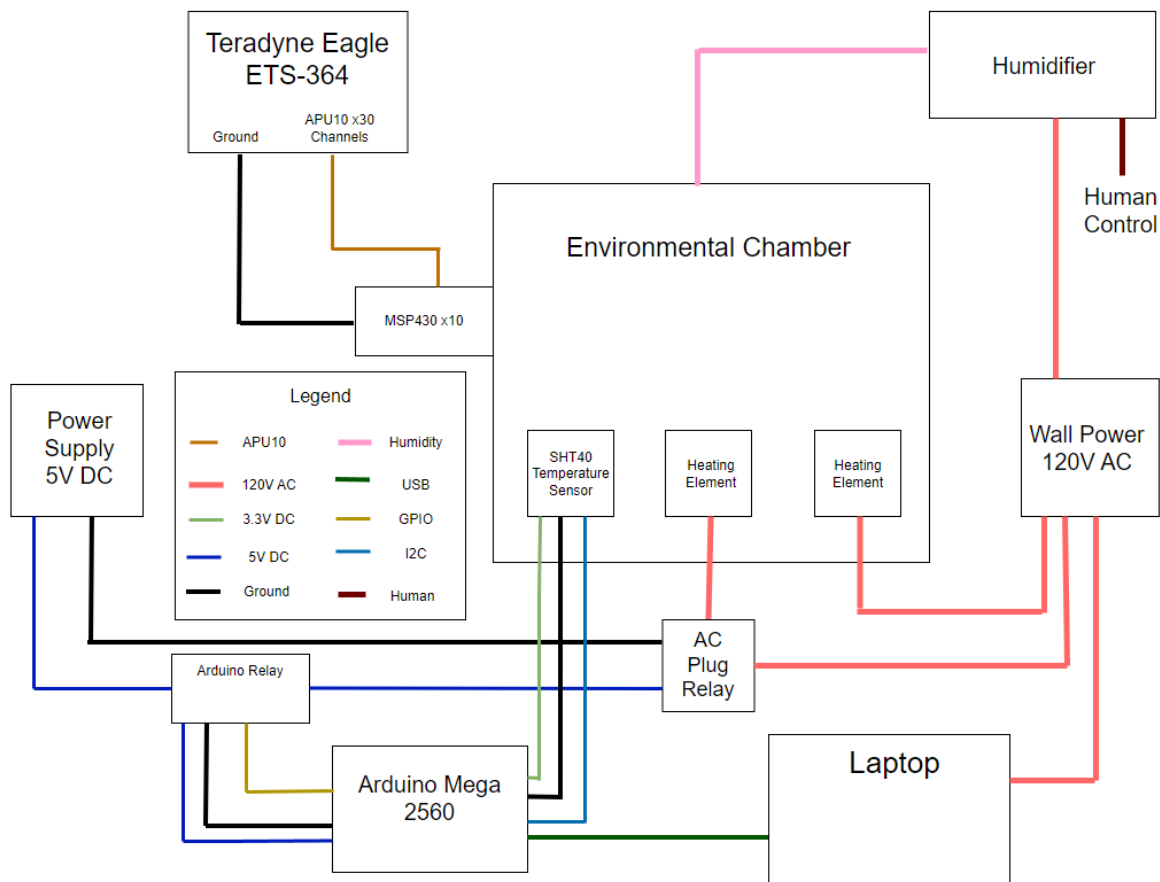
Figure 12. Functional Block Diagram of the Testing Process

5.3 The Eagle ETS-364 Mixed Signal Semiconductor Tester

The Eagle ETS-364 Mixed Signal Semiconductor Tester will collect this project's data. This is an industry-level semiconductor tester that is used throughout the world. We had three options when choosing the instrument within the tester, the SPU(Smart Pin Unit), the DPU (Digital Pin Unit), and the APU10 (Analog Pin Unit). The APU 10 was selected because it has more channels than the SPU and many current ranges for forcing and measuring. The eagle used for testing came equipped with 8 APU10 cards, each containing 8 channels; therefore, to connect all 10 MSP430s simultaneously, we had to use 30 channels of the APU. Each channel is connected to a pin connected to a corresponding pin on the MSP430. The APU10 has a 16-bit

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resolution for both measuring and forcing voltage and current[13]. The minimum possible step size is determined by the range that was selected. The larger the voltage or current range, the larger the minimum step size possible.

5.4 Software Development MSP430

The MSP430 was programmed with one GPIO pin as an input and another as an output. The output was programmed to follow the logic applied to the input pin. This allowed for three values to be acquired at the same time. The program was flashed onto the chips and would run automatically when powered on.

6. DATA COLLECTION PROCESS

6.1 Values Being Searched for

In this project, we are looking for 5 Unique values: Voltage Input Low(VIL), Voltage Input High (VIH), Voltage Output Low (VOL), Voltage Output High (VOH), and Power Consumption at the Power Pin. The easiest of the values to find is the power Consumption at the Power Pin as the voltage level is set on the power pin, and all that is needed to be done is measure the current that the Power Pin is drawing to find the Power Consumption through the Basic Formula Power equals Voltage times Current.

For VIL and VIH, we had to look at the Schmitt Triggers of the MSP430, which can be found in Table 1. Schmitt triggers rely on rising and falling edges to function. The voltage level on the input needs to rise from a low condition for the Positive-going input threshold to be triggered, and the input to fall from a high condition for the Negative-going input threshold to be triggered. "On the input rising edge the part will be guaranteed to switch between (Vt+ min) and (Vt+ max). On the falling edge the part will be guaranteed to switch between (Vt– max) and (Vt– min). The part is guaranteed not to switch between (Vt– max) and (Vt+ min)."[14] The Positive-going input threshold voltage is considered VIH and varies based on the input voltage. The Negative-going input threshold voltage is what is considered to be VIL. Based on Table 1, we see that there are two sets of positive and negative Schmitt Triggers based on the voltage of the input pin. Both the Schmitt trigger ranges would be tested; however, for the Vcc = 1.8-volt condition, previous research proved that the MSP430 could not operate at high temperatures with that low of a voltage, so it was raised to 2 volts for our testing.

Table 1. Schmitt Trigger Values for Positive and Negative Thresholds of MSP430 -

Modified from Texas Instruments Datasheet[15]

8.8.5.1 Schmitt-Trigger Inputs – General-Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1)   The same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

For VOL and VOH, the MSP430 datasheet provided the expected values based on the load applied to the output pin, as seen in Table 2. As the Schmitt triggers section stated, we used 2 volts Vcc instead of 1.8 volts Vcc. For this experiment, we set the output load to the low end of the recommended range provided by the datasheet. This means that under ideal conditions at both 2 and 3 volts Vcc, the VOH value is expected to be between Vcc-0.25 volts and Vcc, and the VOL value is expected to be between Ground and Ground+0.25 volts. A noticeable difference between testing for VOL and VOH is that testing for VOH current is sunk into the output pin while testing for VOL current is pushed into the output pin.

Table 2. GPIO Output Characteristics of the MSP430 - Modified from Texas Instruments

Datasheet[15]

8.8.5.4 Outputs – General-Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)} = -3 \text{ mA}^{(1)}$	1.8 V	$V_{CC} - 0.25$	V_{CC}	V
		$I_{(OHmax)} = -10 \text{ mA}^{(2)}$		$V_{CC} - 0.60$	V_{CC}	
		$I_{(OHmax)} = -5 \text{ mA}^{(1)}$	3 V	$V_{CC} - 0.25$	V_{CC}	
		$I_{(OHmax)} = -15 \text{ mA}^{(2)}$		$V_{CC} - 0.60$	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)} = 3 \text{ mA}^{(1)}$	1.8 V	V_{SS}	$V_{SS} + 0.25$	V
		$I_{(OLmax)} = 10 \text{ mA}^{(2)}$		V_{SS}	$V_{SS} + 0.60$	
		$I_{(OLmax)} = 5 \text{ mA}^{(1)}$	3 V	V_{SS}	$V_{SS} + 0.25$	
		$I_{(OLmax)} = 15 \text{ mA}^{(2)}$		V_{SS}	$V_{SS} + 0.60$	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

6.2 Tester Software Development

There were 8 pieces of C++ software developed for this course of this project. Five of these programs were developed during a previous researcher's project, and three were developed for this project. The Code has two sections: the controls and the tests. The controls are a set of variables that control various aspects of the tests in a single location that is easy to manipulate. The items that can be controlled are the APU channel that is assigned to connect to the MSP430s, the number of MSP430s that are being tested, the number of tests being run, the voltage step that is applied to the input pin of the MSP430, and the file name of the outputted CSV file.

The second section contains all of the tests that were run throughout the project. Each test either ramped the voltage on the input up or down, which will be referred to as ramp up and ramp down, respectively. The First set of tests that were run was the Ramp up and down test at a Vcc voltage of 3 volts. The basic setup of the code had 2 for loops and a while loop. The two loops are located outside to control the test number and the site being tested. A new CSV file

was created for each test number loop to log the collected data. The second For loop enables the pins needed to test that site, set the voltage on the power pin, and ensure that the MSP is low. At this point in the code, an initial voltage level is set on the input pin to make the number of voltage steps to trigger the Schmitt trigger smaller, thus decreasing the required test time. The while loop is located in the furthest inside the program and increases the input pin voltage level until the loop is broken. The while loop runs until the Schmitt trigger is activated or the input pin voltage equals the Vcc voltage. Since the code that was created for the MSP430 sets the output pin state equal to the state of the input pin, when the Schmitt trigger is reached, the output pin goes high, thus breaking the while loop. When the while loop is broken, the input's voltage is logged simultaneously, and the power consumption allows the researchers to find the desired values within the CSV file quickly. Between each Site and test run, all of the APU pins are turned off to ensure all tester's components are deactivated. The main idea behind the ramp-up code can be seen in Figure 13. As shown, the Highest expected voltage is the Vcc voltage, with the VOH voltage slightly below it. The trigger point is set to a voltage level lower than the datasheet's expected value because operating the chip at extreme conditions affects the functionality and can cause the trigger point never to be reached if it is set too high. The arrow represents the voltage on the input pin where it originally starts at 0 volts to ensure the output is low. Then it is raised to a predetermined value based on the Vcc voltage to be slowly incremented up until the Output Voltage goes high. Thus breaking the while loop and moving on to the next chip that needs to be tested.
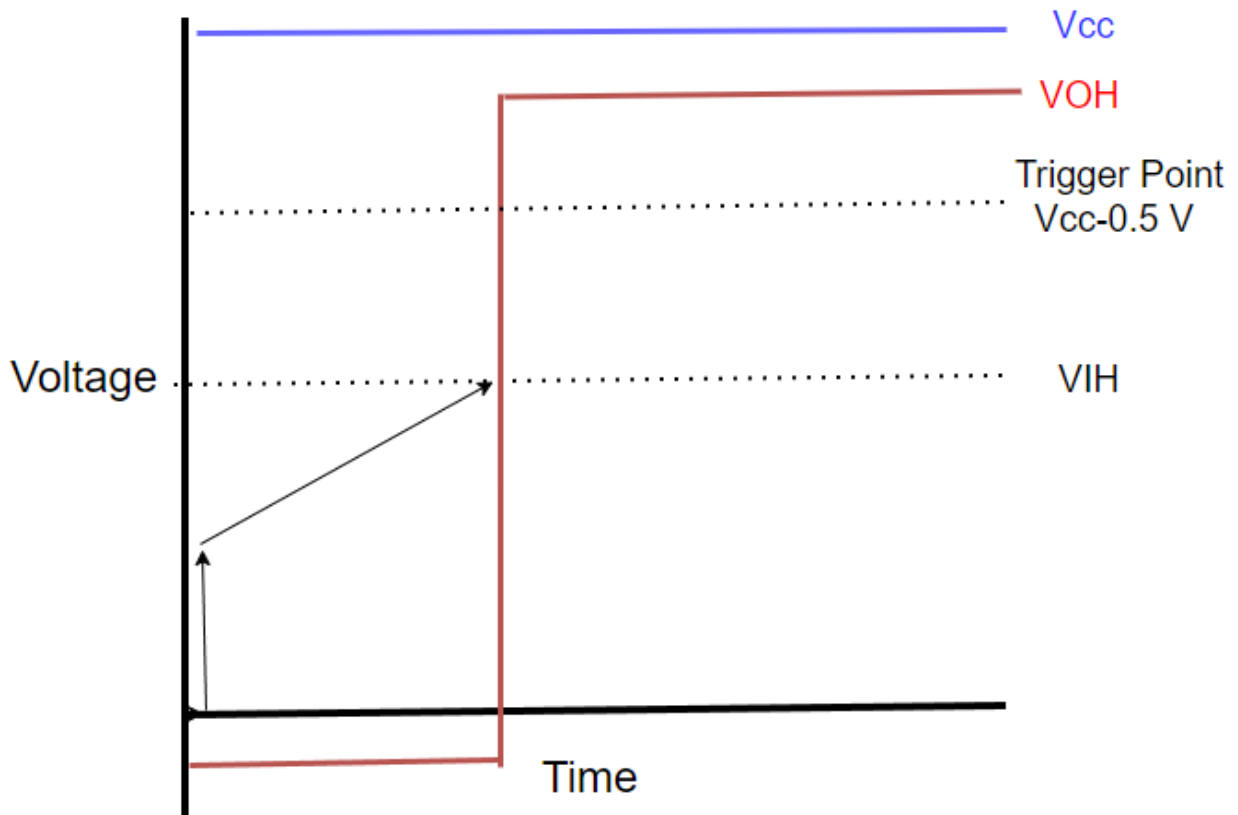
Figure 13. The Expected Output of the Ramp-Up Test

The ramp-down test operates in almost the same way as the ramp-up test. The differences are in the second for loop. The Input pin is set high to make sure the output is high. The voltage on the input pin in the while loop is decreasing, and the trigger value is set to right above ground rather than right below Vcc. These differences can be seen in Figure 14. The input pin voltage is originally set to Vcc to ensure that the output pin voltage is high, then dropped down to the point when it is stepped down until the output pin voltage passes the trigger point. The power consumption and VIL and VOL values are taken at that point. The same process occurs for both 2 volts and 3 volts Vcc and for both the ramp-up and ramp-down tests, equalling the first four tests that were created.
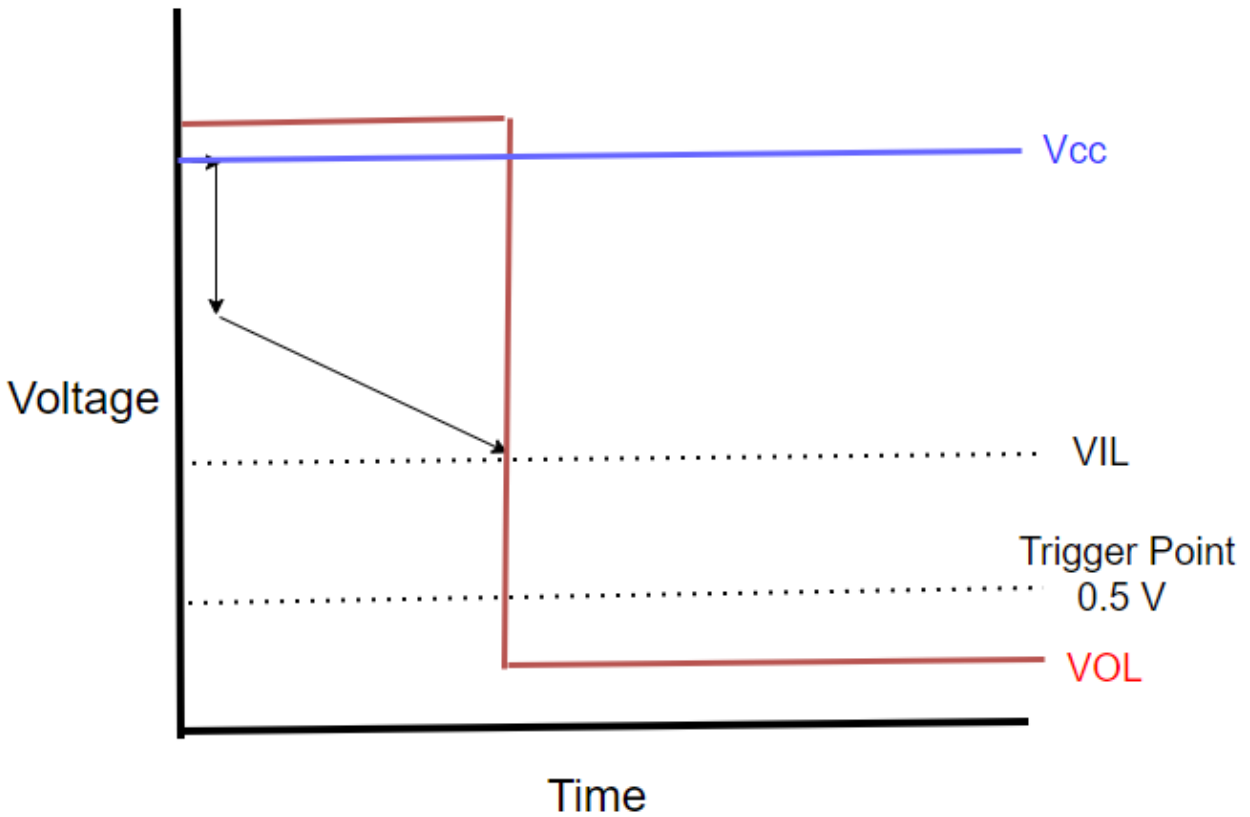
Figure 14. The Expected Output of the Ramp-Down Test

The Vcc ramp test combines the ramp-up and ramp-down test by having both while loops inside a third for a loop that controls the voltage being applied to the power pin. Also, during this test, a new CSV file is created for the chip that is being tested rather than the entire test, as the file size is too large to open when all 10 sites are in the same file. This test originally output the power consumption, VOL, VOH, VIH, and VIL values the same as the 4 other tests; however, it was modified to output all six values(two power consumption values - one for ramp up and one for ramp down) on the same line in the CSV file so that a single copy and paste could be done when cleaning the data than six separate copy and paste segments. The Vcc ramp test increases the voltage on the power pin in steps of 0.05 volts between the two Vcc values that were tested in the first round of the 2 and 3 volts to characterize the output characteristics as Vcc changed. The

starting voltage for the input pin is raised at the same rate as the Vcc voltage to decrease the number of loops that were needed to be completed.

The Mass Test is a variation of the Vcc ramp without changing the Vcc level. This means it still contains both during loops, so low and high can be tested simultaneously. The Mass test was given its own test number variable as rather than running 2 test runs like with the Vcc ramp test, 50 tests were performed one after another. Due to this large amount of tests, the ramp level was decreased to 1 millivolt steps rather than the 0.1 millivolt steps used for the Ramp up, Ramp down, and Vcc ramp tests. Each Test run also created its own CSV file rather than each site in the Vcc ramp test. The Vcc voltage during this test was a constant of 3 volts. The final two tests were implemented much later in the process to replace the 4 different ramp-up and ramp-down tests. The tests were mass tests with a different test number variable and the original step size of 0.1 millivolts. The first of these tests had the Vcc set to 2 volts, and the second set the Vcc to 3 volts. These tests were implemented to make the data cleaning process faster with all 6 values in the same line in the CSV file, which was not the case in the original 4 tests.

6.3 Design of Experiment (DOE) Analysis

DOE, or Design of Experiment analysis, is the primary way this project determines which of the tested factors is statistically significant on the output. It works by taking a group of factors and levels to create a table that contains all of the different combinations that are possible. This is to determine which of the factors is causing the variation in the output. "Experimental design can be used at the point of greatest leverage to reduce design costs by speeding up the design process, reducing late engineering design changes, and reducing product material and labor complexity."[16]. For this experiment, the two levels we are testing are min and max, so -1 and 1 on the DOE table, and the four factors that are being considered are Temperature, Humidity,

Vcc, and Age. With two levels and four factors being considered, this means that 16 different input combinations need to be tested to complete the full DOE analysis. The exact values that were used for the level will be discussed in detail in the next section. The results of the DOE analysis should be a clear picture of the factors that most influence the performance of the MSP430.

6.4 Original Chip Data Collection

The collection process was broken down into two different sets of data; the original data set used chips 0 through 9, which a previous researcher first used to collect data for when they were new. These chips were eventually aged to 10 and 20 years with the same tests as before. The tests that were run on the original chips were the ramp-up and ramp-down tests at 2 and 3 volts Vcc and the Vcc ramp test for all three ages. The 4 ramp-up and down tests were run at 4 different environmental conditions to fill out the DOE table. These were ambient, which was 22 degree Celsius and 45% humidity; High Temperature, which was 80 degrees Celsius and 10% humidity; High Humidity which was 22 degrees Celsius and 90% Humidity; and finally, high temperature and humidity, which was 70 degrees Celsius and 50% Humidity. These conditions were maintained to a range of plus or minus 2 degrees Celsius and 5% humidity. The range was significantly higher than anticipated for this round of tests due to a large number of leaks within the old environmental chamber in which the new and 10 years testing was completed. Due to its improved seal, the new Chamber dropped this range down to 1 degree Celsius and 3% Humidity. If you know anything about DOE analysis, you may have noticed the giant mistake made with the tested temperature and humidity levels. The mistake is that the humidity for the high-temperature test is supposed to be the same as the humidity for the Ambient test. The temperatures for the high temperature and high temperature plus humidity tests are supposed to

be the same, and the humidity for the high humidity and high temperature and humidity test are supposed to be the same. This was not noticed until after the completion of the DOE performed for the chips at 20 years old and led to the creation of updated data collection, which will be discussed later. The Vcc ramp test was run under conditions that were supposed to be the midpoints of the DOE analysis temperature and humidity value, which were 46 degrees Celsius and 30% humidity. Still, as discussed previously, these were not the midpoints of the temperature and Humidity values.

The mass test was introduced when the chips were 10 years old and ran at a constant voltage of 3 volts Vcc and at ambient temperature and humidity. At the 10-year mark, 4 of the 10 chips that were tested and provided by previous research tragically passed away. Chip 3 was fried by user error when testing on a bench setup to ensure the testing program was working properly when 5 volts were applied to the chip's power pin, thus causing an internal short on the chip. Chips 1 and 8 no longer worked after testing at high humidity when they stopped giving the expected responses and were attached to the bench setup where they were confirmed to have an internal short. The day after the high humidity test, chip 2 was not giving the expected results and was also confirmed to have an internal short on the bench equipment. The internal shorts were confirmed by looking at the ammeter associated with the power supply in which the chip was pulling over 400 milliamps, which is way beyond their operation limit. The suspected culprit is water getting into the socket of the MSP430s and causing the short, thus over-currenting the MSP430 and burning them up.

6.5 Updated Chip Data Collection

The second data set was collected in response to the incorrectly performed DOE analysis of the original chips. Of the Six remaining chips that made it to 20 years old (0, 4,5,6,7, and 9),

five would be repurposed in roles as the aged chips factor in the DOE analysis, and 5 new chips were taken from the same batch of MSP430. These new chips would be numbered 0b-4b, while the original chip 0 was discarded and chip 4 was renumbered 8b, chip 5 as 5b, 6 as 6b, 7 as 7b, and 9 and 9b. These "B" chips would undergo the same tests as the original chips, which will be referred to as the "A" Chips from here on out. It was determined that this is an appropriate course of action because previous research in this project determined that chip-to-chip variation has no statistical significance. Once again, the four different combinations of environmental conditions needed to be tested, but with the New environmental chamber being better pressurized, a high temperature and humidity could be tested. For the condition of Temperature and Humidity, low 30 degrees Celsius and 36% Humidity were selected. This was because a larger variation of humidity was desired, so the temperature was increased to lower the humidity. For high temperatures, 70 degrees Celsius and 36% Humidity were tested. For high Humidity, 30 degrees Celsius and 60% Humidity were tested. Finally, for high temperature and humidity, 70 degrees Celsius and 60% humidity were tested as this was the highest temperature and humidity that was able to be maintained by the environmental chamber. For these tests, the Chips were also allowed to soak in the conditions an hour before the tests were run. During the "A" run, the chips were tested when the environmental chamber reached the desired condition. Soaking the chips is necessary to ensure that the chip is at the desired temperature and humidity, which takes time to achieve. The mass and Vcc ramp tests that were run for the "B" runs were both run at ambient conditions of 22 degrees C and 45 % humidity to reduce the amount of time required for testing. During all the tests, a temperature range of plus or minus 1 degree Celsius and a humidity range of plus or minus 3% humidity was maintained. The humidity range was so large because, during the high humidity conditions running the humidifier for a short time, the internal

humidity of the chamber increased by 3-4%. The Aged and New chips were grouped based on their location inside of the environmental chamber, with those being the closest to each other being grouped. This means that Chip 0b and 5b are grouped where 0b is the new chip and 5b is the chip at 20 years old. The rest of the groups were as follows 1b-6b, 2b-7b, 3b-8b, and 4b-9b.

6.6 Anomalies During the Testing Process

One of the biggest issues encountered during the testing process was the output voltage needing to completely reach its Low or High state by the time the next input voltage was triggered. Thus causing a discount between the input voltage and output voltage. An example of this is shown in Table 3 when the recorded input voltage is incorrect by a single step on both the ramp-up and ramp-down tests. This issue persists throughout much of the data collected and is unaccounted for. This issue could be solved by slowing down the rate at which the output voltage is being measured to allow it enough time to go completely low or high based on the test being run.

Table 3. Output Not Lining up with Input Trigger

Output not lining up with Input Trigger						
Ramp Down Trigger Issues				Ramp Up Trigger Issues		
Input Voltage	Output Voltage	PC (mW)		Input Voltage	Output Voltage	PC (mW)
1.2526	3.22226	-13.5569		1.8396	-0.343509	1.47683
1.2525	3.22228	-13.5591		1.8397	-0.343531	1.48123
1.2524	3.22227	-13.5623		1.8398	-0.343469	1.48646
1.2523	3.22225	-13.5627		1.8399	-0.343513	1.48469
1.2522	3.22223	-13.5617		1.84	-0.343612	1.47655
1.2521	3.22227	-13.561		1.8401	-0.343547	1.48001
1.252	3.22227	-13.5584		1.8402	-0.343578	1.47665
1.2519	3.22229	-13.5607		1.8403	-0.343484	1.4844
1.2518	3.22222	-13.5623		1.8404	-0.343553	1.46403
1.2517	3.22226	-13.5637		1.8405	-0.343484	1.47487
1.2516	0.927394	1.06291		1.8406	1.17349	16.2277
1.2515	0.24847	1.04795		1.8407	2.51845	16.2172
Expected VIL	1.2516			Expected VIH	1.8406	
Actual VIL	1.2515			Actual VIH	1.8407	

Another issue that appeared often was the outputs were being triggered seemingly randomly. This caused many hours of retests to be performed, resulting in increased test time. While some of these triggers were truly random, a trend was discovered where whenever the heater was initially powered on, it would cause the output to be triggered. The original theory was that the heater produced an electromagnetic pulse when turned on. However, the same effect was able to be reproduced by the vacuum cleaner on the same circuit as the heater. The current theory is that the large amount of inrush current that these items use causes the AC voltage to drop to the tester, thus causing enough noise to trigger the outputs. An inductor was attached to the heater's cord, but it did not cause the accidental triggering to stop.

7.1 "A" Chips Data Over Time

Due to the "A" chips not being able to have the DOE analysis performed on them as originally intended. Table 4 was created to observe the effects of aging chips across the 4 conditions tested. Tables for chips 4,5,6,7 and 9 can be found in the appendix. The most notable trend is that as the chips increase in Age, VIL decreases while VIH increases. The other outputs do not seem to have a clear trend. This trend is seen in all of the environmental conditions and for both Vcc levels. As they age, this is an expected trend of chips, where their trigger point becomes less precise. What is not observed is the increase in Power Consumption that is expected. While this seems to occur in some conditions, it is not as clear of a trend as shown with both VIL and VIH.

Table 4. Chip 0 Parameters at Different Ages and Conditions.

Chip 0 Parameters Over Time Under Different Environmental Conditions													
Ambient 2V Vcc - 22 Degrees C 45% Humidity							Ambient 3V Vcc - 22 Degrees C 45% Humidity						
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.804675	1.282	0.212777	1.777463	0.60849975	6.6429275	0	1.3111	1.7862	0.254553	2.749083	1.089825	16.19435
10	0.79595	1.289425	0.265713	1.696595	0.59845325	6.6406475	10	1.284925	1.8001	0.34888	2.642468	1.1846675	16.343175
20	0.74185	1.316225	0.18727	1.776635	0.5907865	6.5985575	20	1.2379	1.8399	0.228886	2.74787	1.22059	16.261025
High Humid 2V Vcc - 22 Degrees C 90% Humidity							High Humid 3V Vcc - 22 Degrees C 90% Humidity						
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.8088	1.296175	0.219289	1.777373	0.61584275	6.7767025	0	1.29785	1.8103	0.264199	2.750038	2.727725	16.183825
10	0.75525	1.3104	0.346078	1.658843	1.50545	7.4883925	10	1.25925	1.8354	0.447741	2.596115	5.7875925	23.9217
20	0.741075	1.3169	0.183092	1.778395	0.66977625	6.6179675	20	1.235925	1.840575	0.224575	2.748868	2.3321475	17.044275
High Temp 2V Vcc - 80 Degrees C 10% humidity							High Temp 3V Vcc - 80 Degrees C 10% humidity						
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.889	1.29065	0.221756	1.770438	0.63007675	6.6493975	0	1.30765	1.806675	0.263085	2.742953	1.201025	16.36815
10	0.81585	1.2783	0.344343	1.715905	0.62809225	6.684955	10	1.30725	1.7955	0.338233	2.651805	1.35731	16.474175
20	0.74825	1.3159	0.18707	1.771628	0.804668	6.9010825	20	1.241975	1.843	0.22853	2.709683	3.7341075	20.2296
High Humid and Temp 2V Vcc - 70 Degrees C 50% Humidity							High Humid and Temp 3V Vcc - 70 Degrees C 50% Humidity						
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.79375	1.29865	0.270089	1.740825	1.0305525	7.5845925	0	1.294225	1.83615	0.312164	2.675575	3.0186875	27.71815
10	0.790125	1.283325	0.301746	1.68142	4.1223575	9.876015	10	1.268025	1.82395	0.34752	2.627475	9.77052	26.140225
20	0.740275	1.32155	0.186757	1.773833	1.01513625	7.23425	20	1.24225	1.848625	0.297006	2.737055	4.04132	19.202125

7.2 "A" Chips Vcc Ramp Over Time

The same trends seen in Table X are reiterated with the Vcc Ramp test Performed for the "A" Chips. These trends can be seen in Figures 15 and 16, which show chip 7's performance characteristics. However, in these tests, it is especially noticeable in chips 7 and 9 that it's not

just the Inputs that change but the output and Power Consumption change as well. The strange part is that both Power consumption values decrease as the chip gets older, which is the opposite of the expected trend for a semiconductor chip as it ages. Similarly, the high output voltage increases, and the low output decreases as the chip ages. This follows the trend set by the power consumption numbers that the chip performs better as it ages. This trend is most notable in the Chip 7 graphs but can also be seen in Chips 0, 4, 5,6, and 9, which are located in the appendix. These chips do have a significant amount of noise associated with them, so the trends are harder to see.
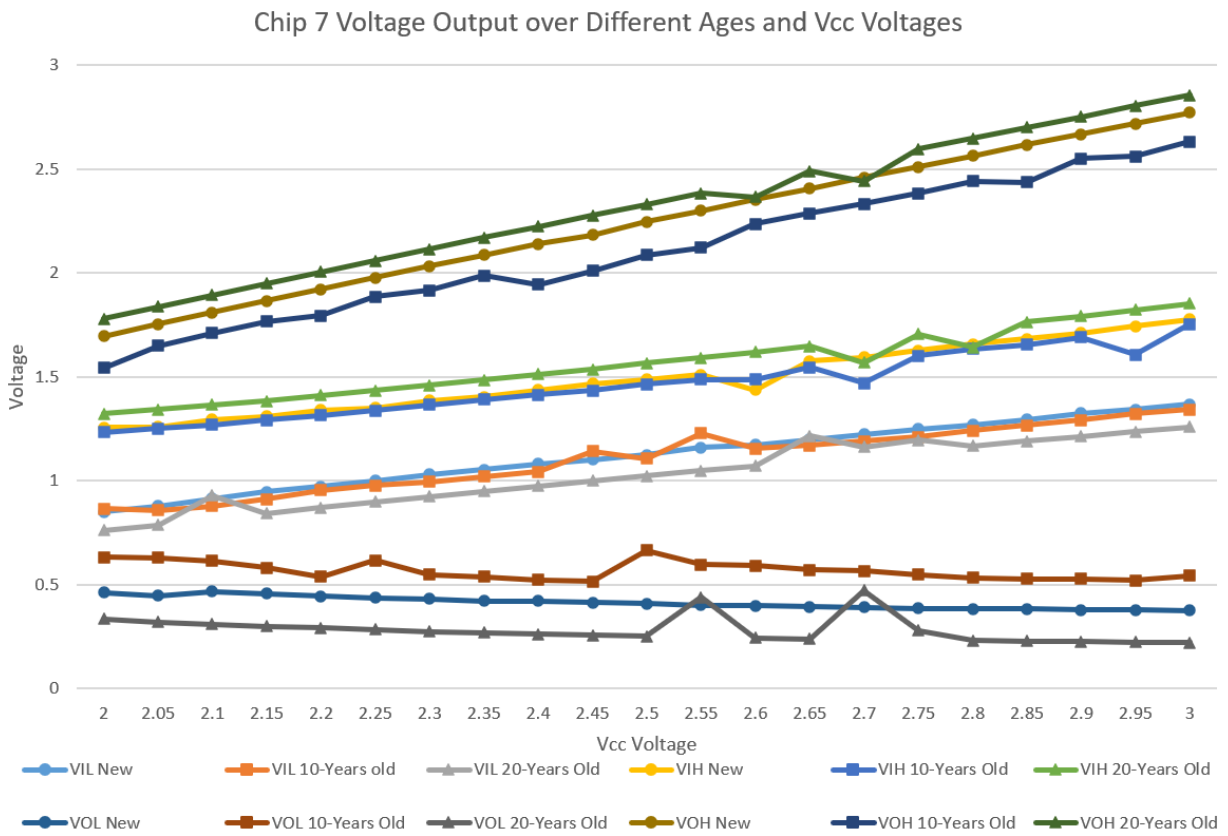
Figure 15. Chip 7 Voltage Values Over Time with Increasing Vcc Levels
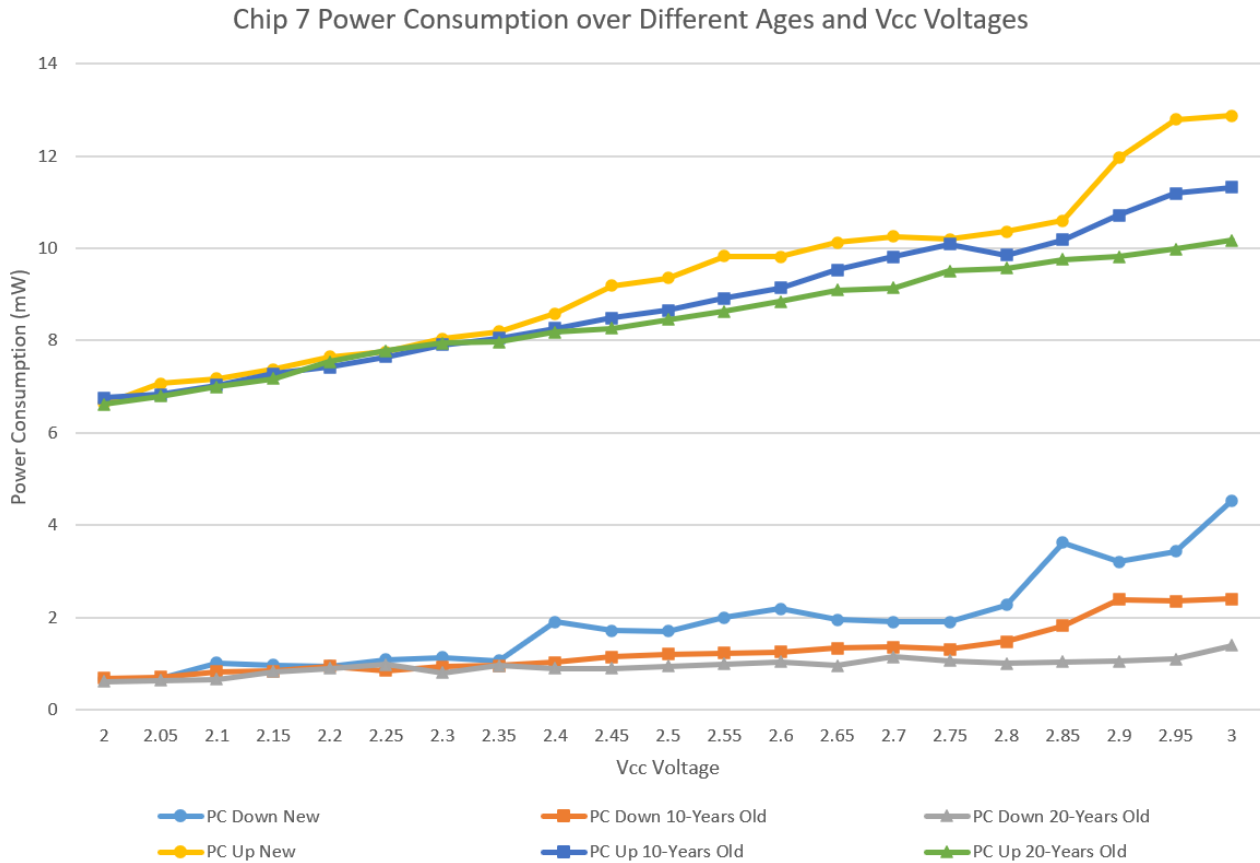
Figure 16. Chip 7 Power Consumption Values Over Time with Increasing Vcc Levels

7.3 "A" Chips Variation Over Time

The mass test was created to see each chip's variation between test runs through a large sample size. The original sample size was 50; however, the first run of every mass test produced statistical outliers that were removed. The best way to easily view this variation is through a box plot. The box plot shows the range of which a dataset is within. 50% of the data is within the area of the box, with the line in the middle showing the median point of the data. The whiskers show the range at which the rest of the data is located in up to 1.5 times the Interquartile range, which is essentially the box's width. Any outliers beyond the whiskers are shown as Dots. Figure 17 shows the data collected from the mass test of the "A" chips at both 10 and 20 years. The variability of the chip's power consumption seems to increase as the chip ages. The number of

40

outliers that occur for VIL, VIH, VOL, and VOH also seems to increase. This either means the chip cannot consistently produce the output voltage or triggers consistently, or it is taking longer for the output to turn low or high, as shown in Chapter 6.6, thus not getting the proper output reading. The Variability for chips 4,5,6,7 and 9 can be found in the appendix.
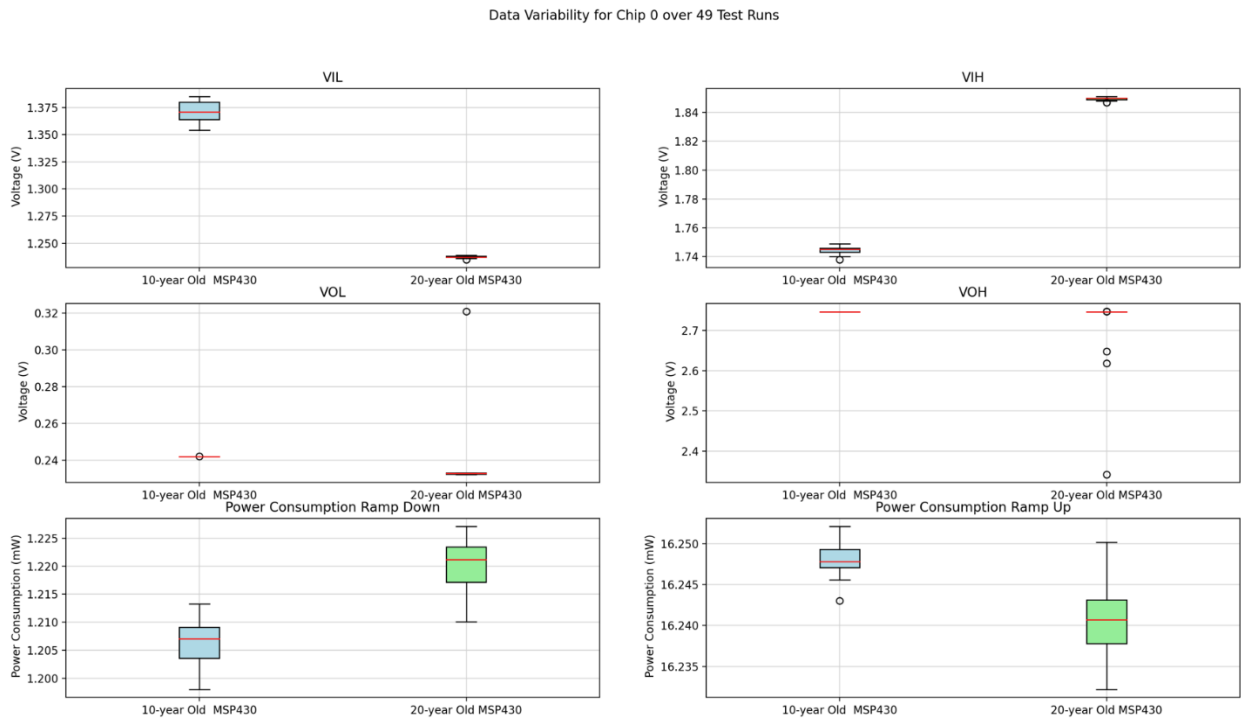
Figure 17. Data Variability of 49 Test Runs of Chip 0

7.4 DOE Analysis of "B" Chips

The DOE analysis will be used to determine which, if any, of the four factors is statistically significant to the performance characteristics of the MSP430. The factors that were considered were temperature, humidity, Vcc, and Age. The DOE table of Chips 0b-5b is shown in Table 5, and the rest are in the appendix. This table was used to produce Praeto charts in the program known as Minitab, which applies the DOE factorial analysis to the table to determine how much each of the inputs and its interactions is affecting each of the outputs. The Praerto Chart of VIL for chips 0b and 5b can be seen in Figure 18. Any interaction or factor that the bar

graph is beyond the red dotted line is considered statistically significant and a leading cause for the change in the observed output. The results for all chips and all outputs are consolidated into Table 6. This table shows that Vcc and its interactions are overwhelmingly the most significant factor in the changes observed across All six outputs. With this being the same conclusion as previous interactions of this research, it was decided to remove Vcc from the equation to see if any other factors are relevant without being covered up by Vcc.

Table 5. DOE Table for Chips 0b and 5b

A	B	C	D	Interactions											Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	VCC	AGE	A*B	A*C	A*D	B*C	B*D	C*D	A*B*C	A*B*D	A*C*D	B*C*D	A*B*C*D	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1.27745	1.845725	0.2521475	2.705828	9.37053	25.188325
1	1	1	-1	1	1	-1	1	-1	-1	1	-1	-1	-1	-1	1.275575	1.85885	0.2769778	2.709865	3.472845	20.66645
1	1	-1	1	1	-1	1	-1	1	-1	-1	1	-1	-1	-1	0.791625	1.3261	0.2296563	1.746323	1.087049	7.16999
1	1	-1	-1	1	-1	-1	-1	-1	1	-1	-1	1	1	1	0.7846	1.29695	0.2524388	1.650368	0.78903225	6.8426375
1	-1	1	1	-1	1	1	-1	-1	1	-1	-1	1	-1	-1	1.265025	1.857075	0.2348125	2.668495	4.1448625	19.856425
1	-1	1	-1	-1	1	-1	-1	1	-1	-1	1	-1	1	1	1.2795	1.861	0.278987	2.720953	2.8845375	19.49675
1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	-1	1	1	0.789775	1.318725	0.2217845	1.62098	1.3675875	7.0922975
1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	-1	-1	-1	0.784325	1.29495	0.2078945	1.759533	1.04606325	7.133325
-1	1	1	1	-1	-1	-1	1	1	1	-1	-1	-1	1	-1	1.254	1.843825	0.2160298	2.735633	2.7431125	18.009525
-1	1	1	-1	-1	-1	1	1	-1	-1	-1	1	1	-1	1	1.2567	1.8567	0.354899	2.735913	1.69595	17.286475
-1	1	-1	1	-1	1	-1	-1	1	-1	1	-1	1	1	-1	0.7648	1.3304	0.2830298	1.76669	0.690298	6.7149425
-1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	-1	1	0.75855	1.30435	0.1919778	1.759923	0.64318125	6.6765825
-1	-1	1	1	1	-1	-1	-1	-1	1	1	1	-1	-1	1	1.264175	1.823975	0.336594	2.63505	1.0620025	16.126875
-1	-1	1	-1	1	-1	1	-1	1	-1	1	-1	1	1	-1	1.26825	1.8583	0.2662608	2.744463	1.065955	16.19185
-1	-1	-1	1	1	1	-1	1	-1	-1	-1	1	1	-1	-1	0.762525	1.32985	0.2032603	1.683895	0.61277375	6.6024675
-1	-1	-1	-1	1	1	1	1	1	1	-1	-1	-1	-1	1	0.7599	1.30005	0.1913333	1.77757	0.61152	6.6424425

Pareto Chart of Chip 0b-5b with all factors
(response is VIL, α = 0.05)

Factor	Name
A	TEMP
B	HUMIDITY
C	VCC
D	AGE

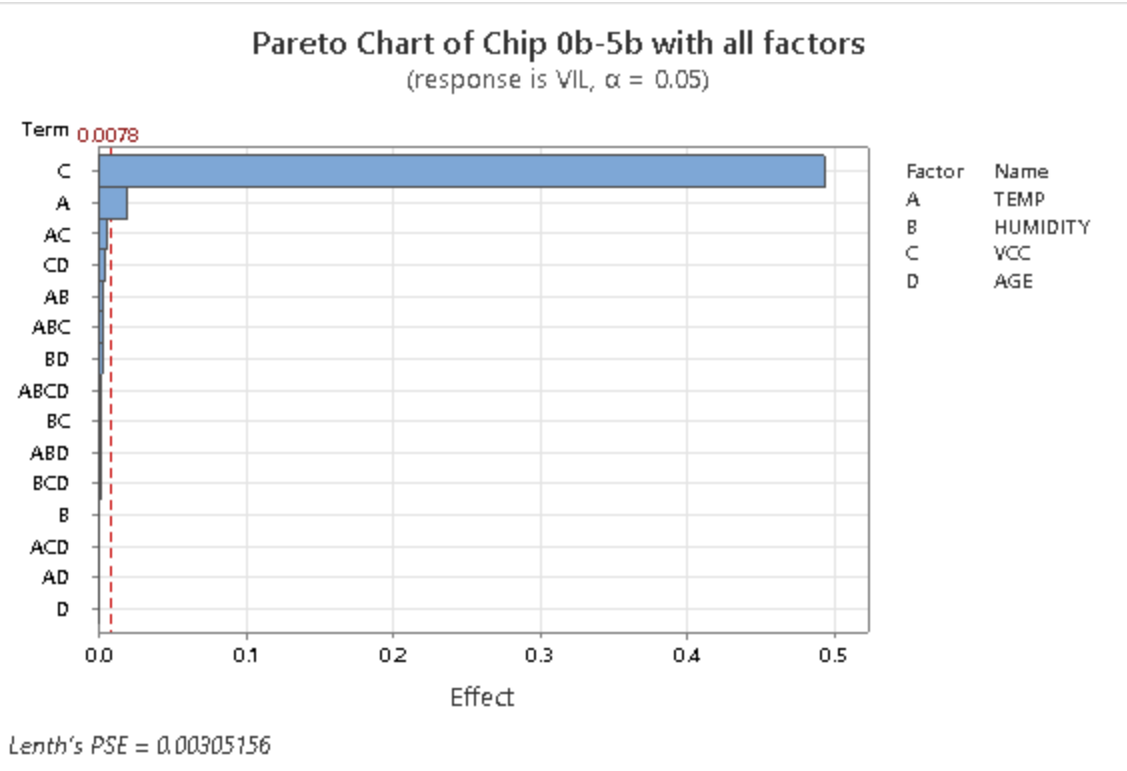Lenth's PSE = 0.00305156

Figure 18. Pareto Chart of Chip 0b-5b for the VIL Response

Table 6. Mapping of Statistical Significance Across All Factors

Chip	0b-5b	1b-6b	2b-7b	3b-8b	4b-9b	
VIL	A, C	A, C, D	A, C, D, AB	A, C	A, C, CD	Statistically Significant
VIH	C, CD	C, D	C, CD, AC	C	A, B, C, AB	Statistically Insignificant
VOL		C, CD		C, CD		A - Temperature
VOH	C	C, CD	C	C	A, C, D	B- Humidity
PC Down				A, C, AC	A, B, C, AB	C - Vcc
PC Up	A, C		C	A, C, AC	A, B, C, AB	D - Age

With Vcc being removed, it created two more sets of DOE tables that must be tested for each chip. The tables were for 2 volts Vcc, which was the Vcc minus input on the full DOE table, and 3 volts Vcc which was the Vcc plus input on the full DOE table. This produces a whole new set of DOE tables and Pareto Plots, which are located in the Appendix. The results of the DOE analysis at 2 volts Vcc can be seen in Table 7. This shows that temperature has a

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consistent effect on VIL and occasional effects on each of the other outputs. Age is also statistically significant in some of the chip's outputs, but it does not have a consistent significance across all chips for a certain factor like temperature does. Table 8 shows the results of the analysis done at 3 volts Vcc. Once again, the temperature is the most significant factor but is not as consistent as when the Vcc is set to 2 volts.

Table 7. Mapping of Statistical Significance Across all Factors at 2V Vcc

Chip	0b-5b	1b-6b	2b-7b	3b-8b	4b-9b	
VIL	A, C	A	A	A	A, C	Statistically Significant
VIH	C	A, C	A, C			Statistically Insignificant
VOL		C			A	A - Temperature
VOH					A, C, AC	B- Humidity
PC Down					A	C - Age
PC Up		A		A, B, AB		

Table 8. Mapping of Statistical Significance Across all Factors at 3V Vcc

Chip	0b-5b	1b-6b	2b-7b	3b-8b	4b-9b	
VIL			A	A		Statistically Significant
VIH			C		A	Statistically Insignificant
VOL		C				A - Temperature
VOH			B			B- Humidity
PC Down				A	A	C - Age
PC Up				A	A	

7.5 Vcc Ramp Load Comparison

When analyzing the Vcc Ramp test data for the "A" Chip, a strange trend was noticed. The first thing is that the supposed power consumption of ramp-up at 3V during the Vcc test is nowhere near the neighborhood of where it is during the standard ramp-up test. Twelve milliwatts on the Vcc ramp test against 16 milliwatts on the standard ramp-up test. Looking at the code solved the issue. For the Vcc ramp test, the load on the output pins was set to constant

values of 5 milliamps for the ramp-down test and -3 milliamps for the ramp-up test. For the

standard ramp-up test at 3 volts Vcc, the load is set to -5 milliamps. This difference in load

causes the power consumption to be lower when the load is lower. This phenomenon also affects

the VOL and VOH values, where the VOL values decrease as the Vcc gets higher, and the

difference between VOH and Vcc decreases as Vcc increases. This led to the idea of running the

Vcc ramp test with a load value for ramp up and down that is normalized to the Vcc value. This

means that the load started at -3 and 3 milliamps at 2 volts Vcc and increased linearly with Vcc

voltage to end at a load of -5 and 5 milliamps at 3 volts Vcc. The voltage levels and power

consumption results can be seen in Figures 19 and 20, respectively. The change in Load value

does not affect the Input voltage levels and the power consumption of the ramp-down test.

However, that is not the case for the other three outputs tested. The power consumption of the

ramp-up test seems to increase logarithmically now in comparison to the linear nature of the

constant load value. The VOH and VOL value now output value that makes more sense as the

VOL value slightly increases as the Vcc voltage increases and the difference between VOH and

Vcc increases at Vcc increases as well. These results conclude that load should be considered

when performing the DOE analysis as it could be a statistically significant input factor, as the

tester easily controls it. The test results for the other 9 chips can be seen in the appendix, but age
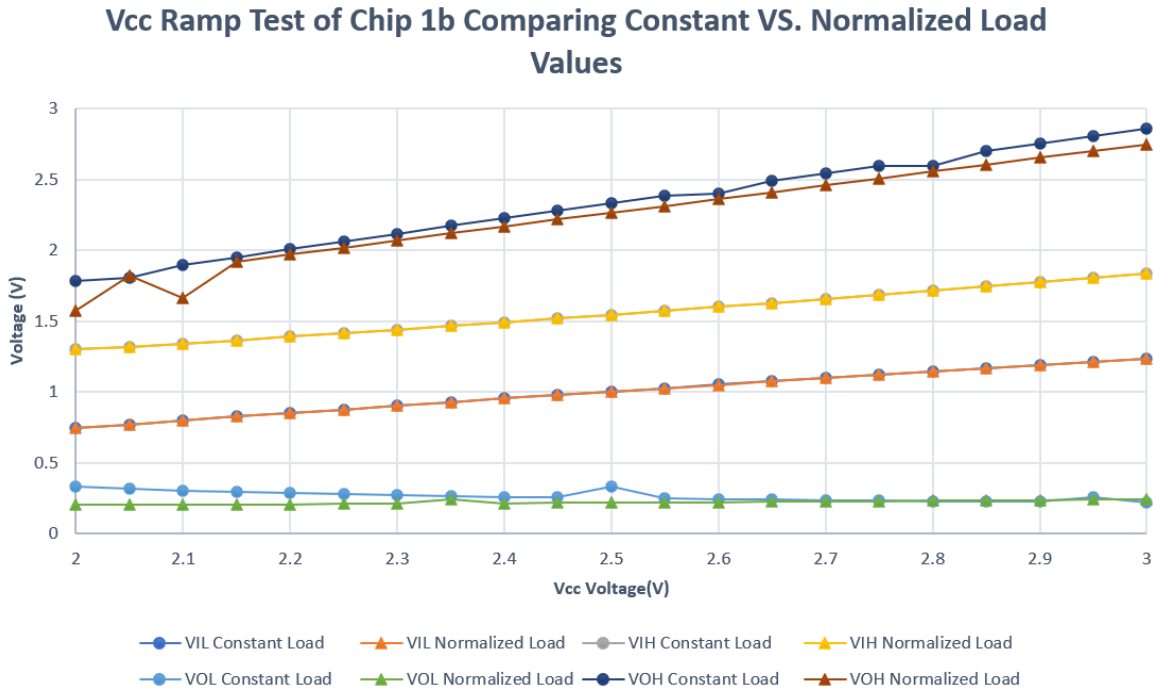
does not play a factor.

Figure 19. Comparison of Normalized to Constant Load as Vcc Increases for Chip 1b –
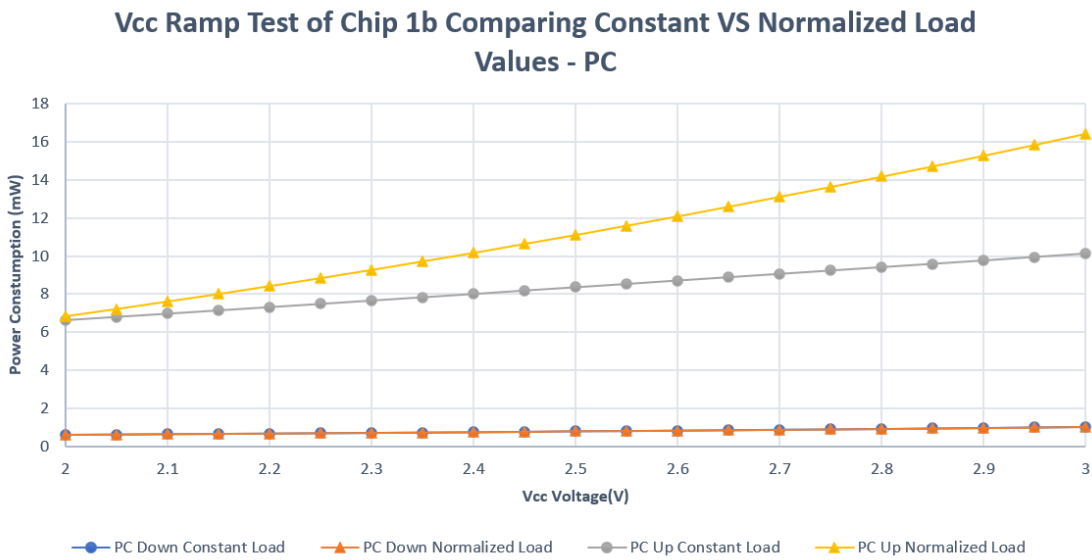
Voltage Levels

Figure 20. Comparison of Normalized to Constant Load as Vcc Increases for Chip 1b –

Power Consumption

7.6 "B" Chips Variation

The last data set that needed to be analyzed was the Mass test from the "B" chips. The box plot from Chip 0b can be seen in Figure 21 and Chip 5b in Figure 22. Overall, the same trend can be concluded as the mass test for the "A" chips; as the chips get older, they experience more variation. However, this variation is within a couple of millivolts for the input and output voltage levels and within 0.01 milliwatts for the power consumption. Hence, it is not noticeable in a statistical sense. The test results for the other 8 chips can be seen in the appendix.
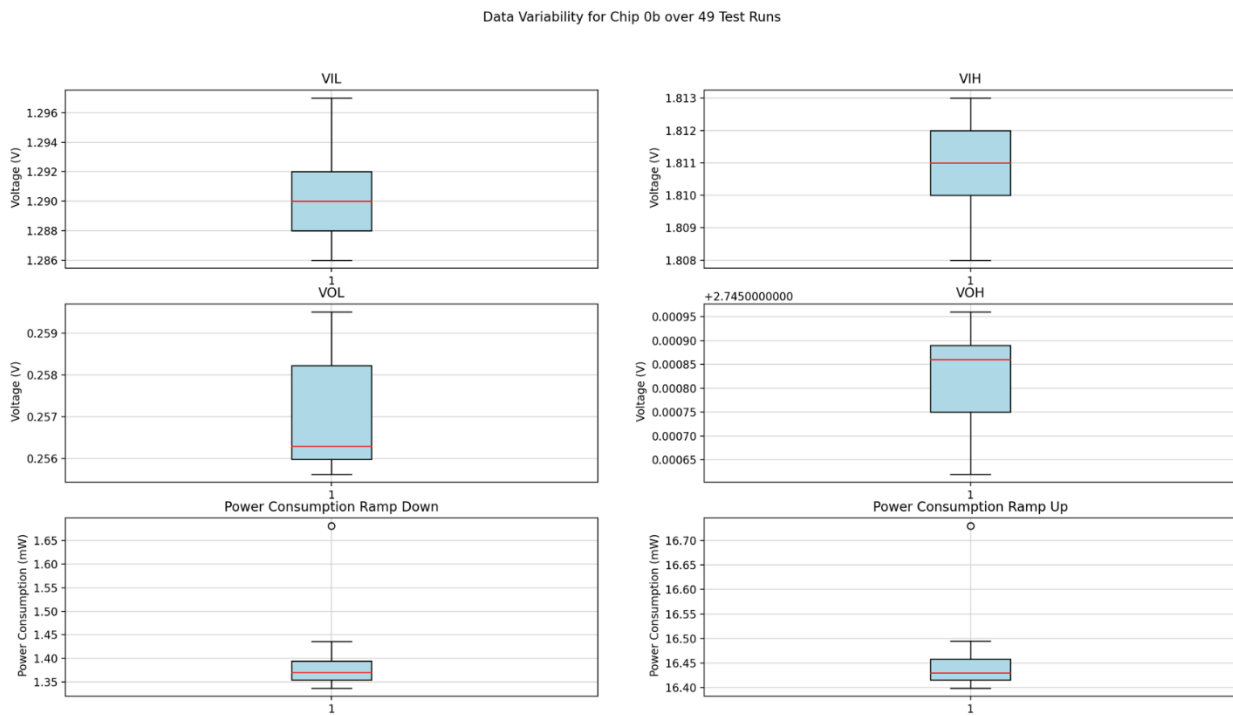

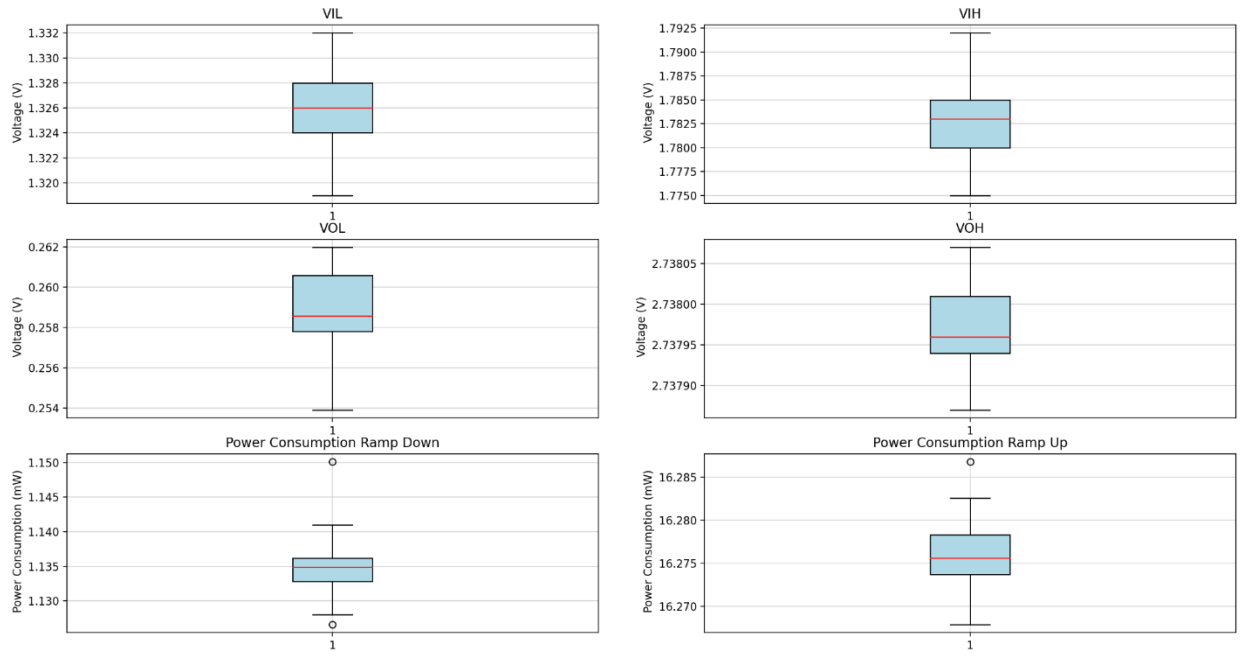**Figure 21. Variability of Outputs on Chip 0b**

Figure 22. Variability of Outputs on Chip 5b

8. DISCUSSION AND CONCLUSION

As proven in previous iterations of this project, Vcc or supply voltage has the greatest effect on the output responses of VIL, VIH, VOL, VOH, and Power Consumption. However, it was also discovered that another factor that was not tested could rival the impact of the responses as much as supply voltage. This factor is the load being applied to the output pins while under test. This value is just as easy to manipulate and does impact Power Consumption as well as VOL and VOH, as shown in the comparison of the constant load against a normalized load value. The second most important factor in the output responses is temperature, which was nowhere near as consistent as the supply voltage. Testing at a higher temperature may lead to a different conclusion. It is commonly known throughout the semiconductor industry that chips switch characteristics change as the chips get hotter and often have separate datasheet lines to account for the temperature difference. Testing at or above 100 degrees Celsius is a good place to start, as the maximum temperature of 70 degrees Celsius is too low to cause any significant changes in the performance characteristics of the MSP430. The third most important factor is Age, which appears in a handful of cases. With the aging of the chips further to 30 years or greater, it is likely that either the chips will have statistically significant changes in performance or outright fail and no longer become operational. Another highly recommended change in the testing method is acquiring two sets of boards. One set of boards would be used to test the chips inside the environmental chamber, while the other set would be used to age the chips. This needs to be done as in the current testing methodology; a single board and socket are used to both test and age the chips. Even though the boards are not fully exposed to the temperature that is experienced at accelerated aging, the socket is and thus could be considered aged. Therefore, the easy solution is to have two sets of boards so that only the chip is being aged. As in previous

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research, the humidity does little to affect the performance characteristics of the MSP430. The only time it ever appears to make any difference is when droplets of water form on the chip and cause a short, thus greatly increasing power consumption or killing the chip outright. It can be eliminated as one of the factors being tested, thus allowing for higher temperatures to be tested during the DOE analysis, as high humidity is holding back the maximum temperature that is capable of being tested in the current test setup. Another way to validate this test method is to acquire some MSP430 that are known to be tampered with and input that as a factor into the DOE analysis to prove that tampered-with chips can be found in a statistically significant manner. Overall, testing with higher temperatures and accounting for the difference in load would greatly improve the results of this research.

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APPENDIX A

ADDITIONAL CHARTS AND TABLES FOR "A" CHIPS

Chip 0 Parameters Over Time Under Different Environmental Conditions

Ambient 2V Vcc - 22 Degrees C 45% Humidity / **Ambient 3V Vcc - 22 Degrees C 45% Humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.804675	1.282	0.212777	1.777463	0.60849975	6.6429275	0	1.3111	1.7862	0.254553	2.749083	1.089825	16.19435
10	0.79595	1.289425	0.265713	1.696595	0.59845325	6.6406475	10	1.284925	1.8001	0.34888	2.642468	1.1846675	16.343175
20	0.74185	1.316225	0.18727	1.776635	0.5907865	6.5985575	20	1.2379	1.8399	0.228886	2.74787	1.22059	16.261025

High Humid 2V Vcc - 22 Degrees C 90% Humidity / **High Humid 3V Vcc - 22 Degrees C 90% Humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.8088	1.296175	0.219289	1.777373	0.61584275	6.7767025	0	1.29785	1.8103	0.264199	2.750038	2.727725	16.183825
10	0.75525	1.3104	0.346078	1.658843	1.50545	7.4883925	10	1.25925	1.8354	0.447741	2.596115	5.7875925	23.9217
20	0.741075	1.3169	0.183092	1.778395	0.66977625	6.6179675	20	1.235925	1.840575	0.224575	2.748868	2.3321475	17.044275

High Temp 2V Vcc - 80 Degrees C 10% humidity / **High Temp 3V Vcc - 80 Degrees C 10% humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.889	1.29065	0.221756	1.770438	0.63007675	6.6493975	0	1.30765	1.806675	0.263085	2.742953	1.201025	16.36815
10	0.81585	1.2783	0.344343	1.715905	0.62809225	6.684955	10	1.30725	1.7955	0.338233	2.651805	1.35731	16.474175
20	0.74825	1.3159	0.18707	1.771628	0.804668	6.9010825	20	1.241975	1.843	0.22853	2.709683	3.7341075	20.2296

High Humid and Temp 2V Vcc - 70 Degrees C 50% Humidity / **High Humid and Temp 3V Vcc - 70 Degrees C 50% Humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.79375	1.29865	0.270089	1.740825	1.0305525	7.5845925	0	1.294225	1.83615	0.312164	2.675575	3.0186875	27.71815
10	0.790125	1.283325	0.301746	1.68142	4.1223575	9.876015	10	1.268025	1.82395	0.34752	2.627475	9.77052	26.140225
20	0.740275	1.32155	0.186757	1.773833	1.01513625	7.23425	20	1.24225	1.848625	0.297006	2.737055	4.04132	19.202125

Chip 4 Parameters Over Time Under Different Environmental Conditions

Ambient 2V Vcc - 22 Degrees C 45% Humidity / **Ambient 3V Vcc - 22 Degrees C 45% Humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.843675	1.25095	0.18508	1.780215	0.6299005	6.611	0	1.36915	1.7611	0.227132	2.750838	1.1229275	16.193
10	0.84785	1.254675	0.174594	1.78334	0.624184	6.622735	10	1.350175	1.77925	0.211145	2.755888	1.285945	16.426675
20	0.843675	1.25095	0.18508	1.780215	0.6299005	6.611	20	1.2502	1.8315	0.28149	2.691088	1.6850025	16.6921375

High Humid 2V Vcc - 22 Degrees C 90% Humidity / **High Humid 3V Vcc - 22 Degrees C 90% Humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.828025	1.25805	0.195805	1.770665	0.65016325	6.781305	0	1.34635	1.78265	0.246436	2.733555	4.53176	17.91135
10	0.80545	1.295625	0.201882	1.77666	3.0642125	13.535275	10	1.319	1.825475	0.266414	2.74853	21.225625	27.25175
20	0.7533	1.302825	0.215948	1.750508	0.740564	6.7500375	20	1.2512	1.8274	0.281654	2.704903	3.2819325	18.382675

High Temp 2V Vcc - 80 Degrees C 10% humidity / **High Temp 3V Vcc - 80 Degrees C 10% humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.84945	1.2281	0.195365	1.775328	0.62940075	6.629435	0	1.3691	1.778975	0.241227	2.744835	1.118965	16.181375
10	0.7988	1.25095	0.247912	1.772978	0.60269725	6.6355425	10	1.3646	1.7822	0.239875	2.744355	1.137425	16.224875
20	0.7643	1.30055	0.205363	1.64287	2.1222125	8.275405	20	1.2594	1.83165	0.872248	2.711423	4.9880775	20.506875

High Humid and Temp 2V Vcc - 70 Degrees C 50% Humidity / **High Humid and Temp 3V Vcc - 70 Degrees C 50% Humidity**

| Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.811475	1.2846	0.261271	1.722895	1.3839125	8.0408775	0	1.305425	1.796525	0.333838	2.664428	4.57276	27.5244
10	0.87015	1.2631	0.23691	1.759003	0.89312	7.037555	10	1.368875	1.7898	0.365083	2.730088	4.2802925	21.876325
20	0.7494	1.3121	0.242831	1.745808	8.9721825	18.08725	20	1.253575	1.83655	0.268166	2.705043	13.56667	28.0676

Chip 5 Parameters Over Time Under Different Environmental Conditions

Ambient 2V Vcc - 22 Degrees C 45% Humidity / **Ambient 3V Vcc - 22 Degrees C 45% Humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.859525	1.266325	0.202773	1.784483	0.61097625	6.5994725	0	1.364625	1.772725	0.250046	2.756383	1.18828	16.260875
10	0.83115	1.2829	0.250629	1.724303	0.5971375	6.59542	10	1.337525	1.79155	0.335201	2.65012	1.2594425	16.344425
20	0.756225	1.325175	0.182093	1.782648	0.597987	6.347705	20	1.257675	1.848275	0.220759	2.75455	1.143205	16.15695

High Humid 2V Vcc - 22 Degrees C 90% Humidity / **High Humid 3V Vcc - 22 Degrees C 90% Humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.8733	1.26785	0.223475	1.784355	0.62934925	6.7746025	0	1.386475	1.75945	0.284517	2.756425	1.5292675	17.1609
10	0.779275	1.3131	0.274714	1.71206	6.56585	12.6168	10	1.283225	1.789	0.283157	2.496345	7.37149	24.993625
20	0.757075	1.322275	0.177268	1.754405	0.705781	6.878625	20	1.25825	1.839675	0.214798	2.748525	3.308755	17.2971

High Temp 2V Vcc - 80 Degrees C 10% humidity / **High Temp 3V Vcc - 80 Degrees C 10% humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.865775	1.26435	0.214406	1.78277	0.60207875	6.624085	0	1.370175	1.77355	0.264445	2.755133	1.1716725	16.360125
10	0.837075	1.270375	0.273529	1.71177	0.59763825	6.634465	10	1.3432	1.786775	0.36534	2.640225	1.2989175	16.440425
20	0.7742	1.3196	0.188346	1.770023	0.6477765	6.6967725	20	1.26915	1.84985	0.22653	2.68261	3.841315	18.433275

High Humid and Temp 2V Vcc - 70 Degrees C 50% Humidity / **High Humid and Temp 3V Vcc - 70 Degrees C 50% Humidity**

Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.81395	1.342425	0.281321	1.727753	1.343915	12.428475	0	1.321525	1.85305	0.374497	2.686268	7.8028325	26.4856
10	0.8275	1.2941	0.272194	1.734403	1.3051675	7.9621	10	1.32105	1.799675	0.371013	2.598418	6.4511575	23.1107
20	0.762975	1.327375	0.187197	1.768473	1.0527525	7.3900625	20	1.2785	1.855525	0.238121	2.732398	5.2699675	21.873325

Chip 6 Parameters Over Time Under Different Environmental Conditions

|	Ambient 2V Vcc - 22 Degrees C 45% Humidity							Ambient 3V Vcc - 22 Degrees C 45% Humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.786725	1.26625	0.19134	1.77851	0.6010735	6.6248025	0	1.286725	1.787375	0.234603	2.748158	1.064525	16.1222
10	0.779675	1.27535	0.21983	1.777333	0.59860225	6.6126625	10	1.2842	1.804825	0.285082	2.745235	1.0623425	16.2302
20	0.734	1.30975	0.192397	1.77675	0.5822185	6.5917275	20	1.232425	1.81335	0.2366	2.747398	1.0983125	16.16505
	High Humid 2V Vcc - 22 Degrees C 90% Humidity							High Humid 3V Vcc - 22 Degrees C 90% Humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.778725	1.281375	0.198084	1.779148	0.60083875	6.65823	0	1.26775	1.815725	0.244883	2.749528	1.3713225	16.6915
10	0.769575	1.30195	0.294532	1.754278	0.80156975	6.95894	10	1.28965	1.829025	0.393033	2.71372	2.790955	19.0419
20	0.72795	1.312525	0.187019	1.674278	0.63585225	6.6187875	20	1.2237	1.843375	0.229187	2.748918	1.28243	16.20345
	High Temp 2V Vcc - 80 Degrees C 10% humidity							High Temp 3V Vcc - 80 Degrees C 10% humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.79055	1.2633	0.208879	1.767115	0.60833125	6.630745	0	1.27235	1.819575	0.254664	2.736203	1.138455	16.1896
10	0.787425	1.253175	0.232256	1.77391	0.6051405	6.6180625	10	1.29105	1.8049	0.293377	2.742968	1.0352425	16.107375
20	0.754575	1.295725	0.196877	1.768355	0.96370125	7.3264375	20	1.251	1.8342	0.243145	2.74014	2.5116575	17.788125
	High Humid and Temp 2V Vcc - 70 Degrees C 50% Humidity							High Humid and Temp 3V Vcc - 70 Degrees C 50% Humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.795575	1.29715	0.216808	1.692518	0.66654975	11.2516	0	1.323575	1.827275	0.261385	2.662875	2.612965	28.993275
10	0.80055	1.287025	0.374967	1.74661	1.063866	7.198275	10	1.263675	1.84265	0.307753	2.722485	4.35214	22.372775
20	0.743425	1.308175	0.199987	1.76393	1.00313525	7.3147325	20	1.2547	1.845575	0.253006	2.725913	7.0023525	23.496775

Chip 7 Parameters Over Time Under Different Environmental Conditions

	Ambient 2V Vcc - 22 Degrees C 45% Humidity							Ambient 3V Vcc - 22 Degrees C 45% Humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.8254	1.205225	0.194013	1.778015	0.6166925	6.634025	0	1.342225	1.77405	0.241319	2.742913	1.7407275	16.7729
10	0.811275	1.2699	0.226053	1.735668	0.6499175	6.6989575	10	1.324425	1.78975	0.314048	2.650985	1.923385	17.2936
20	0.746475	1.318675	0.184249	1.78201	0.6074995	6.6207075	20	1.24765	1.849225	0.226207	2.75229	1.6430925	16.7987
	High Humid 2V Vcc - 22 Degrees C 90% Humidity							High Humid 3V Vcc - 22 Degrees C 90% Humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.848375	1.2906	0.200627	1.777855	0.6387225	6.738095	0	1.313275	1.81175	0.256493	2.74139	2.9266725	17.564675
10	0.7794	1.299325	0.353141	1.65804	0.88724775	7.1917875	10	1.302775	1.83415	0.501153	2.56439	6.33913	24.58105
20	0.748275	1.318925	0.176832	1.784953	0.665511	6.62342	20	1.251375	1.846215	0.215553	2.756935	1.6468075	16.42355
	High Temp 2V Vcc - 80 Degrees C 10% humidity							High Temp 3V Vcc - 80 Degrees C 10% humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.901175	1.15955	0.213538	1.760038	0.7032655	6.72346	0	1.4225	1.702675	0.271972	2.715875	1.869885	17.209425
10	0.844325	1.232375	0.248913	2.893428	0.63722175	6.64547	10	1.345175	1.768025	0.337767	2.586	1.628365	16.720425
20	0.763675	1.312525	0.186166	1.77693	0.62634275	6.649835	20	1.26755	1.84555	0.283253	2.748863	1.780185	17.285775
	High Humid and Temp 2V Vcc - 70 Degrees C 50% Humidity							High Humid and Temp 3V Vcc - 70 Degrees C 50% Humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.787775	1.327	0.315624	1.718238	4.32297	9.8690725	0	1.2019	1.8227	0.350321	2.608063	7.9395725	24.618275
10	0.802075	1.2576	0.335393	1.703023	2.026825	8.275305	10	1.05015	1.831225	0.376506	2.534378	12.64015	25.14955
20	0.752225	1.319425	0.26142	1.779823	1.3182625	7.204645	20	1.263	1.85275	0.232467	2.747343	4.3246925	20.28165

Chip 9 Parameters Over Time Under Different Environmental Conditions

|	Ambient 2V Vcc - 22 Degrees C 45% Humidity							Ambient 3V Vcc - 22 Degrees C 45% Humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.8045	1.2745	0.243235	1.74505	0.61126075	6.6005925	0	1.305925	1.79275	0.320711	2.71164	1.0802225	16.142025
10	0.8231	1.250225	0.202862	1.759828	0.6007925	6.628945	10	1.328375	1.774125	0.255798	2.718738	1.146315	16.394275
20	0.7569	1.298275	0.194665	1.771105	0.58975325	6.59293	20	1.256825	1.82645	0.240787	2.736205	1.199785	16.379325
	High Humid 2V Vcc - 22 Degrees C 90% Humidity							High Humid 3V Vcc - 22 Degrees C 90% Humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.8107	1.272125	0.242174	1.755905	0.61234075	6.7184675	0	1.316325	1.7978	0.319228	2.708505	2.3618275	17.269525
10	0.76845	1.30555	0.246665	1.73407	1.150055	7.242425	10	1.279975	1.835875	0.333486	2.678623	5.271175	23.35605
20	0.743125	1.3107	0.182209	1.77964	0.52181275	6.60431	20	1.238675	1.841675	0.221441	2.749113	1.5761375	16.2442
	High Temp 2V Vcc - 80 Degrees C 10% humidity							High Temp 3V Vcc - 80 Degrees C 10% humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.8434	1.272525	0.26602	1.725903	0.6186465	6.6385075	0	1.308175	1.7703	0.316433	2.707398	1.1530025	16.36925
10	0.83745	1.264975	0.236638	1.732983	0.65052075	6.662635	10	1.33985	1.7842	0.299743	2.67639	1.3233375	16.3662
20	0.895775	1.303925	0.191845	1.7685	0.61303925	6.619125	20	1.25675	1.8419	0.290322	2.73985	1.32283	16.42915
	High Humid and Temp 2V Vcc - 70 Degrees C 50% Humidity							High Humid and Temp 3V Vcc - 70 Degrees C 50% Humidity					
Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)	Age	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
0	0.7213	1.317675	0.265195	1.668638	1.542825	10.3879275	0	1.304825	1.846025	0.348673	2.655145	5.238785	26.8966
10	0.804175	1.294975	0.301404	1.689118	1.5794375	8.0580875	10	1.35345	1.8293	0.423589	2.68417	3.9105425	24.15885
20	0.7484	1.236748	0.187321	1.77528	1.19729	7.38193	20	1.25295	1.843725	0.237529	2.73925	4.78645	20.334275

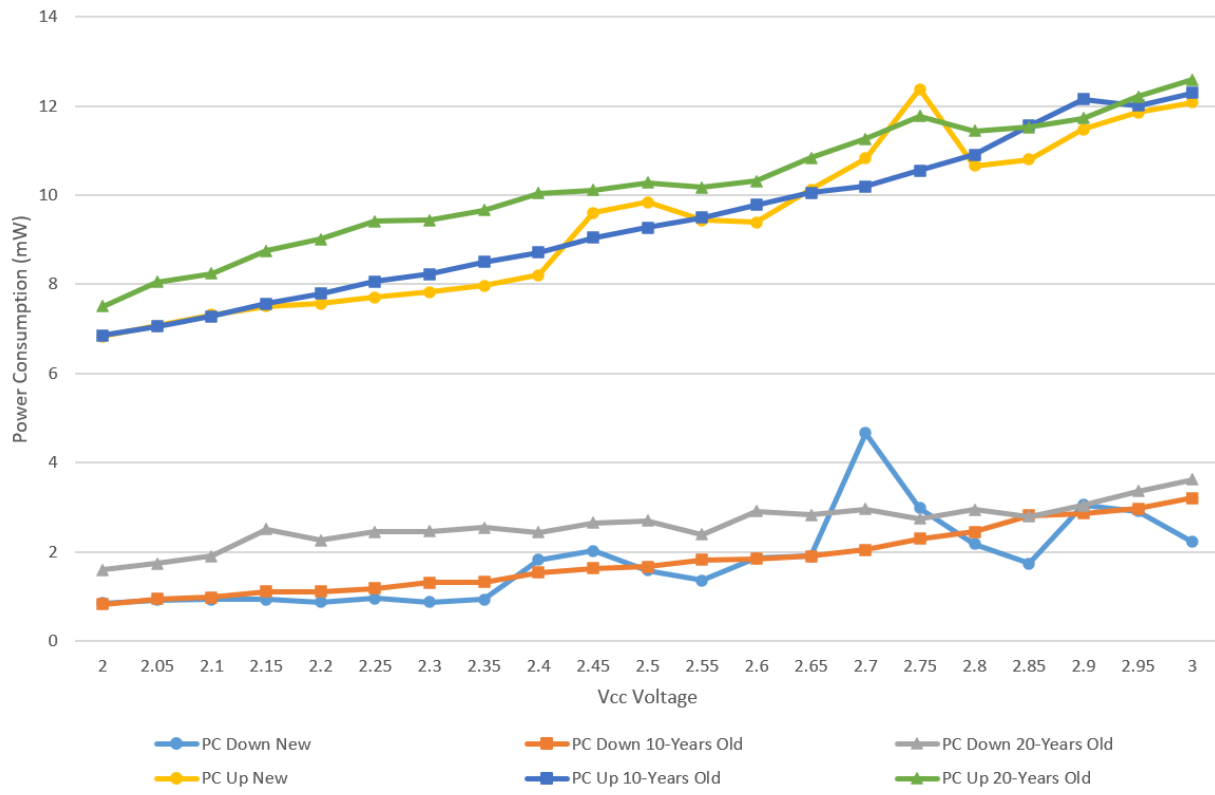Chip 0 Voltage Output over Different Ages and Vcc Voltages
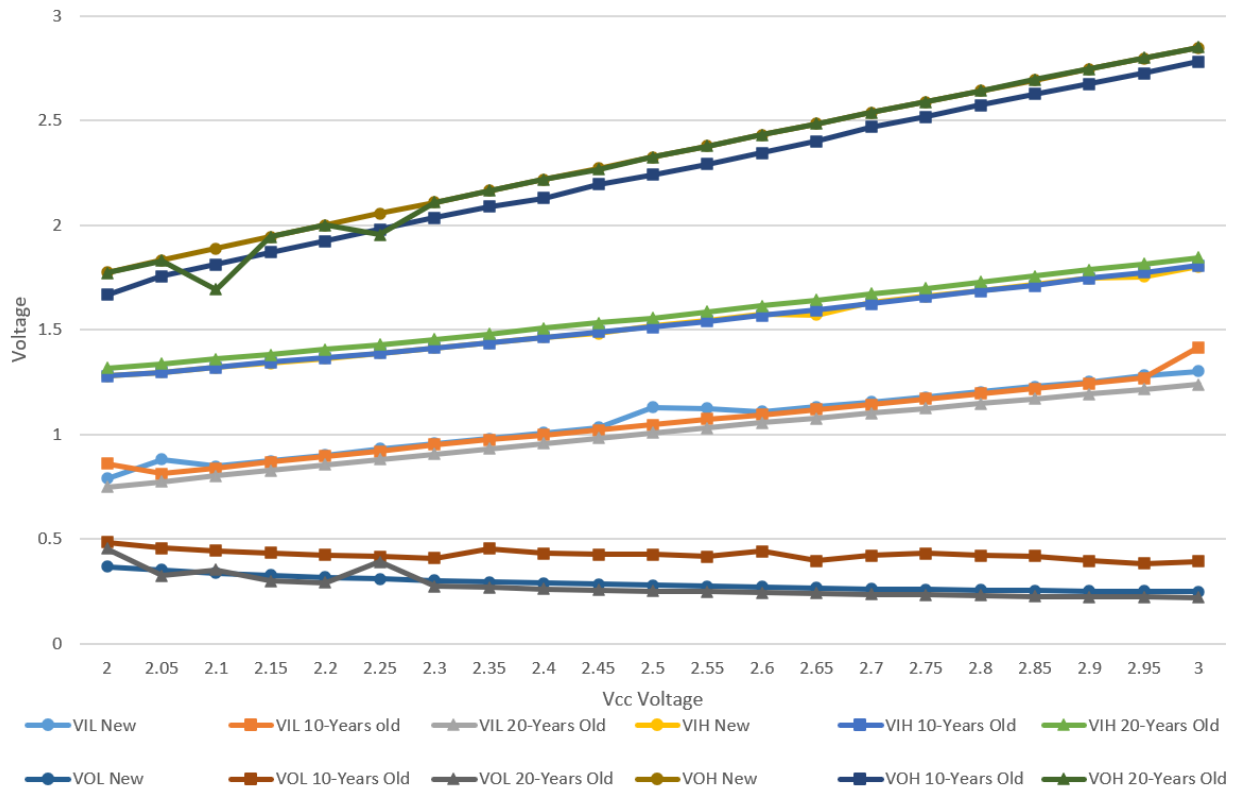
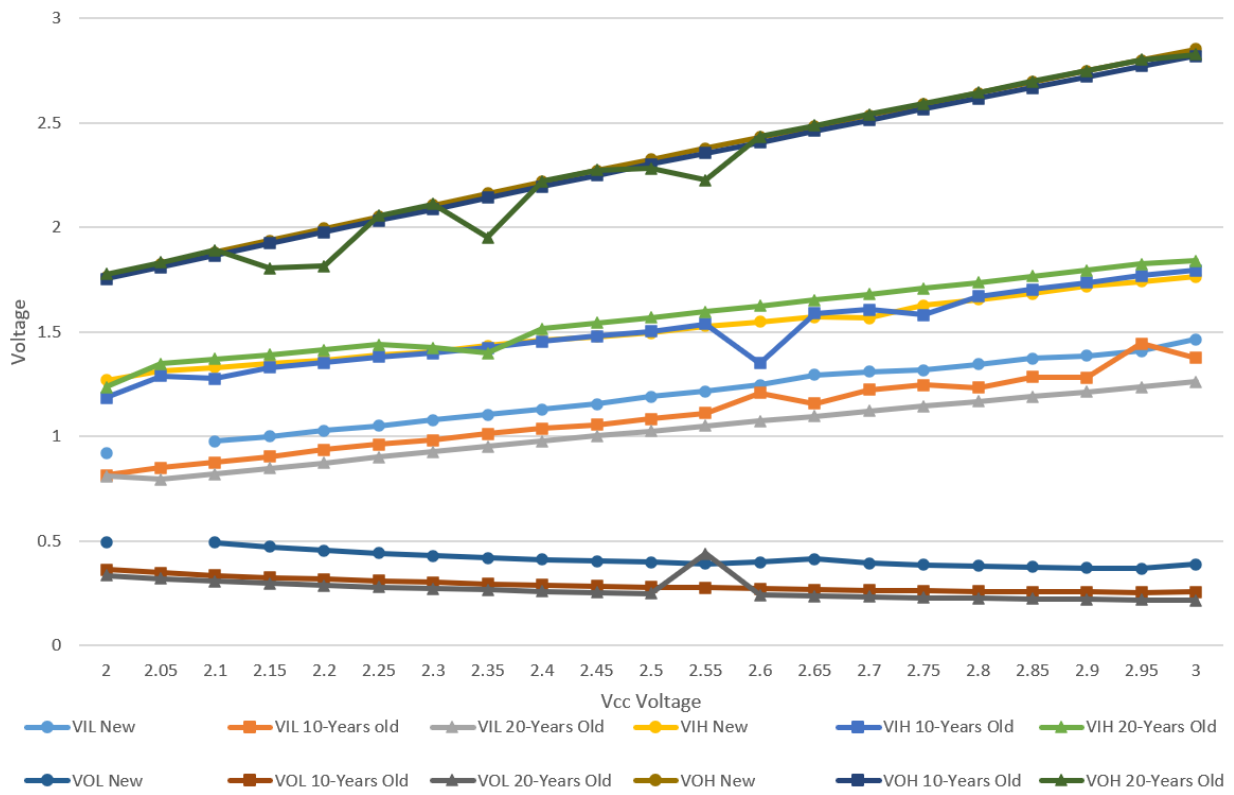Chip 0 Power Consumption over Different Ages and Vcc Voltages
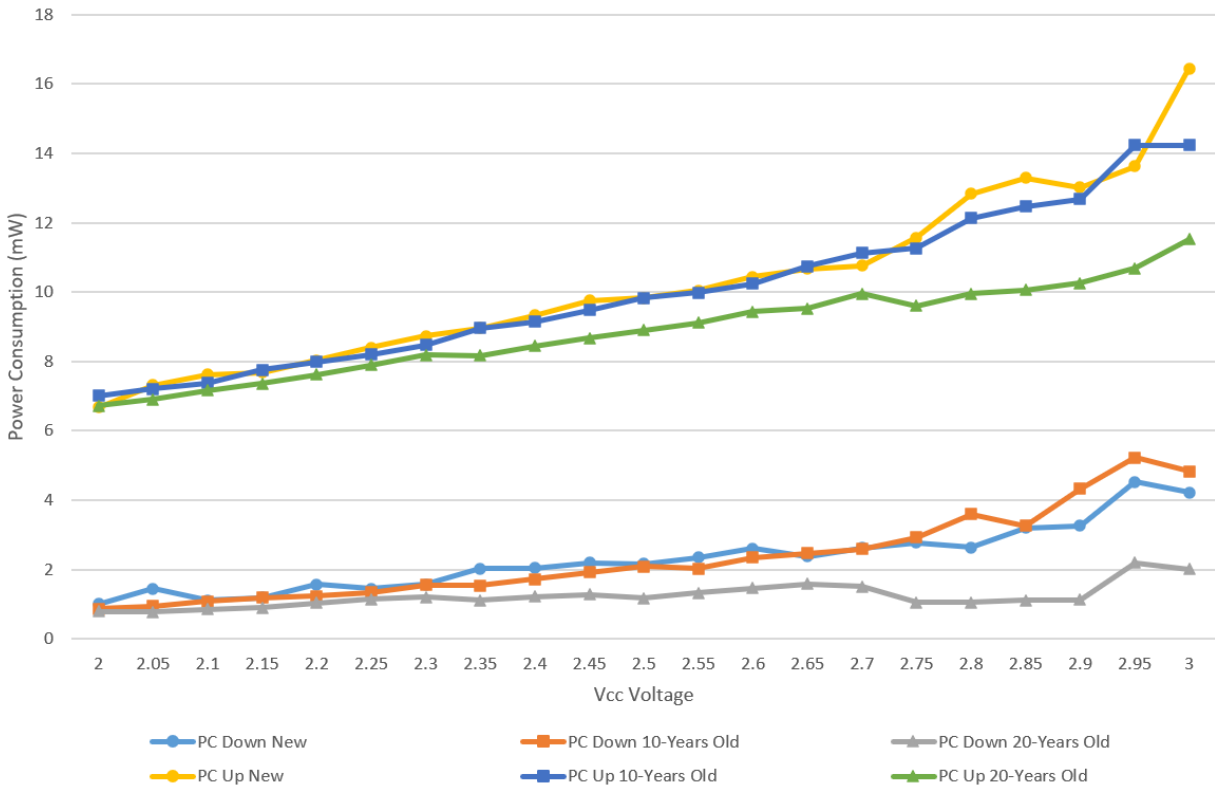
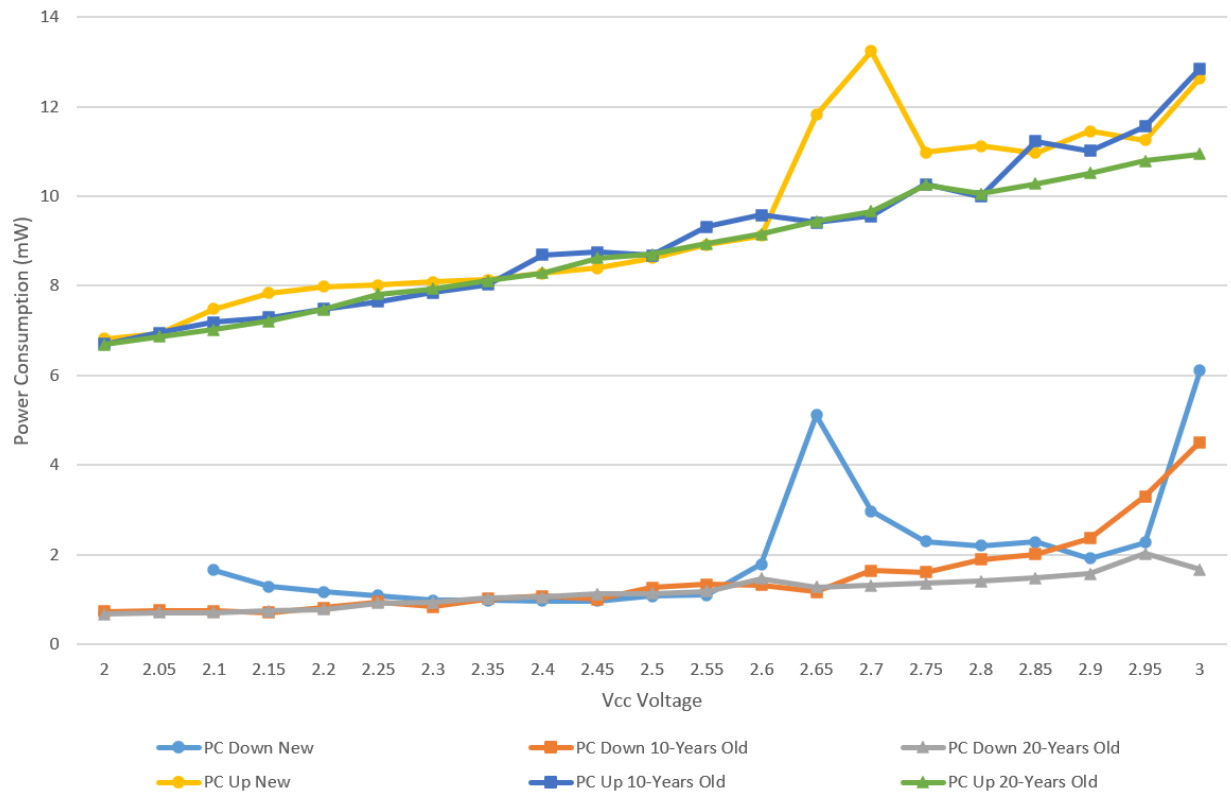Chip 4 Voltage Output over Different Ages and Vcc Voltages
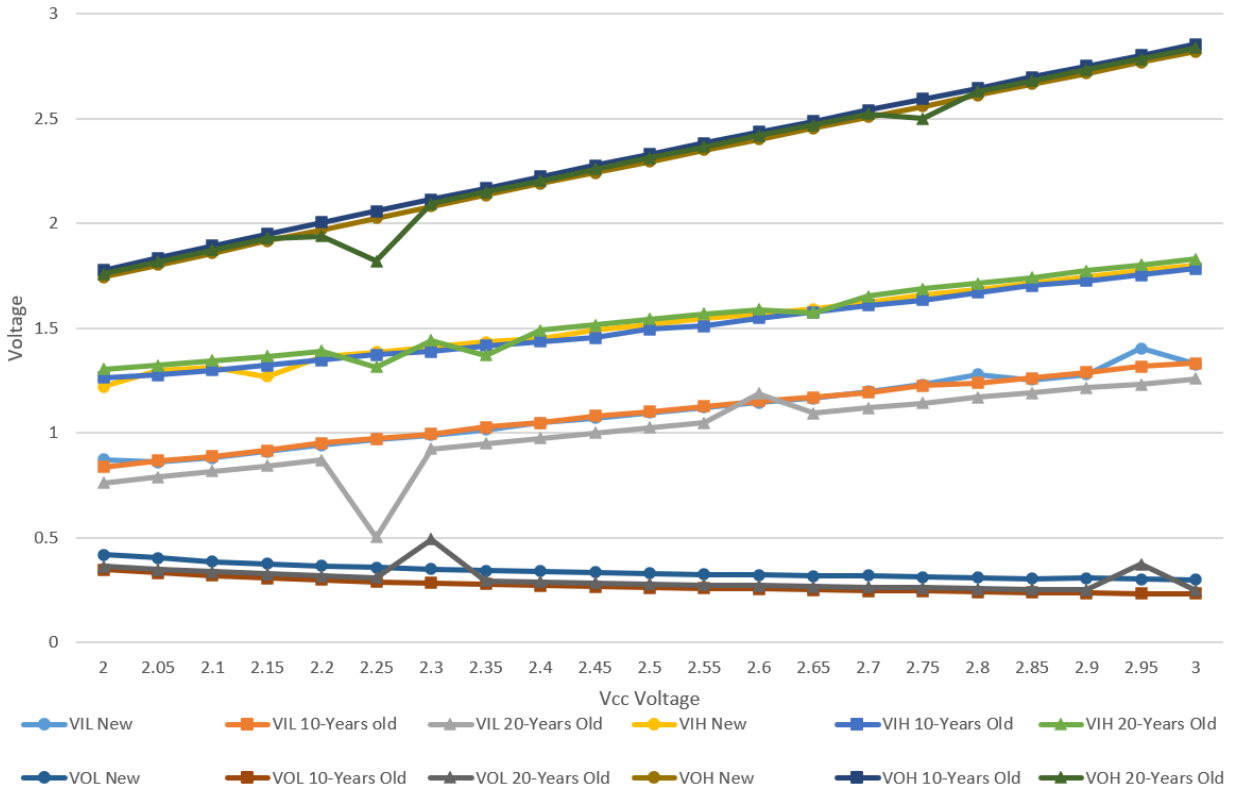
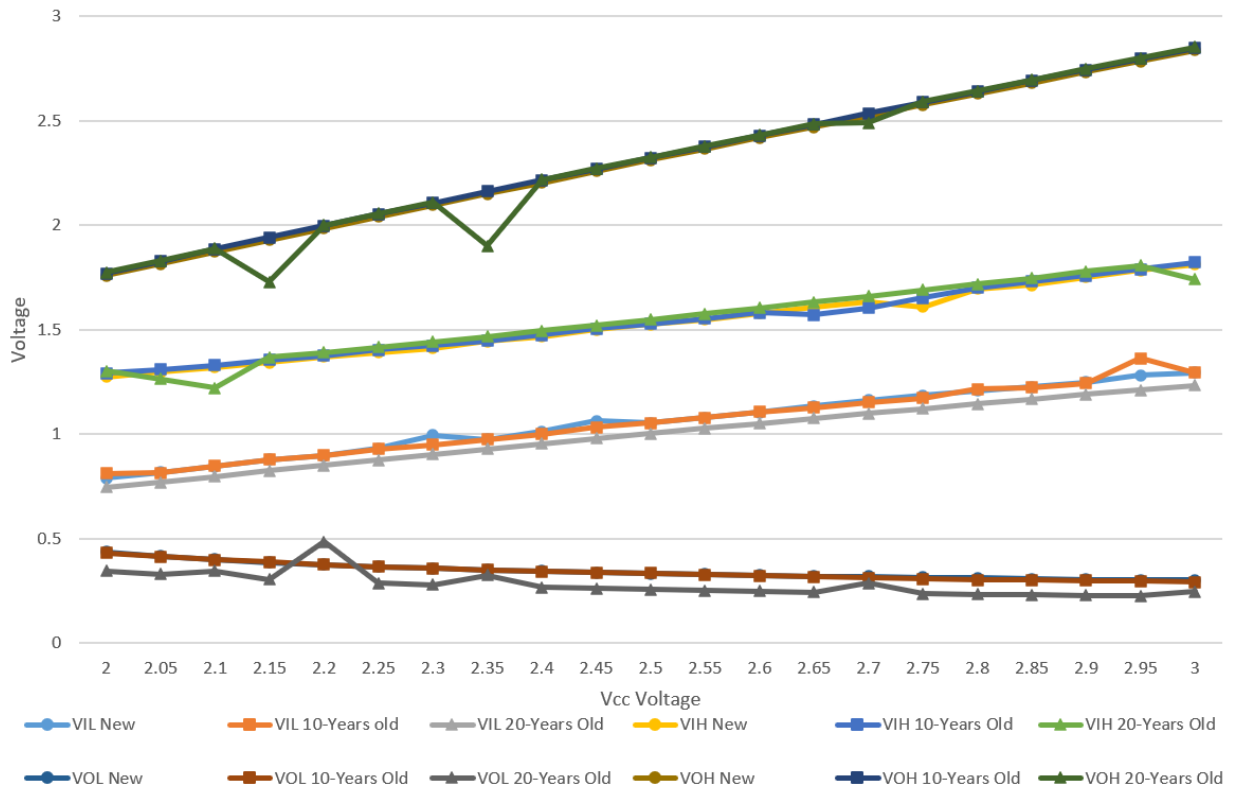Chip 4 Power Consumption over Different Ages and Vcc Voltages

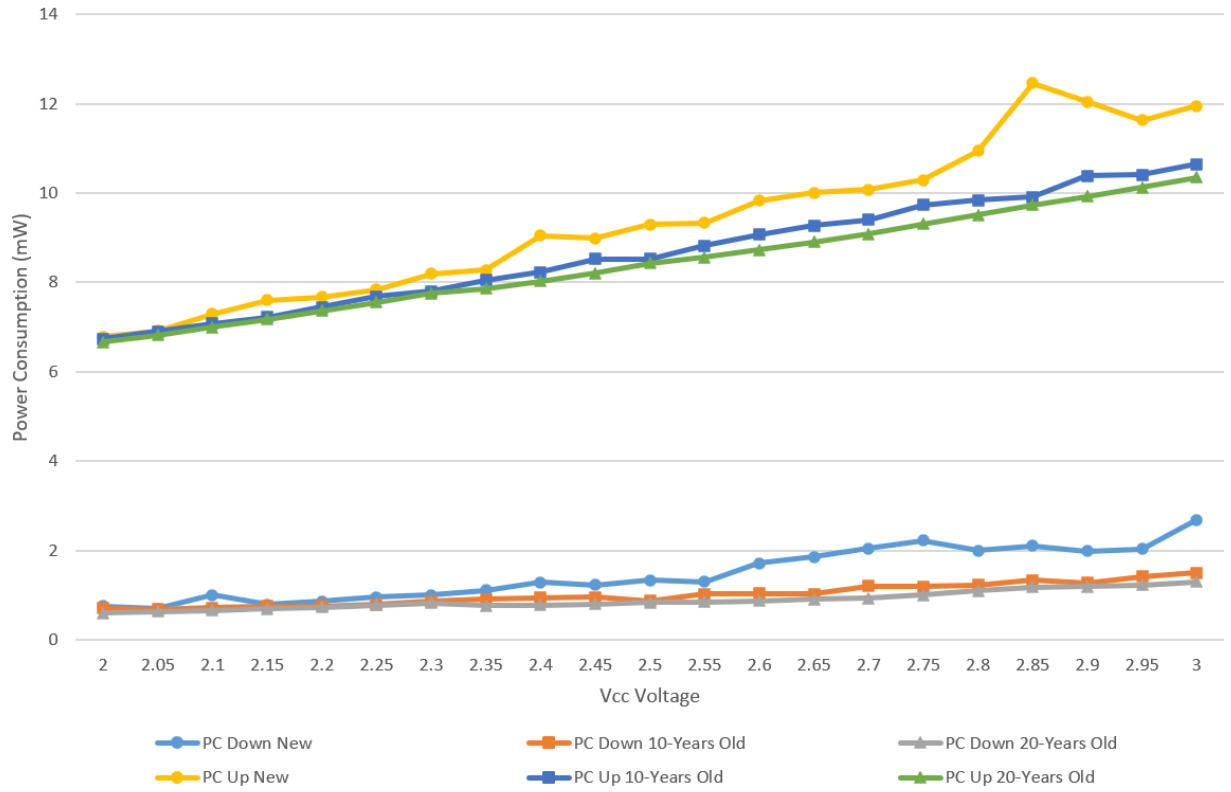Chip 5 Voltage Output over Different Ages and Vcc Voltages

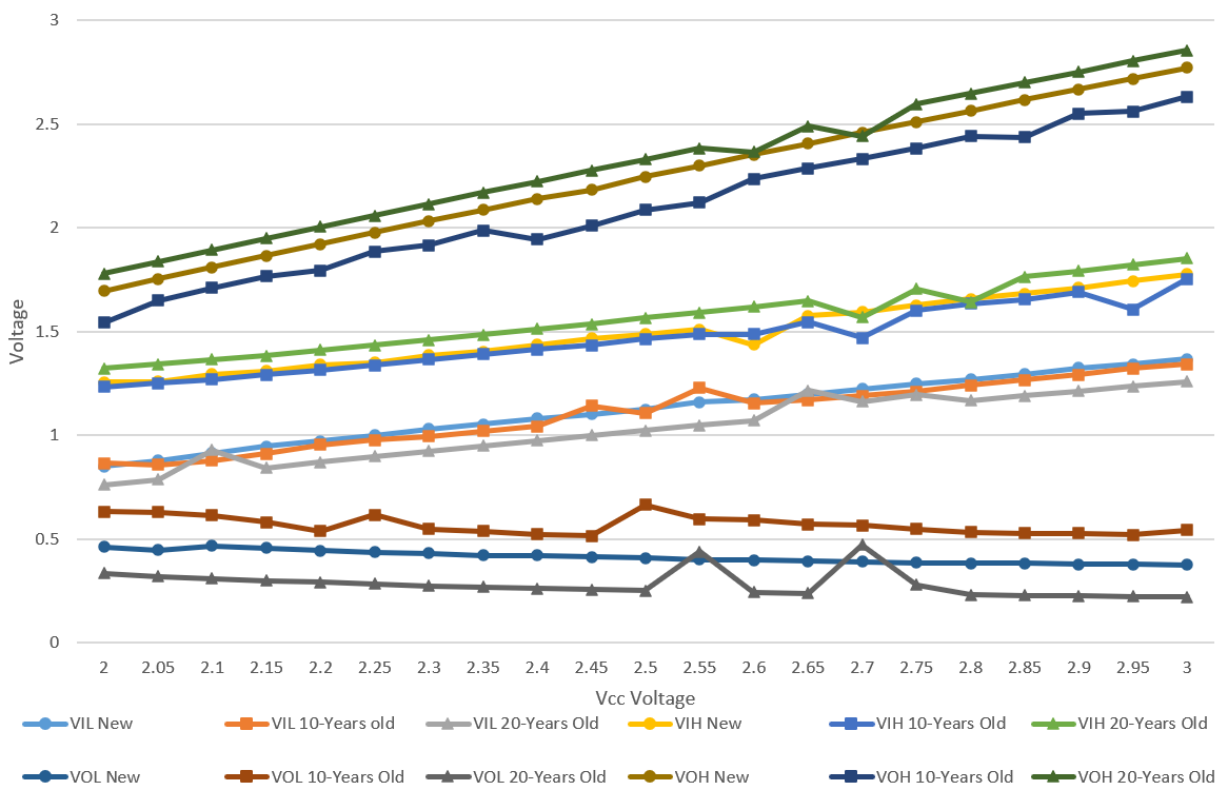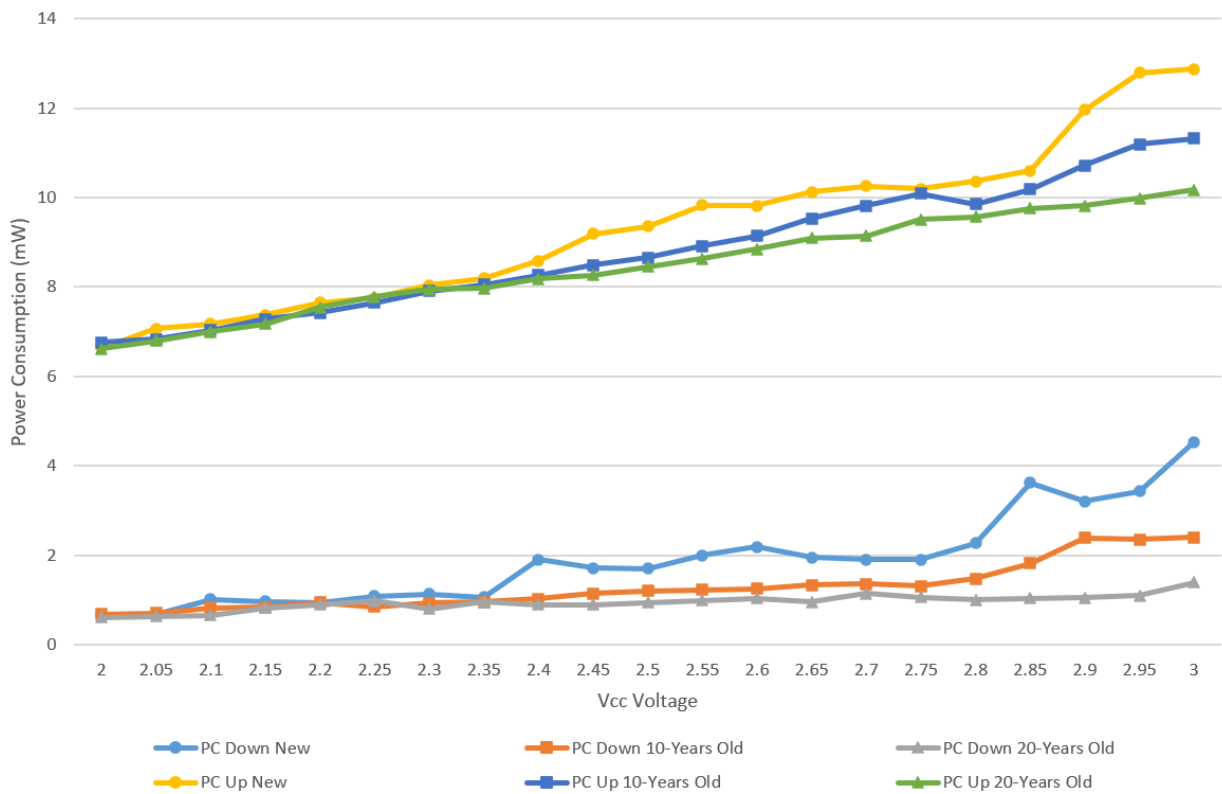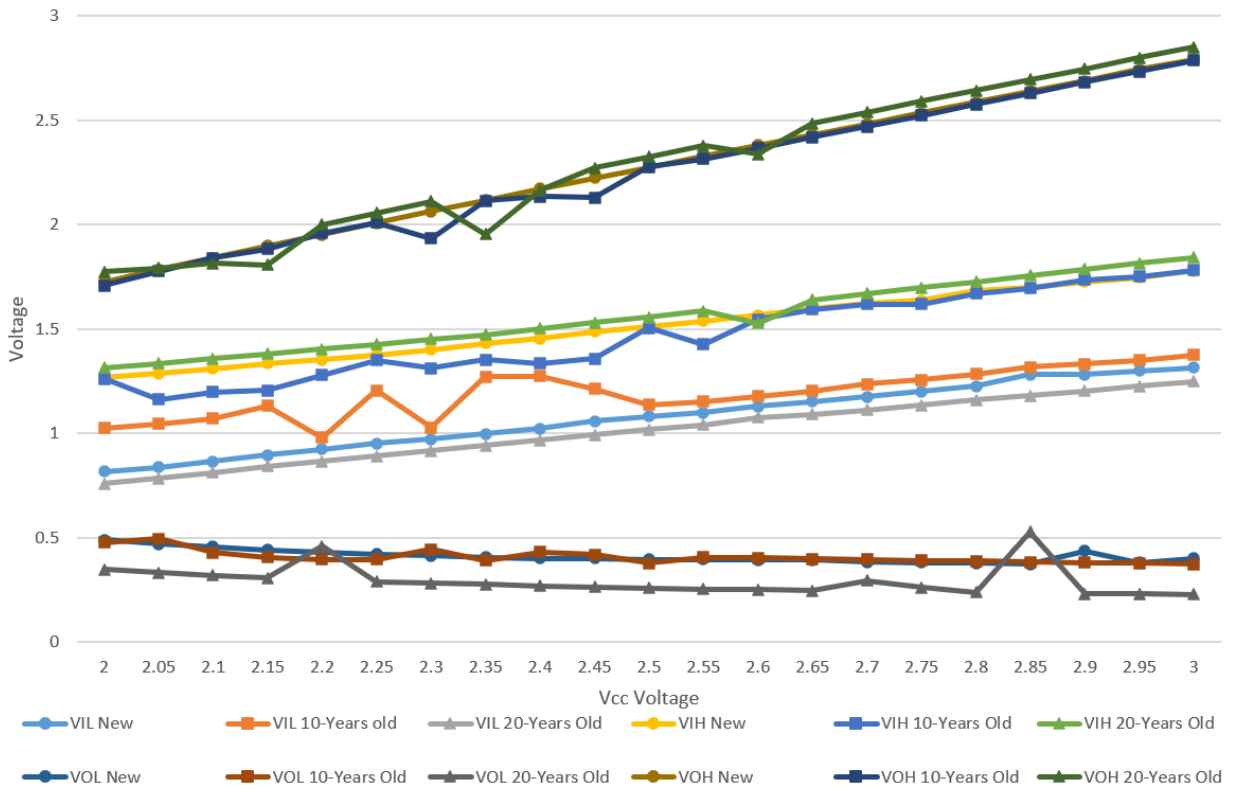Chip 5 Power Consumption over Different Ages and Vcc Voltages

Chip 6 Voltage Output over Different Ages and Vcc Voltages

Chip 6 Power Consumption over Different Ages and Vcc Voltages

Chip 7 Voltage Output over Different Ages and Vcc Voltages

Chip 7 Power Consumption over Different Ages and Vcc Voltages

Chip 9 Voltage Output over Different Ages and Vcc Voltages

Chip 9 Power Consumption over Different Ages and Vcc Voltages
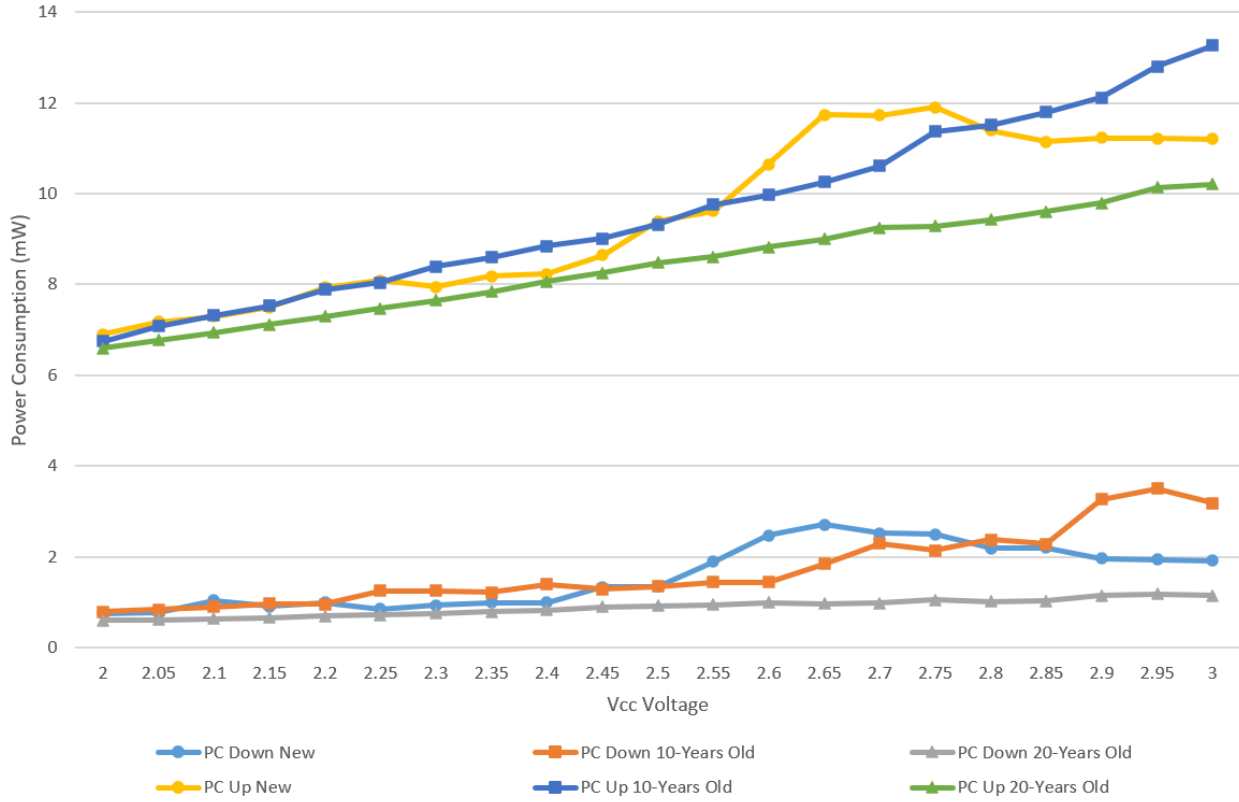
Data Variability for Chip 0 over 49 Test Runs
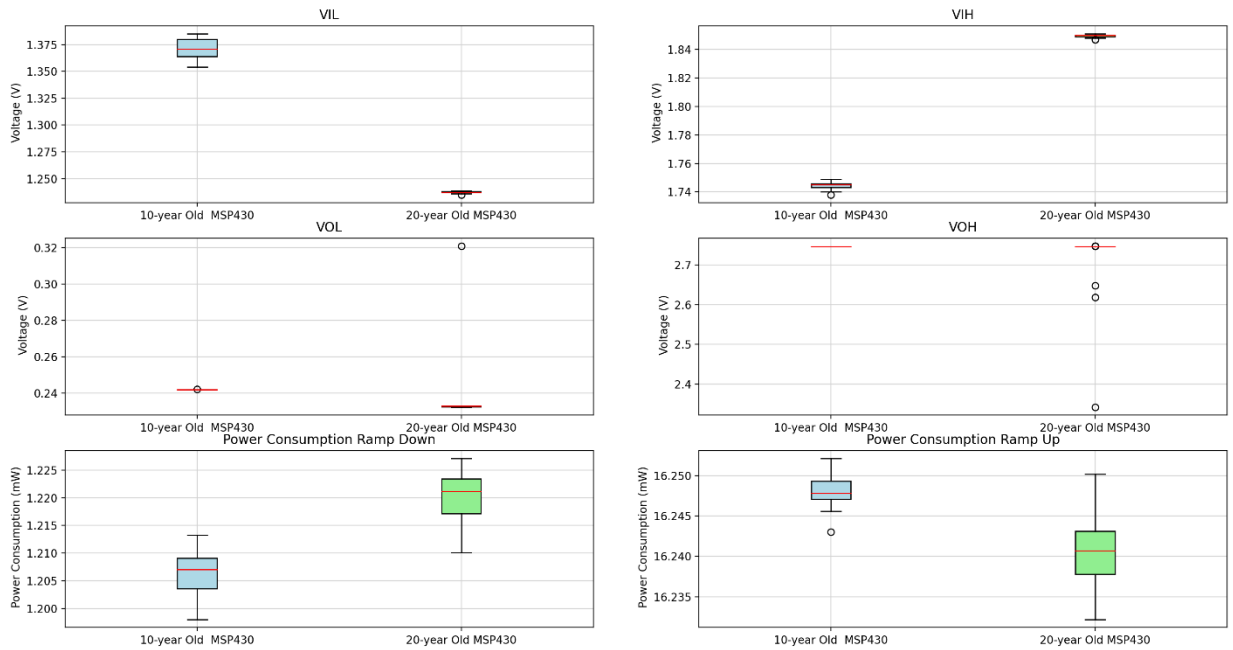
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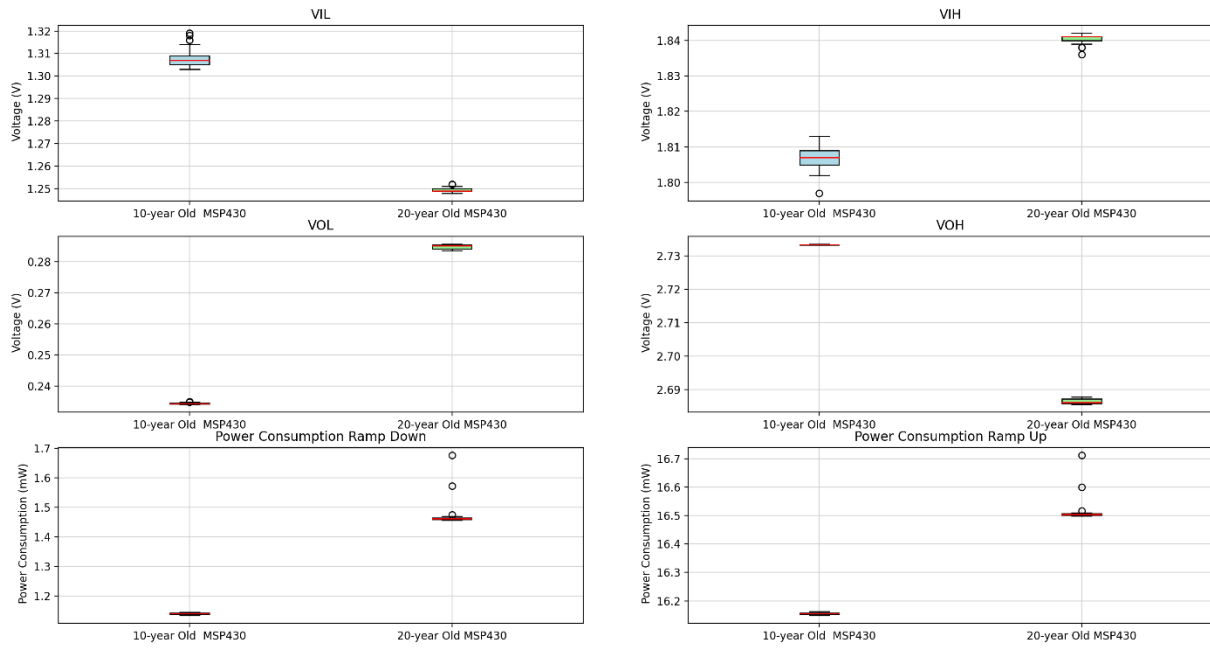
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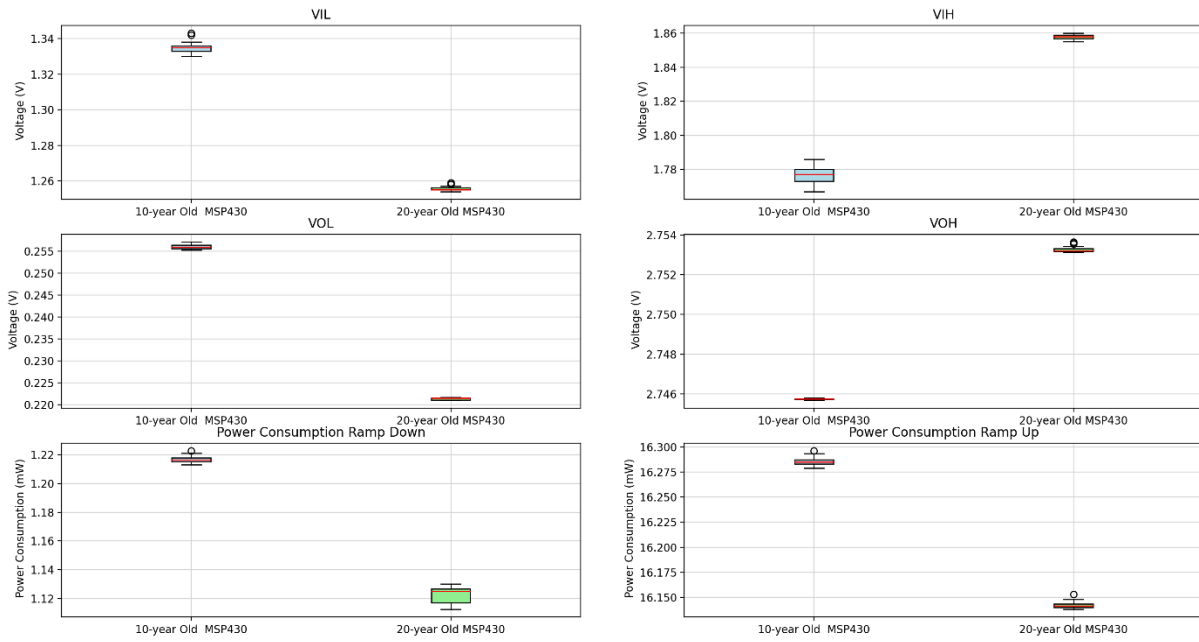
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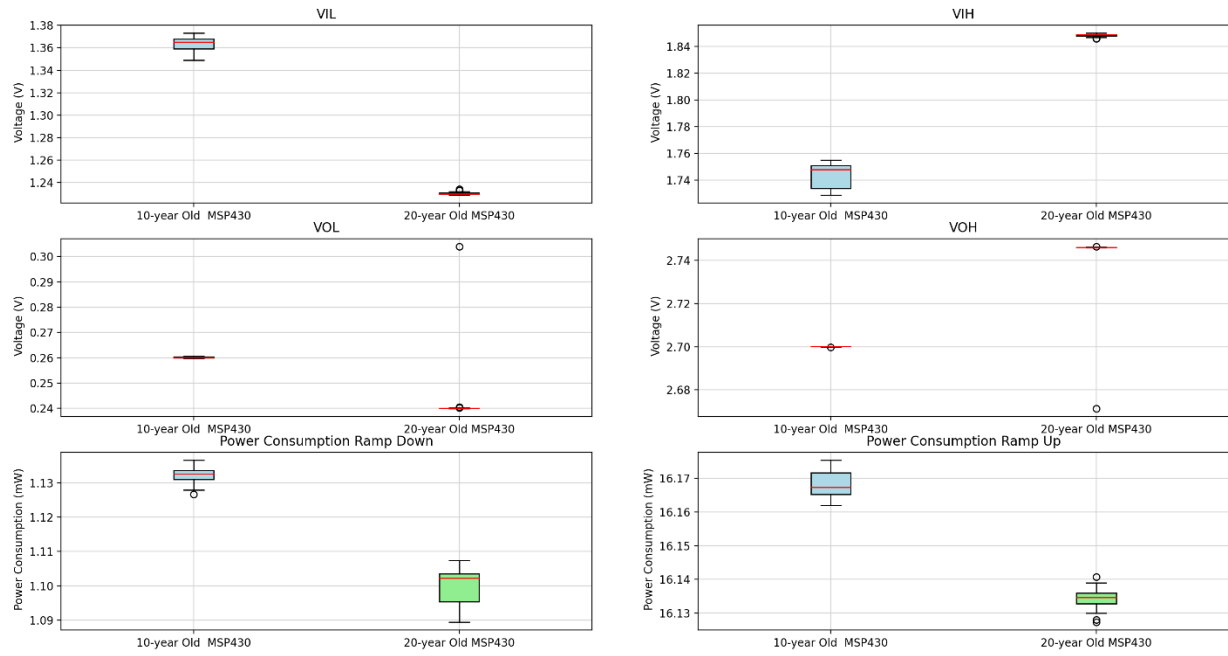
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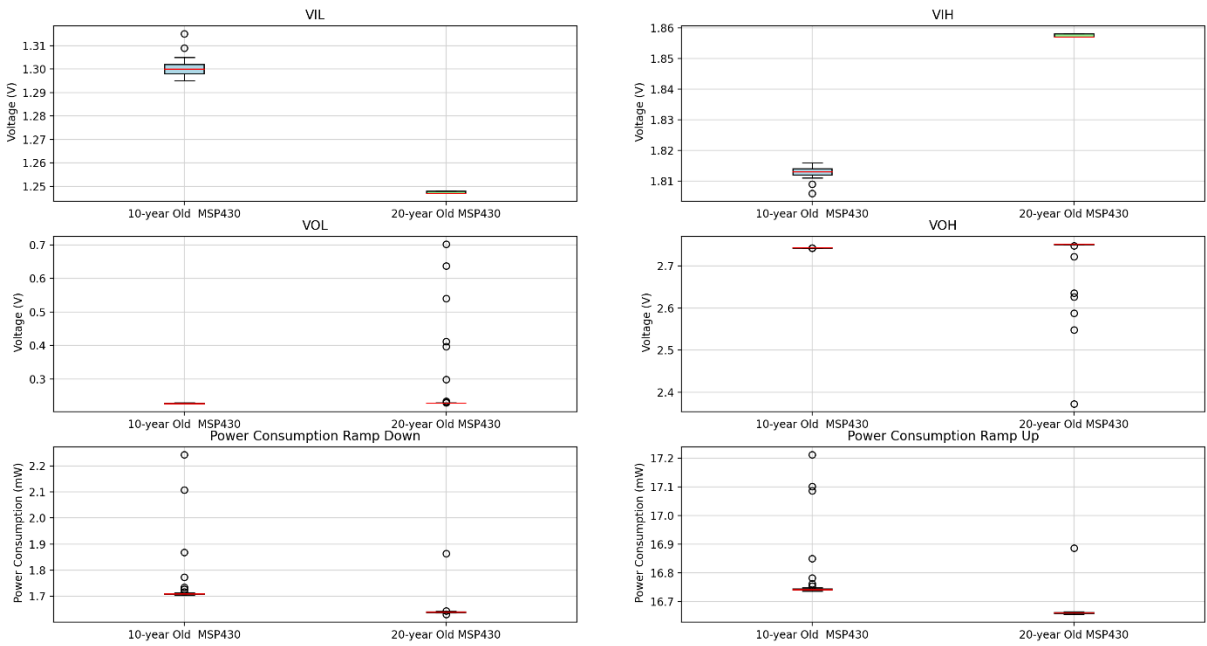
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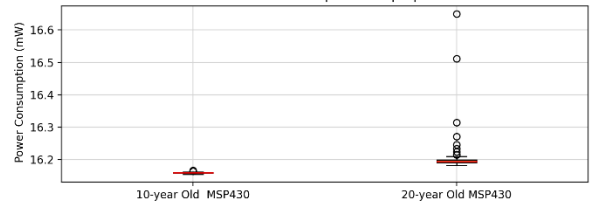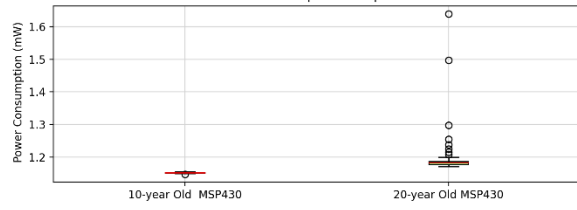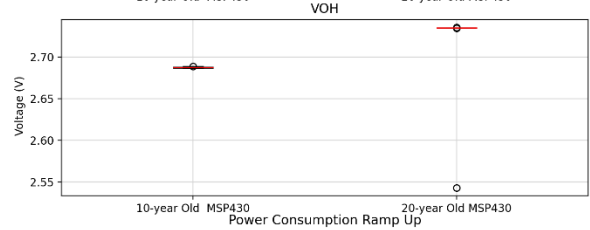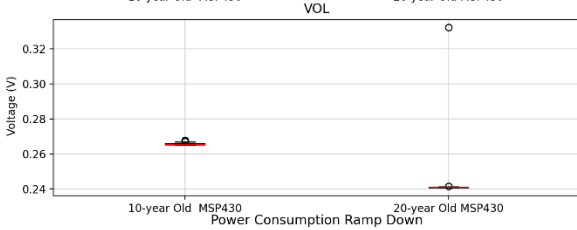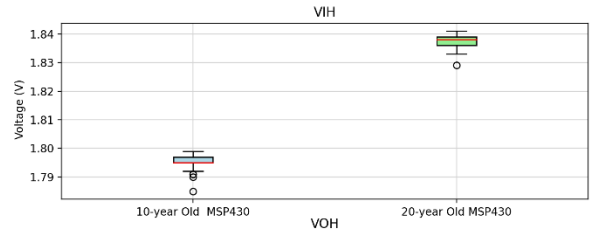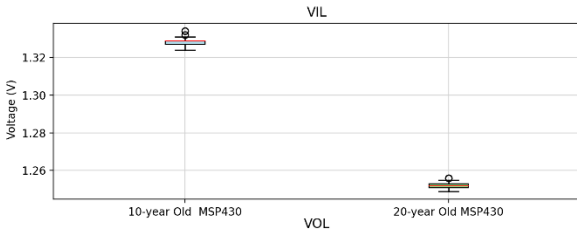
APPENDIX B

ADDITIONAL CHARTS AND GRAPHS FOR "B" CHIPS

DOE Table for Chip 0b and 5b for All Factors

A	B	C	D	Interactions											Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	VCC	AGE	A*B	A*C	A*D	B*C	B*D	C*D	A*B*C	A*B*D	A*C*D	B*C*D	A*B*C*D	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1.27745	1.845725	0.2521475	2.705828	9.37053	25.188325
1	1	1	-1	1	1	-1	1	-1	-1	1	-1	-1	-1	-1	1.275575	1.85885	0.2769778	2.709865	3.472845	20.66645
1	1	-1	1	1	-1	1	-1	1	-1	-1	1	-1	-1	-1	0.791625	1.3261	0.2296563	1.746323	1.087049	7.16999
1	1	-1	-1	1	-1	-1	-1	-1	1	-1	-1	1	1	1	0.7846	1.29695	0.2524388	1.650368	0.78903225	6.8426375
1	-1	1	1	-1	1	1	-1	-1	1	-1	1	1	-1	-1	1.265025	1.857075	0.2348125	2.668495	4.1448625	19.856425
1	-1	1	-1	-1	1	-1	-1	1	-1	1	1	-1	1	1	1.2795	1.861	0.278987	2.720953	2.8845375	19.49675
1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	-1	1	1	0.789775	1.318725	0.2217845	1.62098	1.3675875	7.0922975
1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	-1	-1	0.784325	1.29495	0.2078945	1.759533	1.04606325	7.133325
-1	1	1	1	-1	-1	-1	1	1	1	-1	-1	-1	1	-1	1.254	1.843825	0.2160298	2.735633	2.7431125	18.009525
-1	1	1	-1	-1	-1	1	1	-1	-1	-1	1	1	-1	1	1.2567	1.8567	0.354899	2.735913	1.69595	17.286475
-1	1	-1	1	-1	1	-1	-1	1	-1	1	-1	1	-1	1	0.7648	1.3304	0.2830298	1.76669	0.690298	6.7149425
-1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	1	-1	0.75855	1.30435	0.1919778	1.759923	0.64318125	6.6765825
-1	-1	1	1	1	-1	-1	-1	-1	1	1	1	-1	-1	1	1.264175	1.823975	0.336594	2.63505	1.0620025	16.126875
-1	-1	1	-1	1	-1	1	-1	1	-1	-1	1	1	1	-1	1.26825	1.8583	0.2662608	2.744463	1.065955	16.19185
-1	-1	-1	1	1	1	-1	1	-1	-1	1	1	1	1	-1	0.762525	1.32985	0.2032603	1.683895	0.61277375	6.6024675
-1	-1	-1	-1	1	1	1	1	1	1	-1	-1	-1	-1	1	0.7599	1.30005	0.1913333	1.77757	0.61152	6.6424425

DOE Table for Chip 1b and 6b for All Factors

A	B	C	D	Interactions											Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	VCC	AGE	A*B	A*C	A*D	B*C	B*D	C*D	A*B*C	A*B*D	A*C*D	B*C*D	A*B*C*D	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1.259425	1.846625	0.3029513	2.690035	4.87339	21.403825
1	1	1	-1	1	1	-1	1	-1	-1	1	-1	-1	-1	-1	1.299025	1.80775	0.3196703	2.6022	35.3086	60.5354
1	1	-1	1	1	-1	1	-1	1	-1	-1	1	-1	-1	-1	0.784975	1.3069	0.270689	1.700653	1.00513325	7.04284
1	1	-1	-1	1	-1	-1	-1	-1	1	-1	-1	1	1	1	0.798025	1.269	0.2248438	1.70259	1.175385	7.2293475
1	-1	1	1	-1	1	1	-1	-1	1	-1	1	1	-1	-1	1.25255	1.842975	0.266303	2.60957	3.280795	18.478025
1	-1	1	-1	-1	1	-1	-1	1	-1	1	1	-1	1	1	1.278375	1.837825	0.28286	2.733538	2.8093875	18.47065
1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	-1	1	1	0.7673	1.312875	0.263252	1.719988	0.9463375	6.91844
1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	-1	-1	0.782775	1.275375	0.2128258	1.765423	0.84158825	6.903705
-1	1	1	1	-1	-1	-1	1	1	1	-1	-1	-1	1	-1	1.2324	1.841375	0.243903	2.740478	1.7141175	16.87015
-1	1	1	-1	-1	-1	1	1	-1	-1	-1	1	1	-1	1	1.24925	1.840525	0.3115703	2.628603	1.11528	16.281
-1	1	-1	1	-1	1	-1	-1	1	-1	1	-1	1	-1	1	0.743825	1.31745	0.242581	1.729518	0.6077055	6.622995
-1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	1	-1	0.75925	1.284825	0.2029828	1.78044	0.60266775	6.6306675
-1	-1	1	1	1	-1	-1	-1	-1	1	1	1	-1	-1	1	1.23205	1.834225	0.2562685	2.725828	1.063735	16.361425
-1	-1	1	-1	1	-1	1	-1	1	-1	-1	1	1	1	-1	1.255	1.830925	0.354935	2.726508	1.04975	16.193875
-1	-1	-1	1	1	1	-1	1	-1	-1	1	1	1	1	-1	0.744725	1.315125	0.257921	1.73104	0.61064975	6.618275
-1	-1	-1	-1	1	1	1	1	1	1	-1	-1	-1	-1	1	0.758925	1.279825	0.206063	1.78128	0.59990875	6.63221

DOE Table for Chip 3b and 8b for All Factors

A	B	C	D	Interactions											Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	VCC	AGE	A*B	A*C	A*D	B*C	B*D	C*D	A*B*C	A*B*D	A*C*D	B*C*D	A*B*C*D	VIL	VIH	VOL	VOH	mp Down	amp Up (
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1.310025	1.8343	0.276225	2.709203	13.85248	30.7831
1	1	1	-1	1	1	-1	1	-1	-1	1	-1	-1	-1	-1	1.29745	1.857575	0.26259	2.682583	4.470175	20.27878
1	1	-1	1	1	-1	1	-1	1	-1	-1	1	-1	-1	-1	0.81985	1.3066	0.251157	1.747908	1.05225	7.17223
1	1	-1	-1	1	-1	-1	-1	-1	1	-1	-1	1	1	1	0.8081	1.287875	0.308603	1.742723	1.192433	7.342875
1	-1	1	1	-1	1	1	-1	-1	1	-1	1	1	-1	-1	1.296075	1.83705	0.25969	2.717635	3.203145	19.14533
1	-1	1	-1	-1	1	-1	-1	1	-1	1	1	-1	1	1	1.287075	1.86285	0.263248	2.737898	3.134845	18.3985
1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	-1	1	1	0.80895	1.308075	0.25343	1.684108	0.702206	6.81087
1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	1	-1	-1	0.79615	1.292875	0.2462	1.76789	0.825259	6.943528
-1	1	1	1	-1	-1	-1	1	1	1	-1	-1	-1	1	-1	1.2795	1.83635	0.255171	2.684598	1.338903	16.50008
-1	1	1	-1	-1	-1	1	1	-1	-1	-1	1	1	-1	1	1.264525	1.854525	0.290603	2.645573	1.422035	16.72835
-1	1	-1	1	-1	1	-1	-1	1	-1	1	-1	1	-1	1	0.78345	1.317025	0.305545	1.76779	0.594639	6.613955
-1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	1	-1	0.775375	1.30115	0.265691	1.677563	0.641462	6.656688
-1	-1	1	1	1	-1	-1	-1	-1	1	1	1	-1	-1	1	1.280925	1.820875	0.24759	2.727188	1.556838	17.04643
-1	-1	1	-1	1	-1	1	-1	1	-1	-1	1	1	1	-1	1.273675	1.847725	0.240264	2.754975	1.503893	16.90678
-1	-1	-1	1	1	1	-1	1	-1	-1	1	1	1	1	-1	0.790825	1.320325	0.238287	1.742328	0.637236	6.635843
-1	-1	-1	-1	1	1	1	1	1	1	-1	-1	-1	-1	1	0.7688	1.298275	0.19579	1.671875	0.625056	6.678168

DOE Table for Chip 3b and 8b for All Factors

| A | B | C | D | | | | Interactions | | | | | | | | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 |
TEMP	HUMIDITY	VCC	AGE	A*B	A*C	A*D	B*C	B*D	C*D	A*B*C	A*B*D	A*C*D	B*C*D	A*B*C*D	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1.279475	1.850225	0.3424625	2.666875	5.48768	22.13565
1	1	1	-1	1	1	-1	1	-1	-1	1	-1	-1	-1	-1	1.267075	1.8608	0.286172	2.655803	7.096395	23.2589
1	1	-1	1	1	-1	1	-1	1	-1	-1	1	-1	-1	-1	0.7819	1.310175	0.2304678	1.74751	1.306025	7.43524
1	1	-1	-1	1	-1	-1	-1	-1	1	-1	-1	1	1	1	0.800475	1.315525	0.3256118	1.748933	1.01946375	7.3084775
1	-1	1	1	-1	1	1	-1	-1	1	-1	-1	1	-1	-1	1.267775	1.855925	0.293932	2.647358	3.563	20.607825
1	-1	1	-1	-1	1	-1	-1	1	-1	-1	1	1	-1	1	1.26135	1.846925	0.3402515	2.733705	5.5205725	21.0065
1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	1	1	1	0.7725	1.3127	0.2159165	1.667373	0.99557	6.9286
1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	-1	-1	-1	0.79145	1.313575	0.267658	1.756495	0.7616445	6.864135
-1	1	1	1	-1	-1	-1	1	1	1	-1	-1	-1	1	-1	1.24425	1.850925	0.315121	2.67907	1.2531525	16.496975
-1	1	1	-1	-1	-1	1	1	-1	-1	-1	1	1	-1	1	1.2472	1.85435	0.24986	2.729113	1.9897275	16.988875
-1	1	-1	1	-1	1	-1	-1	1	-1	1	-1	1	-1	1	0.752325	1.316525	0.220247	1.67407	0.620934	6.6154975
-1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	1	-1	0.766825	1.32105	0.235064	1.767203	0.62770925	6.6617275
-1	-1	1	1	1	-1	-1	-1	-1	1	1	-1	-1	-1	1	1.24545	1.846325	0.319172	2.625973	1.1680525	16.219975
-1	-1	1	-1	1	-1	1	-1	1	-1	-1	1	1	1	-1	1.255675	1.86155	0.2588915	2.748325	1.1041225	16.2096
-1	-1	-1	1	1	1	-1	1	-1	-1	-1	1	1	1	-1	0.7523	1.32755	0.2252108	1.745263	0.59186675	6.5849175
-1	-1	-1	-1	1	1	1	1	1	1	-1	-1	-1	-1	1	0.762575	1.316625	0.219159	1.776385	0.58188475	6.6085325

DOE Table for Chip 4b and 9b for All Factors

| A | B | C | D | | | | Interactions | | | | | | | | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 |
TEMP	HUMIDITY	VCC	AGE	A*B	A*C	A*D	B*C	B*D	C*D	A*B*C	A*B*D	A*C*D	B*C*D	A*B*C*D	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1.284	1.8509	0.3575765	2.653883	6.229985	22.06425
1	1	1	-1	1	1	-1	1	-1	-1	1	-1	-1	-1	-1	1.274725	1.855075	0.2620725	2.665688	5.5559775	21.612525
1	1	-1	1	1	-1	1	-1	1	-1	-1	1	-1	-1	-1	0.7759	1.30125	0.2835785	1.685398	1.2055875	7.2067775
1	1	-1	-1	1	-1	-1	-1	-1	1	-1	-1	1	1	1	0.7909	1.306975	0.2403445	1.755763	1.57705	7.700775
1	-1	1	1	-1	1	1	-1	-1	1	-1	-1	1	-1	-1	1.2811	1.845225	0.2931055	2.721305	4.8873025	20.1701
1	-1	1	-1	-1	1	-1	-1	1	-1	-1	1	1	-1	1	1.263975	1.843775	0.24746	2.737648	4.8344925	20.59515
1	-1	-1	1	-1	-1	1	1	-1	-1	1	-1	1	1	1	0.77845	1.295325	0.2782248	1.694735	1.1372825	6.8701125
1	-1	-1	-1	-1	-1	-1	1	1	1	1	1	-1	-1	-1	0.792325	1.2969	0.2253135	1.766893	1.1483695	6.9629925
-1	1	1	1	-1	-1	-1	1	1	1	-1	-1	-1	1	-1	1.269475	1.8277	0.2536538	2.73926	1.4163425	16.5135
-1	1	1	-1	-1	-1	1	1	-1	-1	-1	1	1	-1	1	1.263275	1.824525	0.2314098	2.75706	1.7609425	17.0767
-1	1	-1	1	-1	1	-1	-1	1	-1	1	-1	1	-1	1	0.760325	1.299825	0.2250798	1.74624	0.60498175	6.634965
-1	1	-1	-1	-1	1	1	-1	-1	1	1	1	-1	1	-1	0.770775	1.30005	0.2063955	1.78263	0.66384475	6.735745
-1	-1	1	1	1	-1	-1	-1	-1	1	1	-1	-1	-1	1	1.27145	1.824025	0.3339033	2.664888	1.09261	16.439925
-1	-1	1	-1	1	-1	1	-1	1	-1	-1	1	1	1	-1	1.2583	1.82025	0.2263138	2.759238	1.0555675	16.270475
-1	-1	-1	1	1	1	-1	1	-1	-1	-1	1	1	1	-1	0.756525	1.302325	0.210501	1.754713	0.60269425	6.5973025
-1	-1	-1	-1	1	1	1	1	1	1	-1	-1	-1	-1	1	0.766975	1.296325	0.1956765	1.78455	0.61648675	6.6428675

Pareto Chart of Chip 0b-5b with all factors
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Factor | Name
A | TEMP
B | HUMIDITY
C | VCC
D | AGE

Lenth's PSE = 1.25362

Pareto Chart of Chip 0b-5b with all factors
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Factor | Name
A | TEMP
B | HUMIDITY
C | VCC
D | AGE

Lenth's PSE = 0.915593

Pareto Chart of Chip 0b-5b with all factors
(response is VIH, α = 0.05)

Lenth's PSE = 0.00510469

Pareto Chart of Chip 0b-5b with all factors
(response is VIL, α = 0.05)

Lenth's PSE = 0.00305156

Pareto Chart of Chip 0b-5b with all factors
(response is VOH, α = 0.05)

Pareto Chart of Chip 0b-5b with all factors
(response is VOL, α = 0.05)

Pareto Chart of Chip 1b-6b with all factors
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Pareto Chart of Chip 1b-6b with all factors
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Pareto Chart of Chip 1b-6b with all factors
(response is VIH, α = 0.05)

Lenth's PSE = 0.00620625

Pareto Chart of Chip 1b-6b with all factors
(response is VIL, α = 0.05)

Lenth's PSE = 0.00389531

Pareto Chart of Chip 1b-6b with all factors
(response is VOH, α = 0.05)

Lenth's PSE = 0.0239639

Pareto Chart of Chip 1b-6b with all factors
(response is VOL, α = 0.05)

Lenth's PSE = 0.00893963

Pareto Chart of Chip 2b-7b for all factors
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Lenth's PSE = 1.82218

Pareto Chart of Chip 2b-7b for all factors
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Lenth's PSE = 2.16646

Pareto Chart of Chip 2b-7b for all factors
(response is VIH, α = 0.05)

Lenth's PSE = 0.00214687

Pareto Chart of Chip 2b-7b for all factors
(response is VIL, α = 0.05)

Lenth's PSE = 0.00207187

Pareto Chart of Chip 2b-7b for all factors
(response is VOH, α = 0.05)

Lenth's PSE = 0.0183192

Pareto Chart of Chip 2b-7b for all factors
(response is VOL, α = 0.05)

Lenth's PSE = 0.0154128

Pareto Chart of Chip 3b-8b for all factors
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Pareto Chart of Chip 3b-8b for all factors
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Pareto Chart of Chip 3b-8b for all factors
(response is VIH, α = 0.05)

Lenth's PSE = 0.00379219

Pareto Chart of Chip 3b-8b for all factors
(response is VIL, α = 0.05)

Lenth's PSE = 0.00360938

Pareto Chart of Chip 3b-8b for all factors
(response is VOH, α = 0.05)

Lenth's PSE = 0.0230578

Pareto Chart of Chip 3b-8b for all factors
(response is VOL, α = 0.05)

Lenth's PSE = 0.0129557

Pareto Chart of Chip 4b-9b for all factors
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Lenth's PSE = 0.149901

Pareto Chart of Chip 4b-9b for all factors
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Lenth's PSE = 0.203966

Pareto Chart of Chip 4b-9b for all factors
(response is VIH, α = 0.05)

Lenth's PSE = 0.0010875

Pareto Chart of Chip 4b-9b for all factors
(response is VIL, α = 0.05)

Lenth's PSE = 0.00250312

Pareto Chart of Chip 4b-9b for all factors
(response is VOH, α = 0.05)

Lenth's PSE = 0.0150670

Pareto Chart of Chip 4b-9b for all factors
(response is VOL, α = 0.05)

Lenth's PSE = 0.0228126

DOE Table for Chip 0b and 5b at 2V Vcc

A	B	C	Interactions				Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	AGE	A*B	A*C	B*C	A*B*C	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	0.791625	1.3261	0.2296563	1.746323	1.087049	7.16999
1	1	-1	1	-1	-1	-1	0.7846	1.29695	0.2524388	1.650368	0.78903225	6.8426375
1	-1	1	-1	1	-1	-1	0.789775	1.318725	0.2217845	1.62098	1.3675875	7.0922975
1	-1	-1	-1	-1	1	1	0.784325	1.29495	0.2078945	1.759533	1.04606325	7.133325
-1	1	1	-1	-1	1	-1	0.7648	1.3304	0.2830298	1.76669	0.690298	6.7149425
-1	1	-1	-1	1	-1	1	0.75855	1.30435	0.1919778	1.759923	0.64318125	6.6765825
-1	-1	1	1	-1	-1	1	0.762525	1.32985	0.2032603	1.683895	0.61277375	6.6024675
-1	-1	-1	1	1	1	-1	0.7599	1.30005	0.1913333	1.77757	0.61152	6.6424425

DOE Table for Chip 1b and 6b at 2V Vcc

A	B	C	Interactions				Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	AGE	A*B	A*C	B*C	A*B*C	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	0.784975	1.3069	0.270689	1.700653	1.00513325	7.04284
1	1	-1	1	-1	-1	-1	0.798025	1.269	0.2248438	1.70259	1.175385	7.2293475
1	-1	1	-1	1	-1	-1	0.7673	1.312875	0.263252	1.719988	0.9463375	6.91844
1	-1	-1	-1	-1	1	1	0.782775	1.275375	0.2128258	1.765423	0.84158825	6.903705
-1	1	1	-1	-1	1	-1	0.743825	1.31745	0.242581	1.729518	0.6077055	6.622995
-1	1	-1	-1	1	-1	1	0.75925	1.284825	0.2029828	1.78044	0.60266775	6.6306675
-1	-1	1	1	-1	-1	1	0.744725	1.315125	0.257921	1.73104	0.61064975	6.618275
-1	-1	-1	1	1	1	-1	0.758925	1.279825	0.206063	1.78128	0.59990875	6.63221

DOE Table for Chip 2b and 7b at 2V Vcc

A	B	C	Interactions				Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	AGE	A*B	A*C	B*C	A*B*C	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	0.81985	1.3066	0.251157	1.747908	1.0522495	7.17223
1	1	-1	1	-1	-1	-1	0.8081	1.287875	0.308603	1.742723	1.1924325	7.342875
1	-1	1	-1	1	-1	-1	0.80895	1.308075	0.25343	1.684108	0.70220625	6.81087
1	-1	-1	-1	-1	1	1	0.79615	1.292875	0.2462	1.76789	0.82525925	6.9435275
-1	1	1	-1	-1	1	-1	0.78345	1.317025	0.305545	1.76779	0.594639	6.613955
-1	1	-1	-1	1	-1	1	0.775375	1.30115	0.265691	1.677563	0.641462	6.6566875
-1	-1	1	1	-1	-1	1	0.790725	1.320325	0.238287	1.742328	0.63723625	6.6358425
-1	-1	-1	1	1	1	-1	0.7688	1.298275	0.19579	1.671875	0.62505575	6.6781675

DOE Table for Chip 3b and 8b at 2V Vcc

A	B	C	Interactions				Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	AGE	A*B	A*C	B*C	A*B*C	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	0.7819	1.310175	0.2304678	1.74751	1.306025	7.43524
1	1	-1	1	-1	-1	-1	0.800475	1.315525	0.3256118	1.748933	1.01946375	7.3084775
1	-1	1	-1	1	-1	-1	0.7725	1.3127	0.2159165	1.667373	0.99557	6.9286
1	-1	-1	-1	-1	1	1	0.79145	1.313575	0.267658	1.756495	0.7616445	6.864135
-1	1	1	-1	-1	1	-1	0.752325	1.316525	0.220247	1.67407	0.620934	6.6154975
-1	1	-1	-1	1	-1	1	0.766825	1.32105	0.235064	1.767203	0.62770925	6.6617275
-1	-1	1	1	-1	-1	1	0.7523	1.32755	0.2252108	1.745263	0.59186675	6.5849175
-1	-1	-1	1	1	1	-1	0.762575	1.316625	0.219159	1.776385	0.58188475	6.6085325

							Y1	Y2	Y3	Y4	Y5	Y6
A	**B**	**C**	**Interactions**				**Y1**	**Y2**	**Y3**	**Y4**	**Y5**	**Y6**
TEMP	**HUMIDITY**	**AGE**	**A*B**	**A*C**	**B*C**	**A*B*C**	**VIL**	**VIH**	**VOL**	**VOH**	**PC Ramp Down (mW)**	**PC Ramp Up (mW)**
1	1	1	1	1	1	1	0.7759	1.30125	0.2835785	1.685398	1.2055875	7.2067775
1	1	-1	1	-1	-1	-1	0.7909	1.306975	0.2403445	1.755763	1.57705	7.700775
1	-1	1	-1	1	-1	-1	0.77845	1.295325	0.2782248	1.694735	1.1372825	6.8701125
1	-1	-1	-1	-1	1	1	0.792325	1.2969	0.2253135	1.766893	1.1483695	6.9629925
-1	1	1	-1	-1	1	-1	0.760325	1.299825	0.2250798	1.74624	0.60498175	6.634965
-1	1	-1	-1	1	-1	1	0.770775	1.30005	0.2063955	1.78263	0.66384475	6.735745
-1	-1	1	1	-1	-1	1	0.756525	1.302375	0.210501	1.754713	0.60269425	6.5973025
-1	-1	-1	1	1	1	-1	0.766975	1.296325	0.1956765	1.78455	0.61648675	6.6428675

DOE Table for Chip 4b and 9b at 2V Vcc

Pareto Chart of Chip 0b-5b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Lenth's PSE = 0.214189

Pareto Chart of Chip 0b-5b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Lenth's PSE = 0.108372

Pareto Chart of Chip 0b-5b Effects at 2V Vcc
(response is VIH, α = 0.05)

Pareto Chart of Chip 0b-5b Effects at 2V Vcc
(response is VIL, α = 0.05)

Pareto Chart of Chip 0b-5b Effects at 2V Vcc
(response is VOH, α = 0.05)

Pareto Chart of Chip 0b-5b Effects at 2V Vcc
(response is VOL, α = 0.05)

Pareto Chart of Chip 1b-6b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Lenth's PSE = 0.103125

Pareto Chart of Chip 1b-6b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Lenth's PSE = 0.0754659

Pareto Chart of Chip 1b-6b Effects at 2V Vcc
(response is VIH, α = 0.05)

Lenth's PSE = 0.00188438

Pareto Chart of Chip 1b-6b Effects at 2V Vcc
(response is VIL, α = 0.05)

Lenth's PSE = 0.00675

Pareto Chart of Chip 1b-6b Effects at 2V Vcc
(response is VOH, α = 0.05)

Lenth's PSE = 0.0299269

Pareto Chart of Chip 1b-6b Effects at 2V Vcc
(response is VOL, α = 0.05)

Lenth's PSE = 0.00459741

Pareto Chart of Chip 2b-7b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Pareto Chart of Chip 2b-7b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Pareto Chart of Chip 2b-7b Effects at 2V Vcc
(response is VIH, α = 0.05)

Pareto Chart of Chip 2b-7b Effects at 2V Vcc
(response is VIL, α = 0.05)

Pareto Chart of Chip 2b-7b Effects at 2V Vcc
(response is VOH, α = 0.05)

Pareto Chart of Chip 2b-7b Effects at 2V Vcc
(response is VOL, α = 0.05)

Pareto Chart of Chip 3b-8b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Lenth's PSE = 0.19398

Pareto Chart of Chip 3b-8b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Lenth's PSE = 0.0455184

Pareto Chart of Chip 3b-8b Effects at 2V Vcc
(response is VIH, α = 0.05)

Lenth's PSE = 0.00411563

Pareto Chart of Chip 3b-8b Effects at 2V Vcc
(response is VIL, α = 0.05)

Lenth's PSE = 0.00478125

Pareto Chart of Chip 4b-9b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Pareto Chart of Chip 4b-9b Effects at 2V Vcc
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Pareto Chart of Chip 4b-9b Effects at 2V Vcc
(response is VIH, α = 0.05)

Pareto Chart of Chip 4b-9b Effects at 2V Vcc
(response is VIL, α = 0.05)

Pareto Chart of Chip 4b-9b Effects at 2V Vcc
(response is VOH, α = 0.05)

Pareto Chart of Chip 4b-9b Effects at 2V Vcc
(response is VOL, α = 0.05)

DOE Table for Chip 0b and 5b at 3V Vcc

A	B	C	Interactions				Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	AGE	A*B	A*C	B*C	A*B*C	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1.27745	1.845725	0.2521475	2.705828	9.37053	25.188325
1	1	-1	1	-1	-1	-1	1.275575	1.85885	0.2769778	2.709865	3.472845	20.66645
1	-1	1	-1	1	-1	-1	1.265025	1.857075	0.2348125	2.668495	4.1448625	19.856425
1	-1	-1	-1	-1	1	1	1.2795	1.861	0.278987	2.720953	2.8845375	19.49675
-1	1	1	-1	-1	1	-1	1.254	1.843825	0.2160298	2.735633	2.7431125	18.009525
-1	1	-1	-1	1	-1	1	1.2567	1.8567	0.354899	2.735913	1.69595	17.286475
-1	-1	1	1	-1	-1	1	1.264175	1.823975	0.336594	2.63505	1.0620025	16.126875
-1	-1	-1	1	1	1	-1	1.26825	1.8583	0.2662608	2.744463	1.065955	16.19185

DOE Table for Chip 1b and 6b at 3V Vcc

A	B	C	Interactions				Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	AGE	A*B	A*C	B*C	A*B*C	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1.259425	1.846625	0.3029513	2.690035	4.87339	21.403825
1	1	-1	1	-1	-1	-1	1.299925	1.80775	0.3196703	2.6022	35.3086	60.5354
1	-1	1	-1	1	-1	-1	1.25255	1.842975	0.266303	2.60957	3.280795	18.478025
1	-1	-1	-1	-1	1	1	1.278375	1.837825	0.28286	2.733538	2.8093875	18.47065
-1	1	1	-1	-1	1	-1	1.2324	1.841375	0.243903	2.740478	1.7141175	16.87015
-1	1	-1	-1	1	-1	1	1.24925	1.840525	0.3115703	2.628603	1.11528	16.281
-1	-1	1	1	-1	-1	1	1.23205	1.834225	0.2562685	2.725828	1.063735	16.361425
-1	-1	-1	1	1	1	-1	1.255	1.830925	0.354935	2.726508	1.04975	16.193875

DOE Table for Chip 2b and 7b at 3V Vcc

A	B	C	Interactions				Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	AGE	A*B	A*C	B*C	A*B*C	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1.310025	1.8343	0.2762253	2.709203	13.8524825	30.7831
1	1	-1	1	-1	-1	-1	1.29745	1.857575	0.2625903	2.682583	4.470175	20.278775
1	-1	1	-1	1	-1	-1	1.296075	1.83705	0.2596898	2.717635	3.203145	19.145325
1	-1	-1	-1	-1	1	1	1.287075	1.86285	0.2632475	2.737898	3.134845	18.3985
-1	1	1	-1	-1	1	-1	1.2795	1.83635	0.2551708	2.684598	1.3389025	16.500075
-1	1	-1	-1	1	-1	1	1.264525	1.854525	0.2906025	2.645573	1.422035	16.72835
-1	-1	1	1	-1	-1	1	1.280925	1.820875	0.2475895	2.727188	1.5568375	17.046425
-1	-1	-1	1	1	1	-1	1.273675	1.847725	0.2402643	2.754975	1.5038925	16.906775

DOE Table for Chip 3b and 8b at 3V Vcc

A	B	C	Interactions				Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	AGE	A*B	A*C	B*C	A*B*C	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1.279475	1.850225	0.342463	2.666875	5.48768	22.13565
1	1	-1	1	-1	-1	-1	1.267075	1.8608	0.286172	2.655803	7.096395	23.2589
1	-1	1	-1	1	-1	-1	1.267775	1.855925	0.293932	2.647358	3.563	20.607825
1	-1	-1	-1	-1	1	1	1.26135	1.846925	0.340252	2.733705	5.5205725	21.0065
-1	1	1	-1	-1	1	-1	1.24425	1.850925	0.315121	2.67907	1.2531525	16.496975
-1	1	-1	-1	1	-1	1	1.2472	1.85435	0.24986	2.729113	1.9897275	16.988875
-1	-1	1	1	-1	-1	1	1.24545	1.846325	0.319172	2.625973	1.1680525	16.219975
-1	-1	-1	1	1	1	-1	1.255675	1.86155	0.258892	2.748325	1.1041225	16.2096

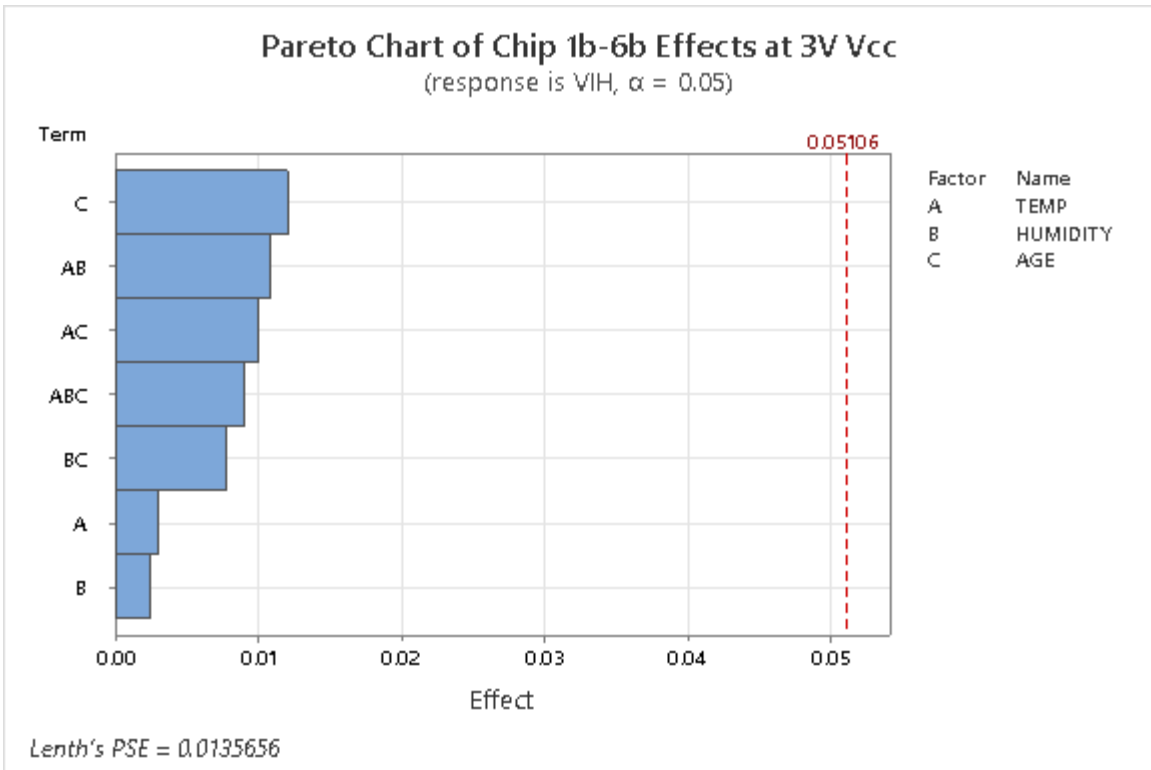## DOE Table for Chip 4b and 9b at 3V Vcc

A	B	C	Interactions				Y1	Y2	Y3	Y4	Y5	Y6
TEMP	HUMIDITY	AGE	A*B	A*C	B*C	A*B*C	VIL	VIH	VOL	VOH	PC Ramp Down (mW)	PC Ramp Up (mW)
1	1	1	1	1	1	1	1.284	1.8509	0.3575765	2.653883	6.229985	22.06425
1	1	-1	1	-1	-1	-1	1.274725	1.855075	0.2620725	2.665688	5.5559775	21.612525
1	-1	1	-1	1	-1	-1	1.2811	1.845225	0.2931055	2.721305	4.8873025	20.1701
1	-1	-1	-1	-1	1	1	1.263975	1.843775	0.24746	2.737648	4.8344925	20.59515
-1	1	1	-1	-1	1	-1	1.269475	1.8277	0.2536538	2.73926	1.4163425	16.5135
-1	1	-1	-1	1	-1	1	1.263275	1.824525	0.2314098	2.75706	1.7609425	17.0767
-1	-1	1	1	-1	-1	1	1.27145	1.824025	0.3339033	2.664888	1.09261	16.439925
-1	-1	-1	1	1	1	-1	1.2583	1.82025	0.2263138	2.759238	1.0555675	16.270475

Pareto Chart of Chip 0b-5b Effects at 3V Vcc

(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Factor	Name
A	TEMP
B	HUMIDITY
C	AGE

Lenth's PSE = 2.29305

Pareto Chart of Chip 0b-5b Effects at 3V Vcc

(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Factor	Name
A	TEMP
B	HUMIDITY
C	AGE

Lenth's PSE = 1.85633

Pareto Chart of Chip 0b-5b Effects at 3V Vcc
(response is VIH, α = 0.05)

Pareto Chart of Chip 0b-5b Effects at 3V Vcc
(response is VIL, α = 0.05)

Pareto Chart of Chip 0b-5b Effects at 3V Vcc
(response is VOH, α = 0.05)

Pareto Chart of Chip 0b-5b Effects at 3V Vcc
(response is VOL, α = 0.05)

Pareto Chart of Chip 1b-6b Effects at 3V Vcc
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Pareto Chart of Chip 1b-6b Effects at 3V Vcc
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

109

Pareto Chart of Chip 1b-6b Effects at 3V Vcc
(response is VIH, α = 0.05)

Lenth's PSE = 0.0135656

Pareto Chart of Chip 1b-6b Effects at 3V Vcc
(response is VIL, α = 0.05)

Lenth's PSE = 0.00863437

110

Pareto Chart of Chip 1b-6b Effects at 3V Vcc
(response is VOH, α = 0.05)

Factor | Name
A | TEMP
B | HUMIDITY
C | AGE

Lenth's PSE = 0.0502978

Pareto Chart of Chip 1b-6b Effects at 3V Vcc
(response is VOL, α = 0.05)

Factor | Name
A | TEMP
B | HUMIDITY
C | AGE

Lenth's PSE = 0.00910603

Pareto Chart of Chip 2b-7b Effects at 3V Vcc
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Lenth's PSE = 3.55530

Pareto Chart of Chip 2b-7b Effects at 3V Vcc
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Lenth's PSE = 4.25242

Pareto Chart of Chip 2b-7b Effects at 3V Vcc
(response is VIH, α = 0.05)

0.01796

Factor	Name
A	TEMP
B	HUMIDITY
C	AGE

Lenth's PSE = 0.00477187

Pareto Chart of Chip 2b-7b Effects at 3V Vcc
(response is VIL, α = 0.05)

0.01768

Factor	Name
A	TEMP
B	HUMIDITY
C	AGE

Lenth's PSE = 0.00469687

Pareto Chart of Chip 2b-7b Effects at 3V Vcc
(response is VOH, α = 0.05)

Pareto Chart of Chip 2b-7b Effects at 3V Vcc
(response is VOL, α = 0.05)

Pareto Chart of Chip 3b-8b at 3V Vcc
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Lenth's PSE = 1.01689

Pareto Chart of Chip 3b-8b at 3V Vcc
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Lenth's PSE = 0.605681

Pareto Chart of Chip 3b-8b at 3V Vcc
(response is VIH, α = 0.05)

Lenth's PSE = 0.00404063

Pareto Chart of Chip 3b-8b at 3V Vcc
(response is VIL, α = 0.05)

Lenth's PSE = 0.0039375

Pareto Chart of Chip 3b-8b at 3V Vcc
(response is VOH, α = 0.05)

Pareto Chart of Chip 3b-8b at 3V Vcc
(response is VOL, α = 0.05)

Pareto Chart of Chip 4b-9b Effects at 3V Vcc
(response is POWER CONSUMPTION Ramp Down (mW), α = 0.05)

Lenth's PSE = 0.381978

Pareto Chart of Chip 4b-9b Effects at 3V Vcc
(response is POWER CONSUMPTION Ramp Up (mW), α = 0.05)

Lenth's PSE = 0.380597

Pareto Chart of Chip 4b-9b Effects at 3V Vcc
(response is VIH, α = 0.05)

Pareto Chart of Chip 4b-9b Effects at 3V Vcc
(response is VIL, α = 0.05)

Pareto Chart of Chip 4b-9b Effects at 3V Vcc
(response is VOH, α = 0.05)

Lenth's PSE = 0.0315009

Pareto Chart of Chip 4b-9b Effects at 3V Vcc
(response is VOL, α = 0.05)

Lenth's PSE = 0.0431003

Vcc Ramp Test of Chip 0b Comparing Constant VS. Normalized Load Values

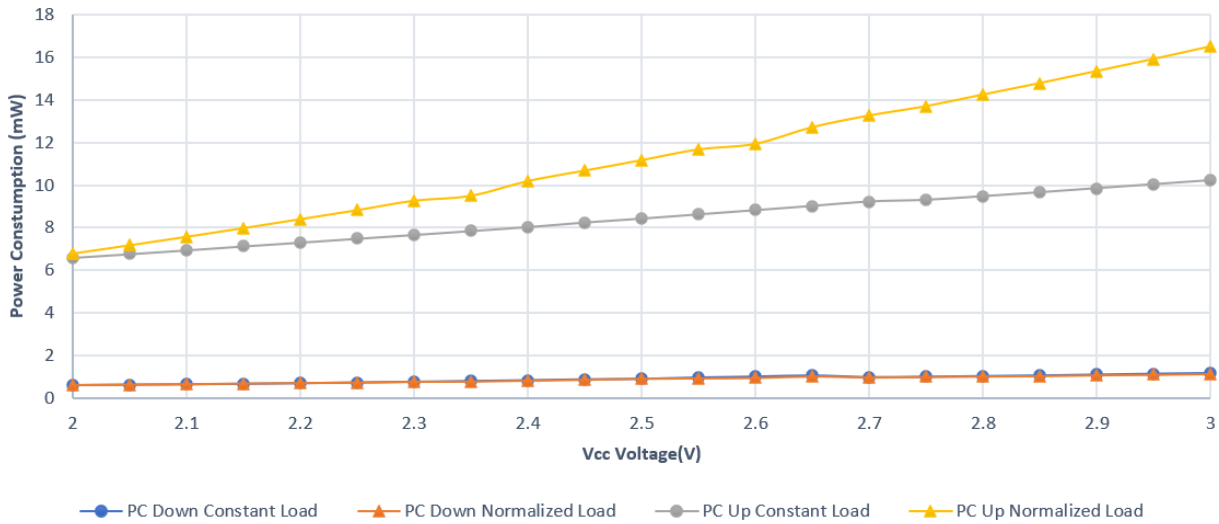# Vcc Ramp Test of Chip 0b Comparing Constant VS Normalized Load Values - PC
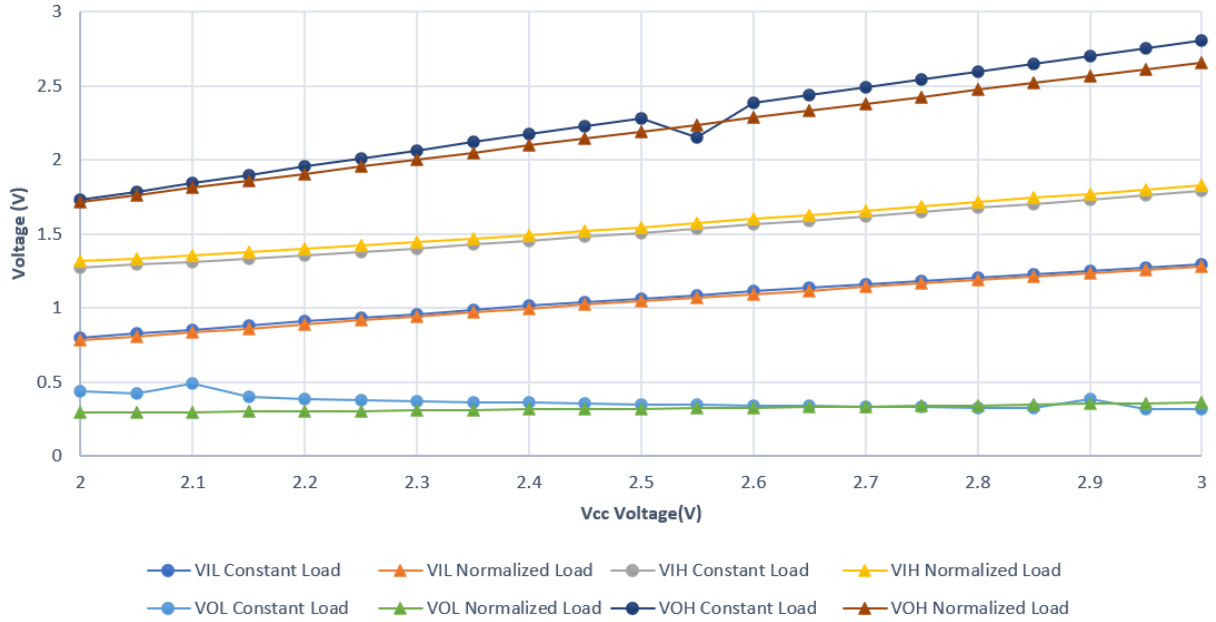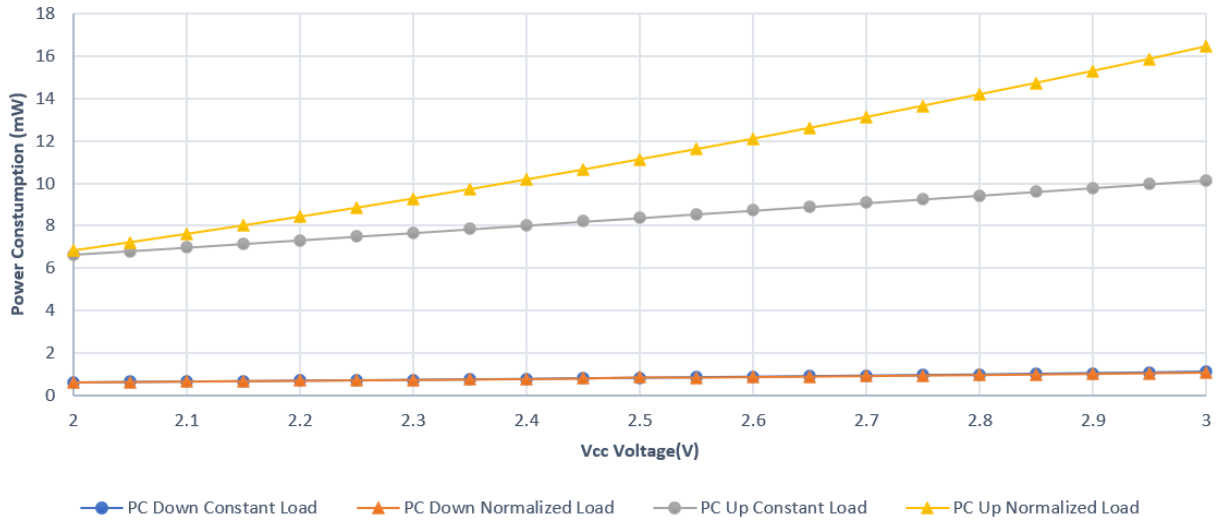
Vcc Ramp Test of Chip 1b Comparing Constant VS. Normalized Load Values

Vcc Ramp Test of Chip 1b Comparing Constant VS Normalized Load Values - PC

122

Vcc Ramp Test of Chip 2b Comparing Constant VS. Normalized Load Values

# Vcc Ramp Test of Chip 2b Comparing Constant VS Normalized Load Values - PC

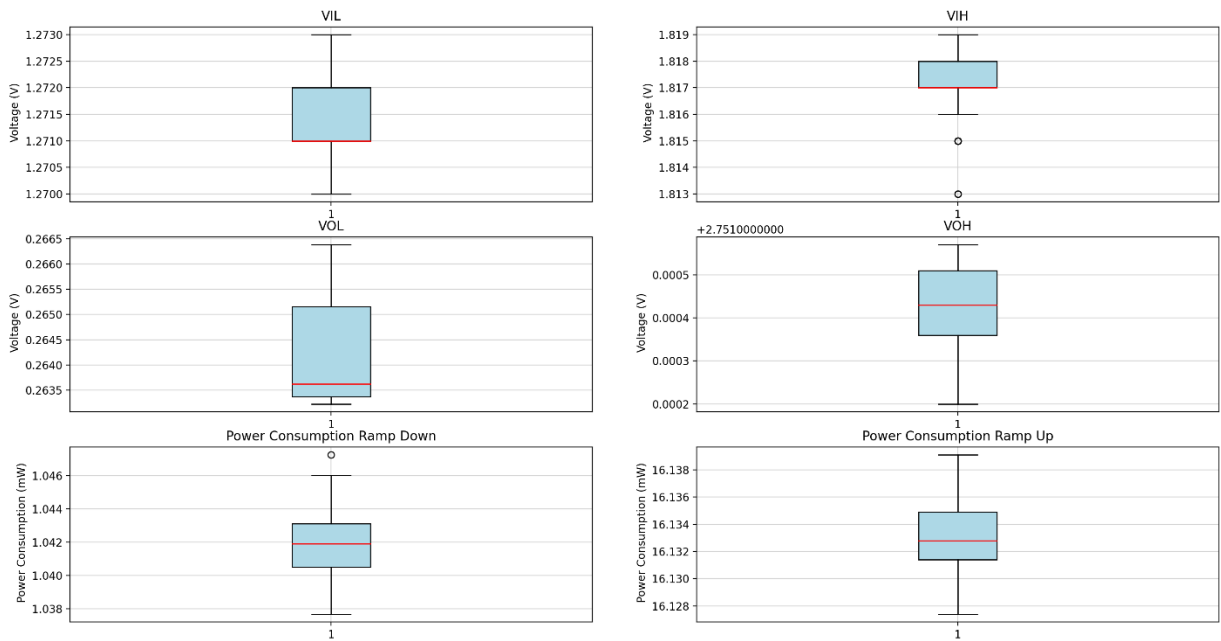# Vcc Ramp Test of Chip 3b Comparing Constant VS. Normalized Load Values

Vcc Ramp Test of Chip 3b Comparing Constant VS Normalized Load Values - PC

Vcc Ramp Test of Chip 4b Comparing Constant VS. Normalized Load Values

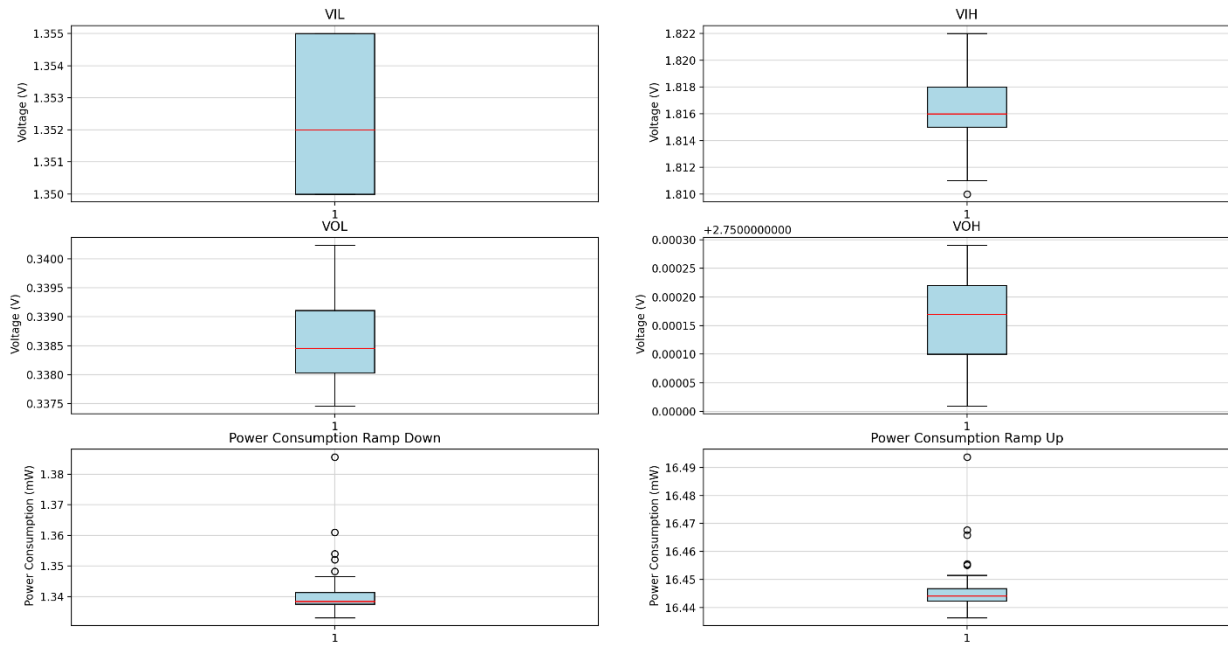## Vcc Ramp Test of Chip 4b Comparing Constant VS Normalized Load Values - PC

125

Vcc Ramp Test of Chip 5b Comparing Constant VS. Normalized Load Values

Vcc Ramp Test of Chip 5b Comparing Constant VS Normalized Load Values - PC

Vcc Ramp Test of Chip 6b Comparing Constant VS. Normalized Load Values
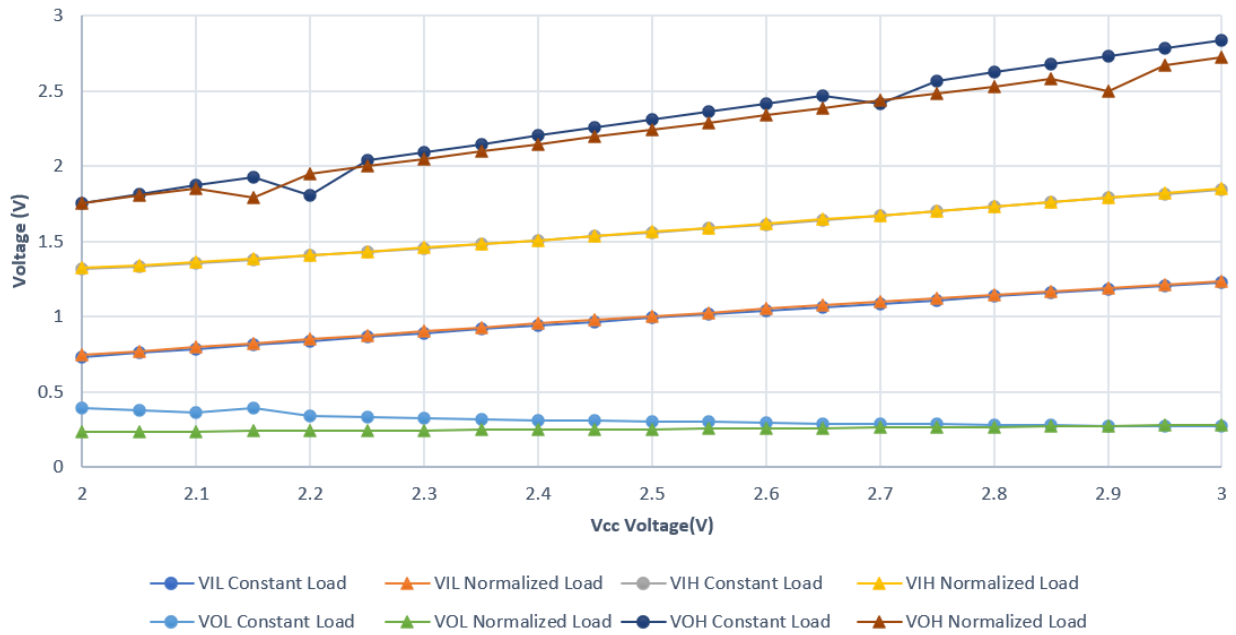
Vcc Ramp Test of Chip 0b Comparing Constant VS Normalized Load Values - PC

Vcc Ramp Test of Chip 7b Comparing Constant VS. Normalized Load Values
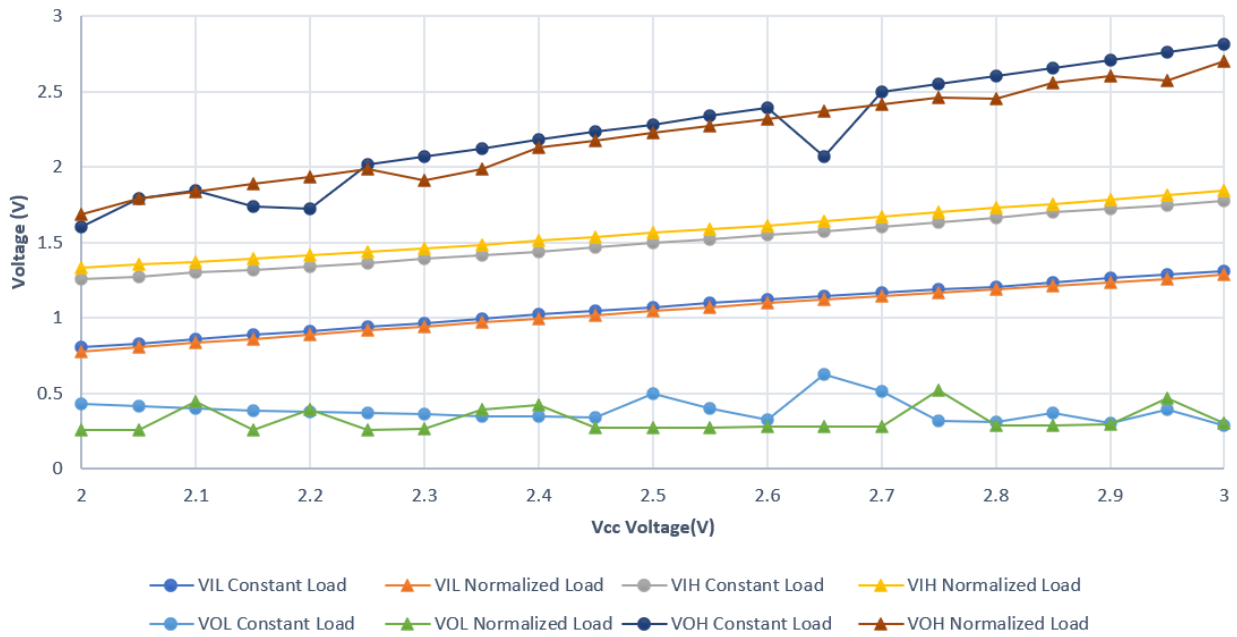
Vcc Ramp Test of Chip 7b Comparing Constant VS Normalized Load Values - PC
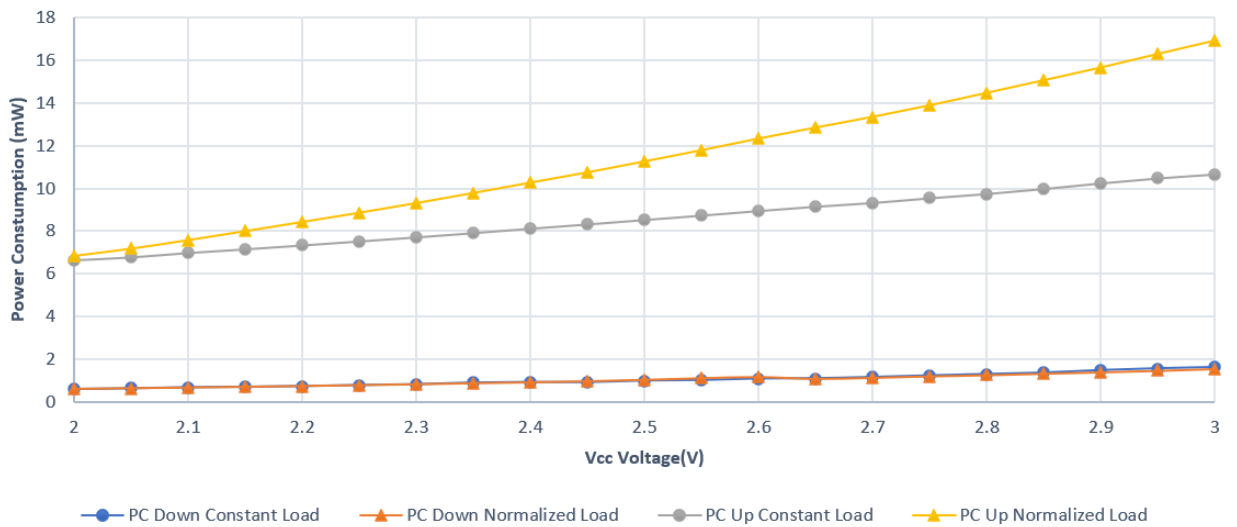
Vcc Ramp Test of Chip 8b Comparing Constant VS. Normalized Load Values
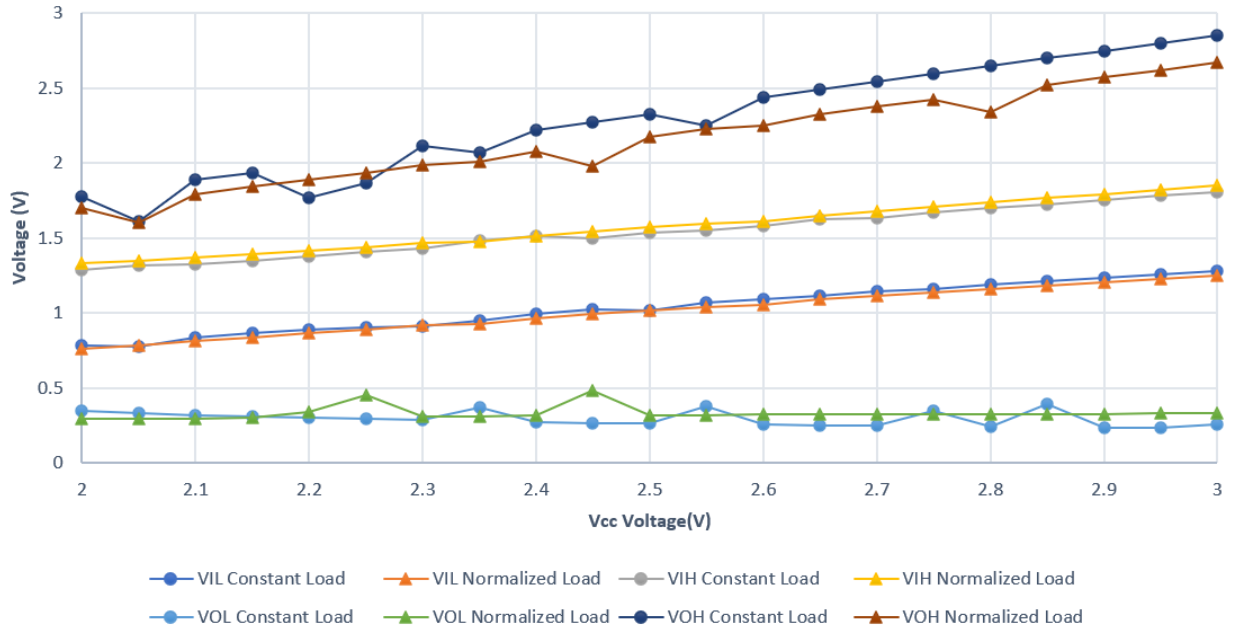
Vcc Ramp Test of Chip 8b Comparing Constant VS Normalized Load Values - PC

Vcc Ramp Test of Chip 9b Comparing Constant VS. Normalized Load Values

Vcc Ramp Test of Chip 9b Comparing Constant VS Normalized Load Values - PC

Data Variability for Chip 0b over 49 Test Runs

VIL

VIH

VOL

VOH

Power Consumption Ramp Down

Power Consumption Ramp Up
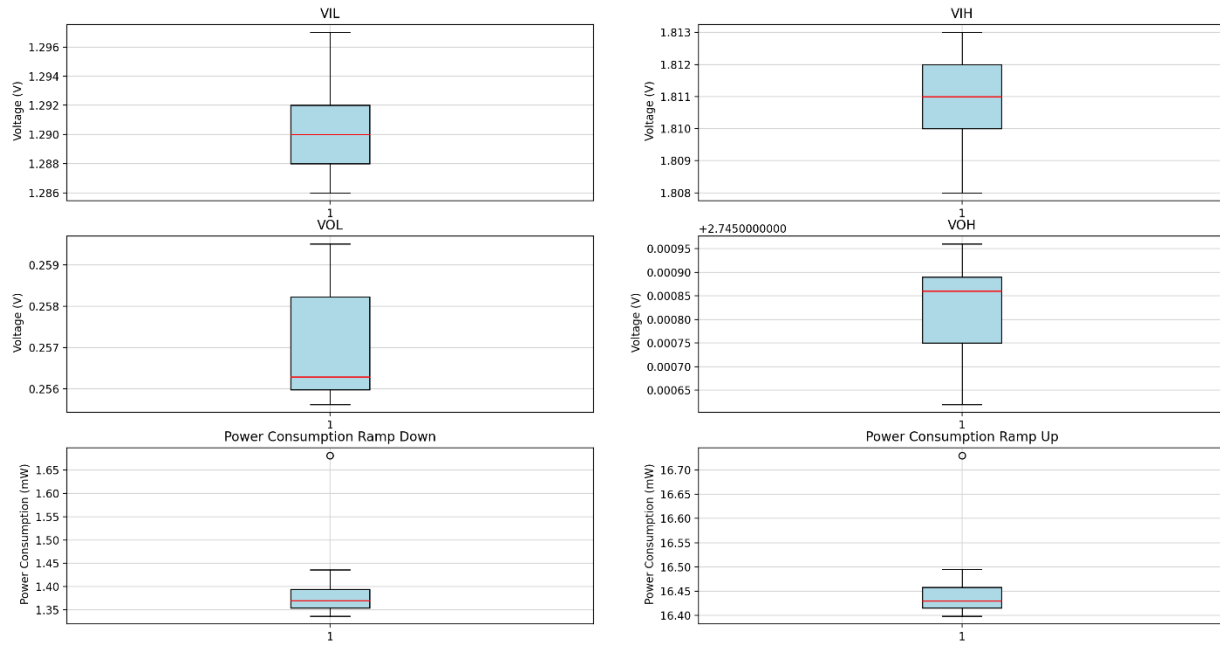
Data Variability for Chip 1b over 49 Test Runs

VIL

VIH

VOL

VOH

Power Consumption Ramp Down

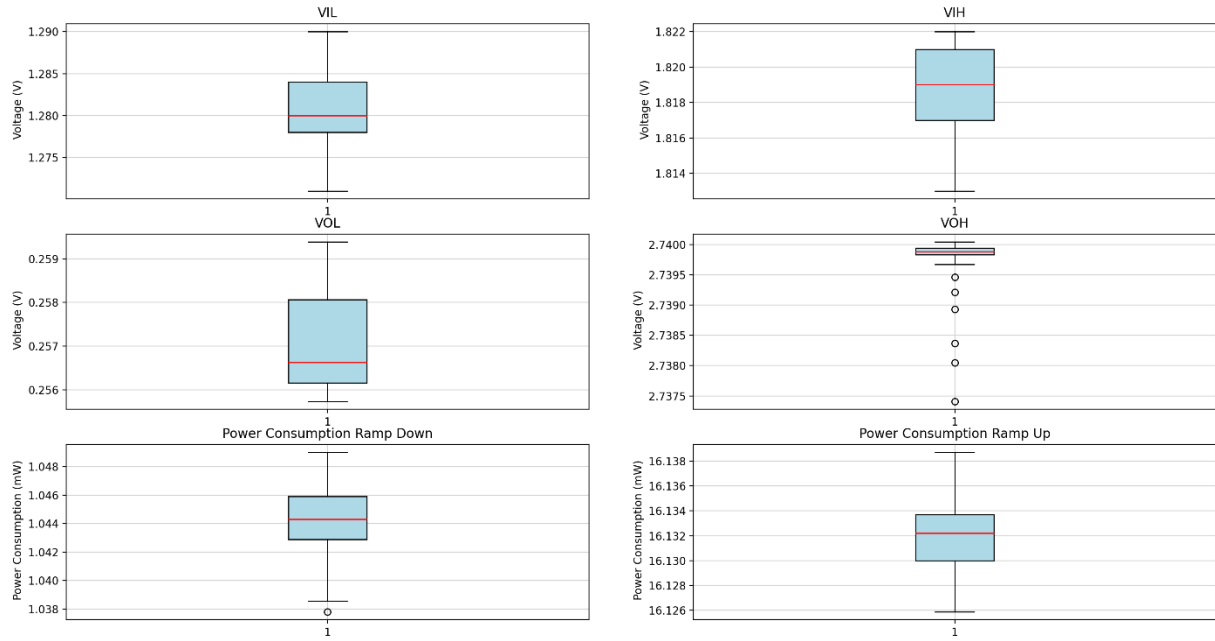Power Consumption Ramp Up

Data Variability for Chip 2b over 49 Test Runs

Data Variability for Chip 3b over 49 Test Runs
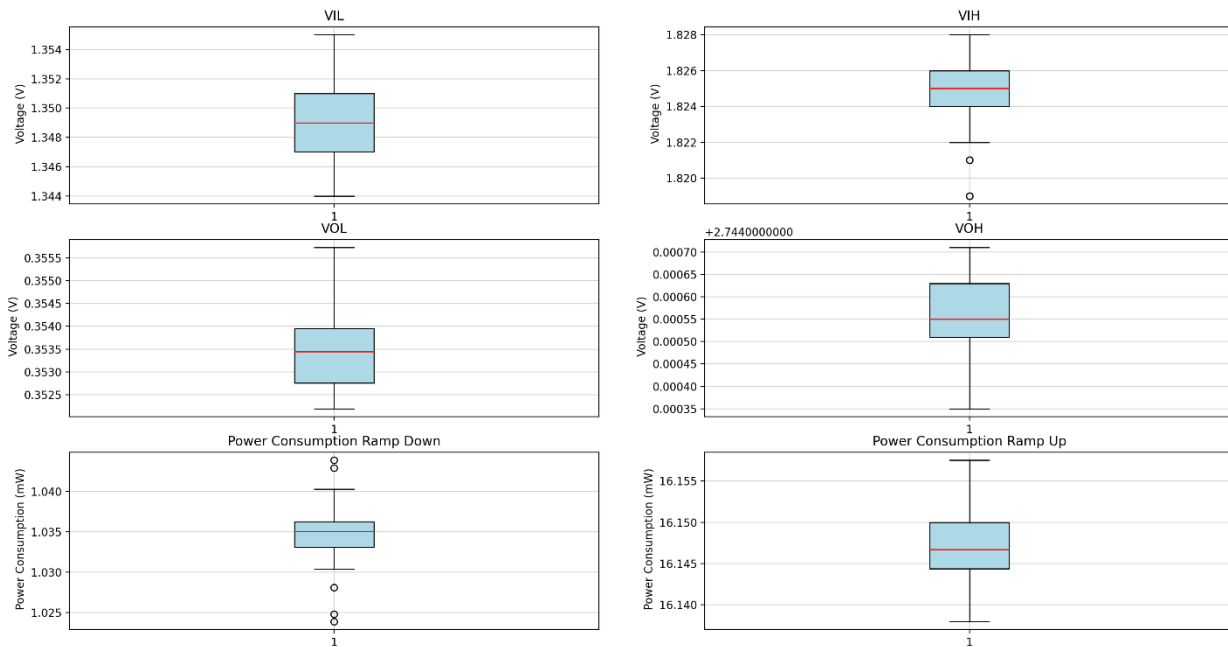
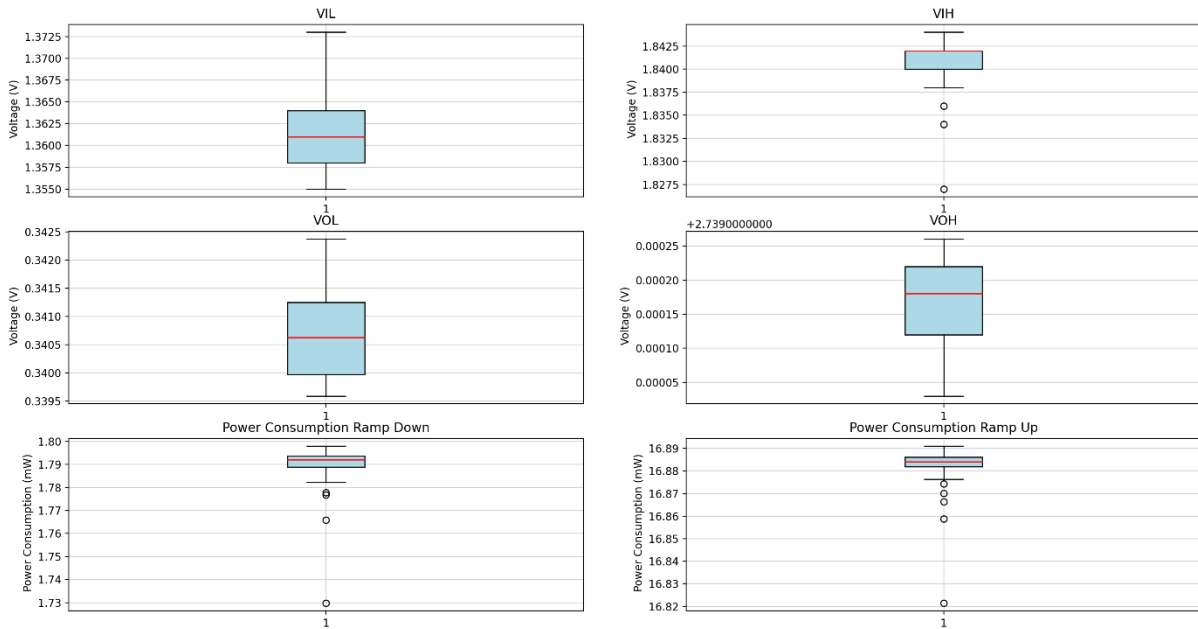Data Variability for Chip 4b over 49 Test Runs
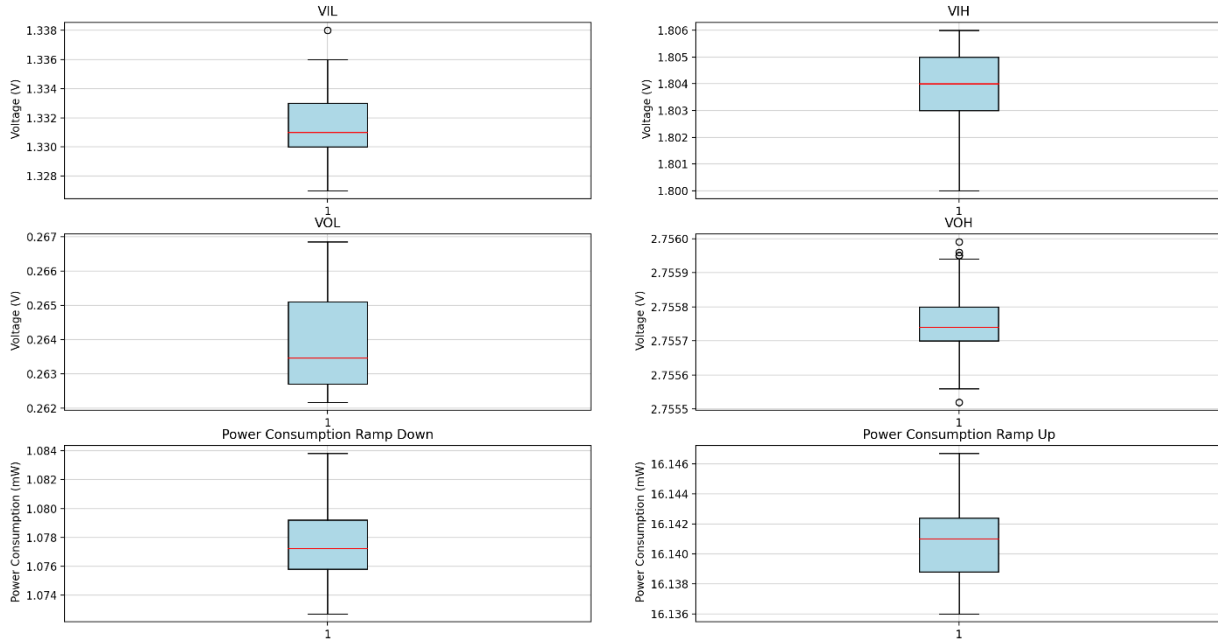
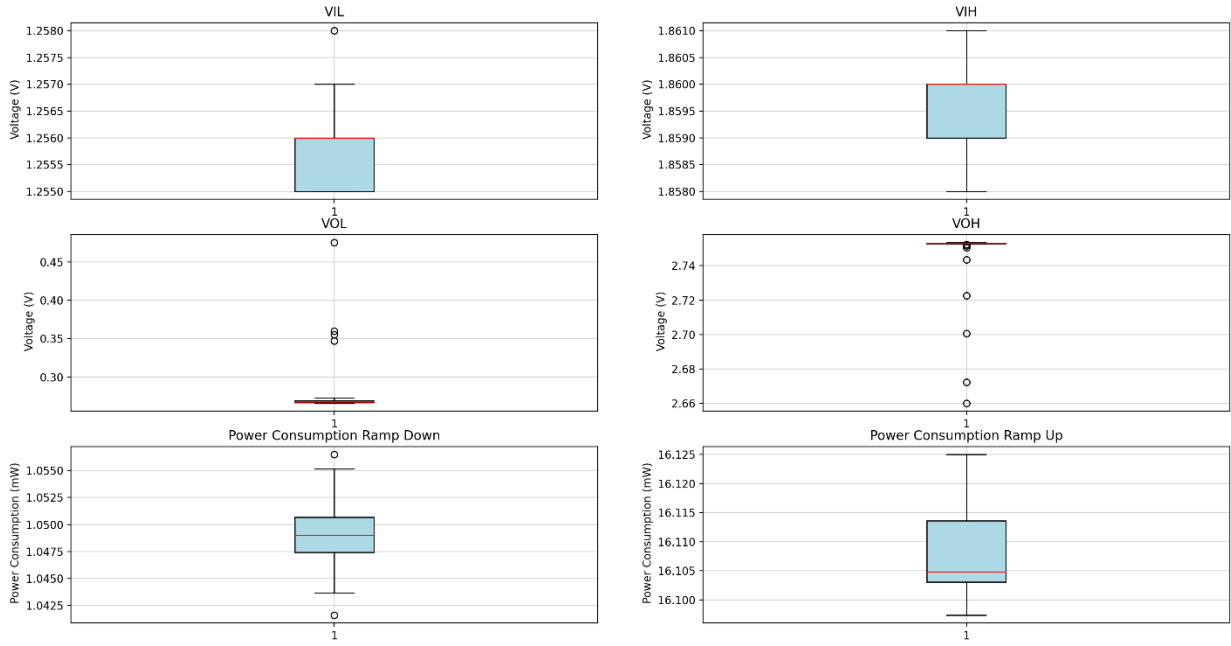Data Variability for Chip 5b over 49 Test Runs
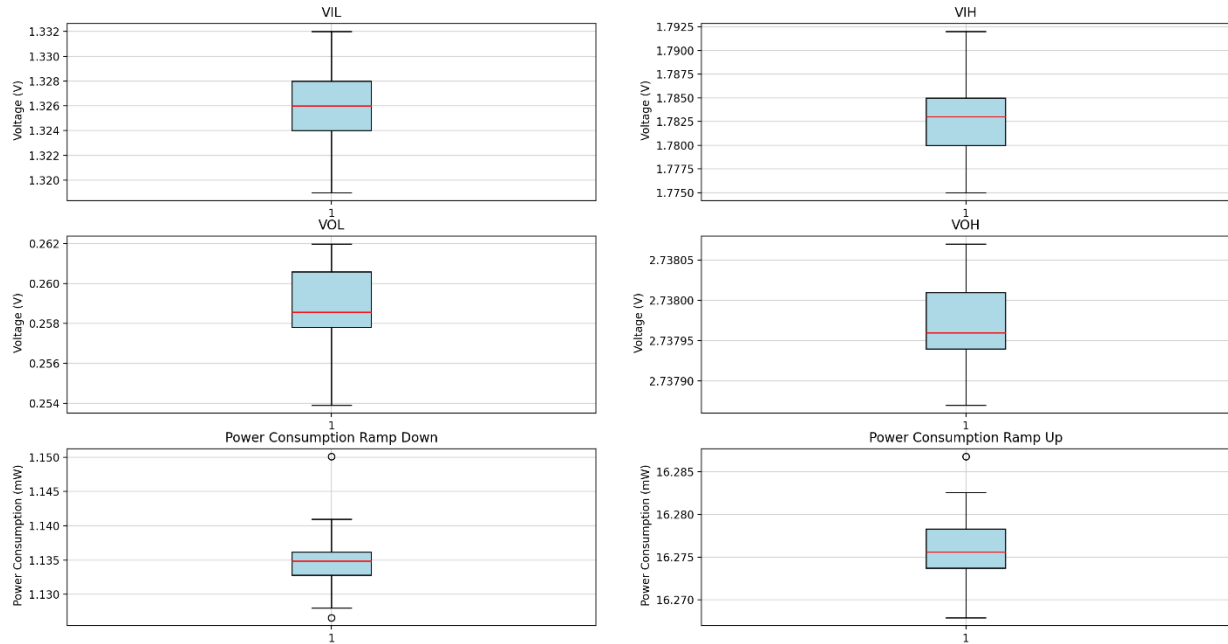
Data Variability for Chip 6b over 49 Test Runs

Data Variability for Chip 7b over 49 Test Runs

Data Variability for Chip 8b over 49 Test Runs

Data Variability for Chip 9b over 49 Test Runs