ULTRA-WIDEBAND LNA DESIGNS IN ADVANCED SIGE BICMOS TECHNOLOGY

A Thesis

by

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MASTER OF SCIENCE

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ABSTRACT

An ultra-wideband (UWB) mm-Wave low noise amplifier (LNA) suitable for use in high performance broadband wireless communication networks is proposed. The LNA is a key building block in any wireless receiver, and there is a growing demand for wireless networks to operate in the mm-Wave frequency range. Two LNA topologies are presented here. These are two stage LNA designs that are based on cascode and common emitter topologies. The key design techniques used to achieve low noise and wide bandwidth are resistive feedback, inductive emitter degeneration, gain staggering, and inductive peaking. The UWB LNA designs are implemented in an advanced SiGe BiCMOS process. The devices used in these designs are high performance heterojunction bipolar transistors (HBT) offered by this process. The LNA designs presented achieve a max 3 dB bandwidth of 23.8 GHz, minimum NF of 2.3 dB, peak gain of 24.8 dB, and maximum IIP3 of -3.4 dBm.

Also presented in this thesis is a proposed design strategy for a radiation-hardened (rad-hard) wideband LNA. It is well known that electronic devices suffer from performance degradation when exposed to significant levels of radiation. Radiation-hardening is the process of making electronics robust and resistant to the effects of radiation through fabrication or design techniques. The use of inversion mode (IM) devices will be presented as a means for designing a rad-hard wideband LNA.

DEDICATION

To my beautiful wife Cara, without whom I could not have completed this degree.

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1. INTRODUCTION

1.1 Motivation

Due to the ever-increasing demand for high performance and broadband wireless communication networks, there is a need for wide bandwidth receivers that operate at mm-Wave frequencies. A broadband mm-Wave receiver has multifunction applications such as 5G support, high data rate communications, military radar, and satellite communications. Future multi-function radios with ultra-wide instantaneous bandwidth have great potential to enable increases in wireless broad-band communications and the co-existence of radar and sensing systems. The integration offered with advanced CMOS and BiCMOS processes provides the potential for small form factor wideband RF systems in defense and space applications, provided these systems can achieve the necessary wideband performance.

The demand for higher data rates and inevitable spectrum crowding necessitates the need for RF systems to operate at higher frequencies. As a result, LNAs must be designed to operate at mm-Wave frequencies. There are many design challenges when it comes to broadband mm-Wave design, such as device parasitics that limit frequency range, unwanted coupling between components, higher power consumption, and higher noise figure (NF) at mm-Wave frequencies [9]. At mm-Wave frequencies, the devices in an LNA are operating much closer to their cutoff frequency resulting in reduced gain and increased noise figure. For this reason, ultra-wideband designs require multiple amplification stages in order to make up for the lower available gain at higher frequencies. This factor increases the power consumption and physical layout area relative to single stage narrow-band designs. The NF of the LNA is the most critical performance metric to consider when designing an LNA. Therefore, it is necessary to implement specific design

techniques, such as resistive feedback, emitter degeneration, and gain staggering, to achieve low noise figure and acceptable input matching over a wide range of frequencies.

1.2 System-Level Overview

The LNA is a key component found in almost any RF receiver system. The LNA is the first block in a typical receiver system, therefore its performance specs such as gain, linearity, and NF directly affect the system specs of a receiver such as sensitivity, dynamic range, and operating bandwidth. The LNAs job, therefore, is to amplify weak wireless signals without significantly degrading the signal to noise ratio (SNR). The SNR is defined as the ratio between the power of the desired signal and the power of the noise. The noise contribution of a system is defined by its noise factor (F) or noise figure (NF) in dB. Where the noise factor is defined as the ratio of the SNR at the input of the system to the SNR at the output of the system. The NF of the LNA sets the NF figure for the entire receiver system, and it is important to design the LNA to have sufficient gain to minimize the noise contributions of proceeding stages. This reality is described by Friis's equation (eq. 2).

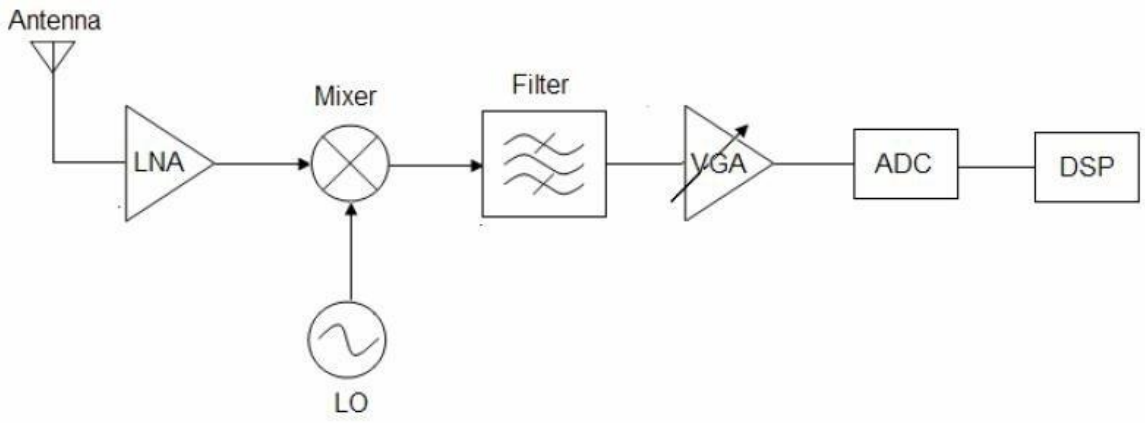

Figure 1. Typical RF Receiver Block Diagram

$$\mathrm{NF} = 10\,log\,\mathrm{F} \tag{1}$$

$$F = \frac{SNR_{in}}{SNR_{out}} = 1 + (F_{LNA} - 1) + \frac{F_{Mixer} - 1}{G_{LNA}} + \frac{F_{Filter} - 1}{G_{LNA}G_{Mixer}} + \cdots \tag{2}$$

As seen in equation 2, the noise figure of the LNA dominates that of the entire system, and the noise contributions of preceding stages are minimized by the gain of the stages before them. Therefore, a LNA needs to be designed to have the lowest noise figure possible, and ideally supply at least 20 dB of gain to reduce the noise contributions of the following stages by at least 2 orders of magnitude. A high performance wireless receiver system needs to be highly sensitive and be able to detect weak wireless signals. Therefore, it is critical to design an LNA with minimal noise contributions. To do this, the designer must implement specific and novel design techniques for low noise.

1.3 Literature Review

Since their conception, many UWB SiGe LNA designs have been proposed for operation in the mm-Wave frequency range. For example, in [3], a bandwidth of 6-18 GHz, NF from 2.7-3.8 dB, and peak gain of 16.3 dB was achieved using a two-stage cascode topology that employed resistive feedback on the first stage and inductive emitter degeneration for the input matching. In [7], a three-stage cascode LNA using inductive emitter degeneration was proposed. This design achieved an impressive operating bandwidth from 43-67 GHz and peak gain of 32.5 dB. However, this design suffered from poor NF and linearity (IP_{1dB}) of 6 dB and -38 dBm respectively. The design presented in [8] is a two-stage LNA using a differential cascode first stage with emitter degeneration and a single ended cascode second stage. Here, they achieved an impressive IP_{1dB} of -10 dBm due to the more complex differential topology, however, the bandwidth is relatively narrow at 23-30GHz. The design presented in [1] used a four-stage differential LNA topology to

achieve a bandwidth of 10-110GHz. While this bandwidth is impressive, the differential four-stage topology that was used has a power consumption of over 100 mW and a sub-optimal NF of 5.3 dB. A bandwidth of 22.2- 43GHz, gain of 21.1 dB, NF of 3.5-5.3 dB, and IIP3 of -3 dBm was achieved by [4], using a three-stage single ended to differential topology and magnetic coupling between gate and drain inductors to increase input impedance magnitude and bring optimum noise source impedance closer to the optimum power matching impedance. The design presented in [5] used a two-stage differential topology with a transformer based dual-tank matching technique for simultaneous noise and power matching. Here, they achieved a peak gain of 28.5 dB and a NF from 3.1-4.1 dB and a bandwidth from 29-37 GHz, while having a high-power consumption of 80mW.

The UWB LNA design presented in this work achieves a wide bandwidth of 23.8 GHz from 8.4-32.2 GHz. The proposed LNA has a greater bandwidth than most of the designs summarized in Table 1. The NF of the proposed LNA ranges from 2.3-3.2 dB across the operating bandwidth. The proposed LNA has the lowest NF compared to most of the designs in Table 1. Specifically, it has the lowest NF with an operating bandwidth greater than 20 GHz. The proposed LNA achieves a high IIP3 of -3.4 dBm, which is higher than all but one LNA design in Table 1, while also having a reasonable power consumption of 45mW compared to the other designs. The proposed LNA has a peak gain of 24.8 dB which is higher than or comparable to most the designs in Table 1.

Table 1. Recent UWB LNA Designs

Ref	Technology	BW (GHz)	Peak Gain (dB)	NF (dB)	IIP3 (dBm)	Pdc (mW)	FOM
[1]	90nm SiGe	10 - 110	25.5	4.8 – 5.3	x	192	NA
[2]	180nm SiGe	22 –32.5	18.6	4.5 – 5.5	-5.7	9	1.24
[3]	130nm SiGe	6 - 18	16.3	2.7 – 3.8	-5	32	6.8
[4]	28 nm CMOS	22.2 - 43	21.1	3.2 - 5.3	-3	22.3	29.2
[5]	250nm SiGe	29-37	28.5	3.1 – 4.1	-12.5	80	1.14
[6]	130nm SiGe	78	21.3	5.5	-4.5	52	NA
[7]	180nm SiGe	43 - 67	32.5	6	-28	11.7	0.43
[8]	130nm SiGe	23 - 30	25.3	2	-1	66	26
[9]	180nm SiGe	23 - 32	12	4.5 – 6.3	-6.3	13	2.5
This Work	**45nm SiGe**	**8.4 - 32.2**	**24.8**	**2.3 – 3.2**	**-3.4**	**45**	**32.7**

$$FOM = \frac{IIP_{3,av}[mW] * Gain\ [abs] * BW[GHz]}{Pdc[mW] * [F_{av} - 1]} * 10$$

1.4 Technology Overview

SiGe heterojunction bipolar transistor (HBT) technologies have effectively achieved high transistor performance that have allowed for applications in the mm-Wave regime where III-V materials such as GaAs and InP have previously dominated [19]. SiGe BiCMOS technologies achieve this high level of performance while also maintaining low-cost integration and fabrication with Si CMOS processes [13],[14]. This high level of integration allows for RF blocks to be integrated directly with CMOS digital blocks on the same die therefore achieving compact system-on-chip (SoC) designs. The advanced band-gap engineering employed in SiGe HBTs has dramatically increased the speed of these devices. The reported unity current gain frequency (f_T) and unity power gain frequency (f_{MAX}) for SiGe HBTs has surpassed 350 GHz and 500 GHz respectively [14],[20]. The increased scaling of HBT technologies to smaller and smaller nodes (sub-50nm) has decreased device paracitics, such as the base resistance (R_b), and has therefore allowed for a decreased minimum noise figure [19]. The superior f_T/f_{MAX} performance and low minimum NF of SiGe HBTs makes them ideal candidates for high performance UWB mm-Wave LNA designs [14].

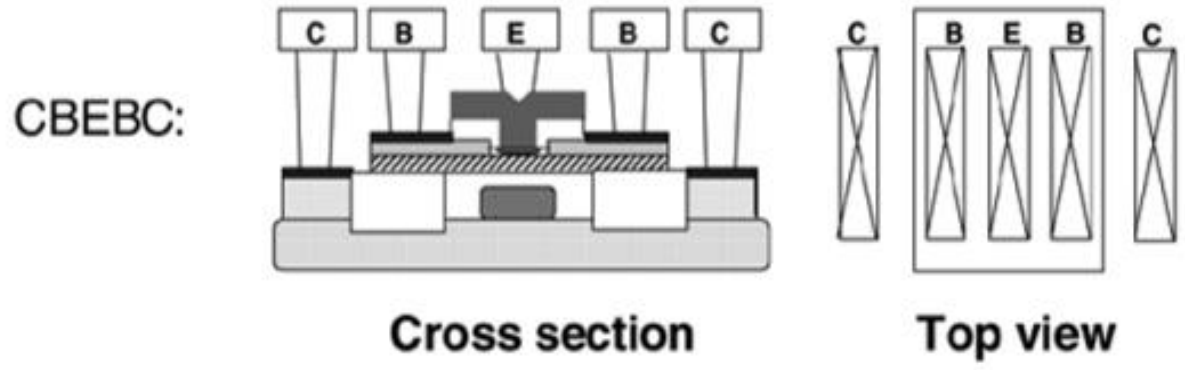

Figure 2. Cross Section of SiGe HBT [14]

Another benefit to SiGe HBT technologies is their ability to offer an adequate solution for SoC ICs that may be exposed to extreme environments [13],[21]. Research has shown that the unique band-gap properties of silicon-germanium make them a viable low-cost solution for robust electronics that may be exposed to very low temperatures, very high temperatures, or significant levels of radiation [21]. The SiGe HBT has been shown to be robust to total ionizing dose (TID) radiation exposure up to a few Mrads, without any Rad-Hard by Design (RHBD) techniques. This means that SiGe HBT technologies are by default Rad-Hard as fabricated [21]. However, these technologies are still susceptible to single event effects (SEE). Single event effects happen when a high energy particle interacts with a semiconductor lattice and can cause unwanted current and voltage transients at the terminals of a device. Specific RHBD techniques would have to be implemented to make these technologies robust to SEE.

The LNA designs presented in this thesis are fabricated in an advanced SiGe BiCMOS process. Included in this process are 10 metal layers with high-density and low-density MIM capacitors, spiral inductors, CPW, and micro strip line models that are used for interstage connections as well as emitter degeneration inductors.

1.5 Objective

The objective of this research is to develop high performance UWB mm-Wave LNA designs in an advanced SiGe BiCMOS process that target applications in the X, Ku, and K bands such as high-speed communications, military radar, satellite communications, and space. This thesis presents multiple design topologies that employ techniques such as inductive emitter degeneration, resistive feedback, gain staggering, and inductive peaking for UWB and low noise operation. The tradeoffs in gain, NF, bandwidth, and linearity between the two topologies will be presented.

As mentioned previously, SiGe HBTs are robust to TID radiation exposure. However, they are still susceptible to SEE. In this research, the use of inverse mode operation HBTs are presented as a strategy for mitigating SEE within a high frequency LNA circuit. The continued scaling of SiGe HBT technologies makes the reality of using inverse mode devices at mm-Wave frequencies possible. The work presented in section 4, will serve as an initial design approach and strategy for continued work to produce a RHBD mm-Wave LNA.

2. LNA THEORY

Some of the primary design considerations and performance metrics that describe a UWB LNA are as follows:

1. Noise Figure (NF)
2. Linearity (IIP3 and OIP3)
3. Input Matching (S_{11})
4. Stability

2.1 Noise Figure in mm-Wave amplifiers

Ideally, the objective of an LNA is to achieve a simultaneous input power match (S_{11}) and input noise match. In a wideband design, the optimum matching condition for minimum NF and the optimum matching condition for maximum power transfer do not occur at the same point. Therefore, it is important to analyze the tradeoff between the two [16]. The noise at the input of an amplifier is amplified by the gain of the amplifier and appears at the output. The noise sources generated within the amplifier propagate to its output and further degrade the SNR. The NF of an amplifier is described as the SNR at the input divided by the SNR at the output. The NF of an LNA can also be described using noise parameters (eq. 4). The noise generated by a transistor is a function of its source termination, where the source termination admittance is given by Y_s (eq. 3).

$$Y_s = G_s + jB_s \tag{3}$$

$$NF = NF_{min} + \frac{R_n}{G_s}\left|Y_s - Y_{s,opt}\right|^2 \tag{4}$$

Where G_s is the real part of the source admittance and B_s is the imaginary part. As seen from equation 4, the NF reaches a minimum when $Y_s = Y_{s,opt}$ leaving the $NF = NF_{min}$. R_n is referred to as the noise resistance, and it determines the sensitivity of the NF to deviations for Y_{opt}. To examine the effects of the transistor characteristics on the NF, the noise terms NF_{min}, $Y_{s,opt}$, and R_n need to be determined in terms of the device parameters. There are three primary noise sources within an HBT transistor: the base current shot noise, collector current shot noise, and the thermal noise from the base resistance r_b.

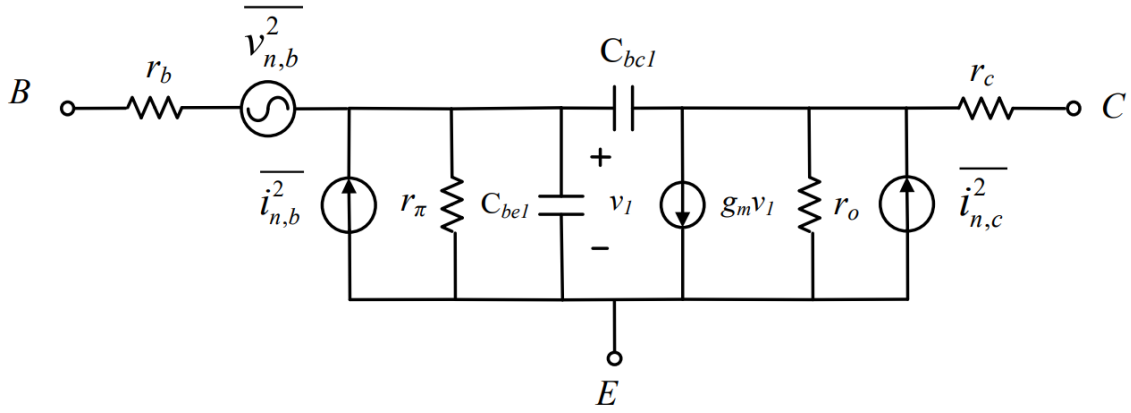

Figure 3. HBT Small Signal Model with Noise Sources

$$\overline{v_{n,b}^2} = 4kTr_b\Delta f \tag{5}$$

$$\overline{i_{n,b}^2} = 2qI_B\Delta f \tag{6}$$

$$\overline{i_{n,c}^2} = 2qI_c\Delta f \tag{7}$$

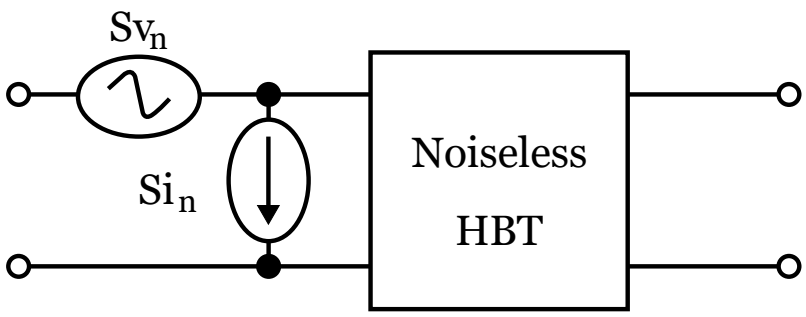

Figure 4. Spectral Density Equivalent

These noise sources can be converted to a spectral density equivalent model as depicted in Figure 4, where S_{vn} and S_{in} are the input voltage noise spectral density and input current noise spectral density respectively. The noise contributions from the collector resistance r_c and emitter resistance r_E are usually neglected from the noise model because they make a negligible contribution to the noise performance [22]. The equivalent current, voltage, and cross correlation noise spectral densities can be expressed in terms of device parameters as shown below.

$$S_{in} = 2qI_c\left[\frac{1}{\beta} + \left(\frac{\omega(C_{be}+C_{bc})^2}{gm}\right)\right] \tag{8}$$

$$S_{vn} = 4KT\left(r_B + \frac{1}{2gm}\right) \tag{9}$$

$$S_{invn^*} = 2KT\left[\frac{1}{\beta} + \left(\frac{j\omega(C_{be}+C_{bc})}{gm}\right)\right] \tag{10}$$

With this, the noise parameters R_n, $G_{s,opt}$, $B_{s,opt}$, and NF_{min} are calculated in terms of device parameters using the linear noisy two-port theory as described in [23].

$$R_n = r_B + \frac{1}{2gm} \tag{11}$$

$$G_{s,opt} = \sqrt{\frac{gm}{2R_n}\frac{1}{\beta} + \frac{\left(\omega(C_{be}+C_{bc})\right)^2}{2gmR_n}\left(1 - \frac{1}{2gmR_n}\right)} \tag{12}$$

$$B_{s,opt} = -\frac{\omega(C_{be} + C_{bc})}{2gmR_n} \tag{13}$$

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{\frac{2gmr_b+1}{\beta} + \frac{2\left(r_B+\frac{1}{2gm}\right)\left(\omega(C_{be}+C_{bc})\right)^2}{gm}} * \sqrt{1 - \frac{1}{2gmr_B+1}} \tag{14}$$

In most cases $g_m r_B >> 1$ so the NF_{min} equation can be further simplified.

$$NF_{min} = 1 + \frac{1}{\beta} + \sqrt{2g_m r_B} * \sqrt{\frac{1}{\beta} + \left(\frac{f}{f_t}\right)^2} \tag{15}$$

As seen from equation 14 and 15, a higher β, lower (C_{bc} + C_{be}) and a smaller r_B is desired to reduce the NF_{min}. Here β is the current gain of the device defined as I_C/I_B. C_{be} and C_{bc} are the base emitter and base collector parasitic capacitances respectively. Reducing these capacitances corresponds to an increase in f_t. From equation 15, the terms under the second square root become equal at $f = ft/\sqrt{\beta}$, thus, dividing the NF_{min} equation into two regions. At frequencies below $f = ft/\sqrt{\beta}$, the NF is independent of frequency and is dominated by the 1/β term and the r_B term. At frequencies above $f = ft/\sqrt{\beta}$, the NF_{min} scales linearly with the frequency, and the effect of β becomes less significant [22]. Therefore, maximizing f_t and minimizing r_B is necessary to improve the NF_{min}. For an advanced SiGe BiCMOS technology, the β can be around 1,500, and the f_t close to 300GHz. For a mm-Wave application the operating frequency is above $f = ft/\sqrt{\beta}$, meaning the f_t and r_B values will dominate the NF_{min} term.

2.2 Linearity

The linearity of an LNA is an important design aspect to consider as it defines the maximum allowable signal the amplifier can amplify without distortions. The LNA is the first block in the receiver chain, therefore it must be adequately linear to suppress interference. This is particularly a

concern in wideband designs, as more interferers will exist in the desired frequency band as opposed to more narrow band designs. Active devices in a LNA will exhibit some form of non-linearity. The linearity of an LNA is described by the 1 dB compression point denoted as P_{1dB} and the third order intercept point denoted as *IP3*.

The input P_{1dB} point is defined as the input power level in which the ideal linear gain of the amplifier is suppressed by 1 dB. The input (x(t)) and output (y(t)) of an amplifier is defined by equations 16, 17, and 18.

$$x(t) = Acos(\omega t) \tag{16}$$

$$y(t) = a_1 x(t) + a_2 x^2(t) + a_3 x^3(t) + \cdots \tag{17}$$

$$y(t) = \frac{a_2 A^2}{2} + \left(a_1 A + \frac{3a_3 A^3}{4}\right) cos\omega t + \frac{a_2 2}{2} cos2\omega t + \frac{a_3 A^3}{4} cos3\omega t \ldots \tag{18}$$

By substituting (16) into (17) we get (18) where the first term is a DC term, the second term is the fundamental, and the third and fourth terms are the second and third harmonics respectively. The input power level at which the gain is compressed by 1-dB is calculated by equation 19.

$$A_{in,1dB} = \sqrt{0.145 \left|\frac{a_1}{a_3}\right|} \tag{19}$$

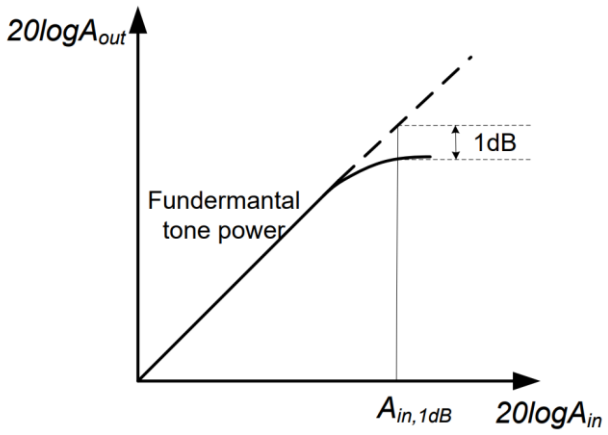

Figure 5. P_{1dB} Compression Point

Third order intermodulation distortion (IMD3) occurs when two interference signals are applied to a non-linear system and from intermodulation products that appear at frequencies close to the desired signal. This is problematic because the intermodulation products that appear close to the desired signal can be very difficult to filter out, and if their power levels are significant, they will severely distort the desired signal.

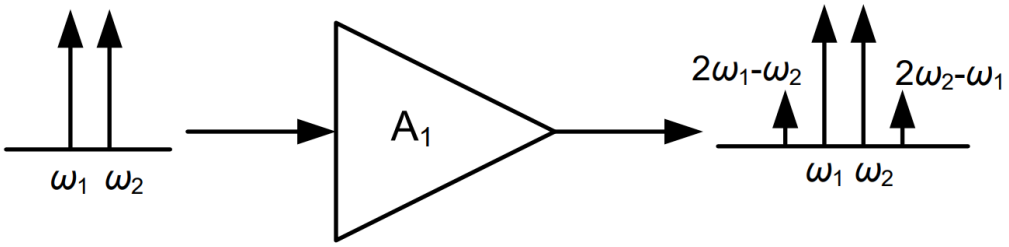

Figure 6. Intermodulation products

If the two-tone signal x(t) in equation 20 is applied to equation 17, then the intermodulation products (IMP) at $2\omega_1-\omega_2$ and $2\omega_2-\omega_1$ will form causing unwanted interference at the output of the amplifier.

$$x(t) = A_1 cos(\omega_1 t) + A_2 \cos(\omega_2 t) \tag{20}$$

$$IMP = \frac{3a_3 A_1^2 A_2}{4}\cos(2\omega_1 - \omega_2)\, t + \frac{3a_3 A_2^2 A_1}{4}\cos(2\omega_2 - \omega_1)\, t \tag{21}$$

The input third order intercept point (IIP3) is defined as the input power level where the fundamental tones amplitude is equal to the third order tones amplitude as depicted in Figure 7. However, this is a conceptual concept, due to the gain compression of a non-linear device, these amplitudes will never actually be equal. The IIP3 point is calculated by extrapolating the fundamental tones output with an imaginary line with a slope of 1, and the third order tones output with a slope of 3.

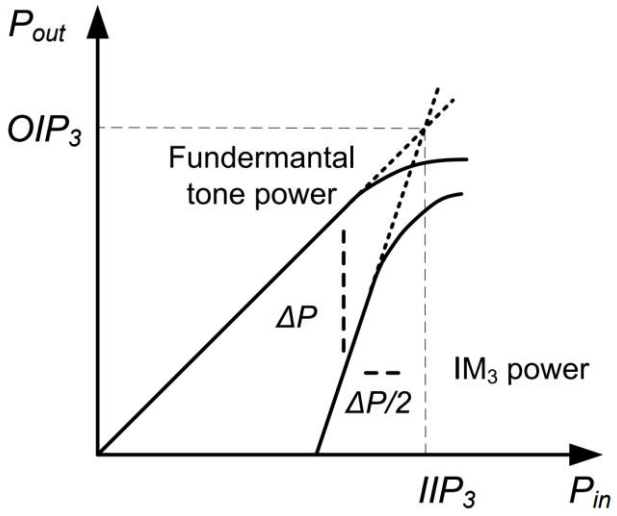

Figure 7. IIP3 Point

Here the IIP3 point can be calculated as

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|} \tag{22}$$

It is important to design an LNA with high linearity to suppress the a_3 term and maximize the IIP3 power level. The IIP3 point and the IP_{1dB} are roughly 10 dB apart from each other, where the IIP3 is 10 dB higher than the IP_{1dB}. The third order intermodulation point and the 1 dB compression point can also be described in terms of the output power. The OIP3 is the output power level at which the fundamental and third order harmonic are equal, and the OP_{1dB} is the output power level at which the gain is compressed by 1 dB.

2.3 Input Impedance Matching

In an RF system, input impedance matching is essential to obtain a maximum power transfer of a signal from the antenna to the input of the LNA. In a typical RF system, the antenna or band

pass filter is designed for a specific real load impedance of 50-Ω. A deviation in this 50-Ω load impedance seen by the antenna or band pass filter will cause significant signal reflections, losses, and voltage attenuations in the system. The input impedance matching is described as the reflected power divided by the incident power. This is called the input return loss (S_{11}) and is expressed in equation 23 where R_s is the source resistance (usually 50-Ω) and Z_{in} is the input impedance of the LNA. A S_{11} equal to -10 dB means that one-tenth of the signals power is reflected back to the source. In general, a S_{11} of -10 dB or less signifies an acceptable input match.

$$S_{11} = 20 \log \frac{Z_{in} - R_s}{Z_{in} - R_s} \tag{23}$$

Since the LNA is the first block in a receiver system, its input impedance must be designed to have a real part of 50-Ω while also having a low reactance or imaginary part. This is typically done by employing specific circuit topologies to introduce a real part into the input impedance that can be controlled with device parameters. A passive matching network is then added at the input to provide a conjugate match and cancel the reactive part of the devices input impedance. The simplest way to do this is to add a resistive termination at the input that is equal to 50-Ω, however, adding a resistive termination will significantly degrade the NF of the LNA due to the thermal noise

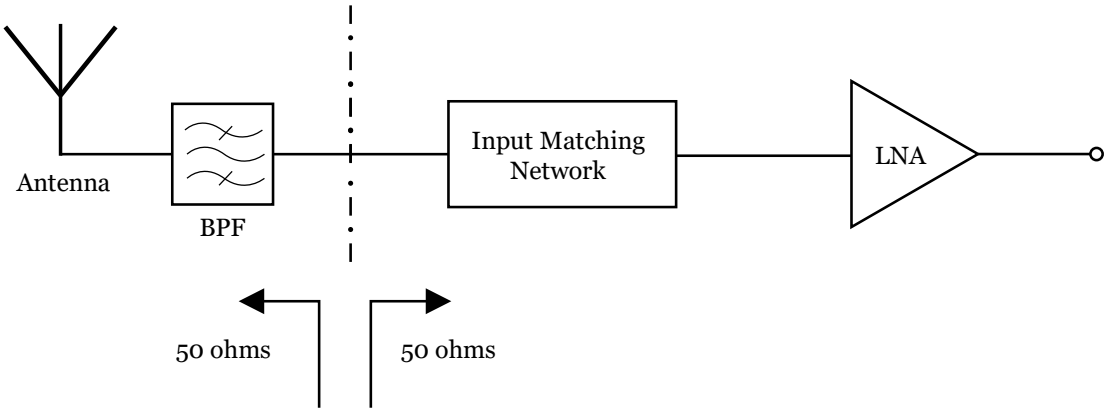

Figure 8. System Level Impedance Matching

contribution. Therefore, techniques must be implemented that use active devices and device parameters to set the real part of the input impedance.

One of the most widely used techniques for LNA input impedance matching is inductive emitter degeneration [3],[9],[16]. This technique is implemented by placing an inductive element from the emitter to ground, and therefore creates a real part in the input impedance.

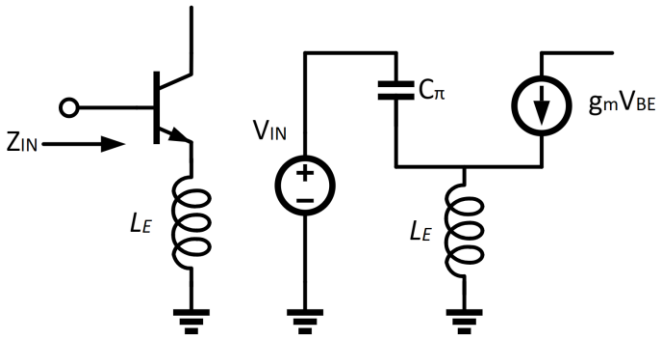

Figure 9. Small Signal Model

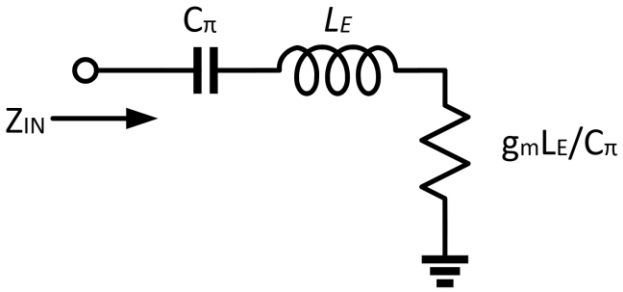

Figure 10. Equivalent Input Impedance

Here, the input impedance model can be simplified to what is shown in Figure 10, where L_E is the emitter degeneration inductor, and C_π is the base-emitter capacitance. By using KVL around the small signal equivalent model shown in Figure 9, the input impedance (Z_{in}) is calculated.

$$Z_{in}(s) = r_B + sL_E + \frac{1}{sC_\pi} + \frac{g_m L_E}{C_\pi} \tag{24}$$

$$Z_{in}(Real) = r_B + \frac{g_m L_E}{C_\pi} = r_B + \omega_T L_E \tag{25}$$

The real term here is dominated by $g_m L_E/C_\pi$ with a small contribution from r_B. From this, the designer can select L_E, g_m, and C_π to set this real part equal to 50-Ω and therefore achieve a real part in the input impedance without using an explicit resistor that would increase the thermal noise contributions. For an HBT device, the transit frequency (ω_T) is equal to g_m/C_π which appears in equation 24. This means the real part of the input impedance is roughly equal to $\omega_T L_E$ where ω_T is equal to $2\pi f_T$. Therefore, the input impedance is directly related to the f_T of the transistor. For technologies with f_T > 200 GHz a relatively small inductor of 20-50 pH can be used to realize a $\omega_T L_E$ = 50-Ω. At mm-Wave frequencies, this emitter degeneration inductor is typically realized using a micro-strip line. The use of micro-strip lines allows the Q of this inductor to be higher and take up less area relative to a spiral inductor. Having a high Q inductor at the emitter is important to limit the gain as little as possible. The use of an emitter inductor has also been shown to increase the linearity of an amplifier while also providing a low-noise solution for impedance matching [16].

2.4 Stability

For an LNA, it is important to be stable over all frequencies, for all source and load impedances. The LNA is a block in the receiver system that interacts with the "outside world" through its source impedance which is typically related to the antenna. Ideally, the antenna's impedance is designed to be 50 Ω. However, in a real application where the antenna is interacting with the outside environment, this impedance can change. Therefore, the LNA must remain stable even under these conditions. The LNA must be designed to be stable at all frequencies, even outside the operating bandwidth. If the LNA becomes unstable at a certain frequency, then its output will start to oscillate, and the LNA will become highly non-linear and significant gain compression will occur.

The parameter often used to define stability is called the Stern Stability Factor and is defined in equation 26.

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{21}||S_{12}|} \tag{26}$$

Here, Δ is defined as

$$\Delta = S_{11} * S_{22} - S_{12} * S_{21} \tag{27}$$

If *K* is greater than 1 and Δ is less than 1 for all frequencies, then the LNA is unconditionally stable, meaning it does not oscillate with any source or load impedances. A stricter way to check the stability is to also look at the *B* factor. The *B* factor is defined as

$$B = 1 + |S_{11}|^2 - |S_{22}|^2 - 2|\Delta|^2 \tag{28}$$

The circuit is unconditionally stable when *K* is greater than 1, and *B* is greater than 0 across all frequencies.

3. UWB SiGe LNA DESIGN

3.1 Transistor Sizing and Biasing

Each HBT in the presented designs are 0.1x10x 2 μm CBEBC devices. There are multiple performance considerations to take into account when choosing a device geometry, such as RF performance (f_{MAX}/f_T), noise performance, and linearity. Traditionally, HBT devices are configured in a CBE layout configuration; however, at mm-Wave frequencies the effects of parasitic resistances on NF and f_{MAX}/f_T become a much more significant, and other layout configurations need to be investigated for improved performance in these areas. The three device layout configurations offered are CBE, CBEB, and CBEBC. An example of these is shown in Figure 11.

The CBEBC layout configuration was chosen due to its superior noise performance and increased f_{MAX}/f_T over the CEBC, and CBE layout options. This increase in f_{MAX}/f_T is due to a decrease in the collector resistor (R_c) and base resistor (R_b) by having more collector and base fingers in parallel [14]. Shown in Figure 12 is the simulated f_{MAX} of a 10 μm emitter width HBT for the three different layout configurations.

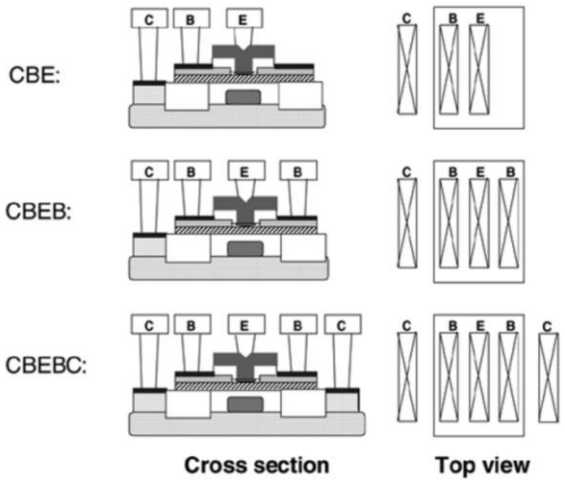

Figure 11. HBT Layout Configurations [14]

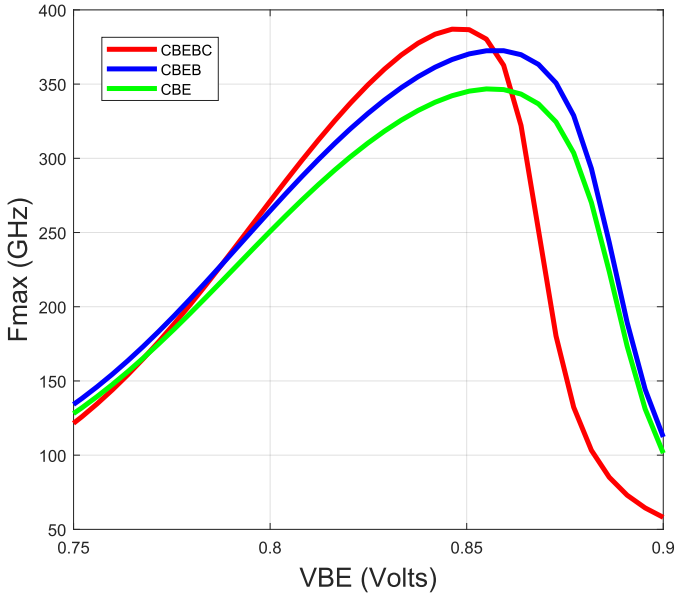

Figure 12. Simulated f_{max}

The CBEBC layout configuration also has the best noise performance when compared to the CBE and CBEB layout options. As seen from the previous discussion on noise in section 2, r_B has a direct impact on the NF_{min} of a device. Therefore, it is critical for SiGe technologies to move toward lower base resistance though process modifications, and to offer the designer ways to minimize this resistance through the physical layout [14]. The CBEBC layout configuration offers the best noise performance for similar reasons to what has been stated, having more base and collector fingers reduces r_B and r_C and therefore reduces their thermal noise contributions. It is also important to note that the biasing condition affects the noise contribution of a device. As seen in Figure 13, the NF is minimum at a particular current density or value of Ic. From this analysis, the bias current can be adjusted to minimize the NF without degrading the other performance metrics such as gain and linearity. Figure 13 shows NF_{min} plots versus I_C for the three layout configurations.

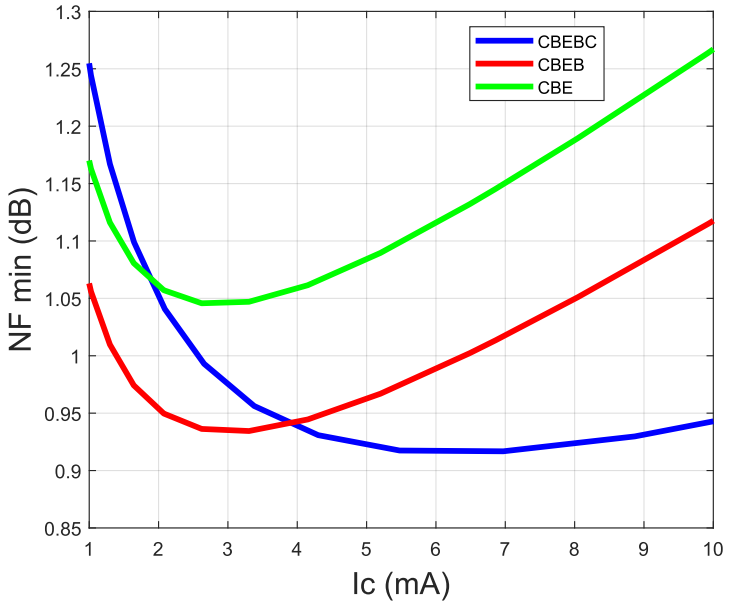

Figure 13. Simulated NF_{min}

Part of the design consideration for this LNA is having high linearity. On the device level, the size of the device and the biasing condition greatly affect the overall linearity of the device. This is due to the strong dependence of I_C and V_{CE} on the avalanche multiplication current and collector-base capacitance. Avalanche nonlinearity and collector-base capacitance nonlinearity are the two primary factors that limit the devices IIP3 and OIP3 [22]. To size the HBT device for maximum linearity, an analysis was performed where the OIP3 of a single device was plotted against the base-emitter voltage for different emitter lengths. For this process, the emitter width is permanently set at 0.1 µm, and the emitter length can be varied from 0.8 µm to 10 µm. The OIP3 simulation in Figure 13 was done using a two-tone analysis at frequencies of 20 GHz and 20.1 GHz. As seen from the results in Figure 14, a 10 µm emitter width device provides the best linearity at a base-emitter voltage of 809 mV.

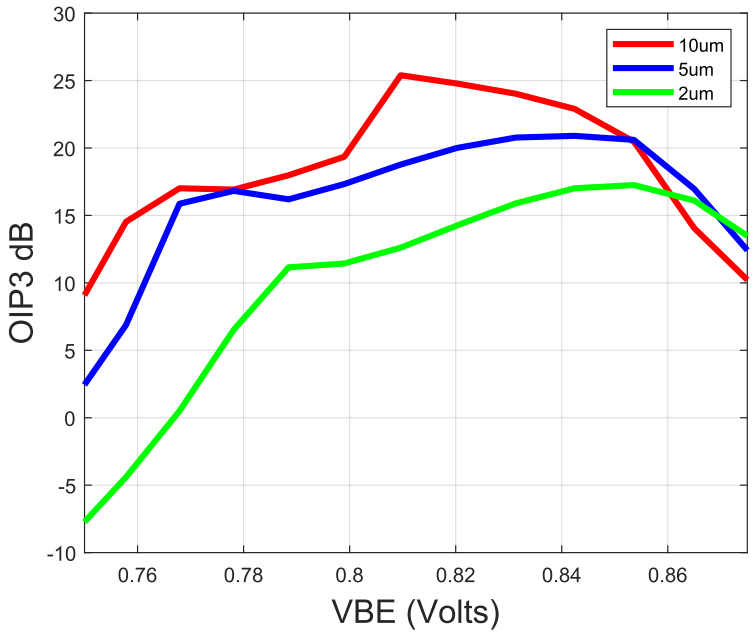

Figure 14. Simulated OIP3

3.2 Resistive Feedback

Resistive feedback is a technique that is employed to achieve wideband performance. Using resistive feedback has been shown to improve gain flatness, S_{11} bandwidth, stability, and linearity [10],[11],[17]. The designs presented in this thesis focus on exploiting resistive feedback specifically for gain flatness and wideband impedance matching. In traditional resistive feedback LNA designs, the feedback resistor R_f is used directly to match the input to 50 Ω by providing a dominant frequency invariant term in the input impedance [10],[11].

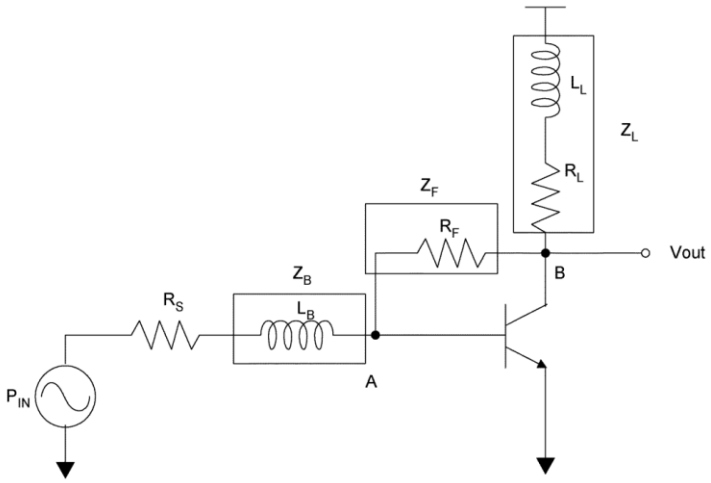

Figure 15. Resistive Feedback LNA [11]

$$Z_{in} = Z_B + (r_\pi || \frac{Z_F}{1 + g_m Z_L}) \tag{26}$$

For the simplified example shown in Figure 15, the feedback resistor R_f is seen as a miller equivalent resistance at the input equal to $R_f/(1-A_V)$ where Av is the open loop gain approximately equal to g_mZ_L. In this case, the $Z_f/(1+g_mZ_L)$ term primarily sets the input impedance and is made up of frequency invariant terms. However, the feedback resistor directly sets the input impedance, the 3 dB bandwidth, and noise performance for the LNA meaning there are not many degrees of freedom between these parameters [11].

In the presented designs, a combination of resistive feedback and inductive emitter degeneration is used to provide impedance matching and wideband performance. Traditionally, LNAs with inductive emitter degeneration can only achieve 50-Ω match over a narrow bandwidth but have proven to have low NF when compared to other architectures [10]. By employing a combination of resistive feedback and emitter degradation, LNAs with wide bandwidth and minimum noise performance can be achieved.

In a typical cascode LNA with emitter degeneration, the impedance looking into the base is given by equation 27 as discussed in section 2.

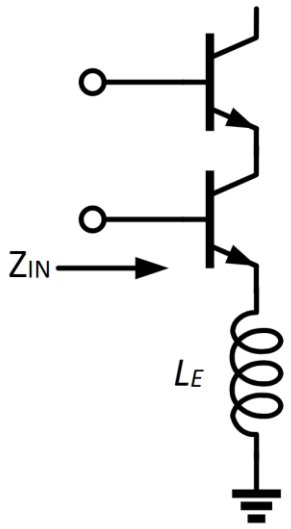

Figure 16. Cascode with Inductive degeneration

$$Z_{in}(s) = sL_E + \frac{1}{sC_\pi} + \frac{g_m L_E}{C_\pi} \tag{27}$$

Where L_E is the emitter inductor, C_π is the base emitter capacitance, and $g_m L_E/C_\pi$ is the real part that is generated by using inductive degeneration. The expression for the input bandwidth as function of the quality factor of the input network (Q_{in}) can be expressed as

$$BW_{in} = \frac{\omega_o}{Q_{in}} \tag{28}$$

Where ω_o represents the resonant frequency of the input network. From this, Q_{in} can be expressed as

$$Q_{in} = \frac{1}{C_\pi \omega_o (\frac{g_m L_E}{C_\pi} + R_s)} \tag{29}$$

By adding a feedback resistor R_f, the bandwidth is broadened. The introduction of R_f degrades the Q_{in} of the input network and therefore increases the bandwidth. This is seen by the inverse relationship of Q_{in} and bandwidth in equation 28. The feedback resistor does this without significantly degrading the NF of the LNA [17].

$$Q_{in(with\ feedback)} = \frac{1}{C_\pi \omega_o (\frac{g_m L_E}{C_\pi} + R_s + \frac{(\omega_o L_B)^2}{R_{fm}})} \quad (30)$$

With the addition of R_f, the Q_{in} can be expressed as seen in equation 30. Here, R_{fm} is the miller equivalent resistance seen at the input, and L_B is the inductor on the base used for conjugate impedance matching [17]. In this case, the input impedance is not directly set by R_f, but is primarily set by $g_m L_E/C_\pi$ making the input impedance less dependent on R_f. This means a larger range of values can be acceptable for R_f while not significantly altering the input impedance or NF. This solution offers more degrees of freedom in designing the LNA.

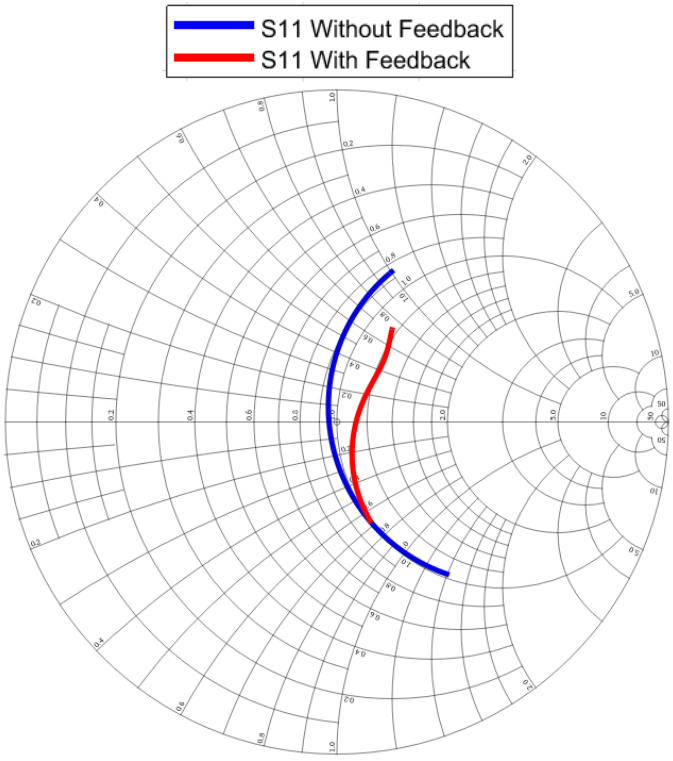

Figure 17. S_{11} With and Without Feedback

To demonstrate this, a simple one stage cascode LNA was simulated with and without resistive feedback to show the differences in the input matching. Figure 17 shows the S_{11} curves plotted on a smith chart from 15 to 30 GHz where R_f= 800 Ω. As can be seen in Figure 17, the S_{11}

curve of the LNA with feedback has values which are much closer to the center of the smith chart (50-Ω) over the same frequency range causing a wider input impedance match. Using resistive feedback also provides the benefit of flattening the gain over a wide range of frequencies. Other parameters of the LNA such as gain, noise, and input impedance are not very sensitive to R_f [10]. This means a larger value of R_f can be used without significantly affecting the other important LNA parameters.

3.3 Gain Staggering

It is common for UWB LNAs to have multiple amplifier stages to achieve high gain, but multi-stage designs are also necessary to realize wide bandwidth operation [9],[18]. For this reason, UWB designs typically have much higher power consumption over narrow band designs. This is a reasonable trade-off to achieve wide bandwidth. This technique is referred to as gain staggering. Each amplifier stage by itself may have a narrow band characteristic. By arranging the resonant peaks of each amplifier stage at different frequencies across the band, a combined wideband response is achieved. For example, if the first amplifier stage has a resonant peak at a lower frequency and is cascaded with a second amplifier stage that has a resonant peak at a higher frequency, the combined gain response will be wide and flat.

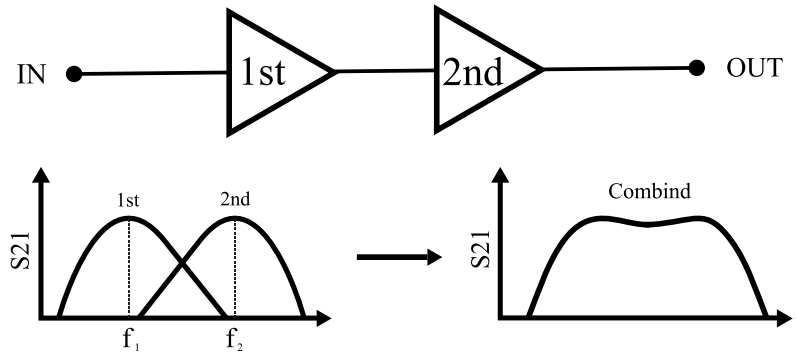

Figure 18. Gain Staggering

3.4 Topology Tradeoffs

The LNA topology is an important consideration in the design process as it determines the various performance limitations and trade-offs that come with each configuration. The most common types of LNAs are common-emitter (CE), common-base (CB), and cascode topologies. Two LNA topology variations are presented in this thesis. The first is a two-stage LNA with a cascode first stage and a cascode second stage both using resistive feedback and inductive emitter degeneration. The second is a two-stage LNA with a cascode first stage and a common-emitter second stage both using resistive feedback and inductive emitter degeneration. This section will analyze the performance advantages, disadvantages, and trade-offs between the common-emitter and cascode topologies.

The common-emitter topology is the simplest amplifier stage that can be implemented. However, it has some performance drawbacks especially for mm-Wave designs such as reduced bandwidth, low reverse isolation, instability, and low gain when compared to the cascode topology. The cascode topology is considered because of its ability to improve upon the draw backs of the simple common-emitter topology. The cascode topology has a significant improvement in reverse isolation over a CE stage. This increased isolation between the input and output makes for easier input and output impedance matching because the impedance seen at the input is less dependent on the impedance at the output and vice versa. Therefore, there is less design complexity for impedance matching using cascode stages [16]. One of the most significant issues of the CE topology is the degradation in its bandwidth due to the miller effect on the base collector capacitance (C_{BC}). The cascode topology greatly suppresses this miller effect and can achieve a higher bandwidth over the CE topology. This factor is especially important for wide-band designs as any technique to widen the bandwidth is an important consideration. The high reverse isolation characteristic of the cascode

topology also improves its stability when compared to a CE stage. Additionally, the cascode topology has an increase in gain over the CE stage. However, the cascode stage does require a higher voltage headroom when compared to a CE stage due to the stacked transistor configuration, and thus has a reduced output swing. This means that the CE stage has an improved linearity performance over the cascode topology because it requires less voltage headroom and can achieve a higher output swing.

To demonstrate these tradeoffs, two simple single-stage LNAs were designed and simulated to show the performance differences between a cascode stage and a common emitter stage both using resistive feedback and inductive emitter degeneration. Between the two designs, everything was kept the same except for the addition of the stacked transistor in the cascode design.

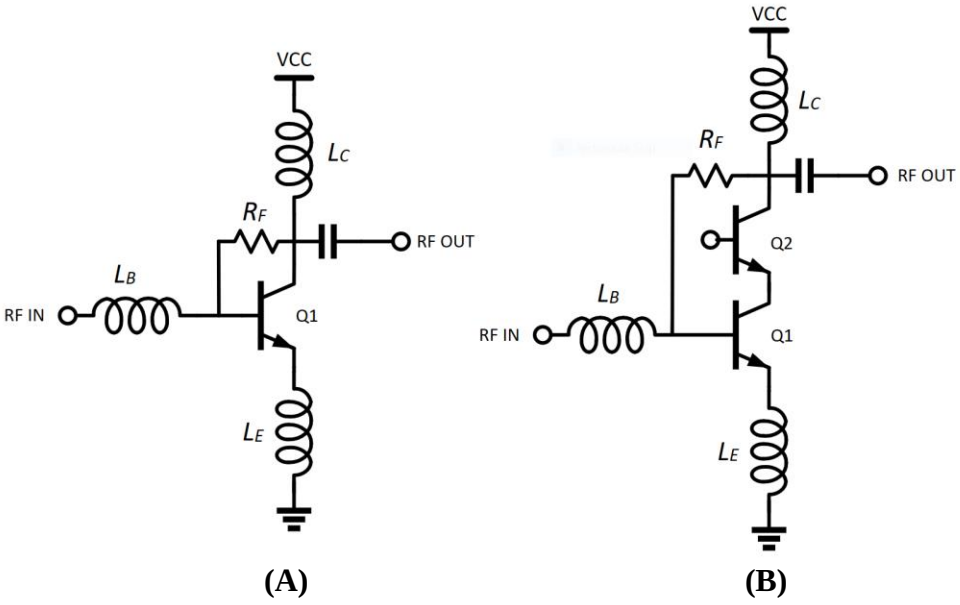

Figure 19. Common Emitter (A) and Cascode Stage (B)

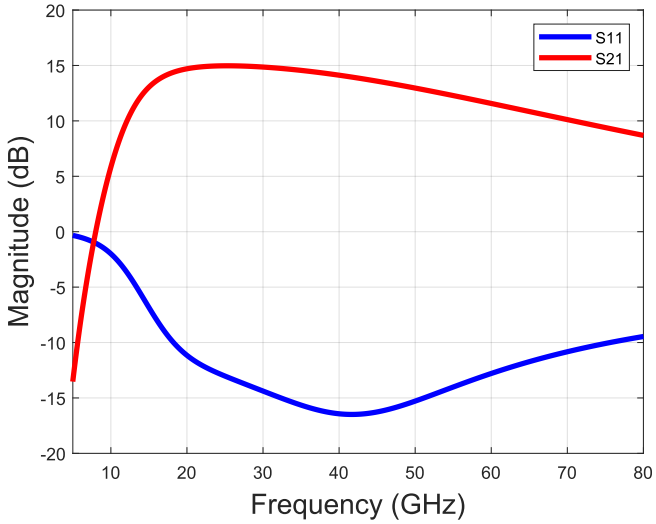

Figure 20. Cascode Stage S21, S11

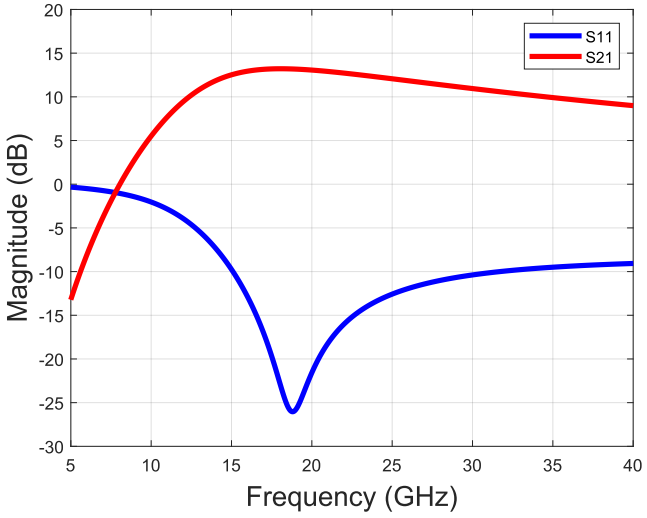

Figure 21. Common Emitter Stage S21, S11

As seen from Figure 21, the CE LNA has a much narrower S_{21} gain and bandwidth when compared to the cascode LNAs S_{21} gain in Figure 20. This is due to the suppression of the miller effect in the cascode LNA. The range of the S_{11} below -10 dB for the CE LNA is from 15-30 GHz. With the addition of the stacked transistor, the range of S_{11} below -10 dB dramatically increased from 15-30 GHz to 18-75 GHz. This demonstrates the increase in isolation of the input impedance

to the output impedance. The simulated OIP3 and IIP3 of the CE LNA are 25 dBm and 11.9 dBm respectively, and the OIP3 and IIP3 of the cascode LNA are 20.8 dBm and 5.8 dBm respectively. This shows a significant increase in linearity when looking at the CE LNA over the cacsode LNA. A 6.1 dBm increase in IIP3 is seen when using the CE LNA. In terms of NF performance, the two LNAs are very similar. The cascode LNA has a negligibly higher NF over the CE LNA.

From this analysis, two UWB LNA topologies will be investigated. One with two cascode stages that target high bandwidth and high gain, and one with a cascode first stage and common-emitter second stage that target high linearity.

3.5 Ultra-Wideband CAS-CAS LNA

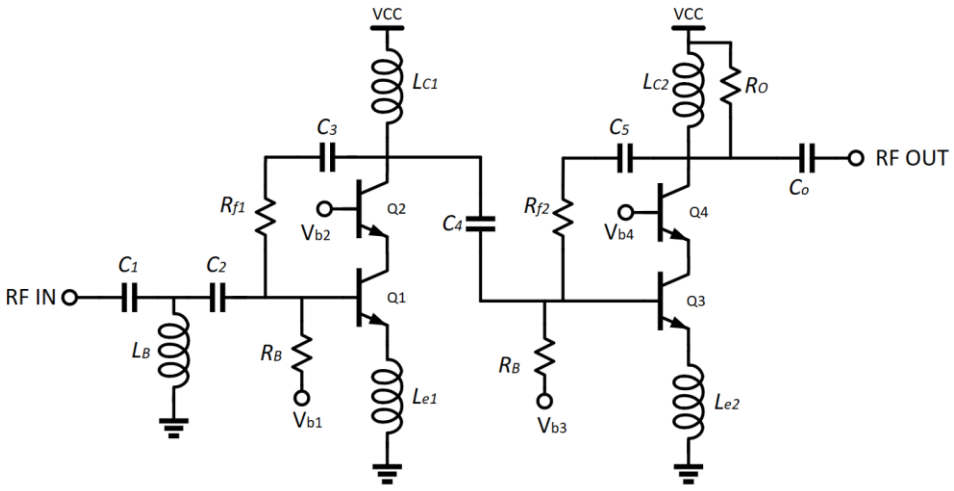

Figure 22. CAS-CAS LNA Schematic

Table 2. CAS-CAS LNA Components

L_B	Le1	Lc1	Le2	Lc2	Ro	R_{f1}	Q_1, Q_2
350pH	30pH	145pH	50pH	400pH	40 Ω	450 Ω	0.1x10x2 µm
C1	**C2**	**C3, C5**	**C4**	**Co**	**Rb**	R_{f2}	Q_3, Q_4
3pF	2pF	100fF	2pF	5pF	5k Ω	500 Ω	0.1x10x2 µm

The schematic of the first proposed LNA is shown in Figure 22, where stacked transistors Q1 and Q2 make up the first cascode stage and Q3 and Q4 make up the second cascode stage. Both stages use the resistive feedback technique for wideband impedance matching and wideband gain flatness. Both stages also use emitter degeneration inductors L_{e1} and L_{e2}. For the input stage, L_{e1} is used to set the real part of the input impedance equal to 50-Ω, while L_{e2} is used at the second stage to improve the linearity of the LNA. For this design, the cascode topology is adopted for its wideband performance, high gain, and superior input and output isolation. The collector inductors L_{c1} and L_{c2} are used for inductive peaking. The value of these inductors are selected so that the resonant peaks of each stage occur at the upper and lower frequencies of the operating band, and therefore achieve a wide bandwidth.

3.6 Wideband Impedance Matching

The small signal equivalent model for the input of the proposed LNA can be shown as in Figure 23.

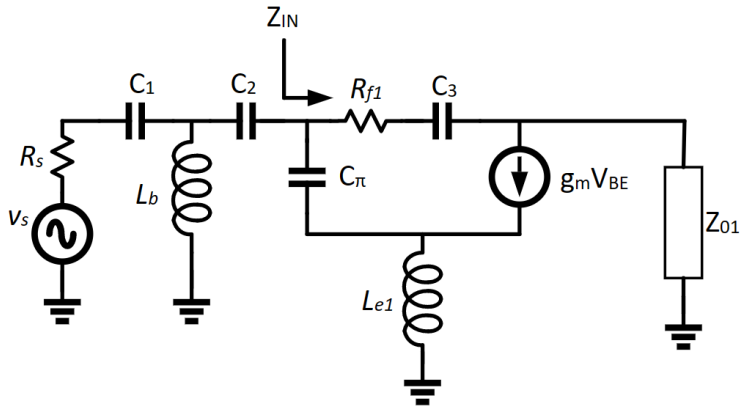

Figure 23. Small Signal Model

For simplicity, r_B, r_π, and r_o are neglected from the small signal model. Components C_1, C_2, and L_b make up the input matching network where L_b is used to resonate with the parasitic capacitances seen at the input of the device. R_{f1} and C_3 form the feedback path from the output of the first stage back to the input. Here, C_3 is used as a DC blocking capacitor. Z_{o1} is the output impedance seen at the output of transistor Q_1, and L_{e1} is the emitter degeneration inductor of the first stage. The impedance looking into the base of Q_1 can be expressed as

$$Z_{in}(s) = 1/\left[\frac{sC_\pi(Z_{o1}+sL_{e1})}{sL_{e1}Z_{o1}(g_{m1}+sC_\pi)+Z_{o1}+sL_{e1}}+\frac{sC_3}{1+sC_3R_{f1}}\right] \quad (31)$$

The output impedance of Q_1 can be expressed as

$$Z_{o1} = sL_{C1} \,||\, \frac{1}{sC_{out}} \,||Z_{o2} \quad (32)$$

Where L_{C1} is the collector inductor of the first stage, C_{out} is the parasitic capacitance of the output stage, and Z_{o2} is the output impedance of the Q_2 transistor. The expression of Z_{in} can be simplified if the assumption is made that $Z_{o1} >> sL_{e1}$ and $g_{m1}Z_{o1} >> 1$. The simplified expression of Z_{in} is shown as

$$Z_{in}(s) = \left(\frac{1}{sC_\pi}+sL_{e1}+\frac{g_mL_{e1}}{C_\pi}\right)||\left(\frac{1+sC_3R_f}{sC_3}\right) \quad (33)$$

Here, the real part of the input impedance is still dominated by g_mL_{e1}/C_π and is primarily controlled by the emitter inductor L_{e1}. The feedback resistor R_{f1} will contribute to the real part of the input impedance seen in equation 33. However, if R_{f1} is chosen to be large enough, then it will have minimal effect on this real part. From equation 33, the small signal equivalent circuit can be simplified to what is shown in Figure 24.

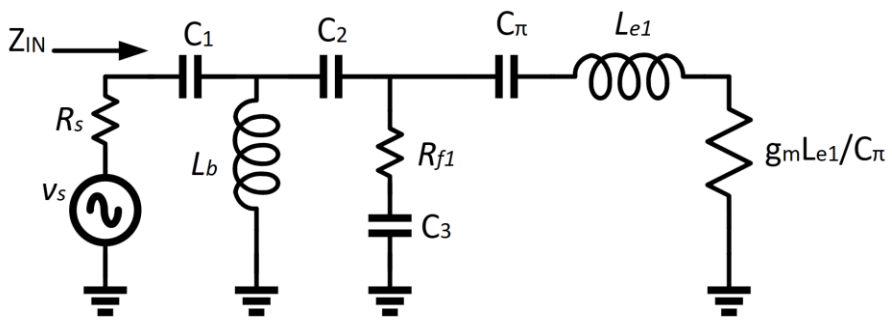

Figure 24. Equivalent Impedance

From this, the total input impedance looking into the LNA from the source resistance R_s can be expressed as

$$Z_{in\ total}(s) = \frac{1}{sC_1} + \left[sL_b \| \frac{1}{sC_2} + \left[\left(\frac{1}{sC_\pi} + sL_{e1} + \frac{g_m L_{e1}}{C_\pi} \right) || \left(\frac{1 + sC_3 R_f}{sC_3} \right) \right] \right] \tag{34}$$

While the emitter inductor L_{e1} serves to set the input impedance equal to 50-Ω, the base inductor L_b is the primary matching component used to resonate with the parasitic capacitances and obtain a conjugate impedance match. In general, the quality factor of the input network decreases as the frequency of operation increases. This means that at mm-Wave frequencies a wideband impedance match can be achieved by using only a few matching components [9]. To demonstrate this point, the S_{11} of the modeled input network in Figure 24 is simulated for different values of L_b showing that the resonant point is controlled by this value and that the S_{11} matching is widened as the resonant point reaches higher frequencies.

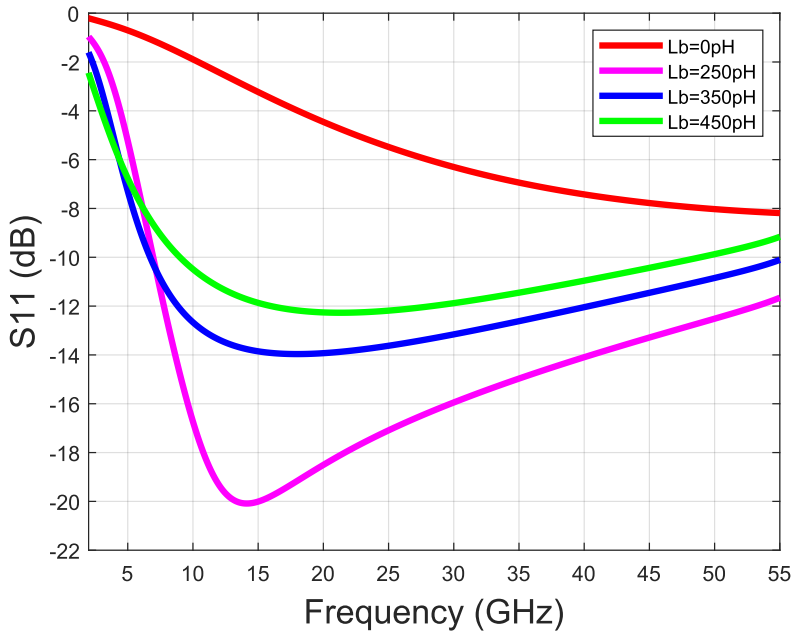

Figure 25. S_{11} with Different L_b Values

As seen in Figure 24, without the addition of L_b to the matching network, a poor input match (S_{11} > -10 dB) is obtained because the parasitic capacitances dramatically affect input impedance. Therefore, it is critical to select the right value of L_b to maximize the S_{11} bandwidth while also having resonance over the desired frequency band. With the combination of resistive feedback to degrade the Q_{in} of the input network and the selection of $L_{b,}$ a wideband impedance match is achieved.

3.7 Ultra-Wideband CAS-CE LNA

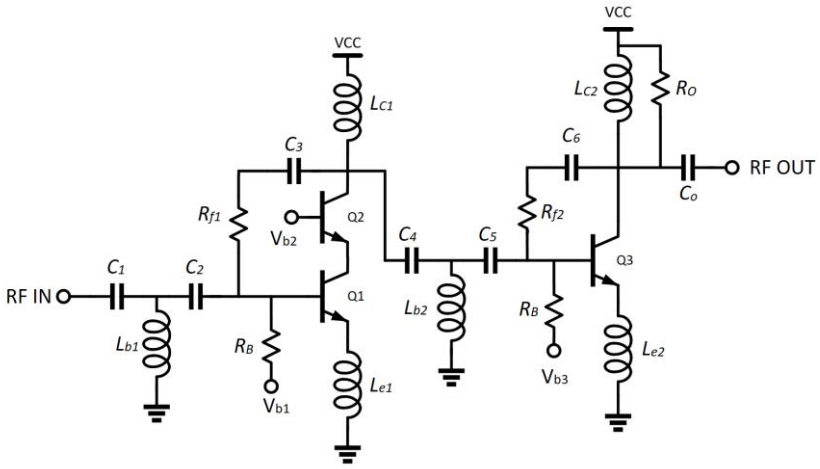

Figure 26. CAS-CE LNA Schematic

Table 3. CAS-CE LNA Components

L_{b1}	L_{e1}	L_{c1}	L_{e2}	L_{c2}	L_{b2}	Ro	R_{f1}	Q_1, Q_2
320pH	30pH	150pH	22pH	420pH	80pH	80 Ω	450 Ω	0.1x10x2 μm
C1	***C2***	***C3***	***C4, C5***	***C6***	***Co***	***Rb***	R_{f2}	Q_3
3pF	2pF	100fF	2pF	200fF	4pF	5k Ω	470 Ω	0.1x10x2 μm

The schematic shown in Figure 26 is the second proposed LNA design. This is also a two-stage LNA where transistors Q_1 and Q_2 make up the cascode first stage, and Q_3 makes up the common emitter second stage. Both stages use the resistive feedback technique for wideband impedance matching and gain flatness. The input matching network is identical to the CAS-CAS LNA where L_{b1} provides the conjugate input matching and inductive emitter degeneration is used to set the real part of the input impedance equal to 50-Ω. The collector inductors L_{C1} and L_{C2} are used for inductive peaking and are set so that the resonant points between the two stages occur at the upper and lower bounds of the operating bandwidth. The cascode configuration is used on the first stage for its wideband performance and good isolation between input and output. A common-emitter stage is used at the output for its improved linearity performance over a cascode stage.

However, because the CE has less input and output isolation, some additional interstage matching was required for this design to have a flat gain response.

3.8 Ultra-Wideband LNA Implementation

Both proposed wideband LNAs were designed in an advanced SiGe BiCMOS process. The schematic simulations and designs were created and determined using Cadence Virtuoso. To minimize resistive loss and parasitic capacitance, all the passive inductors are implemented on the thickest copper metal layer that is 3 μm thick. At mm-Wave frequencies, the losses associated with the passive components can have a significant impact on the RF performance of the LNA. All the inductors used in this design were optimized to have a quality factor of ~20 and a self-resonant frequency greater than 100 GHz. The emitter degeneration inductors were realized using the PDKs micro-strip line models to provide a high Q inductor with a relatively small value (20-50 pH). The interconnects in the layout are CPW based lines with a metal 1 ground. Full wave 3D electromagnetic simulations were done on all passive components and interconnects at the top level using EMX. EMX integrates directly with Cadence and allows for chip-level EM simulations to capture all potential coupling effects between devices and passive components. The layout of the pads is designed to facilitate on-wafer probing and flip-chip packaging. The DC and RF pads are 100x100 μm and have a 200 μm pitch. Each stage of the LNAs consume roughly 15mA from a 1.5 V supply. The total chip area for each LNA is 1.3x1 mm^2.

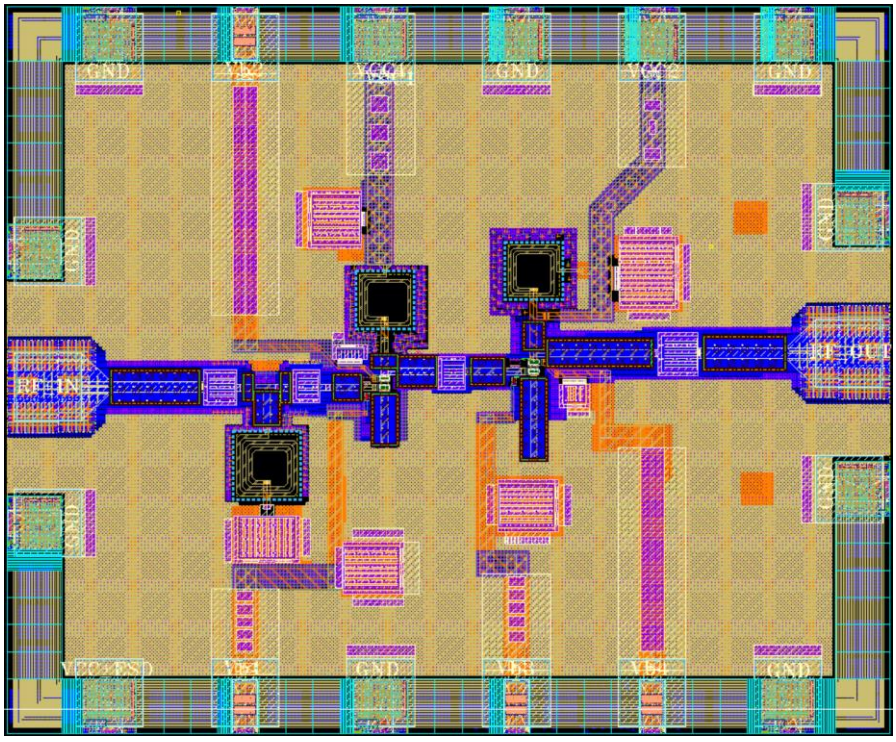

Figure 27. CAS-CAS LNA Layout

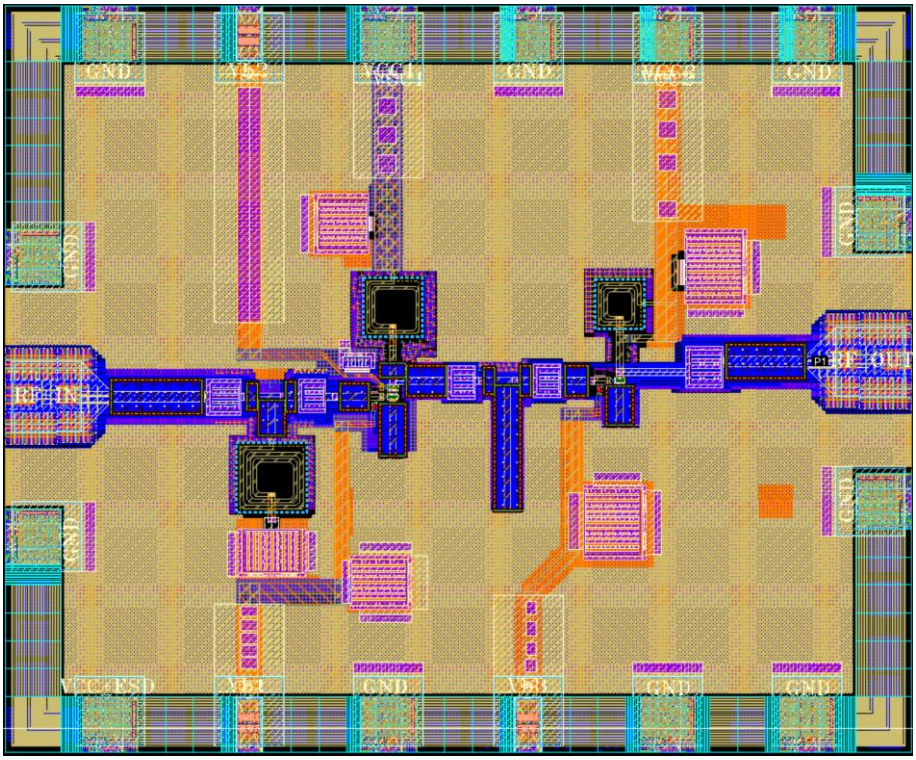

Figure 28. CAS-CE LNA Layout

3.9 Simulation Results

The simulation results for the two proposed LNAs are presented below. The first set of results is from the CAS-CAS LNA and the second set is for the CAS-CE LNA. Each set of simulation results is taken from the EM simulated top level layout of each LNA. The S-parameters are simulated using the *sp* analysis in Cadence Virtuoso; the IIP3 and P1dB values are simulated using a two tone and single tone harmonic balance simulation.

The S_{11}, S_{21}, and S_{22} of the CAS-CAS LNA are shown in Figure 29.

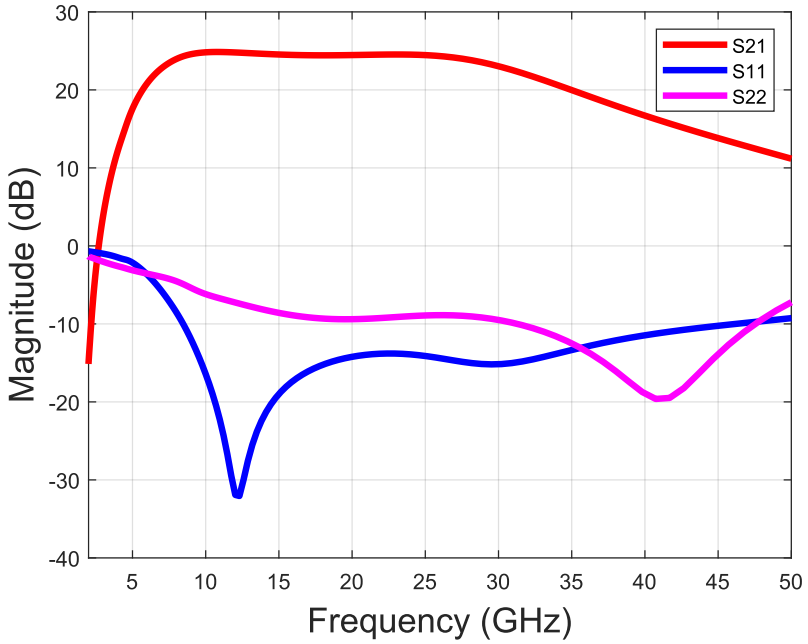

Figure 29. CAS-CAS LNA S21, S11, S21

The CAS-CAS LNA achieves a peak gain of 24.8 dB at 10 GHz and has a wide 3 dB bandwidth from 6.4-32.2 GHz from the S_{21} curve. The LNA has good input return loss (S_{11}< -10 dB) from 8.4-46 GHz. The operating bandwidth, defined from the 3 dB bandwidth and S_{11} bandwidth, is 23.8 GHz from 8.4-32.2 GHz.

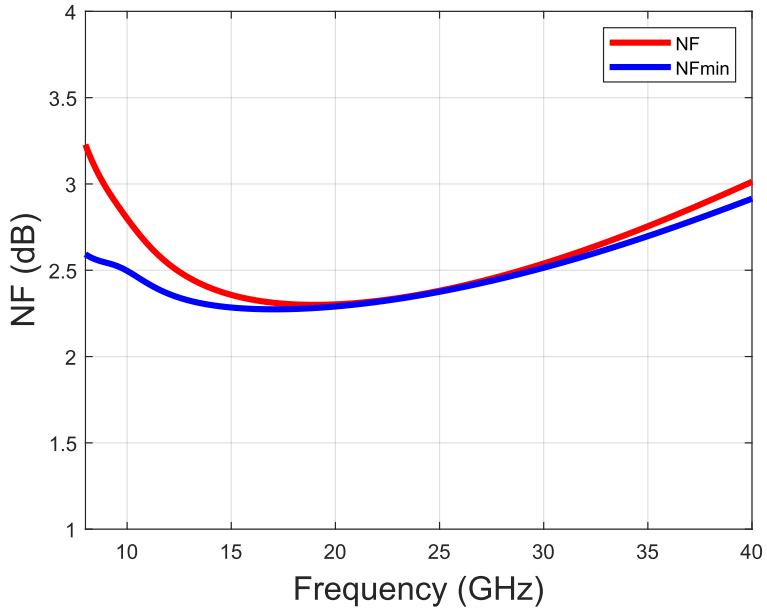

Figure 30. CAS-CAS LNA NF and NF_{min}

Figure 30 shows the simulated NF and NF_{min} of the CAS-CAS LNA. There is minimal deviation of the NF from lowest possible NF (NF_{min}) over a wide bandwidth. The NF ranges from 2.3-3.2 dB across the frequency band of 8.4-32.2 GHz. The minimum NF of 2.3 dB occurs at 20 GHz and the maximum of 3.2 dB happens at 8.4 GHz.

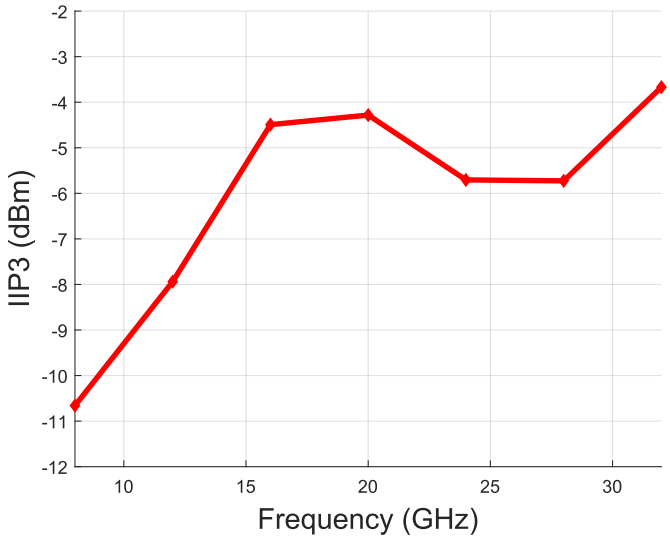

Figure 31. CAS-CAS LNA IIP3 Across Frequency

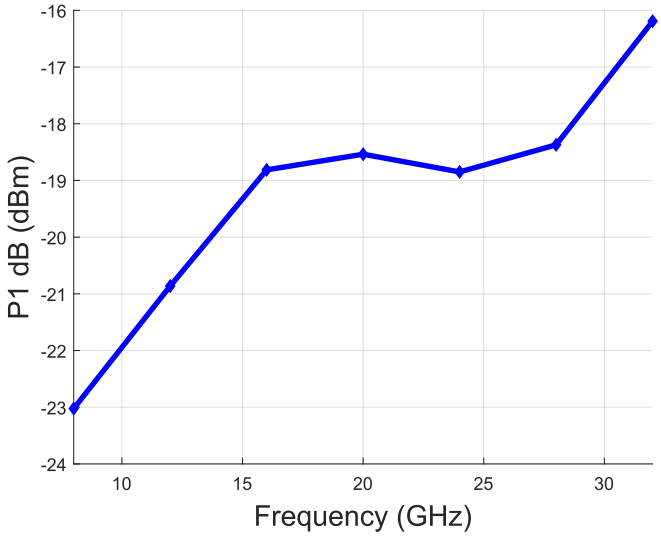

Figure 32. Cas-Cas LNA $P1_{dB}$ Across Frequency

Figures 31 and 32 show the simulated IIP_3 and $P1_{dB}$ compression point across frequency. The IIP_3 ranges from -10.8 to -3.4 dBm, and the $P1_{dB}$ compression point ranges from -23 to -16.2 dBm.

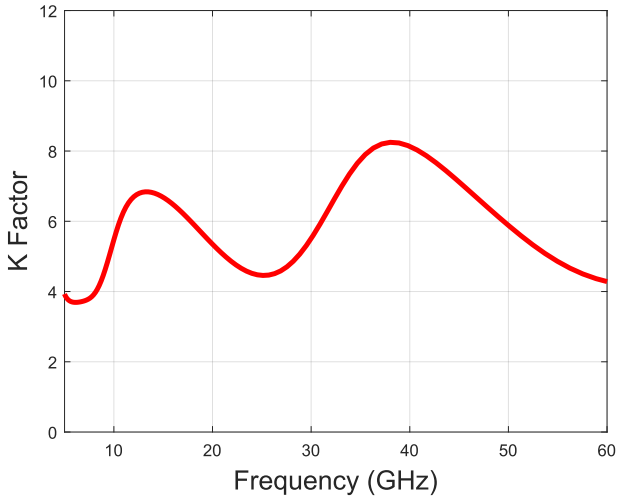

Figure 33. Cas-Cas LNA K-Factor

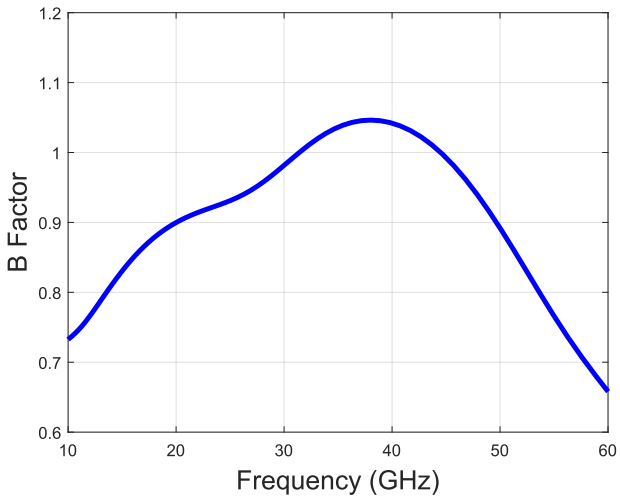

Figure 34. Cas-Cas LNA B-Factor

To check the stability of the LNA, the *K* and *B* factors are simulated. These parameters are defined in section 2.4. To have unconditional stability, *K* must be greater than 0 and *B* must be greater than 1. Figures 33 and 34 show that the LNA is stable across the whole operating frequency band.

Table 4 summarizes the performance of the CAS-CAS LNA.

Table 4. CAS-CAS LNA Summary

Parameter	**Value**
Peak Gain	24.8 dB
BW	8.4-32.2 GHz
NF	2.3-3.2 dB
Max IIP_3	-3.4 dBm

The following results are for the CAS-CE LNA. Figure 35 shows the S_{11}, S_{22}, and S_{21} results of the CAS-CE LNA.

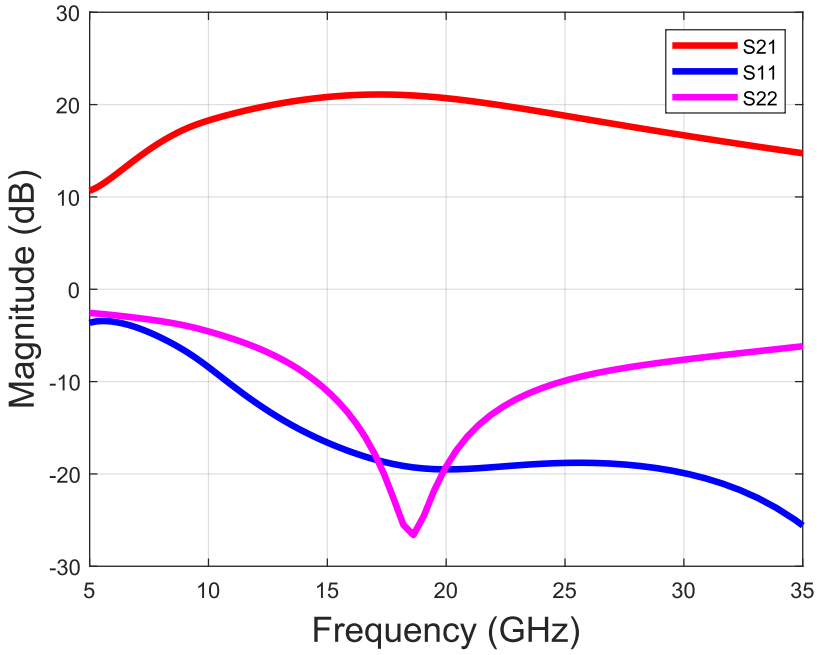

Figure 35. Cas-Ce LNA S21, S11, S22

The CAS-CE LNA achieves a peak gain of 21 dB at 18 GHz and has a 3 dB bandwidth from 11-25 GHz from the S_{21} curve. The LNA has good input return loss (S_{11}< -10 dB) from 10.5-50 GHz. The operating bandwidth, defined from the 3 dB bandwidth and S_{11} bandwidth, is 14 GHz from 11-25 GHz.

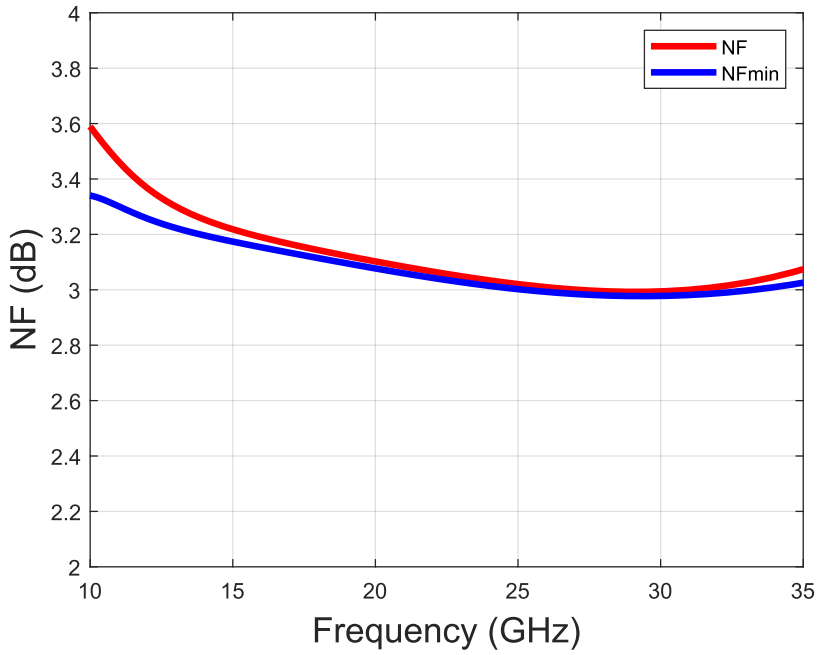

Figure 36. CAS-CE LNA NF and NF_{min}

Figure 36 shows the simulated NF and NF_{min} of the CAS-CE LNA. There is minimal deviation of the NF from lowest possible NF (NF_{min}) over a wide bandwidth. The NF ranges from 2.9-3.4 dB across the frequency band of 11-25 GHz. The minimum NF of 2.9 dB occurs at 27 GHz and the maximum of 3.4 dB happens at 11 GHz.

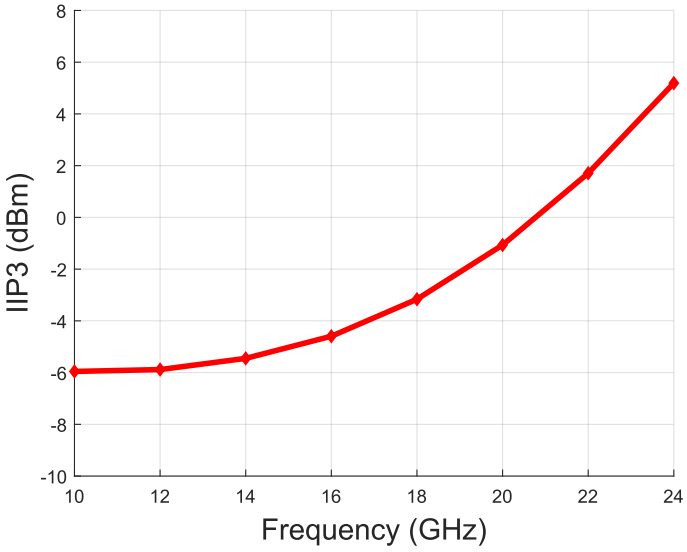

Figure 37. CAS-CE LNA IIP3 Across Frequency

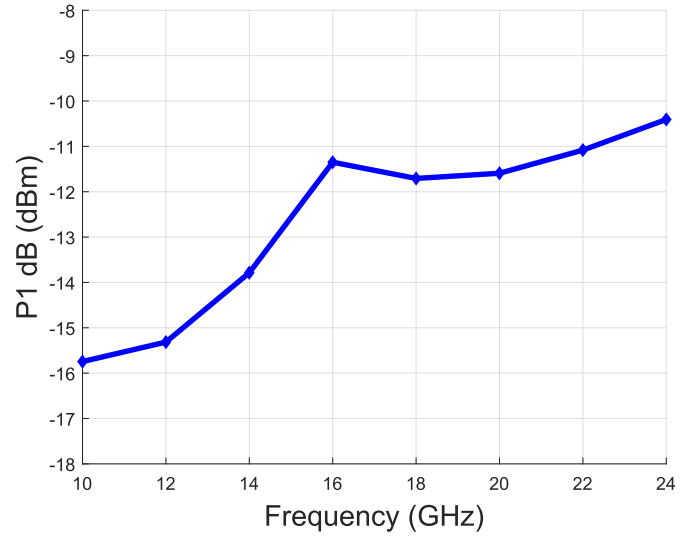

Figure 38. CAS-CAS LNA $P1_{dB}$ Across Frequency

Figures 37 and 38 show the simulated IIP_3 and $P1_{dB}$ compression point across frequency. The IIP_3 ranges from -6 to 5.2 dBm, and the $P1_{dB}$ compression point ranges from -15.7 to -12.2 dBm.

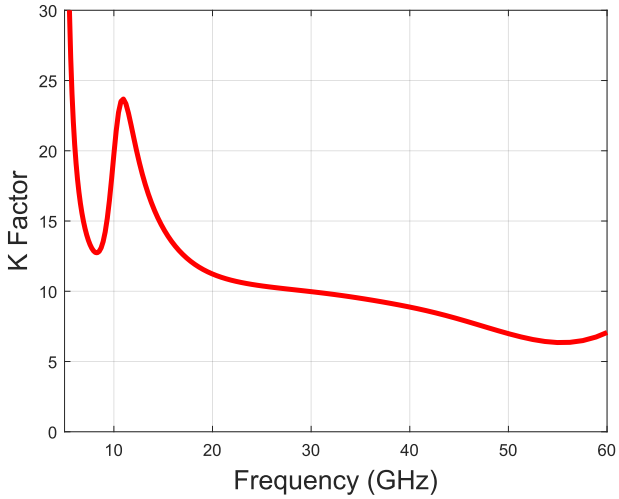

Figure 39. CAS-CE LNA K-Factor

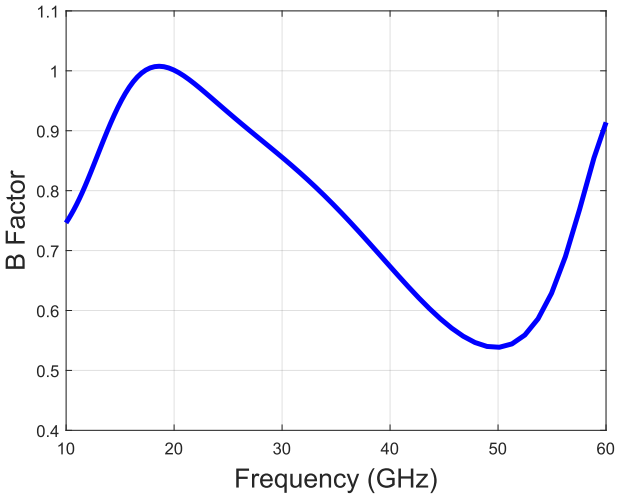

Figure 40. CAS-CE LNA B-Factor

To check the stability of the LNA, the *K* and *B* factors are simulated. These parameters are defined in section 2.4. To have unconditional stability, *K* must be greater than 0 and *B* must be greater than 1. Figures 39 and 40 show that the LNA is stable across the whole operating frequency band.

Table 5 summarizes the performance of the CAS-CE LNA.

Table 5. CAS-CE LNA Summary

Parameter	**Value**
Peak Gain	21 dB
BW	11-25 GHz
NF	2.9-3.4 dB
Max IIP_3	5.2 dBm

Table 6 shows the performance comparison between the CAS-CAS LNA and the CAS-CE LNA.

Table 6. LNA Comparison

Parameter	**CAS-CAS**	**CAS-CE**
Peak Gain	24.8 dB	21 dB
BW	8.4-32.2 GHz	11-25 GHz
NF	2.3-3.2 dB	2.9-3.4 dB
Max IIP_3	-3.4 dBm	5.2 dBm

The CAS-CAS LNA achieves a much wider bandwidth over the CAS-CE LNA. This is due to the second cascode stage providing a higher bandwidth over the CE output stage. As stated previously, a cascode stage has better isolation from input to output and has a smaller miller capacitance. The CAS-CE LNA achieves a higher IIP3 than the CAS-CAS LNA. This was the expected result, because from the previous analysis the CE stage was shown to have a higher linearity over the cascode stage. The NF of each LNA is similar, with the CAS-CE LNA having a slightly higher max NF of 3.4 dB over 3.2 dB of the CAS-CAS LNA.

3.10 Test Plan

These LNA chips will be tested under two different conditions. First, these chips will be tested using on-wafer probing. These chips were designed with a pad pitch of 200 μm and will require two GSG probes for the input and output connections. Additionally, two six-point 200 μm pitch DC probes will be used for the bias connections on the top and bottom of the chip. Secondly, these chips will be tested using a PCB interface with high frequency connectors. These chips are designed to be flip chip packaged and will be mounted to a PCB test board. The measurements required to fully characterize LNA performance are summarized in table 7. The same measurements will take place for both the on-wafer testing and PCB board testing.

Table 7. Measurement Summary

Measurement	**Description**	**Instrument**
S-parameters	S_{11}, S_{22}, S_{12}, S_{21}	R&S ZVA 67
Noise Figure	Y-factor method	R&S FSV-K30
Stability	K and μ factors	R&S ZVA 67
Linearity	P_{1dB} and IIP_3	R&S ZVA 67

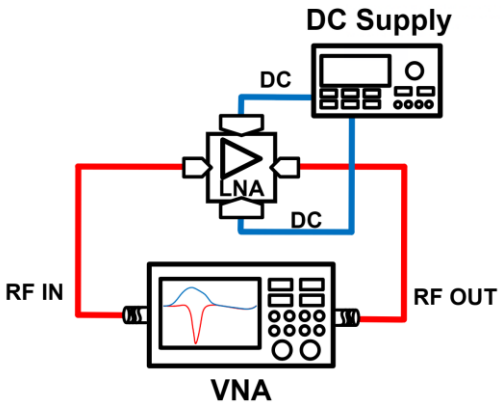

Figure 41. S-parameter Measurement Setup

The S-parameter measurements can be taken by connecting the device under test (DUT) to a network analyzer such as the R&S ZVA 67. For the on-wafer measurements, the VNA is calibrated up to the probe tips using an impedance standard substrate provided by the probe manufacturer. The calibration will be done using short, open, load, and through terminations provided on the impedance standard substrate. For the PCB board measurements, the VNA will be calibrated up to the end of the cables that are used.

For the noise measurements, the Y-factor method will be used. The Y-factor method uses a calibrated noise source to calculate and measure the noise contributions of the DUT. The noise source is typically a reversed biased diode that is used to generate the noise and is defined by its excess noise ratio (ENR). The R&S FSV-K30 spectrum analyzer has the capability to do Y-factor noise measurements

$$ENR_{dB} = 10\log_{10}\frac{(T_s^{ON} - T_s^{OFF})}{T_0} \tag{35}$$

Here, T_s^{ON} and T_s^{OFF} are the noise temperatures of the noise source in its on and off states respectively. T_0 is the reference temperature of 290 K.

The Y-factor is defined as the ratio of the noise power when the noise source is ON to when its OFF.

$$Y = \frac{N^{ON}}{N^{OFF}} \tag{36}$$

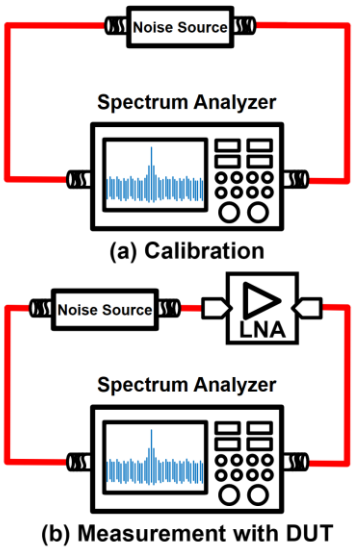

Figure 42. Noise Figure Measurement Setup

The Y-factor measurement method has two steps. The first step is calibration where the measurement is done without the DUT and the noise source is connected directly to the input of the instrument. If T_2 is the noise temperature of the instrument, then the Y-factor in this case will be calculated as

$$Y_2 = \frac{(T_s^{ON} + T_2)}{(T_s^{OFF} + T_2)} \tag{37}$$

$$T_2 = \frac{(T_s^{ON} - Y_2 T_s^{OFF})}{(Y_2 - 1)} \tag{38}$$

With these computed values, the instrument can then normalize the noise figure and gain to 0 dB.

The second step is to introduce the DUT into the measurement. The measurement now is composed of the DUT followed by the instrument and the combined Y-factor is given by equation 39.

$$Y_{12} = \frac{N_{12}^{ON}}{N_{12}^{OFF}} \tag{39}$$

$$T_{12} = \frac{(T_s^{ON} - Y_{12}T_s^{OFF})}{(Y_{12} - 1)} \quad (40)$$

$$G_1 = \frac{(N_{12}^{ON} - N_{12}^{OFF})}{(N_2^{ON} - N_2^{OFF})} \quad (41)$$

From this, T_{12} is calculated, and the gain of the DUT (G_1) can be calculated as in equation 41. With these parameters calculated, the instrument can then solve for T_1 which is the noise temperature of the DUT that is corrected for the noise contribution of the instrument.

$$T_1 = T_{12} - \frac{T_2}{G_1} \quad (42)$$

The value of T_1 is used to calculate the noise factor (F) and the noise figure (NF).

The stability measurements will be done based off the S-parameter measurements. The K and μ factors are calculated from the S-parameters as discussed in section 2.4. The R&S ZVA 67 has a built in stability factor function that can be used to easily obtain this measurement.

For the linearity measurements, the R&S ZVA will be used to measure the P_{1dB} and IIP_3 at frequencies across the band. For the P_{1dB} measurement a power sweep will be run at the input of the DUT and the instrument can calculate the compression point from this sweep. For the two-tone IIP_3 measurement the R&S ZVA can also be used where two of the four ports act as independent RF sources and are fed into the DUT via a power combiner. Here, the power of the two input signals is swept over a large range and the output is measured to calculate the IIP_3 point at different frequencies.

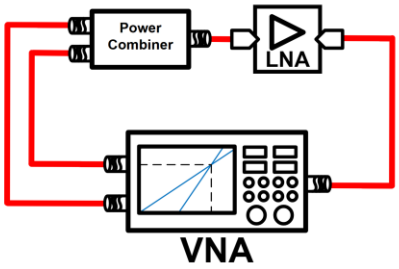

Figure 43. IIP_3 Measurement Setup

4. RAD-HARD WIDEBAND LNA

In this section, a design strategy for producing a rad-hard wideband LNA will be proposed. It is well known that electronic devices suffer from performance degradation when exposed to significant levels of radiation. This becomes a significant design issue with electronics that will inevitably be exposed to radiation, such as in an outer space environment. Radiation-hardening is the process of making electronics robust and resistant to the effects of radiation through fabrication or design techniques. Several rad-hard LNA designs have been presented in the past [24],[25]. However, these designs have narrow band or low frequency operation. In this work the use of inverse mode (IM) devices for radiation hardness will be proposed as a strategy for a wideband rad-hard LNA design.

4.1 Extreme Environments

There is a vast need for high performance SoC ICs to be used in applications in which they are exposed to extreme environments. Extreme environments include very high and low temperatures (-55^{o}C or 125^{o}C), high vibration, high or low pressure, radiation exposure, and chemically corrosive environments [21]. The work presented here focuses on the effects of radiation exposure. The principal application in which ICs would be subject to a radiation-rich environment would be in space applications such as satellite communications or space radar. The two primary types of radiation events that degrade electrical performance are total ionizing dose (TID) and single event effects (SEE).

TID refers to ionizing damage within semiconductor devices caused by exposure to radiation sources such as trapped electrons and protons, solar flares, cosmic particles, gamma rays, and X-rays. TID is the measure of the total energy absorbed by a material. It is most commonly

measured in units of rads (radiation absorbed dose), where 100 rad=1 J/kg. The negative TID effects are caused by the accumulation of trapped charges in the technology's isolation and insolation oxides. When charged particles travel through a device, they create electron-hole pairs in the oxide layers. Due to their higher mobility, the electrons can more easily diffuse out of the oxide, leaving the holes trapped and creating a net positive charge in the oxide. The creation of these trapped charges can lead to degrading of the threshold voltage in CMOS devices, causing a decrease the transconductance. Also, this can lead to an increase in leakage currents between the device terminals. In BJT transistors, TID typically leads to an increase in recombination and thus a higher base current and decreased current gain. Therefore, higher power consumption is needed to compensate for this effect. Total ionizing dose degradation has been reported to be minor in SiGe HBTs for the bias range where the collector current I_C is above 100μA [21]. SiGe HBTs are rad-hard as fabricated due to the high doping levels that are used within the device. This significantly decreases the effects of trapped charge in the oxide layers.

SEEs occur when a high energy particle strikes the active region of a device. These particle strikes often produce abrupt current and voltage transients within a device and lead to distorted output waveforms [24]. As a high energy particle travels through the active region of a device, it leaves a collection of electron-hole pairs behind it. These electron-hole pairs are then separated by the electric fields within the device and cause transient currents and voltages at the terminals of the transistor.

While it has been shown that SiGe HBT devices are robust to TID, they are still susceptible to SEE [13],[24]. The collector-substrate junction within an HBT device is the most sensitive when it comes to SEE because these regions have the largest total volume and collect the most charge [32]. When a particle strike happens, it produces a large number of electron-hole pairs within the

device. This will drastically alter the electrostatic conditions within the device. In a typical biasing condition, the collector-substrate junction is reversed biased. The influx of electron-hole pairs introduced by the particle strike will cause a collapse in the collector-base electric field and the reversed biased electric field in the collector-substrate junction will drive the holes toward the substrate junction and the electrons toward the collector junction [32]. A drift electric field will be present until the excess carriers exit the device by recombination or as terminal currents. In many applications, the collector terminal is directly tied to the output of the circuit. Having the collector terminal directly tied to the output when a SEE happens can cause serious distortions to the expected output waveform since the collector-substrate junction is highly sensitive [26]. Figure 44 illustrates the movement of the excess electron-hole pairs within a device when an SEE occurs.

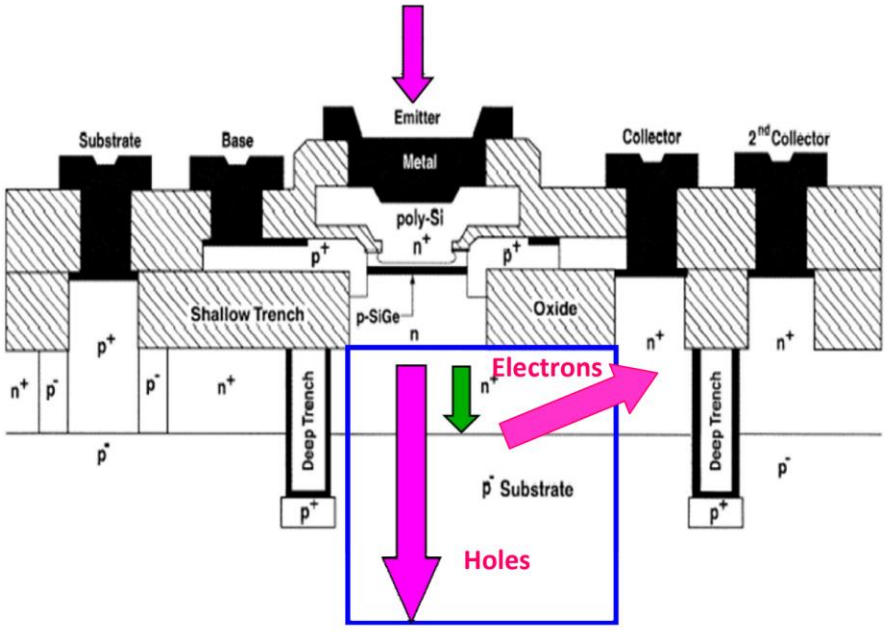

Figure 44. Charge Movement During an SEE [32]

4.2 Inverse Mode Operation

Using inverse mode (IM) HBTs has been a proposed technique for the mitigation of SEE within SiGe BiCMOS technologies in several different designs of digital and RF circuits [24],[26],[27],[28]. While operating a device in inverse mode, the physical collector and emitter terminals are swapped. By changing the applied bias voltages, the physical emitter now operates as the electrical collector [26]. In an HBT device, the electrical emitter is isolated from the highly sensitive subcollector and substrate junctions; therefore, there is a less significant SEE effect seen at the emitter terminal [24]. It has been reported that the emitter terminal in an HBT device collects negligible charge during an ion strike [24],[32]. By swapping the physical collector and emitter, the output of a circuit can be decoupled from the collector-substrate junction. Therefore, the current transients at the output node can be mitigated. While inverse mode operation provides a good strategy for SEE mitigation, it suffers from significant performance limitations when compared to standard forward mode (FM) operation [26]. Inverse mode HBTs are reported to have lower current gain (β), and lower f_T/f_{MAX} than forward mode devices [29]. In the past, this factor has limited the inverse mode HBT to low-speed analog applications [26],[28]. With vertical and horizontal scaling of SiGe BiCMOS technologies the inverse mode performance has improved due to reduced parasitic capacitances and increased current gain. With improved RF and DC performance in modern HBT technologies, the use of inverse mode devices for RF and mm-Wave space applications are becoming a possibility [24].

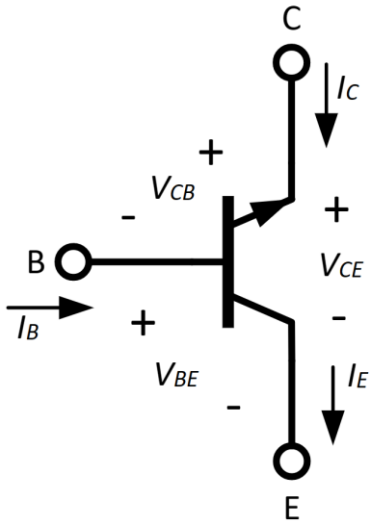

Figure 45. Inverse Mode Operation

Figure 46 shows the simulated DC characteristics between the forward and inverse mode operation of a CBEBC 0.1x2x1 μm HBT device. The Gummel number (G_B), the emitter area, and collector areas are the same for both the forward and inverse mode devices. At a lower bias condition, the collector current is similar between the two modes of operation. However, at a higher bias condition the inverse mode collector current decreases faster than the standard forward mode device. This is because the physical collector resistance, which is now the emitter resistance in IM, is much larger in IM operation [29]. Figure 47 shows the simulated β between the FM and IM operation. The β value in IM operation is relatively constant when compared to the RM operation. However, the base current is higher in IM operation which leads to an overall decrease in the current gain compared to FM operation [30].

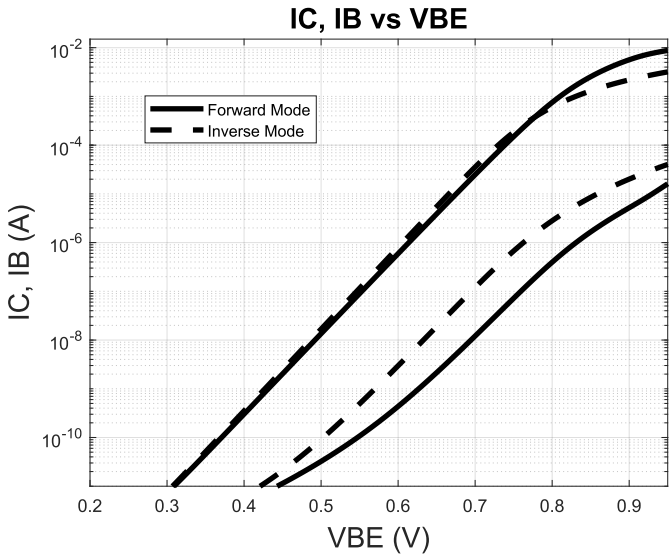

Figure 46. FM and IM: I_c, I_B vs V_{BE}

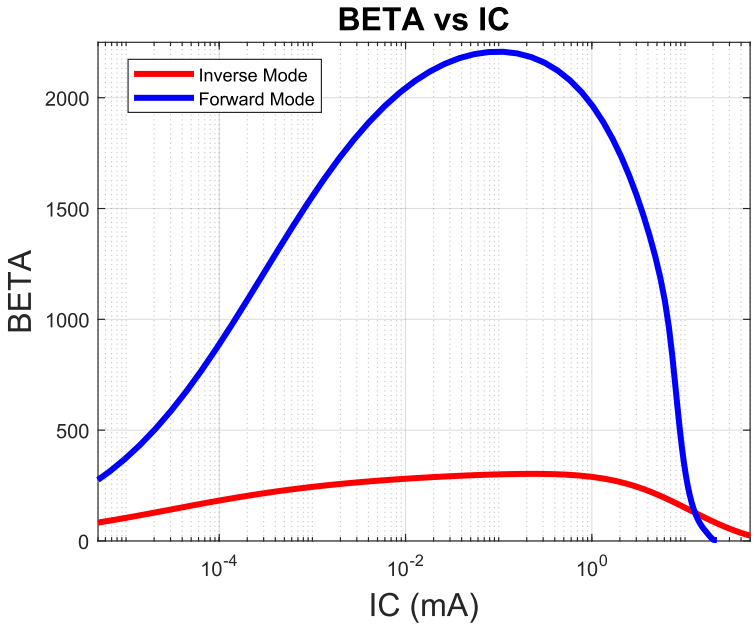

Figure 47. FM and IM: Beta

Figure 48 shows the peak f_T of the IM operation. The IM device has a significantly lower f_T than the standard FM device. It has been reported that the E-B and C-B depletion capacitances and base, collector, and emitter transit times increase when operating the device in IM [29],[31]. This leads to a degradation of f_T when using IM operation. For a CBEBC 0.1x2x1 μm device the simulated peak f_T of the IM device is 10.3 GHz while the peak f_T of a standard FM device is above 300 GHz.

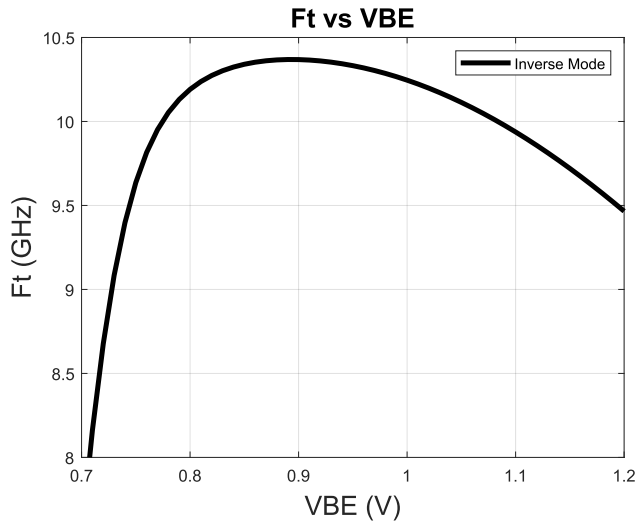

Figure 48. IM f_T vs V_{BE}

4.3 Inverse-Mode Implementation

The IM HBT by itself is not adequate for high frequency mm-Wave circuits due to its significantly lower f_T over the FM operation. Implementing an IM cascode structure has been shown to increase the overall DC and RF performance over a single IM device [24],[26]. This structure is shown in Figure 49 where the IM device is the upper transistor in the cascode pair, and a standard FM device is used as the bottom transistor.

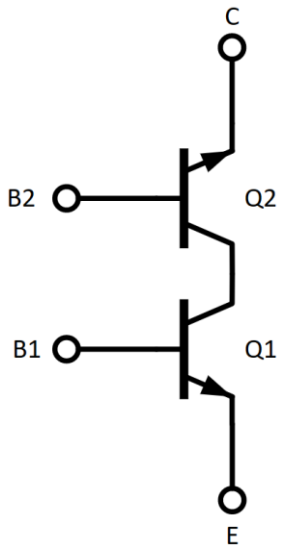

Figure 49. Inverse Mode Cascode

The cascode configuration is the most used core topology for mm-Wave LNAs, due to its multiple advantages such as reduced miller capacitance, increased input and output isolation, and increased voltage gain. The cascode configuration consists of common-emitter (CE) and common-base (CB) transistors in series, and the input signal is applied to the base of the bottom transistor. In the IM cascode structure, the CE transistor is a FM device, and the CB transistor is an IM device. Here, the physical emitter terminal (electrical collector) of the CB transistor is connected to the output. As discussed earlier, this will help mitigate transient currents seen at the output during a SEE, because the sensitive collector-substrate junction is decoupled from the output. For this IM cascode structure, the primary amplification is being supplied by the FM transistor, and the IM transistor is biased in common base configuration and supplies unity current gain. Therefore, high gain can still be achieved even with the use of an IM device. Figure 50 shows the peak f_T of an IM cascode and a standard FM cascode structure. The IM cascode devices f_T is dramatically improved from the single IM device. For this reason, the IM cascode structure has the potential to be

implemented in high-frequency RF applications while providing radiation hardness and adequate *ac* performance [24].

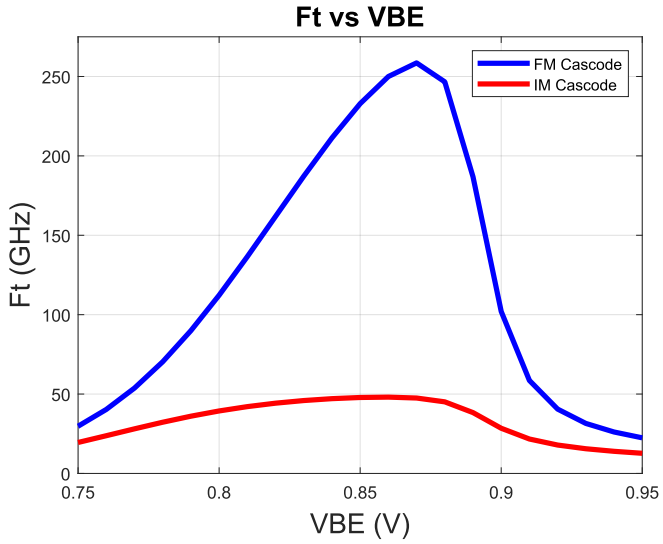

Figure 50. FM and IM Cascode f_T

There is also a difference in linearity between the IM cascode and FM cascode. A drawback of the IM cascode is that it has a decreased linearity compared to the FM cascode. Simulation results show that an IM cascode core has an IIP3 value of -16.5 dBm, and an equivalent FM cascode has an IIP3 of -9 dBm. This decrease in linearity is due to the large output conductance seen in IM operation [30]. In this case, the output current is much more dependent on the output voltage and the linearity is degraded [24]. The use of IM devices is a potential design limitation for systems that require high linearity.

The IM cascode device also has a degradation in NF when compared to standard FM cascode. The simulated NF_{min} of a FM and IM cascode core are compared in Figure 51. The NF_{min} is very close at low frequencies, although still higher in the IM cascode. The separation in NF_{min} increases rapidly as frequencies increase (above 6 GHz). This is due primarily to the much lower f_T associated with the IM cascode. As discussed in section 2.1, the NF_{min} of a device is inversely

proportional to f_T. This is another limiting factor of the IM cascode. There have been reported layout and process modifications that can be implemented to increase the f_T of the IM device and in turn decrease its NF_{min} [32].

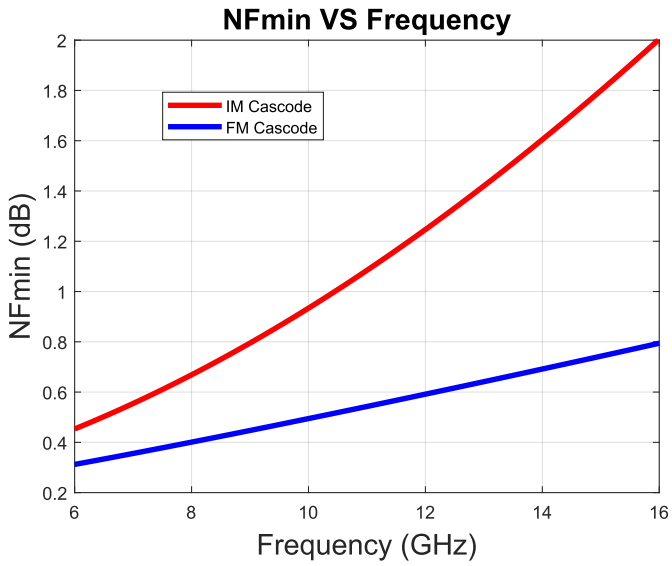

Figure 51. FM and IM Cascode NF_{min}

4.4 Rad-Hard Wideband Inverse Mode LNA

To date, there have been no high frequency (above 2.4 GHz) or wideband LNAs that have utilized inversion mode devices for radiation hardness. To the best of the author's knowledge, the only other LNA design that has utilized inversion mode devices is the design presented in [24]. Here, they used an IM cascode configuration to implement a narrow band single-stage LNA for 2.4 GHz operation and reported a 40% reduction in peak transient magnitude when compared to a standard FM cascode design. The design presented in this work proposes that the IM cascode device can be used for higher frequency and wider bandwidth designs especially with the continued technology scaling to more advanced nodes.

The schematic of the proposed rad-hard LNA is shown in Figure 52.

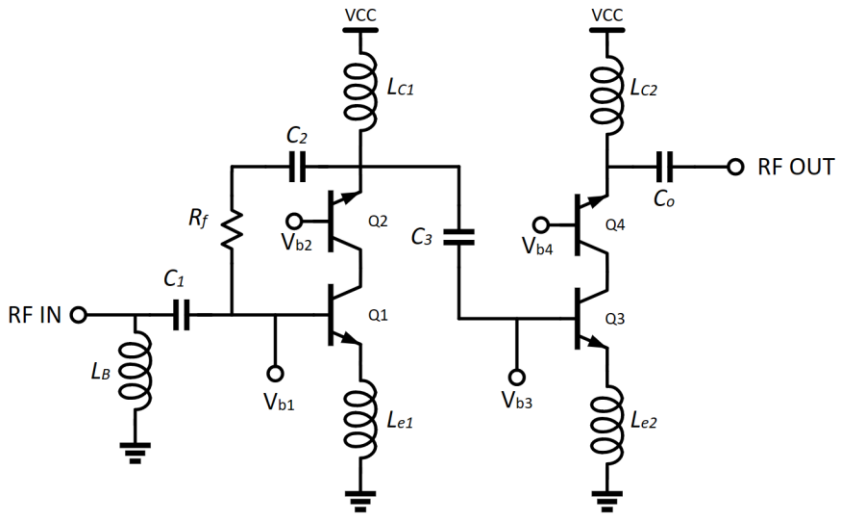

Figure 52. Rad-Hard LNA Schematic

This is a two-stage LNA design that uses the IM cascode structure as the core topology for both stages. The IM device is placed at the output of each stage for the suppression of SEE transients. As mentioned previously, the cascode configuration is used for its reduced miller capacitance and increased isolation between input and output making impedance matching easier. This design also uses inductive emitter degeneration for input matching similar to the designs presented in earlier sections. This LNA also uses resistive feedback in the first stage for the purposes of wideband impedance matching and gain flatness. A shunt inductor (L_B) is used for conjugate impedance matching while the emitter inductor L_E is used to set the real part of the input impedance equal to 50-Ω. Figures 53 and 54 show the initial simulation results of the proposed rad-hard LNA.

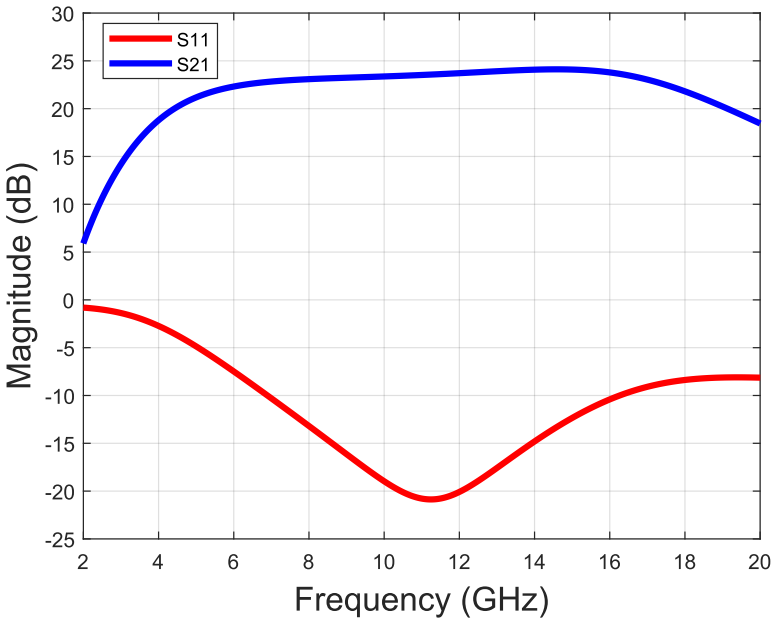

Figure 53. Rad-Hard LNA S21, S11

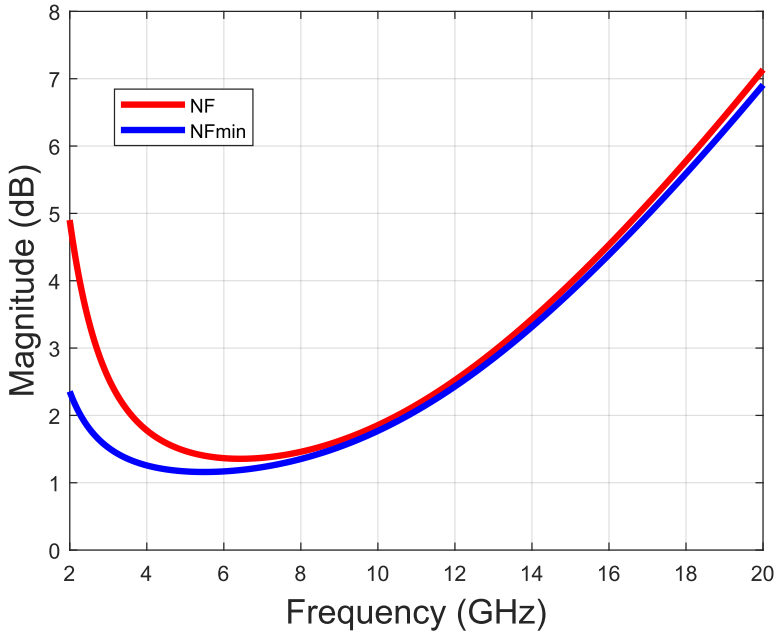

Figure 54. Rad-Hard LNA NF

Table 8. Rad-Hard LNA Summary

Parameter	Value
Peak Gain	24 dB
3dB BW	4.9-18.5 GHz
S11<-10 dB	6.9-16.3 GHz
NF	1.3-4.5 dB
IIP3	-11.3 dBm

This IM rad-hard LNA achieves a peak gain of 24 dB and a BW of 9.4 GHz from 6.9-16.3 GHz. The NF ranges from 1.3-4.5 dB. The NF is quite good at the lower frequency range (below 10 GHz) and would most likely match that of a standard FM cascode LNA. However, the NF increases significantly at higher frequencies (above 10 GHz). This is due to the lower f_T for the IM cascode and the operating frequency being closer to this f_T frequency value.

4.5 Comparison with Other Rad-Hard LNAs

In general, there have not been many published designs showing rad-hard techniques specifically for LNAs. However, in [25] they employed the use of SiGe BiCMOS BJT devices for their inherent radiation hardness to TID. They also use a combination of BJT and CMOS devices to make up for the degradation in β during radiation exposure. This design operated at very low frequencies from 100 Hz–1 MHz. The design in [24] used the IM cascode structure to produce a narrow band LNA design at 2.4 GHz.

Table 9. Rad-Hard LNA Comparison

ref	Gain	BW	NF	IIP3
[25]	20 dB	100HZ-1MHz	Not reported	Not reported
[24]	23 dB	2.4 GHz	2.5 dB	-18 dBm
This Work	24 dB	6.9-16.3 GHz	1.3-4.5 dB	-11.3 dBm

While the frequency range of the proposed rad-hard LNA is more impressive than the other reported designs [24],[25], it suffers from a significantly larger NF at the high end of its frequency range. The most significant trade-off with the IM LNA is certainly in its NF performance at high frequencies. This is a major design consideration for receivers that require high sensitivity. Noise reduction or cancellation techniques would be necessary for future implementation. This proposed design is a good starting point for future work on investigating, designing, and fabricating a wideband rad-hard LNA. The IM cascode has been reported to show significant improvement in SEE mitigation [24],[26],[27],[28]. Therefore, it is a worthwhile strategy to continue investigating for high frequency and even mm-Wave LNA designs, especially with the continued scaling of SiGe technologies that will inevitably increase the performance of inverse mode devices.

5. CONCLUSION

The design of two wideband LNAs in the 8-32 GHz frequency range is presented in this thesis. This research was motivated by ever-increasing demand for high performance and broadband wireless communication networks that operate at mm-Wave frequencies for applications such as 5G support, high data rate communications, military radar, and satellite communications. The LNAs employ resistive feedback for wideband impedance matching and gain flatness. The inductive emitter degeneration technique is used for impedance matching, and gain staggering is used for wideband operation. These designs were implemented in an advanced SiGe BiCMOS process using high performance HBT devices. The post-layout and EM simulation results show that these designs achieved a wide bandwidth of 8-32 GHz, low NF of 2.3 dB, and IIP3 above -3 dBm.

This work also proposed a technique for producing a rad-hard wideband LNA using an inverse mode cascode structure. The simulation results show that a bandwidth from 6.9-16.3 GHz can be achieved using the IM cascode structure. Future work could be performed to continue investigating IM devices for LNA circuits by more detailed modeling and simulations with the potential for fabricating a rad-hard wideband LNA.

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