

**A FULLY DIFFERENTIAL, WIDE BAND, 4-STACKED RF DRIVER  
FOR PHOTONIC MODULATORS**

A Thesis

by

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## ABSTRACT

Advanced sub-micrometer technologies are suffering from the low breakdown voltage of the devices, which makes it hard to achieve high-power and high-frequency RF drivers. To overcome these limitations, power combining techniques are developed to combine the power over multiple stages, such as the transistor stacking technique. This work presents an ultra-wide-band, fully differential stacked RF driver. In comparison to other conventional RF drivers, the stacked driver allows higher output voltage swing and larger output power. The proposed design, prototyped in Global Foundry 22nm FDSOI CMOS technology, shows a 0.4-17.4 GHz bandwidth, with a 20 dB gain. More than 16 dBm output power is achieved at 10 GHz, with 17.6 dBm saturation power. Overall, the driver consumes 288 mW, differential, from a 3.2 V supply and occupies 0.167 mm<sup>2</sup>.

## **DEDICATION**

To my Mother and Sister,  
And in memory of my Father.

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# 1. INTRODUCTION

## 1.1 System Overview

Nowadays, ultra-wideband, ultra-low-phase-noise, and high-resolution mm-wave signal generators can significantly assist applications like current instrumentation, wireless communications, radars, and space systems. To enable simultaneous ultra-wideband, ultra-low phase noise, high-resolution, and continuously tunable signal generation for these applications, transformative mm-wave signal generation architectures are required. The difficulty of simultaneously meeting all of the mentioned specifications for mm-wave signal production is a substantial obstacle to the implementation of these signal generators. Unfortunately, conventional electronic signal generators at the mm-wave range have considerable limitations to overcome this challenge for systems with small form factors. RF photonics technology has the potential to enable mm-wave signal generators to overcome these challenges. On the other hand, nanometers CMOS technologies have the potential to operate in the mm-wave range with ultra-wideband bandwidth, due to their high unity-gain-frequency ( $f_t$ ) and low power consumption.

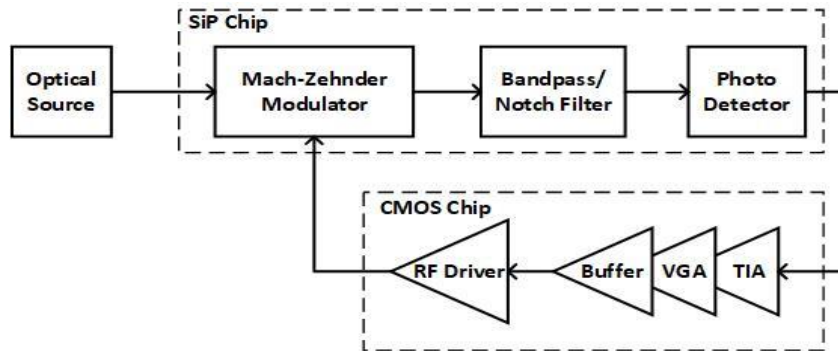


Figure 1 OEO Loop block diagram

Figure 1, shows the overall block diagram of the Optical/Electronic Oscillator (OEO). In this system, the optical power passes through the Mach-Zehnder modulator (MZM) and multiple passband/notch filters. Next, the optical power will be absorbed by the photodetector (PD). The PD transforms the optical power into electrical current and passes it to the CMOS chip. Inside the CMOS chip, the input current transforms and amplifies to the desired voltage swing at the output of the RF driver. Lastly, the voltage swing at the output of the driver will drive the MZM and modulate the light which will be discussed in this chapter.

For Phase 1 of this project, a 17 GHz bandwidth goal was set. From the system analysis, the condition for start-of-oscillation is 45 dB gain for the CMOS chip to compensate for overall loop loss, and  $2 V_p$  (Single-ended) voltage swing at the output of the RF driver, which the gain is distributed between the CMOS devices with 20 dB gain for RF driver and 25 dB for TIA and VGA.

Figure 2, shows a simplified block diagram of the TIA and main amplifier. As mentioned, the optical signal is absorbed by a photodetector (PD), which then transforms the optical signal into an electrical current. Next, the transimpedance amplifier (TIA) will change the electrical current to electrical voltage with a certain gain. However, due to the small voltage swing at the output of the TIA, another amplifier is needed, to provide sufficient voltage swing for the rest of the circuit, which is the main amplifier in Figure 2. The main amplifier can be implemented as a limiting amplifier (LA) or driver amplifier (DA) depending on the application. In this project, because the ultimate goal is to generate low distortion CW signals with low phase noise, and the receiver is driving a Mach-

Zehnder modulator (MZM) in a feedback loop as shown in Figure 1, a DA is chosen as the driver to produce high voltage swing amplitude at the output.

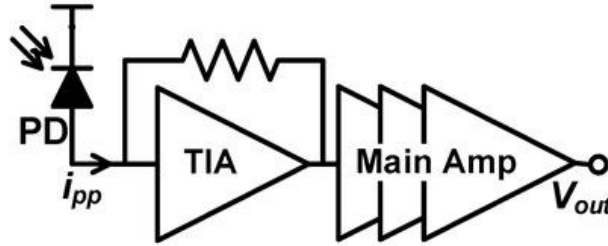
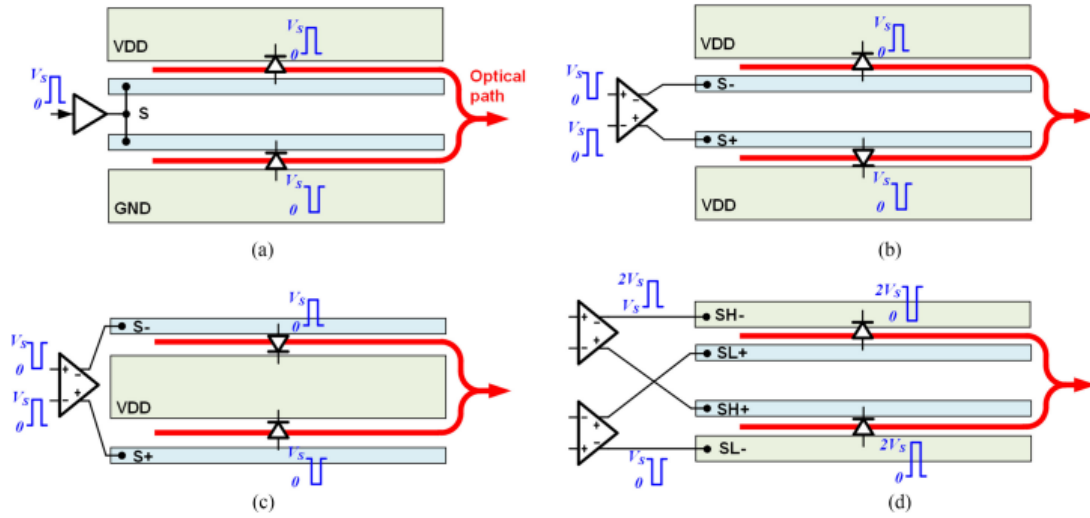


Figure 2 A simplified block diagram of a CMOS chip with PD (Reprinted from [1])

Mach-Zehnder is an optical modulator that changes the light intensity or phase by applying an electric field across the optical path, as is shown in Figure 3 (c). In this figure, the electric field was produced, due to the voltage difference between the S-/S+ and VDD. With the electric field between S-/S+ and VDD, a phase shift will be induced, which depending on that, the recombination of light from the two paths will be constructive or destructive.

A commonly way to implement the MZM is the traveling-wave (TW) electrode architecture. TW modulators are designed as a transmission line (TL), like CPW. Some of the advantages of this modulator are as follows. First, the capacitive loading effect of the electrodes absorbs by the TL, therefore the effective bandwidth of the system expands. Second, unlike the discrete devices, the TL in the TW electrode technique can absorb any possible reflections, by choosing matched-impedance TL. However, there are some disadvantages of TW topology. First, due to the high resistivity of the on-chip metal wires, the TLs are lossy, so the signal attenuates which degrades modulation efficiency. For

instance, in 180nm CMOS technology, a signal attenuates from  $7V_{pp}$  at 20GHz to  $4.6V_{pp}$  over the 4mm-length and 6 $\mu$ m-width wire when it arrives at a  $50\Omega$  termination resistor [2]. Therefore to compensate for this signal attenuation, a larger modulation swing is required which makes the driver circuit design more challenging. Moreover, since the characteristic impedance of the MZM is usually chosen to be  $50\Omega$ , in order to generate large voltage modulation swing, huge currents are needed, which handling this amount of current on advanced CMOS technologies is also challenging.



**Figure 3 Driving schemes of MZM transmitters. (a) Single-ended drive, dual-arm push-pull. (b) Differential drive, dual-arm push-pull. (c) Differential drive, dual-arm push-pull with shared bias. (d) Dual-differential drive, dual-arm push-pull (Reprinted from [2])**

Figure 3 compares different MZM structures. Figure 3 (a) shows a single-ended push-pull driver driving one anode and one cathode arm at the same time. Figure 3 (b) and (c) show a differential driver which drives two anode arms and at the same time, the cathodes are tied up to the highest DC voltage, to make sure the diodes are always reverse-



biased. Lastly, Figure 3 (d) present a dual-differential-driver that drives both the anode and cathode pair for more efficient operation by doubling the swing across each anode/cathode pairs [2].

In this project, a differential-drive, dual-arm, push-pull, Traveling-Wave (TW) MZM was fabricated in SOI with  $2 \times 1.5\text{mm}^2$  area, 50GHz 3-dB bandwidth, and  $50 \Omega$  input impedance which is the load of the differential RF driver.

As mentioned, the RF driver has to be able to drive an MZM, to modulate the optical signal. RF drivers have been traditionally categorized into different classes such as Class A, B, C, and AB, which each have their advantages and disadvantages. For instance, a Class A driver has decent linearity and low distortion due to its biasing operating point, however, the power efficiency of this class is low. On the other hand, the class B driver has more distortion but better power efficiency. Therefore, depending on the application, the proper DA topology needs to be selected. The following table shows a brief comparison between different classes of power amplifiers.

**Table 1 RF driver Class comparison (Reprinted from [3])**

<b>Classes</b>	<b>A</b>	<b>AB</b>	<b>B</b>	<b>C</b>	<b>D</b>	<b>E</b>	<b>F</b>
<b>Conduction angle (%)</b>	100	50-100	50	<50	50	50	50
<b>Max. efficiency (%)</b>	50	50-78.5	78.5	100	100	100	100
<b>Linearity</b>	Excellent	Good	Good	Poor	Poor	Poor	Poor

There are some key parameters of RF drivers that need to be considered in a design and analysis. The power efficiency of the driver is one of the parameters that need to be looked at. Power efficiency defines as the ratio of average output power and average DC consumption over a specified period of time [4].

$$\eta_{AV} = \frac{P_{O(AV)}}{P_{I(AV)}} \quad (1.1)$$

Where  $P_{O(AV)}$  and  $P_{I(AV)}$  are the average output power and average DC consumption, respectively. In theory, the class A RF driver, with RF Choke, can achieve at most 50% efficiency, whereas, the Class B RF driver can go as high as 78% [4]. Moreover, the maximum output power of the driver can be calculated using the following equation.

$$P_{O(max)} = c_p I_{DM} V_{DSM} \quad (1.2)$$

Where  $V_{DSM}$  is the maximum value of instantaneous drain-source voltage,  $I_{DM}$  is the maximum value of instantaneous drain current, and  $c_p$  is output power capability [4]. Also, power-added efficiency (PAE) is another way to measure and analyze efficiency.

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \quad (1.3)$$

Linearity is another parameter that needs to be considered. The definition of linearity is, as the input power of the device varies, the gain of the device remains constant. In other words, in Figure 4, ideally, the first harmonic of the output power should follow

the linear dashed line, however, as the input strength ( $P_{in}$ ) is growing, the output power is acting nonlinear, which is unwanted. There are some other parameters based on linearities that are well-known, such as  $P_{1dB}$  and IIP3. The  $P_{1dB}$  is where the actual output power is 1dB below the expected linear value, and IIP3 (input third harmonic intercept point) is where the first and third harmonic outputs power are equal.

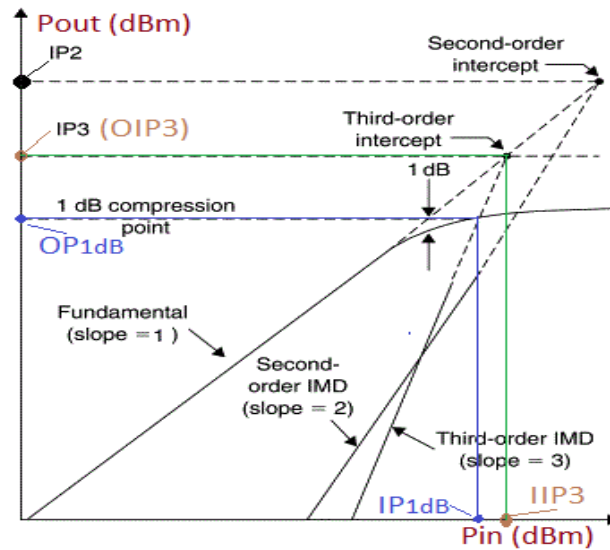


Figure 4 Driver linearity plot (Reprinted from [5])

The next critical parameter for designing an RF driver is its stability. The system is called stable when the system behaves as expected and amplifies the input signal with a certain gain. However, the system is unstable when its output oscillates, which this oscillation is not constant oscillation with fixed amplitude. To analyze the stability of a system, the stability factor, called the “k-factor”, of a system needs to be looked at.

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |D|^2}{2 \cdot |S_{21}| |S_{12}|}$$

(1.4)

And

$$D = S_{11} \cdot S_{22} - S_{12} \cdot S_{21}$$

(1.5)

So in practical terms, the system is called “unconditionally stable” when  $k > 1$ . However,  $k < 1$  the system can be either “conditionally stable” depending on the value of parameter “D” or “unstable” [6].

## 1.2 Research Objective

As mentioned, driving an MZM with a high-frequency CW signal, need a large voltage amplitude to produce the required electric field to modulate the light. However, due to the low nominal voltage and low supply voltage in the 22nm FDSOI CMOS process as the technology of the choice to realize this driver, achieving the required amplitude is challenging. Moreover, due to the high operating frequency of the overall system, an ultra-wide bandwidth driver is required, which is practical because of the low transistor’s parasitic and high  $f_t$  in this technology. Before we delve into solving these issues, it is critical to intuitively analyze different topologies and methods and understand the pros and cons of each topology.

With all being said, an ultra-wide-band, fully-differential stacked RF driver has been proposed using 22nm FDSOI which should be capable of driving the MZM with the required voltage amplitude over ultra-wide frequency bandwidth. The primary objective of this thesis would be to design, implement, and test the functionality of the proposed wide-band Stacked RF driver.

### **1.3 Thesis organization**

Following this introduction, chapter 2 discusses different RF drive and MZM driver topologies and their advantages and disadvantages.

In chapter 3, the proposed stacked RF driver is discussed. This section will illustrate the working of this topology followed by the design, layout, and implementation procedure of the system.

Chapter 4, provides measurement results of the fabricated wide-band driver, followed by a comparison between different state-of-art RF driver and MZM driver topologies.

Lastly, chapter 5 presents the conclusion of this thesis.

## 2. RF DRIVER ARCHITECTURES REVIEW

### 2.1 Distributed Driver

Distributed amplifiers are attractive circuit blocks for ultrawide-band and wireline optical links, due to the ability to process ultra-narrow pulses and multigigabit-per-second signals. Although the bandwidth of these devices can go over 90 GHz, their output power and efficiency are relatively low. Moreover, the distributed driver topologies are not suitable for some applications, due to their large chip area [7].

The distributed driver consists of multiple gain stages and two transmission lines, one at the input and the other at the output of the gain stages, as shown in Figure 5[8]. The concept of the distributed driver is based on combining input and output parasitic capacitance of the active devices with inductors in a way that the two input/output Transmission lines (TL) are obtained. Figure 6, shows the sections of distributed TL of the input and output line which is consisting of inductors and active devices parasitic [8]. This distributed lumped circuit forms a lumped element low pass filter (T-section filter) [8]. To boost the gain, multiple of these filter sections are cascaded and formed into a distributed amplifier.

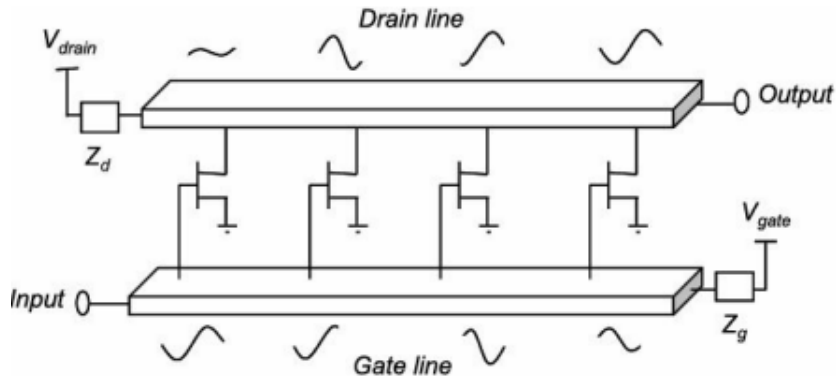


Figure 5 Simplified Distributed power amplifier using TL (Reprinted from [8])

As shown in Figure 5, input and output TL are terminated by  $Z_g$  and  $Z_d$ , which usually are chosen to be  $50\Omega$ , to avoid reflection from each end. However, since a portion of the output absorbs by these terminations, the efficiency of a distributed driver degrades [9]. Moreover, with the large DC current from the supply, the voltage drop across the termination resistor raises which causes efficiency degradation. One way to fix this problem is to use a Bias-T network. Though, the Bias-T networks are expensive and bulky, due to large and high-quality inductors.

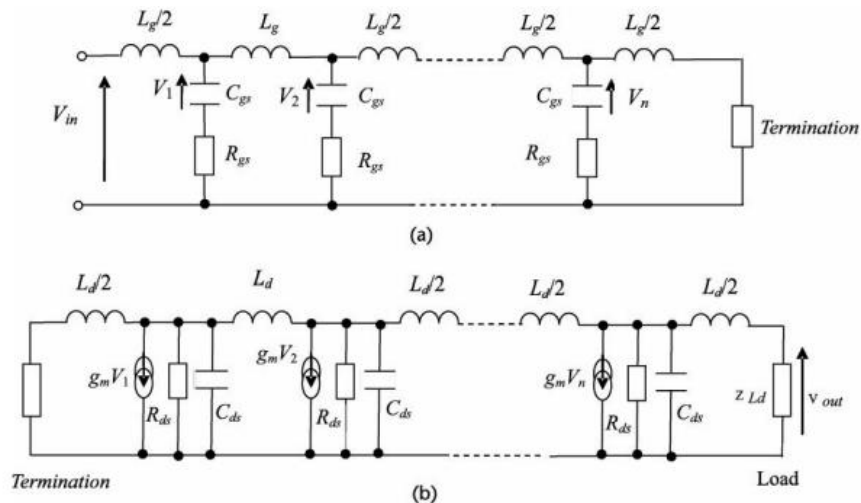


Figure 6 (a) Gate TL, (b) Drain TL (Reprinted from [8])

Assuming the transistors are unilateral, which means the effect of  $C_{gd}$  is neglected, the distributed driver can be simplified into two parts, as shown in Figure 6, in which, Figure 6(a) and (b) correspond to the gate and drain TL, respectively. From Figure 6(b), the current delivered to the load is given by:[8]

$$I_0 = \frac{1}{2} g_m e^{-\frac{\gamma_d}{2}} \left[ \sum_{k=1}^n V_k e^{-(n-k)\gamma_d} \right] \quad (2.1)$$

Where  $V_k$  is the voltage across  $C_{gs}$ ,  $\gamma_d$  is the propagation factor of the drain line, and “n” is the number of transistors in the amplifier. The following equation also expresses  $V_k$  in terms of the gate voltage of the  $k^{\text{th}}$  transistor [8]:

$$V_k = \frac{V_i e^{-\frac{(2k-1)\gamma_g}{2} - j \tan^{-1}\left(\frac{\omega}{\omega_g}\right)}}{1 + \left(\frac{\omega}{\omega_g}\right)^{1/2} \left[ 1 - \left(\frac{\omega}{\omega_c}\right)^2 \right]} \quad (2.2)$$

Where  $V_i$  is the input voltage of the amplifier,  $\gamma_g$  is the propagation factor of the gate line,  $\omega_g$ , and  $\omega_c$  are as follows:

$$\omega_g = \frac{1}{R_{gs} \cdot C_{gs}} \quad \omega_c = \frac{2\pi}{L_g \cdot C_{gs}} \quad (2.3)$$

Additionally, the input power and the power delivered to the load are given by



$$P_0 = |I_0|^2 \Re[Z_{ID}]$$

(2.4)

$$P_i = \frac{|V_i|^2}{2|Z_{IG}|^2} \Re[Z_{IG}]$$

(2.5)

Where  $Z_{IG}$  and  $Z_{ID}$  are the image impedance of the gate and drain line, respectively.

It is also important to understand the concept of image impedance. Let's consider a two-port network forming an artificial transmission line. Each two-port in a cascaded two-port network should function with the necessary impedance terminations to ensure that the maximum power transfer occurs over the specified bandwidth when considering signal transmission and impedance matching. The two-port can be terminated with a pair of impedances known as image impedances to satisfy this need, Figure 7. If the system is symmetrical,  $Z_{i1}$  and  $Z_{i2}$  become identical and the characteristic impedance is denoted as  $Z_0$ . As discussed, the image impedance concept can be applied in distributed driver topology, where each gain stage can be considered as a 2-port network.

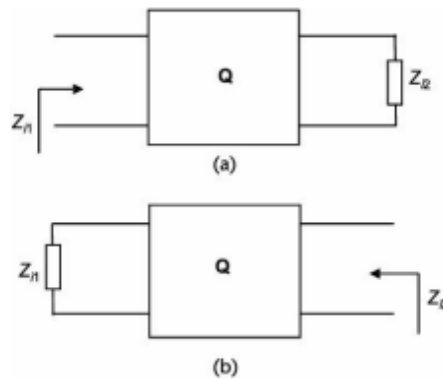


Figure 7 A two-port network terminated by the image impedance (Reprinted from [8])

Where the  $Z_{i1}$  and  $Z_{i2}$  are the image impedances and can be expressed as

$$Z_{i1} = \sqrt{Z_{sc1}Z_{oc1}}$$

$$Z_{i2} = \sqrt{Z_{sc2}Z_{oc2}}$$

(2. 6)

An 8-stage distributed driver is proposed in [10] using the image impedance inter-stage matching, as shown in Figure 8. This design consists of a 2-stacked transistor for each unit gain stage and a low-pass artificial T-line transmission line for the input and the output TLs. Moreover, an off-chip bias-T is used for biasing purposes.

In this design, the m-derived TL is used instead of the conventional constant-k section TL. As is shown in Figure 9, using the m-derived structure introduces a coefficient, “m”, which gives an additional degree of freedom to adjust the frequency response of the filter section. Equation (2.7) and (2.8) shows the reciprocal propagation factor of the k-section and m-derived section TL, respectively, where the effect of “m” can be observed.

$$e^{\gamma} = \left| 1 - \frac{2\omega^2}{\omega_c^2} \right| + \frac{2\omega}{\omega_c} \sqrt{\frac{\omega^2}{\omega_c^2} - 1}$$

(2. 7)

$$e^{\gamma} = \frac{\left| 1 - (1 + m^2) \left( \frac{\omega}{\omega_c} \right)^2 \right|}{\left| 1 - (1 - m^2) \left( \frac{\omega}{\omega_c} \right)^2 \right|} + \frac{\sqrt{\left( \frac{2m\omega}{\omega_c} \right)^2 \left[ \left( \frac{\omega}{\omega_c} \right)^2 - 1 \right]}}{\left| 1 - (1 - m^2) \left( \frac{\omega}{\omega_c} \right)^2 \right|}$$

(2. 8)

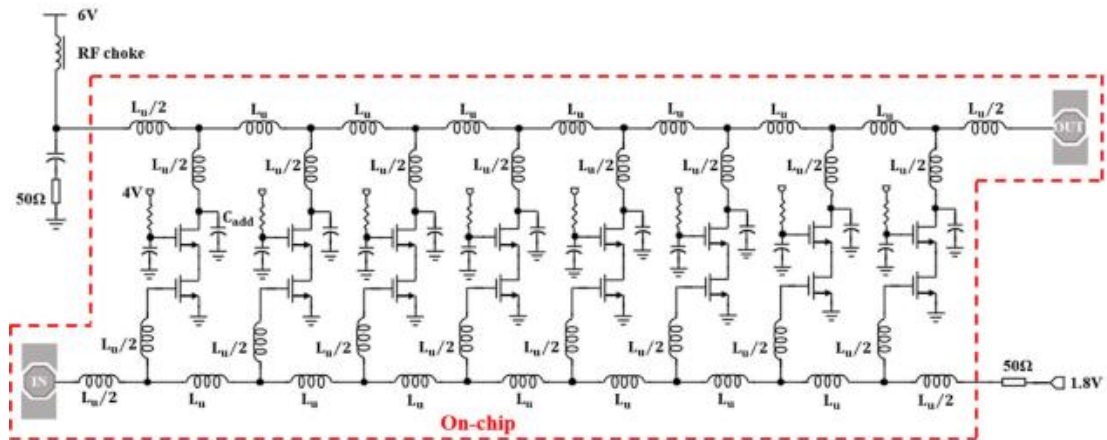


Figure 8 8-stage Distributed Driver using 2-stacked gain unit cell. (Reprinted from [10])

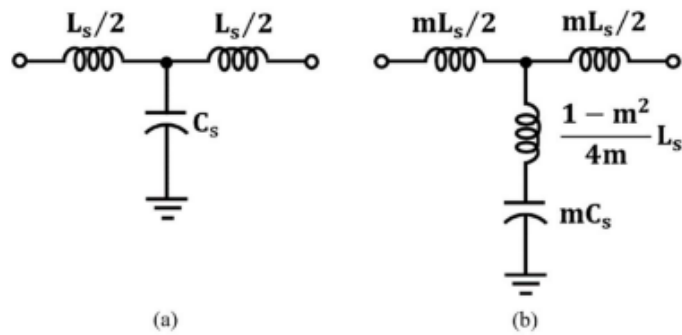


Figure 9 Low-pass filter T-section: (a) constant-k section and (b) m-derived section (Reprinted from [10])

As a result of this architecture, [10], a gain of about 12dB was achieved with a frequency range of DC-12GHz. the  $OP_{1dB}$  is reported as 12.44 dBm at 200 MHz with %12.15 PAE. The overall power consumption is 666 mW with a 6V supply voltage. lastly, the overall size of the design is  $2.23 \text{ mm}^2$  on 250nm CMOS technology.

One way to solve the biasing problem of DPA, as mentioned earlier, is presented in [9]

. A folded pseudo-differential distributed driver is proposed in Figure 10. In this architecture, two NMOS and two PMOS transistors are stacked which solves the biasing problem mentioned earlier. The DC biasing of the gain stage is solved due to PMOS sourcing the DC current from the DC supply without the need for bias-T, as shown in Figure 11. Moreover, stacking the transistors improves the stability of the system, by increasing the isolation between the input and output.

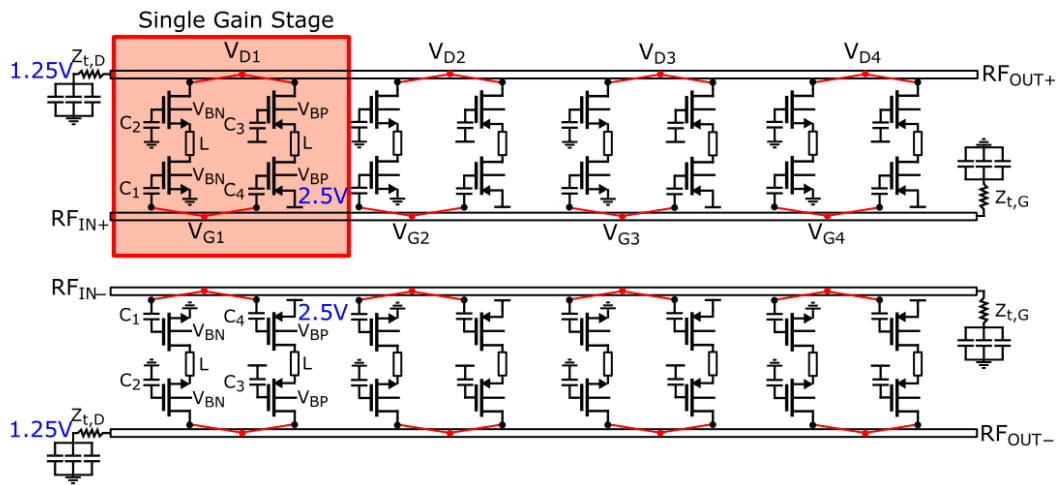


Figure 10 folded pseudo-differential distributed driver schematic (Reprinted from [9]).

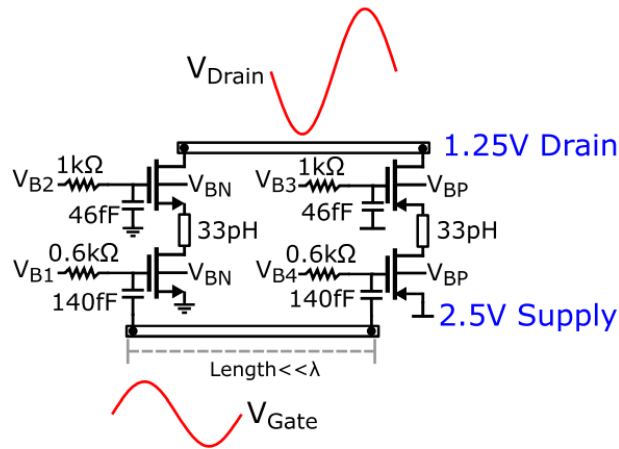


Figure 11 distributed driver gain stage (Reprinted from [9])

With this architecture, the gain of 11.6 dB is achieved with the bandwidth from 0.4-31.6 GHz. The PAE in this work is reported between % 4.8-8.3, while the  $OP_{1dB}$  is about 11.5 dBm. However, the core area of this design was reported as  $0.5 \text{ mm}^2$ , in 22nm FDSOI technology, which is relatively large [9].

Another architecture is proposed in [7] and is called multi-driver stacked topology as shown in Figure 12, where it consists of 8 stages using a 4-stacked gain unit with input and output CPW TL. In this design, elevated CPW TL is used, where the signal line is placed higher than the ground strips. Doing so allows for higher  $Z_0$  without need to decrease signal linewidth. As the operating frequency increases, the importance and the effect of parasitic are more significant. As shown in Figure 13, as the frequency increase, the effect of  $C_{gs}$  of the stacked transistor is more dominant, therefore, part of the “ $i_{D1}$ ” goes through that  $C_{gs}$ , which is called “ $i_{rc2}$ ”. Therefore, less current is delivered to the load, which means less output power. In this topology, by driving the second stacked transistor ( $M_{2CG}$ ) the “ $i_{rc2}$ ” current is compensated by “ $i_x$ ” which is produced by the  $M_{2CG}$ , which in this case, the same current “ $i_{D1}$ ” can be delivered to the load. Since this effect is more on

higher frequencies, a small transformer (T1) is used for driving the stacked transistors, to ensure that its effect is applied only at high frequencies. Moreover, by applying these intra-stacked coupled inductors, the input TL loss will be compensated, due to an increase of the effective transconductance ( $G_m$ ) at higher frequencies, which results in flat gain over the bandwidth [7].

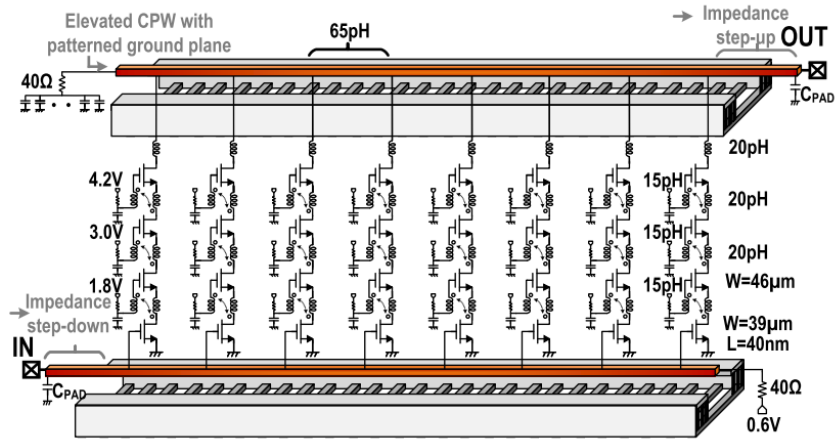


Figure 12 multi-drive stacked topology (Reprinted from [7])

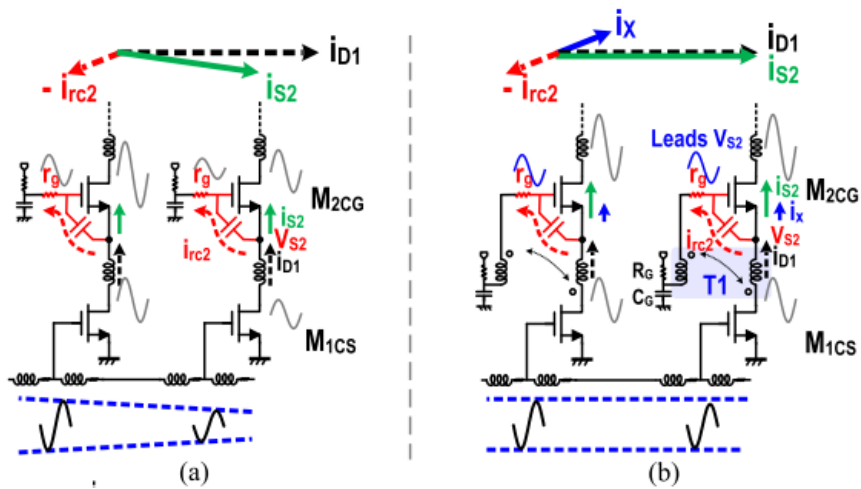


Figure 13 (a) Conventional Stacked and (b) multi-drive stacked topologies (Reprinted from [7])

As a result of this topology, the gain of 16dB is achieved over 120 GHz bandwidth (DC-120GHz). The  $OP_{1dB}$  and  $P_{sat}$  are reported as 21.3 dBm and 22.6 dBm at 20 GHz, respectively. Also, The  $PAE_{P1dB}$  in this topology is about %18 with a core area of 0.51 mm<sup>2</sup> on 45nm RFSOI CMOS technology [7].

Table 2 shows a brief overview of the two distributed drivers which were discussed above. This topology allows for ultra-wide bandwidth operation with sufficient output power, however, the distributed drivers suffer from large chip areas and sometimes, low efficiency. Therefore, due to the limited chip area for this project, distributed RF drivers cannot be the desired architecture and topology.

**Table 2 Table of comparison: Distributed RF Driver**

<b>Distributed Driver</b>	<b>[9]</b>	<b>[7]</b>	<b>[10]</b>
<b>Technology</b>	22 nm FDSOI	45nm RFSOI	250nm CMOS
<b>Gain</b>	11.6 dB	16 dB	11.54 ±1.36
<b>Bandwidth</b>	0.4 – 31.6 GHz	120 GHz <	DC-12 GHz
<b>Psat</b>	14.2 dBm	22.6 dBm @ 20GHz	--
<b>OP1db</b>	11.5 dBm	21.3 dBm @ 20GHz	16.44 dBm @ 0.2 GHz
<b>Supply Voltage</b>	2.5 V	4.2 V	6.0 V
<b>Area</b>	0.5 mm <sup>2</sup>	0.51 mm <sup>2</sup>	2.2327 mm <sup>2</sup>
<b>PAE</b>	% 4.8 – 8.3	% 18	%12.15
<b>DC consumption</b>	238 mW	--	666 mW

## 2.2 Stacked Driver

The more advanced sub-micron CMOS technologies have many advantages such as lower parasitic, and higher unity-gain frequency. However, as the devices are getting smaller, their breakdown voltage reduces, in which, a large voltage swing across the transistor's terminals may cause too much stress on them. Also, the maximum supply voltage that can be used is limited to the device breakdown voltage. Several approaches are proposed in the literature, which combine the power of multiple devices. Among them, cascode configurations have been commonly used to improve the gain performance. As shown in Figure 14, common-source and common-gate transistors are placed in series to allow a larger voltage swing amplitude at the drain of the common-gate device [3]. This configuration can solve the limitation of the supply voltage. For instance in Figure 14, the VDD can be increased up to two times the device breakdown voltage. Yet, the common-gate transistor is still experiencing more stress, compared to the common-source device, especially across its drain and gate terminal, since the gate of this device is AC ground.

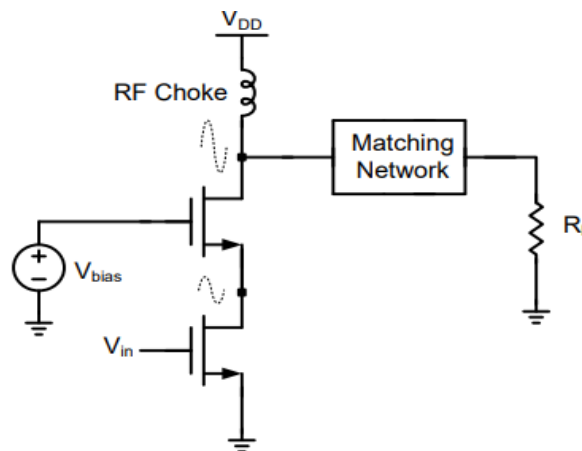
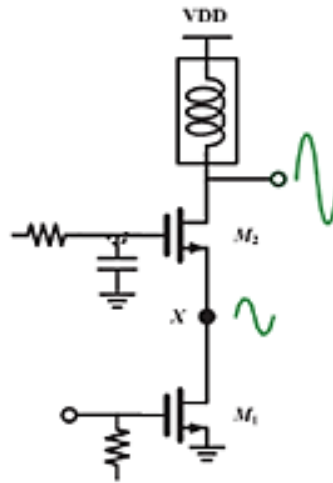


Figure 14 Cascode configuration (Reprinted from [3])



To reduce the stress on the common-gate transistor, a small capacitor is added at the gate of the cascoded device and then it is biased through a large resistor, Figure 15. This technique allows an RF swing at the gate of the cascode device, which is in phase with its drain RF swing. Doing this reduces the gate-drain voltage difference, therefore, the device experiences less stress. Additionally, the gate capacitor can control the real part of the source input impedance of the stage, which will be discussed more in detail later in this chapter. To increase the overall gain of the system, multiple stacked transistors can be placed and biased so all of the transistors experience the same stress, both in DC and AC signal, over all three terminals. For instance, if there are  $K$ -stacked transistors, the overall system can tolerate  $K.V_{\max}$ , where  $V_{\max}$  is the voltage value close to the device's breakdown voltage. Moreover, as is shown in Figure 15, an RF choke is placed after the VDD. The RF choke blocks the high-frequency RF signals and allows DC signal to pass. Also, RF choke has an inductive-peaking effect at higher frequencies which can increase the bandwidth of the system. Using the RF choke increases the overall efficiency of the system since there is no loss across the choke compared to resistive loading.



**Figure 15 Two-Stacked Transistor with Choke inductor (Reprinted from [11])**

To increase the output power of stacked PA, multiple transistors can be used on top of each other. However, after a certain number of stacked devices, the growth of output power becomes insignificant, though, the power consumption increases. Therefore, there is an optimum number of stacked devices that can be used. As shown in Figure 16, up to about 4 stacked devices, with a constant current, the increase in saturation power is more than 1X, however, beyond that, there is not much of a change on  $P_{sat}$  [12]. Therefore, the optimum number of stages is usually between 3 and 4 stages. For the fixed loading impedance  $R_L$ , by stacking K transistors, the current in each transistor increases, therefore, the overall power increases by  $K^2$ . However, due to the increase of parasitic as the devices become larger, the gain of transistors decreases severely, as is shown in Figure 16.

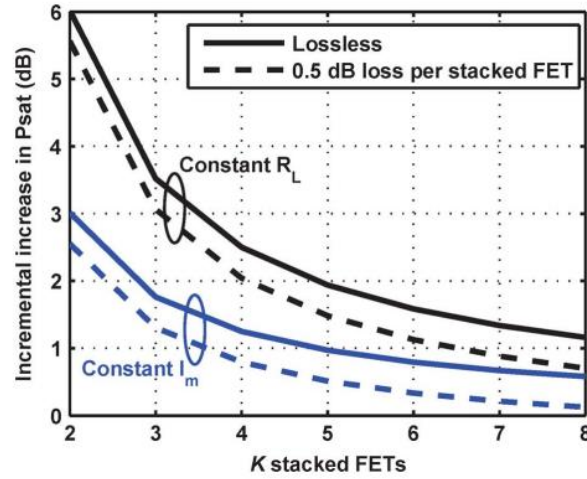


Figure 16 Effect of the number of stacked transistors on Psat (Reprinted from [12])

As previously mentioned, the stacked driver consists of one common source and multiple common-gate amplifiers. Figure 17 shows  $n$ -stacked transistors ( $n = 3$ ). Since the transistors are connected in series, the voltage of the drain and source of each stage are in phase, and the total voltage swing of the  $n^{\text{th}}$  transistor is “ $n$ ” times larger than the drain-source voltage swing of the first stage ( $V_m$ ). In the meantime, the overall current swing ( $I_m$ ) does not change. Therefore, the output impedance of the first stage can be calculated as  $Z_{L1} = \frac{V_m}{I_m} = Z_{\text{opt}}$ . As stated before, to make sure each transistor experiences the same stress, the  $n^{\text{th}}$  stage should experience  $n \cdot V_m$ , thus

$$Z_{Ln} = n \cdot \frac{V_m}{I_m} = n \cdot Z_{\text{opt}} \quad (2.9)$$

Additionally, the optimum load impedance of the  $n$ -stacked transistor  $Z_{Ln}$  can be synthesized close to the  $50 \Omega$  load, which allows a simpler matching network and better matching over a wide range of frequencies [13]. By doing so, each transistor experiences

at most,  $V_m$  voltage swings across their drain-source terminals, in which, the  $V_m$  is less than the device breakdown voltage.

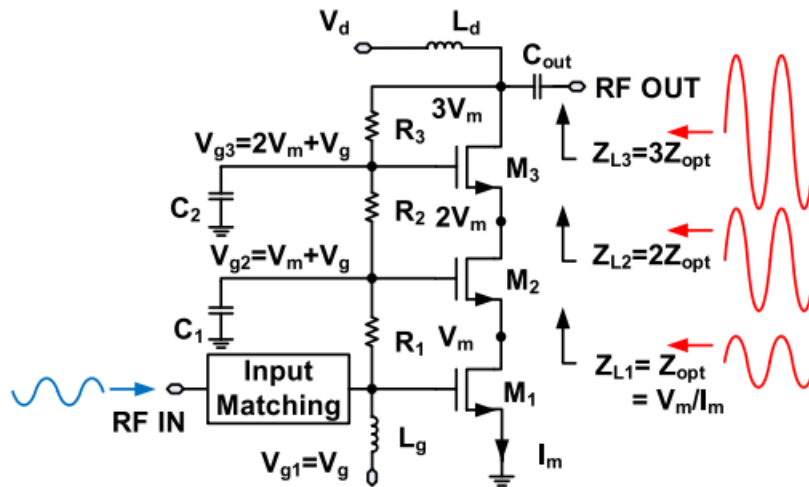


Figure 17 3-stacked driver with resistive biasing network (Reprinted from [13])

To control the  $Z_{Ln}$ , there are two-degree-of-freedom. Figure 18 shows the  $k^{\text{th}}$  transistor model, in which,  $Z_{sk}$  is the source input impedance of that stage.

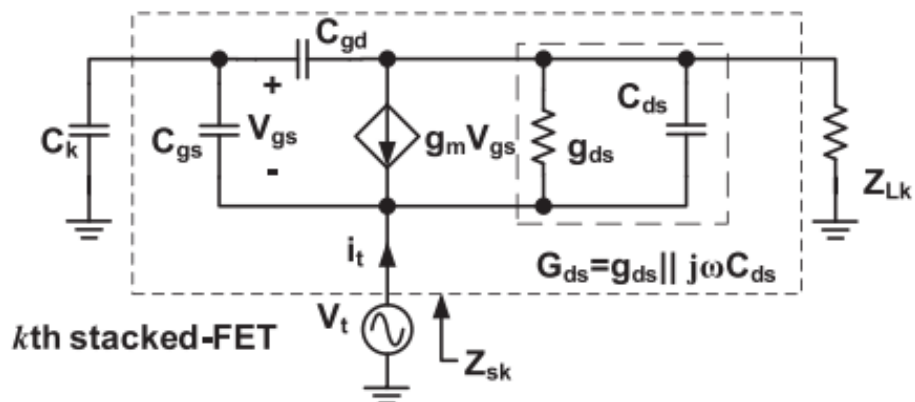


Figure 18 Source input impedance of  $k^{\text{th}}$  transistor (Reprinted from [13])

As reported in [13], the source input impedance of the  $K^{\text{th}}$  stage can be calculated as

$$Z_{sk} = \frac{C_{gs} + C_k}{(g_m + j\omega C_{gs})C_k} \approx \frac{(C_{gs} + C_k)}{g_m C_k} \quad f_0 \ll F_t \quad (2.10)$$

Where  $C_{gs}$  is gate-source capacitance,  $g_m$  is transconductance, and  $C_k$  is the shunt capacitance of the gate of the transistor. It is observed in (2.10) the transconductance and the gate capacitance are inversely proportional to the source input impedance which means, by reducing  $g_m$  and  $C_k$ , the  $Z_{sk}$  increases, therefore these two parameters can be tuned to achieve the desired optimum impedance ( $Z_{opt}$ ).

The other concern in stacked driver design is the intermediate node matching. As the operating frequency increases, the effect of device parasitic is significant and causes a mismatch between the stages. Due to the large voltage swing in PA, the impedance matching between each stage is critical. Three intermediate matchings are proposed in [12], as shown in Figure 19.

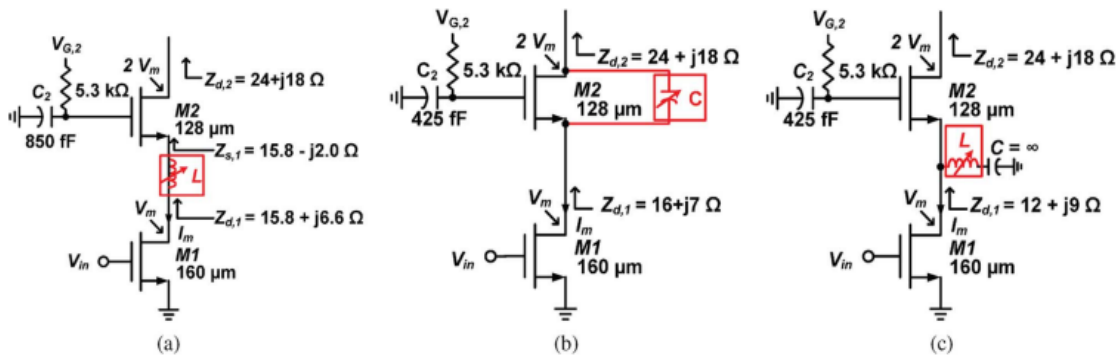


Figure 19 different intermediate matching network solutions: (a) shunt inductive tuning, (b) shunt feedback Cds tuning, (c) series inductive tuning (Reprinted from [12])

In Figure 19(a), the shunt inductive technique is used. Although, the gate capacitor,  $C_k$ , set the  $\text{Re}\{Z_{\text{opt}}\}$  to the desired value, adding a shunt inductor, can ensure the optimal phase alignment [12]. Figures (b) and (c), have the same purpose as the shunt inductive and adjust the phase of each stage. As concluded from [12], the shunt inductive technique has the best performance among the three, which is less sensitive to inductor value error and it has higher PAE and saturation power, followed by shunt feedback capacitor and series inductive tuning. To appropriately align the phase between two stages and match the imaginary part of the impedance with the “shunt inductance” method, the following equation should be solved for  $L_K$

$$\text{Im}\{Y_{s,k+1}\} + \frac{1}{sL_K} = \text{Im}\{Y_{s,k}\} \quad \text{where } k = 1, 2, \dots, K - 1 \quad (2.11)$$

Where

$$\frac{1}{L_K} = \frac{\omega^2(C_{ds,k} - C_{ds,k-1})}{k} + \frac{\omega^2 C_{gs,k+1}}{kg_{m,k+1}R_{\text{opt}}} + \frac{\omega^2(C_{gs,k} + kC_{dsub,k})}{k} \quad (2.12)$$

Many device-stacking technique modifications have been studied in the literature in recent years. For instance, in [14], a transformer-coupled stacked-FET RF driver was reported with 900-MHz bandwidth, in which, multiple on-chip transformers were used to couple the input signals into all stacked transistors, as is shown in Figure 20(a) and (b). Figure 20 (a) shows the simplified 4-stacked design, where Figure 20 (b) shows the

detailed 2-stacked architecture with the value of the components. However, using transformers in this design makes it relatively bulky and also limited in bandwidth.

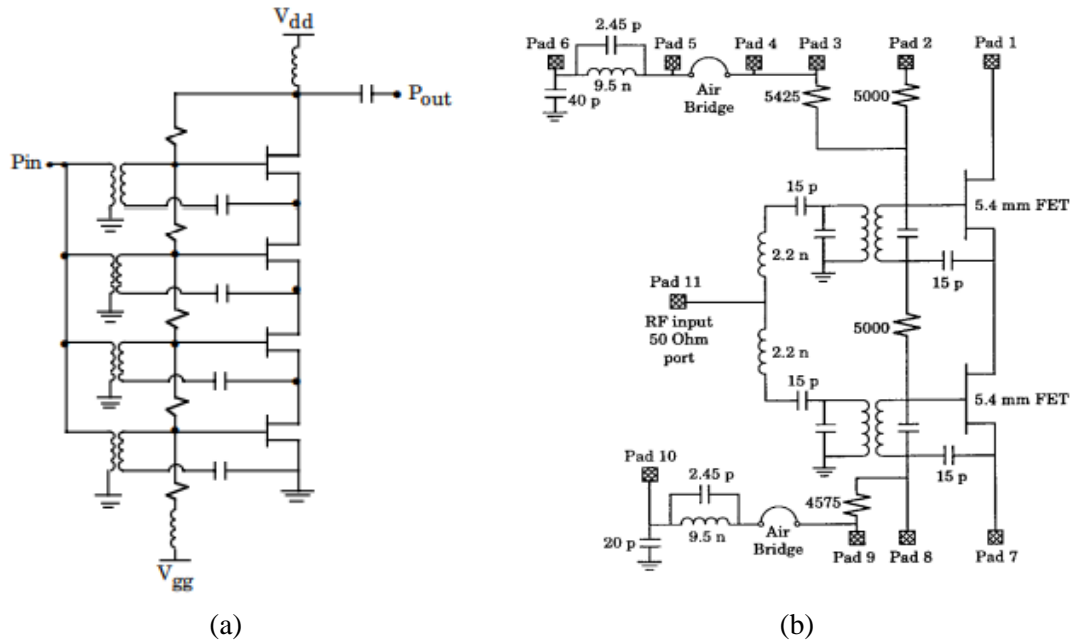


Figure 20(a) simplified 4-stacked Transformer-coupled input-feed technique, (b) 2-stage Transformer-coupled input-feed technique (Reprinted from [14])

Three different stacked-transistor designs are compared in [15]. As shown in Figure 22, 3-stack n-MOSFET, 4-stack n-MOSFET, and 3-stack CMOS structures are used. These stacked transistors are biased through the resistive biasing system, which, biases each transistor without the need for an external bias point. Moreover, each stacked transistor has a relatively small gate capacitance connected in parallel as discussed before. However, on (a) and (b), a varactor is connected to the gate of the top transistor in the stack. Doing so allows controlling the output impedance of the system, to eliminate the need for an extra matching network, as shown in Figure 21.

$$Y_{OUT} \approx \frac{g_0 C_{var}}{C_{var} + C_{gd}} + j\omega(C_{gd} + C_{db})$$

(2.13)

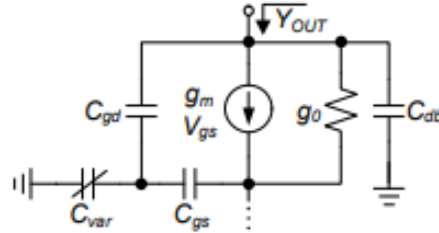


Figure 21 high-frequency transistor model with output admittance (Reprinted from [15])

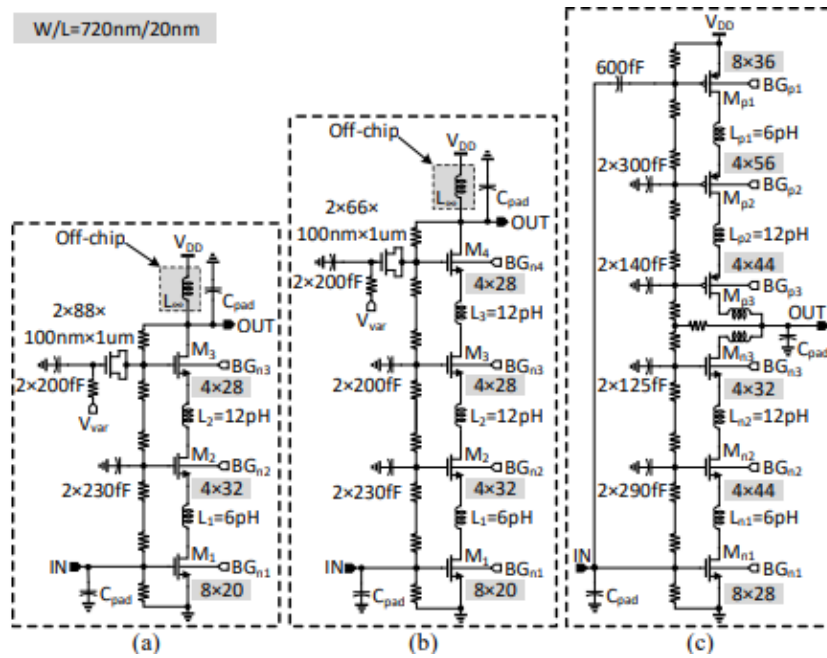


Figure 22 (a) 3-stack n-MOSFET, (b) 4-stack n-MOSFET, and (c) 3-stack CMOS (Reprinted from [15])

Where  $g_0 = \frac{1}{r_o}$  which is the intrinsic output conductance of the MOSFET, and  $C_{VAR}$  is the overall gate-to-ground capacitance of the last stack. As a result of investigating these three configurations, the following outcomes were achieved. Table 3 and Figure 23 show that the “3-stack CMOS” design suffers from high power consumption, which makes this design



inefficient, and relatively limited bandwidth. However, 3 and 4-stack n-MOS designs have less power consumption, higher  $OP_{1dB}$ , and wider bandwidth.

Table 3 Achieved outcomes in (Reprinted from [15])

Output Stage	Psat/P1db	Pdc @ 28GHz
3-stack CMOS	17.5/10.4 dBm	230 mW
3-stack n-MOSFET	15.5/11.2 dBm	107 mW
4-stack n-MOSFET	16.4/11.6 dBm	140 mW

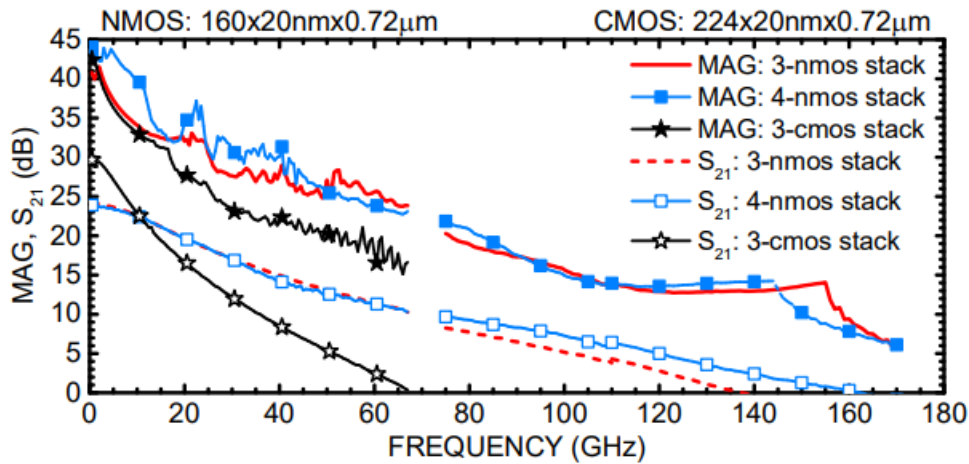


Figure 23 3-stacked nMOS, 4-stacked nMOS, and 3-stacked CMOS architecture (Reprinted from [15])

A similar architecture was proposed in [13]. In this design, a feedback resistor is placed from the output of the driver to its input as shown in Figure 24. By changing the value of the  $R_f$ , gain, bandwidth and the stability of the system can be controlled. For instance, in [13], as the  $R_f$  value changed from  $300 \Omega$  to  $100 \Omega$ , the gain decreased by half, but the bandwidth increased. Also, the stability improved as the  $R_f$  increased. To achieve

the desired gain in [13], two 3-stacked PAs are connected in series, in which the output for the first stage will be amplified by the second stage.

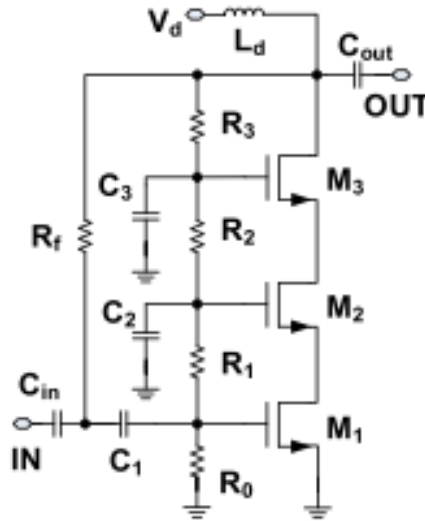


Figure 24 Stacked topology with feedback resistor  $R_f$  (Reprinted from [13])

The overall gain of 20dB is achieved with 3dB bandwidth, over 0.1-6.5 GHz frequency. The maximum P1db and PAE are reported as 19dBm and %13-20, respectively. [13] is implemented in 0.18-um technology with an overall area of 0.64 mm<sup>2</sup>.

With the same stacked topology in [16], the 8 dB gain is achieved over 89 GHz bandwidth. The saturation power, P1dB, and PAE are reported as 17dBm, 11.5dBm, and %9, respectively. Moreover, the driver core area is 0.06 mm<sup>2</sup> in 44nm SOI CMOS technology [16].

Another stacked driver is proposed in [17] with an intrinsic parasitic feedback network biasing method. In this topology, instead of the conventional cascode configuration with a single capacitor at the gate of each transistor, an  $R_{gn}$ ,  $L_{gn}$ , and  $C_{gn}$

passive circuit is used to bias the transistors, as shown in Figure 25. Adding the  $R_{gn}$ ,  $L_{gn}$ , and  $C_{gn}$  changes the source input impedance which can be calculated by

$$Z_{s,i} \approx \frac{1}{g_{m,i}} \frac{\left(1 + sR_{gn}(C_{gs,i} + C_{gn}) + s^2L_{gn}(C_{gs,i} + C_{gn})\right)}{1 + sC_{gn}L_{gn} + s^2C_{gn}R_{gn}} \cdot \left(\frac{1}{1 + \frac{s}{\omega_T}}\right) \quad (2.14)$$

Where additional high-frequency zeros were introduced due to the existence of  $R_{gn}$  and  $L_{gn}$  which cause a bandwidth extension. Additionally, an interstage inductor,  $L_m$ , was inserted to neutralize the effect of  $C_{gd}$  and  $C_{gs}$  parasitic capacitors. In comparison with the conventional biasing network, this method provides 1.5X bandwidth extension, at a cost of %33 larger chip area [17]. Moreover, this technique improves the jitter and amplitude of the driver by about %10-12.

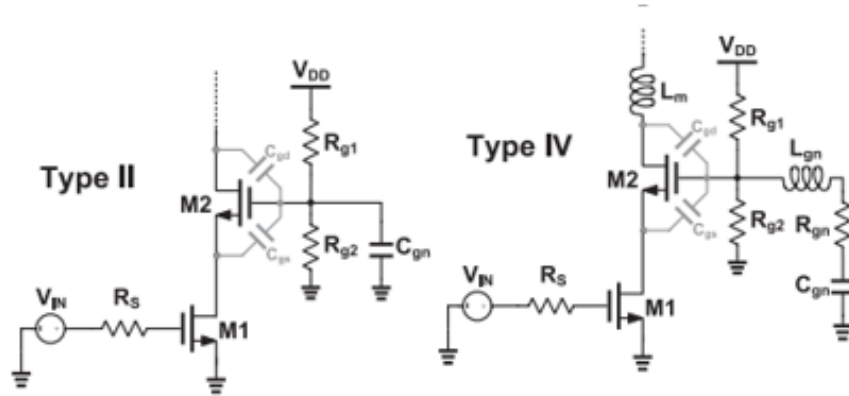


Figure 25 Type II: Conventional biasing; Type IV: proposed intrinsic parasitic feedback biasing network (Reprinted from [17])

Table 4 shows brief a comparison between the discussed stacked drivers. As is discussed, this topology is more compact, compares to distributed drivers. The gain and the bandwidth of this topology are sufficient for the purpose of this project. However, there are some improvements needed for the output power.

**Table 4 Table of comparison: Stacked RF Driver**

<b>stacked Drivers</b>	<b>[15]</b>	<b>[15]</b>	<b>[15]</b>	<b>[16]</b>	<b>[18]</b>
<b>Technology</b>	22nm CMOS	22nm CMOS	22 nm FDSOI	45nm SOI	45nm SOI
<b>Gain</b>	~ 30 dB	~ 24dB	~ 24 dB	8 dB	12.4 dB
<b>Bandwidth</b>	0.5 – 39 GHz*	DC – 39 GHz*	DC – 39 GHz*	88-90 GHz	81-96 GHz
<b>Psat</b>	7.5 dBm @ 28GHz	15.5 dBm @ 28GHz	16.4 dBm @ 28GHz	17 dBm	19.2 dBm
<b>OP1db</b>	10.4 dBm @ 28GHz	11.2 dBm @ 28GHz	11.6 dBm @ 28GHz	11.5 dBm	--
<b>Supply Voltage</b>	4.8 V	2.4 V	3.2 V	4.2 V	3.4 V
<b>Area</b>	--	--	--	0.06 mm <sup>2</sup>	0.228 mm <sup>2</sup>
<b>PAE</b>	% 14.2	% 33.4	% 28.3	% 9	% 14
<b>DC consumption</b>	230 mW	107 mW	140 mW	382 mW	--

\*The reported value is not the 3dB-Bandwidth

### 3. PROPOSED RF DRIVER

#### 3.1 22nm-FDSOI

The proposed architecture is designed using the 22nm FDSOI Global Foundries process. The FDSOI stands for fully-depleted Silicon on Insulator. The main difference between this technology and the Bulk CMOS is that an ultra-thin layer of buried oxide (BOX) is placed as an insulator on the base silicon, in which, the channel will be formed on top of the BOX. In contrast to the bulk CMOS where dopants must be added to the channel, FDSOI eliminated this necessity due to the BOX. Hence the process is called fully depleted. Figure 26 compares the cross-section of Bulk and FDSOI CMOS [19].

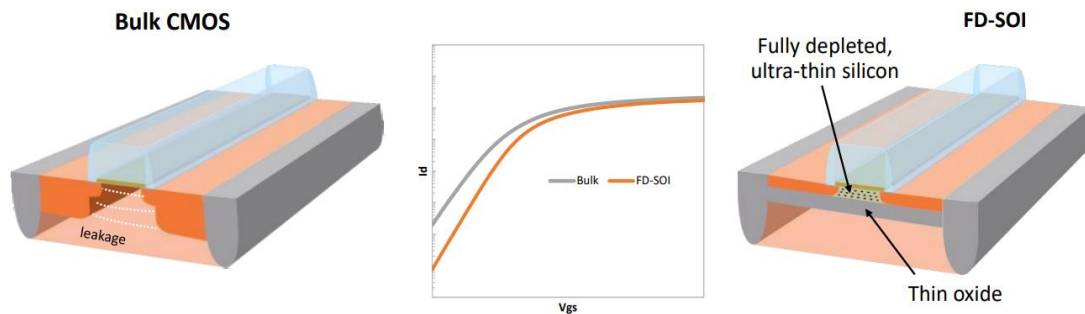


Figure 26 Bulk CMOS Vs. FDSOI CMOS technology (Reprinted from [19])

The FDSOI technology has a shorter channel length as compared to a bulk CMOS, which allows for higher operating speed since the electron must travel a shorter distance. Moreover, lower gate leakage and smaller junction capacitance are some of the other benefits of this technology. Also, since there is no doping needed, the number of steps in the fabrication process is reduced.

The other feature of this technology is to have an access to bias the device from the bulk, or called “back-gate”. As shown in Figure 26, the drain/source of the device is separated from the bulk by a thin layer of insulator, which prevents the device from latch-up at lower voltages. Moreover, the channel is separated from the bulk. Therefore, the bulk voltage can go to a much higher voltage which can act as a secondary gate. Because of this feature, the process allows for a “flip well” technology, where the PMOS transistors are placed in P-Well and NMOS transistors in N-Well, which is the opposite of a conventional well. Some of the benefits of the flip well technology are lower threshold voltage ( $V_{th}$ ) which leads to faster switching and higher drive capability [19]. In this design, a super-low- $V_t$  (SLVT) device is used, with about 70mV/V threshold voltage varying depending on the back gate voltage. As reported in [9] and [20], the maximum  $f_t/f_{max}$  in this technology is 357/290 GHz for NMOS and 260/250 GHz for PMOS devices, which allows PMOS devices to be suitable for RF application and higher operating frequencies too.

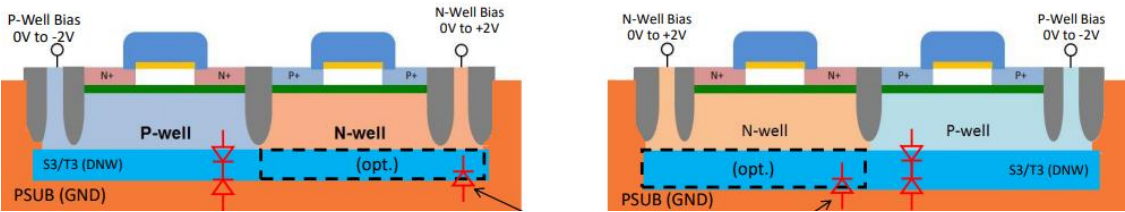


Figure 27 Comparison between flip-well (right) and conventional well (left) (Reprinted from [19])

This technology also offers a wide range of MOM capacitors, as well as alternative polarity MOM (APMOM) with a good quality factor. APMOM5V and APMOM3.3V are

used in this design between layer 1 and layer 7 to achieve relatively large capacitance with a good quality factor.

This process offers a range of back-end-of-line (BEOL) metals. Figure 28 shows the cross-section of stack-up metals.

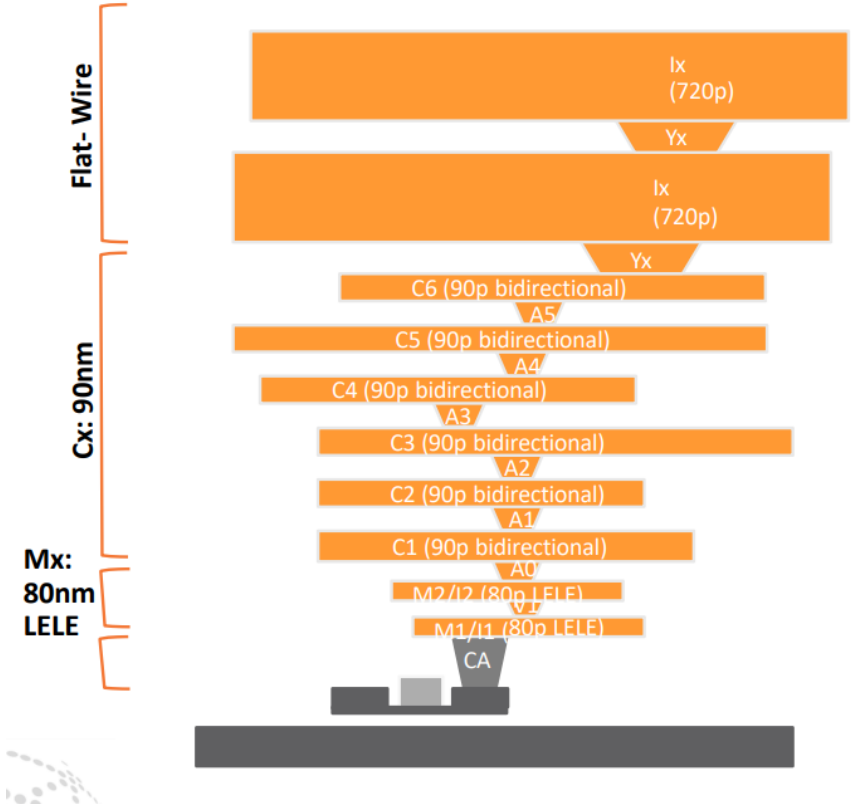
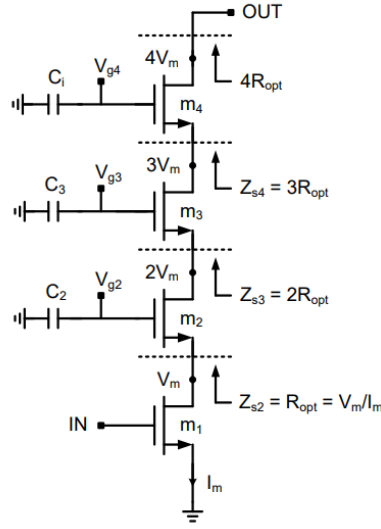


Figure 28 BEOL visualization of 22nm FDSOI (Reprinted from [19])



### 3.2 Stacked RF Driver

As mentioned earlier, the advanced sub-micrometer technologies are suffering from the low breakdown voltage of the devices, which makes it hard to achieve high-power and high-frequency RF drivers. To overcome these limitations, power combining techniques are developed to combine the power over multiple stages, such as the transistor stacking technique. This circuit is composed of a common-source input stage and three common-gate stages connected in series so that the output swings are added in phase. This technique can solve the two major problems in these technologies. First, this technique can support higher supply voltage, therefore, a higher RF voltage swing is achievable. For instance, assuming the breakdown voltage of a device is 0.8 V, in 4-stack PA, the supply voltage can go as high as 3.2 V, which is four times higher than the breakdown voltage of the device, as shown in Figure 29. Second, due to the structure of this technique, a simpler and smaller matching network is required, which results in lower power loss due to the matching network, and smaller area. However, this technique has some limitations at millimeter-wave bands such as limited efficiency due to coupling losses and parasitic of devices and wiring [18].



**Figure 29 Proposed 4-stack NMOS basic structure (Reprinted from [4]).**

The main concern in stacked driver design is an equal division of the voltages, RF and DC. Since the supply voltage in the n-stacked driver technique is “n” times higher than the breakdown voltage of each transistor, it is critical that each transistor experience the same drain-source DC voltage, equal to its breakdown voltage, otherwise, there will be a reliability issue for the device. In this design, a class-A biasing is chosen due to its high linearity, at a cost of more power consumption. In the class-A biasing technique, the biasing point should be well above the threshold voltage of the device so that there is a full voltage swing across the  $V_{GS}$ , as shown in Figure 30 [4]. The drain current in class A driver is

$$i_D = K_{sat}(V_{GS} - V_t) + K_{sat} \cdot V_{gsm} \cos(\omega t) = I_D + I_m \cos(\omega t) \quad (3.1)$$

Where  $I_D$  is DC component of drain current,  $I_m$  is the maximum amplitude of the AC component, and  $K_{sat}$  is the device parameter of the transistor. Furthermore, the maximum

amplitude of the AC component of the drain current is specified by  $I_{m,max} = I_D$  to prevent distortion on the signal [4].

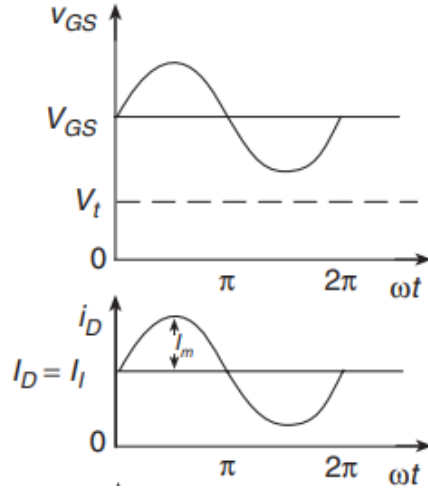


Figure 30 Class-A biasing point (Reprinted from [4])

Figure 29 shows an  $n$ -stacked driver ( $n = 4$ ), in which, one common source and three common-gate gain stages are connected in series. Assuming the voltage swing across the common-source transistors is  $V_m$  and the drain-source AC current is  $I_m$ , the  $Z_{S2}$  can be calculated as

$$Z_{S2} = \frac{V_m}{I_m} = Z_{opt} \quad (3.2)$$

To make sure each transistor has an equal drain-source voltage swing, the next stage also needs to have  $V_m$  swing across its drain and source terminals, and since the drain voltages of each stage are in phase, therefore the overall swing at the drain of the second stage will be  $Z_{S3} = \frac{2 \cdot V_m}{I_m} = 2 \cdot Z_{opt}$ , which can be generalized for the  $n^{\text{th}}$  stage as

$$Z_{s,(n+1)} = \frac{n \cdot V_m}{I_m} = n \cdot Z_{opt}$$

(3.3)

As discussed before, adding  $C_i$ , the gate voltage swing can be controlled which, in contrast with the cascode configuration, this structure reduces the drain-gate and drain-source swing which cause more reliable transistor operation. However, there is a tradeoff between the gain of the driver and its saturation power and drain efficiency. By adding the gate capacitance, the overall gain of the system reduces, however, the saturation power and drain efficiency increase. To compensate for the small gain degradation, more stacked devices can be used.

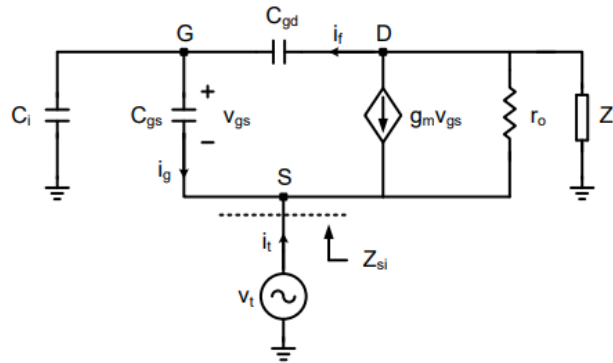


Figure 31 high-frequency stacked-transistor model (Reprinted from [3])

Figure 31 shows the high-frequency stacked-transistor model, where  $Z_L$  is the loading impedance seen by the drain of that device. Assuming  $r_o$  is large, the test voltage  $V_t$  can be applied to the source of the device. By applying the KCL and KVL

$$V_t = \frac{i_f - i_g}{sC_i} - \frac{i_g}{sC_{gs}}$$

(3.4)

$$-i_t = i_g + \frac{g_m i_g}{sC_{gs}} \quad (3.5)$$

$$-i_f = \frac{g_m i_g}{sC_{gs}} + \frac{v_{ds} + v_t}{Z_L} \quad (3.6)$$

$$v_{ds} = \frac{i_f}{sC_{gd}} + \frac{i_g}{sC_{gs}} \quad (3.7)$$

$$i_t + i_g - i_f = \frac{v_t + v_{ds}}{Z_L} \quad (3.8)$$

Therefore, assuming  $f_0 \ll F_t$  and neglect the feedback current through  $C_{gd}$ , the source input impedance,  $Z_{s,i}$ , can be derived and simplified as [3]

$$Z_{s,i} = \frac{C_{gs} + C_i + C_{gd,i}(1 + g_{m,i}Z_{d,(i+1)})}{(g_m + sC_{gs})(C_{gd} + C_i)} \approx \frac{C_{gs} + C_i}{g_m C_i} \quad (3.9)$$

To achieve the optimum load line impedance and make sure each transistor experiences the same stress, the impedance  $Z_{s,i}$  should be  $(i - 1) \cdot R_{opt}$ . Therefore, the value of  $C_2$  to  $C_4$  should be set such that  $Z_{s,2}$ ,  $Z_{s,3}$ , and  $Z_{s,4}$  are  $R_{opt}$ ,  $2R_{opt}$ , and  $3R_{opt}$ , respectively, and the optimum load impedance is  $4R_{opt}$ . This guarantees the growth of absolute voltage swings with respect to ground, but the drain-source, drain-gate, and gate-source voltage swings are the same for each transistor, which causes more reliable

operation. However, as the operating frequency increases and becomes closer to  $F_t$ , the reactance of  $Z_{s,i}$  won't be negligible anymore and needs to be considered.

From the equation above, and assuming  $Z_{s,i}$  is primarily real and  $C_{gd}$  is negligible,  $C_i$  can be calculated and simplified as: [12]

$$C_i = \frac{C_{gs} + C_{gd}(1 + g_m R_{opt})}{(i - 1)g_m R_{opt} - 1} \approx \frac{C_{gs}}{(i - 1)g_m R_{opt} - 1}$$

where  $i = 2, 3, \dots, I$

(3. 10)

The open-loop small-signal gain of the driver can be calculated as

$$A_v = \frac{g_{m1} R_L}{\left(1 + \frac{sC_{gs2}}{g_{m2}}\right) \cdot \left(1 + \frac{sC_{gs3}}{g_{m3}}\right) \cdot \left(1 + \frac{sC_{gs4}}{g_{m4}}\right)} \approx g_{m1} R_L \text{ for } f_0 \ll F_t$$

(3. 11)

One drawback of stacked topology is the stability of the system. With higher voltage swings, stability can be an issue. Figure 32 shows the small signal gain and stability factors of the driver, which is shown in Figure 24, as the feedback resistor changes. As expected, by lowering the feedback resistor value, the gain of the system drops, and the bandwidth increases. However, the stability of the system increases due to the effect of a negative feedback loop.

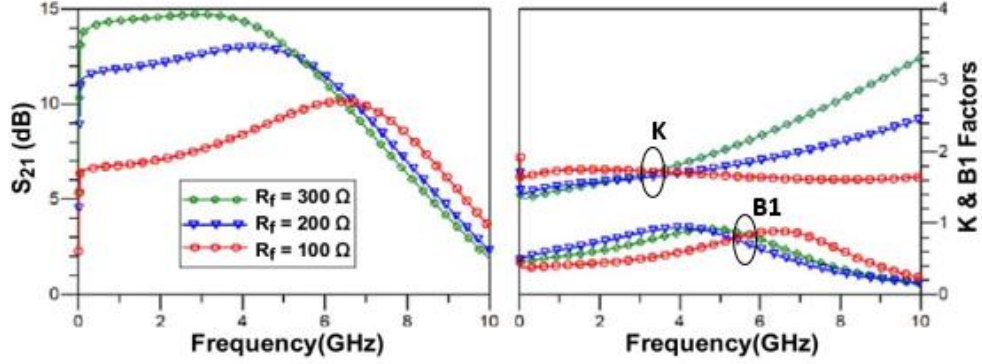


Figure 32 Small signal gain and stability factors Vs. the feedback resistor ( $R_f$ ) (Reprinted from [13])

### 3.3 Intermediate matching network

As previously mentioned, at low frequencies, the drain impedance of the  $k^{\text{th}}$  transistor,  $Z_{d,k}$ , can be approximated as a resistance and can be tuned by the gate impedance of the next stage  $C_{k+1}$ . However, as the frequency increases and reaches the millimeter-wave range, the intermediate node impedance has a significant reactance part, which causes the voltage swing not to be aligned. From Figure 33 the high-frequency admittance can be re-written as

$$Y_{\text{opt}} \approx \frac{1}{k \cdot R_{\text{opt}}} - \frac{s}{k} C_{\text{eqv},k} \quad k = 1, 2, \dots, k \quad (3.12)$$

Where

$$C_{\text{eqv},k} = C_{\text{ds},k} + kC_{\text{dsub},k} + C_{\text{gd},k} \quad (3.13)$$

Additionally, the source input impedance of the next stage can be written as

$$Z_{s,k+1} \approx k \cdot R_{\text{opt}} - \frac{kR_{\text{opt}}}{g_{m,k+1}} s(C_{gs,k+1} - g_{m,k+1}R_{\text{opt}}C_{ds,k+1}) \quad k = 1, 2, \dots, K - 1 \quad (3.14)$$

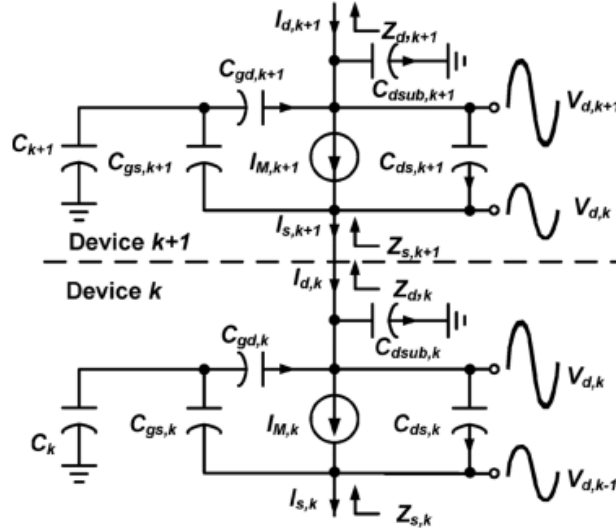


Figure 33 simplified the small-signal model of stacked transistors (Reprinted from [12])

As discussed before, to minimize the intermediate mismatch due to the reactance portion of impedance, three methods are available as previously shown in Figure 19. As shown in Figure 34, the shunt inductance method is the most effective with less sensitivity to the inductance value.

In this design, however, the intermediate matching is not used, since the maximum operating frequency is below the mm-wave range and the effect of the parasitic at the desired bandwidth is not significant.



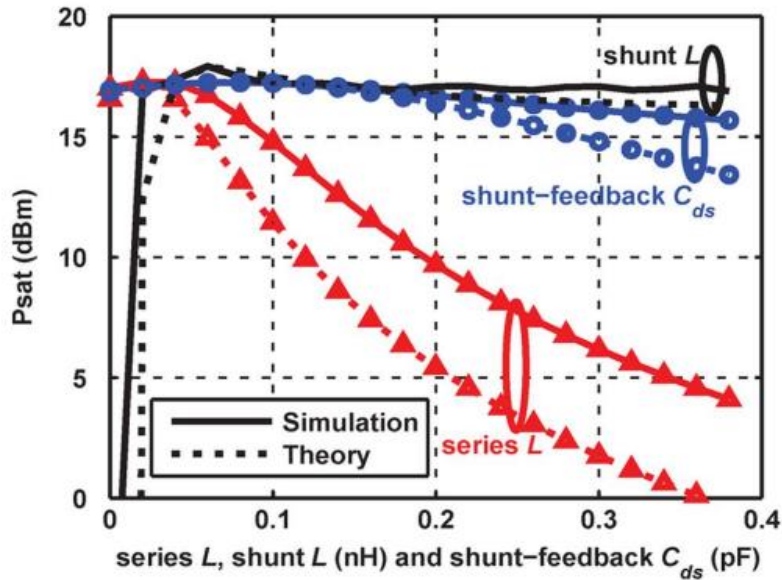


Figure 34 The comparison of different tuning methods on Psat (Reprinted from [12])

### 3.4 Fully differential Stacked RF Driver design FDOSI CMOS

A fully-differential stacked linear RF driver was designed with 17 GHz bandwidth and 20 dB voltage gain, as discussed in chapter 1, using the 22nm FDOSI CMOS process for which the drain-to-source breakdown voltage is 0.8 V [19]. The 4-stacked structure used is shown in Figure 35 together with the feedback network and on-chip input and output matching network. Three gate capacitors  $C_2 - C_4$  determined to enable voltage swing on the gate of each transistor and minimize the stress on each stage, as discussed in the earlier section. With  $50 \Omega$  single-ended output termination (input impedance of the MZM) and 200 mV input signal, the output voltage swing of about 2 V was achieved, which is necessary to properly drive the MZM.

Four SLVT-nFET transistors were used because of lower threshold voltage and faster operation. Due to higher gain for the first stage, a larger transistor was used with a

192- $\mu\text{m}$  overall gate width. A smaller transistor was used for the other three stages, to minimize the parasitic of devices, with 160-  $\mu\text{m}$  overall width for each stage. The supply voltage was chosen to be 3.2 V and the gates were biased with 0.3V, 1.23V, 2.1V, and 3V, respectively from the bottom to top transistor, so that each stage experiences the same drain-to-source DC voltage difference. Additionally, Class-A biasing was used to achieve highly linear operation, as is shown in Figure 36, where the signal is a full cycle sinusoidal signal throughout the circuit. The input and output matching networks are implemented with a high-quality factor on-chip inductor, which was designed using the Sonnet EM simulator, with 650 pH to achieve input/output matching better than -10 dB over the bandwidth. A 24-nH off-chip choke inductor was chosen to push the lower-cutoff frequency to lower frequencies. Additionally, 2-pF coupling capacitors are placed at the input and the output to decouple the DC voltage from other parts of the system.

With 50  $\Omega$  termination and having 4-stacked transistors, the  $R_{\text{opt}}$  was chosen to be about 12.5  $\Omega$ . Also, the overall output swing needed for the MZM was 2  $V_{\text{pk}}$  single-ended. Assuming, the input signal is 200 mV, the voltage swing at the drain of each stage should be 0.5 V, 1 V, 1.5 V, and 2 V, respectively so that each transistor experiences a 500-mV source-to-drain voltage swing which is below the device breakdown voltage. By considering these drain voltages, each stage has to have a gain of 2.5, 2, 1.5, and 1.33  $\frac{\text{V}}{\text{V}}$  respectively from the bottom to the top stage.

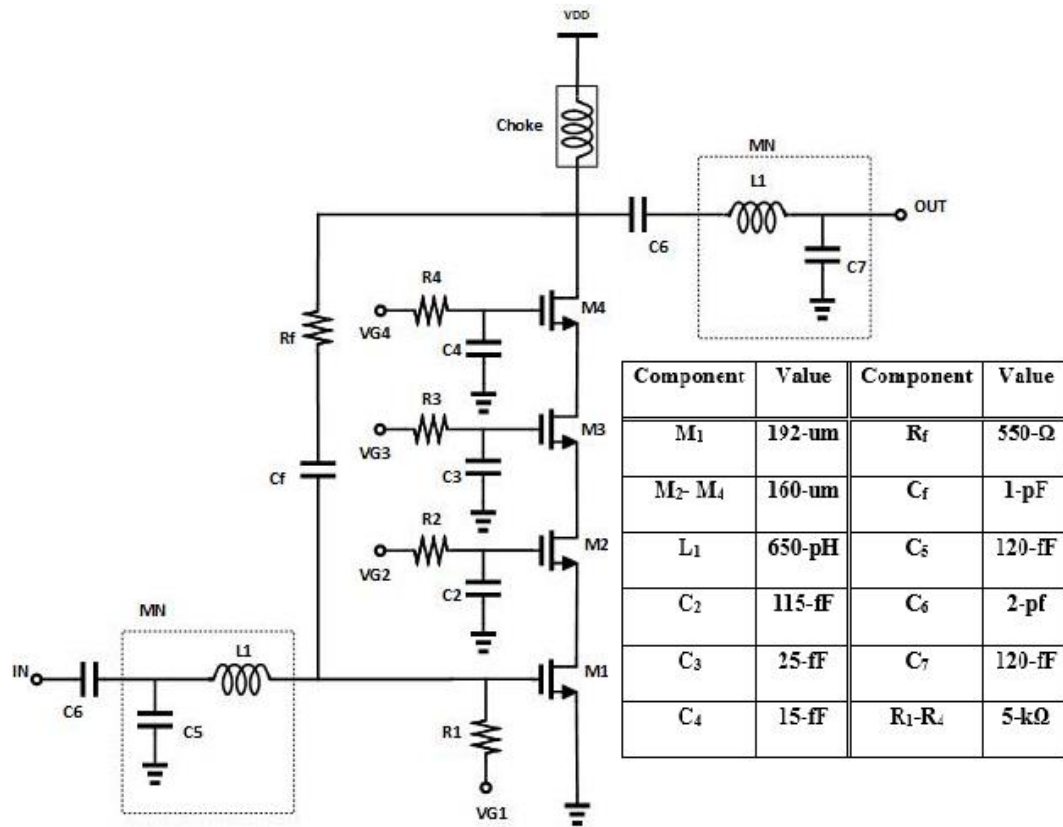


Figure 35 Proposed 4-stacked driver (single-ended) with input and output matching network

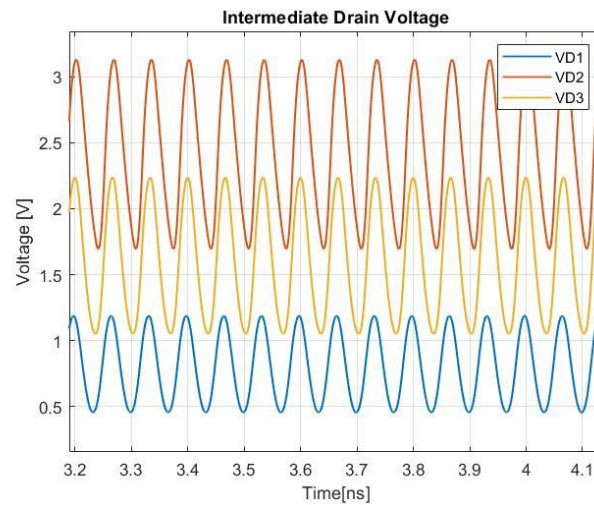


Figure 36 Intermediate drain voltages

### 3.5 Transistor sizing and biasing

In this design, sizing, and biasing of the transistors is the main aspect of the design's challenge. As discussed earlier in (3.4), the stages must have  $2.5 \frac{V}{V}$ ,  $2 \frac{V}{V}$ ,  $1.5 \frac{V}{V}$  and  $1.33 \frac{V}{V}$  gain, respectively from the first to the last stage, to achieve the overall gain of 20dB. Moreover, the DC voltages at the drain of each stage should be 0.8V, 1.6V, 2.4V, and 3.2V, to make sure the  $V_{DS,n}$  does not exceed the nominal voltage of the device. Furthermore, by having a  $50 \Omega$  load at the output of the driver, the  $R_{opt}$  for 4-stack, will become about  $12.5 \Omega$ . By knowing this information, and also, knowing the input signal swing which is  $200 mV_p$ , the transistors can be sized.

Since the first stack transistor has the highest gain, the design of this stage is slightly more challenging compared to other stages. Having the input voltage and the gain of the first stage, the drain voltage of this stage can be calculated as  $500 mV_p$  with  $800 mV_{DC}$  level, as shown in Figure 37 (a). To ensure the signal is not clipping at the bottom, the over-driver voltage,  $V_{ov}$ , should be less than the minimum of the output swing, which is  $300 mV$ , with some margin. However, because of using a choke inductor for  $VDD$  connection, the peak voltage can go as high as  $2 \times VDD$ , ideally, which in this case there is more than  $300mV$  margine. Thus, the transistor must be biased to have a small over-drive voltage while maintaining the required gain. On the other hand, due to the large input signal, which in this case is  $200mV$ , the threshold voltage also need to be minimized to make sure the first stack transistor does not go to the triode region. Having access to the back-gate on this technology, as discussed before, allows us to reduce the threshold voltage to make sure the drain voltage does not clip at its peak value as is shown in Figure

37 (b). However, from the equation (3.15), by reducing the threshold voltage, the over-drive voltage increases, therefore, the  $V_{gs}$  also need to be minimized to reduce the over-drive voltage.

$$V_{ov} = V_{gs} - V_{th} \tag{3.15}$$

Figure 38(a) shows the effect of back-gate voltage on the threshold voltage ( $V_{th}$ ) of a device. As is shown, the threshold voltage of the transistor reduces by about  $80 \frac{mV}{V}$  with maximum of  $250 mV$  and minimum of  $90 mV$ .

Additionally, Figure 38 (b) shows the effect of back-gate voltage on the  $g_m$  of the transistor. As is shown, the peak transconductance value moves to lower  $V_{GS}$  as the back-gate voltage increases. In this work, the  $2V$  back-gate voltage is chosen with about  $0.3V$   $V_{gs}$  to reduce the over-drive voltage while achieving the required gain. Also,  $192\text{-um}$  overall width is divided between 20 fingers and 8 multipliers for the first stack transistor, for power handling purposes. The same design procedure is used for other stages. However, due to the lower required gain, the smaller transistors are used to minimize the parasitic of the device.

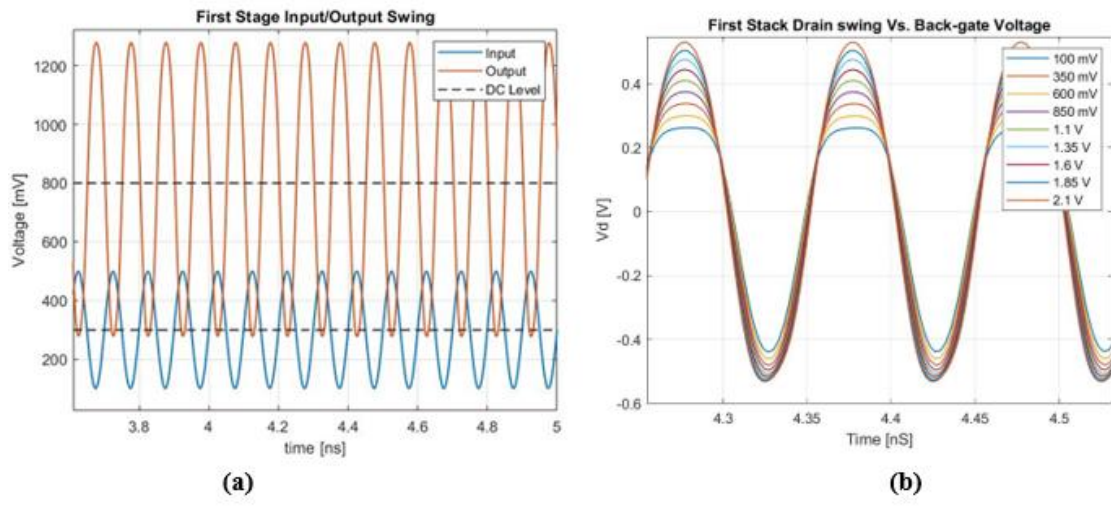


Figure 37 (a) Input/output of first stack transistor, (b) back-gate voltage effect on the first stage drain voltage

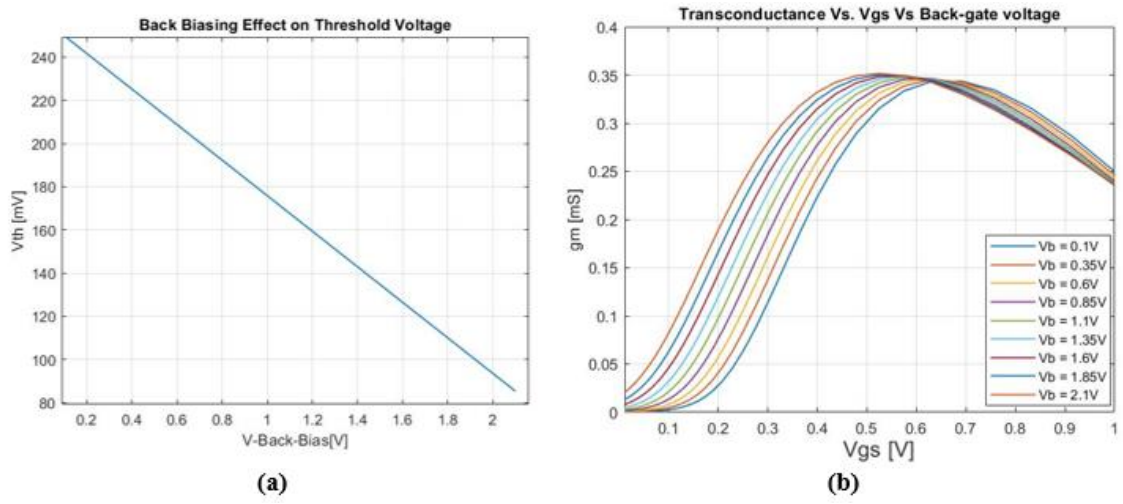
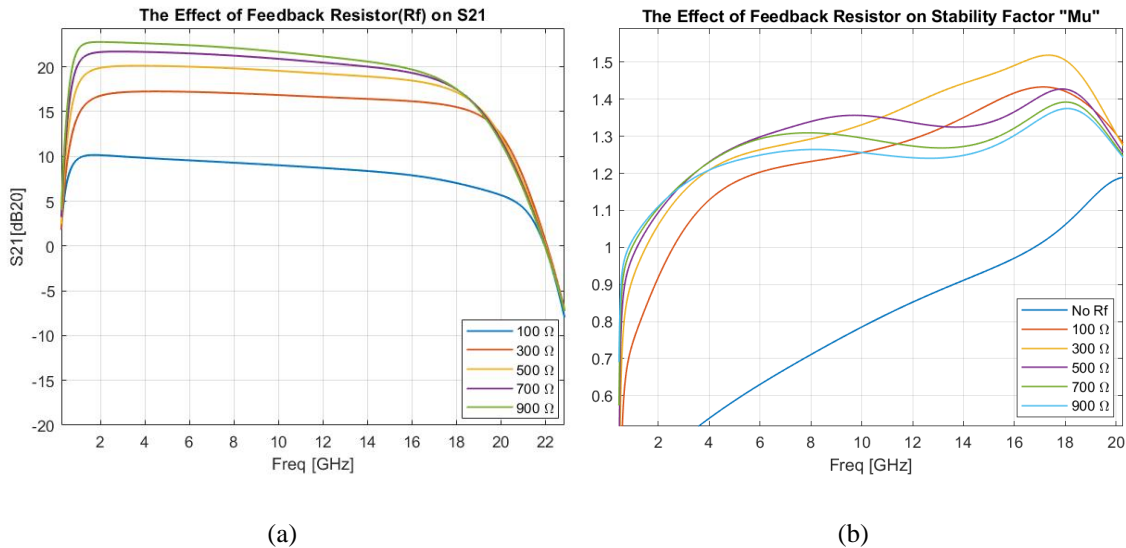


Figure 38 (a) Threshold Voltage Vs. Back-gate voltage; (b) Transconductance ( $g_m$ ) Vs.  $V_{gs}$  for different Back-gate voltages.

### 3.6 Feedback and wideband matching

In this study, the effect of resistive feedback on both gain and stability factors is observed. Figure 39 (a) shows, as the  $R_f$  reduces from  $900\ \Omega$  to  $100\ \Omega$ , the gain of the system reduces from 23dB to 10dB, but the bandwidth of the device increases, as expected. Figure 39 (b), shows the stability factor “Mu” as the  $R_f$  changes from  $100\ \Omega$  to  $900\ \Omega$ . Although, at higher frequencies, the  $R_f = 300\ \Omega$  performs better, but at low frequencies it does not. However, with  $R_f = 500\ \Omega$  better stability observed at low frequencies and high frequencies. At the end, a  $550\ \Omega$  feedback resistor was chosen to achieve desired gain and stability.



**Figure 39** Effect of feedback resistor on (a) gain, bandwidth, and (b) stability.

Another advantage of the feedback resistor is to provide broadband matching, especially at the input of the driver. However, due to the properties of this topology, which have been discussed, the output matching by itself has acceptable matching, if the right value is chosen for  $Z_{opt}$ , which in this design is about  $Z_{opt} = 12.5\ \Omega$ . Nevertheless, the L-

type matching network is used to achieve even better input/output matching. Figure 40 shows the input and the output matching versus frequency on the smith chart. As is shown, both the input and the output plot are close to the center of the smith chart.

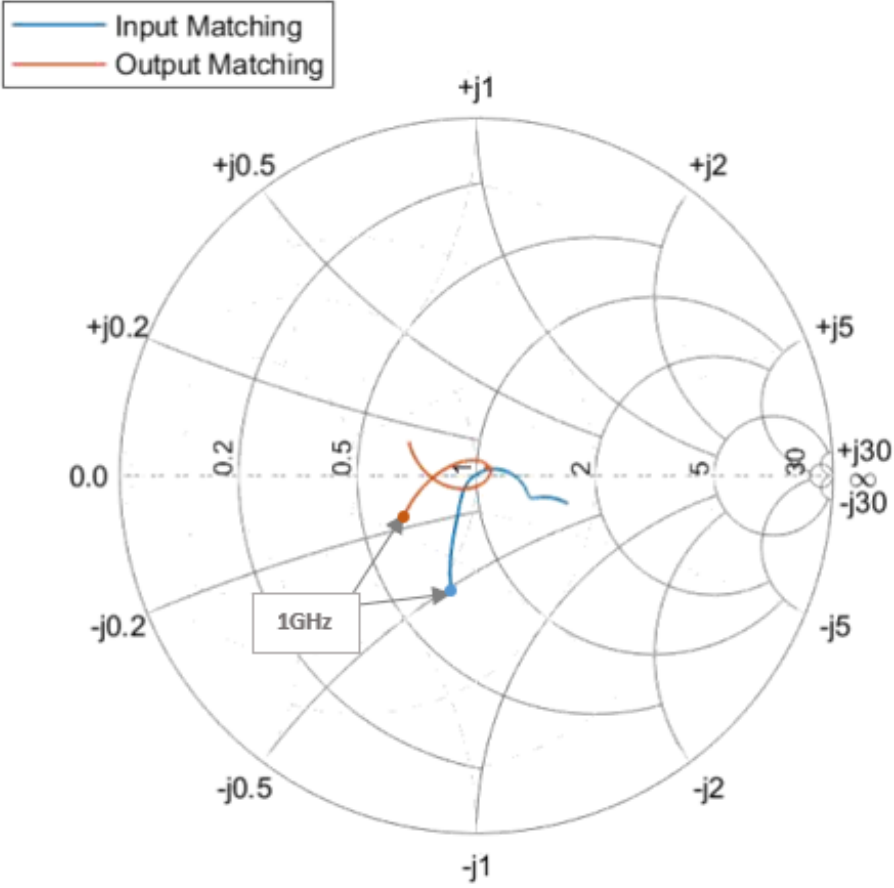


Figure 40 Input/Output matching Vs. Frequency plot from 1GHz to 17 GHz



### 3.7 Choke Inductor

In this design, the choke inductor is placed between the VDD and the circuit. Unlike the conventional resistive load, having a choke inductor has some benefits. Since the impedance looking into the choke inductor is  $j\omega L_f$ , the high-frequency input impedance to the choke inductor is very large, therefore, the choke inductor can filter out the high-frequency RF signal, and also, can minimize the parasitic effect of the device at the higher frequency. This results, in an inductive peaking which causes the extended bandwidth. Moreover, at DC, the choke inductor act as a short circuit, which means the DC signal can pass through with no voltage drop across the choke inductor. Therefore, the efficiency of the device also improves with a maximum of % 50 drain efficiency, as mentioned earlier. However, there are some challenges in designing the choke inductor. due to the limitation of the sub-micron CMOS technology, achieving a large inductance value with a decent quality factor is not possible. Also, to include the low frequency on the bandwidth, relatively, a very large inductor is needed, therefore, an off-chip inductor is a solution. But, as the operating frequency goes to a higher frequency, the self-resonant frequency (SRF) of the inductor also needs to be considered and it must be well above the maximum operating frequency. In this work, a 24-nH off-chip choke inductor is used with more than 40 GHz upper-frequency limit and a quality factor better than 20 at 10MHz. Additionally, this inductor can handle up to 500 mA current.

Figure 41 shows the effect of the choke inductor value on low cutoff frequency. As shown, the choke inductance value swept from 1-nH and 30-nH. As the inductance value increased, the cutoff frequency was pushed to a lower frequency by about 1 GHz.

Moreover, as the inductance increases, the input/output matching of the driver improves at 1GHz by about 4 dB. Additionally, a slightly higher gain was achieved with a higher inductance value, due to less loading effect at the output.

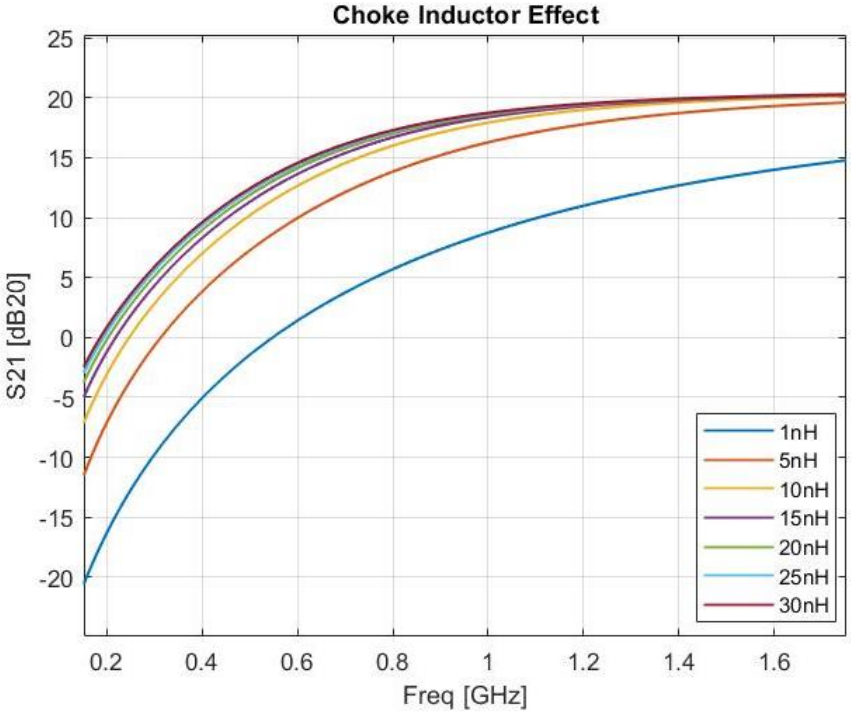


Figure 41 Choke inductor effect on the low cutoff frequency

### 3.8 Layout

The importance of applying good layout techniques at RF and mm-wave frequencies is significant, since all the wiring, pads, and passive devices may introduce parasitic that change the design parameters. Moreover, achieving large-value passive devices is not possible, due to the quality factor degradation as the reactance increases. In this project, a 650pH spiral inductor was designed using the Sonnet EM simulator with a peak quality factor of 19 for input/output matching networks, as shown in Figure 42. Additionally, four MOM capacitors are connected in parallel to form a larger capacitor for input/output coupling purposes, as shown in Figure 43. However, due to its limited quality factor, severe voltage gain drop is observed at a higher frequency, with a coupling capacitor larger than 2pF. Figure 44 shows the 2-pF MOM capacitor quality factor.

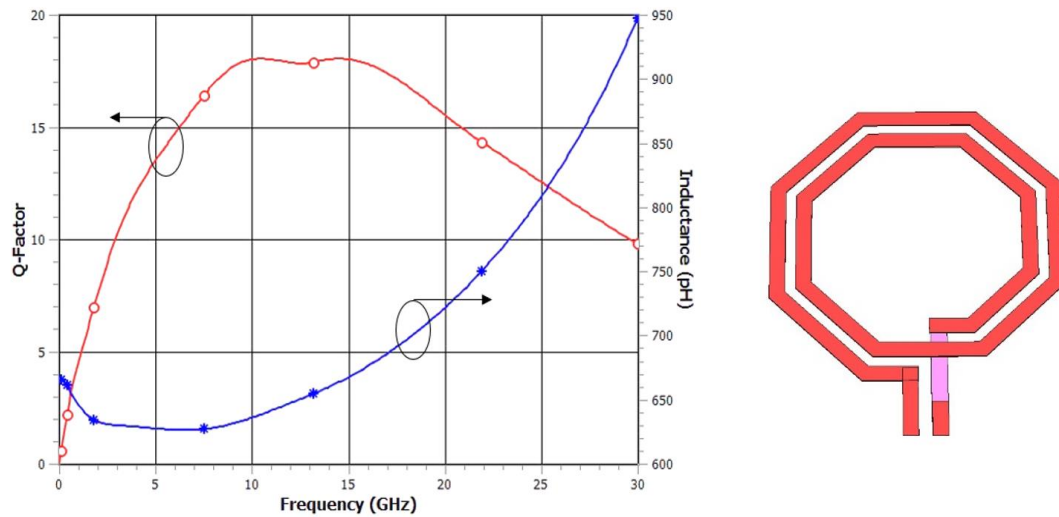


Figure 42 Designed spiral inductor using Sonnet EM simulator

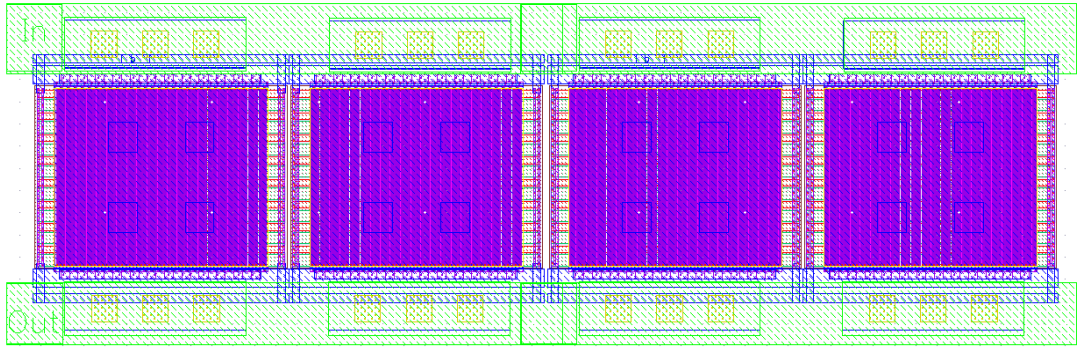


Figure 43 2pF coupling capacitor,  $C_6$  on Figure 35, consists of four 500fF unit capacitors in parallel with  $8\mu\text{m} \times 10\mu\text{m}$  dimension each unit and  $15\mu\text{m} \times 50\mu\text{m}$  overall size for the  $C_6$ .

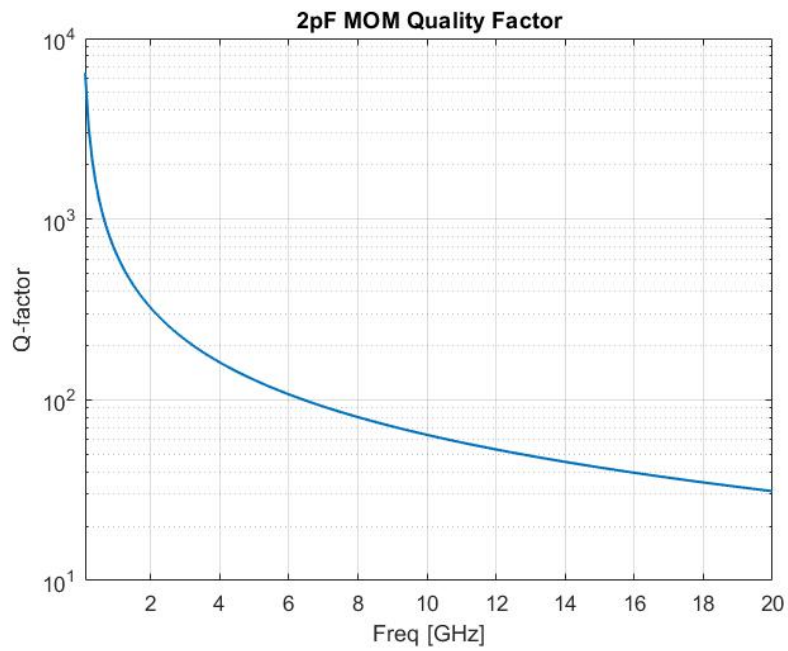
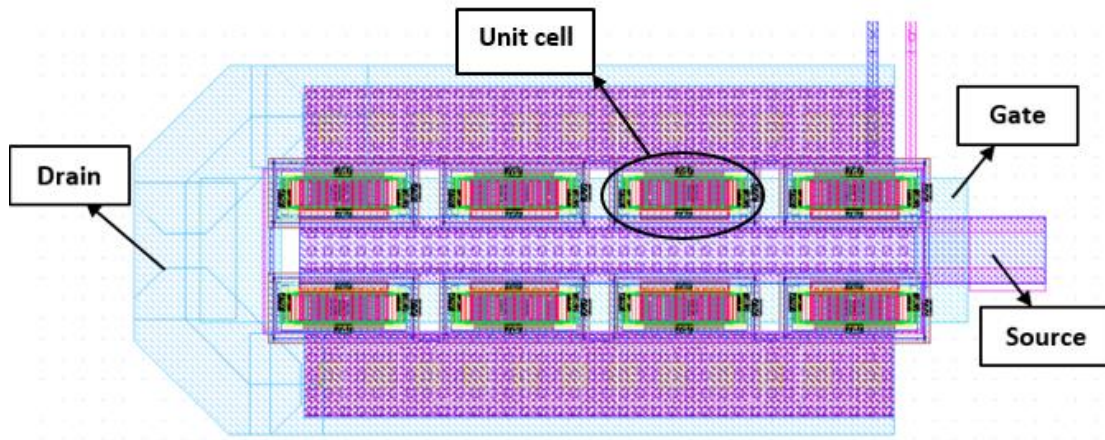


Figure 44 2-pF MOM coupling capacitor Quality Factor



**Figure 45 First stage transistor layout, consists of 8 arrays of SLVTnFET**

Figure 45 shows the first stage transistor. As is shown, it consists of 8 multipliers where each array of a transistor consists of 20 fingers. Multiple arrays are chosen to increase the matching and power handling of the transistor. Moreover, to ensure that the transistor can handle the required current, all the widths of the traces are chosen carefully and all the Vias are counted and checked based on [19]. In this arrangement, the transistor's arrays are placed in two rows so that the sources are facing each other and can be connected easily. Then, all the drains and the sources are connected to the top three metal layers to handle high current flow without burning out the metal. The same structure is used for the rest of the stages with different unit array sizing.

Figure 46 is a close look at the active part of the layout. Each stage corresponds to each stacked transistor, where the 1<sup>st</sup> stage is the common-source transistor and the other three stages are the common-gate transistors cascaded at the top of each other. In this layout, the top three metals are used, due to their thickness and lower loss, for the RF signal path to ensure that the signal path can handle the passing current. Overall, the main

signal path can handle up to 74 mA RMS current, based on the PDK files [19], which is much higher than the overall RMS current on this design.

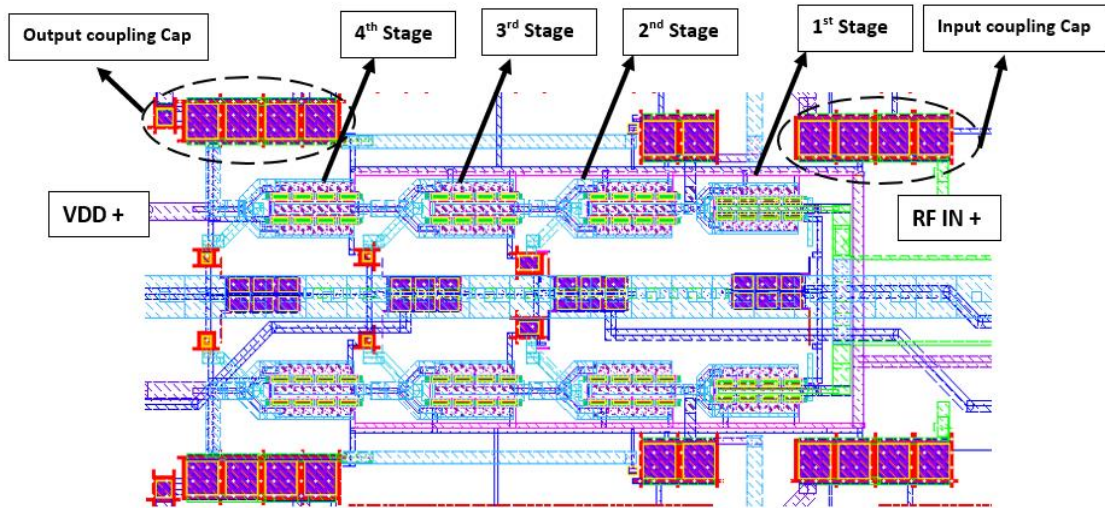


Figure 46 Layout differential stacked PA, Active area layout

Figure 47 shows the overall layout of the fully differential 4-stacked RF driver using 22nm FDSOI with a core area of  $0.167 \text{ mm}^2$ . As is shown, 2 pairs of inductors are used for input and output matching. Also, bypass capacitors are placed at the bottom, close to the DC pads, to filter out the AC signal at those nodes and reduce the power supply noise before entering the circuit.



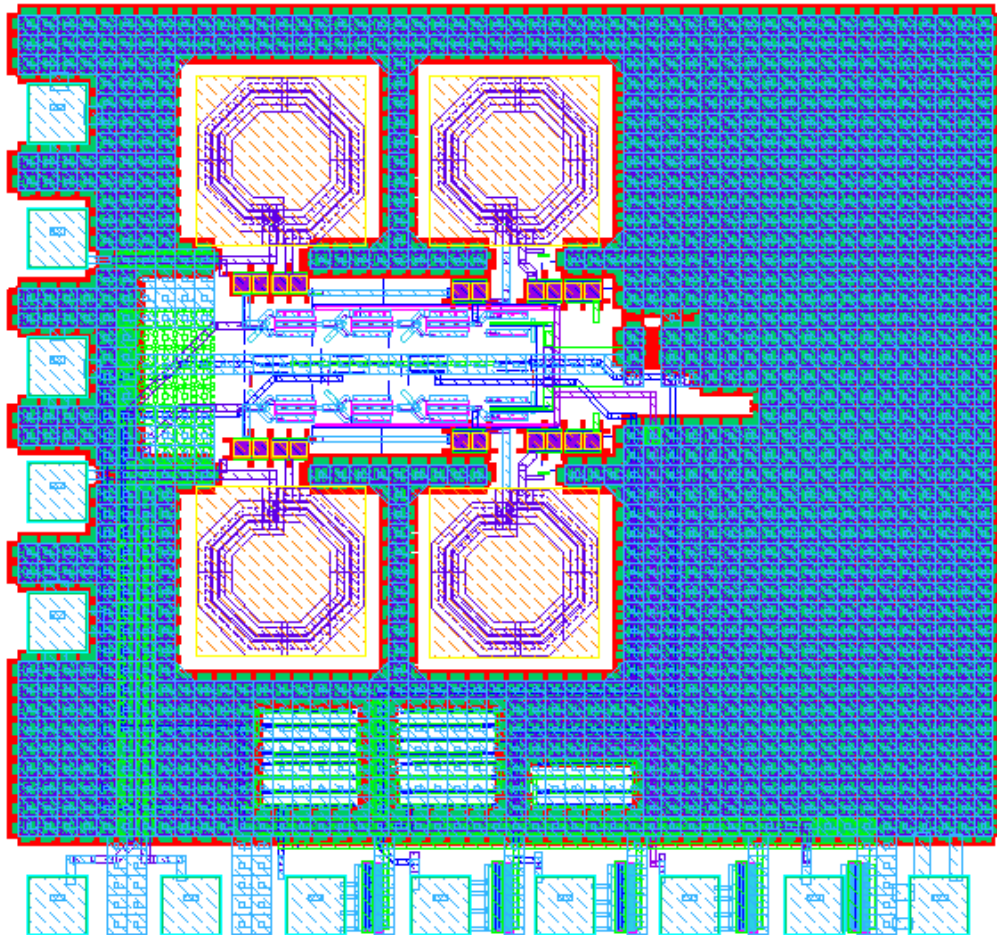


Figure 47 Overall Differential 4-stacked RF driver

### 3.9 Wire bonding effect

In this design, a wire bonding connection was used for measurement purposes. Due to high operating frequency, the parasitic associated with bond pads and the inductance of the wire bonds must be considered in the design. Typically, the effect of the bond wire and bond pads is more critical on the RF path, and for the DC path, the bypass capacitor will bypass those effects. However, in this design, the bypass capacitors cannot be placed on the VDD pads since otherwise, the effect of off-chip choke inductors will also be bypassed. Therefore, the effect of the bond wire and pads needs to be considered, as shown in Figure 48.

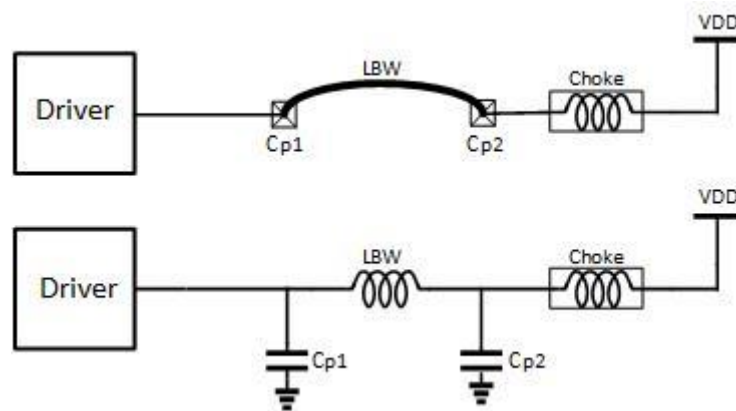


Figure 48 Passive VDD connection and its equivalent circuit model

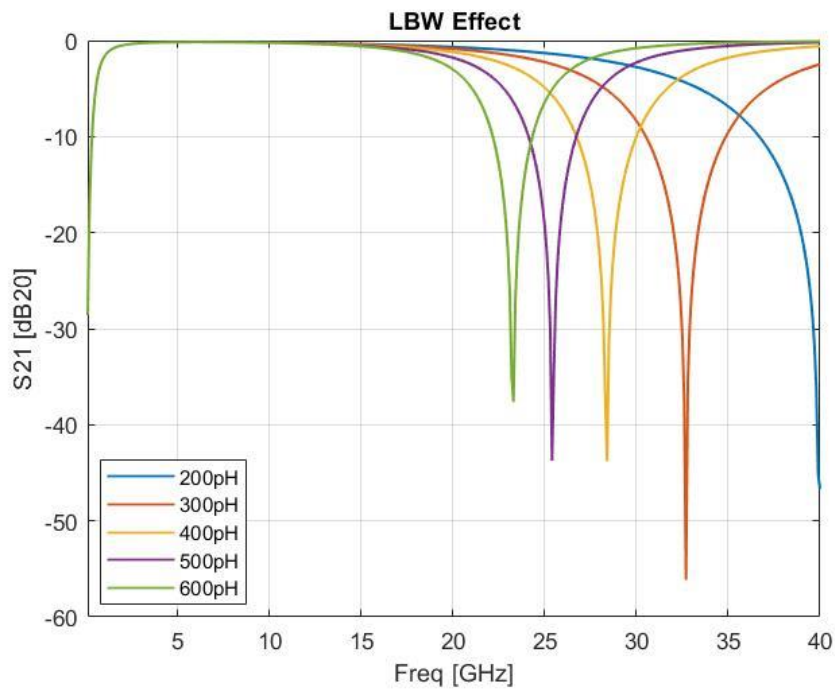
By having a significantly large choke inductor, the choke inductor can be considered an open circuit for high frequencies. In this case, the pad-2 capacitance ( $C_{p2}$ ) and the bond wire (LBW) resonate at their resonance frequency which can be calculated by



$$f = \frac{1}{2\pi\sqrt{(LBW)(C_{p2})}}$$

(3. 16)

Where  $C_{p2}$  is the pad capacitance for the PCB which is considered to be 80-fF. Figure 49 shows the effect of variation of bond-wire inductance (LBW) as it increases from 200pH to 600pH. As is shown, there will be a notch at the resonance frequency for each LBW value and this frequency moves to a higher frequency as the LBW decreases. The same behavior also is observed for the driver transfer function. As is shown in Figure 50, the same notches can be seen at the same frequency. Therefore, it is critical to choose minimum LBW and pad capacitance values to push the notch out of the frequency range of interest.



**Figure 49 Effect of resonance frequency as the bond-wire inductance varies from 200pH to 600pH with fixed 80-fF pad2 capacitance**

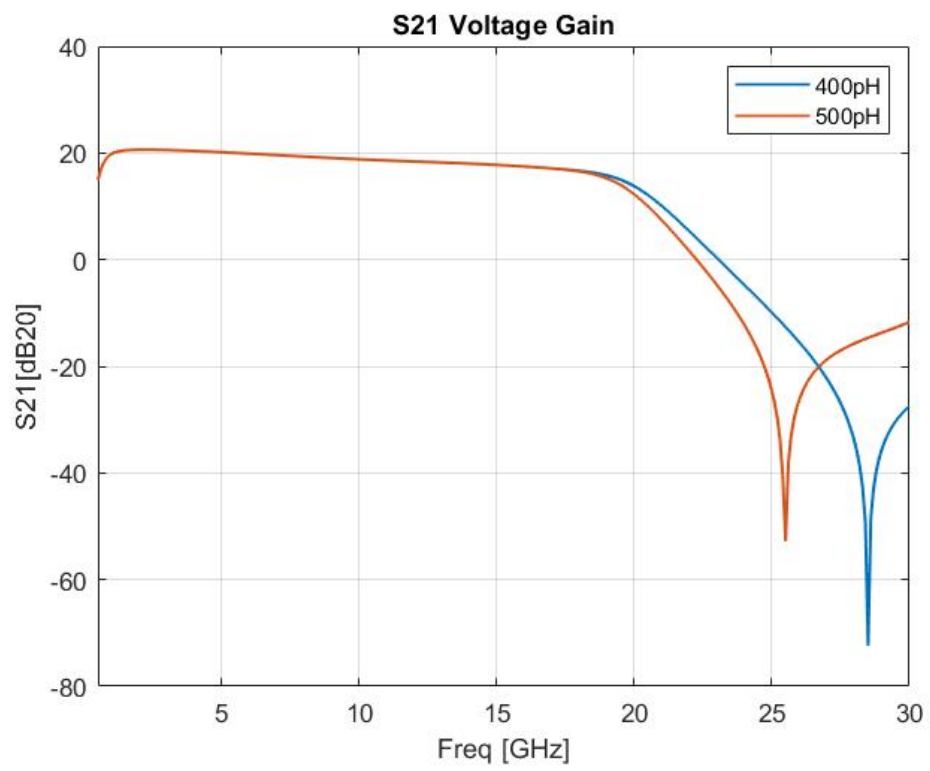


Figure 50 driver transfer function with LBW of 400pH and 550pH

## 4. SIMULATION RESULTS

### 4.1 Post-Layout Simulation Results

#### 4.1.1 S-parameter analysis

Figure 51, shows the “S-parameter” analysis of the proposed design. As shown, the gain of 20 dB is achieved with about 17 GHz 3dB bandwidth. The input and output matching of better than -10 dB is achieved from 1 GHz to 20 GHz. However, below 1 GHz, the matching start to degrade due to the coupling capacitor effect at the input and the output. The effect of wire bonding is noticeable at about 28 GHz, with 400pH bond wire inductance and 80fF PCB pad capacitance.

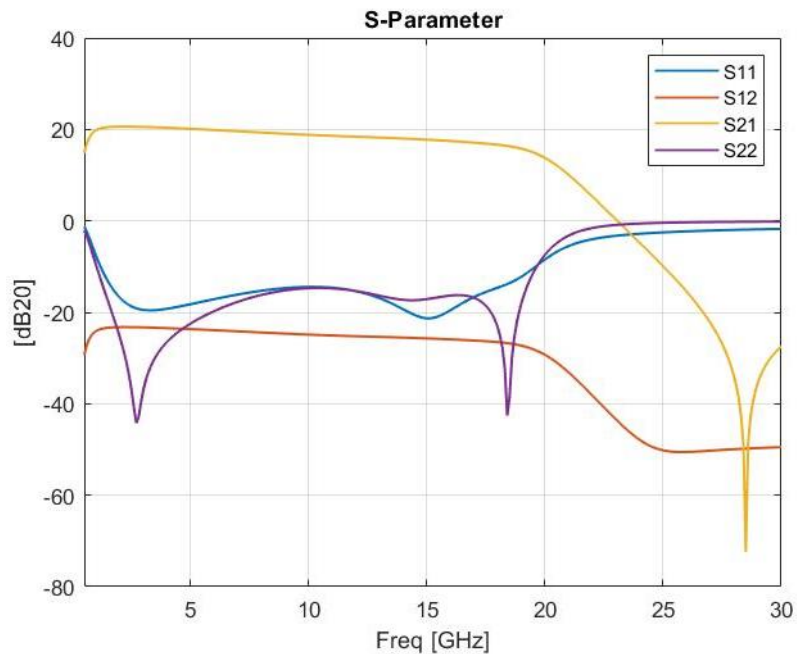


Figure 51 proposes a differential driver S-parameter analysis

### 4.1.2 Design stability

Figure 52 (a) shows the primary stability factor of the design. as shown, the K-factor is greater than 1 for the entire bandwidth, which means the system is unconditionally stable. Moreover, Figure 52 (b) shows the Mu and Mu-prime stability factors, which are greater than 1 which confirms the stability of the system.

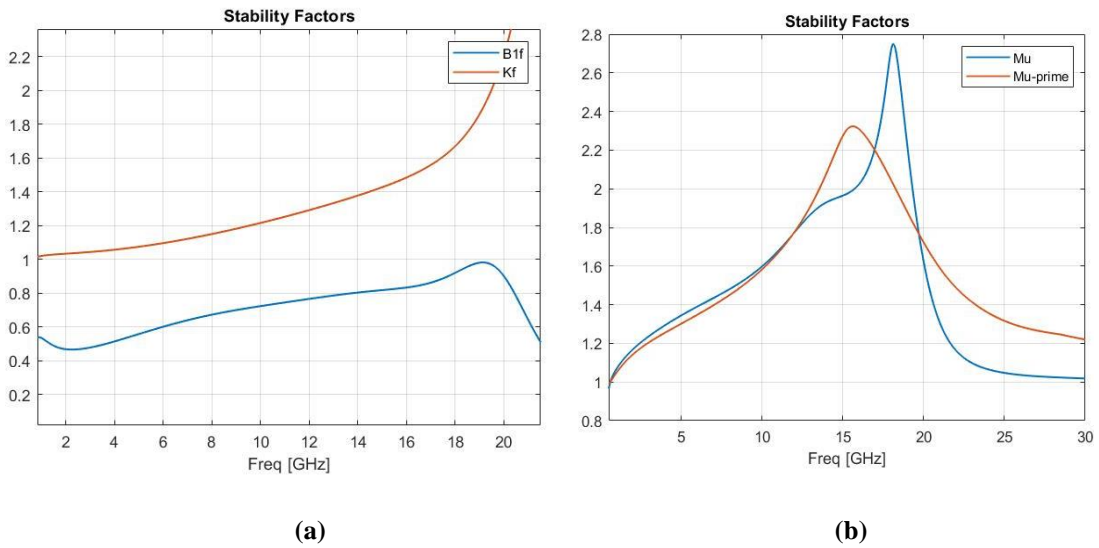


Figure 52 (a) K-factor and B1f stability factors of the PA, (b) Mu and Mu-prime stability factors

### 4.1.3 Harmonic balance analysis (1-dB compression point and Voltage gain)

This section shows the large-signal effect with harmonic balance analysis. Figure 53 (a) and (b), show the output vs input power of the driver at 10 and 16 GHz. as is shown, the IP1dB at 10 and 16GHz are -2.9dBm and -3.2dBm and OP1db are 16dBm and 14.3 dBm, respectively, which means, the system behaves non-linear with signal around IP1dB and beyond. Moreover,  $P_{Sat}$  is about 17.5dBm for 10 and 16 GHz.

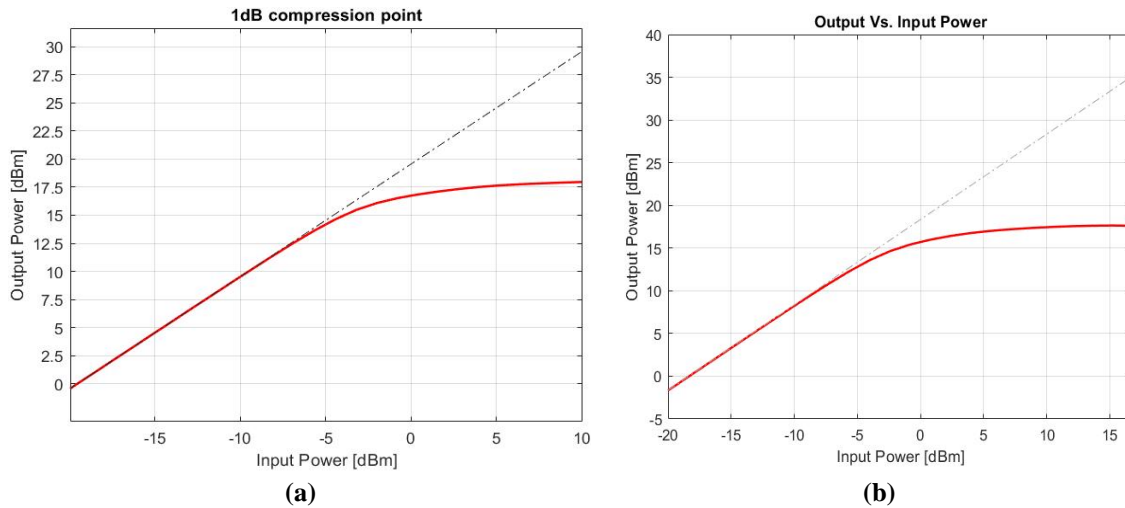


Figure 53 (a) OP1db at 10 GHz is about 16 dBm, IP1db is about -2.9 dBm (single-ended, 50 $\Omega$  termination);

(b) OP1db at 16 GHz is about 14.3 dBm, IP1db is about -3.2 dBm (single-ended, 50 $\Omega$  termination)

Figure 54 (a) and (b), show the voltage gain versus the input power, which up to about -4dBm, the gain is relatively constant and linear, and it starts to degrade for input power beyond that point for 10 and 16 GHz frequencies.

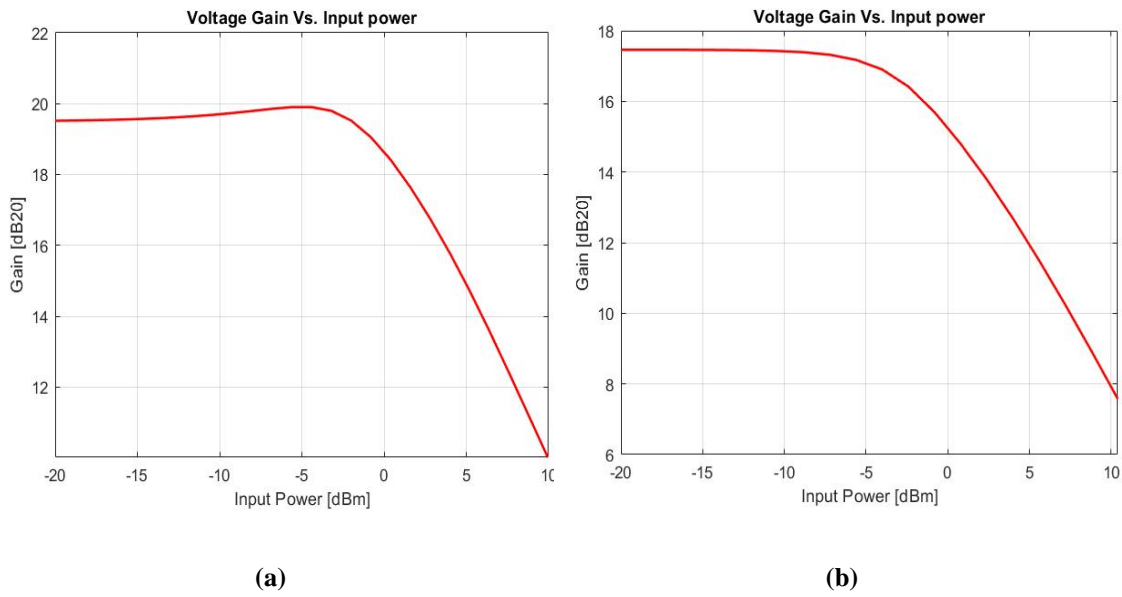


Figure 54 Voltage gain Vs input power at (a) 10 GHz, (b) 16GHz.

#### 4.1.4 Transient Analysis

Figure 55 (a) and (b) show the transient analysis of the driver with a 400mV differential input signal at 10GHz. As shown in Figure 55 (a), a 4V output swing is achieved. Figure 55 (b) shows the input/output single-ended swings. As is shown, there is a small mismatch between the +/- output swing due to the layout mismatch effect.

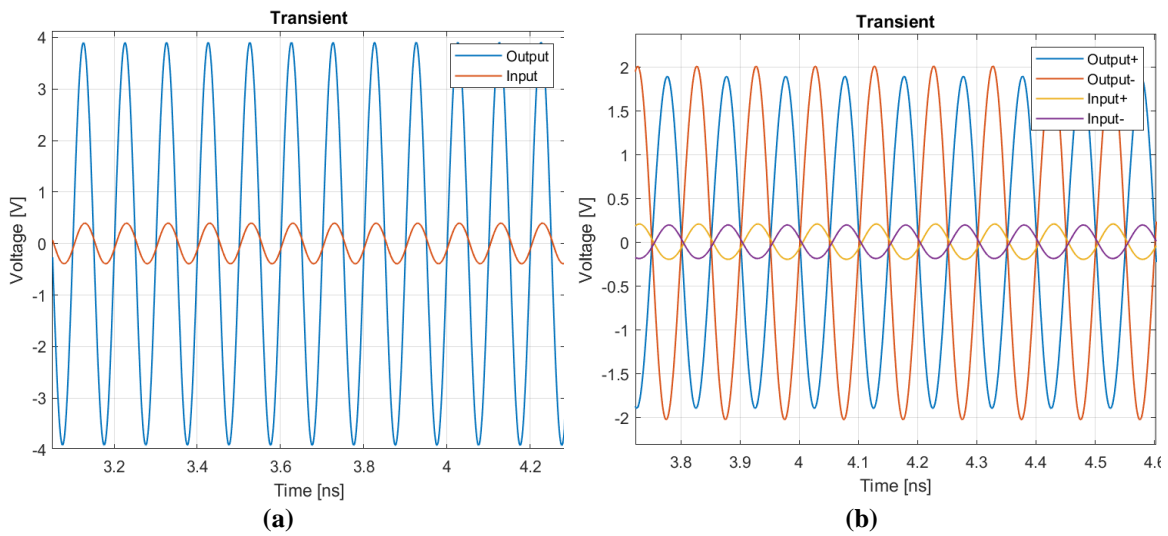


Figure 55 (a) differential and (b) single-ended input/output signal at 10 GHz

## 4.2 Chip microphotograph

Figure 56 shows the microphotograph of the TIA, VGA, and RF driver in a single chip, where the highlighted part is the RF driver. In this chip, the RF ports are all placed on the left side and the bias pads are placed at the top and the bottom of the chip

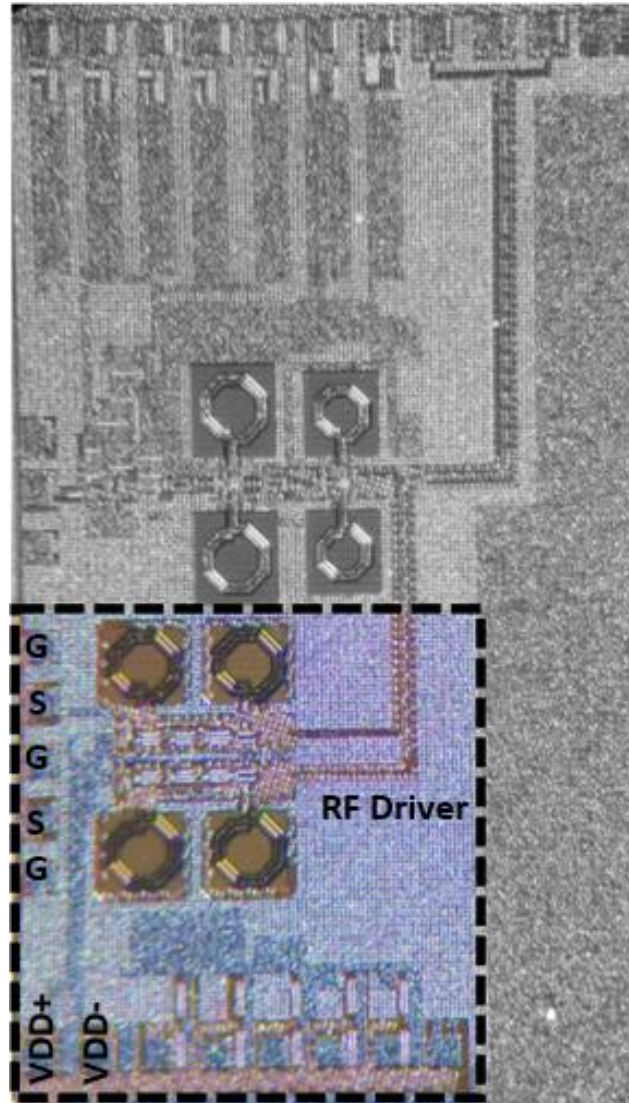


Figure 56 Chip microphotograph



### 4.3 Measurement plan

In this work, to measure the CMOS chip, wire bonding is used instead of using probing for two reasons. First, since there are off-chip components connected to a PCB, which is shown in Figure 58, wire bonding is necessary. Moreover, because the goal of this project is to design the OEO loop, wire bonding is the only way to connect the CMOS chip to the SiP chip. For these reasons, wire bonding is used to connect the CMOS chip to a PCB for measurement purposes. To minimize the length of the bond wires and their inductance, a cavity was designed on the PCB, so that the chip can be placed inside that cavity and the surface of the PCB and the chip are at the same height, therefore the bond wires can be shorter in length. Another challenge of this measurement is to characterize and measure the driver, alone, without the TIA and the VGA. Hence, to overcome this challenge, a test point is designed at the input of the driver, as shown in Figure 57, so that the driver can be measured by subtracting the test point result from the output result.

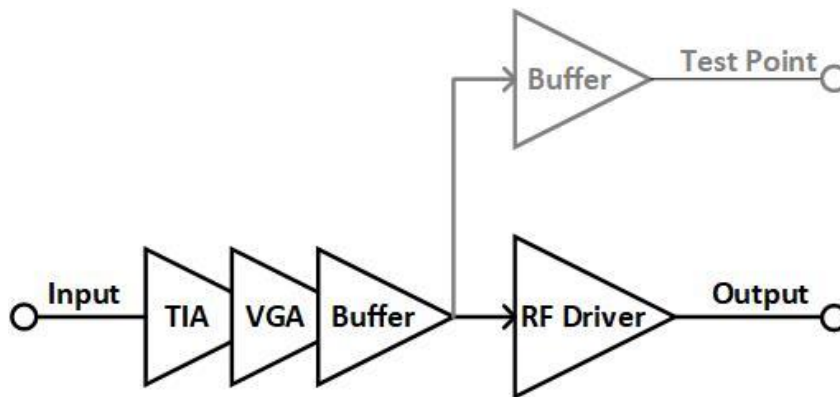


Figure 57 The location of the test point at the CMOS chip

The first step in the measurement is to calibrate the equipment and cables to be able to de-embed the effect of them later from the measurement results.

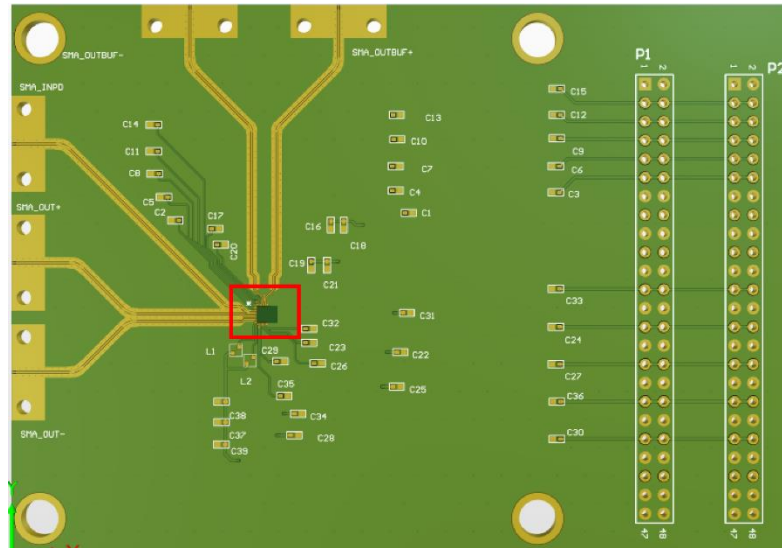


Figure 58 Measurement PCB

### 4.3.1 S-parameter measurement

Figure 59 shows the S-parameter measurement setup using a VNA. A VNA injects a precise sine wave and sweeps the frequency while the receiver tracks the swept input response. From equation (4.1), the S-Parameter can be calculated, where  $a_1$  and  $a_2$  are the incident signal of input and output, and  $b_1$  and  $b_2$  are the reflected signal of input and output, respectively, as shown in Figure 59. However, in this design, since the CMOS chip includes the TIA, VGA, and Driver, the  $S_{11}$  of the driver, alone, cannot be measured. Moreover, since the output of the driver is differential, a balun is needed to measure the  $S_{22}$  and  $S_{21}$ , as shown in Figure 60. Also, since the gain at the output, is the cumulative gain of the TIA, VGA, and the driver, to measure the gain of the driver alone, the gain at the test point can be substituted from the overall output gain.

$$\begin{aligned}
 S_{11} &= \frac{b_1}{a_1} & S_{12} &= \frac{b_1}{a_2} \\
 S_{21} &= \frac{b_2}{a_1} & S_{22} &= \frac{b_2}{a_2}
 \end{aligned}$$

(4.1)

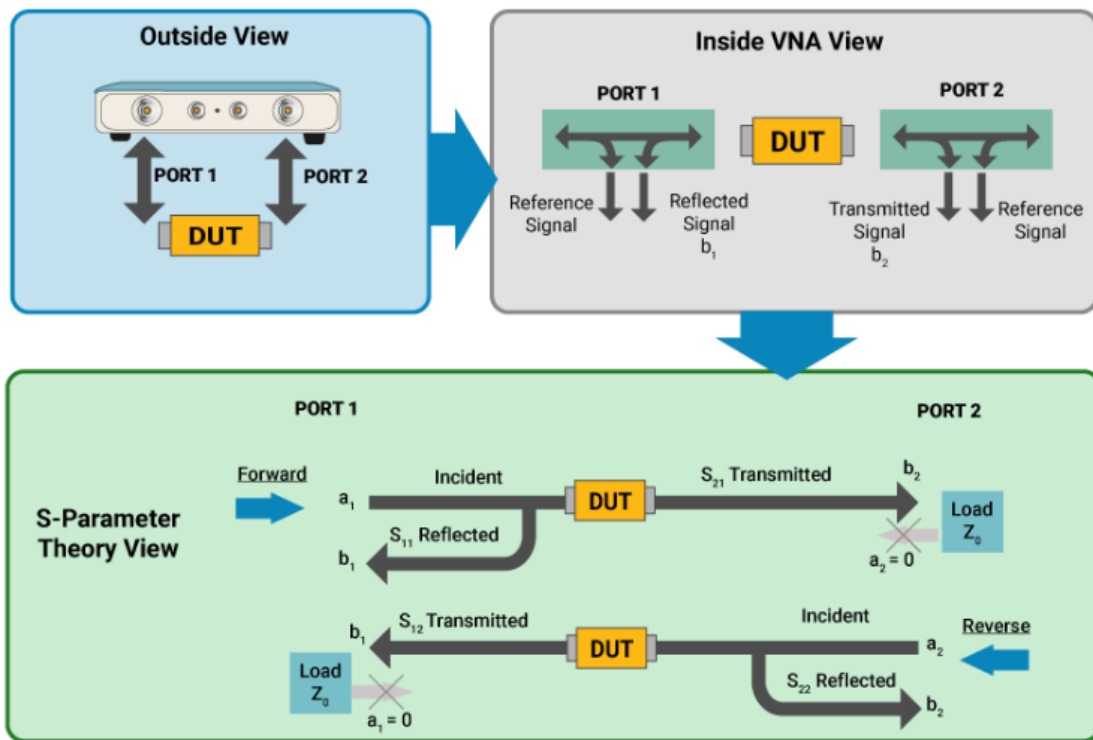


Figure 59 S-Parameter measurement setup (Reprinted from [23])

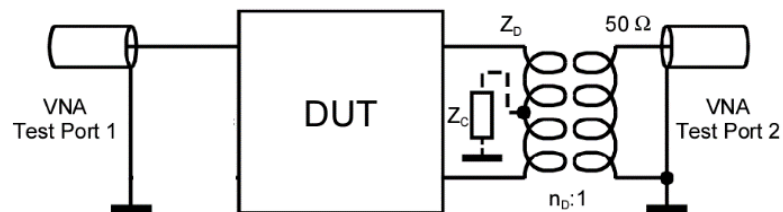


Figure 60 Differential output to single-ended, using a Balun

### **4.3.2 Transient measurement**

To see the transient response of the system, a signal generator and an oscilloscope is needed. The signal generator will inject a signal with a certain amplitude and frequency, and the oscilloscope will track the single-ended output swing using a balun or differential driver's output swing.

### **4.3.3 Large Signal measurement**

For the large-signal measurements, a spectrum analyzer and sweep-signal generator are going to be used, as shown in Figure 61. The signal generator will inject the signal into the device and the output power of the signal generator sweeps while the spectrum analyzer measures the single-ended output power of the DUT using a balun, as shown in Figure 60. The cable and probes are de-embedded using the calibration. The P1db and IP3 are the two main parameters to measure on large signal measurement. To measure the P1db, the input power sweep while the gain is being monitored. The region where the gain drops off 1dB compared to the small-signal linear region, is the 1dB compression point. To measure the IP3, a two-tone signal will be injected, as shown in Figure 62, while their power is swept at the same time. The point where the output power of the first and third harmonics are equal is the IP3 point.

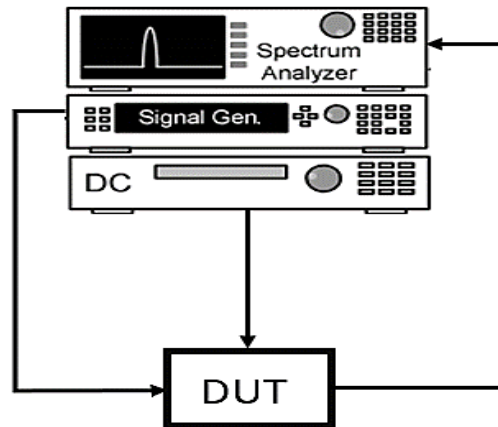


Figure 61 Large-signal measurement setup

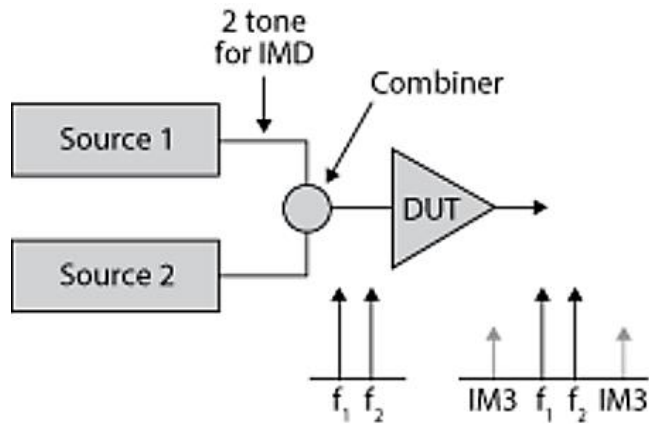


Figure 62 IP3 measurement setup (Reprinted from [24])

## 5. CONCLUSION AND FUTURE WORKS

In this study, different RF driver topologies were analyzed and their advantages and disadvantages were identified, such as distributed and stacked RF drivers. A fully differential, wide-band stacked RF driver was finally presented. The proposed design, prototyped in 22nm Global Foundries FDSOI technology, shows a 0.4-17.4 GHz 3-dB bandwidth with 20 dB voltage gain and about 16 dBm output power at 10 GHz. This design consumes 288mW overall DC power (differential) with 3.2 supply voltage and occupies a core area of  $0.167 \text{ mm}^2$ . Table 5 shows a brief performance comparison between the post-layout simulation result of this work and other works.

For the future, the chip will be measured as soon as it is ready and wire bonded to the PCB. This chip will be measured as a stand-alone CMOS chip and with SOI photonic chip. Moreover, the ultimate goal of this project is to extend the bandwidth of the RF driver and the whole OEO system to 40 GHz.

Table 5 performance comparison table

	<b>This Work</b>	<b>[15]</b>	<b>[16]</b>	<b>[18]</b>
<b>Technology</b>	<u>22-nm</u>	22-nm	45nm SOI	45-nm
<b>Gain</b>	<u>20 dB</u>	~ 24 dB	8 dB	12.4 dB
<b>Frequency</b>	<u>0.4-17.4 GHz</u>	DC – 39 GHz*	88-90 GHz	81-96 GHz
<b>OP1dB</b>	<u>16 dBm @ 10 GHz</u>	11.6 dBm	11.5 dBm	---
<b>P<sub>sat</sub></b>	<u>17.6 dBm</u>	16.4 dBm	17 dBm	19.2 dBm
<b>PAE</b>	<u>27.4%</u>	28.3%	% 9	% 14
<b>Supply</b>	<u>3.2 V</u>	3.2 V	4.2 V	3.4 V
<b>Consumption</b>	<u>144 mW</u>	140 mW	382 mW	379 mW

\* The reported value is not the 3dB-Bandwidth

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