EFFECTS OF TEMPERATURE, HUMIDITY, AND SUPPLY VOLTAGE ON MSP430 BEHAVIORS

A Thesis

by

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ABSTRACT

As the demand for microchips to control a more technologically connected world increases, so does the outsourcing of manufacturing these microchips, which poses risks of old microchips being refurbished as new and new microchips being tampered with Hardware Trojans (HT). The purpose of this research is to develop a systematic testing approach to analyze various microchips for abnormal behaviors. The Design of Experiments (DOE) technique was used to investigate the effects of temperature, humidity, and supply voltage (V_{CC}) on microchip response parameters of VOL, VOH, VIL, VIH, and power consumption values. All these parameters were also individually examined against supply voltage under various temperature and humidity conditions on ten different MSP430FG6626s in 2 separate tests to determine Chip to Chip (C-2-C) variation, microchip defects and potential failures. A sealed enclosure was created to achieve various needed testing conditions and to allow for multiple chips to be tested simultaneously. Corresponding devices were equipped to the enclosure for in-situ input variation and output recording. DOE analysis concluded that supply voltage is the most statistically significant factor affecting key microchip response parameters of VIL, VIH and VOH within the limits of the input factors. The high repeatability and consistency of the response data to supply voltage ramping among the tested chips confirm that the testing setup and method used in this research are valid for screening microchips for defects and irregularities.

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CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was completed under the thesis committee consisting of Dr. Rainer Fink and Dr. Wei Zhan of the Department of Engineering Technology Industrial Distribution, and Dr. Jeyavijayan Rajendran of the Department of Electrical and Computer Engineering.

Jade Chapman provided help and guidance as this research was a contiuation of her previous work.

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NOMENCLATURE

C-2-C	Chip to Chip
IC	Integrated Circuit
HT	Hardware Trojan
VIL	Voltage Input Low
VIH	Voltage Input High
VOL	Voltage Output Low
VOH	Voltage Output High
FDTD	Finite Difference Time Domain
GPIO	General Purpose Input Output
RH	Relative Humidity
CSV	Comma Separated Variable
DUT	Device Under Test

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1. INTRODUCTION

The general lockdown in 2020 stemmed from the COVID-19 virus has brought a sudden supply chain downturn in the microchips industry with effects that can still be felt today. The consequent severe supply shortage of microchips and their unusually long lead production times have forced industries that use microchips to turn to all kinds of chip manufacturers and sources. In the meantime, chip manufacturers are now more willing to outsource manufacturing of these chips to meet the ever-increasing demand on microchips, which in turn has dramatically elevated the risks of microchips being refurbished, counterfeited, and even tampered. If these flawed microchips are not removed in time, they will be marketed as brand-new chips if packaged properly, which will often tarnish the chip manufacturers' reputation and cause their customers to lose confidence in their products. Currently companies are using burn-in tests to reduce the chance of faulty microchips from being sold, but these tests are expensive and time consuming. In addition, although burn-in tests are commonly used to detect early failures in the manufacturing process, they do not give the reasons why microchips fail.

The purpose of this research is to set up and validate a testing protocol that can be used to determine flawed, refurbished, counterfeited, or tampered microchips. Since the testing spectrum with different input and output parameters can be fairly broad, this research has been designed to focus on investigating how temperature, humidity and supply voltage will affect the behaviors of microchips being tested in parallel. It is also

intended that such testing data can be analyzed to facilitate the understanding of microchip failure modes in addition to identifying the “bad” microchips.

The general hypothesis is that aged, refurbished, counterfeited, and tampered chips will have different responses in terms of VIL, VIH, VOL, VOH, power consumptions under different temperature, humidity, and supply voltage (Vcc) conditions. For this reason, the Design of Experiment (DOE) technique was used to arrange the input parameters and their levels to determine how these factors and their interactions would affect the output valves among different microchips. The repeatability and consistence of the collected data have confirmed the effectiveness of the testing protocol and the data has been further analyzed for tends and variances to illustrate any potential microchip issues.

2. BACKGROUND

In the final quarter of 2020, a lockdown stemming from the COVID-19 virus brought a supply chain downturn that felt even in late September 2022. During the lockdown, industrial production of various electrical related products including microchips nearly stopped until the lockdown was lifted. On the other hand, demand for microchips has resumed and increase rapidly after the lockdown. The automobile industry needed more chips for everything from entertainment systems to power steering [6], while the shift towards automation and electric vehicles [6]" has further increased the need for microchips. In fact, a lot of other devices we use in our daily life are controlled by microchips, such as phones, credit cards, watchers, popular work-from-home equipment, etc. So, the pressure to generate more and more microchips has been mounting. Contrary to the ever-increasing demand for microchips, the pace of their development and production was relatively slow. As show in Figure 1 [8], lead time for semiconductor production can exceed four months while switching to a new manufacturer takes a year or longer.

Lack of effective solutions to the drastic microchip shortage issues has naturally resulted in counterfeit or defective microchips becoming increasingly prevalent, some of which are "drop-in replacements or a genuine-but-scavenged part, desoldered from the board it was found on, cleaned up, and pressed back into service as new [10]." The problem of counterfeit chips is worsened by the manufacturing companies that forgo the "elaborate measures to detect and avoid [10]" counterfeit chips when a "question of

whether the line runs or sits idle [10].” This is especially concerning when they also forgo their “normal supply chain verification process [10]” when facing time pressure. Cutting corners to produce faulty chips for a profit now can have dire consequences in the future such as “idle lines or loses money later due to product replacements, lawsuits, and mass recalls [10].”

As technological innovations happen, so does the need to produce semiconductors at a faster pace. This pace is limited by the speed of fabrication along with ensuring the microchips are not defective. Even if the speed of production is increased, defective chips will prove more costly for any company that buys the microchips. For all these reasons, effective and efficient methodologies for detecting and identifying defective and or tampered microchips are much needed to prevent such chips from being used in applications or even entering the market.

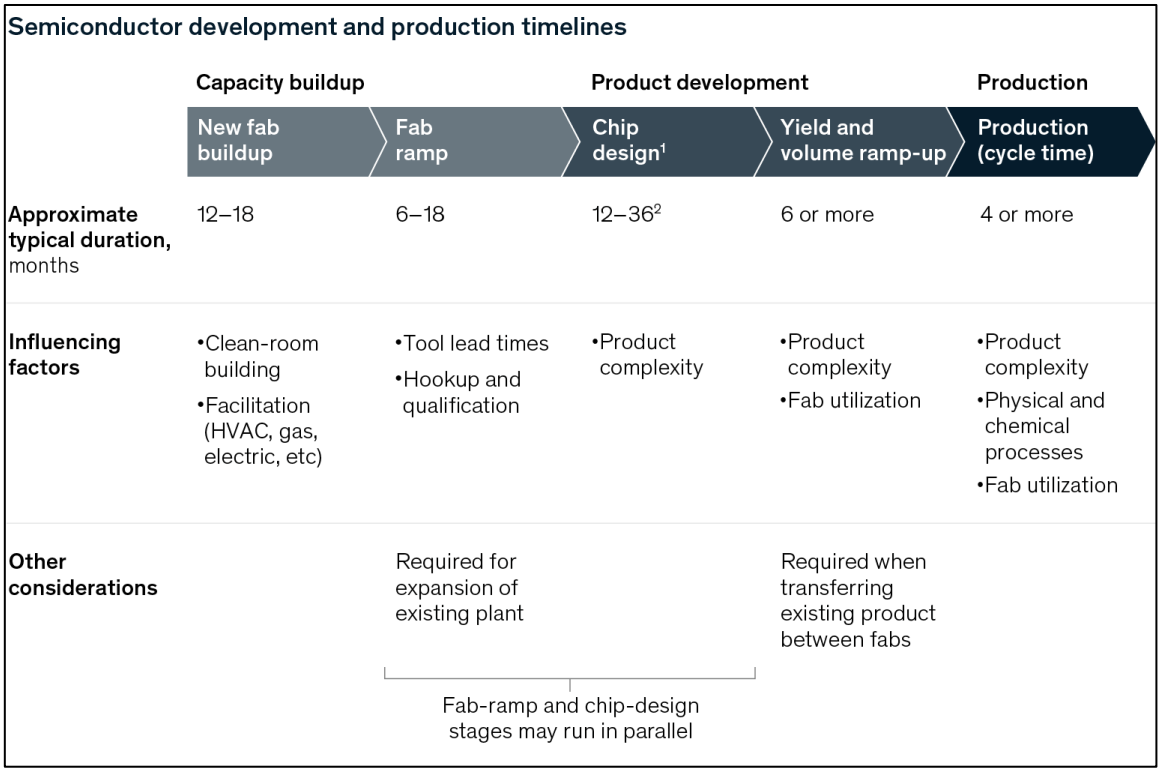

Figure 1 Lead time for Semiconductor Production

Image Credit [8]

3. RELATED RESEARCH

To better plan and arrange this thesis work, the following related research in detecting Hardware Trojans (HT) were reviewed: (1) on-chip testing with local V_{dd}, (2) clock sweeping, (3) power signal processing, (4) backside optical imaging, and (5) EM-based sensor. The methods discussed in these papers are useful in detecting counterfeit and tampered microchips, but they tend to require expensive equipment setup. This thesis work has followed the same intent discussed in these papers but used equipment and materials that are more readily accessible.

3.1. An On-Chip Technique to Detect Hardware Trojans and Assist Counterfeit Identification

This work demonstrated that Hardware Trojans (HT) implanted in microchips can be detected through creating an "fingerprint of static distribution of supply voltage (V_{dd}) over the whole integrated circuit,[1]" and the generated fingerprint can be measured through the use of "an array of sensors that are sensitive to V_{dd} values.[1]" This paper suggested that "on chip monitoring solutions seem relevant in terms of efficiency[1]" and making use of testing multiple ICs may be efficient because "infection of a single device is not realistic[1]". The paper aimed at creating a "distinguisher dedicated to the detection of stealthy Hardware Trojans [1]" and examined the effects of "static and dynamic impacts of an HT insertion.[1]" This concept can be explored further in a project using FPGAs as the primary tool for

detecting Hardware Trojans. To prove "the efficiency of whole detection methodology a set of 24 FPGAs [1]" were used. A "method for detecting Hardware Trojans and rough counterfeits [1]" was created in this paper and this "method was based on cartography done with an array of sensors sensitive to V_{dd} [1]". Investigation into the "limitation due to the aging process of ICs that can induce changes in IC fingerprints [1]" can be investigated. This paper proved that testing more than one microchip is necessary in detecting relatively minor changes in chips, which is relevant to this thesis work.

3.2. A Clock Sweeping Technique for Detecting Hardware Trojans Impacting Circuits Delay

The goal of this paper was to examine a method of detecting Hardware Trojans through creating a pattern file that holds the unique signatures determined through "start-to-fail frequency at each flip-flop for each pattern. [2]" This method followed the industrial standard of "applying a pattern at different clock speed frequencies, from slower to faster [2]." These "start-to-fail clock frequencies can be used to determine the delays of the paths [2]", which allows each path to be fingerprinted and a Trojan to be detected based on start-to-fail frequency changes. It was stated that the "paths will fail sequentially, with longer paths failing before shorter paths. [2]" This paper separated Hardware Trojans into three categories: "Trojans with only payloads (TP), Trojans with only triggers (TT), and Trojans with triggers and payloads (TTP) [2]." It was concluded that "the nodes closer to the scan flip-flops [2]" were more easily detected.

3.3. A Sensitivity Analysis of Power Signal Methods for Detecting Hardware Trojans Under Real Process and Environmental Conditions

This research paper developed a method to detect Hardware Trojans through Power Supply Transient Signals (I_{DDT}) and to determine how small of a Hardware Trojan that could be detected. This method requires nine power ports because the "I_{DDT}'s of neighboring power ports are compared to identify anomalies introduced by the presence of a Trojan circuit. [3]" Once this intersection is created a "three sigma prediction ellipse is derived, and a Trojan free zone is created [3]." The prediction ellipse should bind where "the Trojan free ICs are expected to fall [3]" and any ICs falling outside this region are considered Hardware Trojans. This method was extremely successful because "Trojans as small as a single gate (if that gate switches in response to the test sequence)" were detected in noise free conditions. When noise is a factor, "sensitivity varies from one gate for 30 dB SNR to four gates for 10 dB SNR when the stimulus generates switching in Trojan gates and from three gates to seven gates when the stimulus is not generating switching in Trojan gates. [3]" This method is effective for detecting Hardware Trojans but may not be possible due to design constraints and test chamber conditions.

3.4. Detecting Hardware Trojans Using Backside Optical Imaging of Embedded Watermarks

This paper used an "optical method to detect and localize Trojans inserted during the chip fabrication stage [4]" via "mapping each gate type and location to the

reflectance that is computed from detailed FDTD simulation [4]" for both a clean hardware and a tampered hardware. "The correlation co-efficient can be used to quantify the displacement and deformation of the two images [4]" when determining the differences between the maps. A "thresholding mechanism to determine if the two images match with each other [4]" is implemented which leads to a need to pick a threshold value that will give false positives or negatives. This method is not applicable to this thesis work because we focus primarily on post fabrication defects in microchips. However, this paper does shed valuable light on detecting Hardware Trojans in terms of choosing thresholds to minimize false positives and negatives.

3.5. EM-Based on-Chip Aging Sensor for Detection and Prevention of Counterfeit and Recycled ICs

This paper proposed a "new lightweight on-chip aging sensor, which is based on the electromigration (EM)-induced aging effects for fast detection and prevention of recycled ICs [5]." This research claimed that the "new aging sensor can provide more accurate prediction of the chip usage time at smaller area footprints due to its simple structure [5]." This small aging sensor design not only allows chip designers to better hide the sensor from potential bad actors but also allows the chip to be conveniently tested if it has been tampered with. This sensor "exploits the natural aging/failure mechanism of interconnect wires to time the aging of the chip [5]" which makes the new sensor advantageous over the current technology. Comparing with the ring oscillators, the new sensor has two distinct advantages: its "structure is much simpler as it only

requires metal interconnect wires [5]" and its detection is more accurate as it was "able to measure EM-induced failure [5]." One of the problems that the researchers ran into was "the inherent variations in the metal grain sizes [5]." To resolve this issue, "a number of parallel properly structured wires are employed in the sensor [5]" with the "parameters of the wires being optimized using a new EM mode [5]."

4. EXPERIMENTAL

4.1. Experimental Setup

The Experimental Block Diagram (EBD) in Figure 2 shows the key components and their interactions. The Arduino MEGA on the middle left is responsible for receiving temperature and humidity data from the SHT40 and sends the data to the laptop for further analysis. The Arduino MEGA also sends a PWM signal via a relay to one of the two the heating elements to control the internal temperature of the enclosure. The other heating element stays on continuously to reduce temperature variability. The humidifier is manually controlled, which can be improved in the future by adding a controller to maintain contestant humidity. Both the relay and humidifier require power from a common wall outlet, while the relay also requires a 24V power supply for relay control. The two heating elements are inserted inside the enclosure to make it a closed system. Not shown in the diagram are the MSP430s which are powered by the power rail of the ETS364. VCC data generated from the MSP430s is stored in a CSV file. The MSP430s will also be connected to the ETS364 via jumper wires to a Daughterboard with the relevant pins needed for the project soldered on.

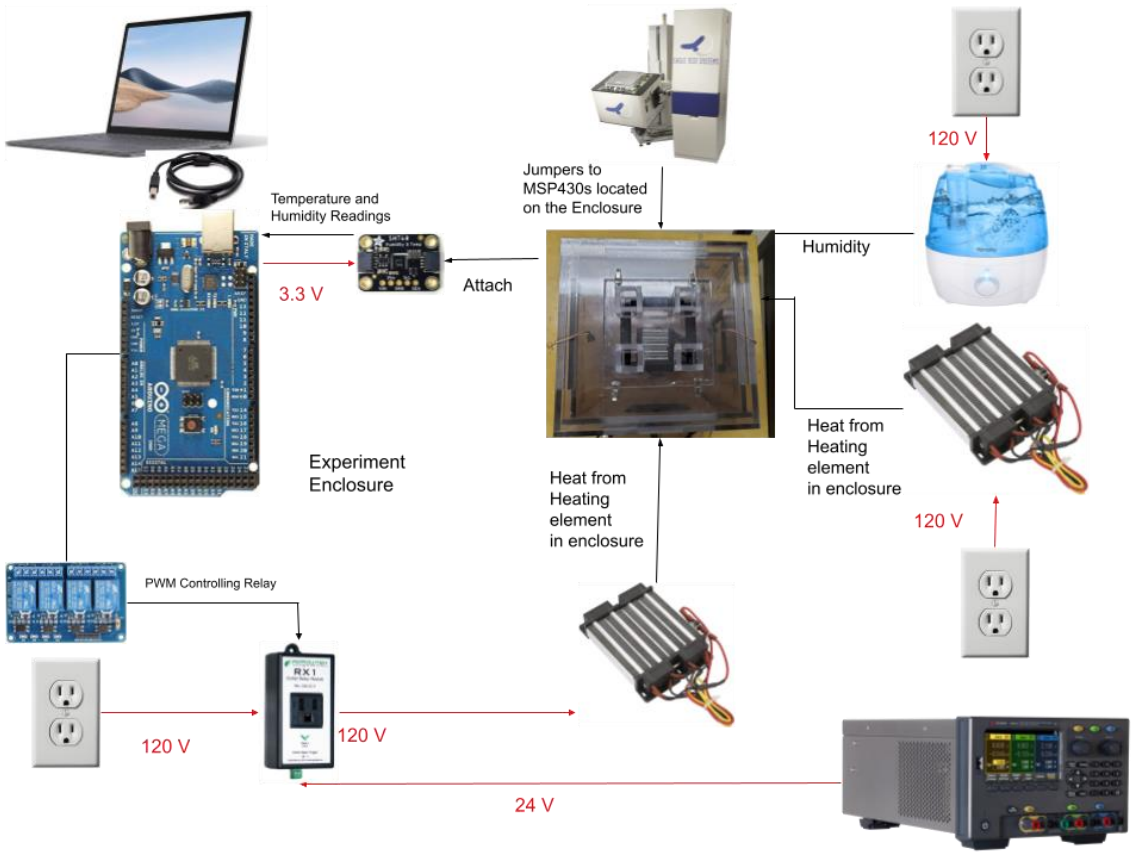

Figure 2 Experimental Block Diagram

4.2. Software Development

All the code for this project is zipped together and attached with the submission of this thesis. The following sections give an overview of how the code works for each of the four parts for the whole project: data collection, Arduino, GPIO state and aging.

The data collection code is written in C++ and has four main sections: setup, functions for testing Vcc at 2V, 3V, and 2V to 3V ramping up. In the setup section, all the necessary variables are defined along with CSV filename generation. The tests for Vcc at 2V and 3V are similar since they both will have code to ramp up and ramp down the voltage on a GPIO pin while measuring the voltage of another GPIO pin. The main

difference between the supply voltage at 2V and 3V with the supply voltage being ramped up is that each microchip will only be tested once instead of four times due to time constraints. All three of the tests will have ramp up and ramp down functions associated with them along with code to determine power consumption. The ramp up code will determine the VIH because it determines when the output voltage switches from low to high, while the ramp down code will determine the VIL because it determines when the output voltage switches from high to low. The ramp up and ramp down function also calculates power consumption by multiplying the measured current at the point when either VIL or VIH is determined by the supply voltage. Each of the GPIO pins and the Vcc pin on the MSP430FG6626 are associated with one of the APU pins through the following scheme: Chip 0 has Vcc on the APU 0, input pin on APU 1, and output pin on APU 2, and so on for the next nine microchips using APU pins 3 through 31. APU 15 and 31 are left open in case any of the APU pins fail. If more than two pins fail, another quadrant of APU pins will be required and configured. This code is separated into distinct functions because it allows for more modularized tests if any set of the data is determined incorrect or missing.

The **Arduino code** is for controlling the relay and connecting to the SHT40s to display and record the current temperature and relative humidity. The SHT40s have a special function, getEvent, for obtaining the current temperature and relative humidity. When the function is called, the variables set to store temperature and relative humidity will have a "&" before the variable name, to indicate they are referenced. The relay chosen for the project is set on "active low." Turn on the relay when the temperature

falls below the desired temperature minus some variation and turn off the relay when it is above the desired temperature plus some variation. The value of the variations has to be experimentally determined.

For the GPIO pins to act in the expected manner, **GPIO State Code** is needed to ensure the state of the output pin matches the state of the input pin. When the input pin state switches from low to high during Vcc ramping-up, VIL and VOL are determined by measuring the voltage of the GPIO pins associated with the input and the output. In the same way, VIH and VOH are determined when the input pin state goes from high to low during Vcc ramping-down.

4.3. Wiring Setup

For Arduino Mega wiring setup, IN1 is connected to PIN 22, GND to GND, and Vcc to 5V. The relay is connected to a power supply with its middle pin connected to the positive terminal and the right pin to ground. The power supply is set to 24V. The SHT40 uses an i2c connection. The SDA pin is connected to the SDA pin, the SCL pin to the SCL Pin, the V_{IN} pin to the 3.3V pin, and the GND to one of the GND pins, all on the Arduino Mega.

4.4. Enclosure Design

The enclosure is made of polycarbonate and consists of detachable panels secured with latches, gaskets, temperature sensors, and a heating element. Figures 3 through 7 show the enclosure with details of various components and their connections.

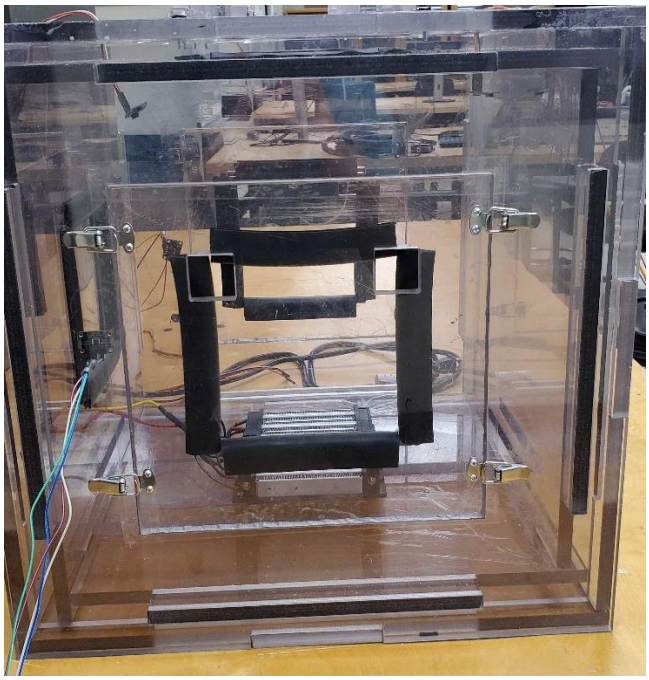

Figure 3 Side View of Gasket and Heating Element

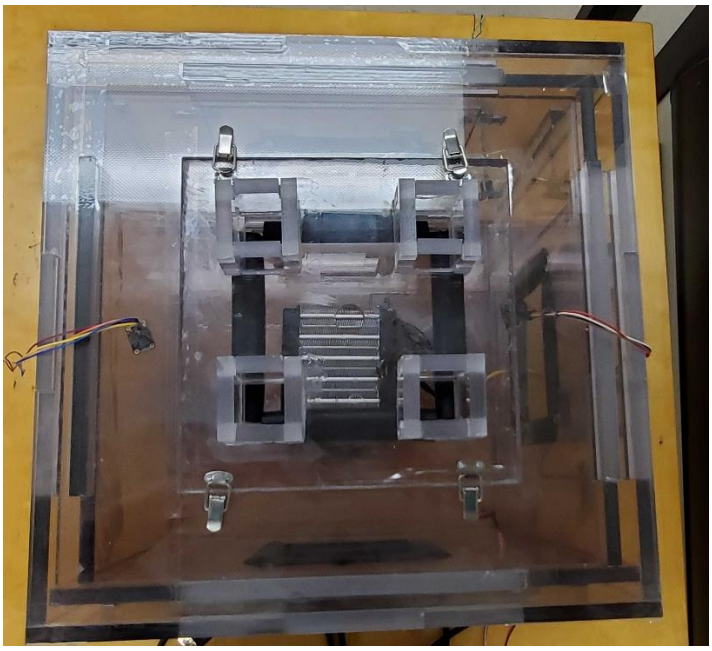

Figure 4 Top View of Temperature and Humidity Sensors Latched on Panel

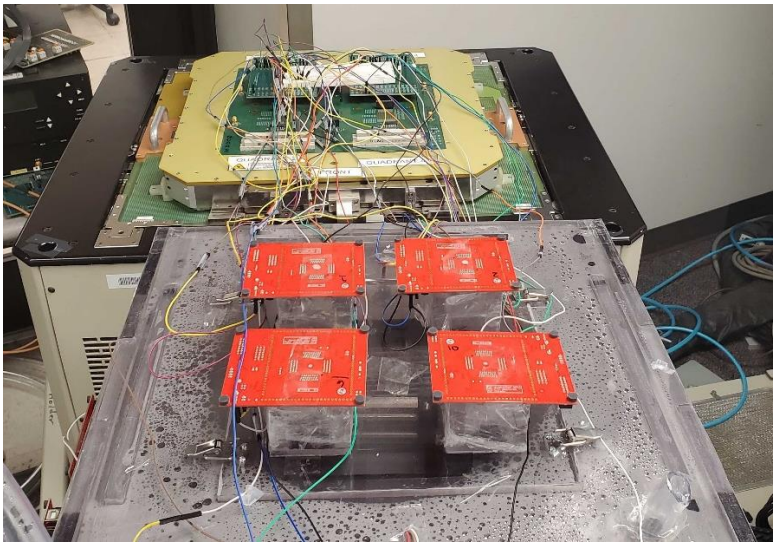

Figure 5 Connection of ETS364 and Enclosure

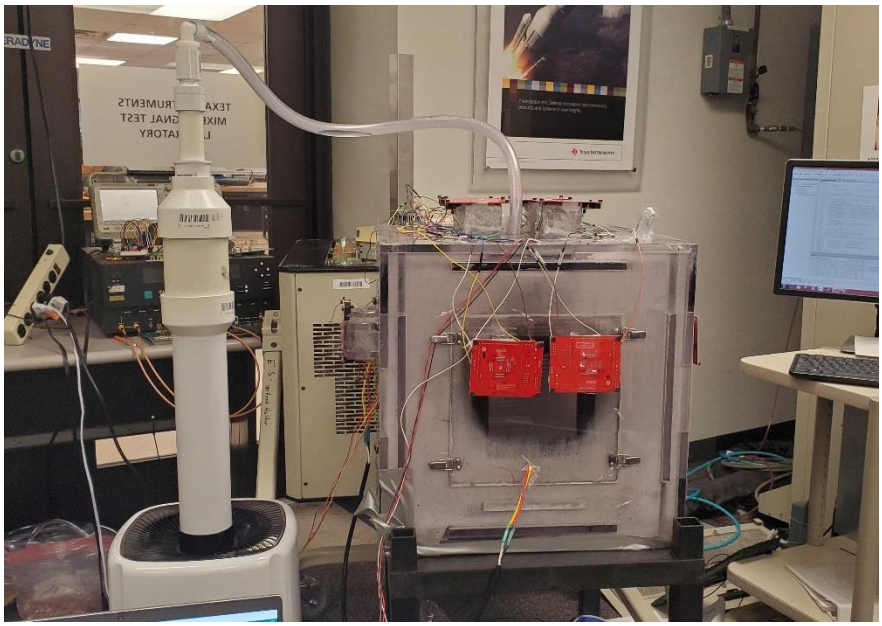

Figure 6 Connection of Humidifier to Enclosure

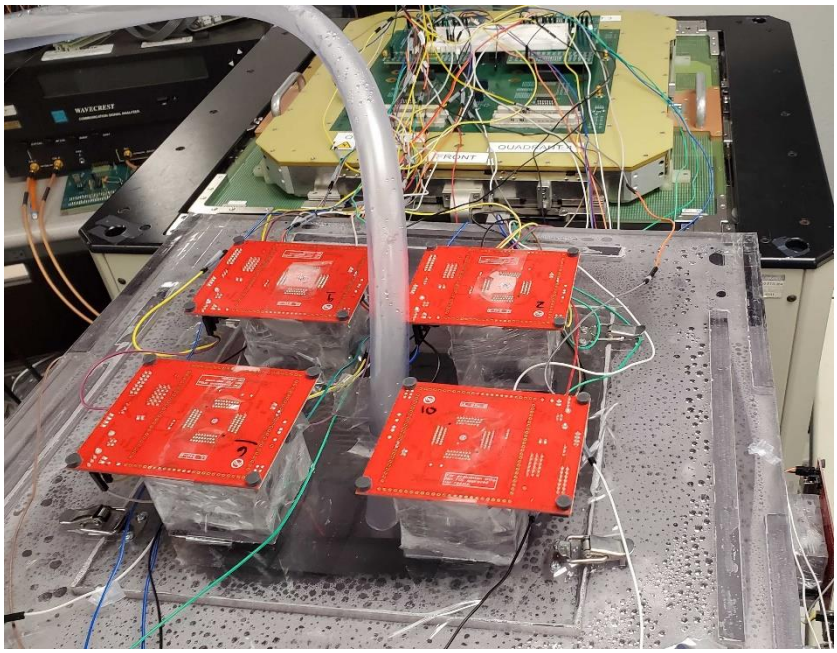

Figure 7 Top View of the Enclosure

The enclosure was sized at 1.5 feet long for each of its sides, big enough to hold ten microchips at once with the heating element being positioned inside the enclosure. Holding ten microchips at once matters because the process of removing and inserting new microchips would cause too much fluctuation as both heat and humidity would escape. The enclosure was designed as a closed system with a heater inside to maintain the desired temperature and humidity for extended periods of time. Polycarbonate, rather than acrylic, was selected as the enclosure material due to its higher heat resistance and less deformation at high temperatures. The enclosure was also designed to have higher re-configurability to allow for other Devices under Test (DUTs) to be tested as such devices can be attached to a panel and the panel can be latched onto the main enclosure.

The design features of the enclosure: include side pieces that can be slotted into each other for stability; interior panels that can hold interchangeable pieces; and ledges that can be used to elevate the heater from the bottom. In addition, an elevated ring was created inside the enclosure to hold the socket on the MSP-TS430PZ100AUSB - 100-pin Target Development Board, and a hole at the top of the enclosure was drilled to insert the humidifier tube. Enclosure design features and details are shown in Figures 8 through 11 below.

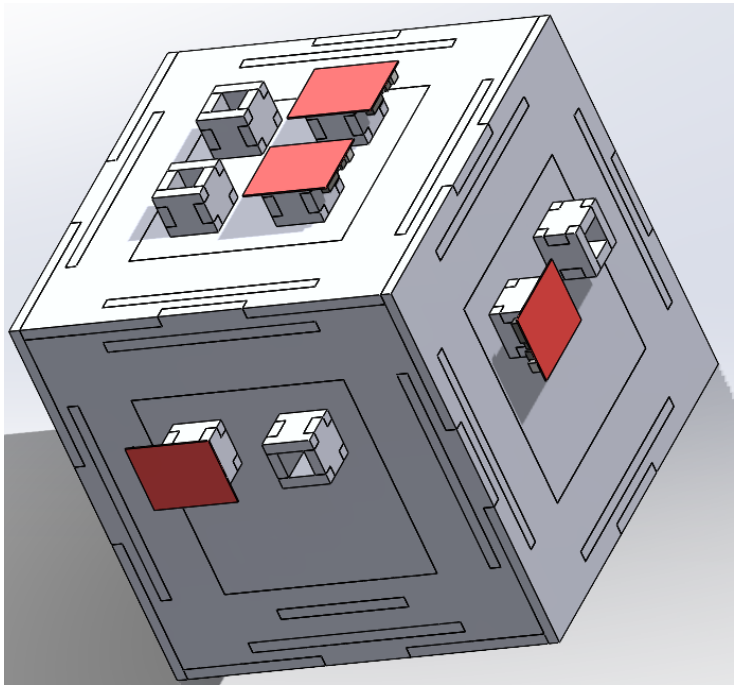

Figure 8 Exterior with Rings and MSP430FG6626s inserted

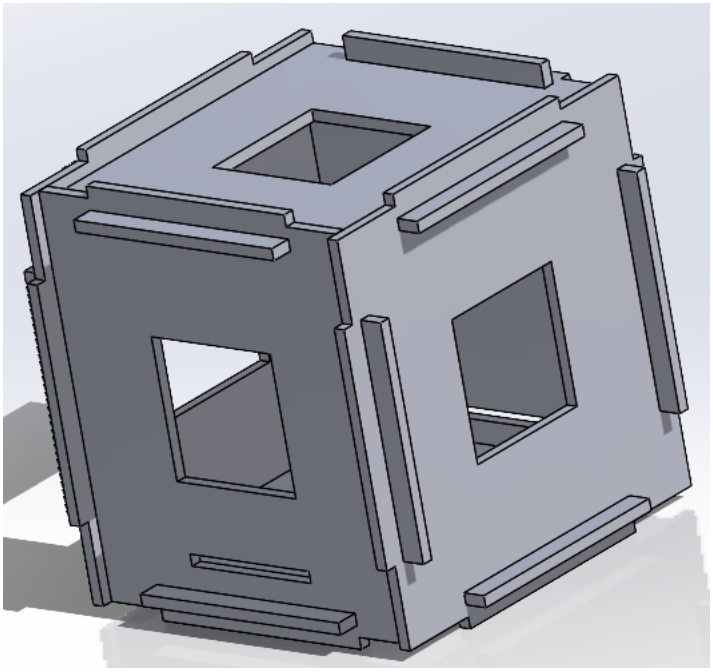

Figure 9 Interior Design of the Enclosure

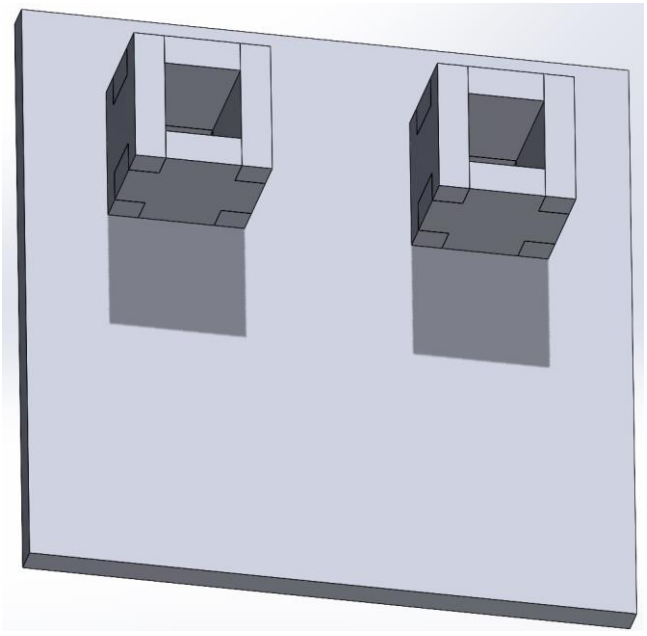

Figure 10 MSP Rings on interchangeable panels

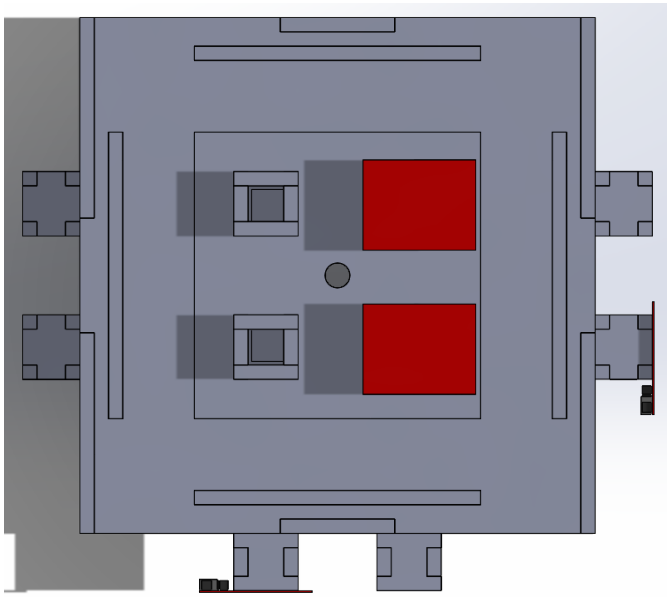

Figure 11 Top View with Hole for Tube From humidifier

Since heating the enclosure to the targeted temperatures with just one 1500W heater took prolonged time, another heat with 1000W power was installed to the enclosure, which was connected to a different power circuit to ensure that no breakers were tripped. The addition of this second heating element dramatically reduced the time needed to heat the enclosure to targeted temperatures. For example, it took 3 hours with just the 1500W heater itself to reach 69^{o}C but only 1 hour to reach 80^{o}C with two heaters working together. Chemical welding technique was used to assemble the enclosure pieces in order to address the issue of regular glue being melted at targeted experimental temperatures.

4.5. Design of Experiment (DOE)

DOE was chosen for experimental design for this research because it gives insight into how the DUT will act when more than one input factors could affect multiple outputs. There are three main factors to be considered in using DOE method for experiments and data collection: blocking, replication, and randomization. Blocking is used "when randomizing a factor is impossible or too costly [12]." This process will "restrict randomization by carrying out all of the trials with one setting of the factor and then all the trials with the other setting [12]." Blocking is not necessary for this research work because the effects of multiple inputs are actually needed for chip performance analysis. Randomization is relevant to this research because it will "help eliminate effects of unknown or uncontrolled variables [12]", especially when bringing the enclosure up to temperature and humidity or back down during tests where residual heat or humidity can cause irregularities in response data. To meet the intent of replication for DOE tests, each test in this research was run four times to ensure that the results of VIL, VIH, VOL, VOH, and power consumption for ramp up and ramp down are valid.

DOE analysis uses minimum (-1) and maximum (1) values to determine how much each input will affect the output. For this experiment, there were three input values (temperature, humidity, and supply voltage) and six output values (VIL, VIH, VOL, VOH, power consumption from ramping up and power consumption from ramping down). Temperature was set to range from room temperature (around 22^{o}C) to 80^{o}C and humidity from around 10% Relative Humidity (RH) to 50% RH based on design limits of the enclosure and the capability of the connected equipment. Vcc was set to range from 2V to 3V. The minimum input voltage was set at 2V because previous experiments

had demonstrated that MSP430FG6626 chips would not function at 1.8V at targeted high temperatures for this research.

5. DATA COLLECTION

Eagle tester was used for data collection in this research which is capable of collecting vast amount of data in relatively short period of time. The general data process follows these three steps: the enclosure is conditioned to the targeted temperature and humidity first, and then Eagle code starts gathering the data, and finally Eagle tester enters the data in a CSV file.

5.1. Determination of Response Values

Figures 12 through 15 shows how the response values of VIL, VIH, VOL, and VOH were determined and collected through ramping up and down the analog input voltages. Two sets of testing runs with voltage ranging respectively from 0V to 1.8V and 0V to 3V at .0001V increments were conducted first to determine the best voltage ranges to fit the data collection needs over the selected microchips. The target boards were programmed in Code Composer Studio, where Pin 1.1 was configured as the input and Pin 1.2 as the output. The output pin reading was set to be equal to that of the input pin to find the response valves of VOH, VOL, VIH, and VIL.

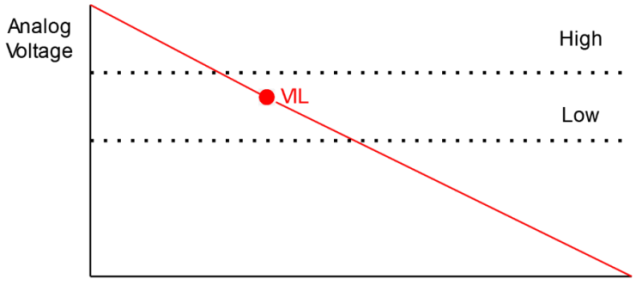

Figure 12 Finding VIL through Ramping Down

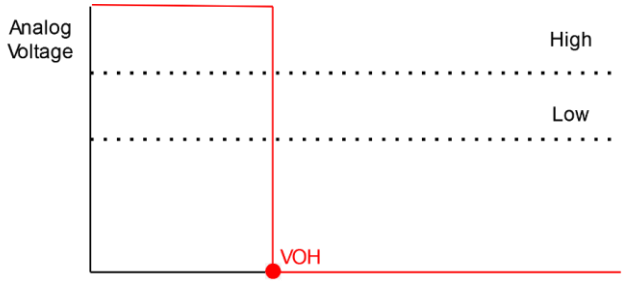

Figure 13 Finding VOL through Ramping Down

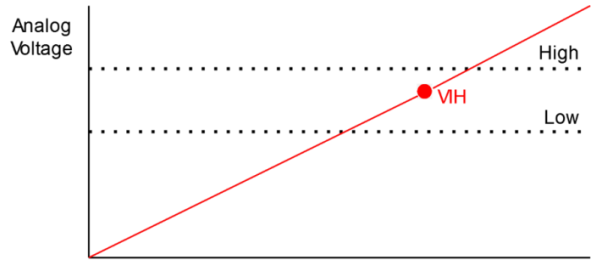

Figure 14 Finding VIH through Ramping Up

Figure 15 Finding VOH through Ramping Up

5.2. Data Collection Problems and Solutions

The issues in collecting VIL, VOL, VIH, and VOH values included long testing time, voltage loss in the length of the wires, and response valves being synchronized at

the same time for multiple-chip testing. Better understanding of microchip functionality and further examination of the collected data helped to resolve these issues.

Reducing Test Time Ramping input voltage up and down between 0V and 3V at 0.001V intervals worked for single microchip testing. However, using the same method to test ten chips consecutively would take a long time to finish – typically 4 days for each set of data. The solutions to this problem were to start the tests at a point closer to the expected value determined from the datasheet, and to reduce the sampling rate and even stop the program right after the output valve has switched from high to low or low to high.

Voltage Loss in the Wire Due to the size of the enclosure and the position of the microchips, the voltage loss from in the wires were significant, which even caused certain microchips to give false positives when the initial set of starting values for the tests were used. This problem was resolved by using the data collection program to adjust the response valves based on recorded starting voltage.

Resolving the Synchronization of Data When multiple microchips were being tested at the same time, the outputs were synchronized in parallel upon the finish of the tests. The consequence of such synchronization was that all the microchips switched from high to low or low to high at the same point thereby causing the data to no longer be useable. This issue was resolved by shifting from testing all ten microchips at once to running them in series. Since all microchips had been placed in the enclosure beforehand and no chips would be moved in or out of the chamber, there was little fluctuation between tests in terms of temperature and relative humidity conditions.

5.3. Optimization of Input Voltage Range

As mentioned earlier, the starting input voltage did not start at 0V or 3V during voltage ramping, but rather it was set a point closer to the expected value based on available datasheet for microchips to be tested. This method not only saved testing time but also allowed for higher precision tests to be performed before the targeted temperature and humidity could no longer be maintained.

Table 1 shows the upper and lower bounds for typical VIL and VIH values for input voltages of 1.8V and 3V. The VIT+ and VIT- values in Table 1 corresponds to VT+ max VT- min values in Figure 16, respectively. Since the microchips were run at 2V in this research, the starting input voltage levels had been adjusted accordingly. The starting input value starts at the max typical value of VIT- + 0.5V when ramping down, while it starts at VIT+ value - .5V when ramping up. As the data was collected from the ETS364, each data point was stored in a CSV file, for which an example is shown in Table 2.

Table 1 Typical VIL and VIH Values for Given Voltages – Modified from Texas Instrument Datasheet [13]

V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80	1.40	V
			3 V	1.50	2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45	1.00	V
			3 V	0.75	1.65	

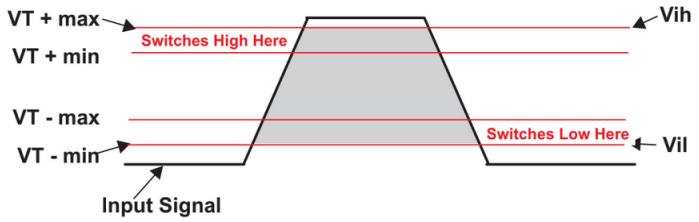

Figure 16 Schmitt Trigger for VIH and VIL – Modified from Texas Instrument Datasheet [14]

Table 2 Example of CSV File

2to0V_Ambient_1.csv					
Test #	1				
VCC =	2				
		Site 0			
Input Voltage		Outputvolt	Power Consumption in mW		
1.4999		2.18163	-5.48764		
1.4998		2.18164	-5.30715		
1.4997		2.18172	-5.29515		
1.4996		2.18184	-5.3264		
1.4995		2.18193	-5.32996		
1.4994		2.18191	-5.32828		
1.4993		2.18194	-5.34615		
1.4992		2.18195	-5.34178		
1.4991		2.18198	-5.34759		
1.499		2.18196	-5.35684		

6. RESULTS AND DATA ANALYSIS

6.1. Expected Output Values

The test conditions in terms of current output high (IOH) and current output low (IOL) were set at -5 mA and +5 mA respectively in this research. As shown in Table 3, the expected VOH values for MSP430FG6626 microchips would be between Vcc and Vcc -0.25 while the expected VOL valves would be between Vss and Vss +0.25. The values for VIL and VIH are not shown in the datasheet in Table 3, but they can be estimated by looking at the Schmitt Trigger portion of the datasheet shown in Table 4, where VIT+ and VIT- correspond to VIH and VIL, respectively.

Table 3 MSP430FG6626 Output Characteristics of GPIO Pins - – Modified from Texas Instrument Datasheet [13]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA(1)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –10 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –5 mA(1)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –15 mA(2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA(1)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 10 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 5 mA(1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 15 mA(2)		V_{SS}	V_{SS} + 0.60	

Table 4 MSP430FG6626 Input Characteristics of GPIO Pins - – Modified from Texas Instrument Datasheet [13]

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	

6.2. DOE Results and Analysis

To determine how temperature, humidity, and Vcc affect microchip performance in terms of VIL, VOL, VIH, VOH, power consumption when ramping down, and power consumption when ramping up, a set of experiments were conducted on 10 MSP430FG6626 chips with DOE experimental design technique. The levels of the three input factors were respectively set at 22^{o}C and 70^{o}C for temperature, 20% and 50% for relative humidity, and 2V and 3V for supply voltage Vcc. The response data of VIL, VOL, VIH, VOH, and power consumptions were collected based on the average values of the four test runs for each microchip. The input and output raw data from all DOE tests are listed in Appendix A, from which Pareto charts were generated by the Minitab software and attached in Appendix B. The Pareto charts not only show the response data to input factors and their combinations and interactions, but also indicate which factors or factor combinations have caused statistically significant responses.

Chip	0	1	2	3	4	5	6	7	8	9
VIL (Y1)	C	C	C	C	C	C	C	C	C	C
VIH (Y2)	C	C	C	C	C	C	C	C	C	C
VOL (Y3)			C				C,A,B			
VOH (Y4)	C	C,AB	C	C	C	C	C	C	C	C
PCRD (Y5)	C,B				C,B,BC					
PCRU (Y6)				C				C		

Statistically Significant

Statistically Insignificant

Factors and Levels:

A = Temperature: 22C, 70 C

B = Humidity: 20%, 50%

C = Supply Voltage: 2V, 3V

Responses:

VIL, VIH, VOL, VOH

Power Consumption Ramp Up

Power Consumption Ramp Down

Figure 17 Statistically Significant Mapping of DOE Results

Figure 17 shows a map of all the statistically significant responses to the three input factors or their combinations over the ten microchips. This map clearly

demonstrates that supply voltage is the only factor that can consistently cause significant responses in terms of VIL VIH and VOL. This implies that unless extremely harsh temperature and humidity conditions are created, supply voltage should be used as the primary factor to analyze microchips for anomalies. The DOE results also tell us that VOL and power consumption responses are generally weak even with strong supply voltage inputs and may not play important roles in differentiating behaviors of microchips. It should be mentioned that all the responses observed here are limited to the limits of input factors applied. If experimental setup allows, the testing limits should be expanded to further validate the findings mentioned above.

6.3. Effects of Supply Voltage on Output Valves

Since supply voltage had the most significant impacts on the outputs based on DOE analysis, a second set of tests were conducted to determine how changes in supply voltage would impact the output valves. The tests were carried out by incrementing the supply voltage from 2V to 3V at 0.05V intervals under the same low temperature and low humidity conditions on the ten microchips in 2 tests.

Figures 18 and 19 show the output valves collected with Chip 0 in Test 1. It is obvious that the output valves of VOH, VIH and VIL, all demonstrating statistically significant responses to Vcc, increased as supply voltage increased, with VOH increasing the most. However, the output values of VOL, power consumptions, all exhibiting statistically insignificant responses to Vcc based DOE analysis, did not show obvious trend as supply voltage increased, as the response data had large variance.

Actually, the same can be said for essentially all the output valves collected on ten microchips in two runs as Vcc ramped from 2 to 3V, as demonstrated in Figures 24 through 29. This further confirms that VOH, VIH and VIL responses to Vcc can be used to surface microchip issues as they have the needed response sensitivity to Vcc and data consistency.

Table 5 shows all the output values against ramping Vcc with Chip 0 in Test 1, where values were marked in red if they did not follow the general trend. The power consumption columns did not have any values highlighted because there were too many values that did not follow the general trend. All output values against ramping Vcc with ten chips in two runs can be found in Appendix C.

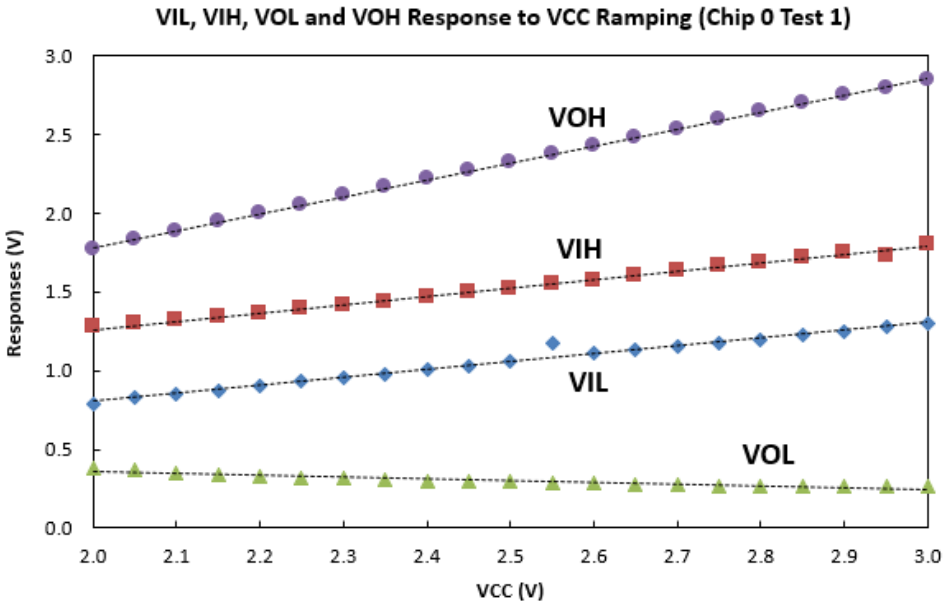

Figure 18 VIL, VIH, VOL, VOH Trends

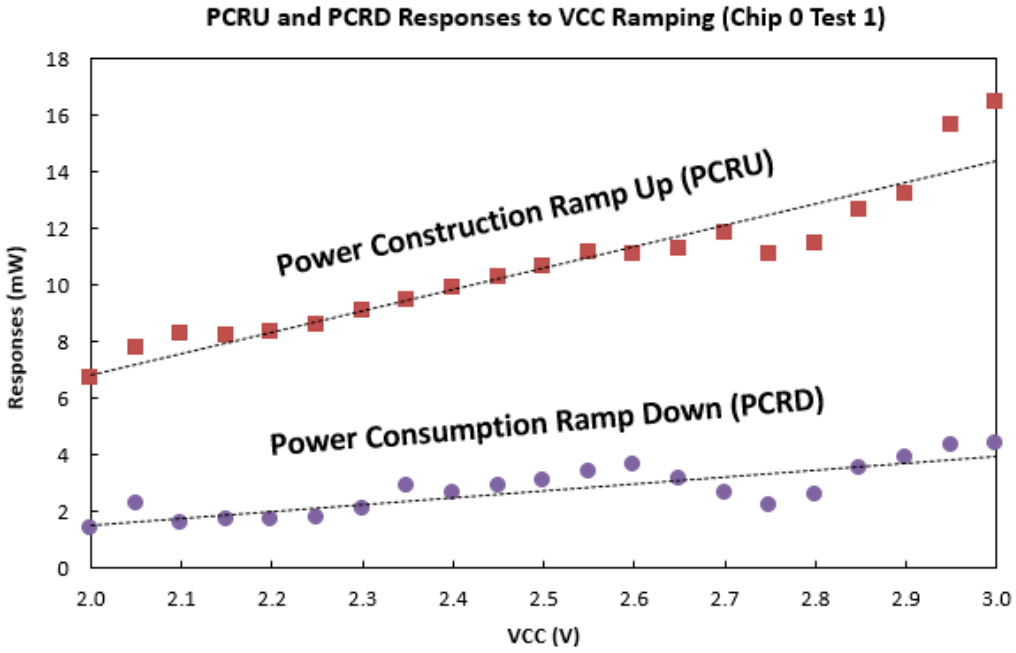

Figure 19 PCRD, PCRU Trends

6.4. Table 5 Output Values against Vcc Ramping with Chip 0 in Test 1

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.7894	1.277	0.383499	1.7734	1.41145	6.70627
2.05	0.8271	1.295	0.371971	1.8292	2.26139	7.79645
2.1	0.8497	1.317	0.354284	1.8853	1.56816	8.2501
2.15	0.8724	1.34	0.341662	1.9424	1.71502	8.18991
2.2	0.9002	1.357	0.330422	1.9985	1.72826	8.31364
2.25	0.9292	1.389	0.322129	2.0541	1.76045	8.59365
2.3	0.9564	1.415	0.315254	2.109	2.09405	9.06379
2.35	0.9776	1.437	0.307482	2.1636	2.87312	9.49231
2.4	1.0052	1.463	0.300848	2.2175	2.64509	9.87841
2.45	1.0319	1.493	0.296104	2.2711	2.87377	10.305
2.5	1.0576	1.518	0.292042	2.3242	3.12056	10.6418
2.55	1.1701	1.546	0.288145	2.3773	3.43129	11.1627
2.6	1.1113	1.572	0.28403	2.4306	3.62444	11.1208
2.65	1.1309	1.606	0.278564	2.4837	3.16776	11.299
2.7	1.1517	1.632	0.273124	2.5361	2.67138	11.815
2.75	1.1728	1.662	0.268499	2.5894	2.21551	11.0885
2.8	1.1974	1.687	0.266321	2.6415	2.57797	11.4949
2.85	1.2277	1.717	0.26579	2.6933	3.52164	12.6521
2.9	1.2501	1.747	0.26398	2.7455	3.92799	13.2003
2.95	1.2757	1.729	0.262587	2.7965	4.36474	15.6798
3	1.3002	1.805	0.260377	2.8483	4.39282	16.477

6.5. Chip to Chip Variation

Theoretically, microchips of the same type should have same or similar output values against input factors under the same testing conditions. If significant variance is observed among the chips tested, it is either caused by chip-to-chip differences or testing inconsistency. This research has collected enough repeatable data to demonstrate that testing inconsistency was not an issue for output valves of VIL, VIH, and VOH. These data can be used for chip-to-chip variation analysis.

Figures 20 through 23 show the various outputs at both high and low supply voltage with ambient temperature and humidity. These conditions were chosen because they best reflected how the microchips would act in normal operating conditions. For these tests, coefficient of variance, standard deviation divided by the mean, was used to quantify how the ten microchips vary with each other. As can be seen in these figures, the variance among the ten chips in terms of VIL, VIH and VOH response to low and high Vcc is relatively small with coefficient of variance being 0.6% to 2.4% in the case of high Vcc and 0.8% to 2.7% in the case of low Vcc. This not only demonstrates that the chip-to-chip variation amount the ten chips is small but also further confirms that there is a high level of data consistency for the three statistically significant responses of VIL, VIH and VOH to Vcc.

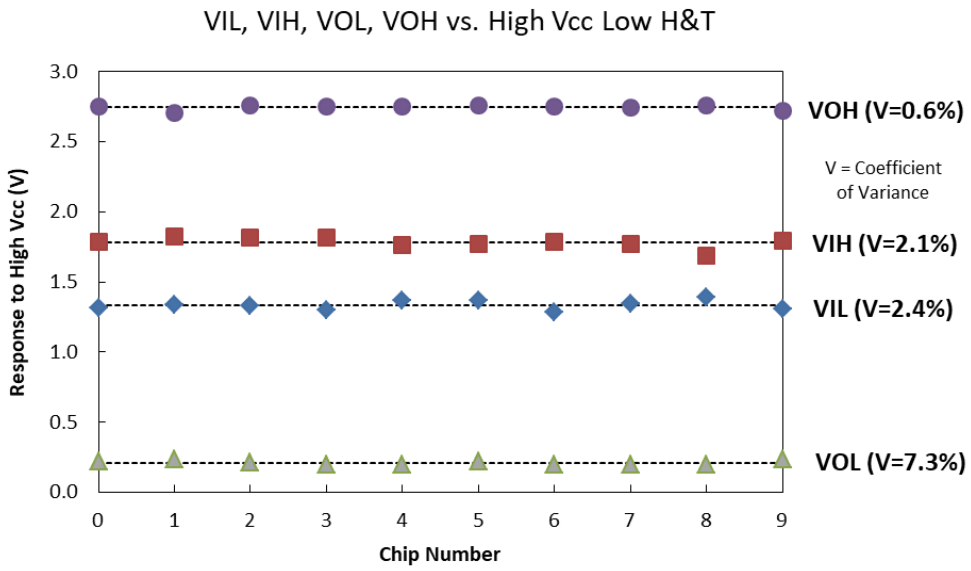

Figure 20 VIL, VIH, VOL, VOH vs. High Vcc

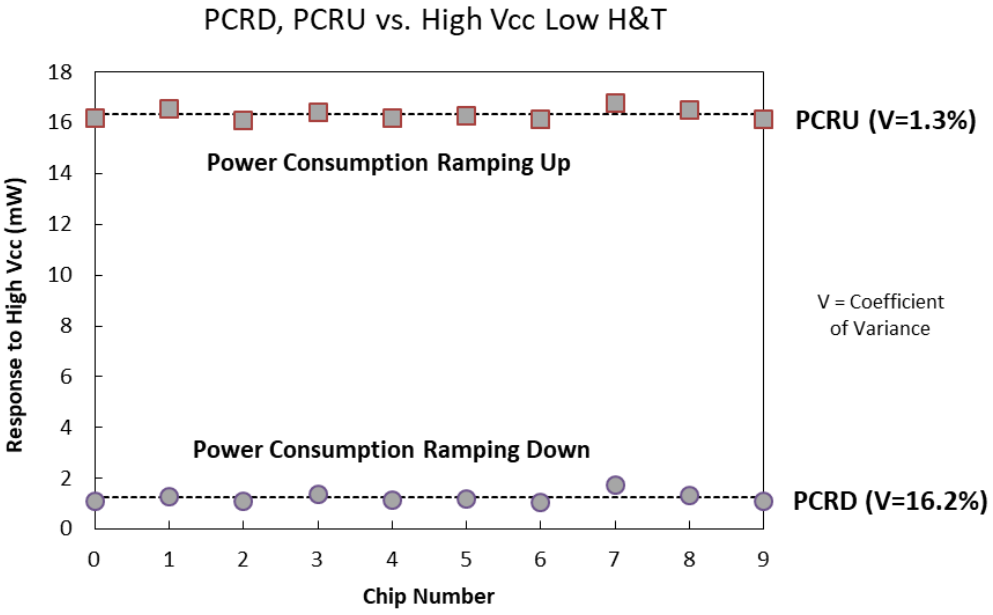

Figure 21 PCRD, PCRU vs. High Vcc

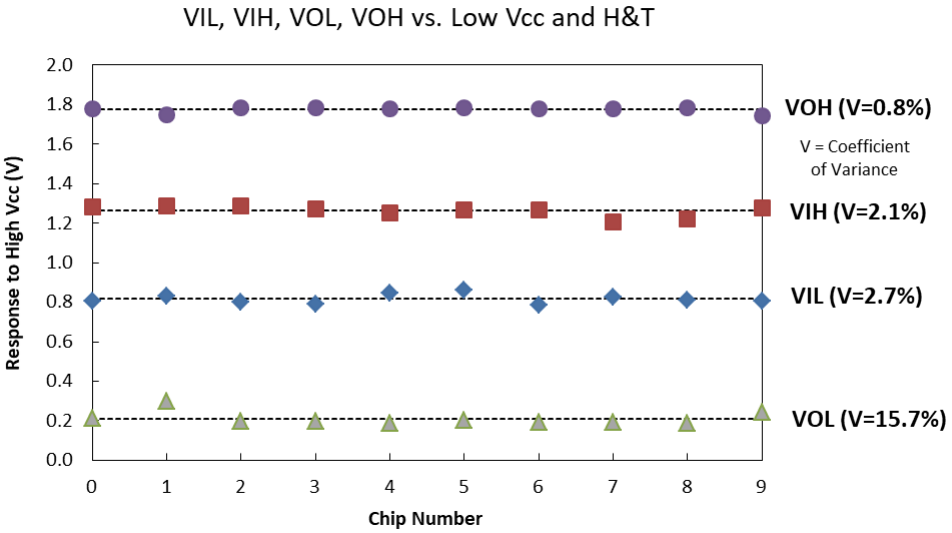

Figure 22 VIL, VIH, VOL, VOH vs. Low Vcc

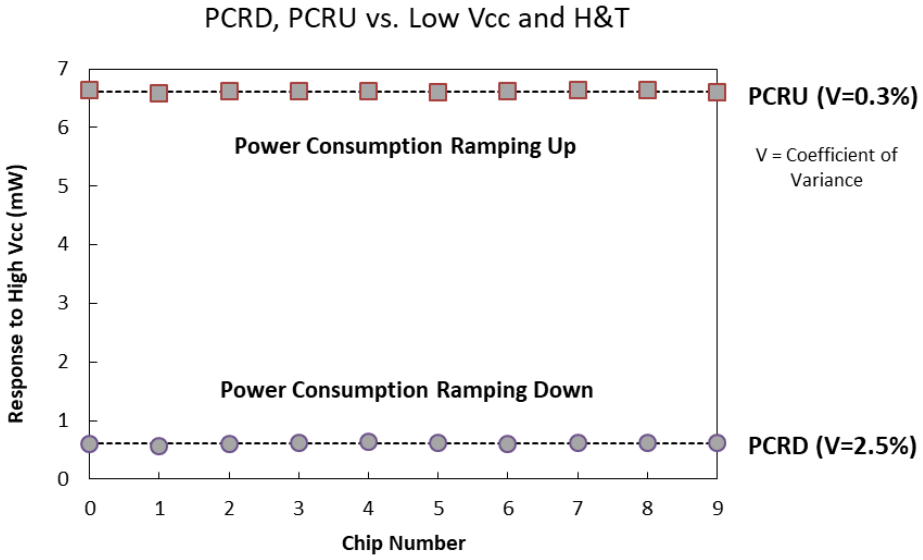

Figure 23 PCRD, PCRU vs. Low Vcc

Figures 24 through 29 respectively show VIL, VIH, VOL, VOH and power consumptions responses to ramping Vcc where the twenty sets of data (10 chips and two tests) were overlaid onto one graph for each of the six output parameters. Again, these graphs clearly show data repeatability and consistence for VIL, VIH and VOH, which are statistically significant responses according to DOE. In the meantime, the data variance among the ten chips for responses of VOL and the two power consumptions is noticeably high. Since these three responses are not regarded as statistically significant, it is not recommended to use these responses (VOL, power consumptions) for chip-to-chip variance analysis, which may change if they can be demonstrated as significant responses in the future under different experimental conditions.

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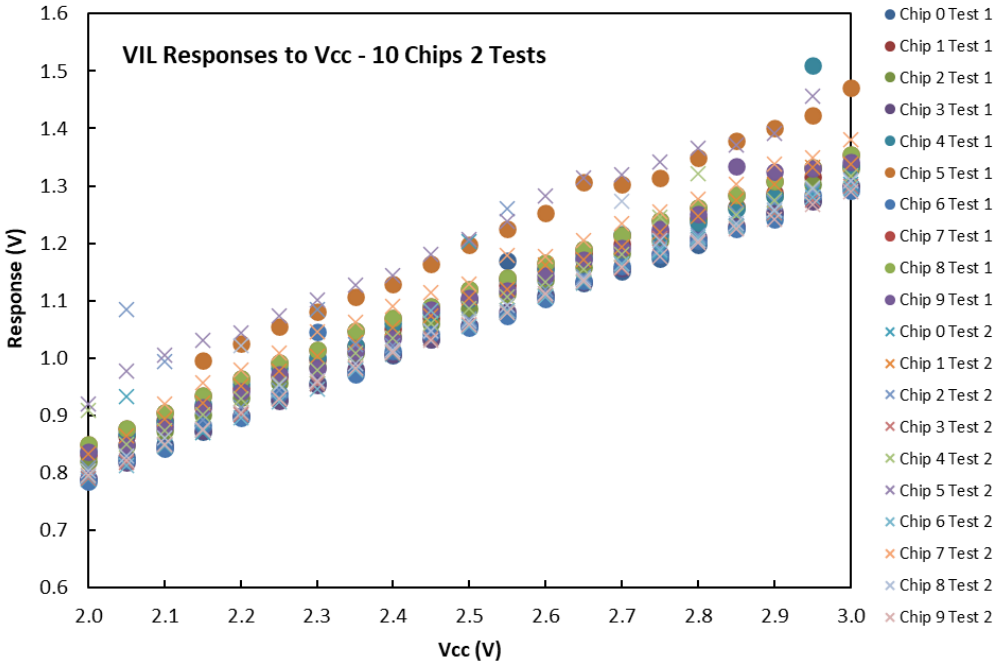


Figure 24 VIL Responses to Ramping Supply Voltage

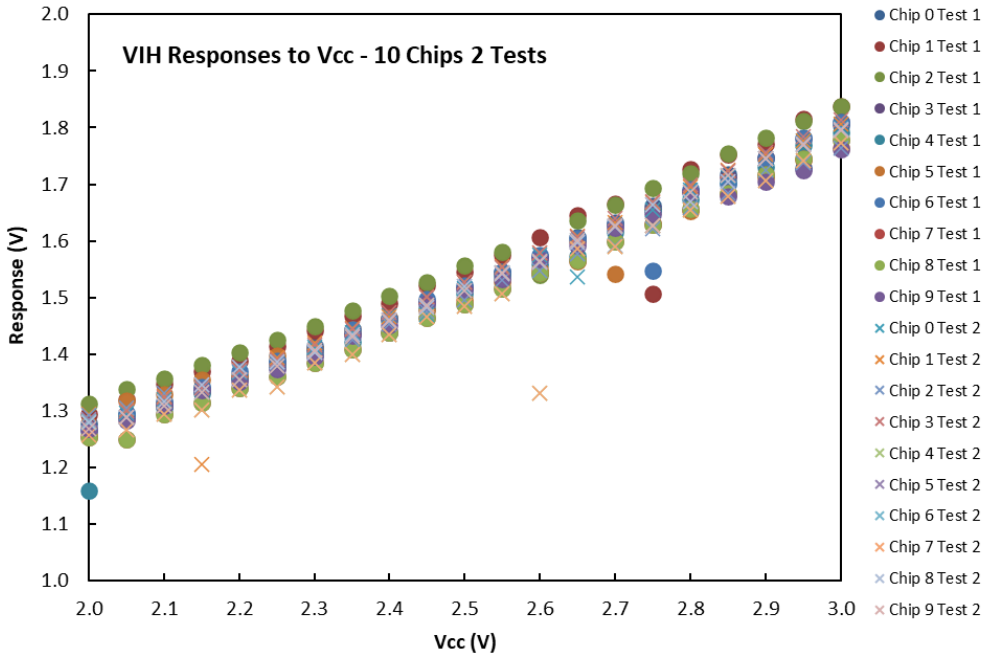


Figure 25 VIH Responses to Ramping Supply Voltage

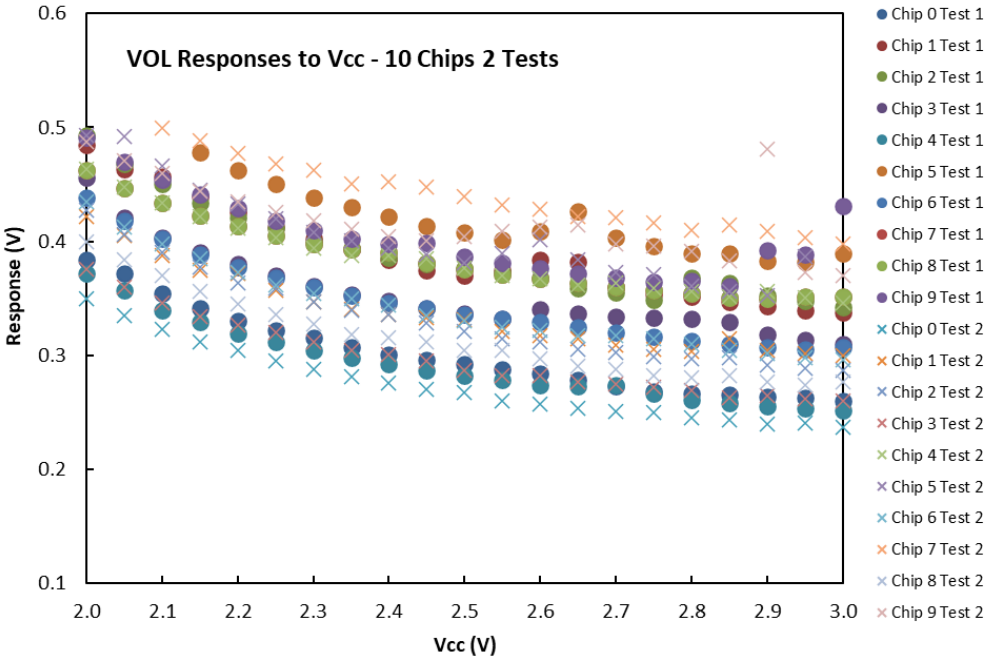


Figure 26 VOL Responses to Ramping Supply Voltage

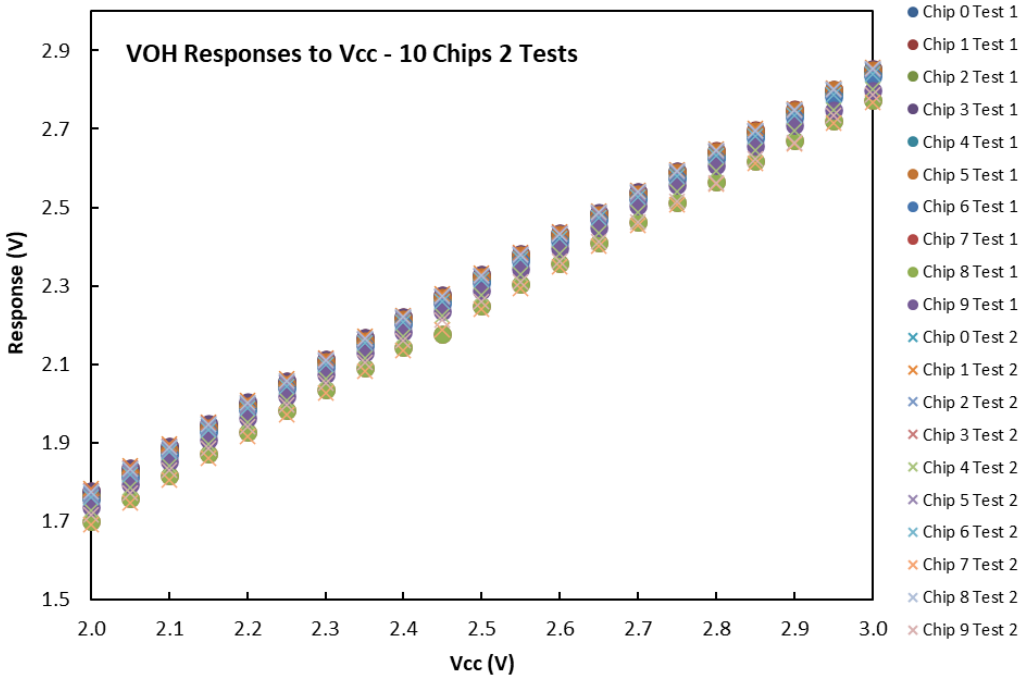


Figure 27 VOH Responses to Ramping Supply Voltage

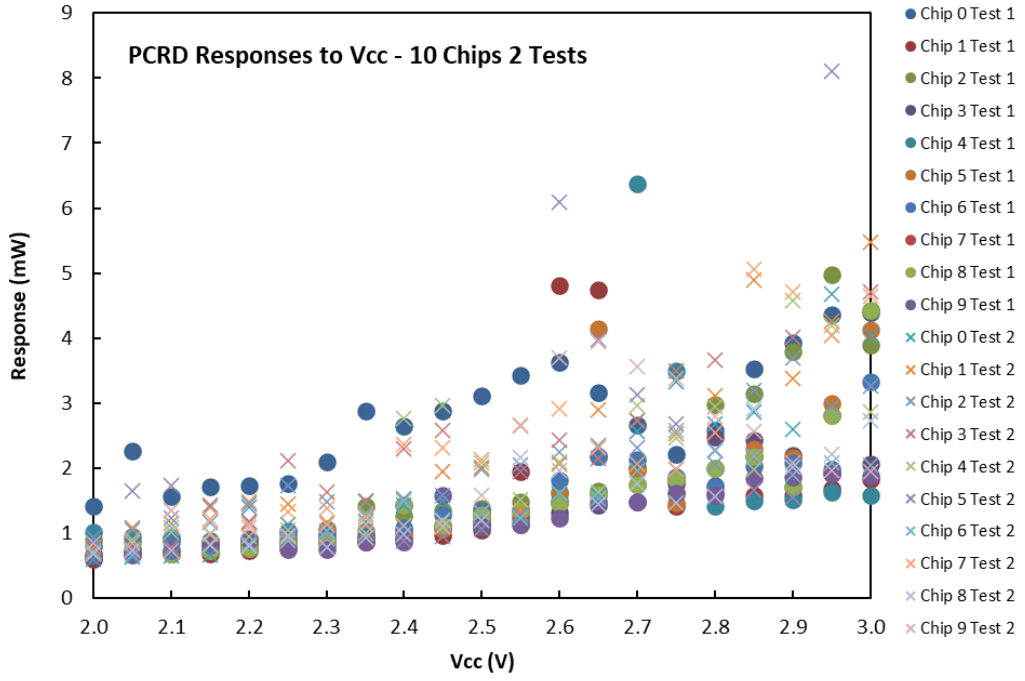


Figure 28 PCRD Responses to Ramping Supply Voltage

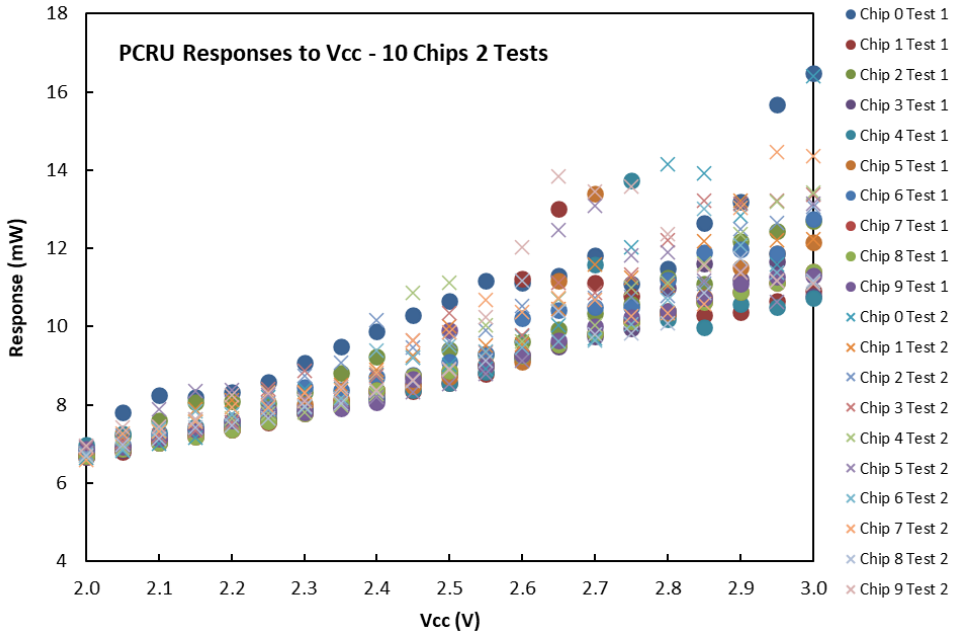


Figure 29 PCRU Responses to Ramping Supply Voltage

7. DISCUSSIONS

The results from this research demonstrated that the supply voltage has the greatest impact on the responses of VIL, VIH, and VOH, which is consistent with the conclusion drawn from a previous iteration of the project. Both experiments stated that examining the output characteristics generated by supply voltage was most revealing in determining whether a microchip has been tampered with. One way to improve the experiment is to develop a method that allows the enclosure to maintain higher temperature and humidity values because experiments conducted in this research were limited to 70C temperature and 50% humidity.

In comparison to the previous iteration of the project, this experimental setup is tedious due to the complexity of this research, but total testing time was significantly less thanks to the optimized starting points.

To reach and maintain the desired temperatures and RH simultaneously is always a challenge. For example, it takes about an hour for the enclosure to reach 80C temperature if humidity is not involved. With humidity being a factor to be considered as well, it would take one and half hours for the enclosure to reach about 70C took and 50% RH. Even the targeted temperature and humidity are achieved, it is never easy to maintain them at a steady state (fluctuation within +- 1%) for 45 min as required for data collection. It should also be mentioned that it takes a long time for the enclosure to go back to ambient temperature and humidity from a set condition. All these challenges would need to be dealt with in the future by further improving the experimental setup.

8. CONCLUSIONS

The effects of temperature, humidity, and supply voltage on VIL, VIH, VOL, VOH, and power consumption were thoroughly studied in this research over ten microchips with the DOE experimental design technique. Factorial analysis of the experimental data clearly shows that supply voltage is the most influential factor that can generate strong VIL, VIH and VOH responses which can be used to differentiate abnormal microchips from normal ones. The consistent and repeatable trend data of VIL, VIH and VOH against ramping supply voltage have further validated the experimental setup and data collection methodology being effective for setting the baseline responses for normal microchips and for detecting irregular or even tampered microchips by comparing the output values with the baseline.

It is highly recommended that more tests be conducted with higher temperatures and humidity to confirm the validity of the above conclusions for expanded testing conditions. In the meantime, different microchips such as aged, defective, counterfeited, refurbished, or tampered chips should be tested along with the normal chips simultaneously to generate comparable response data side by side in the same enclosure. This would be the best way to further confirm the methodology used in this research for microchip characterization and differentiation.

WORKS CITED

[1] Lecomte, Maxime, et al. “An On-Chip Technique to Detect Hardware Trojans and Assist Counterfeit Identification.” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 25, no. 12, Institute of Electrical and Electronics Engineers (IEEE), Dec. 2017, pp. 3317–30. https://doi.org/10.1109/tvlsi.2016.2627525.

[2] Xiao, Kan, et al. “A Clock Sweeping Technique for Detecting Hardware Trojans Impacting Circuits Delay.” *IEEE Design &Amp; Test*, vol. 30, no. 2, Institute of Electrical and Electronics Engineers (IEEE), Apr. 2013, pp. 26–34. https://doi.org/10.1109/mdat.2013.2249555.

[3] Rad, Reza, et al. “A Sensitivity Analysis of Power Signal Methods for Detecting Hardware Trojans Under Real Process and Environmental Conditions.” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 18, no. 12, Institute of Electrical and Electronics Engineers (IEEE), 2010, pp. 1735–44. https://doi.org/10.1109/tvlsi.2009.2029117.

[4] Zhou, Boyou, et al. “Detecting Hardware Trojans Using Backside Optical Imaging of Embedded Watermarks.” *Proceedings of the 52nd Annual*

Design Automation Conference, ACM, June 2015, https://doi.org/10.1145/2744769.2744822.

[5] He, Kai, et al. “EM-based On-chip Aging Sensor for Detection and Prevention of Counterfeit and Recycled ICs.” *2015 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, IEEE, Nov. 2015, https://doi.org/10.1109/iccad.2015.7372562.

[6] J.P. Morgan Chase. “How Long Will the Chip Shortage Last?: J.P. Morgan Research.” J.P. Morgan, J.P. Morgan Chase, 11 Aug. 2022, https://www.jpmorgan.com/insights/research/supply-chain-chip-shortage.

[8] “Chip Shortage: How the Semiconductor Industry Is Dealing With This Worldwide Problem.” *World Economic Forum*, 9 Sept. 2022, www.weforum.org/agenda/2022/02/semiconductor-chip-shortage-supply-chain.

[10] Salter, Jim. “Chip Shortages Lead to More Counterfeit Chips and Devices.” *Ars Technica*, 14 June 2021, arstechnica.com/gadgets/2021/06/chip-shortages-lead-to-more-counterfeit-chips-and-devices.

[11] Yang, Stephanie. “What’s Worse Than a Chip Shortage? Buying Fake Ones.” WSJ, 15 July 2021, www.wsj.com/articles/chip-shortage-has-spawned-a-surplus-of-fraudsters-and-fake-parts-11626255002.

[12] *What Is Design of Experiments (DOE)? | ASQ*. asq.org/quality-resources/design-of-experiments.

[13] Texas Instruments, “MSP430FG662x, MSP430FG642x Mixed-Signal Microcontrollers,” SLAS874B datasheet, May 2015 [Revised Sept. 2020]

[14] Texas Instruments, “Understanding Schmitt Triggers,” SCEA046 datasheet, Sept. 2011

APPENDIX A

DOE RAW DATA

	Main Effects			Interactions				Response				
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.294225	1.83615	0.312164	2.675575	3.0186875	27.71815
2	1	1	-1	1	-1	-1	-1	0.79375	1.29865	0.270089	1.740825	1.0305525	7.5845925
3	1	-1	1	-1	1	-1	-1	1.30765	1.806675	0.2630845	2.7429525	1.201025	16.36815
4	1	-1	-1	-1	-1	1	1	0.889	1.29065	0.221756	1.7704375	0.63007675	6.6493975
5	-1	1	1	-1	-1	1	-1	1.29785	1.8103	0.2641985	2.7500375	2.727725	16.183825
6	-1	1	-1	-1	1	-1	1	0.8088	1.296175	0.219289	1.7773725	0.61584275	6.7767025
7	-1	-1	1	1	-1	-1	1	1.3111	1.7862	0.25455275	2.7490825	1.089825	16.19435
8	-1	-1	-1	1	1	1	-1	0.804675	1.282	0.21277675	1.7774625	0.60849975	6.6429275

DOE Analysis Table Chip 0

	Main Effects			Interactions				Response				
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.349825	1.853775	0.3788395	2.6961125	10.0469875	24.884575
2	1	1	-1	1	-1	-1	-1	0.84515	1.328175	0.288458	1.71116	1.2691925	19.28855
3	1	-1	1	-1	1	-1	-1	1.333325	1.8371	0.26954225	2.752645	1.2827475	16.354675
4	1	-1	-1	-1	-1	1	1	0.834525	1.2946	0.22138525	1.7821075	0.568012	6.5838775
5	-1	1	1	-1	-1	1	-1	1.333	1.835275	0.2873345	2.759425	1.8565925	17.495925
6	-1	1	-1	-1	1	-1	1	0.829525	1.2933	0.23481525	1.786775	0.56001275	6.64528
7	-1	-1	1	1	-1	-1	1	1.335775	1.824775	0.3246495	2.7055525	1.2616775	16.544225
8	-1	-1	-1	1	1	1	-1	0.831575	1.288475	0.29762375	1.7463175	0.57009025	6.5839075

DOE Analysis Table Chip 1

	Main Effects			Interactions				Response				
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.38355	1.8269	0.310606	2.700615	1.84395	28.617075
2	1	1	-1	1	-1	-1	-1	0.82615	1.3285	0.24094625	1.7188975	1.1222325	14.280525
3	1	-1	1	-1	1	-1	-1	1.329175	1.7525	0.26726375	2.7481475	1.0723075	16.135225
4	1	-1	-1	-1	-1	1	1	0.818225	1.273275	0.2193445	1.775985	0.617274	6.618585
5	-1	1	1	-1	-1	1	-1	1.31505	1.81655	0.2703515	2.756255	1.9185425	13.0673375
6	-1	1	-1	-1	1	-1	1	0.811425	1.290075	0.2146625	1.7840675	2.15228875	5.1594035
7	-1	-1	1	1	-1	-1	1	1.3261	1.8148	0.24288475	2.7563825	1.075425	16.100375
8	-1	-1	-1	1	1	1	-1	0.802	1.285175	0.19847025	1.7847075	0.60843125	6.616805

DOE Analysis Table Chip 2

	Main Effects			Interactions				Response				
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.295275	1.665875	0.35064925	2.67821	7.75453	15.198975
2	1	1	-1	1	-1	-1	-1	0.7931	1.2882	0.2629675	1.6896975	2.572585	9.203945
3	1	-1	1	-1	1	-1	-1	1.299125	1.78875	0.283207	2.75041	2.13307	16.93025
4	1	-1	-1	-1	-1	1	1	0.7983	1.281525	0.20475925	1.77749	0.69076475	6.6927075
5	-1	1	1	-1	-1	1	-1	1.2991	1.8149	0.24629225	2.75281	3.6998575	16.873525
6	-1	1	-1	-1	1	-1	1	0.7942	1.28835	0.19796625	1.7810475	0.62500725	6.759715
7	-1	-1	1	1	-1	-1	1	1.301975	1.81255	0.2407405	2.751975	1.376215	16.4299
8	-1	-1	-1	1	1	1	-1	0.79255	1.273525	0.19741875	1.7806975	0.62285175	6.6280575

DOE Analysis Table Chip 3

	Main Effects			Interactions				Response				
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.305425	1.796525	0.33383775	2.6644275	4.57276	27.5244
2	1	1	-1	1	-1	-1	-1	0.811475	1.2846	0.26127075	1.722895	1.3839125	8.0408775
3	1	-1	1	-1	1	-1	-1	1.3691	1.778975	0.24122725	2.744835	1.118965	16.181375
4	1	-1	-1	-1	-1	1	1	0.84945	1.2281	0.19536525	1.7753275	0.62940075	6.629435
5	-1	1	1	-1	-1	1	-1	1.34635	1.78265	0.2464355	2.733555	4.53176	17.91135
6	-1	1	-1	-1	1	-1	1	0.828025	1.25805	0.1958045	1.770665	0.65016325	6.781305
7	-1	-1	1	1	-1	-1	1	1.36915	1.7611	0.22713225	2.7508375	1.1229275	16.193
8	-1	-1	-1	1	1	1	-1	0.843675	1.25095	0.1850795	1.780215	0.6299005	6.611

DOE Analysis Table Chip 4

	Main Effects			Interactions				Response				
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.321525	1.85305	0.37449725	2.6862675	7.8028325	26.4856
2	1	1	-1	1	-1	-1	-1	0.81395	1.342425	0.41011575	1.7277525	1.343915	12.428475
3	1	-1	1	-1	1	-1	-1	1.370175	1.77355	0.26444475	2.7551325	1.1716725	16.360125
4	1	-1	-1	-1	-1	1	1	0.865775	1.26435	0.214406	1.78277	0.60207875	6.624085
5	-1	1	1	-1	-1	1	-1	1.386475	1.75945	0.284517	2.756425	1.5292675	17.1609
6	-1	1	-1	-1	1	-1	1	0.8733	1.26785	0.22347525	1.784355	0.62934925	6.7746025
7	-1	-1	1	1	-1	-1	1	1.364625	1.772725	0.250046	2.7563825	1.18828	16.260875
8	-1	-1	-1	1	1	1	-1	0.859525	1.266325	0.202773	1.7844825	0.61097625	6.5994725

DOE Analysis Table Chip 5

	Main Effects			Interactions				Response				
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.323575	1.827275	0.2613845	2.662875	2.612965	28.993275
2	1	1	-1	1	-1	-1	-1	0.795575	1.29715	0.216808	1.6925175	0.66654975	11.2516
3	1	-1	1	-1	1	-1	-1	1.27235	1.819575	0.25466375	2.7362025	1.138455	16.1896
4	1	-1	-1	-1	-1	1	1	0.79055	1.2633	0.20887875	1.767115	0.60833125	6.630745
5	-1	1	1	-1	-1	1	-1	1.26775	1.815725	0.24488275	2.7495275	1.3713225	16.6915
6	-1	1	-1	-1	1	-1	1	0.778725	1.281375	0.198084	1.7791475	0.60083875	6.65823
7	-1	-1	1	1	-1	-1	1	1.286725	1.787375	0.234603	2.7481575	1.064525	16.1222
8	-1	-1	-1	1	1	1	-1	0.786725	1.26625	0.19133975	1.77851	0.6010735	6.6248025

DOE Analysis Table Chip 6

	Main Effects			Interactions				Response					
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.2019	1.8227	0.350321	2.6080625	7.9395725	24.618275
2	1	1	-1	1	-1	-1	-1	0.787775	1.327	0.31562425	1.7182375	4.32297	9.8690725
3	1	-1	1	-1	1	-1	-1	1.4225	1.702675	0.27197225	2.715875	1.869885	17.209425
4	1	-1	-1	-1	-1	1	1	0.901175	1.15955	0.21353825	1.7600375	0.7032655	6.72346
5	-1	1	1	-1	-1	1	-1	1.313275	1.81175	0.256493	2.74139	2.9266725	17.564675
6	-1	1	-1	-1	1	-1	1	0.848375	1.2906	0.20062725	1.777855	0.6387225	6.738095
7	-1	-1	1	1	-1	-1	1	1.342225	1.77405	0.24131875	2.7429125	1.7407275	16.7729
8	-1	-1	-1	1	1	1	-1	0.8254	1.205225	0.19401275	1.778015	0.6166925	6.634025

DOE Analysis Table Chip 7

	Main Effects			Interactions				Response					
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.285175	1.83465	0.356158	2.6990775	7.4043725	28.972025
2	1	1	-1	1	-1	-1	-1	0.7892	1.311375	0.23717275	1.70616	2.3251275	17.378775
3	1	-1	1	-1	1	-1	-1	1.3157	1.807125	0.22579625	2.7550925	1.448955	16.19555
4	1	-1	-1	-1	-1	1	1	0.787075	1.27665	0.1905685	1.77994	0.609632	6.6265675
5	-1	1	1	-1	-1	1	-1	1.282875	1.804025	0.24258525	2.755895	2.0768175	17.513275
6	-1	1	-1	-1	1	-1	1	0.784025	1.274825	0.19524025	1.7832325	0.602357	6.745645
7	-1	-1	1	1	-1	-1	1	1.39265	1.6875	0.2267545	2.7550175	1.34201	16.493
8	-1	-1	-1	1	1	1	-1	0.808775	1.223275	0.1854975	1.7833025	0.6112435	6.64758

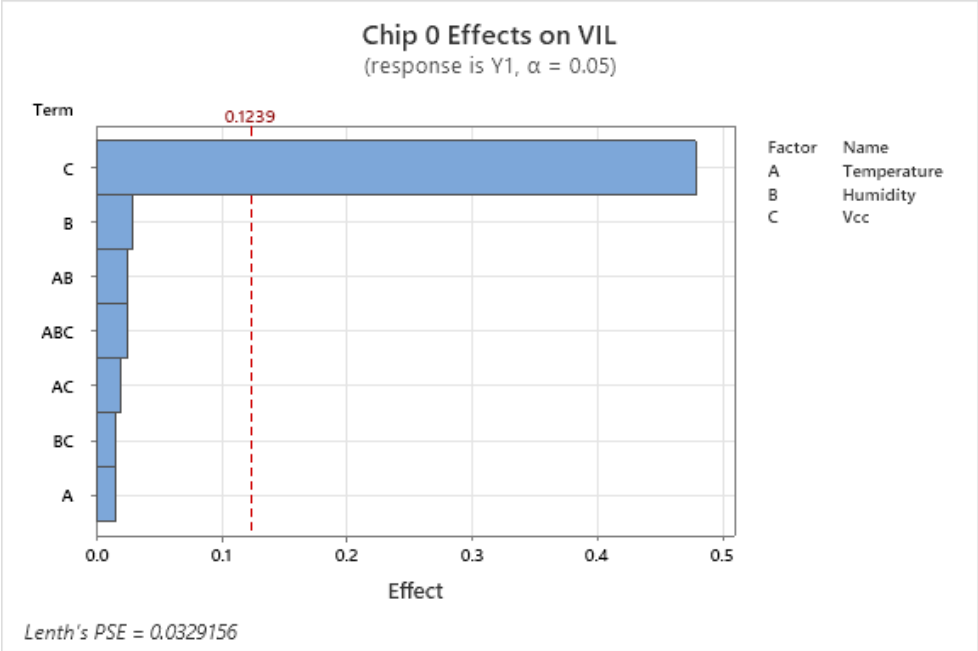
DOE Analysis Table Chip 8

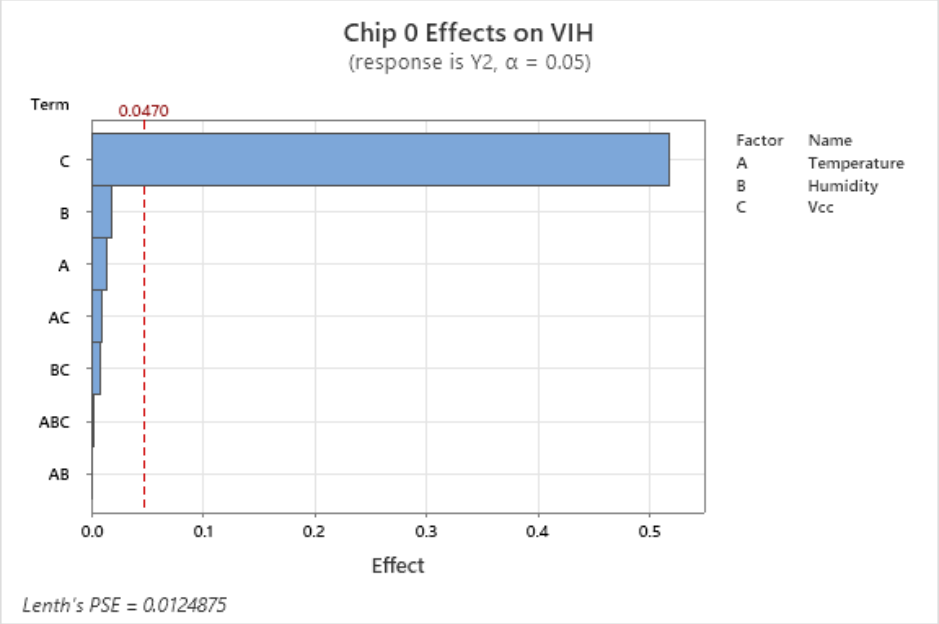
	Main Effects			Interactions				Response					
Test	A	B	C	A*B	A*C	B*C	A*B*C	Y1	Y2	Y3	Y4	Y5	Y6
1	1	1	1	1	1	1	1	1.304425	1.84385	0.34426825	2.657215	4.98192	27.305275
2	1	1	-1	1	-1	-1	-1	0.75385	1.310325	0.2742715	1.69099	1.42537	9.9298325
3	1	-1	1	-1	1	-1	-1	1.3064	1.7756	0.302736	2.7172725	1.165625	16.42645
4	1	-1	-1	-1	-1	1	1	0.845725	1.2763	0.25742525	1.7356875	0.61787825	6.6410275
5	-1	1	1	-1	-1	1	-1	1.31355	1.67195	0.307541	2.480465	3.553835	14.7170575
6	-1	1	-1	-1	1	-1	1	0.8113	1.27915	0.23609325	1.761265	0.61091925	6.7276975
7	-1	-1	1	1	-1	-1	1	1.3086	1.79485	0.30350925	2.7211475	1.0815725	16.153525
8	-1	-1	-1	1	1	1	-1	0.8045	1.2745	0.24323525	1.74505	0.61126075	6.6005925

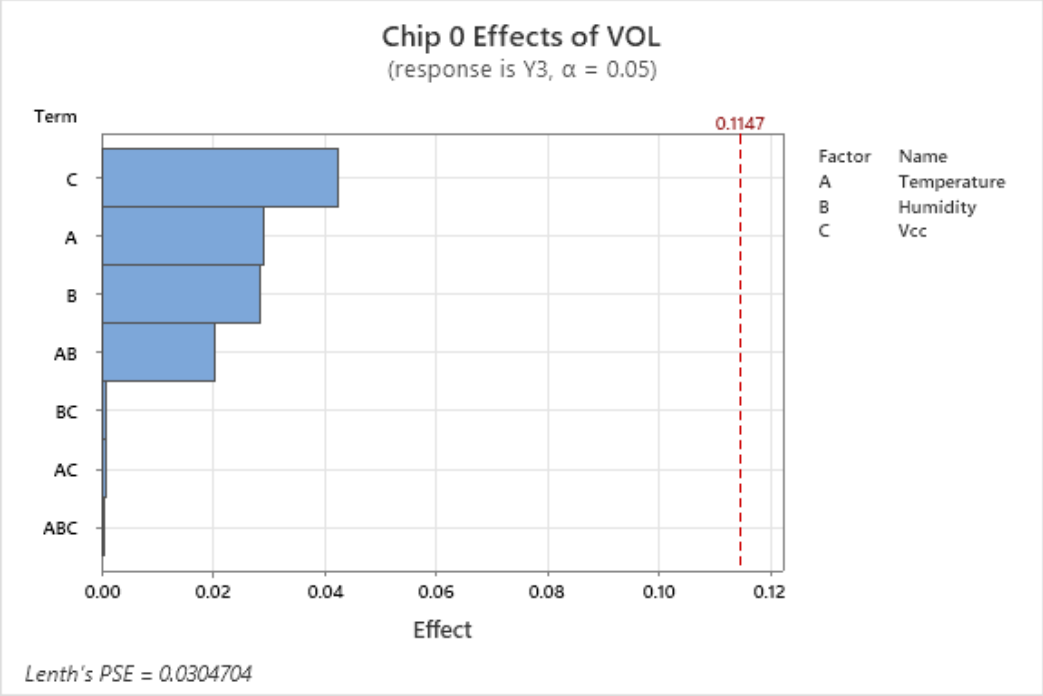
DOE Analysis Table Chip 9

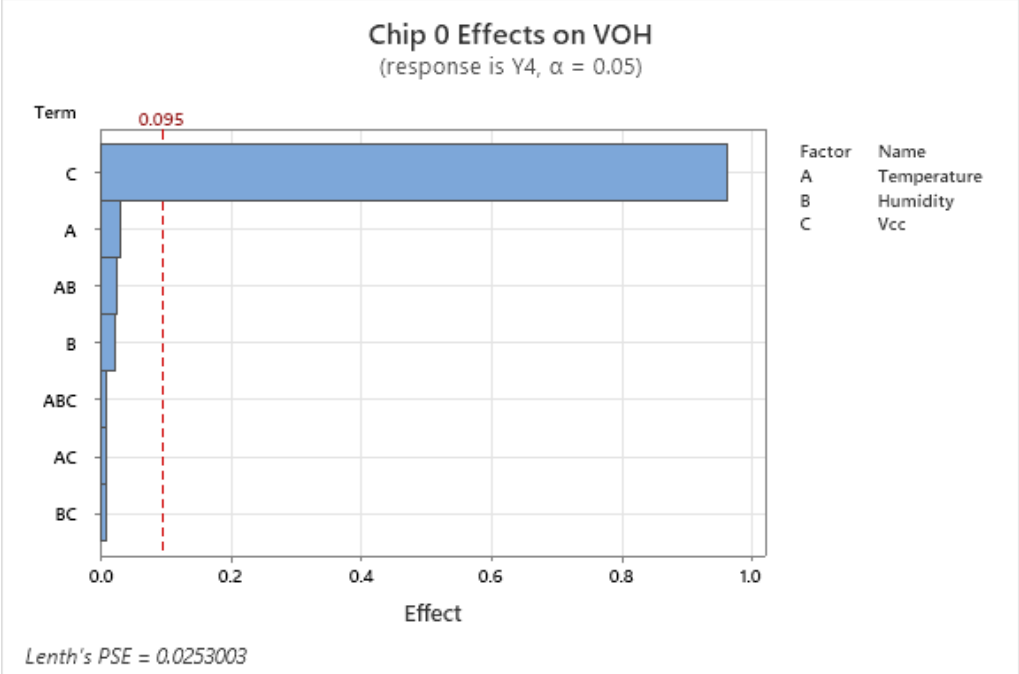
APPENDIX B

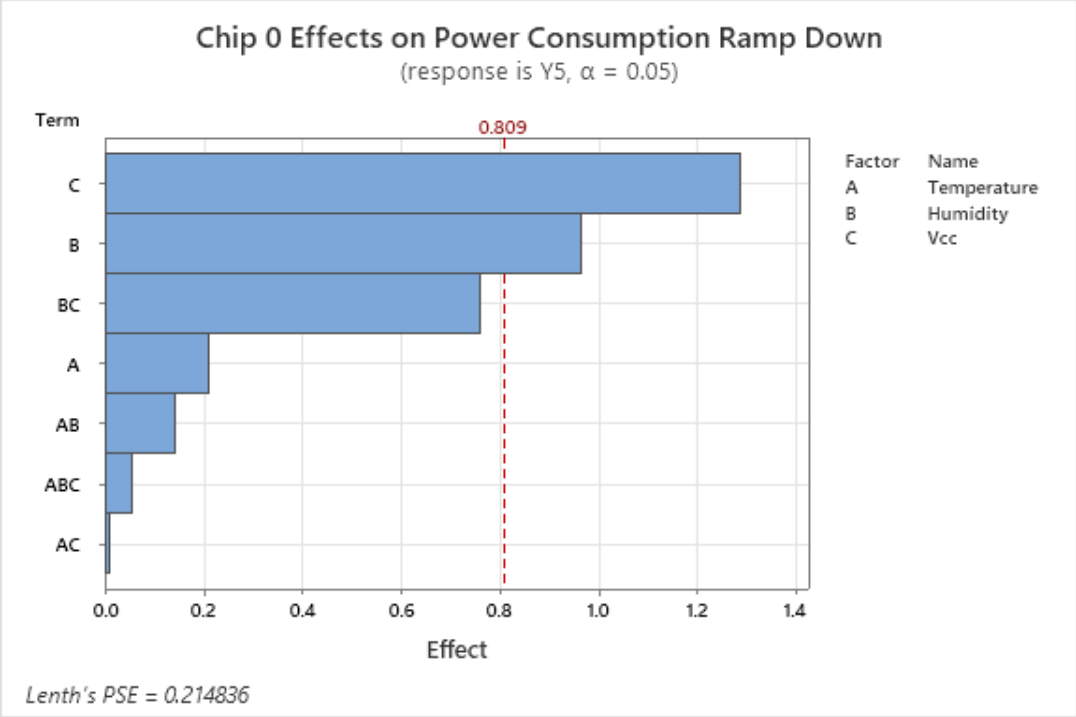
DOE PARETO CHARTS



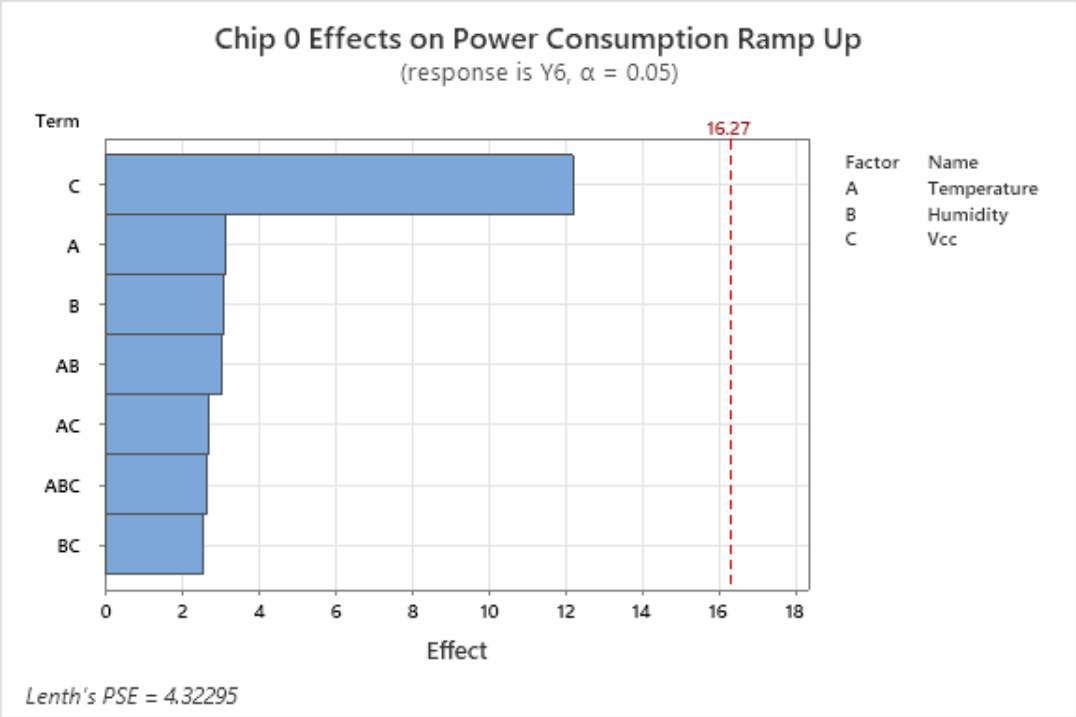



Chip 0 Effects of VOL
(response is Y3, α = 0.05)
Term
0.1147
C
A
B
AB
BC
AC
ABC
0.00
0.02
0.04
0.06
0.08
0.10
0.12
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0304704

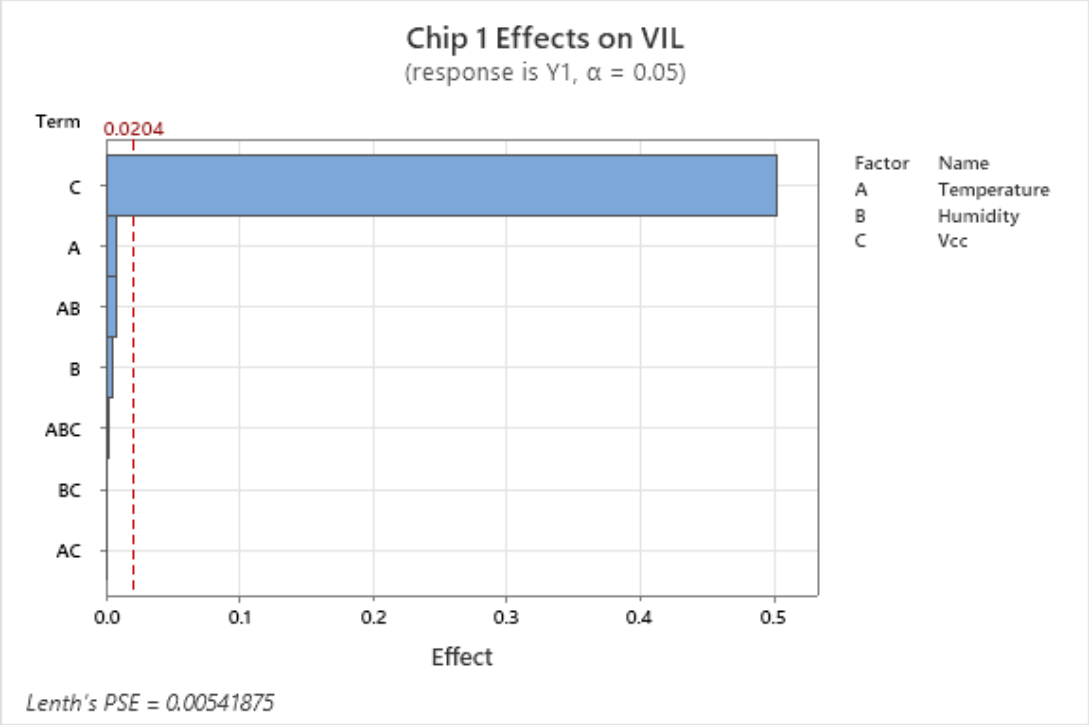

Chip 0 Effects on VOH
(response is Y4, α = 0.05)
Term
0.095
C
A
AB
B
ABC
AC
BC
0.0
0.2
0.4
0.6
0.8
1.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0253003

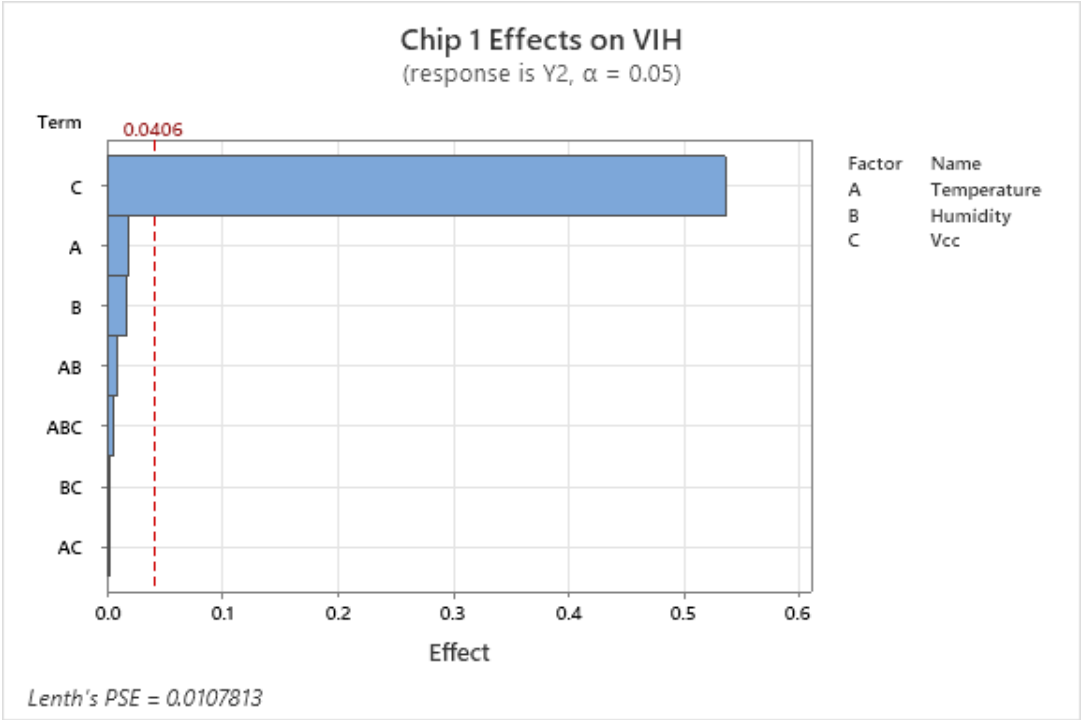


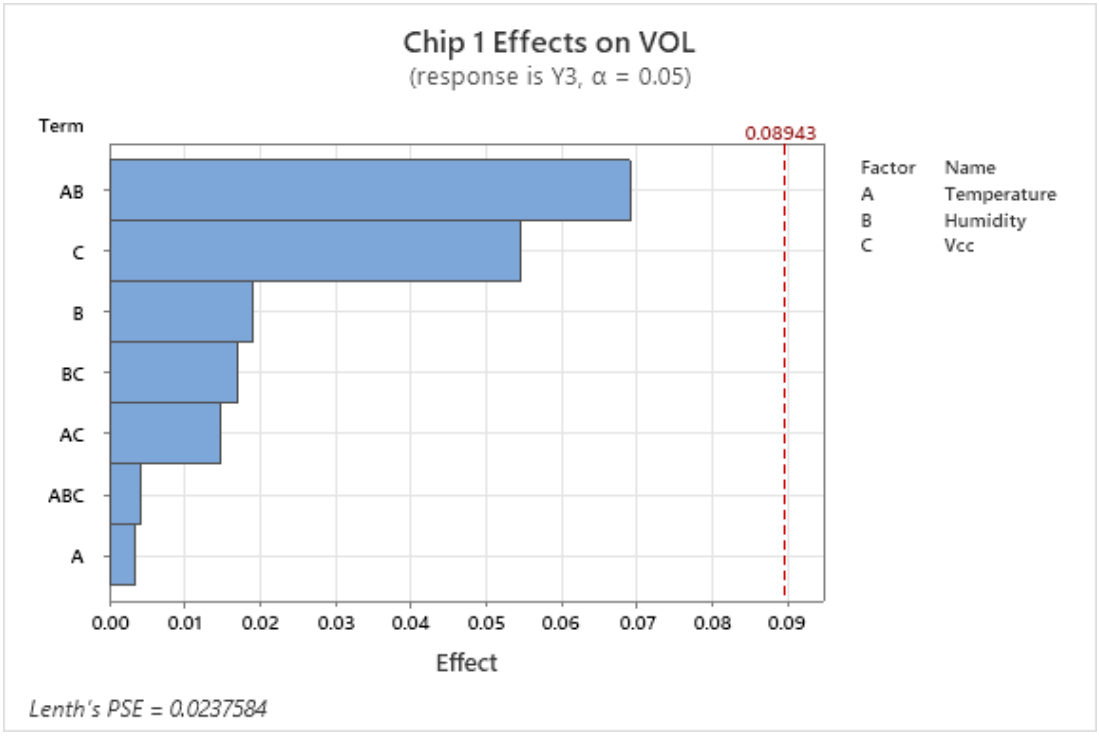
Lenth's PSE = 0.214836

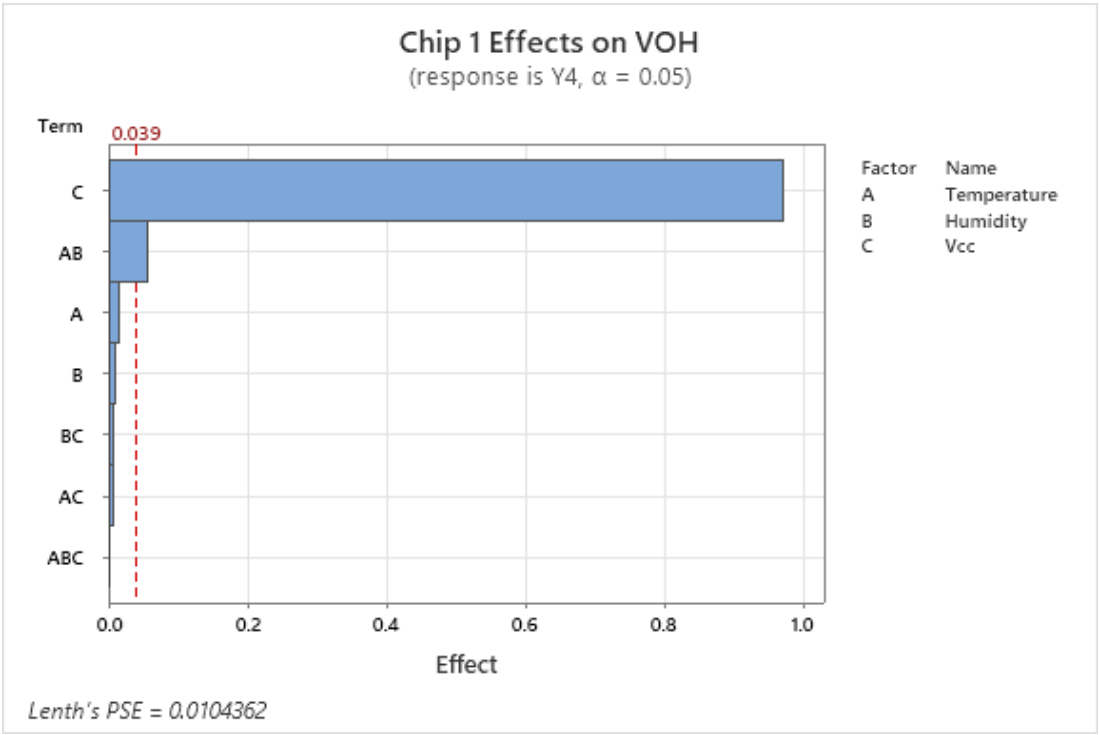


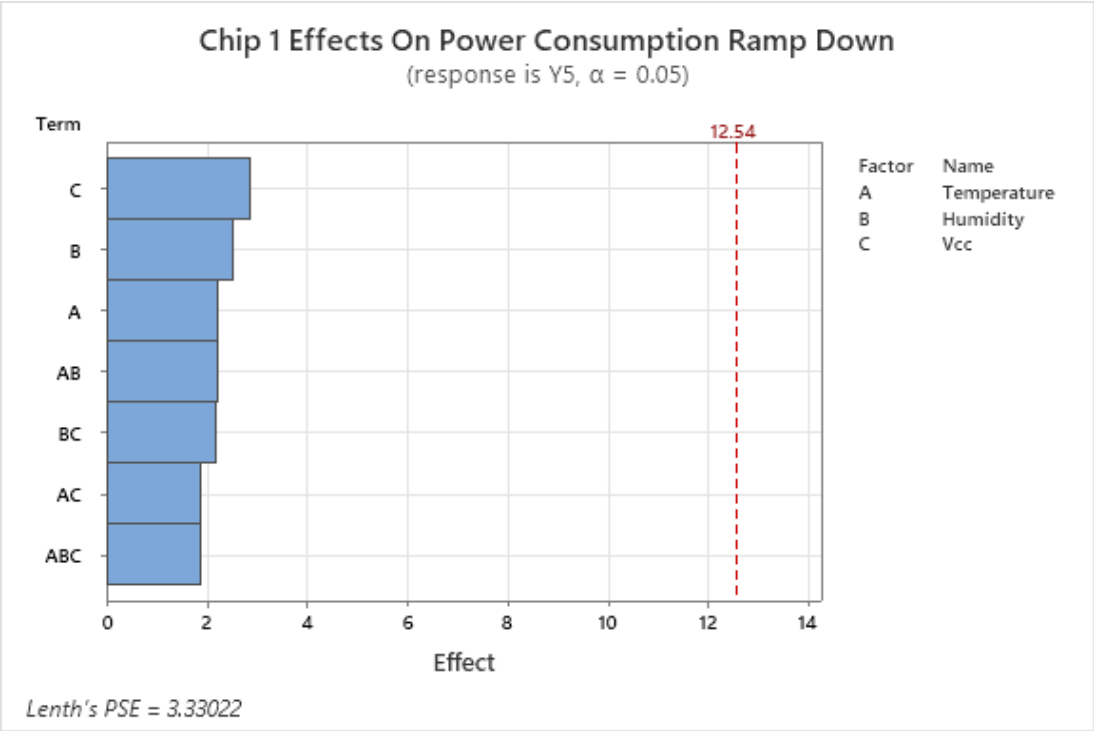
Lenth's PSE = 4.32295

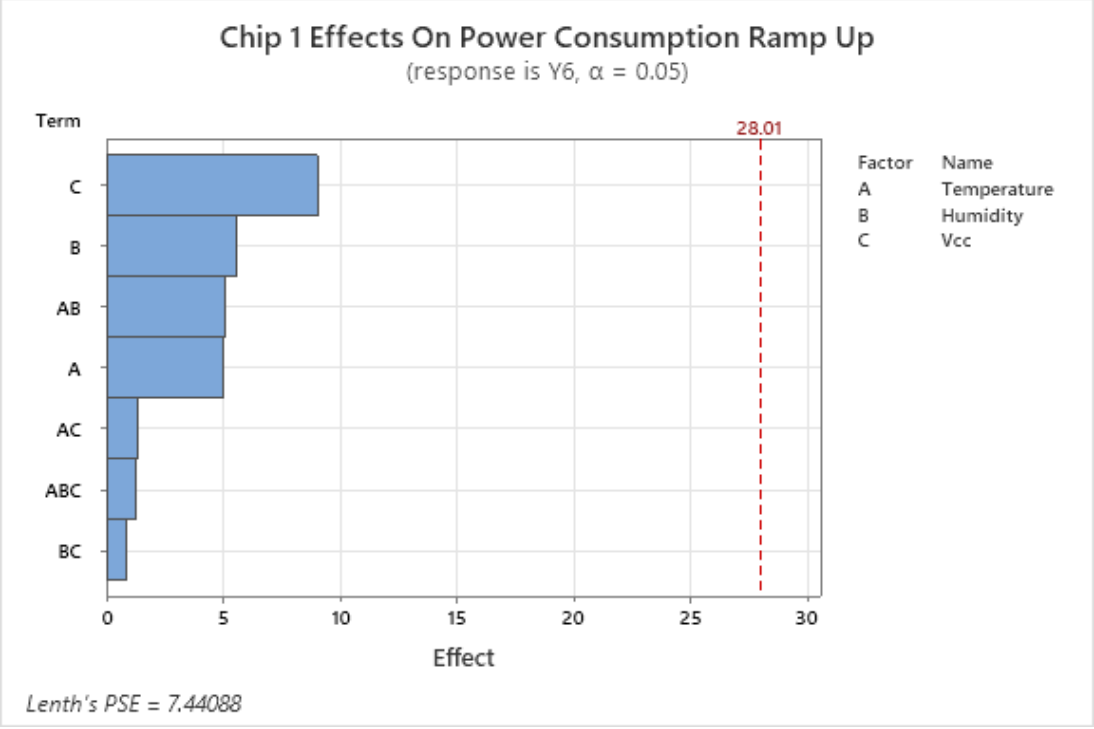

Chip 1 Effects on VIL
(response is Y1, α = 0.05)
Term
0.0204
C
A
AB
B
ABC
BC
AC
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.00541875

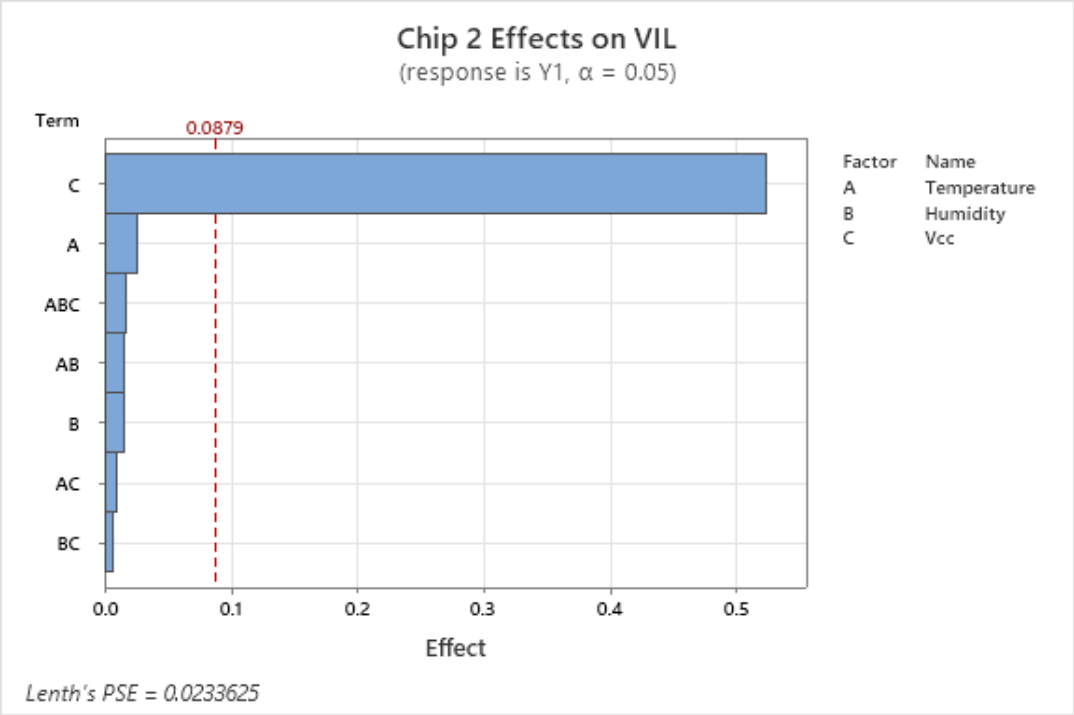

Chip 1 Effects on VIH
(response is Y2, α = 0.05)
Term
0.0406
C
A
B
AB
ABC
BC
AC
0.0
0.1
0.2
0.3
0.4
0.5
0.6
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0107813

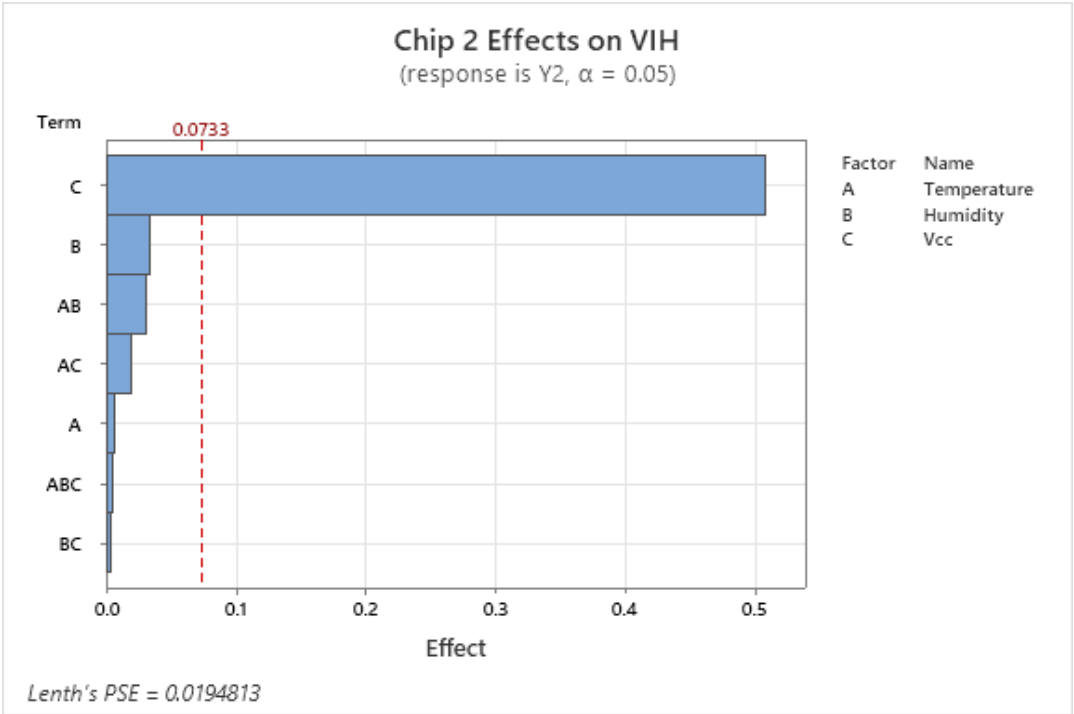

Chip 1 Effects on VOL
(response is Y3, α = 0.05)
Term
AB
C
B
BC
AC
ABC
A
0.08943
0.00
0.01
0.02
0.03
0.04
0.05
0.06
0.07
0.08
0.09
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0237584

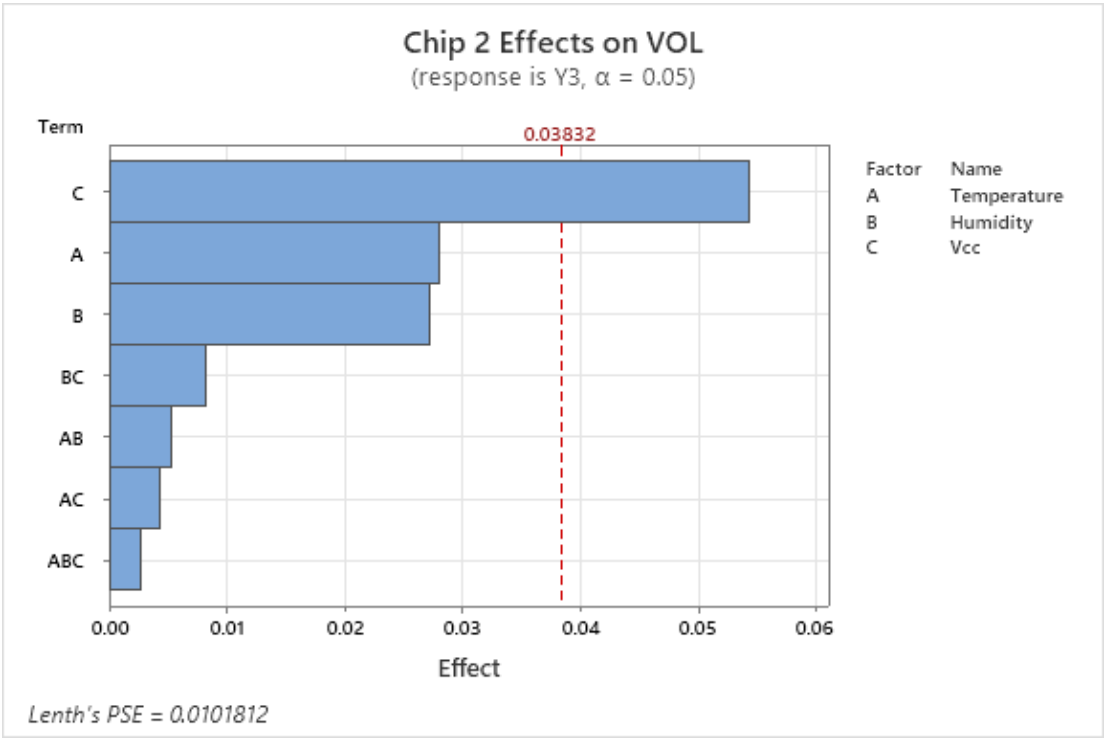

Chip 1 Effects on VOH
(response is Y4, α = 0.05)
Term
C
AB
A
B
BC
AC
ABC
0.039
0.0
0.2
0.4
0.6
0.8
1.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0104362

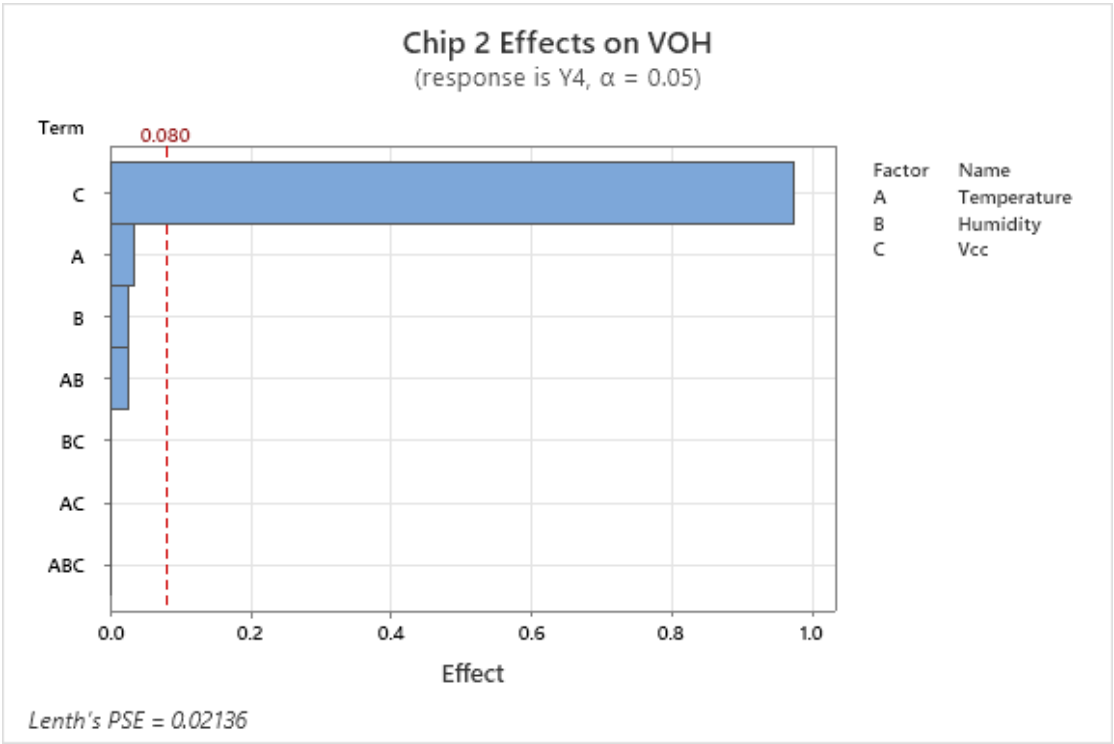

Chip 1 Effects On Power Consumption Ramp Down
(response is Y5, α = 0.05)
Term
C
B
A
AB
BC
AC
ABC
12.54
0
2
4
6
8
10
12
14
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 3.33022

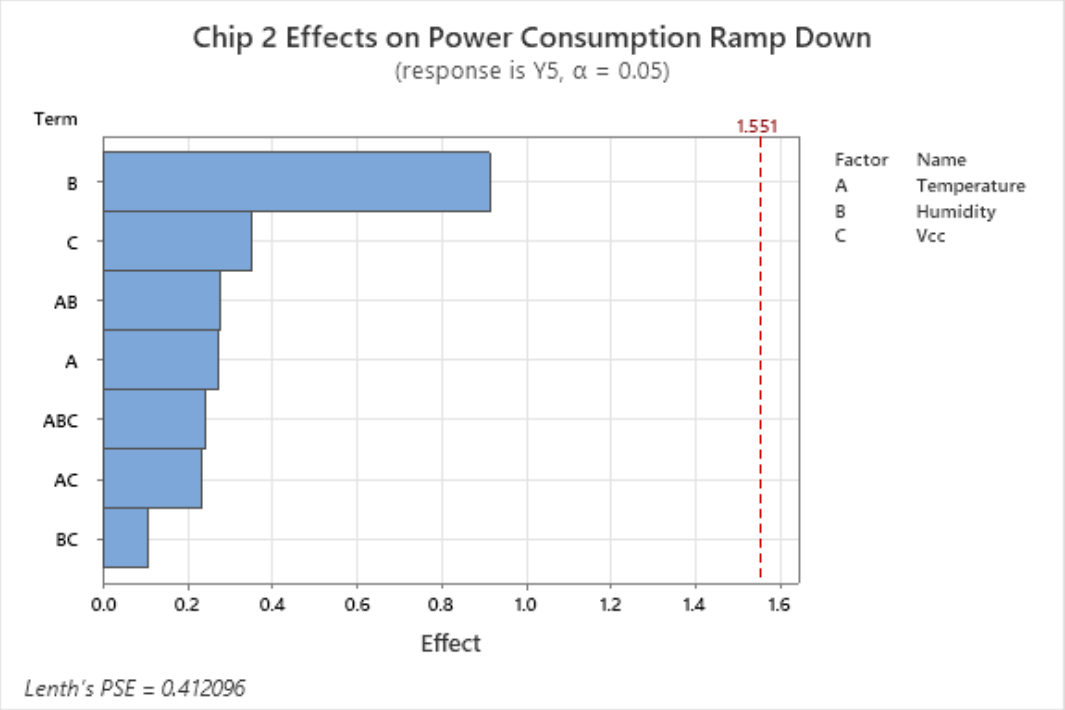

Chip 1 Effects On Power Consumption Ramp Up
(response is Y6, α = 0.05)
Term
C
B
AB
A
AC
ABC
BC
28.01
0
5
10
15
20
25
30
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 7.44088

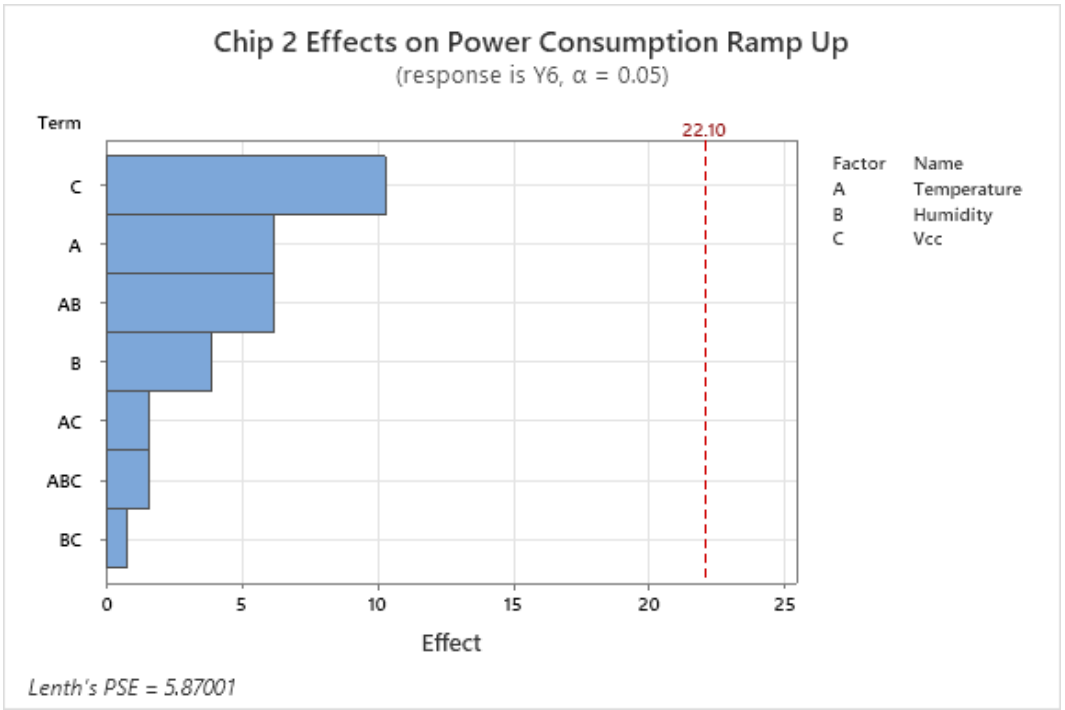

Chip 2 Effects on VIL
(response is Y1, α = 0.05)
Term
0.0879
C
A
ABC
AB
B
AC
BC
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0233625

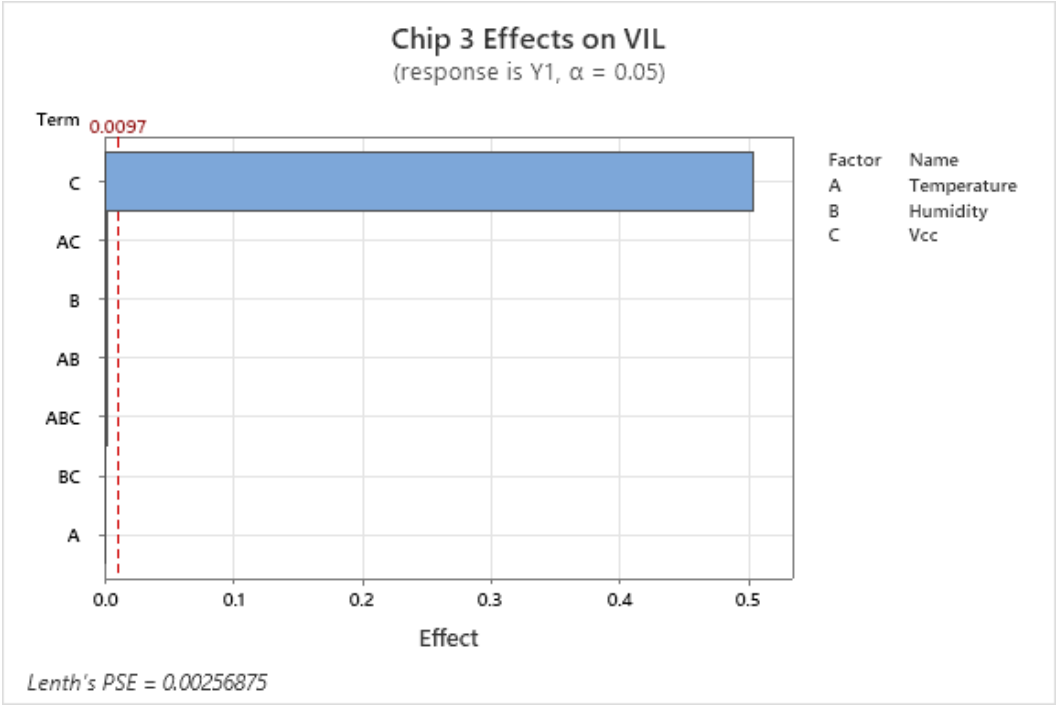

Chip 2 Effects on VIH
(response is Y2, α = 0.05)
Term
0.0733
C
B
AB
AC
A
ABC
BC
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0194813


Chip 2 Effects on VOL
(response is Y3, α = 0.05)
Term
0.03832
C
A
B
BC
AB
AC
ABC
0.00
0.01
0.02
0.03
0.04
0.05
0.06
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0101812

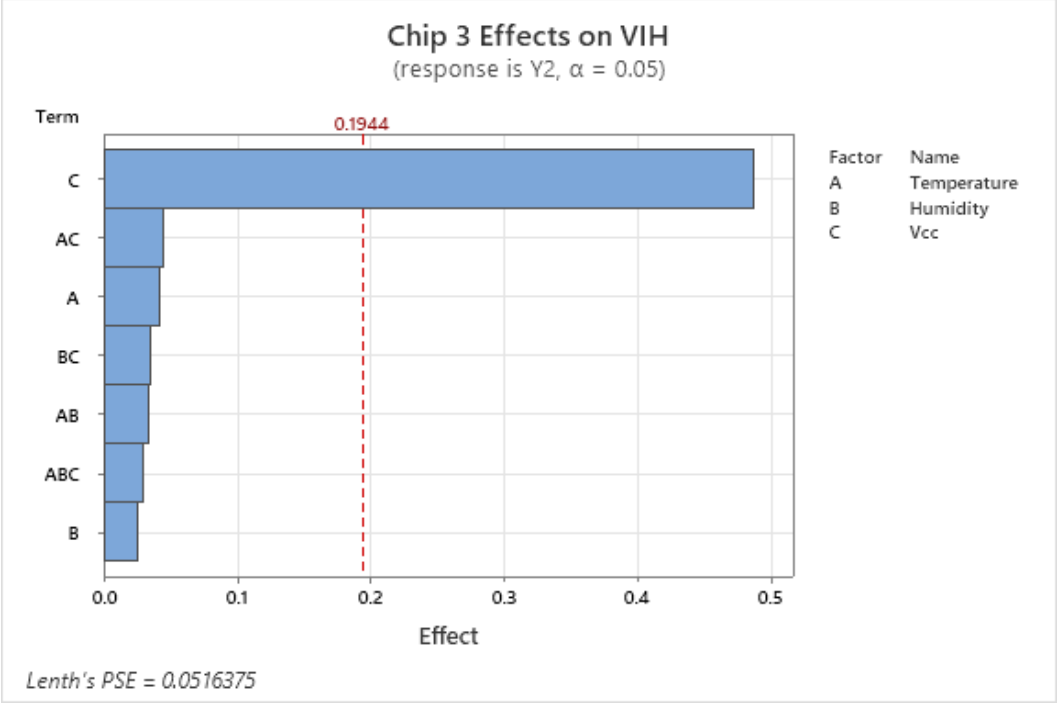

Chip 2 Effects on VOH
(response is Y4, α = 0.05)
Term
0.080
C
A
B
AB
BC
AC
ABC
0.0
0.2
0.4
0.6
0.8
1.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.02136


Chip 2 Effects on Power Consumption Ramp Down
(response is Y5, α = 0.05)
Term
B
C
AB
A
ABC
AC
BC
1.551
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.412096

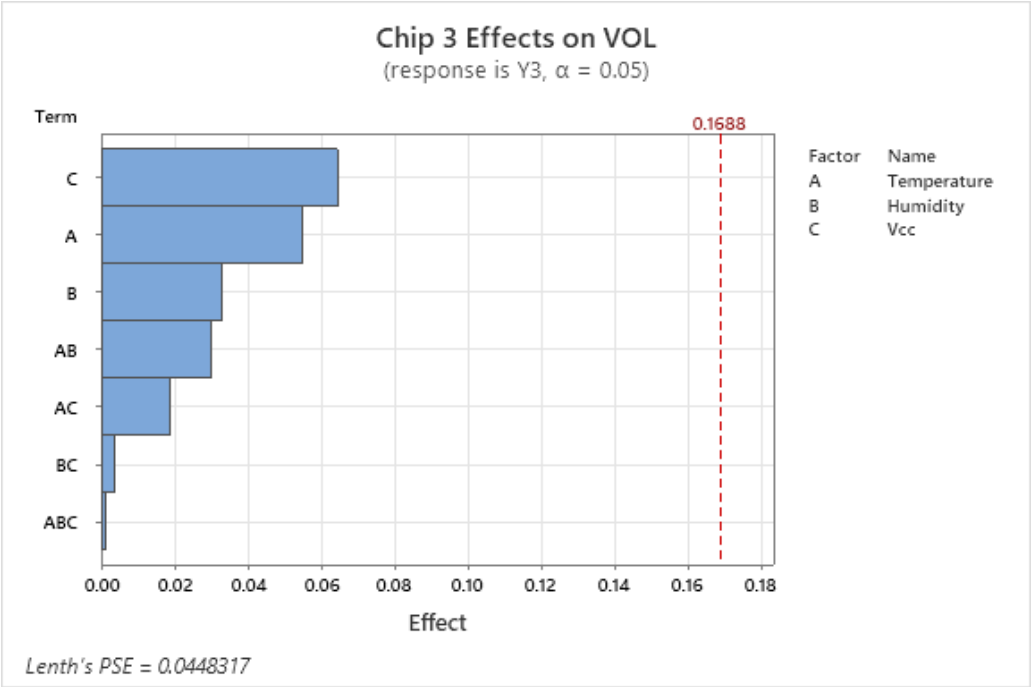

Chip 2 Effects on Power Consumption Ramp Up
(response is Y6, α = 0.05)
Term
C
A
AB
B
AC
ABC
BC
22.10
0
5
10
15
20
25
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 5.87001

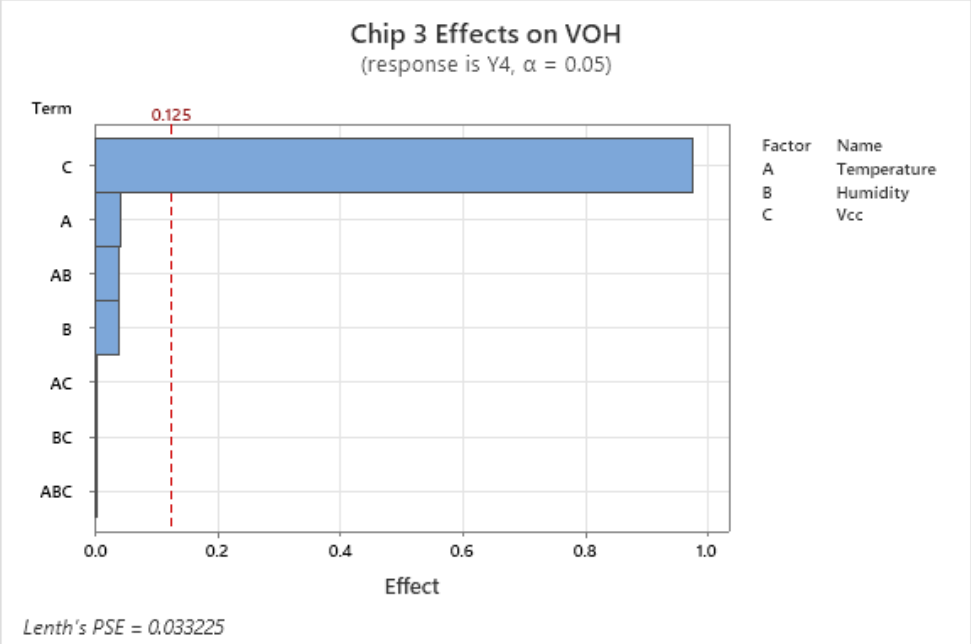


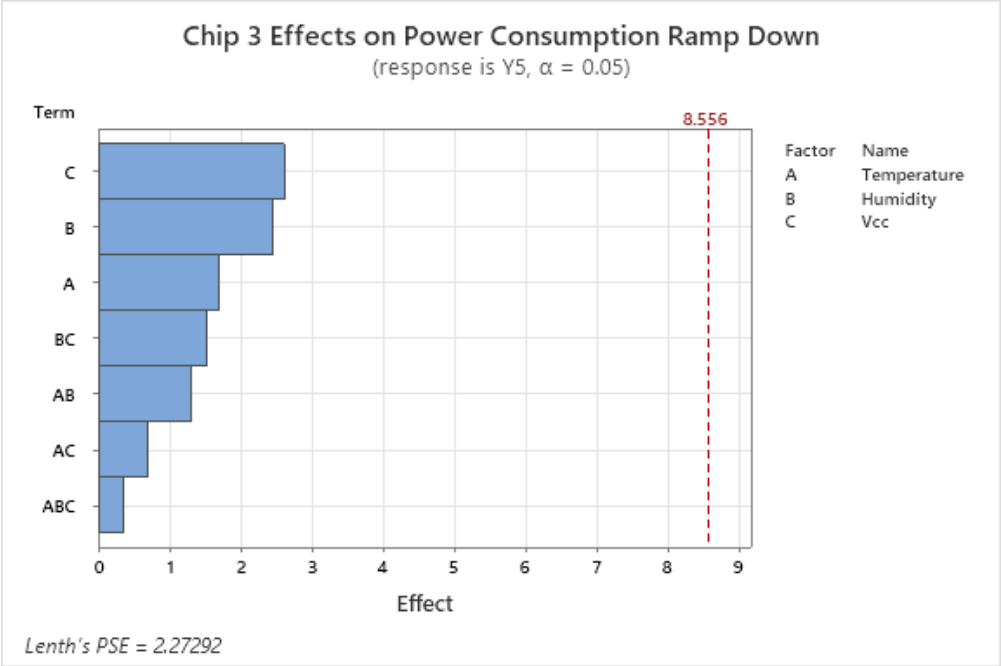
Lenth's PSE = 0.00256875

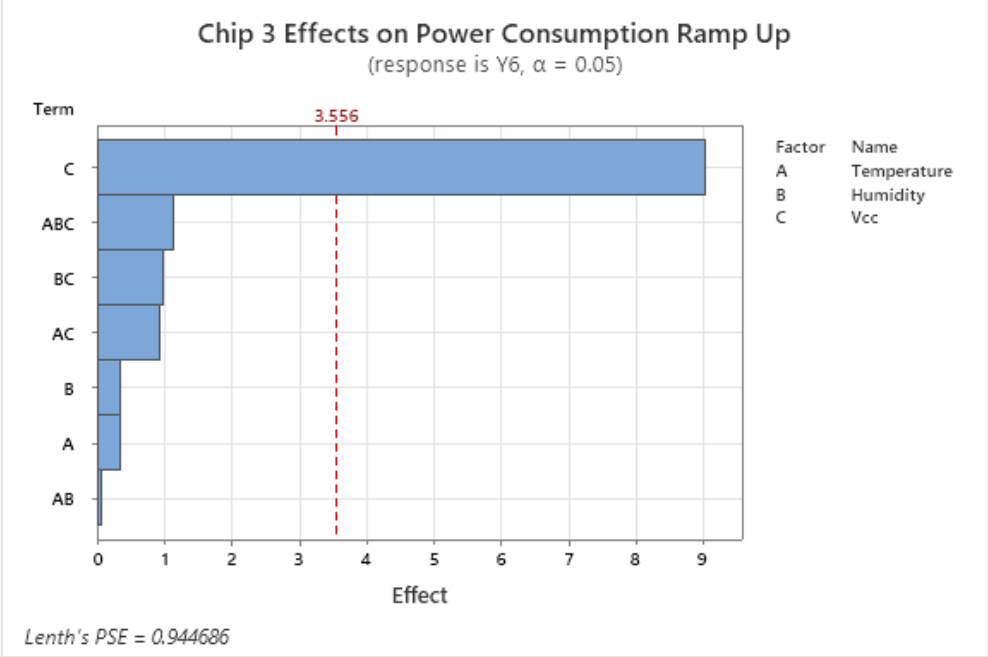


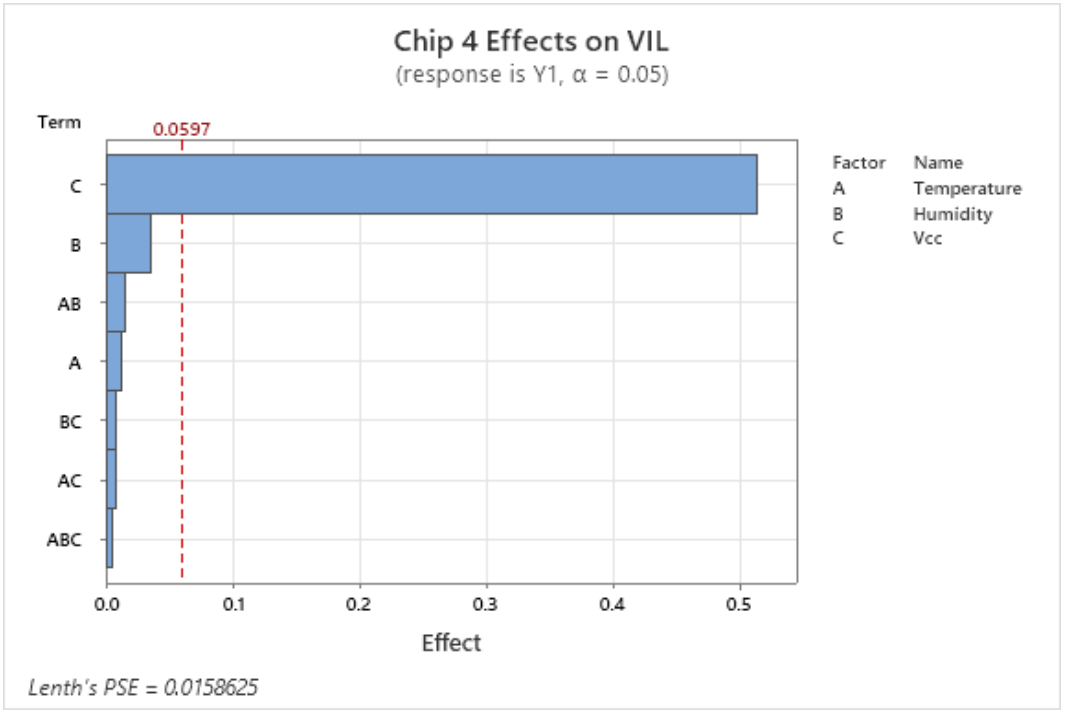
Lenth's PSE = 0.0516375

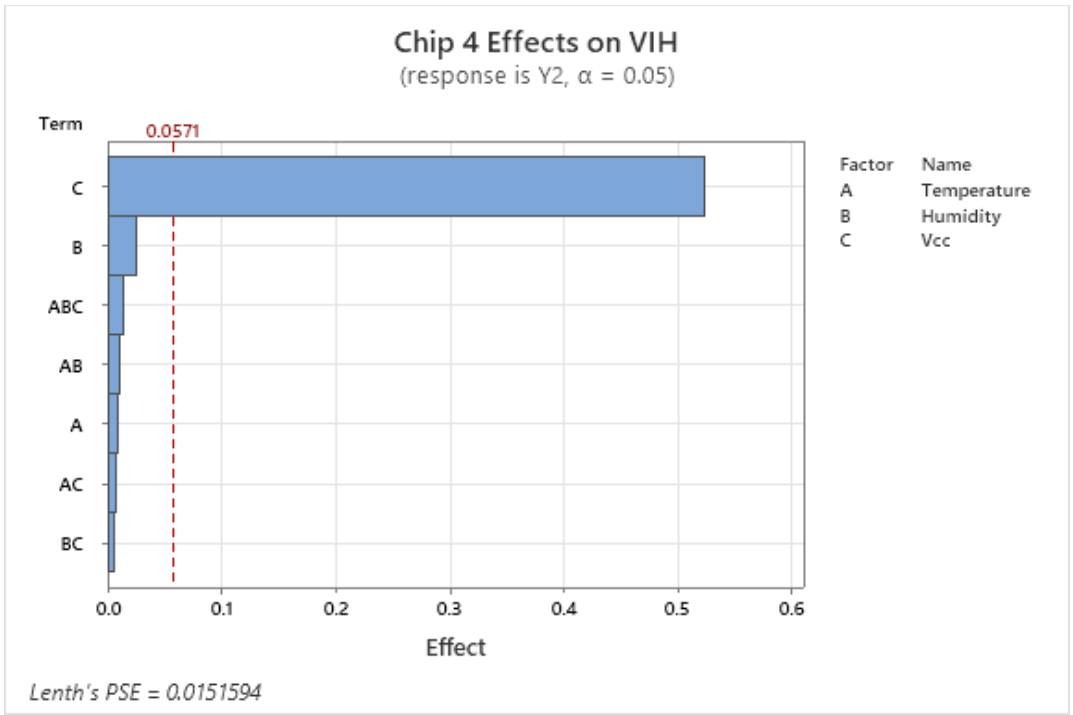

Chip 3 Effects on VOL
(response is Y3, α = 0.05)
Term
C
A
B
AB
AC
BC
ABC
0.1688
0.00
0.02
0.04
0.06
0.08
0.10
0.12
0.14
0.16
0.18
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0448317

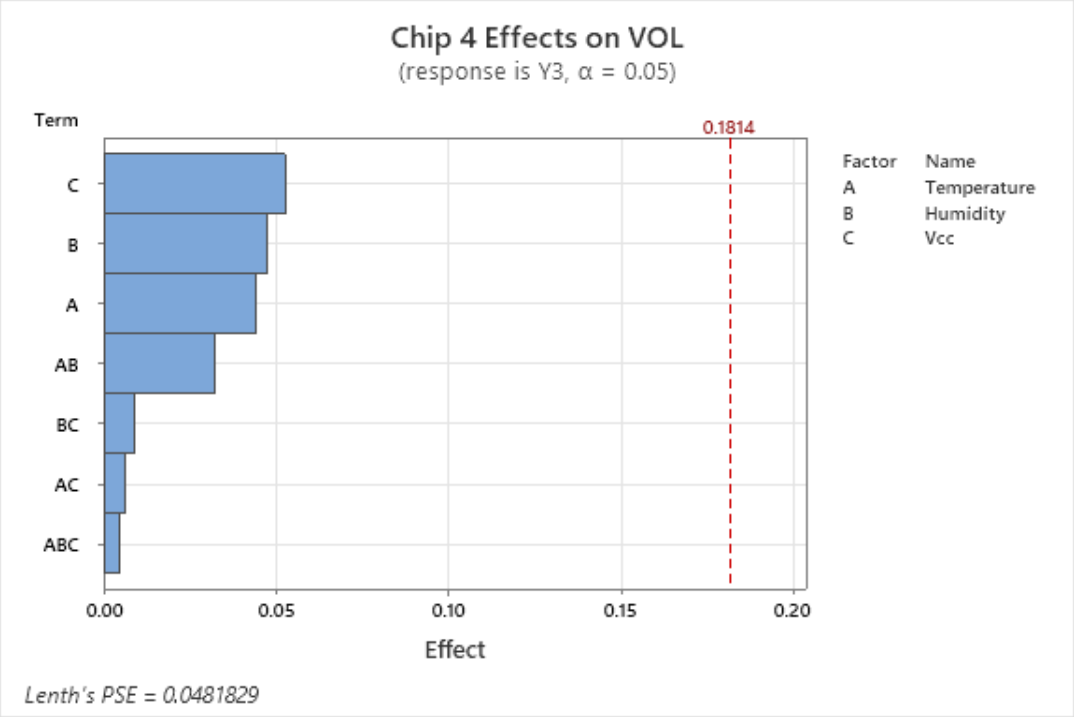

Chip 3 Effects on VOH
(response is Y4, α = 0.05)
Term
C
A
AB
B
AC
BC
ABC
0.125
0.0
0.2
0.4
0.6
0.8
1.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.033225

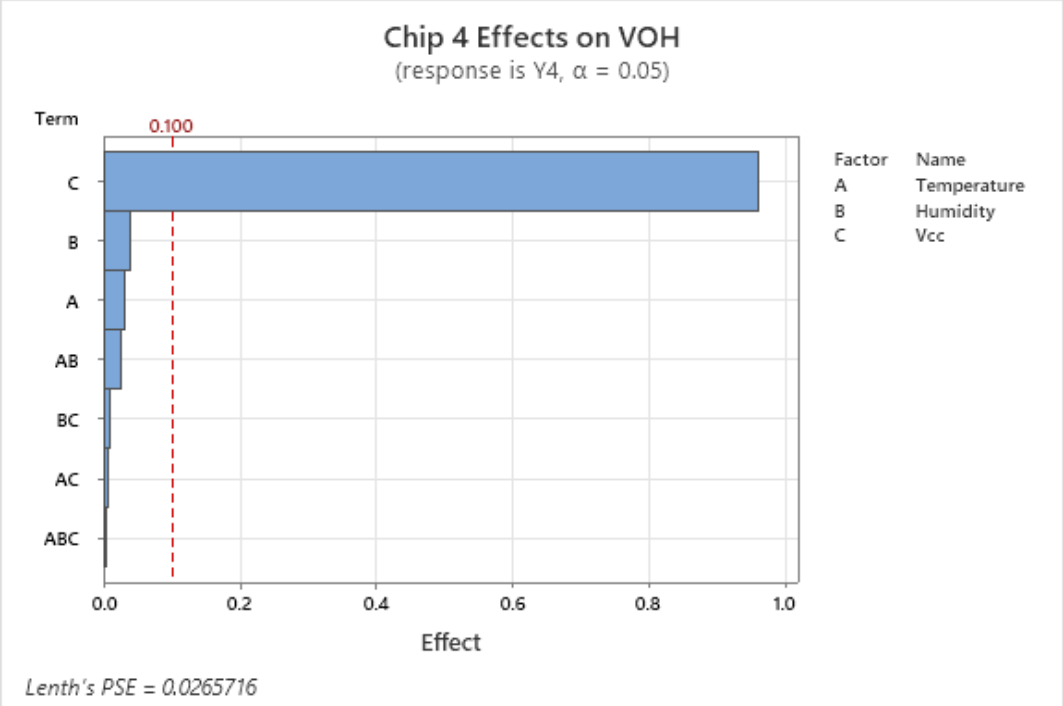

Chip 3 Effects on Power Consumption Ramp Down
(response is Y5, α = 0.05)
Term
C
B
A
BC
AB
AC
ABC
8.556
0
1
2
3
4
5
6
7
8
9
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 2.27292

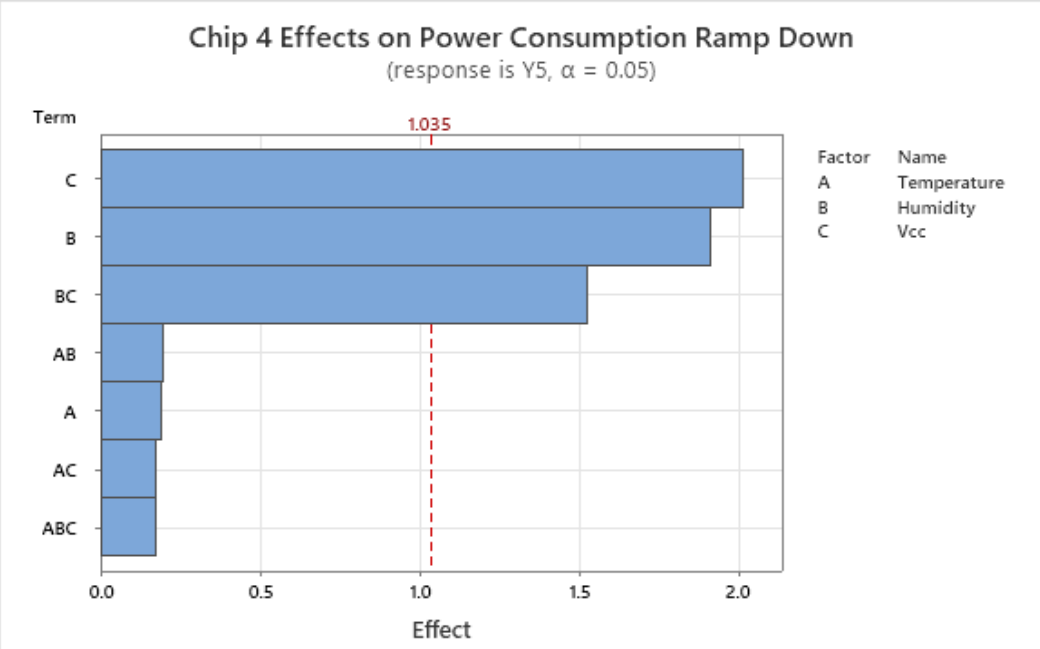

Chip 3 Effects on Power Consumption Ramp Up
(response is Y6, α = 0.05)
Term
C
ABC
BC
AC
B
A
AB
3.556
0
1
2
3
4
5
6
7
8
9
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.944686


Chip 4 Effects on VIL
(response is Y1, α = 0.05)
Term
0.0597
C
B
AB
A
BC
AC
ABC
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0158625

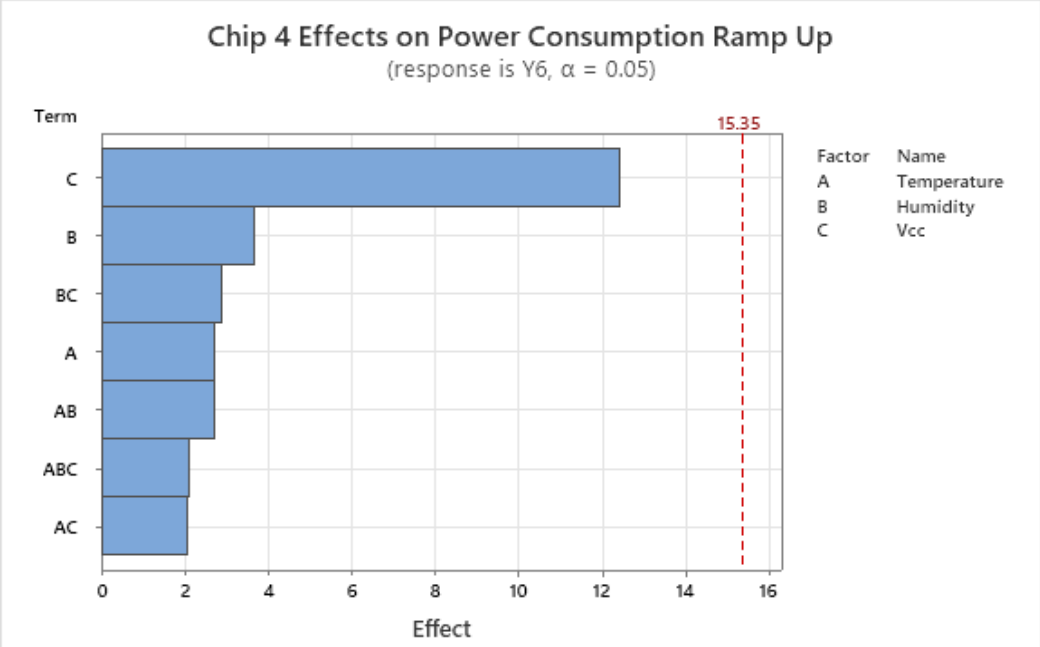

Chip 4 Effects on VIH
(response is Y2, α = 0.05)
Term
0.0571
C
B
ABC
AB
A
AC
BC
0.0
0.1
0.2
0.3
0.4
0.5
0.6
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0151594


Chip 4 Effects on VOL
(response is Y3, α = 0.05)
Term
C
B
A
AB
BC
AC
ABC
0.1814
0.00
0.05
0.10
0.15
0.20
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0481829

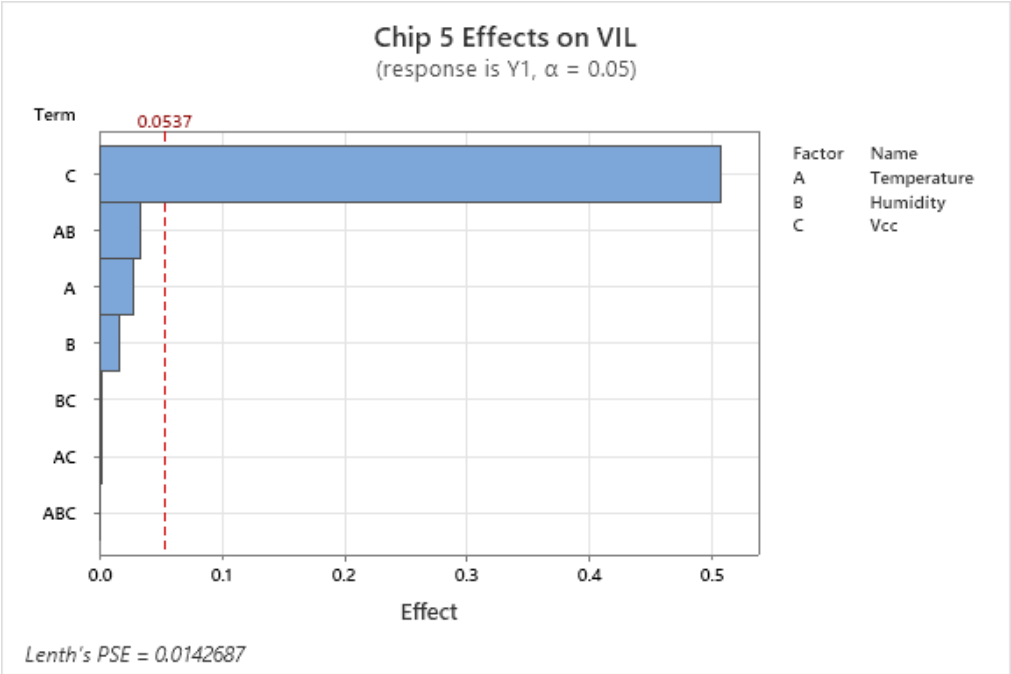

Chip 4 Effects on VOH
(response is Y4, α = 0.05)
Term
C
B
A
AB
BC
AC
ABC
0.100
0.0
0.2
0.4
0.6
0.8
1.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0265716

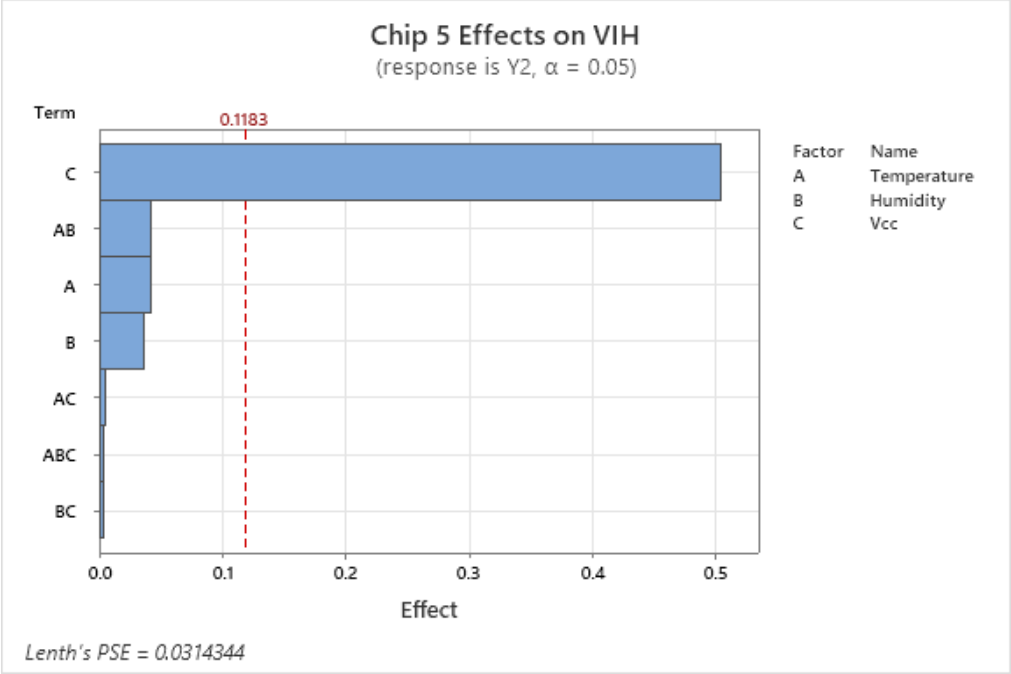


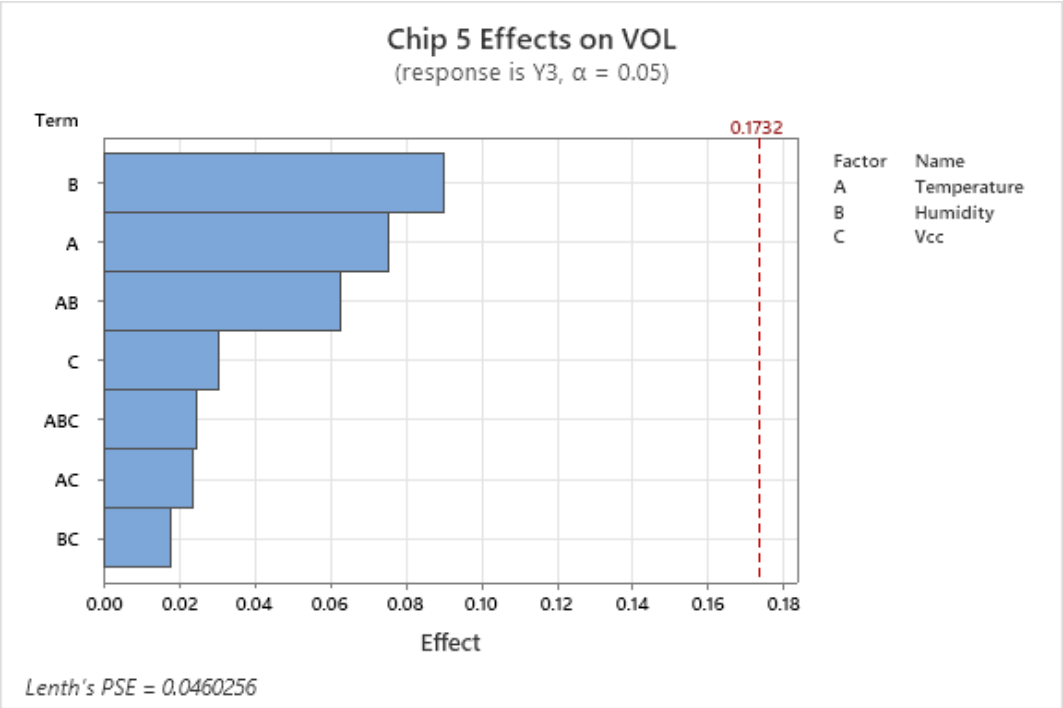
Lenth's PSE = 0.274969

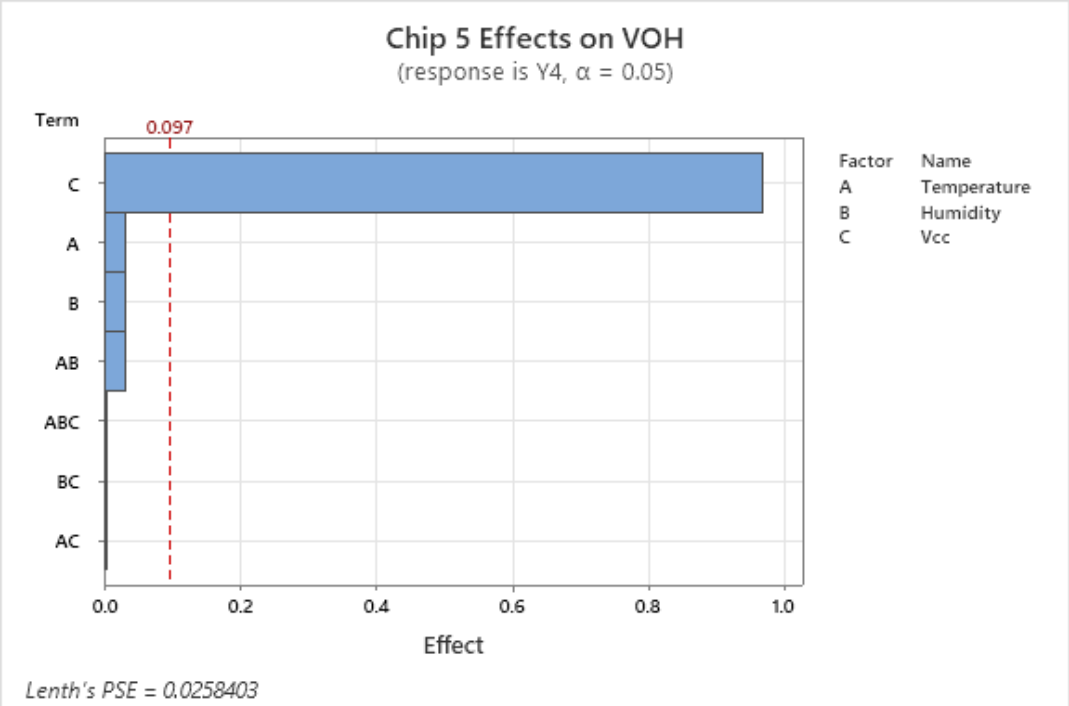


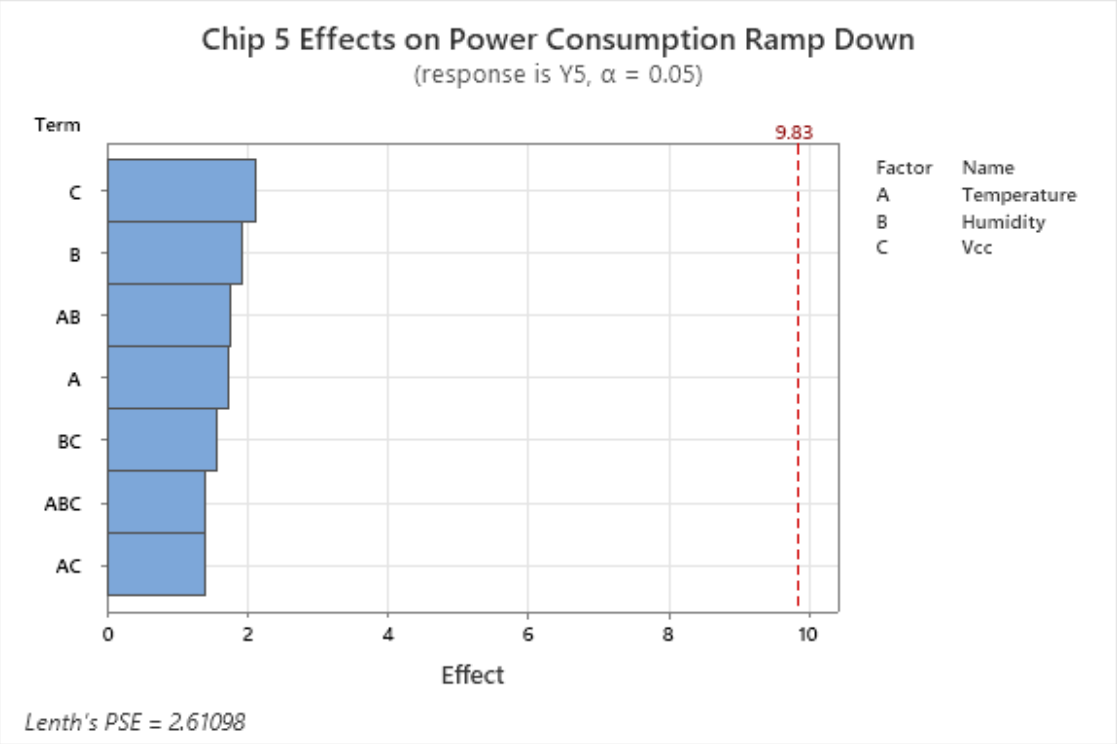
Lenth's PSE = 4.07723

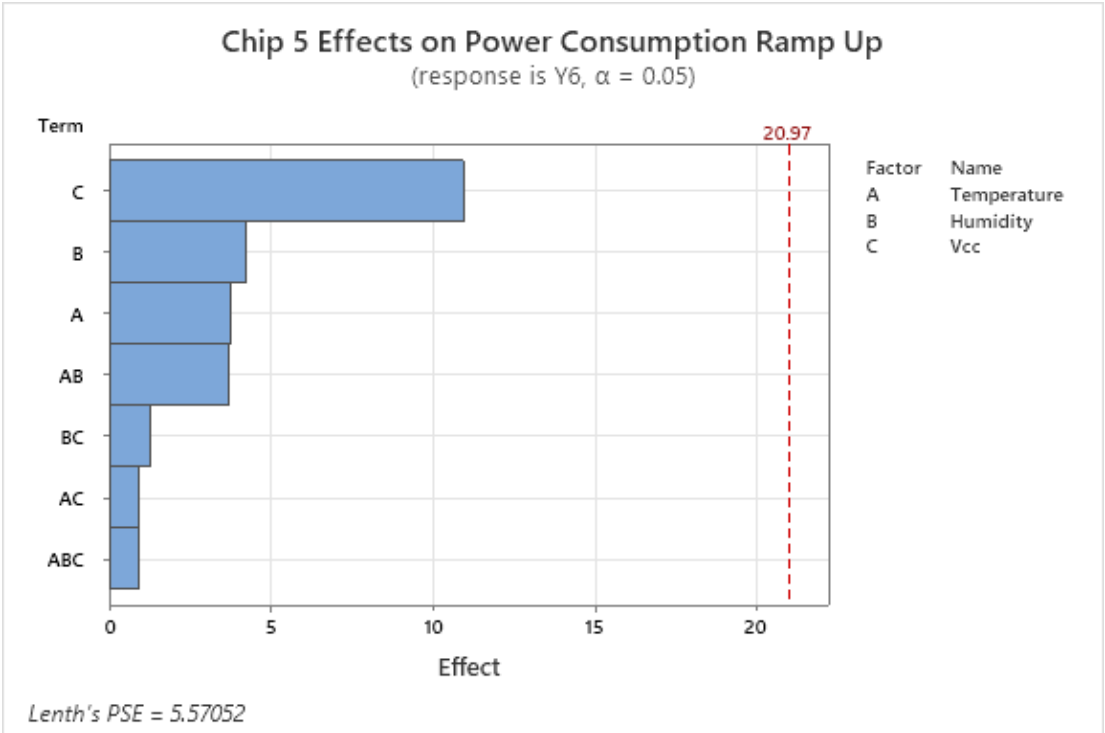

Chip 5 Effects on VIL
(response is Y1, α = 0.05)
Term
0.0537
C
AB
A
B
BC
AC
ABC
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0142687

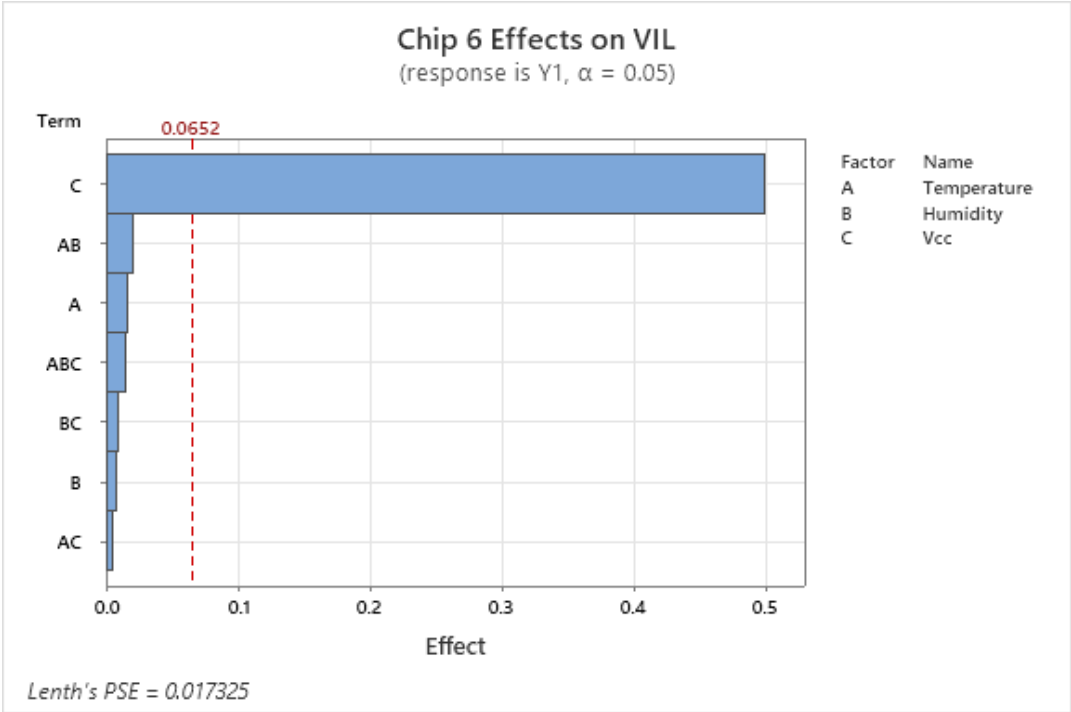

Chip 5 Effects on VIH
(response is Y2, α = 0.05)
Term
0.1183
C
AB
A
B
AC
ABC
BC
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0314344

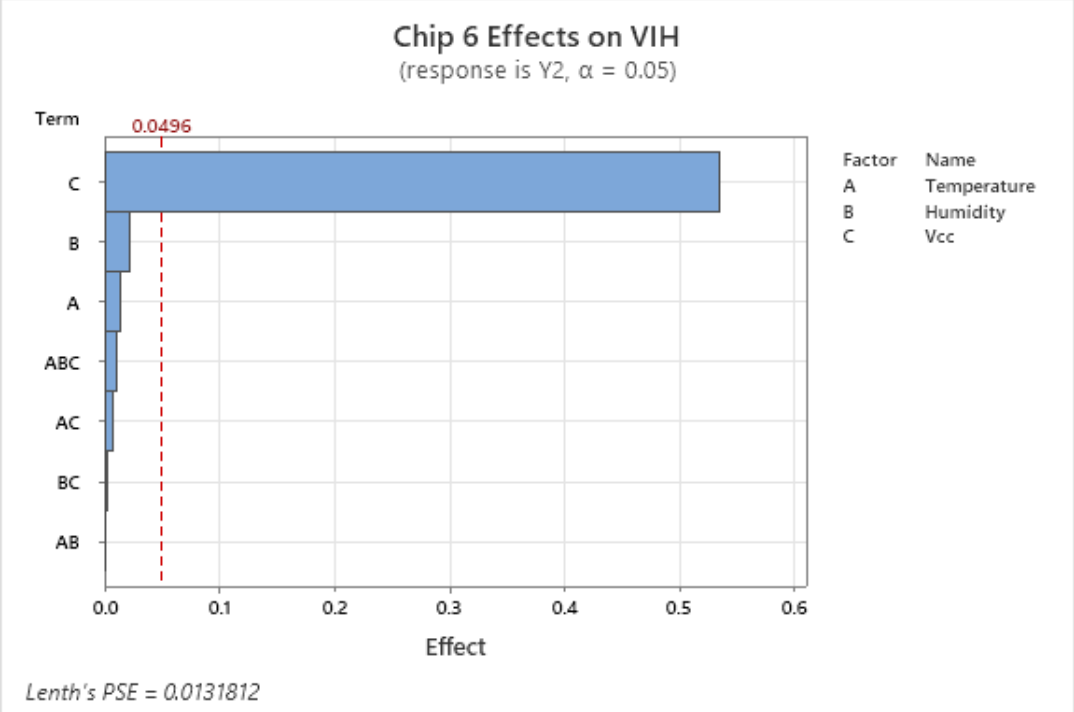

Chip 5 Effects on VOL
(response is Y3, α = 0.05)
Term
B
A
AB
C
ABC
AC
BC
0.1732
0.00
0.02
0.04
0.06
0.08
0.10
0.12
0.14
0.16
0.18
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0460256

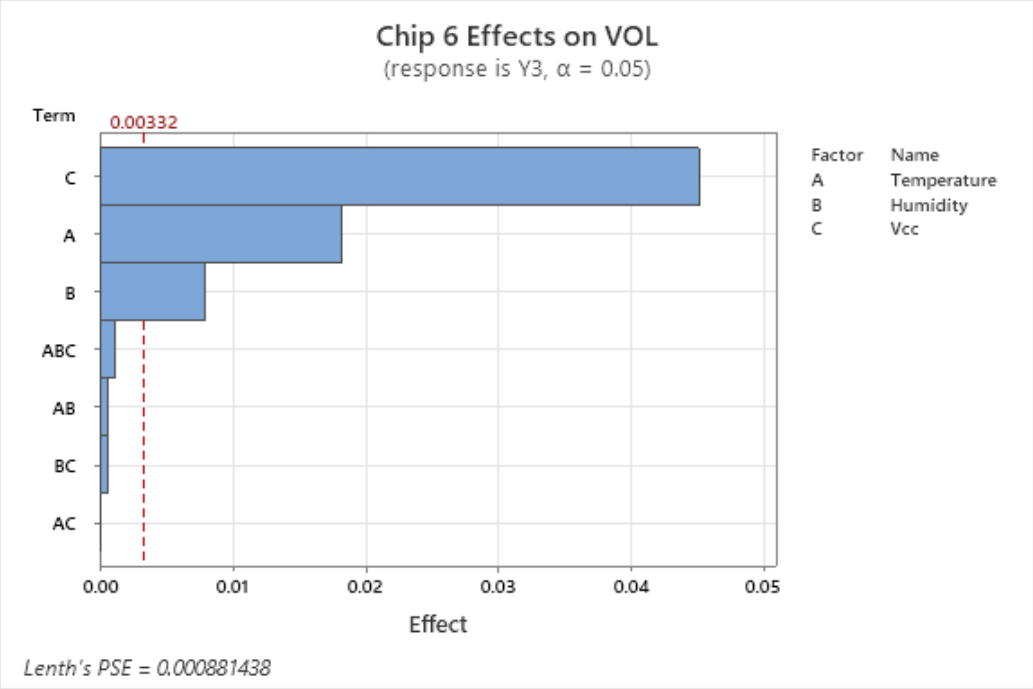

Chip 5 Effects on VOH
(response is Y4, α = 0.05)
Term
C
A
B
AB
ABC
BC
AC
0.097
0.0
0.2
0.4
0.6
0.8
1.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0258403

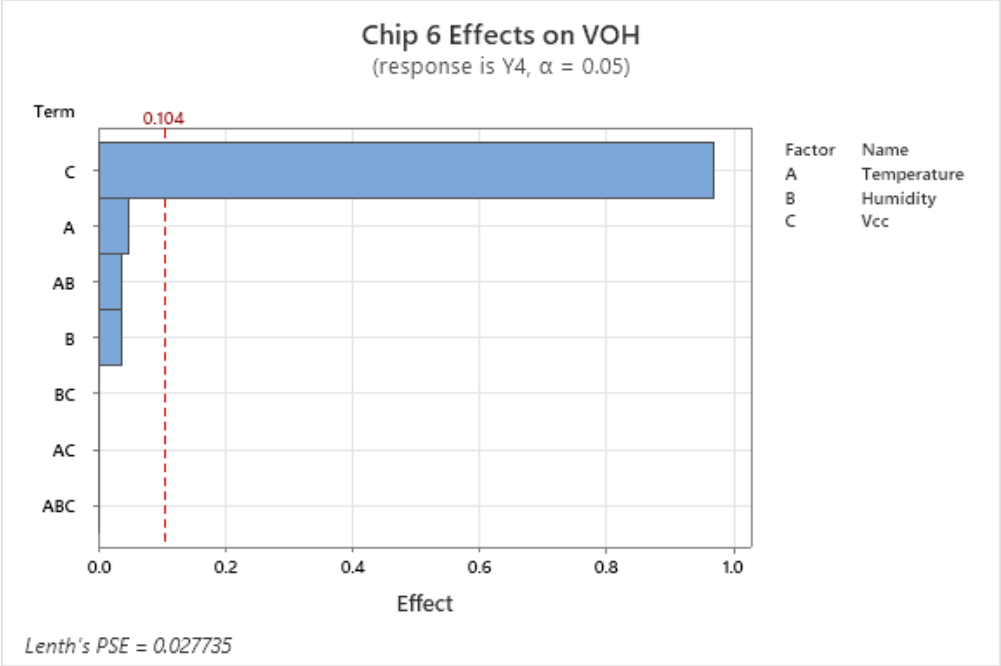

Chip 5 Effects on Power Consumption Ramp Down
(response is Y5, α = 0.05)
Term
C
B
AB
A
BC
ABC
AC
9.83
0
2
4
6
8
10
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 2.61098

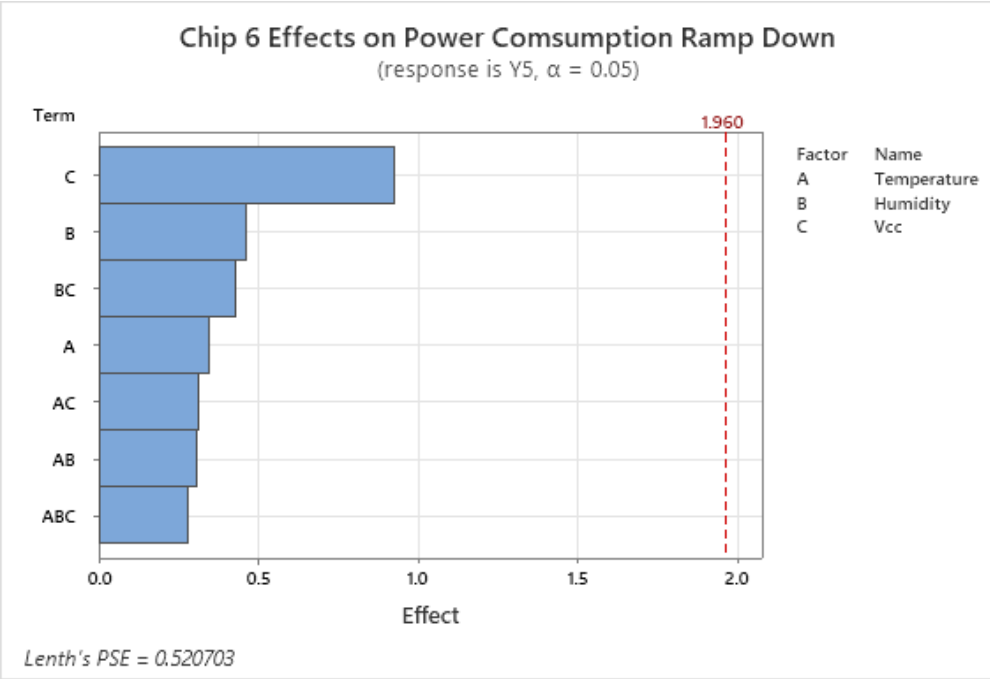

Chip 5 Effects on Power Consumption Ramp Up
(response is Y6, α = 0.05)
Term
C
B
A
AB
BC
AC
ABC
20.97
0
5
10
15
20
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 5.57052

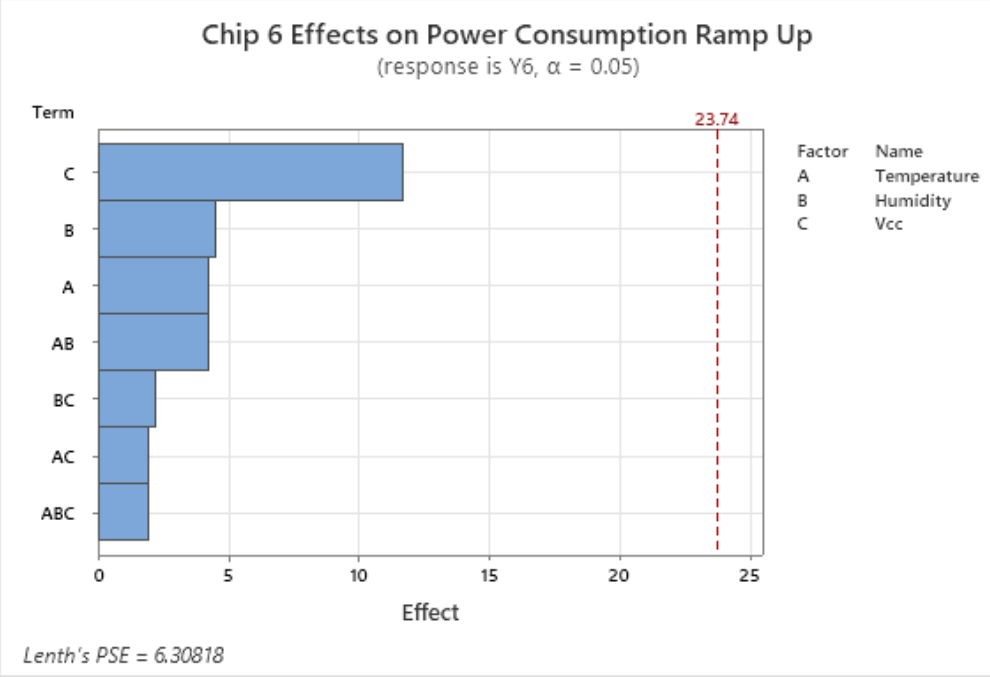

Chip 6 Effects on VIL
(response is Y1, α = 0.05)
Term
0.0652
C
AB
A
ABC
BC
B
AC
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.017325

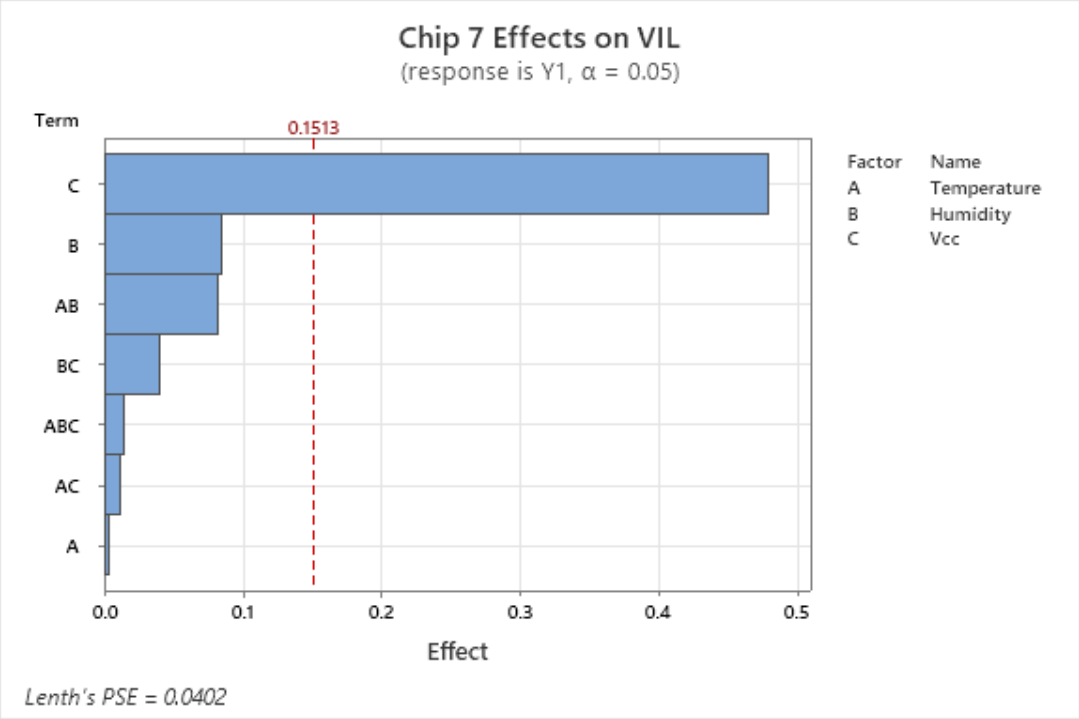

Chip 6 Effects on VIH
(response is Y2, α = 0.05)
Term
0.0496
C
B
A
ABC
AC
BC
AB
0.0
0.1
0.2
0.3
0.4
0.5
0.6
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0131812

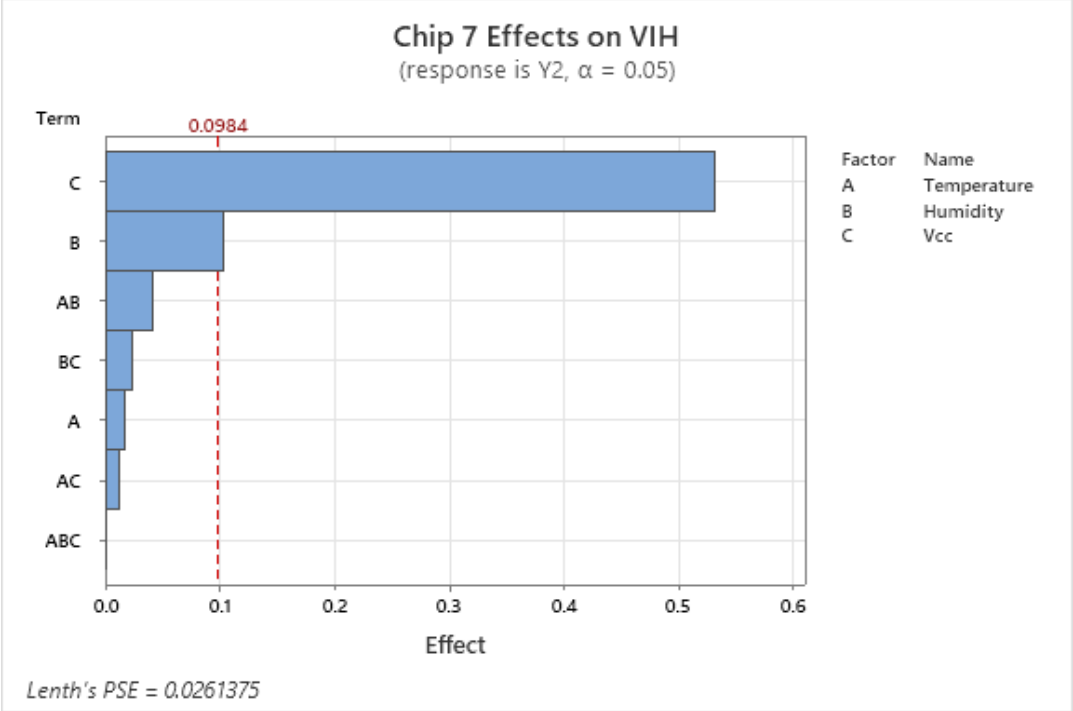

Chip 6 Effects on VOL
(response is Y3, α = 0.05)
Term
0.00332
C
A
B
ABC
AB
BC
AC
0.00
0.01
0.02
0.03
0.04
0.05
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.000881438

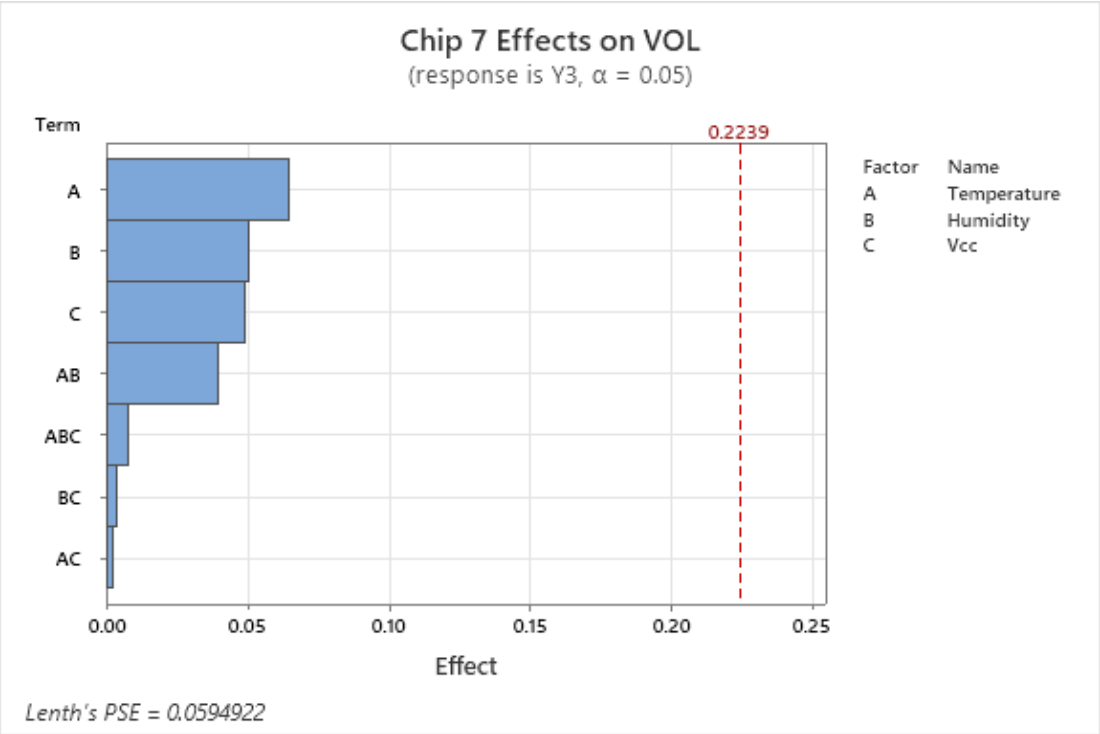

Chip 6 Effects on VOH
(response is Y4, α = 0.05)
Term
0.104
C
A
AB
B
BC
AC
ABC
0.0
0.2
0.4
0.6
0.8
1.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.027735

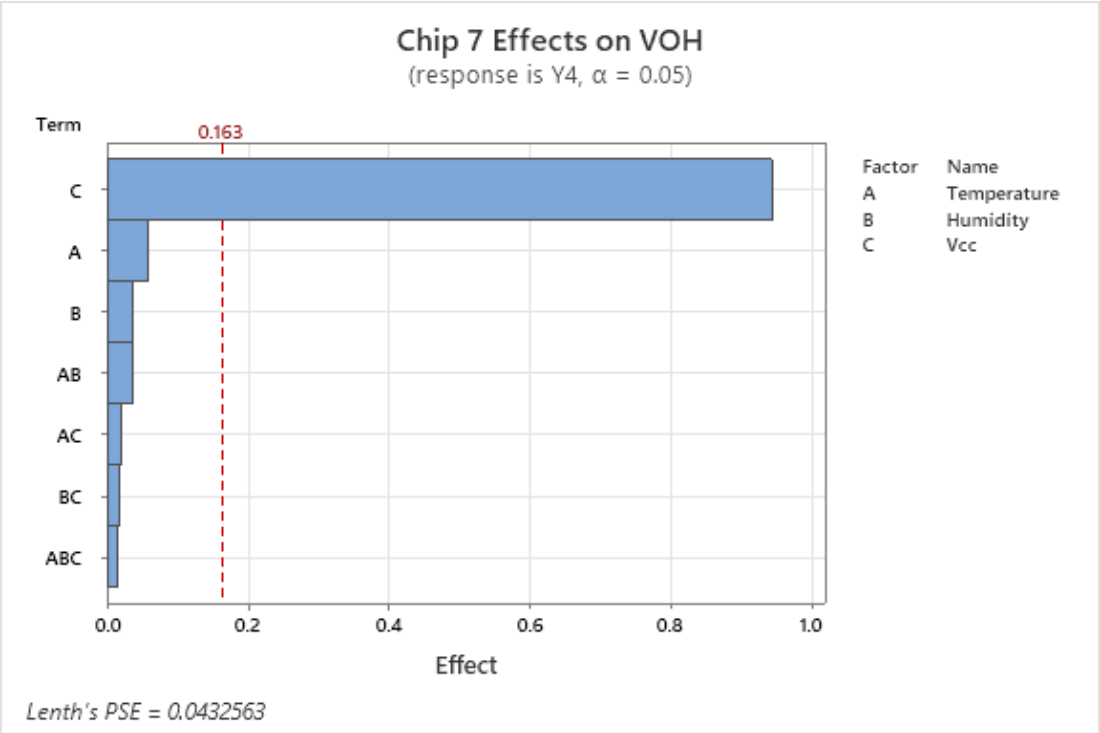

Chip 6 Effects on Power Comsumption Ramp Down
(response is Y5, α = 0.05)
Term
C
B
BC
A
AC
AB
ABC
1.960
0.0
0.5
1.0
1.5
2.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.520703

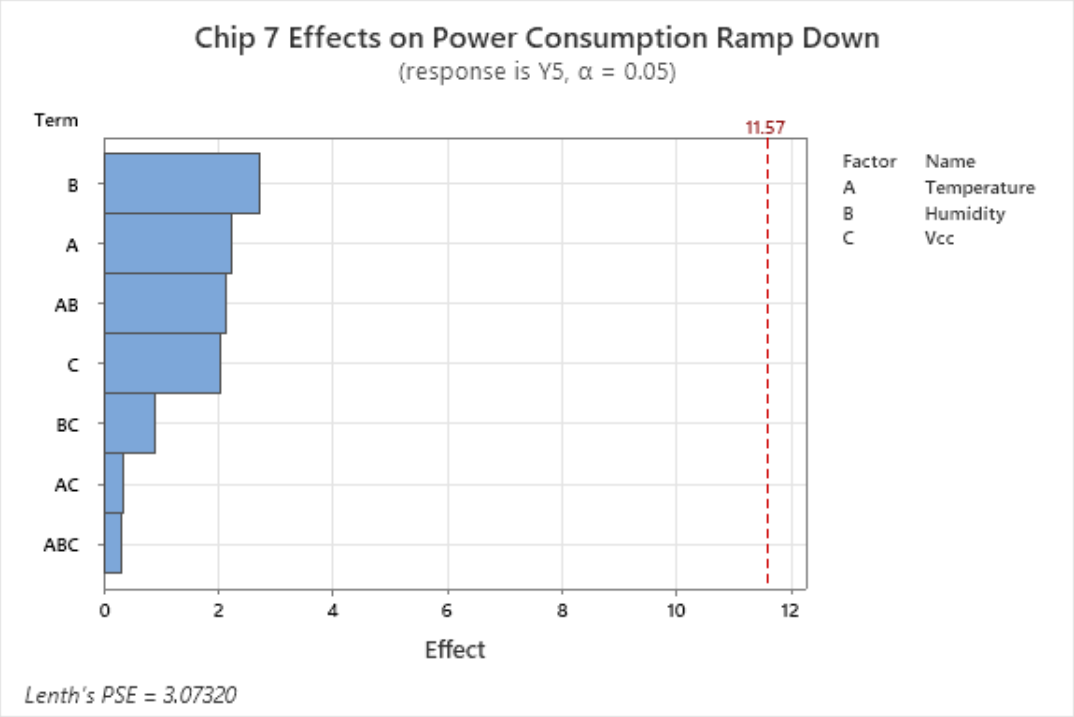

Chip 6 Effects on Power Consumption Ramp Up
(response is Y6, α = 0.05)
Term
C
B
A
AB
BC
AC
ABC
23.74
0
5
10
15
20
25
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 6.30818

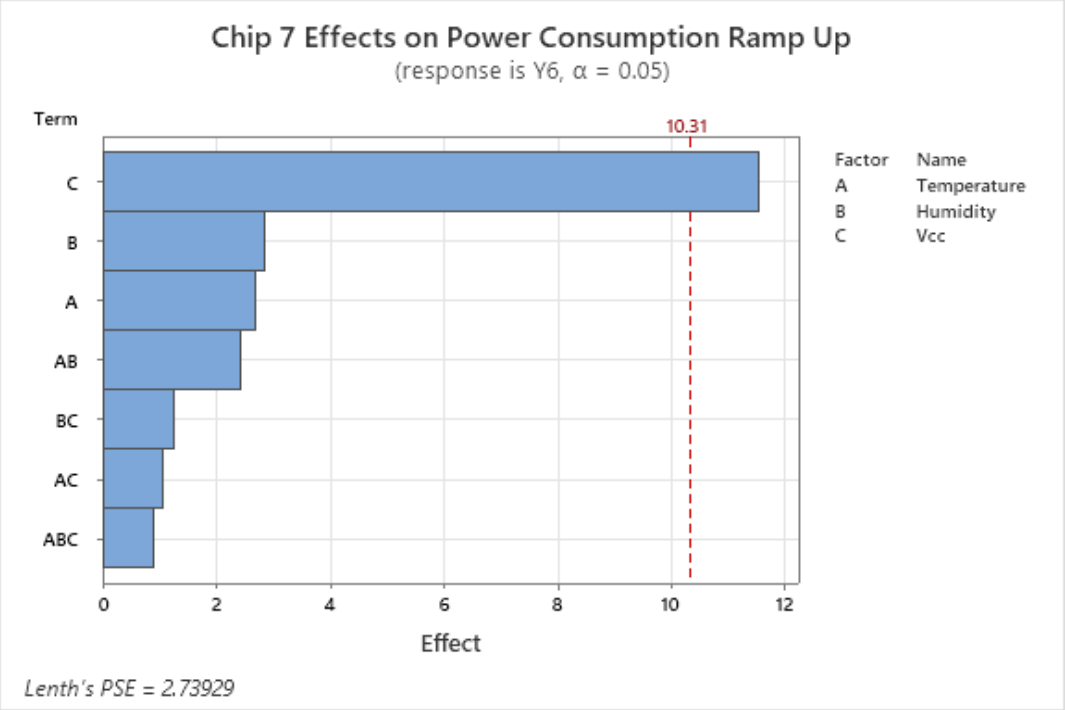

Chip 7 Effects on VIL
(response is Y1, α = 0.05)
Term
0.1513
C
B
AB
BC
ABC
AC
A
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0402

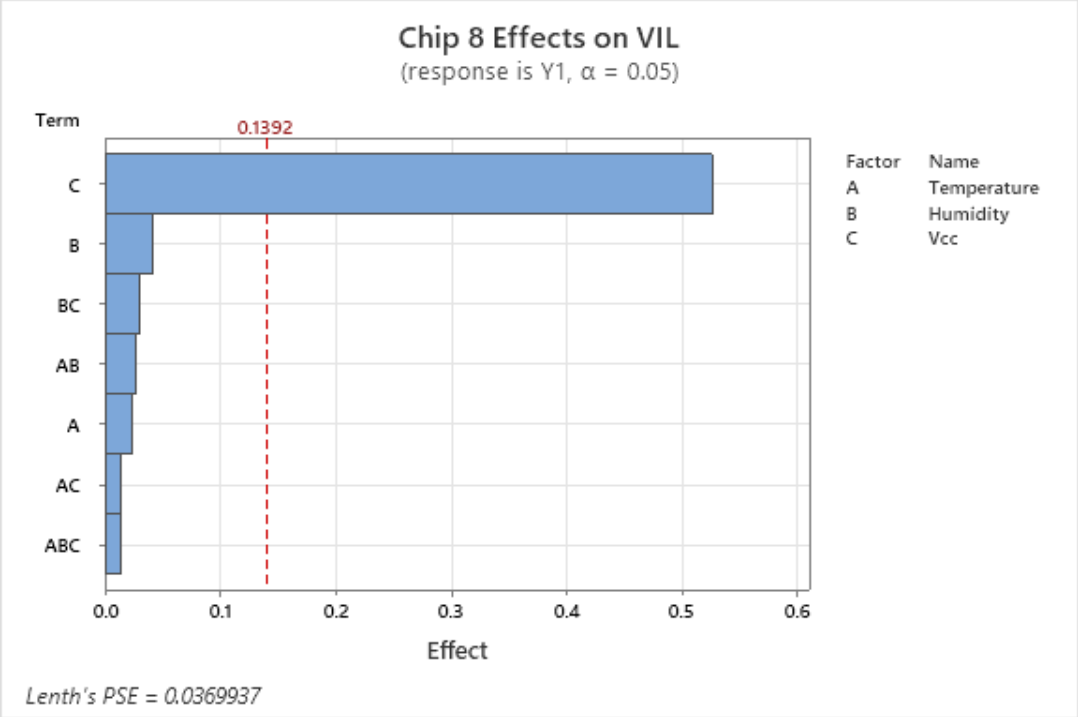

Chip 7 Effects on VIH
(response is Y2, α = 0.05)
Term
0.0984
C
B
AB
BC
A
AC
ABC
0.0
0.1
0.2
0.3
0.4
0.5
0.6
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0261375

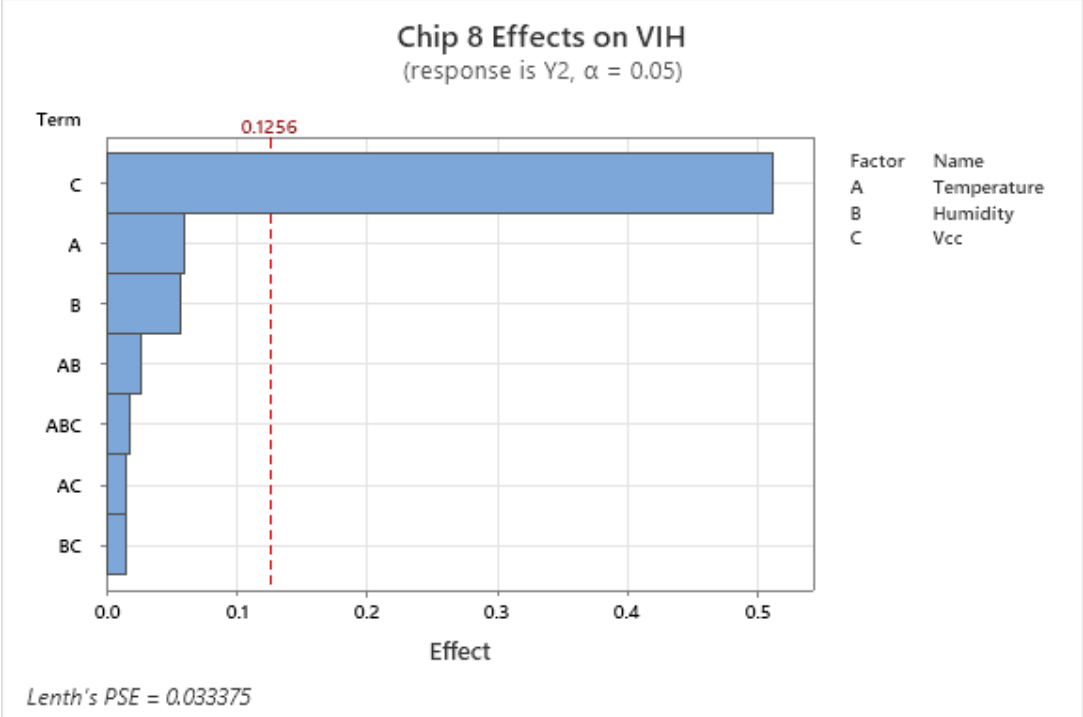

Chip 7 Effects on VOL
(response is Y3, α = 0.05)
Term
A
B
C
AB
ABC
BC
AC
0.2239
0.00
0.05
0.10
0.15
0.20
0.25
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0594922

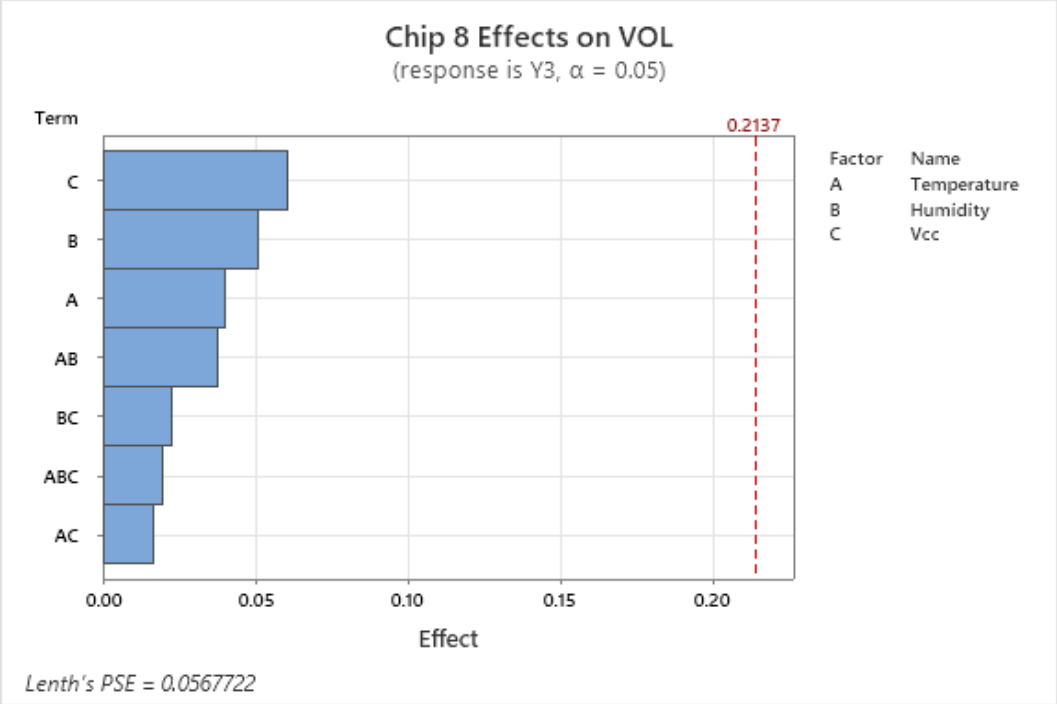

Chip 7 Effects on VOH
(response is Y4, α = 0.05)
Term
C
A
B
AB
AC
BC
ABC
0.163
0.0
0.2
0.4
0.6
0.8
1.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0432563

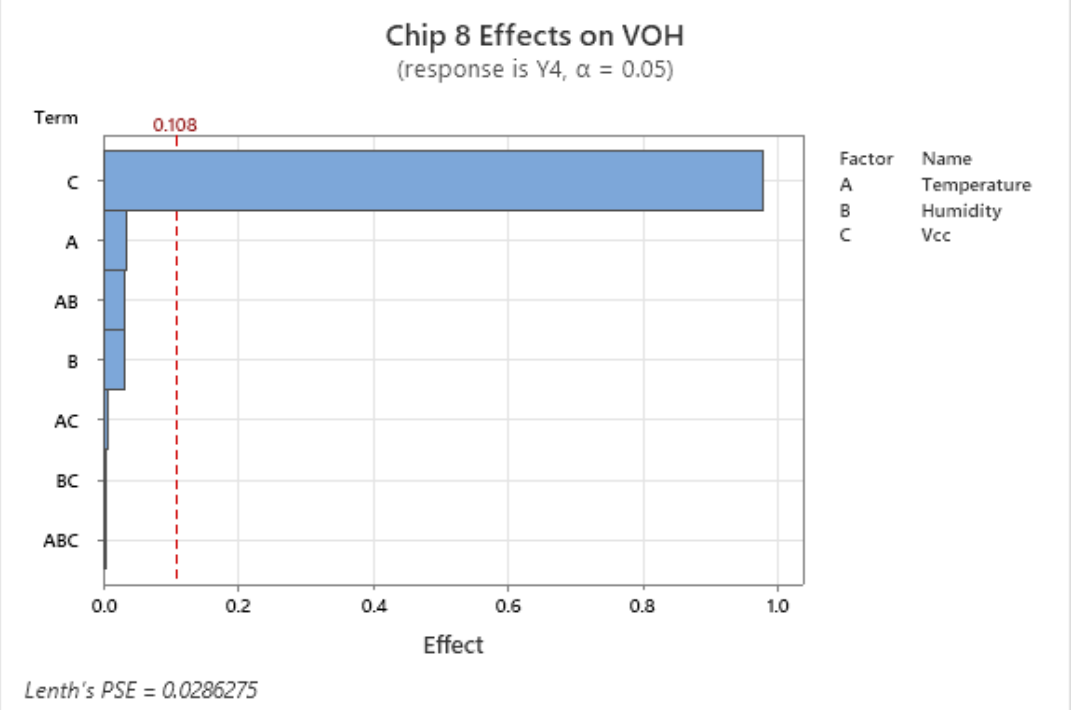

Chip 7 Effects on Power Consumption Ramp Down
(response is Y5, α = 0.05)
Term
B
A
AB
C
BC
AC
ABC
11.57
0
2
4
6
8
10
12
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 3.07320

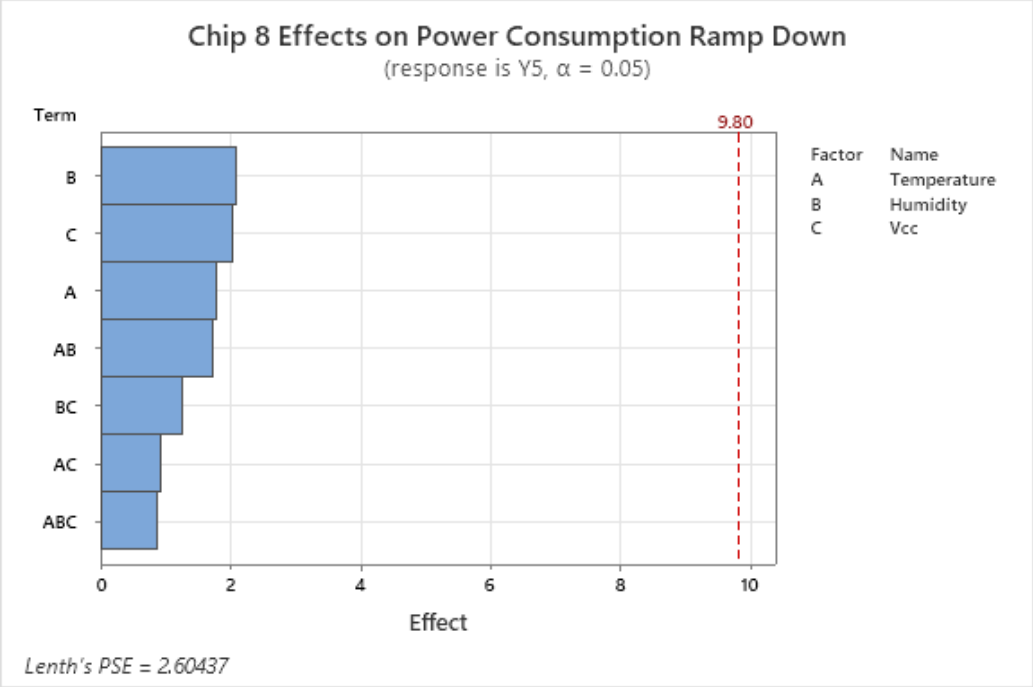

Chip 7 Effects on Power Consumption Ramp Up
(response is Y6, α = 0.05)
Term
C
B
A
AB
BC
AC
ABC
10.31
0
2
4
6
8
10
12
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 2.73929

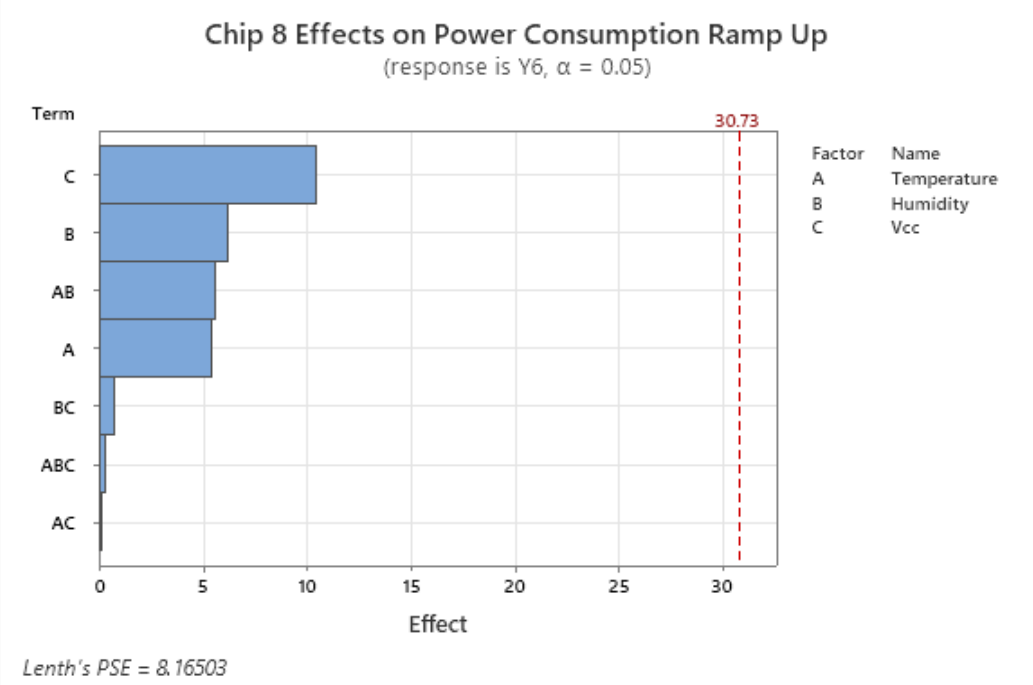

Chip 8 Effects on VIL
(response is Y1, α = 0.05)
Term
0.1392
C
B
BC
AB
A
AC
ABC
0.0
0.1
0.2
0.3
0.4
0.5
0.6
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0369937

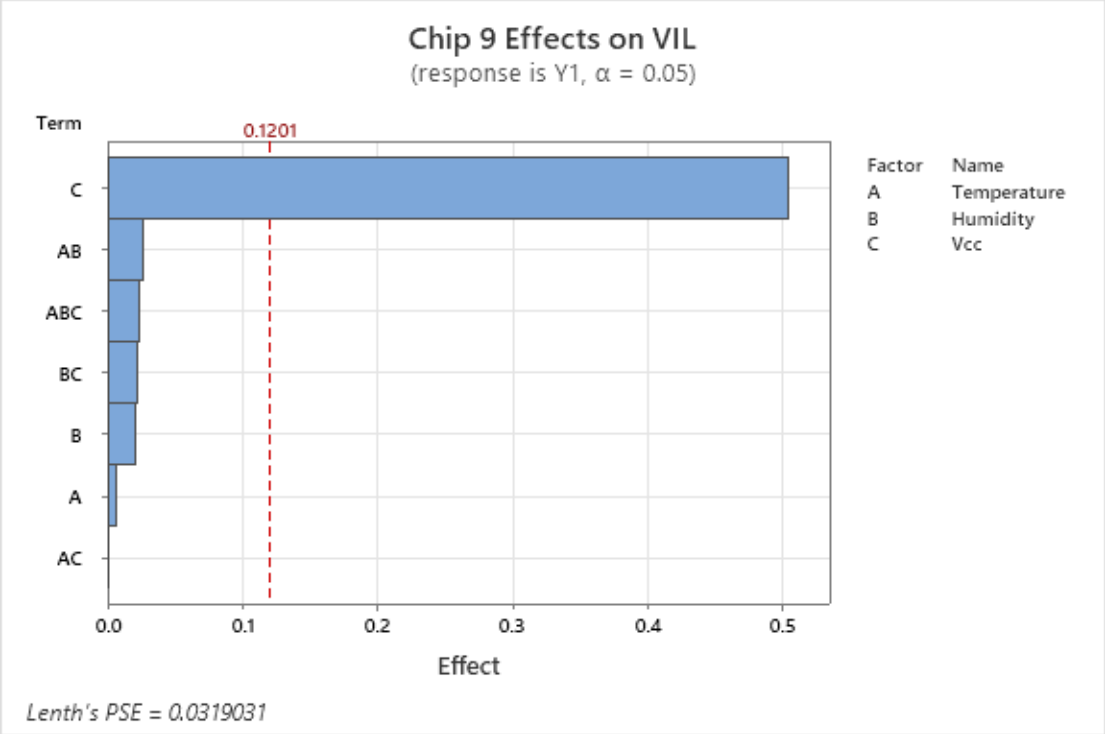

Chip 8 Effects on VIH
(response is Y2, α = 0.05)
Term
0.1256
C
A
B
AB
ABC
AC
BC
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.033375

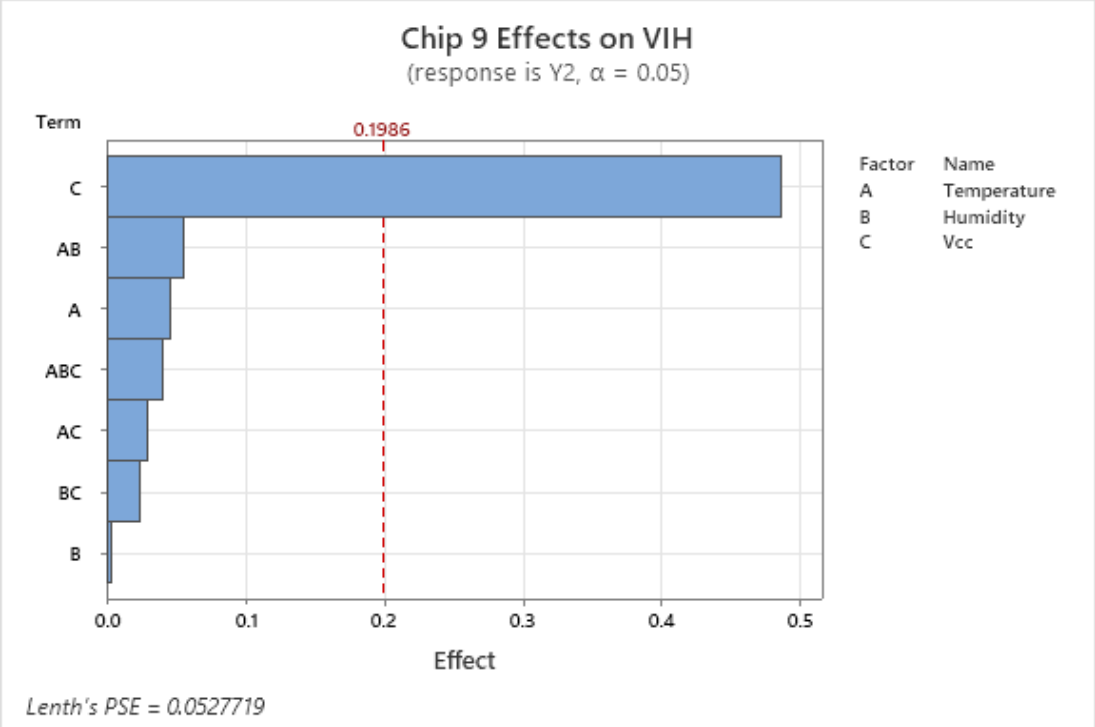

Chip 8 Effects on VOL
(response is Y3, α = 0.05)
Term
C
B
A
AB
BC
ABC
AC
0.2137
0.00
0.05
0.10
0.15
0.20
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0567722

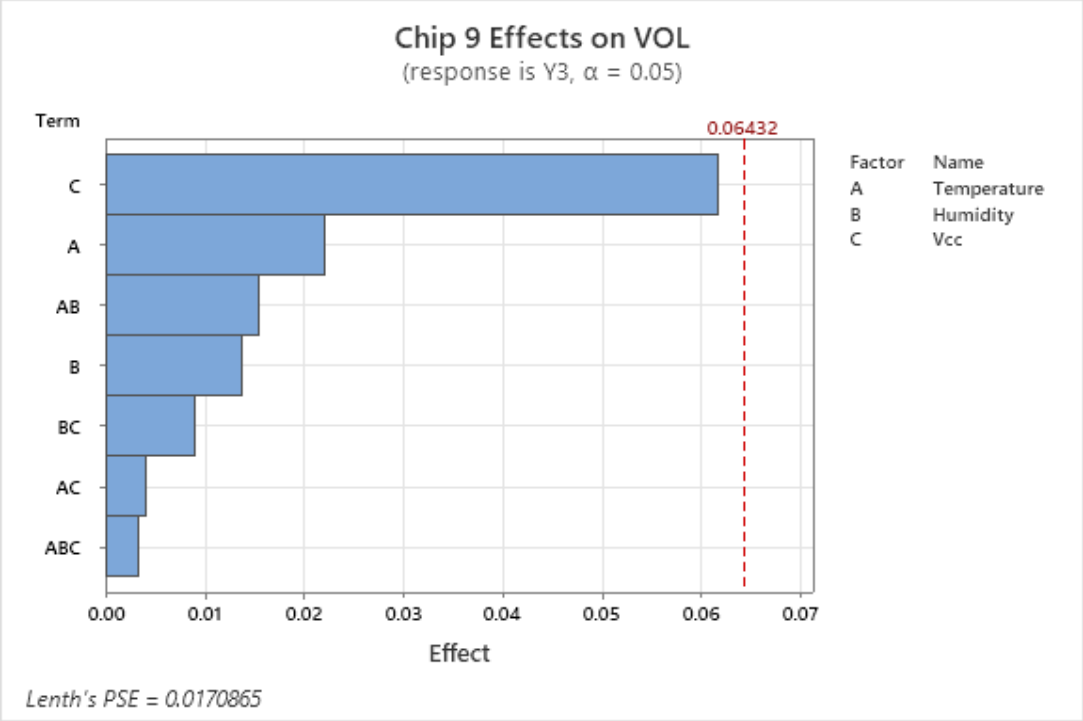

Chip 8 Effects on VOH
(response is Y4, α = 0.05)
Term
C
A
AB
B
AC
BC
ABC
0.108
0.0
0.2
0.4
0.6
0.8
1.0
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0286275

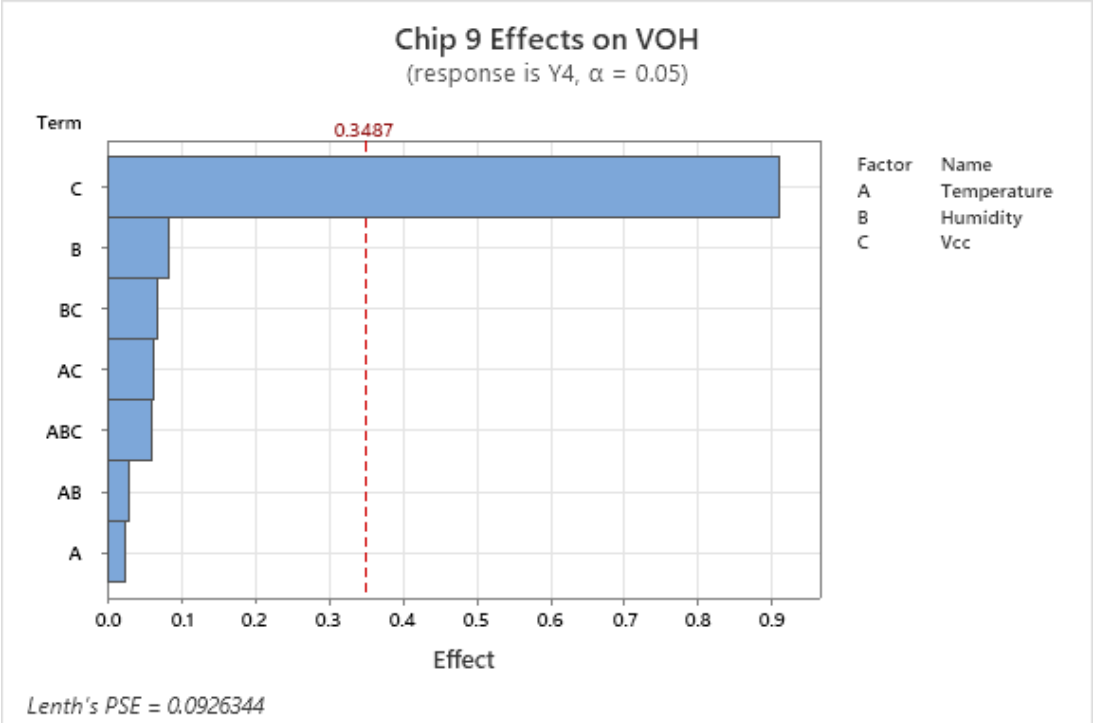

Chip 8 Effects on Power Consumption Ramp Down
(response is Y5, α = 0.05)
Term
B
C
A
AB
BC
AC
ABC
9.80
0
2
4
6
8
10
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 2.60437

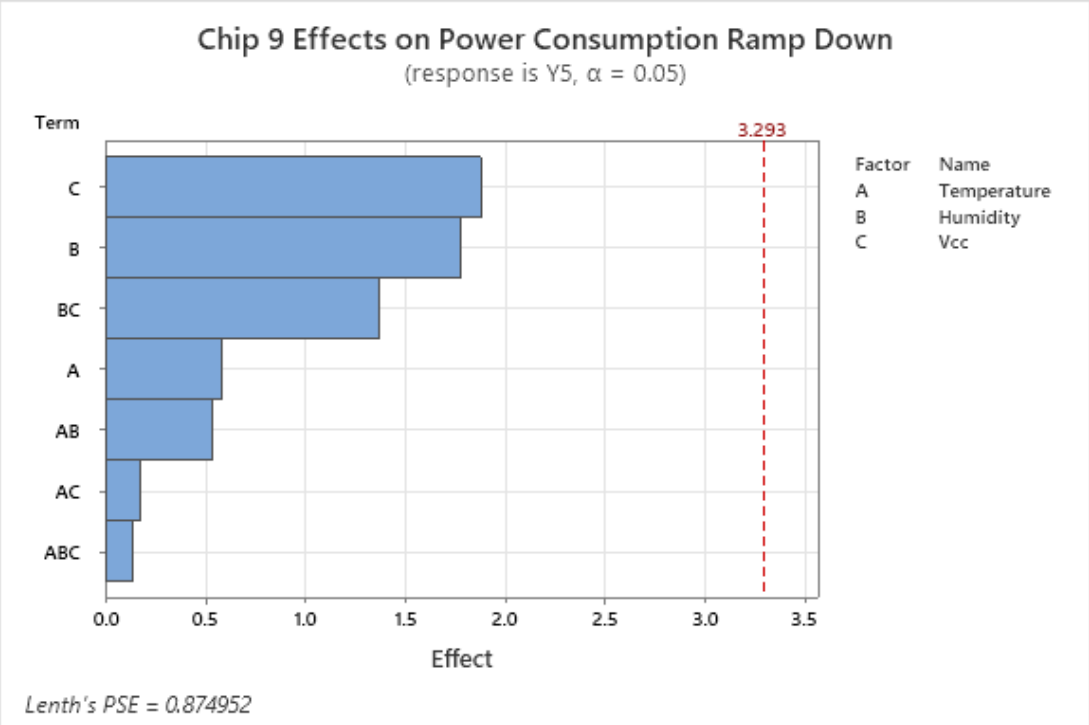

Chip 8 Effects on Power Consumption Ramp Up
(response is Y6, α = 0.05)
Term
C
B
AB
A
BC
ABC
AC
30.73
0
5
10
15
20
25
30
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 8.16503

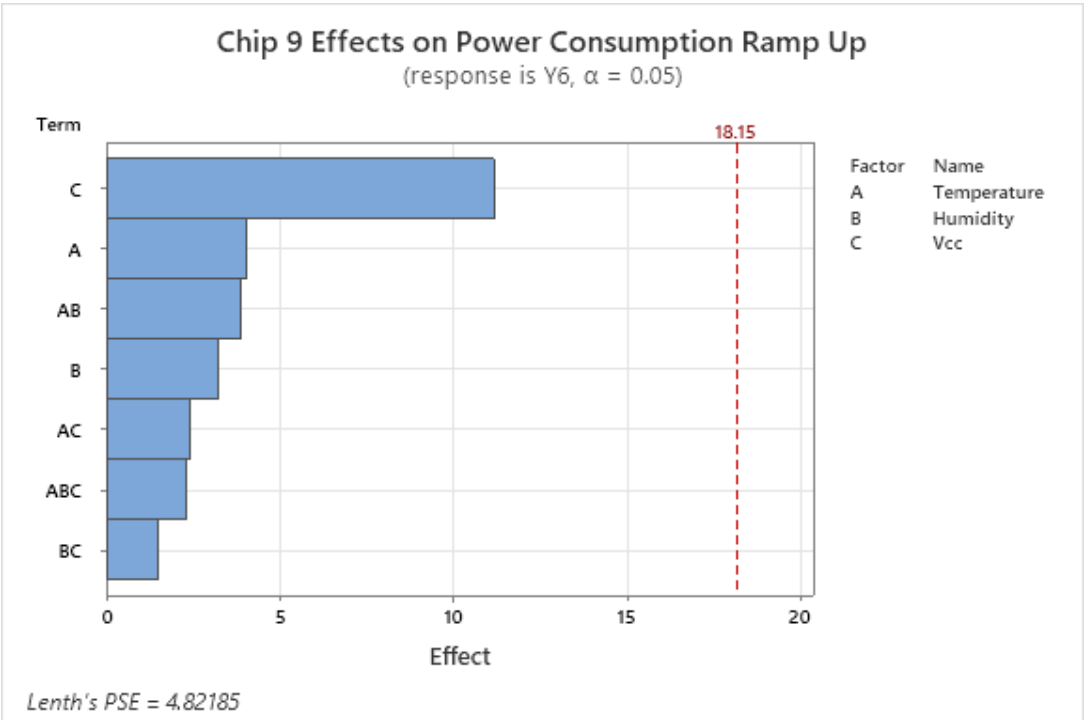

Chip 9 Effects on VIL
(response is Y1, α = 0.05)
Term
0.1201
C
AB
ABC
BC
B
A
AC
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0319031


Chip 9 Effects on VIH
(response is Y2, α = 0.05)
Term
0.1986
C
AB
A
ABC
AC
BC
B
0.0
0.1
0.2
0.3
0.4
0.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0527719


Chip 9 Effects on VOL
(response is Y3, α = 0.05)
Term
C
A
AB
B
BC
AC
ABC
0.06432
0.00
0.01
0.02
0.03
0.04
0.05
0.06
0.07
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0170865


Chip 9 Effects on VOH
(response is Y4, α = 0.05)
Term
C
B
BC
AC
ABC
AB
A
0.3487
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.0926344


Chip 9 Effects on Power Consumption Ramp Down
(response is Y5, α = 0.05)
Term
C
B
BC
A
AB
AC
ABC
3.293
0.0
0.5
1.0
1.5
2.0
2.5
3.0
3.5
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 0.874952


Chip 9 Effects on Power Consumption Ramp Up
(response is Y6, α = 0.05)
Term
C
A
AB
B
AC
ABC
BC
18.15
0
5
10
15
20
Effect
Factor Name
A Temperature
B Humidity
C Vcc
Lenth's PSE = 4.82185

APPENDIX C

RAW RESPONSE DATA TO RAMPING VCC

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.7894	1.277	0.383499	1.7734	1.41145	6.70627
2.05	0.8271	1.295	0.371971	1.8292	2.26139	7.79645
2.1	0.8497	1.317	0.354284	1.8853	1.56816	8.2501
2.15	0.8724	1.34	0.341662	1.9424	1.71502	8.18991
2.2	0.9002	1.357	0.330422	1.9985	1.72826	8.31364
2.25	0.9292	1.389	0.322129	2.0541	1.76045	8.59365
2.3	0.9564	1.415	0.315254	2.109	2.09405	9.06379
2.35	0.9776	1.437	0.307482	2.1636	2.87312	9.49231
2.4	1.0052	1.463	0.300848	2.2175	2.64509	9.87841
2.45	1.0319	1.493	0.296104	2.2711	2.87377	10.305
2.5	1.0576	1.518	0.292042	2.3242	3.12056	10.6418
2.55	1.1701	1.546	0.288145	2.3773	3.43129	11.1627
2.6	1.1113	1.572	0.28403	2.4306	3.62444	11.1208
2.65	1.1309	1.606	0.278564	2.4837	3.16776	11.299
2.7	1.1517	1.632	0.273124	2.5361	2.67138	11.815
2.75	1.1728	1.662	0.268499	2.5894	2.21551	11.0885
2.8	1.1974	1.687	0.266321	2.6415	2.57797	11.4949
2.85	1.2277	1.717	0.26579	2.6933	3.52164	12.6521
2.9	1.2501	1.747	0.26398	2.7455	3.92799	13.2003
2.95	1.2757	1.729	0.262587	2.7965	4.36474	15.6798
3	1.3002	1.805	0.260377	2.8483	4.39282	16.477

Vcc Test 1 Table Chip 0

VCC	VIL	VIH	VOL	VOH	OWER CONSUMPTION Ramp Down (mW	OWER CONSUMPTION Ramp Up (mW
2	0.8305	1.294	0.485142	1.7788	0.596619	6.66017
2.05	0.8645	1.32	0.463232	1.8359	0.750495	6.80216
2.1	0.8917	1.347	0.457042	1.8916	0.678789	7.08522
2.15	0.9169	1.369	0.439127	1.9479	0.686036	7.22236
2.2	0.9475	1.388	0.425922	2.0034	0.733977	7.35899
2.25	0.9687	1.414	0.412155	2.0587	0.776131	7.54996
2.3	0.997	1.441	0.402579	2.1135	0.880865	7.81291
2.35	1.0222	1.467	0.393435	2.1681	0.869856	7.93578
2.4	1.0505	1.49	0.383571	2.2223	0.936382	8.1585
2.45	1.0702	1.521	0.374461	2.2761	0.972909	8.35168
2.5	1.1012	1.545	0.369614	2.3292	1.04169	8.5684
2.55	1.1279	1.575	0.374911	2.3826	1.94446	8.78083
2.6	1.156	1.606	0.383984	2.4339	4.81478	11.2164
2.65	1.1833	1.645	0.382347	2.4852	4.73806	12.9992
2.7	1.1988	1.666	0.359829	2.5394	2.00012	11.1277
2.75	1.2219	1.506	0.353529	2.593	1.41418	10.7802
2.8	1.2429	1.727	0.351162	2.645	1.61219	10.2879
2.85	1.2644	1.753	0.346883	2.6975	1.58197	10.2822
2.9	1.2878	1.772	0.342798	2.75	1.58872	10.3805
2.95	1.3157	1.816	0.339431	2.802	1.68703	10.658
3	1.3349	1.839	0.337638	2.8539	1.8318	10.9111

Vcc Test 1 Table Chip 1

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.821	1.314	0.492649	1.7664	0.89404	6.72982
2.05	0.8474	1.338	0.468375	1.825	0.858399	7.20666
2.1	0.8737	1.358	0.450315	1.8823	0.925771	7.60525
2.15	0.9023	1.382	0.43365	1.9392	0.860255	8.05577
2.2	0.9304	1.403	0.421024	1.9953	0.854528	8.10196
2.25	0.9561	1.426	0.411321	2.0513	0.960329	8.03065
2.3	0.9847	1.449	0.399904	2.1067	1.05588	8.33529
2.35	1.0085	1.476	0.394204	2.1613	1.42048	8.81216
2.4	1.0375	1.502	0.386127	2.2158	1.26357	9.21838
2.45	1.0608	1.527	0.380645	2.2701	1.35609	2.2701
2.5	1.0861	1.556	0.376415	2.3235	1.38936	9.42354
2.55	1.1121	1.582	0.372968	2.3773	1.48294	9.27008
2.6	1.1359	1.54	0.36777	2.4306	1.49672	9.62714
2.65	1.1593	1.636	0.358507	2.4839	1.6505	9.93803
2.7	1.1822	1.664	0.354995	2.5367	2.01461	10.3565
2.75	1.2047	1.694	0.348539	2.5897	1.61374	10.5669
2.8	1.2412	1.719	0.36796	2.6416	2.97176	11.2391
2.85	1.2625	1.755	0.363377	2.693	3.14529	11.0834
2.9	1.2817	1.783	0.352485	2.7448	3.79469	12.1896
2.95	1.3023	1.812	0.348011	2.7981	4.97018	12.4533
3	1.3308	1.837	0.341904	2.8503	3.89689	12.7064

Vcc Test 1 Table Chip 2

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.7901	1.264	0.455897	1.7784	0.625387	6.65777
2.05	0.8175	1.286	0.421262	1.8358	0.673671	6.84194
2.1	0.8433	1.309	0.403189	1.8924	0.71069	7.0401
2.15	0.8729	1.335	0.390639	1.9488	0.760779	7.23887
2.2	0.8994	1.359	0.379821	2.0037	0.817771	7.45201
2.25	0.926	1.383	0.369894	2.059	0.878939	7.66206
2.3	0.9533	1.409	0.361112	2.1136	0.951268	7.90683
2.35	0.9819	1.436	0.353497	2.1679	0.952409	8.1171
2.4	1.0061	1.463	0.347622	2.2218	1.03856	8.30883
2.45	1.0328	1.49	0.341265	2.2756	1.10182	8.54468
2.5	1.0574	1.517	0.337135	2.3287	1.1603	8.78738
2.55	1.0817	1.544	0.33194	2.382	1.2641	9.0321
2.6	1.1065	1.572	0.340866	2.4351	1.31633	9.24111
2.65	1.1328	1.599	0.336767	2.488	1.43377	9.49232
2.7	1.1574	1.629	0.333561	2.5405	1.47894	9.73879
2.75	1.1818	1.656	0.333027	2.5931	1.75656	9.95916
2.8	1.2101	1.689	0.33249	2.6442	2.48192	10.9827
2.85	1.2303	1.713	0.329346	2.6959	2.42313	11.6172
2.9	1.254	1.748	0.318151	2.7487	2.19186	11.1959
2.95	1.2733	1.78	0.313171	2.801	1.90848	11.6666
3	1.2982	1.809	0.309993	2.8534	2.0678	10.7869

Vcc Test 1 Table Chip 3

C	Y1	Y2	Y3	Y4	Y5	Y6
VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.8383	1.158	0.372013	1.7604	1.01098	6.97081
2.05	0.8686	1.292	0.357123	1.8177	0.944768	7.25564
2.1	0.8878	1.305	0.339564	1.8743	0.862871	7.28522
2.15	0.9199	1.331	0.328961	1.9332	0.8782	7.43378
2.2	0.955	1.358	0.319603	1.9884	0.803462	7.49082
2.25	0.9828	1.378	0.31148	2.0436	0.864762	7.62327
2.3	1.0008	1.4	0.304207	2.0983	0.835649	7.84221
2.35	1.0208	1.421	0.297899	2.1527	0.879535	7.96654
2.4	1.0614	1.438	0.292085	2.2069	0.893251	8.14993
2.45	1.0791	1.482	0.28693	2.2607	1.0883	8.36338
2.5	1.1039	1.506	0.282415	2.3137	1.1039	8.55431
2.55	1.1357	1.538	0.278082	2.3674	1.20933	8.84643
2.6	1.1557	1.558	0.274239	2.4204	1.60985	9.18016
2.65	1.176	1.573	0.272733	2.4732	2.1834	9.55955
2.7	1.2166	1.617	0.273852	2.5248	6.37365	11.5944
2.75	1.2145	1.653	0.266631	2.5767	3.5006	13.7461
2.8	1.2369	1.674	0.260845	2.6303	1.41079	10.1891
2.85	1.2596	1.703	0.258271	2.6826	1.50519	9.98486
2.9	1.2825	1.731	0.255815	2.7348	1.52057	10.5831
2.95	1.5093	1.769	0.253738	2.7869	1.62755	10.5078
3	1.3364	1.792	0.25136	2.839	1.58788	10.7427

Vcc Test 1 Table Chip 4

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	x	1.256	x	1.7606	x	6.72436
2.05	x	1.318	x	1.8209	x	6.89192
2.1	x	1.33	x	1.8793	x	7.07943
2.15	0.9951	1.355	0.478191	1.9377	0.848877	7.33731
2.2	1.0248	1.363	0.462177	1.9943	0.912891	7.58125
2.25	1.0559	1.398	0.450078	2.0506	1.01389	7.78694
2.3	1.0815	1.409	0.438793	2.1064	1.07307	8.02094
2.35	1.1075	1.444	0.429699	2.1616	1.02786	8.15037
2.4	1.1288	1.464	0.42157	2.2163	0.998129	8.37883
2.45	1.1643	1.477	0.413513	2.2706	1.06639	8.46761
2.5	1.1965	1.496	0.407573	2.3244	1.20836	8.72224
2.55	1.2244	1.526	0.401539	2.3781	1.13152	9.02783
2.6	1.2534	1.549	0.408637	2.4316	1.63511	9.10446
2.65	1.3063	1.564	0.426487	2.4823	4.14694	11.1738
2.7	1.3023	1.542	0.403103	2.5341	1.96786	13.3999
2.75	1.3145	1.631	0.396379	2.5896	1.46821	10.1381
2.8	1.3495	1.652	0.389761	2.6424	1.71955	10.3505
2.85	1.3791	1.682	0.389077	2.695	2.3012	10.7482
2.9	1.4014	1.712	0.382762	2.7473	2.15634	11.5074
2.95	1.4227	1.744	0.381853	2.7997	3.00006	11.8819
3	1.4716	1.763	0.389061	2.8518	4.12088	12.1485

Vcc Test 1 Table Chip 5

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.7857	1.267	0.438597	1.7541	0.800913	6.85735
2.05	0.8219	1.294	0.417702	1.8121	0.713615	6.98777
2.1	0.8427	1.315	0.401933	1.8699	0.92085	7.22262
2.15	0.8826	1.343	0.388746	1.9265	0.768475	7.3684
2.2	0.8968	1.37	0.377807	1.982	0.89251	7.57744
2.25	0.939	1.388	0.368313	2.0375	1.03137	7.79727
2.3	1.0452	1.406	0.359532	2.0923	0.977767	8.46547
2.35	0.9715	1.444	0.352801	2.1467	0.943191	8.38386
2.4	1.0122	1.462	0.34641	2.201	1.08516	8.72378
2.45	1.0422	1.498	0.341034	2.2548	1.27681	8.77488
2.5	1.0534	1.522	0.335858	2.3079	1.35359	9.09189
2.55	1.0728	1.545	0.331719	2.3615	1.36363	9.30616
2.6	1.1025	1.576	0.329652	2.414	1.81995	10.2028
2.65	1.1348	1.605	0.324285	2.4669	2.17359	10.4123
2.7	1.1603	1.629	0.319821	2.52	2.13263	10.504
2.75	1.1812	1.547	0.3161	2.5728	1.87132	10.5108
2.8	1.2039	1.691	0.312544	2.6247	1.73029	11.1878
2.85	1.2244	1.7	0.309681	2.6771	2.0239	11.907
2.9	1.2419	1.746	0.307308	2.7294	2.07697	11.9865
2.95	1.2837	1.783	0.305079	2.7818	1.97892	11.8723
3	1.2909	1.81	0.30728	2.8334	3.32942	12.761

Vcc Test 1 Table Chip 6

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.8495	1.253	0.462675	1.7	0.662645	6.68615
2.05	0.8782	1.249	0.447139	1.7577	0.687766	6.86609
2.1	0.9051	1.294	0.433894	1.8151	0.68533	7.03162
2.15	0.9357	1.315	0.422693	1.8713	0.724874	7.17883
2.2	0.9647	1.341	0.413083	1.9265	0.767905	7.35868
2.25	0.9926	1.36	0.40496	1.9817	0.825635	7.57851
2.3	1.0137	1.384	0.397722	2.0363	0.881631	7.78256
2.35	1.0468	1.409	0.39269	2.0906	0.888338	8.0149
2.4	1.0692	1.438	0.390531	2.1436	1.43397	8.36912
2.45	1.0902	1.465	0.380989	2.1781	1.11943	8.73251
2.5	1.1194	1.488	0.375714	2.2504	1.2756	8.86112
2.55	1.1395	1.516	0.371257	2.3038	1.34804	8.98703
2.6	1.1655	1.543	0.367013	2.3566	1.47069	9.25572
2.65	1.19	1.566	0.363569	2.4091	1.60351	9.54281
2.7	1.2133	1.599	0.360197	2.4619	1.75048	9.82869
2.75	1.2399	1.629	0.356853	2.514	1.82637	10.1409
2.8	1.2612	1.657	0.353871	2.5658	1.99568	10.3974
2.85	1.2845	1.684	0.351008	2.6179	2.17734	10.6234
2.9	1.3087	1.717	0.349452	2.6701	1.71064	10.8838
2.95	1.3332	1.746	0.351437	2.7219	2.81285	11.1318
3	1.3539	1.778	0.351574	2.7737	4.42667	11.3936

Vcc Test 1 Table Chip 7

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.7967	1.284	0.381762	1.7754	0.69105	6.84435
2.05	0.8167	1.304	0.361047	1.8338	0.627224	6.82031
2.1	0.8438	1.323	0.346621	1.8914	0.645983	6.96009
2.15	0.8742	1.349	0.334551	1.9477	0.663225	7.13056
2.2	0.9615	1.307	0.324806	2.0031	0.688125	7.3102
2.25	0.9291	1.392	0.315792	2.0583	0.702473	7.48026
2.3	0.9626	1.418	0.308368	2.1134	0.719355	7.64495
2.35	0.9826	1.441	0.301735	2.1678	0.744675	7.82332
2.4	1.0062	1.464	0.294771	2.2221	0.758316	7.99141
2.45	1.0337	1.48	0.288903	2.2757	0.783901	8.17611
2.5	1.0578	1.516	0.283704	2.3291	0.814892	8.38331
2.55	1.0838	1.543	0.278942	2.3827	0.833636	8.52717
2.6	1.1043	1.576	0.274718	2.4358	0.859961	8.722
2.65	1.1352	1.601	0.274677	2.4886	1.36097	8.88142
2.7	1.1483	1.633	0.270328	2.5408	1.06786	9.32261
2.75	1.1786	1.661	0.265785	2.5936	0.948984	9.45521
2.8	1.2031	1.692	0.469934	2.6458	0.976109	9.44082
2.85	1.2156	1.544	0.259036	2.6982	1.00492	9.67332
2.9	1.2418	1.749	0.256615	2.7505	1.07162	9.79581
2.95	1.2619	1.781	0.253656	2.8027	1.11406	10.024
3	1.2936	1.807	0.254243	2.8547	1.77762	10.1808

Vcc Test 1 Table Chip 8

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.8359	1.268	0.491536	1.735	0.665824	6.86928
2.05	0.8502	1.283	0.470349	1.7935	0.683909	6.9389
2.1	0.8804	1.309	0.453755	1.8512	0.734266	7.14287
2.15	0.9153	1.336	0.440797	1.9078	0.808835	7.36969
2.2	0.9421	1.352	0.428877	1.9634	0.896318	7.61189
2.25	0.9715	1.373	0.418513	2.0188	0.742163	7.87863
2.3	0.9827	1.396	0.409787	2.0741	0.750553	7.80873
2.35	1.0133	1.433	0.40265	2.1288	0.870966	7.91623
2.4	1.0353	1.451	0.397517	2.1832	0.868499	8.0768
2.45	1.0845	1.49	0.39907	2.2362	1.57983	8.65707
2.5	1.1047	1.515	0.386706	2.2886	1.11967	9.89836
2.55	1.1184	1.533	0.381016	2.3433	1.13157	9.00594
2.6	1.1433	1.568	0.376042	2.3965	1.23963	9.27247
2.65	1.1719	1.593	0.372152	2.45	1.48137	9.63303
2.7	1.1915	1.623	0.368281	2.5031	1.49001	10.0089
2.75	1.225	1.648	0.364491	2.5558	1.61205	10.232
2.8	1.2518	1.685	0.365362	2.608	1.58908	10.402
2.85	1.3351	1.678	0.361154	2.6569	1.84663	10.7224
2.9	1.3241	1.704	0.392417	2.7103	1.85955	11.084
2.95	1.3309	1.724	0.388537	2.7487	1.91104	11.2681
3	1.3414	1.762	0.431286	2.7974	1.8755	11.3061

Vcc Test 1 Table Chip 9

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.7895	1.279	0.349593	1.7758	0.60125	6.64758
2.05	0.9326	1.296	0.334506	1.833	0.640194	6.82129
2.1	0.8458	1.321	0.322494	1.8895	0.645591	6.99286
2.15	0.8709	1.34	0.311679	1.9455	0.669716	7.16455
2.2	0.903	1.367	0.303989	2.0003	1.40398	7.75872
2.25	0.9316	1.386	0.294808	2.0551	1.13822	8.19058
2.3	0.956	1.412	0.287695	2.1098	1.02835	8.40488
2.35	0.9815	1.438	0.281477	2.1642	1.18232	8.41307
2.4	1.0074	1.467	0.27593	2.218	1.42566	8.75956
2.45	1.0343	1.469	0.27053	2.2716	1.50178	9.20436
2.5	1.2025	1.515	0.26754	2.3251	1.2063	9.0192
2.55	1.0787	1.544	0.260359	2.3784	1.27347	8.91155
2.6	1.1068	1.575	0.256812	2.4314	1.59794	9.74594
2.65	1.1308	1.537	0.253084	2.4844	1.5776	10.0256
2.7	1.158	1.625	0.251187	2.5371	2.56524	9.68819
2.75	1.1837	1.655	0.249487	2.5888	3.33435	12.036
2.8	1.2061	1.689	0.245331	2.6402	2.6876	14.1626
2.85	1.23	1.714	0.242972	2.6923	2.87081	13.9125
2.9	1.2508	1.745	0.23995	2.7452	2.60141	12.8311
2.95	1.2872	1.777	0.240994	2.7978	4.68379	11.5787
3	1.3025	1.799	0.237188	2.8482	4.0499	16.4064

Vcc Test 2 Table Chip 0

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.8333	1.294	0.42195	1.7827	0.790667	6.75391
2.05	0.865	1.322	0.405084	1.8402	1.08917	7.1678
2.1	0.8946	1.337	0.387597	1.8972	1.15578	7.33425
2.15	0.9212	1.363	0.374895	1.9528	1.39038	7.89069
2.2	0.952	1.283	0.372034	2.008	1.47683	8.11945
2.25	0.9774	1.414	0.356855	2.0627	1.44314	8.3123
2.3	1.0024	1.437	0.34737	2.1171	1.16245	8.31672
2.35	1.0278	1.444	0.34048	2.1716	1.25471	8.50525
2.4	1.0538	1.495	0.335727	2.2254	1.50807	8.89547
2.45	1.0732	1.521	0.332891	2.2789	1.95131	9.26309
2.5	1.1052	1.552	0.33083	2.3318	2.01998	10.0081
2.55	1.1205	1.58	0.320673	2.3853	1.37092	9.52664
2.6	1.1618	1.571	0.317247	2.4386	2.06865	9.55285
2.65	1.1708	1.631	0.314923	2.4912	2.88816	10.4429
2.7	1.1941	1.663	0.308586	2.5435	2.72484	11.5828
2.75	1.2198	1.688	0.305029	2.5963	2.52561	11.2484
2.8	1.247	1.723	0.303376	2.6484	3.11096	11.0407
2.85	1.2743	1.525	0.314564	2.7004	4.90197	12.1846
2.9	1.3023	1.788	0.304204	2.7518	3.38568	13.2244
2.95	1.3317	1.814	0.301871	2.8044	4.26569	12.2119
3	1.3371	1.735	0.299903	2.8564	5.47512	12.2375

Vcc Test 2 Table Chip 1

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.8091	1.292	0.427165	1.769	0.925286	6.77588
2.05	1.0853	1.113	0.406404	1.8266	1.04121	7.20314
2.1	0.9945	1.343	0.390261	1.8842	1.23332	7.42867
2.15	0.8923	1.154	0.377479	1.9408	1.17184	7.62172
2.2	0.9139	1.391	0.36359	1.9971	1.45231	7.53683
2.25	0.9446	1.417	0.358779	2.0525	1.72419	8.0277
2.3	1.0855	1.435	0.346628	2.1074	1.48967	8.75096
2.35	1.024	1.179	0.339504	2.1621	1.4826	9.07386
2.4	1.0216	1.491	0.335376	2.2159	1.53422	10.1532
2.45	1.0459	1.519	0.328808	2.2703	1.58093	9.46621
2.5	1.0679	1.468	0.320878	2.324	1.98508	9.61203
2.55	1.2603	1.564	0.3145	2.3777	2.03965	9.90767
2.6	1.1196	1.418	0.311546	2.4309	2.2391	10.5376
2.65	1.1421	1.626	0.305377	2.4839	2.34059	10.7002
2.7	1.164	1.656	0.302446	2.5371	2.3147	10.7218
2.75	1.1911	1.68	0.299127	2.5898	1.97464	10.7621
2.8	1.214	1.713	0.296614	2.6417	2.05697	10.7822
2.85	1.2535	1.738	0.29795	2.6939	3.20086	11.0873
2.9	1.2713	1.762	0.291763	2.7459	3.70371	12.4982
2.95	1.2909	1.802	0.288903	2.798	2.94633	12.6426
3	1.3106	1.832	0.286895	2.85	3.25824	13.0549

Vcc Test 2 Table Chip 2

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.7904	1.284	0.375348	1.7777	0.735221	6.90505
2.05	0.8188	1.304	0.359507	1.8353	0.763581	7.05877
2.1	0.8472	1.325	0.34627	1.8918	0.784622	7.19865
2.15	0.8745	1.347	0.334397	1.9482	0.839158	7.34727
2.2	0.902	1.372	0.326377	2.0035	1.18119	7.53778
2.25	0.9296	1.395	0.32038	2.0577	2.1209	8.3948
2.3	0.9554	1.213	0.312166	2.1123	1.62765	8.86284
2.35	0.9816	1.447	0.304371	2.1669	1.49278	8.46256
2.4	1.0096	1.469	0.300349	2.2211	2.29824	8.74187
2.45	1.0348	1.5	0.295267	2.2745	2.57441	9.63789
2.5	1.0575	1.528	0.28666	2.3275	1.31875	10.355
2.55	1.082	1.555	0.281836	2.3814	1.29366	9.34181
2.6	1.1086	1.582	0.282186	2.4343	2.42498	9.77431
2.65	1.1327	1.613	0.276844	2.4866	2.14453	11.1085
2.7	1.1562	1.642	0.274528	2.5395	2.73718	10.8604
2.75	1.2094	1.671	0.271834	2.5921	3.49829	11.3281
2.8	1.2056	1.699	0.269099	2.6441	3.66571	12.2073
2.85	1.228	1.729	0.263177	2.6962	2.16771	13.2145
2.9	1.2531	1.761	0.264625	2.7486	4.00704	13.1481
2.95	1.275	1.789	0.262018	2.8005	4.04939	13.2222
3	1.2982	1.82	0.260048	2.8526	4.70241	13.3727

Vcc Test 2 Table Chip 3

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.9093	1.281	0.463373	1.727	0.689661	6.6931
2.05	0.8501	1.304	0.447439	1.7844	0.905512	6.89138
2.1	0.8743	1.326	0.43373	1.8409	1.01212	7.35319
2.15	0.9016	1.206	0.421967	1.897	0.987878	7.57624
2.2	0.9288	1.372	0.411847	1.9524	0.945311	7.64071
2.25	0.9555	1.394	0.402946	2.0077	1.05271	7.78908
2.3	0.98	1.421	0.39408	2.0624	0.916839	7.80549
2.35	1.0086	1.446	0.387403	2.117	0.995892	7.97579
2.4	1.034	1.466	0.387775	2.1709	2.76271	8.26045
2.45	1.0607	1.502	0.384932	2.2228	2.96441	10.852
2.5	1.0863	1.527	0.376299	2.2763	2.07363	11.1276
2.55	1.1063	1.555	0.369642	2.3304	1.51044	10.0365
2.6	1.1333	1.579	0.367558	2.3834	2.09466	9.61153
2.65	1.1547	1.609	0.3621	2.4355	1.6242	10.6958
2.7	1.1801	1.632	0.363881	2.4883	2.96391	10.0427
2.75	1.2451	1.668	0.358535	2.5404	2.46868	11.0011
2.8	1.3212	1.696	0.356489	2.5925	2.94237	11.1195
2.85	1.2495	1.725	0.351446	2.6446	1.98239	11.6212
2.9	1.2744	1.753	0.355851	2.6964	4.58153	12.3741
2.95	1.2972	1.776	0.350837	2.7484	4.19323	13.1921
3	1.318	1.806	0.345657	2.8005	2.86608	13.4156

Vcc Test 2 Table Chip 4

C	Y1	Y2	Y3	Y4	Y5	Y6
VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.9207	1.284	0.493416	1.7645	0.69605	6.92307
2.05	x	1.305	x	1.8241	x	6.96796
2.1	0.9773	1.332	0.492198	1.8805	1.6564	7.89621
2.15	1.0057	1.341	0.466323	1.9369	1.73117	8.34984
2.2	1.0302	1.37	0.444846	1.9941	1.42519	8.37563
2.25	1.0436	1.384	0.432821	2.0512	1.15849	8.25733
2.3	1.0739	1.403	0.4204	2.1069	0.900797	8.15466
2.35	1.1007	1.425	0.407819	2.162	0.932468	8.11208
2.4	1.1279	1.454	0.400324	2.2172	0.938159	8.18706
2.45	1.144	1.475	0.394253	2.2713	0.881888	8.3179
2.5	1.1815	1.496	0.388727	2.3248	0.952306	8.52717
2.55	1.2072	1.531	0.381104	2.3787	1.06485	8.7956
2.6	1.2385	1.548	0.389005	2.432	1.94539	9.12837
2.65	1.2817	1.576	0.401685	2.4828	6.09423	12.4551
2.7	1.3143	1.592	0.384145	2.5356	3.98516	13.0773
2.75	1.32	1.622	0.373056	2.5897	3.12804	11.8221
2.8	1.3421	1.658	0.370849	2.6424	2.67489	11.8902
2.85	1.3653	1.685	0.361238	2.6953	2.27411	11.1758
2.9	1.3719	1.725	0.355959	2.7479	1.67059	11.4005
2.95	1.3921	1.738	0.352391	2.8006	1.55468	10.6204
3	1.4562	1.763	0.386742	2.8516	8.10813	13.1311

Vcc Test 2 Table Chip 5

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.7933	1.281	0.43461	1.7609	0.70969	6.71119
2.05	0.8122	1.299	0.412435	1.819	0.671609	6.84316
2.1	0.8486	1.325	0.397978	1.8762	1.07845	7.36867
2.15	0.8744	1.341	0.384582	1.9325	0.82282	7.83518
2.2	0.8961	1.372	0.372406	1.9884	0.830224	7.76189
2.25	0.9236	1.391	0.362026	2.0439	0.88869	7.89188
2.3	0.9451	1.417	0.354202	2.0988	1.03605	7.93411
2.35	0.979	1.444	0.349392	2.1534	1.29056	8.17875
2.4	1.0115	1.473	0.344244	2.2068	1.50493	9.37375
2.45	1.0819	1.501	0.335203	2.261	1.17855	9.19873
2.5	1.0547	1.527	0.330457	2.3143	1.318	9.5107
2.55	1.0834	1.553	0.325088	2.3676	1.23854	9.35554
2.6	1.1073	1.579	0.321647	2.4207	1.60896	9.46061
2.65	1.1327	1.607	0.317245	2.4737	1.53715	9.61192
2.7	1.1644	1.641	0.316952	2.5265	1.95905	9.65032
2.75	1.1876	1.67	0.314991	2.5788	2.58038	10.0605
2.8	1.2096	1.698	0.310109	2.6311	2.26181	10.6884
2.85	1.2288	1.724	0.304477	2.6828	2.18367	13.0126
2.9	1.2566	1.756	0.301898	2.7357	1.90396	12.0909
2.95	1.2797	1.784	0.29827	2.7882	2.08616	11.3878
3	1.296	1.813	0.295729	2.8405	2.05043	11.1286

Vcc Test 2 Table Chip 6

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	x	1.257	x	1.691	x	6.57946
2.05	x	1.266	x	1.7469	x	7.27028
2.1	0.9202	1.293	0.499747	1.8045	1.34937	7.31964
2.15	0.9566	1.302	0.488221	1.8613	1.21964	7.56844
2.2	0.9786	1.337	0.476835	1.9161	1.12901	7.94145
2.25	1.008	1.342	0.468072	1.9723	1.34003	7.94452
2.3	1.0458	1.385	0.462469	2.0269	1.38121	8.2917
2.35	1.0616	1.4	0.450705	2.0818	1.24291	8.38094
2.4	1.0909	1.436	0.452149	2.1353	2.37105	8.80433
2.45	1.1146	1.467	0.447773	2.1872	2.31889	9.65118
2.5	1.1286	1.485	0.439504	2.241	2.12265	9.83919
2.55	1.1783	1.506	0.431625	2.2945	2.65937	10.6692
2.6	1.1776	1.331	0.428403	2.3483	2.91018	10.3743
2.65	1.2052	1.587	0.421721	2.4015	2.31111	10.7195
2.7	1.2343	1.59	0.42059	2.4546	2.06111	10.6912
2.75	1.2547	1.626	0.415855	2.5079	1.9815	10.2548
2.8	1.277	1.656	0.410161	2.5608	2.55106	10.3362
2.85	1.3027	1.68	0.414139	2.6137	5.06293	10.5852
2.9	1.3383	1.706	0.408795	2.6625	4.71124	13.046
2.95	1.3495	1.741	0.403551	2.714	4.05194	14.4569
3	1.3796	1.772	0.397819	2.7684	4.64376	14.3588

Vcc Test 2 Table Chip 7

VCC	VIL	VIH	VOL	VOH	POWER CONSUMPTION Ramp Down (mW)	POWER CONSUMPTION Ramp Up (mW)
2	0.804	1.279	0.399715	1.7742	0.685168	6.70348
2.05	0.8295	1.288	0.384008	1.8322	0.724919	6.97304
2.1	0.8607	1.316	0.369904	1.8889	0.74054	7.12633
2.15	0.8755	1.346	0.356044	1.9455	0.815737	7.41392
2.2	1.0215	1.377	0.345071	2.0012	0.792761	7.47954
2.25	0.9528	1.386	0.33617	2.0566	0.944592	7.65528
2.3	0.961	1.403	0.327193	2.1116	0.775922	7.9624
2.35	0.9894	1.434	0.31857	2.1663	0.927698	8.04613
2.4	1.0143	1.461	0.315551	2.2205	0.978126	8.34068
2.45	1.048	1.484	0.311399	2.2739	1.1932	8.61431
2.5	1.0647	1.52	0.304575	2.3272	1.19883	8.93004
2.55	1.0913	1.543	0.304197	2.3807	2.16367	9.13877
2.6	1.1131	1.562	0.297439	2.4329	1.95851	11.1648
2.65	1.1383	1.598	0.29095	2.4867	1.4453	10.4085
2.7	1.2737	1.625	0.287541	2.5399	1.76976	9.8089
2.75	1.204	1.664	0.282398	2.5926	1.45874	9.8216
2.8	1.2047	1.67	0.280083	2.6447	1.56628	10.0907
2.85	1.2344	1.705	0.282592	2.6966	2.91798	10.8531
2.9	1.259	1.745	0.276196	2.7487	2.00608	11.7483
2.95	1.2957	1.771	0.273412	2.8012	2.2223	11.165
3	1.3081	1.797	0.276461	2.8531	2.73249	11.1786

Vcc Test 2 Table Chip 8

VCC	VIL	VIH	VOL	VOH	OWER CONSUMPTION Ramp Down (mW	OWER CONSUMPTION Ramp Up (mW
2	0.796	1.268	0.487506	1.7158	0.843205	6.94232
2.05	0.8218	1.288	0.470377	1.773	0.84898	7.40717
2.1	0.8499	1.309	0.459341	1.8301	1.3406	7.44071
2.15	0.8764	1.333	0.444294	1.8863	1.00389	7.62073
2.2	0.9059	1.354	0.434495	1.9412	1.08517	8.25948
2.25	0.9301	1.379	0.425662	1.9962	0.958968	8.30541
2.3	0.9585	1.407	0.417739	2.0513	1.12938	8.0829
2.35	0.983	1.431	0.410555	2.1053	1.12388	8.46096
2.4	1.0109	1.458	0.404469	2.1595	1.11561	8.37528
2.45	1.0308	1.486	0.400113	2.2121	1.10568	8.6241
2.5	1.059	1.512	0.404403	2.2594	1.58511	8.89543
2.55	1.0791	1.543	0.409137	2.3099	2.64614	10.2345
2.6	1.1126	1.564	0.412158	2.3619	3.70368	12.0173
2.65	1.1344	1.601	0.414114	2.4133	3.9491	13.8372
2.7	1.1587	1.627	0.398229	2.4626	3.55418	13.4501
2.75	1.1774	1.627	0.396239	2.5153	3.3869	13.5812
2.8	1.2016	1.686	0.391293	2.5638	2.79693	12.3751
2.85	1.2257	1.717	0.382903	2.6231	2.56257	11.565
2.9	1.2411	1.745	0.481238	2.6642	2.07682	11.3704
2.95	1.2678	1.77	0.372677	2.7358	1.97262	11.161
3	1.2891	11.16	0.369743	2.7881	1.95305	11.0986

Vcc Test 2 Table Chip 9