# PCM BEHAVIOR IN FINITE THICKNESS SLABS UNDER A STEP RESPONSE HEAT INPUT

A Thesis

by

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ABSTRACT

Phase change materials (PCMs) can provide thermal buffering to systems that experience transient heat loads, including electronics packaging. Placing the PCM in the primary path of heat rejection decreases the thermal resistance between the heat source and the PCM volume, but increases the total thermal resistance between the heat source and heat sink. In systems that operate in both steady-state and transient regimes, this introduces tradeoffs between cooling performance in these distinct regimes. Employing a conductive finite volume model, Parapower, we investigate those tradeoffs considering the impact of adding a layer of gallium, a low melting point metal, and a layer of copper between a planar heat source and a convective boundary condition heatsink. We demonstrate: 1) side-by-side comparisons of latent (Ga) and sensible (Cu) heat storage layers must consider different layer thicknesses to account for the different thermal storage mechanisms, 2) for short periods of time, conditions exist in which a PCM outperforms a traditional heat sink for transient thermal buffering at an equivalent steady state temperature rise, and 3) under these conditions, the Ga layer is approximately an order of magnitude thinner than the equivalent Cu, leading to significant mass and volume savings.

# DEDICATION

Dedicated to my wife, mother, father, brother, and Ramon Olachia, whom have made me far greater a person than I otherwise would be, and without which this work would not exist. To my younger self, who always doubted I would accomplish anything of substance.

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Thanks also go to my friends and colleagues and the department faculty and staff for making my time at Texas A&M University a great experience.

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## CONTRIBUTORS AND FUNDING SOURCES

### Contributors

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# 1. INTRODUCTION

Phase change materials (PCMs) have the capability of providing transient thermal buffering by absorbing/discharging thermal energy during melting/freezing. Thermal storage and temperature suppression applications for this are numerous, and include heat transfer modules, power storage, and composite material design for these applications. In my time at Texas A&M, I have incorporated PCM physics into physics based simulations, aided in the design and evaluation of heat transfer modules, contributed to the design of lamellar composite PCMs, and performed a study on the effectiveness of PCMs in electronic heat sinks. For the sake of brevity, this master's thesis shall focus on the most latter of these.

As power electronics modules decrease in size and increase in power, transient temperature spikes become a greater threat to module lifespan.[1], [2] PCMs have shown to be promising candidates for reducing transient temperature spikes in power electronics packaging under transient thermal loads, due to their large effective thermal storage capability, derived from the latent heat of fusion, in a small and compact volume.[3]–[5] Generally speaking, two principle configurations exist for integrating PCMs into an electronics package: 1) locating PCMs in the primary path of heat rejection (i.e., thermally in series between the heat source and heat sink), or 2) locating PCMs in a secondary position, creating a secondary thermal reservoir which is not in the primary path of heat rejection (i.e., thermally in parallel) (Fig. 1). Placing PCMs in a secondary position could include integrating PCMs in a potting compound that

surrounds a device, or using a thermal ground plane to move spread heat laterally and into a volume of PCM.[6]–[8] PCMs in secondary positions utilize volume which was not previously utilized as part of the thermal management system, but have the potential downside that the PCM is not as closely integrated, and therefore not as responsive, as if it is in more direct thermal path to the heat source. Placing PCMs directly in the primary path of heat rejection could include integrating PCMs into an electronics package or integrated within a heat sink.[4], [5], [9], [10] While this configuration generally reduces the thermal resistance between the heat source and the PCM volume, it does so at the cost of increasing the resistance between the heat source and heat sink, thereby increasing the temperature of at the heat source in the steady state condition. Thus, while integrating PCMs in the primary path of heat rejection offers intriguing possibilities, the general tradeoffs associated with this configuration have not been fully explored.

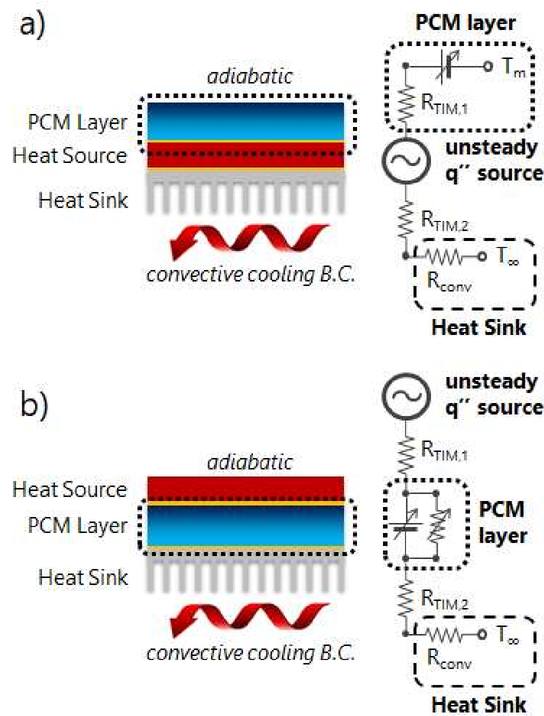


**Figure 1 Generalized configurations of electronics package, where a PCM volume may be introduced either a) not in the primary path of heat rejection (i.e., thermally in parallel), or b) in the primary path of heat rejection (i.e., thermally in series between the heat source and heat sink)**

Electronic devices are subject to both transient and steady state temperature rises, based on the device operation mode (pulsed or steady). Mitigating these temperature rises can introduce competing thermal requirements for a system. For example, the transient temperature rise may be mitigated by increasing the total thermal capacitance of the system, either by increasing sensible heat storage (by increasing the package mass), or by introducing latent heat storage (introducing PCMs).[11] However, introducing thermal capacitance can increase the overall thermal resistance of the system if the additional package mass or PCM is in the primary path of heat rejection, which in

turn increases the steady-state temperature rise. Thus, in systems which operate under mixed pulsed and steady modes, there likely exist tradeoffs between the transient and the steady state temperature rise. It is currently unclear how to assess such tradeoffs, particularly for cases which include PCMs.

In the case of PCMs in the primary path of heat rejection, it is clear that the effective thermal conductivity is a critical thermophysical property. In the steady state case, higher thermal conductivity tends to decrease the temperature rise due to Fourier law effects. In the transient case, higher thermal conductivity (as well as higher volumetric latent heat of fusion) tends to increase the rate of heat transfer into a PCM volume, also resulting in decrease in the junction temperature. Efforts to increase thermal conductivity in PCMs generally consists of creating composites of PCMs and thermally conductive materials such as carbon nanotubes,[12] pin or finned heatsinks [13]–[15], inverse opal structures [16], and expanded graphite [13]. Alternatively, metallic PCMs have larger intrinsic thermal conductivity, and are not subject to some of the issues associated with other thermal enhancement approaches (separation, manufacturing issues, etc.).[17]–[19]

Krishnan and Garimella investigated introducing a slab of copper or PCM between the heat source (electronic package) and the heat sink, simulated by a convectively cooled boundary condition.[9] This paper established that, under certain circumstances, PCMs with high thermal conductivities (metallic alloys or copper foam/wax composites) can suppress junction temperature compared to copper heat sinks in the primary conduction path.[9] In addition, approximate expressions were derived to

estimate the volume of PCM needed and the relative magnitude of performance improvement vs copper or other PCMs. However, this study 1) focused on a very limited range of low heat fluxes (3 to 6 $W \cdot cm^{-2}$) and heat transfer coefficients on the cooled side of a slab (12 $W \cdot m^{-2}$ °C), which are not representative of many different conditions of interest in high power density systems, 2) does not directly address the relative tradeoffs between temperature rise in the steady state and in the transient condition, 3) considers only a single identical thickness slab, whereas it is clear that the optimal thickness for a PCM slab will vary greatly from that of a copper slab which stores heat through sensible heating, and finally 4) only considers systems which are initially at the melting point of the PCM, with no undercooling. Thus, in general, the relative tradeoffs introduced by placing a PCM volume directly in the path between the heat source and the ultimate heat sink remain unresolved.

Here, the feasibility of incorporating a metallic PCM (gallium) into the primary conduction path of a power electronics package under transient loads is examined. The response of a PCM under a step input transient load in comparison to a conductor in the primary path of thermal conduction with an initial steady state load is determined. It is shown that PCMs can provide superior temperature suppression for transient thermal loads in comparison to traditional conduction technologies under steady state load initial conditions. The effects of altering backside convection, initial and ambient temperatures, and PCM thickness on comparative temperature suppression are discussed. This study demonstrates that PCMs in the primary path of conduction can be a viable thermal management solution and introduces design trends useful to optimizing PCM use.

## 2. METHODS

### 2.1. Simulation

### 2.1.1. Program and Discretization

Simulations were performed with the Army Research Lab (ARL) Parapower program.[20] Parapower is a finite volume simulation tool built in Matlab that uses an implicit Euler finite difference method, combined with an implementation of the enthalpy method to simulate melting. [21] The program is a parametric solver capable of iterating over several different designs in a short span of time. Parapower has been extensively validated through a benchmark comparison to ANSYS, and analytical solutions. [20], [22], [23] Additionally, Parapower demonstrates the properties of convergence and consistency by trending towards a given solution value as mesh and time step size are decreased and mesh quality remains constant.[24] Parapower approximates the solution to the cartesian heat diffusion equation

$$\frac{\partial}{\partial x}\left(k\frac{\partial T}{\partial x}\right)+\frac{\partial}{\partial y}\left(k\frac{\partial T}{\partial y}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)+q=\rho c\frac{\partial T}{\partial t}. \qquad \text{Eq.1}$$

This is done by creating a thermal resistance network and solving for the temperature at each time embodied by a matrix of the form:

$$\begin{bmatrix} C_{1,1}^{p} & \cdots & C_{1,n}^{p} \\ \vdots & \ddots & \vdots \\ C_{n,1}^{p} & \cdots & C_{n,n}^{p} \end{bmatrix}\begin{bmatrix} T_{1}^{p+1} \\ \vdots \\ T_{n}^{p+1} \end{bmatrix}=\begin{bmatrix} q''^{p+1}_{1} \\ \vdots \\ q''^{p+1}_{n} \end{bmatrix}-\frac{1}{\Delta t}\begin{bmatrix} \rho_{1}^{p}c_{1}^{p}V_{1}T_{1}^{p} \\ \vdots \\ \rho_{n}^{p}c_{1}^{p}V_{n}T_{n}^{p} \end{bmatrix}, \qquad \text{Eq. 2}$$

where $T$ is the temperature, $q''$ is the heat flux, $\Delta t$ is the size of the time step, $\rho$ is the density, $c$ is the specific heat, and $V$ is the volume of a given node. $C$ indicates the total conductance between two given adjacent nodes in the rectilinear grid. The subscript indicates the specific element in the resistance network. The superscript indicates the time step of being referenced where $p$ is the current time. PCM liquid fraction and temperature during melting are modified by the equation

$$\Phi_j^{p+1} = \Phi_j^p + \frac{\left(T_j^{p+1} - T_{mj}\right)c_j^{p+1}}{H_j}, \qquad \text{Eq. 3}$$

where the $j$ subscript indicates a particular PCM element, $\Phi$ is the melted phase fraction in that element , $T_m$ is the melting temperature of the element, and $H$ is the enthalpy of fusion of the PCM element. Once the melted phase fraction reaches 1, the melting reaction is complete, and additional heating results in sensible heating of a volume. Thus, all of the melting materials in this study melt at a single well-defined temperature.

A variable grid size was used to capture the relevant physics within the materials with minimum computational complexity. The meshes generated within Parapower are natively 3D, however X and Y spatial discretization was not used, resulting in simulations that are effectively 1D. All element size dimensions given correspond to the Z direction. The silicon carbide had an element size of 0.05 mm. The test layer had two different element sizes: one near the silicon carbide/test layer interface to capture more early melting processes that are more sensitive to element size and a second courser element size to describe the remainder of the test layer. The finer test layer element size is used for the first $1/10^{\text{th}}$ of the thickness of the test layer next to the silicon carbide

interface, and subdivides this space into 10 elements. The remainder of the test layer is subdivided into 9 elements. For the thickest PCM test layer of 10 mm, this resulted in elements too large to adequately capture the melting physics. The finer grid was changed to compose the first $3/10^{th}$ of the test layer with an element size of 0.025 mm for the 10 mm thickness case to address this. Interfacial thermal resistance is considered negligible and is not included in this model. Likewise, convection within melted PCM is considered negligible as both the small timescales of interest and small thicknesses reduce the impact of convection.[9]

### 2.1.2. System Geometry and Material Properties

The geometry of this study consists of a bilayer slab, heated on one side by a constant heat flux for a finite period of time, and subject to a convective boundary condition on the opposing side (Fig. 2). The slab is composed of a 0.5 mm thick silicon carbide slab, representing a power electronics chip, directly in contact with a slab referred to as the 'test layer', composed of either copper or a PCM material. The test layer has a thickness of $L$ (from 0.1 to 10 mm). The top surface ($y = L + 0.5$ mm) is cooled by convection, where the convection coefficient, $h_\infty$, varies from $10^1$ to $10^4$ $W \cdot m^{-2} \cdot °C^{-1}$, and the temperature of the coolant fluid, $T_\infty$, varies from -70.2 °C To 29.8 °C, corresponding to $T_m$ to $T_m$-100°C, where $T_m$=29.8°C. All other boundary conditions are adiabatic. All temperature measurements are taken at the heated base surface, which represents the hottest location within the simulation. The thermophysical properties for the phases used in this study can be found in Table 1. Material properties are not

strongly temperature dependent over the temperature range concerned. Therefore, the temperature dependence of the material properties are neglected.

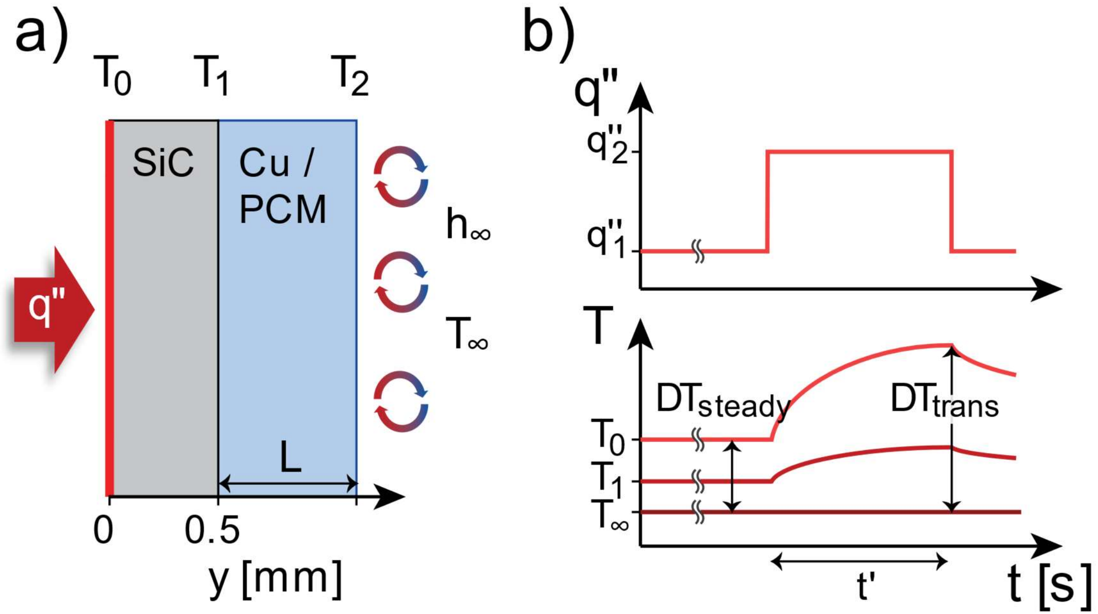


**Figure 2 a) Geometry of the system of study. b) schematic of temperatures initially at steady state undergo a transient heat pulse for the geometry of a)**

**Table 1 Thermophysical properties of materials used in this study**

| | | SiC[a] | Copper[b] | Gallium[c] |
|---|---|---|---|---|
| Thermal cond. (sol.), $k_{solid}$ | $W \cdot m^{-1} \cdot {}^{\circ}C^{-1}$ | 370 | 390 | 33.7 |
| Thermal cond. (liq.), $k_{liquid}$ | $W \cdot m^{-1} \cdot {}^{\circ}C^{-1}$ | - | - | 24 |
| Density (sol.), $\rho_{solid}$ | $kg \cdot m^{-3}$ | 3210 | 8,900 | 5,903 |
| Density (liq.), $\rho_{liquid}$ | $kg \cdot m^{-3}$ | - | - | 6,093 |
| Specific Heat (sol.), $c_{, sol}$ | $J \cdot kg^{-1} \cdot {}^{\circ}C^{-1}$ | 750 | 390 | 340 |
| Specific Heat (liq.), $c_{, liq}$ | $J \cdot kg^{-1} \cdot {}^{\circ}C^{-1}$ | - | - | 397 |
| Melting temp., $T_m$ | C | - | - | 29.8 |
| Enthalpy of Fusion, $H$ | $J \cdot g^{-1}$ | - | - | 80.3 |

[a] Properties from ref. [25], [26]

[b] Properties from ref. [27], [28]

[c] Properties from ref. [29]

## 2.2. Theory

For the majority of the cases outlined in this paper, the lumped capacitance method applies. This states that if the Biot is less than 0.1, then the temperature variation within the system is small compared to the temperature differences outside of the system, and the system may be treated as being at a uniform temperature with a small amount of relative error. Lumped capacitance does not apply during melting of a PCM. The Biot number here takes the form

$$Bi = h_{\infty}\left(\frac{\Delta x_s}{k_s} + \frac{\Delta x_t}{k_t}\right)$$

where $\Delta x_s$ and $\Delta x_t$ are the thicknesses and $k_s$ and $k_t$ are the thermal conductivities of the silicon carbide chip and test layers, respectively. Under the conditions of this paper, all simulations with the exception of PCM cases with convections coefficients at or over 1000 $\mathrm{w/m^2}$k and thicknesses at or greater than 0.001 m have a biot number less than 0.1.

When evaluating a transient thermal response, it is useful to identify different characteristic times, which govern the key phenomena occurring within the volume a point in time. Of key importance is the relative thermal rise constant $\tau$. This quantity describes the time taken to reach $\approx 63.2\%$ of the steady state temperature rise assuming no melting effects are taken into account. Thus, for all the systems described here, if a

PCM is not actively melting, the temperature rise with time takes a characteristic shape that can be described by $\tau$. Utilizing the lumped capacitance assumption, this quantity can be defined as:

$$\tau = \frac{\rho_s V_s c_s + \rho_t V_t c_t}{h_\infty A}, \quad \text{Eq. 4}$$

where $\rho_s, V_s, c_s$, and $\rho_t, V_t, c_t$ are the densities, volumes, and specific heats of the silicon carbide chip and test layers, respectively. $A$ is the convective area.[30] Temperature rise $T$ within the simulation before melting can be then be found as:

$$\frac{T - T_\infty - \frac{q''}{h_\infty A}}{T_i - T_\infty - \frac{q''}{h_\infty A}} = \exp\left(-\frac{t}{\tau}\right), \quad \text{Eq. 5}$$

where $T_i$ is the initial temperature.[30] From Eq. 5, the onset of melting is found to be:

$$t_{m,start} = -\tau \ln\left(\frac{T_m - T_\infty - \frac{q''}{h_\infty A}}{T_i - T_\infty - \frac{q''}{h_\infty A}}\right). \quad \text{Eq. 6}$$

$t_{m,finis}$ , the time at which all PMC in a system has fully melted, can be found using the quasi-steady state approximation and takes the form

$$t_{m,fini} \quad = \frac{L\rho H}{q''} + t_{m,start}.\text{[5]} \quad \text{Eq. 7}$$

# 3. RESULTS & DISCUSSION

## 3.1. Transient and Steady State Temperature Rise Trade Offs

A parametric sweep of test layer thickness is performed for both PCM and Cu layers to determine transient and steady state temperature rise trade-offs and to evaluate Pareto optimal dominance at any point. As the test layer thickness increases, the steady state temperature rise increases due to higher total thermal resistance, while transient temperature rise decreases, due to the higher total thermal capacitance. In these simulations, the system starts with a uniform initial temperature equal to the ambient temperature. The two cases are exposed to an initial heat flux at the heated surface, $q_1'' =$ 10 W·cm$^{-2}$, and allowed to equilibrate. The heat flux is then increased to a higher value, designated $q_2''$ = 100 to 500 W·cm$^{-2}$ at $t'$ = 0 s. Convection coefficients range from $H$ = 5,000 to 25,000 W·m$^{-2}$·°C$^{-1}$. The test layer thickness in these simulations is chosen to reach a target steady state temperature $\Delta T_{\text{steady}} = T_0 - T_\infty$, $t' = 0$ s, and ranges from 0.116 mm to 7.739 mm for the conductor, and from 0.01 mm to 0.913 mm for the PCM. The ambient temperature is chosen such that the SiC-test layer interface is less than 0.2 °C below the melting temperature of the PCM after equilibrating. The PCM test layer begins melting immediately after exposure to $q_2''$ and the transient temperature rise $\Delta T_{\text{trans}} = T_0 - T_\infty$, $t' > 0$ s at the heated surface is recorded at various times. The transient temperature rise at various times and steady state temperatures are compared. An introductory figure detailing a single selected time is shown in Fig. 3.

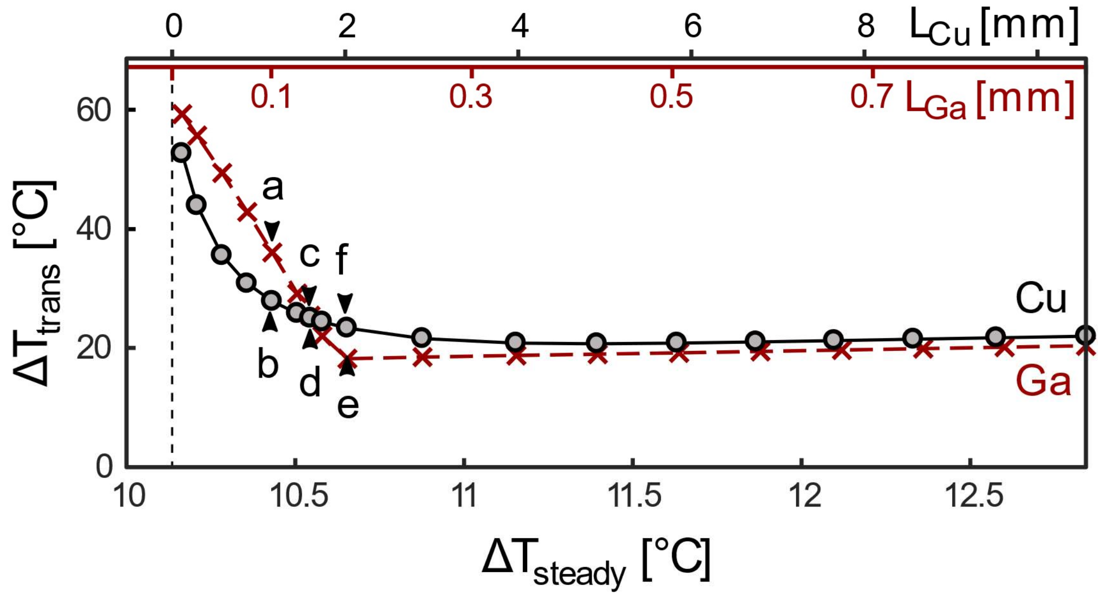


**Figure 3 Transient temperature rise above the ambient at a time of $t'$ = 0.1 s, for both conductor (Cu) and PCM (Ga) test layer cases, at $q''_2$ = 100 W·cm$^{-2}$, and $H$ = 10,000 W·m$^{-2}$·°C$^{-1}$.**

Parametric plots, which illustrate $\Delta T_{\text{trans}}$ and $\Delta T_{\text{steady}}$ as parametric functions of layer thickness, $L$, allow for a ready comparison of the two different layer types on the temperature rise at the junction (Fig. 3). For thicknesses which result in an equivalent steady-state temperature rise, the PCM case remains cooler during the transient heat pulse for thicknesses greater than the crossover (points c, d; Fig. 3), while the conductor case remains cooler for thicknesses less than the crossover point. As the steady-state temperature rise is directly correlated to the thermal resistance between the heat source and the heat sink, it is also linearly related to the thickness of both the PCM and conductor cases. The total heat capacitance in the conductor case increases increasing steady-state temperature rise, and results in decreasing transient temperature rise. As the steady-state temperature rise of the PCM case increases, the total potential latent heat

stored increases and at point e, the PCM has just fully melted at this time. At steady-state temperatures lower than point e (Fig. 3), the PCM has fully melted and the transient temperature rise increases at a more rapid pace than the conductor case due to the lower specific heat derived thermal capacitance of the PCM.

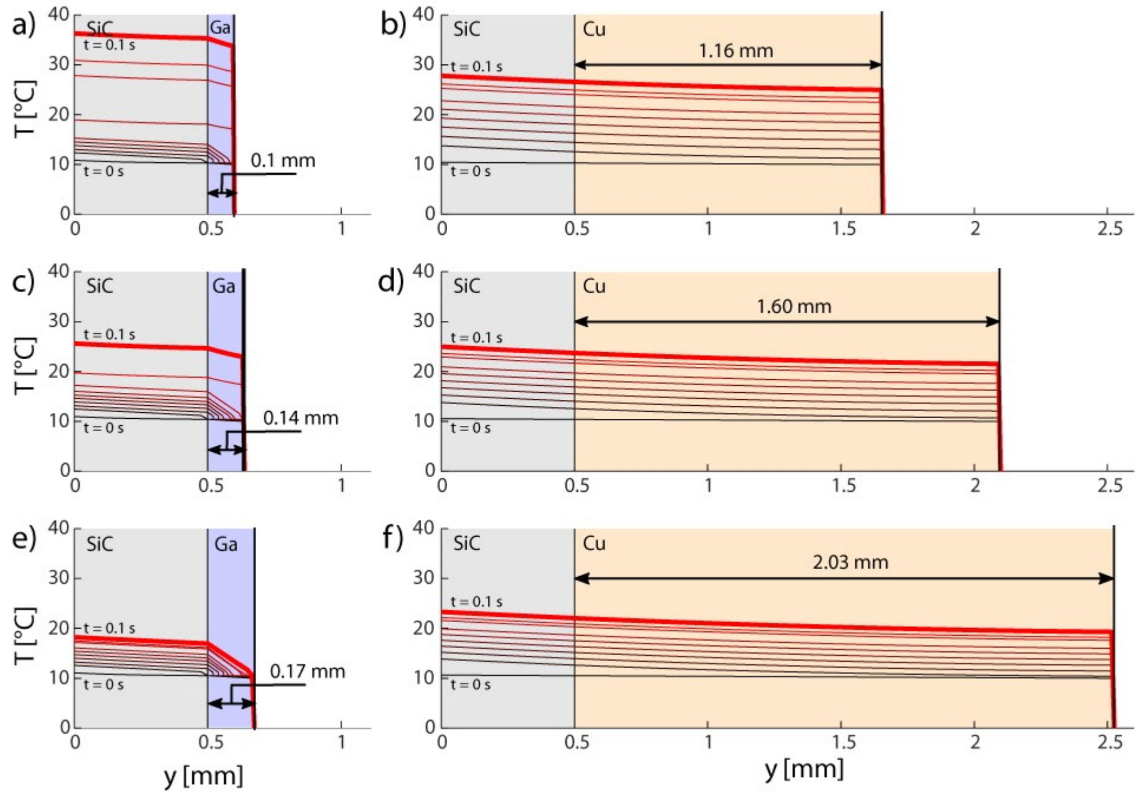


**Figure 4 Internal temperature distributions at times between 0 and 0.1 s for thickness corresponding to points a-f in Fig. 3. The silicon carbide/test layer interface is shown with a vertical line. Bold line indicates T(y) at t = 0.1 s. For all cases, Ga layer thickness is approximately an order of magnitude thinner than Cu layer thickness for points corresponding to the same $\Delta T_{\mathrm{steady}}$, due to the ratio of thermal conductivities of Ga and Cu.**

The internal temperature distribution at various times during a transient heat pulse is shown in Fig. 4. Cases horizontal to each other e.g., a and b, have the same total thermal resistance (using solid PCM material properties) and have the same steady-state

temperature rise. At many times less than 0.1 s (Fig. 4), the PCM cases have not fully melted and the temperature distribution within the PCM rapidly drops to the melting temperature. At ~0.1 s (the time shown in Fig. 3), although the PCM has fully melted in all cases, the PCM in cases c and e still provide for better transient temperature rise suppression than the copper cases d and f. Although brief, this is due to the PCM cases having superior temperature suppression up until this point and the rapidly rising temperature still catching up to the copper test layer cases. This is shows that PCM based transient temperature suppression can extend briefly beyond the time where the PCM fully melts. The copper test layer cases b, d, and f demonstrate the largely uniform temperature distribution within the entire structure. The large space taken up by the copper layer is necessary as energy is stored there as sensible heat, but since the thermal conductivity and diffusivity is large, there are only small temperature drops across the length of the test layer. This contrasts with the PCM case as energy is stored in a more energy dense form as latent heat but with much lower thermal conductivities which results in much smaller layers, but with steeper temperature drop. The difference in

thickness between similarly performing PCM and copper cases may be an important design decision for space limited applications.

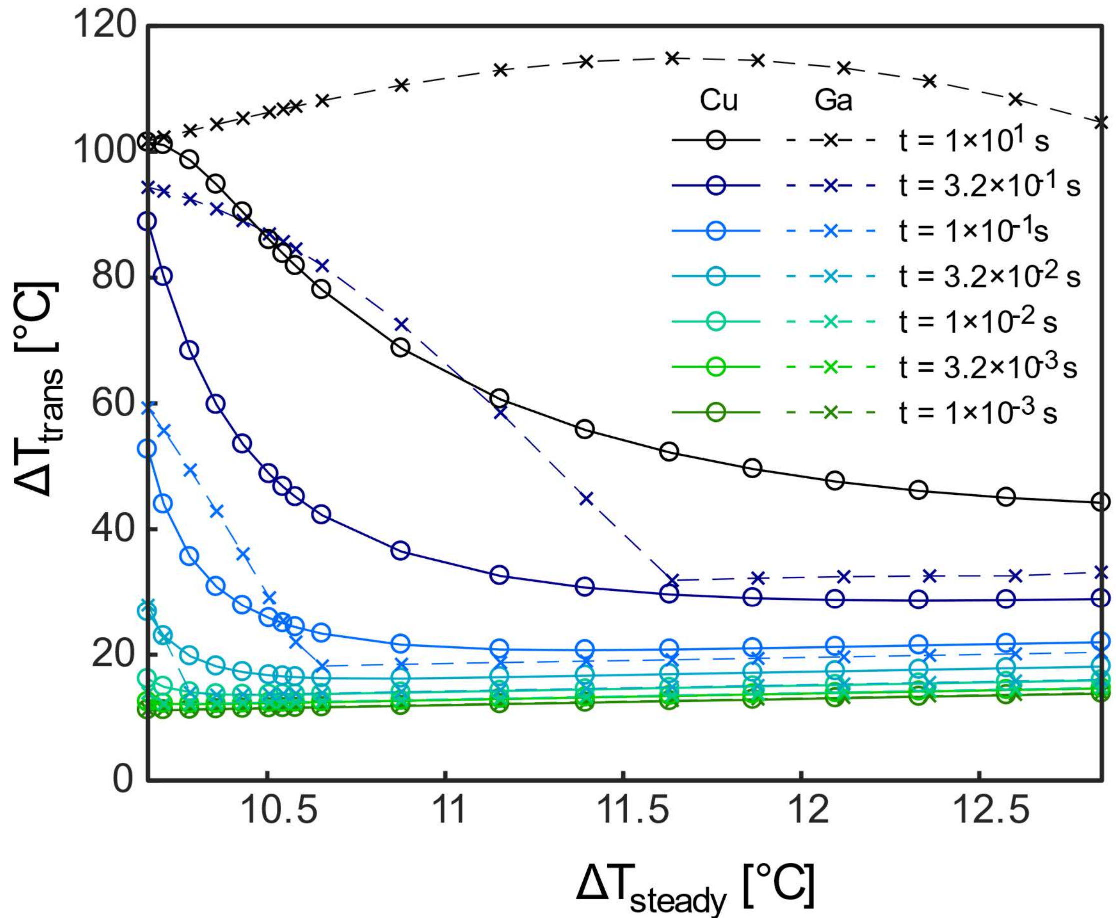


**Figure 5 Transient temperature suppression for conductor and PCM heatsinks as functions of steady state temperature rise at times ranging from 1 ms to 1 s. For all cases, $q_2''$ = 100 W·cm$^{-2}$, and $H$ = 10,000 W·m$^{-2}$·°C$^{-1}$.**

Fig. 5 shows the comparative transient temperature rise above the ambient temperature at different levels of steady-state temperature rise for PCM and conductor test layer cases. At times of 0.1 s and less, there exist conditions under which a pure PCM can achieve a greater degree of transient temperature suppression performance at the same level of steady-state temperature suppression performance. Fig. 6 and Fig. 7

perform this same comparison, but additionally compare selected values of transient heat flux and convection coefficient, respectively. The benefits of the PCM diminish as transient heat flux increases and disappears altogether at $q_2'' = 500$ W·cm$^{-2}$. Convection coefficient has little effect on the comparative performance between the PCM and conductor cases, but the overall magnitude of the temperature rise differs between cases with different convection coefficients.

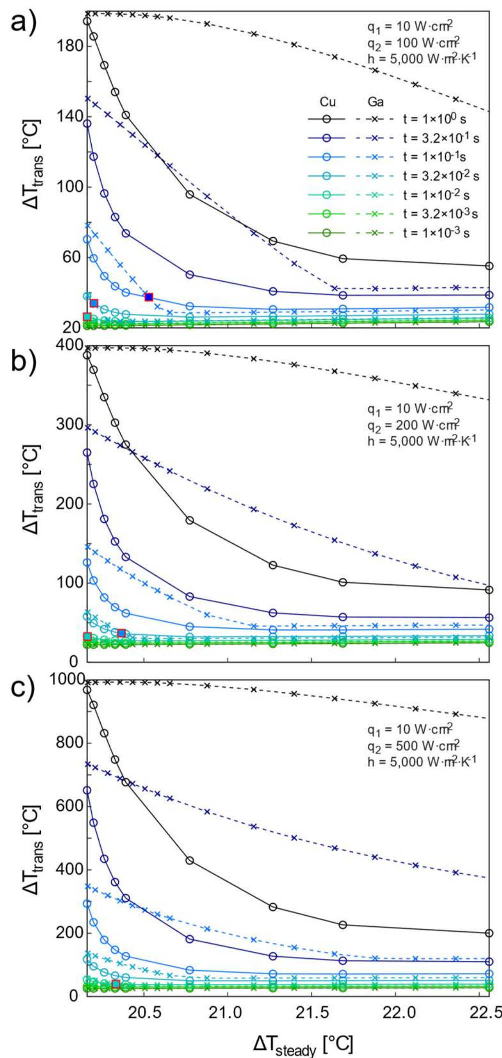


**Figure 6 Parametric temperature rise at different times for systematically increasing $q_2''$: a) $q_2''$ = 100 W·cm$^{-2}$, b) $q_2''$ = 200 W·cm$^{-2}$, c) $q_2''$ = 5100 W·cm$^{-2}$. For**

**all cases, $H$ = 5,000 W·m$^{-2}$·°C$^{-1}$. Legend for times illustrated in Fig. 6a. Squares illustrate crossover points for times 0.1 s and below.**

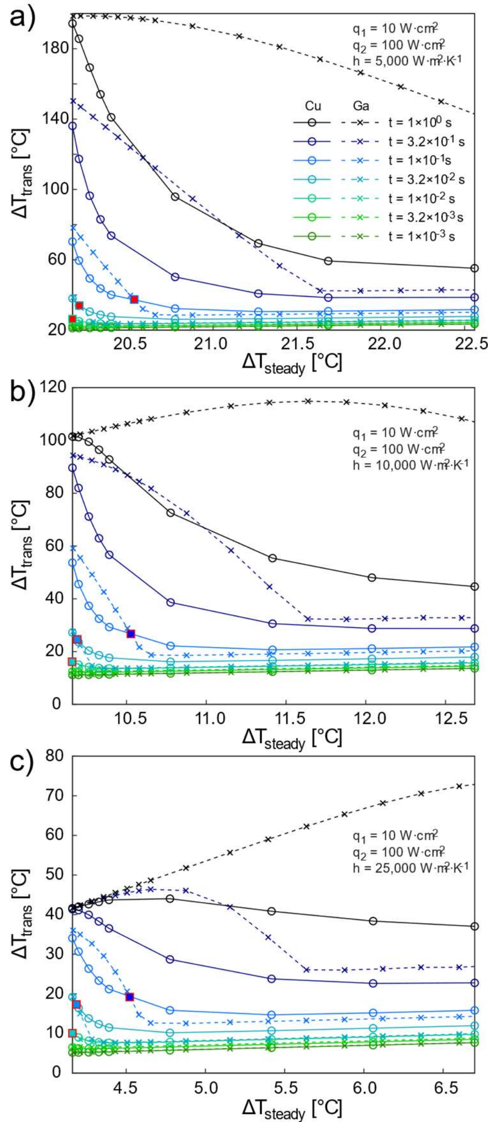


**Figure 7 Parametric temperature rise at different times for systematically increasing $H$: a) $H$ = 5,000 W·m$^{-2}$·°C$^{-1}$, b) $H$ = 10,000 W·m$^{-2}$·°C$^{-1}$, c) $H$ = 25,000 W·m$^{-2}$·°C$^{-1}$. For all cases, $q_2''$ = 100 W·cm$^{-2}$. Legend for times illustrated in Fig. 7a. Squares illustrate crossover points for times 0.1 s and below.**

### 3.2. Effects of individual Variables on PCM Versus Conductor Performance

The factors in relative transient thermal buffering between PCMs and conductors are investigated to develop design guidelines for incorporating PCMs for in-path pulsed thermal loads. The variables investigated are the thickness of the test layer $L$, the convection coefficient on the cooled surface of the test layer $h_{\infty}$, and the initial & ambient temperature of the system measured as the degree of undercooling below the melting point of the PCM $T_{\text{diff}}$. The initial and ambient temperature are always equal to one another. The PCM is initially entirely solid. The system begins at a uniform initial temperature and is exposed to a heat flux of 100 $W \cdot cm^{-2}$ at time $t = 0$ s and is simulated for 2.5 s with a timestep of 0.25 ms. The test layer is composed of either gallium or copper. For the simulations where $L$ is the variable, $H = 10{,}000$ $W \cdot m^{-2} \cdot {}^{\circ}C^{-1}$ and a $T_{\text{diff}} = 0$ °C are used, while $L$ takes values of either 0.1 mm, 1 mm, or 10 mm. For the simulations where $H$ is the variable, $T_{\text{diff}} = 0$ °C and $L = 1$ mm, while $H$ varies from 10 $W \cdot m^{-2} \cdot {}^{\circ}C^{-1}$ to 10,000 $W \cdot m^{-2} \cdot {}^{\circ}C^{-1}$ by orders of magnitude. For the simulations that determined the trends in changing the initial and ambient temperatures, $H = 10{,}000$

W·m$^{-2}$·°C$^{-1}$ and $L$ = 0.1 mm, while $T_{diff}$ takes values of either 0 °C, 25 °C, 50 °C, or 100 °C.

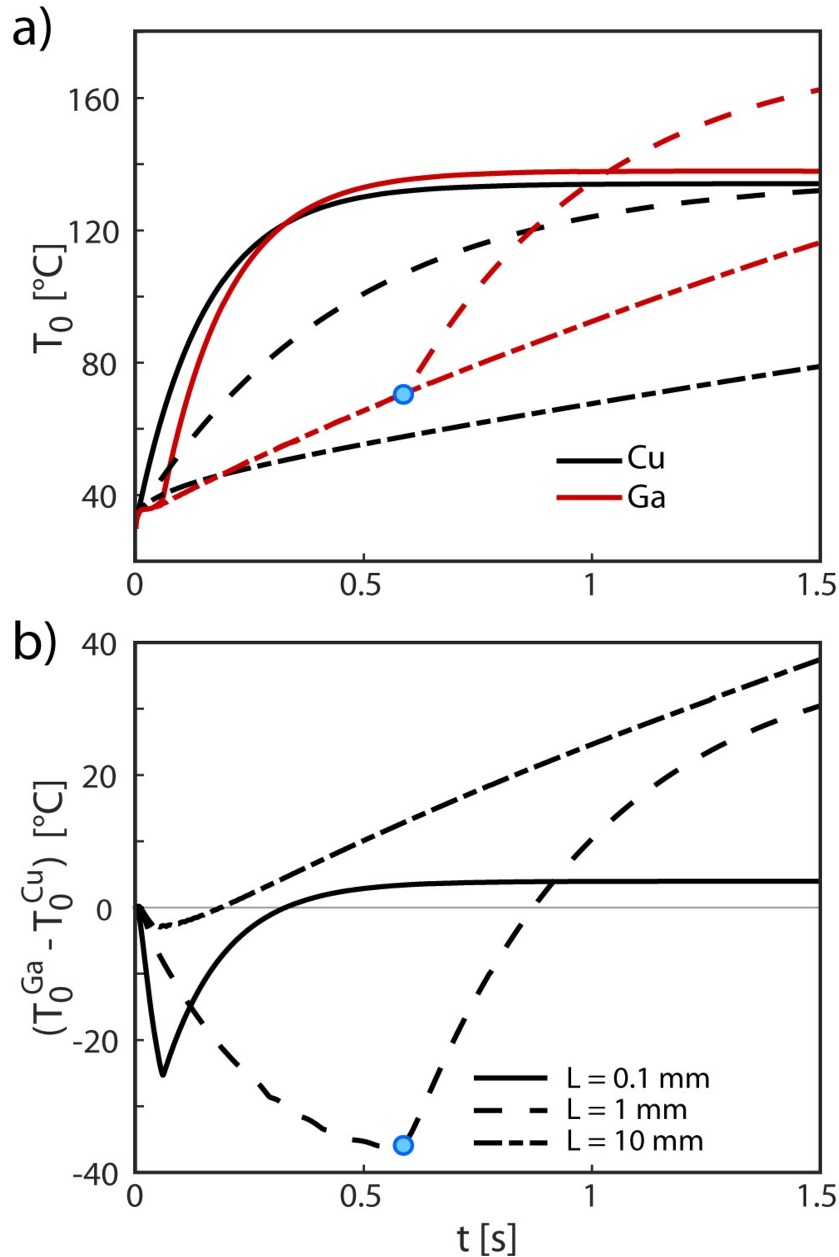


**Figure 8 a) Maximum temperature within the simulation for Copper and Gallium test layers with $T_{\text{diff}} = 0$ °C and $H$ = 10,000 W·m$^{-2}$·°C$^{-1}$, and b) the difference of the maximum temperature between simulations with Copper and Gallium test layers. The blue dot represents the time at which the Gallium fully melts.**

As the thickness of the test layers increases the maximum comparative performance of the PCM to the conductor first increases and then decreases (Fig. 8). Additionally, time until the PCM is fully melted increases as well. This may be seen by the sharp transitions in the temperature vs time behavior of the PCM cases. The time for fully melting for $L = 1$ mm is displayed as an example by the blue dots. Finally, the rate at which PCM case begins to outperform the conductor, shown as the slope of temperature difference, decreases as the thickness increases.

The decrease in the rate of temperature rise in the copper case with increasing thickness can be attributed to an increase in the thermal capacitance of the system. This can be seen from the increase in $\tau$ from Equation 4 and the resulting decrease in temperature at a given time from Equation 5. For the cases here, the temperature rise in the PCM cases are unaffected by thickness, except for, and until, the PCM melts. Therefore, the cause of the larger slope for the comparative temperature suppression in the 0.1 mm and 1 mm cases is due to the difference in thermal capacitance of the conductor case. The time that temperature suppression occurs over is directly related to the thickness of the PCM. As the PCM increases in thickness, the amount of thermal energy it can absorb before melting increases, which in turn increases the time of the thermal suppression. For the case of a 10 mm copper test layer compared to PCM, the thermal capacitance of the copper is large enough to suppress the temperature rise at the heated surface to a significant degree. In this case, the larger temperature gradient that develops in the PCM layer due to its lower thermal conductivity is now the limiting

factor in the performance of the temperature suppression of the system.

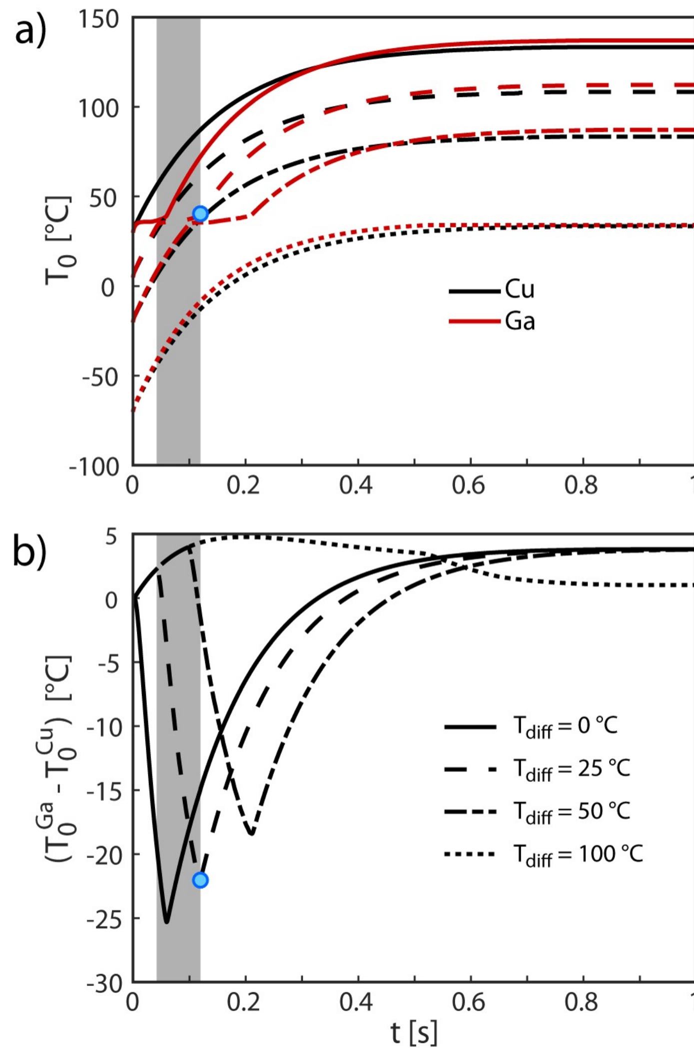


**Figure 9 a) Maximum temperature within the simulation for Cu and Ga test layers with L = 0.1 mm and $H$ = 10,000 W·m$^{-2}$·°C$^{-1}$, and b) the difference of the maximum temperature between simulations with Cu and Ga test layers. Grey boxes highlight the times at which the Gallium case for $T_{\mathrm{diff}} = 25\ °C$ is melting**

Greater degrees of undercooling of the PCM increases the time at which the temperature suppression effects of the PCM begin(Fig. 9). This additionally affects the time at which the temperature suppression from the PCM ends in most cases. For the majority of cases, the duration of the temperature suppression remains relatively

unchanged. The degree of undercooling has an effect on the amount of time that passes before the PCM reaches the melting temperature, and the relative difference between the rate of temperature rise in the PCM and copper cases before melting determines the extent of the detriment of the inactive PCM. The degree of comparative temperature suppression that the PCM grants is dependent upon the rate of increase in the temperature of the copper case during melting in the PCM. In cases of very large undercooling such as $T_{\text{diff}}$ = 100 °C, the PCM may never reach the melting temperature,

and the benefits of the PCM never materialize.

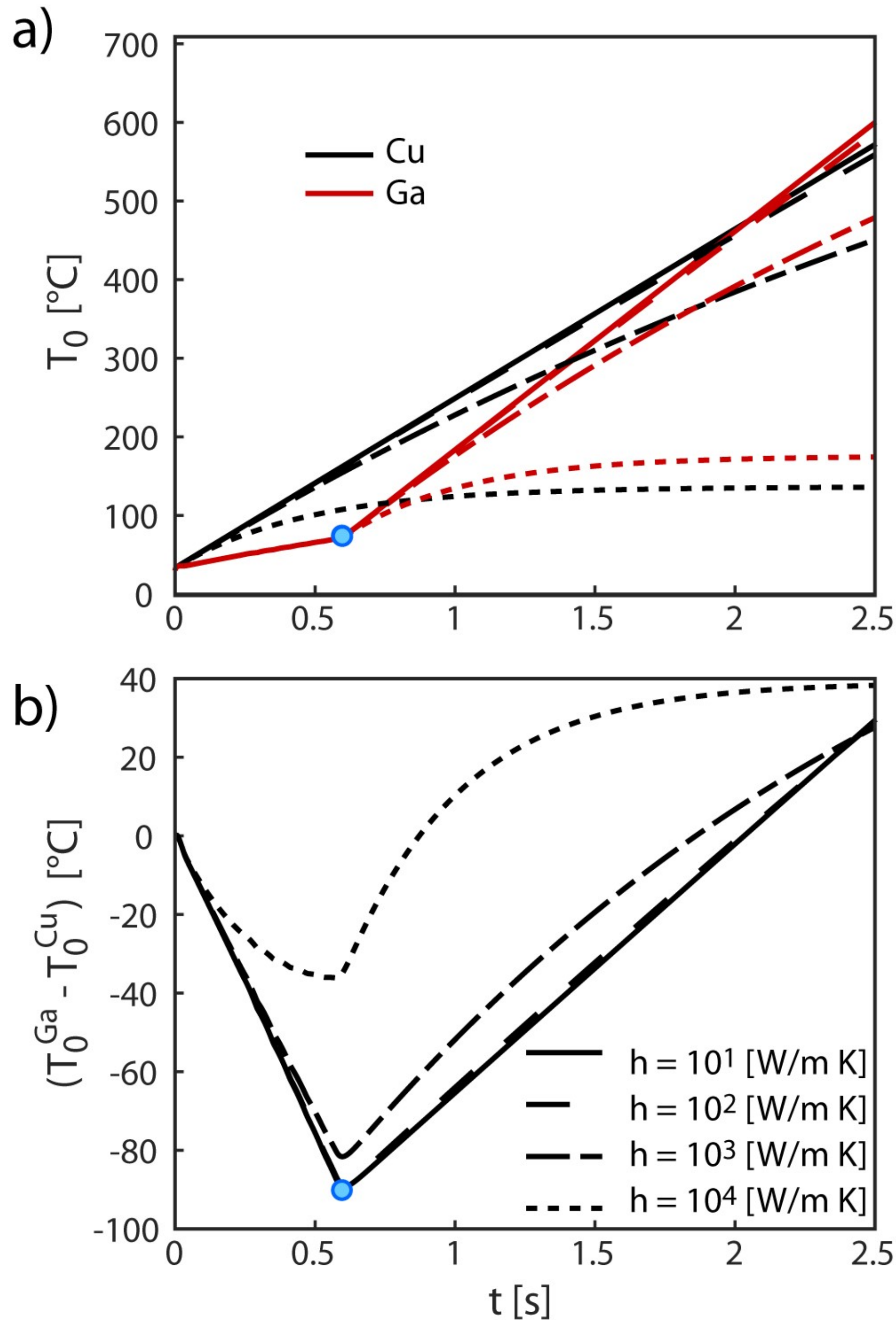


**Figure 10 a) Maximum temperature within the simulation for Copper and Gallium test layers with $T_{diff}$=0°C and L= 1 mm and b) the difference of the maximum temperature between simulations with Copper and Gallium test layers where negative numbers indicates the Gallium case is at a lower temperature**

In Fig. 10, results are show for selected cases where the convection coefficient is the only varying factor. As the convection coefficient changes, the copper case is affected at all times, but convection effects are only seen in the PCM case after melting. In addition, the degree of temperature suppression granted by use of the PCM is decreased with increasing convection coefficient.

For cases where the ambient and initial temperatures are equal to the melting temperature of the PCM, there are no convection effects on the PCM case before melting finishes. As such, convection only plays a role in the copper case before melting. The change in the effectiveness of the comparative temperature suppression with variable convection can be contributed wholly to the change in the response of the copper case with convection. As convection increases, the $\tau$ and $\Delta T_{\text{steady}}$ decrease, resulting in a decreased improvement in performance when compared to the PCM case. In addition, after melting has occurred, convection effects have a stronger effect on the PCM case than the copper case due to the greater temperature differences across the convection interface, ultimately due to the lower thermal conductivity of the PCM. As a result, as convection increases, the detriment of inactive melted PCM is reduced compared to the copper case.

Under conditions where the initial temperature and ambient temperature are not equal to the melting temperature of the PCM, a change in convection can have further effects such as extending melting time and can have an impact on temperature rise in the PCM case before melting has occurred. The impact of higher convection coefficients in

such cases can mean the difference between a PCM being beneficial to a system or being completely a detriment.

There are design decisions to be made in addressing the degree of thickness of a conductive layer in transient problems. As the thickness increases, the steady state temperature rise increases. However, the thermal capacitance increases with increasing thickness as well, which reduces the temperature rise at a given time (Fig. 3). In heat sinks that are built to handle high steady state load condition with lower transient loads, this trade-off is moot as the steady state temperature is always greater than the temperature rise of the transient response. However, systems built to operate in a transient regime need to consider reducing transient temperature rise and for the steady state temperature rise that may be encountered during a system failure or overload.

# 4. CONCLUSIONS

It is shown that there exists reasonable conditions under which a pure PCM in the path of primary heat transfer will have superior transient temperature suppression performance over a pure conductor. The benefit of whether a pure PCM will be beneficial in the primary direction of heat transfer depends on a number of criteria. Low convection coefficients result in greater temperature rise in the copper case, resulting in greater benefits from the temperature suppression from PCM. Greater degrees of undercooling below the melting point of the PCM results in less efficient use of the temperature suppressing effects of the PCM, and delayed benefits from the PCM. Low existing thermal capacitance in the system results in large transient temperature rises, allowing greater PCM temperature suppression benefits. The thickness of the PCM should be tailored to absorb a designated thermal pulse and no greater to avoid the existence of untransformed PCM which only acts as an insulator.

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