FULLY-INTEGRATED MILLIMETER-WAVE DUPLEXER MODULES WITH INTERNAL POWER AMPLIFIER AND LOW NOISE AMPLIFIER ON 0.18-μm BiCMOS PROCESS FOR FDD 5G AND OTHER MILLIMETER-WAVE APPLICATIONS

A Dissertation

by

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ABSTRACT

This research demonstrates two novel millimeter-wave (mm-wave) fully-integrated frequency-division duplexing (FDD) transmitting-receiving (TX-RX) front-end modules, including duplexer (DUX), power amplifier (PA), and low noise amplifier (LNA) on TowerJazz 0.18-μm SiGe BiCMOS. Additionally, two new proposed structures of BiCMOS PAs operating at mm-wave ranges are presented. These new contributions would benefit the developments of next generation wireless communications as well as other mm-wave wireless systems.

First, for the proposed structures of BiCMOS PAs, we adopt both advantages of hetero-junction bipolar transistor (HBT) and metal-oxide-semiconductor field-effect transistor (MOSFET, NMOS) to improve PA performances such as larger maximum output power (P_{sat}), higher gain, and better output 1-dB compression point (OP1dB). A detail investigation about cascode amplifiers of the HBT and NMOS combinations is presented. Ultimately, HBT with body-floating NMOS structure can provide medium gain with higher linear output power. The other new structure PA is three transistors stacked-amplifier, which is two stacked HBT and cascoded with a body-floating NMOS, leading to decent gain, larger P_{sat}, and OP1dB.

A SAW-less high-isolation fully-integrated 23.5–36.2-GHz FDD TX-RX front-end module, containing a DUX, PA, and differential LNA, is demonstrated on a single Si substrate to facilitate the development of system with DUX on a chip (SoC). The isolation between PA output and LNA input is better than 42 dB in 13 GHz bandwidth (BW). For the RX path, LNA has better than 19 dB gain with the minimum 13.8 dB noise figure (NF) at 28 GHz. On the TX path, PA provides about 12.9 dB gain with better than 12.5 dBm P_{sat} in BW. TX signals leakage through Si-substrate is also considered and suppressed,

using PA with deep-N-well structure and p-type/n-type grounding guard ring. This module only occupies 2.1-mm^2 without dc and RF pads.

In order to overcome the antenna imbalance issue of electrical balanced DUXs (EBDs) and high power consumption issue of active DUXs, a new power-efficient 28 GHz TX-RX front-end module with more than 60-dB TX-RX isolation, including DUX, PA, and LNA, is designed, which combines the advantage of passive microwave circuit and active cancellation technique to achieve higher TX-RX isolation, low NF, and being power-efficient. The cancellation path consists of a variable gain amplifier (VGA) and reflection-type phase-shifter (RT-PS) to control the feedback signal amplitude and phase. A detailed analysis and design methodology are also proposed. This narrow-band TX-RX module also occupies small area with 2-mm^2 without dc and RF pads.

DEDICATION

To my parents

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1. INTRODUCTION

In the past couple of decades, the wireless communication industry has grown up remarkably in order to satisfy the needs of people. 2nd, 3rd, and 4th generation wireless communications (2G, 3G, and 4G), global positioning system (GPS), wireless local area network (Wi-Fi), Bluetooth, near field communication (NFC) have become the essential part of people's lives. Most of these applications happen in the industrial, scientific and medical frequency band (ISM-band). Due to the explosive number of applications, developing communication systems suffers from overlapping and shortage of available frequencies. The microwave and millimeter-wave frequencies are suitable for both military and commercial applications. Recently, some of the microwave and millimeter-wave frequencies, especially those in K-band (18-26.5 GHz), Ka-band (26.5-40 GHz), V-band (50-75 GHz), and W-band (75-110 GHz) have been utilized for commercial usage such as 5th generation wireless communications and car radar systems. Use of proper microwave and millimeter-wave frequencies can overcome the frequency shortage and overlapping dilemmas for next generation wireless communication systems [1].

Designing a high performance radio frequency integrated circuits (RFIC) and monolithic microwave integrated circuits (MMICs) are still a technical challenge. Silicon germanium (SiGe) Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) is the technology of choice for millimeter-wave RFICs due to its various merits. A SiGe bipolar-junction-transistor (BJT) is an advanced technology from Si BJT. The main difference between SiGe BJT and Si BJT is the material of base of BJT. By using SiGe for base, the speed, gain, RF and 1/f noises, base resistance and operating frequency of the BJT are improved. In comparison with CMOS, although the BiCMOS process consumes more time and cost, it has a benefit of having available BJT and CMOS on the same sub-

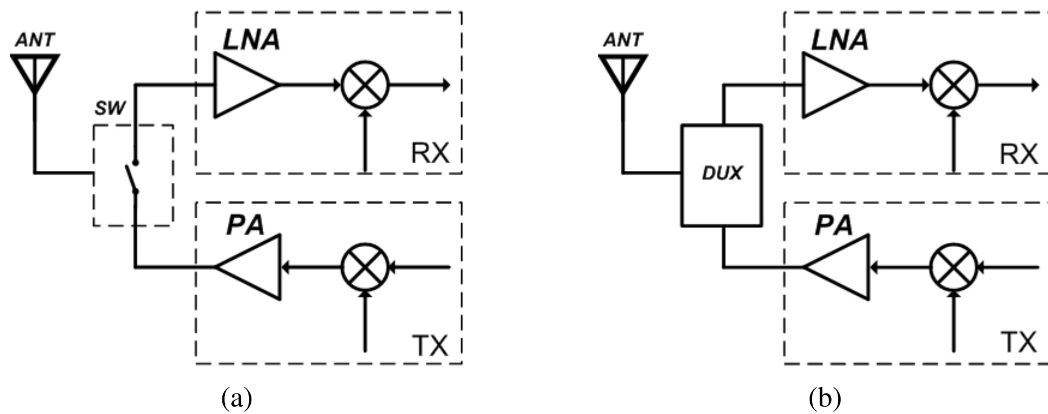

Figure 1.1: RF wireless system TX-RX architecture (a) TDD scheme and (b) FDD scheme.

strate. The two types of transistors enable enhanced system performances, integration, and functionalities. The BJT has higher speed and better high-frequency characteristics ($f_T \approx 200$ GHz for 0.18μm BJT) than CMOS. Also, it provides a larger current capability, which means more output power, and higher transconductance (g_m) and lower RF noise. So, the BJT is considered better for active circuits such as power amplifier (PA), low noise amplifier (LNA), and gain-stage amplifier in RFIC systems. While, CMOS has lower cost and can be used more than BJT for passive or digital circuits such as an attenuator, phase shifter, switch, DC control circuit, etc., since CMOS has lower static power dissipation without DC current at gate, and higher yield capability.

1.1 The Architectures of Wireless Communication Front-Ends

A wireless transceiver contains various circuit blocks such as antenna, LNA, PA, mixer, synthesizer, and analog to digital converter (ADC). Especially, the building block of antenna, LNA, PA is also known as RF front-end. Fig. 1.1 shows the two typical RF front-end scheme: (1) Time division duplex (TDD) and (2) Frequency division duplex (FDD). The most well-known RF system operated in TDD scheme is the 2nd generation

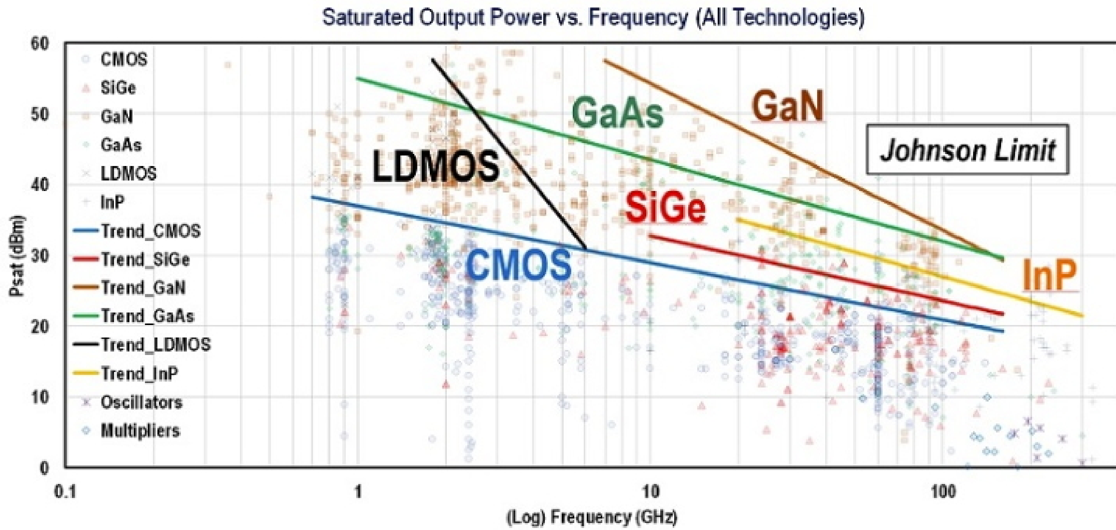

Figure 1.2: Current developement of PAs. Reprinted from [2].

wireless communication (2G). In TDD system, a RF switch (SW) functions to separate transmitting and receiving signals. In FDD system, a duplexer (DUX) also plays a role to separate transmitting and receiving signals. Well-known FDD systems are Wideband Code Division Multiple Access (WCDMA). Typically, TDD system is easier to be integrated with others circuits than FDD system. However, FDD system has faster data rates. DUX is a design bottleneck in RFIC and MMIC design.

1.2 Current Literature Survey

In this section, we will study and survey the development of current state-of-the-art of PA and DUX. A high performance PA should have large output power, high linearity, power-efficient. In this dissertation, we mainly focus on the Si-based PA. An ideal DUX should have high isolation between TX and RX port. Besides, it should have low insertion loss for TX and RX paths and good matches for all ports.

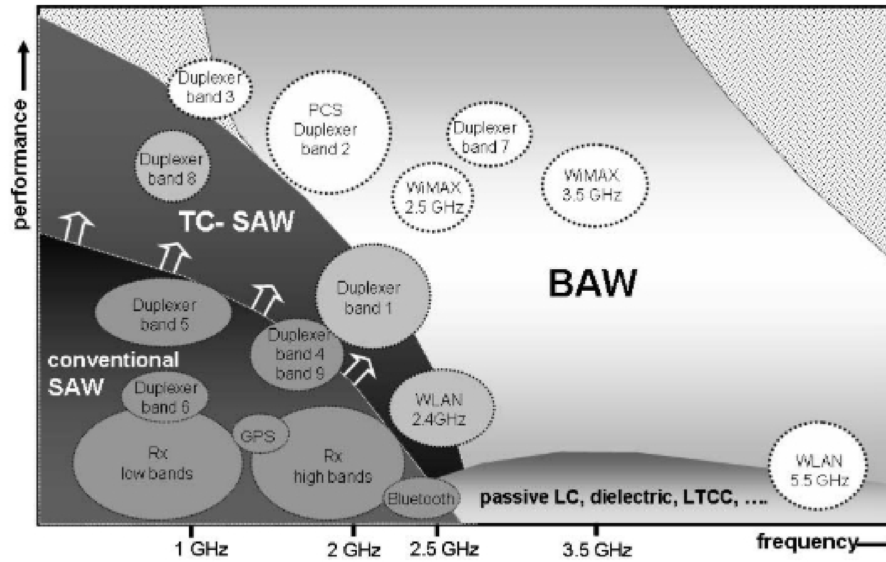

Figure 1.3: Current development of SAW and BAW filters. Reprinted from [4].

1.2.1 Current Development of Power Amplifiers

Fig. 1.2 reports the current PA status of development [2]. We can see that PAs designed on GaN, InP, and GaAs obviously can operate at higher frequency and have large output power. However, it is very hard to integrate with digital and analog circuit since most of digital and analog are designed on Si substrates. Hence Si-based PAs have advantage to facilitate the development system on a chip (SoC) and have lower cost. SiGe process which is also known as BiCMOS process is a between CMOS process and non-Si (III-V) process. BiCMOS process can provide high performance HBT and CMOS at the same time. Generally, two main strategies can be identified to improve PA performance: (1) improve active devices performance (2) reduce the insertion loss from internal passive networks.

First, there are several well-known ways to boost PA gain or extend PA's frequency response. In [3], it proposes the peaking technique using inductor and transformer to enhance CMOS frequency response. Others such as negative miller capacitance or active

negative feedback can also enhance PA gain in millimeter wave ranges.

Second, for passive devices, most of papers reports using baluns to efficiently transformer the impedance between PA output and load impedance and combine the RF power from each PA cell. LC-Lumped Wilkinson power combiner can combine RF power and filter out the second harmonic to improve PA efficiency and reduce inter-modulation distortion. It is noted that some PA output matching networks are designed to provide a short-circuit to ground at second harmonic frequency to improve power efficiency or improve adjacent channel leakage ratio (ACLR).

In this dissertation, our main contributions are using both advantages of HBT and NMOS to extend PA performances.

1.2.2 Current Development of Quasi-Circulators and Dulexpers

Currently, most of FDD wireless communication systems adopt surface acoustic wave (SAW) or bulk acoustic wave (BAW) technology to realize the DUX, which has low insertion loss, high TX-RX isolation, and good out-band rejection. However, SAW and BAW are very hard to operate at frequencies higher than 10 GHz [4] and not fully-integrated, needed to mount on print circuit board (PCB). Generally, mm-wave DUXs can be designed using ferrite circulators, active devices, or passive components. DUXs based on ferrite circulators are narrow-band, bulky, and difficult to integrate with on-chip integrated circuits. Active-based DUXs have inherent non-linearity and high power consumption needed to achieve sufficient linearity for handling PA large signals [5],[6]. Besides, active devices also generate noise, leading to degrading NF, at least 3-4 dB in mm-wave ranges. Passive-based DUXs are perhaps the best candidate considering trade-off in integration, size, power consumption, and linearity.

There are three ports in a DUX: (1) TX port, (2) ANT port, and (3) RX port. In this dissertation, we assume TX port is port 1, ANT and RX ports are port 2 and 3,

respectively, for the DUX. The scattering matrix of an ideal DUX transformer can be expressed as

$$S = \begin{bmatrix} S_{11} & S_{12} & S_{13} \\ S_{21} & S_{22} & S_{23} \\ S_{31} & S_{32} & S_{33} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \tag{1.1}$$

Assuming all ports are matched, S_{ii} is 0. One of the most important parameters of DUX is the isolation between TX and RX port (S_{31}). High TX-RX isolation can prevent PA output signal from desensitizing LNA input. When TX and RX port are totally isolated, S_{31} equals 0. Practically, isolation between TX and RX ports (S_{31}) is around 40$\sim$50 dB. Others important parameters are insertion loss on the TX and RX paths, defined by S_{21} and S_{32}, respectively. When S_{21} and S_{32} are 1 (0-dB), the DUX is lossless. S_{12}, S_{13}, and S_{23} mean the reversed insertion loss or isolation, which should also be 0 in an ideal DUX.

1.2.3 Thesis Organization

This dissertation is organized into 7 chapters. Chapter 2 gives a detail study about cascode amplifiers performance with the combinations of NMOS and HBT transistor. Chapter 3 proposes a new cascode amplifier architecture, which adopts the advantages of NMOS and HBT with body-floating technique to extend maximum saturated power and output linearity with reasonable gain. Chapter 4 reports a BiCMOS stacked-amplifier PA structure, further combining the technique with stacked amplifier technique with BiCMOS process to achieve better PA performance. Chapter 5 demonstrates and designs an ultra-wideband mm-wave passive balanced DUX with better than 40-dB isolation between TX and RX port across dc to 60 GHz. Chapter 6 reports a wide-band mm-wave fully-integrated FDD TX-RX module, including internal DUX, PA, and LNA. Chapter 7 demonstrate a 28 GHz fully-integrated FDD TX-RX module, adopting passive microwave

circuit and active cancellation path to create higher isolation, maintain low NF and being power efficient at the same time. Finally, in Chapter 8, the contributions of this dissertation are summarized.

2. ON THE INVESTIGATION OF CASCODE POWER AMPLIFIERS FOR 5G APPLICATIONS*

2.1 Introduction

PAs implementing cascode topology are attractive and widely used due to their good input-output isolation, gain, bandwidth, and stability. Cascode PAs consist of two transistors. Most reported cascode PAs solely use HBT [8] or NMOS [9] for the two transistors. The first transistor (the input transistor) is a common-emitter (CE) or common-source (CS) transistor, which primarily dominates the transconductance in the whole cascode amplifier. The second transistor (the output transistor) is a common-base (CB) or common-gate (CG) transistor, provides additional reversed isolation and handles large signal swings amplified by the first transistor. Cascode PAs implementing different combinations of HBT and NMOS that exploit individually unique advantages of these transistors for improved performance have not been reported.

In this dissertation, we investigate the performance of cascode PAs employing all possible combinations of HBT and NMOS including NMOS-NMOS, HBT-HBT, HBT-NMOS, HBT-NMOS with deep-nwell (DNW) and body-floating resistor. DNW and body-floating resistor [10] are used for the NMOS in one cascode PA to reduce the NMOS parasitics and provide more headroom for the voltage swing. By exploiting the distinctive advantages of HBT, NMOS, and DNW, a high-performance 28 GHz PA for 5G applications can be achieved.

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2.2 HBT and NMOS DC Characteristics and Maximum Available Gain (MAG)

Each HBT in the designed PAs consists of four transistor constituents, each having 0.13-μm emitter width and 10-μm emitter length. Each NMOS transistor is also composed of four transistor constituents, each having 0.18-μm length and 4.5-μm width with 12 fingers. Although longer NMOS gate lengths have higher breakdown voltage, larger lengths also cause more parasitics. For simplicity without loss of generality, only the minimum gate length of 0.18-μm is discussed.

Fig. 2.1 shows the HBT and NMOS I-V characteristics. The employed HBT can not be biased higher than 1.8 V, while the employed NMOS has a breakdown voltage larger than 5 V, leading to more headroom for voltage swing. Based on the load-line theory, NMOS can provide 17-dBm linear power, while HBT can only produce 14-dBm linear power. Therefore, Fig. 1 implies that NMOS has more headroom for drain voltage swing to function as the output transistor in cascode amplifiers. Additionally, Fig. 2.1 also shows that HBT has larger transconductance than NMOS.

Fig. 2.2 shows the MAG of the CE HBT and CS NMOS with 50-mA collector and drain currents. HBT provides a higher power gain and has a larger f_{max} than NMOS. Specifically at 28 GHz, HBT has 17.2-dB MAG, while NMOS only provides 9.9-dB gain. Consequently, HBT is better for the first transistor in cascode amplifiers.

2.3 Analysis and Results of Four HBT and NMOS Combinations

Fig. 2.3 shows four possible arrangements of HBT and NMOS devices in cascode amplifiers. Fig. 2.3a shows a PA consisting of two identical NMOS transistors. Fig. 2.3b shows a PA consisting of two identical SiGe HBT devices. The NMOS-HBT combination is not considered since NMOS provides less transconductance and HBT has worse headroom for output voltage swing, leading to the worst gain, output power, and linearity among all combinations.

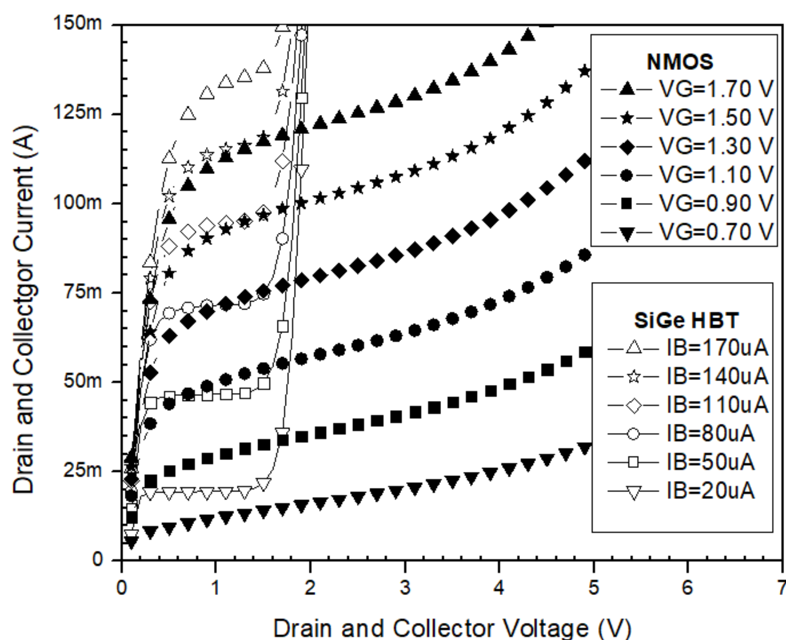

Figure 2.1: I-V characteristics of HBT and NMOS. Reprinted with permission from [33].

The dc current of the drain or collector in all considered transistor combinations is set at 50 mA to provide roughly 15-dBm output power. For high linearity and PAE, all combinations are biased in class-AB region. As can be inferred from Fig. 2.1, the NMOS-NMOS structure needs the highest bias voltage, around 4-5 V, for V_{DD}. The HBT-HBT combination has the lowest bias voltage of 2.5 V. The HBT-NMOS has the medium voltage of 3.5 V.

In order to meet the condition of unconditional stability, all PAs implement a 25-pH degenerative inductor. In addition, the quality factor of all inductors used in the matching networks, as shown in Fig. 2.3, is assumed to be 15 for practical considerations. All input matching networks are designed to have input return loss better than 15 dB at 28 GHz. All output matching networks are optimized based on load-pull resulting in maximum power. Cadence [42] is used for all simulations as well as extracting the post-layout transistor parasitics along with the process design kit (PDK) of TowerJazz SBC18H3

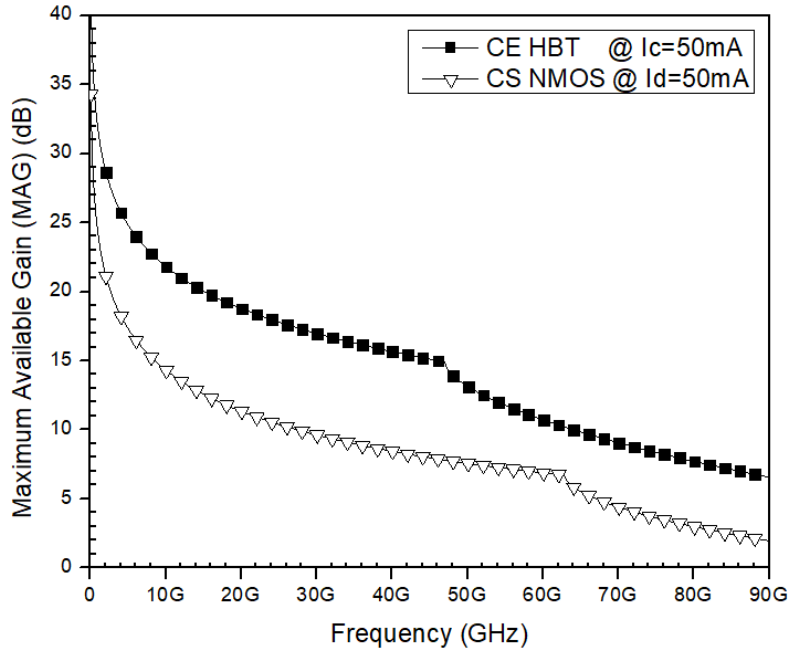

Figure 2.2: MAG of HBT CE and NMOS CS amplifier versus frequency. Reprinted with permission from [33].

0.18-μm BiCMOS process [13].

Figs. 2.4 and 2.5 show the simulated power gain and PAE at 28 GHz for all PAs shown in Fig. 2.3. The PA shown in Fig. 2.3a (Case A) provides 18.5-dBm Psat and 14-dBm OP1dB. However, it has only 9.1-dB gain and 14.4 % maximum PAE due to the NMOS' low transconductance as shown in Figs. 2.4 and 2.5, respectively.

The PA shown in Fig. 2.3b (Case B) implements HBTs having large transconductance and over 150-GHz f_T. It provides 20.1-dB power gain and almost 30 % maximum PAE. Nonetheless, the small headroom for voltage swing from the HBTs results in only 17.6-dBm P_{sat} and 14.9-dBm OP1dB as shown in Fig. 2.4.

The PA in Fig. 2.3c (Case C) is realized with both NMOS and HBT. The HBT provides good transconductance and the NMOS handles large voltage swing. This PA has better P_{sat} of 18.6-dBm and OP1dB of 15.1-dBm than Case B, as seen in Fig. 2.4. Com-

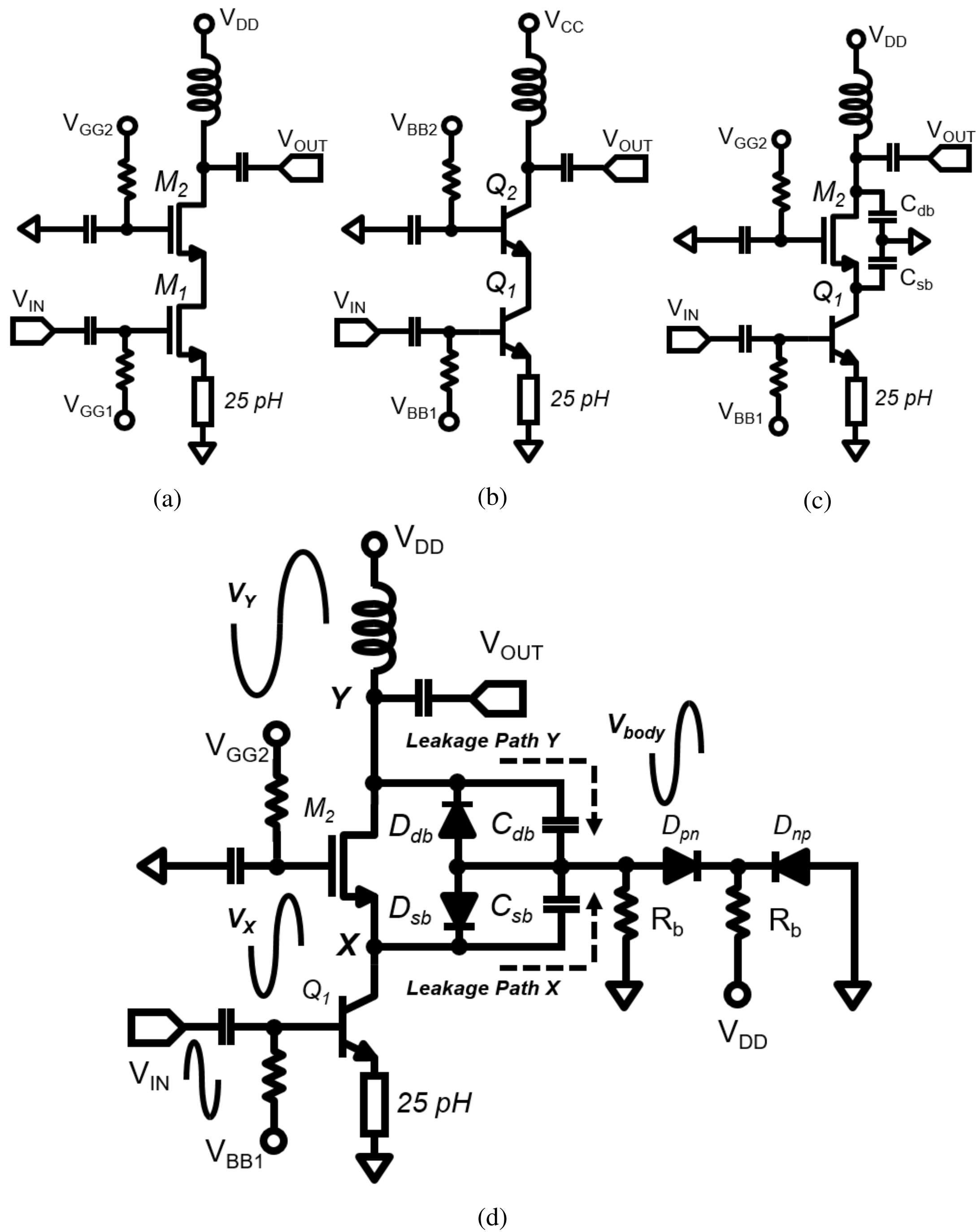

Figure 2.3: Simplified cascode amplifier schematic for (a) Case A: NMOS-NMOS (b) Case B: HBT-HBT (c) Case C: HBT-NMOS (d) Case D: HBT-NMOS with DNW and body-floating resistor (R_b). Reprinted with permission from [33].

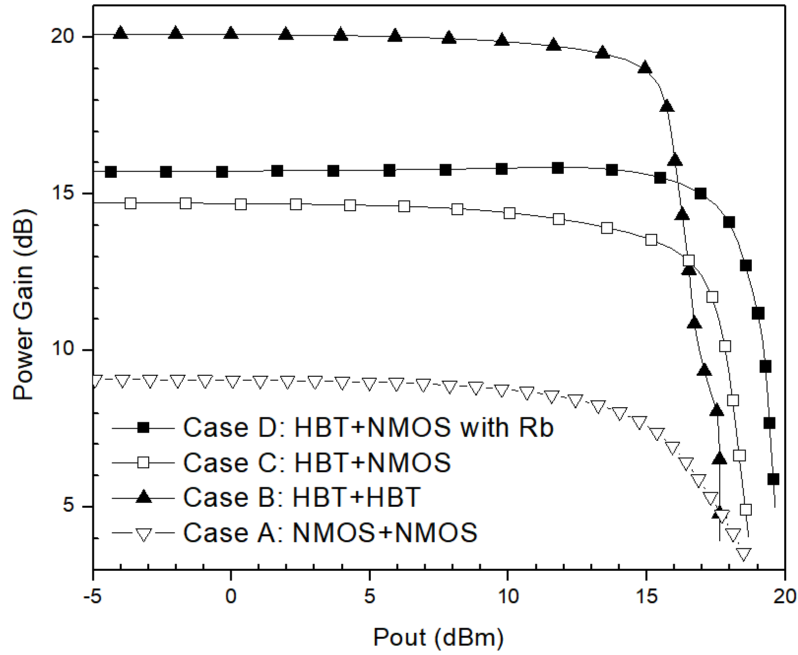

Figure 2.4: Power gain for Case A, B, C, and D versus output power at 28 GHz. Reprinted with permission from [33].

pared with Case A, the gain and PAE improve from 9.1-dB to 14.7-dB (61.5 %) and from 14.4 % to 18.5 % (28.5 %), respectively. It should be noted that, at low frequencies, Case B and Case C should have the same gain [11], which is different at high frequencies. At high frequencies, the NMOS (M2) parasitics, such as C_{sb} and C_{db}, cause more signal leakages, primarily resulting in the gain difference between Case B and Case C. The PA in Fig. 2.3d (Case D) is also realized with HBT and NMOS as in Case C, but with the body of the NMOS floated for improved performance. A body-floating NMOS provides two advantages. Firstly, in small swings, the large resistance (R_b= 4k-Ohm) maintains high impedance helping suppress the leakage through paths X and Y, hence improving the gain from 14.7-dB to 15.7-dB (6.8 %). Secondly, under large signal operations, the body-floating resistor (R_b) also improves the NMOS power handling ability. Without Rb, when the signal intensity increases, large voltage swings at node X and Y could become negative and turn on the p-n diodes between the source-substrate (D_{sb}) and drain-substrate

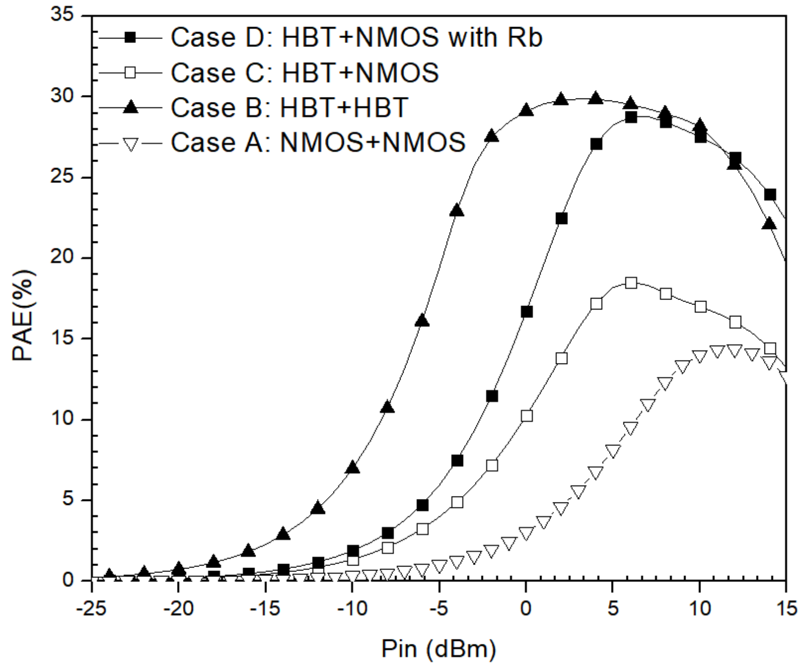

Figure 2.5: PAE for Case A, B, C, and D versus input power at 28 GHz. Reprinted with permission from [33].

(D_{db}), leading to signal leakage. With R_b, large resistance could remain the same when the voltage swings are negative at node X and Y. Furthermore, the simulated transient signals also suggest that the voltage swings at the drain (V_Y), source (V_X), and body (V_{body}) have almost the same phase, which can relax large voltage differences across the p-n junctions as depicted in Fig. 2.3d.

As seen in Fig. 2.4, Case D has the largest P_{sat} of 19.6-dBm, OP1dB of 17.5-dBm, with 15.7-dB power gain. Besides, Case D has almost the same PAE with Case-B as shown in Fig. 2.5. Compared with Case B and Case D, P_{sat} and OP1dB improve from 17.6-dBm to 19.6-dBm (11.4 %) and from 14.9-dBm to 17.5-dBm (17.4 %), respectively. Table 2.1 summaries the performances for Case A to Case D, which demonstrate that a combination of HBT, NMOS, and body-floating effectively extends the output power and linearity, with Case D representing the best performance for 5G applications.

Table 2.1: Performance Summary of Case A, B, C, and D. Reprinted with permission from [33].

	Case A	Case B	Case C	Case D
Power Gain (dB)	9.1	20.1	14.7	15.7
P_{sat} (dBm)	18.5	17.6	18.6	19.6
OP1dB(dBm)	14.0	14.9	15.1	17.5
Max PAE (%)	14.4	29.9	18.5	28.8
V_{DD} or V_{CC}(V)	4.3	2.5	3.5	3.5

2.4 Conclusion

This dissertation analyzes four different combinations of HBT and NMOS for cascode PAs. The best-performance PA implements a SiGe HBT for the input transistor, which dominantly provides large transconductance to amplify the input signals, and a NMOS with body-floating for the output transistor, which has reduced parasitics and better power-handling ability. This PA attains 15.7-dB gain, 19.6-dBm P_{sat}, 17.5-dBm OP1dB, and 28.8 % maximum PAE at 28 GHz for 5G applications. This investigation exploits the advantages and flexibility of BiCMOS processes to improve PA linearity and P_{sat}, benefiting Si-based PAs design for 5G applications.

3. DESIGN OF A WIDE-BAND POWER AMPLIFIER IN Ku AND K BANDS*

3.1 Introduction

Wide-band devices in Ku-band (12-18 GHz) and K-band (18-27 GHz) have received compelling attention for high-data-rate communications and high-resolution sensing. Especially, devices operating around 24 GHz are doubly attractive for communications due to their unlicensed operations. One of the most important building blocks in RF systems is power amplifier (PA). Various PAs have been developed in the Ku- and K-band on different processes like GaAs, InP, and Silicon (Si). Although PAs using GaAs or InP process could have better power handling and efficiency than those realized on Si, it is very hard to integrate an entire RF system on the same substrate for GaAs or InP, making it difficult to design single-chip RF systems. On the other hand, PAs on Si, together with other Si-based RF components, enable realization of single-chip RF systems.

Cascode amplifiers are a popular architecture due to their good input-output isolation, gain, bandwidth, and stability. Typical cascode amplifiers in CMOS or BiCMOS process employ two cascode NMOS transistors or HBTs, respectively. Particularly, in standard CMOS processes, the two transistors must be NMOS since only NMOS transistors are available in the process. In BiCMOS processes, however, both NMOS transistors and HBT are available, allowing use of either NMOS or HBT, or a combination of them, for the two transistors for proper circuit design and/or possible optimization of circuit's performance. In general, HBTs have higher f_T and f_{MAX}, and larger transconductance than NMOS transistors, leading to higher gain, especially in the high frequency region of suitable operating frequencies. Specifically, in the Tower-Jazz 0.18-μm SiGe BiCMOS

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process [1] that we use for the PA reported in this dissertation, the HBTs have smaller voltage swing than the NMOS transistors. Moreover, NMOS with the body-floated by a resistor [2], [3] can improve the voltage swing, and hence linearity, besides having less parasitic capacitances between the source and bulk (C_{sb}) and between the drain and bulk (C_{db}) for enhanced gain at high frequencies. For PA design, transistors having high gain and large voltage swing for enhanced linearity are desired, hence making a combination of both HBT and body-floating NMOS attractive for cascode PAs. In this dissertation, we report a new 0.18-μm SiGe BiCMOS PA implementing both HBT and NMOS to exploit the advantages of these devices together for attaining decent gain, output power, PAE, and OP1dB. The PA achieves 18.5-20.8 dBm P_{sat}, 16.6 $\pm$ 1.5 dBm OP1dB, 13.5-23 % maximum PAE, and 19.5 $\pm$ 1.5 dB gain measured across 16.5-25.5 GHz. At 24 GHz, the PA has measured P_{sat}, OP1dB, maximum PAE, and gain of 20.8 dBm, 18.1 dBm, 23%, and 20 dB, respectively.

3.2 Design and Analysis

Fig. 3.1 shows the schematic of the PA consisting of a drive amplifier in the first stage and two identical main amplifiers in the second stage - all in a cascode topology. The PA was designed and fabricated using the Tower-Jazz 0.18-μm SBC18H3 process and, as shown in Fig. 3.2, occupies a 1.68$\times$0.76 mm^2 die without the RF and dc pads. The two main amplifiers in the PA are integrated through lumped-element Wilkinson power divider and combiner, each simulating a low-pass filtering response to suppress the harmonics for improved PAE [4]. All the transmission lines and interconnects are realized with coplanar waveguides on the thickest topmost metal layer for minimum conductor loss. The transmission lines, interconnects, and inductors are designed and simulated using the HyperLynx 3D EM simulator [5]. Cadence [6] is used for circuit simulations as well as extracting the parasitic elements produced by the layout.

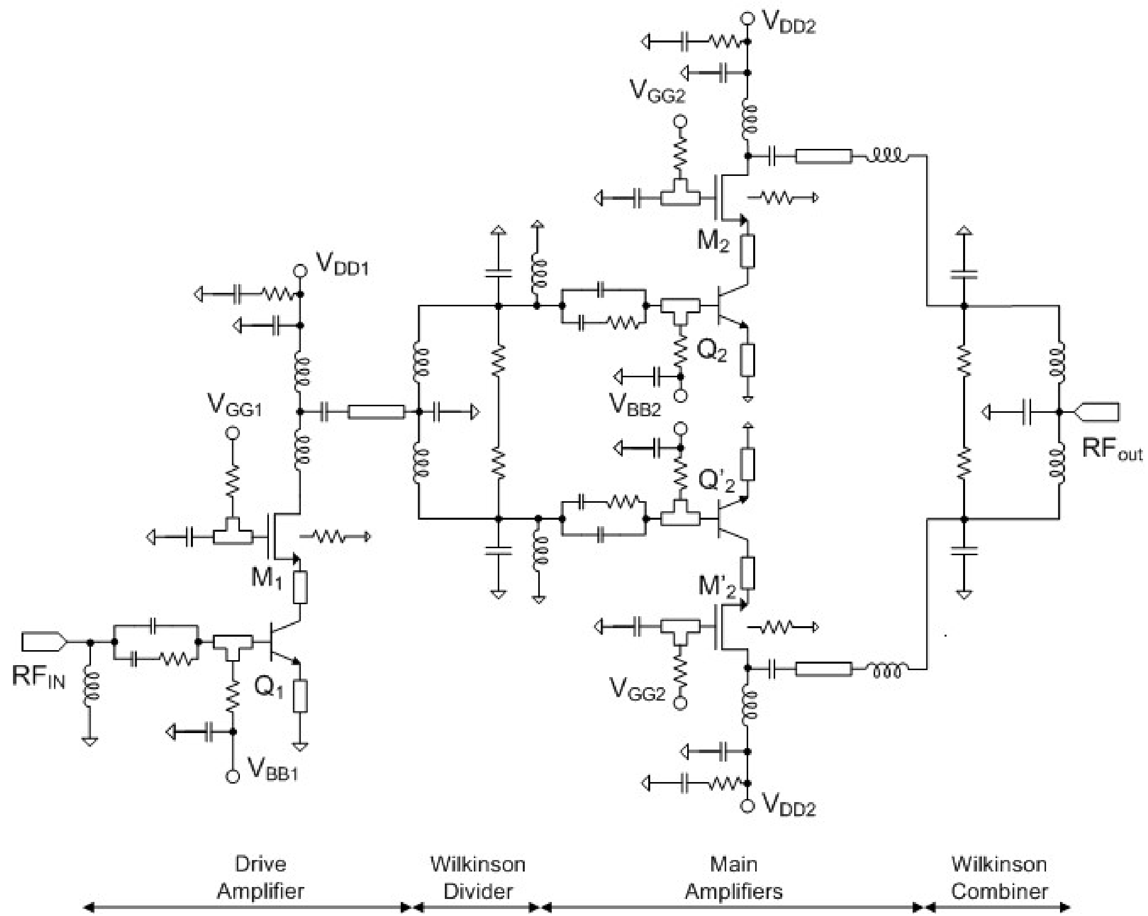


Figure 3.1: Schematic of the proposed PA. Reprinted with permission from [34].

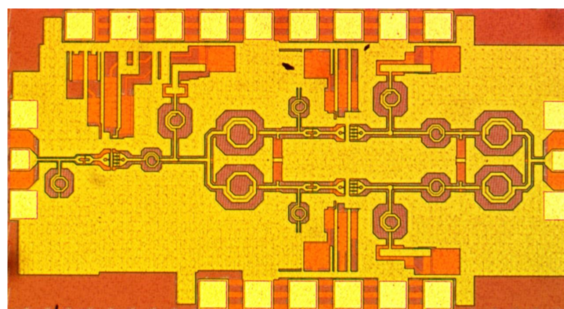


Figure 3.2: Photograph of the fabricated PA. Reprinted with permission from [34].

A typical cascode amplifier implements both NMOS transistors or both HBTs for the two transistors. The first transistor (input transistor) is normally a common-source (CS)

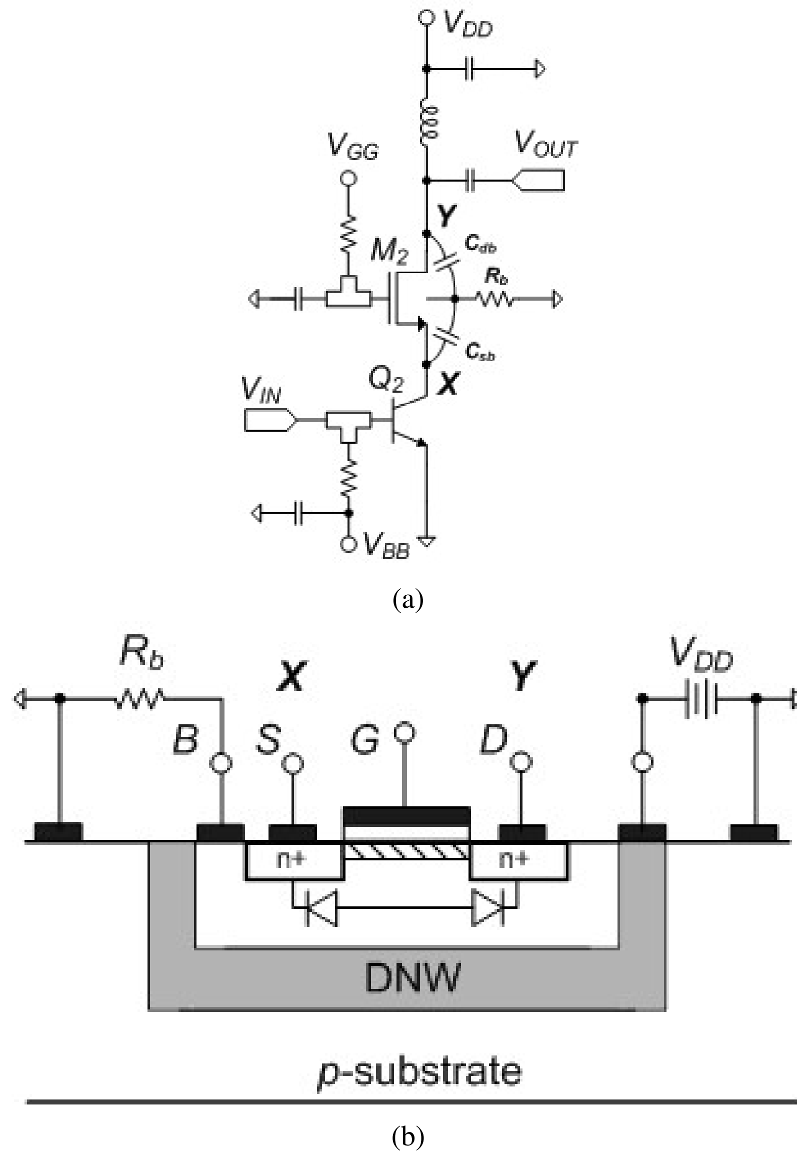


Figure 3.3: (a) Schematic of the main cascode amplifier with HBT-NMOS (excluding some components like stability resistor for simplicity). (b) Cross-section of a DNW NMOS with body floated by R_b. Reprinted with permission from [34].

or common-emitter (CE) type, while the second one (cascode transistor) is normally a common-gate (CG) or common-base (CB) type. The first transistor amplifies the input signal through its transconductance that is fed into the second transistor, which needs to handle the large voltage signal amplified by the first transistor. In our design, however,

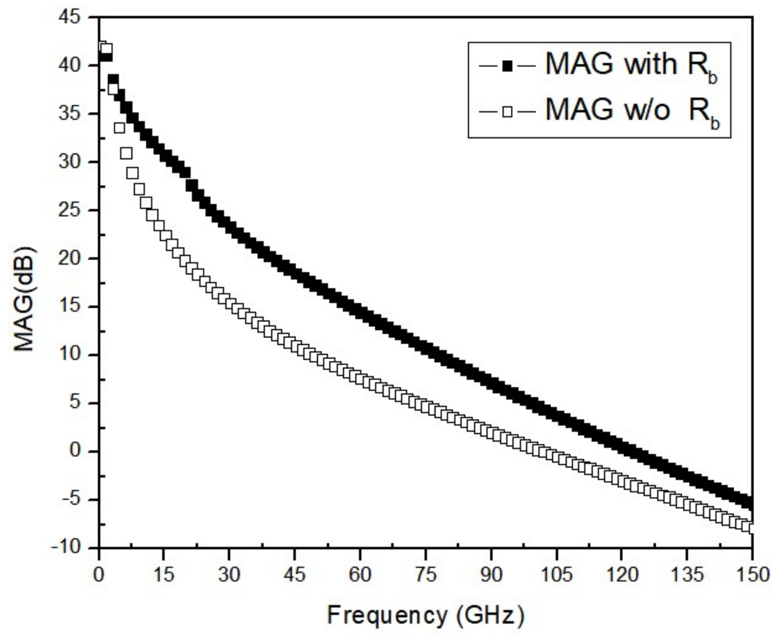
we use both NMOS and HBT to take advantage of the larger voltage swing and higher transconductance of the NMOS and HBT available in the employed process, respectively, as mentioned earlier. Fig. 3.3a shows the schematic of one of the two identical main amplifiers in the second stage, which is a cascode amplifier implementing both CE HBT and CG NMOS devices. While the NMOS device in the employed process can handle large output voltage swings, its (f_T) is lower than that of the HBT, hence leading to degraded gain at high frequencies. To resolve this issue, a deep-n-well (DNW) NMOS with a body-floating resistor (R_b) is implemented to reduce C_{sb} and C_{db} to enhance the NMOS gain under small signal operation and hence the maximum available power gain (MAG) of the main amplifier. The body-floating resistor can also enhance the large-signal operation of the NMOS as can be inferred from Fig. 3.3b, which shows a cross sectional view of the physical structure of the DNW NMOS transistor with the body floated by R_b. The resistor R_b indeed helps reduce the signal leakage from the source to body and drain to body that occurs through the parasitic p-n junctions when the signal's voltage swing gets larger. Fig. 3.4a demonstrates the enhancement of the MAG of the main amplifier when the NMOS body is floated with R_b, showing that the MAG is actually improved by 44 % at 24 GHz. Fig. 3.4b shows the simulated power gain and PAE of the main amplifier as a function of the input power with and without the NMOS body being floated at 24 GHz, demonstrating that using a body-floating resistor can improve 11 % of the power gain (from 9 dB to 10 dB), 100 % of PAE (from 13% to 26% at 13 dBm input power), and 21 % of OP1dB (from 14 dBm to 17 dBm). These results show that a cascode PA employing both HBT and body-floating NMOS devices could provide high gain and good linearity as expected and mentioned earlier.

Each input transistor (Q2 and Q2') in the main amplifiers, as shown in Fig. 3.1, consists of four constituent transistors, each having 0.13-μm emitter width and 10-μm emitter length designed mainly for optimum MAG. The cascode transistors (M2 and M2'), each

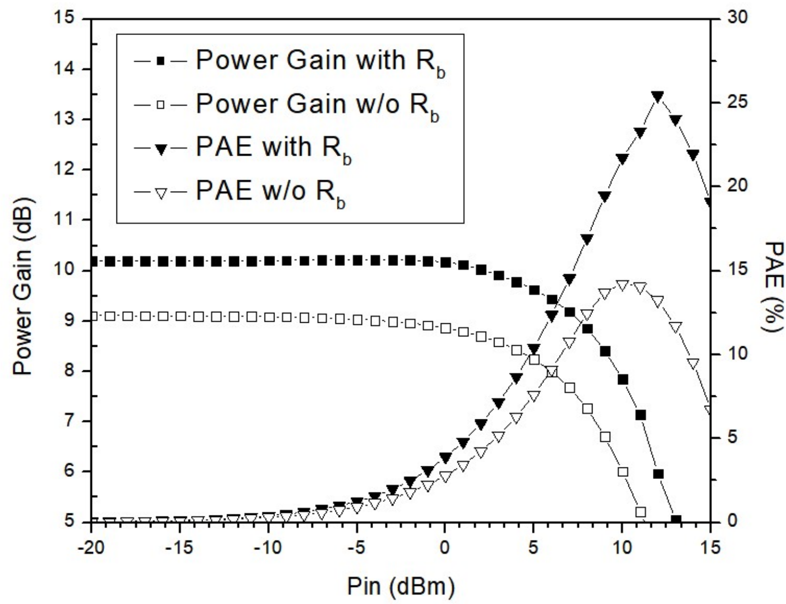
combining four transistors, are selected to have 12 fingers with a unit finger width of 4.5 μm through load-pull simulations for high output power. A 4K-Ohm resistor (R_b) is used for the body-floating resistor. It should be mentioned here that the large HBT used in the PA would degrade the reversed gain and stability due to the resultant high parasitic capacitances between the base and collector (C_{bc}) of the HBT, which should be taken into consideration in the design. In the high-frequency region of the designed PA's operating frequency range, however, the stability is well maintained because of the decay of the loop gain resulting from the lower MAG of the main amplifiers and the increased parasitic capacitances. At low frequencies, a combination of series RC and shunt C is utilized at the HBT's base to improve the stability. The input transistor (Q1) of the drive amplifier as shown in Fig. 3.1 consists of four transistors with 5-μm emitter length. The cascode transistor (M1) has 12 fingers with 2.5-μm width each. M1 also adopts the body-floating configuration with a 4K-Ohm resistor to improve the gain, linearity and PAE.

3.3 Measured Results

The designed PA was measured on-chip with a vector network analyzer and probe station. The drain voltage (V_{DD2}) of the main amplifiers is set to 3.45 V, while that (V_{DD1}) of the drive amplifier is 3.35 V. The dc currents of the first and second stage are 30 and 60 mA, respectively. Fig. 3.5a shows the measured and simulated small-signal S-parameters of the PA, which match very well with each other. The measured gain (S_{21}) is 20 dB gain at 24 GHz and has less than 3-dB variation across 16.5- 25.5 GHz. The measured input (S_{11}) and output (S_{22}) return losses are better than 10 dB from 20 to 28 GHz and 8 dB from 19.5 to 27.5 GHz, respectively. Fig. 3.5b shows the measured and simulated K factor of the whole PA along with the simulated K factors of the drive amplifier and one amplifier of the main amplifier, demonstrating their good stability. The PA's measured K factor is larger than 35 from DC to 50 GHz. Fig. 3.6a shows the measured and simulated

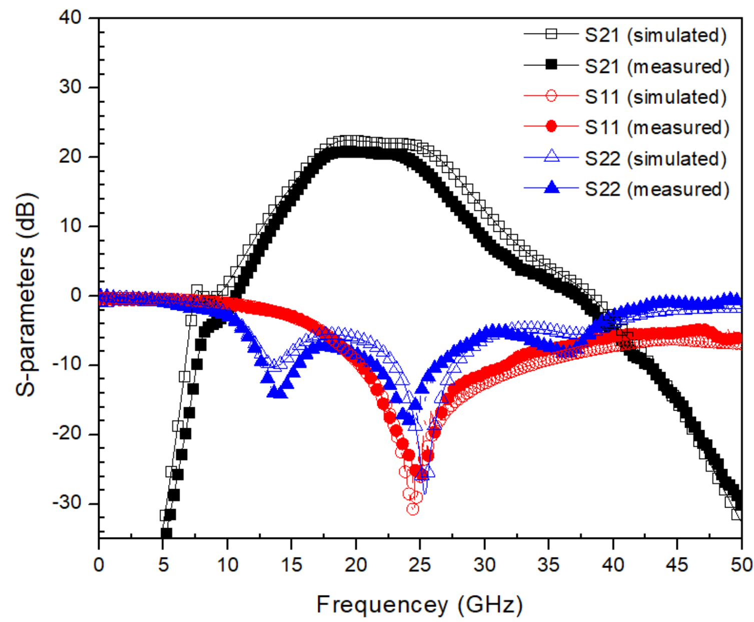


(a)



(b)

Figure 3.4: (a) Main amplifier's MAG with and without the NMOS body-floating Rb. (b) Main amplifier's power gain and PAE at 24 GHz with and without the NMOS body-floating Rb. Reprinted with permission from [34].



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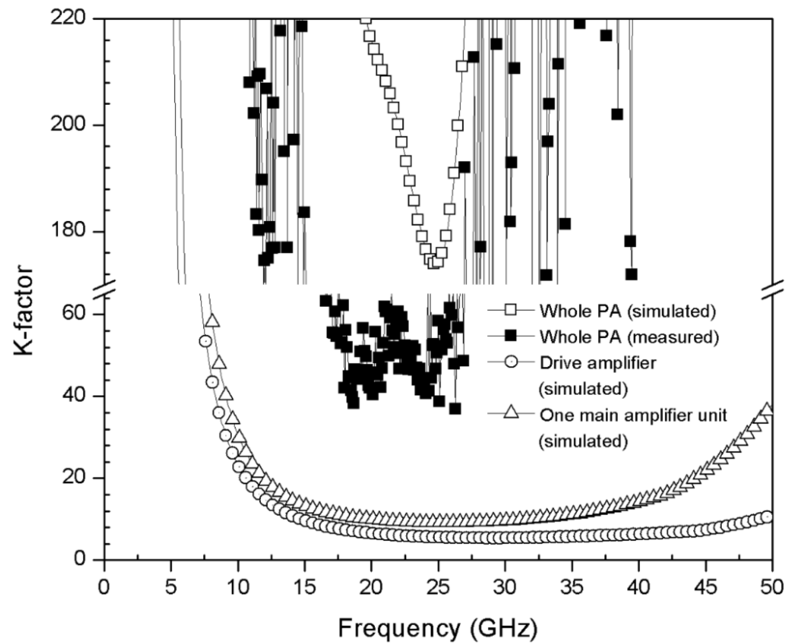
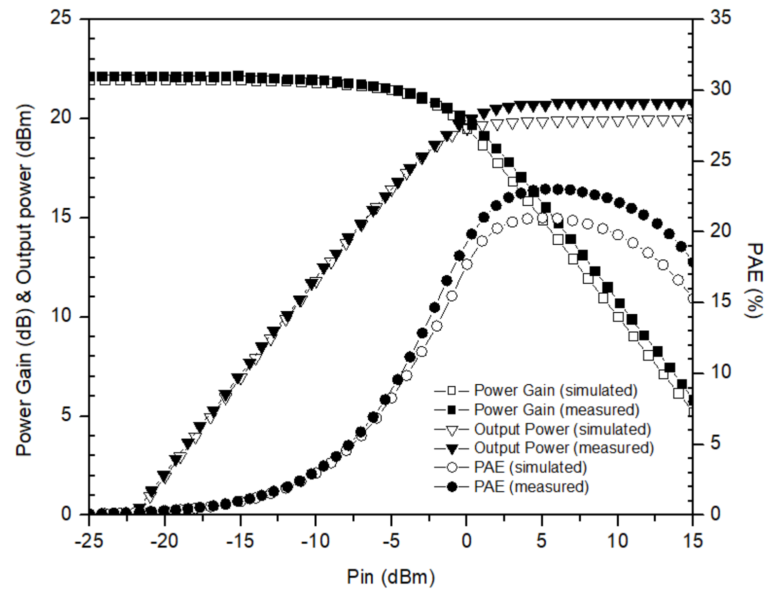
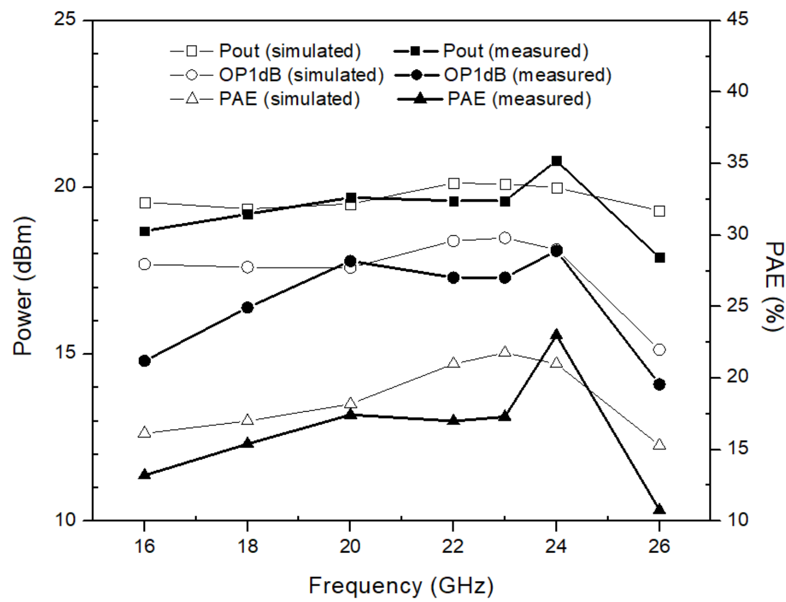


(b)

Figure 3.5: Simulated and measured performance of the PA: (a) S-parameters, (b) stability. Reprinted with permission from [34].



(a)



(b)

Figure 3.6: Simulated and measured performance of the PA: (a) power gain, output power and PAE at 24 GHz, and (b) Psat, OP1dB and PAE. Reprinted with permission from [34].

results of the power gain, output power and PAE with respect to the input power at 24 GHz. At 24 GHz, the measured P_{sat}, OP1dB and maximum PAE are 20.8, 18 dBm and

23%, respectively. Fig. 3.6b displays the measured and simulated performance of P_{sat}, OP1dB and PAE as a function of frequency. The measured Psat, OP1dB, and PAE are 18.5-20.8 dBm, 15.1-18.1 dBm, and 13.5-23 % across 16.5-25.5 GHz, respectively. Table 3.1 summarizes and compares the measured performance of the PA with those published K-band PAs on 0.18-μm CMOS and BiCMOS processes [4], [7]-[9]. At 24 GHz, the designed PA has the highest OP1dB of 18.1 dBm and Psat of 20.8 dBm. Compared with [4] fabricated in the same process, which employed all HBTs, this PA has OP1dB improved by about 3 dBm on the average over 16.5-25.5 GHz due to the use of the NMOS with body-floating technique. The PA in [7] only operates at the single frequency of 24 GHz and, while it has higher PAE, it provides lower gain, P_{sat} and OP1dB. It is noted that the PAs in [8] and [9] do not operate at 24 GHz.

Table 3.1: Performance Summary and Comparison with Other PAs. Reprinted with permission from [34].

	This	[12]	[36]	[37]	[17]
Technology	0.18-μm BiCMOS	0.18-μm BiCMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Freq (GHz)	16.5-25.5	16.5-28	24	18-23	18.8-23.3
Gain (dB)	20 @24 GHz >18 (in BW)	37.6 @24 GHz >34.5 (in BW)	19	22.5 @20.5 GHz >19.5 (in BW)	26.2 @21 GHz >25 (in BW)
P_{sat} (dBm)	20.8 @24 GHz 18.5-20.8 (in BW)	19.4 @24 GHz 18.3-20.6 (in BW)	19	20.1 @20 GHz 18-20.1 (in BW)*	20.3 @21 GHz 19-20.3 (in BW)*
OP1dB (dBm)	18.1 @24 GHz 15.1-18.1 (in BW)	13.8 @24 GHz 12.5-15 (in BW)*	15.7	16 @20 GHz 14.9-16.2 (in BW)*	17.2 @21 GHz 16-17.2 (in BW)*
PAE (%)	23 @ 24GHz 13.5-23 (in BW)	22.3 @24 GHz 17-29 (in BW)	24.7	9.3 @20 GHz 7-9.3 (in BW)*	24.1 @21 GHz 20-24.1 (in BW)*
Topology	2 stages, cascode, single-end	2 stages, cascode, single-end	2 stages, cascode, single-end	3 stages, cascode, single-end	2 stages, cascode, single-end

*Estimated from figures; BW= 3-dB Bandwidth

3.4 Conclusion

This dissertation reports the design and performance of a new 0.18-μm SiGe BiCMOS PA utilizing both HBT and body-floating NMOS in a cascode configuration. The high f_T/f_{max} of the HBT together with the large voltage swing of the NMOS and the advantages of the body-floating technique are exploited to provide relatively flat gain and high linearity over a wide frequency range. The PA provides Psat of over 16.5-25.5 GHz. At 24 GHz, The PA delivers 20.8 dBm PAE of 13.5-23%, and relatively flat gain of 19.5$\pm$1.5 dB 18.5-20.8 dBm, OP1dB of 16.6$\pm$1.5 dB dBm, maximum P_{sat} with 18 dBm OP1dB, 23% maximum PAE, and 20 dB gain. The developed PA's high performance demonstrates the unique advantage of combined HBT and NMOS in a cascode PA topology. The performance also makes the PA attractive for use in Ku/K-band communication and radar systems, especially for non-licensed applications at 24 GHz.

4. A HIGH-PERFORMANCE 25–36-GHz BiCMOS STACKED POWER AMPLIFIER FOR 5G APPLICATIONS

4.1 Introduction

Wide-band devices in K-band (18-27 GHz) and Ka-band (27-40 GHz) have received compelling attention for high-data-rate communications such as 5-th generation wireless communication system (5G). One of the most important building blocks in RF systems is power amplifier (PA). Various PAs have been developed in the K and Ka-band on different processes like GaAs, InP, and Silicon (Si). Although PAs using GaAs or InP process could have better power handling and efficiency than those realized on Si, it is very hard to integrate an entire RF system on the same substrate for GaAs or InP, making it difficult to design single-chip RF systems. On the other hand, PAs on Si, together with other Si-based RF components, enable realization of single-chip RF systems. Furthermore, BiCMOS process adopts both advantages of the IV (Si) and III-V (GaAs, InP) processes, having high performance HBT and standard NMOS devices.

Cascode amplifiers are a popular architecture due to their good input-output isolation, gain, bandwidth, and stability. Typical cascode amplifiers in CMOS or BiCMOS process employ two cascode NMOS transistors or HBTs, respectively [33]. Particularly, in standard CMOS processes, the two transistors must be NMOS since only NMOS transistors are available in the process. In BiCMOS processes, however, both NMOS transistors and HBT are available, allowing use of either NMOS or HBT, or a combination of them, for the two transistors for proper circuit design and/or possible optimization of circuit's performance. In general, HBTs have higher f_T and f_{MAX}, and larger transconductance than NMOS transistors, leading to higher gain, especially in the high frequency region of suitable operating frequencies. Specifically, in the Tower-Jazz 0.18-μm SiGe BiCMOS

process [1] that we use for the PA reported in this dissertation, the HBTs have smaller voltage swing than the NMOS transistors. Moreover, NMOS with the body-floated by a resistor [2], [3] can improve the voltage swing, and hence linearity, besides having less parasitic capacitances between the source and bulk (C_{sb}) and between the drain and bulk (C_{db}) for enhanced gain at high frequencies. For PA design, transistors having high gain and large voltage swing for enhanced linearity are desired, hence making a combination of both HBT and body-floating NMOS attractive for cascode PAs. In this dissertation, we report a new 0.18-μm SiGe BiCMOS stacked-amplifier PA implementing both HBT and NMOS transistors with body-floating technique and stacked-amplifier concept to exploit the advantages of these devices together for attaining decent gain, output power, PAE, and OP1dB. In the simulation, the PA achieves around 23 dBm P_{sat}, 21 dBm OP1dB, 18 % maximum PAE, and over 30 dB gain across 25-36 GHz. At 28 GHz, the PA has simulated P_{sat}, OP1dB, maximum PAE, and gain of 24 dBm, 21 dBm, 18 %, and 34 dB, respectively.

4.2 Design and Analysis

Fig. 4.1 shows the schematic of the PA consisting of a drive amplifier in the first stage and two identical main amplifiers in the second stage. Drive amplifier adopts classical HBT-HBT cascode amplifier to function a gain stage. Second stage is implemented with the proposed new structure, which will be addressed more in the following paragraph. The PA was designed and fabricated using the Tower-Jazz 0.18-μm SBC18H3 process and, as shown in Fig. 4.2, occupies a 1.68$\times$0.76 mm2 die without the RF and dc pads. The two main amplifiers in the PA are integrated through lumped-element Wilkinson power divider and combiner, each simulating a low-pass filtering response to suppress the harmonics for improved PAE [4]. All the transmission lines and interconnects are realized with coplanar waveguides on the thickest topmost metal layer for minimum conductor

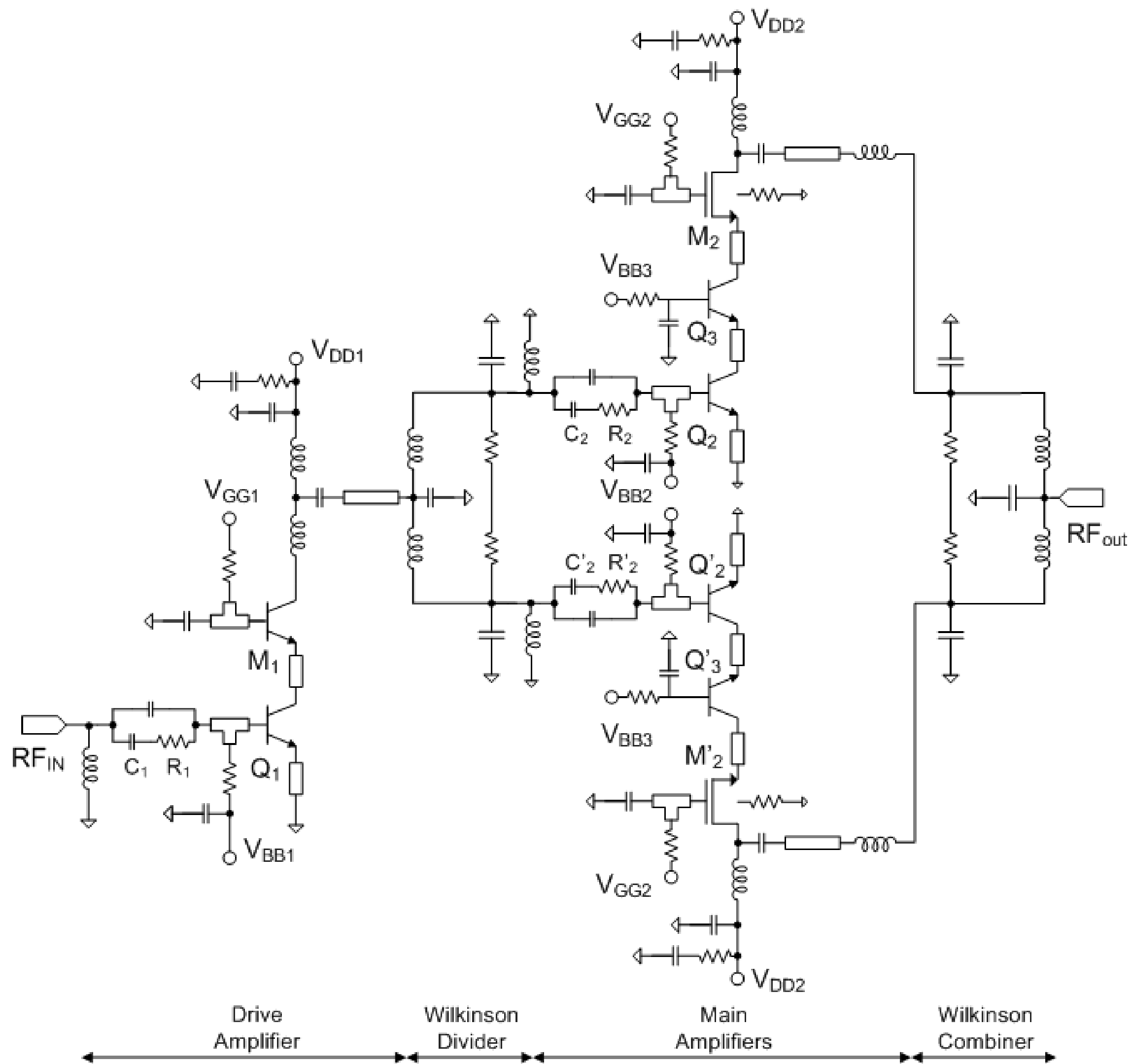


Figure 4.1: Schematic of the proposed HBT-HBT-NMOS PA.

loss. The transmission lines, interconnects, and inductors are designed and simulated using HyperLynx 3D EM simulator. Cadence is used for circuit simulations as well as extracting the parasitic elements produced by the layout.

Fig. 4.3a shows the schematic from the previous Chapter 3 summary [34]. The high f_T/f_{max} of the HBT together with the large voltage swing of the NMOS and the advantages of the body-floating technique are exploited to provide relatively flat gain and high

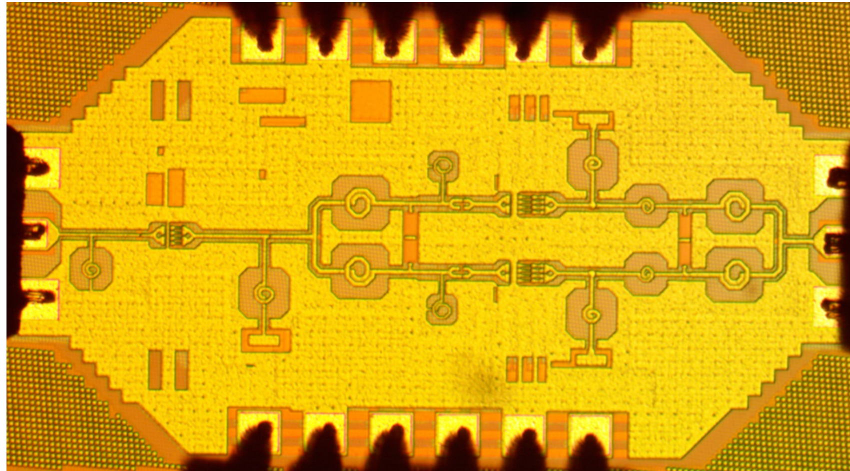


Figure 4.2: Photograph of the fabricated PA.

linearity over a wide frequency range. Fig. 4.3b elaborate the proposed three stacked amplifier: HBT-HBT cascode with body-floating NMOS. Fig. 4.4a demonstrates the enhancement of the current gain of the main amplifier between two amplifiers, showing that the f_T is actually improved by 80 % from 50 GHz to 90 GHz. Further, Fig. 4.4b reports the maximum available power gain (g_{max}) over frequency. The newly proposed amplifier has around 25 dB g_{max} at 40 GHz, better than around 18 dB in HBT-NMOS with body floating resistor (38 % improvement). The major reason of the improvement is the second transistor (Q2) acts as a buffer to suppress miller capacitor phenomenon, leading to better f_T and g_{MAX}.

However, since one more transistor is stacked, a higher biasing voltage (V_{DD}) is needed, resulting in worse power efficiency. Hence the stacked amplifier concept is introduced to create more headroom for voltage swing. Figs. 4.5a and 4.5b compares the voltage swing between two conditions. Obviously, the amplifier with technique of stacked amplifier has larger voltage swing as shown in Fig. 4.5b, leading to better power efficiency.

Each input transistor (Q2 and Q2') in the main amplifiers, as shown in Fig. 4.1, con-

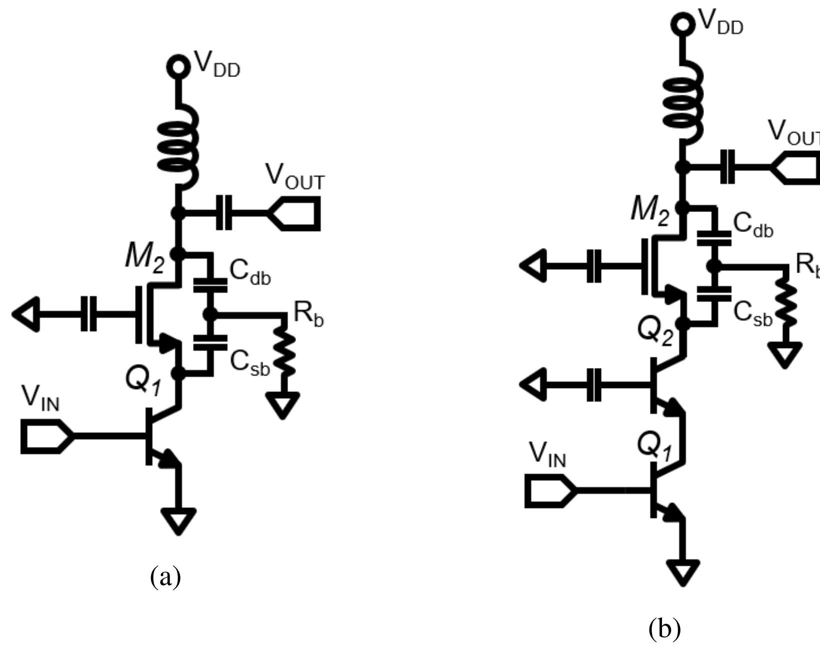


Figure 4.3: Simplified schematic (a) HBT-NMOS with body-floating technique and (b) HBT-HBT-NMOS with body-floating technique.

sists of four constituent transistors, each having 0.13-μm emitter width and 10-μm emitter length designed mainly for optimum MAG. The cascode transistors (M2 and M2'), each combining four transistors, are selected to have 12 fingers with a unit finger width of 4.5 μm through load-pull simulations for high output power. A 4K-Ohm resistor (R_b) is used for the body-floating resistor. It should be mentioned here that the large HBT used in the PA would degrade the reversed gain and stability due to the resultant high parasitic capacitances between the base and collector (C_{bc}) of the HBT, which should be taken into consideration in the design. In the high-frequency region of the designed PA's operating frequency range, however, the stability is well maintained because of the decay of the loop gain resulting from the lower MAG of the main amplifiers and the increased parasitic capacitances. At low frequencies, a combination of series RC and shunt C is utilized at the HBT's base to improve the stability.

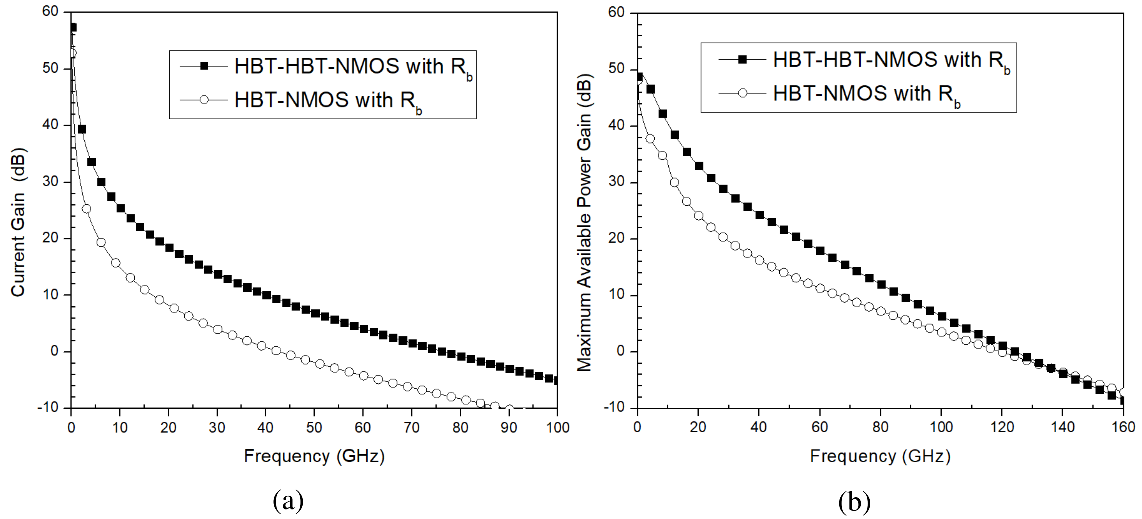


Figure 4.4: Comparison of performance over frequency (a) current gain and (b) maximum available power gain.

The each transistor (Q1, Q2) of the drive amplifier as shown in Fig. 4.1 consists of four transistors with 5-μm emitter length. The cascode transistor (M1) has 12 fingers with 2.5-μm width each. It is noted that HBT-HBT cascode can provide higher gain as a drive stage.

4.3 Measured Results

The designed PA was measured on-chip with a vector network analyzer and probe station. The drain voltage (V_{DD2}) of the main amplifiers is set to 5, 6, or 7 V, while that (V_{DD1}) of the drive amplifier is 3.35 V. The dc currents of the first and second stage are 30 and 60 mA, respectively. Fig. 4.7 shows the simulated gain (S_{21}) is 34 dB gain at 28 GHz and has less than 3-dB variation across 252- 36 GHz. The simulated input (S_{11}) and output (S_{22}) return losses are better than 10 dB from 30 to 40 GHz and 8 dB from 35 to 40 GHz, respectively. Fig. 4.7 shows the measured and simulated results of the power gain, output power and PAE with respect to the input power at 24 GHz. At 28 GHz, the

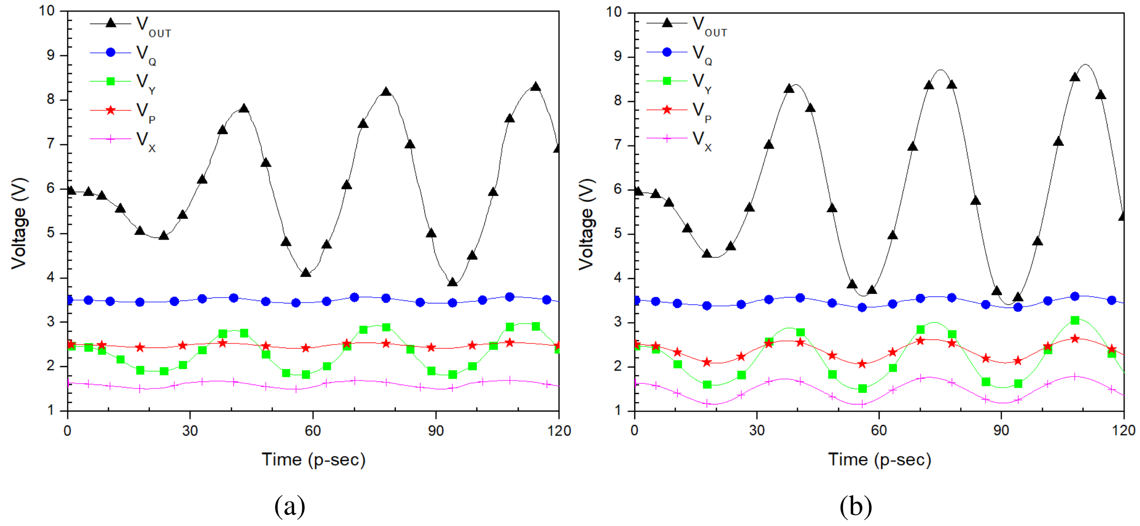


Figure 4.5: Voltage swing of (a) HBT-NMOS with body-floating technique and (b) HBT-HBT-NMOS with body-floating technique.

measured P_{sat}, OP1dB and maximum PAE are 23, 21 dBm and 18%, respectively. Fig. 4.8 displays the simulated performance of P_{sat}, OP1dB and PAE as a function of frequency. The measured Psat, OP1dB, and PAE are 20-23 dBm, 18-21 dBm, and 15-18 % across 25-36 GHz, respectively. Table 4.1 summarizes and compares the measured performance of the PA with those published Ka-band PAs on 0.18-μm CMOS and BiCMOS processes [4], [7]-[9]. At 28 GHz, the designed PA has the highest OP1dB of 18.1 dBm and Psat of 20.8 dBm. Compared with [4] fabricated in the same process, which employed all HBTs, this PA has OP1dB improved by about 3 dBm on the average over 16.5-25.5 GHz due to the use of the NMOS with body-floating technique. The PA in [7] only operates at the single frequency of 24 GHz and, while it has higher PAE, it provides lower gain, P_{sat} and OP1dB. It is noted that the PAs in [8] and [9] do not operate at 24 GHz.

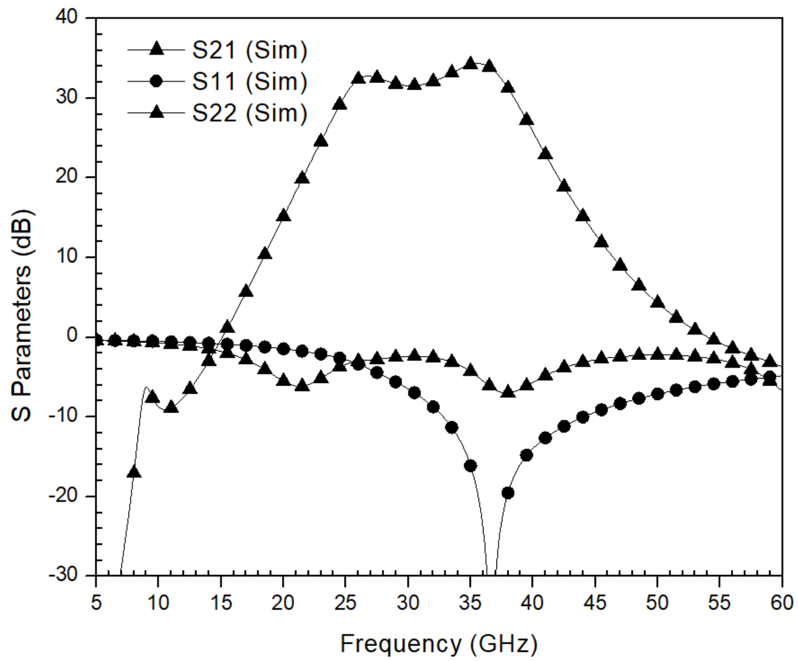


Figure 4.6: Simulated performance of the PA S-parameters.

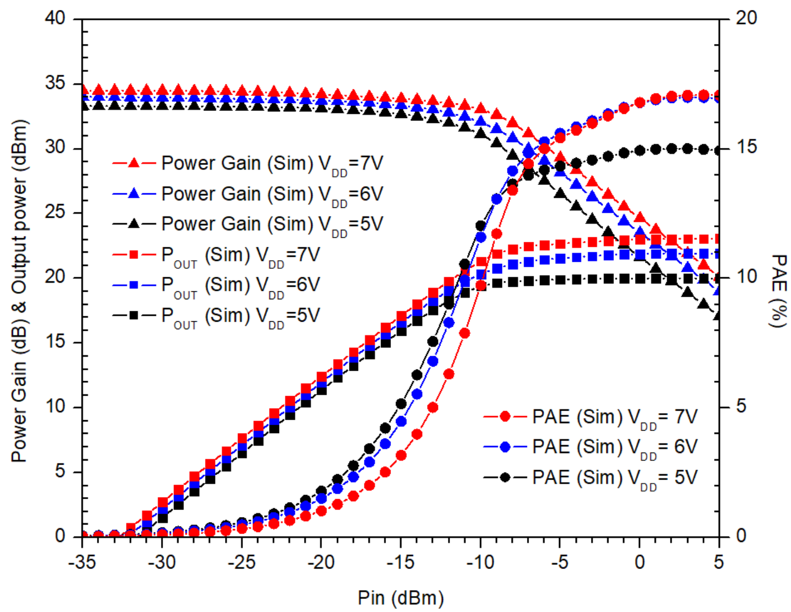


Figure 4.7: Simulated performance of the PA: power gain, output power and PAE at 28 GHz with 5, 6, and 7-V biasing.

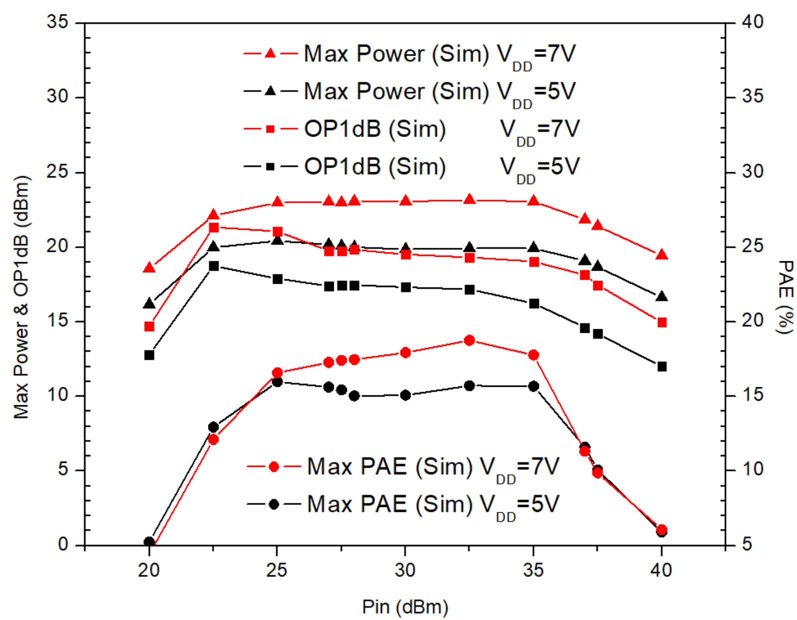


Figure 4.8: Simulated performance of the PA: power gain, output power and maximum PAE in bandwidth with 5, 6, and 7-V biasing.

Table 4.1: Performance Summary and Comparison with Other PAs

	This	[12]	[36]	[37]	[17]
Technology	0.18-μm BiCMOS	0.18-μm BiCMOS	0.18-μm CMOS	0.18-μm CMOS	0.18-μm CMOS
Freq (GHz)	25-36	16.5-28	24	18-23	18.8-23.3
Gain (dB)	30 @28 GHz >27 (in BW)	37.6 @24 GHz >34.5 (in BW)	19	22.5 @20.5 GHz >19.5 (in BW)	26.2 @21 GHz >25 (in BW)
P_{sat} (dBm)	20 @28 GHz 18.5-20.8 (in BW)	19.4 @24 GHz 18.3-20.6 (in BW)	19	20.1 @20 GHz 18-20.1 (in BW)*	20.3 @21 GHz 19-20.3 (in BW)*
OP1dB (dBm)	18.1 @28 GHz 15.1-18.1 (in BW)	13.8 @24 GHz 12.5-15 (in BW)*	15.7	16 @20 GHz 14.9-16.2 (in BW)*	17.2 @21 GHz 16-17.2 (in BW)*
PAE (%)	20 @28 GHz 13.5-23 (in BW)	22.3 @24 GHz 17-29 (in BW)	24.7	9.3 @20 GHz 7-9.3 (in BW)*	24.1 @21 GHz 20-24.1 (in BW)*
Topology	2 stages, cascode, single-end	2 stages, cascode, single-end	2 stages, cascode, single-end	3 stages, cascode, single-end	2 stages, cascode, single-end

*Estimated from figures; BW= 3-dB Bandwidth

4.4 Conclusion

This dissertation reports the design and performance of a new 0.18-μm SiGe BiCMOS PA utilizing both HBT and body-floating NMOS in a three-device cascode configuration. The high f_T/f_{max} of the HBT together with the large voltage swing of the NMOS and the advantages of the body-floating technique are exploited to provide relatively flat gain and high linearity over a wide frequency range. Besides, stacking technique could create more headroom for voltage swing, leading to larger output power and higher linearity. The PA provides P_{sat} of over 25-38 GHz. At 28 GHz, this PA delivers 24 dBm P_{sat} with 22 dBm OP1dB, 17 % maximum PAE, and 34 dB gain. The developed PA's high performance demonstrates the unique advantage of combined HBT and NMOS in a stacked PA topology. The performance also makes the PA attractive for use in K/Ka-band communication and radar systems, especially for 5G applications at 28 GHz.

5. A 25-53 GHz ULTRA-WIDEBAND HIGH-ISOLATION PASSIVE BALANCED DUPLEXER ON 0.18-μm BiCMOS FOR 5G APPLICATIONS

5.1 Introduction

In frequency division duplex (FDD) communication systems, duplexer (DUX) is the key component separating transmit (TX) and receive (RX) signals, preventing the power amplifier (PA) signals from desensitizing the low noise amplifier (LNA) input. Typical DUXs employ surface acoustic wave (SAW) or bulk acoustic wave (BAW) filters, which are hard to operate above 10 GHz [18]. The fifth generation (5G) mobile communication is going to be built in millimeter-wave (mm-wave) range at 28, 37, and/or 39 GHz [20]. Hence, for 5G wireless systems, fully-integrated mm-wave DUXs are essential.

In principle, mm-wave DUXs can be designed using ferrite circulators, active devices, or passive components. DUXs based on ferrite circulators are bulky and difficult to integrate with integrated circuits. Active-based DUXs have inherent non-linearity and high power consumption needed to achieve sufficient linearity for handling PA large signals [5],[6]. Passive-based DUXs are perhaps the best candidate considering tradeoff in integration, size, power consumption, and linearity. The passive DUX implementing a quasi-circulator in [21] uses three Langer couplers to cancel out TX signals, but only operating in a narrow bandwidth and occupying a large chip area. Electrical balanced DUX (EBD) is an attractive approach in passive DUXs. However, developed EBDs only work at low frequencies below 2.5 GHz [23, 24, 25, 26]. A mm-wave fully-integrated passive DUX covering the entire 5G spectrum of 28, 37, and 39 GHz has not yet been developed and is hence urgently needed for 5G wireless systems.

This dissertation presents the design of a new 25-53 GHz ultra-wideband mm-wave passive balanced DUX on 0.18-μm BiCMOS, covering the entire 28, 37, and 39 GHz 5G

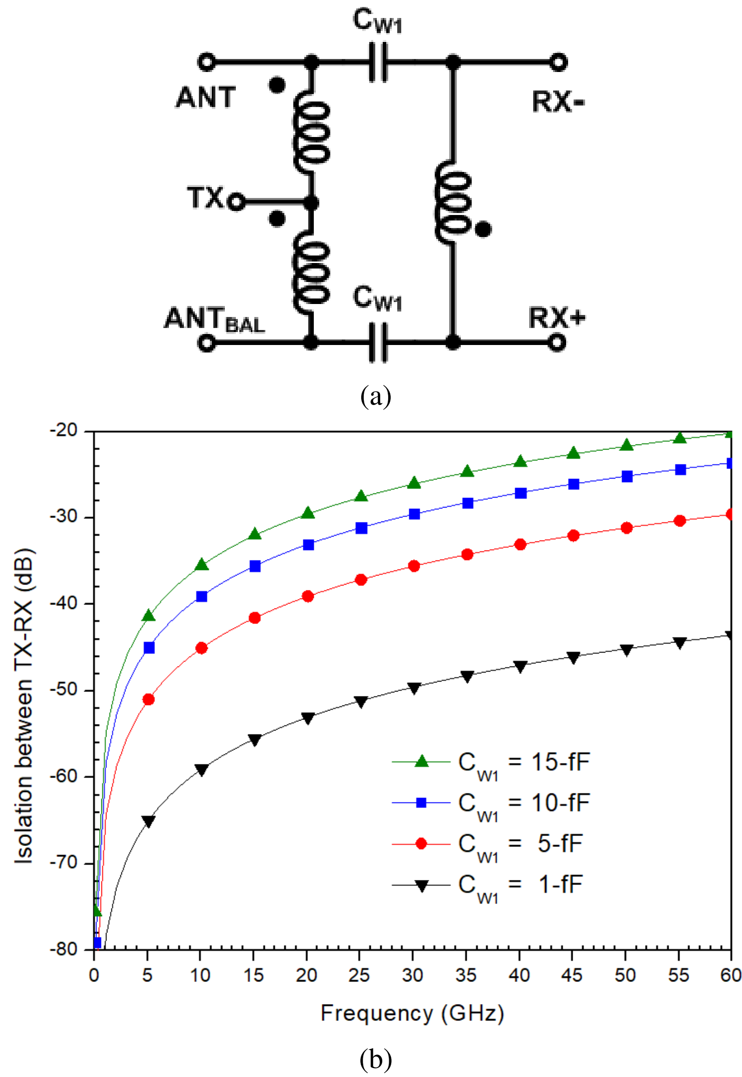


Figure 5.1: (a) Schematic of EBDs and (b) effects on isolation for different C_{W1}.

spectrums and beyond. The developed mm-wave balanced DUX enables single-ended TX and ANT, and differential RX, facilitating direct integration with a differential LNA in receivers to enhance power supply rejection as well as interference rejection against undesired signals and noise. It provides inherent matching at TX, RX and ANT ports, high TX-RX isolation, and highly balanced differential RX waveforms. An analysis of the mm-wave balanced DUX is performed and its analytically calculated results confirm

the DUX's operation and show good agreement with those simulated.

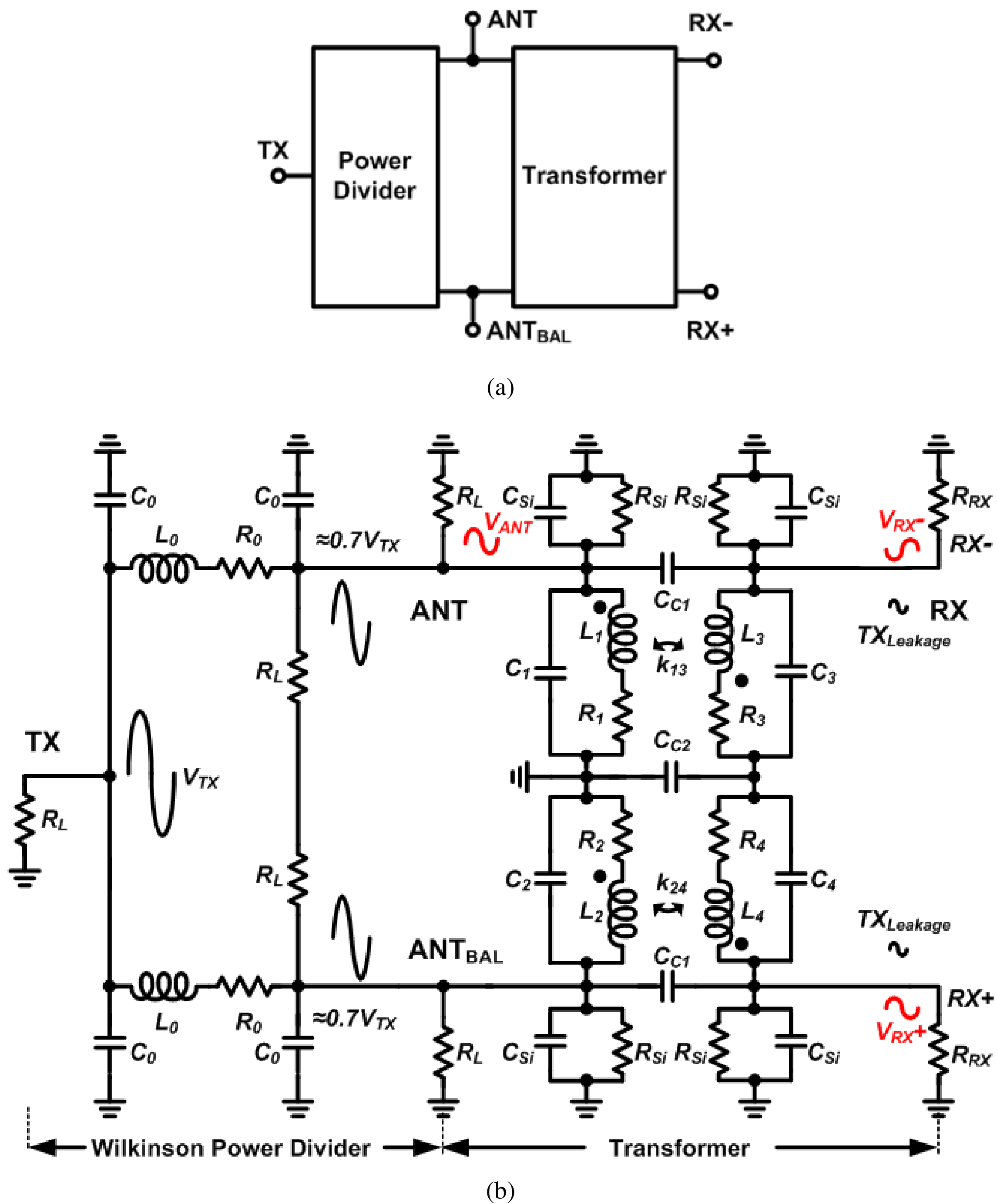


Figure 5.2: Proposed mm-wave balanced DUX: (a) block diagram and (b) schematic. R_L and R_{RX} are typically $50\,\Omega$.

5.2 DUX Architecture and Design

The proposed mm-wave balanced DUX adapts the concept of EBD to develop a performance-enhanced DUX for 5G applications.

5.2.1 Principle of EBD

Various EBDs have been developed [23, 24, 25, 26]. Fig. 5.1a shows an overall schematic of EBDs [25], where ANT represents the antenna port, TX denotes the transmitter port, and RX+ and RX- are the RX differential ports. It basically consists of a transformer, represented by a simplified model consisting of the inter-winding capacitances C_{W1} between the primary and secondary coils, and a load impedance (Z_{BAL}), which is ideally equal to the antenna's impedance for optimum TX-RX isolation.

These EBDs have two major drawbacks. Firstly, the TX port's input impedance is 25-Ohms, assuming 50-Ohm load impedance [23]. Consequently, a matching network is always needed at the TX port for interface with a PA. Secondly, the TX-RX isolation degrades at high frequencies due to C_{W1} as seen in Fig. 5.1b, which shows that even a small 5-fF capacitance of C_{W1} would reduce the isolation significantly from around 50 dB at 5 GHz to 35 dB at 40 GHz. For transformers fabricated on Si RFIC, inter-coupling capacitances are not contributed only by a single capacitor C_{W1}, but by multiple capacitors, and their capacitances could be large, especially at mm-wave frequencies, hence possibly degrading the isolation further. This inherent isolation limitation impedes these EBDs as viable candidates at mm-wave frequencies.

5.2.2 Proposed mm-Wave Balanced DUX

Fig. **??** shows the proposed mm-wave balanced DUX's block diagram and its schematic, which consists of a lumped-element Wilkinson power divider and a 1:1 ratio transformer with its primary center-tap grounded. It has three separate ports: single-ended TX and

ANT for direct integration with typical single-ended TX and ANT, and differential RX for direct integration with a differential LNA normally utilized in receivers for rejection of undesired common signals and noises. The $\mathrm{ANT_{BAL}}$ port represents a duplicate of the antenna connected to the ANT port, which can be terminated with an impedance equal to that at the ANT port. It is noted that the terminations at the ANT, $\mathrm{ANT_{BAL}}$ and TX are R_L, which is typically $50\,\Omega$, while the termination at the RX ports are R_{RX}, which represents the impedance looking into the LNA without matching network - for instance, the LNA's first transistor. By using this (R_{RX}) as the termination at the RX ports, instead of 50 Ohms, we can integrate an LNA directly with the DUX without designing an input matching network for the LNA as typically done for 50-Ohms system. The models and designs of the lumped-element Wilkinson power divider and transformer are described later. The proposed DUX has the following major advantages:

Firstly, the impedance matching of the proposed mm-wave balanced DUX is readily obtained at the TX, ANT and RX ports, facilitating its integration with PA, antenna and LNA. The matching at the TX port is inherent without a matching network due to the 50-Ohm input impedance of the TX port for the 50-Ohm Wilkinson power divider. The matching at the ANT port is also easily obtained without a matching network. The input impedance looking into the DUX at the ANT port is around $R_L \| (0.5R_L + 2R_{RX})$, where R_L is the termination at the TX, ANT and $\mathrm{ANT_{BAL}}$ ports, and R_{RX} is the termination at the RX ports, for a transformer with 1:1 ratio winding. Typically, R_{RX} for optimum gain and noise matching (to the LNA's transistor) is larger than 50 Ohms. Consequently, the input impedance at the ANT port is approximately close to 50 Ohms.

Secondly, as will be seen later, the grounding of the primary center-tap improves the isolation between TX and RX ports substantially. The grounded center-tap also improves the balance of the waveforms of differential signals at the RX ports. Additionally, it also results in a slightly lower insertion loss between TX and ANT.

Table 5.1: Element Lump Model Values of the Proposed DUX

Devices	Value	Device	Value
R_L (Ohm)	50	R_1, R_2 (Ohm)	0.57
R_0 (Ohm)	1.5	R_3, R_4 (Ohm)	0.43
L_0 (pH)	250	L_1, L_2 (pH)	114
C_0 (fF)	50	L_3, L_4 (pH)	110
C_{C1} (fF)	0.5	k_{13}	0.59
C_{C2} (fF)	21	k_{24}	0.59

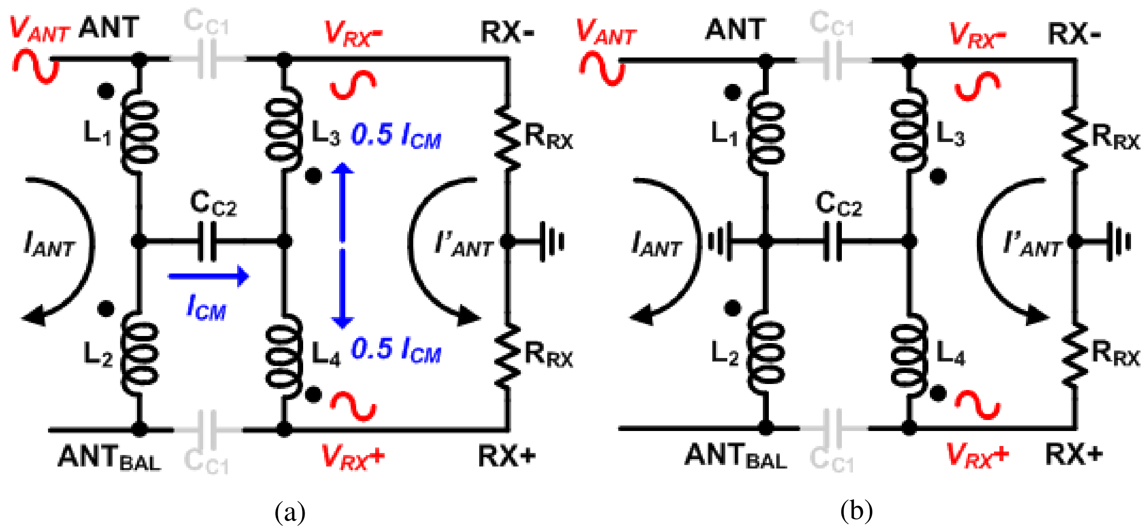


Figure 5.3: Equivalent circuits of transformer under ANT excitation: without (a) and with (b) center tap grounded. C_{C1} is neglected.

Thirdly, as described later, the lumped-element Wilkinson power divider provides a low-pass frequency response that helps suppress leakage through the inter-coupling capacitors of unwanted high-frequency signal such as harmonics from the TX.

5.2.3 Design of Lumped-Element Wilkinson Power Divider

Lumped-element Wilkinson power divider has two advantages as compared with its transmission-line counterpart: smaller size and low-pass filter response [12]. The low-pass response helps suppression of unwanted high-frequency signals such as harmonics from the TX, hence enhancing the TX-RX isolation at these high frequencies, effectively lessening the effects of high-frequency signals from disrupting the RX operation. The inductance and capacitance of the lumped-element Wilkinson power divider, as denoted in Fig. 2(b), can be determined from $L_0 = \sqrt{2}Z_0/(2\pi f_0)$ and $C_0 = 1/(2\pi f_0\sqrt{2}Z_0)$, respectively, where Z_0 is terminating impedance and f_0 is the design frequency. R_0 represents the inductor's resistive loss. In this design, 45 GHz is chosen to cover 28, 37, 39 GHz and filter out unwanted signals at higher frequencies. Table I lists the component values of the designed lumped-element power divider.

5.2.4 Design of Grounded-Center-Tap Transformer

The transformer model is shown in Fig. 5.2b. L_1, L_2, L_3, and L_4 are the principal inductances of the primary and secondary coils, respectively, with inductive coupling coefficients k_{13} between L_1, L_3 and k_{24} between L_2, L_4. R_1, R_2, R_3 and R_4 are the resistances of the corresponding inductors' conductors, accounting for the losses due to finite conductivity, skin effect and eddy currents. C_1, C_2, C_3, and C_4 are the coupling capacitances between the inductors' terminals. C_{C1} and C_{C2} represent the coupling capacitances between the primary and secondary coils. C_{Si} and R_{Si} represent the capacitances and resistances of oxide dielectrics and silicon substrate underneath the transformer, respectively. It is noted that, for transformers on Si RFIC employing primary and secondary inductors on different metal layers separated by thin dielectric layers such as oxide, large (parasitic) coupling capacitances between the inductors can occur, effectively causing more signal leaking (and hence reduced isolation) between the primary and secondary coils, as well

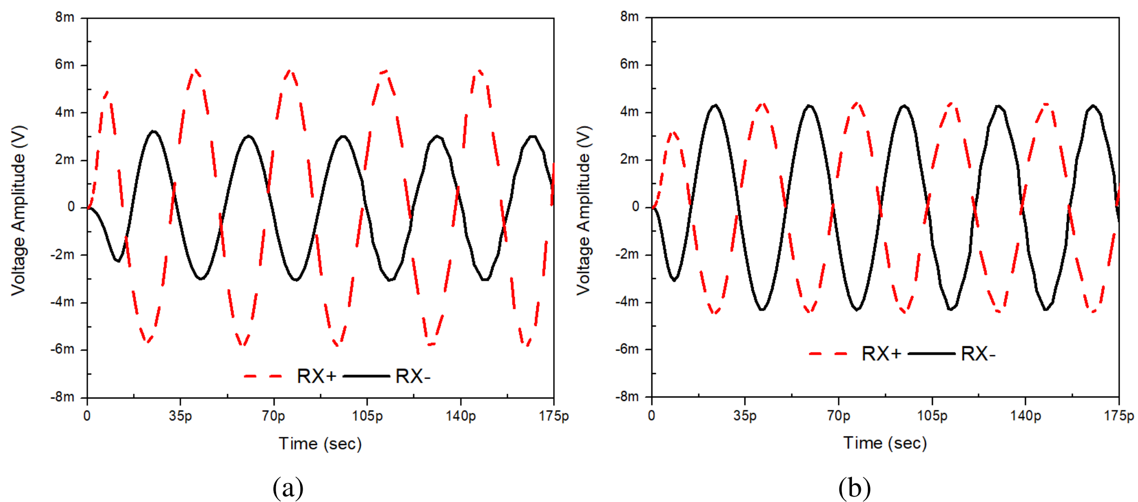
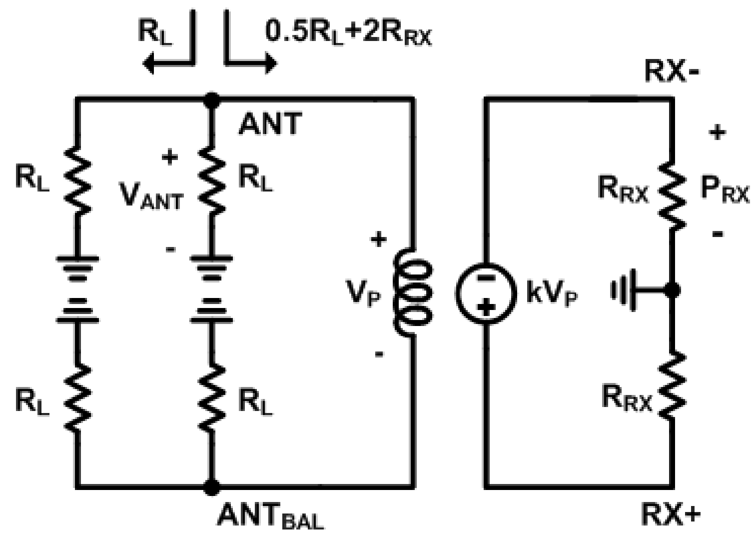


Figure 5.4: Time-domain differential RX signals under ANT excitation without (a) and with (b) center-tap grounded.

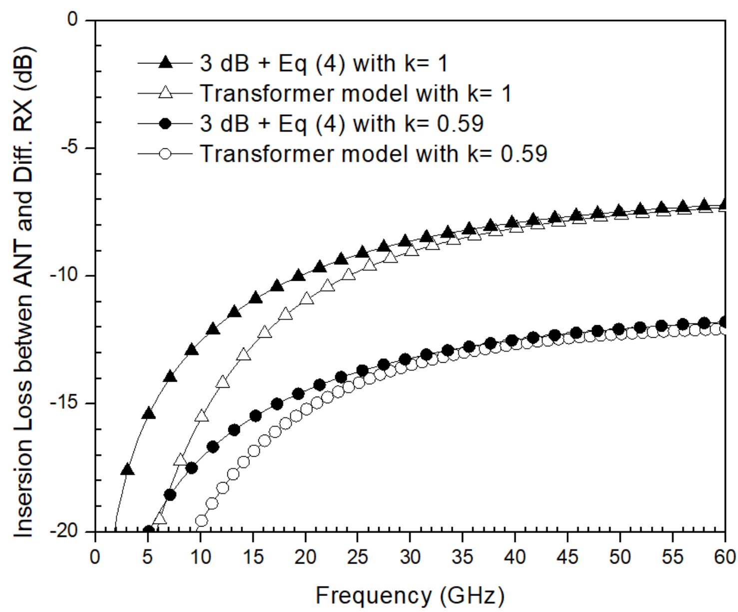
as lowering the self-resonant frequency and quality factor [29]. For simplicity in analysis, without loss of generality, we only consider L_1, L_2, L_3, L_4, k_{13}, k_{24}, C_{C1} and C_{C2} in the transformer model.

The transformer is designed to have a 1:1 ratio. To reduce the coupling capacitance between the terminals of the primary and secondary coils, these coils should be placed as far away as possible - for instance, in opposite positions - which, effectively, also helps reduce the coupling between and facilitate appropriate placement of ANT, ANT_{BAL}, and RX+- ports. Moreover, increasing the spacing between the two coils, reducing the turn number, and/or reducing the transformer size can decrease C_{C1} and C_{C2}. Due to the symmetry of the 1:1 ratio transformer, it can be inferred from the transformer model that C_{C2} is at least twice of C_{C1}, which is also confirmed through EM simulations.

Frequency response of transformers is similar to that of bandpass filters [30]. The lower cut-off frequency (f_L) of the 1:1 ratio transformer is mainly determined by the



(a)



(b)

Figure 5.5: (a) Equivalent circuit used for ANT-RX insertion loss analysis and (b) comparison of insertion losses between ANT and differential RX port using Eq. (4) and transformer model for k =1 and 0.59.

termination resistance (R_L) and inductance of the primary coil (L_p), and can be approximated as

$$f_L \simeq \frac{R_L}{2\pi L_p} \tag{5.1}$$

For simplicity, it is assumed that the inductance of the secondary coil ($L_s = L_3 + L_4$) is equal to L_p. Consider 27 GHz for f_L, the inductance of each coil, as calculated from (1), should be around 294 pH. Choosing a suitable f_L according to L_p is important. Less L_p results in high f_L and hence filtering out unwanted signals below f_L. Small L_p also leads to small coupling capacitances, resulting in better TX-RX isolation.

The upper cut-off frequency (f_U) is primarily determined by parasitics from oxide dielectrics, Si substrate (C_{Si}), and coupling capacitances (C_{C1} and C_{C2}). It is noted that, the transformer is designed to provide not only low insertion loss from ANT to RX ports, but also high isolation between TX and RX ports. Additionally, it is also desirable to have high out-of-band isolation to help suppress unwanted signals like harmonics from the TX, which otherwise may disrupt the RX operation. To that end, each inductor of the transformer is designed to have a self-resonant frequency higher than 80 GHz to possibly suppress unwanted signals including second harmonics from TX up to 80 GHz.

Table 5.1 lists the component values of the designed 1:1 ratio transformer. The designed transformer has 150- and 130-μm outer dimensions for the primary and secondary coils with 8-μm trace width on the top-most metal, respectively.

5.2.5 Insertion Loss between ANT-RX

As shown in Fig. 5.2b, the signals at two terminals of the secondary coil are differential. The coupling capacitance, however, degrades the amplitude and phase balance between them, especially at mm-wave frequencies.

Figs. 5.3a and 5.3b show the equivalent circuits of the transformer excited by a signal

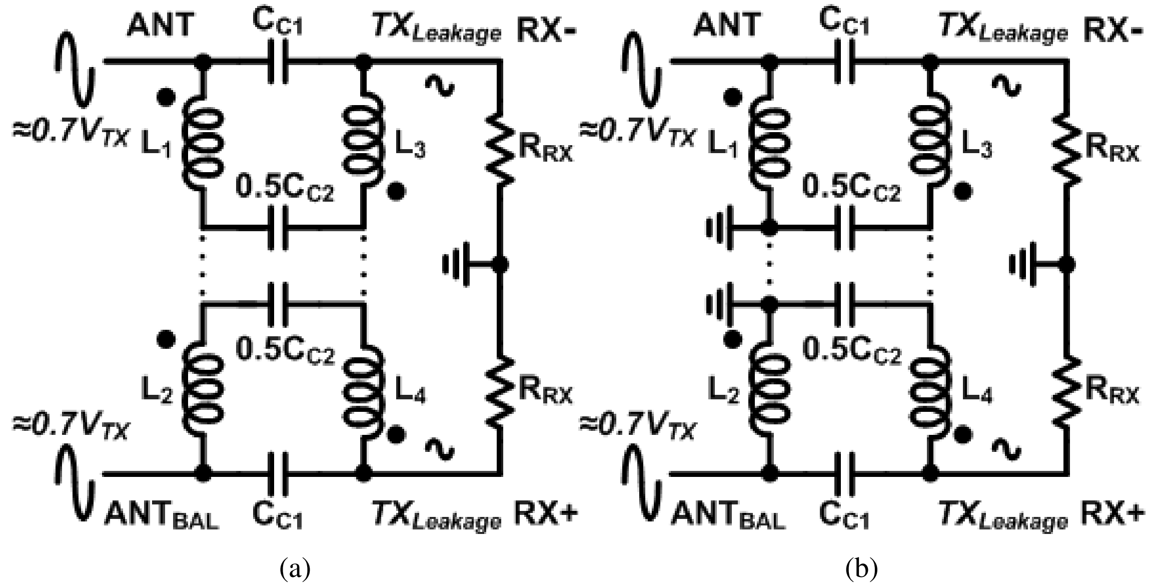


Figure 5.6: Equivalent circuit of the transformer under TX excitation without (a) and with (b) the center-tap grounded.

from ANT without and with the primary center-tap grounded, respectively. As C_{C1} is much smaller than C_{C2}, it is reasonably neglected in this analysis.

Fig. 5.3a is the current induced by I_{ANT} assuming ideal transformer behavior. However, the leakage current (I_{CM}) through C_{C2} injects additional currents ($0.5I_{CM}$) into the secondary, as shown in Fig. Fig. 5.3a, which impair the RX differential signals, especially at mm-wave frequencies.

In Fig. 5.3b, because C_{C2} is connected to ground, the ANT signal does not leak through C_{C2}, hence resulting in zero-I_{CM}.

To verify the waveforms of the RX differential signals without and with the primary center-tap grounded, these RX signals are simulated with ANT signal at -20 dBm ($V_{pp} \simeq$ 40-mV) at 28.2 GHz, as shown in Fig. 5.4. As seen in Fig. 5.4a, V_{RX^+} and V_{RX^-} are asymmetric when the center-tap is not grounded due to crosstalk between the primary

and secondary coil through C_{C2}, as expected. On the other hand, Fig. 5.4b for grounded center-tap shows almost perfect differential RX signals. Grounding the primary center-tap indeed improves the balance of the RX differential signals.

To simplify the formulation without loss of generality, the coupling factors (k) representing the magnetic coupling between primary and secondary inductors are assumed ideal without any loss. Fig. 5.5a shows the equivalent circuit used for deriving the insertion loss from ANT to RX. For high k, the leakage inductances [$(1-k)L_p$ and $(1-k)L_s$] are ignored in this analysis. The impedance looking into the transformer is around $(0.5R_L + 2R_{RX})$ while that looking into the Wilkinson power divider is R_L. The power injected into the DUX at the ANT port can be expressed as

$$P_{ANT} \simeq \frac{V_{ANT}^2}{R_L \| (0.5R_L + 2R_{RX})} \tag{5.2}$$

and the power at a single-ended RX port (RX+ or RX-) can be derived as

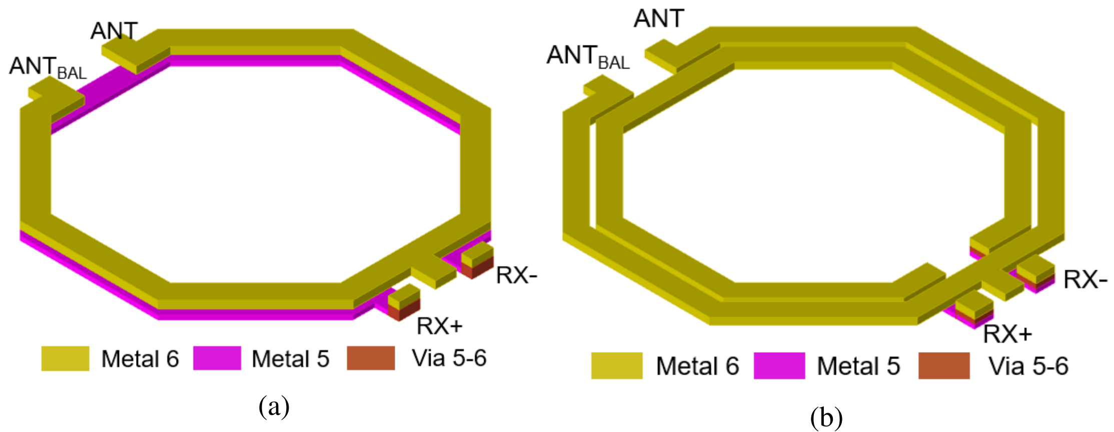
$$P_{RX^+} = P_{RX^-} \simeq \frac{k^2 R_{RX} V_{ANT}^2}{(0.5R_L + 2R_{RX})^2} \tag{5.3}$$

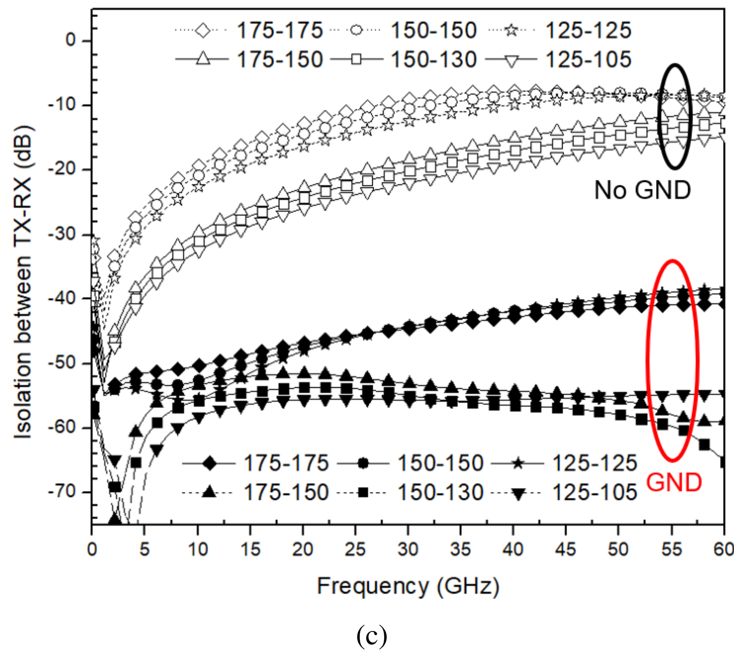
The (power-based) insertion loss from ANT to a single-ended port can then be obtained from (5.2) and (5.3) as

$$IL_{ANT-RX}^P(\omega) \simeq \frac{k^2 R_{RX}}{\sqrt{1 + (R_L/\omega L_p)^2}} \frac{R_L \| (0.5R_L + 2R_{RX})}{(0.5R_L + 2R_{RX})^2} \tag{5.4}$$

which includes the lower cut-off frequency described in (5.1) needed for frequency response.

Fig. 5.5b compares the insertion loss from ANT to differential RX port calculated





(c)

Figure 5.7: (a) Broadside-coupled on M5, M6 and (b) co-planar on M6 transformers. (c) Isolation with and without center-tap grounded. 175-150 implying 175 and 150-μm for the respective primary and secondary coils - likewise for other pairs.

from (5.4), with 3-dB reduction accounting for the differential port, and transformer model in Fig. 5.5b for $k = 1$, 0.59, showing good agreement between them. It is noted that $k = 1$ is for ideal case and $k = 0.59$ is for the actual transformer obtained from its EM simulations. The model elements are extracted from the EM-simulator Hyper Lynx

3D EM [39]. R_{RX} and R_L are assumed to be 50 Ohms in these calculations. As can be seen, the insertion loss between the ANT and differential RX ports approaches a constant value of around 6.4 dB for $k = 1$ and 11 dB for $k = 0.59$.

5.2.6 Isolation between TX-RX

For simplicity without loss of generality, we assume the Wilkinson power divider and the interconnects between it and the transformer are lossless. Under this condition, the voltage arriving at each of the primary coil's terminals is $0.707\mathrm{V_{TX}}$, where $\mathrm{V_{TX}}$ is the incident voltage at the TX port, as shown in Fig. 5.2b. Due to identical TX signals at the primary terminals, the inductive coupling parameters k_{13} and k_{24} can be discarded in the isolation analysis. Fig. 5.6a and Fig. 5.6b show the equivalent circuits of the transformer excited by a signal from TX without and with the primary center-tap grounded, respectively. For simplicity, we assume all inductors are ideal and have identical value ($L_1 = L_2 = L_3 = L_4$). Consider Fig. 5.6a, the (voltage-based) isolation between the TX and a single-ended RX port without grounded center-tap, assuming no reflections, can be derived as

$$ISO_{TX-RX}^{V,O}(\omega) \simeq \frac{1}{\sqrt{2}} \left| \frac{R_{RX}}{[(2sL_1 + \frac{2}{sC_{C2}}) \| \frac{1}{sC_{C1}}] + R_{RX}} \right| \tag{5.5}$$

which becomes, neglecting $\mathrm{C_{C1}}$,

$$ISO_{TX-RX}^{V,O}(\omega) \simeq \frac{1}{\sqrt{2}} \left| \frac{R_{RX}}{2sL_1 + \frac{2}{sC_{C2}} + R_{RX}} \right| \tag{5.6}$$

To avoid TX signal from leaking to ground and maintain the voltages at the two primary inductors as $0.707\mathrm{V_{TX}}$, L_1 and L_2 should be large enough. For the case with the center-tap grounded, the (voltage-based) isolation between the TX and a single-ended RX port can

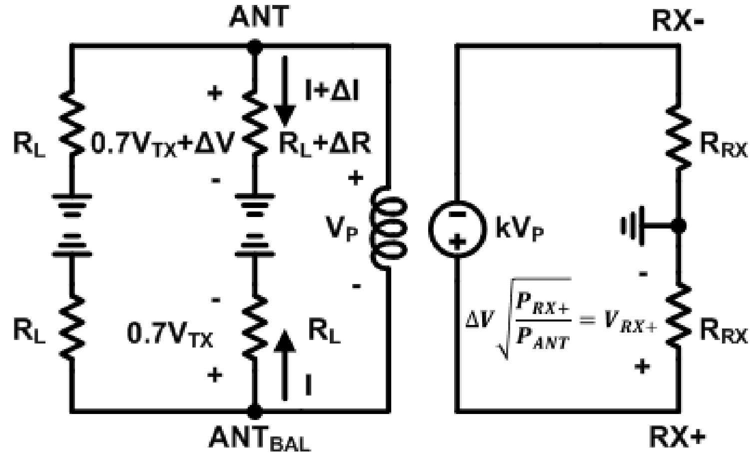


Figure 5.8: Equivalent circuit for analysis of impedance mismatch between ANT and $\mathrm{ANT_{BAL}}$ under TX excitation.

then be derived as

$$ISO^{V,G}_{TX-RX}(\omega) \simeq \frac{1}{\sqrt{2}}\left|\frac{R_{RX}\|(sL_1+\frac{2}{sC_{C2}})}{\frac{1}{sC_{C1}}+[R_{RX}\|(sL_1+\frac{2}{sC_{C2}})]}\right| \tag{5.7}$$

Examination of (5.6) and (5.7) shows that the numerator in (5.6) is larger than that in (5.7), while having smaller denominator than (5.7) since C_{C2} is typically much larger than C_{C1}. Consequently, the isolation between the TX and RX port is significantly improved by grounding the center-tap. We also see, through this analysis, that C_{C1} plays an important role in the leakage when the center-tap is grounded, and hence the isolation between TX-RX, and needs to be minimized.

Fig. 5.7a and Fig. 5.7b show broadside-coupled and co-planar 1:1 ratio transformers on metal layers M5, and M6, respectively, with 8-μm width and 125, 150, 175-μm outer dimensions that are considered in the design of an optimum transformer. Fig. 5.7c displays EM-simulated isolations, between the primary and secondary coils for these transformers with and without center-tap grounded, showing higher isolation for co-planar

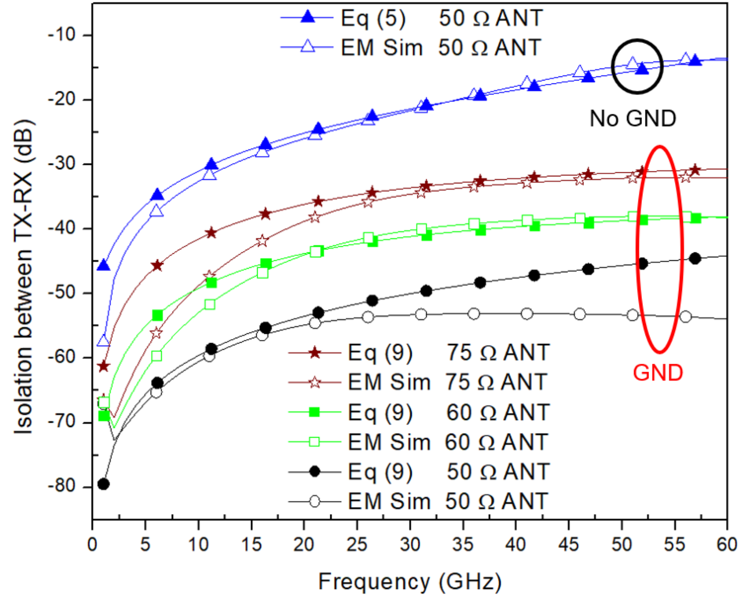


Figure 5.9: Comparison of isolations between calculations and EM simulations with and without center-tap grounded for different loading at ANT.

transformers, which is expected, due to less undesirable coupling capacitance between the two coils. Furthermore, the isolation degrades when the transformer's outer dimension is increased, which further confirms the effects of the coupling capacitances on the isolation. It can be seen that the grounded-center-tap transformers, either in broadside-coupled or co-planar structure, improves the isolation to more than 20 dB, primarily due to suppressing TX leakage through C_{C2}. In view of these simulations, the co-planar transformer on M6 with 150-μm outer dimension, 8-μm trace width, and 2.01-μm turn-spacing is chosen.

While the transformer plays an important role in the isolation between TX-RX of the DUX, the balance between the loading at the ANT and ANT_{BAL} port also affects the isolation. Fig. 5.8 shows the equivalent circuit used for the impedance mismatch analysis between ANT and ANT_{BAL} under TX excitation. The voltage difference ΔV caused by

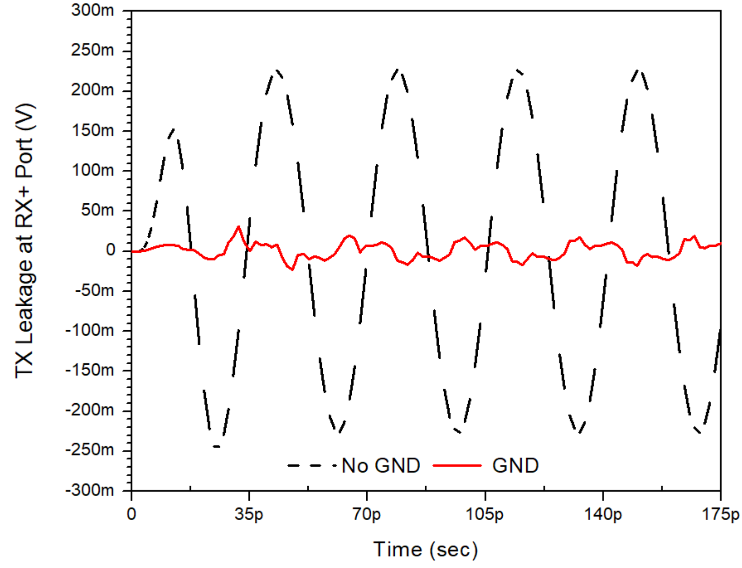


Figure 5.10: TX leakage at RX+ terminal in time-domain with and without center-tap grounded.

the impedance mismatch ΔR can be derived, neglecting ΔI, as

$$\Delta V \simeq \frac{V_{TX}}{\sqrt{2}} \frac{\Delta R}{R_L} \tag{5.8}$$

The isolation with grounded center-tap, taking into account the coupling capacitances and impedance imbalance at the ANT and ANT_{BAL} ports, can be derived utilizing (5.2), (5.3), (5.7) and (5.8) as

$$\begin{aligned} ISO^{V,G}_{TX-RX}(\omega) \simeq & \frac{1}{\sqrt{2}} \left| \frac{R_{RX} \| (sL_1 + \frac{2}{sC_{C2}})}{\frac{1}{sC_{C1}} + R_{RX} \| (sL_1 + \frac{2}{sC_{C2}})} \right| \\ & + \frac{1}{\sqrt{2}} \frac{\Delta R}{R_L} \frac{1}{\sqrt{1 + (R_L/\omega L_p)^2}} \sqrt{\frac{P_{RX+}}{P_{ANT}}} \end{aligned} \tag{5.9}$$

where the first and second term show the effects of TX leakages through C_{C1} and ΔR, respectively. Eq. (5.9) indicates clearly that, besides minimizing the coupling capacitance

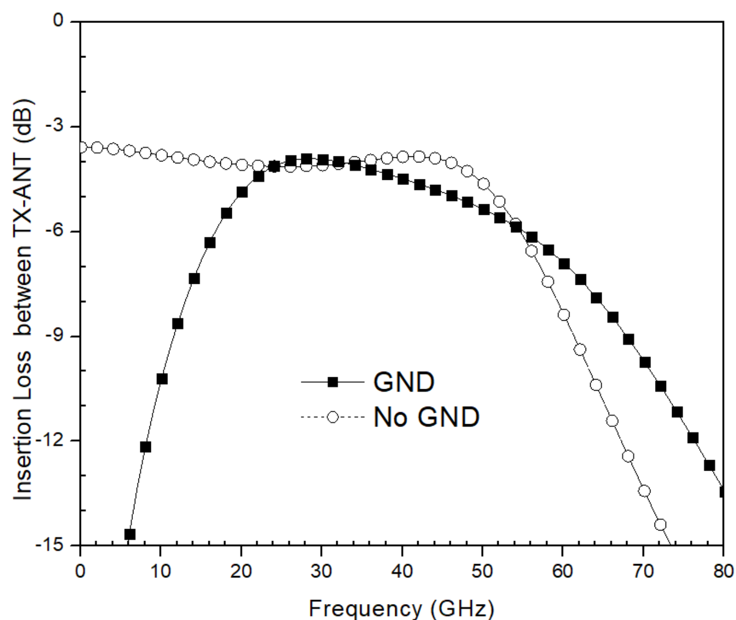


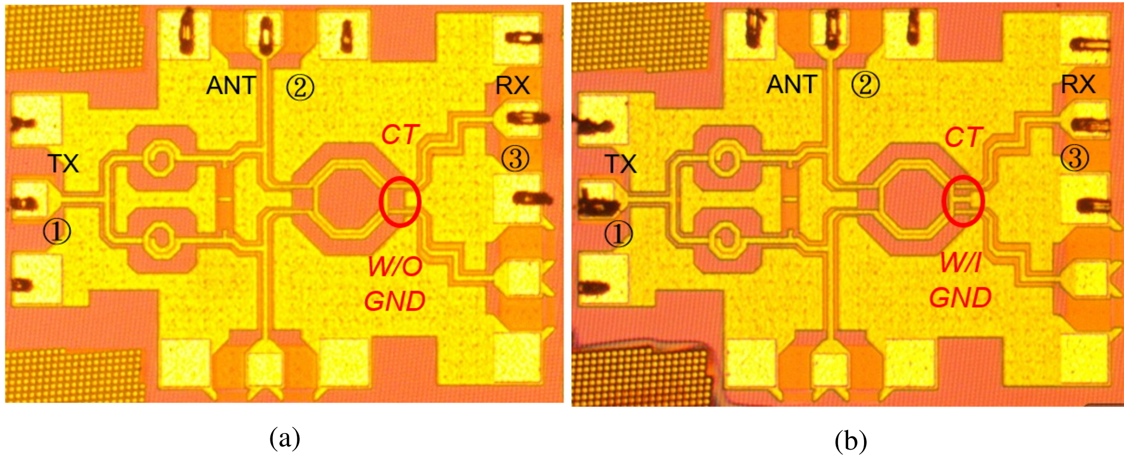
Figure 5.11: Insertion loss from TX to ANT port with and without center-tap grounded.

C_{C1} for reduced leakage, the impedance imbalance ΔR needs to be kept as small as possible, which emphasizes the significance of a symmetric layout.

Fig. 5.9 compares the results between calculations using (5.5), (5.9) and EM simulations for 50, 60, and $75\,\Omega$ loading impedances at ANT port and $50\,\Omega$ loading at ANT_{BAL}, which show good agreement, except between Eq. (5.7) calculation and EM simulation for equal $50\,\Omega$ loading at ANT and ANT_{BAL}. This difference is expectedly due to the low-pass response of the lumped-element Wilkinson power divider in the EM simulation while maintaining perfect impedance balance at ANT and ANT_{BAL}.

Fig. 5.9 also shows that the proposed mm-wave balanced DUX can theoretically achieve 55 dB isolation under the perfectly balanced load condition. With a relatively large mismatch loading of 75-50 Ohms for ANT-ANT_{BAL} ports, the DUX provides better than 34 dB isolation, which is still decent but significantly less than the ideal balance case.

Fig. 5.10 shows the leakage intensity at a single-ended RX port (RX+) with and with-



(a) (b)

Figure 5.12: Photographs of the fabricated mm-wave balanced DUX without (a) and with (b) grounded center-tap.

out center-tap grounded when a 20 dBm ($V_{pp} \simeq 6300$-mV) signal at 28 GHz is injected into the TX port. The voltage at a single-ended RX port is around 500-mV_{pp}, corresponding to 20 dB isolation, and 40-mV_{pp}. corresponding to 40 dB isolation, without and with ground at the center-tap, respectively.

5.2.7 Insertion Loss between TX-ANT

Fig. 5.11 shows the EM-simulated insertion loss from TX to ANT without and with the center-tap grounded, showing respectively low-pass and band-pass responses. When the center-tap is not grounded, the impedance at each output port of the Wilkinson power is R_L. However, with grounded center-tap, that impedance consists of R_L in parallel with a L_1 or L_2. As a result, with grounded center-tap, the frequency response between TX and ANT is a combination of low-pass response (due to the Wilkinson power divider) and high-pass response (due to shunt L_1 or L_2), ultimately making it as band-pass response. It is seen that the inductors of the primary coils (L_1, L_2) determine the lower cut-off frequency of the insertion loss between TX and ANT port.

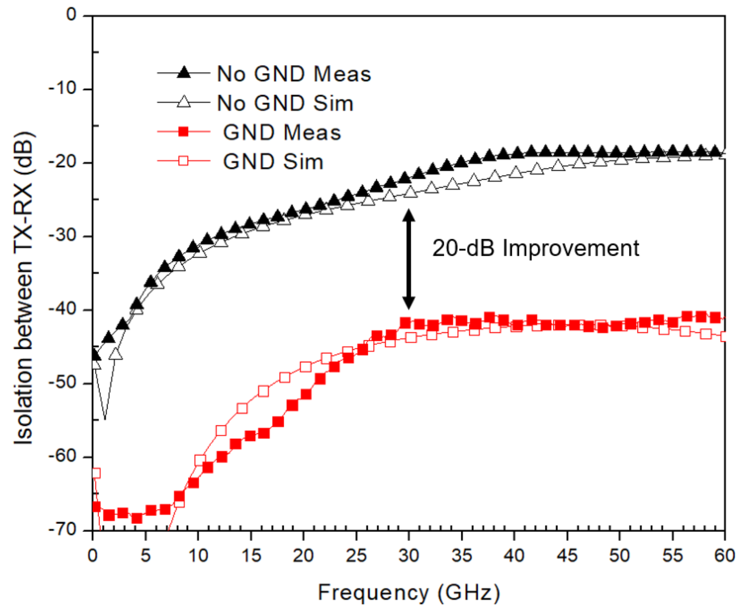


Figure 5.13: Simulated and measured TX-RX+ or TX-RX- isolation (S_{31}) with and without grounded center-tap.

5.3 Measurement Results

Fig. 5.12 shows photographs of the mm-wave balanced DUXs without and with grounded center-tap fabricated using Tower-Jazz 0.18-μm SBC18H3 process [40]. The chip only occupies a die size of 0.6-by-0.5 mm^2 without RF pads. All components except resistors and capacitors were simulated using EM simulator Hyper Lynx 3D EM and Keysight Momentum [41]. The chip was also simulated and laid out with Cadence [42]. All interconnects and transmission lines are coplanar waveguide (CPW) on the topmost metal layer, and all spiral inductors are surrounded with co-planar ground. Special care in layout was taken to maintain well symmetry and minimize additional coupling from the TX to the RX sides. All measurements were performed on-wafer using Rhode & Schwarz vector network analyzer (VNA) and Cascade probe station. The short-open-load-thru calibration method along with Microtech's impedance standard substrate standards was used.

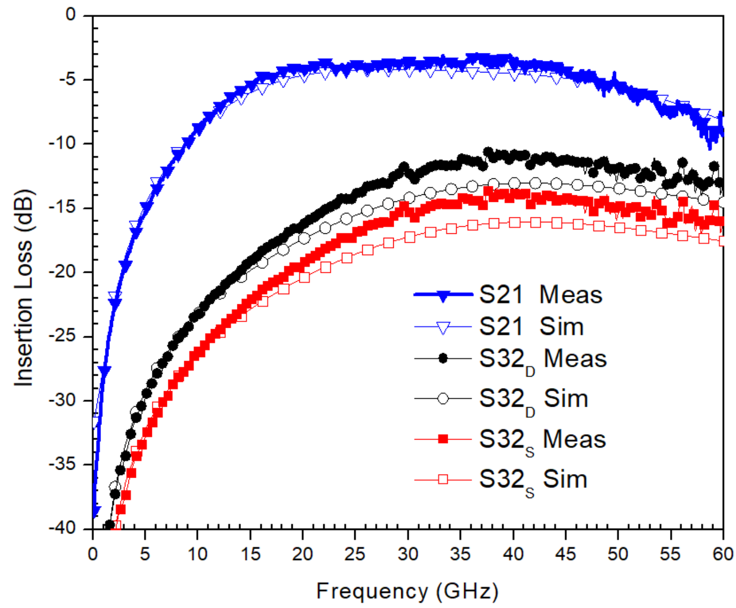


Figure 5.14: Simulated and measured insertion losses with grounded center-tap.

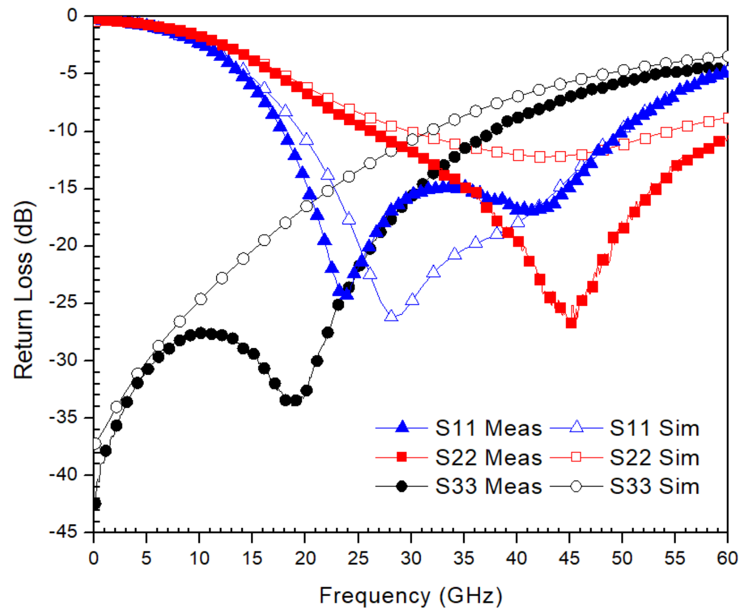


Figure 5.15: Simulated and measured return losses of TX (S_{11}), ANT (S_{22}), and RX (S_{33}) ports.

In measurements, the TX, ANT and RX ports at ports 1, 2 and 3 as shown in Fig. 12, respectively, were connected to the VNA's ports. The ANT_{BAL} and the other RX ports are terminated with on-chip 50-Ohm resistors.

Fig. 5.13 shows simulated and measured isolations between TX and a single-ended RX port (RX+ or RX-) of the mm-wave balanced DUXs with and without grounded center-tap with good agreement between them. As can be seen, the DUX with grounded center-tap provides more than 20 dB improvement in isolation from TX to RX+ or RX- port as compared to that with floating center-tap. The grounded-center-tap DUX provides more than 50 dB isolation from dc-20 GHz and better than 40 dB up to 60 GHz.

Fig. 5.14 shows the simulated and measured insertion losses for the grounded-center-tap DUX between TX-ANT (S_{21}), ANT and single-ended RX (S_{32S}) ports, and ANT and differential RX (S_{32D}) ports. Note that S_{32D} is obtained by adding 3 dB to S_{32S}. Measured S_{21} is less than 6.3 dB from 13-53 GHz and reaches 3.3 dB at 36 GHz. Measured S_{32D} is better than 13.8 dB from 25-57 GHz, reaching 10.8 dB at 40 GHz.

Fig. 5.15 shows the return losses at the TX (S_{11}), ANT (S_{22}), and RX (S_{33}) ports. Measured S_{11}, S_{22}, and S_{33} are better than 10 dB between 18-50 GHz, 10 dB from 25-58 GHz, and better than 10 dB from dc-37 GHz.

Table 5.2 compares the performance of the mm-wave grounded-center-tap balanced DUX with reported quasi-circulators [5, 6, 21]. It is noted that this comparison is not conclusive due to lower operating frequencies of some reported quasi-circulators. The developed mm-wave balanced DUX is the only passive DUX addressing the entire 5G spectrums of 28, 37, 39 GHz, and beyond. It demonstrates the highest isolation (more than 40 dB) across an unprecedented ultra-wide band (dc-60 GHz). It also has the smallest chip size (0.3-mm^2), good return losses, and ease of integration with PA, antenna, and LNA. Although [5] and [6] have lower insertion loss, they are active circuits.It is noted that the insertion loss between ANT and RX can be reduced by 3 dB by using

Table 5.2: Performance Summary and Comparison with Other Quasi-Circulators

	This Work	[21]	[5]	[6]
Technology	0.18-μm BiCMOS	0.25-μm pHEM	90-nm CMOS	0.18-μm CMOS
Freq. (GHz)	25-53	10.2-12.8	14-67	29-31
TX-RX ISO (dB)	>50 (dc-20 GHz) >40 (20-60 GHz)	>35	>12	>12
TX-ANT IL (dB)	$=3.3$ (@ 36 GHz) ≤ 6.3 (13-53 GHz)	≤ 4.5	-3.5 –4.3	≤ 6
ANT-RX IL (dB)	= 10.8 (@ 40 GHz) ≤ 13.8 (25-57 GHz)	≤ 4.5	-9 –1.2	≤ 7.9
S_{11} (dB) S_{22} (dB) S_{33} (dB)	>10 (18-50 GHz) >10 (25-58 GHz) >10 (dc-37 GHz)	>12* >15* >15*	>5* >10* >5*	>6 >5 >11.5
$IP1dB_{TX}$ (dBm)	High (Passive)	High (Passive)	-3	-7
P_{dc} (mW)	0 (Passive)	0 (Passive)	41.8	15
Area (mm^2)	0.3	16	0.93	0.36

*Estimated from figures

another antenna at the ANT_{BAL} port (instead of terminating it with R_L), which can be implemented in systems. Using two such antennas along with a tight coupling between the transformer's coils would ultimately result in lower insertion loss from ANT and RX, leading to improved system performance.

5.4 Conclusion

A new 0.18-μm BiCMOS ultra-wideband mm-wave passive balanced DUX for 5G applications has been developed. The mm-wave DUX combines a lumped-element Wilkinson power divider with a co-planar transformer having its primary coil's center-tap grounded and possesses several unique advantages. Impedance matching is readily obtained at the TX, ANT and RX ports, making it easy to integrate with external PA, antenna, and LNA. The mm-wave DUX allows direct integration with single-ended TX and ANT as well as differential LNA (facilitating rejection of common-mode signals preferred in receivers). Grounded center-tap increases significantly TX-RX isolation, as well as provides well-balanced RX differential waveforms. Enhanced TX-RX isolation is also attained for the harmonics of TX, which in turn, further minimizing disruption of RX from TX. The mm-wave balanced DUX's miniaturization coupled with its high performance, especially isolation and differential RX port, across an ultra-wide bandwidth of 25-53 GHz make it attractive for 5G operations at 28, 37, 39 GHz and beyond, thereby benefiting the development of 5G as well as other mm-wave wireless systems.

6. A FULLY-INTEGRATED 23.5–36.2-GHz FDD TX-RX FRONT-END DUX MODULE ON 0.18-μm BiCMOS FOR FDD 5G RADIOS

6.1 Introduction

Systems on a single chip (SoC) are attractive with lower cost, more functions, and smaller area. Currently, several Time Division Duplex (TDD) fully-integrated transmitting-receiving (TX-RX) front-end modules have been demonstrated [31, 32]. However, frequency-division duplex (FDD) fully-integrated TX-RX front-end DUX module has not been yet reported.

Indeed, surface acoustic wave (SAW) or bulk acoustic wave (BAW) filters can function a duplexer (DUX) perfectly below 10 GHz, while are discrete and hard to operate at millimeter-wave (mm-wave) ranges. Ferrite circulators are bulky and hard to integrated in semiconductor processes. DUXs based on active devices consume huge power to achieve high TX linearity and futher degrading RX noise figure (NF). Although [21] reports a quasci-circulator, the size is narrow-band and not fully-integrated with large chip area. Hence developing a mm-wave FDD fully-integrated TX-RX front-end DUX module is strongly needed for 5G applications.

This dissertation not only demonstrates a wide-band mm-wave fully-integrated TX-RX front-end DUX module, but also provides a design methodology to achieve high TX-RX isolation and directly integrate with DUX, PA, and LNA together. We also consider and overcome the low resistivity of p-type Si substrate, causing TX signal leaking through substrate. Additionally, this proposed architecture can directly integrate with a balance mixer.

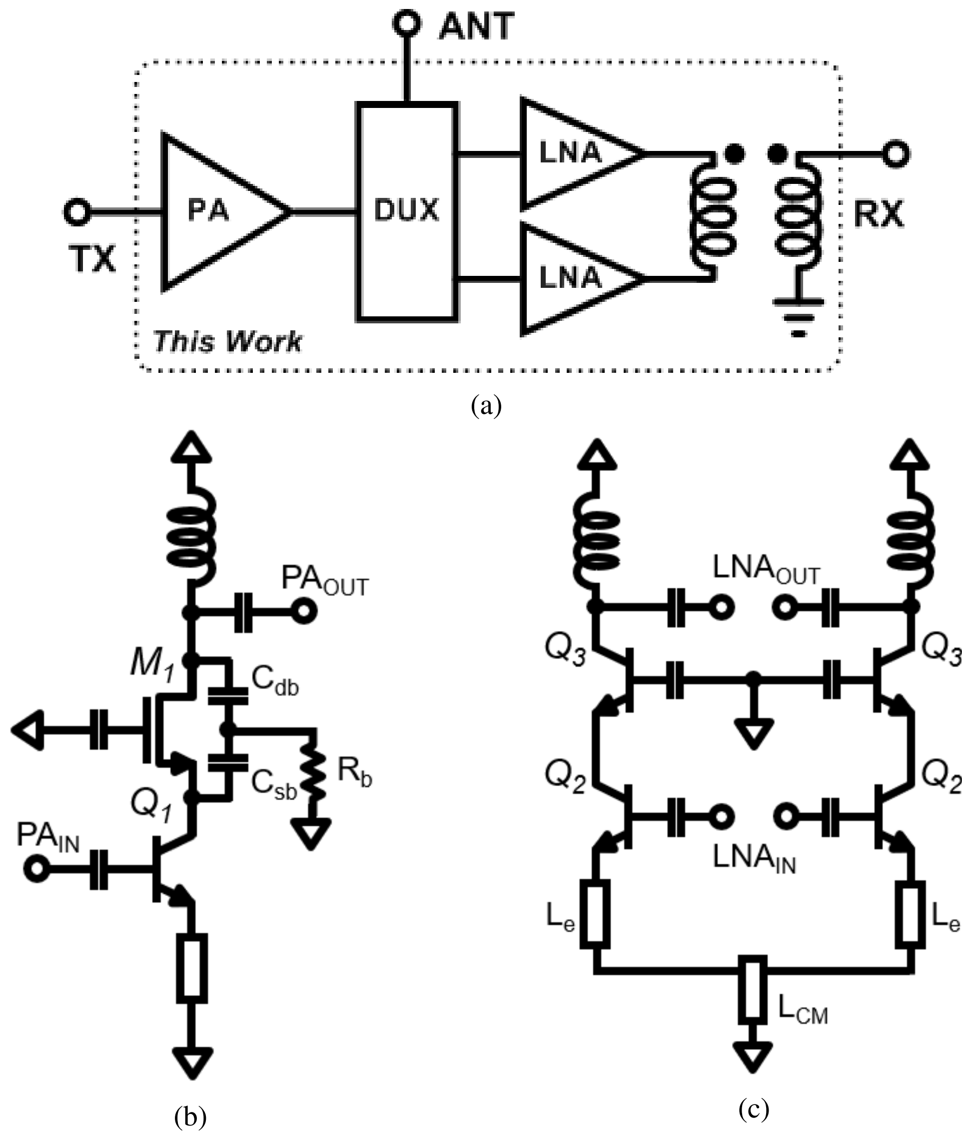
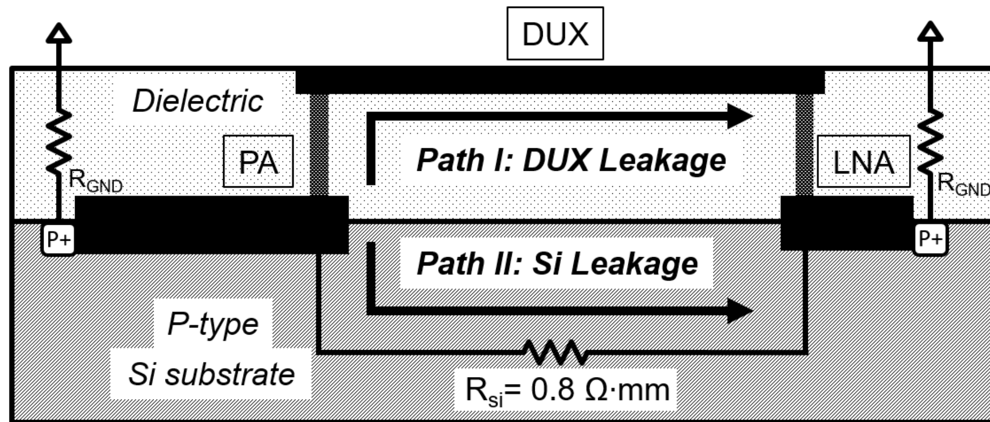


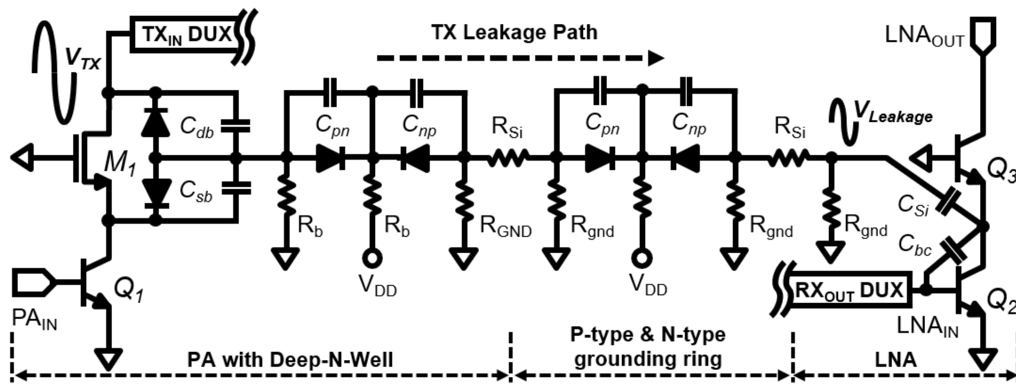
Figure 6.1: Simplified schematic of the proposed (a) TX-RX front-end module system architecture, (b) PA, and (c) LNA.

6.2 System and circuits design

Fig. 6.1a presents the proposed FDD TX-RX front-end DUX module system-level schematic, which has TX, antenna (ANT), and RX port. The module contains a PA, DUX, and differential LNA. DUX consists of a LC-lumped Wilkinson power divider and



(a)



(b)

Figure 6.2: (a) Equivalent circuit used for TX leakage through Si substrate and (b) cross-section of Si substrate including DUX, PA, and LNA.

transformer. RX output is differential. Hence LNA is adopted with differential structure which provide better common-mode signal rejection and have better IM2 performance.

For integrating DUX on a silicon substrate, DUX isolation itself is not the only isolation parameter dictating the entire DUX isolation. Leakage through Si-substrate will is another isolation issue. Generally, PA output has the largest swing (V_{TX}), which will be the main issue causing the leakage to LNA input.

In passive DUX design isolation between TX and RX is critically important when

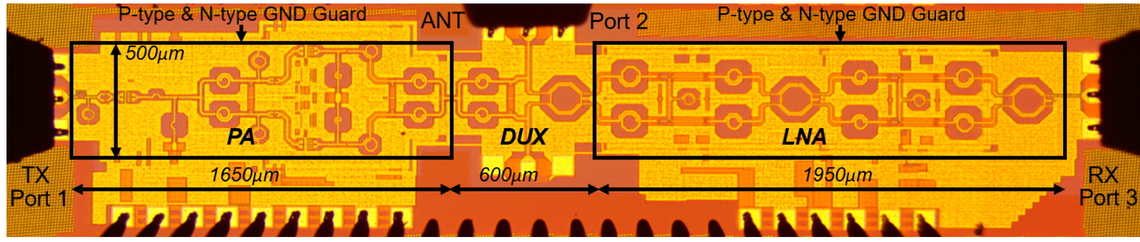


Figure 6.3: Photograph of the fabricated fully-integrated TX-RX front-end DUX module including DUX, PA, and LNA.

passive DUX is integrated with active circuits on Si substrate. More details on Si-leakage behavior will be discussed in the following section.

6.2.1 Duplexer design

In this FDD TX-RX module, we adopt the wide-band millimeter-wave balanced passive EBD DUX consisting of LC-lump wilkinson power divider and 1:1 balun. Central-tap grounding not only can improve isolation, but also make perfectly balanced RX differential signals. This also will enhance balance mixer linearity and suppress the signal distortion. Additionally, LC-lumped Wilkinson power divider can filter out higher frequency signals such as second harmonic. It is noted that the duplicate antenna (ANT_{BAL}) port is terminated with an on-chip 50-Ohm.

6.2.2 PA and LNA design

Fig. 6.1b shows the proposed BiCMOS PA schematic [35], which has two advantages. First, first transistor, HBT, will dominate the transconductance of the whole amplifier and the second transistor, body-floating NMOS, has the more headroom for voltage swing. Second, the body-floating NMOS has better isolation between PA output and Si substrate, leading to suppress the TX leakage through Si substrate. This part will be discussed further in the following section.

PA has two stages and includes Wilkinson power divider as a combiner and divider.

The two main amplifiers in the PA are integrated through lumped-element Wilkinson power divider and combiner, each simulating a low-pass filtering response to suppress the harmonics for improved PAE. Each input transistor (Q_1) in the main amplifiers, as shown in Figure 1, consists of four constituent transistors, each having 0.13-μm emitter width and 10-μm emitter length designed mainly for optimum MAG. The cascode transistors (M_2), each combining four transistors, are selected to have 12 fingers with a unit finger width of 4.5 μm through load-pull simulations for high-output power. The input transistor (Q_1) of the drive amplifier as shown in Figure 1 consists of four transistors with 5-μm emitter length. The cascode transistor (M_2) has 12 fingers with 2.5 μm width each. A 4 K-Ohm resistor (R_b) is used for the body-floating resistor.

Fig. 6.1c shows a unit of the differential LNA. RX chain contains two stage amplifiers to attain higher gain. For suppressing common-mode signals from TX side, matching network between stages also adopts transformer. All transistors in RX chain have one emitter finger (w = 0.13-μm and l = 4-μm), two base fingers, and two collector fingers considering the trade-off between noise characteristic and high frequency gain performance of the transistor. L_{CM} is, as shown in figure , also implemented to suppress the common-mode gain from desensitize LNA inputs.

6.2.3 Si leakage consideration

Due to low resistivity of Si substrate (R_{Si} around 3 Ohm-cm), TX leakage through substrate is also important. Since this TX-RX front-end module is fully integrated with Si substrate, typically the intrinsic resistance of a p-doping Si substrate is low. Hence, TX leakage through Si substrate is obvious, further leading to desensitizing LNA inputs. Hence TX leakage to LNA input ($V_{Leakage}$), as shown in Fig. 6.2a, could be expressed as

$$V_{Leakage} \simeq V_{TX} ISO_{DUX} + V_{TX} ISO_{Si} \tag{6.1}$$

where V_{TX} represents the TX voltage intensity at PA output. In an ideal PA, PA output has the largest swing (V_{TX}). In order to simply the analysis, the largest voltage swing at PA output is only considered. ISO_{DUX} is the TX-RX isolation of DUX itself and ISO_{Si} is the leakage ratio through Si-substrate. It is assumed that DUX isolation (ISO_{DUX}) is 40 dB. Based on equation (6.1), to achieve a total isolation better 40 dB, the TX leakage ratio between PA output and LNA input through Si substrate (ISO_{Si}) should be better than 50 dB. Then the total isolation can achieve 40 dB. In order to achieve high TX-RX isolation, the leakage through Si substrate need to be minimized.

Fig. 6.2b represents the TX leakage path from PA output through Si substrate with the resistivity of Si substrate modeled as R_{Si}. R_{GND} represents the resistance from ground via and contact from Si substrate to the topmost metal, typically value around 1 Ohm. More solid contact between Si substrate and top-layer ground would cause TX leakage connecting to real ground, leading to better isolation (ISO_{Si}). In order to enlarge the impedance between PA output and LNA input, p-type and n-type grounding guard ring are implemented. Besides, the parasitic capacitor (C_{Si}) of the input transistor's in cascode LNA between collector and Si substrate is a main issue causing the leakage. Hence, C_{Si} and C_{bc} should be carefully laid out to suppress leakage.

6.2.4 Design Methodology

Based on the analysis and design above, a design methodology is conceived as follows.

Step 1: Using the proposed wide-band millimeter-wave EBD with center-tap grounding technique to improve isolation between PA output and LNA input

Step 2: Adopting the BiCMOS cascode PA structure, HBT cascoded with body-floating NMOS, for maintaining PA performance and suppress TX leakage through Si substrate

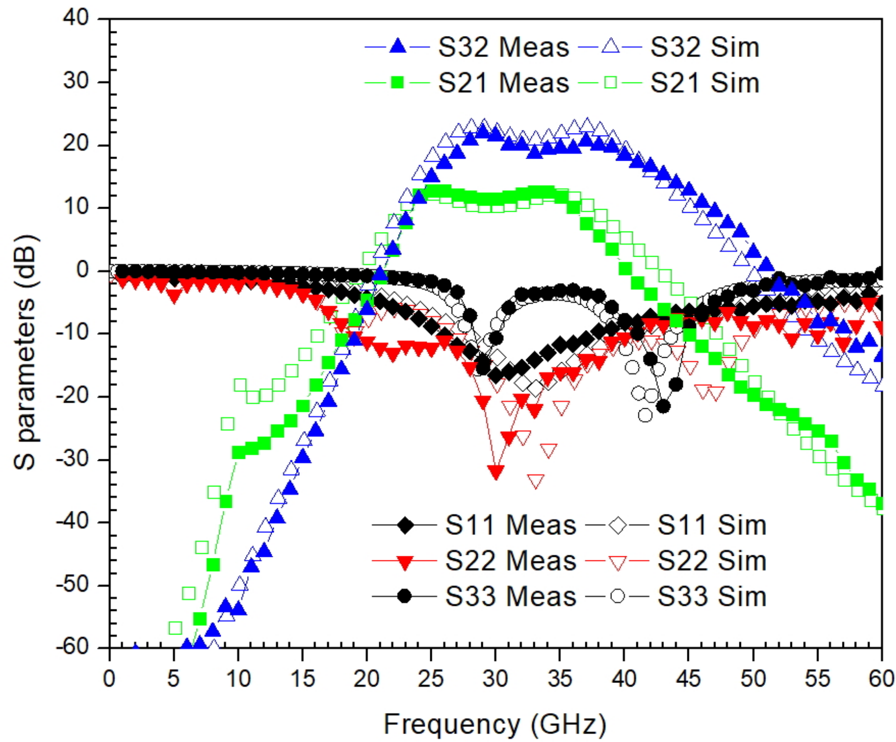


Figure 6.4: Simulated and measured S-parameters of TX-RX front-end DUX module.

Step 3: Design optimized input and output matching networks of LNA for NF and RX gain considerations

Step 4: After completing PA and LNA design, adding n-well and p-well ground surrounding PA and LNA to further suppress the TX leakage through Si substrate.

Step 5: Fine-tune all matching networks between the boundary of DUX, PA, and LNA for achieving high isolation, large TX output power, low NF, and good return losses.

6.3 Measured Results

Fig. 6.3 shows the photo of fabricated circuits using the Tower-Jazz 0.18-μm SBC18H3 process, which occupies 4.2-by-0.5 mm^2 area without the RF and dc pads. All measure-

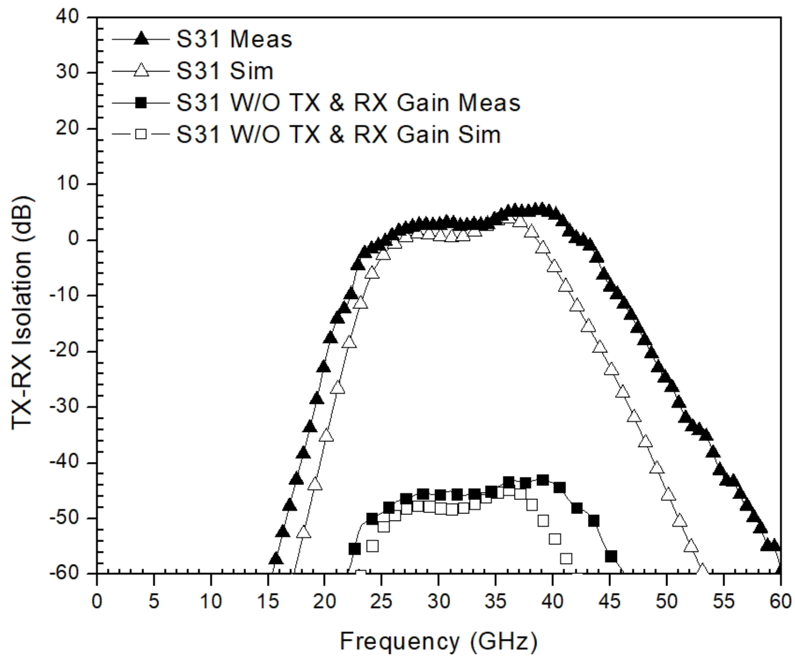


Figure 6.5: Simulated and measured TX-RX isolation of TX-RX front-end DUX module with active gain and without active gain.

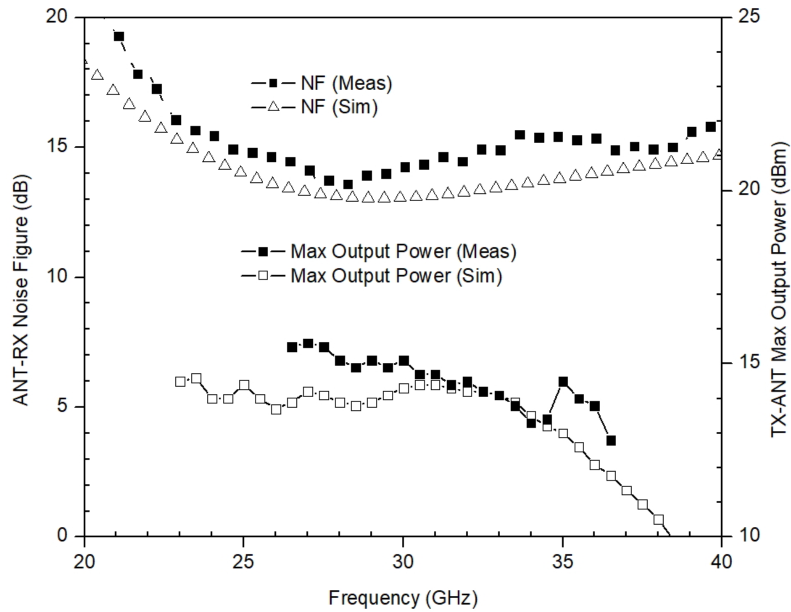


Figure 6.6: Simulated and measured performance of TX-RX front-end module for LNA NF and PA maximum power.

ments were performed by on-wafer probing using Rohde & Schwarz ZVA67 vector network analyzer (VNA). In measurements, the TX, ANT and RX ports at ports 1, 2, and 3 as shown in Fig. 6.3, respectively, were connected to the VNA's ports.

Cadence is used for circuit simulations as well as extracting the parasitic elements produced by the layout. All the passive elements including RF pads, except for MIM capacitors in the process design kit, are simulated using IE3D EM simulator and Kesight ADS momentum.

Two-stage differential LNA totally consumes 12.2 mA dc current with 1.8 V supply voltage (P_{DC}= 22 mW) and two-stage PA takes 129 mA dc current with 3.45 V biasing (P_{DC}= 445 mW).

Fig. 6.4 reports the measured and simulated small-signal S-parameters of this module. The measured and simulated result match very well. The TX gain (S_{21}) is 12.9 dB gain at 30 GHz and has less than 3-dB variation across 23.5-36.2 GHz. It is noted that the TX gain also include 3.5 dB insertion loss from PA output to ANT port. The RX gain (S_{32}) is 19 dB gain at 32.5 GHz and has less than 3-dB variation across 25-40 GHz. It is noted that the RX gain also include 10.8 dB insertion loss from ANT port to LNA inputs. The measured return loss of TX (S_{11}), ANT (S_{22}), and RX ($_{33}$) port are better than 10 dB from 25 to 35 GHz, 10 dB from 25 to 40 GHz, and 10 dB from 28 to 31 GHz, respectively.

Fig. 6.5 shows the TX-RX isolation (S_{31}) with and without active gain. It is noted that DUX has insertion loss of TX and RX path with 3.5 dB and 10.8 dB, respectively. Besides, Fig. 6.4 also shows around 12.5 dB gain on TX path and 19 dB gain on RX path. Hence, the difference is around 45 dB with and without active gain.

First, fig. 6.6 shows the LNA NF and PA linearity. The measured NF within the 3 dB bandwidth ranges between 13.8 and 15 dB, including around 10 dB insertion loss of DUX RX path. The measured and simulated performance of P_{sat}, as a function of frequency, are 13-16 dBm, 15.1-18.1 dBm, whcih include about 3.5 insertion loss for the DUX TX

path.

Table 6.1 compares the performance of the designed TX-RX module with others reported TX-RX modules [21, 31, 32]. This mm-wave wide-band fully-integrated TX-RX front-end module is the only one operated in FDD mode. [31, 32] is operated in TDD mode. [21] is narrow-band and not fully-integrated, with external PA. Our developed module also occupies the smallest chip size (2.1-mm^2).

Table 6.1: Performance Comparison of the TX-RX Front-Ends

		This work	[21]	[31]	[32]
Process		0.18-μm BiCMOS	0.25-μm pHEMT	45-nm CMOS SOI	0.13-μm BiCMOS
Freq. (GHz)		23.5-36.2	10.25-12.6	24-30	30-40
Scheme		FDD	FDD	TDD	TDD
$ISO_{TX\text{-}RX}$ (dB)		42*	35*	–	–
NF (dB)		13.8	5.0**	3.7	8.4
Gain (dB)	*RX*	19.0	-4.7	16	17
	TX	12.9	1.5	16.5	14
P_{sat} (dBm)	*RX*	–	–	–	–
	TX	15	–	12.5	22.5
OP_{1dB} (dBm)	*RX*	-0.7	–	1.0	–
	TX	13.3	31	8.0	20.5
P_{DC} (mW)	*RX*	12	–	54	528
	TX	440	4205	100	1587
Size (mm^2)		2.1	25	3	7
Fully-Integrated		Yes	No	Yes	Yes

* Without active devices gain
** Without LNA Noise

6.4 Conclusion

This dissertation reports the first mm-wave wide-band fully-integrated FDD TX-RX front-end DUX module, including internal DUX, PA, and LNA, which has flat gain on TX and RX path and better than 42 dB isolation between PA output and LNA input across 23.5-36.2 GHz. At 28 GHz, the module has minimum 13.8 dB NF for the RX path. The PA provide better than 12 dBm output power at ANT port. This work considers both of the TX leakage through DUX path and the suppression of the leakage through the path underneath the Si substrate. A design methodology is also suggested. This circuit would benefit SoC development for FDD 5G communication and others FDD millimeter-wave wireless systems as well.

7. A POWER-EFFICIENT 28-GHz HIGH-ISOLATION FULLY-INTEGRATED FDD TX-RX FRONT-END DUX MODULE WITH INTERNAL DUPLEXER, POWER AMPLIFIER, AND LOW NOISE AMPLIFIER ON 0.18-μm BiCMOS FOR 5G APPLICATIONS

7.1 Introduction

Systems on a single chip (SoC) are attractive with lower cost, more functions, and smaller area. Presently, several Time Division Duplex (TDD) fully-integrated transmitting-receiving (TX-RX) front-end modules have been demonstrated [31, 32]. However, few frequency-division duplex (FDD) fully-integrated TX-RX front-end modules are reported.

Indeed, surface acoustic wave (SAW) or bulk acoustic wave (BAW) filters can be used to produce a duplexer (DUX) functioning well below 10 GHz, while are discrete and hard to operate at millimeter-wave (mm-wave) ranges. Ferrite circulators are bulky and hard to integrated with semiconductor process. DUXs based on active devices consume huge power to achieve high TX linearity and further degrading RX noise figure (NF). [21] reports a quasci-circulator, which is narrow-band and not fully-integrated with large chip area. Although the previous chapter mention a mm-wave fully-integrated EBD, it suffers from the imbalance impedance problem between ANT and ANT_{BAL} port, especially while being used in practice. Hence developing a high-performance mm-wave FDD fully-integrated TX-RX front-end DUX module is urgently needed for 5G applications.

This dissertation presents the design of a new 28 GHz mm-wave DUX, combing the both advantages of passive DUX and active cancellation, on 0.18-μm BiCMOS. The developed mm-wave DUX also includes internal PA and LNA. It provides inherent matching at TX, RX and ANT ports, high TX-RX isolation, low insertion loss on RX and TX paths, and power efficient. Low resistivity of p-type Si substrate is also considered in

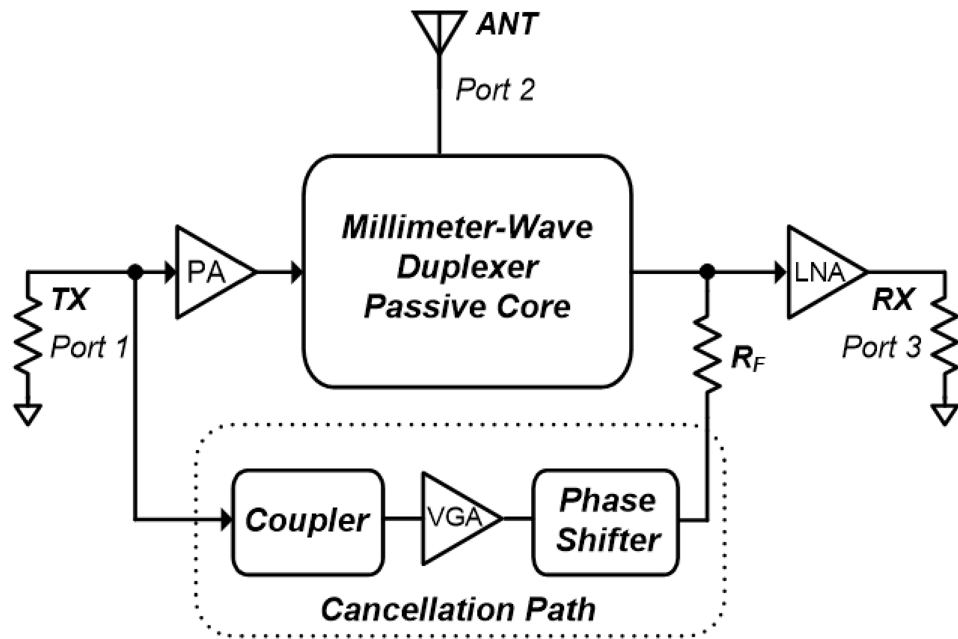


Figure 7.1: The proposed narrow-band DUX module architecture.

further suppression of leakage signals. A methodology of designing the mm-wave DUX is demonstrated to achieve high TX gain, low NF, high TX-RX isolation, and power-efficient.

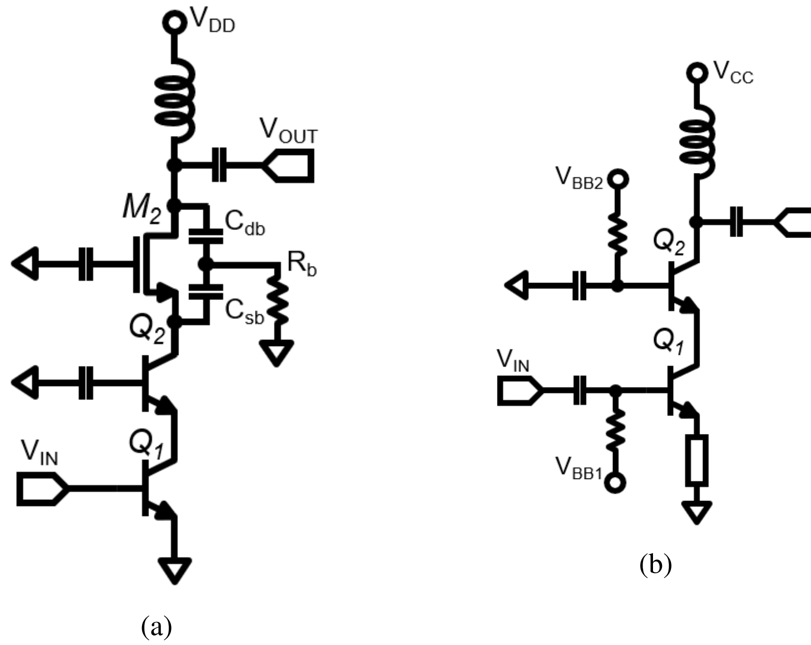


Figure 7.2: Simplified schematic of (a) PA and (b) LNA.

7.2 System Architecture and Design

Fig. 7.1 shows the structure of this mm-wave narrow-band FDD TX-RX DUX module, which includes internal DUX, PA, LNA, and cancellation path. The cancellation path is implemented to improve the TX-RX isolation further. A Wilkinson power divider is used in the passive DUX since there is around 40 dB isolation between the two balance ports. In this design, a 28 GHz LC-lumped Wilkinson power divide is adopted which has a low-pass profile to filter out unwanted higher-frequency signals.

Fig. 7.2a shows the PA schematic, adopting three cascode structures (HBT-HBT with a body-floating NMOS). This structure has decent gain, large output power, and high linearity as mentioned earlier. HBT transistor (Q_1, Q_2), as shown in Fig. 7.2a, consists of four constituent transistors, each having 0.13-μm emitter width and 10-μm emitter length designed mainly for optimum MAG. The third transistors (M_3), each combining

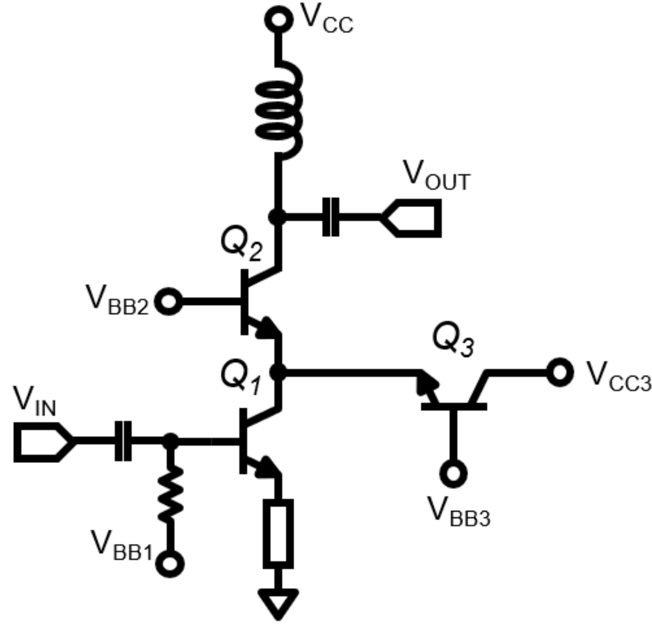


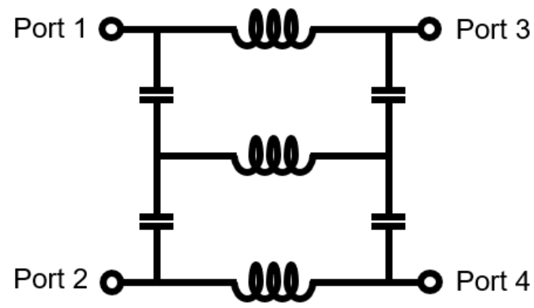
Figure 7.3: Current steering gain cell of the variable gain amplifier (VGA).

four transistors, are selected to have 12 fingers with a unit finger width of 4.5 μm through load-pull simulations for high-output power. A 4K-Ohm resistor (R_b) is used for the body-floating resistor.

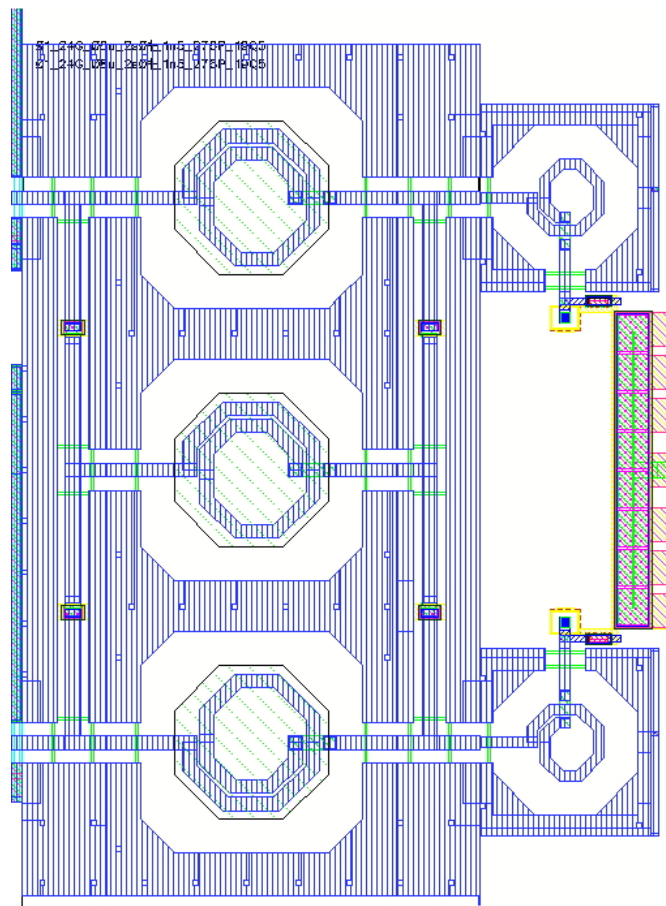
Fig. 7.2b depicts a unit of the cascode LNA. All transistors in RX chain have one emitter finger ($w = 0.13\mu$m and $l = 4\mu$m), two base fingers, and two collector fingers considering the trade-off between noise characteristic and high frequency gain performance of the transistor.

On the cancellation path, the first component is a coupler to sense the TX signal intensity from the PA input. In this design, we design a co-planar balun with 0.4 coupling factor (k) to function as a coupler.

The second component on the cancellation path is a current-steering variable gain amplifier (VGA), as shown in Fig. 7.3. All transistors in Fig. 7.3 have one emitter finger ($w = 0.13\mu$m and $l = 4\mu$m), two base fingers, and two collector fingers considering



(a)



(b)

Figure 7.4: (a) Schematic and (b) layout of the LC-lumped reflection-type phase-shifter.

the trade-off between noise characteristic and high frequency gain performance of the transistor. When Q_3, as shown in 7.3, turns on, partial ac currents will flow into the emitter of Q_3, resulting in less voltage gain. This is the mechanism to control the voltage gain by V_{BB3}.

In order to control the phase of the compensation signal, a phase shifter (PS) is needed for this system. We adopt a reflect-type (RT) PS, which is a continuous-type analog PS. Fig. 7.4b shows the layout of this RT-PS. Conventional RT-PS uses a coupler implemented with a distributed circuit. To minimize the chip size, the coupler is implemented with lumped elements as shown in Fig. 7.4a. More detailed about the design procedure will be addressed in the following section.

7.2.1 Linearity Analysis on Cancellation

A function of DUX is to suppress TX leakage, which is important especially for TX operating in maximum output power situation such as 23 dBm at the PA output. Hence, the cancellation is designed in the condition, under which PA is at maximum power mode. In the condition of PA operating at maximum output range, the VGA would drain the most current. When PA operates at less power range such as 10 dBm, VGA requires less power consumption. It is noted that if the Wilkinson power divider has higher TX-RX isolation, VGA would have less power consumption.

7.2.2 Phase Analysis on Cancellation

As shown in Fig. 7.4a, Port 1 and Port 2 are the input and through port, respectively. Port 3 and Port 4 are terminated with varactors, which idelly behaves as a capacitor causing total reflections back to the these ports and then then through Port 2. In order to choose the suitable LC value at 28 GHz, the following two equations are used

$$L = Z_0/(2\pi f_0) \tag{7.1}$$

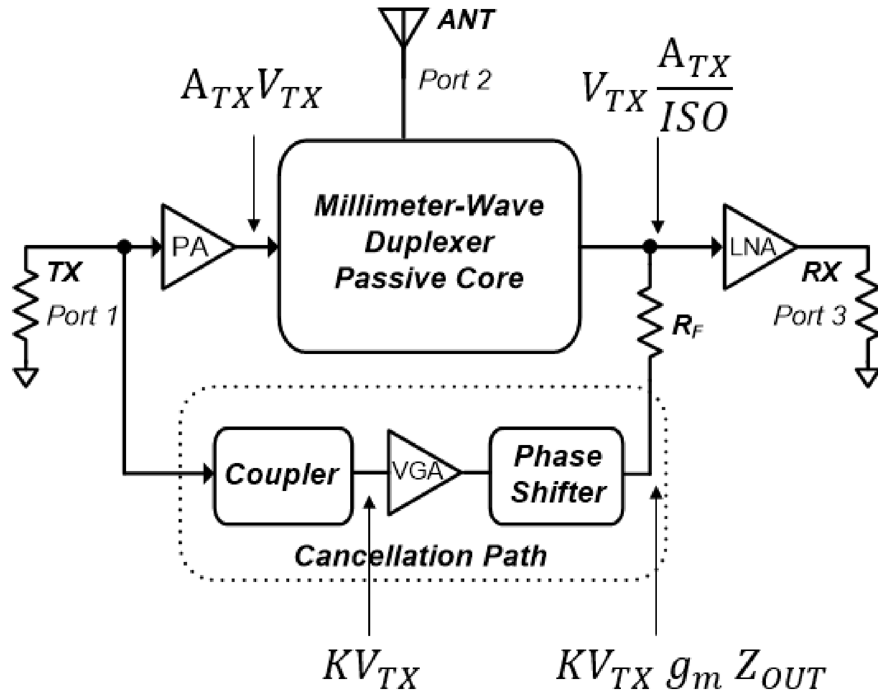


Figure 7.5: Block diagram of the narrow-band DUX module showing TX signal amplitudes in the TX and cancellation paths.

$$C_0 = 1/(2\pi f_0 Z_0) \tag{7.2}$$

where Z_0 is terminating impedance and f_0 is the design frequency.

7.2.3 Leakage Amplitude on Cancellation Path

Fig. 7.5 shows the contributions of TX signal at LNA input from the leakage path and the cancellation path. The basic operation of amplitude cancellation can be illustrated with the aid of Fig. 7.5 and can be expressed by

$$\frac{V_{TX}}{2}\frac{A_{TX}}{ISO} = \frac{V_{TX}}{2} k g_m Z_{out} \frac{Z_{in}}{R_F + Z_{in}} \tag{7.3}$$

where V_{TX} is signal intensity at PA input. Also we can write the transconductance (g_m) of VGA as

$$g_m = \frac{A_{TX}}{ISO}\frac{1}{k}\frac{R_F + Z_{in}}{Z_{out}Z_{in}} \tag{7.4}$$

7.2.4 Noise Figure Consideration and Design

In order to understand completely the NF and hence possibly minimizing it, the NF contributions from all components in the TX-RX front-end DUX are analyzed. The total NF of the whole TX-RX front-end DUX can be described as [38]

$$NF = NF_{LNA} + \frac{R_S}{R_F} + \frac{2KTg_m Z_{In}^2 \alpha^2 A_{LNA}^2}{4KTR_s A_{LNA}^2} + NF_{R_s-TX} + NF_{PA} \tag{7.5}$$

There are five terms in (7.5). The first term, NF_{LNA}, represents the NF of the cascode LNA. For second term, R_S/R_F, means the noise contribution from the feedback R_F. The third term is contributed by the VGA transistors. For simplicity without loss of generality, the structure of VGA is assumed as a common source amplifier. The last two terms are from the source resistor of TX port and PA transistors, respectively. However, from the system architecture, the coupler of cancellation path only couples around 10 % of the signal from the TX input, equal to -10 dB coupling. Hence the last two terms could be reasonably neglected and expressed as:

$$NF = NF_{LNA} + \frac{R_S}{R_F} + \frac{2KTg_m Z_{In}^2 \alpha^2 A_{LNA}^2}{4KTR_s A_{LNA}^2} \tag{7.6}$$

Which is then simplified as

$$NF = NF_{LNA} + \frac{R_S}{R_F} + \frac{g_m}{2R_s} Z_{In}^2 \alpha^2 \tag{7.7}$$

Substitute (7.4) into (7.6) to get

$$NF = NF_{LNA} + \frac{R_S}{R_F} + \frac{\alpha^2 Z_{In}^2}{2R_s} \frac{A_{TX}}{ISO} \frac{1}{k} \frac{R_F + Z_{in}}{Z_{out} Z_{in}} \tag{7.8}$$

$$NF(R_F) = NF_{LNA} + \frac{R_S}{R_F} + \frac{\alpha^2}{2R_s} \frac{A_{TX}}{ISO} \frac{R_F + Z_{in}}{k} \frac{Z_{in}}{Z_{out}} \tag{7.9}$$

when Z_{in} is close to R_s, we can get

$$NF(R_F) = NF_{LNA} + \frac{R_S}{R_F} + \frac{\alpha^2}{2} \frac{A_{TX}}{ISO} \frac{R_F + R_s}{k} \frac{1}{Z_{out}} \tag{7.10}$$

Another design point is the feeding back position. It is related to α, which means the ratio of noise from VGA injecting into LNA input. Fig. 7.6a shows the first way to feedback, which all the noise from the VGA transistors will inject into LNA input ($\alpha = 1$). Fig. 7.6b shows the second way to feedback, in which only partial noise caused by the cancellation path will inject into LNA input ($\alpha = 0.7$). Fig. 7.7 shows NF_{min} over frequency in three different conditions. First condition is VGA off, having the lowest NF_{min}. When $\alpha = 1$, direct feedback at LNA input, will degrade NF more than feedback before input matching network ($\alpha = 0.7$). In this observation, it suggests feeding back before LNA input matching network will have better NF performance.

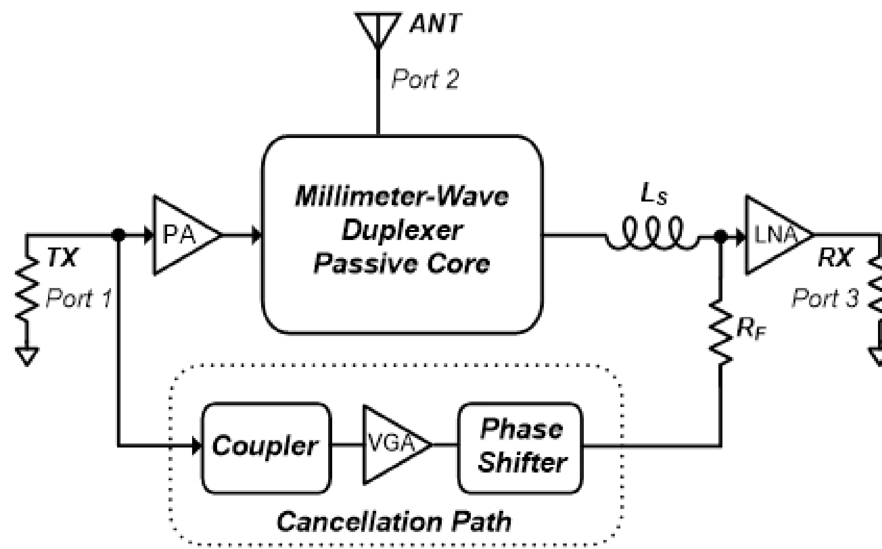
In (7.10), the third term is reverse proportional to R_F. But the fourth term is direct relationship with R_F. It means that it exhibits a minimum value for R_F variance. Therefore,

we can differentiate it and let it equal to zero to get the following equations

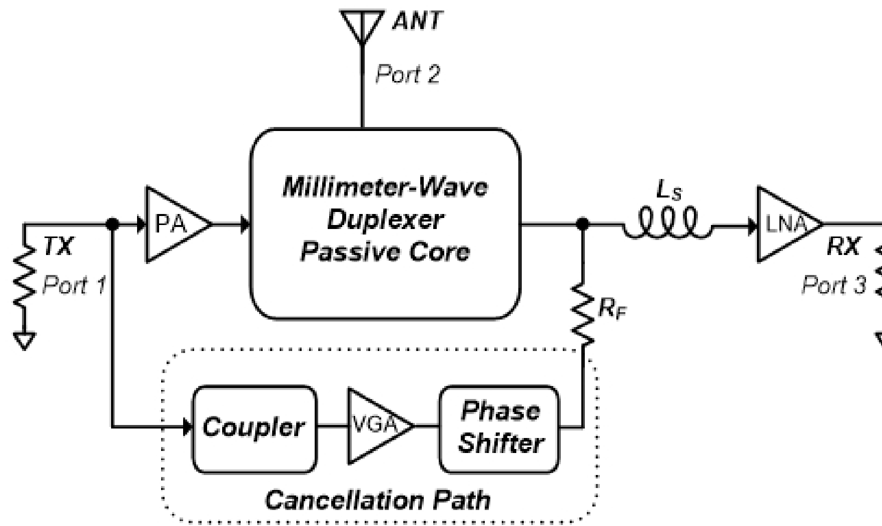
$$\frac{\partial NF(R_F)}{\partial R_F} = -\frac{R_S}{R_F^2} + \frac{\alpha^2}{2}\frac{A_{TX}}{ISO}\frac{1}{k}\frac{1}{Z_{out}} = 0 \tag{7.11}$$

$$R_F = \sqrt{R_S \frac{2}{\alpha^2}\frac{ISO}{A_{TX}} k Z_{out}} \tag{7.12}$$

Equation (7.12) suggests that this specific feedback resistor (R_F) value can achieve high isolation and low NF at the same time. We also verify that this value is really close to the design value (around 1K-Ohm). This design methodology, analyzing the amplitude and NF contribution, indeed provide an efficient way to design this module.



(a)



(b)

Figure 7.6: Schematic of showing feeding (a) after series inductor (L_S) and (b) before series inductor (L_S).

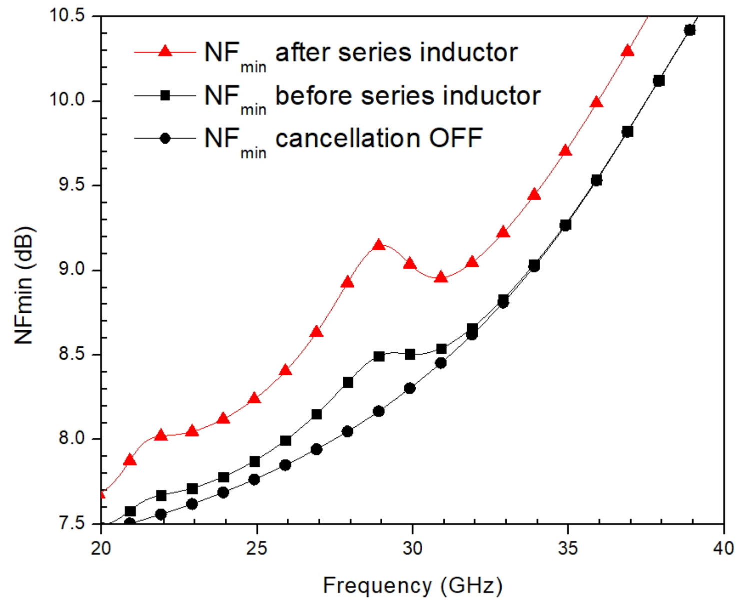


Figure 7.7: Simulated NF without cancellation, feeding after and before series inductor (L_S) when VGA is enabled.

7.2.5 Design Methodology

Based on the analysis and design above, the following design methodology is suggested as follows.

Step-1. Design a LC-lumped Wilkinson power divider at a wanted frequency such as 28 GHz.

Step-2. Design a narrow-band PA and connect to one of the balance port in the Wilkinson power divider.

Step-3. Design a narrow-band LNA and connect to the other balance port in the Wilkinson power divider.

Step-4. Design the leakage cancellation at the condition that PA input is 0 dBm.

Step-5. Design a coupler for cancellation path such as a transformer with 0.4 coupling

factor (k).

Step-6. Using Eq (7.4) to determine the transconductance (g_m) of the current-steering VGA

Step-7. Using Eq (7.12) to determine the feed-back resistor value (R_F).

Step-8. Connect all building blocks together to determine the phase of cancellation signal.

Step-9. Design a RT-PS to modify the cancellation signal which is 180-deg out-of-phase with TX leakage

Step-10. Fine-tune all building blocks and matching networks to achieve high isolation, high gain, and low NF at the same time

7.3 Measurement Results

Fig. 7.8 shows a photo of the fabricated circuits using the Tower-Jazz 0.18-μm SBC18H3 process, occupying 2-mm^2 area without the RF and dc pads. All measurements were performed by on-wafer probing using Rohde & Schwarz ZVA67 vector network analyzer (VNA). In measurements, the TX, ANT and RX ports at ports 1, 2 and 3 as shown in Fig. 7.8, respectively, were connected to the VNA's ports.

Cadence is used for circuit simulations as well as extracting the parasitic elements produced by the layout. All the passive elements including RF pads, except for MIM capacitors in the process design kit, are simulated using IE3D EM simulator and Keysight ADS momentum.

Single-end LNA consumes 2.6 mA dc current with 1.8 V supply voltage (P_{DC}= 4.68 mW) and one-stage PA takes 94 mA dc current with 3.45 V biasing (P_{DC}= 330 mW).

When PA input is 0 dBm, the active circuit of cancellation path will drain 4.6 mA with 1.8 V biasing (P_{DC}= 8.28 mW).

Fig. 7.9 reports the simulated small-signal S-parameters of this module. The TX gain (S_{21}) is 15.6 dB gain at 28 GHz. It is noted that the TX gain also includes 3.5 dB insertion loss from PA output to ANT port. The RX gain (S_{32}) is 18 dB gain at 28 GHz. It is noted that RX gain also includes 3.5 dB insertion loss from ANT port to LNA inputs. The measured return loss of TX (S_{11}), ANT (S_{22}), and RX ($_{33}$) port are better than 10 dB from 27 to 29 GHz, 10 dB from 23 to 29 GHz, and 10 dB from 27.5 to 28.5 GHz, respectively.

Fig. 7.10 shows TX-RX isolation (S_{31}) with and without cancellation. It is noted that this figured excludes the TX gain, RX gain, insertion loss between PA output and ANT port, and insertion loss between ANT port and LNA input. When cancellation is off, the Wilkinson power divider can provide around 50 dB isolation. When cancellation is enabled, it can enhance isolation by 25 dB (50%). From this comparison, we can know that this proposed circuit indeed can significantly improve the isolation between PA output and LNA input.

Fig. 7.11 shows the NF of the RX path. When the cancellation is off, the minimum NF is 8.1 dB at 28 GHz. When cancellation is enabled, the minimum NF is 8.4 dB at 28 GHz. In other words, the cancellation path only degrades the NF by 0.3 dB. It implies that the proposed design methodology indeed can achieve high isolation and low NF at the same time.

Table 7.1 compares the performance of the designed TX-RX module with others reported TX-RX modules [31, 32]. This mm-wave wide-band fully-integrated TX-RX front-end module has the lowest NF in FDD TX-RX module. [31, 32] are operated in TDD mode. This module occupies the smallest chip size (2-mm^2).

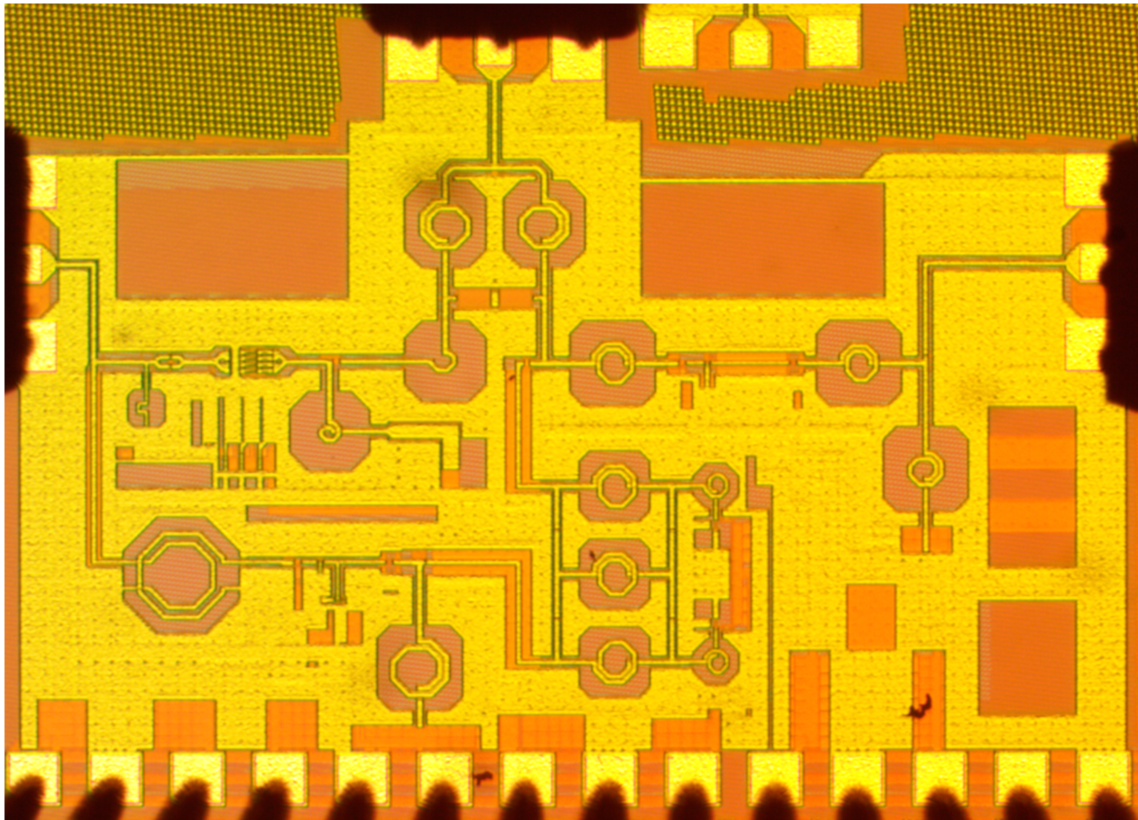


Figure 7.8: Photograph of the FDD TX-RX front-end DUX module.

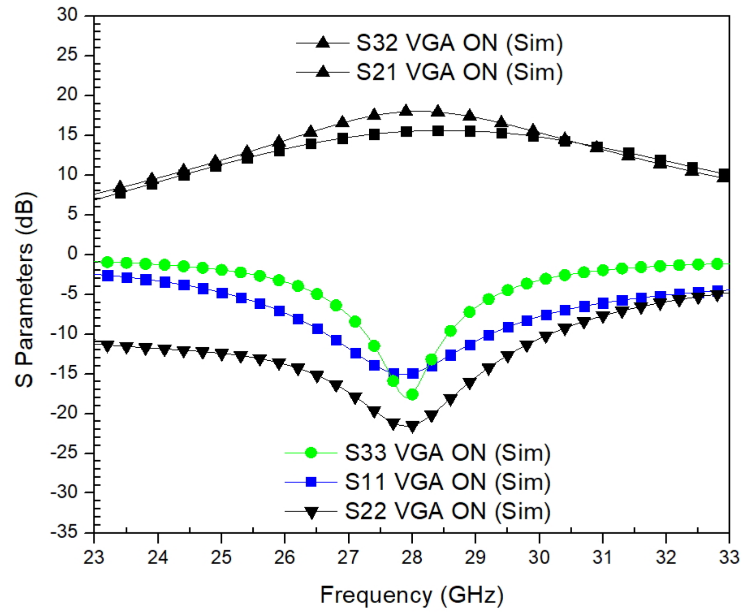


Figure 7.9: Simulated S-parameters.

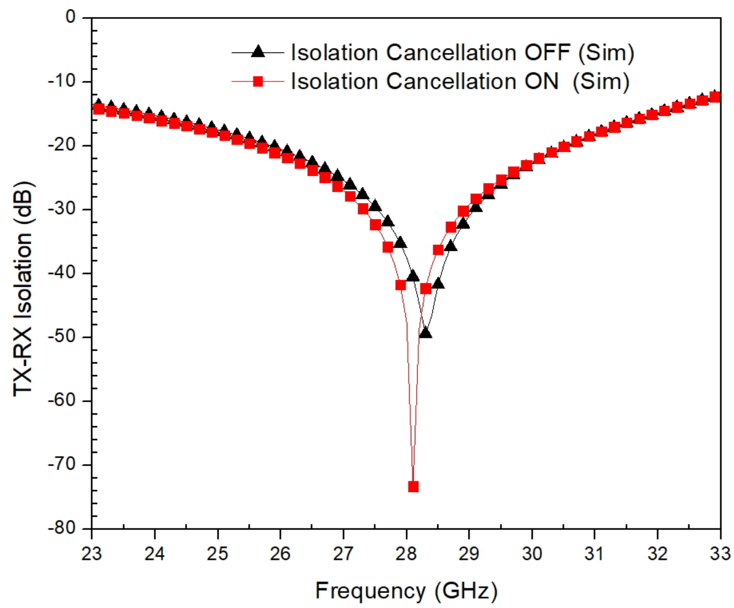


Figure 7.10: Simulated TX-RX isolation with and without cancellation technique.

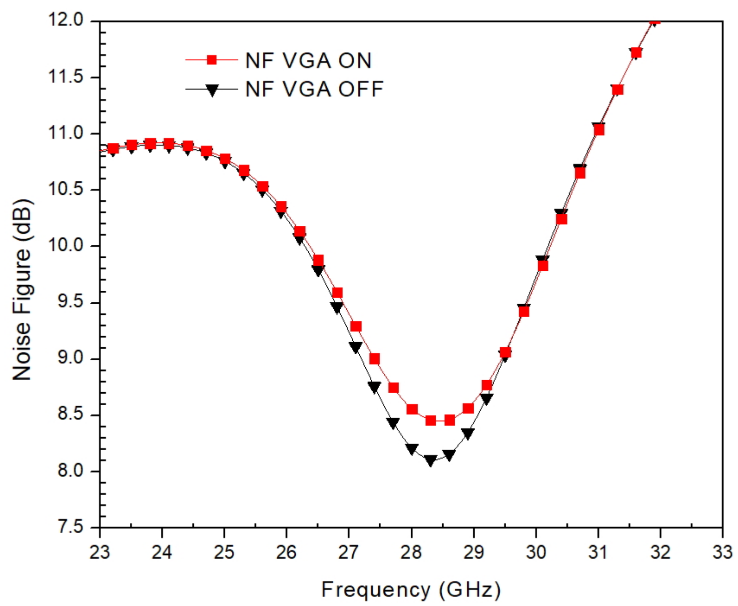


Figure 7.11: Simulated NF with and without cancellation technique.

Table 7.1: Performance Comparison of the TX-RX Front-Ends

		This work	Work in Chapter-6	[31]	[32]
Process		0.18-μm BiCMOS	0.18-μm BiCMOS	45-nm CMOS SOI	0.13-μm BiCMOS
Freq. (GHz)		26-30	23.5-36.2	24-30	30-40
Scheme		FDD	FDD	TDD	TDD
ISO_{TX-RX} (dB)		65*	42*	–	–
NF (dB)		8.5	13.8	3.7	8.4
Gain (dB)	*RX*	18.0	19.0	16	17
	TX	15.6	12.9	16.5	14
P_{sat} (dBm)	*RX*	–	–	–	–
	TX	15.3	15	12.5	22.5
OP_{1dB} (dBm)	*RX*	-6.8	-0.7	1.0	–
	TX	13.3	13	8.0	20.5
P_{DC} (mW)	*RX*	4.68	12	54	528
	TX	330	440	100	1587
	DUX	8.28	0	–	–
Size (mm^2)		2	2.1	3	7

* Without active devices gain

7.4 Conclusion

A mm-wave narrow-band fully-integrated FDD TX-RX front-end DUX module, including DUX, PA, and LNA, has been demonstrated, which has high gain on TX and RX path and better than 60 dB isolation between PA output and LNA input with cancellation technique. At 28 GHz, the module has minimum 8.5 dB NF for the RX path. PA provide better than 10 dBm output power at ANT port. This work only considers the TX leakage through DUX path but also through the path underneath the Si substrate. A design methodology is also suggested for achieving high isolation, good NF, and power efficient at the same time. This FDD TX-RX module would benefit SoC development for FDD 5G communication and other FDD millimeter-wave wireless systems as well.

8. CONCLUSION

8.1 Dissertation Summary

High demands for numerous wireless applications in our lives have pushed engineers and scientists to develop advanced technologies for people's smart life-styles. It gives rise to new applications in microwave and mm-wave ranges, resulting in drawing high attention for developing new wireless communication systems. The great merits of silicon technologies drive aggressively the development of microwave and mm-wave components and systems. However, some challenges still remain.

In this dissertation, several promising techniques and circuit architectures manifesting unprecedented performance have been proposed and validated for developing microwave and mm-wave circuits and systems using a commercial SiGe BiCMOS process.

In Chapter 2, the best-performance PA of four considered combinations implements a SiGe HBT for the input transistor, which dominantly provides large transconductance to amplify the input signals, and a NMOS with body-floating for the output transistor, which has reduced parasitics and better power-handling ability. This PA attains 15.7-dB gain, 19.6-dBm P_{sat}, 17.5-dBm OP1dB, and 28.8 % maximum PAE at 28 GHz for 5G applications.

Chapter 3 reports the design and performance of a new 0.18-μm SiGe BiCMOS PA utilizing both HBT and body-floating NMOS in a cascode configuration. The high fT/fmax of the HBT together with the large voltage swing of the NMOS and the advantages of the body-floating technique are exploited to provide relatively flat gain and high linearity over a wide frequency range. The PA provides P_{sat} of over 16.5-25.5GHz. At 24 GHz, the PA delivers 20.8 dBm PAE of 13.5-23%, and relatively flat gain of 19.5$\pm$1.5 dB 18.5-20.8 dBm, OP1dB of 16.6$\pm$1.5 dB dBm, maximum P_{sat} with 18 dBm OP1dB, 23%

maximum PAE, and 20 dB gain.

In Chapter 4, a new amplifier structure is proposed, which exploits both advantages of HBT, NMOS, body-floating technique, and stacked amplifier to achieve high maximum output power and high gain. The second HBT could improve frequency response and maximum available power gain. The stacked amplifier technique could create more headroom for voltage swing. As a result, this circuit can achieve more 30-dB gain and 23 dBm maximum output power in bandwidth. At 28 GHz, PA has 25 dBm maximum output power and 34 dB gain with 18 % power efficiency.

Chapter 5 demonstrates a mm-wave duplexer that has inherent matching at TX, RX and ANT ports, high TX-RX isolation, and highly balanced differential RX waveforms, and is ready for direct integration with a differential low-noise amplifier. Analysis has been performed to confirm the DUX's characteristics and assess its performance. Measured isolation from TX to each single-ended RX port is higher than 50 and 40 dB from dc-20 GHz and dc-60 GHz, respectively. Measured insertion loss from TX to antenna is better than 6.3 dB across 13-53 GHz. Measured insertion loss from ANT to differential RX port is lower than 13.8 dB from 25-57 GHz with 10.8 dB at 40 GHz. The core chip only occupies 0.3-mm^2

In Chapter 6, a 23.5–36.2-GHz fully-integrated FDD TX-RX front-end DUX module, containing DUX, PA, and LNA, is developed and demonstrated on a single Si-substrate. The isolation from TX to RX, without PA and LNA gain, can achieve more than 42 dB over 13 GHz bandwidth. For the RX path, LNA provides better than 19 dB gain with the minimum 13.8 dB NF at 28 GHz. On the TX path, PA has over 12.9 dB gain with 10 dBm maximum output power (P_{sat}). The TX signals leakage through Si-substrate is also considered and suppressed in this TX-RX module design. The fully-integrated TX-RX module only occupies 2.1-mm^2 without DC and RF pads.

In Chapter 7, a 28 GHz fully-integrated FDD TX-RX front-end module is presented.

This module can achieve 70 dB high isolation between TX and RX. Besides, it has 15.6 dB gain on TX gain and 18 dB on RX gain with good return losses for all ports. Especially, at 28 GHz,this circuit has minimum 8.5 dB NF, which includes the DUX RX loss, LNA, and VGA noise. The cancellation path only consumes 10-mW. This TX-RX front-end module also has small chip size with 2-mm^2 without DC and RF pads.

The circuits and TX-RX front-end DUX modules developed in this dissertation represent new contributions for mm-wave integrated-circuit systems and promise to advance the wireless communication and sensing technologies, especially for 5G and other wireless applications beyond 5G including 6G and others.

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