MIXED-MODE IC DESIGN TECHNIQUES FOR SPECTRUM SHARING

A Dissertation

by

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Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

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May 2021

Major Subject: Electrical Engineering

ABSTRACT

With the development in wireless communication technique, new wireless services with high demand of frequency band resources are emerging every day. The emergence of these new services further aggregates the problem of spectral congestion in radio frequency spectrum. Spectrum sharing or dynamic spectrum access with cognitive radio, as one of the most promising solution has drawn great interest from global research resources.

Spectrum sharing, as the most essential technique in cognitive radio, will fundamentally improve the spectral efficiency. Compared with conventional wireless communication services, spectrum sharing based system requires the capability of co-existence with in-band interferences before baseband ADC.

Although spectrum sharing has been proved possible in code domain with direct sequence spread spectrum (DSSS) technique, this technique has two main issues to alleviate before coming into industry: spectral leakage to adjacent channel due to binary pseudo random sequence and need for accurate synchronization.

This dissertation introduces the solutions to the two main problems in analog DSSS system. In the first phase of this project, a sinusoid-like pseudo random sequence based modulator/demodulator system is designed to alleviate the adjacent channel leakage issue of conventional DSSS system. In the second phase of this project, a mixed signal synchronization scheme for DSSS system is designed to accurate synchronize the received signal with the reference signal in receiver.

The two mixed signal IC solutions are not restricted to any communication standard or applications, but can be applied to existing applications and new radio services in the era of 5G and 6G.

DEDICATION

To my wife and parents

ACKNOWLEDGEMENTS

First of all, I would like to thank my advisor, Professor Jose Silva-Martinez from the bottom of my heart. It was Dr. Silva to offer me the opportunity to work in the field I fell in love with. It was Dr. Silva to guide me through the difficulties, and encourage me when I felt uncertain and less confident. It was Dr. Silva to provide me the valuable advises both on my research and my career plan. It was also Dr. Silva to set an example of an outstanding person that I want to become in the future. I am always impressed by his spirit of innovation, his smart way of thinking and his dedication to this academic field. I am really grateful and honored to work with him and receive advices along my entire Ph.D. program.

I would like to thank Professor Aydin Ilker Karsilayan for his valuable suggestions on my research. I also would like to thank my committee member, Professor Jiang Hu, Professor Jay R. Porter for their comments and sparing time to serve on my graduate committee.

I feel honored to be part of the AMSC group, and would like to thank Qiyuan Liu, Dadian Zhou, Suraj Prakash, Sungjun Yoon and Tanwei Yan for their friendship. In particular, I want to thank Tanwei Yan for the many course works we worked as a team and the collaborations we had with each other. I want to thank Sungjun Yoon for all the help you provided on working in a TA position. Last but not least I want to thank Ella Gallagher for her always kind help and sense of humor.

I would like to express my gratitude to the Department of Electrical & Computer Engineering of Texas A&M University for providing such a good environment for academic research, and for offering such a comprehensive course work that prepares me for my career. In particular, I want to thank Professor Edgar Sanchez-Sinencio for offering the course of Active Network synthesis and his great insights in filter designs. I want to thank Professor Kamran Entesari for offering the course of Integrated CMOS RF circuit and his great sharing of knowledge in RF IC designs. I want to thank Professor Sebastian Hoyos for offering the course of Mixed-signal interfaces and his deep understanding of data converters. These courses laid a solid basis of my knowledge and inspired me in my research.

Outside of Texas A&M University, I also want to thank Dr. Christopher T. Rodenbeck for the valuable advices on my research and his collaboration with our group.

Finally, I want express my deepest appreciation for my wife and my parents. I want to thank my wife Jingyi Zhang for the kind company with me for these ten years. It was her to give me the understanding and tolerance for focusing on my research and study and not being a competent husband, it was her to encourage me for thousands of times when I felt like to give up and it was also her to provide the endless love that make me not feeling lonely in this world unfamiliar to me. I am deeply thankful to my parents Shikui Shao and Jing Zhang. I want to thank them for growing me up, giving me the best environment for study and providing me this precious opportunity to study abroad.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supervised by a dissertation committee consisting of Professors Jose Silva-Martinez [advisor] Aydin Ilker Karsilayan [co-advisor] and Jiang Hu of the Department of Electrical and Computer Engineering and Professor Jay R. Porter of the Department of Engineering Technology and Industrial Distribution.

All work for the dissertation was completed by the student, under the advisement of Professor Jose Silva-Martinez.

Funding Sources

Graduate study was supported by teaching assistantship from Texas A&M University.

This work was also made possible with the support from Taiwan Semiconductor Manufacturing Company Limited (TSMC) on chip fabrication.

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1. INTRODUCTION

1.1. Background

Starting from the birth of wireless telegraph in 1890, wireless communication based on electromagnetic wave has gradually become an essential part of daily life, because of its high flexibility and mobility. Nowadays, these wireless communication can be found around us ubiquitously, from Wi-Fi, cellular phone, satellite television, smart home to radio broadcasting, radar, GPS and even RFID toll device. Among various services, cellular service in particular has witnessed the development of wireless communication ever since 1970s, as a result, the generations of wireless communication are also usually defined by the generations of cellular network. As a brief history, the cellular wireless communication has never stopped its evolution, ever since the 1G cellular system based on analog modulation was launched in 1979, to 2G cellular system based on narrowband digital communication in early 1990s, to 3G cellular system based on wideband digital communication in early 2000s, to 4G cellular system in 2010s, and towards 5G cellular systems in 2020s. On the other hand, the achieved data rate, as a criterion of the performance of cellular systems, has developed from 0.1Mbit/s (2G) to over 1Gbit/s (5G). The corresponding supported service, as shown in Figure 1.1 has also evolved from only analog voice call to streaming of Ultra HD video, smart home, high speed internet browsing and so on. Not surprisingly, new communication services based on wireless local area network (WLAN), radar at mmWave, and Bluetooth besides 5G cellular services will continue to emerge one after another, enabling applications such as

IoT, self-driving automotive, and remote biomedical services when the wireless communication technique steps into the era of 5G.

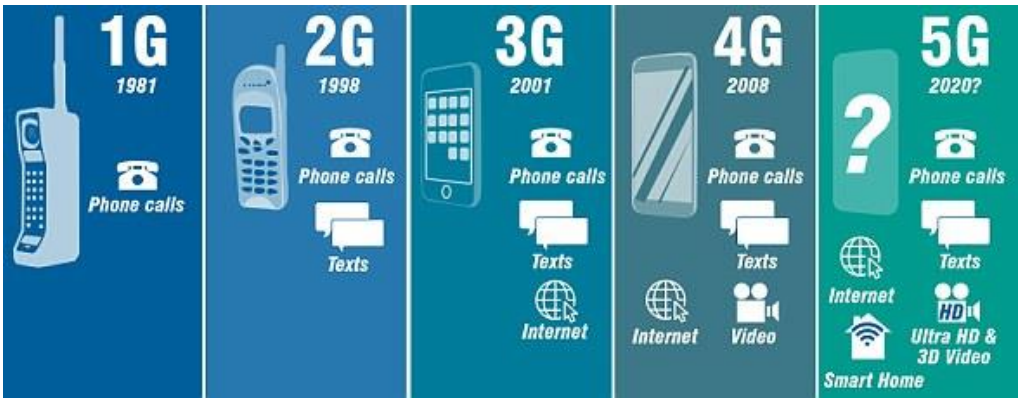


Figure 1.1. Reprinted from [1] Generations of cellular network.

From another aspect, the market size of these RF components shown below can be used as an indicator for the development of wireless communication services, because these RF components, including antennas, power amplifiers and filters, are the necessary parts of wireless services.

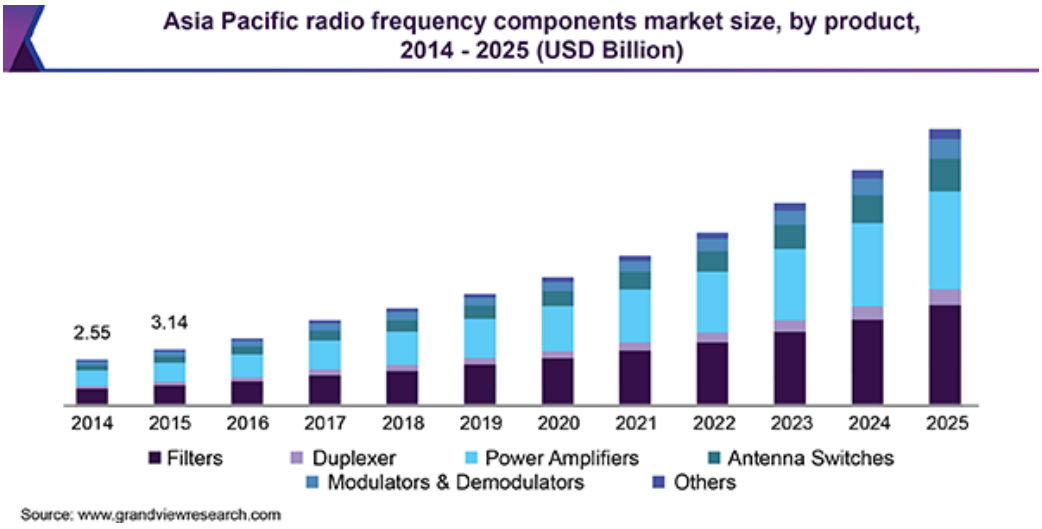


Figure 1.2. Reprinted from [2] Asia Pacific radio frequency components market size.

Easily seen from Figure 1.2, the size of this market is almost increasing exponentially, which shows the potentially growing emergence of wireless communication services and increasing congestions in the frequency bands.

1.2. Motivation

The co-existence of increasing numbers of emerging communication services with existing communication services within the limited frequency spectrum, as a result, inevitably starts to become a problem. The issue of spectrum congestion can also be seen from the price of spectrum. Globally, spectrum prices reached all-time highs with the 3G auctions at the start of the millennium, before falling gradually until 2007. From 2008-2016, when 4G auctions became common, the average final price paid for spectrum sold at auction increased significantly – by 3.5 fold [3].

Due to this high demand, even the guard frequency bands dedicated for protecting military applications are starting to be released for new wireless services. As emerging services get closer and closer to military applications in frequency, the leakage from these services starts to contaminate signals of military applications and degrade their performance and reliability. What's even worse, these affected military systems could be for applications such as navigation radars and ground surveillance, which are of vital importance to national security. Therefore, the degradation due to spectral collision that may result in missed hostile targets and false alarm of non-existing targets must be alleviated.

Besides increasing number of services, emerging services are usually more demanding than existing ones in many different aspects, for example data rates, latency, reliability and so on. These performance metrics inevitably translate to the thirst for wide reliable frequency bands. But the availability of such bands is already limited, which can be easily seen from the frequency allocation table [4]. However, the actual spectrum usage measurements obtained by the FCC's Spectrum Policy Task Force [5] indicate that, at any given time and location, a large portion of the prized spectrum lies idle. It means that the prevalent static spectrum allocation (SSA), instead of physical limitation, is the main reason for unavailability of reliable frequency bands. On the contrary, dynamic spectrum access (DSA) which is able to make more flexible use of frequency spectral resources, becomes a promising solution to improve spectral efficiency. Cognitive radio (CR) as one of the technique that enables dynamic spectrum access, thereby, has attracted enormous research interest from both academia and industry.

CR based communication as a two-phase process, is composed of spectrum sensing and spectrum sharing, and is usually explained with an analogy of "listen before talk". Spectrum sharing in CR network among different users, or cognitive transmission is of vital importance, because it is the technique that fundamentally improves the spectral efficiency. This dissertation aims at introducing a new mixed signal IC technique for spectrum sharing that enables the users to co-exist with large in-band interferences from other users in the same or adjacent channel within a hybrid mode spectrum sharing paradigm.

1.3. Organization of the Dissertation

This dissertation aims at proposing a mixed signal IC technique spectrum sharing among different wireless services at present or in the future. As a result, knowledge on different wireless communication standard is necessary. Apart from that, the proposed mixed signal IC technique requires: knowledge of high speed analog and digital circuit design, which is necessary to design circuits with sufficient performance but at minimum cost of power and silicon area, knowledge of digital coding to select the proper codes based on their advantages and limitations.

Section 2 introduces different paradigms of spectrum sharing, gives examples of each type of paradigms, and compares them to understand their advantages and disadvantages.

Section 3 introduces the code domain multiple access (CDMA) system and the different types of codes that may be used in CDMA system. And this part also introduces the spread spectrum technique embedded in CDMA system and compares the two types of spread spectrum technique.

Section 4 explains in detail the benefit of spread spectrum technique on in-band interference attenuation.

Section 5 explains the problem of conventional direct sequence spread spectrum (DSSS) system with binary pseudo random sequences (BPRS), and proposes a solution based on sinusoid-like pseudo random sequence (SPRS).

Section 6 introduces the synchronization in CDMA systems, and compares different types of synchronization technique, and proposes a three-level synchronization scheme.

Based on the preceded discussion, section 7 introduces the proposed mixed signal IC technique for spectrum sharing. In this section, the new type of digital code SPRS is implemented to alleviate the adjacent channel leakage issue of conventional BPRS; a delay lock loop for multi-phase clock generation is explained for generation of SPRS; the analog modulator/demodulator based on programmable gain amplifier is explained in details; a high speed OTA with gain enhancement and feed forward compensation is presented. The simulation results and experimental results of this IC prototype fabricated with 40nm technology are shown to prove the feasibility and benefits.

Section 8 explains the need for the synchronization scheme in DSSS systems, and introduces the proposed three-level synchronization scheme; describes the system architecture and circuit implementations of the main analog and digital building blocks. The I present relevant post-layout simulation results to prove the feasibility and benefits of the proposed technique and demonstrate the interference tolerance of the proposed synchronization scheme through experimental results.

The conclusions of this dissertation are provided in Section 9.

2. PARADIGMS OF SPECTRUM SHARING

According to the network information that is available to the users, spectrum sharing techniques are divided into three paradigms: underlay, overlay and interweave [6]. In underlay paradigm, cognitive users are required to keep the transmitted power level below the tolerable level of incumbent users, in which case cognitive users achieve data transmission without affecting the incumbent users. In overlay paradigm, the cognitive radios use sophisticated signal processing and coding to maintain or compensate the communication of noncognitive radios for the degradation on these noncognitive radios due to obtaining bandwidth for their own communication. In interweave systems, the cognitive radios opportunistically exploit spectral holes to communicate without disrupting other transmissions. In the following sections, these three paradigms are explained in more detail and examples of these three paradigms are also given.

2.1. Underlay spectrum sharing

The spectrum sharing technique based on underlay paradigm is usually between the primary users with licensed and unlicensed users. In this paradigm, unlicensed users are required to guarantee the performance of licensed users not being affected due to their behavior of spectrum sharing. Therefore, the unlicensed users are also called secondary users, with respect to the primary users. This requirement is satisfied by restricting the interference power from the secondary users on the receiver of the primary users to below an tolerable threshold, which have been reported achievable by research facilities around

the world. The techniques reported in these works can be divided into two categories: beamforming and spread spectrum technique.

Beamforming technique is a technique that enables directional transmission based on multi-antenna. Making use of the coherence of transmitted signals from different antennas, the total signal at different directions are significantly different. The comparison of the radiation pattern of an omni-directional antenna and a two-antenna is given in the following figure.

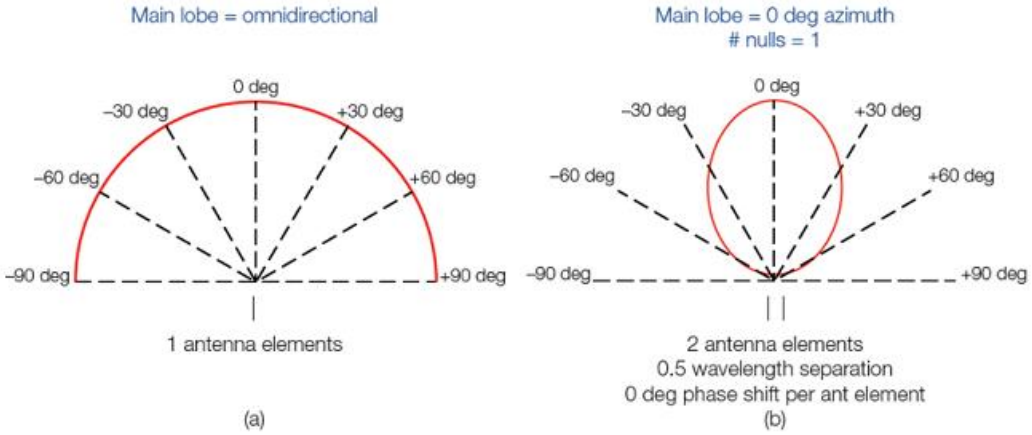


Figure 2.1. Adapted from [7] Comparison of radiation pattern of an omni-directional antenna and a two-antenna system.

With beamforming technique [8-12], the secondary users are able to limit the interference power they generate in the direction of primary users, while maintaining the signal power in the direction of their desired targets.

Spread spectrum technique [13-17] is another technique to reduce the interference power received by the primary users. By doing frequency spreading before transmission in the secondary users' transmitters, the signal is spread into a larger bandwidth with a high speed digital signal to reduce the power spectral density. In this case, when this spread

signal is received by the primary users' receiver, with the restricted bandwidth, the total interference power is reduced. However, in the secondary users' receivers, the spread signal is despread with the same digital signal before further data processing. An example of a block diagram of spread spectrum system is shown in the following figure.

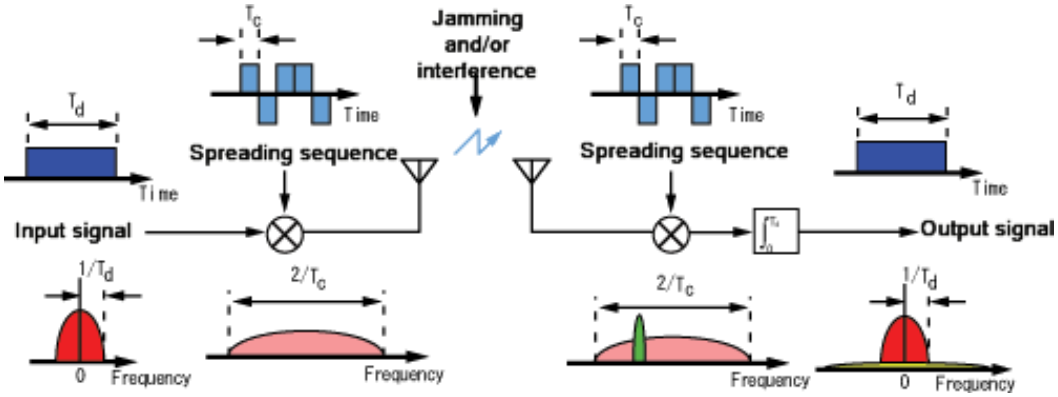


Figure 2.2. Reprinted from [18] Block diagram of transceiver based on spread spectrum technique.

However, the cognitive transmitter tends to be over pessimistic in its output power limitation to ensure that its signal remains below the tolerable interference threshold, which sometimes may be relaxed by the actual channel condition. In this case, since the interference constraints in underlay systems are typically quite restrictive, cognitive users are limited to short range communications or in-door applications.

2.2. Overlay spectrum sharing

The spectrum sharing based on overlay paradigm [19-24] is more demanding than underlay paradigm in terms of the sharing of information between licensed users and unlicensed users, which may include signal codebooks and channel states. Based on these

knowledge of licensed users, unlicensed users are responsible for enhancing or assisting the communication of licensed users, while accessing certain portion of spectrum for their own communication.

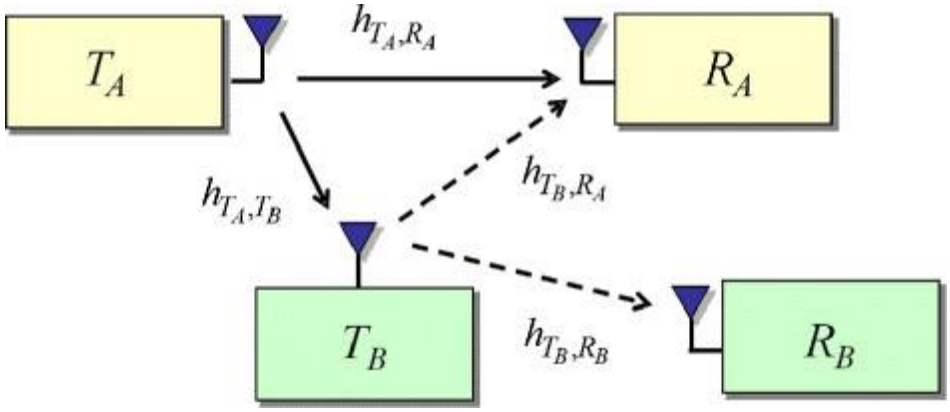


Figure 2.3. Reprinted from [24] Overlay paradigm based spectrum sharing.

As an example of overlay spectrum sharing shown in Figure 2.3, a spectrum sharing network is composed of one licensed transmitter (T_A), one licensed receiver (R_A), one unlicensed transmitter (T_B), and one unlicensed receiver (R_B). With the knowledge of the signal from T_A, T_B is able to eliminate the interference generated by the primary communication at R_B and improve the performance of the primary transmission through relaying the accumulated messages through the transmission from T_B to R_A.

However, the shared information from licensed users inevitably cause a security issue on the primary transmission, which will be not acceptable in the network involving military applications. What's more, the shared information from licensed users may require additional overhead in the data transmitted by unlicensed users, which will reduce the throughput and degrade the spectral efficiency.

2.3. Interweave spectrum sharing

As the original motivation of spectrum sharing, interweave spectrum sharing or opportunistic spectrum access (OSA) [25-27], requires the information of spectrum occupancy, based on which the unlicensed users are able to access the so-called spectrum holes (the idle or under-utilized frequency band in time and frequency domain), and vacate when the licensed users come back or increase their usage of the band. The working principle of interweave spectrum sharing network is shown in the following figure [28].

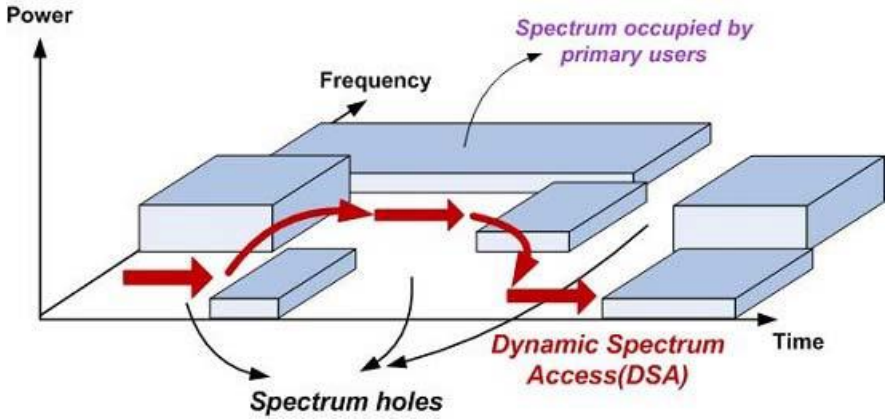


Figure 2.4. Reprinted from [28] Interweave paradigm based spectrum sharing.

With the information of spectrum occupancy acquired by periodic spectrum sensing, the unlicensed users are able to find the spectrum holes and make use of these frequency bands by doing frequency hopping from time to time.

However, the imperfection of spectrum sensing may cause improper use of spectrum and thereby degrade the quality of primary transmission of licensed users. Moreover, the fast frequency hopping capability requires power consuming frequency synthesizers that is not applicable for low power applications, for example smart homes.

2.4. Hybrid spectrum sharing

To overcome the shorting comings of the aforementioned three paradigms and maximize the spectral efficiency, different types of hybrid paradigms [29-34] have been proposed. The mixed signal IC technique proposed in this project borrows the idea of code division multiple access to make feasible a hybrid spectrum sharing paradigm involving underlay and interweave paradigm, with CMOS implementation. As shown in the following figure, based on the frequency occupancy information from spectrum sensing, the proposed system is able to switch between the interweave paradigm and underlay paradigm.

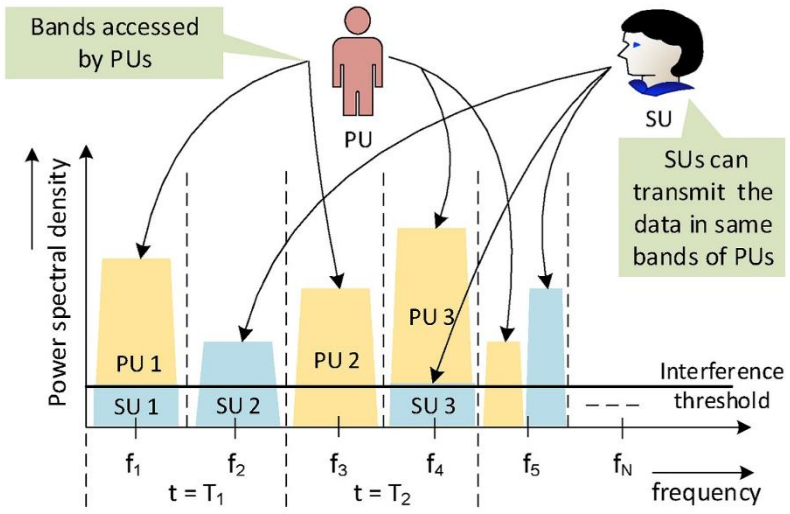


Figure 2.5. Adapted with permission from [35] Hybrid paradigm based spectrum sharing.

More importantly, the proposed technique makes it possible for unlicensed users to co-exist with the interference from licensed users, thereby relax the requirement of frequency synthesizer in interweave paradigm for fast frequency hopping, and improve

the spectral efficiency of underlay paradigm by relaxing the interference restriction forced by licensed users.

3. CODE DOMAIN MULTIPLE ACCESS

3.1. Spectral co-existence in code domain

In order for two signals to be distinguishable, the two signals need to be orthogonal at least in one domain. For example, signals are orthogonal in time domain within time division multiplexing systems; are orthogonal in frequency domain in frequency division multiplexing systems; or orthogonal in space domain in spatial division multiplexing systems. However, due to the nature of probable overlapping between licensed users and unlicensed users in time, frequency, and space, signals from these two types of users in cognitive radio network need to be separated in the receiver by exploiting other properties of signals. Coding is one of the promising solution of this problem. A comparison of time division multiple access (TDMA), frequency division multiple access (FDMA) and code division multiple access (CDMA) based system is given in the following figure [36].

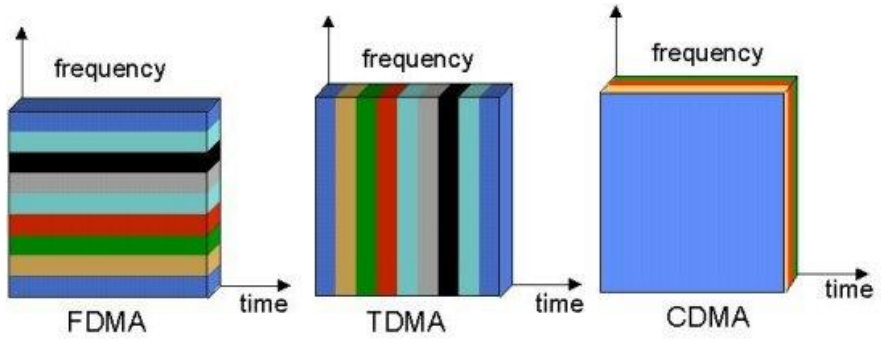


Figure 3.1. Reprinted from [36] Comparison of FDMA, TDMA and CDMA.

As is shown in Figure 3.1, although signals in CDMA system are sharing the same frequency band and the same time slot, signals are still distinguishable in coding information. The differentiation is done by converting the 2D signal into 3D signal with

the third dimension of coding. This idea of code division makes it possible for spectrum sharing between licensed users and unlicensed users in cognitive radio network.

3.2. Spread spectrum technique

In code division multiple access system, a group of users are assigned a common frequency band that is larger than the Nyquist bandwidth required and each user is able to separate in the receiver the desired signal from others with a unique code assigned to himself. This is achieved by spreading the signal bandwidth to a larger bandwidth with the help of digital codes in the transmitter, and despreading only the desired signal bandwidth to its original state with the same digital code, therefore code division multiple access is also called spread spectrum (SS) multiple access. Based on the realization method of frequency spreading, SS technique is divided into frequency hopping spread spectrum (FHSS) and direct sequence spread spectrum (DSSS).

3.2.1. Frequency hopping spread spectrum

Seen from its name, in this type of system frequency spreading is achieved with an operation called frequency hopping, which is changing the carrier frequency of the transmitted signal among many distinct frequencies occupying a large frequency band. The fast changes in carrier frequency are usually achieved by controlling the frequency synthesizer with a digital code called pseudo random sequence (PRS) shared between transmitter and receiver, without which the spread signal cannot be recovered. A block diagram of FHSS based wireless system is shown in the following figure.

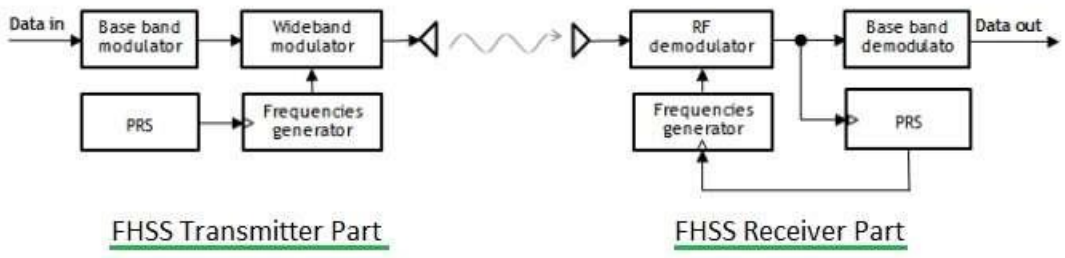


Figure 3.2. Reprinted from [37] Block diagram of FHSS based wireless system.

As shown in Figure 3.2, FHSS system requires a frequencies generator, which is usually achieved with frequency synthesizer. To realize fast frequency hopping, the frequency synthesizer must be able to settle within the limited time slot, which is not easy to achieve with low power. As a result, to get rid of this demanding frequency synthesizer, another type of SS system is introduced.

3.2.2. Direct sequence spread spectrum

In a DSSS technique based wireless system, instead of frequency hopping, frequency spreading is achieved by direct modulation of signal with a wideband digital PRS. Based on the accurate synchronization of PRS, signal can be recovered with acceptable loss. The block diagram of DSSS based wireless system is shown in the following figure.

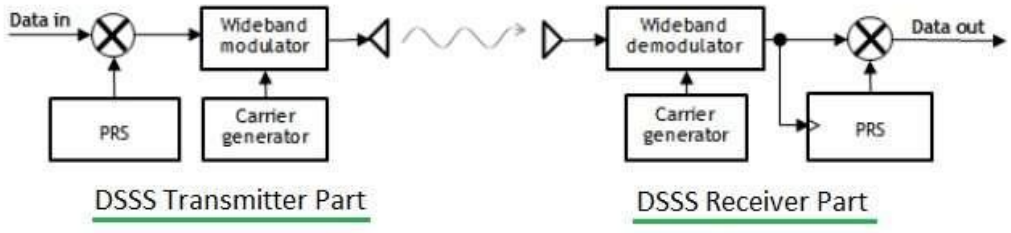


Figure 3.3. Reprinted from [37] Block diagram of DSSS based wireless system.

A comparison in the frequency spectra of the spread signal in FHSS system and DHSS system is shown in the following figure.

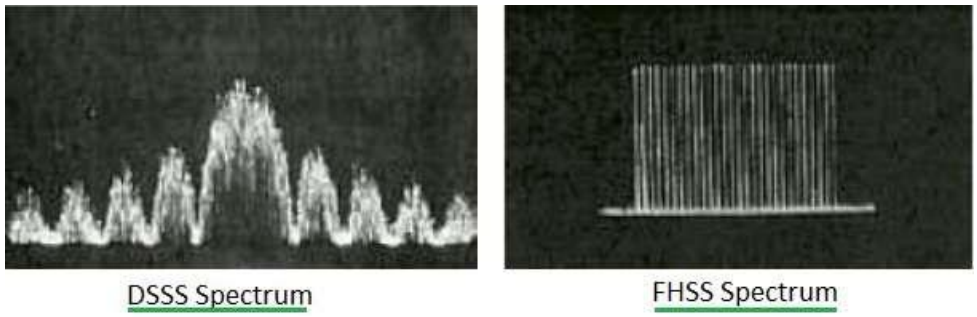


Figure 3.4. Reprinted from [37] Comparison of spread signal spectra in DSSS and FHSS system.

Although different in spreading method, both FHSS system and DSSS system require a digital code whether it is for controlling frequency synthesizer in FHSS system or it is for direct convolution in DSSS system. More importantly, this digital code should have the following properties:

1. Reconstructable
2. Random
3. Narrow autocorrelation

3.3. Pseudo Random Sequence

Pseudo Random Sequence (PRS) is a binary sequence with a low periodicity that, although generated with a deterministic algorithm, is difficult to predict and exhibits statistical behavior similar to a truly random sequence. However, it is fully reconstructable with the structure information of PRS generator.

3.3.1. Generation of PRS

In practice, the PRS is generated with a building block called Shift Register with Linear Feedback (LFSR). For a given LFSR, the generated PRS has a known periodicity, and fixed permutation of bits. An example of such 9th order PRS generator is shown in Figure 3.5.

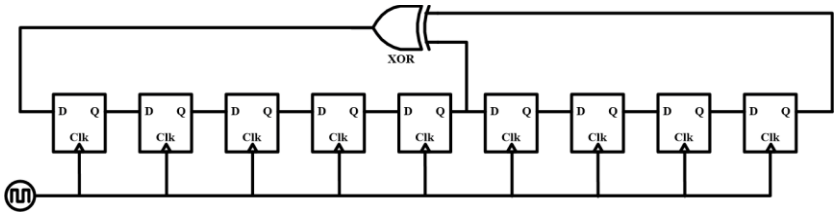


Figure 3.5. Example of 9th order Shift Register with Linear Feedback.

3.3.2. M Sequence

For an LFSR based PRBS generator with a given order of N, theoretically, the PRS generator may have 2^N-1 different states, only excluding the all “0” state. However, for a given order, only a few structures of the LFSRs can generate PRS that has all these 2^N-1 possible states. Sequences of this kind are called maximum length sequence or m sequence.

For a given order of N, and a given bit duration of T, the m sequence has several nice properties,

1. The period of the m sequence is the longest, which is $(2^N\text{-}1)T$;
2. Bipolar m sequence has a negligible dc content, because it has 2^{N-1} "1"s, and 2^{N-1}-1 "-1"s;
3. The autocorrelation $R_{\alpha\alpha}[t_0/T]$ of a bipolar m sequence $\alpha[n]$ is a periodic function, which can be seen in Figure 3.6,

$$R_{\alpha\alpha}[t_0/T] = \sum_{n=1}^{2^N-1} \alpha[n]\alpha[n + t_0/T] = \begin{cases} 2^N - 1 & t_0/T = M * (2^N - 1) \\ -1 & t_0/T \neq M * (2^N - 1) \end{cases} \quad (1)$$

Here, $\alpha[n]$ is an m sequence, M is an arbitrary integer, t_0 is the timing offset between two m sequences.

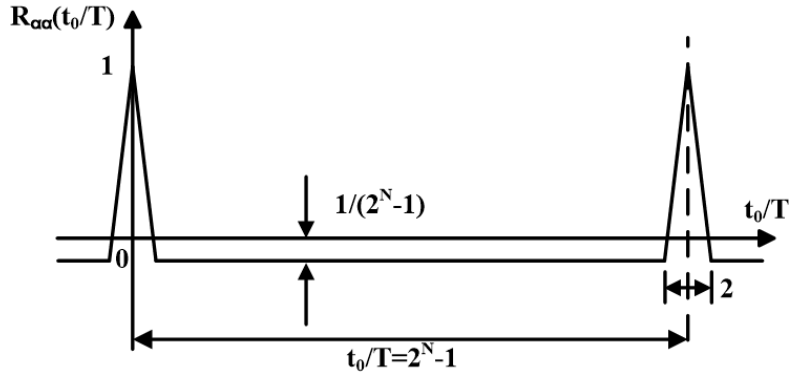


Figure 3.6. Autocorrelation of an Nth order m sequence.

4. The maximum number of consecutive "1" is N, while the maximum number of consecutive "0" is N-1;
5. The frequency spectrum of the m sequence is flat like white noise in the main lobe of the PRS. Figure 3.7 shows a 9th order bipolar m sequence with a bit duration of 10ns and power of 0 dBm.

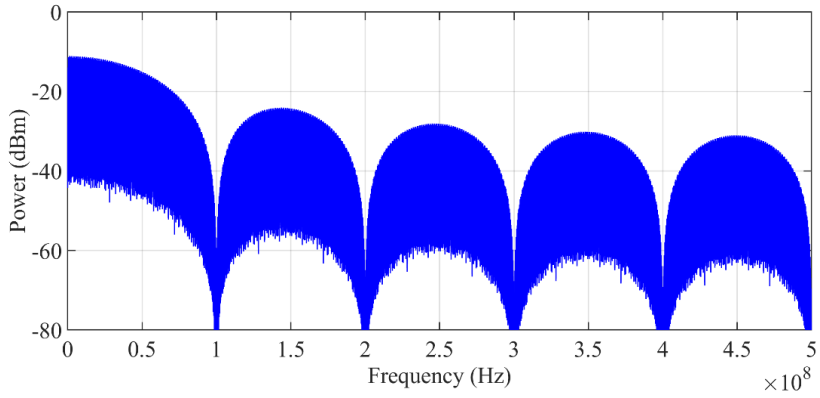


Figure 3.7. Frequency spectrum of a 9th order m sequence.

However, as mentioned before, the number of m sequences generated with a given order PRS generator based on LFSR is limited, which limits the number of co-existing users and is not suitable for multiplexing. More importantly, even if the number of m sequences meet the number of users requirement, the cross correlation of m sequence is not well defined, therefore the mutual interference level is not well defined. To solve these issues, Robert Gold proposed a new type code, namely Gold sequence.

3.3.3. Gold sequence

These gold sequences are constructed by EXOR-ing two m-sequences of the same length with each other. Thus, for a Gold sequence of length 2N-1, one uses two LFSR, each of length 2N-1. If the two LFSRs are chosen appropriately, these Gold sequences generated from the Gold sequence generators with same LFSRs structure have better cross-correlation properties than m sequences. An example of Gold sequence generator based on LFSR structure is shown below,

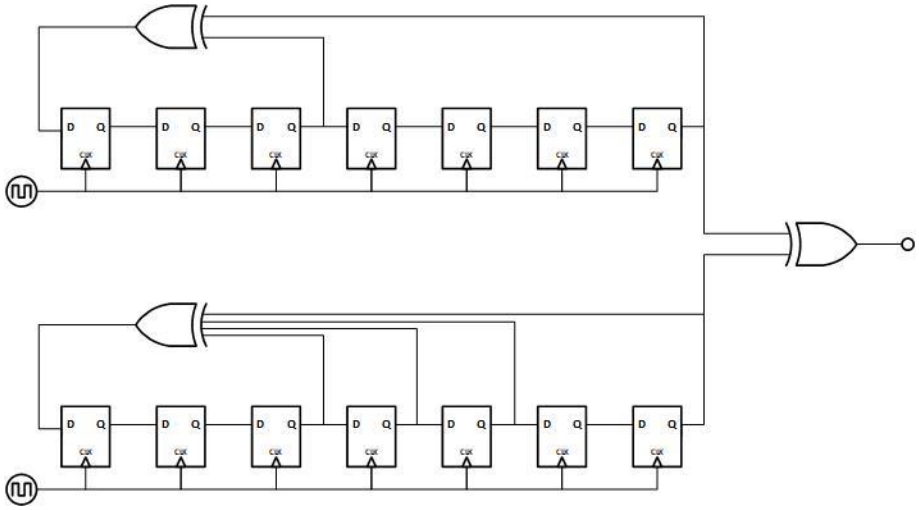


Figure 3.8. Gold sequence generator based LFSR.

For the number of Gold sequences a structure shown above is able to generate, compared with the number of m sequences LFSR is able to generate, Gold sequence generator has one more freedom to work with, which is the initial condition of LFSR on the bottom with respect to LFSR on the top, thereby increases the number of Gold sequences to 2^N-1.

For the cross correlation between two sequences with the same length, the Gold sequences have a three-valued cross correlation, better than the m sequences. However, the autocorrelation of Gold sequences is not as ideal as that of m sequences.

3.3.4. Walsh-Hadamard Code

Mutually orthogonal codes are perfect for multiple users' coexistence, because when assigned to all the users in the same network signals of each user are distinguishable. A series of codes generated with Hadamard Metrices, namely Walsh-Hadamard Code, are

one of the orthogonal codes, and are used in IS-95 or CDMA One standard for this property. The Walsh8 codes, are shown below as a brief example.

Table 3.1. List of Walsh8 code

$Walsh_8^0$	00000000
$Walsh_8^1$	01010101
$Walsh_8^2$	00110011
$Walsh_8^3$	01100110
$Walsh_8^4$	00001111
$Walsh_8^5$	01011010
$Walsh_8^6$	00111100
$Walsh_8^7$	01101001

However, the problem with Walsh code is that the period of the sequence is short or in another word the randomness is not as good as m sequence. This indicates that this code is not suitable for randomization in radar applications and synchronization in harsh environment.

3.3.5. Comparison of codes

Different codes have different properties and are suitable for different applications. Gold sequences and Walsh codes have better cross-correlation properties, are more suitable for multiplexing than m sequences. Gold sequences and m sequences have lower

periodicity and are better for randomization purpose. M Sequence has the best autocorrelation function and is best for synchronization process.

3.4. Randomization

Another benefit of spread spectrum technique is that the demodulation process may also randomize components other than the desired signal, if the digital code form modulation and demodulation has a low periodicity and good randomness.

The randomization is especially useful when the recovered signal is highly predictive and is compatible with averaging technique, for example in radar applications and in synchronization process. In this type of system, it is very common that the recovered signal is averaged in time to gain further attenuation on random noises. In the case of systematic interferences, however, those interferences are not attenuatable like random noise and will limit the processing gain of averaging technique as explained below.

Consider that part of the interference signal is not fully random and that the interference power P_I is composed of two parts: a systematic part P_{I_S} and a random component P_{I_R}. Therefore, the processing gain PG with an average of X samples is computed as,

$$PG = \frac{\frac{P_{sig} \cdot X^2}{P_{I\_S} \cdot X^2 + P_{I\_R} \cdot X}}{\frac{P_{sig}}{P_{I\_S} + P_{I\_R}}} = \frac{P_{I\_S} + P_{I\_R}}{P_{I\_S} + \frac{P_{I\_R}}{X}} \quad (2)$$

Notice in this equation that the systematic interference component P_{I_S} does not reduce with the averaging factor X, thus limiting the value of the PG.

With the randomization, all interference components become random Therefore, the processing gain PG becomes equal to the averaging factor X. Thus, the processing gain increases proportionally with the averaging factor regardless if the original interference is systematic or random.

$$PG = \frac{\frac{P_{sig} \cdot X^2}{P_{I\_S} \cdot X + P_{I\_R} \cdot X}}{\frac{P_{sig}}{P_{I\_S} + P_{I\_R}}} = X \tag{3}$$

As a result, m sequence is the most promising candidate among the three types of digital codes for radar application and synchronization process.

4. INTERFERENCE REJECTION OF DSSS TECHNIQUE

4.1. Introduction

As mentioned in the previous sections, DSSS technique is able to help attenuate in-band interferences. This benefit of attenuation will be more elaborated with mathematical derivation in this section.

4.2. Block diagram of DSSS transceiver

To begin with, a simplified block diagram of DSSS transceiver is shown below. In a DSSS system, code domain modulator and demodulator can be implemented at RF frequency, baseband or digital domain. In this example, the code domain modulation and demodulation is achieved at baseband in analog domain.

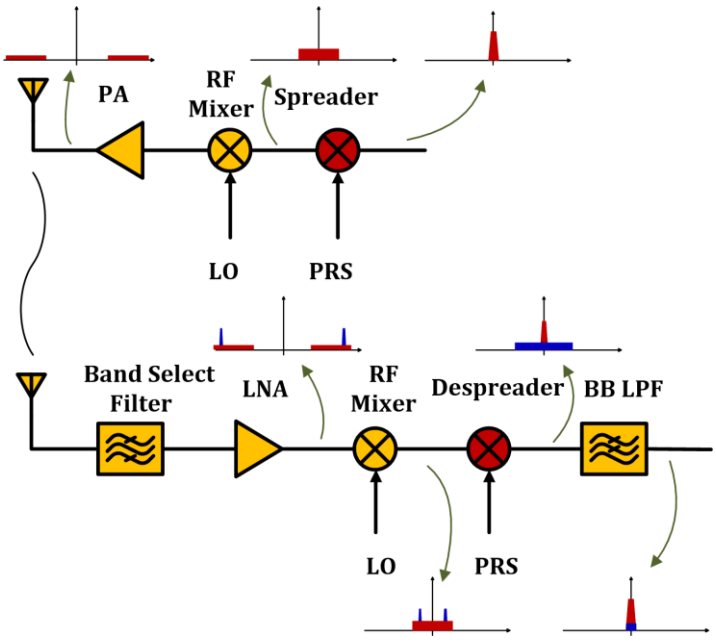


Figure 4.1. Block diagram of a DSSS transceiver.

4.3. Interference rejection

For the sake of simplicity, let me consider the case of an ideal RF front end, which means linear gain, no bandwidth limitation, and perfect timing between the PRS modulated echo signal and the reference PRS. According to Figure 4.1, the signal S(t) with a power of P_{sig} and a bandwidth of BW is mixed with a binary PRS(t) which has a bandwidth of the first lobe equal to BW_{PRS} and amplitude of ±1. As shown in Figure 4.1, the frequency spectrum of the desired signal is spread into a larger bandwidth of BW_{PRS}. If the gain in TX and RX are A_{TX} and A_{RX} respectively, and the loss in the signal channel is A_L. After up-converted, amplified and transmitted, corresponding desired signal of RX (ignoring the up-conversion function) is,

$$D(t) = A_{TX}A_L S(t - t_0) \times PRS(t - t_0) \tag{4}$$

This signal is received by RX antenna together with the in-band interference signal $I_{rf}(t)$. After amplification and down-conversion, let me assume that A_{RX} I(t) has a power density of S_I and is flat in its bandwidth of BW_{PRS}. The total received baseband signal is then,

$$S_{total}(t) = A_{TX}A_L S(t - t_0) \times PRS(t - t_0) + I(t) \tag{5}$$

After mixing with the reference PRS(t), ignoring the PRS timing mismatch, the recovered signal R(t) is given by,

$$R(t) = A_{TX}A_{RX}A_L S(t - t_0) \times PRS(t - t_0) \times PRS(t - t_0) + A_{RX}I(t) \times PRS(t - t_0) \tag{6}$$

Ideally, if the PRS(t) in the RX is synchronized to the PRS(t) embedded in the received signal, according to the property of PRS,

$$PRS(t - t_0) \times PRS(t - t_0) = 1 \tag{7}$$

Therefore, as shown in Figure 4.1 the received signal is perfectly recovered while the inference is spread into a larger bandwidth of BW_{PRS}. As a result R(t) reduces to,

$$R(t) = A_{TX}A_{RX}A_L S(t - t_0) + A_{RX}I(t) \times PRS(t - t_0) \tag{8}$$

Employing the Parseval's theorem and assuming that $I(t)$ and $PRS(t - t_0)$ are uncorrelated, the double sideband RX signal components are,

$$R(f) = A_{TX}A_{RX}A_L S(f) + A_{RX}I(f) * PRS(f) \tag{9}$$

After the de-spread signal $R(t)$ is filtered out with an ideal low pass filter, total received power becomes,

$$R(f)_{filtered} = A_{TX}A_{RX}A_L S(f) + A_{RX}H_{filter}\big(I(f) * PRS(f)\big) \tag{10}$$

Note that the desired signal $S(f)$ is perfectly recovered. The interference signal, however, convolves with the reference $PRS(f)$ and its power is widely spread and then most of it is effectively removed to a large extent by the baseband filter with a bandwidth equal to BW Hz. The estimated interference power reduction after mixing and filtering can be obtained as,

$$Interference_{reduction} = \frac{\int_{-BW}^{BW} |I(f)|^2 df}{\int_{-BW}^{BW} |I(f) * PRS(f)|^2 df} \cong \frac{BW_{PRS}}{BW} \tag{11}$$

Therefore, for example if we want to achieve an power attenuation of 10dB, we need to use a PRS(t) with a bandwidth of 10 times the signal bandwidth.

5. SIDEBAND LEAKAGE ISSUE

5.1. Introduction

As discussed in the previous section, the benefit of DSSS system on in-band interference rejection comes from the operation of modulation with PRS in TX and demodulation with PRS in RX. The modulation with PRS in TX results in the occupancy of a wider frequency band than that is required by the signal, while improves the capability of spectrum sharing. This frequency band occupancy could be even worse, when the PRS used for modulation is rich in harmonics. In this case, the transmitted wideband signal could have significant leakage to adjacent channels. This inevitably makes the DSSS system hard to satisfy the spectral mask for communication standards and not feasible to co-exist with other services.

5.2. Spectral mask

In wireless communications, a spectral mask, also known as a channel mask or transmission mask, is a mathematically-defined set of lines applied to the levels of radio transmissions. An example of the spectral mask for 802.11b is shown below [38].

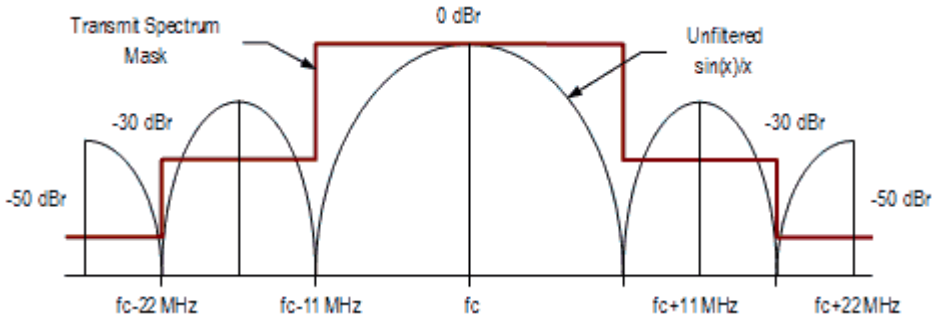


Figure 5.1. Reprinted from [38] Spectral mask for 802.11b standard.

The spectral mask is generally intended to reduce adjacent-channel interference by limiting excessive radiation at frequencies beyond the necessary bandwidth.

5.3. Frequency spectrum of Binary PRS

Binary PRS as a digital signal has only two levels of 1 and -1, and also has ideal transitions. Therefore, it is not a surprise to find that binary PRS is rich in harmonics. As an example, the following figure shows the frequency spectrum of a 9^{th} order binary PRS that is generated with a 9^{th} order LFSR with a clock frequency of 100MHz. The binary PRS, as a result, has a minimum pulse width of 10ns.

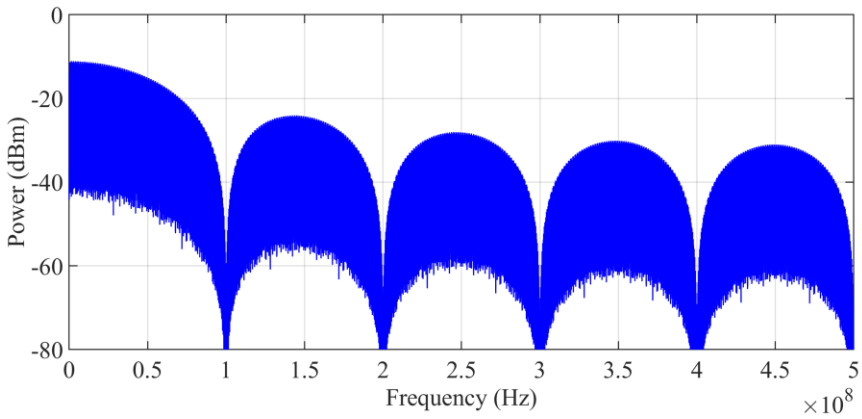


Figure 5.2. Frequency spectrum of a 100MHz binary PRS.

Seen from above, the fourth side lobe of this signal is only 20dB lower than the main signal channel. Evidently, signal after modulated with binary PRS is not able to satisfy the spectral mask of 802.11b standard. The frequency spectrum of the modulated signal, in this case, must be cleaned with sharp filters before transmission. However, the implementation of these filters could be area and power consuming.

5.4. Sinusoid-like interpolation

To attenuate the power in the sidelobes due to sharp transitions, apart from smoothening with analog filters, we can also interpolate more steps during each transition. Or equivalently, we can consider the operation of interpolation as digital filtering with FIR filters.

To satisfy the spectral mask of 802.11b standard with the minimum number of steps or minimum number of taps in the FIR filter, we borrow the idea of raised cosine filter and propose an interpolation method that follows the steps of a discrete cosine waveform.

Compared with pulse-like binary PRS signal, in this sinusoid like PRS (SPRS) the low-high and high-low transitions are implemented using a piecewise linear transition with six levels spaced according to a sinusoid variation. Figure 5.3 shows an example of a 100MHz SPRS and its binary counterpart, where the SPRS employs five steps to achieve one transition of the original BPRS.

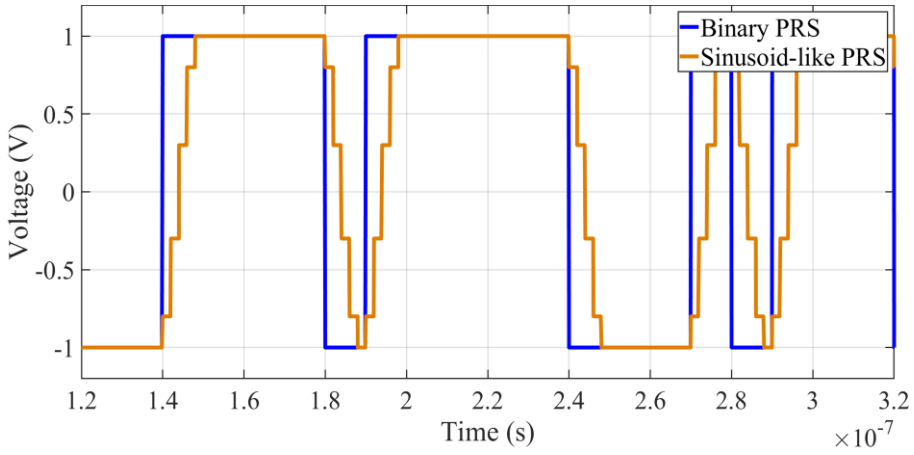


Figure 5.3. 100MHz Binary PRS and 100MHz Sinusoid-like PRS in time domain.

As mentioned above, the SPRS can also be considered as a BPRS filtered by a 5-tap FIR filter. For each digital delay cell in the FIR filter, the sample frequency T_S is 0.2T. The discrete time transfer function H(z) of this 5-tap FIR filter is,

$$H(z) = 0.1 + 0.25z^{-1} + 0.3z^{-2} + 0.25z^{-3} + 0.1z^{-4} \quad (12)$$

The magnitude response and phase response of this FIR filter is shown in Figure 5.4.

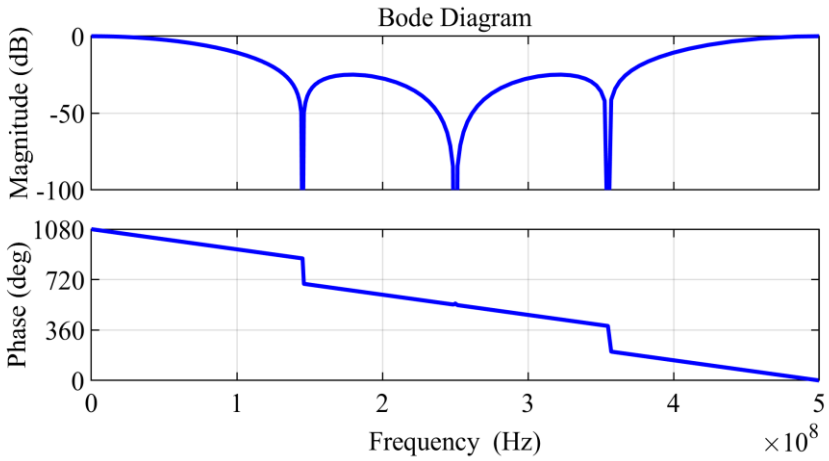


Figure 5.4. Frequency response of 5-tap FIR filter.

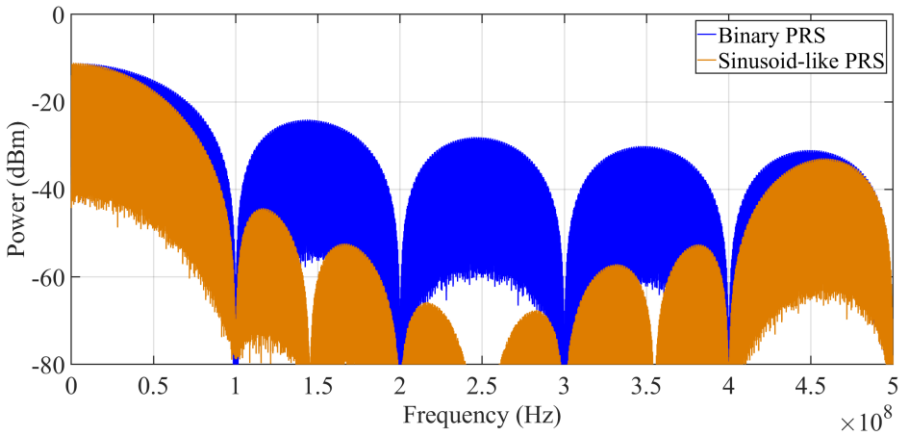


Figure 5.5. Power spectral density functions of Binary PRS and Sinusoid-like PRS.

This FIR filter adds notches at the middle of the original lobes to reduce further the power on the adjacent channels, as depicted in Figure 5.5. For the case of the proposed SPRS sequence, the ratio of power of main signal channel to adjacent channel including the two consecutive adjacent lobes is computed as,

$$\frac{P_{main}}{P_{2nd}+P_{3nd}} = \frac{\int_0^{BW_{PRS}} 2sinc^2(f/BW_{PRS})\times|H(jf)|df}{\int_{BW_{PRS}}^{3BW_{PRS}} 2sinc^2(f/BW_{PRS})\times|H(jf)|df} \quad (13)$$

This power reduction meets the requirement transmission spectral mask for several standards, including 802.11b, which can only be achieved in the conventional BPRS case by adding an 11th order 100MHz Butterworth. With the proposed technique, however, only cheap filtering will be needed to reduce the power of the high frequency lobes to co-exist with more demanding standards such as 802.11ax.

To proof the feasibility of this sinusoid-like PRS concept and the benefit of DSSS system on spectrum sharing, an IC prototype was designed and fabricated with 40nm CMOS technology.

6. SYNCHRONIZATION IN DSSS SYSTEM

6.1. Need for synchronization

In the previous section we assumed that the PRS signal in TX and that in RX are fully synchronized in time. However, if there is a timing mismatch of t_0 s between the two PRSs in TX and RX and we ignore the linear gain signal go through, the recovered signal becomes,

$$S'(t) = S(t) \times PRS(t) \times PRS(t - t_0) \tag{14}$$

If we take the Fourier transform of the recovered signal S'(t),

$$S'(f) = S(f) * \int_{-\infty}^{+\infty} PRS(t) \times PRS(t - t_0)\, e^{-j2\pi ft} dt \tag{15}$$

From (11), we can easily see that the dc component of $PRS(t) \times PRS(t - t_0)$ is the frequency content that is able to recover the signal. Interestingly, this dc component is also related to the autocorrelation of PRS(t), which is elaborated in Section 3.3.2. And as we know that this autocorrelation function has the same period as PRS(t), which is $(2^N-1)T$, where T is the period of the clock signal used in the PRS generator, we only need to consider the case when t_0 is smaller than $(2^N-1)T$.

For the Fourier transform of the $PRS(t) \times PRS(t - t_0)$,

$$\int_{-\infty}^{+\infty} PRS(t) \times PRS(t - t_0) e^{-j2\pi ft} dt = \alpha\delta(f) + W(f) \tag{16}$$

Where, $\alpha\delta(f)$ is the dc component responsible for recovering the signal, $W(f)$ is the wideband noise generated due to the timing error. Therefore, it is of great importance to find out the degradation of in-band SNR for the recovered signal due to timing error t_0.

6.1.1. Recovered signal power

In order to find out the in-band SNR, we need to find out the signal power first. Because PRS(t) is a periodic signal with a period of $(2^N\text{-}1)T$, the dc coefficient α of $PRS(t) \times PRS(t - t_0)$ can be calculated as,

$$\alpha = \frac{1}{(2^N-1)T}\int_0^{(2^N-1)T} PRS(t) \times PRS(t - t_0)dt \quad (17)$$

Notice that $PRS(t) \times PRS(t - t_0)$ in each clock period T can only have two posibilities: 1) when there is no transition in $PRS(t)$, the value of $PRS(t) \times PRS(t - t_0)$ is 1; 2) when there is a transition in $PRS(t)$, $PRS(t) \times PRS(t - t_0)$ generates a rectangular glitch related to the t_0 as shown in Figure 6.1.

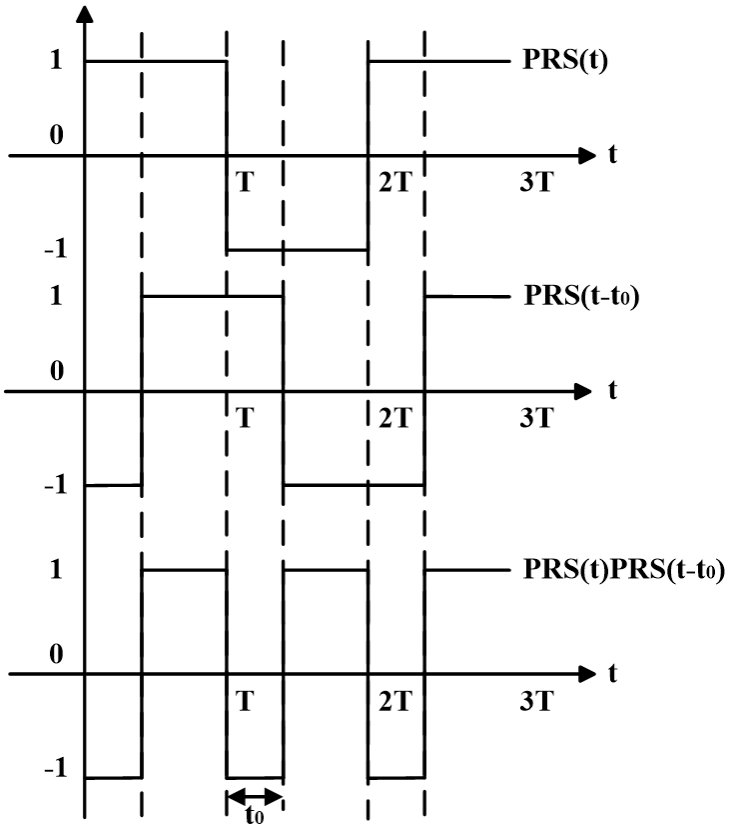


Figure 6.1. Time domain waveform of PRS(t) and PRS(t)×PRS(t-t0).

Therefore,

$$\alpha = \frac{1}{(2^N-1)T}\left(\sum_1^M \int_0^T PRS(t) \times PRS(t-t_0))dt + \sum_{M+1}^{2^N-1} \int_0^T PRS(t) \times PRS(t-t_0)dt\right) \tag{18}$$

Where, M is the number of transitions in one period of $PRS(t)$. According to Figure 6.1, the dc component of $PRS(t) \times PRS(t-t_0)$ in one clock period, with transition, is equal to $1\text{-}2t_0/T$. Evidently, the dc component of $PRS(t) \times PRS(t-t_0)$ in one clock period without transition is 1.

For an N^{th} order PRS, in each period the number of "ones" is 2^{N-1}, and the number of "zeros" is 2^{N-1}-1. Therefore, the probability P_{01} of a "zero" followed by a "one" and the probability P_{00} of a "zero" followed by a "zero" are,

$$P_{01} = \frac{2^{N-1}}{2^N-2}, P_{00} = \frac{2^{N-1}-2}{2^N-2} \tag{19}$$

Similarly, the probability P_{10} of a "one" followed by a "zero" and the probability P_{11} of a "one" followed by a "zero" are,

$$P_{11} = \frac{2^{N-1}-1}{2^N-2}, P_{10} = \frac{2^{N-1}-1}{2^N-2} \tag{20}$$

Thus, the probability of a transition PT and number of transitions M considering the two possible current states can be calculated as,

$$P_T = \frac{2^{N-1}-1}{2^N-1}P_{01} + \frac{2^{N-1}}{2^N-1}P_{10} = \frac{2^{N-1}}{2^N-1} \tag{21}$$

$$M = (2^N-1) \times P_T = 2^{N-1} \tag{22}$$

Thus for $N \geq 7$, the coefficient α can be approximated with an error of less than 1% by the following simplified equation,

$$\alpha = \left(1 - \frac{2t_0}{T}\right) \times \frac{M}{2^N - 1} + \left(1 - \frac{M}{2^N - 1}\right) \cong 1 - \frac{t_0}{T} \quad (23)$$

Therefore, it is easily seen that the recovered signal power decreases with the increasing of timing error.

6.1.2. Noise power generated

To calculate the noise power generated because of timing error, we need to find out the frequency spectrum of $PRS(t) \times PRS(t - t_0)$. In time domain, this signal resembles another PRS $PRS'(t)$ sampled with a square wave $P(t)$. The mathematical expression is as follows,

$$PRS(t) \times PRS(t - t_0) = PRS'(t) \times P(t) + 1 - P(t) \quad (24)$$

Where $PRS'(t)$ is a PRS with the same period of $(2^N\text{-}1)$T, and $P(t)$ is a square wave with a period of T and with a pulse width percentage of t_0/T. Hence, the noise power caused by the timing error has two parts; namely i) the higher order harmonics of P(t), and ii) the wide band noise that appears like a sinc^2 function with main lobe bandwidth of 1/ t_0 Hz. Total power of part (i) is,

$$P_i = \left[1 - \frac{t_0}{T} - \left(1 - \frac{t_0}{T}\right)^2\right] P_{sig} \quad (25)$$

Thus, the power of part (ii) is,

$$P_{ii} = P_{sig} - P'_{sig} - P_{nh} = \frac{t_0}{T} P_{sig} \quad (26)$$

Similarly, the total noise power P_n falling in the original signal band is,

$$P_n = P_{ii} \times \int_0^{BW} \frac{2}{BW_{PRS}} sinc^2(\pi f / BW_{PRS}) df \quad (27)$$

To figure out the degradation in SNR, let us assume a 20% timing mismatch. The recovered signal power is 64% of P_{sig}, and total in-band noise power is 0.8% of P_{sig}.

Therefore, the in-band SNR without any interference after baseband filtering is limited to 19dB.

If $t_0 > T$, the two PRSs are mismatched by more than one bit. The product of these two PRSs has a negligible dc component, and the echo signal cannot be recovered. In general, it is necessary to guarantee a timing mismatch less than 25% of clock cycle T.

6.2. Synchronization scheme

As demonstrated in the previous section, a synchronization scheme limiting the timing error is necessary to guarantee the signal quality of DSSS technique based communication systems.

As mentioned before, because the PRS used for modulation and demodulation has an autocorrelation function that is highly sensitive to timing error, the recovered signal power is significantly affected by the timing error. However, this high sensitivity of timing error also makes the autocorrelation function a criteria to determine whether synchronization is achieved or not.

As is shown in Figure 3.6, the autocorrelation function of Nth order PRS has a period of $(2^N-1)T$, where T again is the period of the clock cycle used in the PRS generator based on LFSR structure; the peak of the autocorrelation has a width of two clock cycles; for any timing offset that is more than ±T, the autocorrelation function is constant and small enough to be negligible. Therefore, by calculation of the correlation between the received PRS and the PRS in the RX, we can determine if the PRSs are synchronized within one clock cycle.

Tons of researches on synchronization scheme in DSSS system have been reported in the area of digital communication. The synchronization process is usually achieved in two steps: code acquisition or coarse synchronization and code tracking or fine acquisition.

6.2.1. Code acquisition

The code acquisition is to match the code words in the reference PRS to that in the received PRS, or to minimize the timing error within one clock cycle with coarse synchronization. However, because the peak of the autocorrelation function is as narrow as two clock cycles, an exhaustive search of correct code word has to be done. The basic working principle can be depicted in the following block diagram.

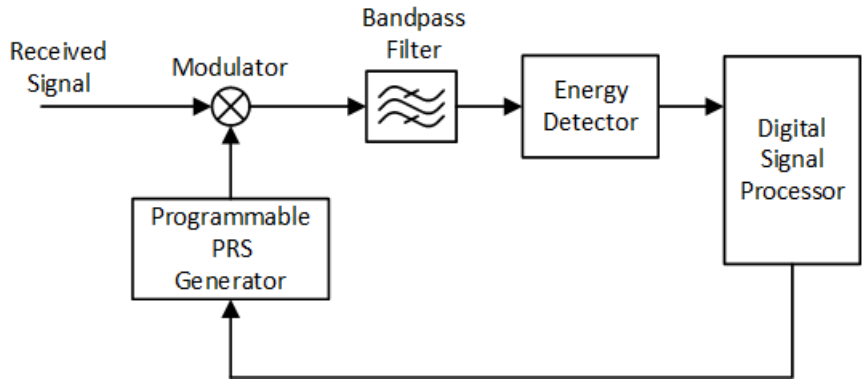


Figure 6.2. Block diagram of code acquisition module.

As shown in the block diagram above, the code acquisition process is done by trying to recover the received signal with all the PRSs with every possible code phases. For each attempt, the power of the recovered signal is used as a criteria to decide whether the code acquisition process is accomplished. Based on the number of code phases that can be tried at one time, the search strategies can be categorized into two large groups: serial search and parallel search [39].

Serial search [40,41] requires the reference PRS in RX to compare with the received PRS clock cycle by clock cycle in one direction. This although inevitably increases the time required for code acquisition process, is the most hardware efficient method, because only one code acquisition module is required. Therefore, serial search strategy is more attractive to low power portable applications, such as GPS systems.

On the contrary, parallel search [42] can increase the speed of code acquisition drastically by doing multiple attempts at the same time. However, multiple code acquisition modules have to be implemented, which inevitably increase the cost of power and silicon area. This strategy is more suitable for performance-first applications, such as cellular base stations.

6.2.2. Code tracking

Code tracking or fine synchronization is the process to align the transition in the received signal with the transition in the reference PRS, and guarantee the timing of the received signal is tracked by the reference PRS. This process is usually achieved with a delay lock loop. With the help of negative feedback, large DC loop gain limit the timing error between the two signals within certain tolerance. The delay lock loop can be achieved in both digital and analog domain, which means the timing of the reference PRS can be either modified based on the timing errors feedback both by changing number of discrete digital delay cells and by tuning analog delays continuously.

6.3. Three-level synchronization scheme

When PRS itself is used for synchronization purpose, the recovered signal has a DC component according to (12), which is highly sensitive to timing mismatch. In this case the bandpass filter and energy detector are replaced with a lowpass filter. The block diagram of this system is shown below.

In this type of system for synchronization, for serial search strategy, during synchronization phase the timing of the PRS in RX can be adjusted according to the DC component of the recovered signal, which is directly proportional to the correlation between the received PRS and the PRS in RX. However, due to the high selectivity of the autocorrelation function of PRS, the width of the peak is only two bits of the PRS, while all other timing error beyond ±T will give a low DC component. This DC component is so small and unreliable that it cannot be used as an indication for comparison to decide if the moving direction is correct or not, when timing error is beyond ±T. As a result, this DC component can only be used for comparison with a preset threshold to indicate if the timing error is within ±T, and as an indication for moving direction only when timing error is already within ±T. In this case, the narrow peak of correlation function and the long period of PRS may cause a long time dedicated for serial search, if the first arbitrary selection for moving direction is incorrect. To alleviate this effect, it is necessary to have a starting point for search that is as close as possible to the correct timing.

Therefore, we propose a synchronization scheme shown in the following figure, that is achieved in three levels.

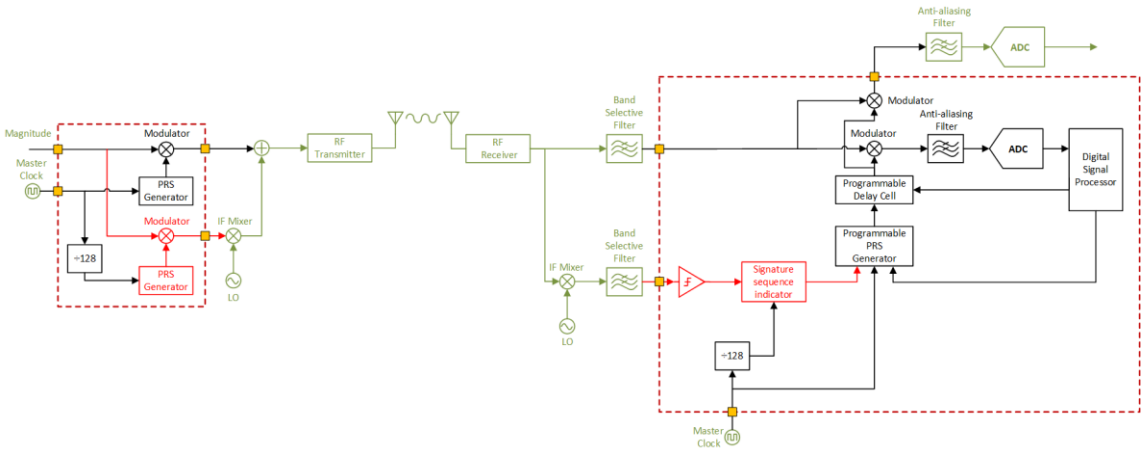


Figure 6.3. Block diagram of three-level synchronization scheme.

1) Firstly in the red path, a narrowband PRS is transmitted through another dedicated frequency band, where on the RX side noise and blockers are filtered by a sharp low pass filter. The digital PRS is recovered by a comparator and passed through a signature sequence indicator to find out if the correct timing is close or not.
2) Secondly, after the indicator shows the coming of the signature sequence, the wideband PRS in RX is activated and preset to be several bits behind the correct timing. From this starting point, the timing of the wideband PRS is moved forward by one clock cycle every period of the PRS, and the DC component of the output signal is compared with the preset threshold in digital domain. When this DC component is higher than the preset threshold, it indicates that the timing error is within ±T.
3) Finally, the timing of the PRS is modified slightly by 10% of the clock cycle each time with a programmable delay cell, and the DC component of the output

signal is compared with the previous case. According to the result of comparison, the system determines to move forward or backward, until the DC component of the output signal is maximized.

The flow chart of the algorithm embedded in RX for synchronization is shown as follows.

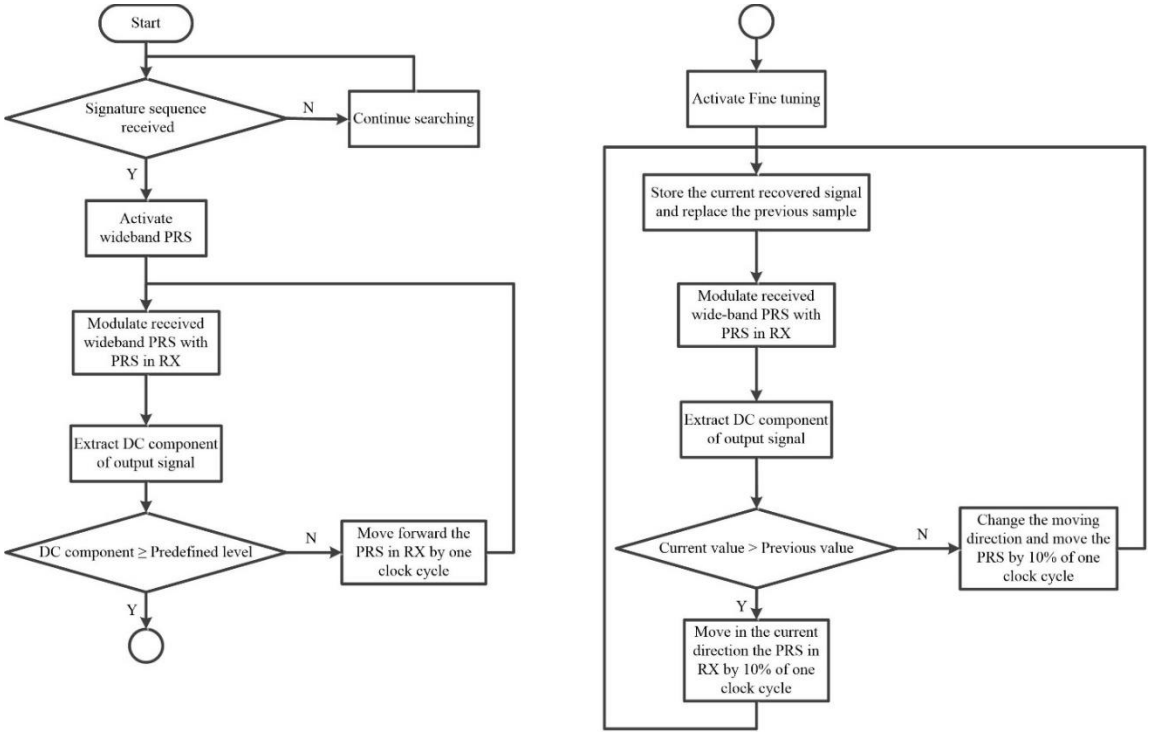


Figure 6.4. Flow chart of three-level synchronization scheme.

To proof the feasibility of this synchronization scheme, an IC prototype was designed and fabricated with 40nm CMOS technology.

7. AN EFFICIENT SINUSOID-LIKE PSEUDO RANDOM SEQUENCE MODULATOR/DEMODULATOR SYSTEM WITH REDUCED ADJACENT CHANNEL LEAKAGE AND HIGH REJECTION TO RANDOM AND SYSTEMATIC INTERFERENCE[1]

7.1. Introduction

Frequency spectrum has become a scarce natural resource with the emergence of new wireless communication services. Wider frequency bands have been demanded by wireless communication services in the era of 5G to provide over 1Gbps data rate and less than 5ms latency [4]. In contrast, high bandwidth for radar translates into fine range resolution, which directly relates to sensing capability [43]. The increasing demand for frequency spectrum from both communication services and radar system inevitably leads to the increasing possibility of spectral collision.

From the radar point of view, spectral collisions with either the main channel signals or merely the adjacent channel leakage of wireless communication systems will degrade radar performance [44] and cause false alarm or missed detections. Although the spectral mask for communication standard is stringent to limit the neighbor channel to under -30dBr [45], the amount of power transmitted by base stations may still interfere with radar systems, considering that desired echo signal can go through round trip

[1] © 2020 IEEE. Reprinted with permission from J. Shao, A. I. Karsilayan, C. T. Rodenbeck and J. Silva-Martinez, "An Efficient Sinusoid-Like Pseudo Random Sequence Modulator/Demodulator System With Reduced Adjacent Channel Leakage and High Rejection to Random and Systematic Interference," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 11, pp. 3790-3803, Nov. 2020.

attenuation in excess of 100dB. Increasing the communications system's guard bands limit interference to the radar systems, filtering techniques in base stations can alleviate this issue. In addition, several interference rejection strategies have been reported based on spatial solutions using MIMO and beamforming techniques [46-50], on spectral solutions using frequency hopping [51,52], on coding solutions [53-59]. MIMO and beamforming techniques are suitable for phased array radar; the use of multiple antennas multiple RF frontends and ADCs, higher power consumption and increased complexity are some of the drawbacks of this approach. Authors in [51,52] are able to change the frequency modulation parameters of the radar signal to mitigate mutual interference; frequency hopping technique requires high performance frequency synthesizers which potentially consume a large amount of power, therefore, it is not suitable for wideband interference attenuation. Apart from spectral collision, self-interference due to TX RX coupling in compact single chip transceiver design, is also a major concern in both radar systems and communication systems. Direct sequence spread spectrum (DSSS) is a promising solution for self-interference issues, because it is capable of reducing overall interference by making use of coding properties. The self-interference reaches the RX much earlier than the echo signal. When demodulated with the pseudo random sequence, the self-interference is randomized and spread over wide frequency, whose power is attenuated through filtering and processing gain.

In this paper, we propose a pseudo-random modulator/demodulator system that operates at baseband in analog domain and use a sinusoid-like pseudo random sequence (SPRS) that improves the adjacent channel leakage ratio (ACLR) by 22dB when compared

with the binary pseudo random sequence (BPRS). Modulation at baseband is more power and area efficient than at RF frequency [55-60], and makes possible modulation schemes that are more sophisticated than just BPSK. Modulation in analog domain rather than in digital domain [54,61] reduces the bandwidth requirement of data converters, and relaxes the dynamic range requirement of the receiver ADC, because random and systematic interferers are further rejected before the ADC. The proposed system randomizes the systematic interferences, thereby increases the effectiveness of averaging techniques against both systematic and random in-band interference.

The paper is organized as follows. Section 7.2 introduces the proposed pseudo-random modulator/demodulator system based on a SPRS modulator to reduce the adjacent channel leakage. Section 7.3 introduces the system architecture and circuit implementations of the main analog and digital building blocks. Section 7.4 presents some important post-layout simulation results to prove the feasibility and benefits of this technique. Section 7.5 demonstrates the benefits through measurement results and compares with other related works. The conclusions are provided in Section 7.6.

7.2. Mixed signal IC technique for co-existence

For two signals to be distinguishable, they need to be orthogonal. For example, signals are orthogonal in time for TDM, in frequency for FDM, in digital coding for CDMA. TDM and FDM schemes are frequently used but they do not offer efficient use of the spectrum available, and do not make the communication system tolerant to in-band interferers. FDM is currently used to protect radars from wireless communication systems

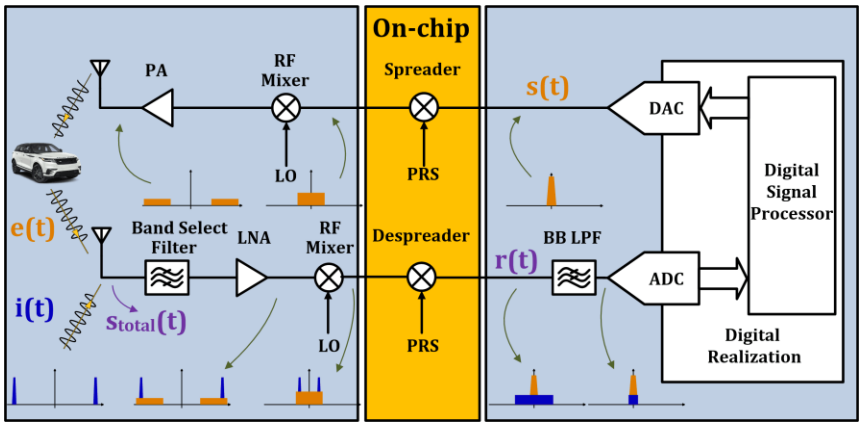
but the guard frequency band is being reduced, therefore, spectral collisions increased. Digital coding is another option for minimizing the effect of these collisions. Given the information about coding implemented in the transmitter (TX), the signals can be decoded in the receiver (RX), while arbitrary in-band interference can be attenuated to a larger extent. Thus an improvement in signal to noise ratio is achieved. For example, [55] combines binary code domain modulation with n-path mixer; [56] merges the binary code domain modulator with PA and LNA design; [57] implements an n-path integrate and dump filter after code modulation. Authors in [58] add two extra modulators and a band reject filter in between to reject the interference with specific modulation. Radar designs based on binary PRS have also been reported [59,60]. These radar systems modulate the phase of the RF carrier at RF frequency, then are harder to implement with CMOS process compared with the proposed DSSS system implemented at baseband.

In the proposed modulator/demodulator system, the radar RX has the capability of attenuating the leakage from communication systems falling in the radar signal band. Contrary to the case of out-of-band interference, in-band interference power cannot be attenuated by conventional filtering, since the signal will be attenuated by the same ratio as well. Another relevant issue is the self-leakage from the TX into the RX if the transceiver or radar operates in the same frequency band. In this paper, we propose a mixed signal IC technique that operates at baseband in front of the ADC that employs direct sequence spread spectrum (DSSS) techniques. A sinusoid-like modulation is used to reduce the adjacent channel leakage.

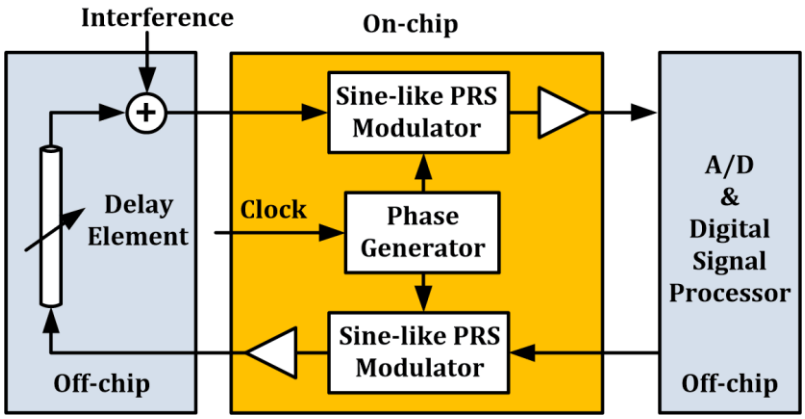
7.2.1. Direct sequence spread spectrum

The block diagram of a proposed analog DSSS system is shown in Figure 7.1. In this system, a baseband signal (that could be a single tone, chirp, CDMA or OFDM signal) is first mixed with a wideband PRS in TX before the signal is up-converted to radio frequency band. The received signal is then mixed with the synchronized PRS signal in RX after down-conversion to baseband. The two modulations in baseband help attenuating the effects of the in-band interference power. This approach is especially effective in reducing the power of systematic interference, which cannot be attenuated through averaging techniques unless these signals are randomized.

In the frequency domain, the input signal's spectrum is first convolved with the PRS to expand its bandwidth. The spread signal is then amplified and up-converted to the radio frequency band. In the RX, the echo signal is detected by the antenna altogether with in-band interference. Desired echo signal and interference, are amplified and down-converted to baseband; after that the signals convolve with a PRS signal with the same coding. If synchronized, this operation compresses the bandwidth of the desired signal to the original bandwidth, while expands the bandwidth of the uncorrelated interference. Non-random uncorrelated interference are randomized due to the pseudo-random property of the PRS. Finally after baseband filtering, the out-of-band noise is removed before the ADC.



(a)



(b)

Figure 7.1. (a) Block diagram of the proposed modulator/demodulator system based on DSSS technique and (b) The PRS systems and phase generator are realized on-chip, and the RF front-end is emulated by an external delay element.

7.2.2. Pseudo-Random Sequence

The PRS can be generated employing a digital structure known as Linear Feedback Shift Register (LFSR) [62]. For an Nth order LFSR, which has N shift registers, the period of a generated PRS is $(2^N-1)T$, where T is the clock period. The power spectral density of a bipolar BPRS is a $sinc^2(f)$ function with a main lobe of BW_{PRS} that can be described as,

$$PRS(f) = \frac{1}{BW_{PRS}} \cdot \left[\frac{sin(f/BW_{PRS})}{f/BW_{PRS}}\right]^2 \quad (28)$$

The single side power spectral density function of a 100MHz BPRS is shown in

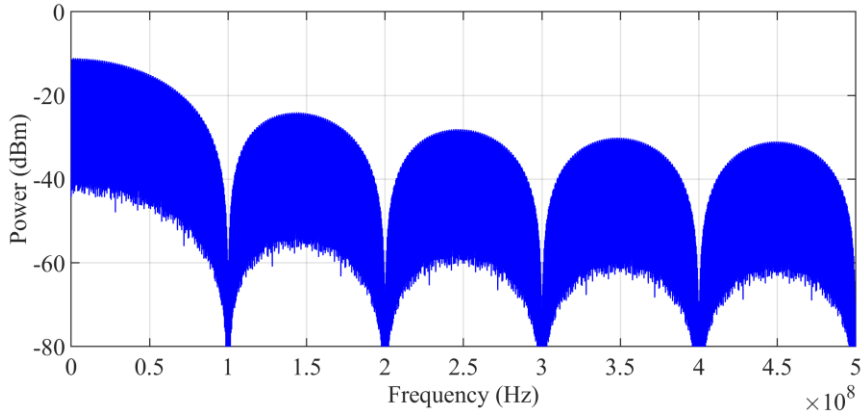


Figure 7.2. Power spectral density function of a 100MHz Binary PRS.

Figure 7.2. For this BPRS, the main lobe has a bandwidth of 100MHz, with nulls at multiples of the clock frequency. This signal is broadband and even the 5th lobe is only attenuated by -20dB compared with the first lobe. If BPSK is used for the PRS signal in Figure 7.1, significant leakage in adjacent channels will be generated, therefore, broadband high-order phase linear filtering is needed to attenuate the high frequency lobes.

7.2.3. In-band interference attenuation

Let us consider the case of an ideal RF front end, which means linear gain, no bandwidth limitation, and perfect timing between the PRS modulated echo signal and the reference PRS. According to Figure 7.1, the signal $s(t)$ with a power of P_{sig} and a bandwidth of BW is mixed with a binary $prs(t)$ which has a bandwidth of the first lobe equal to BW_{PRS} and unity amplitude. If the gain in TX and RX are A_{TX} and A_{RX} , respectively, and the loss in the signal channel is A_L, the echo signal (ignoring frequency conversion) is characterized as follows:

$$e(t) = A_{TX}A_L s(t - t_0) \times prs(t - t_0) \tag{29}$$

Where t_0 is the round trip delay of the echo signal. This signal is received by RX antenna together with the in-band interference signal $i(t)$. After amplification and down-conversion, let us assume that $A_{RX}i(t)$ has a power density of S_I and its bandwidth is BW_{PRS}. The total received baseband signal $s_{total}(t)$ is then mixed with the reference $prs(t - t_0)$. Ignoring the PRS timing mismatch, the de-spread or recovered signal $r(t)$ is given by,

$$r(t) = A_{TX}A_{RX}A_L s(t - t_0) \times prs(t - t_0) \times prs(t - t_0) + A_{RX}i(t) \times prs(t - t_0) \tag{30}$$

Employing the Parseval's theorem and assuming that $i(t)$ and $prs(t - t_0)$ are uncorrelated, the double sideband RX signal components are,

$$R(f) = A_{TX}A_{RX}A_L S(f) + A_{RX}I(f) * PRS(f) \tag{31}$$

Where the symbol * stands for the convolution operation. After the de-spread signal $r(t)$ is filtered out with a low pass filter with a bandwidth of BW Hz, the echo signal $S(f)$ is perfectly recovered. The interference signal, however, convolves with the reference $PRS(f)$ and its power is widely spread and then most of it is effectively removed to a large extent by the baseband filter. The estimated interference power reduction after mixing and filtering can be obtained as,

$$Interference_{reduction} = \frac{\int_{-BW}^{BW} |I(f) * PRS(f)|^2 df}{\int_{-BW_{PRS}}^{BW_{PRS}} |I(f)|^2 df} \tag{32}$$

If $I(f)$ shows a flat power spectral density S_I, which is the case for a frequency modulated continuous waveform (FMCW), PRS or OFDM signals, with a bandwidth of BW_{PRS}. Therefore,

$$Interference_{reduction} = \frac{BW}{BW_{PRS}} \frac{\int_{-BW}^{BW} \left[\sqrt{\frac{S_I}{2BW_{PRS}}} \times rect\left(\frac{f}{2BW_{PRS}}\right) * \frac{1}{BW_{PRS}} \left[\frac{sin(f/BW_{PRS})}{f/BW_{PRS}}\right]\right]^2 df}{S_I \times 2BW} \quad (33)$$

In this prototype, BW_{PRS}=10BW, or equivalently, the spectrum spreading ratio is 10. Equation (6) predicts an SNR improvement of 10.9dB. However, the main advantage of this approach lays on the random nature of the resulting interference.

Consider that part of the interference signal $i(t)$ is not fully random and that the interference power P_I is composed of two parts: a systematic part P_{I_S} and a random component P_{I_R}. Without the DSSS technique, the processing gain PG with an average of X samples is computed as,

$$PG = \frac{\frac{P_{sig} \cdot X^2}{P_{I\_S} \cdot X^2 + P_{I\_R} \cdot X}}{\frac{P_{sig}}{P_{I\_S} + P_{I\_R}}} = \frac{P_{I\_S} + P_{I\_R}}{P_{I\_S} + \frac{P_{I\_R}}{X}} \quad (34)$$

Notice in this equation that the systematic interference component P_{I_S} does not reduce with the averaging factor X, thus limiting the value of the PG.

When using the DSSS technique, all interference components become pseudo-random after mixing with $prs(t)$ in the RX. Therefore, the processing gain PG becomes equal to the averaging factor X. Thus, the processing gain increases proportionally with the averaging factor regardless if the original interference is systematic or random.

7.2.4. Synchronization requirement

In the previous section we assumed that the PRS signal in TX and that in RX are fully synchronized in time. In the presence of a timing mismatch of t_0 seconds between the two PRSs, the Fourier transform of the recovered echo signal is,

$$S'(f) = S(f) * \int_{-\infty}^{+\infty} PRS(t) \times PRS(t - t_0)\, e^{-j2\pi ft} dt \tag{35}$$

The dc component of $prs(t) \times prs(t - t_0)$ is used to recover the signal $s(t)$, and is the autocorrelation function $R_{\alpha\alpha}(t_0/T)$ of the N[th] order PRS with a clock period of T. This function is shown in Figure 7.3.

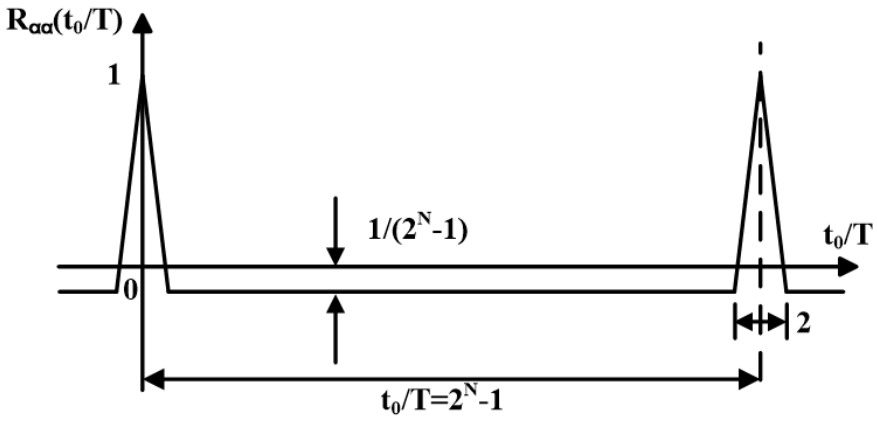


Figure 7.3. Autocorrelation function of PRS.

According to Fig.3, $R_{\alpha\alpha}(t_0/T)$ has a period of $(2^N-1)T$ seconds, which is also the period of the PRS. For an 11[th] order 100MHz PRS, T_{PRS} is about 20.5us. Consider the case of transmission through the air, the round trip time delay of the echo signal is 0.67μs, 6.7μs and 67μs for the distance of 100m, 1km, and 10 km, respectively. To avoid ambiguity, proper order N of the PRS must be selected, so that T_{PRS} is larger than the

round trip delay associated with the maximal detectable range. The ambiguity of detecting two targets at the same time requires the difference of distance D to the RX antenna to be,

$$D = \frac{c\times(2^N-1)T}{2} \tag{36}$$

Where c is the speed of the light. It is assumed that the electromagnetic wave is travelling through the air at $c=3\times10^8$ m/s. If N is properly selected and ambiguity has already been avoided for a particular application, it is expected that $t_0 < (2^N - 1)T$. Thus, the Fourier transform of $prs(t) \times prs(t - t_0)$ becomes,

$$\int_{-\infty}^{+\infty} prs(t) \times prs(t - t_0)e^{-j2\pi ft}dt = \alpha\delta(f) + W(f) \tag{37}$$

Where, $\alpha\delta(f)$ is the dc component responsible for recovering the signal, $W(f)$ is the wideband noise generated due to the timing error. Because $prs(t)$ is a periodic signal with a period of $(2^N-1)T$, the dc component α of $prs(t) \times prs(t - t_0)$ can be calculated as,

$$\alpha = \frac{1}{(2^N-1)T}\int_0^{(2^N-1)T} prs(t) \times prs(t - t_0)dt \tag{38}$$

Notice that $prs(t) \times prs(t - t_0)$ in each clock period T can only have two posibilities: 1) when there is no transition in $prs(t)$, the value of $prs(t) \times prs(t - t_0)$ is 1; 2) when there is a transition in $prs(t)$, $prs(t) \times prs(t - t_0)$ generates a rectangular glitch related to the t_0 as shown in Figure 7.4. Therefore,

$$\alpha = \frac{1}{(2^N-1)T}\left(\sum_1^M \int_0^T prs(t) \times prs(t - t_0))dt + \sum_{M+1}^{2^N-1} \int_0^T prs(t) \times prs(t - t_0)dt\right) \tag{39}$$

Where, M is the number of transitions in one period of $prs(t)$.

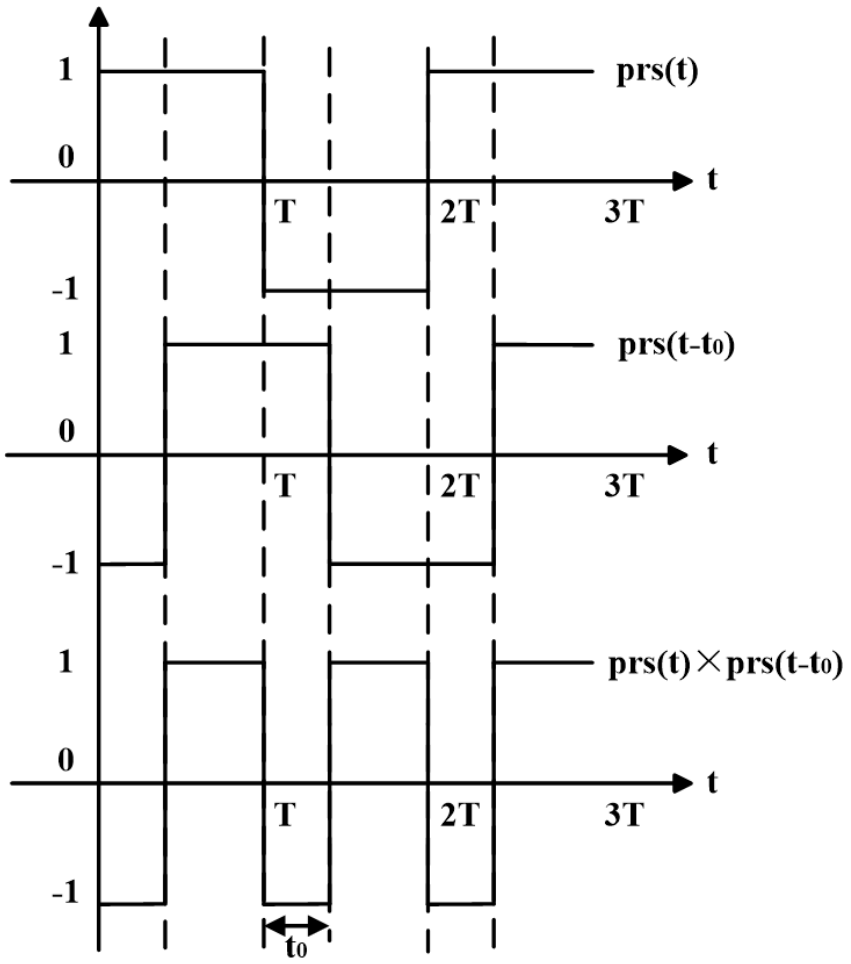


Figure 7.4. Time domain waveform of prs(t) and prs(t)×prs(t-t0).

According to Figure 7.4, the dc component of $prs(t) \times prs(t - t_0)$ in one clock period, with transition, is equal to $1\text{-}2t_0/T$. Evidently, the dc component of $prs(t) \times prs(t - t_0)$ in one clock period without transition is 1. For an N^{th} order PRS, in each period the number of "ones" is 2^{N-1}, and the number of "zeros" is 2^{N-1}-1. Therefore, the probability P_{01} of a "zero" followed by a "one" and the probability P_{10} of a "one" followed by a "zero" are,

$$P_{01} = \frac{2^{N-1}}{2^N - 2}, P_{10} = \frac{2^{N-1} - 1}{2^N - 2} \tag{40}$$

Thus, the probability of a transition P_T and number of transitions M considering the two possible current states can be calculated as,

$$P_T = \frac{2^{N-1}-1}{2^N-1}P_{01} + \frac{2^{N-1}}{2^N-1}P_{10} = \frac{2^{N-1}}{2^N-1} \tag{41}$$

$$M = (2^N - 1) \times P_T = 2^{N-1} \tag{42}$$

Thus for N ≥ 7, the coefficient α can be approximated with an error of less than 1% by the following simplified equation,

$$\alpha = \left(1 - \frac{2t_0}{T}\right) \times \frac{M}{2^N-1} + \left(1 - \frac{M}{2^N-1}\right) \cong 1 - \frac{t_0}{T} \tag{43}$$

To calculate the noise power generated because of timing error, we need to find out the frequency spectrum of $prs(t) \times prs(t - t_0)$. In time domain, this signal resembles another BPRS $prs'(t)$ sampled with a square wave $p(t)$. The mathematical expression is as follows,

$$prs(t) \times prs(t - t_0) = prs'(t) \times p(t) + 1 - p(t) \tag{44}$$

Where $prs'(t)$ is a BPRS with the same period of $(2^N\text{-}1)T$, and $p(t)$ is a square wave with a period of T and with a pulse width percentage of t_0/T. Hence, the noise power caused by the timing error has two parts; namely i) the higher order harmonics of $p(t)$, and ii) the wide band noise that appears like a sinc^2 function with main lobe bandwidth of $1/ t_0$ Hz. Total power of part (i) is,

$$P_i = \left[1 - \frac{t_0}{T} - \left(1 - \frac{t_0}{T}\right)^2\right] P_{sig} \tag{45}$$

Thus, the power of part (ii) is,

$$P_{ii} = P_{sig} - P'_{sig} - P_{nh} = \frac{t_0}{T} P_{sig} \tag{46}$$

Similarly, the total noise power P_n falling in the original signal band is,

$$P_n = P_{ii} \times \int_0^{BW} 2t_0 sinc^2(\pi t_0 f) df \quad (47)$$

To figure out the degradation in SNR, let us assume a 20% timing mismatch. The recovered signal power is 64% of P_{sig}, and total in-band noise power is 0.8% of $P_{sig.}$ Therefore, the in-band SNR without any interference after baseband filtering is limited to 19dB.

If $t_0 > T$, the product of the two PRSs has a negligible dc component, and the echo signal cannot be recovered. As a special, yet relevant case, the self-interference due to TX leakage has a much smaller delay than the round trip delay of the desired echo signal. As a result, when the $prs(t - t_1)$ is tuned for a desired range, the self-interference signal $l(t)$ after demodulation will be randomized,

$$l(t) = s(t - t_0) \times prs(t - t_0) \times prs(t - t_1) \quad (48)$$

Then this randomized signal is attenuated by averaging. In general, it is necessary to guarantee a timing mismatch less than 25% of clock cycle T to recover the echo signal.

7.2.5. Enhancing ACLR performance: Sinusoid-like PRS

A major issue in BPRS based designs [55-58] is that the power level of the high frequency side lobes are not acceptable in most of the wireless communication standards, such as the different varieties of 802.11 series. In 802.11b, according to its spectral mask, the ACLR is required to be 30dB, and the 2nd and 3rd signal lobes of the PRS signal must be suppressed 30dB and 50dB below the power of the main lobe. For the conventional BPRS, it can be found that the power of the first and second lobes are related as follows,

$$\frac{P_{main}}{P_{2nd}} = \frac{\int_0^1 2sinc^2(\pi x) dx}{\int_1^2 2sinc^2(\pi x) dx} = 12.8dB \quad (49)$$

Although filtering techniques [63,64] can be used to limit the adjacent channel power leakage, power (≥30mW) and silicon-area (≥0.5mm^2) hungry filtering is needed. On top of these approximations, filtering with linear phase response is required to preserve the range information. As an alternative, a sinusoid-like PRS (SPRS) is proposed in this paper. Instead of the pulse-like BPRS signal, the low-high and high-low transitions are implemented using a piecewise linear transition with six levels spaced according to a sinusoid variation. Figure 7.5 shows an example of a 100MHz SPRS and its binary counterpart, where the SPRS employs five steps to achieve one transition of the original BPRS. The SPRS can be considered as a BPRS filtered by a 5-tap FIR filter. For each digital delay cell in the FIR filter, the sample frequency T_S is 0.2T. The discrete time transfer function H(z) of this 5-tap FIR filter is,

$$H(z) = 0.1 + 0.25z^{-1} + 0.3z^{-2} + 0.25z^{-3} + 0.1z^{-4} \quad (50)$$

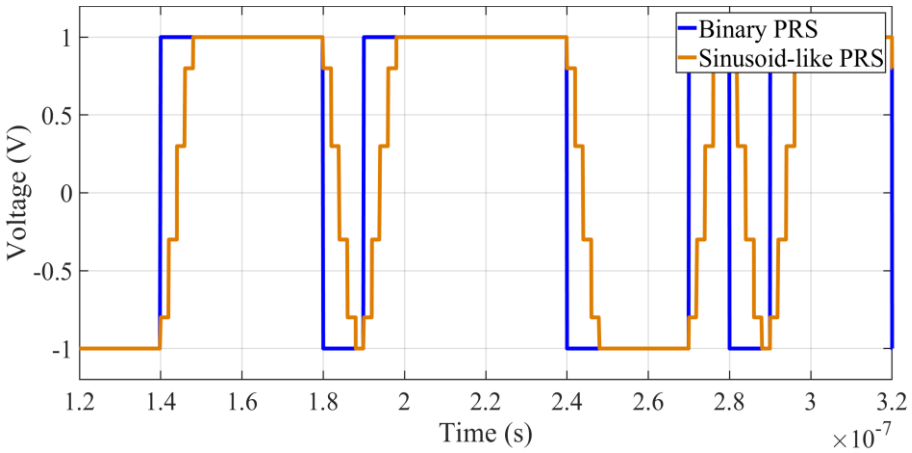


Figure 7.5. 100MHz Binary PRS and 100MHz Sinusoid-like PRS in time domain.

The magnitude response and phase response of this FIR filter is shown in Figure 7.6. This FIR filter adds notches at the middle of the original lobes to reduce further the power on the adjacent channels, as depicted in Figure 7.7.

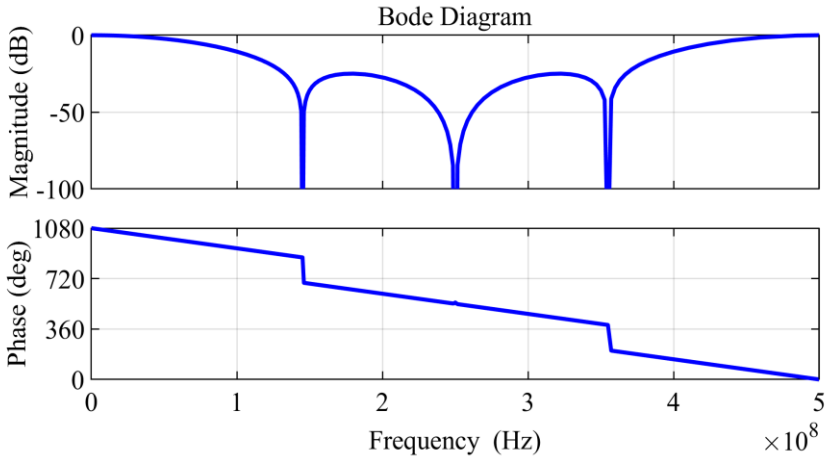


Figure 7.6. Frequency response of 5-tap FIR filter.

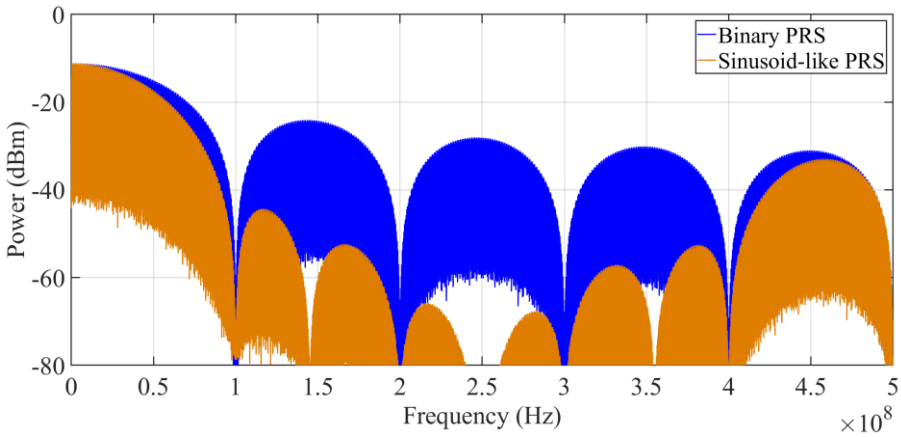


Figure 7.7. Power spectral density functions of Binary PRS and Sinusoid-like PRS.

For the case of the proposed SPRS sequence, the ratio of power of main signal channel to adjacent channel including the two consecutive adjacent lobes is computed as,

$$\frac{P_{main}}{P_{2nd}+P_{3nd}} = \frac{\int_0^{BW_{PRS}} 2sinc^2(f/BW_{PRS})\times|H(jf)|df}{\int_{BW_{PRS}}^{3BW_{PRS}} 2sinc^2(f/BW_{PRS})\times|H(jf)|df} \quad (51)$$

This power reduction meets the requirement transmission spectral mask for several standards, including 802.11b, which can only be achieved in the conventional BPRS case by adding an 11th order 100MHz Butterworth. With the proposed technique, however, only cheap filtering will be needed to reduce the power of the high frequency lobes to co-exist with more demanding standards such as 802.11ax. Apart from filtering, some other works are reported [59,65] to improve spectral efficiency.

7.2.6. Recovered signal

For the case of modulation and demodulation with an ideal BPRS, the signal is perfectly recovered because,

$$prs(t) \times prs(t) = 1 \tag{52}$$

However, due to bandwidth limitation in different blocks, $prs(t)$ presents smooth transitions that inevitably results in the glitches in the waveform of $prs(t) \times prs(t)$. For $prs(t)$ with an arbitrary shape of transition the spectrum of output signal $r(t)$ follows,

$$R(f) = S(f) * \int_{-\infty}^{+\infty} prs(t) \times prs(t) e^{-j2\pi ft}\, dt \tag{53}$$

Again, the Fourier transform of $prs(t) \times prs(t)$ is composed of two parts, the dc component $\alpha\delta(f)$ which is responsible for recovering the signal and the wideband noise $W(f)$ generated due to the shape of transition in $prs(t)$. The computation of α follows the same approach discussed in part D, therefore, we only show the final result here.

$$\alpha = \frac{2^{N-1}}{2^N-1}\frac{1}{T}\int_0^T prs(t) \times prs(t) dt + \frac{2^{N-1}-1}{2^N-1} \tag{54}$$

In the case of $sprs(t)$, $sprs(t)$ and $sprs(t) \times sprs(t)$ follow the waveforms shown in Fig.8, the value of α is estimated as 0.7455, which means the modulation and

demodulation with $sprs(t)$ results in a 2.55dB degradation in the signal power. The value of in-band $W(f)$ is calculated employing MATLAB, and is around 0.013, which translates to an in-band SNR of 16.4dB.

But notice that this wideband noise is random and can be attenuated employing averaging techniques.

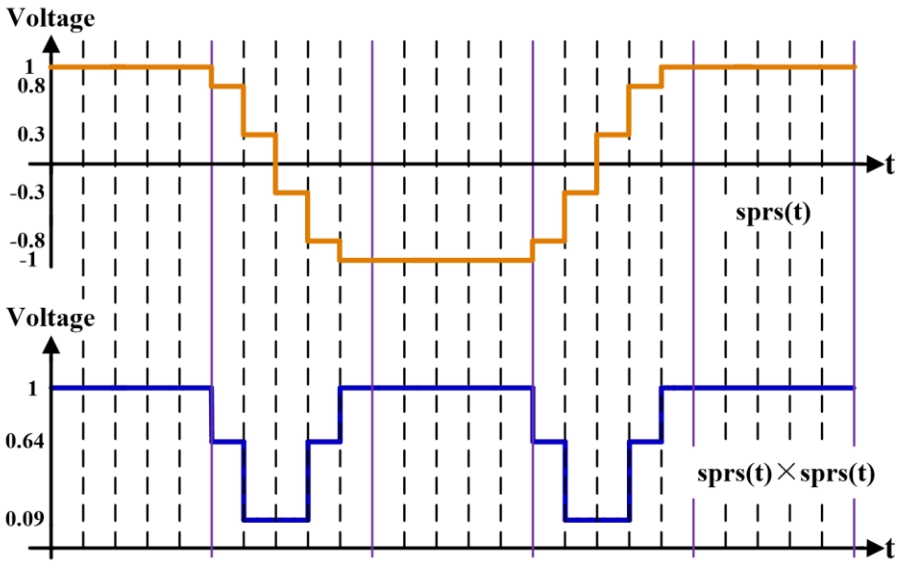


Figure 7.8. Time domain waveform of sprs(t) and sprs(t)×sprs(t).

7.3. Physical Implementation

As an experimental proof of the proposed concepts, a chip is designed and fabricated employing 40nm CMOS technology. The system level architecture is shown in Figure 7.9.

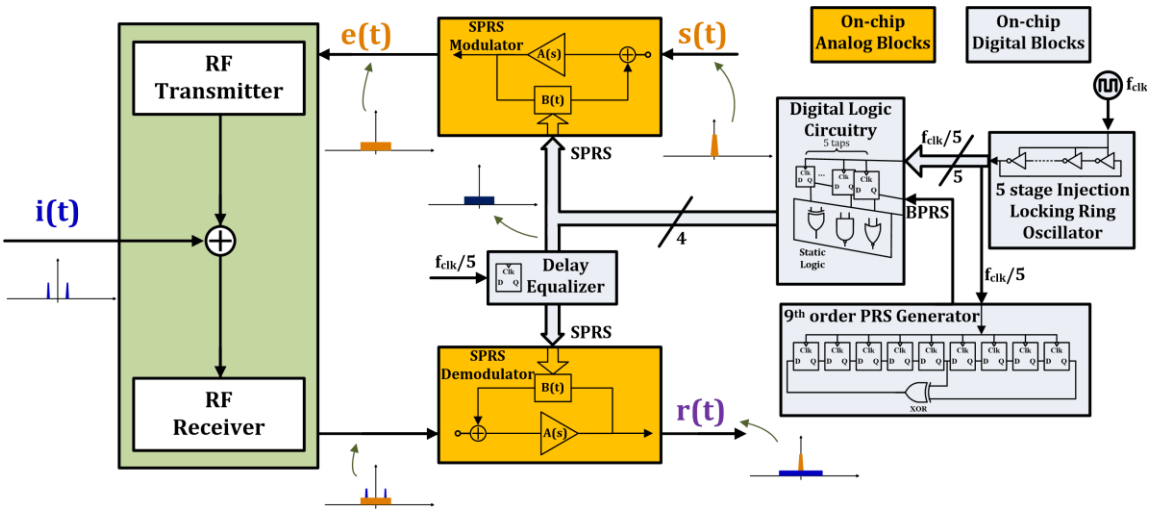


Figure 7.9. System level of the proposed SPRS based modulator-demodulator.

7.3.1. System level architecture

Four main parts are implemented on chip, including the sinusoid-like analog modulator/demodulator, the locking oscillator, a BPRS generator, and the control phase generator that generates 5 coherent time shifted replicas of the BPRS to generate the 4 control signals.

The sinusoid-like modulator is based on a programmable resistive feedback amplifier, whose input resistors are swapped according to the BPRS; this operation modulates the incoming signal with the BPRS. Two control signals generated from 5 synchronized BPRS signals control the voltage gain of the programmable gain amplifier

(PGA) with the aim of making the modulation transitions to follow a discrete sinusoid-like waveform. The sinusoid-like transition requires the generation of 5 clock phases, whose difference between each clock phase is T_{clk}, the period of the master clock, which is 5 times the clock rate of the BPRS. The required clock phases are generated from a 5-stage injection locking ring oscillator; one of these phases is used as a reference and is fed into a 9^{th} order Linear Feedback Shift Register (LFSR) for the generation of the BPRS, which runs at an equivalent clock frequency of $f_{clk}/5$. The demodulator employs the same control signals and a similar PGA.

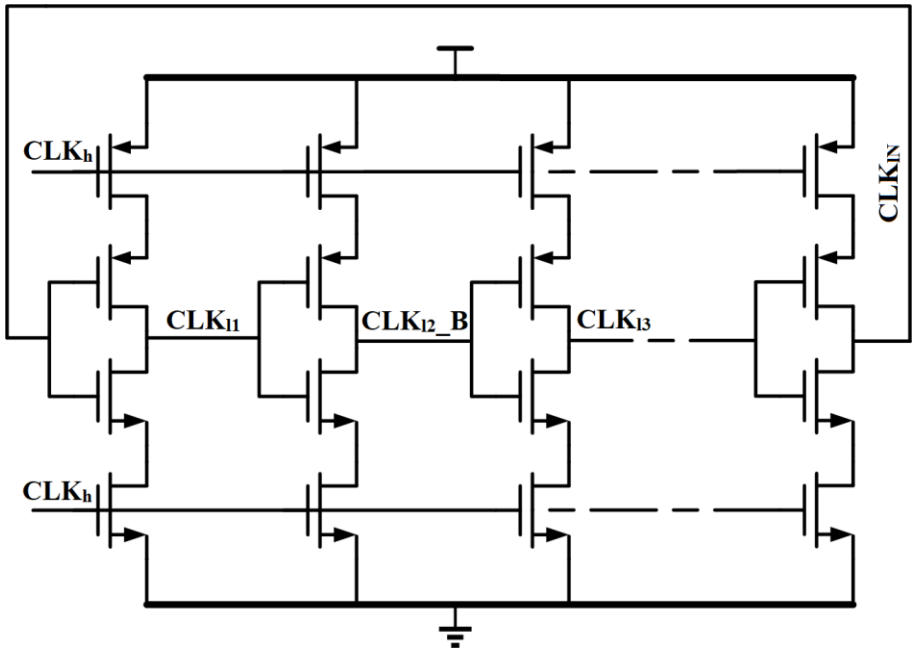
The programmable delay control unit based on a chain of flip-flops in the delay equalizer determines the objects at a given range through the adjustment of the time delay Δt. In a real radar system, multiple delayed replicas of the BPRS are employed to detect objects at multiple distances. Only the echo signal with similar delay as Δt will be detected by the RX, since the autocorrelation function of the BPRS with a delay over one clock period T is almost zero, as shown in Figure 7.3.

The received echo signals $e(t)$ plus the interference $i(t)$ (random and systematic) are then convolved with the SPRS in the RX. The echo component with a time delay similar to the one defined by the delay equalizer block is recovered, while other echoes whose timing are over one clock period different will be randomized since the SPRSs are uncorrelated due to the time mismatch. To the best of authors' knowledge, the conventional radar system does not deal with the case of systematic interference, because averaging techniques are not effective in this case as is shown in (10).

Before discussing the modulator/demodulator architectures, let us describe the circuits that generate the required clocks.

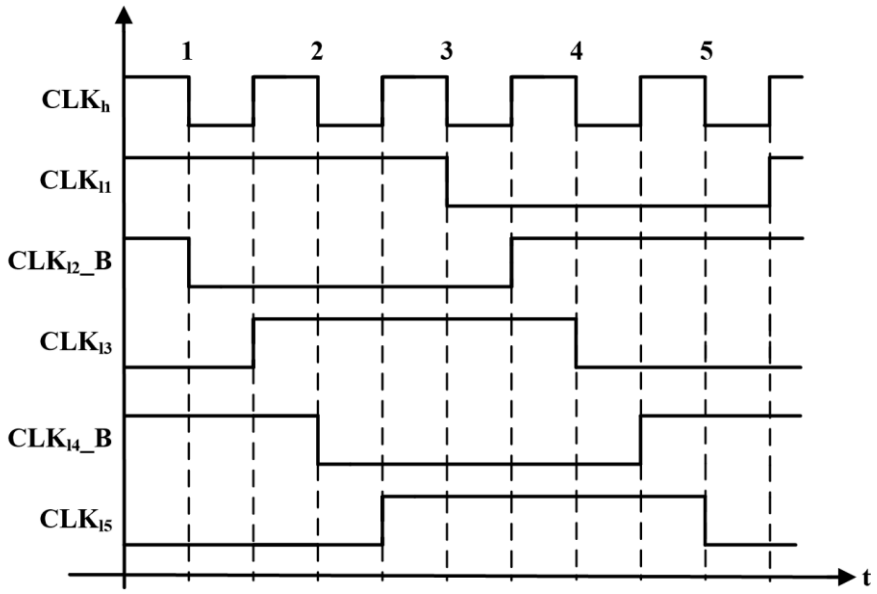
7.3.2. Digital signal generator

The schematic of the injection locking ring oscillator is shown in Figure 7.10 (a). The time domain waveform of each output is shown in Figure 7.10 (b). One of the locking oscillator's outputs is fed into the PRS generator based on LFSR structure. To guarantee the randomness of PRS, the order of the LFSR must be large enough to generate a PRS with a long enough period. I this prototype, a 9^{th} order LFSR to generate a PRS with a period of 511 clock cycles is selected. The polynomial of this LFSR is x^9+x^5+1[63]; the schematic of this block is shown in Figure 7.9.



(a)

Figure 7.10. Injection locking ring oscillator: (a) schematic and (b) 5-stage waveforms.



(b)

Figure 7.10. Continued.

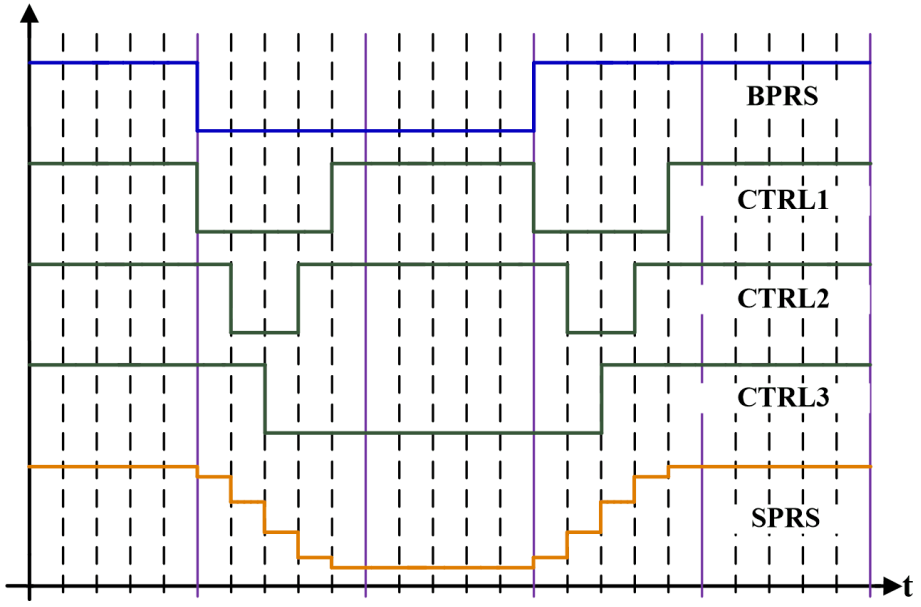


Figure 7.11. Control signals for SPRS generated from 100MHz BPRS.

Five replicas of the BPRS are generated employing the sequential 5-clock phases obtained from the ring oscillator and the control signals shown in Figure 7.11. are generated with them according to the following digital logic,

$$ctrl1(t) = bprs(t) \odot bprs(t - 4T_{clk}) \quad (55)$$

$$ctrl2(t) = bprs(t - T_{clk}) \odot bprs(t - 3T_{clk}) \quad (56)$$

$$ctrl3(t) = bprs(t - 2T_{clk}) \quad (57)$$

Where, $\odot$ stands for the XNOR logic function, T_{clk} is the period of the high frequency master clock. These control signals determine the gain of the PGA. Each time the BPRS signal presents a transition, the gain of the PGA changes in a staircase manner. For the case of a high to low transition in the BPRS, 0.3, then changes the polarity to -0.3, after that changes to -0.8 and finally in the 5th clock period of the master clock finishes at -1. The reverse sequence is generated when a low-high BPRS transition happens. Figure 7.12 shows an example of a 10MHz tone modulated with a 100MHz SPRS.

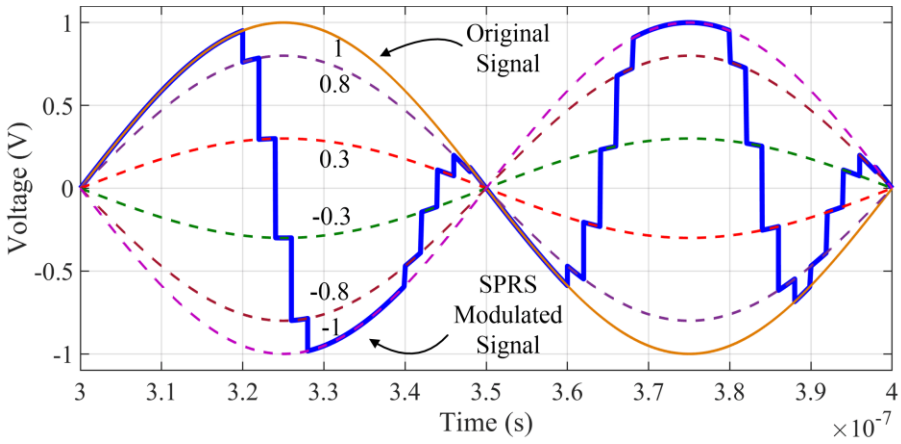


Figure 7.12. Time domain waveform of modulated sine wave. The BPRS clock period is 10ns and the BPRS in the time frame of 300-400ns is {1, 1, -1, -1, 1, 1, -1, -1, 1, -1}.

7.3.3. Analog modulator

The schematic of the analog modulator based on a PGA is shown in Figure 7.13. The voltage gain transitions of the sinusoid-like analog modulator are completed in 5 clock cycles of the master clock as follows.

1) 1st clock period: CTRL1 signal turns on the two 4R branches to change amplifier's gain from 1 to 0.8;
2) 2nd clock period: CTRL2 signal turns on the two 0.5R branches to change amplifier's gain from 0.8 to 0.3;
3) 3rd clock period: CTRL3 signal turns off and CTRL3_B turns on to change input signal polarity, thereby changing amplifier's gain from 0.3 to -0.3;
4) 4th clock period: CTRL2 signal turns off the two 0.5R branches to change amplifier's gain from -0.3 to -0.8;
5) 5th clock period: CTRL1 signal turns off the two 4R branches to change amplifier's gain from -0.8 to -1.

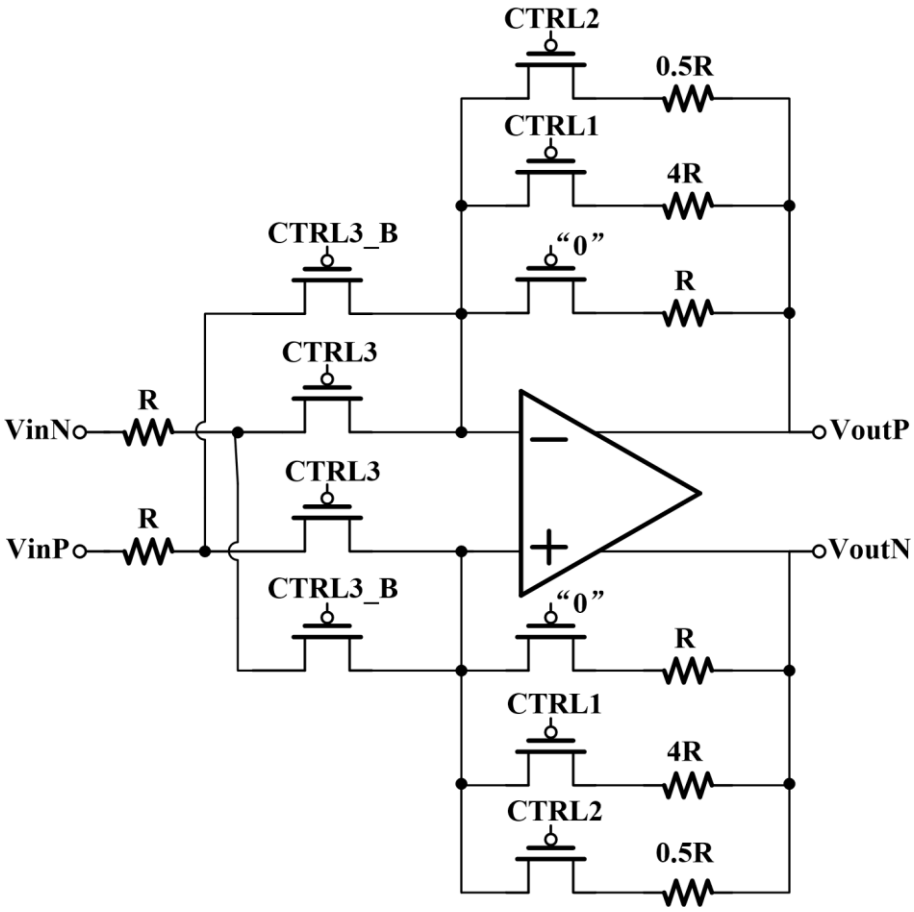


Figure 7.13. Schematic of Sinusoid-like Analog Modulator based on Programmable Gain Amplifier.

The switches in series with the feedback resistors R are used for matching purposes, but they are permanently closed. The switches used in analog modulator are PMOS switches only due to the high common mode level of 850mV, which is close to power supply. Also, due to the continuous-time nature of the modulator charge injection and clock feedthrough are not as important as in the case of charge redistribution based circuitry.

7.3.4. Fully differential OTA

A two stage amplifier is used for the realization of the PGA in sinusoid-like analog modulator. For this design, the BPRS clock period is 10ns, and is generated from a master clock that runs at 500MHz. This means each interpolated step of the five-step 100MHz SPRS has a duration of 2ns. Assuming large DC gain and that the non-dominant poles are placed well beyond the amplifier's unity gain frequency, the step response of the first order system is,

$$V_{out}(t) = -\frac{V_{in}(1-\beta)}{\beta}\left(1 - e^{-\beta \times GBW \times t}\right) \quad (58)$$

Where $\beta=R_{in}/(R_{in}+R_f)$ is the feedback factor, R_{in} is the input resistance and R_f is the overall feedback resistance; $(1-\beta)/\beta$ is the ideal analog modulator's close loop gain which can be programmed for 0.3, 0.8 or 1; and GBW is the amplifier's gain bandwidth product. The most stringent requirement happens when the modulator demands a gain of 1, in which case the β factor is the minimum (=1/2) and the effective gain bandwidth product of the analog modulator β×GBW is minimum.

In order to maintain the settling error within 2% at the end of every master clock cycle, the time constant $1/(\beta \times GBW)$ must be less than $T_{clk}/4$ (=0.5ns). Then a GBW over 320 MHz is necessary; GBW=400MHz is needed for the case of 1% settling time. Therefore, the feedforward stabilization technique is more efficient than the feedback technique with miller compensation, which usually trades stability with GBW. The schematic of this fully differential OTA is shown in Figure 7.14.

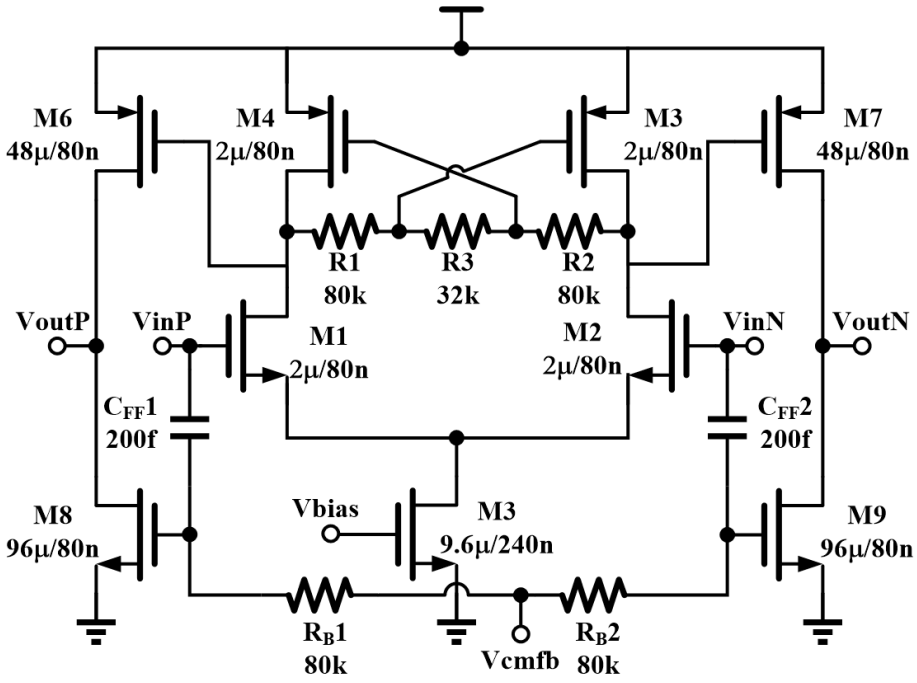


Figure 7.14. Schematic of Feedforward Fully Differential OTA.

In the first stage, the output signal is sensed by the resistive network composed by R1, R2 and R3, and fed back to the gate of M4 and M5. The cross coupling connection increases stage's output impedance. If R3=K·R1=K·R2=K/g, it can be shown that the single branch's first stage output conductance gout yields,

$$g_{out} = \frac{2g}{(K+2)} + g_{o1} + g_{o4} - g_m \frac{K}{K+2} \tag{59}$$

Where g_{o1} and g_{o4} are the output conductance of M1 and M4 respectively, and g_m is the transconductance of M4. The resistors R1, R2 and R3 provide common mode detection to accommodate a local common-mode feedback network and split the resistors allowing us to realize the negative yet linear equivalent resistance that improves DC gain of the first stage.

The second stage is realized employing the P-transistors M6 and M7. M8 and M9 are used to provide a feedforward path that adds a left hand plane zero that helps with the stabilization of the amplifier. The high-frequency gain of the feedforward path provided by $C_{FF}1$, $C_{FF}2$, M8 and M9 is crucial for amplifier's stability. The feedforward capacitors bypass the first stage and creates a phantom zero that compensates the phase margin [66].

7.4. Simulation Results

7.4.1. Performance of analog modulator

The loop stability of the analog modulator was simulated under different feedback settings. AC performance is summarized in Table 1. Amplifier's power consumption is around 2mW.

For the closed loop frequency response of the analog modulator, the 1st pole is located at 1.02GHz; gain and phase error at 100MHz are 53mdB and 9 degrees. The power of 3rd order intermodulation product of the analog modulator was simulated to be -80dBm under unity gain setting with two single-tone in-band interference with equal power of -10dBm. Therefore, the system is able to leave a 40dB dynamic range for the desired signal with power of -40dBm, while tolerating in-band interference power of 30dB higher.

Table 7.1. Analog Modulator AC Performance

Feedback Factor (β)	Specifications	Performance
0.5	Loop Gain	34.64dB
	Gain Bandwidth Product	680.19MHz
	Phase Margin	66.5°
0.56	Loop Gain	35.35dB
	Gain Bandwidth Product	746.98MHz
	Phase Margin	64.4°
0.77	Loop Gain	37.23dB
	Gain Bandwidth Product	1.017GHz
	Phase Margin	66.8°
1	Loop Gain	42.82dB
	Gain Bandwidth Product	1.757GHz
	Phase Margin	85.67°
	Power Consumption	2.02mW

In a real scenario, the in-band interference power received by the LNA could be around -55dBm. Although the main signal power in adjacent channel could be much higher, only the leakage will impact the desired band. For example, 55dBm interferer power in adjacent channel generates 25dBm in-band leakage power for an ACLR of 30dB, and this leakage power is attenuated by more than 80dB after traveling through the air,

then the antenna will be impacted by no more than -55dBm. If the received radar echo signal is as small as -125dBm, system dynamic range should be 70dB or better, requiring the front end IIP3 to be -20dBm (=Pin-IM3/2). However, if the RX antenna is targeted by an intentional interferer, the interference power received by the LNA could be around -25dBm requiring front-end IIP3=25dBm to detect the -125dBm echo signal. Evidently we have to improve system performance to accommodate these specs for this case.

7.4.2. Timing requirement

The impact of timing mismatch between the transmitted PRS and the received PRS can be evaluated by quantifying the autocorrelation function of the SPRS sequences at RX and TX in presence of timing mismatches. In these simulations, we used a 10MHz test tone, modulated at the TX by a 100MHz SPRS; we add a tunable delay cell to emulate the up/down conversion as well as the channel delay. The tunable delay cell is varied in the range of 10ns to 50ns. The received signal is convolved with a replica of the 100MHz SPRS with a fixed 10ns timing delay. The normalized rms value of the recovered 10MHz tone is displayed in Fig.15 as a function of the timing mismatch Δt.

Without timing mismatch, the power of recovered signal $r(t)$ at the RX is about 3dB lower than the original input signal $s(t)$. Even if the timing offset is as large as 50% of the PRS clock cycle, the power of $r(t)$ drops by no more than 6dB compared with the value at zero timing delay, the echo signal is detectable. When the timing error is larger than one clock cycle, the power of the recovered $r(t)$ is very small, making this approach useful for effective timing information extraction.

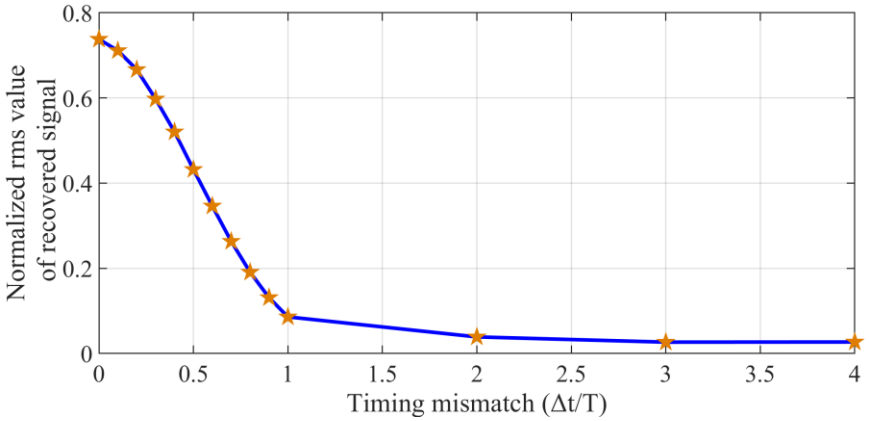


Figure 7.15. RMS values for the normalized recovered signal as function of the timing mismatch between SPRS in TX and SPRS in RX.

7.4.3. Adjacent channel leakage rejection

The advantage of SPRS over BPRS on adjacent channel leakage is demonstrated in this section. A 200mVpk 10MHz sine wave is modulated by both a 100MHz BPRS as well as by the 100MHz SPRS sequence. The spectra of the received signals, after passing it through a channel that attenuates the signals by -27dB, are depicted in Figure 7.16.

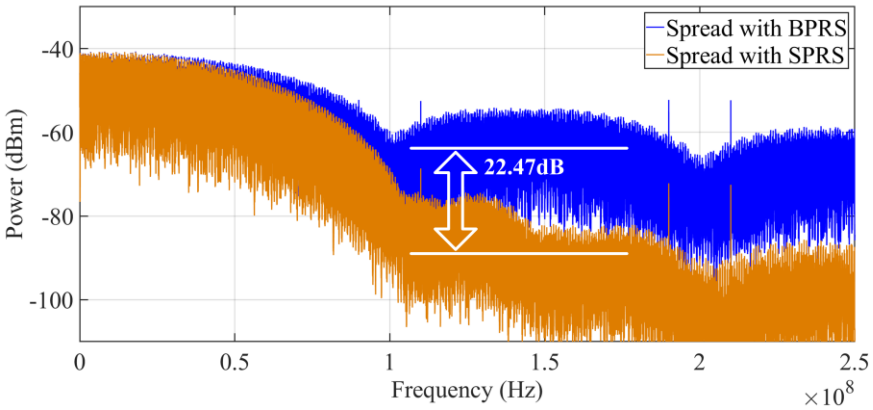


Figure 7.16. Post-layout simulation result: frequency spectra of 10MHz sine wave spread with 100MHz BPRS and with 100MHz SPRS for comparison of adjacent channel leakage.

The difference of signal power (considering 100MHz) bandwidth between two cases is less than 3dB, but out-of-band power of the proposed SPRS technique is well below compared with the case of the conventional BPRS case. The ACLR for the SPRS case is -34.0dB, which meets the -30dB requirement in 802.11b standard without any additional filtering. Relaxed filtering may be required to improve further the ACLR figure for more demanding standards such as 802.11ax.

7.4.4. Single tone signal with single tone interferer

Figure 7.17 (a) shows the test setup of another post-layout simulation; the RF front-ends are not included in this simulation, but a finite bandwidth channel is added. A -37dBm 10MHz tone is used as the transmit signal $s(t)$ at node A; its spectrum is depicted in Figure 7.17 (b). The signal is then modulated by the SPRS sequence and its spectrum after modulation is shown in Figure 7.17 (c). The power of the tone is spread after the modulation with the SPRS sequence. Another 8MHz -37dBm test tone $i(t)$ is injected at the input of the RX to emulate an in-band interferer. Frequency spectra of the received signal after down conversion is shown in Figure 7.17 (d).

After the demodulation with the properly synchronized SPRS in RX, the original test tone at 10MHz is recovered with a loss of 3dB, while the energy of the interferer tone at 8MHz is spread out and randomized, as shown in Fig.17 (e). After passing $r(t)$ through a low pass filter, we are able to improve SNR of RX output by filtering out the out-of-band components.

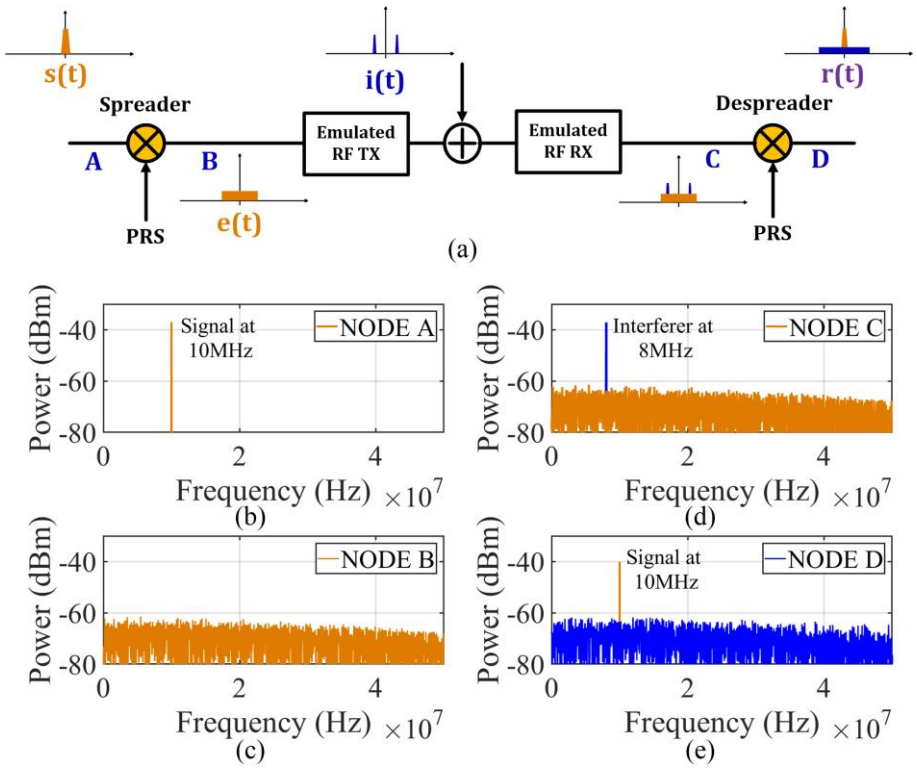


Figure 7.17. Post-layout simulation results for a single test tone signal s(t) with single tone interferer i(t): (a) test setup, (b) input tone, (c) spectrum of input after SPRS modulation, (d) spectrum RX input including the interferer tone and (e) spectrum after

7.4.5. Wideband signal with wideband interferer

Two additional post-layout simulations were performed. In the first case, a -30dBm 1-9MHz FMCW signal is injected at the input of the spreader while a -10dBm uncorrelated in-band 1-9MHz FMCW interference is injected at the input of the de-spreader; time domain waveforms for input signal of the spreader and output signal of the de-spreader before and after 100 sample averaging are compared in Figure 7.18 (a) and (b), respectively. Notice in Figure 7.18 (a) that the timing and frequency information are completely contaminated by the interference. However in Figure 7.18 (b), although the magnitude of the recovered signal presents some variations, the timing and frequency

information are completely recovered. The second case considers a -30dBm 1-9MHz FMCW signal injected at the input of the spreader with a -10dBm 10MHz OFDM interference inserted at the input of the de-spreader; time domain waveforms for input signal of the spreader and output signal before and after 100 sample averaging are compared in Figure 7.18 (c) and (d), respectively.

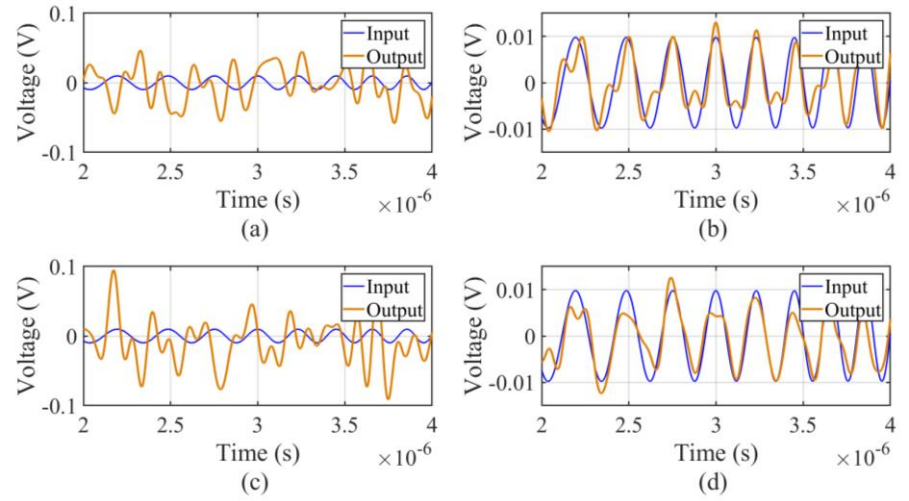


Figure 7.18. Post-layout simulation results for a 1-9MHz FMCW input and a 20dB higher power 1-9MHz FMCW uncorrelated interference. Time domain waveform for spreader's input and de-spreader output (a) before averaging and (b) after averaging. Results for a 1-9MHz FM FMCW input and a 20dB higher power 10MHz OFDM interference: time domain waveform for spreader's input and de-spreader's output (c) before averaging and (d) after averaging.

These two simulations show that the proposed technique is effective in randomizing the interference regardless of the modulation scheme of the interference, the only condition is that the interference must be uncorrelated with the PRS used in the RX.

For the same test setup, we also vary the power of these two types of wideband interferer with respect to the input signal power; displayed in Figure 7.19 is the SNR of

the de-spreader's output as a function of the ratio of interferer power to signal power at de-spreader's input. Because the interference signal is randomized after convolved with SPRS, its power is attenuated employing the averaging technique, therefore an average factor of 10 and 100 leads to the 10dB and 20dB SNR improvement shown in Figure 7.19 respectively. Because the plots for two types of interferer FMCW and OFDM are similar, we only provide the plots for case of FMCW interferer.

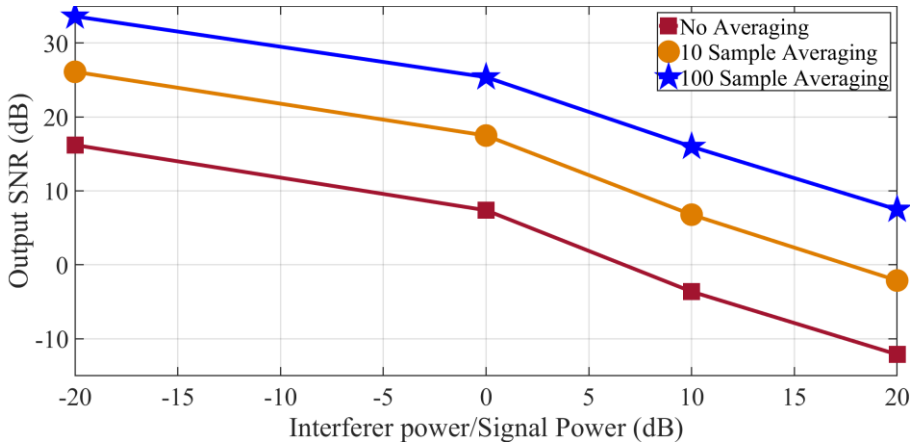


Figure 7.19. Post-layout simulations for an FMCW transmit signal and an uncorrelated FMCW interference: SNR at RX output as a function of ratio of interferer power to received signal power, both measured at RX input.

7.5. Measurement Results

The proposed SPRS system was implemented in a standard 40nm CMOS technology. The baseband circuits including the generation of the BPRS and SPRS sequences were implemented on chip. The RF up/down converters as well as the PA, LNA and PGA were not included. Instead, the channel attenuation and dispersion were emulated by a programmable delay line. The micro photo of the chip is shown in Figure 7.20. The total effective area of the chip is about 0.05 mm^2.

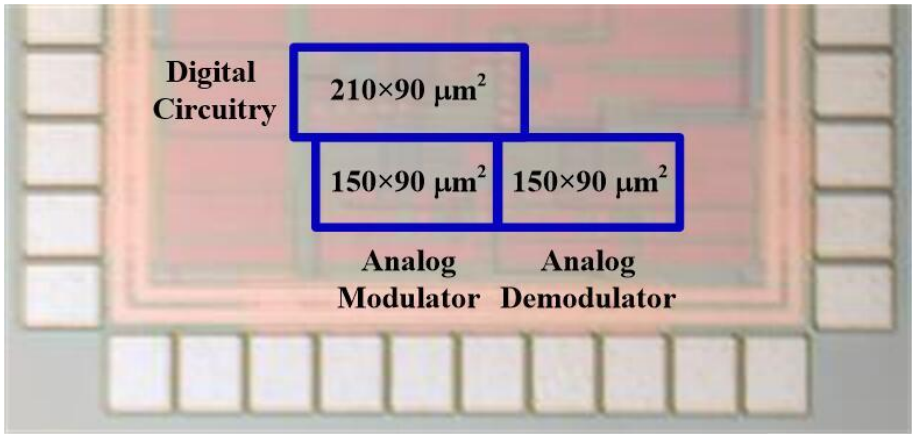


Figure 7.20. Microscopic photo of the chip fabricated with 40nm technology.

7.5.1. Adjacent channel leakage improvement

For the following results, chip data was captured and post-processed in MATLAB. For ACLR characterization, a 200mVpk tone at 10MHz is used. The signal is modulated by a 100MHz SPRS. The signal after the programmable delay line that emulates the transmit channel, is recorded and partly shown in Figure 7.21 and processed to show signal spectrum in Figure 7.22. The SPRS modulation case is compared with the spectral mask of 802.11b standard in Figure 7.22 and confirms the aforementioned properties of the SPRS based modulation scheme. In the case of the sinusoid interpolation, the ACLR is about -35.50dB, 1dB better than simulation result, mainly due to uncertainties on the prediction of the gain of on-chip buffers.

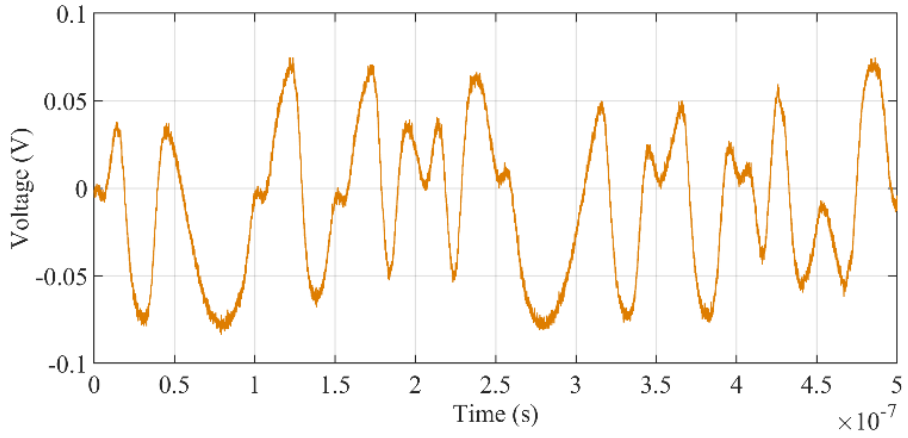


Figure 7.21. Experimental results: time domain waveform for a 10MHz sine wave modulated with a 100MHz SPRS.

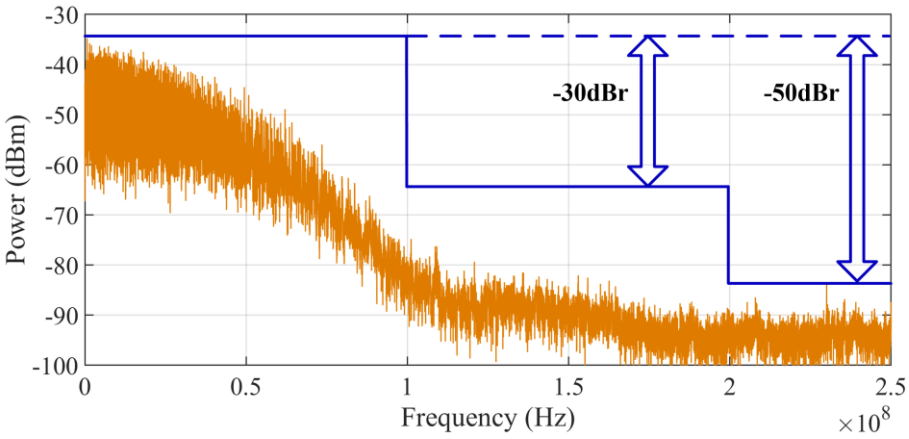


Figure 7.22. Experimental results: frequency spectrum of 10MHz sine wave spread with 100MHz and compliance with 802.11b spectral mask.

7.5.2. Single tone signal with single tone interferer

A 200mVpk test tone at 10MHz is modulated with a 100MHz SPRS, and then goes through an attenuation of 27dB caused by the on-chip and off-chip buffers as well as the programmable delay line implemented with coaxial cables. This attenuation value refers

to the difference between the modulator's output power at TX and the demodulator's input power at RX. This value accounts for PA gain at TX, channel loss (air travel), antenna's gain and gain of LNA, mixers and PGA. For example, if we assume the PA has a gain of 30dB, the channel has a loss of 100dB, the LNA and the mixer together has a gain of 30dB, and the PGA has a gain of 15dB, the attenuation between the output of the modulator in TX and the input of the demodulator in RX could be in the range of 25dB. A second tone at 8MHz is injected at the input of the RX to emulate an interferer. The power of the interferer tone is set at the same power of the echo signal after the buffers and emulated TX channel. The pseudo-random modulators are disabled, and the signal at RX output is shown in Figure 7.23 (a). The two tones at 8MHz (interferer) and 10MHz (desired signal) show the same power level. The SPRS modulations at TX and RX are then activated, and the results are shown in Figure 7.23 (b). The desired signal at 10MHz is recovered, while the power of the interferer at 8MHz is spread over a wider bandwidth (108MHz) and appears as random noise which can be rejected by conventional baseband filtering. The remaining in-band random noise is attenuated by averaging the signal in the digital domain; processing gain of 30dB is commonly achieved employing an averaging factor of 1000, if the interferer is truly random.

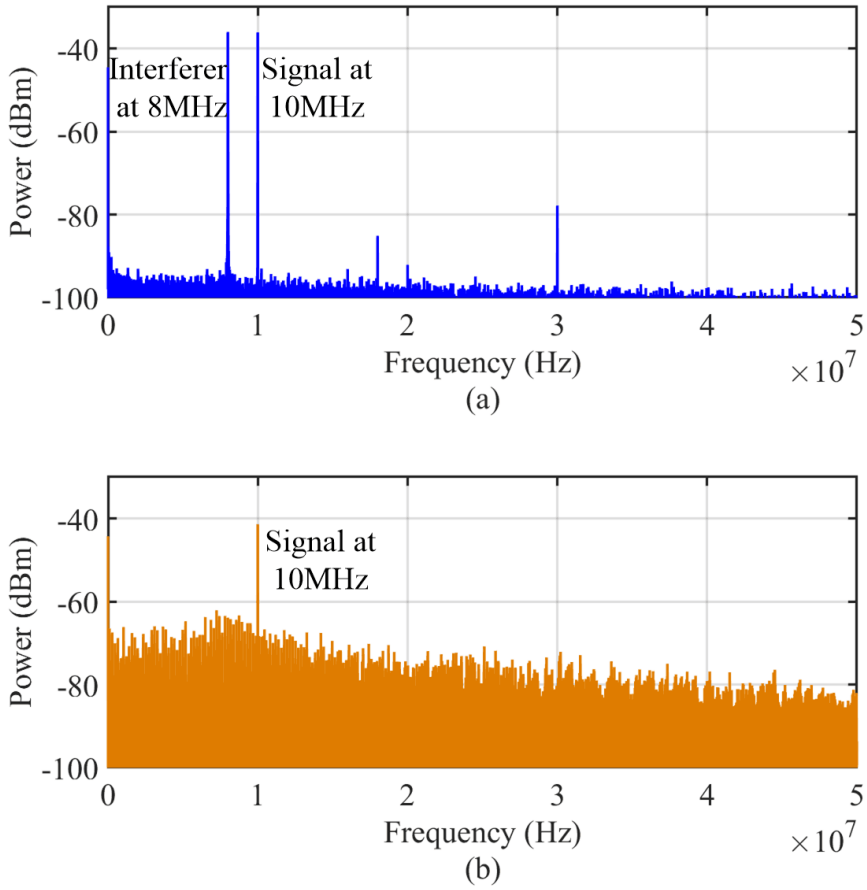


Figure 7.23. Experimental results output r(t) employing an input test tone s(t) and an interferer tone i(t) with (a) the DSSS engine disabled and (b) with the DSSS technique activated.

The proposed architecture is also experimentally tested employing a 5MHz -4dBm test tone modulated by the SPRS. The modulated signal is attenuated by around 27dB and passed through a coaxial cable that introduces around 12ns delay. The received signal is then combined with a second test tone that emulates the interferer; power of the interferer is set at -11dBm with the frequency set at 7MHz. Figure 7.24 shows the spectra of RX output after the PRS demodulation for two cases: interferer power/desired input power

equals to 0 and 100 (20dB), respectively. The desired signal at 5MHz is recovered in both cases, while the power of the interference tone at 7MHz is spread over the PRS bandwidth. The in-band SNR at RX's output improves by 11.8 dB after removing the out-of-band noise by baseband filtering and employing an averaging factor of 4. SNR improves proportional to the averaging factor if the noise is random.

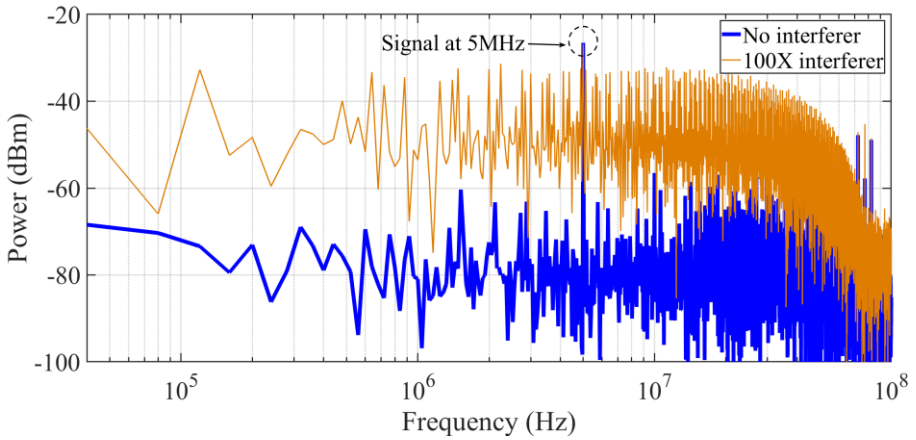


Figure 7.24. Experimental results: frequency spectra of the recovered signal (tone at 5MHz) for the case of no interference (bottom trace) and for the case of 20dB interference to signal power ratio (top trace).

7.5.3. Recovering FMCW waveform

The capability of this system to recover signals with frequency modulation is tested by using a FMCW signal with a frequency span in the range of 1-5MHz. The FMCW signal is modulated and demodulated employing a 100MHz SPRS. Note that the chirp signal goes through 27dB attenuation channel and 3dB loss due to SPRS modulation. The time domain input and recovered signals after a 27dB multiplication are compared in Figure 7.25. Although a bit noisy, it is evident that the chirp signal is recovered. The spectra of the input signal and the recovered signal are shown in Figure 7.26. Part of the

signal power is leaked to high frequency and appears as wideband noise. Interferer signal was not present in these results.

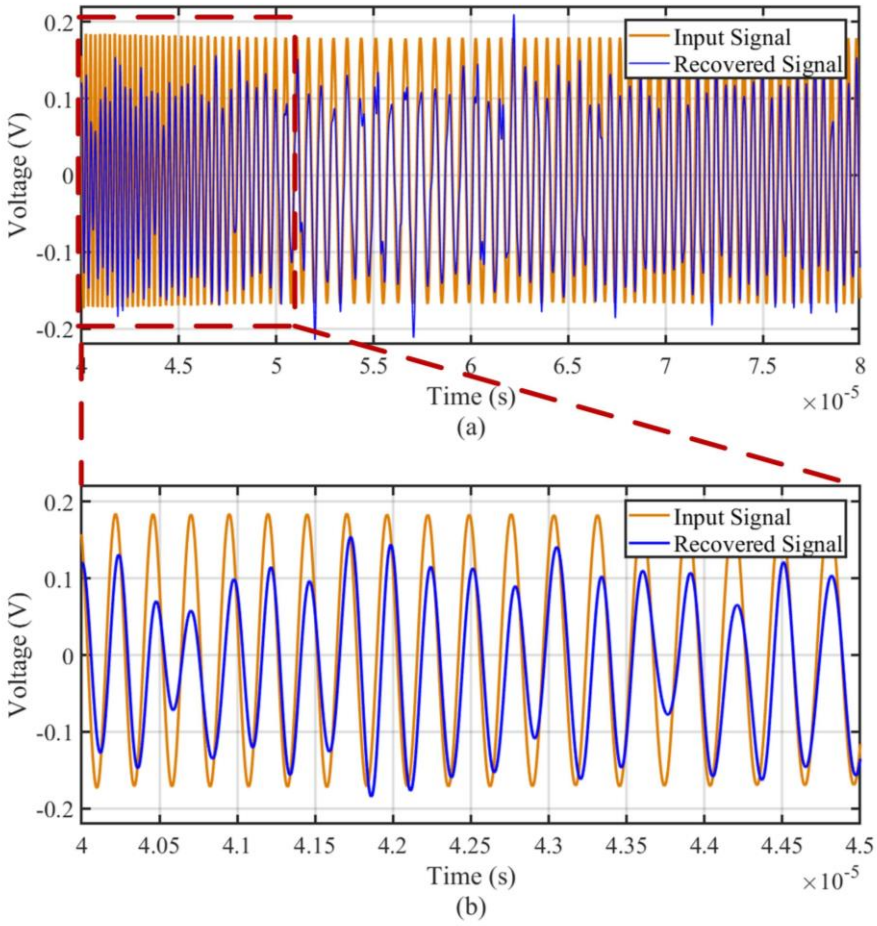


Figure 7.25. Experimental results: time domain waveform of (a) input FMCW signal s(t) and recovered signal r(t) amplified by 27dB, (b) zoom-in in time scale.

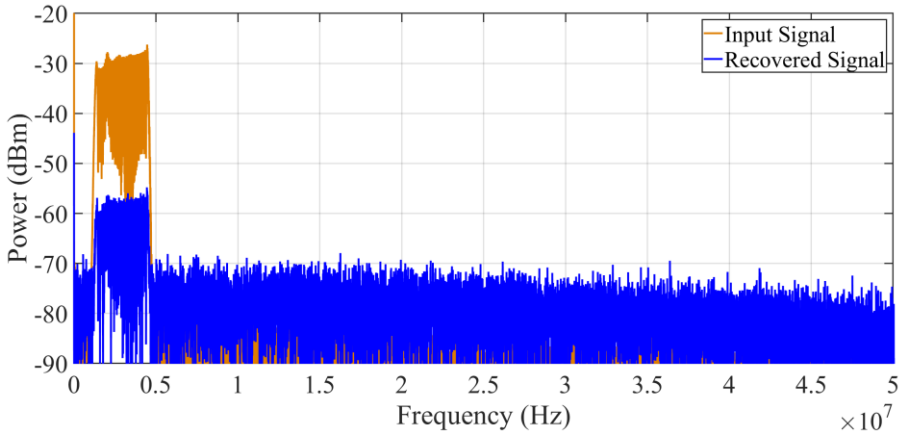


Figure 7.26. Experimental results: frequency spectra of the input FMCW signal s(t) and recovered signal r(t).

7.5.4. Interference tolerance test

To evaluate the transceiver interference tolerance, an FMCW signal with a bandwidth of 0-10MHz is used as the interferer. A test tone at 7MHz is used as the input signal. Figure 7.27 (a) shows the demodulated output signal when the SPRS signals are disabled. The tone at 7MHz and the wideband FMCW interferer centered at 5MHz are both visible in this case. Figure 7.27 (b) shows the spectrum at demodulator output with the SPRS systems enabled. The transmit tone at 7MHz is recovered while the interferer power of the FMCW type interferer is spread over the entire bandwidth due to modulation with the uncorrelated SPRS sequence. By varying the power of the interferer (FMCW), the resulting signal to noise ratio as a function of the ratio of interferer power to received signal power that arises at RX input is shown in Figure 7.28. For very small interferer power, the SNR at RX output approaches the SNR of the proposed scheme (~ 16dB). For large interferer power, the signal to interferer power ratio at RX output is about 6dB better

than that at the input when noise is integrated in a bandwidth of 10MHz. This meets our expectation of limited improvement without averaging.

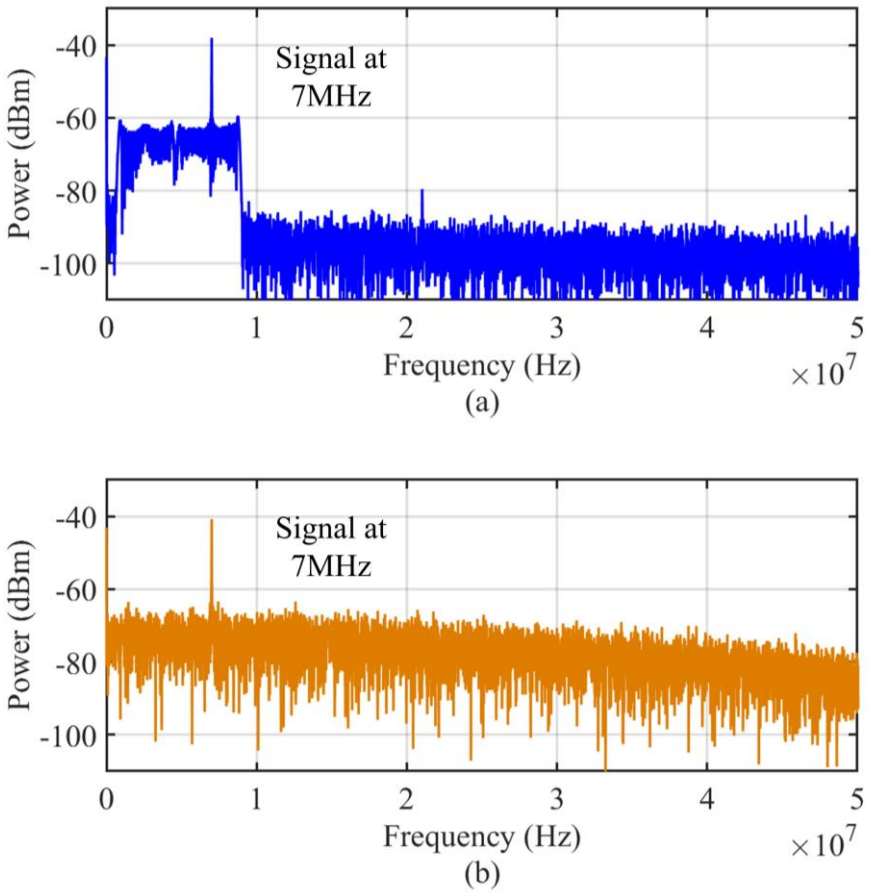


Figure 7.27. Experimental results employing an input test tone s(t) and an FMCW interferer i(t) with (a) the DSSS technique disabled and (b) with DSSS technique activated.

A major advantage of the demodulation with SPRS in RX is that the interference power is randomized, which can be attenuated by averaging the output signal. Fig.28 compares the output SNR after an average factor of 4; as expected, the SNR improves by 6dB. However, without randomization, this benefit is not achievable under the periodic FMCW interferer condition. In this measurement, the clock frequency of the PRS

generator is 80MHz. According to calculation of ideal model, after demodulation in RX, about 75% of the received signal power is recovered, 1.7% of the signal power appears as random noise in the 10MHz signal band, and 24% of the interference power falls into the signal band. The curve shown in Figure 7.28 follows the following equation,

$$SNR = 10\,log_{10}\left(\frac{0.75}{0.017+0.24N}\right) \tag{60}$$

Where, N= P_{int} / P_{sig}, P_{sig} is the received signal power without SPRS modulation and demodulation, P_{int} is the received interference power. If the interferer is randomized by the PRS in the RX, and then averaged by a factor X, therefore,

$$SNR_{AVG} = 10\,log_{10}\left(\frac{0.75}{0.017+0.24N}\right) + 10\,log_{10}\,X \tag{61}$$

The SNR can be even better if the noise is integrated in smaller bandwidth or the average factor X is increased.

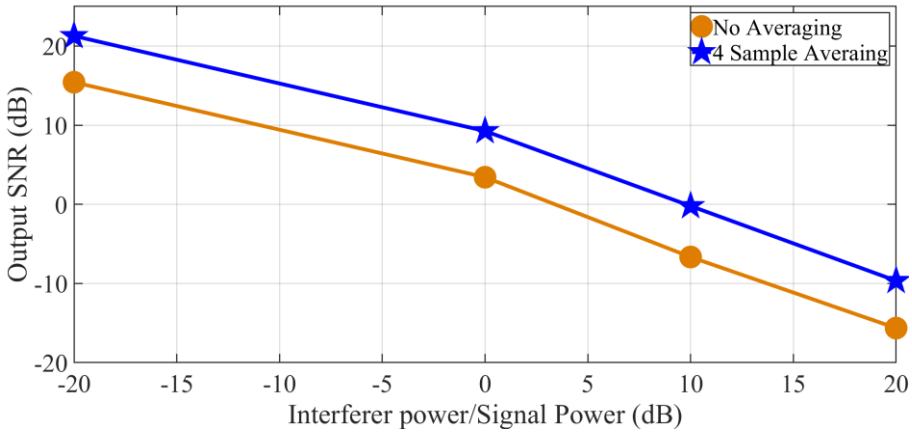


Figure 7.28. Experimental results: Output SNR as a function of ratio of interferer power to received signal power at RX input.

7.5.5. Comparison with other state-of-art

Previously CMOS transceiver designs with in-band interference rejection were reported in [55-58]. [55] combines the N path RF filter technique with code domain modulation, and reports a 38.5dB TX self-interference rejection. This rejection is based on a spectrum spreading ratio of 19.7dB and more importantly it is achieved based on the orthogonality of coding information in TX and RX. This means this rejection is not achievable on an arbitrary in-band interference. [56] combines the code domain modulation with LNA and PA design, and reports an 18.8dB in-band interference rejection ratio with a frequency spreading ratio of 20dB, which means with a frequency spreading factor of 10dB, the in-band interference rejection ratio cannot be higher than 10dB. Authors in [57] implement the code domain modulation and filtering before LNA. The achieved 49.5dB TX self-interference rejection also relies on the orthogonality of the coding information in TX and RX. Even more, that design relies on the baluns for impedance matching and single-ended to fully-differential conversion, therefore inevitably introduces insertion losses and noise before LNA. [58] introduces two extra code modulators and a band reject filter structure in addition to the regular code modulator before LNA to achieve rejection to in-band interference with specific coding. The 52dB rejection ratio is only achieved on interference with one specific code. Unfortunately, the implementation of band reject filter inevitably degrades the quality of the signal, which makes this technique not attractive for high quality communication applications such as QAM256 or better. All these designs do not consider the adjacent channel leakage issue due to modulation with BPRS in TX, which means that to comply with spectral mask of

commercial communication standards like the series 802.11, they have to consume a larger bandwidth than the main lobe of the modulated signal, therefore will degrade the spectral efficiency.

In the proposed system, 11.8dB in-band interference rejection ratio is achieved for a spreading ratio of 10 and an averaging factor of 4, and the total power consumption is 4.33mW and requires 0.0459μm2 silicon area. Clearly this solution is more efficient than BPRS modulation schemes at RF frequency. Additional processing gain techniques improves drastically the SNR for radar applications.

Table 7.2. Comparison with other solutions for Adjacent Channel Leakage Reduction

	JSSC 2014 [59]	JSSC 2019 [65]	This work
Architecture	Mutiphase PRS	Binary phase OOK	Sinusoid-like PRS
Technology (nm)	28	65	40
Supply (V)	0.9	1	1.2
Power (mW)	BB: 1 Modulator: 3	4.2*	2.31**
Area (mm^2)	0.04	0.01*	0.0324**
1st Sidelobe Power (dBr)	-23	-20	-40
ACLR (dB)	20	20	≥35

* Only digital blocks and low pass filter for Binary phase coding are accounted.

** Includes on modulator and the digital blocks for SPRS generation.

A comparison with other reported solutions for adjacent channel leakage issue is given in Table II. This work is more effective than [59] and [65] for sidelobe rejection.

[65] and this work are both spectral efficient for different modulation schemes. Power consumption of the scheme in TX is only 2.31mW, offering an ACLR over 35dB.

7.6. Conclusion

In this paper, we introduce a modulator/demodulator system based on direct sequence spread spectrum to improve rejection to in-band interference from adjacent frequency bands and self-leakage, systematic or random. With the proposed mixed signal IC technique, systematic interference become pseudo-random and can be attenuated by averaging techniques. Theoretical explanations of this technique are provided to substantiate this concept and to show the limitation on adjacent channel leakage of Binary PRS. Sinusoid-like PRS is introduced to alleviate this limitation. Main analog and digital building blocks are explained in detail to show the feasibility of the proposed system. Post-layout simulation results and measurement results show an ACLR improvement of about 22dB, and the capability of attenuating systematic or random high-power interference.

8. AN INTERFERENCE-TOLERANT SYNCHRONIZATION SCHEME FOR WIRELESS COMMUNICATION SYSTEMS BASED ON DIRECT SEQUENCE SPREAD SPECTRUM

8.1. Introduction

Wide frequency bands are the basis of developing new wireless communication services that require high data rates and low latency. Lack of available licensed bands has become one of the biggest obstacles for governments and companies in this field. However, the actual spectrum occupancy measurements obtained by FCC and other worldwide research resources [5,67,68] indicate that, at any given time and location, a large portion of the prized spectrum lies idle. This implies that the prevalent static spectrum allocation is the fundamental reason for scarcity of available frequency bands. Dynamic spectrum access used in cognitive radios (CR) is more flexible in the use of frequency spectrum resources, therefore, improves spectral efficiency.

The operation of cognitive radio system consists of two phases: spectrum sensing and spectrum sharing. During the spectrum sharing phase, cognitive radio users select available frequency bands and adapt transmission parameters based on the collected spectrum information [69]. In terms of spectrum sharing paradigms, cognitive radio systems can be divided into three categories, underlay overlay and interweave [6]. Multiple researches [70-74] on hybrid paradigm composed of underlay and interweave have been reported capable of relaxing the demanding requirement on ADCs enforced by output power restriction [75] in underlay paradigm [76-81] and the fast frequency hopping requirement of frequency synthesizer in interweave paradigm [25-27,82-84]. In this hybrid

paradigm, CR users are able to co-exist with primary users when the in-band interference level is tolerable and switch to other bands only when the interference level is excessive. In this paper, a hybrid mode CR system of underlay and interweave paradigms is considered, in which the operation of spectrum sharing is achieved with direct sequence spread spectrum (DSSS) technique.

In the DSSS technique based systems, the spectral coexistence is achieved by making use of code domain information. To realize this functionality, most importantly, synchronization of codes in the CR receiver (RX) and CR transmitter (TX) must be guaranteed. Among the code domain transceivers operating at radio frequency [55-58] only few of them [57] have claimed the capability of synchronization but in absence of in-band interferences. The interference tolerance of the synchronization process is of great importance, since the time to wait for a completely vacant frequency band directly adds up to the latency of data transmission. The synchronization scheme proposed in this paper embedded in the hybrid mode CR system is verified to be able to tolerate an in-band interference power of 5dB higher than the signal power.

The rest of this paper is organized as follows. Section II explains the need for synchronization scheme in DSSS system, and explains the proposed three-level synchronization scheme. Section III introduces the system architecture and circuit implementations of the main analog and digital building blocks. Section IV presents some important post-layout simulation results to prove the feasibility and benefits of this technique. Section V demonstrates the interference tolerance of the proposed

synchronization scheme through experimental results. The conclusions are provided in Section VI.

8.2. Synchronization in DSSS system

In the cognitive radio system based on direct sequence spread spectrum (DSSS), CR users have the capability of attenuating in-band interferences from other CR users. Since in-band interferences cannot be attenuated by conventional filtering, DSSS system makes use of code domain information to differentiate desired signal from in-band interferences.

8.2.1. DSSS system with built-in synchronization

In the DSSS technique based system shown in Figure 8.1, the baseband signal S(t) is first modulated in analog domain by a wideband pseudo random sequence (PRS) to spread the signal bandwidth. The modulated signal is then up-converted to radio frequency band, amplified by a PA and transmitted by an antenna. In the RX the modulated signal $Srf(t-t_0)$ is received, altogether with in-band interferences Irf(t) including the TX leakage power. All these components are amplified by an LNA and down-converted to baseband. These baseband signals are then convolved with another wideband PRS signal at baseband, by which the signal $S(t-t_0)$ can be recovered, while all other uncorrelated components are spread into a larger bandwidth. As a result, the system is able to differentiate the desired signal $S(t-t_0)$ from other in-band interferences. One important thing to emphasize, the synchronization of the two PRS signals is necessary condition to guarantee the proper functionality of this type of system.

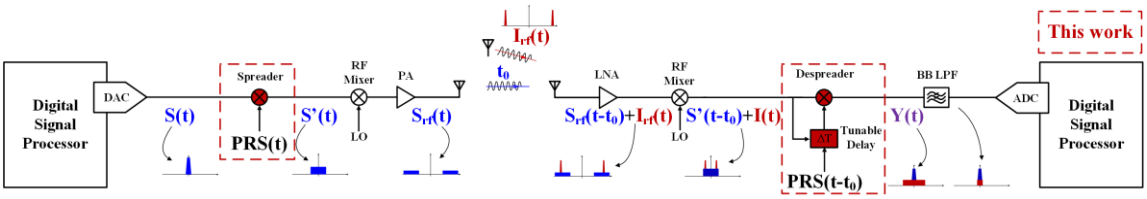


Figure 8.1. Block diagram of CR transceiver based on DSSS technique.

8.2.2. Necessity of precise synchronization

The in-band interference reduction property of the DSSS system is due to the modulation with PRS signal in RX that results in the frequency spreading of uncorrelated interferences [85]; the interference reduction ratio is defined as the ratio of the in-band power of the interference convolved with a PRS to the original interference power:

$$Interference_{reduction} = \frac{\int_{-BW}^{BW} |I(f) * PRS(f)|^2 df}{\int_{-BW}^{BW} |I(f)|^2 df} \tag{62}$$

Where I(f) and PRS(f) are the frequency spectra of the unwanted in-band components and PRS, respectively; BW is the bandwidth of the desired signal.

On the other hand, the desired signal S(t) can only be recovered if the PRS in RX and the PRS embedded in the received signal are synchronized. Ignoring the effects of the up and down conversion as well as the filters, the desired signal is recovered through the following operation,

$$Y(t) = A \cdot S(t) \times PRS(t) \times PRS(t - \Delta t) \tag{63}$$

Where A is the overall linear gain between TX and RX; Δt is the timing offset of the PRS at RX with respect to the PRS embedded in the received signal. According to [85], the recovered signal power is negligible if Δt is larger than one PRS's clock cycle T. A reliable synchronization requires to maintain the timing offset $\Delta t < 0.2T$.

Figure 8.2 shows MATLAB result for quantifying the in-band SNR of recovered 10MHz signal after convolving with a couple of 100MHz PRS signals in the presence of 1st order 100MHz bandwidth limitation at TX output. 5dB loss in SNR results if the timing offset among the two PRS signal is 20% of the PRS clock cycle; loss in SNR is as high as 15dB if the timing offset is around 0.5T.

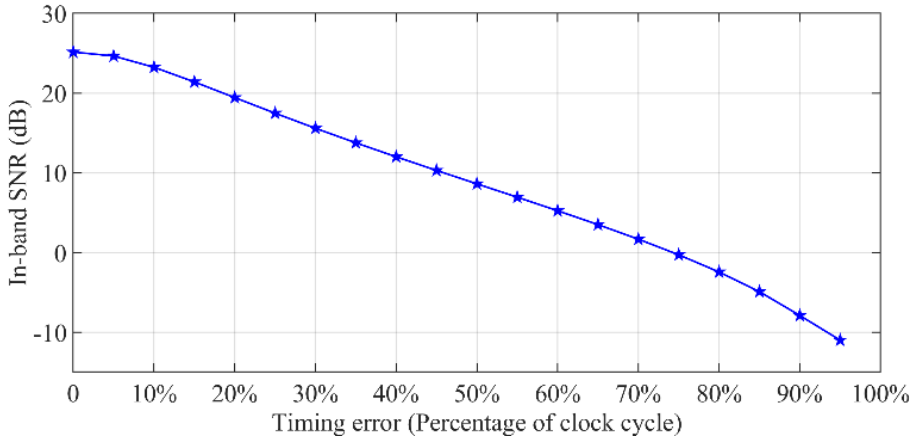


Figure 8.2. In-band SNR of recovered signal as a function of the timing error Δt.

8.2.3. Synchronization scheme

Multiple works in the field of digital communication have shown that the so-called code acquisition process can be achieved employing two strategies: serial search and parallel search [39]. In serial search strategies [40,41], the PRS sequences are compared bit by bit employing either an active correlator based on multiplier and integrator/envelop detector or a passive correlator based on digital matched filter. In parallel search strategies [42], multiple PRS sequences with different timing are compared employing a bank of correlators. In addition, authors in [87] report a hybrid strategy involving a two-level coarse code acquisition scheme, in which the first level is achieved serially with passive correlator and the second level is achieved parallelly with a bank of active correlators.

Although parallel search is proved to be more time efficient than serial search, it is more expensive in terms of hardware and may not be suitable for low power applications. Serial search, as demonstrated in [39], is more hardware efficient but this approach it is not tolerant to large in-band interferences. To reduce the code acquisition time and achieve high interference tolerance during synchronization, we propose an agile three-level synchronization scheme that is composed of coarse acquisition, intermediate acquisition and fine tuning.

8.2.4. Synchronization Algorithm

For serial search strategy, the timing of the PRS functions can be adjusted according to the DC component of the correlation function between the received PRS and the reference PRS in RX. However, due to the high timing selectivity of the autocorrelation function of PRS functions, this approach is sensitive only when the timing error is within ±T. The auto-correlation function cannot be used as an error function when timing error is beyond ±T. The narrow sensitivity region of the auto-correlation function and the long period of PRS (time to repeat the sequence) demand long time for exhausted serial search to finally align the code information of the two PRS signals. A quick search strategy that reduces the timing error between the PRS sequences within ±T is proposed here; the synchronization scheme is shown in Figure 8.3. The TX employs two PRS generators of the same structure to modulate two dc signals thereby generate two PRS of different bandwidth but with correlated phase information during synchronization process. The RX makes use of the slower PRS as a reference for estimating the phase of the faster PRS. The scheme operates as follows.

1. A narrowband PRS is transmitted together with the wideband PRS in a frequency division fashion; the RX side noise, interferences and the wideband PRS can efficiently be filtered by a sharp low pass filter in the RX. The narrowband PRS is then recovered by a comparator and passed through a signature sequence indicator. This part of the circuit is highlighted in red in Figure 8.3. Since the narrowband PRS generator has a structure same as the wideband PRS generator and the clock signal used in these two PRS generators are correlated in phase, the phase of the narrowband PRS is guaranteed always correlated with that of the wideband PRS. As a result, the coming of the signature sequence in the narrowband PRS can be used as an indication that the correct starting point of the wideband PRS is close.

2. Secondly, after the indicator shows the coming of the narrowband signature sequence, the wideband PRS in RX is then activated to modulate with the received wideband PRS, since it is guaranteed that the correct staring point is very close. The timing of the wideband programmable PRS in RX is tuned in steps of clock cycles according to the DC component of the output signal, which is proportional to the correlation level between the two wideband PRS signals. At the end of this synchronization level, the algorithm eventually captures the timing that generates the maximum DC power, which indicates the timing error is within ±T.

3. Finally, according to an LMS algorithm the timing of the reference PRS is fine-tuned to align with the received PRS by selecting from options provided by a

programmable delay cell composed of a series of digital registers and a multiplexer.

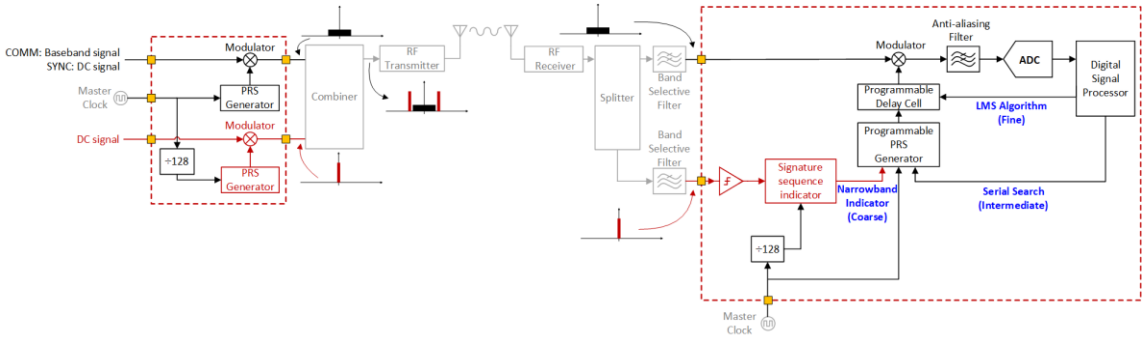


Figure 8.3. Block diagram of three-level synchronization scheme.

The flow chart of the algorithm embedded in RX for synchronization is shown as follows.

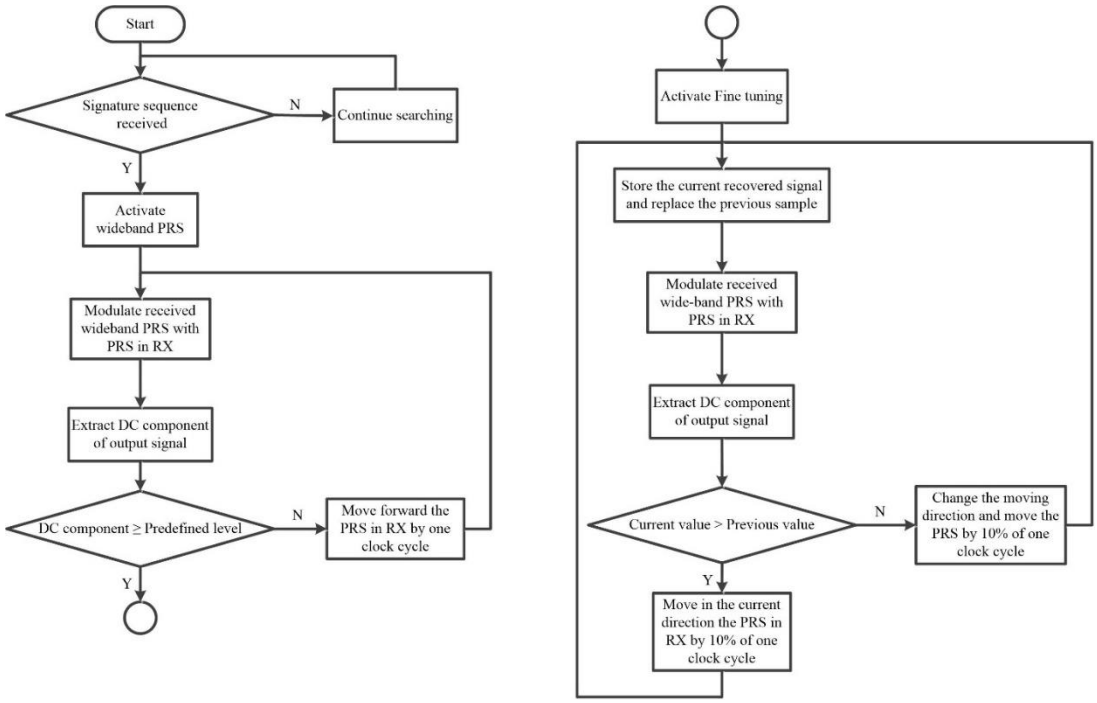


Figure 8.4. Flow chart of three-level synchronization scheme.

8.3. Physical Implementation

To verify the feasibility of the synchronization scheme, a prototype was designed; the system architecture is shown in Figure 8.5. The TX part on the left is composed of two similar PRS generators based on 9th order LFSR structures and two analog modulators. The PRS generator in red runs 128 times slower and is used for the estimation of the starting point of intermediate tuning as mentioned before. The MAG input signal is a dc signal used to control the power of the narrowband PRS during the synchronization phase. The faster PRS generator in black is used for modulating a dc signal during synchronization and modulating desired signal during data communication. The two PRS signals are combined in frequency domain and contaminated with an interference off-chip and separated from each other before injected into the RX.

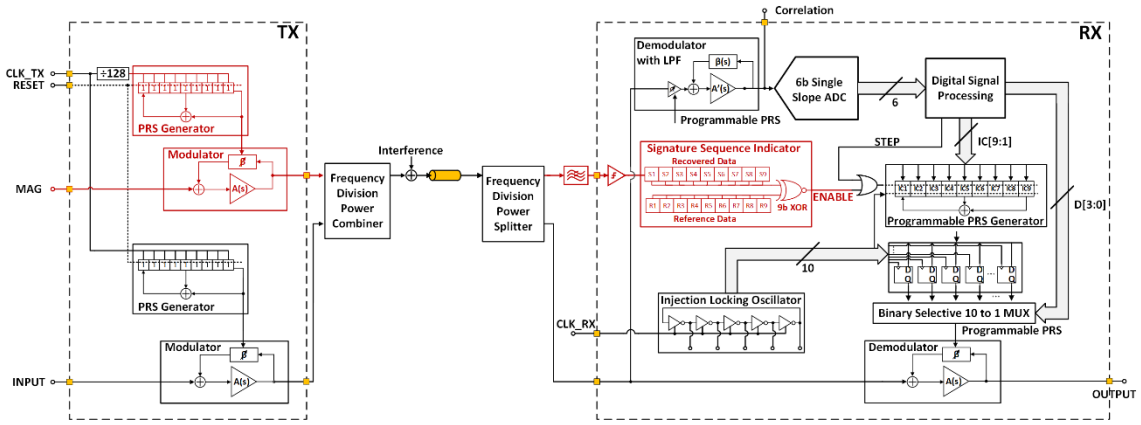


Figure 8.5. System architecture of IC prototype.

The RX requires three input signals: the narrowband RX input, the wideband RX input and the RX master clock. During the first level synchronization, a signature sequence in the narrowband PRS is detected by a simple comparator after cleaned by a low pass

filter off-chip, and gives an enable signal that indicates the completion of first level synchronization. This enable signal activates the programmable PRS generator and the demodulator on the upper part when the reference in the RX is close to synchronization. This demodulator has an embedded low pass filter and extracts the correlation information between the received PRS and the reference PRS. After that, A 6b single slope ADC converts this information into digital and a digital signal processor processes this digital information and gives out the command to change the timing of the reference PRS in clock cycles to search for the timing that maximizes the correlation level, which indicates the completion of second level synchronization. The RX master clock is fed into an on-chip injection locking oscillator [85] to generate 10 copies of lower frequency clocks that are 10% apart from each other, which will help generate 10 replicas of reference PRS to select with a fast multiplexer. During the third level synchronization, an LMS algorithm is activated to search among the 10 replicas to maximize the correlation level, and eventually restricts the timing error within 15% of the clock cycle.

8.3.1. Working principle

During the synchronization process, the 100MHz master clock is frequency divided by 128 with a digital synchronous counter to get a 781.25KHz low frequency clock signal. This low frequency signal is injected into a low frequency PRS generator to generate a PRS with a bit duration of 1.28μs. This narrowband PRS is used to control one of the analog modulators, thereby generate a fully differential 781.25KHz PRS. At the same time, the 100MHz master clock is also directly injected into a high frequency PRS

generator with the same structure to generate a PRS with a bit duration of 10ns. This wideband PRS controls another analog modulator thereby generate a fully differential 100MHz PRS with desired power. The wideband PRS and the narrowband PRS are correlated in phase and both affected by in-band interferences. The narrowband signal is filtered by a low pass filter in the TX to limit its bandwidth.

The 781.25KHz PRS is recovered in the RX through a zero crossing detector. This signature sequence indicator then compares every 9 consecutive bits of the recovered data with a signature sequence bit by bit to indicate when the signature sequence is detected and the first level of synchronization is achieved. This indicator signal initiates the wideband PRS generator, with a priori defined initial conditions that correlates with the phase of incoming narrowband PRS. Since the received narrowband PRS and the wideband PRS are correlated in phase, the first level synchronization reduces the timing error to several clock cycles. During the second level synchronization, the received 100MHz PRS is convolved with the programmable 100MHz reference PRS to extract the correlation level information that increases with reducing timing error. The recovered correlation information is then converted into digital format through a 6b 4MHz single slope ADC. The result is averaged 16 times in the digital domain to further attenuate the impact of the interference and all other random noise components. After the correlation level is maximized with serial search strategy, the third level synchronization employing a conventional LMS algorithm and finer tuning steps is activated to maximize this correlation level.

8.3.2. Analog PRS modulator/demodulator

Three analog modulator/demodulators based on a PGA were implemented: the first modulator in TX for fully differential narrowband PRS generation, the second one for spreading with wideband PRS; the third one demodulator in RX for frequency despreading. The schematic of this modulator/demodulator is shown in Figure 8.6. In this modulator/demodulator, the gain of this PGA changed between 1 and -1 according to the control signal $CTRL = \overline{PRS}$. When the PMOS switches in red are turned on the PGA provides a gain of +1. The two dummy switches in the feedback path are always on, and added for matching purposes.

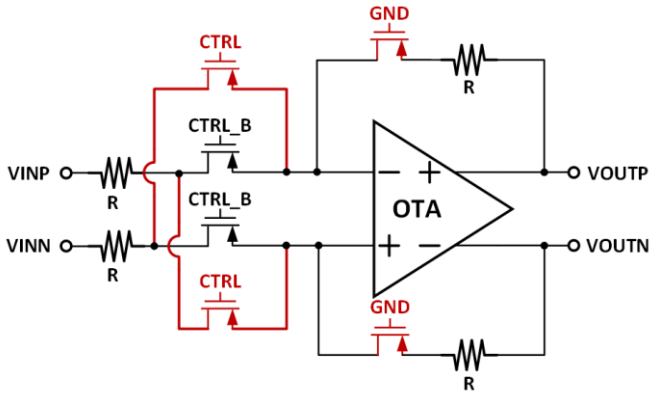


Figure 8.6. Schematic of analog PRS modulator/demodulator.

8.3.3. Demodulator with low pass filtering capability

The demodulator in the feedback loop is only used for computing the correlation function between the received PRS and reference PRS. The relevant information is the dc power that is proportional to the level of correlation between the two PRS signals. The demodulator shown in Figure 8.7 is merged with a 5^{th} order low pass filter design. The five poles of this 5^{th} order low pass filter are real. Although this filter may not provide a

sharp attenuation outside the passband, it is easy to implement with single OTA and is still effective. With $\omega_0 = 2\pi \times 2.1MHz$, this filter is able to achieve a 99% settling within 1μs and an attenuation of 55dB at the frequency of 10MHz.

If implemented at the input of the OTA, the switches are subject to a smaller V_{GS} variation, thereby, they will not generate large nonlinearity effects due to input signal dependent switch resistance. However, this is not possible with this demodulator, the demodulation must be done before, to compress the bandwidth of the desired information, after which the filter reduces the remaining high-frequency signals. The nonlinear switch resistance is not a major issue here because the series resistance R is much larger than that of the switch resistance.

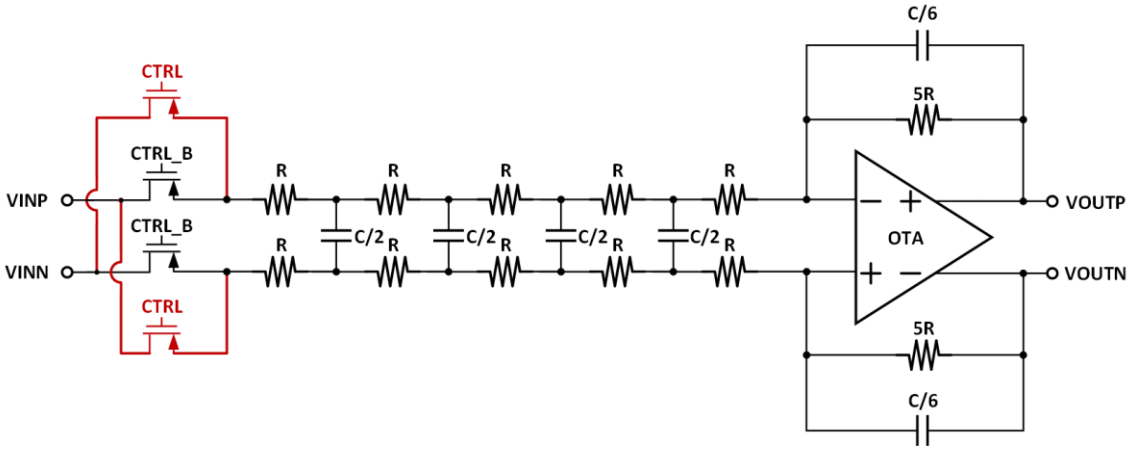


Figure 8.7. Schematic of demodulator with low pass filtering capability.

8.3.4. 6b single slope ADC

Even though the demodulated signal is filtered, the in-band random noise makes it hard to identify the dc content of the demodulated signal. To further reduce these unwanted in-band frequency components, this signal is averaged in time domain. This operation is

realized in the digital domain. The cheap 6b single slope ADC shown in the Figure 8.8 is implemented because of its power and area efficiency. The output of the demodulator is sampled at a rate of 250MS/s. The fully differential ramp signal is generated by injecting two opposite currents into a resettable fully differential analog integrator. The two 5 bit counters then count the number of master clock cycles needed by the ramp signal to exceed the demodulator output. These two counters, however, are counting at different clock edges, thereby the equivalent maximum number of clock cycles counted during each conversion is doubled from 32 to 64. Then the effective resolution doubles for the same clock frequency.

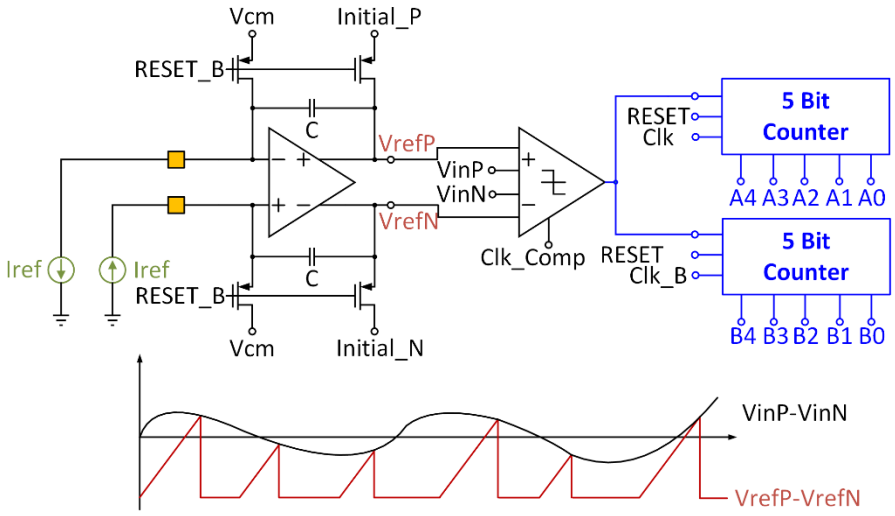


Figure 8.8. Schematic of 6b single slope ADC.

8.3.5. Digital signal processor

The 6b correlation level between the reference PRS and the received PRS is fed into the digital signal processor shown in Figure 8.9, which is mainly composed of three parts. A 16 taps digital adder is used to compute the average of the input signal; this operation smooths the value of the autocorrelation function. While the average signal is below a threshold, an intermediate tuning step signal is sent to a digital memory that stores three set of optional initial conditions F[9:1] R[9:1] and B[9:1] and selects the needed initial conditions IC[9:1] to be sent to the programmable PRS in Figure 8.10. Together with IC[9:1] as shown in Figure 8.5, a step signal is also sent to the programmable PRS generator to reset. By resetting the initial conditions of the programmable PRS to different values, the timing of the reference PRS can be changed back and forth with tuning steps of one clock cycle until the average signal is higher than the threshold. While the average signal surpasses the threshold, the current value is stored in memory and used for comparison with the next state. The comparison result is used as a control signal to change the direction of a 4b up/down counter, which sends out a 4b command D[3:0] to select the timing of the reference PRS provided by the tunable delay line.

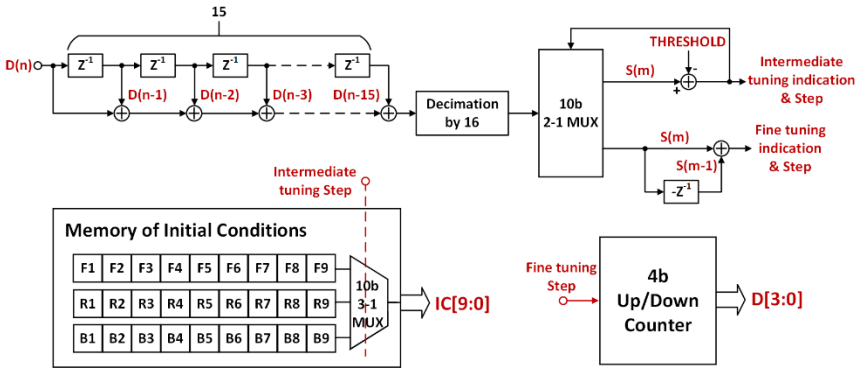


Figure 8.9. Schematic of programmable PRS generator for intermediate tuning.

8.3.6. Tunable delay line

In order to achieve the tuning in the timing of reference PRS, a tunable delay line is necessary. However, the length of the 9th order PRS sequence has as many as 511 bits. As a result, to achieve an exhausted serial search of the correct timing, at least 511 delay cells will be needed even without considering the timing error within one clock cycle. Clearly, it is not efficient to physically implement this entire delay loop. To alleviate this issue, instead of delaying the reference PRS with actual digital delay cells, we modify the initial conditions of the PRS generator after each period of the PRS and achieve the intermediate tuning of the PRS by intentionally setting the initial condition IC[9:1] either one bit ahead to F[9:1] or one bit behind to B[9:1]. The schematic of this PRS generator with programmable initial conditions is shown in Figure 8.10.

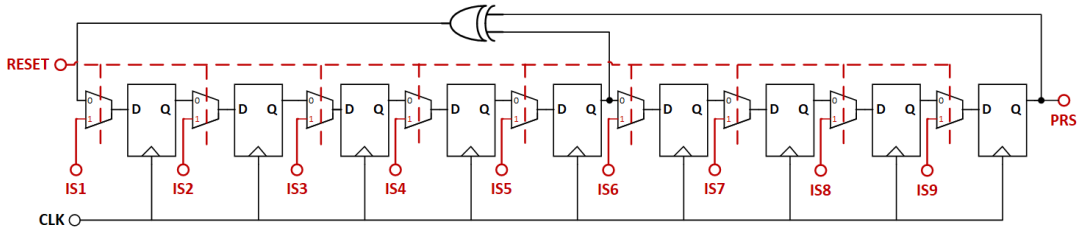


Figure 8.10. Schematic of programmable PRS generator for intermediate tuning.

Different from regular PRS generator, this programmable PRS generator has the 2 to 1 muxes between the D flipflops to provide the flexibility to reset the PRS generator to IC[9:1] received from the digital signal processor, thereby to change the timing by clock cycles.

Once the timing error is within a clock cycle, the fine tuning phase employing the tunable delay line in Figure 8.11 starts. During this third level of synchronization, the

clock phases generated by the 5-tap injection locking oscillator are employed. Considering the complementary pairs, 10 replicas of the master clock are generated. These 10 replicas of clock signal with different phases drive the flip-flops to generate 10 replicas of the PRS with a time offset of T/10. A 10:1 multiplexer selects one of them in rotation according to the control signal D[3:0], which is generated by the fine tuning branch in Fig. 8, while the correlation function is monitored. Once the maximum value is achieved, the clock phase is set, therefore, the timing error at steady state can be reduced to ±15% of the clock cycle. Note that the error can be further reduced by increasing the number of taps of the injection locking oscillator.

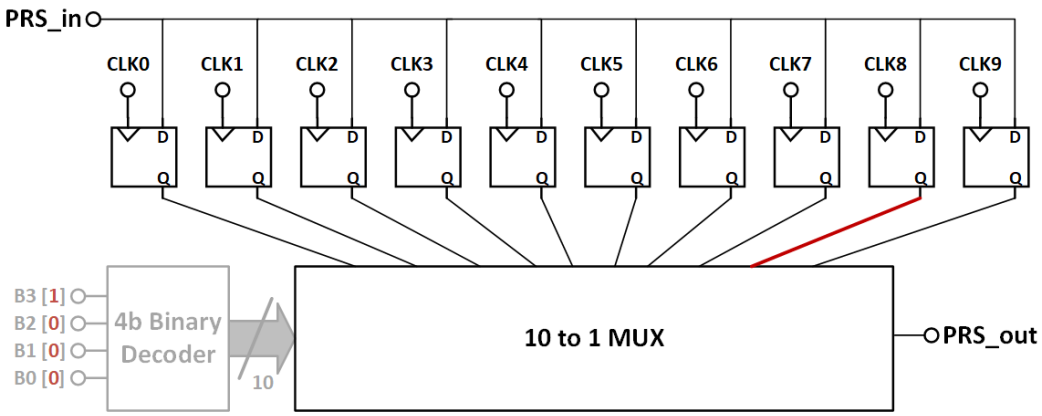


Figure 8.11. Schematic of tunable delay line for fine tuning.

8.4. Simulation Results

In this section, several post-layout simulation results show the feasibility of the proposed approach.

8.4.1. PRS modulation with analog modulator/demodulator

The analog PRS modulators in Figure 8.6 is utilized to modulate dc signals during the synchronization process. If the modulator has a sufficient phase margin and follows the settling behavior of a 1st order system with a gain bandwidth product of GBW, the step response of modulator's output S'(t) is,

$$S'(t) = 1 - 2e^{-2\pi \times GBW \times t} u(t) \tag{64}$$

If we consider the band limiting filter at TX output is also a first order system with a bandwidth of BW, the transitions in the transmitted signal T(t) will follow the step response of a second order system with two real poles at f=GBW and f=BW,

$$T(t) = 1 - 2\left(\frac{GBW}{GBW-BW} e^{-2\pi \times BW \times t} - \frac{BW}{GBW-BW} e^{-2\pi \times GBW \times t}\right) u(t) \tag{65}$$

If GBW=5BW, in the case a 100MHz PRS has a limited bandwidth of 100MHz, the loss in the dc component of the recovered signal due to this finite GBW when fully synchronized is less than 1%. For this design, the GBW of the amplifier used in the PRS modulator is simulated over 500MHz under all conditions of different process corners and temperatures.

8.4.2. Performance of the 5th order low pass filter

According to the simulation results summarized in Table 8.1, the 700KHz low pass filter embedded in the de-spreader shown in Figure 8.7 is able to provide enough attenuation at 10MHz, and is able to settle with a tolerable timing error before the output is sampled by ADC's first stage. Post-layout ac and transient simulation results of this low pass filter in Table I confirm that although the process variations result in large settling time tolerances, the filter is able to provide at least 49dB attenuation at 10MHz and a settling error of less than 5% in 1μs.

Table 8.1. Performance of 5th low pass filter

Temperature (℃)	Process corners	Attenuation at 10MHz (dB)	Settling error (%)
27	tt	58	2.0
27	ss	65	4.9
27	ff	49	0.4
27	sf	58	1.8
27	fs	58	2.1
80	tt	58	2.0
80	ss	65	4.9
80	ff	49	0.4
80	sf	58	1.9
80	fs	58	2.1

8.4.3. Performance of the 6b single slope ADC

The SNDR of this ADC is found to be 35dB, which translates to an effective number of bits (ENOB) of 5.5b. ADC's resolution limitation results in a detection error in the correlation level of less than 3%, which is sufficient for this application, considering the fact that this random error is further reduced by averaging in digital domain.

8.4.4. Programmable PRS generator

A fix and a programmable PRS generators are simulated to test the functionality of the programmable one. At the beginning of this simulation, the two sequences present an intentional timing offset of two clock cycles. As shown in Figure 8.12, the transitions in the two sequences become aligned at 10.22µs, which indicates the completion of intermediate tuning.

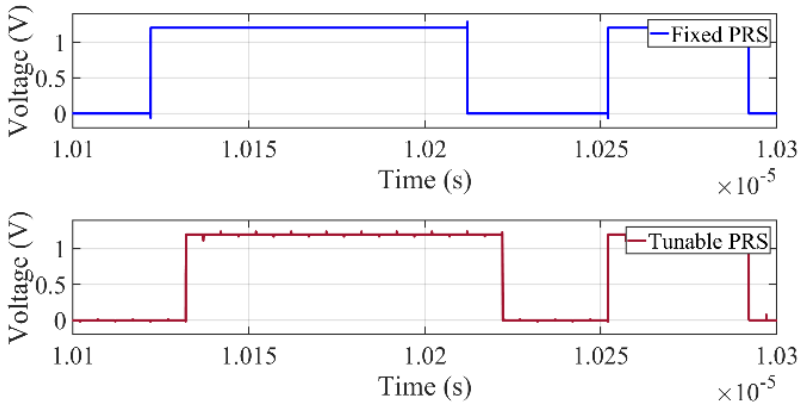


Figure 8.12. Functionality of programmable PRS generator.

8.4.5. Synchronization scheme based on correlation level

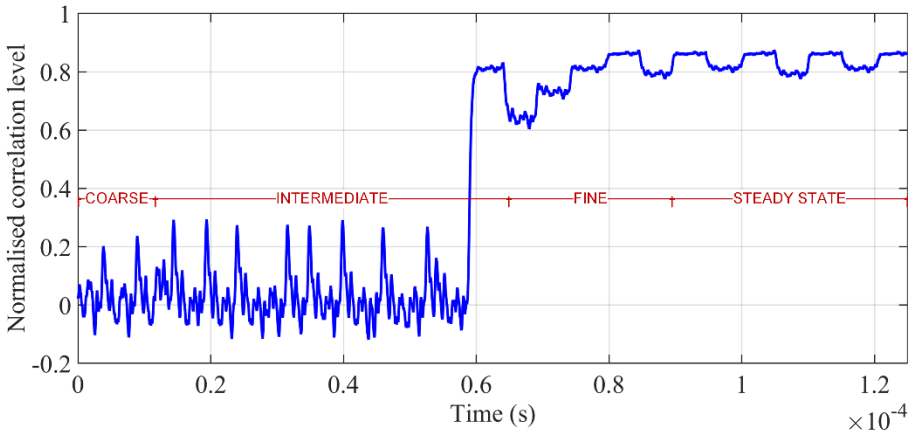
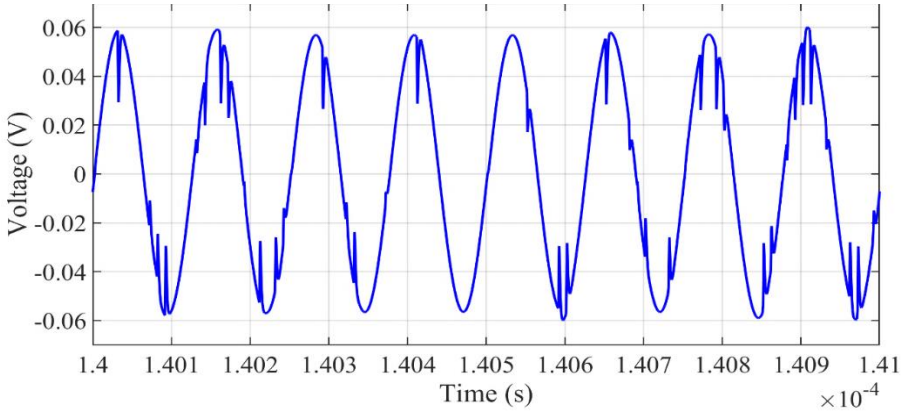


Figure 8.13. Correlation level during synchronization process.

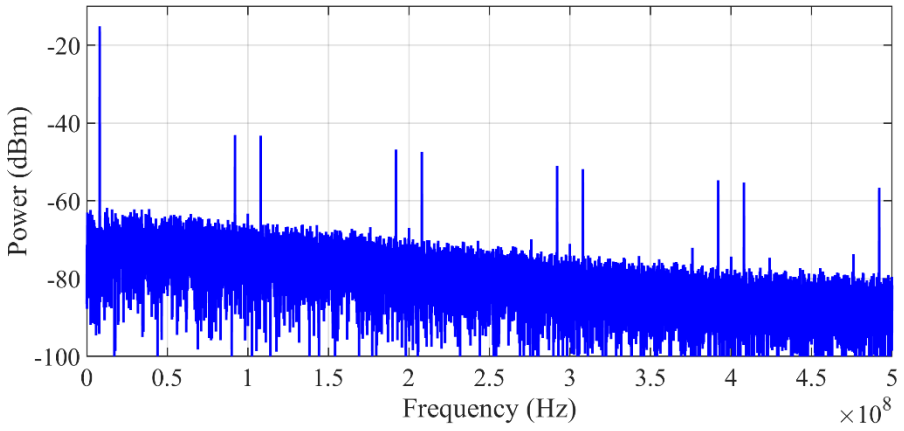
During this simulation, the TX transmits a narrowband PRS and a wideband PRS together, the received wideband PRS signal is then convolved with the reference PRS in the RX. The demodulator output which stands for the normalized correlation level between the received PRS and the reference PRS across the entire synchronization process is displayed in Figure 8.13. During the first level of synchronization, with the help of the narrowband PRS, the timing offset of the two PRS is reduced but not enough to reach a reliable correlation level. The second level takes a few extra PRS periods to synchronize the reference PRS to the received PRS within one clock cycle, when the correlation level exceeds 50%. The fine tuning further reduces the timing error during the third level, until the correlation level surpasses 80% and is changing up and down. At steady state, the correlation level shown ensures that the timing offset is kept smaller than 15% of one clock cycle.

8.4.6. Quality of the recovered signal at steady state

After the synchronization is achieved the baseband signal is transmitted. As a test example, an 8MHz tone is used as the TX input. The transient waveform of the recovered signal at RX output after the PRS demodulation is shown in Figure 8.14(a), and the frequency spectrum of this recovered signal is shown in Figure 8.14(b).



(a)



(b)

Figure 8.14. (a) Time domain waveform and (b) frequency spectrum of the recovered signal after synchronization.

As shown in Figure 8.14(b), the 8MHz sinusoidal waveform is recovered with some harmonics due to the PRS modulation and demodulation operation in the TX and RX. It is clear that these spurious components do not degrade the in-band signal quality and can be easily removed with low pass filtering. The in-band SNR measured in a signal bandwidth of 10MHz is around 34dB.

8.5. Experimental Results

As a proof of concept, an IC prototype shown in Figure 8.15 is fabricated with the process of 40nm technology. The area of TX part and RX part on this chip are measured as 0.015mm2 and 0.072mm2 respectively. The total power consumption of the chip during the synchronization process is measured to be 18.7mW.

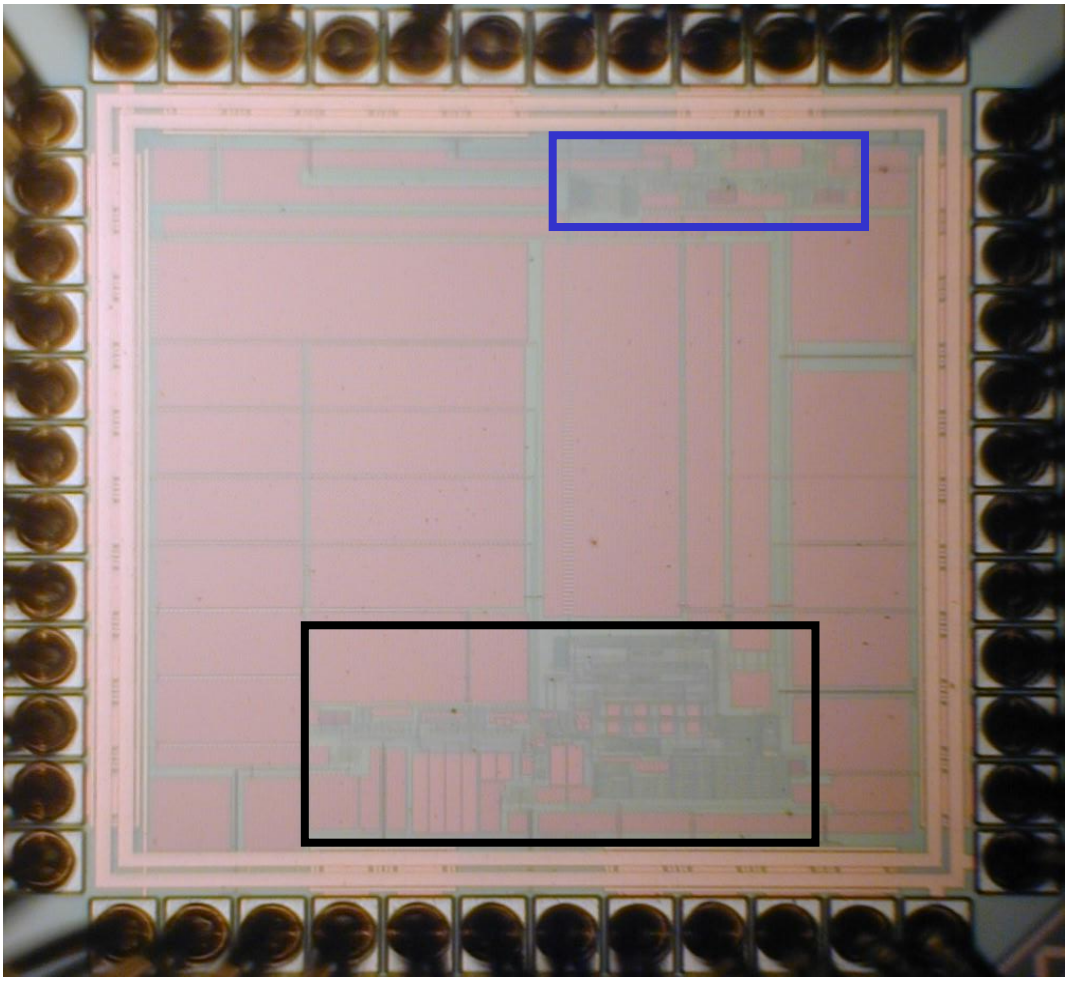


Figure 8.15. Microscopic photo of IC prototype.

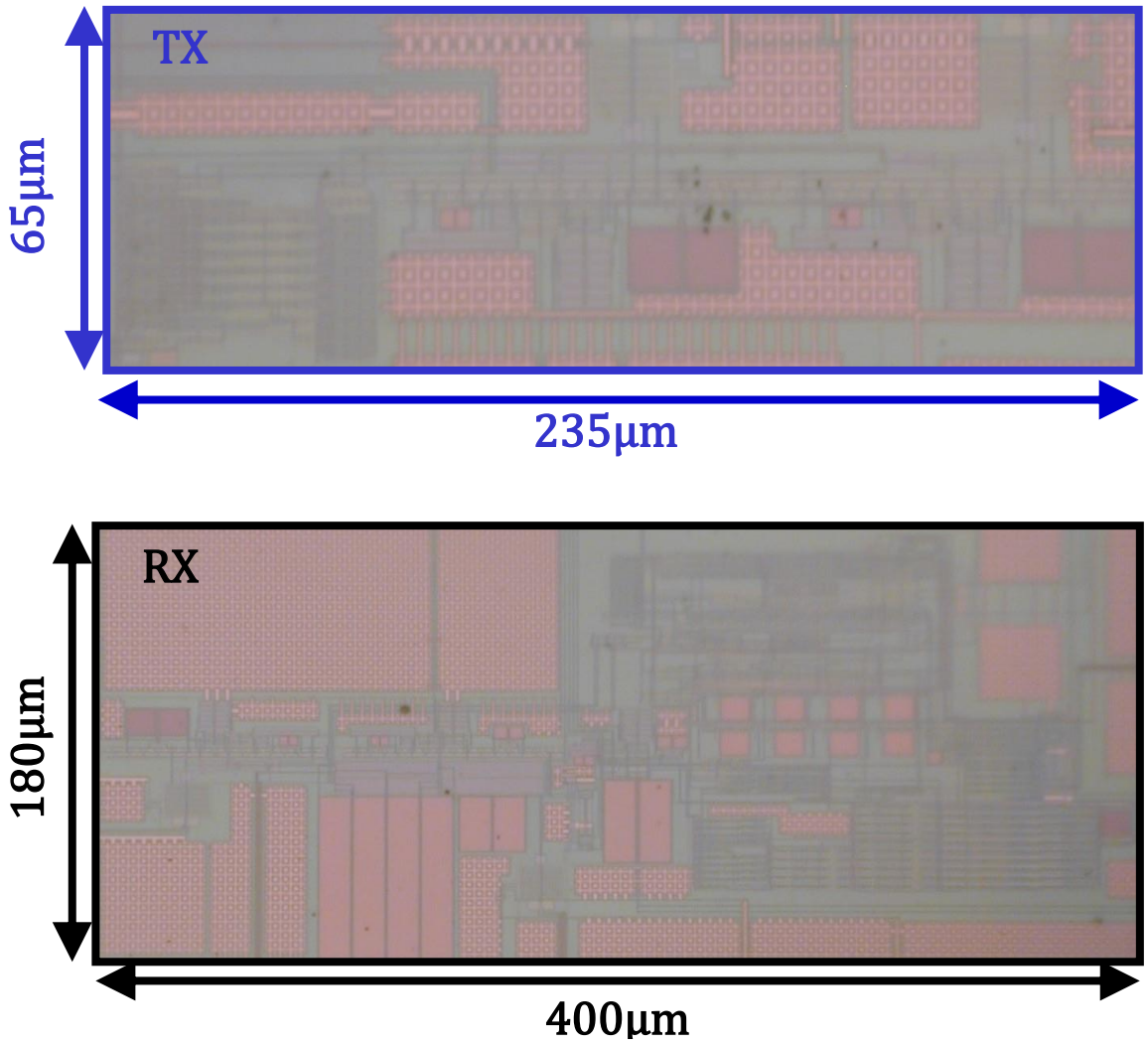


Figure 8.15. Continued.

The experimental results shown in the following sections are obtained with the test setup shown in Figure 8.16. In this test setup, the desired baseband signal is injected into the TX part of the chip and processed on-chip. Then a wideband signal and a narrowband signal are transmitted off-chip and delayed by two coaxial cables of the same length and combined with the same in-band interferences to mimic the transmission through two independent channels. In the narrowband channel, this combined signal is filtered with a

low pass filter before injected into the RX part of the chip, while in the wideband channel, the signal is directly injected back on-chip. The recovered wideband signal at the RX output is then recorded with a broadband oscilloscope and processed in MATLAB.

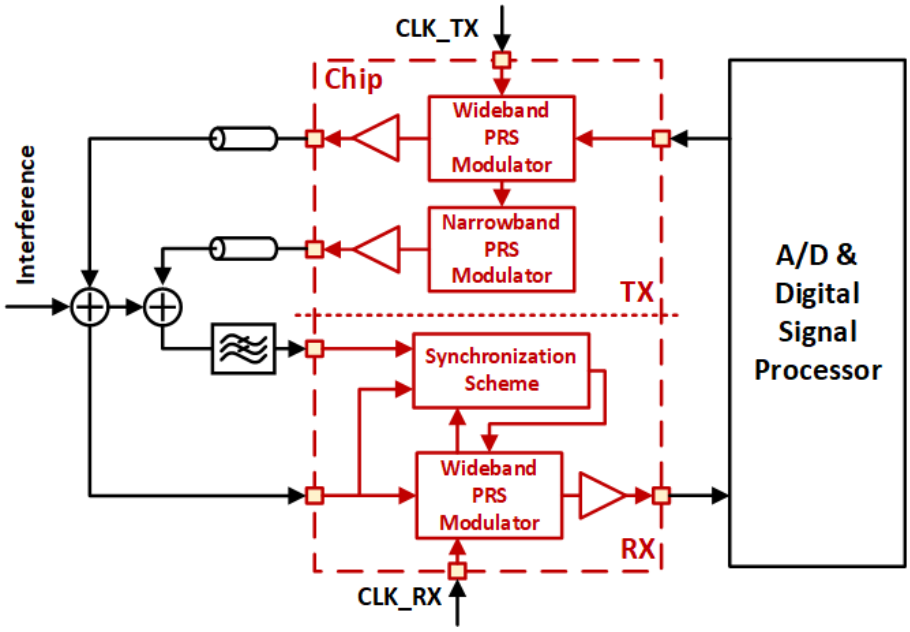


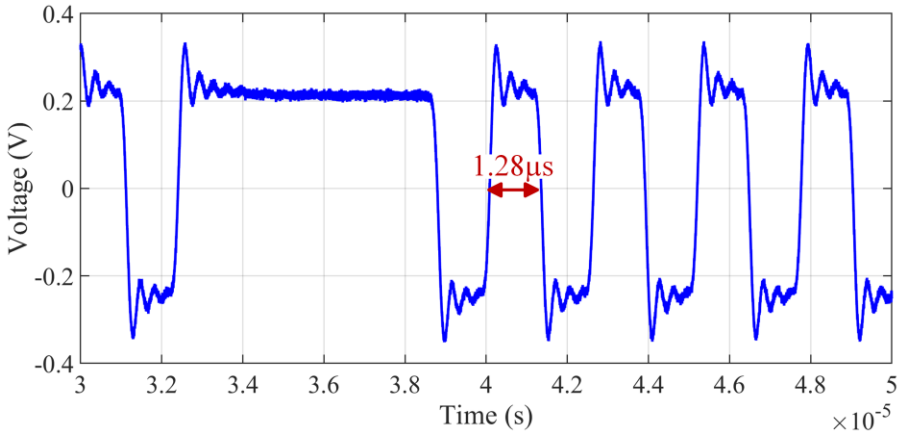
Figure 8.16. Test setup for the experiments.

8.5.1. Wideband PRS and narrowband PRS at TX output during synchronization

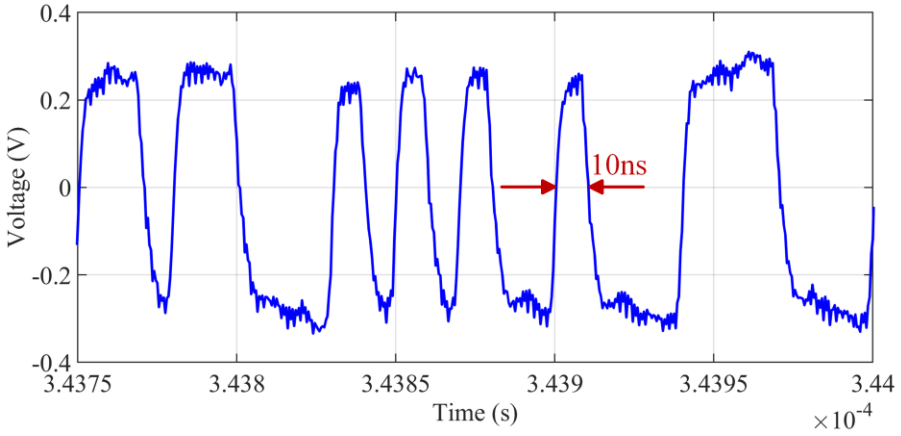
Here in this measurement, we show the wideband PRS and narrowband PRS at TX outputs during the synchronization process. In this measurement, a 100MHz clock and a DC signal that controls the power of the output signal are injected into the TX part. The time domain waveform at the wideband output and narrowband output are recorded and shown in Figure 8.17.

As we can see from Figure 8.17, the wideband PRS has a minimum bit duration of 10ns due to the clock frequency of 100MHz. The narrowband PRS has a minimum bit

duration of 1.28us, this is because on-chip frequency divider reduces the clock frequency by 128 times.



(a)



(b)

Figure 8.17. Transient waveform of TX narrowband (a) and wideband outputs (b) during synchronization.

8.5.2. Wideband output after synchronization

In this measurement, we show in Figure 8.18 the transient frequency spectrum of a 2MHz sinusoid signal modulated with a 100MHz wideband PRS at TX output.

As is shown in Figure 8.18, the frequency spectrum shows that the single tone signal is spread into a bandwidth of 100MHz as expected.

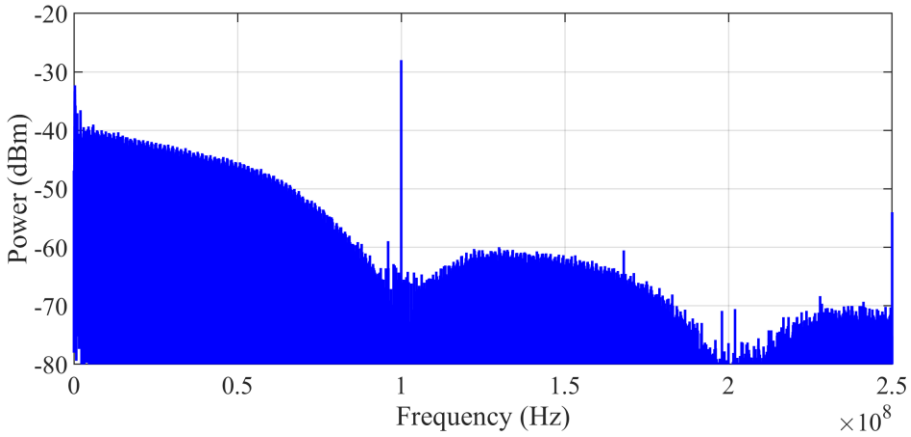


Figure 8.18. TX wideband outputs corresponding to 10MHz sinusoid input.

8.5.3. RX output after synchronization

In this measurement, we went through the three-level synchronization process. After synchronization we used a 10MHz sinusoid waveform as the TX input and recorded the recovered signal at RX output. Notice that this measurement involve an interference with a power of 5dB higher than the received signal measured at the RX input. The frequency spectrum of this recovered signal is shown in Figure 8.19.

Clearly seen from Figure 8.19, the original single tone signal at 10MHz is recovered with some wideband noise. The in-band SNR evaluated in a bandwidth of 10MHz is calculated to be -6dB. The in-band SNR is slightly worse than -5dB at the RX

input, because the desired signal power is degraded by about 10dB due to the degradation in synchronization accuracy in the presence of large interferences.

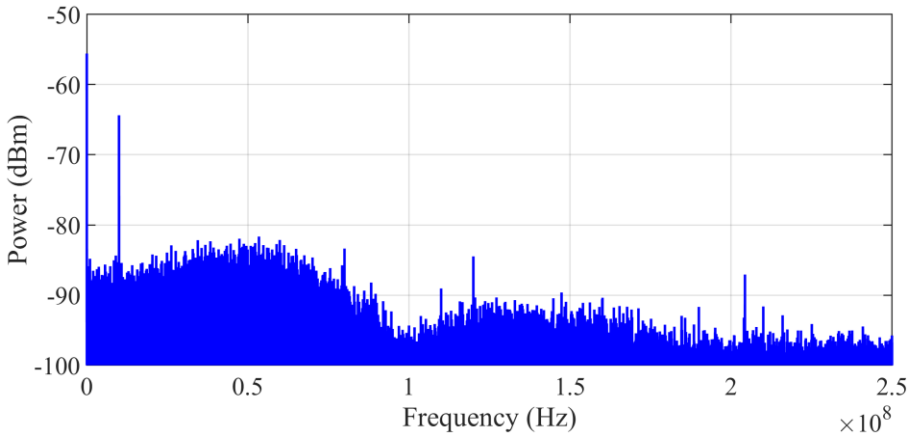


Figure 8.19. Frequency spectrum of RX outputs corresponding to 10MHz sinusoid TX input in the presence of 5dB higher power interference after synchronization.

8.6. Conclusions

In this paper, we propose an interference-tolerant three-level synchronization scheme for wireless communication systems based on direct sequence spread spectrum technique in the context of spectrum sharing. With this synchronization scheme, DSSS system is able to attenuate interferences and recover signal with a desired quality at the same time. An IC prototype fabricated with 40nm CMOS technology is demonstrated capable of achieving synchronization even in the presence of an interference that has power of 5dB higher than the received signal measured at the RX input.

9. CONCLUSIONS

In this dissertation, I briefly talked about the background of spectrum sharing, including the history of wireless communication and the future development, talked about the present spectral congestion issue and its potential solution of spectrum sharing. Then I reviewed the four main existing spectrum sharing paradigms, talked about the pros and cons of each paradigm with examples, and proposed a new hybrid mode spectrum sharing system based on direct sequence spread spectrum (DSSS) technique. Later, I briefly talked about the fundamentals of code domain multiple access (CDMA) including different spread spectrum techniques, different types of codes used in CDMA systems, and the benefit of randomization systematic interferences that is always ignored. Next, I provided the block diagram of a conventional DSSS system and explained the theoretical reason for the benefit in interference rejection. Later, I talked about the first main challenge in the current analog DSSS transceiver designs, TX sideband leakage issue, and proposed the solution of sinusoid-like PRS to reduce the power in sidelobes of binary PRS. In the following chapter, I talked about the second main challenge in the current analog DSSS transceiver designs, synchronization in DSSS system. Here, I explained in detail the reason for synchronization and the existing synchronization schemes, and provided our solution of three-level synchronization scheme. In the following two chapters, I explained in detail the two projects I worked on. In the chapter of An Efficient Sinusoid-like Pseudo Random Sequence Modulator/Demodulator System with Reduced Adjacent Channel Leakage and High Rejection to Random and Systematic Interference, I showed the effectiveness of the proposed SPRS based system in knocking down sideband leakage of

conventional DSSS system. Then in the chapter of An interference-tolerant synchronization scheme for wireless communication systems based on Direct Sequence Spread Spectrum, I showed the benefit and feasibility of the proposed three-level synchronization scheme. In summary, this thesis effectively solve the two main challenges of conventional DSSS system and convinced us the feasibility of this new hybrid mode spectrum sharing.

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