A DUAL BAND CMOS CLASS F VCO AT MMWAVE FREQUENCIES

A Thesis

by

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ABSTRACT

With growing demand for 5G applications, there is huge amount of interest for communication systems operating at 5G frequencies. An integral part of these systems is a Voltage Controlled Oscillator (VCO). RF signals need to be modulated on-to a carrier frequency for wireless communication. A VCO are used to generate the carrier frequency signal. Communication standards dictate the Phase Noise requirement of the oscillator based on the number of channels in the band.

Class F VCOs are known to provide 3dB better Phase Noise than traditional Class B VCOs. Current work explores this benefit at mmWave frequencies. This work proposes a Class F dual band VCO with active switching capability, centered around the two mmWave bands at 22 and 35GHz. A Class B VCO is also designed for similar frequency bands, to validate the FoM improvement of a Class F design. Both the VCOs are designed using Global Foundaries 22nm FDSOI process.

The Class F VCO achieves a tuning range of 22% and 14% in the 22 and 35GHz bands, and phase noise 1MHz is less than -112dBc/Hz and -103dBc/Hz in the low and high bands, respectively. The Oscillator consumes 17mW at 0.8V supply. In comparison, the Class B Oscillator provides FoM of 190dB and 185dB while the Class F design gives FoM less than -192dB and -190dB in 22 and 35GHz bands respectively, suggesting that the Class F design gives superior performance.

DEDICATION

To my Mother and Father

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1. INTRODUCTION

The development of CMOS technology has made mobile handsets more affordable to the common man. With increasing usage, mobile traffic is increasing exponentially, necessitating the availability of high bandwidths for data transfer. The advent of 5G and mmWave technology has helped tackle this problem. Universities and corporates alike, are highly invested in the research leading to mm-Wave front end modules that can be feasibly deployed for mobile communications.

The fifth generation of mobile communication standard [2] currently comprises of low band (< 1GHz), mid band (sub 6GHz) and high band (24GHz – 40GHz) spectra. For an average user in the US, realistic download speeds are 40Mbps, 125Mbps and 1Gbps for low, mid, and high bands, respectively. Coverage being the trade-off for speed, high band 5G is still a lucrative option for urban, densely populated areas. Mm-wave "small cells" that use high band 5G cover a 1-mile radius, giving download speeds as high as 3Gbps. Top network and handset providers have begun their foray into the 5G market [3], paving the way for at least a couple of decades' worth of applications for mm-Wave chip-sets. In view of these developments, this work focuses on building a low phase noise VCO for high-band 5G applications.

1.1 Research Objective

The objective of this research is to provide detailed methodology for designing a VCO that is simultaneously Class F and Dual Band, at mmWave frequencies. While numerous implementations of Class F structures exist in literature, there is only one implementation [12] at mmWave frequencies, but it lacks the tank analysis and detailed design steps. In this work, the tank is thoroughly analyzed and the insights gained are used to extend the topology to a Dual Band VCO.

Wide Band VCOs based on active switching of inductively and capacively coupled tanks was used in [14], [6] and [10]. This idea is adapted to the current tank, to implement a VCO operating in two distinct 5G bands. To verify the phase noise advantage claimed by Class F architecture, a Class B Dual Band VCO is also designed as part of the research.

1.2 Thesis Organization

Following the Introduction, Section 2 describes the Phase Noise mechanisms in LC oscillators, followed by a discussion of various figures of merit for Class B and multiple Class F architecture

Section 3 discusses the intricacies involved in designing a Class F oscillator at mmWave, with detailed analysis of the tank

In Section 4, the Dual Band topology is discussed, followed by how it is extended to the Class F tank.

Section 5 starts with the features offered by the 22nm Fully Depleted Silicon on Insulator (FDSOI) process, followed by the design implementation of active and passive portions. The high frequency EM effects are also discussed here.

In Section 6, results are discussed, accompanied by the simulated ISF. Comparison with the state-of-the-art VCOs at mmWave is presented here.

The final Section 7 concludes the thesis with future work.

2. LC OSCILLATORS

2.1 Phase Noise in LC oscillators

Phase noise is a critical parameter in VCOs. The effects of phase noise in the RX and TX paths in shown in Fig 2.1. In RX path, non-ideal skirt of the VCO can down-convert the significant levels of a nearby interferer, then degrading the SNR of the signal. In the TX path, the VCO up-converts the signal which then falls within the VCO skirt. This degrades the SNR of the transmitted RF signal. In this section we review the phase noise derivation discussed in [13], as this approach helps understand the VCO classification.

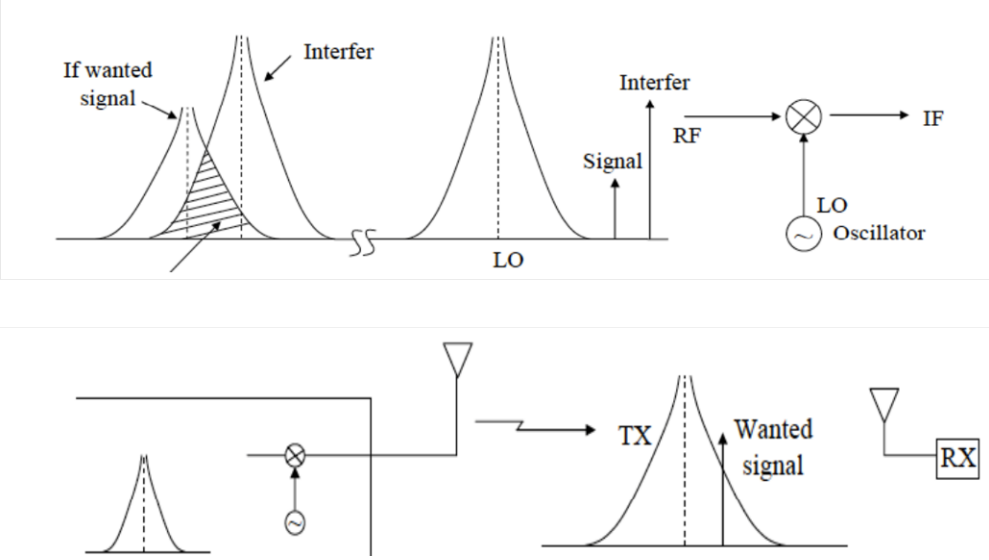


Figure 2.1: Effect of Phase Noise in RX (above) and TX (below) front-end systems [17]

2.1.1 Noise in an LC tank

Figure 2.2 shows an LC oscillator. The initial voltage on capacitor dictates only the amplitude of oscillation, has no bearing on the frequency. Frequency of operation is determined by the amount of time taken for the exchange of energy between L and C. This is dependent entirely on L and C

values. We start off by considering a current noise source that injects a noise charge equivalent to

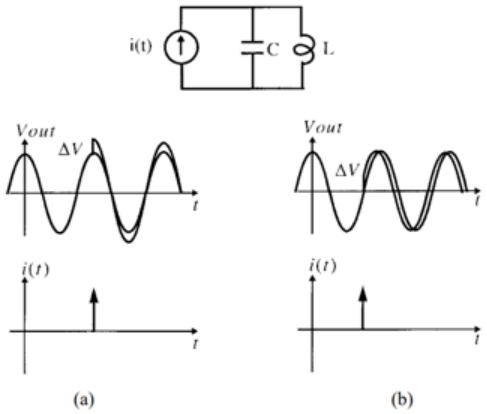


Figure 2.2: Current noise manifestation at different time instances in an LC oscillator [13]

Δq_n. This changes the voltage on the capacitor, V_c, by ΔV_n. The inductor current is unaffected as it opposes sudden changes in current. If this ΔV_n is caused at the peak of oscillation, the charge is static and hence modifies V_c, therefore modifying just the *amplitude* of oscillation. On the other hand, if it is caused at the zero-crossing, the charge is moving at the fastest rate (since current is at its peak), hence the added charge is also moved, causing a *phase* delay. Injecting noise at any intermediate point would result in a combination of both amplitude and phase changes.

2.1.2 ISF

For the reasons mentioned in Section 2.1.1, the oscillator system is characterized as a linear time variant system. As seen in Figure 2.3, the phase introduced by a current pulse is a function of the time instant that it gets introduced, given by $h_\phi(t, \tau)$ or simply, Impulse Sensitvity Function. It is also seen that any amplitude perturbations die down, due to the limiting behavior of practical systems. According to [13], there are three ways to derive ISF.

- **Measurement-based:** Current noise impulses are injected at different time instances and the shift in phase is measured for few cycles

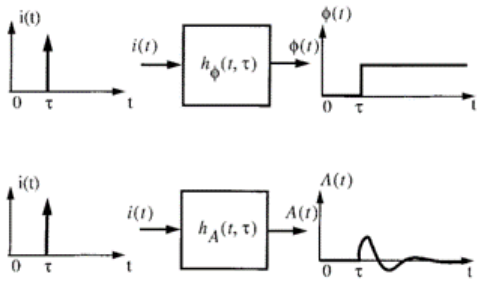


Figure 2.3: Impulse sensitivity function for a Linear Time variant system

- **Closed-form:** An n-th order system is viewed as an n-dimensional state space. l is the projection of the perturbation vector ΔX (noise) onto the unity vector in the direction of motion ($\frac{\dot{\bar{X}}}{|\dot{\bar{X}}|}$). The excess time caused by this perturbation is calculated as distance/velocity ($\frac{l}{|\dot{\bar{X}}|}$). The excess phase is then calculated from Δt. These steps are indicated below.

$$\Delta t = \frac{l}{|\dot{\bar{X}}|}$$
$$l = \Delta\bar{X}.\frac{\dot{\bar{X}}}{|\dot{\bar{X}}|} \implies \Delta t = \Delta\bar{X}.\frac{\dot{\bar{X}}}{|\dot{\bar{X}}|^2}$$
$$\Delta\phi = 2\pi\frac{\Delta t}{T} = \frac{2\pi}{T}\left(\Delta\bar{X}.\frac{\dot{\bar{X}}}{|\dot{\bar{X}}|^2}\right)$$

Now we substitute the perturbation ΔX (noise) with the noise voltage given by $\frac{\Delta q_i}{C_i}$, where i represents the state space dimension.

$$\Delta\phi_i = \frac{2\pi}{T}.\frac{\Delta q_i}{C_i}.\frac{\dot{v}_i}{|\dot{v}|^2}$$
$$\Gamma_i(x) = \frac{f_i'}{|\bar{f}'|^2} = \frac{f_i'}{\sum_{j=1}^{n} f_j'^2}$$

For example, in a second order system, v and v' can be chosen as the state variables. So

assuming v=sin(ωt), the ISF for a second order system is given as below.

$$\Gamma(\omega t) = \frac{v'}{|\bar{v}'|^2} = \frac{cos\omega t}{cos^2\omega t + sin^2\omega t}$$
$$\implies \Gamma(\omega t) = cos\omega t;$$

It is worth noting that for an n-th order system, the ISF is inversely proportional to the magnitude of first derivative.

- **Approximation:** ISF is proportional to the first derivation of voltage waveform

$$\Gamma_{approx} = \frac{V'(t)}{V_o} \tag{2.1}$$

where V_o is the maximum value of $V(t)$.

In addition of the time-variant system itself, the statistical properties of the random noises maybe periodic (cyclo-stationary) in nature. For example, g_m of the transistor varies periodically, due to varying gate voltage. Therefore, we need to calculate the "effective ISF" (Γ_{eff}), by taking this effect into account. Then the cyclo-stationary noise source can be treated as a stationary noise source with the ISF = Γ_{eff}. Examples of Γ_{eff} are shown in Figure 2.4. As seen, Γ of the Colpitt's and LC is modulated by the corresponding cyclostationary parameter α, resulting in a modified Γ_{eff}.

The phase noise equation for thermal noise sources discussed so far, is given as below [13]

$$\mathcal{L}\{\Delta\omega\} = 10log_{10}\left(\frac{\Gamma_{rms}^2}{q_{max}^2}.\frac{\bar{i_n^2}/\Delta f}{4.\Delta\omega^2}\right) \tag{2.2}$$

where,

$q_{max} = \Phi_{max} = LI_{swing}$, where L is the inductance of the tank Γ_{rms} is the root-mean square value of ISF $\Delta\omega$ is the offset at which Phase Noise is measured $i_n^2/\Delta f$ is the current noise spectral density

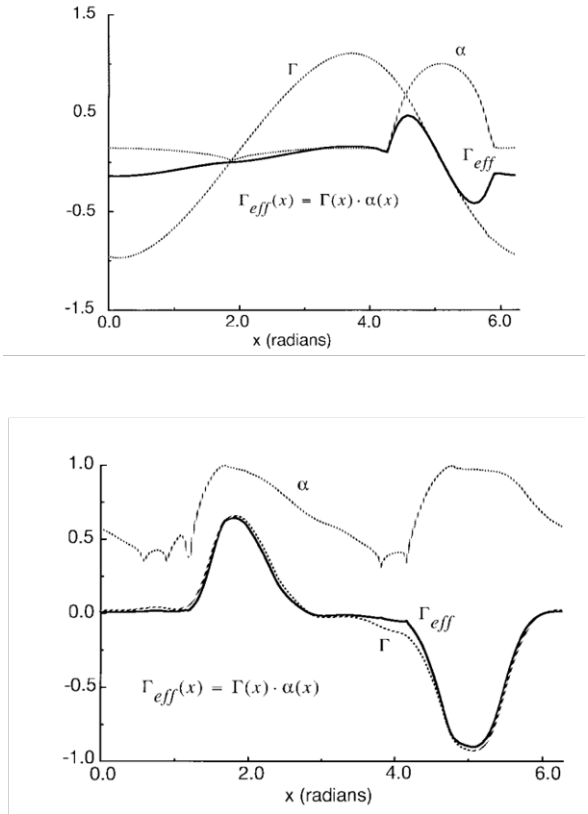


Figure 2.4: Γ_{eff} of (above) Colpitt's oscillator (below) Cross coupled LC oscillator [13]

2.1.3 Flicker noise manifestations

The $\frac{1}{f^n}$ noise sources in the system appear with a $\frac{1}{f^{(n+2)}}$ in the phase noise spectrum due to the inherent f^2 in the denominator of Equation 2.2. As a result, flicker noise translates to the $\frac{1}{f^3}$ region of the phase noise curve. This portion of the phase noise spectrum is given by the Equation 2.3, where c_o is the DC component of the ISF and $\omega_{1/f}$ is the flicker noise corner of the transistors. Therefore, flicker noise to phase noise conversion can be minimized if the DC component of Γ_{eff} is zero. i.e., if Γ_{eff} is symmetric.

$$\mathcal{L}\{\Delta\omega\} = 10log_{10}\left(\frac{c_o^2}{q_{max}^2}.\frac{\bar{i_n^2}/\Delta f}{8.\Delta\omega^2}.\frac{\omega_{1/f}}{\Delta\omega}\right) \tag{2.3}$$

2.2 VCO Classes

Integrated VCO Classes have been extensively studied in literature. Each of these classes targets different drawbacks of the traditional cross-coupled oscillator and aims to mitigate them. The class differentiation is based on power amplifier classification. In this section we review the Class B, Class C and variants of Class F VCO architectures.

2.2.1 VCO Figure of merit

Before delving into the Class specifications, it is worth looking at a comparison metric. The Figure of Merit (FoM) is a useful combined representation of the key parameters of a VCO, namely Phase Noise, Power Consumption, Oscillation frequency and Amplitude. One such FoM that is frequently used to compare performance of different VCO Classes is given below [11]

$$FoM = -10\log_{10}\left(\frac{10^3\kappa_B T}{2Q^2\alpha_I\alpha_V}(\gamma + 1 + \eta\gamma_T g_{m_T} R_{tank})\right) \tag{2.4}$$

where,

Q is Quality Factor of load tank

α_I the ratio of Current Amplitude of Fundamental harmonic to I_{bias} (current efficiency)

α_V the ratio of Voltage Amplitude of Fundamental harmonic to VDD (voltage efficiency)

g_{m_T} is the transconductance of tail transistor

η is the measure of oscillation amplitude (varies from 0 to 1)

T is Temperature in Kelvin, κ_B is Boltzmann constant

γ is the channel noise factor

2.3 Class B VCO

The traditional cross-coupled LC oscillator is the most widely used design due to its simplicity and robustness. Due to the band-pass filter characteristic of the LC load impedance that the switching square wave current sees, the output voltage is sinusoidal at the fundamental frequency.

The oscillator wakes-up if the tank losses, represented by a parallel resistor R$_tank$ is *sufficiently* cancelled by the negative resistance imposed by the cross-coupled g$_m$ pair. Such an oscillator is shown in Figure 2.5 [11]

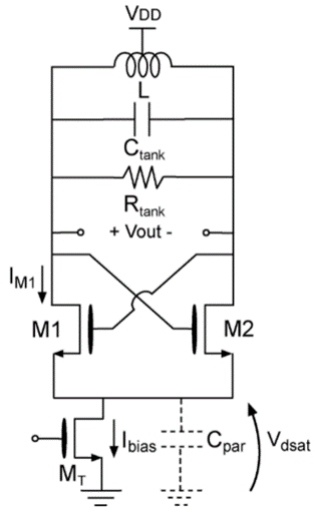


Figure 2.5: Cross-coupled pair LC Oscillator (Class B) [11]

To understand why it is also known as a Class B VCO, shown in Figure 2.6 is a Class B PA. Each of the transistors M_1 and M_2 are on for 50% of the cycle. The drain current in the transistors is a square wave, with opposite phase, same as the transistors in the cross-coupled oscillators. In PAs, the 'on' time of the transistor device, also referred to as the conduction angle dictates the power efficiency of the amplifier. The smaller the angle, the higher the efficiency. In terms of VCO figures of merit, the conduction angle dictates the current (α_I) and voltage efficiencies (α_V), i.e., how much of the bias current (or voltage) is present at the desired frequency of interest.

The theoretical FoM_{max} of a Class B VCO is -194dB at 1MHz offset from the carrier [11]. To arrive at this number, two assumptions were made:

- The tail current source is ideal, which allows for seamless rail-rail swings while injecting *no noise*.

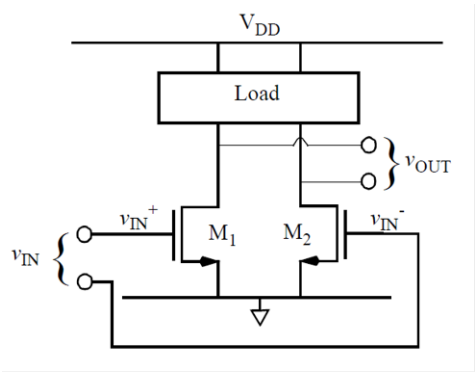


Fig 1 (a) Class B PA

Figure 2.6: Class B Power Amplifier [17]

- Transistors switch abruptly, resulting in perfect square wave I_D current

More realistically, the tail current source is implemented using a transistor (M_T), which requires a finite voltage headroom $V_{D_{Sat}}$, which results in reducing α_V parameter. To reduce $V_{D_{Sat}}$, the width W_T can be increased. Since this results in an increase in g_{mT}, the **current noise** injected by M_T, given by $4kTg_{mT}$ also increases. So when we try to improve α_V, the phase noise degrades after a point. This effect is elucidated in Figure 2.7 A second concern is the effect of **parasitic**

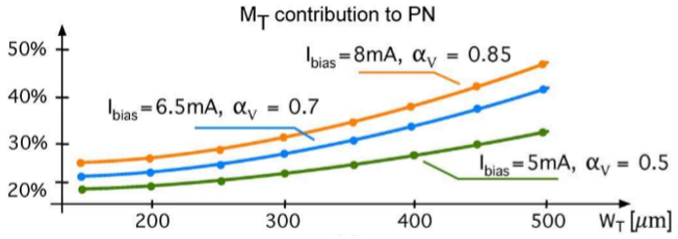


Figure 2.7: Trade off between α_V and phase Noise in Class B VCOs [11]

capacitance introduced by M_T. As W_T increases, C_{par} increases. Generally, Class B oscillators are designed for high peak-to-peak swings, as this reduces phase noise. High swings cause the cross coupled transistors to enter triode region during a portion of oscillation. The high parasitic capacitance at the tail limits the voltage change by consuming current during that period. Due to

this, the periodic current resembles that shown in Figure 2.8. This reduces α_I, and hence the figure of merit. This issue is explained in Figure 2.8

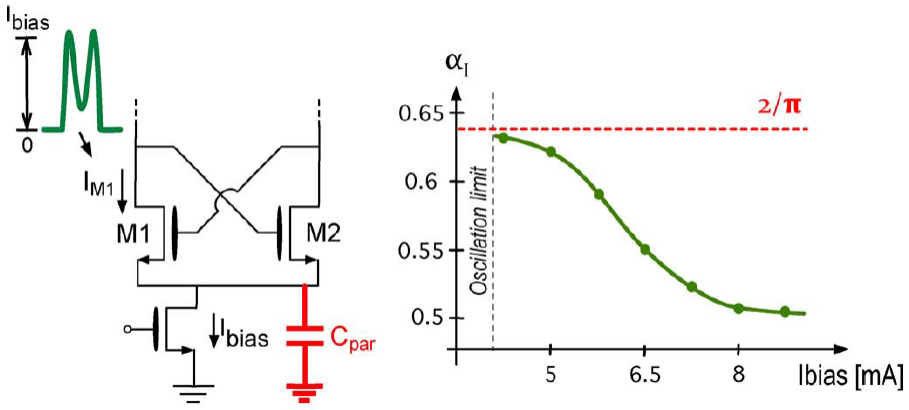


Figure 2.8: Effect of C_{par} on α_I [11]

Figure 2.9 depicts the drawbacks of Class B amplifiers discussed above. To summarize, increasing $I_{bias} \rightarrow$ Increasing W/L to maintain low $V_{D_{sat}} \rightarrow$ Increases parasitic $C_{par} \rightarrow$ reducing α_I. This also increases the Phase Noise due to noise from M_T, thus degrading the achievable FoM in a Class B VCO.

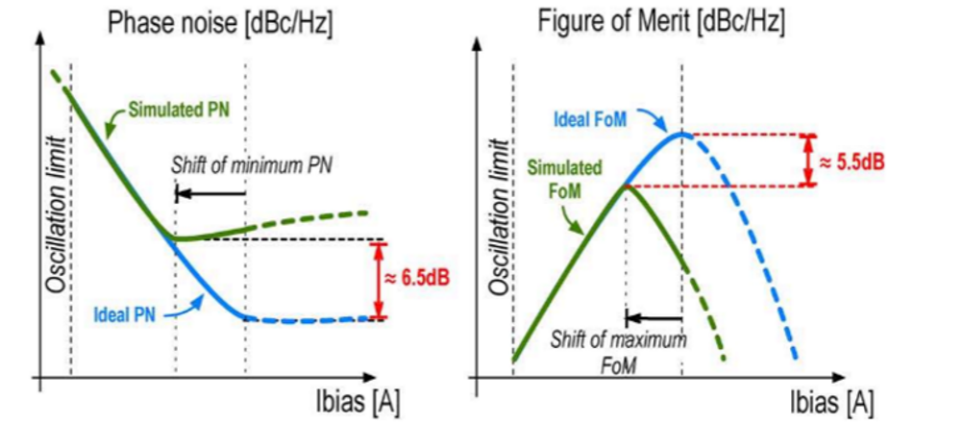


Fig 6

Figure 2.9: Effect of non-idealties on the FoM of a Class B VCO [11]

2.4 Class C VCOs

Class C VCOs aim to mitigate the above drawbacks faced by Class B VCOs. Due to the cross coupled nature of the g_m pair, the transistors are biased as diode connected transistors at DC. By explicitly biasing them close to threshold or sub-threshold regions, the triode region operation can be avoided, as long as the swing is not too high. With this is implemented, the tail transistor can afford to be wider. A wider M_T also leads to lower $V_{D_{sat}}$, resulting in better α_V as well. Since the transistors do not enter triode, C_{par} no longer affects the drain current waveform. In fact, intentional C_{tail} can now be added that filters M_T noise components at $2\omega_o, 4\omega_o, 6\omega_o, ...$

Class C VCOs derive the nomenclature due their likeness to Class C power amplifiers. Shown in Figure 2.10 is the topology of a Class C VCO. Figure 2.11 shows the drain current waveforms

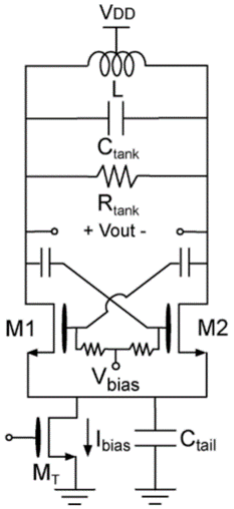


Figure 2.10: Class C VCO [11]

in Class C, Class B (ideal), Class B(realistic) VCOs. As seen, Class C VCOs have a DC biasing circuit. Φ, the conduction angle is lowest in a Class C VCO/amplifier.

The drawback of a Class C VCO is its start-up robustness. Due to biasing close to V_{th}, the g_m of the cross-coupled pair is low, which leads to damped oscillations. For this reason, Class C

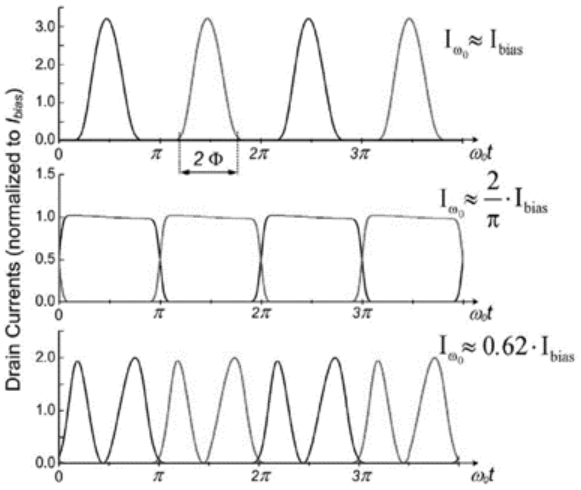


Figure 2.11: Drain current comparison: (Top) Class C (Middle) Ideal Class B (Bottom) Class B with core transistors in deep triode [16]

VCOs need explicit start-up circuitry. In [11], a feedback circuit is implemented that is shown in Figure 2.12. The functionality of this circuit is discussed as follows.

The node voltages during start-up are shown in Figure 2.13. When powered up, V_{CM} is tied to ground due to the cap. The amplifier increases V_{bias}, trying to bring V_{CM} to V_{ref}. Due to this behaviour, at startup, V_{bias} is high. Once V_{CM} reaches V_{ref} (which is set just sufficient to bias the tail transistor in saturation), the cross-coupled transistors achieve enough transconductance to start the oscillations. As the oscillations increase, the large signal excursions at the gate and drain cause V_{CM} node to move. The charging current for C_{tail} is provided by VDD. The polarity of the amplifier is such that this deviation is amplified and used to reduce it (negative feedback). As a result, V_{bias} is brought down. This is reflected at the gate of the cross-coupled transistors with a certain delay due to the Class C Resistor and Capacitor connected to V_{bias}. Hence the amplitude variation follows the V_{bias} curve with a certain delay. As the amplitude of oscillations adjusts to lower value, the spike in V_{CM} begins to discharge into the C_{tail}. This is detected by the Amplifier, which recovers the over-correction in V_{bias}. For Class C, the cross-coupled transistors are biased around $\frac{VDD}{3}$. If we size the transistors for a given I_{bias}, the settled value of V_{bias} will be V_{ref} + $\frac{VDD}{3}$.

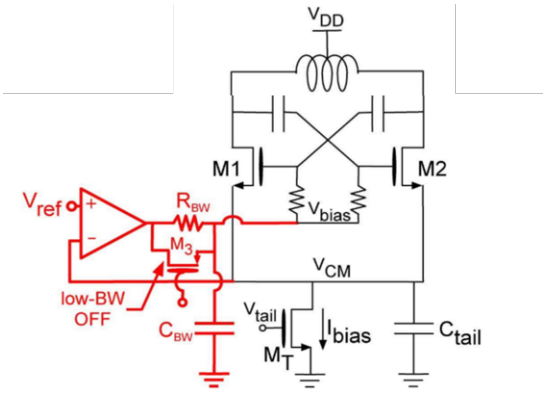


Figure 2.12: Start-up feedback circuitry for a Class C VCO [11]

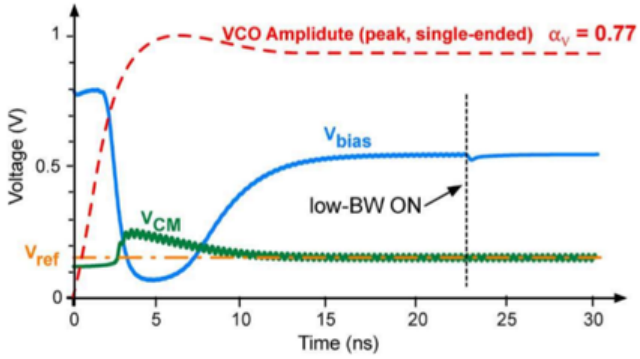


Figure 2.13: Various Node voltages during start-up of a Class C VCO [11]

Other Class F implementations exist in literature that use transformers based DC biasing [16]. In [9], the feedback mechanism relies on peak detection of the output node, rather than the common mode node. Another drawback of Class C toplogy is squegging. It is the phenomenon where amplitude instability is caused due to high parasitic tail capacitance. It causes a low frequency amplitude modulation in the ocillator output, and is undesired. When proper start-up is ensured and squegging is avoided, the Class C oscillator is seen to give FoM $\simeq$ -191dB at 1MHz offset from the carrier.

2.5 Class F VCOs

As seen in previous sections, Class B VCO's noise performance has a trade-off with voltage swing, as g_m devices enter triode region for higher swings. This poses limitation on M_T transistor sizing as well. Even though Class C architecture improves Phase Noise, FoM is limited by α_V, the voltage efficiency, which cannot go beyond 0.7 [4], if the g_m devices are to be in saturation throughout. Hence, there is a need to reduce phase noise without compromising on other figures of merit.

2.5.1 Class F_3 VCOs

As discussed in Section 2.1.2, Γ_{eff} determines the extent of voltage to phase noise conversion. Approximately, Γ_{eff} is proportional to the first derivative of voltage waveform. Hence, a square waveform at drain voltage would ensure that no noise from triode devices gets converted to phase noise. This is elucidated in Figure 2.14.

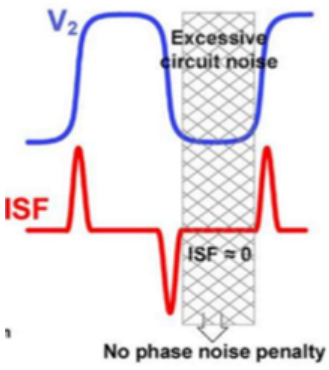


Figure 2.14: Noise contribution with a square waveform at Drain [4]

The drain current is known to contain higher order components. In a traditional Class B/C Oscillator, these components get filtered out by the tuned tank impedance (They flow through low impedance capacitances and slightly distort the voltage waveform, causing Groszkowski effect [7]. So, by introducing a peak in tank impedance at $3\omega_o$, the 3rd harmonic can be added to the drain

voltage waveform, making it closer to a square wave. As long as the 1st and 3rd harmonics add up constructively with a phase error less than $\frac{\pi}{8}$, the closed form ISF of drain voltage waveform can be calculated as below [4].

$$\Gamma_{rms}^2 = \frac{1}{2}\frac{1+9\zeta^2}{(1+3\zeta)^2} \tag{2.5}$$

where $\zeta = \frac{V_{p3}}{V_{p1}} = \frac{R_{p3}}{3R_{p1}}$. As per the expression in 2.5, Γ_{rms} reaches a minimum of 0.25 for $\zeta = 0.33$. The traditional Class B/C oscillators have Γ_{rms} value of 0.5. Due to this, the Class F_3 oscillator achieves a theoretical 3dB better phase noise. The schematic in Figure **??** depicts the first Class F architecture seen in literature. Here, two resonances are achieved by one transformer to reduce the area. The resonant frequencies are a function of L_s, L_p, C_s,C_p, k_m as seen in Equation 2.6. For choosing X-factor, the ratio of $\frac{\omega_2}{\omega_1}$ is plotted vs X. Two solutions are seen for km = 0.7. The amplitude of waveforms being added is determined by the ratio of $\frac{R_{p2}}{R_{p1}}$. If R_{p2} is very high, the required conductance to satisfy Barkhaussen's criteria will be low, leading to oscillations at $3\omega_o$.

$$\begin{aligned}
\omega_1^2 &= \frac{1}{(L_pC_1 + L_sC_2)} \\
\frac{\omega_2}{\omega_1} &= \sqrt{\frac{1+X+\sqrt{1+X^2+X(4k_m^2-2)}}{1+X-\sqrt{1+X^2-X(4k_m^2-2}}} \\
X &= (\frac{L_s}{L_p}.\frac{C_2}{C_1}) \\
\frac{R_{p2}}{R_{p1}} &\approx \frac{(1-k_m^2)(1+X)}{6}
\end{aligned} \tag{2.6}$$

2.5.1.1 Interpreting impedance from two-port analysis

Figure 2.17 shows the two port parameters of the circuit shown in Figure 2.16. In Figure 2.17(a) the ratio of Resistance peaks determines he sharpness of drain voltage waveform. It is seen that Z_{in} has same phase for both frequencies. This means constructive addition (sharper zero crossing, which is good for ISF) It is seen that for Z_{21}, the peaks are out of phase. This means destructive addition (slower zero crossing, bad for ISF). To mitigate the phase noise degradation

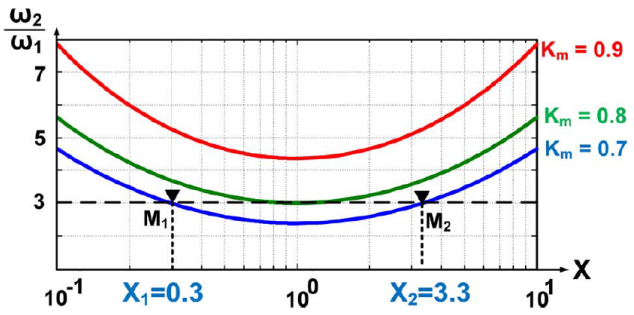


Figure 2.15: Ratio of tank resonant frequencies versus X-factor for different k_m [4]

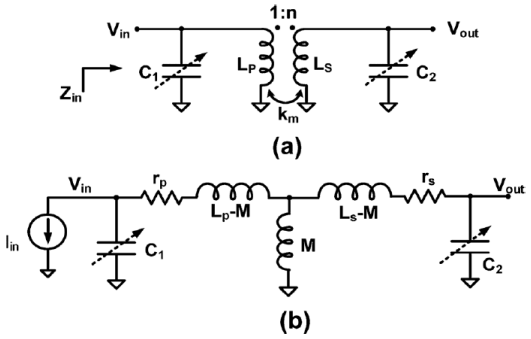


Figure 2.16: (top) Transformer-based resonator (bottom) Equivalent tank circuit for 2 port analysis[4]

due to slow zero crossings at the secondary, the magnitude of Z_{21} is designed to be negligible at the 3rd harmonic. This leads to sine wave at the secondary output. To increase the slope of sine wave at zero crossing (to improve ISF), the gain from primary to secondary is made higher by choosing higher X-factor. The problem of oscillation occurring at $3\omega_o$ due to high X-factor (discussed earlier) is mitigated by slight architecture change. Instead of connecting the secondary coil as floating, it is cross-connected to the gates, as seen in the Figure 2.18 on the left. Due to the high gain from primary to secondary, gate transitions are sharper, resulting in a shorter commutation time leading to lesser noise from gm devices. It also results in high 3rd harmonic component in the drain current, which leads to sharper voltage waveform at the drain.

In summary, a Class F_3 oscillator enhances the 3rd harmonic current, resulting in a square

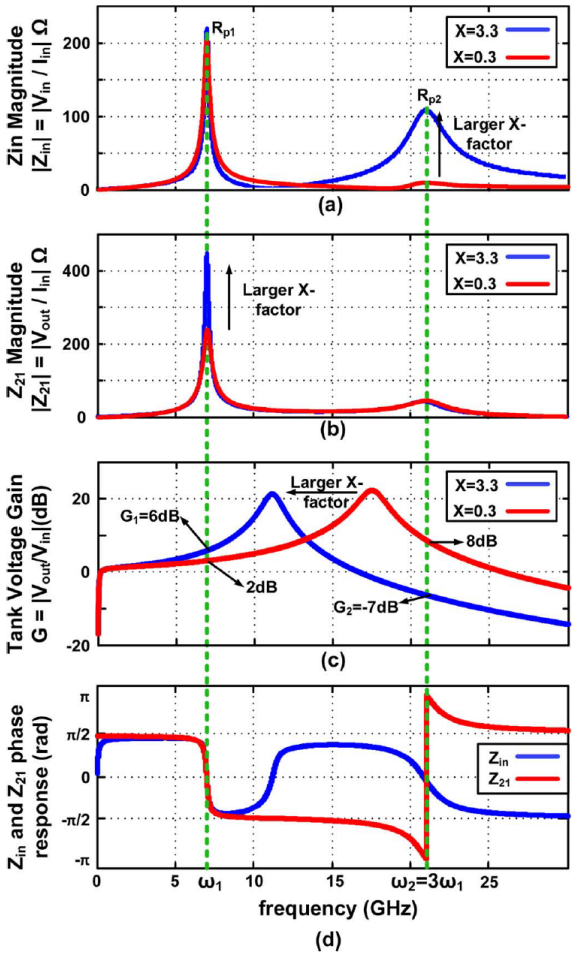


Figure 2.17: Transformer-based tank characteristics: (a) Input-impedance magnitude; (b) Trans-impedance; (c) Transformers' primary to secondary voltage gain; (d) phase of Z_{in} and Z_{21} [4]

waveform at the output. It achieves a the theoretical 3dB phase noise improvement when compared to its Class B counterpart. Due to the inductive gain in the cross-coupling path, gain voltage sees high sinusoidal swings. This is avoids slow zero crossings, which are known to degrade Phase Noise.

Figure 2.19 compares the drain and gate voltages of the VCOs discussed so far. Table 2.1 compares the figures of merits of these VCOs from literature [4]

where F_{source} is the *noise factor* due to the source (eg: R_P, G_{DS})

As seen, F_{RP} for Class F is best due to the opitimized ISF. F_{GDS} is lower compared to Class

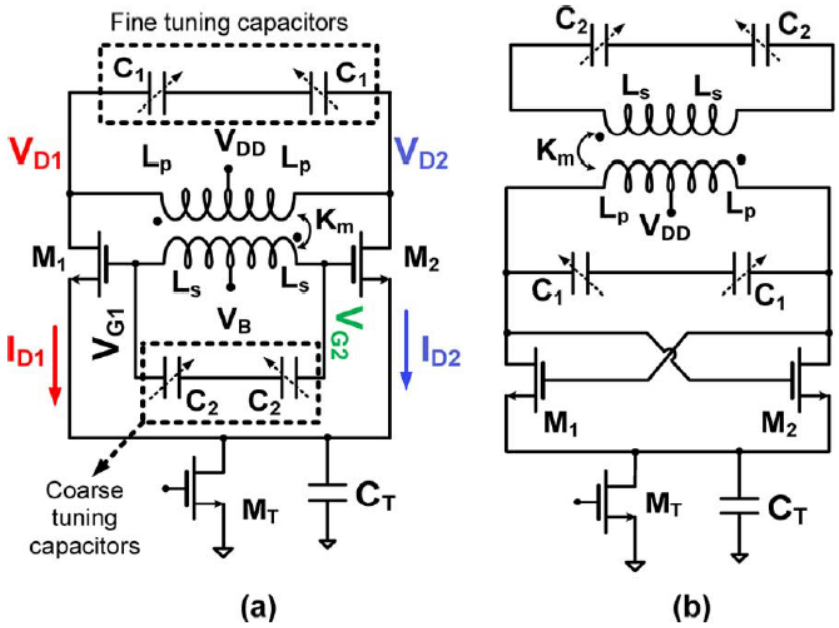


Figure 2.18: Two options of the transformer-based class-F oscillator: (left) transformer-based coupling (right) cross-coupled [4]

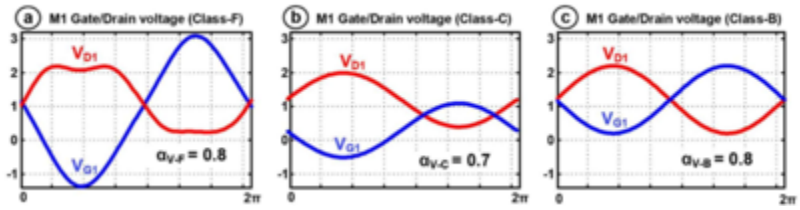


Figure 2.19: Comparing Gate (red) Drain (blue) voltage: (Left) Class F (center) Class C (right) Class B [4]

C, but better than Class B because of high swings at the gate. F_{GM}, is the sum of the above two noise factors. As seen, the improvement caused in F_{RP} is sufficiently high, so that the overall noise factor for Class F is the best. α_I is best for Class C, due to the low conduction angle. α_I for Class F is better than Class B, as it has an alternate current path (through the transformer) other than C_{tail}, which reduces the undesired second order content in the drain current. α_V is 0.8 because g_m devices are allowed to enter triode region, giving similar swings as Class B. As expected Phase Noise is best, due to the combined effect of improved ISF and sharper gate transitions.

Parameter	Class-B	Class-C	Class-F_3
F_{RP}	1	1	0.7
F_{GDS}	0.56	0.07	0.27
F_{GM}	1.56γ = 2.02	1.07γ = 1.39	0.7γ = 0.91
F (dB)	5.5	3.9	2.8
α_I	0.55	0.9	0.63
α_V	0.8	0.7	0.8
PN (dBc/Hz)	-133.5	-134	-136
FoM (dB)	191.2	194.5	194.2

Table 2.1: Comparing figures of merit across Class B,Class C and Class F VCOs [4]

2.5.2 Class F_2 VCOs

Another VCO class that has emerged to mitigate the drawbacks of Class B is Class F_2 VCO. If falls in Class F category due to its characteristic wave-shaping architecture. We discuss the evolution and working principle of Class F_2 VCO in this section. It is seen in literature **??** that a tank with step-up transformer improves the Q by lowering the equivalent Rp by $(1 + n^2)$. But this alone did not help reduce phase noise, as the classic triode region problem of Class B oscillator still persists. Figure 2.20 shows a VCO implemented with a step-up transformer load. The transformer gives high primary to secondary gain, which causes high swing at the gate (GA). The parasitic cap at M_T forms low impedance path to ground and degrades the Q of the system. Finite V_{DSAT} reduces α_V. If size of M_T is increased to improve α_I, it's noise contribution increases. For this reason, Class F_2 operation is proposed, which allows higher headroom for M_T without degrading α_V, while also giving lower Γ_{rms} as compared to Class B/C. The principle of F_2 oscillators is as discussed.Second harmonic in drain current is in quadrature with the fundamental and appears as common mode current. Third and first harmonic currents appear as differential mode currents. If the tank impedance is designed to add first and second harmonics in the desired ratio, it would give rise to a soft-clip waveform (V_{DA} and V_{DB}). The waveform and its corresponding ISF for different amplitude ratio of 1st and 2nd harmonics is shown in the Figure 2.22. The sharper transitions improve ISF and hence Phase noise For $\zeta = 0.3$, $\Gamma_{rms} = 0.35$ (recall that $\Gamma_{rms|ClassB} = 0.5$ and

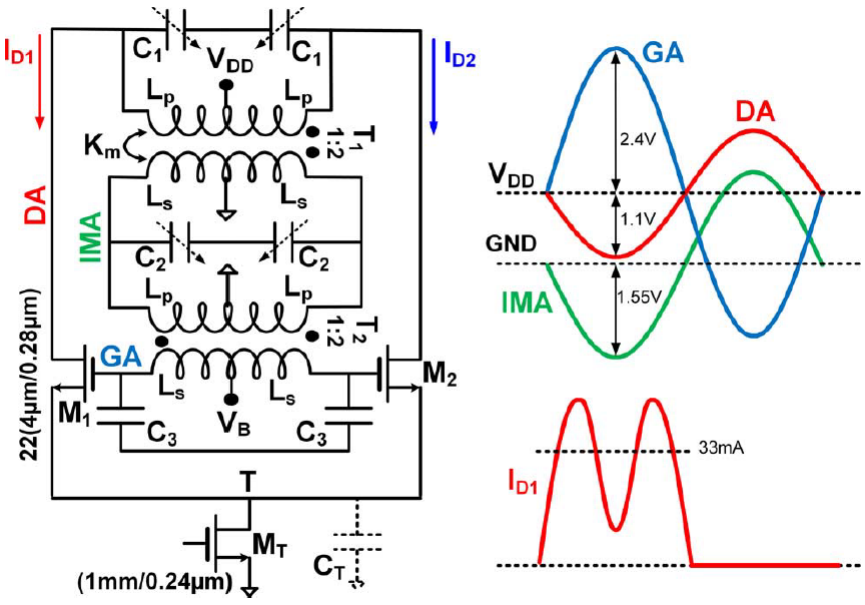


Figure 2.20: (Left) VCO implementing step-up transformer load (Right) Effect of C_T for high swings [5]

$\Gamma_{rms|ClassC} = 0.25$). As seen, the waveform is shifted up by $\zeta * VDD$, allowing headroom for M_T transistor without compromising on α_V. It is seen that the increased headroom allows M_T to stay closer to an ideal current source, reducing the dimple in the drain current waveform. This improves α_I and hence the FoM. ISF at the drain is improved as expected. Shown in table 2.2 is a comparison of Class F_3 and Class F_2 oscillators. It is seen that Class F_2 has better α_V, but is poorer in Phase Noise due to poorer ISF. It is worth noting that the F_2 design still has a better phase noise than its Class C and Class B counterparts.

2.5.3 Class F_{234} VCOs

Another VCO architecture based on wave-shaping is the Class F_{234} VCO. Figure 2.23 shows the topology proposed in [12]. It proposes a wide $3f_o$ peak, which mitigates the need for an explicit tuning circuitry for the 3rd harmonic, which improves both the quality factor and the phase noise. Additionally, due to the boosting of 3rd harmonic current component, the voltage waveform is closer to that of a tradition Class F_3 oscillator. Additionally, the tank passives are chosen such that the common mode tank impedance sees a peak at the second harmonic. For this reason, the final

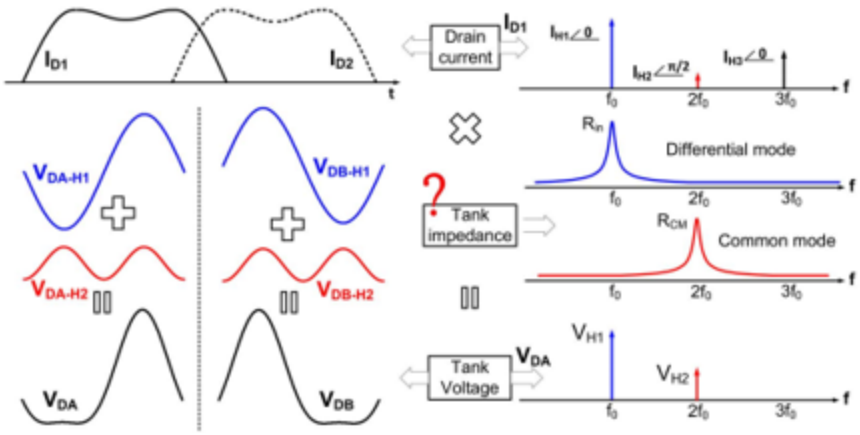


Figure 2.21: Principle of Class F_2 oscillators [5]

Parameter	Class-F_3	Class-F_2
α_I	0.6	0.6
α_V	0.8	0.9
F_{Tank}	0.7	0.8
F_{GDS}	0.3	0.25
F_{GM}	$\simeq 0.7\gamma_{M1}$	$\simeq \gamma_{M1}$
F_{GMT}	$\simeq 0.5\gamma_{M1}$	$\simeq 0.4\gamma_{M1}$
F_{GMT}	3.7dB	4.1dB
P_{DC}	8mW	36mW
PN(dBc/Hz)@10MHz offset	-144	-150.5
FoM (dB)	192.9	192.9

Table 2.2: Comparing figures of merit across Class F_3 and Class F_2 VCOs [5]

drain waveform has a second harmonic components in quadrature to the first and third harmonics, resembling the Class F_2 oscillator. This design uses lumped inductors as opposed to transformers. This helps to optimize individual L for Q. The gain achieved by transformer in a traditional Class F_3 is achieved here by the inductive multiplication. Therefore, the gate swing in this design is high, similar to Class F_3. The Figure 2.24 shows the impedance graphs (differential mode and common mode) for the Class F_{234} topology. The tank is designed to have two differential mode impedance peaks, one at the first harmonic and a wider one at third harmonic. Due to this wide peak, the

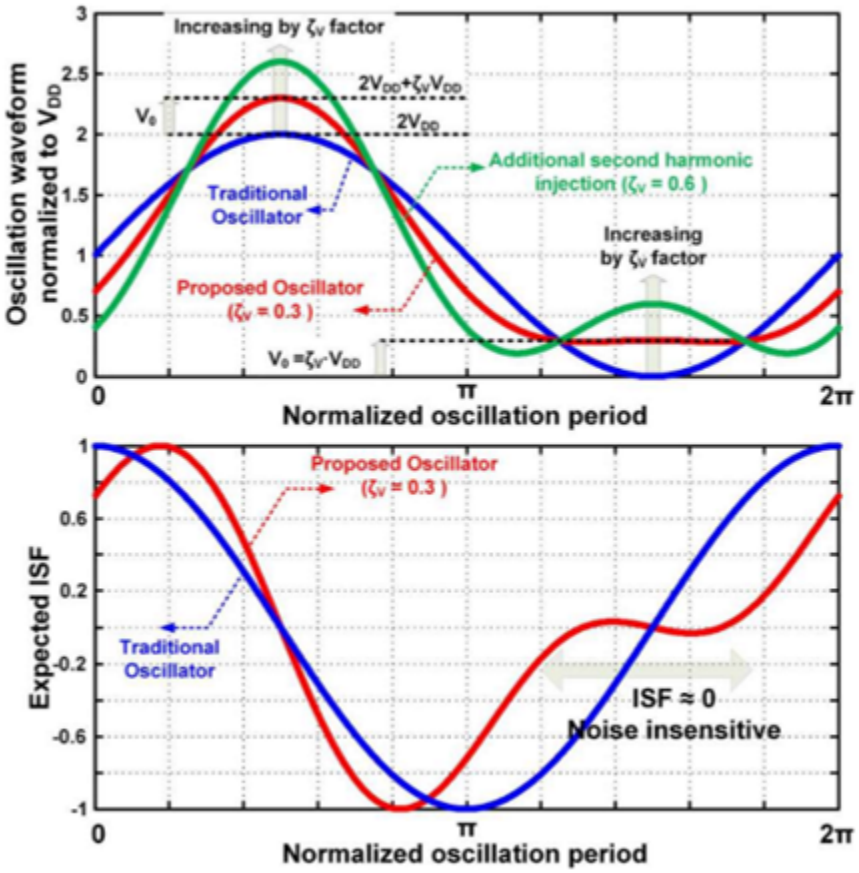


Figure 2.22: (Top) Drain waveform of Class F_2 VCO for different ζ (Bottom) Resultant ISF [5]

differential current component at the fourth harmonic can also get converted to voltage at the drain. Although this is unintended by theory, there is no significant phase noise degradation caused by this, as the current fourth harmonic current flows through the common mode impedance. The tank is designed to simultaneously obtain a second harmonic peak in common mode impedance, to obtain the benefits of Class F_2 oscillators. Figure 2.25 compares the drain and gate waveforms of a Class F_3 and Class F_{234} oscillator. $\alpha_{v,C}$ and $\alpha_{v,P}$ represent the voltage efficiencies of the conventional Class F_3 and the proposed Class F_{234} oscillators. As seen, the ISF of Class F_{234} VCO resembles Class F_3 in the first half of the cycle and Class F_2 in the second half of the cycle. Due to this, the $\Gamma_P = 0.54$, which is slightly higher than $\Gamma_C = 0.5$. The Class F_{234} VCO achieves a FoM of -189.6dB at 1MHz offset [12].

In this work, we use the passive design of Figure 2.23 to build a dual band Class F_3 VCO.

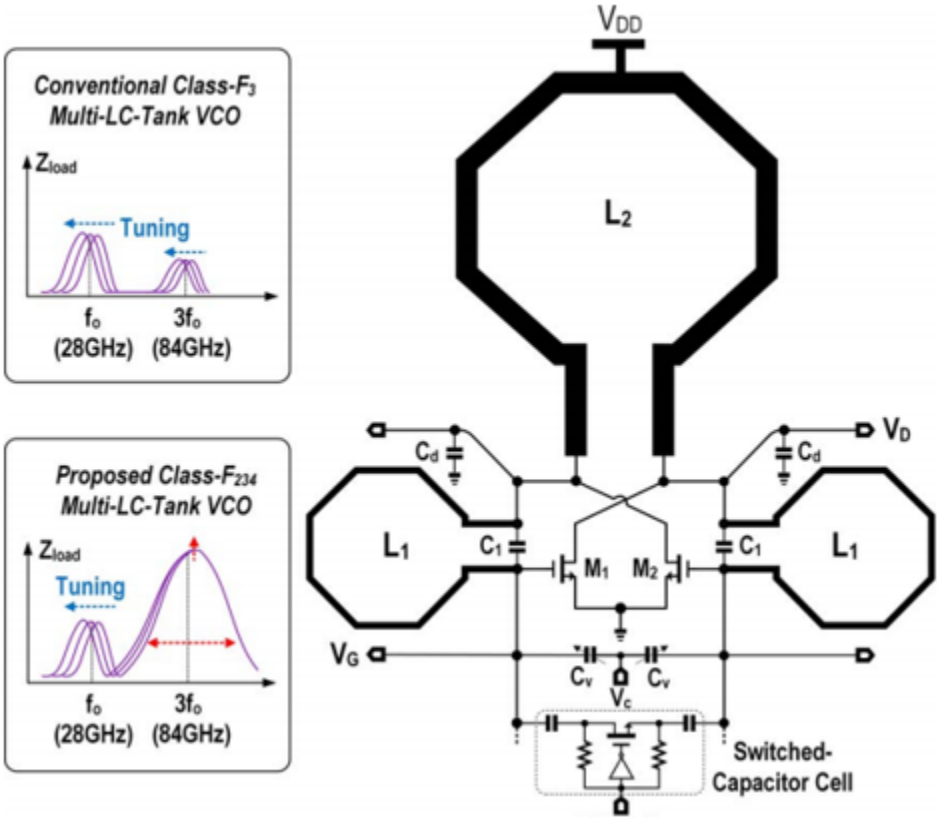


Figure 2.23: Class F_{234} architecture [12]

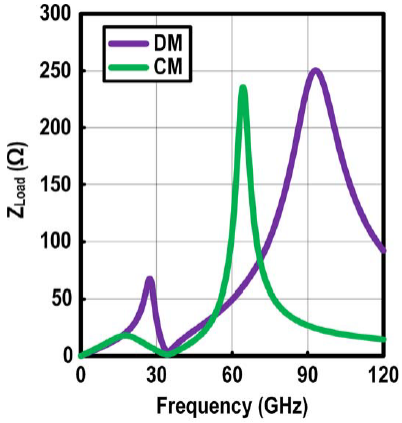


Figure 2.24: Drain Impedance: (purple) Differential Mode (green) Common Mode [12]

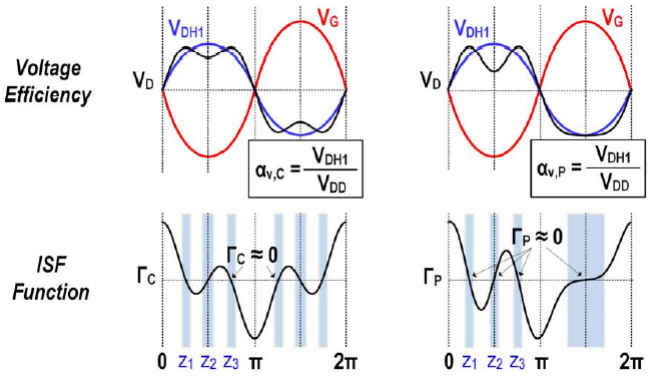


Figure 2.25: Top: Drain (black) and Gate (red) Voltage waveforms of a Class F_3 (left) and Class F_{234} (right) VCO
Bottom: Corresponding ISF functions [12]

3. CLASS F OSCILLATORS AT MMWAVE FREQUENCIES

As seen in Section 2, Class F oscillators provide a near square waveform at the output node, which is achieved by a 4th order tank that results in fundamental and third harmonics components to get added *in the right proportion.*

3.1 Effect of f_T

As the frequency increases, the harmonic content of the drain current diminishes. At mmwave frequencies, 3rd harmonic can be close to or beyond the f_T (transfer frequency) of the MOSFET. f_T is the frequency where the current gain of the MOSFET becomes unity. It is determined by the process, type of transistor and the layout.

To show this effect, Figures 3.1a - 3.1c compare the harmonic content of drain current of a cross-coupled Class B VCO at 7GHz and 24GHz respectively.

For this reason, the third harmonic of current needs to be enhanced by a higher value than the fundamental. This differs from the Class F_3 structure originally discussed in [4], which claims that the tank peak at third harmonic needs to be one third of the fundamental peak. The ClassF_{234} topology discussed in Chapter 2 implements such a tank. We understand here, that such a tank is not a choice but a necessity at mmWave frequencies.

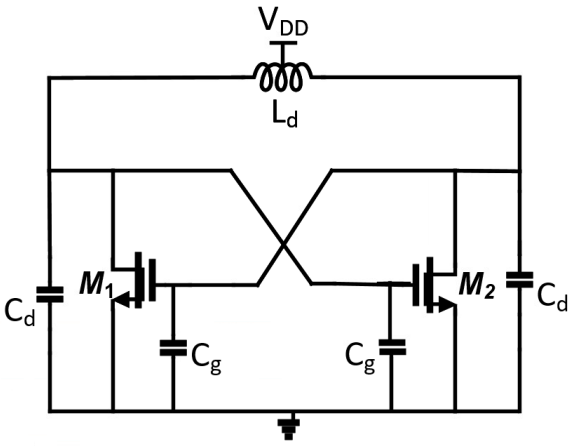
3.2 Tank analysis

The Class F topology is shown the Figure 3.2. The equivalent circuits for tank analysis are shown in Figure 3.3

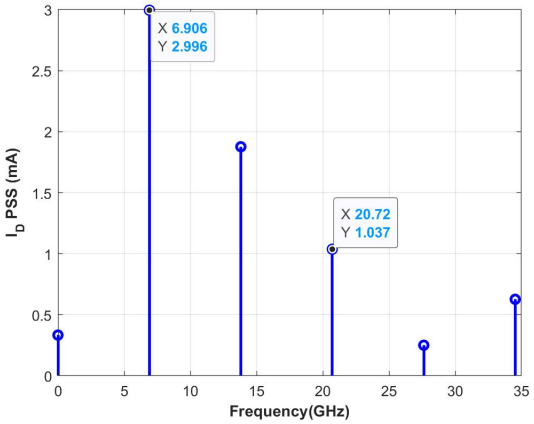
3.2.1 C_{gd} translation

Due to the presence of an LC resonator between the drain and gate nodes, C_{gd} of the transistor has a frequency dependent manifestation to the tank. We look at the value of C_{gd} in three different scenarios, which are useful in the subsequent analyses.

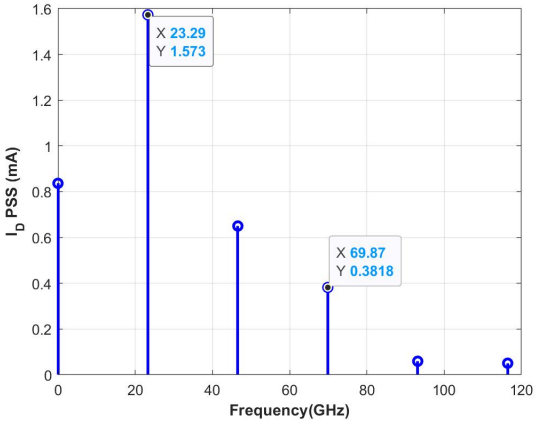
- When V_g = 0, the tank sees C_{gd}, C_m and C_d in parallel



(a) Class B oscillator



(b) 7GHz Class B oscillator



(c) 24GHz Class B oscillator

Figure 3.1: Effect of fT on the drain current of a Class B VCO

- In all other cases, we translate the intrinsic C_{gd} to a value $C_{gd'}$ that appears in parallel to C_m. Its value is frequency dependent, and it translates as derived below.

$$V_{gd} \propto \frac{1}{C_{gd}}$$
$$V_g - V_d \propto \frac{1}{C_{gd}}$$
$$V_g - V_{d\angle 180^\circ} \propto \frac{1}{C_{gd'}}$$

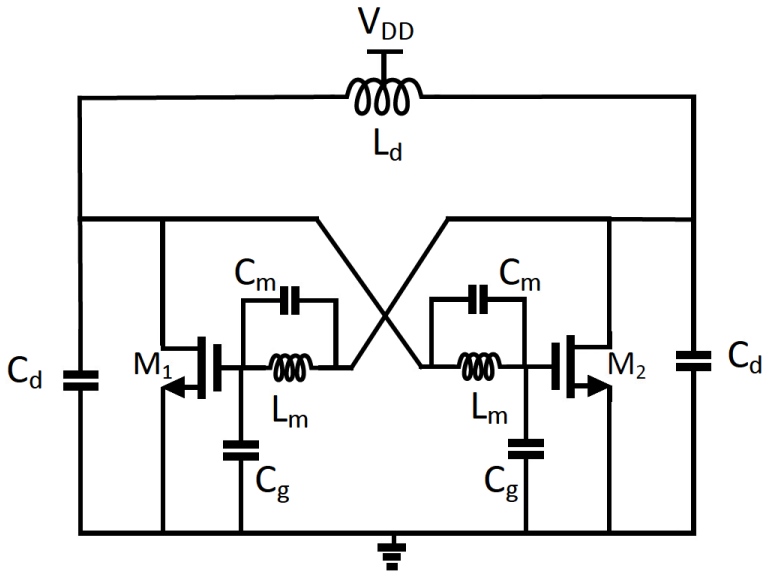
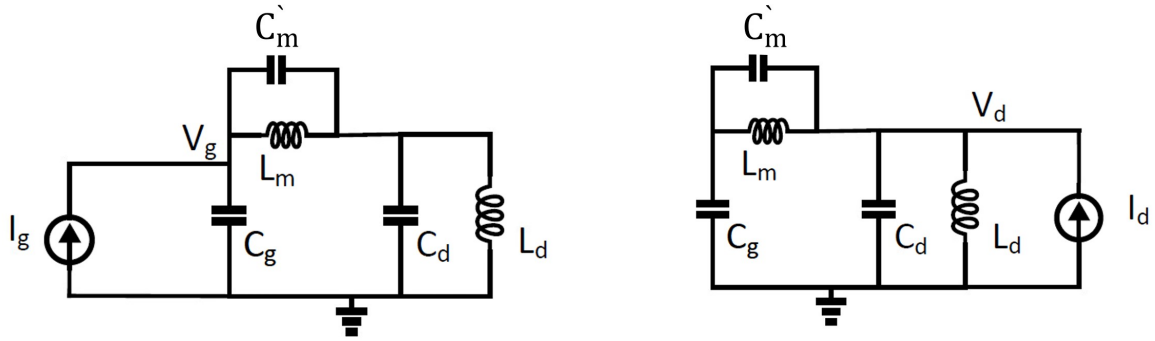


Figure 3.2: Class F topology with inductive multipliers



(a) Z_g (b) Z_d

Figure 3.3: Equivalent Differential half circuits for tank analysis

$$\implies C_{gd'} = C_{gd}\left(\frac{\frac{V_g}{V_d}-1}{\frac{V_g}{V_d}+1}\right) \tag{3.1}$$

The fraction $\frac{V_g}{V_d}$ can be derived as follows.

$$\frac{V_g}{V_d} = \left(\frac{L_m+L_d}{L_d}\right)\frac{s^2\frac{L_mL_d}{L_m+L_d}(C_{m'}+C_d)+1}{s^2L_mC_{m'}+1} \tag{3.2}$$

It is worth noting that, due to the frequency dependent nature of $\frac{V_g}{V_d}$, $C_{gd'}$ is a function of frequency, better represented as $C_{gd'}(s)$. As in Figure 3.3 and the subsequent derivations, $C_{m'}$ is used, where

$$C_{m'}(s) = C_m + C_{gd'}(s)$$

Next, we derive the gate and drain impedances Z_g and Z_d assuming *lossless elements*

$$\begin{aligned} Z_d = \frac{V_d}{I_d} &= \left(\, sL_d \, || \, \frac{1}{sC_d} \, \right) || \left((\frac{1}{sC_g}) + \left(\, sL_m \, || \, \frac{1}{sC_{m'}} \, \right) \right) \\ &= \frac{s(L_d)(s^2(L_m)(C_{m'} + C_g) + 1)}{s^4(L_m L_d C_g(C_{m'} + C_d) + L_m L_d C_{m'} C_d) + s^2(L_d(C_d + C_g) + L_m(C_g + C_{m'}) + 1} \\ &= \frac{s(L_d)\left((\frac{s}{\omega_{z_d}})^2 + 1\right)}{\left((\frac{s}{\omega_{p1}})^2 + 1\right)\left((\frac{s}{\omega_{p2}})^2 + 1\right)} \end{aligned} \tag{3.3}$$

$$\begin{aligned} Z_g = \frac{V_g}{I_g} &= \left(\left(\, sL_d \, || \, \frac{1}{sC_d} \, \right) + \left(\, sL_m \, || \, \frac{1}{sC_{m'}} \, \right) \right) \, || \, (\frac{1}{sC_g}) \\ &= \frac{s(L_d + L_m)(s^2(\frac{L_d L_m}{L_d + L_m})(C_{m'} + C_d) + 1)}{s^4(L_m L_d C_g(C_{m'} + C_d) + L_m L_d C_{m'} C_d) + s^2(L_d(C_d + C_g) + L_m(C_g + C_{m'}) + 1} \\ &= \frac{s(L_d + L_m)\left((\frac{s}{\omega_{z_g}})^2 + 1\right)}{\left((\frac{s}{\omega_{p1}})^2 + 1\right)\left((\frac{s}{\omega_{p2}})^2 + 1\right)} \end{aligned} \tag{3.4}$$

The fourth order polynomial in the denominators of Z_d and Z_g can be expressed as the product of two poles.

3.2.2 Choice of poles

3.2.2.1 Class F at the Gate

In the first approach, the zero of the drain impedance Z_d is made to coincide with one of the poles.

$$\omega_{z_d} = \omega_{p2} \tag{3.5}$$

For a quadratic equation of the form $ax^2 + bx + c = 0$, the product of roots is given by $\frac{c}{a}$

$$\begin{aligned}
&\implies \omega_{p1}^2\omega_{p2}^2 = \frac{1}{L_m L_d C_g (C_{m'} + C_d)} \\
&\implies \omega_{p1^2}\omega_{z_d}^2 = \frac{1}{L_m L_d C_g (C_{m'} + C_d)} \\
&\implies \omega_{p1}^2 * \frac{1}{L_m (C_{m'} + C_g)} = \frac{1}{L_m L_d C_g (C_{m'} + C_d)} \\
&\implies \omega_{p1} = \sqrt{\frac{1}{L_d (C_d + \frac{C_{m'} C_g}{C_{m'} + C_g})}}
\end{aligned} \tag{3.6}$$

With the above organization of ω_{p1} and ω_{p2}, the drain and gate impedances take the following form:

$$Z_g = \frac{s(L_d + L_m)(s^2(\frac{L_d L_m}{L_d + L_m})(C_{m'} + C_d) + 1)}{\left(s^2(L_d(C_d + \frac{C_{m'} C_g}{C_{m'} + C_g}) + 1)\right)(s^2(L_m(C_{m'} + C_g) + 1))} \tag{3.7}$$

$$Z_d = \frac{sL_d}{s^2(L_d(C_d + \frac{C_{m'} C_g}{C_{m'} + C_g})) + 1} \tag{3.8}$$

We see that the drain impedance resembles a *sinusoidal* resonator. The gate impedance, on the other hand, resembles a dual resonator, with two distinct poles and one distinct zero. Therefore, by appropriate choice of the passives, we can set $\omega_{p2} = 3\omega_{p1}$, achieving **a Class F waveform at the gate node.** The impedances at gate and drain are of such a choice of poles is shown in Figure 3.4

3.2.2.2 Class F at the Drain

In the second approach, the zero of the Gate impedance Z_g is made to coincide with one of the poles.

$$\omega_{z_g} = \omega_{p2} \tag{3.9}$$

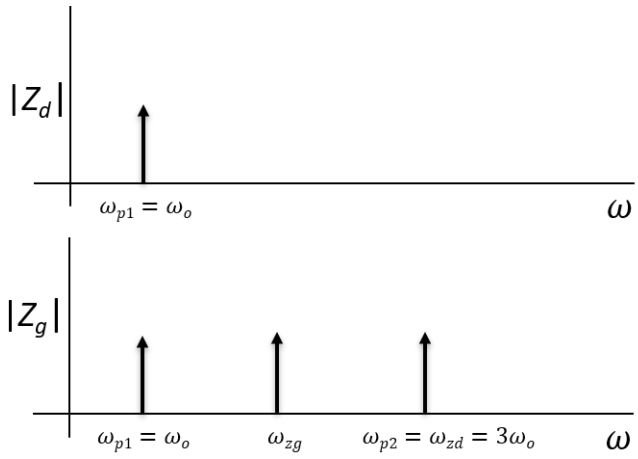


Figure 3.4: Poles and Zeros in the Drain (top) and Gate (bottom) impedances

For a quadratic equation of the form $ax^2 + bx + c = 0$, the product of roots is given by $\frac{c}{a}$

$$\begin{aligned}
&\implies \omega_{p1}^2\omega_{p2}^2 = \frac{1}{L_m L_d C_g (C_{m'} + C_d)} \\
&\implies \omega_{p1}^2\omega_{z_g}^2 = \frac{1}{L_m L_d C_g (C_{m'} + C_d)} \\
&\implies \omega_{p1}^2 * \frac{1}{\frac{L_d L_m}{L_d + L_m}(C_{m'} + C_d)} = \frac{1}{L_m L_d C_g (C_{m'} + C_d)} \\
&\implies \omega_{p1} = \sqrt{\frac{1}{(L_d + L_m)(C_g + \frac{C_{m'} C_d}{C_{m'} + C_d})}}
\end{aligned} \tag{3.10}$$

With the above organization of ω_{p1} and ω_{p2}, the drain and gate impedances take the following form:

$$Z_g = \frac{s(L_d + L_m)}{s^2((L_d + L_m)(C_g + \frac{C_{m'} C_d}{C_{m'} + C_d})) + 1} \tag{3.11}$$

$$Z_d = \frac{sL_d(s^2 L_m(C_{m'} + C_g) + 1)}{\left(s^2(L_d + L_m)(C_g + \frac{C_{m'} C_d}{C_{m'} + C_d}) + 1\right)\left(s^2 \frac{L_m L_d}{L_m + L_d}(C_{m'} + C_d) + 1\right)} \tag{3.12}$$

Here, we see that the gate impedance resembles a *sinusoidal* resonator. The drain impedance resembles a dual resonator, with two distinct poles and one distinct zero. Therefore, by appropriate choice of passives, we can set $\omega_{p2} = 3\omega_{p1}$, thus achieving **a Class F waveform at the drain node.**

The impedances at gate and drain are of such a choice of poles is shown in Figure 3.5

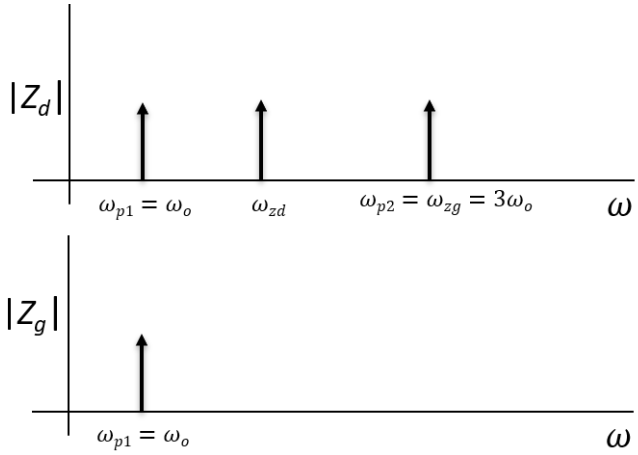


Figure 3.5: Poles and zeros in the drain (top) and gate (bottom) impedances

3.2.2.3 Advantages of Class F at Drain

Going forward, we will discuss the topology with Class F at the drain for the following advantages that it provides:

- **Noise Contribution:** Transistor thermal noise current flows from drain to source. Designing the drain waveform for ideal ISF will reduce this noise contribution
- **Design Reliability:** It is seen in Section 3.3 that peak at ω_{p1} for the sinusoidal resonator is higher than that of the Class F resonator. High peak-peak swings are better suited for the Gate node than the Drain node, due to the presence of oxide layer. Thus the topology with Class F at drain and sinusoidal at gate is better for design reliability.
- **Layout feasibility:** It is worth noting that for the Class F at gate structure, $\omega_{p1}(\equiv f_o)$ is determined by L_d and $\omega_{p2}(\equiv 3f_o)$ is determined by L_m. For the Class F at drain structure, $\omega_{p1}(\equiv f_o)$ is determined by the *series* combination of L_d and L_m, while $\omega_{p2}(\equiv 3f_o)$ is determined by the *parallel* combination of L_d and L_m. This aids in the choice of passive and facilitates a more feasible layout, as seen later in Chapter 5

3.2.3 Quality factor analysis

In this section, we analyse how the losses in the passive elements affect the effective quality factor of the tank. Quality factor of a passive element is defined as below.

$$quality\_factor(Q) = \frac{Im\{Z\}}{Re\{Z\}} \tag{3.13}$$

First, we look at the effective quality factors at each of the pole frequencies, namely $\omega_{p1} = \omega_o$ and $\omega_{p2} = 3\omega_o$. Figure 3.6 shows the way the passives interact to resonate at each of these frequencies, where $R_{s_{L_x}}$ and $R_{s_{C_x}}$ are the losses in the corresponding inductors and capactiors respectively. Using Equation 3.2.3, we define quality factor of individual passive elements as below.

$$Q_{C_x} = \frac{1}{\omega C_x R_{C_x}}$$
$$Q_{L_x} = \frac{\omega L_x}{R_{L_x}}$$

Assuming L_m = nL_d, C_g = mC_d and $C_{m'}$ = pC_d, $r = \frac{m(p+1)}{p}$, $C_{gd'}$ = tC_m the effective quality factors are derived as shown below.

$$Q_{\omega_o} = \left(\frac{nQ_{L_d}{}^{1} + Q_{L_m}}{(n+1)Q_{L_d}Q_{L_m}} + \frac{Q_{C_g} + r(\frac{Q_{C_d}+pQ_{C_{m'}}}{(p+1)Q_{C_d}Q_{C_{m'}}})}{(r+1)Q_{C_g}\frac{Q_{C_d}+pQ_{C_{m'}}}{(p+1)Q_{C_d}Q_{C_{m'}}}} \right)^{-1} \tag{3.14}$$

$$Q_{3\omega_o} = \left(\frac{Q_{L_d} + nQ_{L_m}}{(n+1)Q_{L_d}Q_{L_m}} + \frac{Q_{C_{m'}} + pQ_{C_d}}{(p+1)Q_{C_{m'}}Q_{C_d}} \right) \tag{3.15}$$

[1] Q for all elements is extracted from EM simulation as per Equation 3.2.3

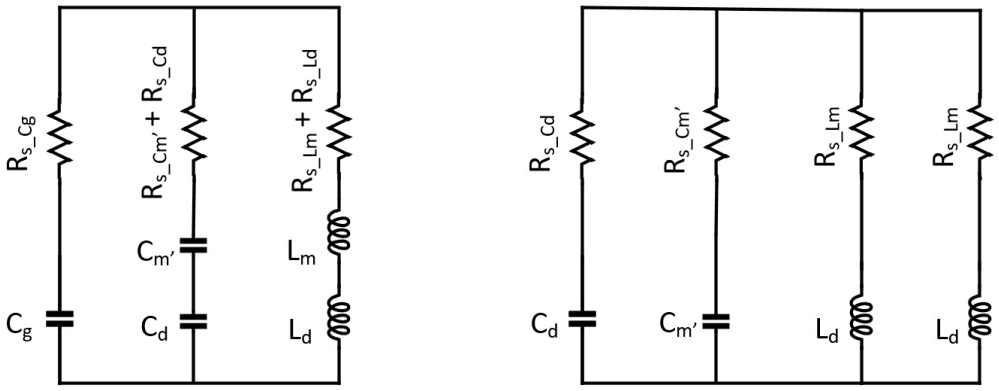


Figure 3.6: Resonator circuits with corresponding passive losses: (left) at gate and drain, for $\omega = \omega_o$ (right) at drain, for $\omega = 3\omega_o$

where

$$Q_{C_{m'}} = \frac{Q_{C_{gd}} + tQ_{C_m}}{(t+1)Q_{C_{gd}}Q_{C_m}}$$

Going by the discussion in Section 3.2.1, t is different for ω_o and $3\omega_o$.

3.2.3.1 Impedance peaks

For calculating the peak values of the gate and drain impedances, it is worth noting that, for a single pole LC resonator with inductance of L and capacitance of C, the impedance in the presence of losses transforms as below at for frequencies close to resonance.

$$\begin{aligned} Z_{lossless}(\omega) &= \frac{sL}{s^2LC+1} \\ Z_{lossy}(\omega_o \pm \delta\omega) &= \frac{sL}{s^2LC + \frac{1}{Q_{eff}}(\frac{s}{\omega_o}) + 1} \\ R_{p|\omega_o \pm \delta\omega)} &\simeq Z_{lossy}(\omega_o) = \omega_o L Q_{eff} \end{aligned} \tag{3.16}$$

where Q_eff is the effective quality factor of the resonator, which can be derived as discussed in the beginning of Section 3.2.3

Following this, the resonator shown on the left of Figure 3.6 transforms to a loss R_g given

below.

$$R_{g|\omega_o} = \omega_o(L_d + L_m)Q_{\omega_o} \tag{3.17}$$

The drain impedance comprises of two poles ω_{p1} and ω_{p2}, intended at ω_o and $3\omega_o$ respectively, accompanied by one zero, intended to be in between the two poles. To calculate the peak at ω_o, the zero and $3\omega_o$ resonators are assumed lossless. While computing the peak at $3\omega_o$, the zero and ω_o resonators are assumed lossless. Since the resonator contribute negligible losses out of their respective bands, this is a reasonable approximation that simplifies the calculation. For calculating the peak at ω_o, we rearrange Z_d as below.

$$Z_d = \frac{L_d}{L_d + L_m} * \left(\frac{s(L_d + L_m)}{s^2(L_d + L_m)(C_g + \frac{C_{m'}C_d}{C_{m'}+C_d}) + 1} \right) * \left(\frac{s^2 L_m(C_{m'} + C_g) + 1}{s^2 \frac{L_m L_d}{L_m + L_d}(C_{m'} + C_d) + 1} \right)$$

Using the analysis in Equation 3.16,

$$\begin{aligned} R_{d|\omega_o} &= \frac{L_d}{L_d + L_m} * (\omega_o(L_d + L_m)Q_{\omega_o}) * \left(\frac{1 - \frac{\omega_o^2}{\omega_z^2}}{1 - \frac{\omega_o^2}{9\omega_o^2}} \right) \\ \implies Z_{d|\omega_o} &= \omega_o(L_d)Q_{\omega_o} \left(\frac{1 - \frac{\omega_o^2}{\omega_z^2}}{1 - \frac{\omega_o^2}{9\omega_o^2}} \right) \\ \implies R_{d|\omega_o} &= \frac{9\omega_o(L_d)Q_{\omega_o}(1 - \frac{\omega_o^2}{\omega_z^2})}{8} \end{aligned} \tag{3.18}$$

Similarly, for calculating peak at $3\omega_o$, we rearrange Z_d as below.

$$\begin{aligned} Z_d &= \frac{L_d + L_m}{L_m} * \left(\frac{s\frac{L_d L_m}{L_d + L_m}}{s^2 \frac{L_m L_d}{L_m + L_d}(C_{m'} + C_d) + 1} \right) * \left(\frac{s^2 L_m(C_{m'} + C_g) + 1}{s^2(L_d + L_m)(C_g + \frac{C_{m'}C_d}{C_{m'}+C_d}) + 1} \right) \\ \implies R_{d|3\omega_o} &= \frac{L_d + L_m}{L_m} * (3\omega_o \frac{L_d L_m}{L_d + L_m} Q_{3\omega_o}) * \left(\frac{1 - \frac{9\omega_o^2}{\omega_z^2}}{1 - \frac{9\omega_o^2}{\omega_o^2}} \right) \\ \implies R_{d|3\omega_o} &= \frac{3\omega_o L_d Q_{3\omega_o}(\frac{9\omega_o^2}{\omega_z^2} - 1)}{8} \end{aligned} \tag{3.19}$$

The above equations show that the position of ω_z determines the heights of the two peaks in

Z_d. For example, if we intend $3\omega_o$ to be at least 2 times ω_o peak,

$$Z_{d|3\omega_o} \geq 2 * Z_{d|\omega_o}$$

$$\left(\frac{3\omega_o L_d Q_{3\omega_o}(\frac{9\omega_o^2}{\omega_z^2} - 1)}{8}\right) \geq 2\left(\frac{9\omega_o(L_d)Q_{\omega_o}(1 - \frac{\omega_o^2}{\omega_z^2})}{8}\right)$$

Assuming the quality factors of the passives stay relatively constant across the frequency, $Q_{\omega_o} \simeq Q_{3\omega_o}$ [2]

$$\implies \frac{\omega_o^2}{\omega_z^2} \geq \frac{7}{15} \implies \omega_z \leq 1.46\omega_o \tag{3.20}$$

Figure 3.7 shows a visualization of the drain and gate impedances with losses considered based on the derivations discussed above.

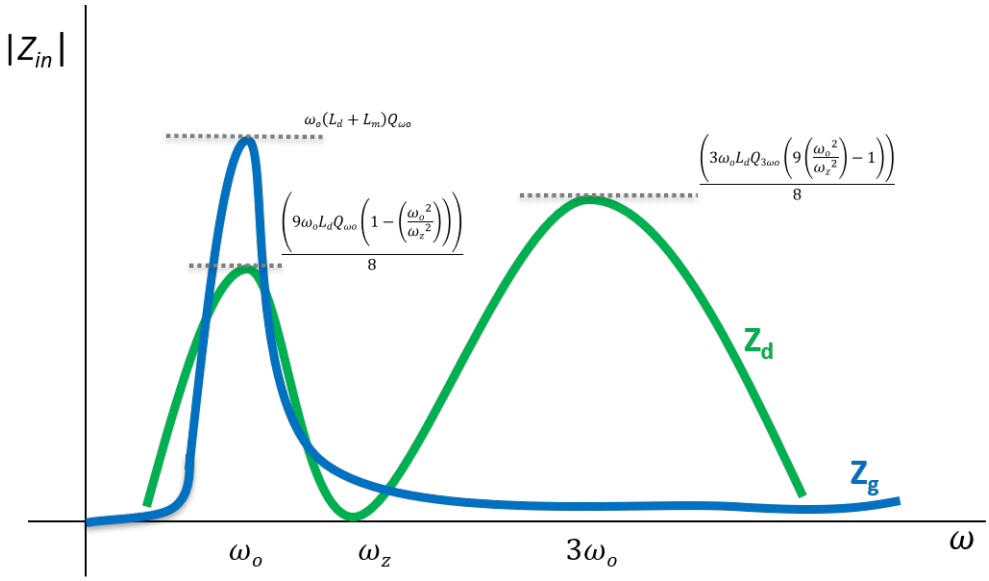


Figure 3.7: Visualizing drain (green) and gate (green) impedances

[2]This is only an approximation to enable design intuition. Quality factors vary across frequency depending on the implementation

3.2.4 Start-up condition

To derive the start-up condition, we use Barkhausen stability criterion stating that the magnitude of closed loop gain should be greater than unity, while the net phase change should be zero (or 360) degrees. This is stated below.

$$\begin{aligned} |H(s)|_{|\omega_o} &\geq 1 \\ \angle H(s)_{|\omega_o} &= 0^\circ \; or \; 360^\circ \end{aligned} \tag{3.21}$$

For the Class F circuit, the loop is cut at the gate as shown in Figure 3.8 calculating the loop gain as below.

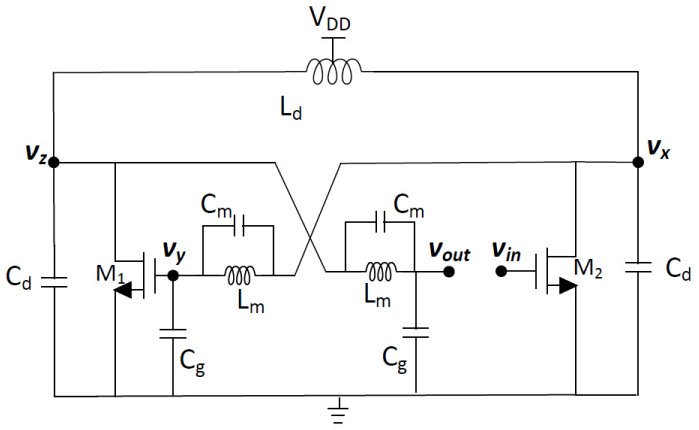


Figure 3.8: Circuit to calculate closed loop gain of the oscillator

$$
\begin{aligned}
v_x &= -g_m v_{in} Z_d \\
v_y &= -g_m v_{in} Z_d \frac{v_g}{v_d} \\
v_z &= g_m^2 v_{in} Z_d^2 \frac{v_g}{v_d} \\
v_{out} &= \left(g_m Z_d \frac{v_g}{v_d} \right)^2 v_{in} \\
\implies \frac{v_{out}}{v_{in}} &= H(s) = \left(g_m Z_d \frac{v_g}{v_d} \right)^2
\end{aligned}
\tag{3.22}
$$

Substituting Z_d and $\frac{V_g}{V_d}$ from Equations 3.2 and 3.12,

$$
\begin{aligned}
& H(s)|\omega_o > 1 \\
\implies & (g_m R_{p'})^2 > 1 \\
where\ & R_{p'} = \omega_o (L_d + L_m) Q_{\omega_o} \frac{(1 - \omega_{fo|even}^2 L_m C_m)}{(1 - \omega_{fo|even}^2 L_m (C_m + C_g))}
\end{aligned}
\tag{3.23}
$$

A Class B oscillator at the same frequency would exhibit a parallel resistance of $\omega_o(L_d + L_m)Q_{\omega_o}$. Therefore, we see from equation 3.23 that the multiplying inductors of the Class F oscillator boost the equivalent parallel resistance by the factor $\frac{(1-\omega_{fo|even}^2 L_m C_m)}{(1-\omega_{fo|even}^2 L_m (C_m+C_g))}$. Equivalently, it can be interpreted that the G_m of the cross-coupled pair gets boosted by the same factor.

$$
G_{m|ClassF} = G_{m|ClassB} \frac{(1 - \omega_{fo|even}^2 L_m C_m)}{(1 - \omega_{fo|even}^2 L_m (C_m + C_g))} \tag{3.24}
$$

Usually, the start-up condition is designed with considerable margin, as to ensure reliable oscillations across PVT variations.

$$
G_m > \frac{4}{R_{p'}} \tag{3.25}
$$

It is also worth noting that, since $\frac{V_g}{V_d}|_{3\omega_o} = 0$, accidental oscillations at $3\omega_o$ are avoided by the

mere choice of architecture.

3.3 Design Procedure

In this section, we discuss the design procedure for a **stand-alone** Class F VCO at mmWave frequencies. Since the parasitics from the g_m devices is comparable to the desired fixed cap, the passive selection is iterative in nature. The following procedure is suggested:

- Based on the desired tuning range, an external C_g is chosen. Since capacitance array and varactor implementations introduce significant fixed cap, it is suggested to choose C_g to be 20-30 times C_{gs} introduced by a minimum length, minimum width transistor. For initial estimation, the effect of C_{gd} is neglected.

- Use $C_d = C_{dd_{min}}$[3], $C_g = 25 * C_{g_{min}}$[4], $\omega_o = 2\pi f_o$, $\omega_z = 1.46\omega_o$ (as per Equation 3.20)

$$\omega_o^2 = \frac{1}{(L_d + L_m)(C_g + \frac{C_m C_d}{C_m + C_d})} \tag{3.26}$$

$$9\omega_o^2 = \frac{1}{\frac{L_d L_m}{L_d + L_m}(C_m + C_d)} \tag{3.27}$$

$$\omega_z = \frac{1}{L_m(C_m + C_g)} \tag{3.28}$$

  Using Equations 3.26, 3.27 and 3.28, the three unknowns L_d, L_m and C_m are calculated

- The quality factors for all the passives involved can then be estimated/simulated. Using these in Equation 3.14, $Q_{\omega o}$ is computed. This result is utilized in Equation 3.25, to calculate the required g_m for the transistors. The transistors are sized to provide the desired g_m. Once the sizes of the transistors are known, the C_{gd} introduced by them is known. This is used to compute $C_{m'}$ as discussed in Section 3.2.1, which is then used in Equations 3.26, 3.27,3.28 to readjust the passive values. The effect of parasitic C_{gd} can now be considered as per the discussion in Section 3.2.1.

[3]Depicts the total parasitic drain capacitance of the chosen transistor at its minimum size
[4]Depicts the total parasitic gate-source capacitance of the chosen transistor at its minimum size

As an example, the circuit in Figure 3.2 was implemented following the above procedure and simulated in Cadence Virtuoso using 22nm FDSOI process by Global foundaries. For a VCO with $f_o = 40GHz$, following the steps mentioned above, $C_g = 150fF$, $C_m = 20fF$, $L_m = 100pH$, $L_d = 60pH$, $g_m = 18m\Omega^{-1}$ were computed. Figure **??** shows the impedance curves and the corresponding voltage waveforms. As seen, the drain waveform emulates a square wave. Figure 3.11 shows the phase noise profile of the oscillator.

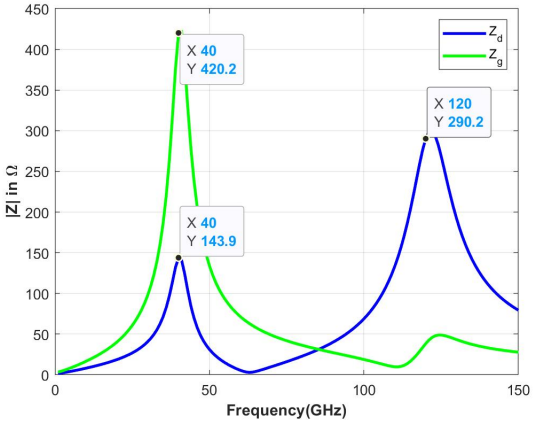


Figure 3.9: Example design: drain impedance (blue), gate impedance (green)

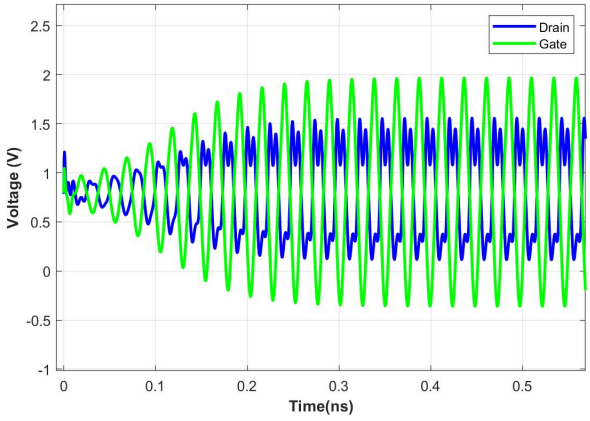


Figure 3.10: Example design: drain voltage (blue), gate voltage (green)

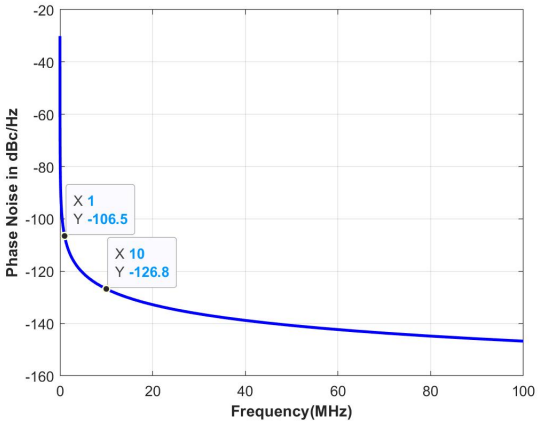


Figure 3.11: Example Design: Phase noise vs frequency offset

4. DUAL-BAND CLASS F VCO

As discussed in Chapter 1, the objective of this research is to design a dual-band VCO that behaves as a Class F oscillator in both bands. There Dual band structures in literature that rely on switching the passive elements [15](capacitors/inductors) to change the frequency band of operation. In [18], a active switching method is described, but it has two outputs, one for each of the bands. Since implementing a passive switch at mmWave frequencies is extremely lossy, leading to poor phase noise of the oscillator, we explore an active switching mechanism that was originally discussed in [14]. In this method, two oscillators are *inductively and capacitively* coupled. By choosing to oscillate the two resonators in or out of phase, the shared coupling passives can be made to behave differently. The result is that two distinct bands are formed, one each for the even and odd modes.

In [14], this topology is utilized to design a *wide-band* oscillator. This idea is extended to a QVCO in [6], where a wide-band quadrature VCO is designed using inductively and capacitvely coupled resonators. In [10], this active switching topology is extended to a Class F VCO, again, to obtain a wide-band low phase noise VCO operating in mid-band 5G frequency range. In this work, we extend the active switching topology to create a *dual band* Class F VCO for high band 5G frequencies. In the following sections, we first discuss the dual-mode resonator of [6], followed by the method to extend it to the Class F topology.

4.1 Dual-Mode Class B Oscillator

4.1.1 Method of Operation

Figure 4.1 shows the Class B dual-mode resonator operation discussed in [14]. For such a resonator, the impedance peaks resemble that shown in Figure 4.2. The frequency bands and the corresponding impedance peak values are as given below.

$$\omega_{even} = \frac{1}{\sqrt{(L+M)C}} \tag{4.1}$$

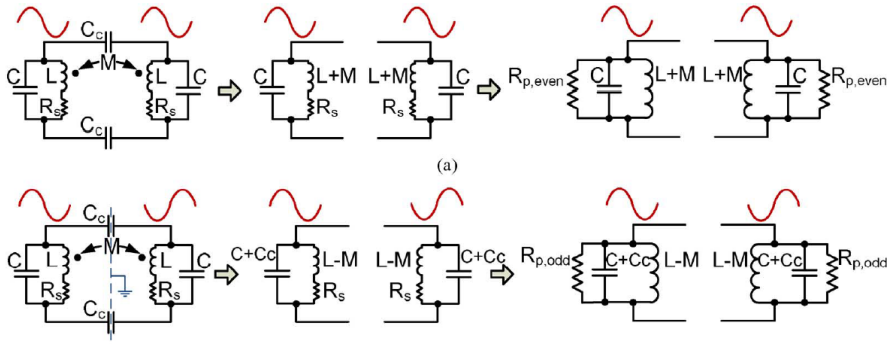


Figure 4.1: Dual-mode-based resonator operation [14]: (top) Even mode (bottom) Odd mode

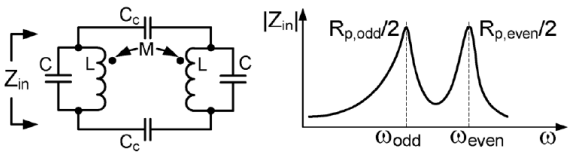


Figure 4.2: Dual-mode-based resonator impedance vs frequency [14]

$$\omega_{odd} = \frac{1}{\sqrt{(L-M)(C+C_c)}} \tag{4.2}$$

$$R_{p_{even}} = \frac{L+M}{C.R_s} \tag{4.3}$$

$$R_{p_{odd}} = \frac{L-M}{(C+C_c).R_s} \tag{4.4}$$

The mutual coupling inductance is preferred to be negative. This way, C_c and M will both aid in lower the frequency of operation of the lower band. This will also ensure similar R_p in both the bands, which is necessary to have balanced phase noise performance in both the bands. It is preferred to have identical resonators, as to maximize the output swing in both the oscillators, hence optimizing phase noise.

4.1.2 Mode switching network

The circuit shown in Figure 4.3 depicts the complete dual-mode resonator. The mode switching network is designed as a differential input - differential output cell, whose transconductance is

represented as G_{mc}. Two sets of this differential pair are connected to couple the oscillators in even and odd modes.

For odd mode operation, the plus/minus (P/M) voltages of one oscillator are converted to currents and pumped into the P/M nodes of the other oscillator. Since the differential pair introduces an inherent phase reversal, this ensures that the two resonators oscillate with opposite polarity, or *odd mode*. In this mode, the effective transconductance seen by the tank for odd mode signals is given by

$$G_{m_{effective|odd}} = -G_m - G_{mc} \tag{4.5}$$

The effective transconductance seen by the tank for even mode signals is given by

$$G_{m_{effective|even}} = -G_m + G_{mc} \tag{4.6}$$

i.e., when odd mode is selected, the mode selection circuitry *suppresses* even mode oscillations due to reduced negative transconductance.

Similarly, even mode operation is achieved when the P/M voltages of one oscillator are converted to currents and pumped into the M/P nodes of the other oscillator. Due to the inherent phase reversal by the differential pair, both the oscillators now oscillate with the same phase. In this mode, the effective transconductance seen by the tank is given by

$$G_{m_{effective|even}} = -G_m - G_{mc} \tag{4.7}$$

The effective transconductance seen by the tank for odd mode signals is given by

$$G_{m_{effective|odd}} = -G_m + G_{mc} \tag{4.8}$$

i.e., when even mode is selected, the mode selection circuitry *suppresses* odd mode oscillations due to reduced negative transconductance.

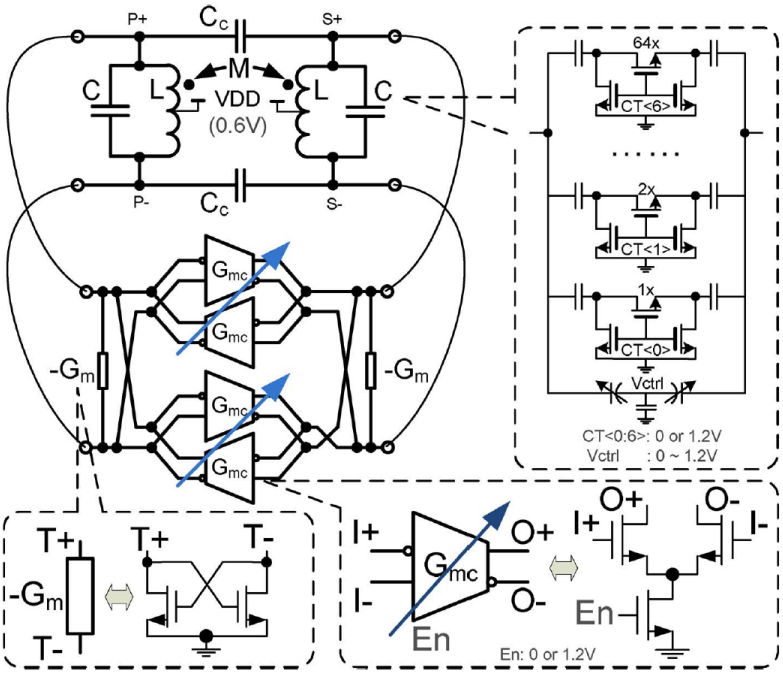


Figure 4.3: Complete dual-band Class B architecture from [14]

It is worth noting that topologically, G_{mc} pairs alone are enough to start oscillations. But the G_m stages are used to improve the tuning range, as the contribute lower parasitic capacitance for the same amount of negative transconductance. As seen, the parasitics from two G_{mc} units load the tank for the benefit of one unit of negative conductance given by $-G_{mc}$. On the other hand the parasitics of only one G_m unit loads the tank with the benefit of one unit of negative conductance, given by $-G_m$.

4.2 Dual Mode Class F Oscillator

For designing a dual-band Class F oscillator, the dual-mode idea from the previous section is used. In Chapter 3, the passives involved in choosing fundamental and third harmonics for a mmWave class F VCO are discussed. In this section, we look at how these passives are modified to obtain dual-band for both f_o and $3f_o$ frequencies.

4.2.1 Even mode operation

Figure 4.4 shows how the differential half circuit of Figure 3.3 transforms when the two oscillators are coupled in *even* mode. The corresponding resonant frequencies are hence transformed as below.

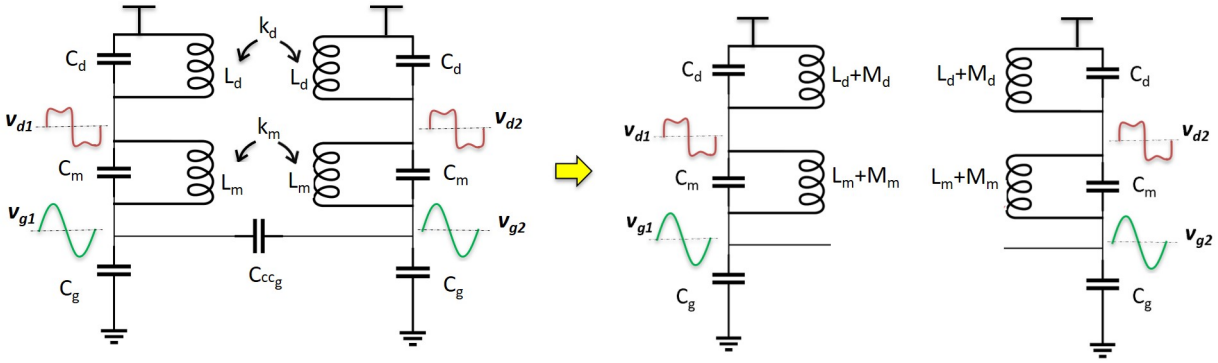


Figure 4.4: Differential passive half circuit: Transformation in even mode

$$\omega_{f_o|even} = \frac{1}{\sqrt{(L_d + M_d \ + \ L_m + M_m)(C_g + \frac{C_{m'}C_d}{C_{m'}+C_d})}}$$

where

$$M_m = k_m.L_m$$

$$M_d = k_d.L_d$$

$$\implies \omega_{f_o|even} = \frac{1}{\sqrt{(L_d(1+k_d) + L_m(1+k_m))(C_g + \frac{C_{m'}C_d}{C_{m'}+C_d})}} \tag{4.9}$$

Similarly, the third harmonic frequency transforms as below.

$$\omega_{3f_o|even} = \frac{1}{\sqrt{\frac{L_m(1+k_m)L_d(1+k_d)}{L_m(1+k_m) \ + \ L_d(1+k_d)}(C_{m'} + C_d)}} \tag{4.10}$$

The zero frequency that determines the peak value of Z_d at the 3rd harmonic, is a critical design parameter, as discussed in section 3.2.3. The zero frequency of the proposed structure transforms as below in the even mode.

$$\omega_{z|even} = \frac{1}{\sqrt{(L_m + M_m)(C_{m'} + C_g)}}$$

$$\implies \omega_{z|even} = \frac{1}{\sqrt{L_m(1 + k_m)(C_{m'} + C_g)}} \tag{4.11}$$

4.2.2 Odd mode operation

Figure 4.5 shows how the differential half circuit of Figure 3.3 transforms in when excited in the *odd* mode. The corresponding resonant frequencies are transformed as derived below.

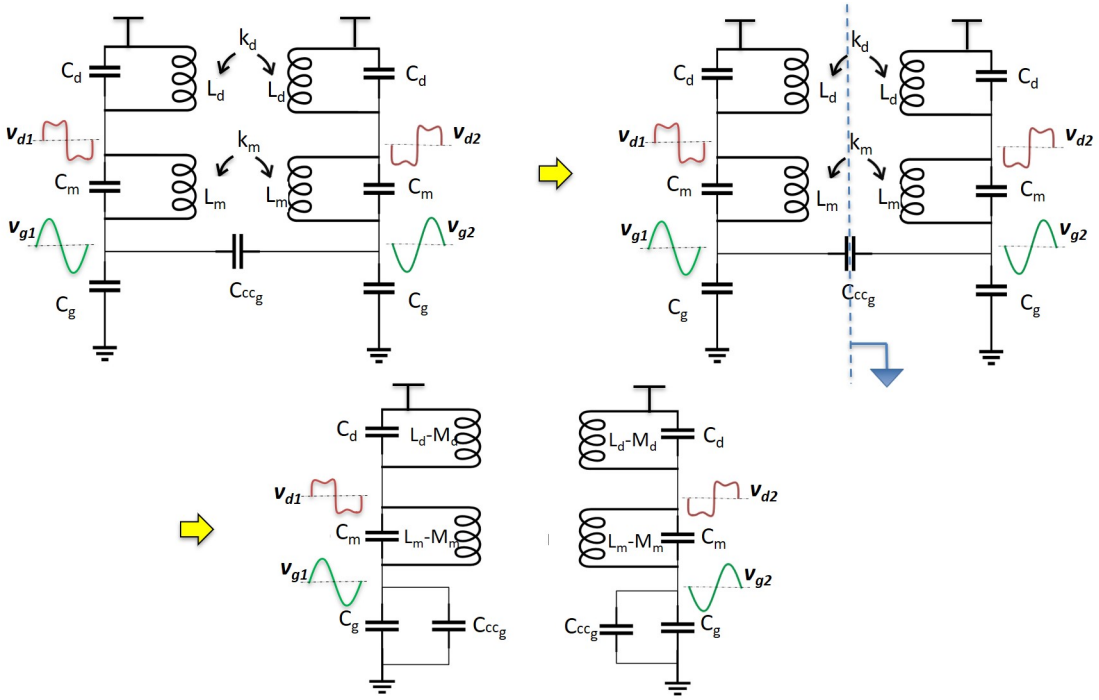


Figure 4.5: Differential passive half circuit: Transformation in odd mode

$$\omega_{f_o|odd} = \frac{1}{\sqrt{(L_d - M_d \ + \ L_m - M_m)(C_g + C_{cc_g} + \frac{C_{m'}C_d}{C_{m'}+C_d})}}$$

Letting C_{cc_g} = αC_g,

$$\implies \omega_{f_o|odd} = \frac{1}{\sqrt{(L_d(1-k_d) \ + \ L_m(1-k_m))(C_g(1+\alpha) \ + \ \frac{C_{m'}C_d}{C_{m'}+C_d})}} \tag{4.12}$$

Similarly, the third harmonic frequency transforms as below.

$$\omega_{3f_o|odd} = \frac{1}{\sqrt{\frac{L_m(1-k_m)L_d(1-k_d)}{L_m(1-k_m) \ + \ L_d(1-k_d)}(C_{m'} + C_d)}} \tag{4.13}$$

The zero frequency transforms as below for odd mode excitation.

$$\omega_{z|odd} = \frac{1}{\sqrt{(L_m - M_m)(C_{m'} + C_g + C_{cc_g})}}$$

$$\implies \omega_{z|odd} = \frac{1}{\sqrt{L_m(1-k_m)(C_{m'} + C_g(1+\alpha))}} \tag{4.14}$$

4.2.3 Choice of coupling factors

In this section we derive equations for the coupling factors k_m, k_d and α. Dividing Equation 4.9 by Equation 4.12,

$$\frac{\omega_{fo|even}}{\omega_{fo|odd}}^{1} = \sqrt{\frac{(1-k_d)(1-k_m)(1+\alpha)}{(1+k_d)(1+k_m)}} \tag{4.15}$$

$$\frac{\omega_{3fo|even}}{\omega_{3fo|odd}} = \sqrt{\frac{L_m(1+k_m) + L_d(1+k_d)}{L_m(1-k_m) + L_d(1-k_m)}} \tag{4.16}$$

$$\frac{\omega_{z|even}}{\omega_{z|odd}}^{2} = \sqrt{\frac{(1-k_m)(1+\alpha)}{(1+k_m)}} \tag{4.17}$$

[1] $\frac{C_{m'}C_d}{C_{m'}+C_d}$ is neglected in comparison to C_g

With the above three equations, the three unknown coupling coefficients k_m, k_d and α can be calculated. This is further discussed in Section 4.2.7, during the design process of the proposed oscillator.

4.2.4 Mode selection

The complete architecture of the proposed oscillator is shown in Figure 4.6. The mode selection circuitry is a differential pair that connects the P/M gate nodes of one Class F oscillator to the P/M (odd) or M/P (even) nodes of the other Class F oscillator. The differential pair introduces a negative G_m in addition to the negative G_m introduced by the core transistors.

Using Equations 4.5 - 4.8 in conjunction with Equation 3.24, we can analyze how the transconductance gets transformed for the proposed structure.

When even mode is excited, the negative resistance offered by the structure at $\omega_{fo|even}$ is given by Equation 4.18

$$G_{m|even} = -G_{m|core}\frac{(1-\omega_{fo|even}^2 L_m C_m)}{(1-\omega_{fo|even}^2 L_m (C_m + C_g))} - \frac{G_{m|coup}}{2} \tag{4.18}$$

At the same time, the odd mode is suppressed by the $G_{m|coup}$ as below

$$G_{m|odd} = -G_{m|core}\frac{(1-\omega_{fo|odd}^2 L_m C_m)}{(1-\omega_{fo|odd}^2 L_m (C_m + C_g))} + \frac{G_{m|coup}}{2}$$

Similarly, when odd mode is excited, the negative resistance offered by the structure at $\omega_{fo|odd}$ is given by Equation 4.19

$$G_{m|odd} = -G_{m|core}\frac{(1-\omega_{fo|odd}^2 L_m C_m)}{(1-\omega_{fo|odd}^2 L_m (C_m + C_g))} - \frac{G_{m|coup}}{2} \tag{4.19}$$

[2] $C_{m'}$ is neglected in comparison to C_g

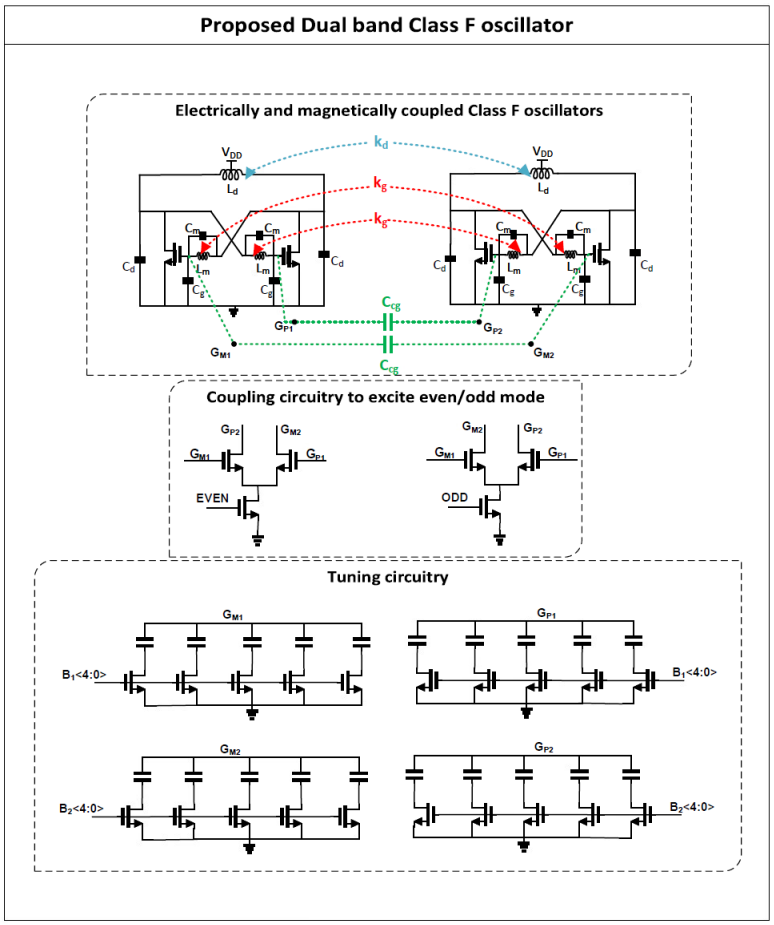


Figure 4.6: Proposed Dual-band Class F structure

At the same time, the even mode is suppressed by the $G_{m|coup}$ as below

$$G_{m|even} = -G_{m|core}\frac{(1-\omega_{fo|even}^2 L_m C_m)}{(1-\omega_{fo|even}^2 L_m(C_m+C_g))} + \frac{G_{m|coup}}{2}$$

4.2.5 Quality factor analysis

Figures 4.7 and 4.8 conceptualize the transformation in Z_d and Z_g when two identical ClassF_3 oscillators of Chapter 3 are coupled inductively and capacitively as discussed above. The equivalent parallel resistance that appears at the tank is derived from Equations 3.17 - 3.19 as below.

$$R_{g_{fo|even}} = \omega_{fo|even}(L_d(1-k_d) + L_m(1-k_m))Q_{\omega_{fo|even}} \tag{4.20}$$

$$R_{g_{fo|odd}} = \omega_{fo|odd}(L_d(1+k_d) + L_m(1+k_m))Q_{\omega_{fo|odd}} \tag{4.21}$$

$$R_{d_{fo|even}} = \frac{9\omega_{fo|even}L_d(1-k_d)Q_{\omega_{fo|even}}(1-\frac{\omega^2_{fo|even}}{\omega^2_{z|even}})}{8} \tag{4.22}$$

$$R_{d_{fo|odd}} = \frac{9\omega_{fo|odd}L_d(1+k_d)Q_{\omega_{fo|odd}}(1-\frac{\omega^2_{fo|odd}}{\omega^2_{z|odd}})}{8} \tag{4.23}$$

$$R_{d_{3fo|even}} = \frac{3\omega_{fo|even}L_d(1-k_d)Q_{\omega_{3fo|even}}(\frac{9\omega^2_{fo|even}}{\omega^2_{z|even}}-1)}{8} \tag{4.24}$$

$$R_{d_{3fo|odd}} = \frac{3\omega_{fo|odd}L_d(1+k_d)Q_{\omega_{3fo|odd}}(\frac{9\omega^2_{fo|odd}}{\omega^2_{z|odd}}-1)}{8} \tag{4.25}$$

4.2.6 Phase noise analysis

A major source of phase noise is the voltage equivalent of the noise source at R_p, given by $4kTR_p$, where R_p is given by $R_p(=\frac{\omega_o LQ}{R_s})$. This can be lowered by lowering the value of inductor, while maintaining the same Q. As the inductor value is lowered, it will be more and more challenging to design it for a good Q. For this reason, N-coupled oscillators are used. The coupling between these oscillators lowers the effective inductance, which reduces R_p for the same Q. The trade off here is power consumption. Coupling N identical oscillators achieves $10\log N$ phase noise improvement while increasing the power consumption by N times [8]. This implies that when compared to a stand-alone Class F designed with passives $L_d(1-k_m)$, $L_m(1-k_m)$, $C_g + C_{cc_g}$, C_d and C_m, the proposed architecture achieves 3dB better phase noise in the even band. Similarly, when compared to a stand-alone Class F designed with passives $L_d(1+k_m)$, $L_m(1+k_m)$, C_g, C_d and C_m, the proposed architecture achieves 3dB better phase noise in the odd band. On the other hand, for the same power consumption, the Class F design achieves 3dB better phase noise than it's Class B counterpart [4]. This is because the Γ_{rms} of a square wave is $\frac{1}{\sqrt{2}}$ times the Γ_{rms} of a sine wave. In conclusion, the proposed dual-band Class F structure provides 6dB better phase noise in each band, as compared to two single band Class B structures at the same frequencies.

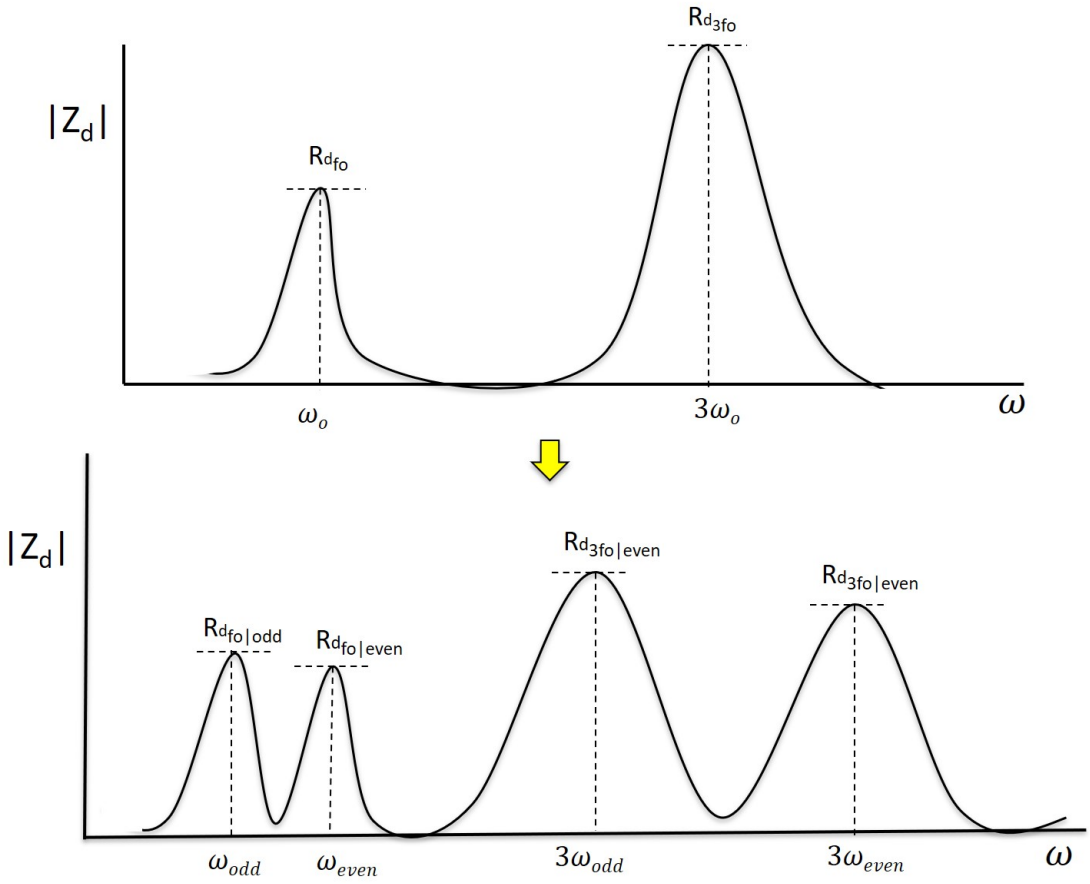


Figure 4.7: Visualizing drain impedance transformation from single-band Class F to dual-band Class F

4.2.7 Design procedure

The procedure mentioned in Section 3.3 elucidate the method to choose the L and C values. The equations in Section 4.2.3 explain how the additional coupling variables can be selected. Having theoretically covered all the variables, a step-by-step approach is proposed here to find passive element values for certain dual-band Class F VCO specs.

- Let the two required bands be centered around ω_{even} (low band) and ω_{odd} (high band)
- First we design passives L_d, L_m and C_m for a single band Class F. The frequency of band for this design is to be centered around ω_{SB}. How do we choose ω_{SB}? We know that mutual inductive coupling splits the band locations to ω_{even} and ω_{odd} by dividing ω_{SB} by

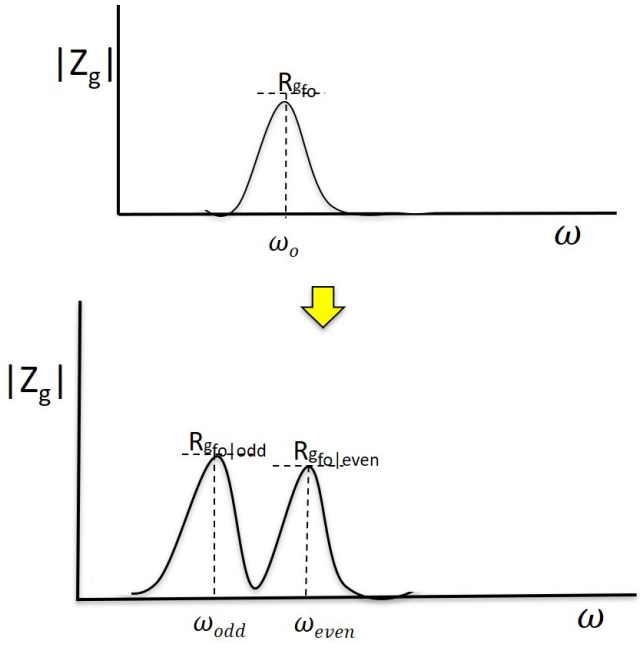


Figure 4.8: Visualizing gate impedance transformation from single-band Class F to dual-band Class F

$\sqrt{(1+k_x)}$ and $\sqrt{(1-k_x)}$. So if only inductive coupling were to be used, $\frac{1}{\omega_{even}^2}$, $\frac{1}{\omega_{SB}^2}$, $\frac{1}{\omega_{odd}^2}$ would make an arithmetic progression, with a common difference of k_x. But we also need to take care of the capacitive coupling effect. We know that C_{cc_g} manifests only in the odd mode. If $C_{cc_g} = \alpha C_g$, ω_{odd} would be shifted to $\frac{\omega_{odd}}{\sqrt{1+\alpha}}$. Hence, while choosing ω_{SB}, we need to compensate for this shift. So ω_{SB}^2 is calculated as the harmonic mean of ω_{even}^2 and $\omega_{odd}^2(1+\alpha)$.

$$\omega_{SB} = \frac{\omega_{even}\omega_{odd}\sqrt{1+\alpha}}{\sqrt{\omega_{even}^2 + \omega_{odd}^2(1+\alpha)}} \tag{4.26}$$

where $\alpha = 0.25$ is used, to reduce calculation complexity. We start with initial value and iterate as necessary. Another way to estimate α is discussed in Appendix A.

- Now that the frequency is known, the design procedure mentioned in Section 3.3 is followed to obtain L_m, L_d, C_m and C_g

- Now we have a Class F oscillator working at ω_{SB} that resembles the design in Figure 3.2, with drain and gate impedances resembling the *top* portions of Figures 4.7 and 4.8, respec-

tively

- Using the equations in Section 4.2.3, k_m,k_d and α can be calculated.
- Using these transformers and coupling capacitor, the design resembles that in Figure 4.6, with drain and gate impedances resembling the *bottom* portions of Figures 4.7 and 4.8, respectively

5.1 About FDSOI

To implement the proposed design, a 22nm FDSOI Global Foundaries process was used. FD-SOI stands for Fully-depleted Silicon on Insulator. An ultra thin layer of insulator called the buried oxide (BOX) is placed on the base silicon. On that, the channel is laid, which is a very thin silicon film. Due to presence of BOX, there is no need to add dopants to the channel, which is not the case for bulk CMOS processes. Hence the process is called 'full-depleted'. A cross-section view of a typical FDSOI transistor is shown in Figure 5.1 [1].

Since no doping is needed, this reduces the number of steps in fabrication process. More importantly, the variance in device parameters that rely on doping will now be eliminated. As a result, FDSOI transistor performance is closer to the average of the population. Additionally, for the same technology node, an FDSOI transistor has shorter channel length as compared to a bulk CMOS process. This allows for higher operating speeds, as electrons can travel faster. Other benefits of the process include lower gate leakage, lower short channel effects and reduced junction capacitances.

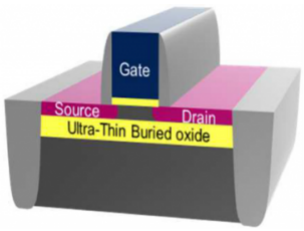


Figure 5.1: Cross section view of an FDSOI transistor [1]

5.1.1 Process features

Some of the process features and special devices that have been used in the current work are discussed in this section.

5.1.1.1 Back gate biasing

In bulk CMOS, the voltage on the bulk cannot exceed the source/drain voltage as it will cause the diode in between them to get forward biased. In FDSOI, due to the presence of the thin film of insulator, there bulk voltage can go much higher. The bulk hence acts as a *second gate*, also called back-gate. Due to this flexibility, the process allows for a *flip well* technology, in which NMOS transistors are placed in n-well and PMOS transistors are placed in a p-well. Due to this configuration, the flip-well/back-gate for these NMOS transistors can have a positive relative voltage on the Body (for PMOS transistors,negative relative voltage on the Body) which lowers V_{th}, leads to faster switching and higher drive capability, at the cost of higher power-consumption. This technique is called Forward Body Biasing (FBB). In a *regular well*, the PMOS transistors are placed in n-well and NMOS transistors are placed in p-well. Due to the SOI, the NMOS body can have a negative relative voltage (PMOS body can have a positive relative voltage). This effect increases the V_{th}, lowering the leakage and the power consumption. This technique is called Reverse Body Biasing (RBB). Figure 5.2 shows the distinction between a regular well and a flip well.

In this work, super-low V_{th} flip-well transistors are used. If the ISF is asymmetric, the flicker noise can be up-converted to the desired band. low threshold transistors exhibit lower flicker noise, reducing this up-conversion noise. Secondly, the back gate voltage allows to control the diode to substrate. This diode is used as a varactor to achieve continuous tuning, as discussed in Section 5.2.2.4.

5.1.1.2 Erase gate transistors

Erase gate transistors are used in memory cells, where high gate voltages are needed to program voltages. The 22nm FDSOI process provides a series of erase gate transistors with varying voltage

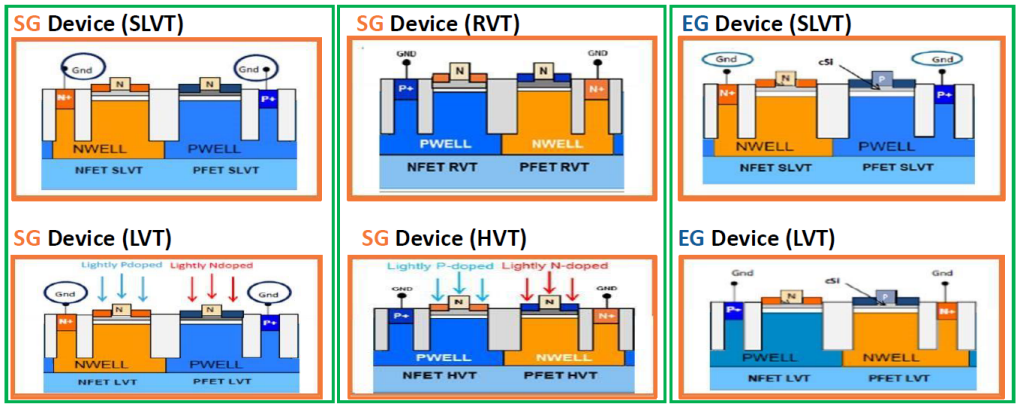


Figure 5.2: Transistor cross section view: (left) Flip-well (center) Regular well (right) Erase gate flip-well

ratings. In this design, since the gate node sees high voltage swings, erase gate transistors of channel length 70nm (eguslvtnfet_mmw) are used for the core transistors. This is because the swing at the drain of the core transistors is less compared to the gate. On the other hand, since the drain and gate nodes of the coupling transistors are connected to the gate nodes of the two cores, transistors with high drain voltage rating need to be used. For this reason, erase gate transistors with channel length of 150nm (egslvtnfet_mmw) are used for the coupling transistors. Due to lower flicker noise contribution, low-V_{th} (flip-well) versions of these erase-gate transistors are used in this design.

5.1.1.3 Process BEOL

The process offers a wide range of back-end-of-line metals. The stack-up is shown in Figure 5.3. As seen, there are two M_x layers, five C_x layers, one J_x layer, 2 Q_x layers, and one L_B ($2.8\mu m$) layer.

5.1.1.4 MOM capacitors

The PDK offers a wide range of MOM capacitors for different voltage ratings. Alternate polarity Metal-Oxide-Metal (APMOM) capacitors with good quality factor are available. For the current design, since low capacitor values are needed for the switch capacitor arrays, APMOM5V capacitors between layer 3 and layer 7 are used. These capacitors have wider vias leading to lower

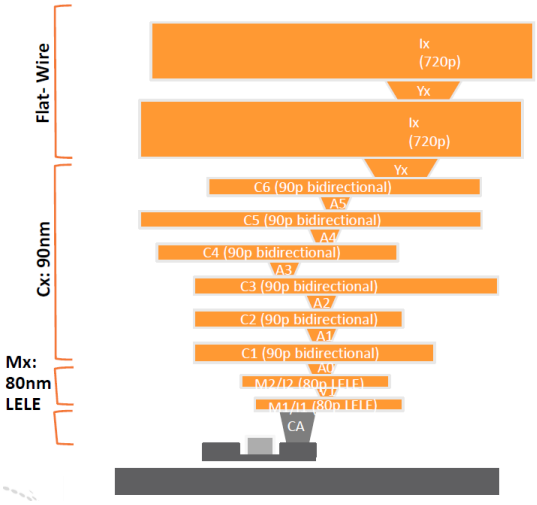


Figure 5.3: 22nm FDSOI BEOL visualization

resistance and better quality factor.

5.2 Proposed Design

For the proposed dual-band VCO design, we target the two high band 5G standard frequency bands. As per the standard, the bands are between 24.5GHz - 28.5GHz and 38.5GHz-42GHz. This translates to 15% of tuning range around 26GHz and 8.7% of Tuning range around 40GHz. Following the steps in Section **??**, the following tentative design parameters are calculated. $L_m = 110pH, L_d = 60pH, C_m = 30fF, C_g = 160fF, C_{cc_g} = 30fF, k_m = -0.3, k_d = -0.25$. If the Q is between 15-20 from 10GHz-130GHz, the active design is to be such that $G_{m|core} \geq 5mS, G_{m|coup} \geq 7.5mS$.

5.2.1 Passive design

5.2.1.1 Challenges in Passive design

For the proposed dual-band Class F oscillator, three transformers are needed to be designed. Following are the challenges in designing the passives:

- **Wideband design:** Since Class F design requires peaks at 3rd harmonics, the passives need to be wideband in nature. The individual primary and secondary inductances *and* the mutual

coupling factor need to be maintained over the band 20GHz-130GHz. Moreover, it is also desired to have a good quality factor in the entire band of interest.

- **Negative coupling factor:** A negative mutual coupling factor is needed between each set of transformers. An easy way to accomplish this is to have the coils face away from each other. Such a design would cause the two core transistors to be far from each other. But since the coupling G_{mc} cells and C_{cg} need to be placed in between the two cores, the coils *must* face the same direction. Hence, floorplan being the constraint, maintaining a *constant, low, negative* mutual coupling factor over the wide frequency band is a challenge

- **Shielding:** Since mmWave frequencies are targeted, the inductances are of small value. Due to this, the coils tend to be of relatively small sizes (eg: $60\mu m$ X $60\mu m$). This means that long routing lines can cause a significant change in the inductance value. Due to this issue, the transformers cannot be too far away. As a result, the mutual coupling between the transformers needs to be considered in the passive design process.

5.2.1.2 Transformer Design methodology

The wideband challenge is addressed by making sure to have a small form factor, This is necessary, as the capacitance to substrate can become signficant at mmWave frequencies and cause self resonance. Since the inductance value starts rising exponentially close to f_{SR}, it is good to design the f_{SR} sufficiently away from the desired band of operation.

The challenge of negative mutual coupling is addressed by having a big outer coil and a smaller inner coil. By designing the outer coil with wider and lower metal, and the inner coil with narrower and top-most metal, the inductances can be made reasonably close in value, while maintaining a low, negative mutual coupling. Ideally, we would want to have identical passives in both the Class F cores, as the peak-peak swings will be balanced, improving the phase noise. Following this approach, made it feasible to achieve a reasonable balance in passives between the Class F cores.

The shielding challenge was a relatively trickier issue. It was tackled by taking advantage of the fact that the drain node is common to both the load and multiplying transformers. So, by choosing

to have a common drain connection for the outer inductor, the shielding can be avoided. It also helps in balancing the mismatch in the cores. The final passive topology is shown in Figure 5.8

As seen in figure 5.4, the drain transformer can be designed as a symmetric transformer around $V_D D$. This will save the area and allow to design smaller form factor passive with a better quality factor. It is designed and simulated as shown in Figure 5.4. The design is laid out in ADS Momentum using 22nm FDSOI process profile and the transformer parameters are extracted as shown in Figure 5.5.

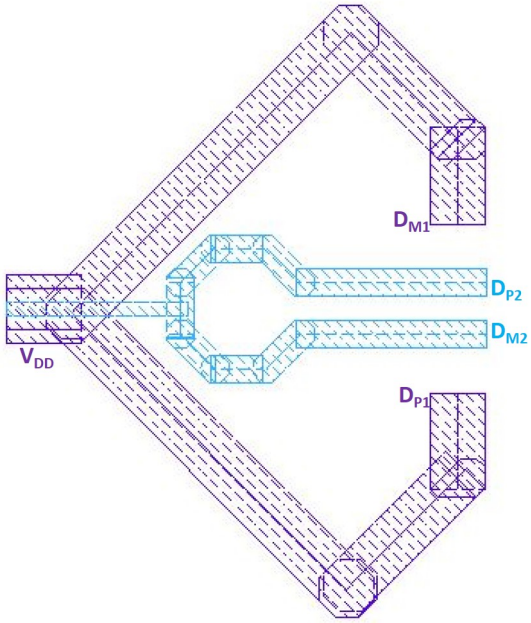


Figure 5.4: Layout of Symmetric drain transformer

The gate-drain transformer is designed as shown in Figure 5.6. The design is laid out in ADS Momentum using 22nm FDSOI process profile and the transformer parameters are extracted as shown in Figure 5.7.

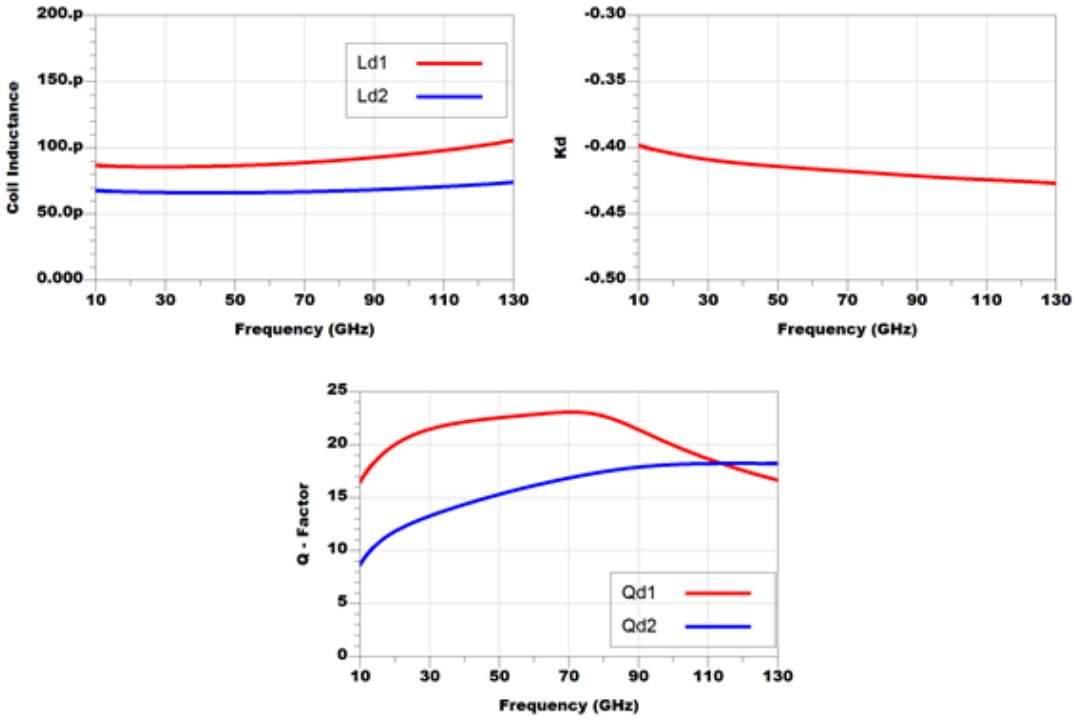


Figure 5.5: Symmetric drain transformer parameters (red)Outer coil (blue)inner coil (top left) Coil self inductances (top right) Coupling factor (bottom) Coil quality factors

5.2.2 Active design

5.2.2.1 Core design

The main focus for the active design is to achieve the best G_m and G_{mc} while introducing minimum fixed capacitance and flicker noise into the system. The eguslvtnfet_mmw_5t transistor is characterized for a trade-off between noise contribution and transconductance. Left axis of Figure 5.9 shows this integrated noise at 10KHz contributed by the core transistor, plotted for varying widths. To contrast, the transconductance offered is plotted on the right axis. ($\frac{W}{L} = \frac{19.2\mu m}{70nm}$) are used for the core, using four multipliers to reduce gate resistance. Each multiplier provides a $G_m = 5.5mS$, while consuming 4.5mA each.

To avoid the flicker noise upconversion from tail current source, the VCO is designed in a pseudo-differential fashion. Usually, for such a design, the slow-varying noise on the supply causes

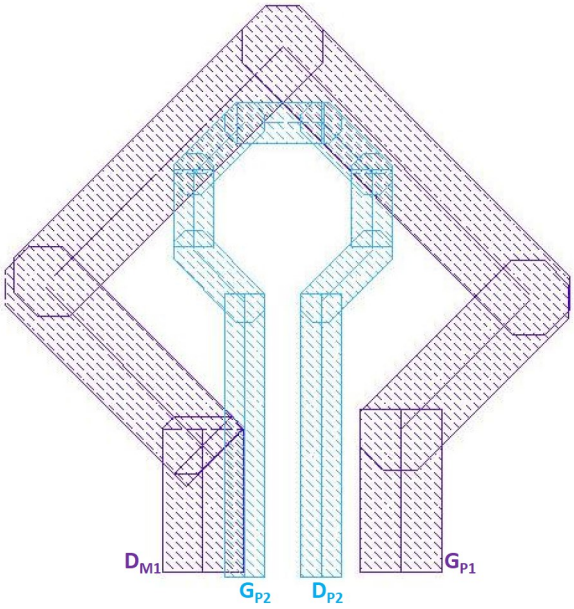


Figure 5.6: Layout of Gate to Drain transformer

frequency modulation in the presence of varactors (AM - PM conversion). Since the current design does not have varactors on the output node, this is still a safe choice.

The coupling cells are designed using egslvtnfet_mmw_5t transistors. For this, the current through the differential pair is varied (by varying the width tail transistor), while plotting g_m and integrated device noise at 10KHz for different widths of the core transistor, as shown in Figure 5.10. This helps in understanding the right bias point for lowest noise, while achieving optimal transconductance. From the graphs, $\frac{W}{L} = \frac{9.6\mu m}{150nm}$ is chosen for M_5. Two multipliers are used to reduce gate resistance. Each coupling transistor gives a $G_{mc} = 7.5mS$, biased at 1.2mA using a tail slvtnfet_mmw_5t transistor of $\frac{W}{L} = \frac{38.4\mu m}{20nm}$.

5.2.2.2 Tuning circuitry

For the calculation, a fixed $C_{g|fixed} = 90fF$ and $C_{g|var} = 60fF$ was used. So the fixed capacitance introduced by the switches in the cap array needs to be within 90fF. The switch transistor was chosen after careful simulation for on-resistance and off-capacitance resistance. Following are the features of the cap-array switches:

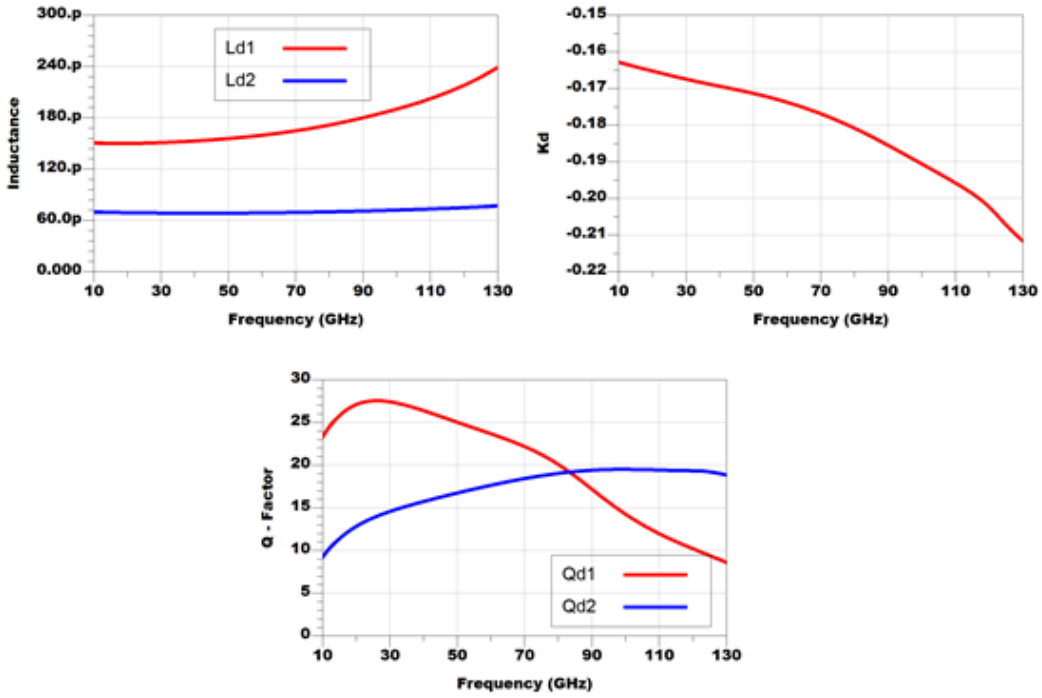


Figure 5.7: Gate to drain transformer parameters (red)Outer coil (blue)inner coil (top left) Coil self inductances (top right) Coupling factor (bottom) Coil quality factors

- **Single-ended:** The switches are designed to be single-ended. This is because the entired V_{gs} can be used to to turn the switch on with low resistance ($\propto \frac{K}{(V_{gs}-V_{th})}$).

- **Back-gate biasing:** By using flip-well transistors, the back-gate voltage is set to 2V (maximum) for best switching performance. This reduces the V_{th}, reducing the dc and ac resistance of the switch. Figure **??** illustrates this across different transistor widths.

- **Off capacitance:** Minimum length mm-wave transistors are used, which have the least parasitic capacitance in the pdk.

- **On-resistance:** The simulated on-resistance (ac) of an slvtnfet_mmw_5t transistor ($\frac{W}{L} = \frac{40\mu m}{20nm}$) was seen to be 8.5$\Omega$. For a fixed cap of 45fF, this resistance results in a Q $\simeq$ 11. This is the switch size chosen for the MSB capacitor.

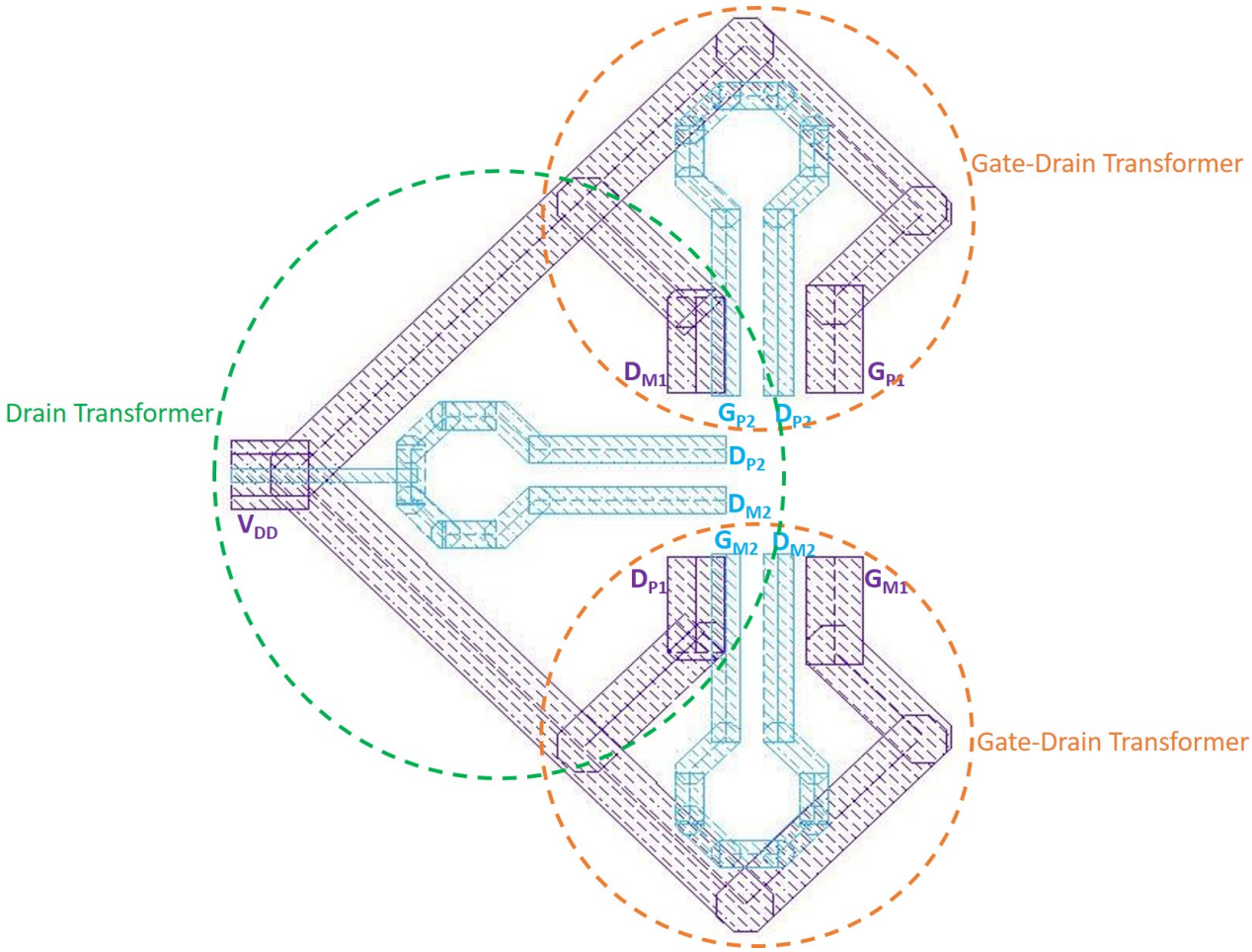


Figure 5.8: Final Class F Passive layout

5.2.2.3 Discrete tuning

As shown in 4.6, a 5 bit cap-array is designed. The cap-arrays are designed to 2 bit binary and 3 bit thermometric. To achieve the desired tuning range, entire MSB is not needed. So three-fourth of MSB is implemented using 3 thermometric arms instead. The switch sizes are scaled similar to the capacitance, to maintain linearity in tuning.

Four such cap arrays are placed at each of the gate nodes. The cap-arrays of each core are controlled separately. This allows to achieve a finer LSB size, as the cores can tolerate up to 15%-20% of mismatch in the passives without phase noise degradation [14]. As seen in the Class F tank equations of Section 3.3, the gate capacitance affects only the fundamental peak. Since the third

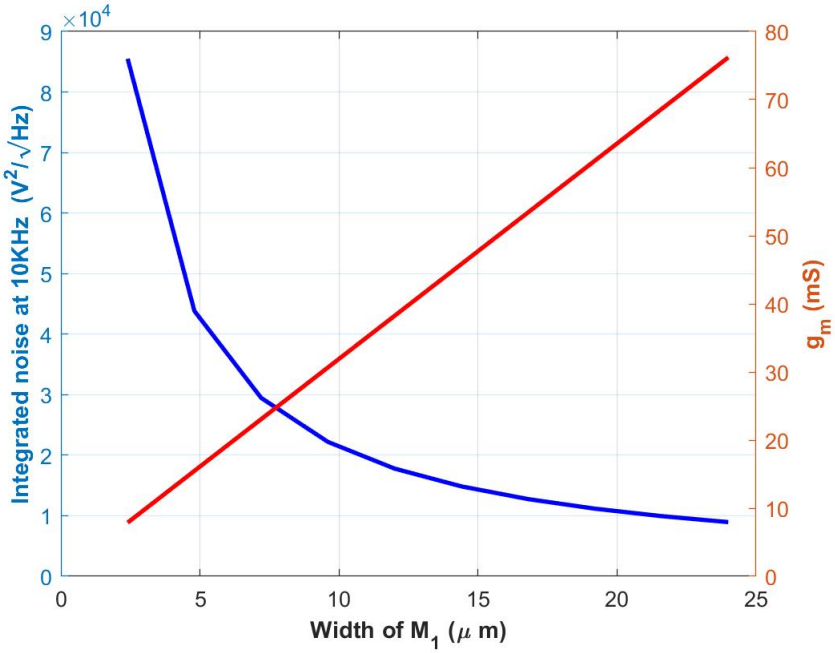


Figure 5.9: Core transistor characterization: (left) Integrated noise at 10KHz (right) g_m

harmonic peaks are wide by design, explicit tuning is not needed as long as the tuning range is not too high.

5.2.2.4 Fine tuning

The coupling transistors' flip-well diode to substrate poses a variable cap on the gate net, the continuous tuning of which provides fine tuning for the fundamental frequency. As seen in the equations of 3.3, the drain capacitance affects the third harmonic peak. So, for fine-tuning of 3rd harmonic peak, the flip-well to substrate varactor posed by the core transistors is used. In this way, existing elements are re-used, rather than introducing lossy varactors.

5.2.3 Class B design

The Class B design from Section 4.1.1 is implemented for similar bands, to be able to compare the phase noise performance and validate the improvement claimed by Class F architecture. By synthesizing a tank with Z_g impedance, a sinusoidal Class B oscillator is realised. Hence, $L_d = 180pH$, $C_g = 100fF$, $C_{cc_g} = 40fF$, $k_d = -0.3$. The active core and coupling circuitry from

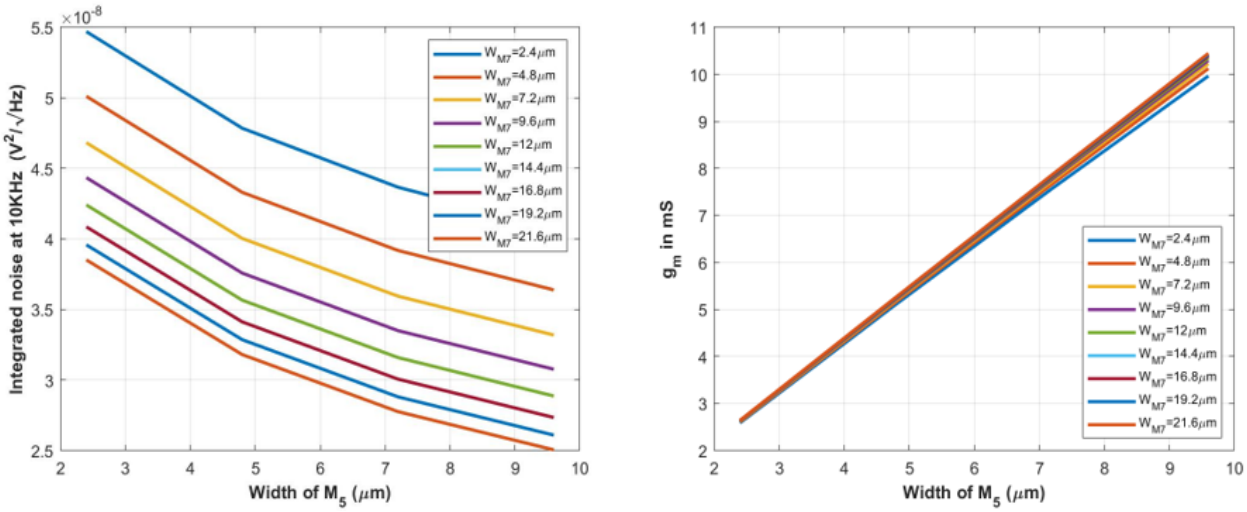


Figure 5.10: Coupling transistor characterization vs tail transistor width (left) Integrated noise at 10KHz (right) g_m

Class F design is reused.

The passive design is slightly relaxed, as the design does not need to be as wide-band as a Class F passive. Figure 5.13 shows the symmetric transformer design used in the Class B VCO. Figure 5.14 shows the parameters of the transformer simulated in ADS Momentum using 22nm FDSOI process profile.

5.2.4 Layout

The top-layout of the Class F VCO is shown in Figure 5.15. The Class F design occupies an active area of 400μm X 300μm. The Class B design occupied an active area of 260μm X 180μm The overall chip including shielding, decaps and the Class B design occupies 1mm X 750μm.

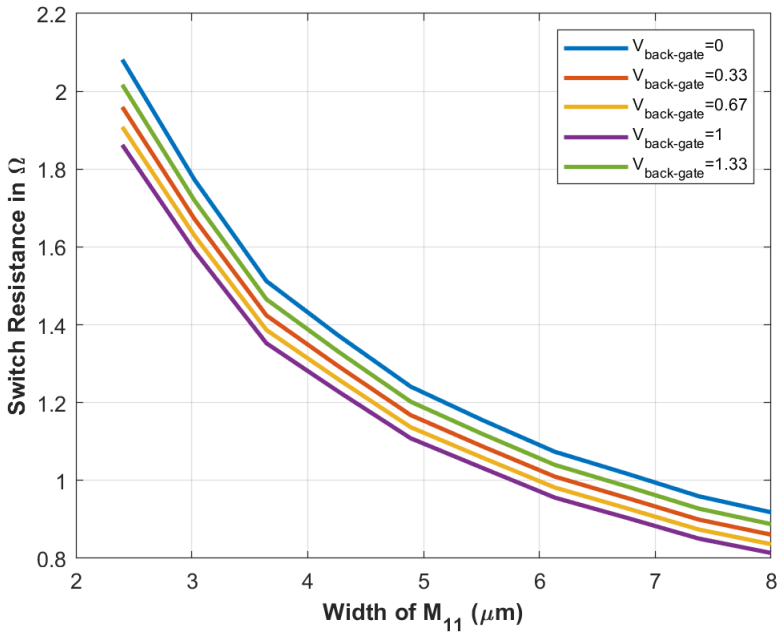


Figure 5.11: Switch resistance vs width for different back-gate voltages

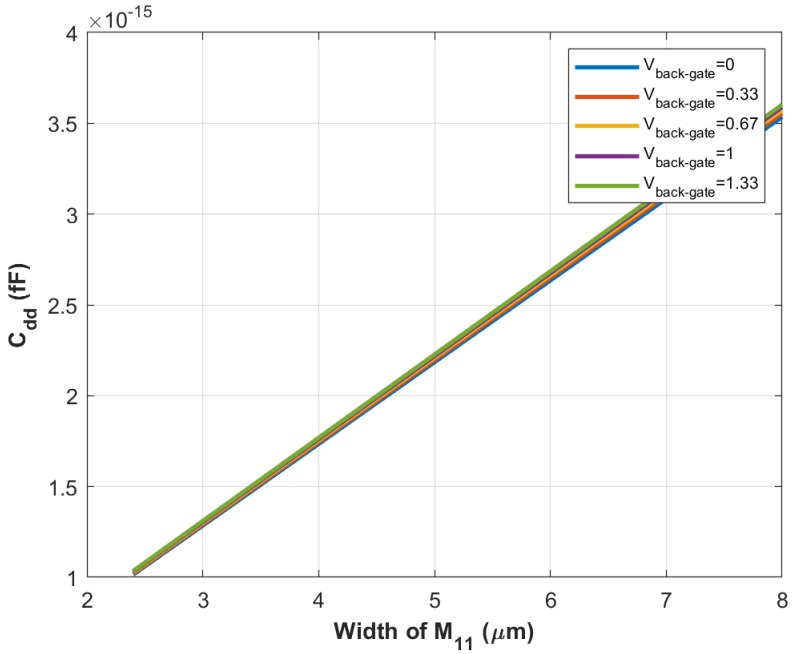


Figure 5.12: Switch parasitic drain capacitance vs width for different back-gate voltages

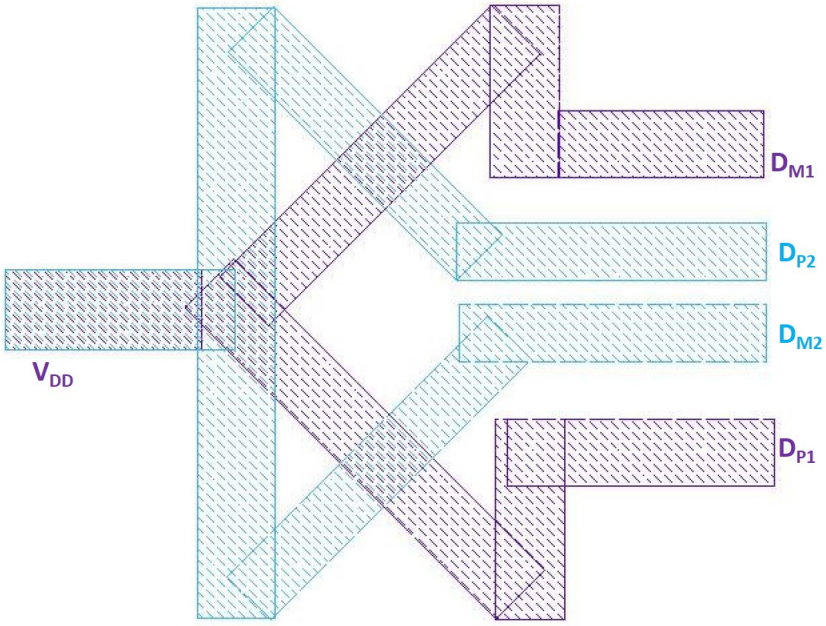


Figure 5.13: Class B: Symmetric load transformer

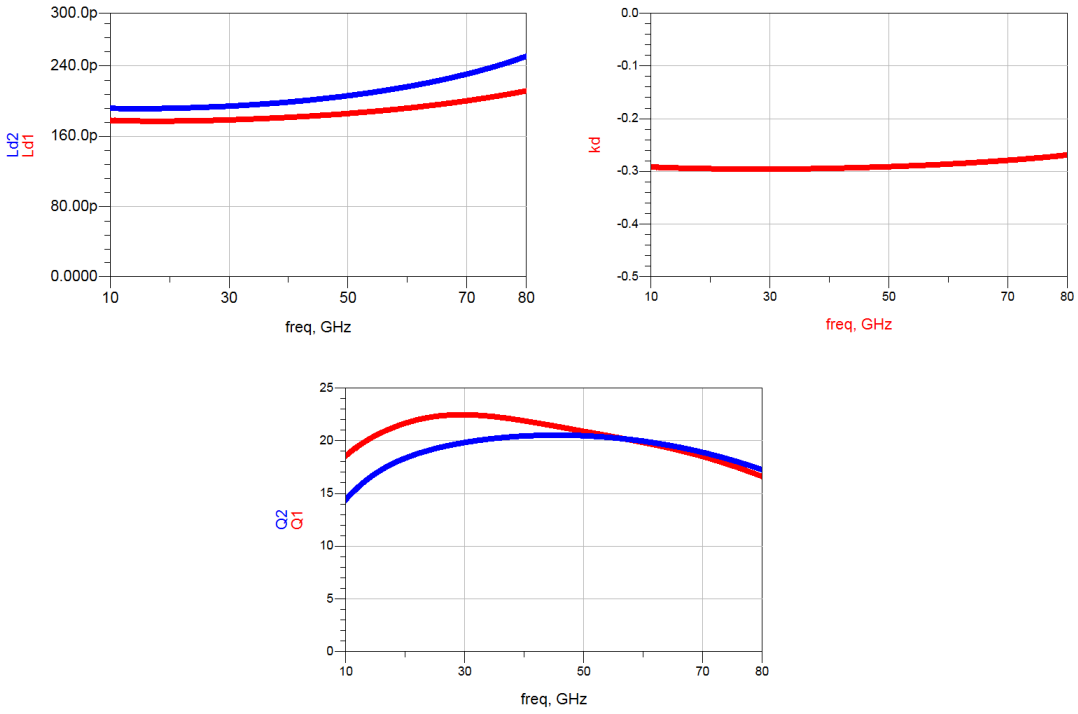


Figure 5.14: Class B symmetric load transformer: (top left) Coil self inductances (top right) Coupling factor (bottom) Coil quality factors

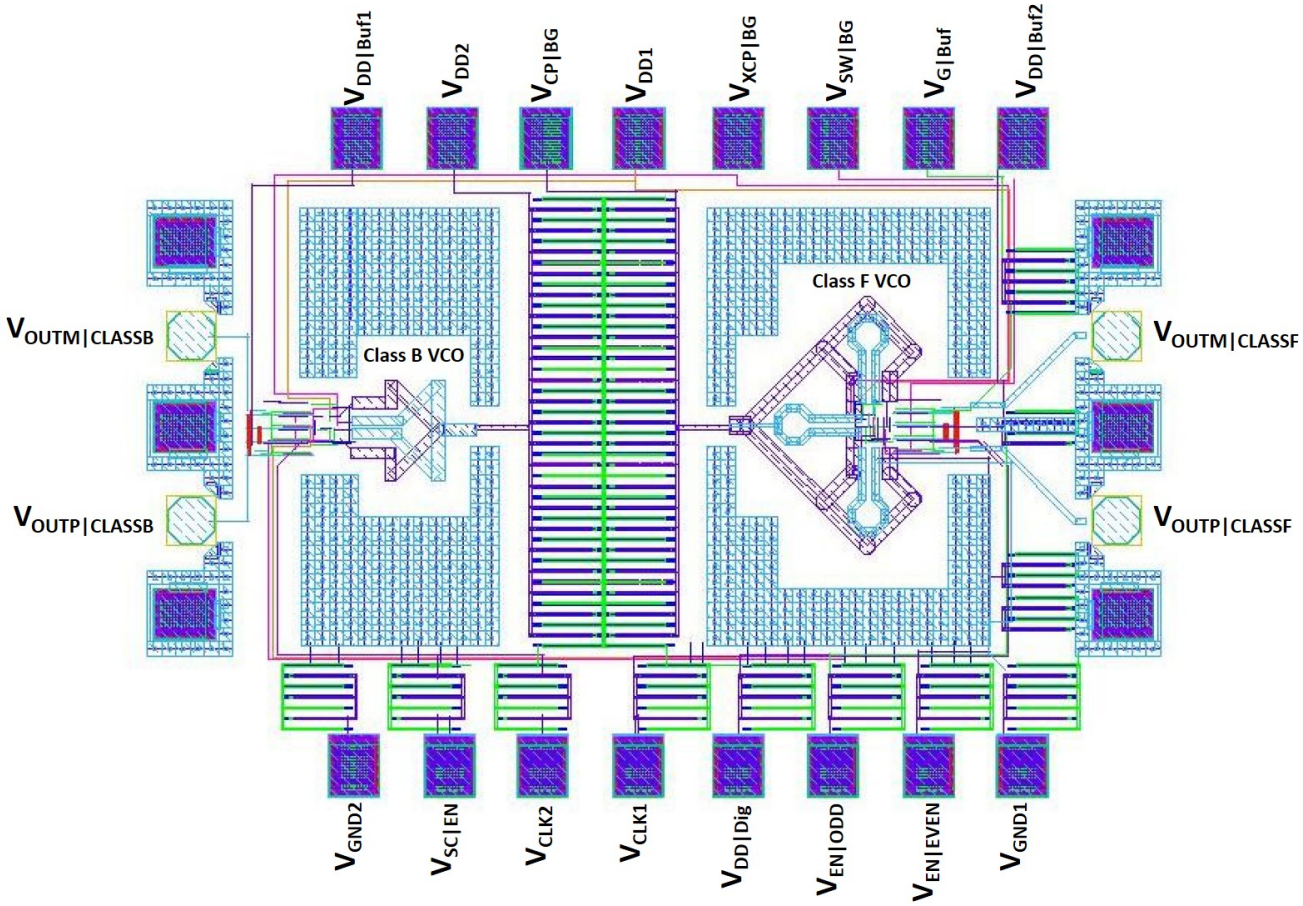


Figure 5.15: Layout: (left) Class B VCO (right) Class F VCO

6. RESULTS

In this section, the post-layout results for the dual-band Class B and Class F designs are presented and compared to state of the art.

Figure 6.1 shows the simulated impedance graphs of both the designs. As seen, the Class F peak at 120GHz is not as high as desired. This is due to Q degradation at mm-wave frequencies. Figures 6.3-**??** show the VCO parameters across tuning range. As seen, the Class F structure gives a minimum of 3dB improvement in the 22GHz band for the entire range. The improvement is slightly lesser in the 39GHz band, with a minimum of 2.1dB for the entire range. This loss is attributed to the low third harmonic peak at 120GHz.

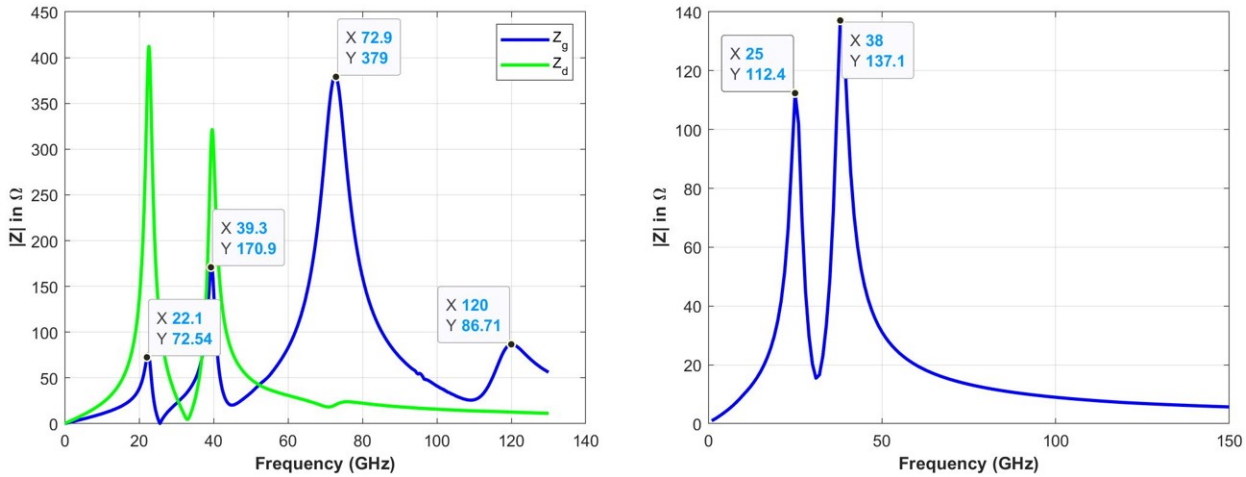


Figure 6.1: Impedance curves: (left) Class F VCO - (green) Gate (blue) Drain (right) Class B VCO

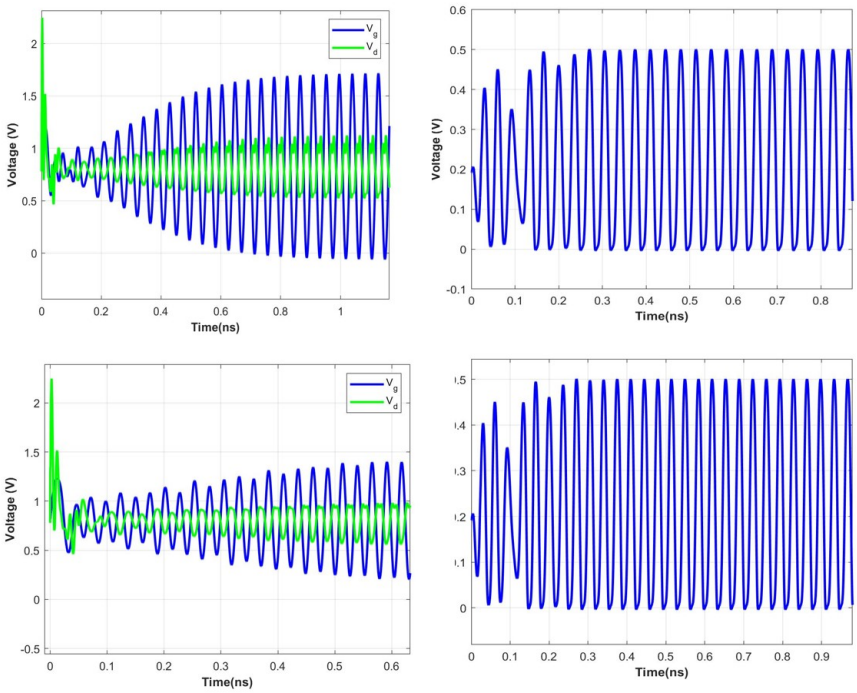


Figure 6.2: Start-up: (green) Gate voltage (blue) Drain voltage
(left) Class F (right) Class B
(top) 39GHz (bottom) 22GHz

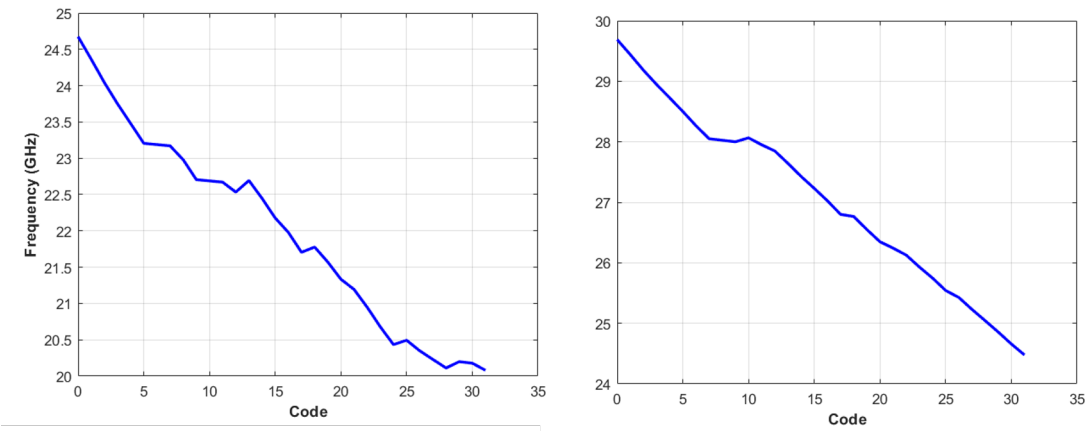


Figure 6.3: Lower band tuning range: (left) Class F (right) Class B

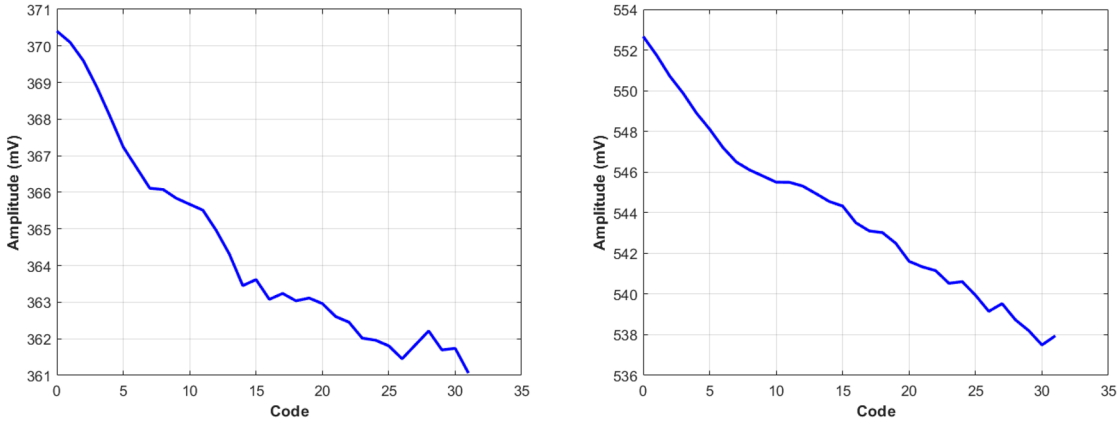


Figure 6.4: Lower band amplitude: (left) Class F (right) Class B

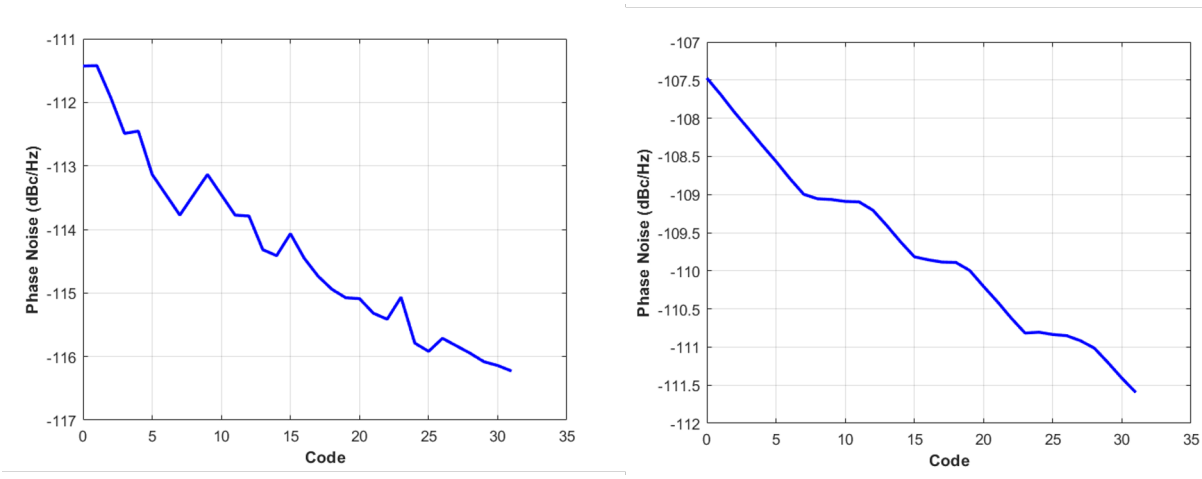


Figure 6.5: Lower band phase noise: (left) Class F (right) Class B

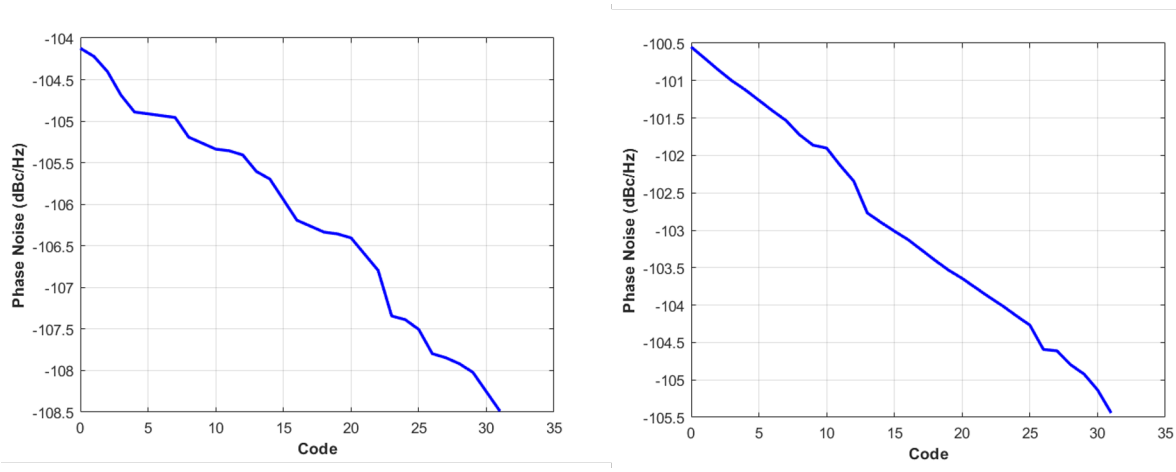


Figure 6.6: Higher band phase noise: (left) Class F (right) Class B

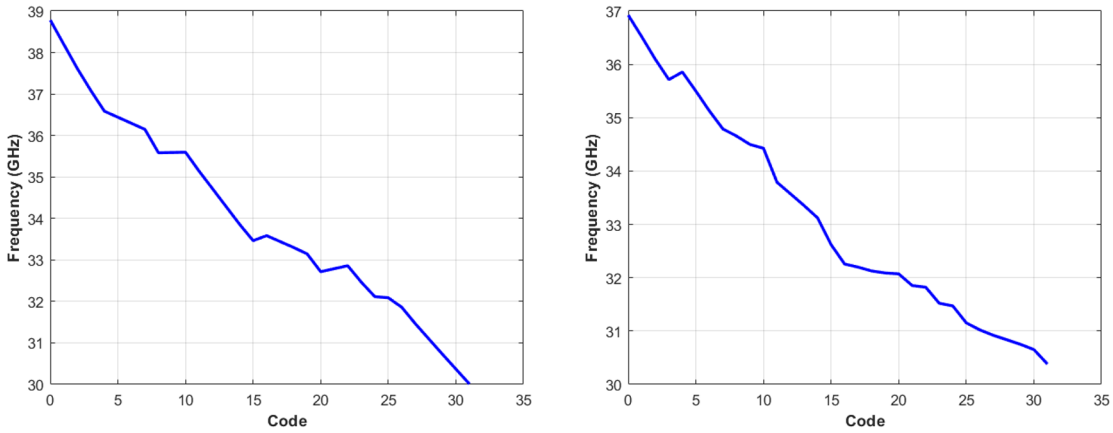


Figure 6.7: Higher band tuning range: (left) Class F (right) Class B

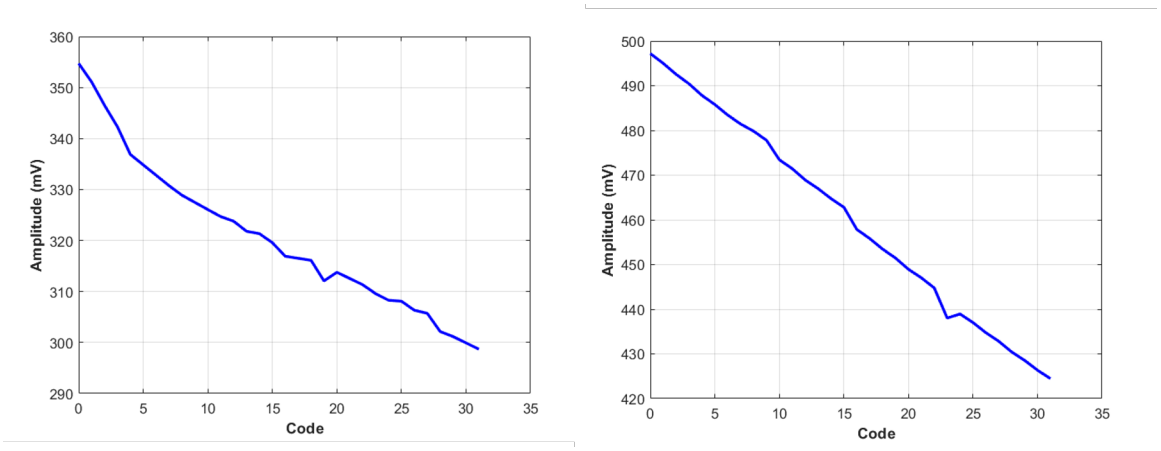


Figure 6.8: Higher band amplitude: (left) Class F (right) Class B

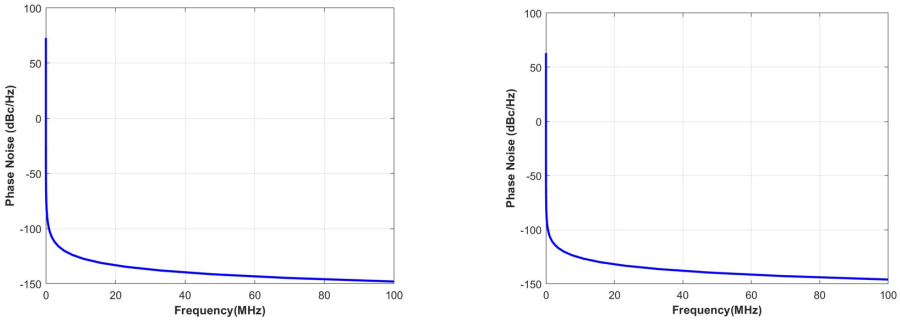


Figure 6.9: Lower band phase noise vs offset frequency: (left) Class F (right) Class B

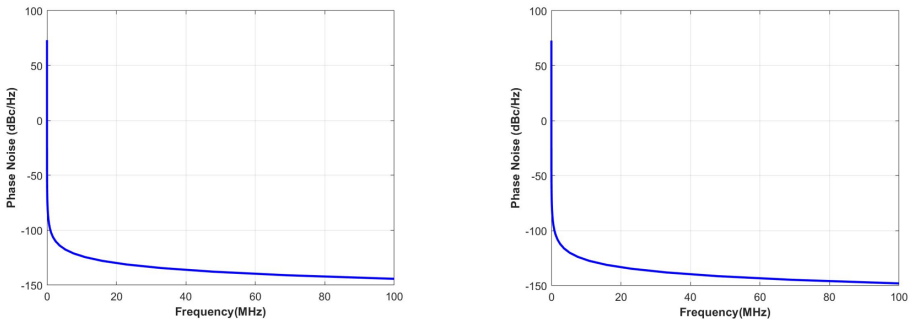


Figure 6.10: Higher band phase noise vs offset frequency: (left) Class F (right) Class B

Parameter	Class-B (Lower)	Class-F (Lower)	Class-B (Higher)	Class-F (Higher)
α_I	0.6	0.6	0.6	0.6
α_V	0.55	0.8	0.55	0.8
F_{Tank}	0.7	0.8	0.7	0.8
F_{GDS}	0.3	0.25	0.3	0.25
F_{GM}	$\simeq 0.7\gamma_{M1}$	$\simeq \gamma_{M1}$	$\simeq 0.7\gamma_{M1}$	$\simeq \gamma_{M1}$
P_{DC}	21.6mW	18mW	21.6mW	18mW
PN(dBc/Hz)	-109	-112.4	-99	-101
FoM (dB)	190.1	193.2	185.4	189.1

Table 6.1: Comparing figures of merit across the Dual Band Class B and Class F in VCOs in the both the bands

7. CONCLUSION AND FUTURE WORK

In conclusion, it is seen the claim that a Class F topology can improve provide up to 3dB of phase noise improvement over a Class B VCO is verified for the proposed dual-band topology. For comparison, both dual-band versions of both the VCO classes have been designed and sent for fabrication. Post-layout simulations are presented, that validate the superiority of a Class F design in terms of phase noise and overall figure-of-merit. The chip has been sent for tape-out and is expected to return in August'21. Probe level measurement activity is planned to measure the VCOs' performance.

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APPENDIX A

FIRST APPENDIX

A.1 Tuning range and C_{cc_g}

The ratio of $C_{cc_g} and C_g$ can be acutely related to the tuning range in the individual bands. Let TR_{even} and TR_{odd} be the fractional tuning ranges in the even and odd bands respectively, where TR is defined as

$$TR = \frac{f_{max} - f_{min}}{f_{min}} \tag{A.1}$$

$$\implies \frac{f_{max}}{f_{min}} = (1 + TR)$$

In the even band,

$$\begin{aligned} \frac{f_{max}}{f_{min\ even}} &= \sqrt{\frac{C_{g|fixed} + C_{var}}{C_{g|fixed}}} \\ \implies (1 + TR_{even})^2 &= 1 + \frac{C_{var}}{C_{g|fixed}} \\ \implies C_{var} &= C_{g|fixed}((1 + TR_{even})^2 - 1) \end{aligned} \tag{A.2}$$

In the odd band, C_{cc_g} manifests along with C_{g_fixed}.

$$\begin{aligned} \frac{f_{max}}{f_{min\ odd}} &= \sqrt{\frac{C_{g|fixed} + C_{cc_g} + C_{var}}{C_{g|fixed} + C_{cc_g}}} \\ \implies (1 + TR_{odd})^2 &= 1 + \frac{C_var}{C_{g|fixed} + C_{cc_g}} \end{aligned}$$

Substituting C_{var} from Equation A.2,

$$(1 + TR_{odd})^2 - 1 = \frac{C_{g|fixed}((1 + TR_{even})^2 - 1)}{C_{g|fixed} + C_{cc_g}}$$

Since $\frac{C_{ccg}}{C_g|fixed} = \alpha$,

$$
\begin{aligned}
(1 + TR_{odd})^2 - 1 &= \frac{((1 + TR_{even})^2 - 1)}{1 + \alpha} \\
\implies (1 + \alpha) &= \frac{((1 + TR_{even})^2 - 1)}{((1 + TR_{odd})^2 - 1)} \\
\implies (1 + \alpha) &= \frac{TR_{even})^2 + 2TR_{even}}{TR_{odd})^2 + 2TR_{odd})}
\end{aligned}
$$

TR is typically a fraction between 0 to 0.2. So TR^2 can be neglected when compared to 2TR.

$$(1 + \alpha) \simeq \frac{TR_{even}}{TR_{odd}} \tag{A.3}$$