AN EXPLORATION OF RADIATION EFFECTS ON LOW-NODE, HIGH-SPEED, MIXED-SIGNAL INTEGRATED CIRCUITS

A Thesis

by

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ABSTRACT

As circuits decrease in size and increase in speed, there will be a push to use higher performance electronics in the space sector, military sector, and the energy sector. As technology nodes decrease, they typically become more sensitive to radiation effects so extra design techniques must be utilized in order to make the circuits immune to radiation effects. Single Event Effects (SEEs) are a major concern as they will upset the transient response of the system. Total Ionizing Dose (TID) effects are also a concern as they will degrade the performance of the device until failure over a long period of time.

Voltage Controlled Oscillators (VCOs) and Phase-Locked Loops (PLLs) are critical in serial communication systems and must perform in the 10s of Gigahertz (GHz) range. This thesis focused on implementing a varactor scheme in order to reduce the sensitive area of the varactors inside of the VCO and implementing Triple Modular Redundancy in the digital blocks for the PLL to make it immune the Single Event Effects.

A SEE analysis was done on both the VCO and PLL to ensure radiation tolerance along with measuring the overall electrical characteristics. The radiation hardened VCO was found to have a nominal tuning range of 14GHz to 17.7GHz with a Phase Noise performance of -124dBc/Hz. The PLL was found to have a total peak to peak jitter performance at a Q of 7.5 of approximately 400fs with a rms jitter of 40fs and deterministic jitter equal to approximately 200fs. The total power consumption is 20mW for the PLL and a total area of 0.046mm^2.

DEDICATION

To my Loving and Supportive Family

And

To my Love Paulina

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I would like to thank my advisor, Dr. Palermo, for his guidance, patience, and support throughout this research. Thank you for giving me this opportunity, for having faith in me and always pushing me to do better work. I will take all of the lessons he has taught me and use them in my professional life.

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Contributors

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The Single Event Effect study in section 3.3 for the VCO was assisted by the Ph.D. student David Dolt in the department of Electrical Engineering. Also, I would like to thank Tong, Ph.D. student for his help with the layout of the VCO.

All the other work conducted for the thesis was completed by the student independently.

NOMENCLATURE

TID	Total Ionizing Dose
SEE	Single-Event Effects
SEU	Single-Event Upsets
SEL	Single-Event Latchup
VCO	Voltage Controlled Oscillator
PFD	Phase-Frequency Detector
CP	Charge Pump
PLL	Phase-Locked Loop
FFT	Fast-Fourier Transform
TD	Transition Density
GHz	Giga-Hertz
RadHard	Radiation Hardened
BW	Bandwidth

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1. INTRODUCTION

1.1 Radiation Effects in Electronics

There is a growing need for radiation hardened electronics for space applications, nuclear energy, and safety management as well as high-energy physics experiments like the ones done at CERN. Because of the aggressive scaling of integrated circuit technology nodes and the increased complexity of analog and digital circuitry there is an ever-increasing importance of assuring radiation tolerant performance in these rapidly growing application spaces.

For better understanding of the type of damage that can occur to silicon and silicon dioxide, which are the materials of interest in electronics, an introduction in radiation effects must be presented. Radiation effects can be broken down into two main categories that can occur in matter, there are ionizing and non-ionizing radiation. An ionizing event is when a particle of high enough momentum will knock off an electron from the incident's particle electron cloud temporarily. This can occur from either heavy particles or from high energy photons such as gamma rays and x-rays. Neutrons will not directly ionize particles; however, they will indirectly ionize particles by changing the isotope of an atom which will lead to indirect ionizing from the subsequent decay that particle.

There are 4 main types of radiation particles in radiation events, there are: Alpha particles, beta particles, gamma particles and neutron particles [1]. Alpha particles are a helium nucleus that is emitted by a radioactive substance. A beta particle is an electron or a positron that is been emitted during radioactive decay from the nucleus of an atom during beta decay. A gamma ray is a form of electromagnetic radiation that is released from the

nucleus of an atom during radioactive decay. Radioactive decay can occur from any unstable atom and is probabilistic by nature but can result in any of the four main types of radiation. Two other types of particles that are important for radiation effects considerations are protons and neutrons. Protons are predominant in space environments while neutrons are predominant in a reactor setting. Neutrons are produced from fission, which occurs spontaneously from fission from an atom such as uranium-235 which is fissile meaning it can sustain a fission chain reaction [2].

In order to characterize how radiation will affect a material we measure the energy that is absorbed by the material. This definition is used from both a health perspective but also from an electronics perspective as well. The unit for absorbed dose that is used is called a “rad”. A rad is defined as 1 Joule per unit kilogram, while a human can at best take about 100 rad, a radiation tolerant electronic chip can withstand approximately 10 KRad to 10MRad depending on the process and the circuit design techniques incorporated.[3]

Ionizing radiation will lead to electron-hole pairs which are the first forms of radiation damage in electronics. These electron-hole pairs will then go on to change the semiconductor’s electrical characteristics. This is known as Total Ionizing Dose (TID) and will be discussed further in section 1.2. When a large particle strikes a device, it will also ionize the semiconductor, but it will lead to an instantaneous pulse current that can also lead to failure, this will be discussed furth in section 1.3. Total Ionizing Dose effects will occur in the oxide of the device while Single Event Effects will originate in the silicon [4].

1.2 Total Ionizing Dose

Total Ionizing Dose is caused by the charge trapping from ionizing radiation in the silicon oxide around CMOS transistors. There are three main steps to this mechanism. Firstly, the electron-hole pairs are created with the radiation strikes the oxide and ionizes the region. One particle is capable of creating many electron-hole pairs in the substrate which depends on the total energy and the type of interaction that it has with the oxide. Once the interaction takes a place, a portion of the electrons will immediately recombine and not leave any damage, but some will not recombine which will lead to an excess of free electrons. Because there are now free electrons, they are capable of relocating to the gate under a positive bias if it is a nmos, if it is a pmos then the opposite will be true. The second phase will result in the positive charges migrating through the oxide to the silicon interface [5]. This can result from a thermal bias or an electric bias and when the charge arrives at the interface of the device it will remain trapped at that location. The positively trapped charge will result in a threshold shift approximately equal to equation below.

$$V_{ot} = \frac{-Q_{ot}}{C_{ox}}$$

The total charge generated is a direct result of the radiation interaction which is proportional to the gate thickness. This means that lower nodes will generate less charge and larger nodes will generate more charge. Thus, the threshold voltage will approximately shift proportionally to $\boldsymbol{t_{ox}^2}$ [5].

The threshold change can be calculated to the first order as the sum of silicon-oxide traps (Q_{ot}) and the interface traps (Q_{it}) for typical NMOS devices as shown in equation below [5,6].

$$V_{th} = -\frac{Q_{ot} + Q_{it}}{C_{ox}}$$

In pmos devices the oxide traps will be negative and interface traps will be positive. This leads to a conflicting effect in the threshold shift. For pmos devices both oxide traps and interface traps will be negative leading to a compounding effect.

A major assumption is that the radiation effects are uniform on the devices because there is no gradient in the beam which can be assumed for small chips but may be inaccurate for larger chips. In reality, even if the chip is small then the gradient will not be zero as this would assume every device is changed in the same way because the devices are identical. Device mismatches will also result in different Vth effects from the mismatch of the transistors along with the charge distribution being non-uniform.

1.3 Single Event Effects

Single Event Effects (SEEs) are a transient effect creating from a radiation effect striking the silicon. It is more predominant with larger particles as they will be more likely to create more electron-hole pairs. Depending on what location the particle hits will change the number of charges generated and the most charge was found to be generated near the source and drain junctions of the device. Because there is a high electric field, this will lead to the charge being moved as seen in Figure 1.1. Some of the charge will recombine and the rest of the particles that do not recombine will result in a transient current being generated.

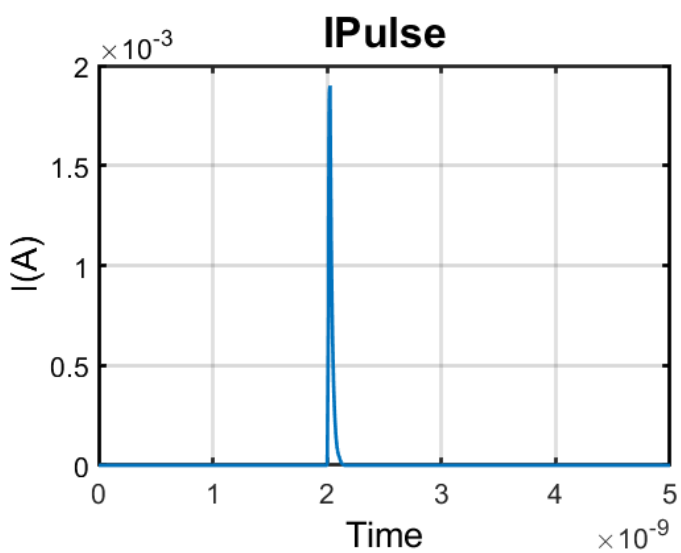

Figure 1.1: Pulsed Current Source

The currents that are created from this effect can be modeled by a double exponential Gaussian function as shown in the equation below [7].

$$I(t) = Q\frac{e^{\frac{t}{\tau_1}} - e^{\frac{t}{\tau_2}}}{\tau_2 - \tau_1}$$

Q is the total charge accumulated and τ_1 and τ_2 are the rise and fall times. Q can be difficult to predict due to the charge being highly dependent on doping levels, location of impact, recombination rates and the electric field of the MOSFETs [7]. This is best to be experimentally determined for a specific process design kit. Figure 1.2 shows the device model when there is a SEE. A heavy ion such as an Alpha particle will hit the substrate and generate charge which will then migrate creating a pulsed current as previously mentioned.

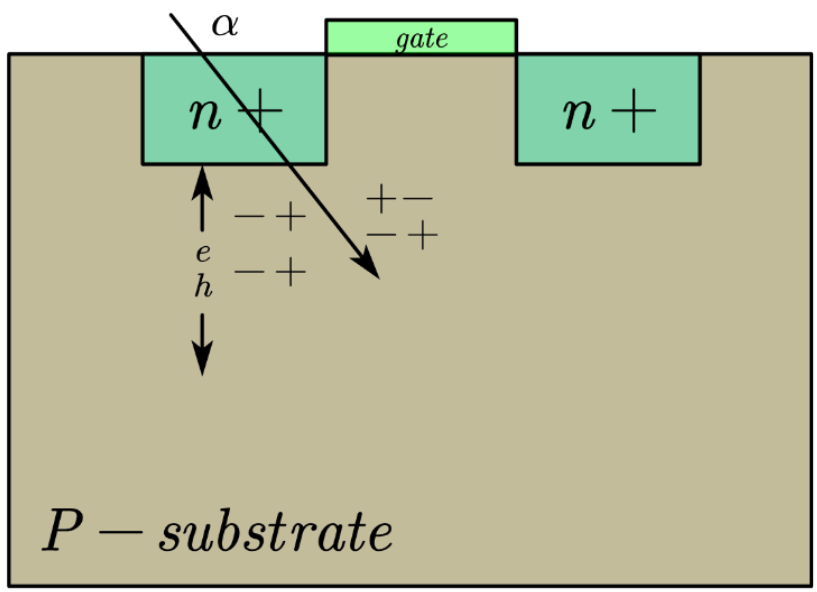

Figure 1.2: SEE Model

2. LITERATURE SURVEY

2.1 VCO Background

Voltage-Controlled Oscillators (VCOs) are circuits that can generate an output voltage that will be dependent on the input voltage based on the following equation. [8]

$$\omega_{out} = \omega_0 + K_{VCO}V_c$$

Where the VCO will have a center frequency of ω_0 and can be changed based on the Kvco of the oscillator. An oscillator will oscillate based on positive feedback so the voltage will grow in time. Because oscillators are LC tanks with time domain differential equation solutions such as

$$h(t) = e^{\omega t}(A * e^{\omega_o t} + B * e^{-\omega t})$$

For the equation above, the criteria for oscillation will be for the circuit to have complex poles inside of the right-half plane, this means the solution to the differential equation will not tend to 0 but will exponentially increase leading to oscillation.

Where the closed loop transfer function will follow the form of:

$$\frac{H(j\omega)}{1 - H(j\omega)}$$

This will lead to oscillation if H(jω)=1 leading to a zero in the dominator leading to positive feedback. This is also known as Barkhausen's Oscillation Criteria [8]. Which states that the phase of the loop should be zero at the oscillation frequency and that the magnitude of the loop gain should be one at the oscillation frequency.

2.1.1 Ring Oscillators

Ring Oscillators are oscillators created from inverter chains or really, delay cells. If there is an odd number of inverters, then the oscillator will oscillate at a frequency according to:

$$f_o = \frac{1}{2NT_{inv}}$$

Where T_{inv} is the delay of the inverter cell and N is the number of the inverter cells in the design. The delay of the cell can be controlled with controlled capacitance on the output of the inverter cells digitally. If there is an even number of inverter cells, then the oscillator will not oscillate.

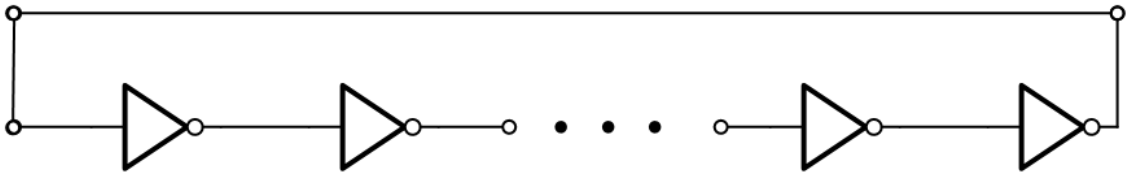

Figure 2.1: Ring Oscillator Diagram

One main advantage of using a ring oscillator is that they consume a lot less area compared to their LC oscillator counterparts as LC oscillators will consume a large amount of area due to the inductors that are needed for oscillation. They will also have a naturally higher tuning range than that of their LC counterparts, but their major drawback is that they will have a higher phase noise than an LC oscillator [9]. The typical CMOS inverter delay cell can be seen from Figure 2.2 below and is a typical digital inverter delay cell.

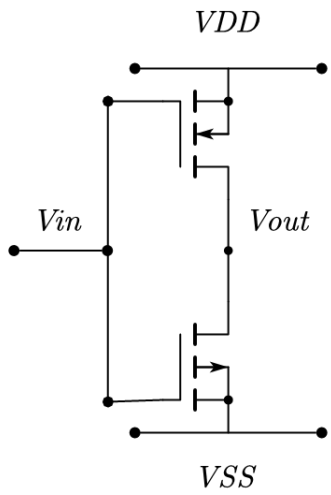

Figure 2.2: CMOS Inverter Delay Cell

The transfer function of the individual cell is equal to:

$$H(s) = \frac{-K}{1 + sT_{inv}}$$

Where T_{inv} and K are equal to:

$$K = (gm_n + gm_p) * (rds_p || rds_n)$$

$$T_{inv} = (C_{out}) * (rds_p || rds_n)$$

In feedback, the oscillator chain will follow the form of equation below, then the transfer function of the inverter chain will become:

$$H(s) = \frac{-(K)^N}{(1 + sT_{inv})^N}$$

So, to satisfy Barkhausen's criteria then:

$$1 = \frac{-(K)^N}{(1 + sT_{inv})^N}$$

And based on the number of delay cells, the delay and the gain can be solved for where $s = j\omega_{osc}$.

2.1.2 LC Oscillators

LC oscillators work off of the intrinsic oscillation properties of an LC tank, which is an inductor and a capacitor in a system. A general series LC tank is shown in Figure 2.3 which include the parasitic resistance from the inductor and the capacitor. The negative resistance which will negate the losses from the inductor and the capacitor. The series resistance can be converted into a parallel resistance at a give resonance frequency which can be shown from the equations below [10].

$$Q_L = \frac{\omega_0 L_s}{R_s} = \frac{R_P}{\omega_0 L_P}$$

$$Q_C = \frac{\omega_0 L_s}{R_s} = \frac{R_P}{\omega_0 L_P}$$

$$L_p = L_s \frac{Q^2 + 1}{Q^2}$$

$$C_p = C_s \frac{Q^2}{Q^2 + 1}$$

$$R_p = R_s(Q^2 + 1)$$

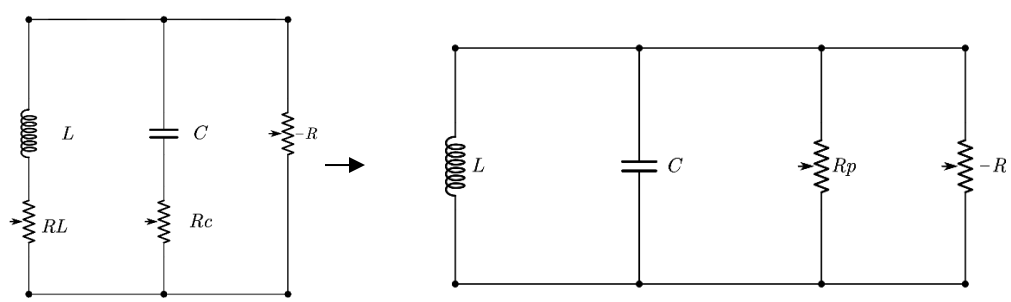

Figure 2.3: Series resistance LC tank converted to parallel resistance LC tank

From the above equations, it can be seen that if quality factor of the inductor and the capacitor are large meaning the parasitic resistance is low then the parallel

inductance/capacitance will be approximately equal to the series impedance. The quality factor is the proportion of the amount of energy contained vs the energy dissipated. Essentially it is the real impedance compared to the imaginary impedance. The quality factor of the passive components is critical in order to have an oscillator that can not only oscillate but also give good jitter performance.

An LC oscillator will naturally oscillate at:

$$f_o = \frac{1}{2\pi\sqrt{(L_p C_p)}}$$

A negative impedance component can be implemented with a negative transconductance value. To satisfy Barkhausen's criteria of oscillation, we have:

$$G_m R_p \geq 1 \text{ or } \frac{1}{gm} \leq R_p$$

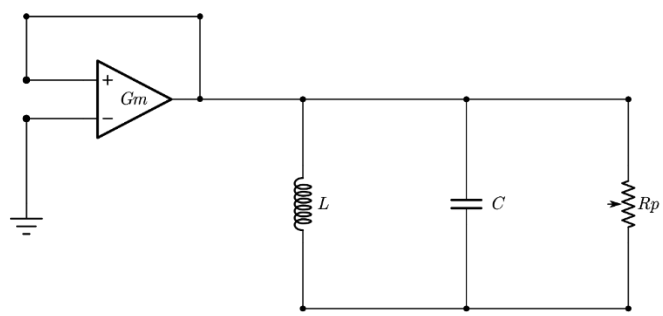

Figure 2.4: LC tank with -1/Gm load

2.1.3 Jitter and Phase Noise

Jitter is the time domain noise that is having the incorrect edges as compared to the ideal waveform. This can be shown in figure 2.5. Phase Noise is measured in units of dBc/Hz at an offset from the carrier frequency of the circuit. Phase noise is measured at an offset frequency with respect to the carrier [11]. The phase noise can be quantified as the noise power in a 1Hz bandwidth at a certain offset frequency represented as:

$$L(\Delta\omega) = 10\log\left(\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right)$$

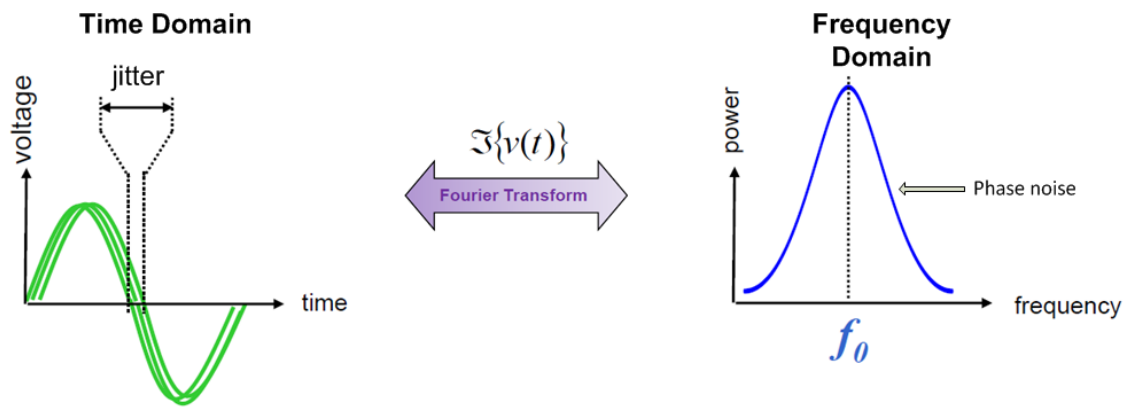

Figure 2.5: Time and Frequency representation of noise

As can be seen from the figure above, phase noise can be seen as “skirts” around the carrier frequency f_0 while the jitter is seen as the incorrect timing in the time domain. Jitter performance is critical for a timing system, high jitter in a system can cause real life errors such as a monitor to flicker, degrade processor performance and degrade the bit error rate (BER) of a given system.

2.1.4 Phase Noise Modelling in Oscillators

The ideal oscillator is shown as an LCR circuit with a noiseless device that can give energy to hold constant oscillation [12]. The only noise source would be the resistor that is in parallel. The noise spectral density could thus be represented by:

$$L(\omega_m) = 10\log\left[\frac{2kTF}{P_{sig}}\left(\frac{\omega_0}{2Q_L\omega_m}\right)^2\right]$$

Where k is the Boltzmann constant, T is the temperature in units of kelvin and R is the resistance of the parallel resistance of the oscillator. Q_L expresses the quality factor of the tank. This equation does not account for the high frequency noise floor and thus, is not an exact model but rather an introductory model for the oscillator.

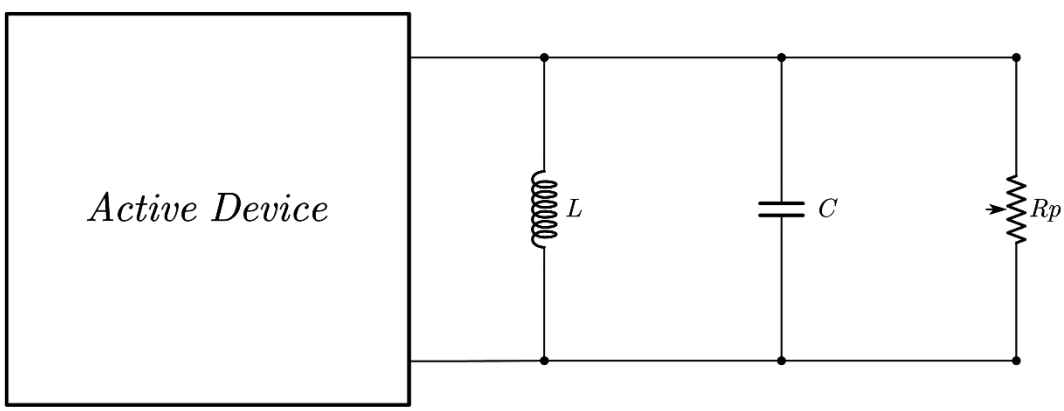

Figure 2.6: Phase Noise Circuit Model

Leeson's model is a more accurate and commonly used model to estimate the phase noise of the VCO. Leeson's model will account for the high frequency noise floor caused by white noise and also account for the 1/f noise introduced by the CMOS cross coupled pair. This equation can be represented by:

$$L(\omega_m) = 10\log\left[\frac{2kTF}{P_{sig}}\left(1+\left(\frac{\omega_0}{2Q_L\omega_m}\right)^2\right)\left(1+\frac{\Delta\omega_{\frac{1}{f^3}}}{|\omega_m|}\right)\right]$$

One downside of Leeson's model is the need of having an empirical fitting coefficient F which must be experimentally derived and can change depending on the process [11]. Another unknown variable is $\Delta\omega_{\frac{1}{f^3}}$ which represents the border of the f^{-3} and the f^{-2} areas of the phase noise graph shown in figure 2.7.

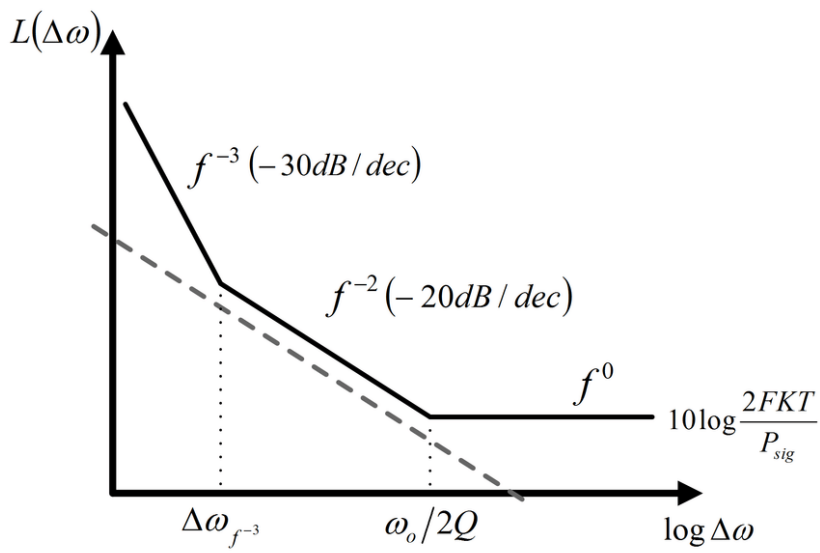

Figure 2.7: Leeson's Model for Phase Noise

Another noise model to accurately describe phase noise is using a time-variant method[13-15]. Noise that is injected into an LC oscillator will only sometimes contribute to the phase noise, so if a signal is at its maximum amplitude it will contribute to amplitude modulation noise but not to the phase modulation noise. Alternatively, when the signal is crossing a zero, this will lead to contribute to the PM noise of the system.

An impulse charge that is injected into a tank will create a phase step and the amount of the phase shift will be dependent on what time that impulse charge arrives. This can be due to noise or a radiation effect for example. The equation is given by:

$$h_{\phi}(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau)$$

Thus, $\Gamma(\omega_0\tau)$ is the Impulse Sentivity Function (ISF) which is a function of time and the response of the system. Where $q_{max} = C_{node}V_{max}$ which is the maximum charge and $u(t-\tau)$ is the unit step function for the system. The ISF represents how sensitive an oscillator is to an periodic impulse function and the units are dimensionless. This can be shown in figure 2.8.

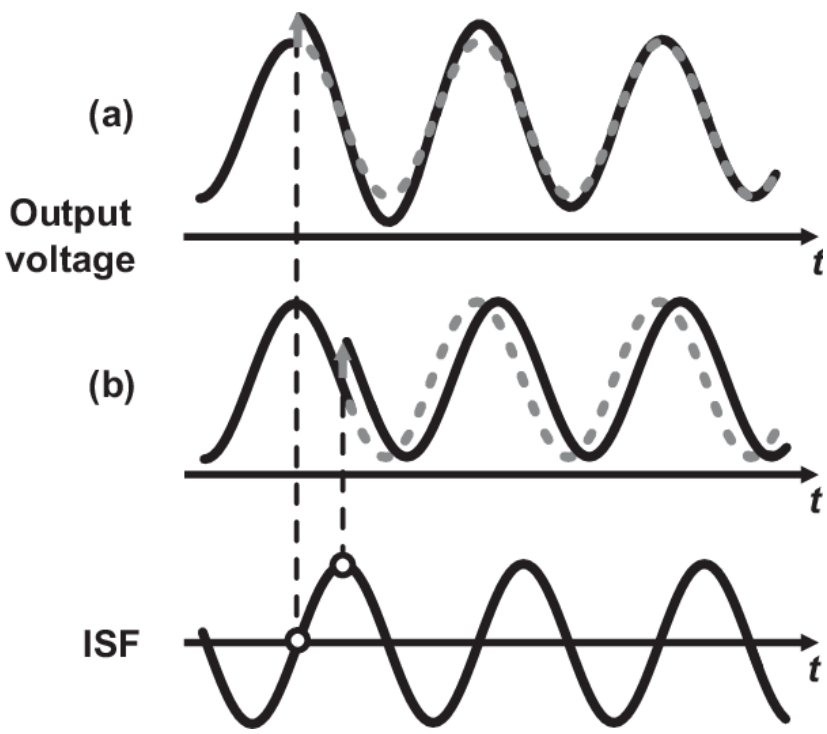

Figure 2.8: AM and PM error created by ISF

So, because the ISF is periodic, it can be represented as a fourier series as:

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos\left(n\omega_0\tau + \theta_n\right)$$

The coefficients of c_0 and c_n are real and θ_n are the coefficients and phase of the nth harmonic of the ISF. If the noise components are uncorrelated, which is typically assumed, then the θ_n of the harmonics is ignored. The phase noise can then be computed by [15]:

$$\Phi(t) = \frac{1}{q_{max}}(c_0 \int_{-\infty}^{t} i_n(\tau)dt + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i_n(\tau)\cos(n\omega_0\tau)\, d\tau$$

This equation represents the mixing of the input signal with the n_{th} harmonics. As shown in the figure below, each branch will mix the input signal with the nth harmonics and a $\frac{1}{s}$. Integration filter is applied. Because there is a conversion from current to phase, white current noise will then be converted to phase noise which then will be shaped with a $\frac{1}{f^2}$ factor which is why higher ordered harmonics are able to contribute to lower frequency noise. One consideration is the c_n will generally decrease with higher ordered harmonics as well. Since c_0 is mixed, this is why lower frequency phase noise is converted to phase noise and the the normal linear model cannot describe this effect. This makes sense because c_0 is the DC component and arrives from the symmetry of the signal.

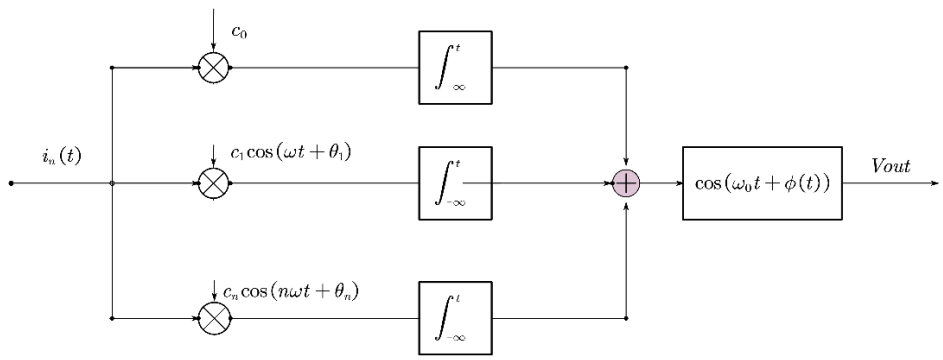

Figure 2.9: ISF mixing

From this the white noise is known to be:

$$L(\Delta\omega) = \frac{\frac{di_n^2}{df}\sum_{n=0}^{\infty} c_n^2}{4q_{max}^2\Delta\omega^2}$$

This represents the $1/f^2$ region of the phase noise and by using Parseval's theorem [16] this equation be converted to:

$$L(\Delta\omega) = \frac{\frac{di_n^2}{df}\Gamma_{rms}^2}{4q_{max}^2\Delta\omega^2}$$

This indicates that in order to minimize the phase noise we can minimize c_n or rather Γ. The 1/f phase noise can be represented by:

$$L(\Delta\omega) = 10\log\left(\frac{\frac{i_n^2}{\Delta f}c_0^2}{8q_{\max}^2\Delta\omega^2} * \frac{\omega_{\frac{1}{f}}}{\Delta\omega}\right)$$

Extracting the $1/f^3$ corner frequency and using Parseval's theorem again results in:

$$\Delta\omega_{\frac{1}{f^3}} = \omega_{\frac{1}{f}}\left(\frac{\Gamma_{\mathrm{dc}}}{\Gamma_{\mathrm{rms}}}\right)^2$$

Showing that if Γ is reduced there will be a reduction in phase noise overall.

2.2 Phase Locked Loop Overview

A Phase Locked Loop (PLL) is a feedback system that will generate an output signal that is in phase with the input signal. A general analog PLL diagram is shown below in Figure 2.10. It works by taking an input signal and comparing it to the feedback signal. In this case, if there is a difference in phase then an error voltage will be created which will drive a charge pump. The charge pump will then push or pull current to charge the control node Vc which will set the oscillation frequency of the VCO. The output of the VCO will then be passed back to the phase detector after being divided by a programmable frequency divider in order to try to match the input and output frequencies.

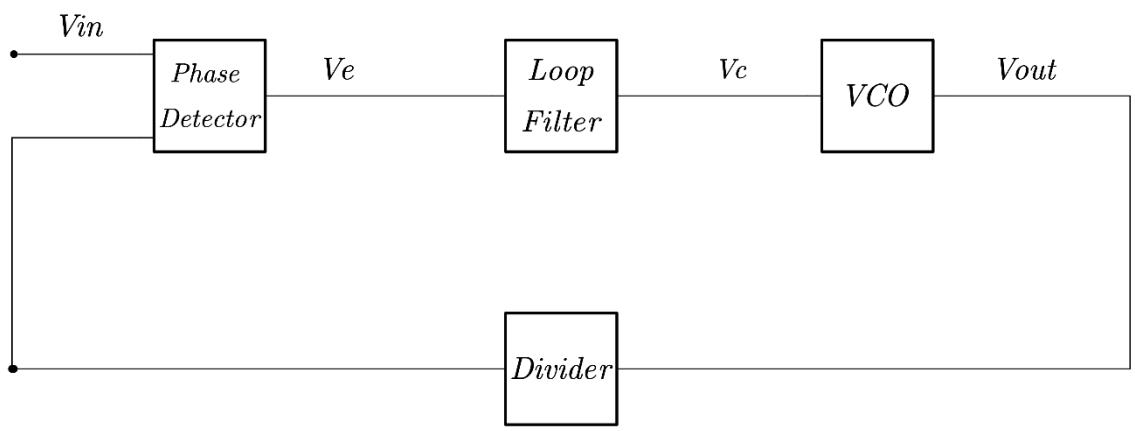

Figure 2.10: Typical Analog PLL

There are a few different forms of PLLs, there are analog and digital PLLs. In this document, only analog PLLs will be discussed but digital PLLs offer their own merit [17].

2.2.1 Phase Locked Loop Linear Analysis

A PLL can be modeled by a linearized phase domain model, and by using control theory we can calculate the loop transfer function by using Mason's rule, which is [17]:

$$G(s) = \frac{1}{\Delta}\sum_{i} G_i \Delta_i$$

Where G_i is the path gain of the ith forward path, Δ is the system determinant which is equal to 1 minus the sum of the individual loop gain plus the sum of the gain products of all the possible combinations of two loops that do not touch, then minus the gain products of three loops that do not touch. This pattern is repeated for as many cases as possible. Then Δ_i is the ith forward path determinant which is equal to the value of the determinants that do not touch the forward path. The PLL can be represented in the s domain by Figure 2.11.

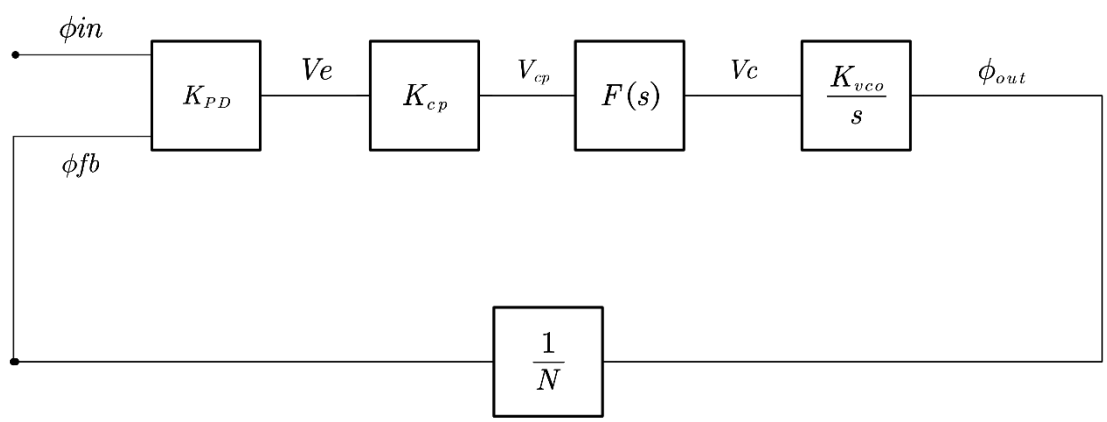

Figure 2.11: Full Loop PLL with Divider

By using Mason's rule, the loop transfer function of the system can be estimated linearly, where the forward gain path can be found as:

$$G(s) = \frac{K_{pd} K_{cp} K_{VCO} F(s)}{s}$$

The phase detector gain and the charge pump gain can be combined generally into one term which is represented here by K_{PDC}. The loop gain of the system can then be calculated as the forward path multiplied by the feedback path which results in:

$$l_1 = -\frac{G(s)}{N} = -\frac{K_{PDC}K_{VCO}F(s)}{sN}$$

Where F(s) is a low pass that is set by the loop filter. This will predominantly set the order of the transfer function. The order refers to the total number of poles in the system. The type of PLL will refer to the number of integrators or number of 1/s blocks in the system. This is because if the inverse Laplace transform is done, this will result in an integrator.

For the PLL shown in Figure 2.12, if the loop filter, F(s), is what will predominantly set the order of the PLL, because depending on the type of filter, this will change F(s). For a first order PLL, the PLL will have a low-pass transfer function response for the system. The overall transfer function can be found from the previous equations which is:

$$H(s) = \frac{K_{PDC}K_{VCO}F(s)}{s + \frac{K_{PD}K_{VCO}F(s)}{N}}$$

This will set the closed-loop bandwidth equal to approximately the first pole, which will set the 3-dB bandwidth as:

$$\omega_{3dB} = \frac{K_{PDC}K_{VCO}F(s)}{N}$$

Which is equal to the DC loop gain. The problem with having a first ordered PLL is that since there is no true filtering of the charge-pump/phase-detector output, this will

result in issues actually modeling the phase-detector as it may not accurately be predicted by a simple gain term of K_{cp}/K_{PD} which is because there may be higher ordered harmonics that are not filtered which result in non-linear behavior that has not been accounted for. Another issue with first ordered PLLs is that because the bandwidth is set by the loop gain and not by F(s), for example, then there is very little control over the system, which means that it will be difficult to adjust parameters to fit the need of the application.

Second order PLLs are more useful than their first order counterparts, by using a simple passive lag-lead filter the order can be increased to a second order PLL. A passive lag lead filter can be shown by the figure below.

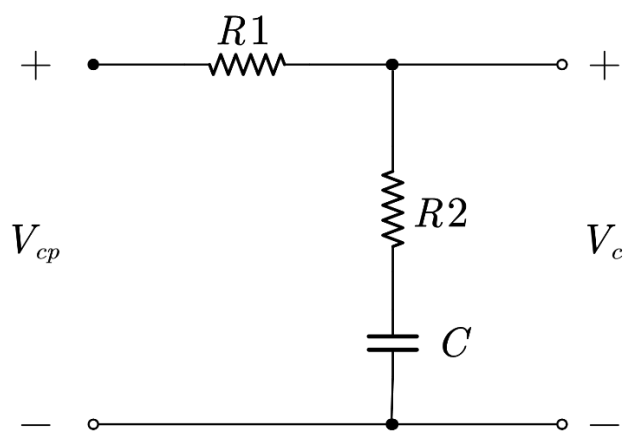

Figure 2.12: Lag Lead Filter

The Passive lag lead's transfer function can be found from simple analysis as:

$$F(s) = \frac{(1 + sR_1C)}{1 + s(R_1C + R_2C)}$$

This will result in the forward gain path of the system changing to where now the resultant transfer function will be:

$$H(s) = \frac{\frac{K_{PDC}K_{VCO}R_2C}{R_1C + R_2C}\left(s + \frac{1}{R_2C}\right)}{s^2 + \frac{1 + \frac{K_{PDC}K_{VCO}R_2C}{N}}{R_1C + R_2C}s + \frac{K_{PDC}K_{VCO}}{N(R_1C + R_2C}}$$

From this, we can extrapolate the natural frequency, which is the frequency at which a system will oscillate if there is no dampening factor. However, in this system there is a dampening factor which will prevent oscillation. The natural frequency is represented by, ω_n, and the dampening factor by, ζ. In order to extrapolate the natural frequency and the damping factor, the denominator of the transfer function in the s domain follows a quadratic form of [17]:

$$s^2 + 2\zeta\omega_n s + \omega_n^2$$

The natural frequency from this system is found to be:

$$\omega_n = \sqrt{\frac{K_{PD}K_{CP}K_{VCO}}{N(R_1C + R_2C)}}$$

Then the damping factor can be found as well from the denominator as:

$$\zeta = \frac{\omega_n}{2}(R_2C + \frac{N}{K_{PDC}K_{VCO}})$$

The benefit of having the second ordered PLL is that there are enough design parameters so that the loop dynamics can be sufficiently controlled. One problem however, is that if the loop incurs a frequency offset which can be represented by [17]:

$$\lim_{s=0}\frac{\Delta\omega}{s^2}\left(sE(s)\right) = \lim_{s=0}\frac{\Delta\omega\left(s + \frac{N\omega_n^2}{K_{PDC}K_{VCO}}\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{\Delta\omega N}{K_{PDC}K_{VCO}}$$

This implies that a second order type one PLL will still lock with some phase error if there is a frequency ramp that is very realistic in a system, especially in the presence of

radiation effects. Also, because of the second pole introduced into the system, phase margin now becomes a concern in order to properly lock. In order to combat this, a second ordered type two PLL can be used. The following analysis will show this benefit.

A type two PLL will typically incorporate a series-RC lag-lead filter in which can be shown by Figure 2.13 along with the charge pump that will charge the control node of the VCO. While the charge pump is typically used with this type of filter, it is not necessary in the preceding topologies, so it is not always included.

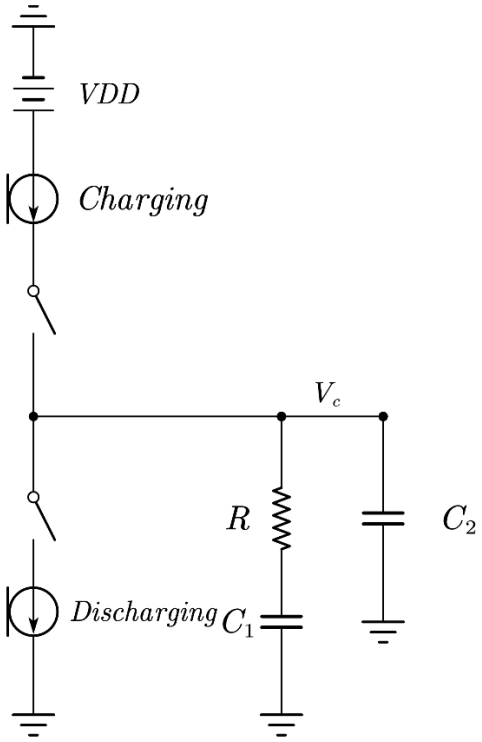

Figure 2.13: Charge Pump with Filter

This filter does not have to incorporate C_2 but it is included here because it is used in order to reduce ripple so it is a commonly used and will be included in this analysis. The transfer function of this filter is:

$$F(s) = \frac{\left(\frac{1}{C_2}\right)\left(s + \frac{1}{RC_1}\right)}{s(s + \frac{(C_1 + C_2)}{RC_1C_2})}$$

This will essentially average the error pulse that are created by the phase frequency detector of the system. While the transfer function is the same regardless of if the capacitor or the resistor is on top, one major consideration is that if the capacitor is on top then there will be extra parasitics from the bottom of the plate to ground.

The forward gain of the second order type 2 PLL, we find that firstly the forward path gain can be found as:

$$G(s) = \frac{K_{PDC}K_{VCO}\left(\frac{1}{C_2}\left(s + \frac{1}{RC1}\right)\right)}{s^2\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}$$

From this, the transfer function of the system can be found from similar analysis and letting K earlier in the section as:

$$H(s) = \frac{K_{PDC}K_{VCO}\left(\frac{1}{C_2}\right)\left(s + \frac{1}{RC_1}\right)}{s^3 + \frac{C_1 + C_2}{RC_1C_2}s^2 + \frac{K_{PDC}K_{VCO}}{NC_2}s + \frac{K_{PDC}K_{VCO}}{NRC_1C_2}}$$

Because this is a third order system, stability is a critical concern, so the system needs to be designed carefully in order to ensure the phase margin is large enough to be stable. To calculate the loop stability of this system, first the loop gain transfer function can be found by cutting the loop, and “walking around” the loop, which results in a loop gain response of [17]:

$$LG(s) = \frac{K_{PDC}K_{VCO}\left(s + \frac{1}{RC_1}\right)}{NC_2s^2\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}$$

From this, we can see that there are 3 poles and 1 zero in this system. There are 2 DC poles, 1 high frequency pole and 1 zero. Because we have two DC poles, we have:

$$\omega_{p1} = \omega_{p2} = 0$$

With the higher frequency pole equaling:

$$\omega_{p3} = \frac{C_1 + C_2}{RC_1C_2}$$

And finally, the zero equaling:

$$\omega_z = \frac{1}{RC_1}$$

So by ensuring that the phase margin which is equal to:

$$\Phi_m = \tan^{-1}\left(\frac{\omega_u}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_u}{\omega_{p3}}\right)$$

Because there are two DC poles in the system, the system will start at $-180°$ which means that it is inherently unstable. Fortunately, the zero will compensate for this which means that the loop can be stabilized if designed properly. Where ideally the maximum phase will occur at the unity gain frequency of the system to ensure that there is enough margin.

2.2.2 Phase Detector Overview

The first block of both digital and analog PLLs is a phase detector, that will be able to detect the difference in phase between the reference signal and the feedback signal. It will then produce an error voltage. The units for a phase detector is in volts per radians,

which represents that the larger the phase error the higher the voltage, but this is only if the phase detector is linear. This can vary based on the detector, a few phase detectors will be explored in this section.

An analog mixer can be used as a phase detector, because when two signals are mixed with relatively close phase and close frequency then the following diagram will represent the inputs and output of the mixer [17].

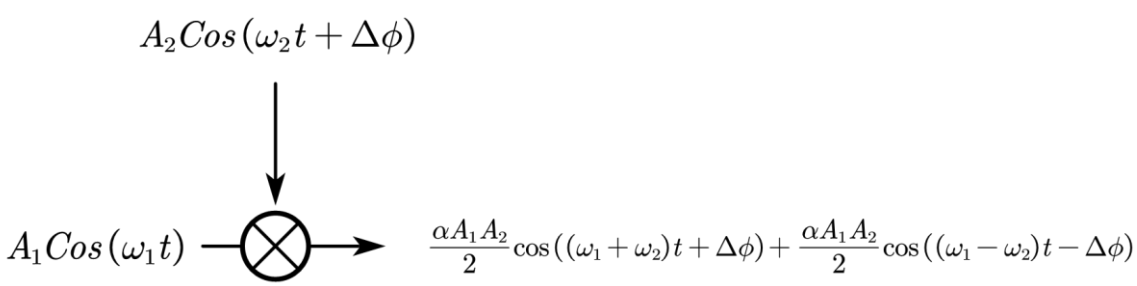

Figure 2.14: Mixer as PFD

After the output is filtered then only coefficients will results if $\omega_1 = \omega_2$ and the phase difference is equal to $\frac{\pi}{2}$. This will result in the mixer having a gain of:

$$K_{PD} = -\frac{\alpha A_1 A_2}{2}$$

This means that there will be a static phase shift of 90 degrees. This type of detector is unable to detect the difference in frequency, which is unfortunate, because this means that the input frequency must already be equal to the feedback frequency and because the gain is equal to the input frequency, it is not necessarily controllable. This makes this type of phase detector undesirable for a lot of applications.

The most commonly used phase detector is the digital implementation that is a Phase Frequency Detector. This type of detector is very useful because it detects not only a phase difference but also a frequency difference. This will allow for a wide frequency locking range. The schematic for the digital Phase Frequency Detector is shown in figure 2.15. The way this circuit operates is that every rising edge the UP signal, which is based on the reference signal, will produce a pulse, assuming this is leading the feedback signal, then when the feedback signal goes high the reset will be triggered. This will result in either an up or down signal that's pulse width is equal to the difference between the rising edge of the leading signal to the leading edge of the lagging signal.

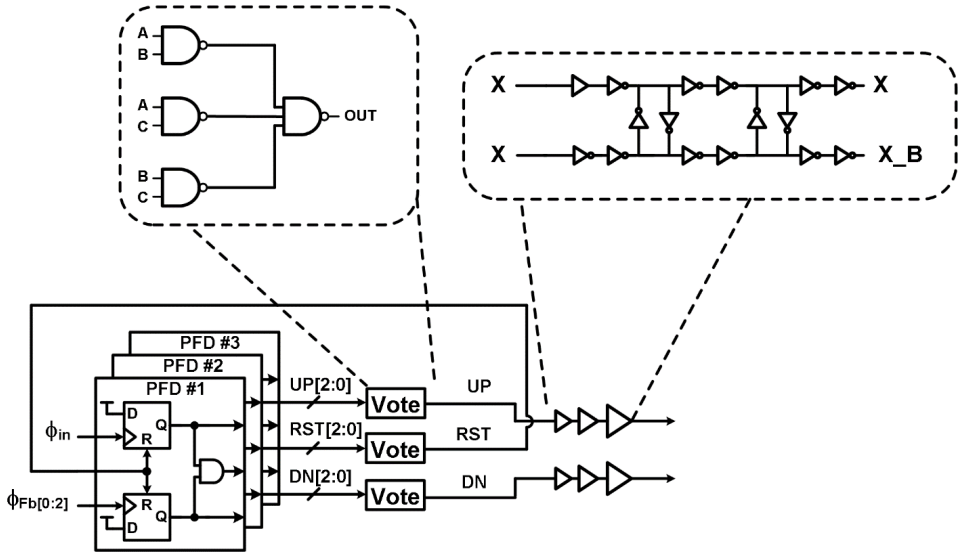

Figure 2.15: Phase Frequency Detector Schematic

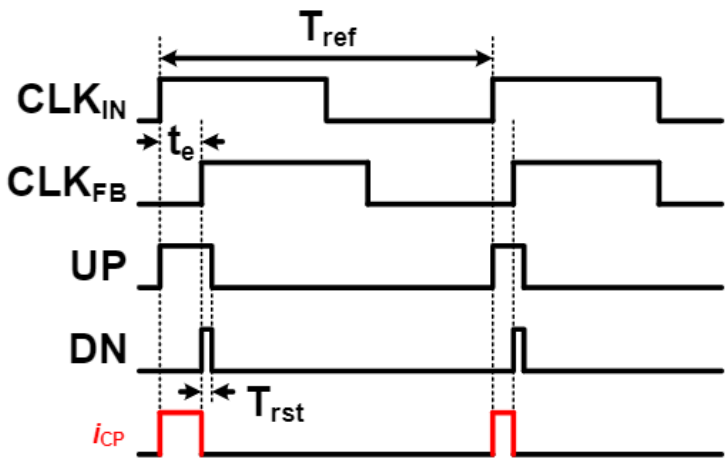

Figure 2.16: PFD Input and Output Waveforms

A delay element is typically needed to ensure that there is not a "deadzone" in the PFD, this is because if the reset delay is too small then when the phase error is small there will be very short output pulses that are provided by the PFD resulting in the charge pump not having enough time to either push or pull current onto the control node [18]. This will decrease the overall loop gain because of the reason stated previously, the delay however will also lead to cycle slipping if the delay is a large portion of the reference cycle. The maximum period of the delay is equal to:

$$T_{rst} = \frac{T_{ref}}{2}$$

And the maximum frequency of the PFD is found to be:

$$F_{PFD,max} = \frac{1}{2T_{rst}}$$

As shown in Figure 2.17 if the reset period is too long then this could cause a negative or positive error voltage which would absolutely lead to cycle slipping, so while

it is important to ensure there is no deadzone, the delay of the PFD must also not be too long.

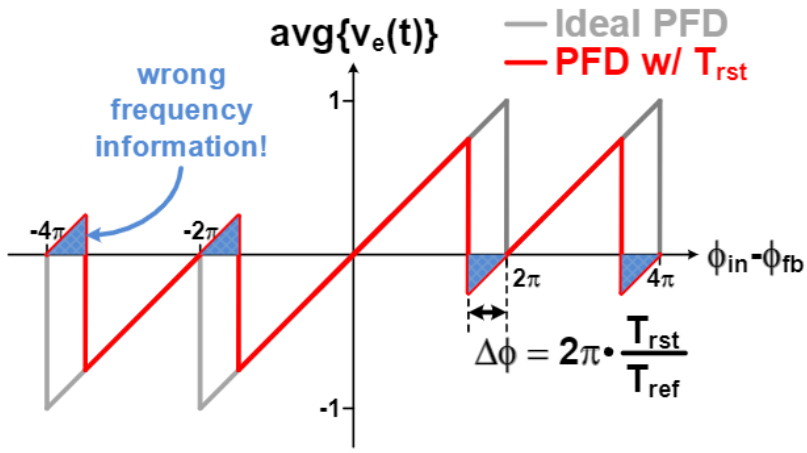

Figure 2.17: PFD Characteristics with Reset Delay

The cycle slipping can be seen in Figure 2.18 below. In this case the PFD will tell the charge pump to pull current rather than push current resulting in a cycle slip in the VCO.

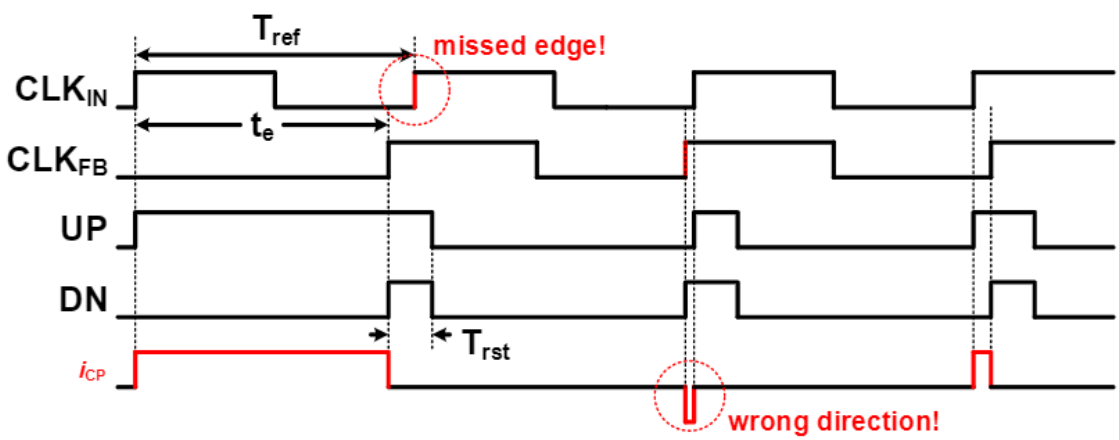

Figure 2.18: PFD-Charge Pump Interaction

2.2.3 Charge Pump Overview

A Charge Pump works by suppling current to the control node of the VCO, it is imperative that up and down currents are properly matched to ensure that there will not be a phase error created by the mismatch of the charge pump. A simple charge pump is shown in Figure 2.19.

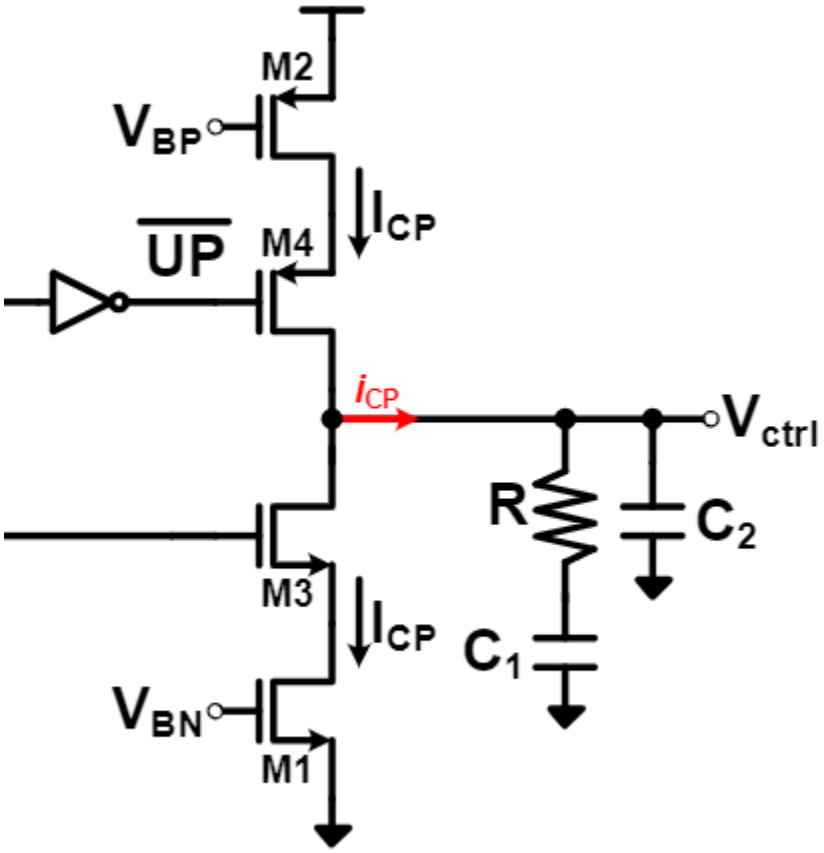

Figure 2.19: Simple Charge Pump

Another major consideration is that the UP and DWN delays from the PFD need to be properly matched in order to have the charge pump push or pull current at the same

rate. In order to do this, a simple strategy is to add a transmission gate on M3 as shown in Figure 2.20, below. This will help match the UPB and the DWN pulses but will create bad edge rates going into the gate of M3.

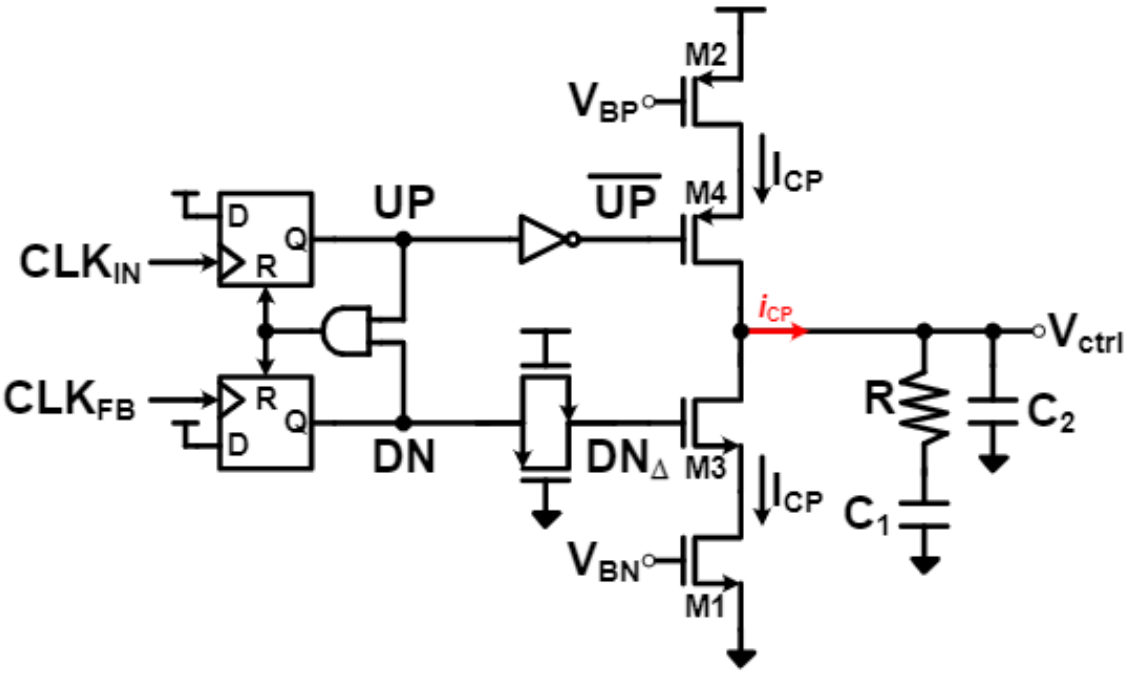

Figure 2.20: Charge Pump with Transmission Gate compensation

To get around this problem a Fanout of inverters can be used leading up to the switch of the charge pump as shown in Figure 2.21. By Utilizing a different fanout to match the edge rates and delay of the UPB and Down signals. With equal fanouts, one can try to use a Transmission gate to get proper matching for the delay of the two signals, but this needs to be properly designed or else it will lead to reference spurs [19].

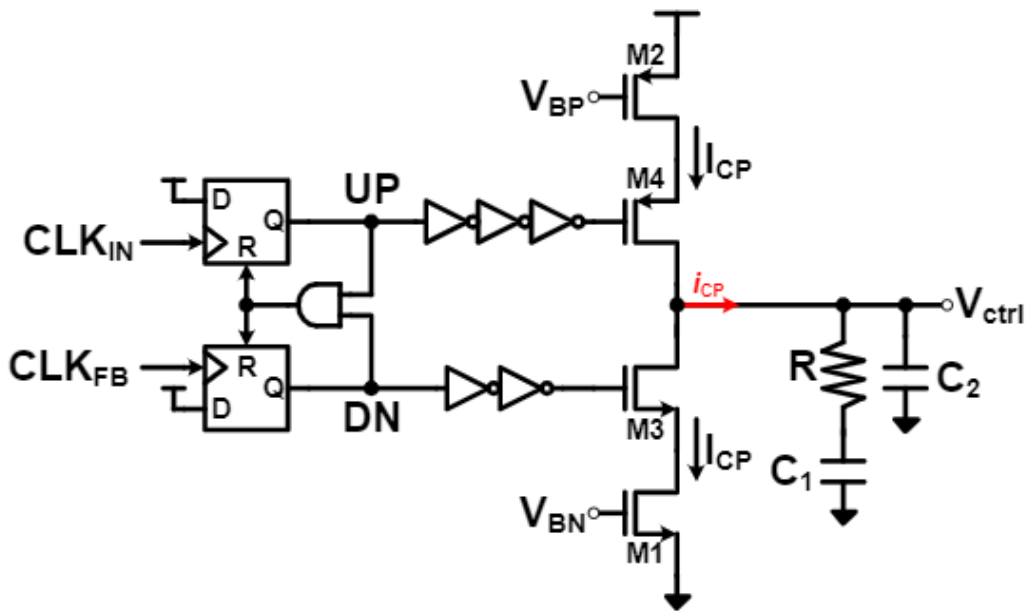

Figure 2.21: Charge-Pump with Fanout difference for matching

The Phase Offset created by the charge pump mismatch can be characterized by:

$$\phi_{os} = 2\pi\left(\frac{\Delta I}{I_{CP} - \frac{\Delta I}{2}}\right)\left(\frac{T_{rst}}{T_{ref}}\right)$$

This shows that the phase error created by the charge pump is a function of the reset delay and the mismatch from the charge pump. So, in order to get good performance, it is critical that the charge pump mismatch is minimized along with the reset delay to ensure a minimal phase offset. This phase error will result in more time domain spurs on the control voltage leading to even more ripple [20].

2.2.4 Divider Overview

A simple divider will divide an output frequency by whatever divisor the circuit is designed for. The simplest divider is implemented by two D-Flip-Flops, which can be shown in the following Figure 2.22.

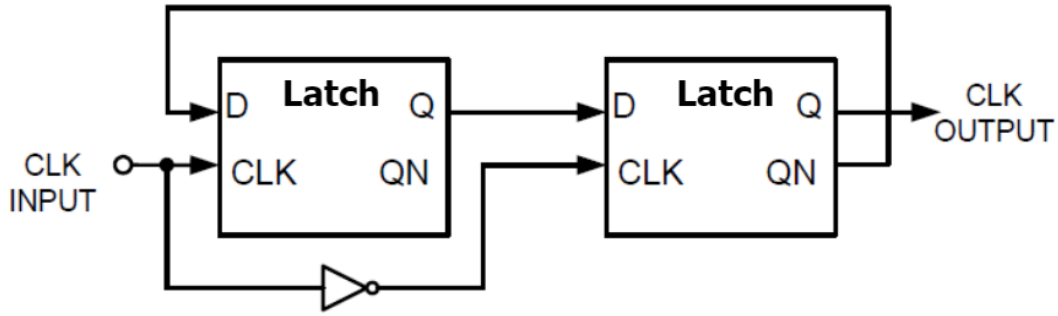

Figure 2.22: Divide by 2 Circuit

The benefit of these circuits is they are somewhat fast and easy to implement but can only provide integer of two divide ratios. This can be cascaded in order to divide by a higher ratio, but because of the limitations of only being able to divide by an integer of 2. A more useful implementation is using a modulus pre-scaler. A modulus pre-scaler can divide by either N or N+1, for example, a divide by 3 circuit can be shown in Figure 2.23. Assuming Q1 and QB2 are both equal to 00 then after Q1 goes to zero and then QB2 will go to one, then in the next three cycles we see Q1 and QB2 go to 10,11 and 01. Because if we remove the and gate from the circuit, it would just be a divide by 2.

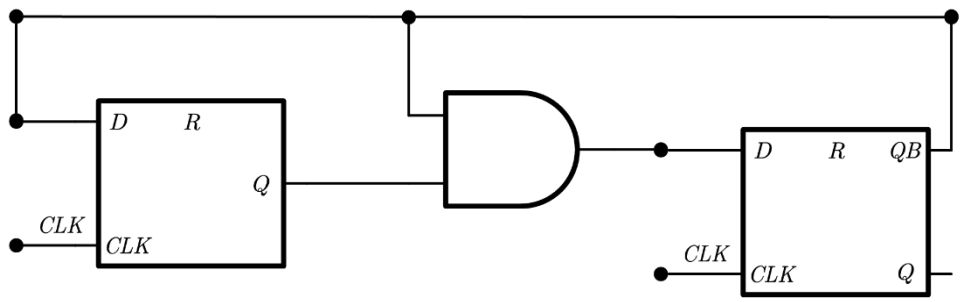

Figure 2.23: Divide by 3

We can add a modulus control as shown in Figure 2.24, resulting in a divide by 2/3 circuit. If MC is low then the circuit will look like a divide by 3 circuit but if MC is high then the circuit will only look like a divide by 2 circuit.

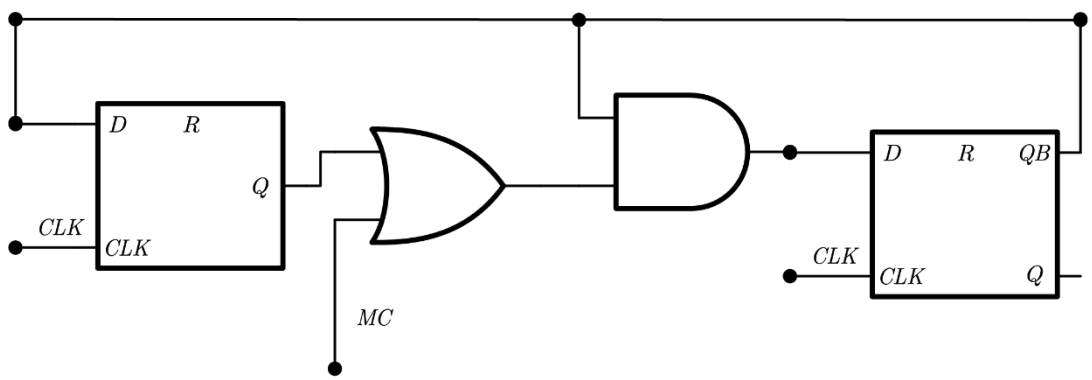

Figure 2.24: Divide by 2 or by 3

For a faster implementation of a divide by 2 circuit which is typically required at very high speeds, a CML divide by 2 circuit can be implemented before the modulus prescaler in order to reduce the frequency so CMOS logic can divide the signal down further. Some downsides of doing this is that there is a large power draw, so it typically is

not worth it at lower speeds. It also requires a differential input and there will be a tail current source [20]. This divider is shown in Figure 2.25.

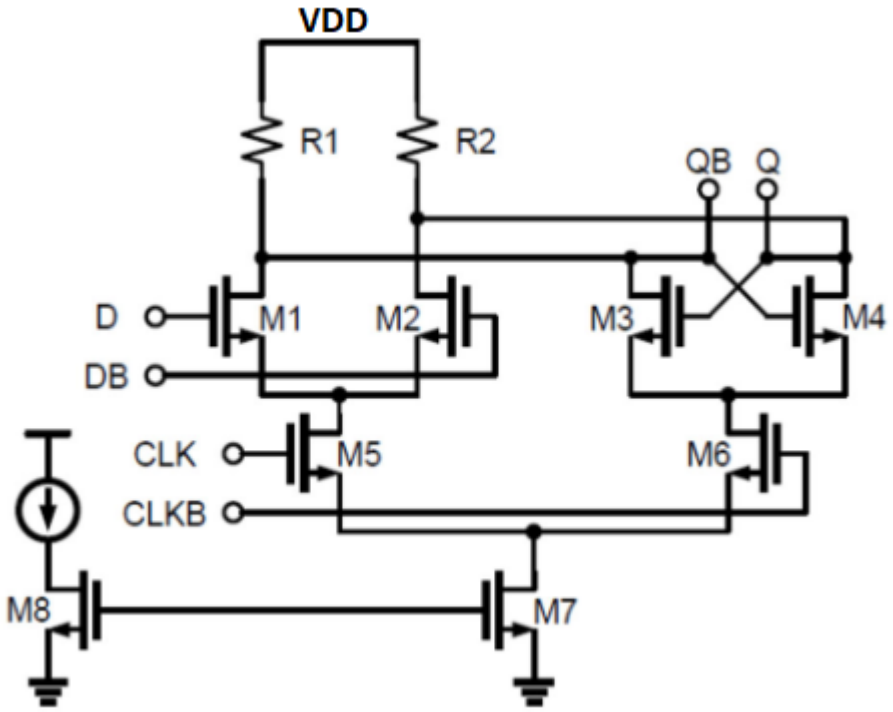

Figure 2.25: CML Divide by 2

In order to have a controllable divider, a Pulse Swallow Counter can be implemented as shown in Figure 2.26. The Pulse Swallow counter works by having the prescaler count by N+1, so every N+1 pulse, the program counter will count the output of the prescaler until the swallow counter's count reaches the S value, in which case then the swallow counter will change the modulus control. This means that the program counter requires P-S pulses to count up again. The prescaler will produce P-S pulses to fill the program counter. So the main input will receive N(P-S) pulses, thus resulting in the total number of pulse equal to (N+1)S+N(P-S) which equals the divide ratio being NP+S.

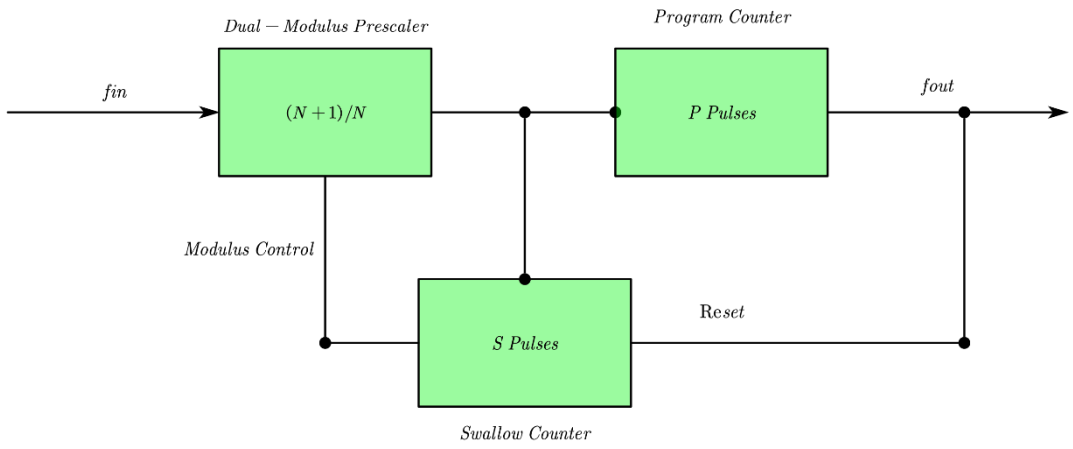

Figure 2.26: Pulse Swallow Counter

The Pulse Swallow Counter gives the most control over the divider, while still being able to operate at a high frequency. The downside of using this architecture is that it can only divide integer wise and cannot divide fractionally [21].

2.3 Radiation Hardening Techniques in LC VCO's

In LC VCO's, the main contributing factor to a phase shift from a Single Event Upset is that from an interaction with varactor [22]. This will typically lead to a positive phase shift in the varactor. The varactor's can be a large area of an LC VCO, so this can be a critical concern [22]. A typical varactor will be implemented with an NMOS where the drain and source are tied together letting this node act as a capacitor. In the case of an NMOS cap, the n-well will act as a collection junction for a single event effect. The charge will be accumulated, and the charge collected will then flow to the substrate, which will result in a change in voltage on the control node of the VCO/ PLL. This will result in a

change in frequency of the VCO, because of the tuning curve changing the frequency and this will cause an accumulated phase error over time. [22]

A decoupling scheme can be implemented to alleviate this burden, by grounding the N-Well of the varactor, the charge that is inject will be immediately grounded [22]. The decoupling scheme can be shown in Figure 2.27. Another sensitive node that may be vulnerable is the IBIAS node, because any transient current that is injected here will be mirrored over N-Times due to the mirroring ratio of the current mirror. Most VCO's use a large current mirror in order to save power.

From a Total- Ionizing Dose perspective, the active devices will have their transconductance shifted due to the charge accumulation on the oxide and this can lead to failure of the VCO at a high enough dose because the cross coupled pair will no longer be able to provide sufficient transconductance to oscillate [23].

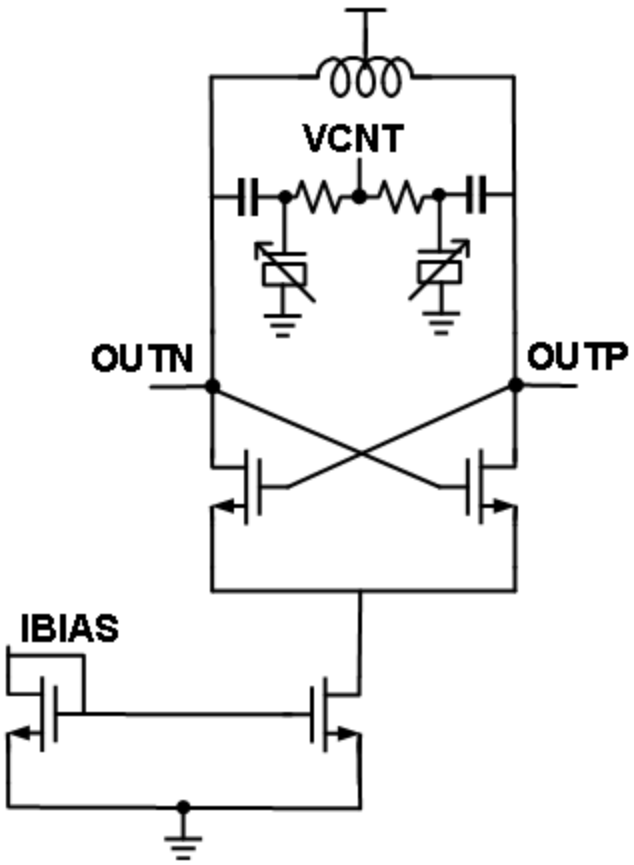

Figure 2.27: LC VCO with decoupling scheme

The downside of using this scheme is that because there is an addition resistor and capacitor in the system, this will degrade the noise performance from the system because of the 4KTR noise and the additional capacitor will reduce the operating frequency which also must be accounted for. So overall, this scheme will reduce the performance of the VCO electrically but improve the radiation tolerance of the system [23].

2.4 Radiation Hardening Techniques in PLLs

Because a PLL is a mixed signal circuit, the PFD and Divider need digital fixes for a radiation event. Whereas, the VCO and the Charge Pump are analog circuits and relatively robust to a single event effect but can completely fail due to TID effects if the total dose is high enough. This is because the threshold voltage will shift until the charge pump no longer operates correctly.

To harden digital circuits again radiation strikes from single event effects, triple modular redundancy is a very popular topology to use. It works by replicating the main logic unit three times and then passing the output through a voter so that as long as two of the logic units have not been corrupted then the output will be correct. This can be illustrated in Figure 2.28.

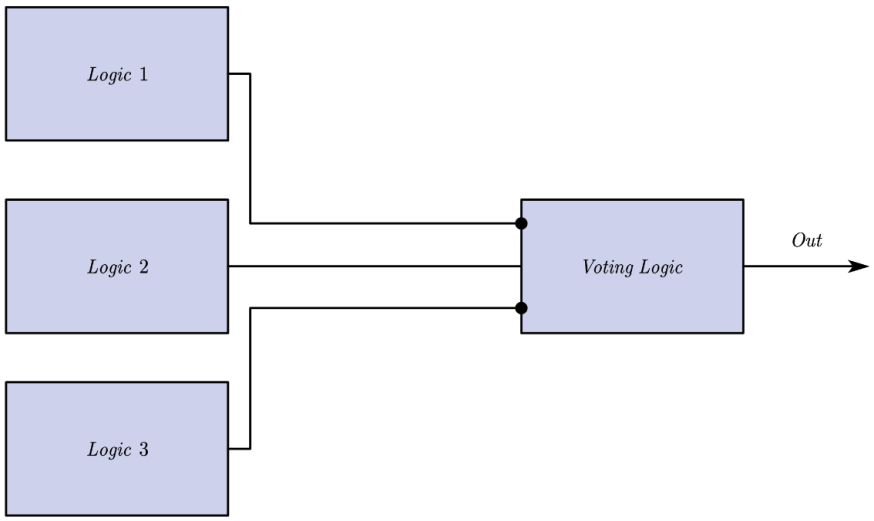

Figure 2.28: Triple Modular Redundancy

The voting unit can be implemented in a variety of ways, but the most common way is by using 4 nand gates as shown in Figure 2.29 [23]:

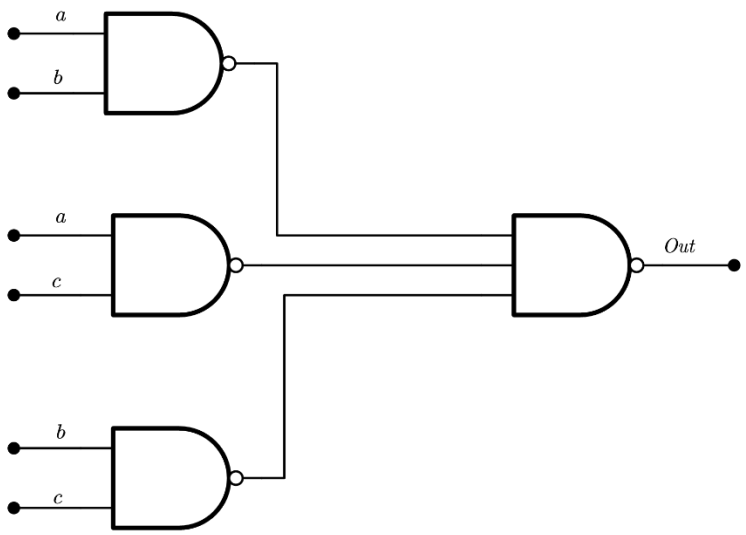

Figure 2.29: Voter Implementation

The truth table for a voter can be seen as:

a	b	c	Out
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	1	0	1
1	1	1	1

Table 2.1: Voter truth Table

The downside of triple modular redundancy is that it will increase the power by three-fold and increase the area by three-fold as well [24]. Another technique for digital logic is to implement a solution at the transistor level as shown in Figure 2.30. This circuit will help harden CMOS logic against TID effects, because when V_i is low, then the output of the lower inverter will go high. In this case, the lower nmos transistor will have a

negative V_{GS}. This will reduce leakage current improving the response to a threshold voltage shift.

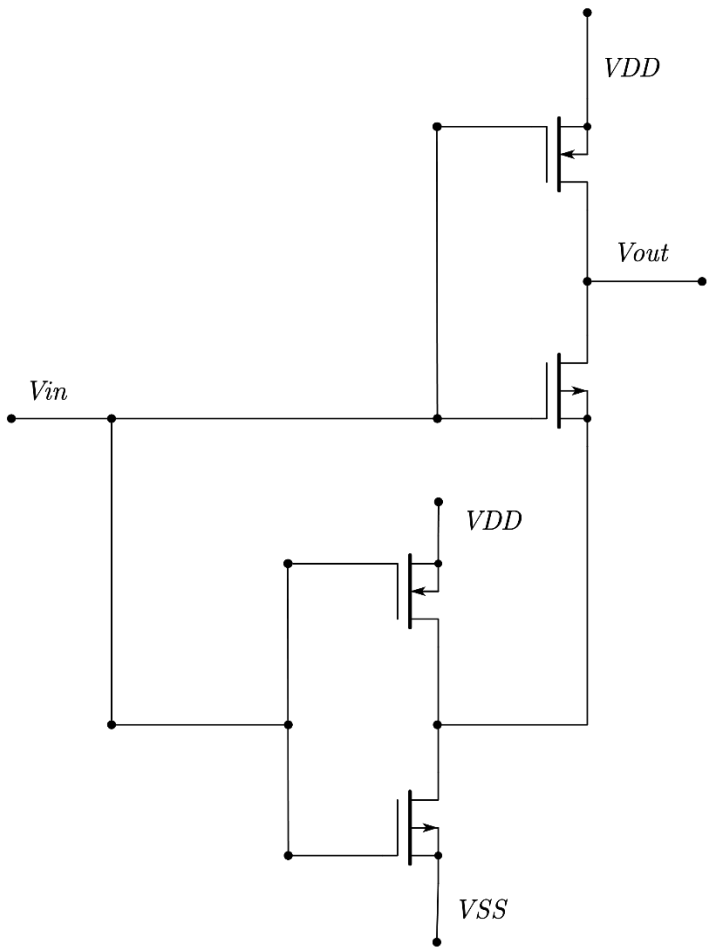

Figure 2.30: RHBD Inverter

The downside of this, is that completely new logic cells that consume more power and more area when on will have to be designed. Also, they will be inherently slower as the size is effectively doubled.

Charge Pumps are dynamic push-pull circuits as previously mentioned, if there is no feedback then a charge pump may be susceptible to single event effects, however if the feedback system as shown in Figure 2.31 is implemented, then the OTA will be

compensating for any change in the system dynamics in order to match the up and down currents.

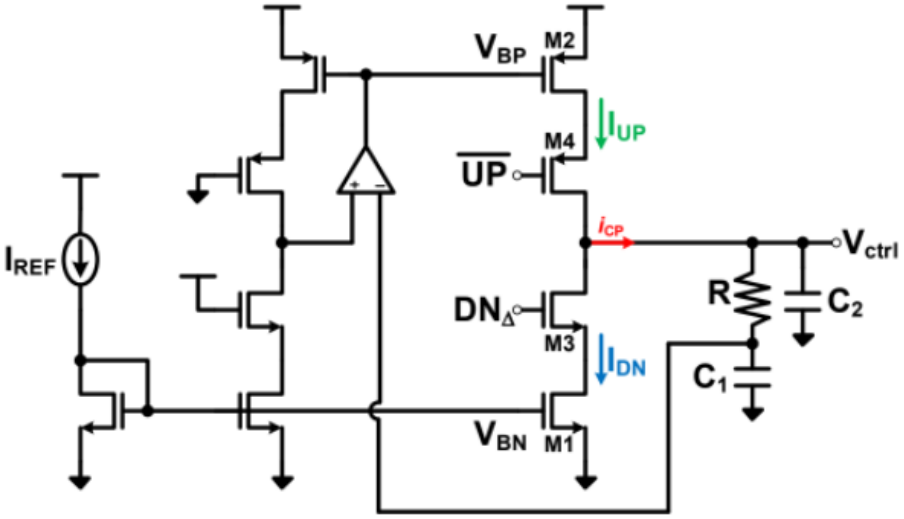

Figure 2.31: Charge pump with OTA feedback

A possible sensitive node is I_{ref} because again, any charge that is deposited on this node may lead to the down current increasing and changing the control node, but this will eventually settle. In order to harden this node, a RC filter can be added to this node in order to increase the time constant, so a SEE will not disrupt the current flow in the other branches.

3. RADIATION HARDENED VCO ARCHITECTURE

3.1 VCO Architecture

In order to evaluate the robustness of a radiation hardened by design VCO, a non-radiation hardened design was implemented as a comparison. The LC-VCO was implemented with an NMOS current mirror, as it was found that in this 22nm FINFET process that the NMOS transistors are less noisy than their PMOS counterparts. The standard LC-VCO is shown in Figure 3.1.

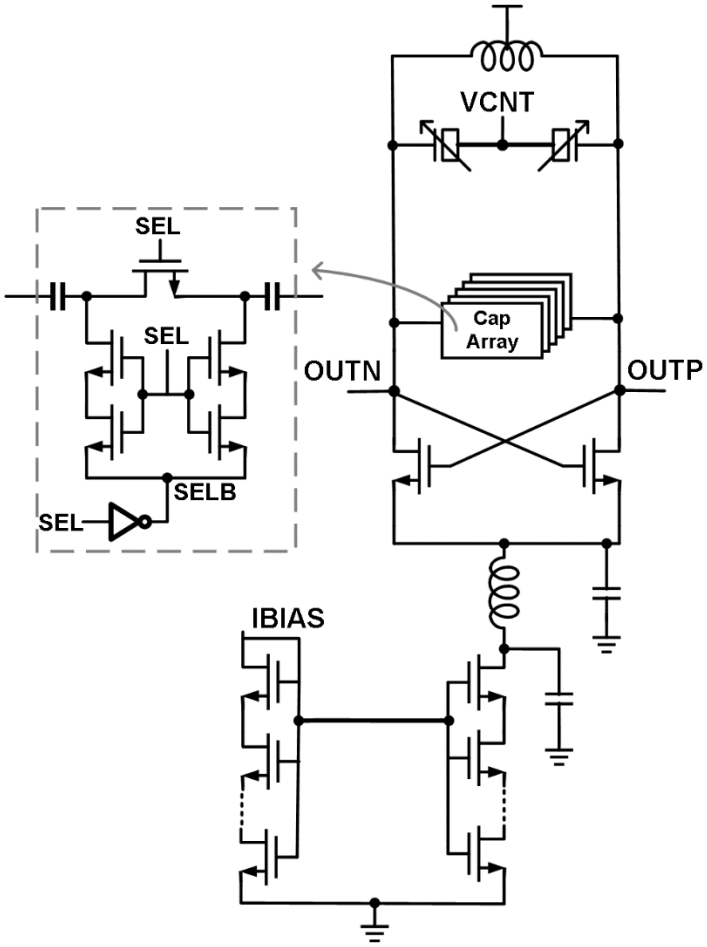

Figure 3.1: Standard VCO Schematic

A capacitor array is implemented in order to increase the tuning range of the VCOs, this will allow the nominal tuning range of standard VCO to be approximately 12.7GHz to 17GHz. The capacitor array uses a high impedance switch shown in the figure to ensure there is very low leakage. The LC filter on the drain of the current source is used in order to filter out higher frequency noise. This is designed to resonate at $2\omega_0$ so at 32GHz nominally for this architecture. In order to make this design radiation hardened, the varactor decoupling scheme shown in Figure 3.2 is used. By grounding the N-Well, this will prevent the control voltage from being pulled down when there is a leakage path from the N-Well to the substrate caused by the SEE.

Another radiation hardening technique that was not used in the first iteration of this design is an RC filter can be applied on the IBIAS node, which will increase the time constant for this node, so an impulse current source will not cause a large change in the voltage, as capacitors resist the change in voltage. The pulsed current will not be mirrored in this case. Future iterations of the chip included this change, and this is a good way to improve the radiation robustness, so it is worth analyzing in this section.

In order to compare the radiation tolerance, three VCOs were tested and implemented to compare their radiation tolerance and electrical performance. The radiation hardened version is shown in Figure 3.2.

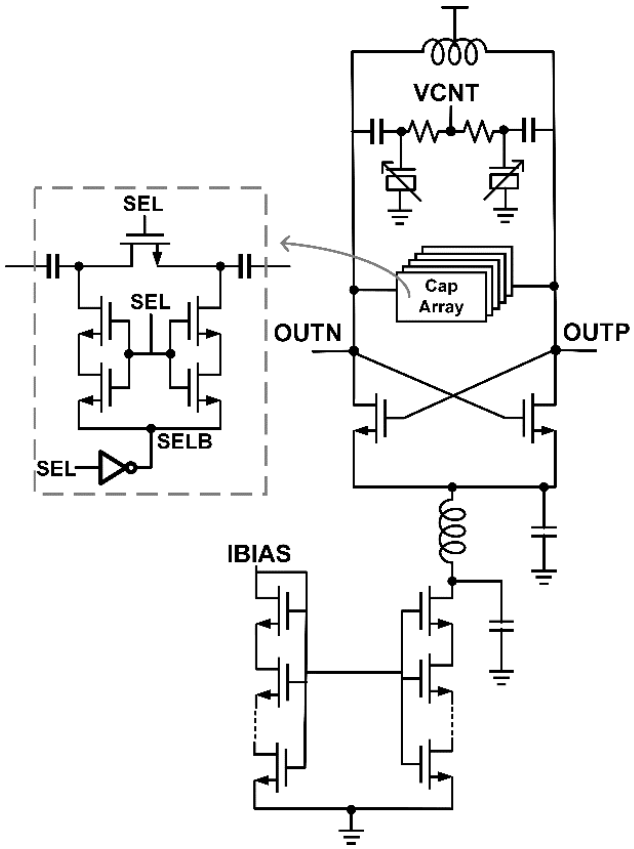

Figure 3.2: Radiation Hardened VCO

The downside of using this scheme is it will introduce another pole into the PLL system, but this is typically at such a high frequency it can be neglected, but what cannot be neglected is the increase in noise that this scheme causes. The phase noise that this scheme introduces can be given by [25]:

$$PN = \frac{4kTR_bK_{vco}^2}{4\pi^2 f^2}$$

Where the noise is thermally introduced by the resistor and is a function of the offset frequency and the gain of the VCO. The third VCO that was implemented is similar to that of the radiation hardened VCO, but it does not include the LC tail filter in

order to see if the filter provide any radiation performance improvements. This is shown by Figure 3.3.

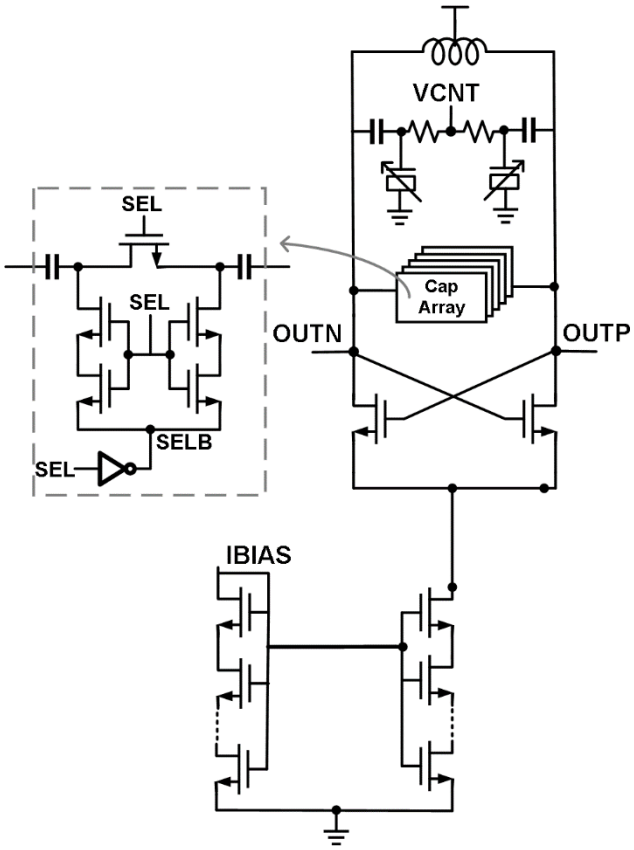

Figure 3.3. Radiation Hardened VCO with no LC filter

The performance of these VCOs will be compared in the coming sections. The NMOS transistors were stacked in order to increase the effective impedance of the current sources. By stacking them, it is essentially like increasing the length of the devices.

3.2 Layout of VCOs

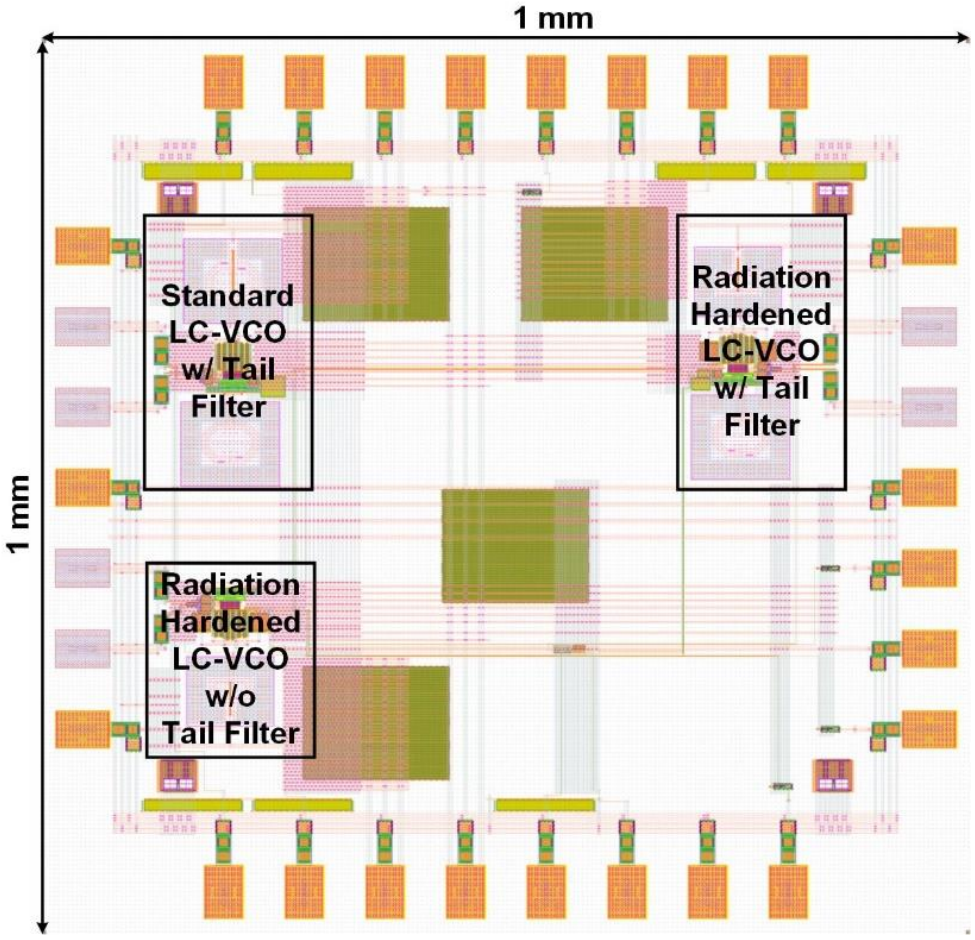

Figure 3.4: Full Chip with all 3 VCOs

The total chip area is $1mm^2$. The total area of the LC-VCO with the tail filter is approximately $0.0276mm^2$ and for the LC-VCO with no tail filter the total area of the VCO is approximately $0.0164mm^2$. The LC oscillator layout for the RADHARD VCO can be seen in Figure 3.5.

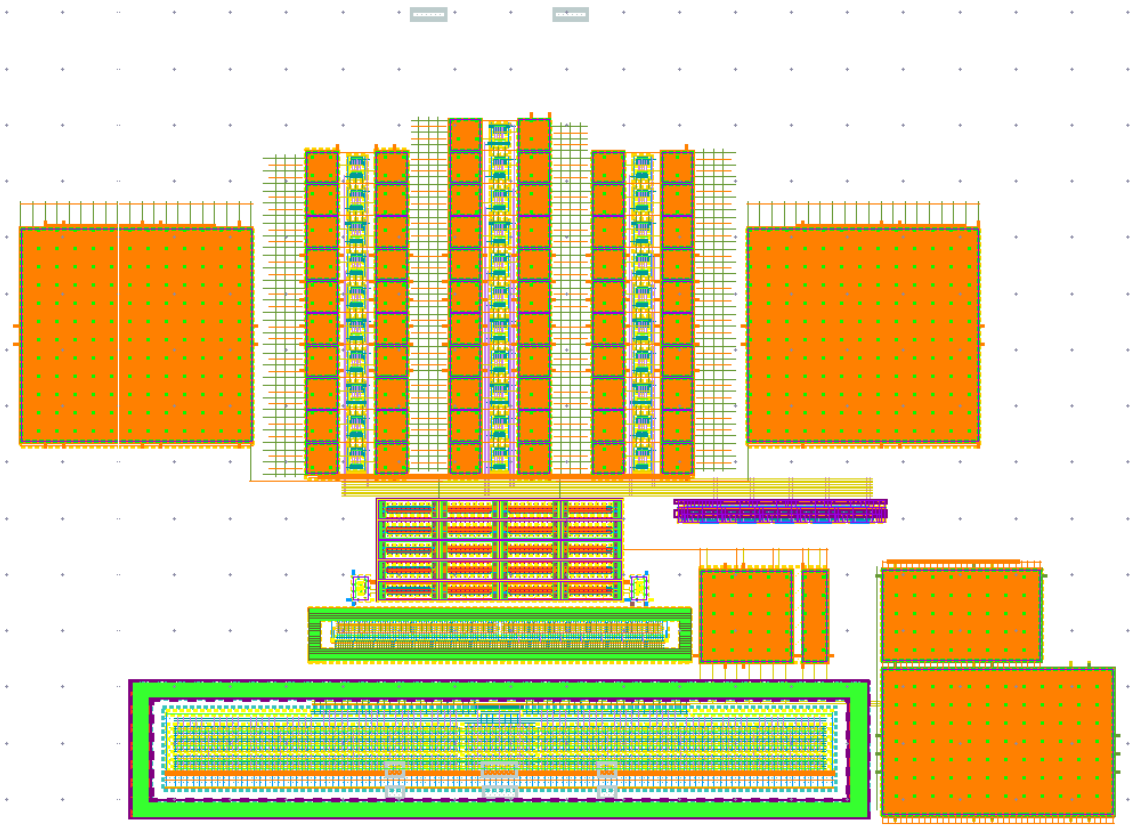

Figure 3.5: Layout for Radiation Hardened VCO

3.3 VCO Simulation Results

The frequency range for the VCOs can be found by sweeping the digital control and the control voltage of the VCO. The tuning bands for the standard VCO is shown in Figure 3.6.

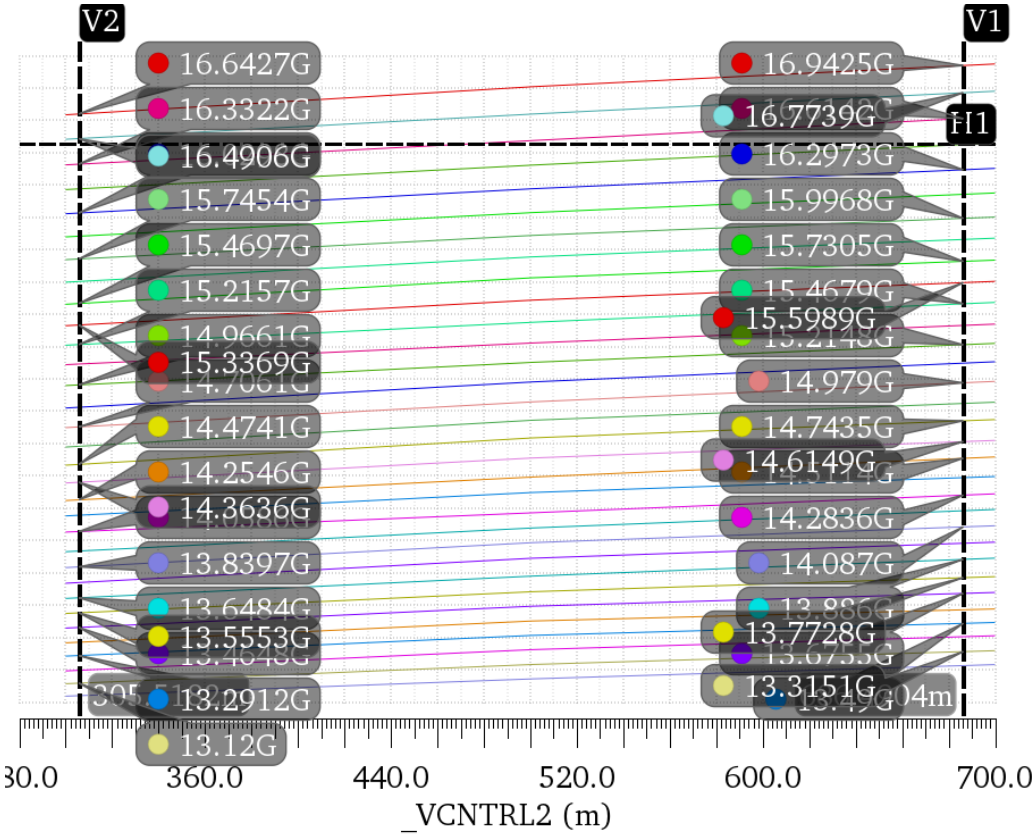

Figure 3.6: Standard VCO Tuning Curve

The tuning range from the standard VCO can be found to be approximately from 13.12GHz up to 16.94GHz. The performance of the VCO tuning range will be degraded by adding the RADHARD scheme, as it will add additional capacitance to the system because of the decoupling capacitor. The tuning range for the radiation hardened VCO can be seen in Figure 3.7.

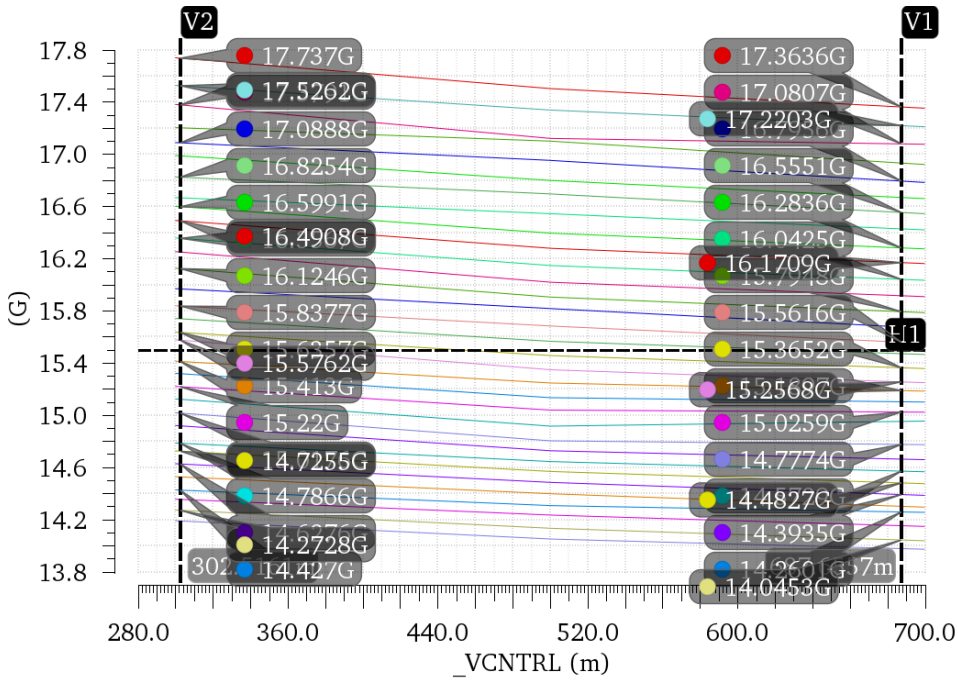

Figure 3.7: RADHARD VCO Tuning Curve

In order to achieve a higher tuning range after parasitics, the inductor sizing was reduced in order to reduce the inductance, which will increase the oscillation frequency. One problem with this is that it will decrease the phase noise performance of the VCO. Because the phase noise is such a critical component of the VCO, this could be detrimental in some systems, so the phase noise needs to be maximized as much as possible. One way to improve the phase noise is to use more current which will also consume more power. The current that was used in these designs was 1mA as the bias current which was then mirrored to 8mA nominally. The phase noise of the standard VCO and the radiation hardened VCO can be seen in Figures 3.8 and 3.9.

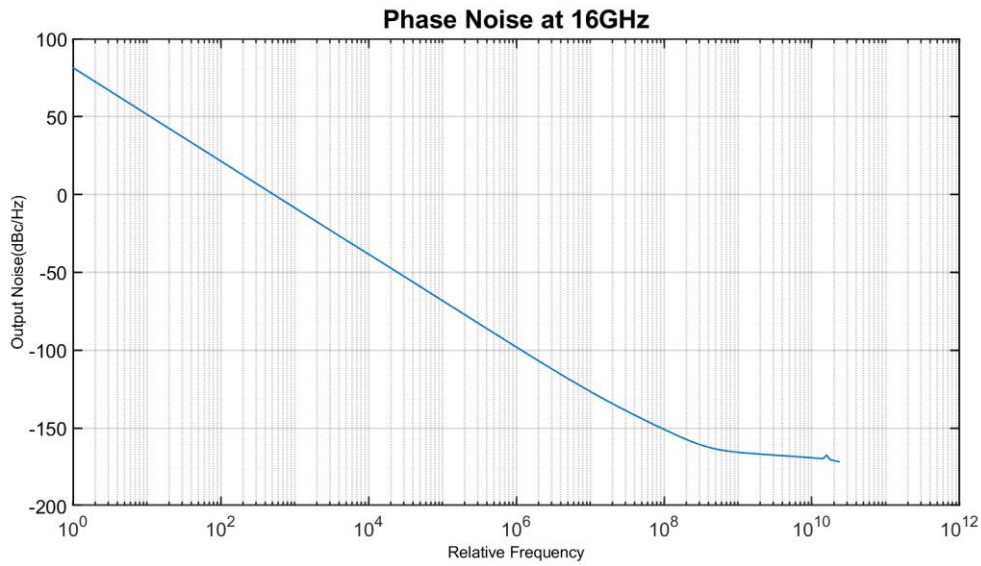

Figure 3.8: Phase Noise of Standard VCO

The phase noise was measured at a 10MHz offset and found to be equal to -126dBc/Hz. This is relatively good performance but could still be improved with more current or by improving the LC coupling technique used.

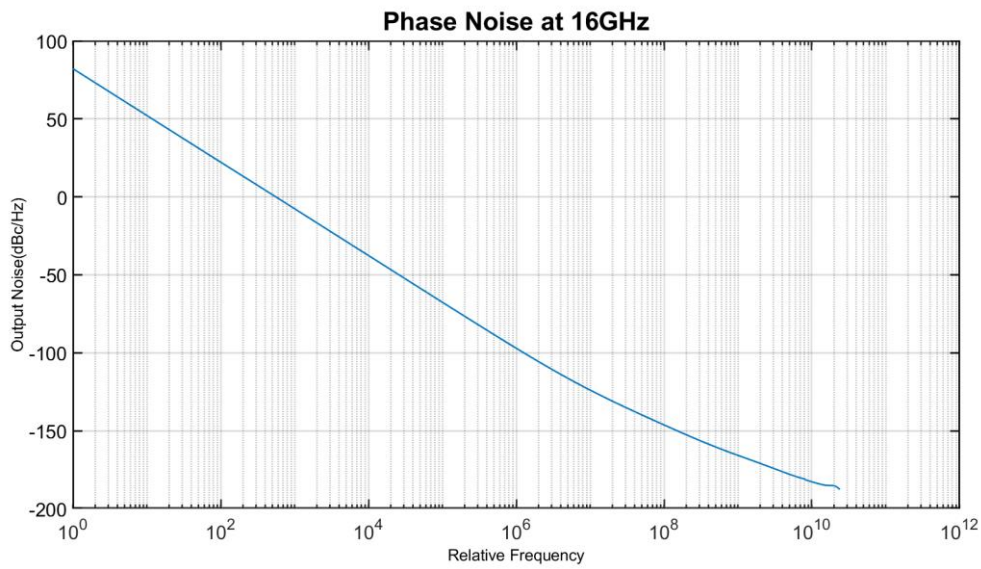

Figure 3.9: Phase Noise of the radiation hardened VCO

The phase noise for the radiation hardened VCO was found to be approximately -124dB/Hz which is about what we expect from the degradation from radiation hardened scheme because of the resistor. The post-fabrication phase noise plots can be seen in Figures 3.10 and 3.11.

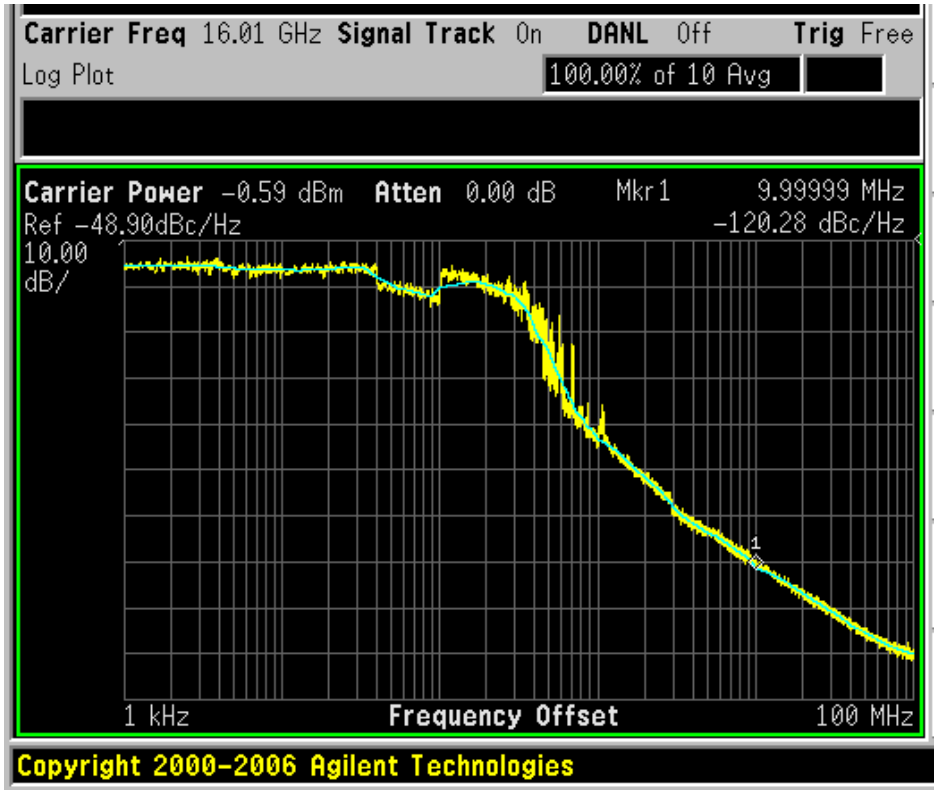

Figure 3.10: Standard VCO Phase Noise Post Fabrication

As can be seen from the figure, the phase noise is shown to be -120dBc/Hz approximately, but a power amplifier with a noise figure between 5dB and 6dBs was used to give the proper carrier power to be accurately measured. This means the actual phase noise is anywhere from -125dBc/Hz to -126dBc/Hz which is the expected value. These measurements were taken with the spectrum analyzer E4446A.

The same setup was used for the radiation hardened VCO for the electrical testing. The phase noise for the post-fabrication can be seen in Figure 3.11.

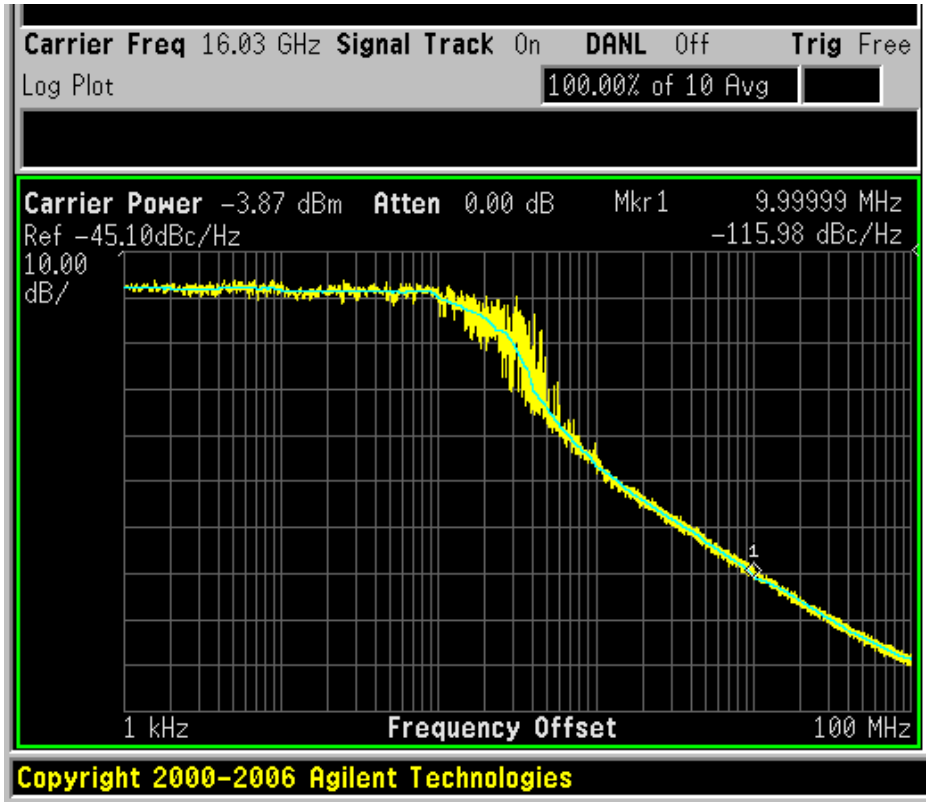

Figure 3.11: Phase Noise of RadHard VCO

The Phase Noise for the radiation hardened VCO is seen to be -116dBc/Hz which accounting for the power amplifier that was used, means that the phase noise is actually approximately -122dBc/Hz which is 2dBc/Hz off of the expected value. The FFT of the signal for the standard VCO can be shown in Figure 3.12.

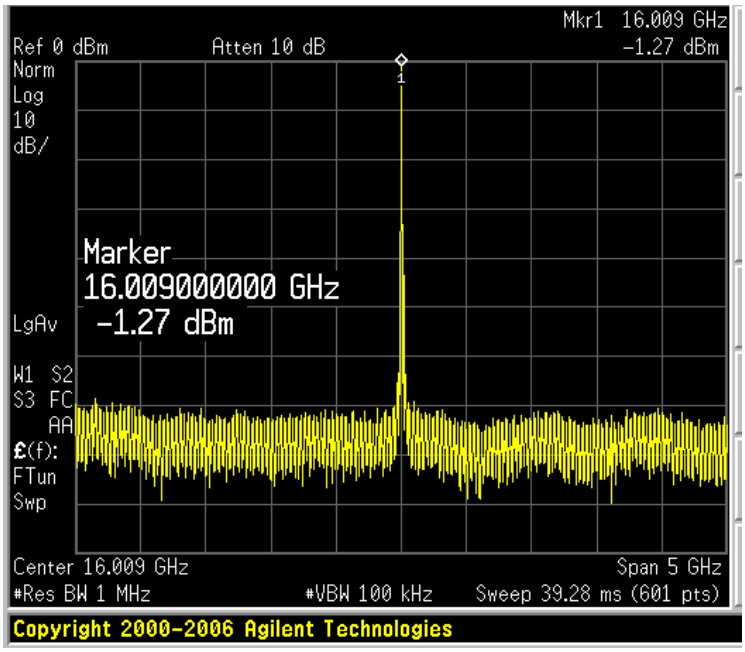

Figure 3.12: FFT of Standard VCO

The FFT for the RADHARD VCO is shown below.

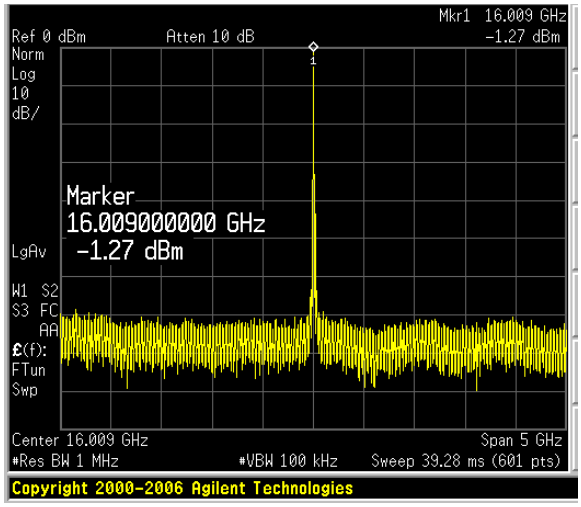

Figure 3.13: FFT of RadHard VCO

In order to test the theoretical sensitivity of each node, a pulsed current source is used in order to emulate a radiation event. Figure 3.14 shows each node that is struck.

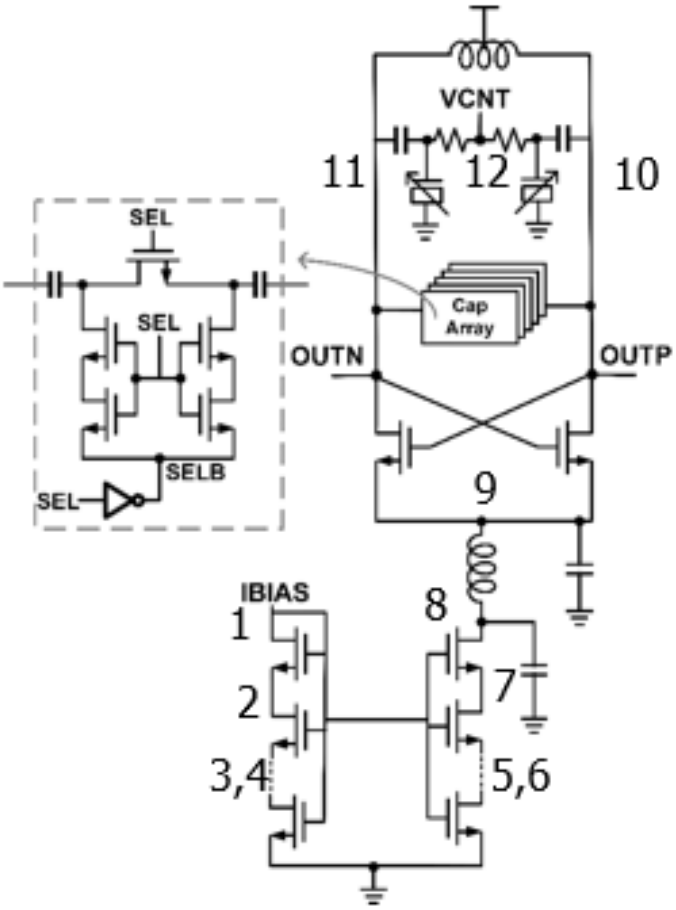

Figure 3.14: Radiation strike locations

Each node was struck to test the sensitivity that it has which corresponds to a frequency, phase, or amplitude shift on the output of the VCO. The results of each node can be seen in Table 3.1 for the standard VCO. The results for the RadHard VCO can be seen in Table 3.2 and the results for the RadHard VCO with no LC results can be seen in Tabl3 3.3.

Stand VCO Node	Recovery Time	Amplitude Error |%|	Phase Error |Radians|
1	6.46E-09	26	1.92
2	5.63E-09	14	0.968
3	4.93E-09	10	0.659
9	4.65E-09	14.04	0.591
8	2.56E-09	14	0.58
4	2.61E-09	4	0.264
7	2.54E-09	4.11	0.216
6	2.54E-09	2.48	0.14
11	2.57E-09	1	0.074
5	1.14E-09	1.1	0.069
10	1.00E-09	1	0.052
12	1.40E-09	0.57	0.026

Table 3.1: Summary of Errors Introduced by Radiation Strikes in Standard VCO

Rad Hard VCO Node	Recovery Time	Amplitude Error |%|	Phase Error |Radians|
1	5.60E-09	53	1.88
2	5.18E-09	25	0.88
3	4.55E-09	17	0.57
9	2.58E-09	18.63	0.438
8	2.30E-09	18.6	0.436
4	4.42E-09	6	0.212
7	3.09E-09	5.7	0.185
6	3.20E-09	3.22	0.137
5	2.70E-09	1.4	0.073
10	1.10E-09	1.4	0.028
12	2.00E-09	0.84	0.028
11	1.20E-09	1.55	0.00709

Table 3.2: Summary of Errors Introduced by Radiation Strikes in Radhard VCO

Rad Hard VCO No L Node	Recovery Time	Amplitude Error |%|	Phase Error |Radians|
1	5.77E-09	45	2.26
2	5.18E-09	23	1.09
3	4.92E-09	15	0.714
8	2.60E-09	19.11	0.389
4	4.32E-09	6	0.286
7	3.27E-09	5.95	0.171
6	3.41E-09	3.43	0.101
5	2.90E-09	1.34	0.036
10	1.10E-09	0	0.0076
12	3.00E-09	0.46	0.003
11	2.00E-09	0.45	0.000000043
9	0.00E+00	0	0

Table 3.3: Summary of Errors Introduced by Radiation Strikes in No-LC Radhard VCO

It can be seen from the table results above that the most sensitive nodes are the Ibias nodes. The next most sensitive nodes are the mirrored nodes on the VCO side of the current mirror. The RC filter shown in Figure 3.15 will help alleviate the sensitivity of nodes 1-4. The pull-down effect that is expected to see on the N-Well of the varactor is equal to the 7th in the list for phase error as shown in Table 3.5. If nodes 10-12 are directly hit this causes very little error along with nodes 5 and 6. So, the may nodes that need to be hardened are the current bias, the tail nodes and the n-well of the varactor.

It can be seen that the most sensitive node is the Ibias node, this makes sense because all of the current that is introduced on this node will be mirrored 8 times to the main VCO circuit. So, to reduce this we can add the RC filter as discussed previously.

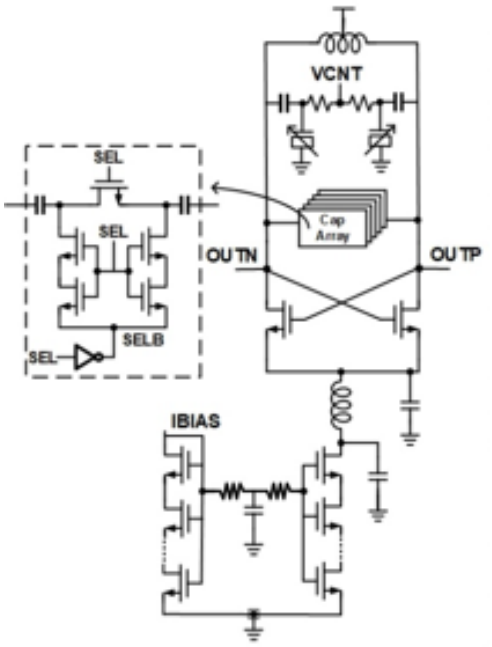

Figure 3.15: VCO with RC filter

The benefit of this can be seen from Table 3.4 as shown below.

RADHARD VCO Node	Recovery Time (Seconds)	Amplitude Error	Phase Error (Radians)
1	None	0	0.0758
2	None	0	0.0675
3	None	0	0.0558
4	None	0	0.0112

Table 3.4: Summary of most sensitive nodes with RC filter

With the added RC filter, the oscillator does not encounter really any amplitude error, but it does still encounter a permanent phase shift. In a real PLL system, this will be corrected for by the system, but a large phase error would be much more detrimental.

In order to show the improvement of the varactor scheme, a pulsed current source is added to the N-well of the varactor acting as a Single Event Upset. As discussed in previous sections, an ionizing radiation will create a pulsed current from the N-Well to the substrate pulling charge away from the control node. This will cause a drop in the control voltage leading to an instantaneous phase and frequency shift. The results of the standard varactor compared to the radiation hardened VCO can be shown in Table 3.5.

	Frequency Shift (MHz)	**Phase Shift |Radians|**
Standard VCO	412	0.1709
RADHARD VCO	0	0

Table 3.5: Standard Vs RADHARD VCO

Because the N-well is grounded, there is no frequency or phase shift that occurs in the radiation hardened version, but with the standard version there is a significant phase and frequency shift. The pulsed current source that was implemented was one of the worst-case scenarios of having a pulse width of approximately 1ns. For my particular layout, this results in approximately an 11% increase in the insensitive area, shifting it from 55% to 65% of the total area being insensitive. With the RC filter scheme implemented, this increases as well to approximately 90% of the area being robust as the current mirror is a large portion of the area.

4. RADIATION HARDENED PLL ARCHITECTURE

4.1 PLL Architecture

The radiation hardened PLL was designed with predominantly Single Event Effects in mind, the design was also tested for TID in simulation by shifting the threshold which was previously discussed as an effective way to simulate TID effects. The schematic design was implemented with triple modular redundancy in the digital blocks to prevent an upset to the state machine. This is also done for the divider blocks as well. The overall schematic can be seen in figure 4.1.

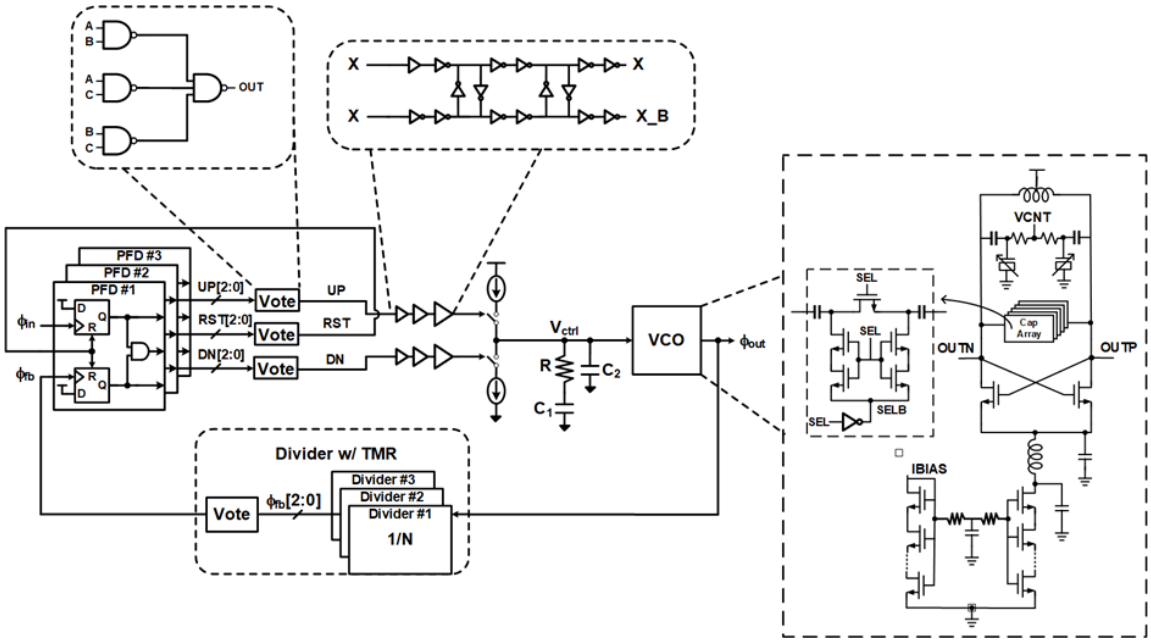

Figure 4.1: PLL Schematic

The PFD was designed with the fanout leading u to the charge pump in mind to appropriately drive the charge pump switches. The delay between the UP, DWN, UPB and DWNB is designed to be matched exactly in order to appropriately drive the charge pump. The PFD implementation can be seen more closely in figure 4.2.

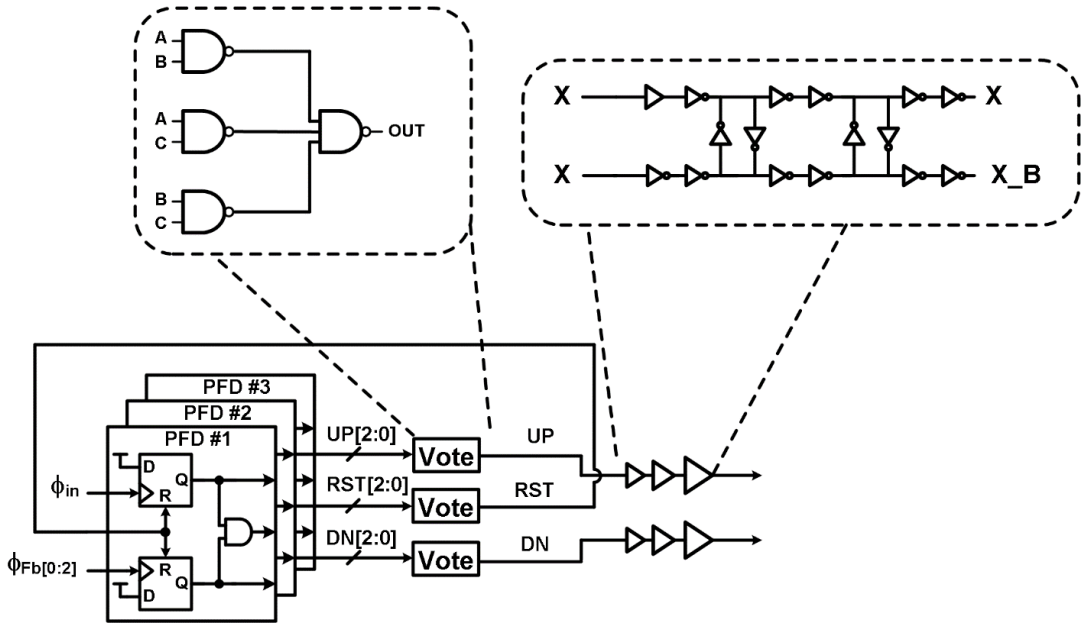

Figure 4.2: PFD schematic

The charge pump schematic is shown in Figure 4.3, where the RC filter scheme is implemented on the bias node of the charge pump in order to reduce the sensitivity to a Single Event Effect. The feedback Op-Amp is used in order to set the PMOS gate voltage in order to try to set the PMOS current equal to the NMOS current for better matching. The unity-gain feedback OPAMP is used to try to keep the output common mode constant in order to reduce dynamic charge pump mismatch.

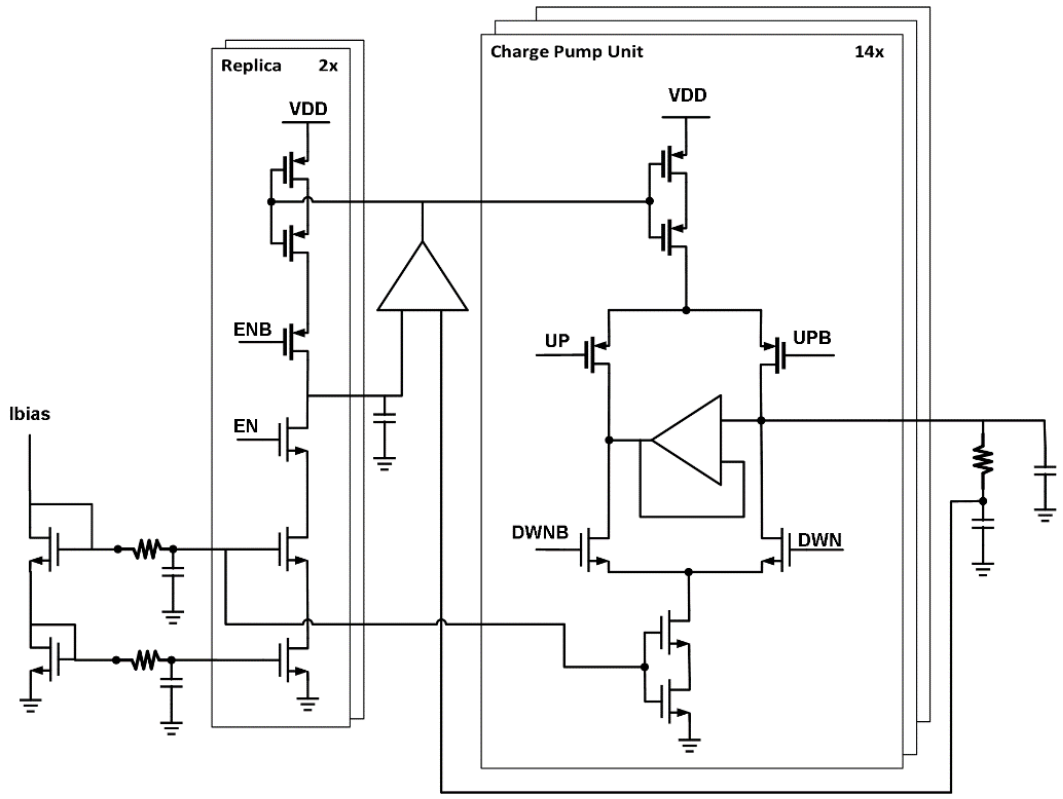

Figure 4.3: Charge Pump Schematic

The VCO was discussed in the previous section. The divider was implemented with a pulse-swallow integer divider as discussed in a previous section. The divider was implemented in Verilog and then synthesized and placed and routed. The input and output of the divider has a voter so that the PLL will not incur a cycle slip if there is a radiation strike on the digital blocks. Because this will cause a bit flip. The overall PLL specifications are shown in Table 4.1. The specifications were derived from matlab code using the transfer function of the PLL in order to find the phase margin, loop bandwidth, etc.

PLL parameters	Specifications
Ref clk frequency	100MHz
CLK frequency	14-17 GHz
Divider ratio	140-170
Icp	800uA
R	6.5kΩ
C1	30pF
C2	1.5pF
Kvco	1.05GHz/V
Damping Factor	1.32
Phase Margin	65.25°
BW	3-4MHz
RMS jitter(fs)	~40

Table 4.1: PLL Specifications

4.2 PLL Layout

The PLL was implemented in 22nm FINFET, the same as the VCO chip. This PLL was only simulated however, because there was a mistake with the routing from the PFD to the CP and this severely degraded the performance on this iteration of the chip. In a future design that was not this project, the PLL operated at 21GHz and did not encounter this issue. The layout of the chip can be seen in Figure 4.4. The area of the chip is $1mm^2$.

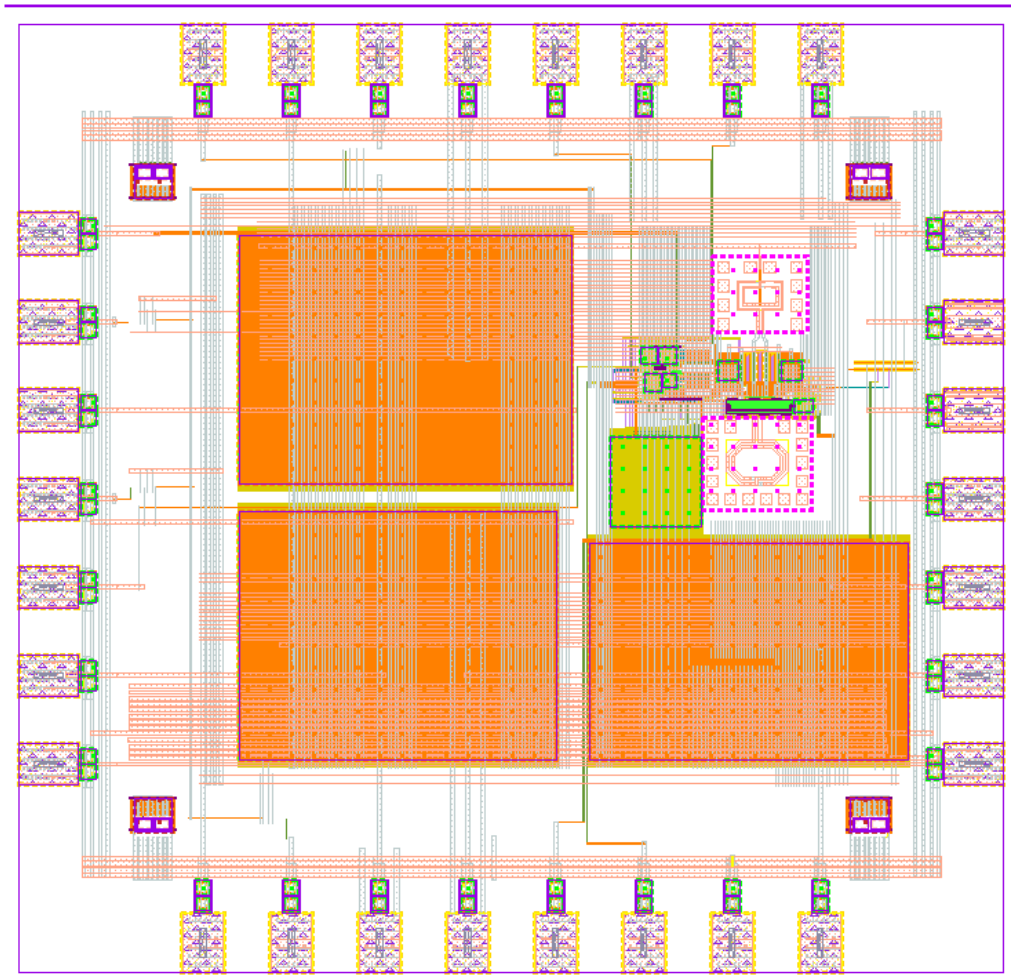

Figure 4.4: Full Chip Layout

The layout for just the PLL is shown in Figure 4.5.

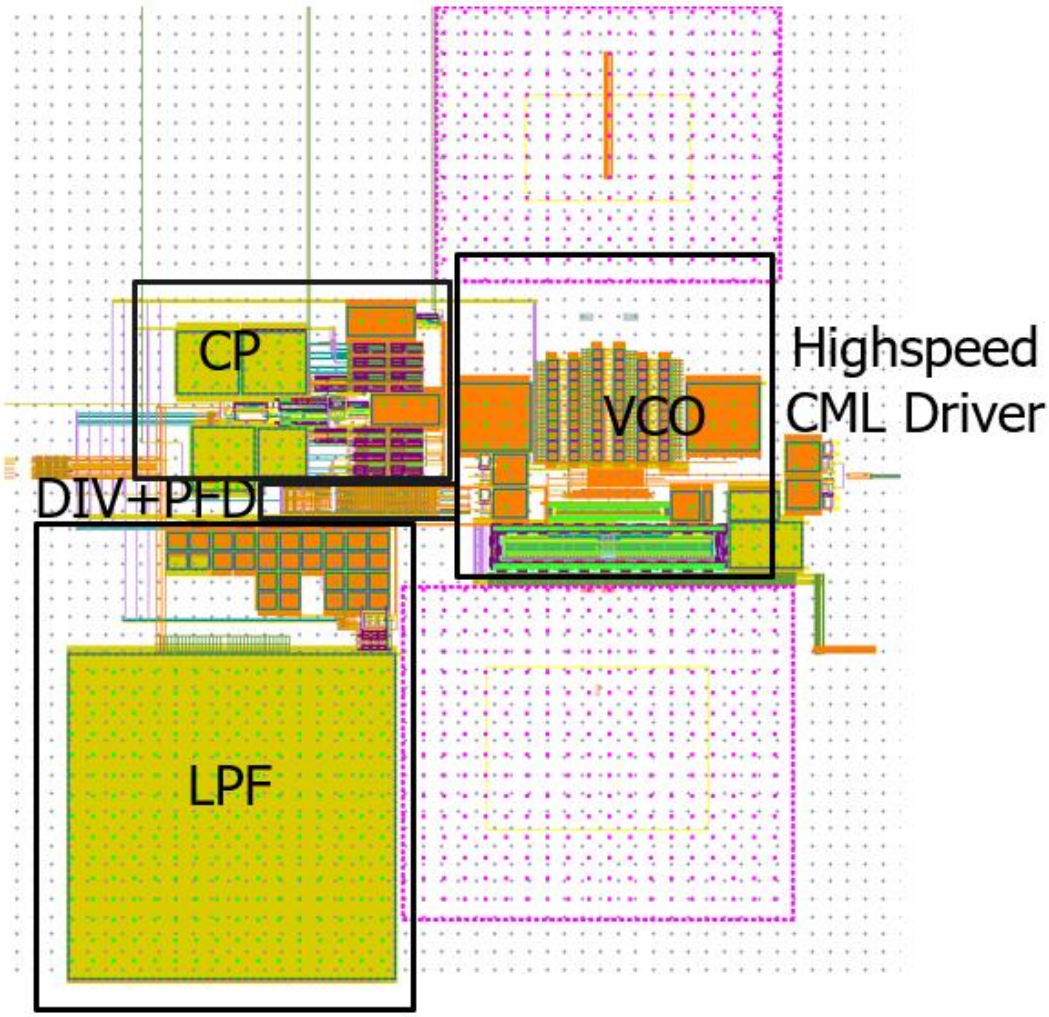

Figure 4.5: PLL Layout

To improve this design in future iterations, CP is moved much closer to the divider and the PFD. This will reduce the parasitics that effect the critical signal routing.

4.3 PLL Simulation

Firstly, the loop specifications were derived from the VCO gain as the initial deciding factor. Since the VCO gain was small, the charge pump current was increased to compensate for this. The closed loop transfer function for the PLL is shown in Figure 4.6.

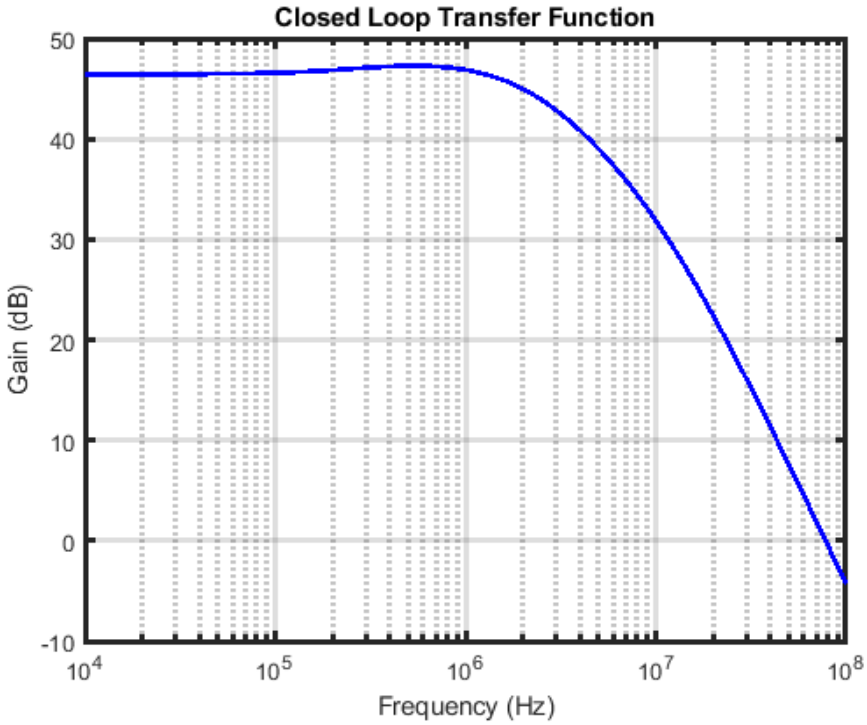

Figure 4.6: PLL Closed Loop Transfer Function

Figure 4.7 shows the nominal locking of the PLL.

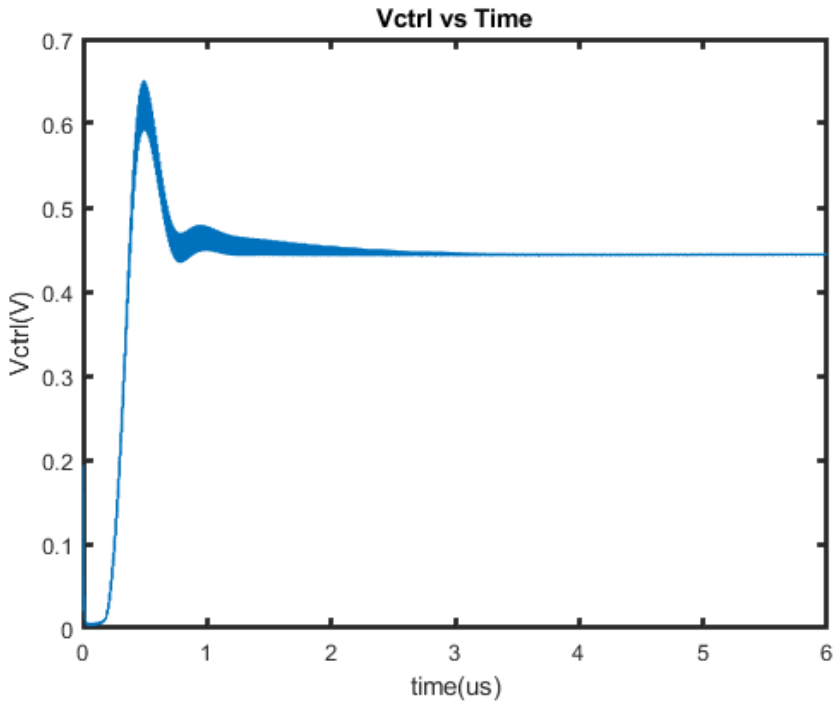

Figure 4.7: Nominal Locking of PLL

After the PLL was confirmed to lock, it was tested for SEE and for TID effects. For the SEE, the device was struck at multiple nodes and the control voltage was observed to see if it would lock or not. Table 4.2 shows which nodes were struck at which time. It is worth noting that other nodes were also struck, but they did not cause any major disruption in the locking of the PLL. Loss of lock for a PLL can be detrimental to the system performance as it will change the frequency which will add more noise to the system and if it takes too long to relock, could possibly increase the BER tremendously. So, both TID and SEE should be tested in order to account for robustness. Only the nominal corner was used in this research, but in the future, it will need to be test for robustness across all process corners.

Strike Location	Strike Time(us)	Loss of Lock
$\phi_{fb} = [1:0]$	1	Yes
Ibias CP	3	No
Vctrl	4	No
Ibias VCO	5	Slight perturbation
ϕ_{out}	6	No

Table 4.2: PLL SEE Strike Locations

Figure 4.8, shows the control Voltage with hitting the feedback voter with two strikes on at each voter input. We see detrimental loss of lock. Hitting the control node directly only results in a small perturbation for approximately 50ns. This will add inherent jitter to the system because the control node is changing.

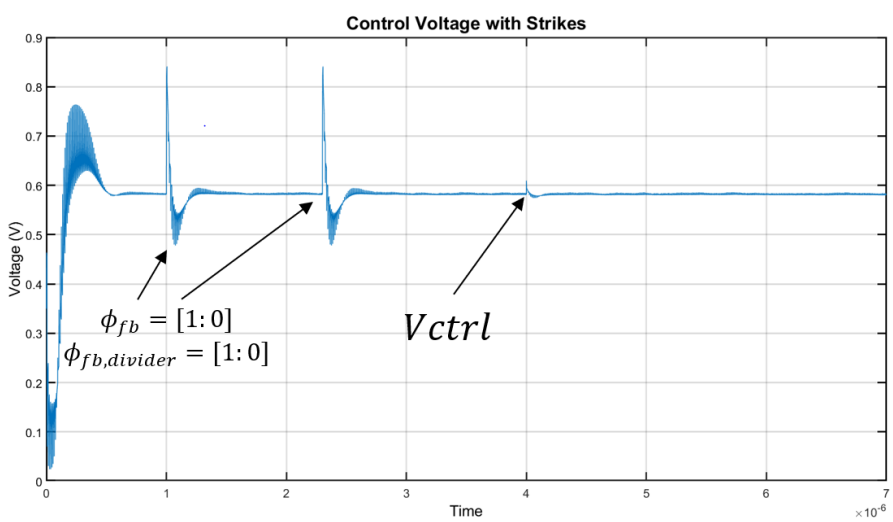

Figure 4.8: Control Voltage Strikes

TCAD modeling was done to emulate the threshold shift in the 22nm FINFET process. This will be discussed further in a future section. The results were used to approximate a threshold shift caused by a total dose. A 20% threshold shift was implemented in the model files to replicate TID effects, where the PMOS will have a positive threshold shift and the NMOS will have a negative threshold shift. The standard PLL control voltage versus the PLL control voltage. There is a clear shift in the loop dynamics, but the PLL is still able to lock. The locking time is increased from a little less than 1 micro-second to over 2 microseconds to completely settle.

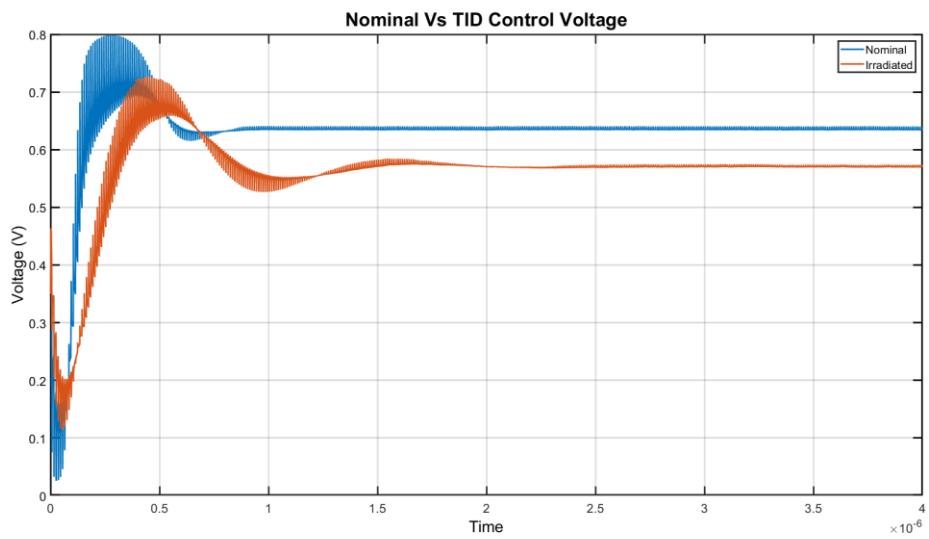

Figure 4.9: PLL Nominal vs TID Locking Performance

In order to accurately characterize the PLLs performance beyond if the loop is stable, the jitter performance will need to be characterized in order to get a more detailed look at the performance. The dual-dirac model will be used in order to characterize the performance of the PLL. The eye diagram for the nominal PLL can be seen in Figure 4.10.

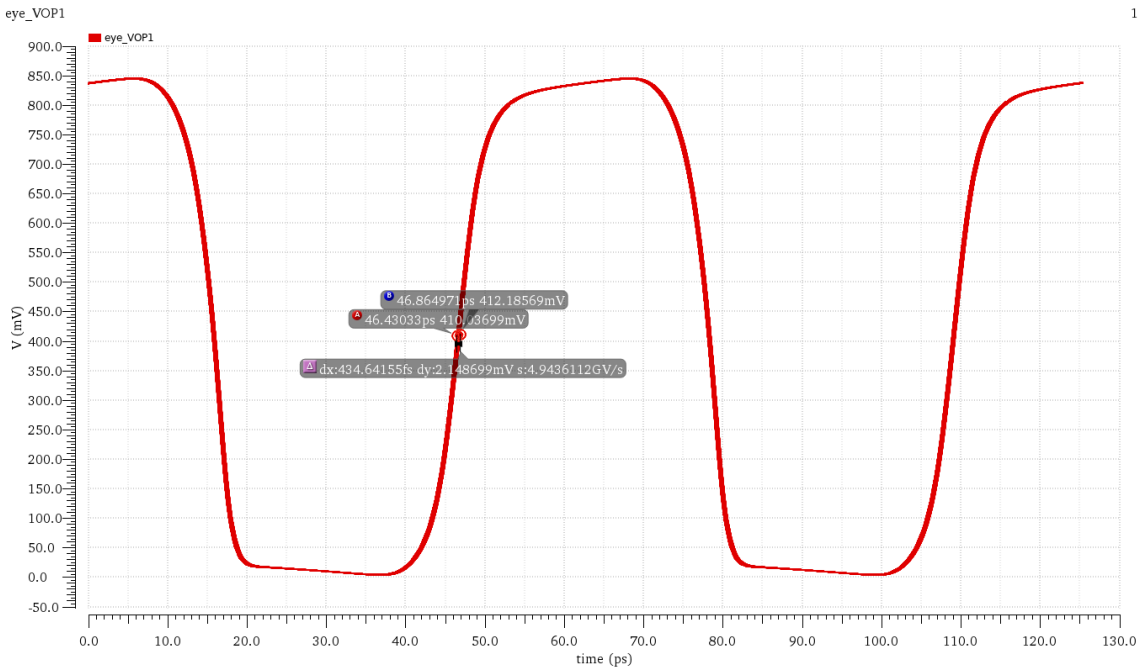

Figure 4.10: Eye Diagram of Nominal PLL

The total peak to peak jitter can be seen to be approximately 434fs. To get the deterministic and rms jitter, a dual dirac model can be used. By converting the eye diagram into an x histogram with a threshold of 425mV we see the X histogram in Figure 4.11. Where the x axis is centered around the weighted average of the distribution. You can convert the probability into a Q function in order to get a more detailed look at the rms and deterministic jitter. This is given by:

$$Q = \sqrt{2}\,\mathrm{erf}^{-1}(1 - \frac{BER}{TD})$$

Where TD is the transition density of the eye which will be 1 in this case.

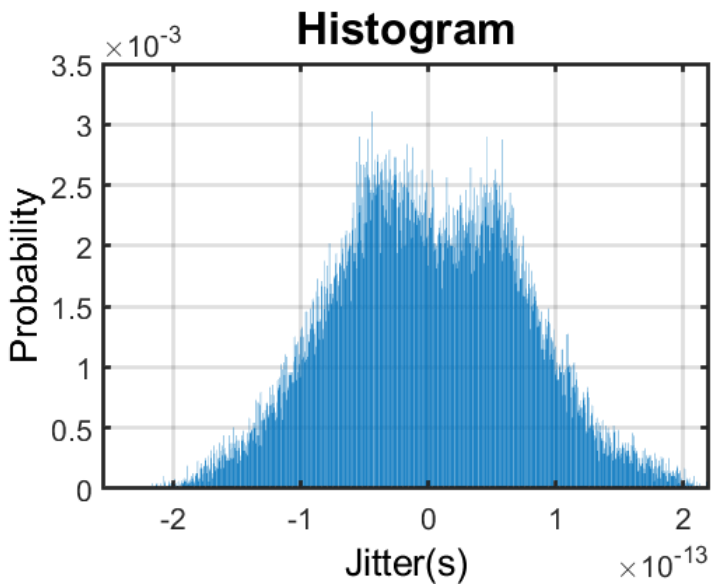

Figure 4.11: Probability vs Jitter

One the previous mentioned equation is used. Figure 4.12 shows the Q vs jitter. From this the rms jitter can be extracted from the inverse of the slope. The deterministic jitter can be found from the spacing of the 0 crossings of the slope which is approximately 200fs. The rms jitter was found to be approximately 40fs in simulation and with a sample size of 50 thousand, a total jitter for this system was approximately 200fs+7*40fs=480fs.

The FFT was used in order to determine the 100MHz offset rejection with respect to the carrier. This was found to be approximately -70dBc. This can be seen in Figure 4.13. This shows that the nominal radhard PLL has good jitter performance along with having a good ripple rejection. The total ripple on the control node was only 4mV which is less than 1% of the supply voltage.

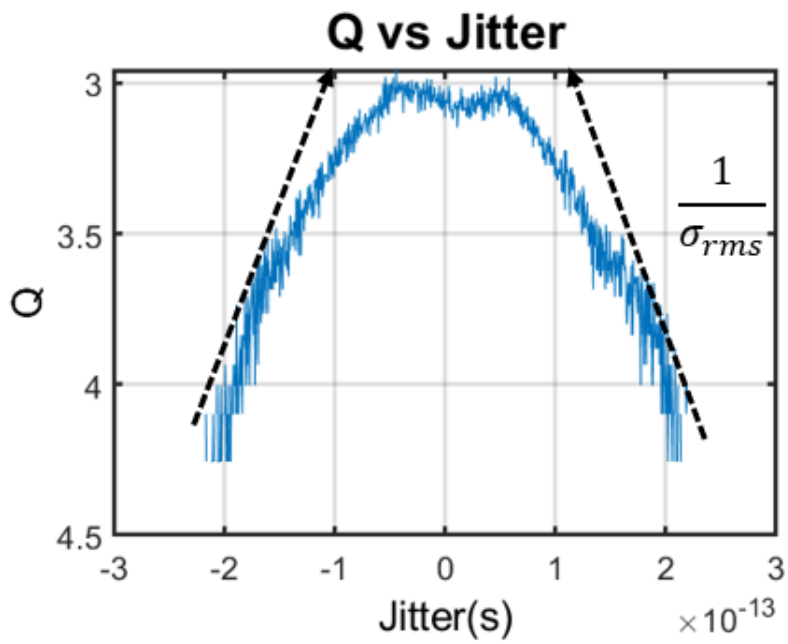

Figure 4.12: Q vs Jitter

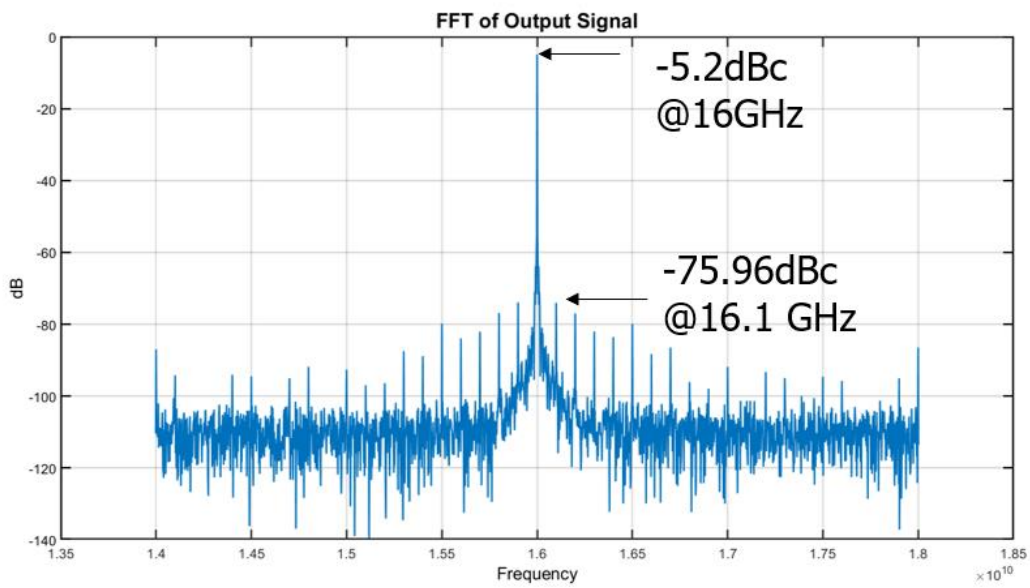

Figure 4.13: FFT of Carrier

The next simulation results are the PLL after it has been simulated with the threshold shifts, simulating a total ionizing dose effect. The eye diagram can be seen in

Figure 4.14. There is a large increase in the total peak to peak jitter of approximately 2.3ps

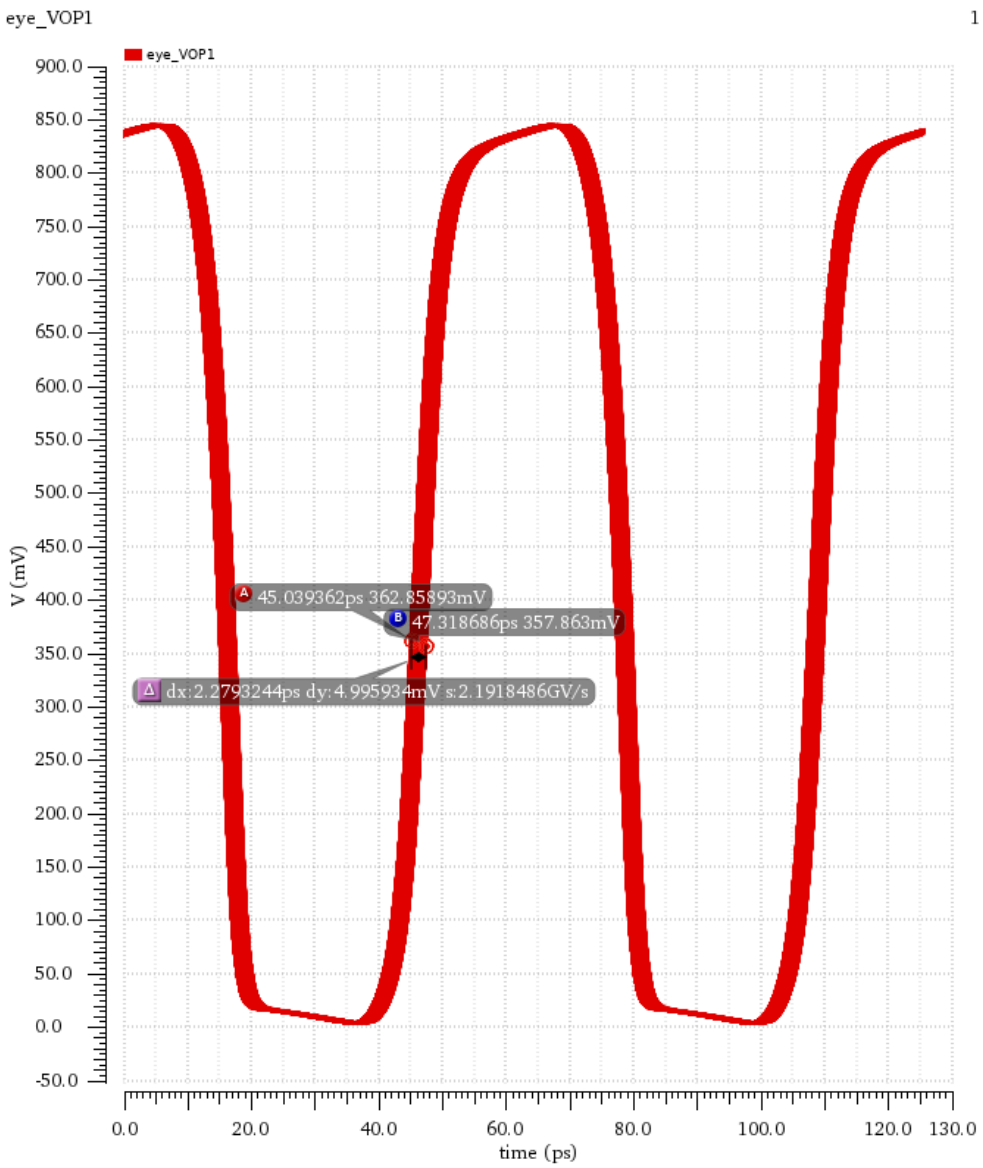

Figure 4.14: Eye Diagram with TID effects

Following the same procedure as before Figure 4.15 shows the X histogram and Figure 4.16 shows the Q vs jitter.

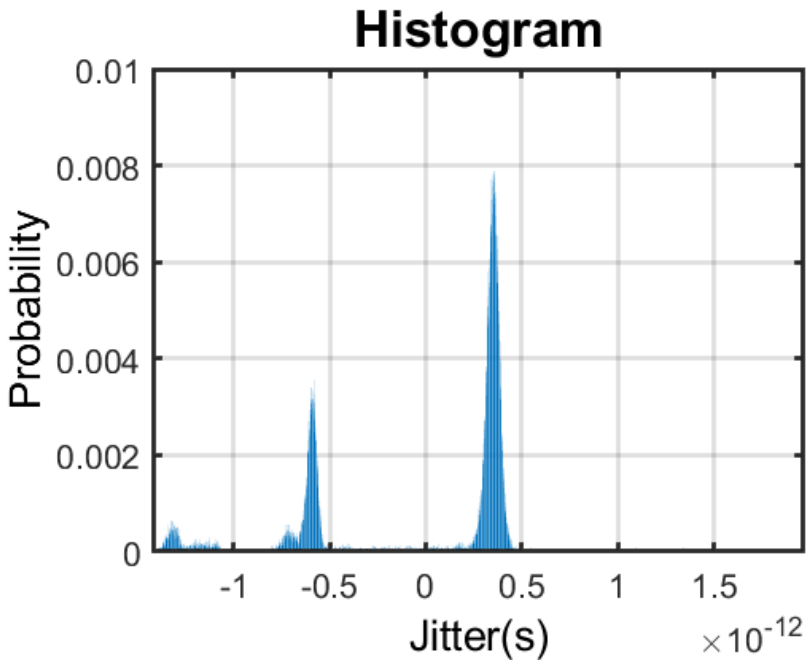

Figure 4.15: X Histogram with TID Effects

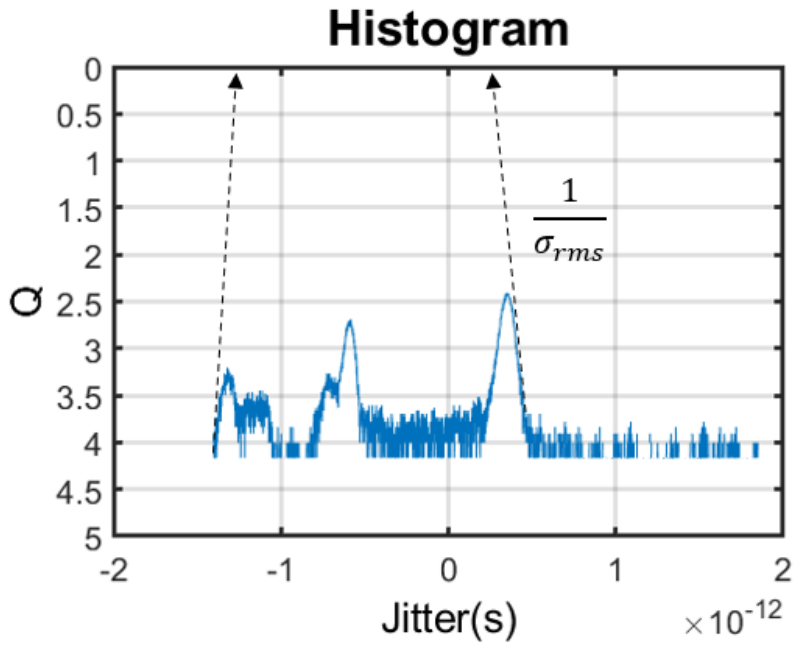

Figure 4.16: Q vs Jitter with TID effects

From this, we see there is a massive degradation in the performance after the circuit has been irradiated. The total jitter massively increases. This makes sense because there will be a large amount of skew between the NMOS and PMOS devices, this will lead to mismatch in the charge pump which will create a larger phase offset in the PLL. This will lead to larger deterministic and RMS jitter. The RMS jitter will come from the uncorrelated noise in the devices since they will be on for a longer time. This will also increase the delay in the digital cells leading to larger deterministic jitter as well. Table 4.3 shows the relative performance of this chip versus other cutting-edge technologies.

	Gao ISSCC 2016	Raj IEEE 2017	Turker ISSCC 2018	Prinzie A-SSCC 2016	This Work
Process(nm)	28	16 FINFET	16 FINFET	65 CMOS	**22 FinFet**
Measurement Frequency (GHz)	5.82	1.2	1.08	1.2	**0.85**
Frequency Range(GHz)	2.7-4.3	18-Sep	7.4-14	5.8-7.2	**13-17**
Average Power(mW)	8.2	29.2	45	11.7	**20**
RMS Jitter(fs)	159	164	53.6	345	**40**
Reference Spur (dBc)	-78	N/A	-75.5	N/A	**-70.7**
RHBD	No	No	No	Yes	**Yes**
FOM*	-243.4	-239.4	-246.8	-232.4	**-249.5**

Table 4.3: Summary of Work Comparison

$$* FOM_T = 10\log\left(\left(\frac{\sigma_{rms}}{1s}\right)^2\left(\frac{P}{1mW}\right)\left(\frac{1}{TR}\right)\right) \qquad TR = \frac{f_{max}-f_{min}}{f_{min}}$$

5. TCAD SIMULATION

The TCAD modeling was done in order to approximately predict the threshold voltage shift in the 22nm FINFET process. Because the process is proprietary, the geometry and materials were estimated in order to match the Id vs Vgs curves of the NMOS transistors, there may be some inaccuracies in the actual devices that cannot be accounted for without further information. Figure 5.1 shows the general geometry of the device. A fine mesh was used in order to try to get a more exact solution at the cost of time to solve the system of equations.

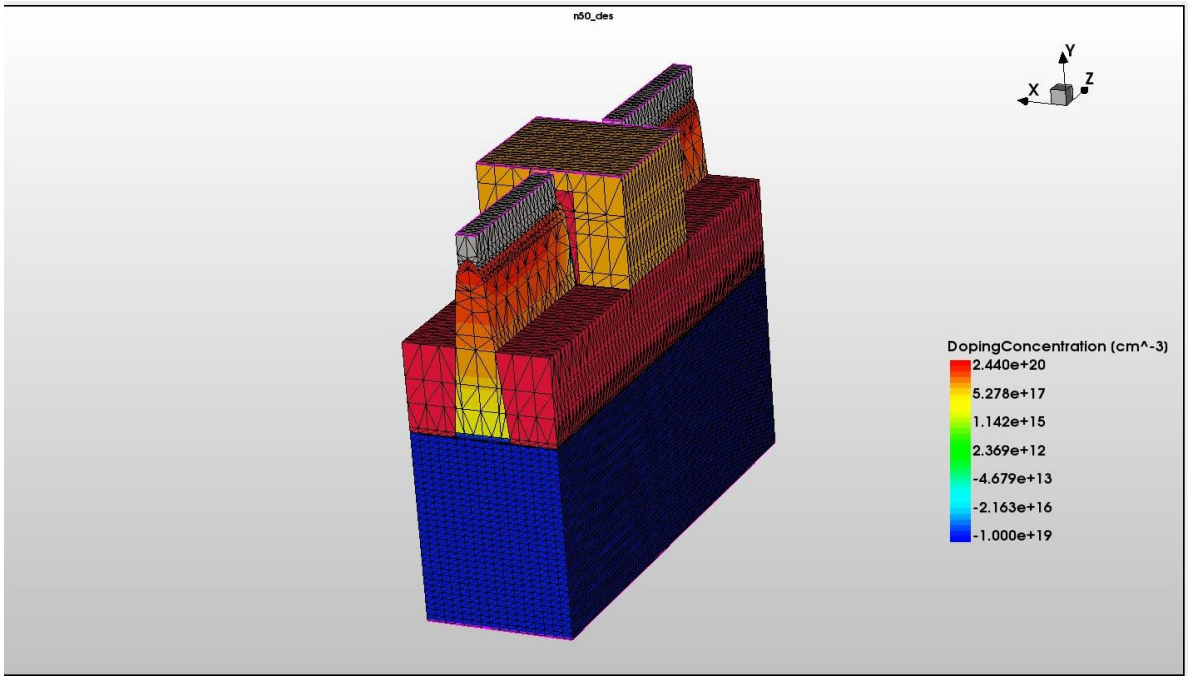

Figure 5.1: Designed 22nm Device

The table of materials used is listed in Table 5.1. The first method is to match the Vth and this was done by changing the bandgap of the material as the bandgap can have a range for a given material. After this is found then the mobility constants are adjusted

in order to improve the Id curves. This device is compared to the Intel device in Figure 5.2.

Location	Material	Doping Concentration	Work function
Gate	Titanium	N/A	4.35eV
Contact	Aluminum	N/A	N/A
Channel	Silicon	1e19	Eg0=1.12eV
Fins	Silicon	2e20	Eg0=1.12eV
Oxide	HfO2	N/A	Eg0=5.9eV

Table 5.1: Materials List of TCAD Device

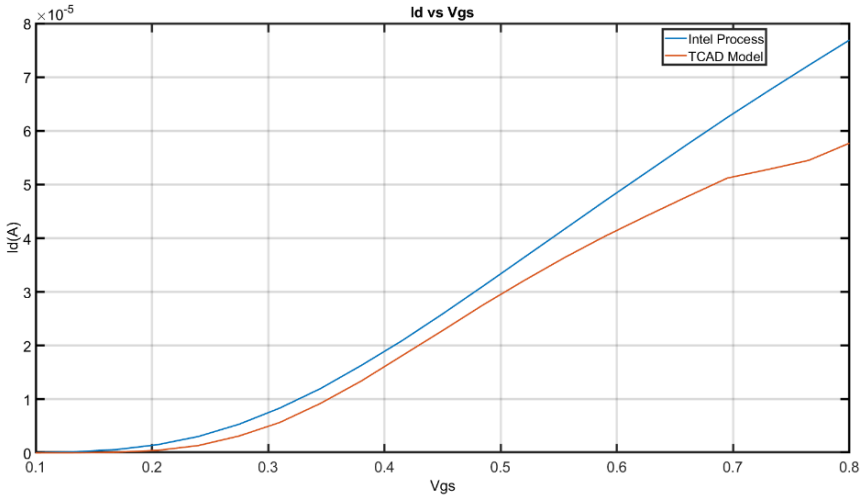

Figure 5.2: TCAD Id curves vs Intel Devices

After the Id curves were relatively matched, a dose rate was applied in order to simulate the threshold shift as previously mentioned. This occurs due to the trapped charge in the oxide of the device. The amount of charge can be estimated from the equation:

$$G_r = g_0 D * Y(F)$$

And

$$Y(F) = \frac{(F + E_0)^m}{(F + E_1)^m}$$

Where Gr is the electron hole pairs created from a dose D. g0 is the intrinsic electron hole creation rate for a given material. Y(F) is the yield which will be a function of the electric field, F and E0, E1 and m are constants determined experimentally [26]. The amount of charge generated in the oxide is first determined and the amount of charge is the homogenously distributed in the oxide of the device to emulate radiation effects. Figure 5.3 shows the radiation generation in the device.

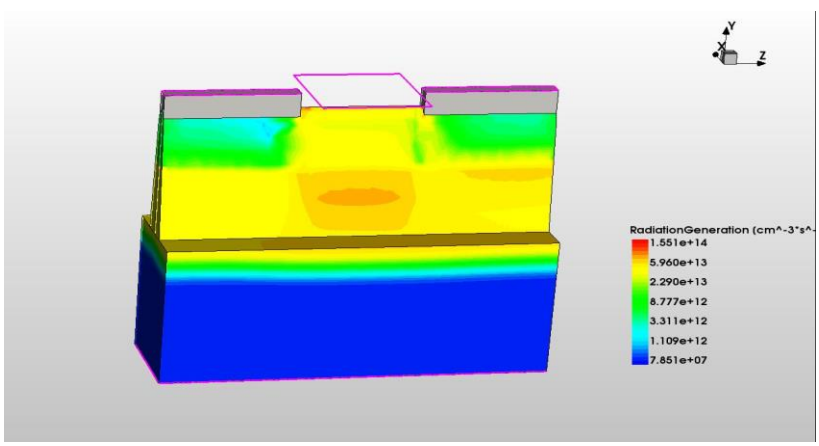

Figure 5.3: Radiation Generation

Figure 5.4 shows the threshold voltage shifts for a give total dose. We see total device failure where the transistor will always be on at approximately 300krad.

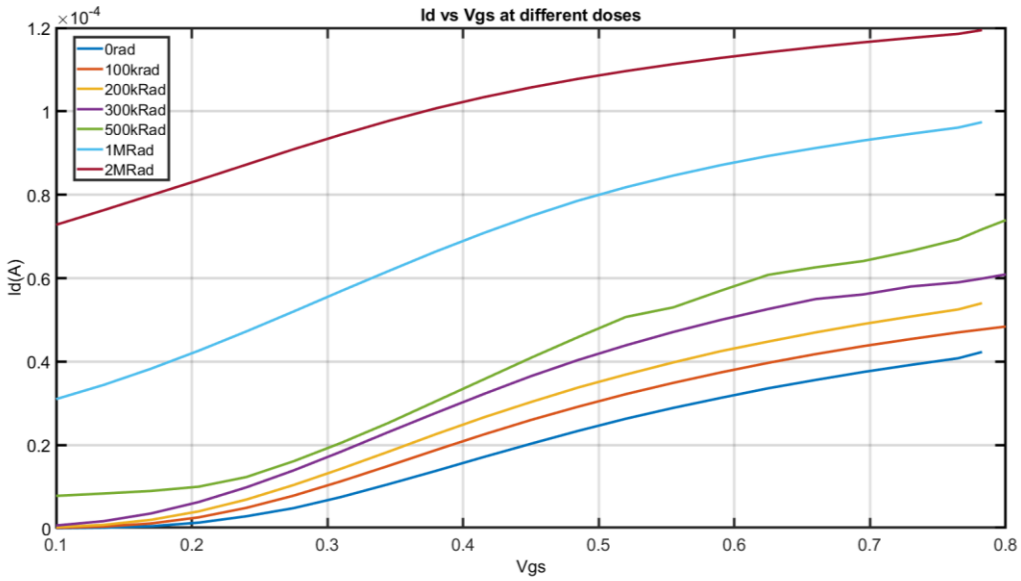

Figure 5.4: Id vs Vgs at Different Doses

6. CONCLUSION

Overall, this worked showed that it is possible to design a radiation tolerant high-speed, low node analog mixed signal PLL that can function under a radiation intensive environment. This worked showed that with proper techniques such as TMR and RC tail node biasing will significantly reduce the sensitive area of the PLL. The VCO uses a varactor decoupling scheme in order to reduce the sensitive area in the VCO.

The VCO has a phase noise of -126dBc/Hz at a 10MHz offset for the standard design and a performance of -124dBc/Hz at a 10MHz offset for post fabrication for both of these chips. The PLL design has rms jitter of a 40fs in schematic simulation with a power consumption of 20mW approximately with a supply voltage of 0.85 volts. With a total peak to peak jitter of approximately 400fs at 50 thousand samples of the wave form. The deterministic jitter was approximately 200fs. The design is radiation hardened by design compared to other high performance PLLs that are not radiation hardened by design.

This work also did TCAD modeling in order to approximate the threshold voltage shifts in the 22nm technology node. This data was used in the PLL simulation study for the TID effects on the loop performance of the PLL.

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