TRANSFORMERLESS UTILITY INTERFACE FOR SOLAR PV AND BATTERY HYBRID SYSTEMS

A Dissertation

by

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ABSTRACT

This research will provide new knowledge essential for the establishment of a transformerless utility interface for hybrid solar PV and battery systems. The dissertation is divided into four main parts. The first responds to the growing interest in deploying medium voltage DC collection grid technology in renewable energy applications to improve energy efficiency and power density. Thus, a new medium voltage DC collection grid method for large-scale PV plants with a DC-DC interleaved modular multilevel (boost) converter (IMMC) is proposed. This proposed IMMC is synthesized with lower voltage half-bridge SiC inverter blocks connected in a series to support medium voltage DC-DC conversion. A power sharing stage is an integral part of this proposed converter, enabling two series of connected PV plants to supply unequal power under partial shading conditions.

The second part of this dissertation explores a proposed single-stage transformerless (SSTL) microinverter that resolves recent microinverter-related challenges. Current microinverters require a high-frequency transformer and DC link buffers. This adds additional power loss and size constraints to the design. Most currently available microinverters do not incorporate a battery storage system (BSS). Thus, an auxiliary DC-DC converter is needed for battery state of charge control. In response to these challenges, an SSTL microinverter with an integrated BSS is proposed to eliminate transformer and DC link buffers. These buffers are replaced with low voltage half-bridge modules along with film capacitors.

The third part of this dissertation expands the SSTL microinverter concept for three-phase hybrid PV/battery inverters for commercial grid applications. The proposed converter uses a minimum number of sensors to integrate both solar PV and battery sources, offering the ability to control for maximum power transfer, as well as charge/discharge functions in the BSS. It was found that the resulting zero voltage switching operation yields higher conversion efficiency.

The fourth part of this dissertation involves implementation of a defense control mechanism in a PV inverter system, offering protection against cyber-attacks via a hardware-in-the-loop platform. A harmonic injection type of cyber-attack was used to test the inverter's behavior. Additionally, a watermarking technique was added to the DSP controller to allow for fast intrusion indication.

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Contributors

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Section 6 is a part of a collaborative effort lead by Drs. Xie, Enjeti, and Kumar in the Electrical Engineering department in Texas A&M University. The main cyber security for solar inverter hardware-in-the-loop implementation is derived from a MATLAB and PSIM simulations collaboratively conducted by graduate students Jaewon Kim, Woo-Hyun Ko and Tong Huang and postdoc Jorge Ramos in the Electrical Engineering department in Texas A&M University.

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1. INTRODUCTION

The 21st century global industrial revolution has led to increasing electrical energy demands that are estimated to grow 2.6% annually, as shown in Figure 1 [1]. Renewable energy resources offer a viable sustainable solution capable of meeting this growth, while also maintaining a minimum environmental impact. The adoption of renewable energy is estimated to reduce global CO_2 emissions by 33% by 2030 [2]. Moreover, a high level of penetration of renewable energy will save up to 26% of industrial and building energy and 35% of transportation energy, due its high efficiency [3]. Because it is highly accessible, solar energy currently dominates the renewable energy industry. It is estimated to have a power density of 15,000$\mu W/\mathrm{cm}^3$, which is equivalent to 5,000 times the typical hydrocarbon fuel energy modules [4].

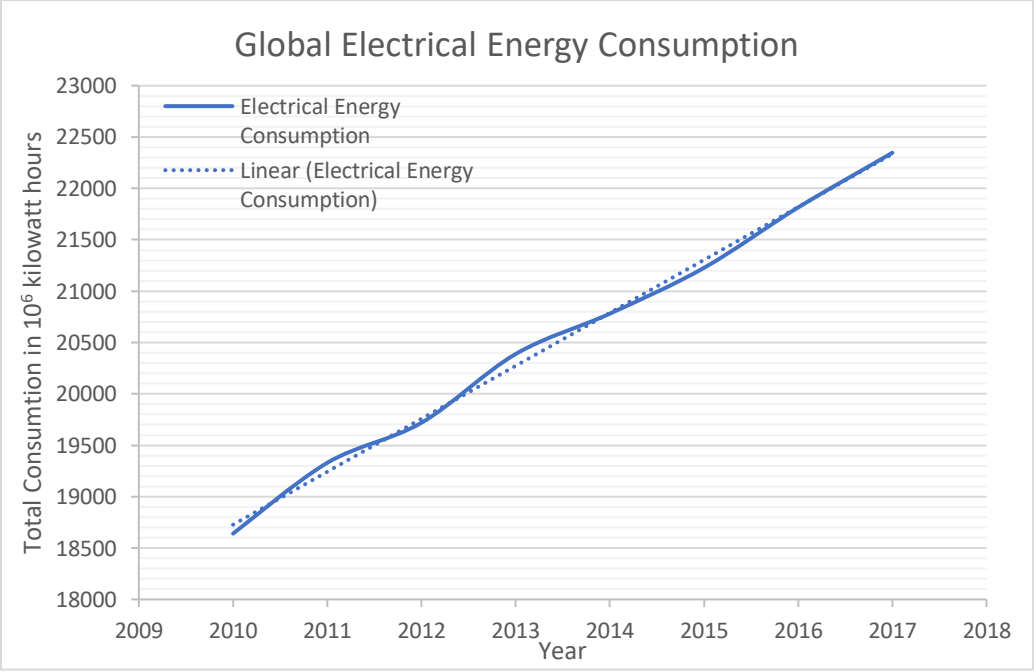


Figure 1 Global electrical energy consumption for 2010 to 2017 (Adopted from [1]).

1.1 Need for high PV-solar energy penetration

Solar energy is the most abundant energy resource on earth; this is due to its high intermittency, which requires very efficient energy conversion and storage stages. Solar energy resources are mainly divided into two main types. The first involves utilizing the sun's radiation through the photovoltaic (PV) effect by PV panel harvesters, while the second harnesses the sun's heat through concentrated thermal solar power harvesters. PV-based energy conversion is the most viable means of harnessing solar energy, due to its direct electrical energy conversion process, potential for high conversion efficiency, modularity, and ability to be used in both distributed and centralized configurations [5]. As a result, the total installed solar PV capacity has increased 14 times globally and 21 times in the US in nine years, as shown in Figure 2 [6].

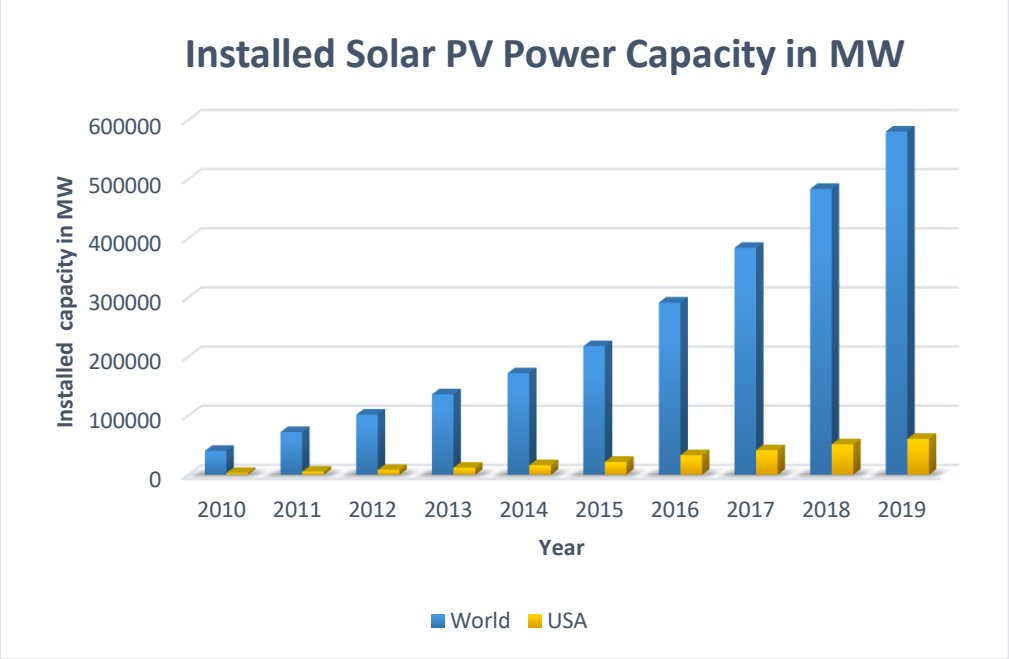


Figure 2 Total installed solar PV capacity in the US and across the globe from 2010 to 2019 (Adopted from [6]).

1.2 Need for an efficient hybrid PV/battery system

Hybrid PV-battery systems are decentralized, smart, clean electricity systems that generate and store energy close to the point of consumption [7]. They offer a viable solution for utilities seeking improved ways to meet their power requirements [7]. Hybrid PV systems solve the intermittent nature of solar PV power and offer a reliable option when connected to a microgrid. The increase in lithium ion (Li-ion) battery technology has attracted interest for use in many applications, including hybrid PV systems.

Li-ion batteries have become the battery of choice for most portable devices, especially electric vehicles. They have nearly a 100% efficiency at various C-rates and are capable of lasting for 20 to 25 years. Conversely, lead acid batteries have a 55% to 75% lower efficiency and can last only two to five years, but offer a cost advantage of $150 to $200. Lead acid batteries are also bulky in size, due to the lower cell voltage (2.1V compared 3.7V) [8, 9].

The major drawback limiting the use of Li-ion batteries in stationary applications is the higher cost of $500 to $600 per kWh. This is expected to drop to $160 per kWh by 2025, as a result of mass production increasing such that it matches with the current cost of lead acid batteries [8, 10]. In fact, the Tesla Power Wall, which is based on Li-ion battery technology, is already widely used in residential applications. Similar other products such as Encharge 3 storage that is manufactured by ENPHASE are widely exploited for residential application. In case of utility-scale application, one of the world's largest Tesla lithium battery energy storage system of 100MW / 129MWh has been in operation in Australia in 2017 [11]. This plant is 60% larger than previously installed

battery storage plant in the whole world [12]. In August 2020, this large battery storage plant record has been surpassed by LS Power's 250 MW Gateway project, located in the East Otay Mesa community in San Diego County, California, USA[13]. The US's utility-scale battery power is set to expand from 1.2 GW in 2020 to around 7.5 GW in 2025[14].

1.3 Importance of reliable high power density and inverter systems

Wide-bandgap semiconductor devices such as GaN and SiC have allowed for new designs for power electronics converters. They can realize a much higher switching frequency than traditional IGBT switching devices, with much better efficiency. As a result, the passive components and required heat sinks are minimized. Consequently, the market size for power electronics usage is growing larger and larger[15, 16].

Relatively large transformer stages are often needed to increase the voltage to meet the load demand and offer galvanic isolation. IGBT's low switching frequency limitation forces the DC link design to be bulky[17]. The most viable solution for such high capacitance is a faulty/lossy electrolytic capacitor. It has been argued that electrolytic DC link capacitors are the shortest life component in power electronic converters [18, 19]. This increases the need to explore power electronics solutions that make possible high power density converters such as transformerless inverters.

1.4 Significance of a PV inverter system's immunity to cyber-attack

In 2015, the first known successful cyber-attack on a power grid in the Ukraine left 225,000 customers without power for up to six hours, as shown in Figure 3 [20]. As distributed energy resource penetration increases, so does the vulnerability to threats [21]. More importantly, by 2025, it is projected that more than 50 billion Internet of Things (IoT) devices will be connected [22]. This creates a crucial demand for defense against cyber-attacks to grid-tied systems such as PV inverter arrangements.

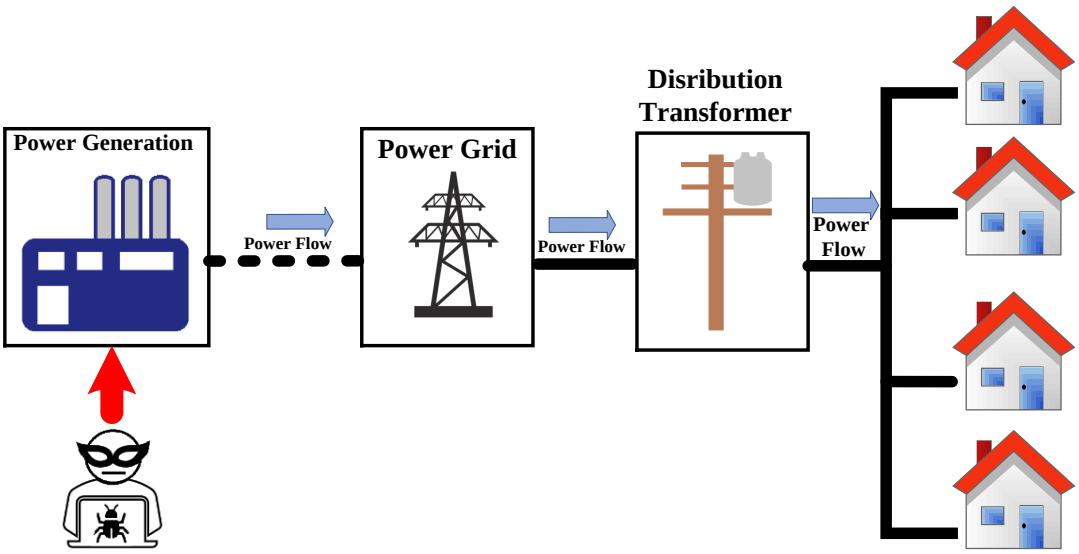


Figure 3 Cyber-attack on a Ukraine power plant.

1.5 Research objective

The main goal of this dissertation is to enable high penetration of renewable energy systems via transformerless microgrids. The first objective was to explore and analyze a new medium voltage DC collection grid method with a DC-DC interleaved modular multilevel (step-up) converter (IMMC) for use in large-scale PV plants. This involved a detailed comparison of the newly proposed IMMC DC-DC boost converter with other DC-DC high gain modular DC-DC converter approaches in terms of maximum power harvesting capability, efficiency, and power density. A reduced scale half-kilowatt prototype is also presented.

The second objective was to eliminate bulky transformers and lossy electrolytic DC links in microinverter systems and replace them with highly efficient wide-bandgap power modules utilizing compact passive components. This was achieved via a newly proposed single-stage transformerless micro-inverter with an integrated battery (energy) storage system (BSS) for residential applications. This DC-AC converter approach includes a DC-DC IMMC, thus realizing the first objective. Control of the proposed approach includes 180^{o} phase shift control for symmetrical upper and lower DC-DC IMMC units to cancel ripple voltage. It also incorporates an integrated active decoupling stage to eliminate twice the line frequency ripple in the DC link capacitor. This function, along with the 180^{o} phase shift control of the DC-DC IMMC stage, drastically reduces the size of the DC link capacitor. As a result, the highly reliable DC link film capacitor can replace the faulty lossy electrolytic capacitor. Thus, various modes of operation need to be explored in simulation to illustrate the performance of the proposed system under different insolation

conditions and demonstrate the battery charge/discharge functions. A 420W single stage transformerless (SSTL) microinverter prototype was selected as a test platform in the lab.

The third objective of this research was to explore the proposed SSTL microinverter derived from Objective 2 in a grid-tie system with linear and non-linear loads and compare the DC link size reduction to that of classical passive decoupling. The fourth objective is derive a merged maximum power point tracking (MPPT)/state of Charge (SoC) technique, as a built-in function within the proposed converter and uses only one voltage sensor and one current sensor. In addition, both the zero-voltage switching (ZVS) operation and switching states need to be investigated in process.

The fourth objective of this research was to examine the PV-inverter system cyber-security performance in response to a cyber-attack, using a watermarking technique via a hardware-in-the-loop (HIL) concept. This was achieved by applying a harmonic injection cyber-attack on the grid tie inverter. The inverter was modeled as a plant in the PLECS RT box to represent the HIL platform, and the plant was controlled via a TI DSP controller.

1.6 Dissertation outline

The dissertation is divided into five main parts. The first section describes the significance of PV and hybrid PV/battery utilization in an electrical power system. This lays a foundation for understanding the necessity of highly efficient, reliable, and cyber-attack immune power conversion stages. The second section includes a literature review of the work that has been done to improve AC and DC collection grids. The review includes descriptions of several high-gain DC-DC converter and transformerless microinverters available in the literature. The third section provides an analysis of the newly proposed medium voltage DC collection grid for large-scale PV plants with a DC-DC IMMC boost.

The fourth section of the dissertation proposes the SSTL microinverter with integrated BSS. Both the MPPT function for PV and charge/discharge controller function for battery storage is enabled by the power sharing stage. High-quality 240V AC is realized via two 50V supply sources (representing the PV and battery) without the use of an electrolytic DC link or transformer buffers. In addition, the SSTL microinverter is capable of operating in a grid-tie system where the grid can charge the battery. The detailed DC link sizing is also explored and compared under different loading conditions.

The fifth section proposes a transformerless hybrid PV three-phase microinverter with integrated battery energy storage. The proposed converter expands the SSTL concept into a three-phase hybrid PV inverter that is used for a commercial grid. The inverter is able to control for maximum power transfer as well as the charge/discharge functions of the BSS using the minimum number of sensors. This is followed by the proposed IMMC boost to the suitable DC link voltage value to enable a transformerless interface with a commercial electric utility grid. An analysis of ZVS operation expressing six switching states is included to enable high power efficiency.

The sixth section investigates a defense control mechanism for the PV inverter system that protects against cyber-attacks via the HIL platform. The defense mechanism involves variance tests to differentiate between normal and malicious signals with a rapid indication response.

2. LITERATURE REVIEW

2.1 AC and DC collection grids

Generally, power is harvested from a large-scale solar energy power system through an AC or DC collection grid [23-30], as shown in Figures 4 and 5. Researchers [24, 26] have discussed the benefits of increasing PV system voltage from 1,000V to 1,500V, reducing system losses and increasing conversion efficiency. AC collection grids [25] convert PV system power collected at 1,000V/1,500V and are connected to three-phase DC-AC inverters (see Figure 1(a)). Generally, several DC-AC inverters are organized in parallel and interfaced with the AC grid via transformers. Conversely, DC collection grids (see Figure 1(b)) consist of several parallel connected DC-DC converters and one DC-AC inverter, followed by transformers connected to the utility [27-29]. Both of these approaches require large line filters, boost converters, and multiple step-up transformers, and suffer from high losses [23-25]. A medium voltage DC collection grid approach has been explored in large-scale offshore wind power systems, and has been shown to improve conversion efficiency due to the elimination of several conversion stages [31, 32]. Studies [27-29, 33] have detailed this concept for large-scale PV power plants.

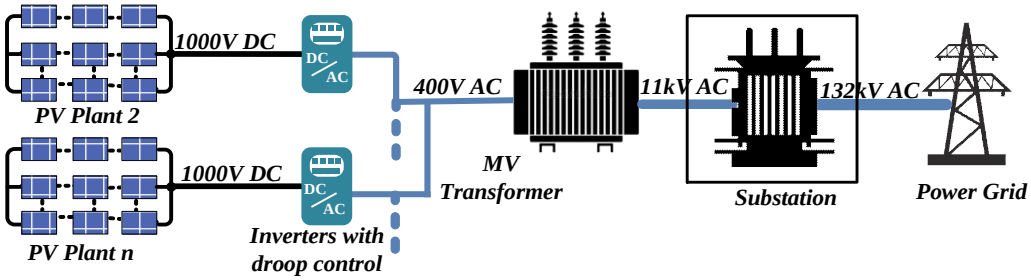


Figure 4. Conventional low voltage three-phase AC collection grid for a large-scale PV power plant.

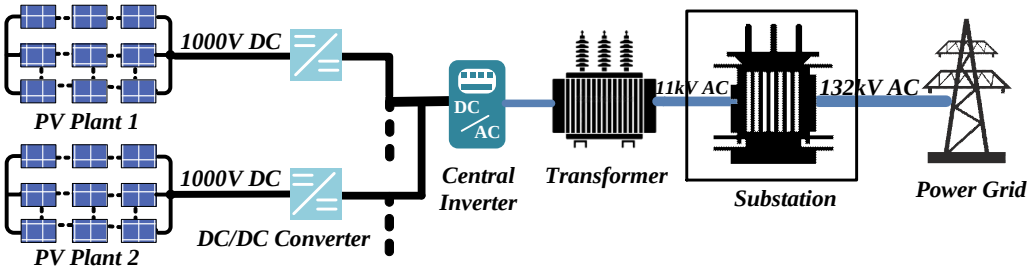


Figure 5 Conventional low voltage DC collection grid for a large-scale PV power plant [10-11].

An important component of a medium voltage DC collection grid is a DC-DC step-up converter. DC-DC is capable of tracking the MPPT without additional medium voltage transformer stages, which tend to be bulky. It has been argued that the DC collection grid has the advantage of 1.6% more system efficiency as compared to a classical AC collection grid [29]. In light load conditions, DC grids also sustain a higher relative efficiency as compared to AC collection [29].

2.2 High gain modular DC-DC converters

Two studies [34, 35] discussed various high step-up ratio DC-DC converters suitable for DC collection grid applications. In [34], a rainstick converter with a cascaded half-bridge inverter submodule operating in step down was described. This converter suffers from unbalanced capacitor voltages that eventually limit its modularity. Another version of this converter, discussed in [35], is called a triangular modular multilevel converter (TMMC). The TMMC facilitates step-up and step-down operation while also achieving a higher gain ratio. The TMMC is designed and controlled to balance its capacitors voltages. However, its configuration involves significantly large passive elements. The TMMC submodule voltages across the capacitors suffer from ripple voltage that forces a large capacitance design. This voltage ripple is increased with each extra boosting stage added. Thus, there is currently a knowledge gap with regards to high-gain DC-DC converters. Consequently, in Section 3, a new power electronics topology is proposed in pursuit of a higher efficiency and better power density high-gain DC-DC converter.

2.3 Microinverter systems evolution

Microinverters offer the most innovative inverter technology on the market, due to their high reliability and quality, supreme intelligence, easy installation, compact size, and modularity [36, 37]. As a result, the microinverter market accounted for US $2.07 billion in 2017, and is expected to increase to five times that by 2026 [38]. Currently available microinverters do not incorporate BSS. A Tesla Wall BSS has its own power converter that interfaces separately with the utility line (see Figure 6(a)) [39]. Figure 6(a) shows a

galvanically isolated microinverter family of topologies introduced in the literature [40, 41]. These consist mainly of the DC-DC stage and contain a high-frequency transformer buffer to achieve MPPT and step up the voltage. PV panel voltages range from 30V to 50V for high-quality 240/110Hz and 50/60Hz outputs. Transformer-based inverters have a peak efficiency of roughly 94% [42, 43]. Thus, an alternative approach is necessary. A transformerless family of topologies is shown in Figure 6(b). These have been explored widely in the literature, enabling better efficiency and volumetric size [44-47]. In residential applications, transformerless inverters have been found to significantly reduce power loss, achieving a new efficiency record of 99% when accompanied by the integration of wide-bandgap semiconductor devices [42, 43]. Consequently, transformerless microinverters have gained much popularity in US, after also being effectively deployed on the European and Australian markets. However, A bulky electrolytic DC link capacitor is still required to process the harmonic power naturally presented in a single-phase system. Thus, there is currently a knowledge gap in this area, which will be addressed in Sections 4 and 5.

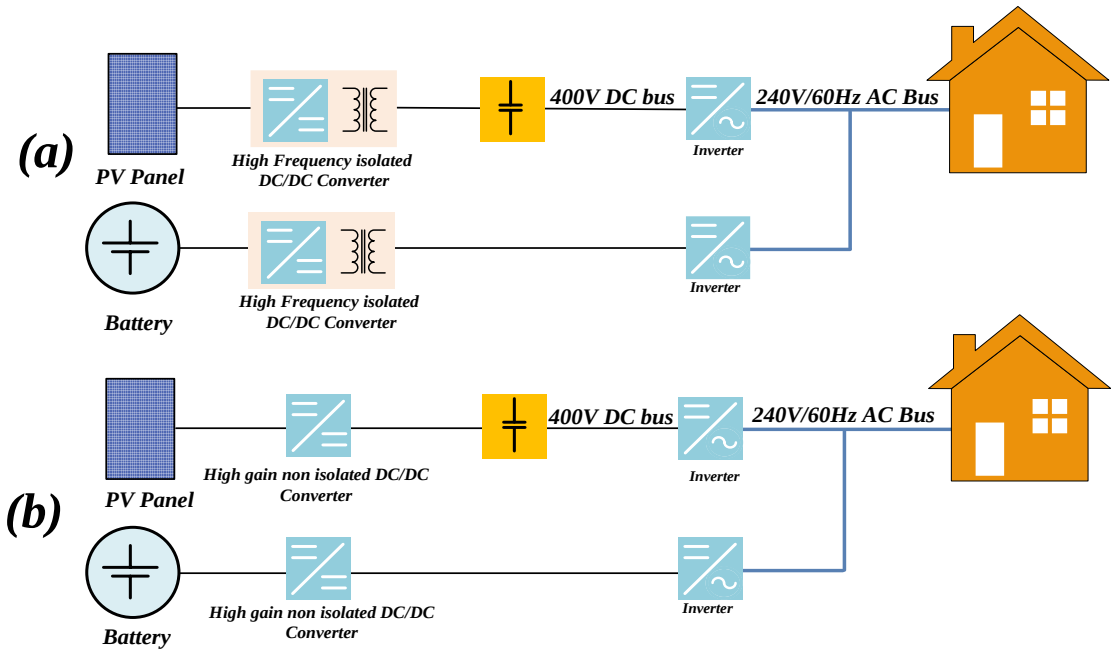


Figure 6 Evolution of a microinverter with an additional battery storage electrical system: (a) isolated microinverter family of topologies introduced in the literature [40, 41] and (b) transformerless family of topologies proposed in the literature to enable non-isolated microinverters [44, 45].

2.4 Cyber-attack defence for AC and DC grids

The rapid growth of commination networks has encouraged business entities and society to adopt IoT platforms. It was estimated in [22] that each person will eventually possess at least six devices that connect to the internet. Thus, vulnerable hacking points will increase exponentially, leading to a generally unsecured network structure. The electrical grid is one severe hacking point that can lead to power blackouts. In fact, a successful cyber-attack in the Ukraine in 2015 left 225,000 customers without power for between two and six hours. The attack targeted the supervisory control and data acquisition system, disabling protection systems, compromising modems, sensors, and

actuators, and initiating a denial of service attack [20]. Another attempted cyber-attack was made on a US nuclear power plant in 2017 [48]. This required the government to focus attention on developing a highly intelligent and resilient power grid. Smart grids have been widely praised for allowing the integration of renewable energy resources, but this also contributes to an increase in the number of hacking points.

There are four main layers that can be targeted by hacking: the control, network, sensor/actuator, and physical layers (see Figure 7) [49]. The focus in this study is on sensor actuator anomalies in residential PV inverter grid-tie systems. Figure 8 displays several sensor/actuator attack points in typical residential home microgrid systems, such as the PV inverter, BSS, and smart meter. The PV inverter is vulnerable to several types of assault, including false data injection and stealth, replay, noise attacks, etc. [48]. Various studies have explored how to protect PV inverter systems from these attacks [48-55]. Most require communication with another agent to differentiate authentic from malicious signals. One intrinsically cyber-secure approach was presented by a bedrock company, mainly for UPS inverter systems. This product has state-of-the-art cyber-protection for all four of the system layers shown in Figure 7 [56]. However, cost and feasibility limit its use, at least for the time being. Thus, there is a significant demand for a robust defense mechanism for residential PV inverter systems.

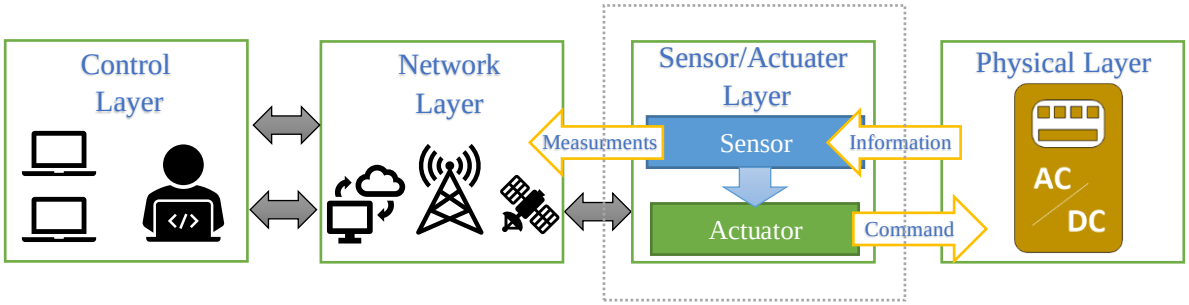


Figure 7 The four main layers where intrusion could occur (Adopted from [49]).

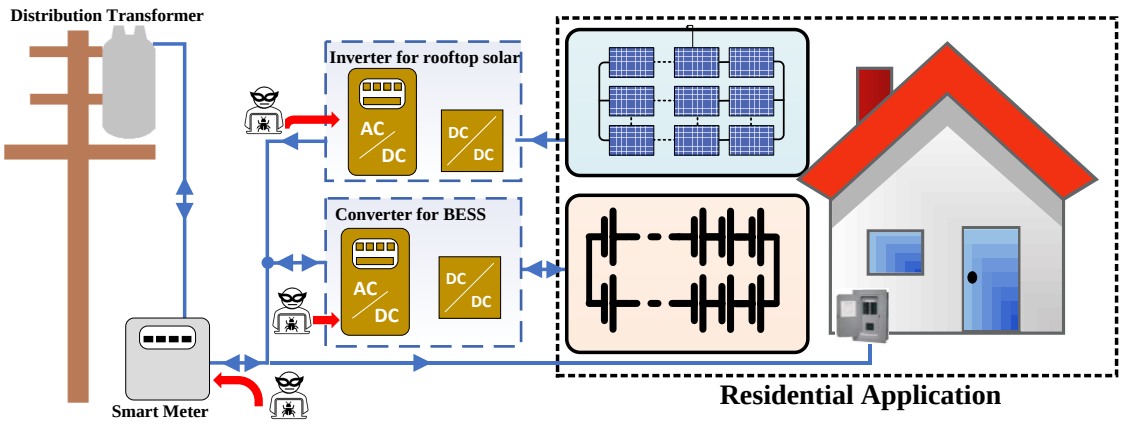


Figure 8 Sensor/actuator attack points, including the PV inverter, BSS, and smart meter.

3. A NEW MEDIUM VOLTAGE DC COLLECTION GRID FOR LARGE-SCALE PV POWER PLANTS WITH INTERLEAVED MODULAR MULTILEVEL CONVERTERS[1]

3.1 Introduction

The global solar market had a cumulative 500GW power production by the end of 2018 [57]. The Kuwait Institute of Scientific Research has initiated and developed a master plan for a 2,000MW multi-technology renewable energy park. Over 100km^2 has been allocated to the initiative [58]. This plant, named "Shagaya," was selected as a design example for the present study. A new medium voltage DC collection grid for large-scale PV power plants (e.g., Shagaya) is proposed (see Figure 9(c)) as a viable solution to the disadvantages accompanying several types of AC and DC collection grids (see Figures 9(a) and 9(b)).

The new medium voltage DC collection grid for large-scale PV power plants with a DC–DC IMMC configuration (see Figures 9(c) and 10) lays the foundation for an enhanced DC collection grid, due to its unique structure of two integrated and interconnected PV plants. The approach consists of a collection of two 1,500V solar panels connected in series, with a center ground point followed by a power sharing stage (see SM9 in Figure 2). The power sharing stage (SM9) facilitates independent adjustment of the MPPTs of PV Plants 1 and 2. The power sharing stage is followed by two sets (one

1. © [2020] IEEE. Reprinted, with permission, from [Fahad M. Alhuwaishel, Ahmed K. Allehyani, Sinan A. Sabeeh Al-Obaidi, Prasad N. Enjeti, A Medium-Voltage DC-Collection Grid for Large-Scale PV Power Plants With Interleaved Modular Multilevel Converter, Aug/2020]

positive and one negative) of the proposed DC–DC IMMC converter, achieving 16kV DC. Each set of DC–DC IMMCs boost the PV plant voltage of 1,500V DC to 8kV, with the help of lower voltage half-bridge modules, achieving a total of 16kV. The technical focus of this section is limited to the DC–DC converter stage. The proposed IMMC-based MVDC architecture has the following advantages. 1) The modular architecture with interleaved half-bridge SMs ensure that the system is scalable. 2) Employing SiC switching devices results in a higher power density for large-scale PV power plants. 3) The IMMC DC–DC converter regulates the MVDC grid voltage under varying levels of solar insolation. The control strategy to achieve the MPPT is implemented via PWM control. 4) The MVDC architecture results in lower ohmic losses and improves power density [7, 12]. 5) The 180◦ phase shift between the sets of two DC–DC IMMCs cancels voltage ripple at the DC output port, allowing for a more compact capacitor design. 6) The DC output is of a higher quality, due to the reduction in voltage ripple.

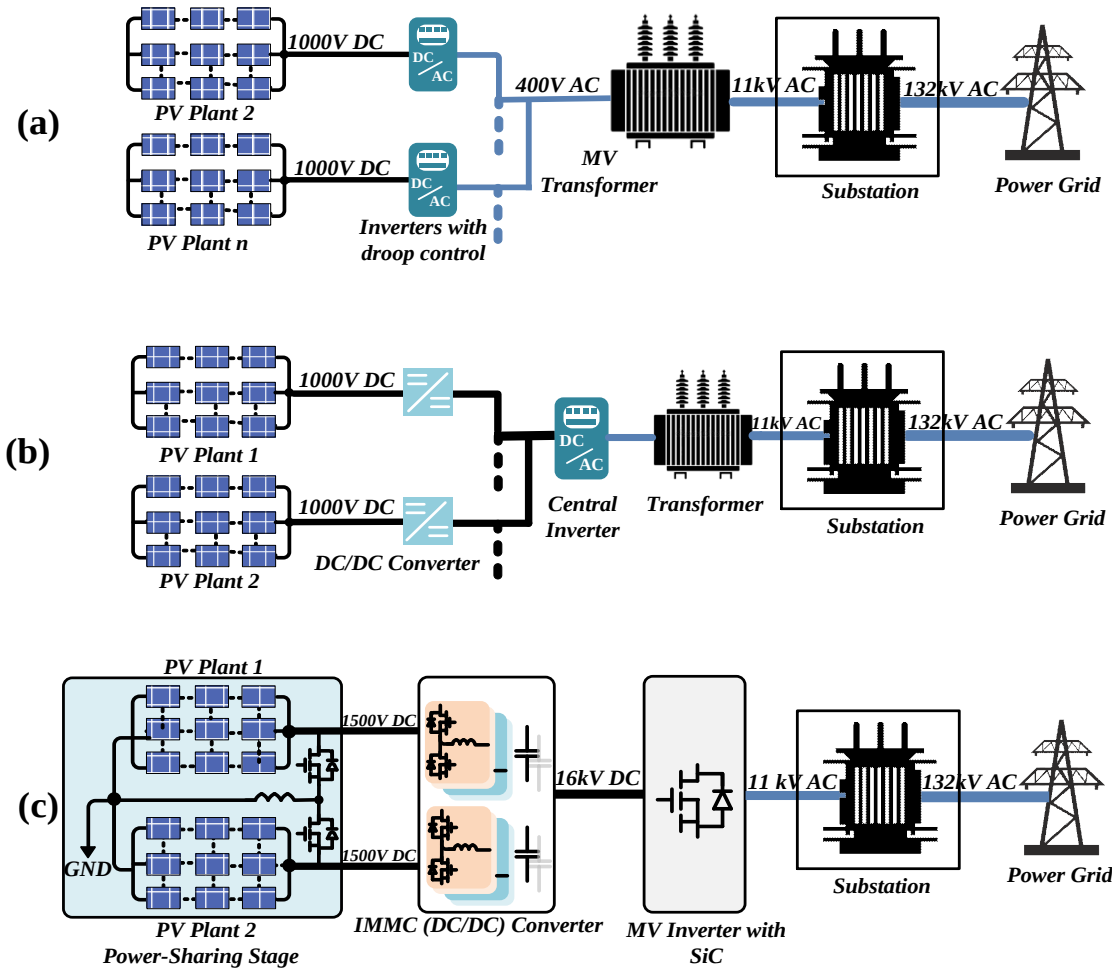


Figure 9 Evolution of the proposed large-scale PV power collection grid using the new medium DC collection grid with SiC converters.

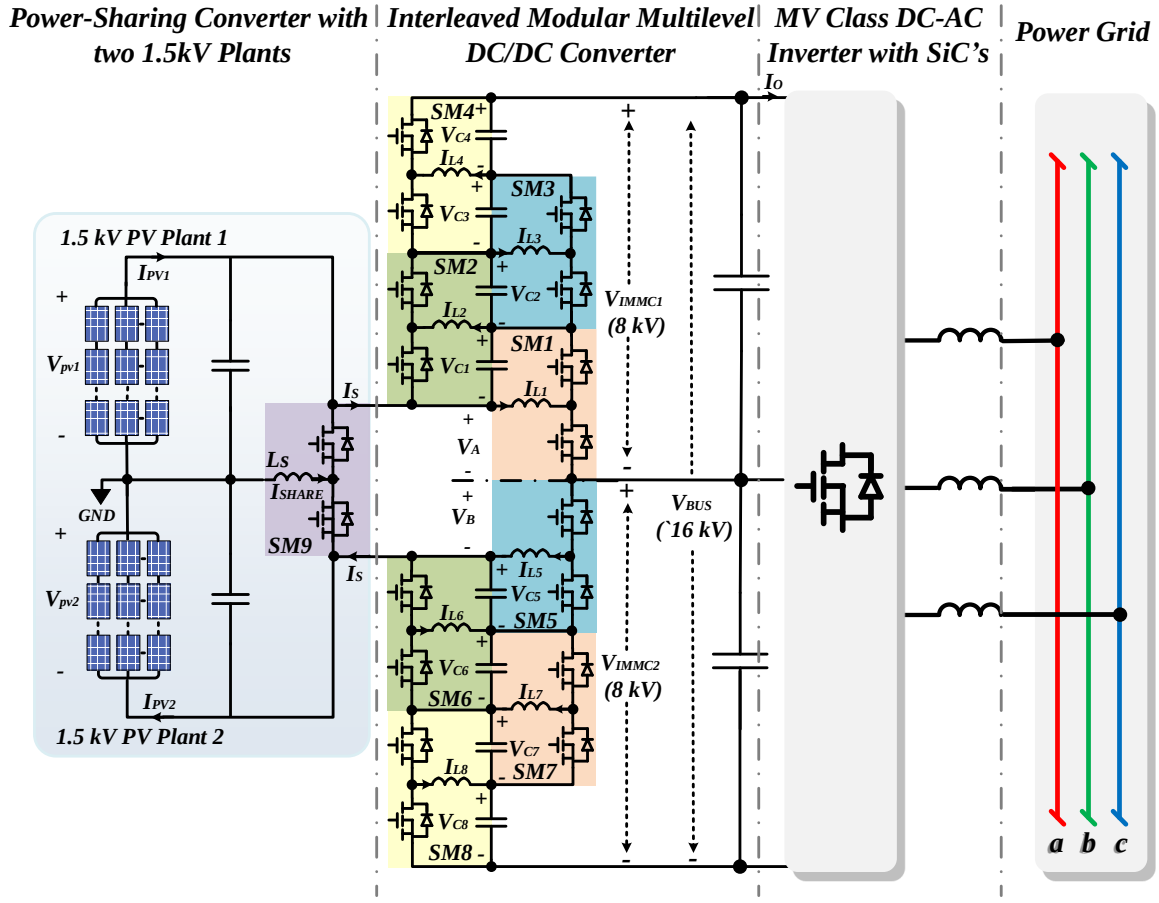


Figure 10 Circuit topology of the proposed DC-DC IMMC for the medium voltage DC collection grid for large-scale PV power plants; IMMC has the ability to independently adjust the MPPT for PV Plants 1 and 2.

3.2 DC-DC IMMC design and operation

Figure 10 shows the proposed converter, which can be viewed as twin series of cascaded blocks of half-bridge modules. Figure 11 shows the upper half, with the voltages and current loops marked. As explained above, an IMMC is a series of connecting half-bridge modules operated at a high frequency, with a PWM duty ratio to regulate voltages across the series of connected capacitors. Figure 11 also demonstrates the two states of DC-DC IMMC operation. Figure 11(a) shows State 1, where the lower switches for SM1 to SM4 are turned on and the upper switches are off. Figure 3(b) shows State 2, where the upper switches are turned on and the lower switches are off. By employing a high switching frequency, the size of the required inductor and capacitor can be small. Hence, additional states of operation can be deployed but States 1 and 2 are the dominate states in this design example. Starting with SM1 (see Figure 11) as a basic cell block, the voltage V_{c1} across capacitor C_1 can be expressed as:

$$V_{c1} = \frac{\delta_1}{1-\delta_1} V_A \tag{1}$$

where δ_1 is the duty ratio of SM1, as shown in Figure 11. For this relation, SM1 is assumed to operate in continuous conduction mode, where Equation 1 is realized with the assumption of a small ripple approximation. For the remaining submodules (SM2 to SM4), the capacitor voltages C_2 to C_4 can be defined similarly, as:

$$V_{cn} = \frac{\delta_n}{1-\delta_n} V_{cn-1} \tag{2}$$

where n = 2 to 4. Thus, each V_{cn} voltage can be independently controlled via its corresponding duty cycle δ_n by the half-bridge modules. The output voltage of the converter V_{IMMC1} (see Figure 11) is the sum of the capacitor voltages and V_A.

$$V_{IMMC1} = V_A + V_{c1} + V_{c2} + \ldots + V_{cn} \tag{3}$$

The output voltage V_{IMMC1} is a function of the duty cycles δ_1 to δ_n. By choosing the proper duty cycle, the incoming voltage of the PV for Plant 1 can be suitably boosted. Further, from Figure 11, the node voltage/current loops equations can be written to express inductor and capacitor values in terms of the current/voltage ripple, PWM duty cycle, and switching frequency. From Figures 11(a) and 11(b), expressing the voltage across the inductor for one switching cycle, the required inductor value L_1 can be expressed as:

$$L_1 = \frac{V_A}{(\frac{\Delta i_{L1}}{\delta_1 T})} \tag{4}$$

A general equation for determining inductors L_2 to L_n is given by:

$$L_n = \frac{V_{cn-1}}{\frac{\Delta i_{Ln}}{\delta_n T}} \tag{5}$$

The capacitor currents can be derived from the Figure 11(b) node equations. It is clear that I_{C1} can be expressed as:

$$I_{C1} = I_s + \delta_2 I_{L2} - I_{L1} = C_1 \frac{dV_{C1}}{dt} \tag{6}$$

Conversely, from the design equations for capacitors C_1 to C_n and ripple voltage cancellation, capacitor C_1 can be expressed as:

$$C_1 = \frac{I_s + \delta_2 I_{L2} - I_{L1}}{\frac{\Delta V_{C1}}{\delta_2 T}} \quad (7)$$

A general equation to determine capacitors C_2 to C_{n-1} is given by:

$$C_{n-1} = \frac{I_s - \delta_1 I_{L1} - (1 - \delta_{n-1}) I_{Ln-1} + \delta_n I_{Ln}}{\frac{\Delta V_{Cn}}{\delta_n T}} \quad (8)$$

The last capacitor C_n can be expressed as:

$$C_n = \frac{I_o - (1 - \delta_n) I_{Ln}}{\frac{\Delta V_{Cn}}{(1 - \delta_n) T}}$$

In, addition, the capacitance C_1 to C_n values can be viewed as the definite integral of the capacitor currents I_{c1} to I_{cn} (see Equations 6 to 9, respectively) for pre-specified duty cycle operation limits, divided by the respective voltage ripples ΔV_{C1} to ΔV_{Cn}. The total voltage ripple of the upper half of the IMMC is ΔV_{IMMC1}, which can be found using Equations 7, 8, and 9 as:

$$\Delta V_{IMMC1} = \sum_1^n \Delta V_{Cn} \quad (10)$$

Similarly, ΔV_{IMMC2} for the lower half of the IMMC is:

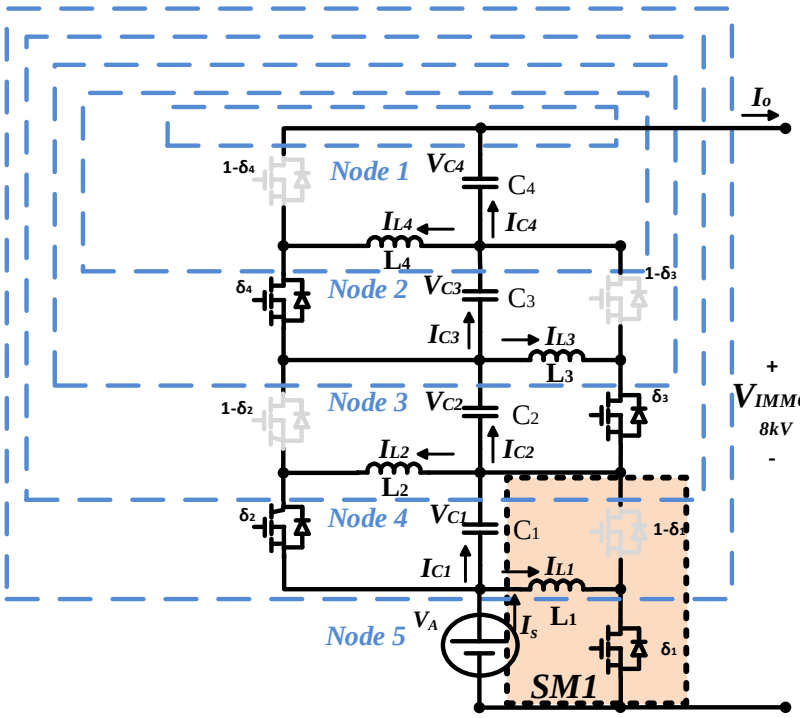
$$\Delta V_{IMMC2} = -\sum_1^n \Delta V_{Cn} \quad (11)$$

Consequently, the total ripple across the output V_{BUS} is given by:

$$V_{BUS} = (V_{IMMC1} + \sum_1^n \Delta V_{Cn}) + (V_{IMMC2} - \sum_1^n \Delta V_{Cn}) \quad (12)$$

The capacitor voltage ripple across V_{BUS} is therefore cancelled. As a result, the capacitors C_1 to C_n can be designed for a high capacitor ripple $\Delta V C_n$ of 30%, allowing for a more compact capacitor size.

(a)



(b)

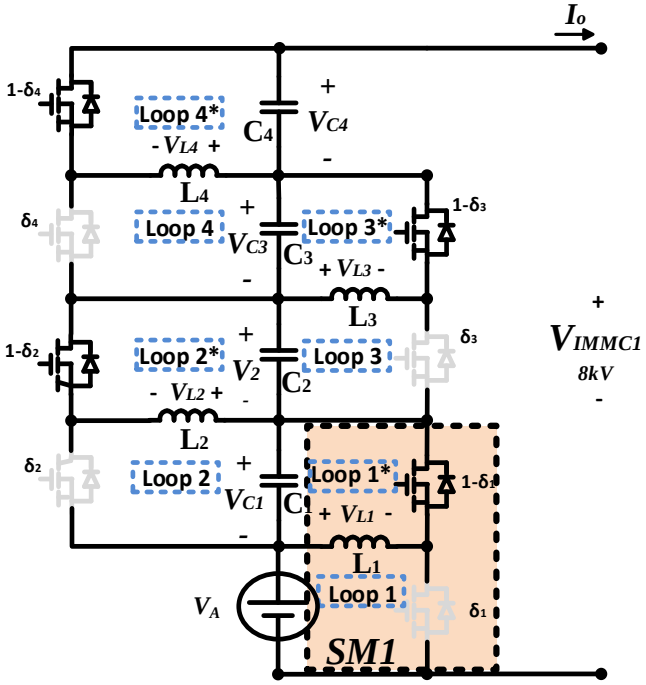


Figure 11 Equivalent circuit for the upper half of the proposed DC-DC IMMC in Figure 10: (a) defined node voltages and (b) defined loop currents.

The average inductor currents I_{L1} for the basic cell SM1 (see Figure 3(a)) are derived as:

$$I_{L1} = I_s + \delta_2 I_{L2} \tag{13}$$

Similarly, a general equation to determine the average inductor currents I_{L2} to I_{Ln-1} is:

$$I_{Ln-1} = \frac{[I_s - \delta_1 I_{L1} + \delta_n I_{Ln}]}{1 - \delta_{n-1}} \tag{14}$$

I_{Ln} is a boosted version of the output current I_o, such that:

$$I_{Ln} = \frac{I_o}{1 - \delta_n} \tag{15}$$

3.3 Power sharing converter operation principle

Figure 10 shows two series of connected solar fields (PV Plants 1 and 2). Under varying climate conditions and cloud coverage, each plant is expected to operate at a different maximum power point (MPP) on the V-I curve (see Figures 13 and 14). The power sharing converter is the half-bridge module SM9 (see Figure 10). Along with the inductor, it is operated at a high frequency with a duty cycle that allows for independent control of PV Plants 1 and 2, producing output currents I_{PV1} and I_{PV2}, respectively. The difference between the two currents I_{PV1} and I_{PV2} (due to different MPPT operations) circulates in the inductor L_s in the form of I_{SHARE}. Therefore, PWM operation of the SM9 guarantees individual MPPTs for PV Plants 1 and 2. The inductor current I_{SHARE} is given by:

$$I_{SHARE} = I_{PV1_{max}} - I_{PV2_{max}} \tag{16}$$

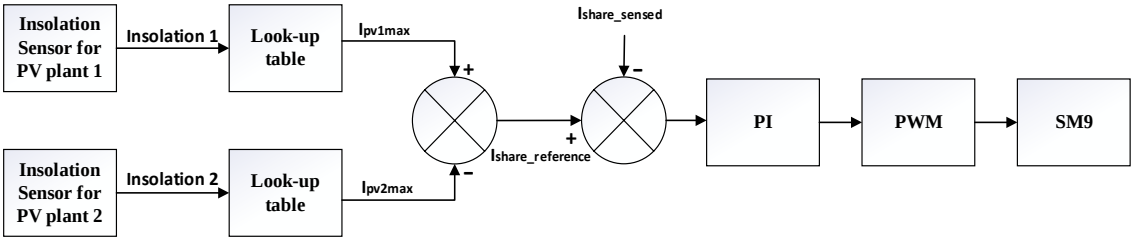


Figure 12 Control loop of the SM9 power sharing unit.

The control aspect of the power sharing unit (SM9) is illustrated in Figure 12. Once the insolation data are collected from each PV plant, the respective MPP currents I_{pv1max} and I_{pv2max} can be obtained. Then, the deference current $I_{SHARE\_reference}$ is computed and compared with the sensed current I_{SHARE_sensed}. The resulting signal is sent to SM9 via a pulse width modulation operation.

3.4 Design example

In this section, a design example for a 1MW PV power plant is detailed. Plant specifications were derived from the Kuwait Shagaya 60MW solar power plant, as discussed above. Table 1 shows the design specifications for the 1MW PV plant block. The 1MW PV plant is divided into two sets, PV Plants 1 and 2, as shown in Figure 10. A monocrystalline Helios 9T6, rated at 420W, was selected as a building block, due to its high efficiency and elevated temperature endurance [59]. To realize a 1.5kV DC output, each PV string can accommodate 30 series-connected panels. A total of 40 parallel string structures were needed for a 500kW capacity (see Table 1). Figures 13 and 14 show typical PV current voltage (IV) curves for the two PV plants.

3.4.1 IMMC half-bridge submodule voltage rating

Figure 10 shows the proposed DC-DC IMMC connected to two PV plants with center ground points. The upper half of the IMMC processes the power from PV Plant 1 and boosts the voltage V_A (~1.5kV) to V_{IMMC1} (~8kV). For the converter shown in Figure 10, we can write the following from Equation 3:

$$V_{IMMC1} = V_A + V_{c1} + V_{c2} + V_{c3} + V_{c4} \tag{17}$$

Given $V_A \approx 1.5\ kV$ and $V_{IMMC1} \approx 8\ kV$, from Equation 17, we have:

$$V_{c1} = V_{c2} = V_{c3} = V_{c4} = 1.625kV \tag{18}$$

It is clear from Figure 10 that each semiconductor switch in the half-bridge submodules SM1 to SM9 has a blocking voltage of 2*V_{cn}, which is equal to 3.25kV. Therefore, the 6.5kV SiC developed by CREE (or something similar) would be suitable. Researchers [60] have discussed the operational characteristics of the 6.5kV 200A SiC MOSFET developed by CREE, which was the model chosen for the proposed design.

3.4.2 Current rating of the IMMC half-bridge submodule

The next step was to determine the IMMC device's current ratings. From Figure 10 and Equation 15, the submodule SM4 inductor current is given by:

$$I_{L4} = \frac{I_o}{1 - \delta_4} \tag{19}$$

Substituting I_o = 62.5A and $\delta_4 \approx 0.5$, we have I_{L4} = 125A from Equation 19. Therefore, for the SM4 submodule, two 6.5kV SiC devices from the CREE rated at 200A were considered sufficient. Repeating the same calculation for I_{L1} we can show from Equation 13 that I_{L1} = 521A. Therefore, the submodules closer to the center of the IMMC converter (SM1 and SM5) carry the maximum current (four times that of SM4 and SM8), while the submodules located at the top and bottom of SM4 and SM8 (see Figure 10) are rated lowest in terms of current. Thus, Figure 15 shows the interleaved parallel arrangement of 6.5kV and 200A CREE submodules meeting the converter rating shown in Table 1.

3.4.3 IMMC capacitor/inductor selection

The required inductor value could be determined from Equation 5. Choosing a ripple of $\Delta i_{L\mathrm{n}}$= 5% and V_{cn} = 1500V, the switching frequency of 20kHz, L = 3mH is obtained. Further, the capacitor value is given by Equations 7 to 9. Defining the voltage ripple as ΔVC_n= 3%, then C = 100μF. Table 2 Summarizes the design parameters for each DC-DC IMMC.

Table 1 1MW PV Plant Design Specifications

Parameter	
Total maximum power capacity	1MW
Number of PV plants	2
PV plant output voltage	1,500V
Selected PV module building block	Helios 9T6 [59]
Maximum power, voltage, and current power for each PV panel	420W, 49.5V, 8.5A
Number of PV panels per string	30
Number of PV strings	40
Number of sets of DC-DC IMMC converters	2
Output DC bus voltage (V_{BUS})	16kV
Output DC current (I_0)	62.5A

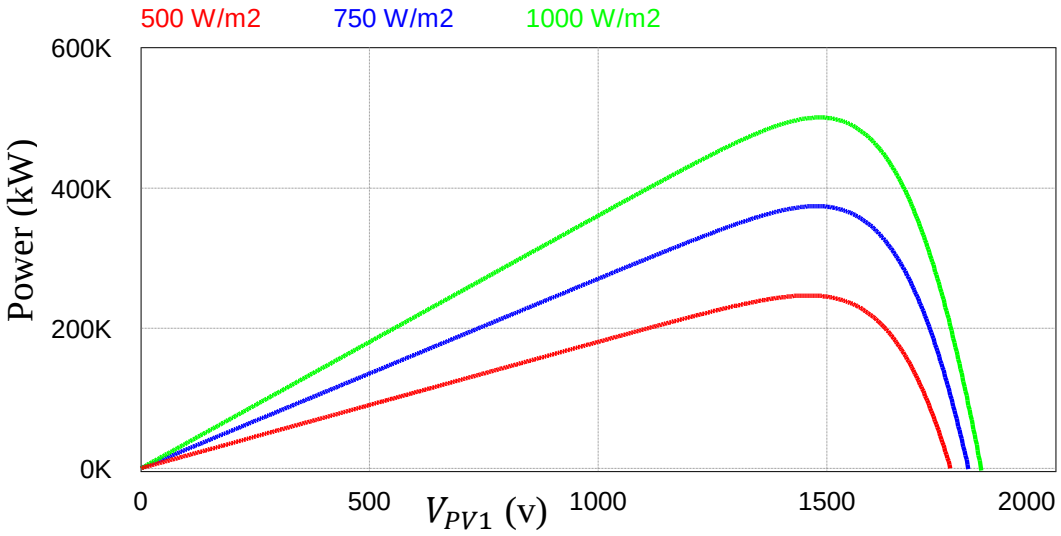


Figure 13 Variations in power vs. voltage for PV Plants 1 and 2, under different insolation conditions.

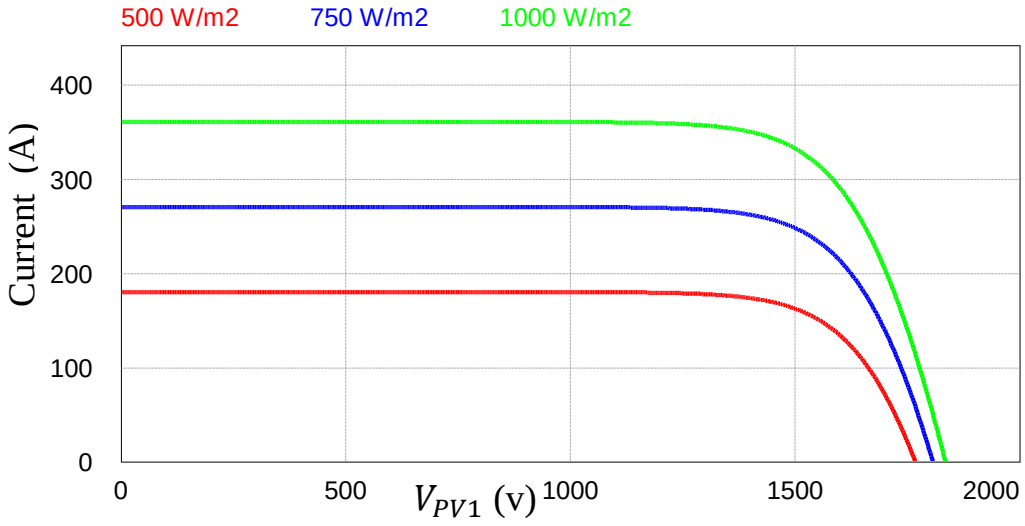


Figure 14 Variations in current vs. voltage for PV Plants 1 and 2, under different insolation conditions.

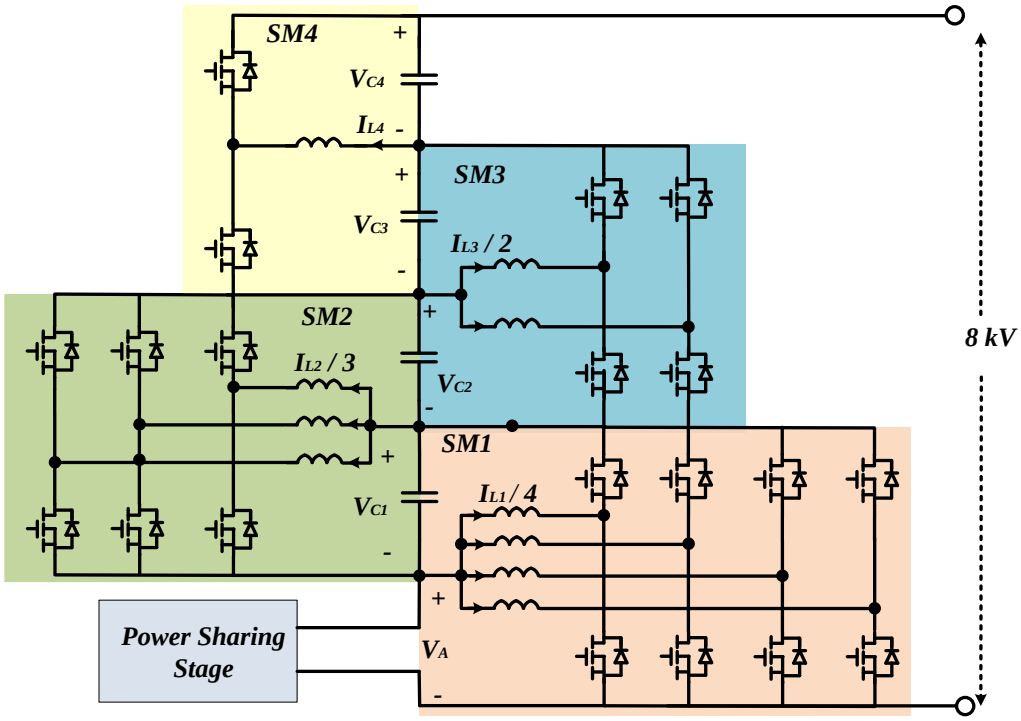


Figure 15 Parallel interleaved half-bridge modules for handling the current of the proposed upper half of the DC-DC IMMC shown in Figure 10. Example 6.5kV and 200A SiC half-bridge modules developed by CREE [60] were employed. Note that the bottom half is identical to the upper.

Table 2 Design Criteria for Each DC-DC IMMC

Design Criterion	
Number of submodules per DC-DC IMMC	4
Switching frequency	20kHz
Switching device type	SiC 6.5kV, 200A, 12.5mΩ developed by CREE [60]
Inductor value	3mH
Capacitor value	100μF

3.5 Comparison of DC-DC IMMC with TMMC

In this section, the proposed DC-DC IMMC concept (see Figure 10) is compared with the TMMC configuration (see Figure 16) [35]. The TMMC was designed to process power for a solo 1MW 1.5kV PV. Table 3 provides a detailed comparison of the proposed DC-DC IMMC (shown in Figure 10) and the TMMC configuration (shown in Figure 16). Equations 1 to 9 detail the passive element (L and C) design of the DC-DC IMMC, which is tabulated in Table 3. Equations 1 to 9 have also been used to design the TMMC configuration. Hence, the TMMC configuration is designed to boost the voltage from 1.5kV to 16kV. As a result, nine submodule boosting stages are needed. In addition, the first submodule SM1 (in Figure 16) is forced to process a large current of 1.1kA, as can be concluded from Equations 13 to 15.

Therefore, a parallel configuration similar to what is shown in Figure 15 is required. The current I_{L9} shown in Figure 16 describes the submodule-rated current. Hence:

$$\boldsymbol{I_{L9}} \cong \frac{\boldsymbol{I_{L1}}}{\boldsymbol{9}} \cong \frac{\boldsymbol{I_{L2}}}{\boldsymbol{8}} \cong \frac{\boldsymbol{I_{L3}}}{\boldsymbol{7}} \cong \frac{\boldsymbol{I_{L4}}}{\boldsymbol{6}} \cong \frac{\boldsymbol{I_{L5}}}{\boldsymbol{5}} \cong \frac{\boldsymbol{I_{L6}}}{\boldsymbol{4}} \cong \frac{\boldsymbol{I_{L7}}}{\boldsymbol{3}} \cong \frac{\boldsymbol{I_{L8}}}{\boldsymbol{2}} \quad (20)$$

Thus, in the case of the very first submodule (SM1), the inductor current I_{L1} is equivalent to nine times the rated current I_{L9}. As a result, SM1 must be divided into nine smaller parallel identical submodules to overcome the 200A current limitation specified for the SiC 6.5 CREE device. The total number of submodules for the TMMC can found as:

$$Total\ number\ of\ TMMC\ Submodules = \sum_{1}^{y}(x) \tag{21}$$

where y is the number of original submodules before performing a parallel configuration, which is equal to nine in the case of the TMMC. Table 3 shows that the TMMC requires a total of 45 submodules, 25 more submodules more than proposed DC-DC IMMC. As shown in Table 3, the total energy stored in the capacitors for the proposed DC-DC IMMC is 10.5% that of the TMMC, due to the voltage ripple cancelation described in Equation 12. Also, the total energy stored in capacitors for the DC-DC IMMC is 55.5% less than that which is stored for the TMMC. The sizes of the passive elements of the proposed IMMC are also reduced by 73%. The power loss per submodule includes losses associated with the inductor and SiC-based half-bridge. The inductor losses (174W) are contained, and the current ripple is within 5%. The half-bridge SiC module losses are also detailed in Table 3, using data from [60]. Table 3 shows that the TMMC power losses are 2.25 greater than that of the proposed DC-DC IMMC. Consequently, the power efficiency of the proposed DC-DC IMMC is 95.2%, while the efficiency of the TMMC is 89.3%.

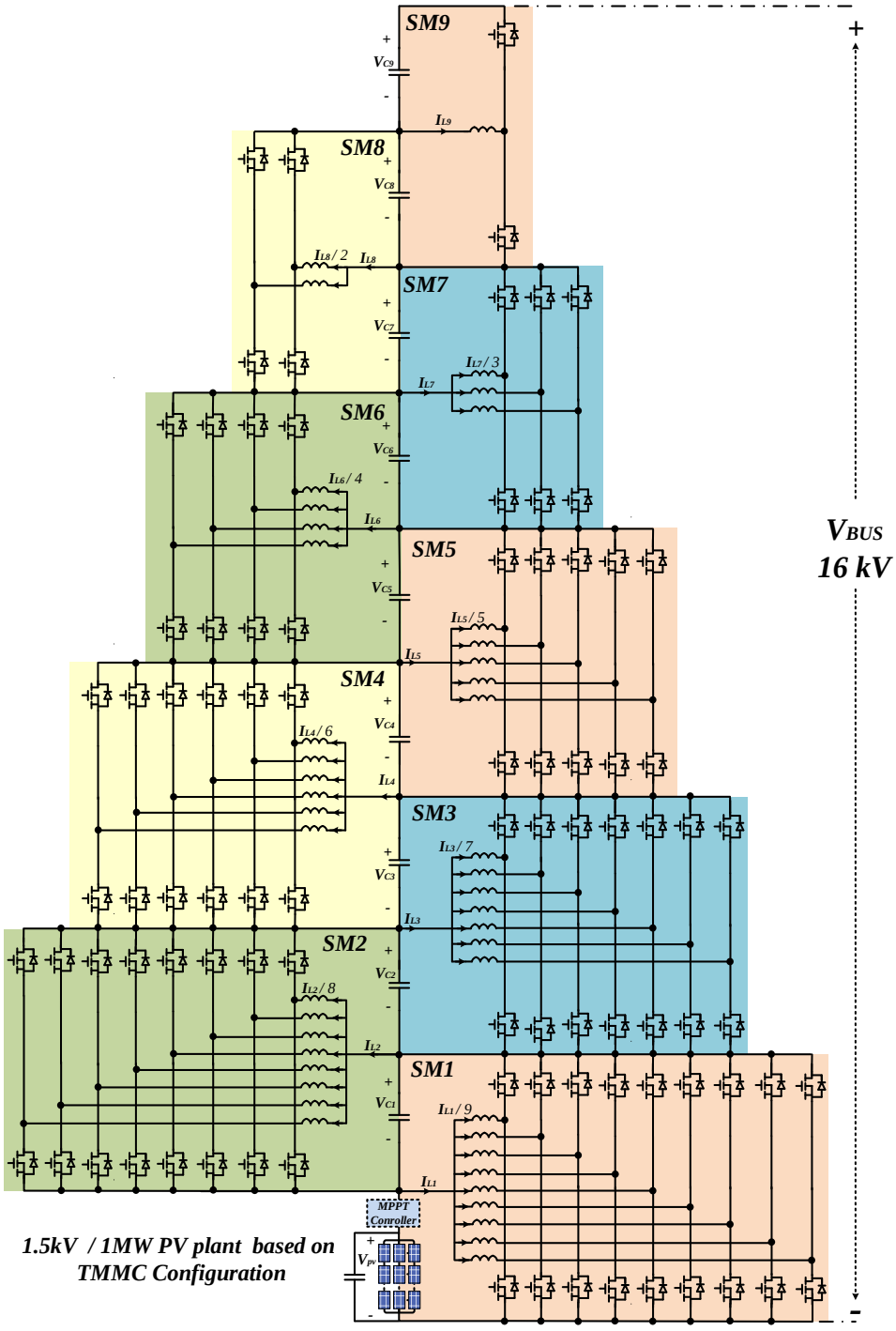


Figure 16 The 1.5kV 1MW rated power conversion stage via the TMMC approach [35]. The currents $\frac{I_{L1}}{9}, \frac{I_{L2}}{8}, \frac{I_{L3}}{7}, \frac{I_{L4}}{6}, \frac{I_{L5}}{5}, \frac{I_{L6}}{4}, \frac{I_{L7}}{3}, \frac{I_{L8}}{2}$, and I_{L9} are all equal. These currents describe a submodule rating suitable for a 6.5kV, 200A SiC CREE model [60]. Note that the parallel submodule configuration is similar to what is shown in Figure 15.

Table 3 Comparison of the Proposed DC-DC IMMC Design with the TMMC General Converter Design

Comparison Criterion	DC-DC IMMC Configuration	TMMC
Power generation	1MW	1MW
Number of PV plants	Two 0.5MW PV plants	One 1MW PV plant
PV plant output voltage	1,500v	1,500v
Switching frequency	20kHz	20kHz
DC-DC converter modularity	Modular (optimizing parallel submodules)	Modular (optimizing parallel submodules)
Number of half-bridge submodules	$2 * \sum_{k=1}^{y=4}(x) = 20$	$\sum_{k=1}^{y=9}(x) = 45$
Controller complexity	Less complex	More complex due to higher number of submodules
Power sharing capability	Allows power sharing between two PV plants	Each PV plant has its own independent MPPT control
Switching device type	SiC 6.5 kV, 200A, 12.5mΩ developed by CREE	SiC 6.5 kV, 200A, 12.5mΩ developed by CREE
Inductance, % ripple	3mH, 5%	3mH, 5%
Capacitance, % ripple	10µF, 15% max	100µF, 5.5% max
DC link capacitor, ripple	20µF, 0.04%	20µF, 1.4%
Total energy stored in capacitors (excluding DC link)	129J (10.5%)	1,228J (100%)
Total energy stored in inductors	517J (44.5%)	1,163J (100%)
Power loss per inducer in submodule P_{IND} (SM4)	P_{IND} = 174W	P_{IND} = 174W
Power losses per device pair in submodule	$P_{switch\ pairs} = P_{Sw} + P_{Cond} = (2{,}000 + 208) =$ 2,208W	$P_{switch\ pairs} = P_{Sw} + P_{Cond} = 2{,}000 + 2{,}200 =$ 2,208W
Power loss per submodule	2,382W	2,382W
Total power loss	$20 * (P_{switch\ pairs} + P_{IND}) =$ = 47.6kW (44.4%)	$45 * (P_{switch\ pairs} + P_{IND}) =$ = 107.2kW (100%)
Efficiency	95.2%	89.3%

3.6 Simulation results

In this section, the simulation results of the proposed converter (see Figure 10) with the design example parameters specified in Tables 1 to 3 are discussed. Figure 17 shows the V_{IMMC1}, V_{IMMC2}, V_{BUS}, V_A, and V_B voltages illustrated in Figure 10. The V_{BUS} of 16kV DC was achieved with a less than 1% voltage ripple. This high-quality DC voltage output with low voltage ripple was realized without the need for over-sizing the DC-DC IMMC submodule capacitors, due to the ripple cancelation technique implemented by phase-shifting V_{IMMC1} and V_{IMMC2} by 180º (as detailed in Equation 12). Figure 18 displays the inductor currents I_{L1}, I_{L2}, I_{L3}, and I_{L4}. As detailed in Equations 4 and 5, the current ripple in the inductors was equal. Also notice that the average inductor current varied from I_{L1} to I_{L4}, as illustrated by Equations 13 to 15. Figure 19 shows the DC-DC IMMC capacitor voltages V_{C1}, V_{C2}, V_{C3}, and V_{C4}; as expected, they were all balanced at 1,625V. The power sharing aspects of the proposed approach are demonstrated in Figures 20 to 23. Due to the effect of unequal shading on PV Plants 1 and 2 (i.e., the PV Plant 2 insolation was set to half its original value), the proposed converter was found to be capable of harvesting the total available power, 750kW (i.e., 500kW from Plant 1 and 250kW from Plan 2), while regulating V_{Bus} at 16kV.

Also, the current I_{Share} was equal to zero when PV Plants 1 and 2 had the same insolation. Figure 24 shows the dynamic response of the proposed converter for different loading and insolation conditions. The transient operation exhibited a stable response. Figure 25 shows a parallel submodule simulation (see Figure 15). Figure 25(a) shows that the V_{C1} ripple was unchanged. Figure 25(b) indicates that the original inductor current I_{L1}

was reduced four times to four equal currents I_{L1_A}, I_{L1_B}, I_{L1_C}, and I_{L1_D}, as illustrated in Figure 15. Figures 26 and 27 offer a simulation comparison between the DC-DC IMMC and TMMC in terms of capacitor voltage ripple. Figure 28 depicts the TMMC inductor current ripple simulation. It can be noticed that the current ripple increased towards the PV plant power source, which enforced more parallel submodule requirements (see Equations 20 and 21).

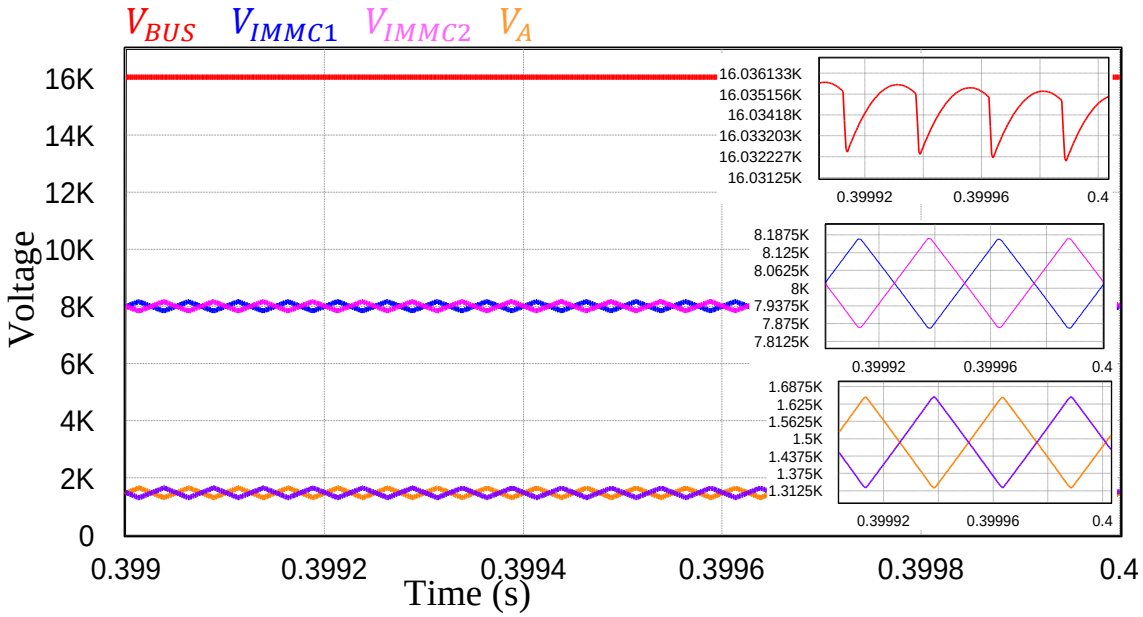


Figure 17 Steady-state voltages for the IMMC: V_{IMMC1}, V_{IMMC2}, V_{bus}, V_A, and V_B.

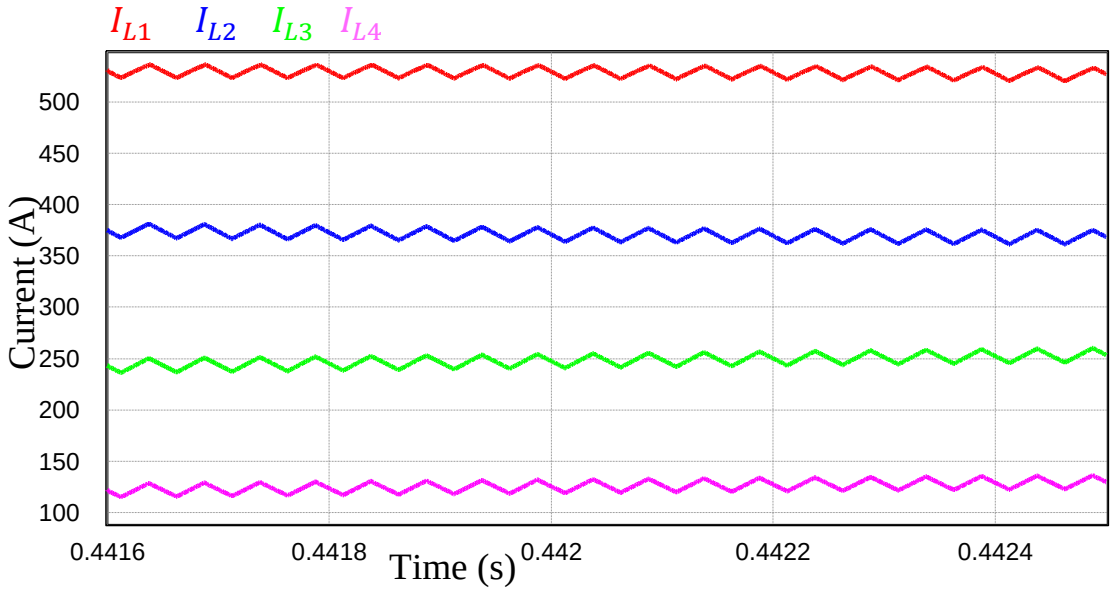


Figure 18 Steady-state inductor currents: I_{L1}, I_{L2}, I_{L3} and I_{L4}.

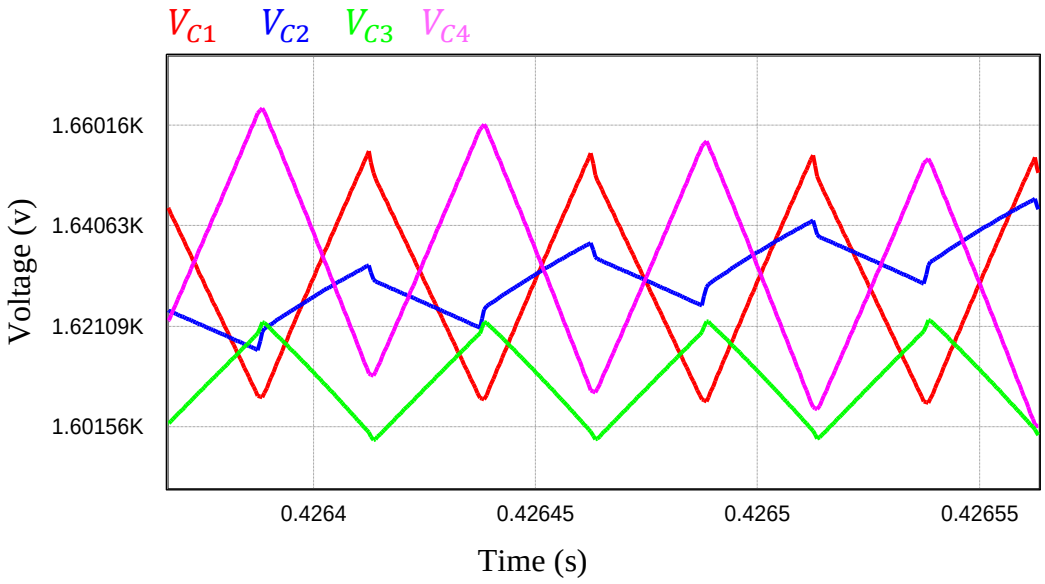


Figure 19 Steady-state capacitor voltages: V_{C1}, V_{C2}, V_{C3}, and V_{C4}; as expected, they were all balanced at 1625V.

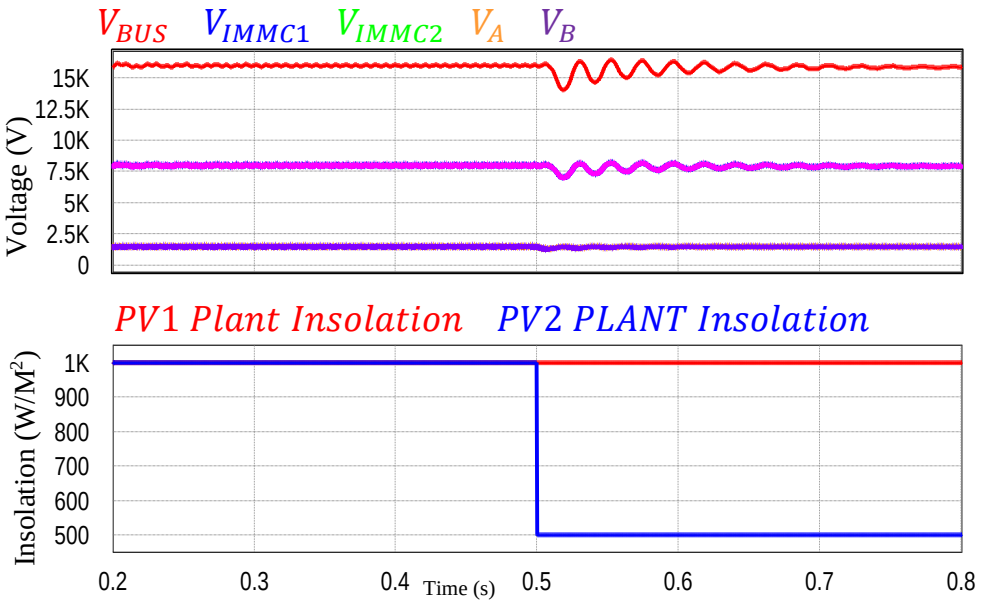


Figure 20 Simulation results showing a change in insolation level due to partial shading for PV Plant 2 and the resultant DC voltages: V_{IMMC1}, V_{IMMC2}, V_{bus}, V_A, and V_B. The DC voltages were regulated.

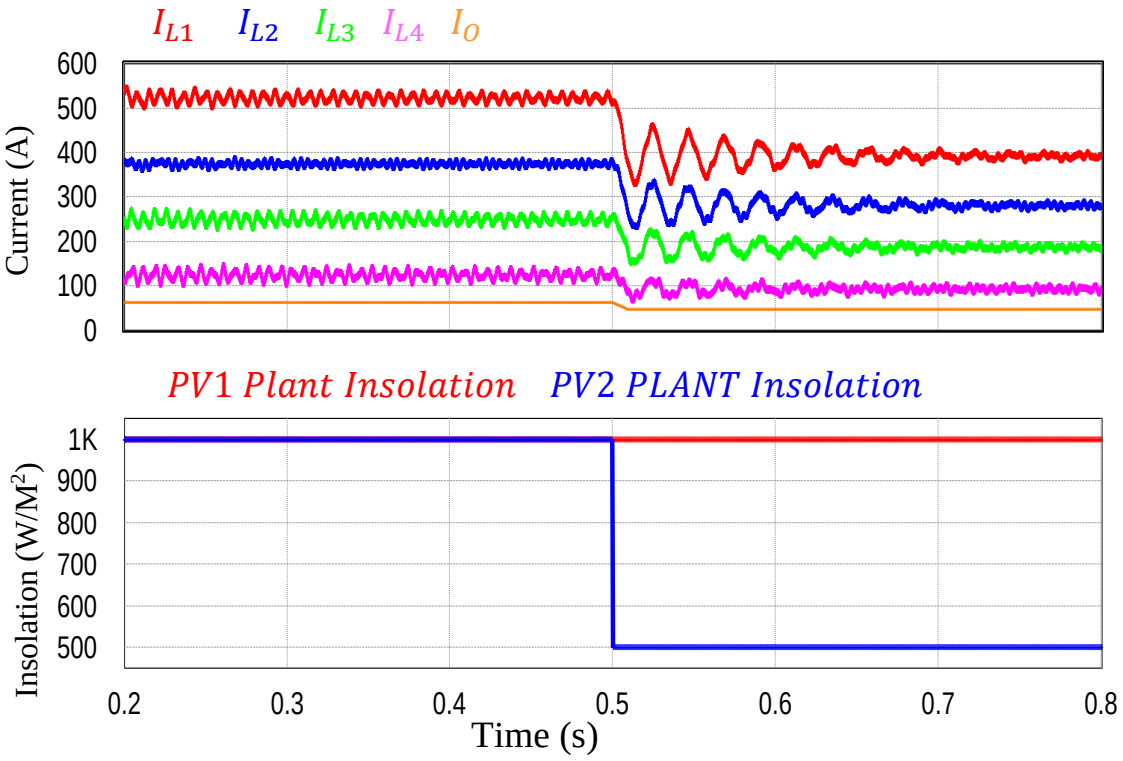


Figure 21 Simulation results showing a change in insolation level due to partial shading for PV Plant 2, and the resultant inductor currents. There was a decrease in the average current due to the insolation reduction.

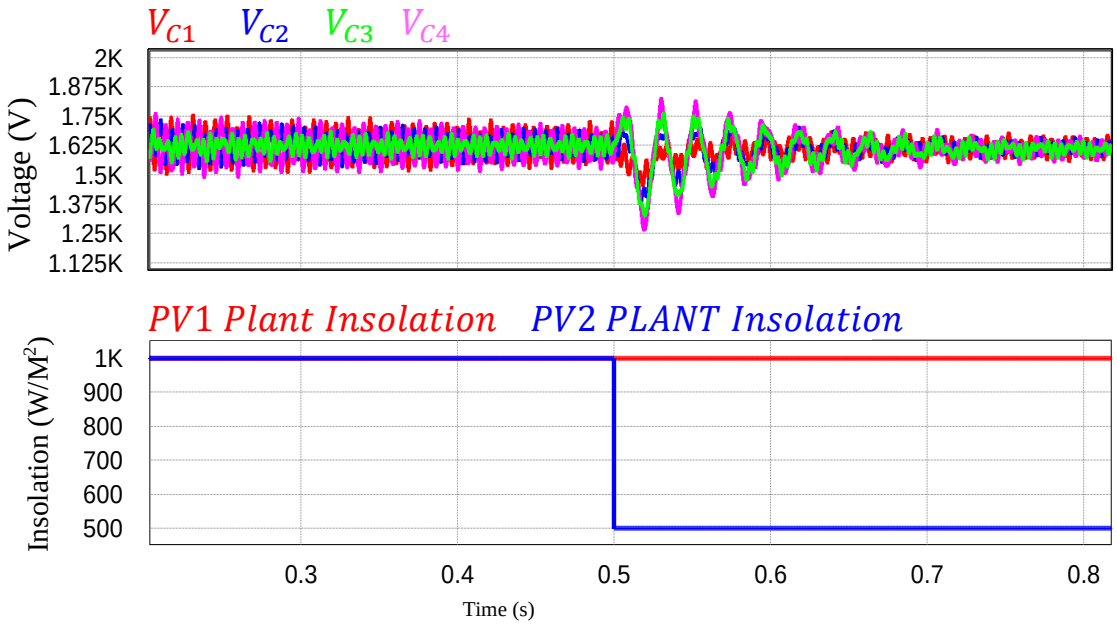


Figure 22 Simulation results showing a change in insolation level due to partial shading for PV Plant 2, and the resultant capacitor voltages. The voltages were regulated.

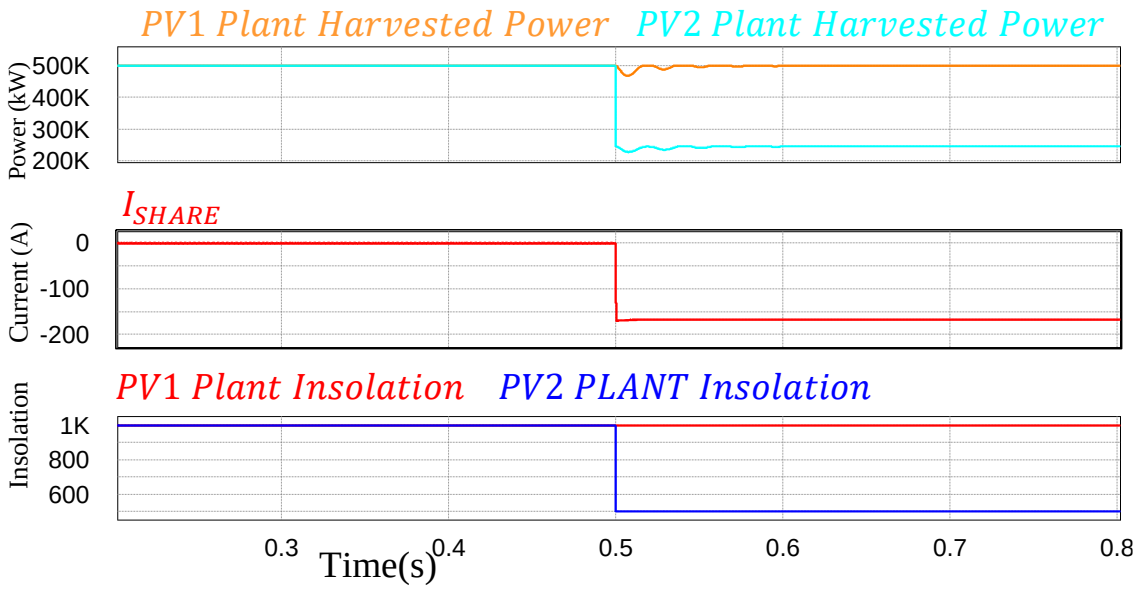


Figure 23 Simulation results showing the performance of the power sharing converter (SM9). The current I_{SHARE} was altered to adjust to different MPPT points, due to the insolation change.

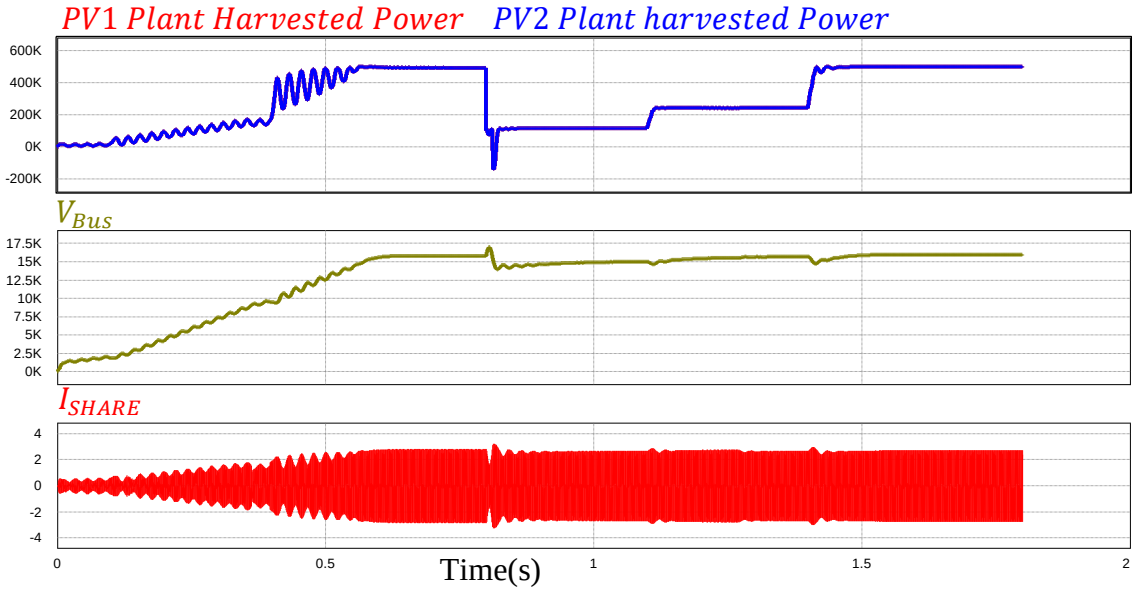


Figure 24 The dynamic response of the proposed converter under different loading and insolation conditions.

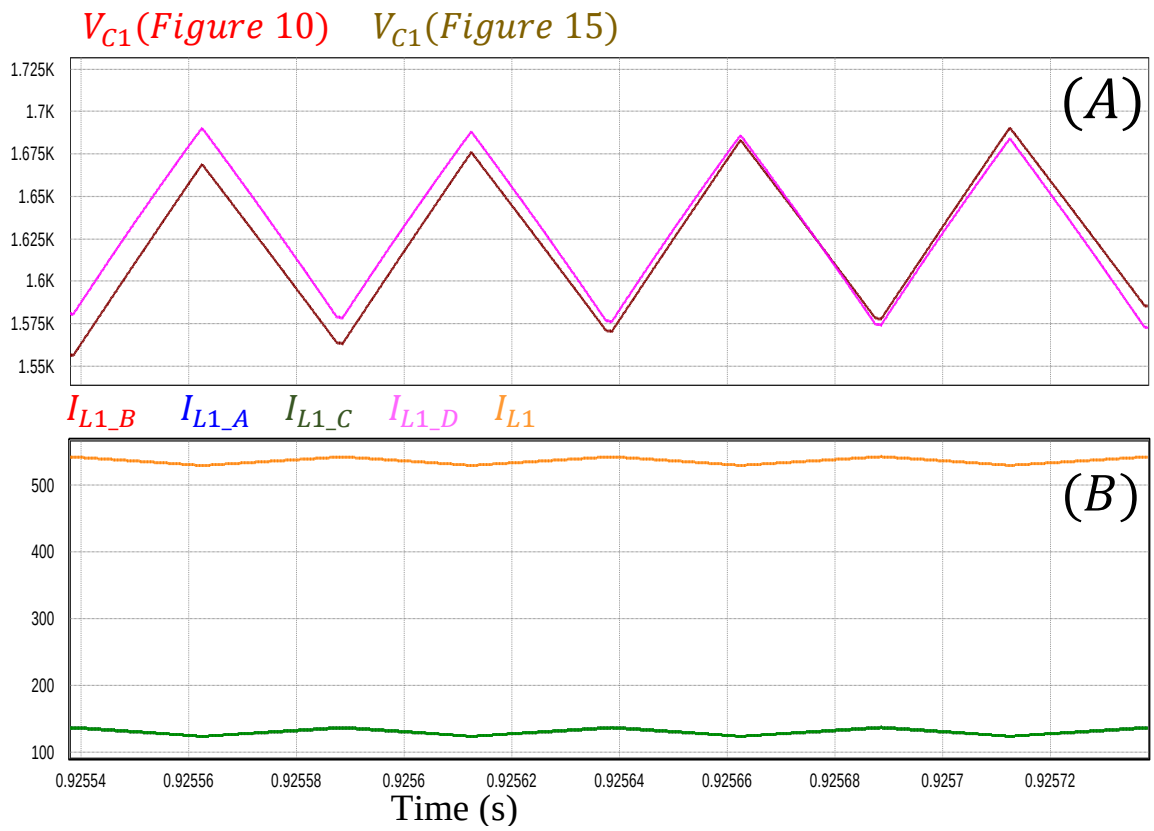


Figure 25 Parallel submodule simulation: (a) V_{C1} was unchanged and (b) the inductor current I_{L1} was divided equally, four times ($I_{L1}/4$).

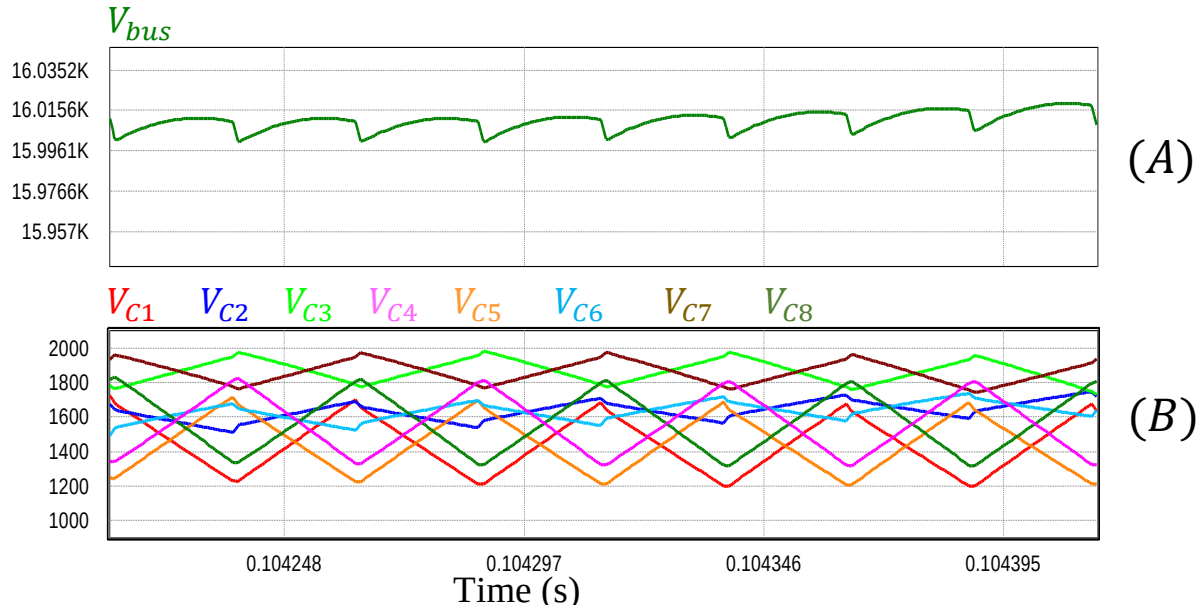


Figure 26 (a) Simulation of the DC-DC IMMC showing a 0.4% ripple of V_{Bus}, and (b) V_{C1} to V_{C8} voltages. The V_{C1} high 15% voltage ripple in the upper IMMC was 180° phased, as opposed to V_{C5} in the lower IMMC. Thus, the ripples cancelled each other out. Similarly, the V_{C2} ripple cancelled out V_{C6}, and so on.

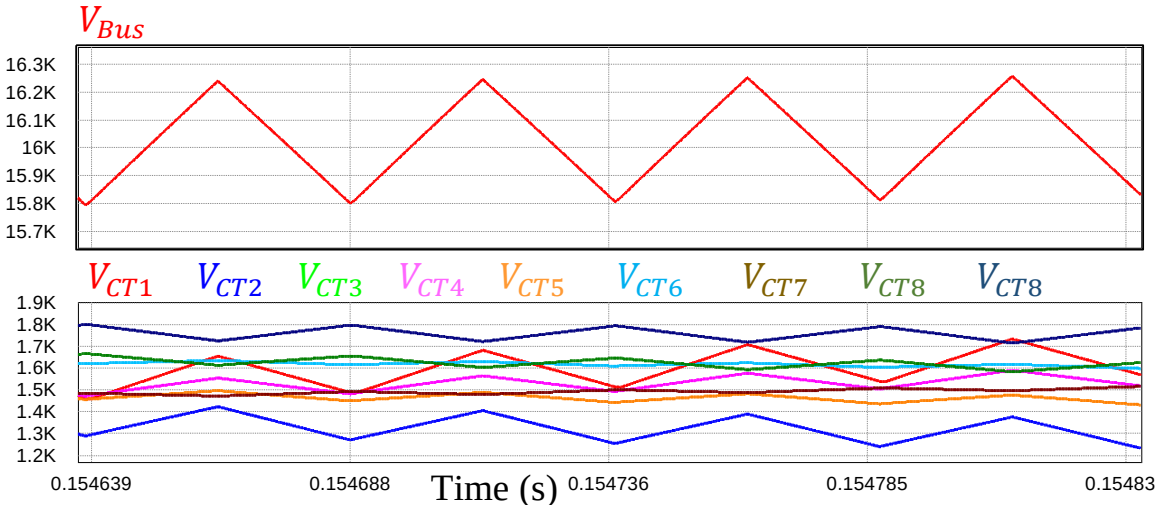


Figure 27 TMMC voltage ripple simulation. Although the capacitance was 10 times greater than that of the DC-DC IMMC, the ripple accumulating towards the DC link enforced high capacitor design ratings.

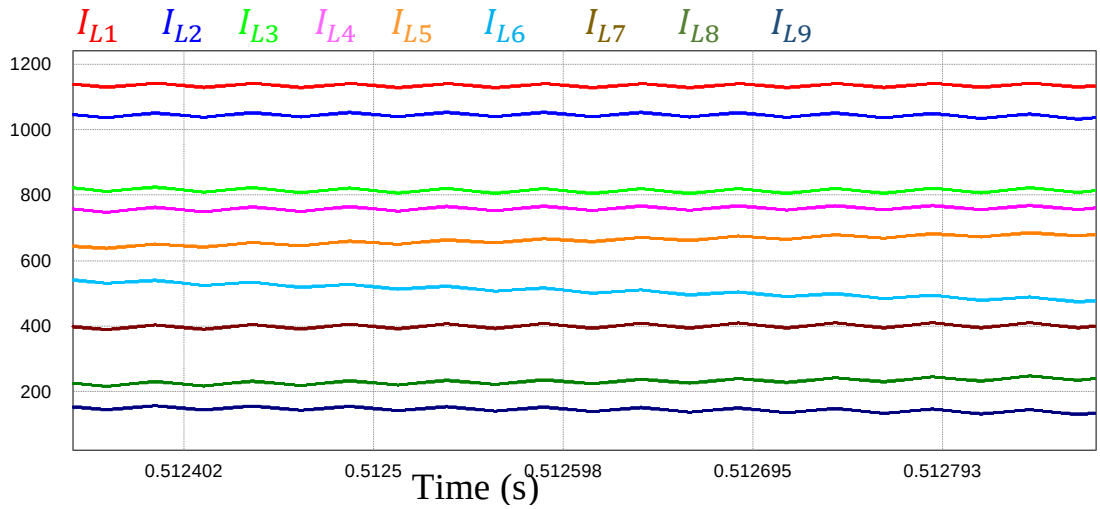


Figure 28 TMMC inductor current ripple simulation. The current ripple increased towards the PV plant power source.

3.7 Experimental setup and results

This section discusses the experimental results from a scaled down laboratory prototype employing GaN half bridge modules. Figure 29 shows the hardware prototype for the proposed upper half of the IMMC (see Figure 11). The input voltage V_A shown in Figures 30 and 31 represents the PV Plant 1 voltage after the power sharing stage. For simplicity, it was assumed to be an ideal DC voltage source. Four half-bridge modules were connected in series, as shown in Figure 11, along with the inductors and capacitors. A TIF28335 DSP designed by Texas Instruments in Dallas, TX, USA was employed as the PWM controller. The selected switching device for this experiment was the LMG3410-HB-EVM GaN. The GaN belongs to the family of wideband gap devices and shares similar high performance and low power loss properties with the proposed SiC device. Table 4 indicates the experimental setup parameters. A power rating of 0.5kW was chosen based on the implementation in Figure 11.

Figures 30 and 31 show the experimental waveforms for the four stages of the upper DC-DC IMMC. Figure 30(a) shows a high gain in DC output V_{IMMC1} of 445V. The voltage ripple in the DC output V_{IMMC1} is also noticeable. However, when the lower half of the converter was implemented, it could be controlled to have the opposite phase of the voltage ripple, resulting in ripple cancellation (as shown in the simulation results). Figures 30(b) and 30(c) also verify the capacitor voltage balance. Figures 31(a) through 31(c) show the current waveforms in the inductors. The total power efficiency of the tested prototype was determined to be 89.2%. This efficiency can be further improved with better control and ZVS.

Table 4 DC-DC IMMC Prototype Design Parameters

Experimental Prototype	
Input voltage V_A	90V
Output voltage V_{IMMC1}	445V
Inductor values L_1 to L_4	100µH
Capacitors values C_1 to C_4	100µF
Switching frequency	100kHz
Switching devices T_1 to T_4	LMG3410-HB-EVM GaN device rated 600V and 12A at peak
DC load	0.5kW
Efficiency	89.2%

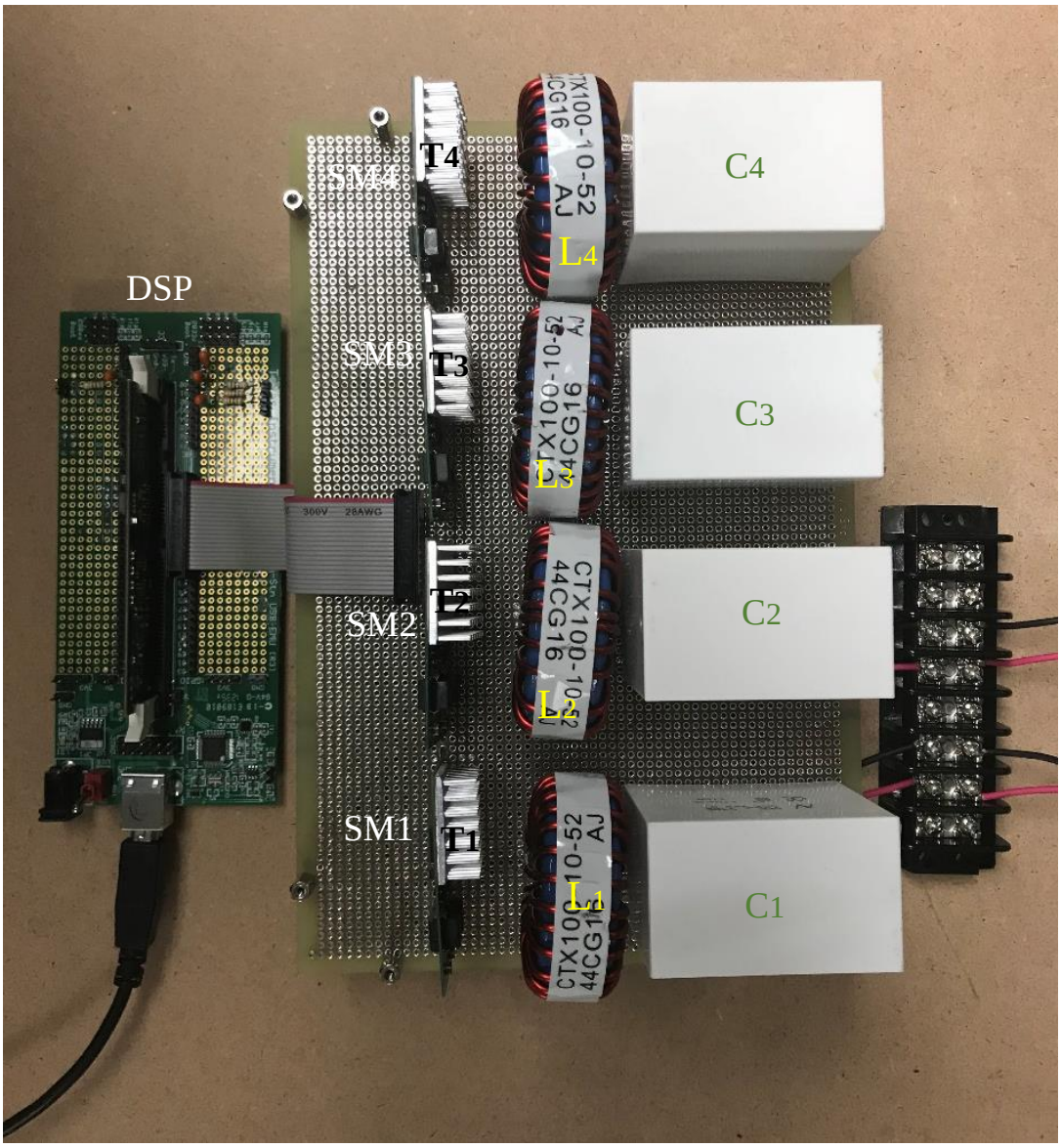


Figure 29 Laboratory prototype of the upper half of the DC-DC IMMC.

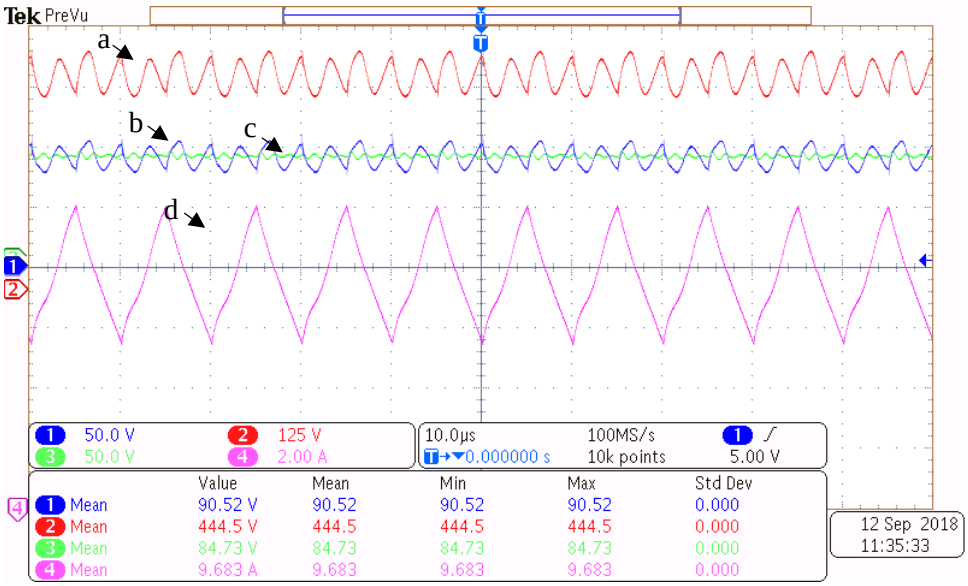


Figure 30 Experimental results of the proposed DC-DC IMMC operating on a reduced scale: (a) V_{IMMC1} y-axis: 125 v/div, x-axis: 10µs/div; (b) V_{c1} y-axis: 50v/div, x-axis: 10µs/div; (c) V_{c2} y-axis: 50v/div, x-axis: 10µs/div; and (d) I_{L1} y-axis: 2A/div, x-axis: 10µs/div.

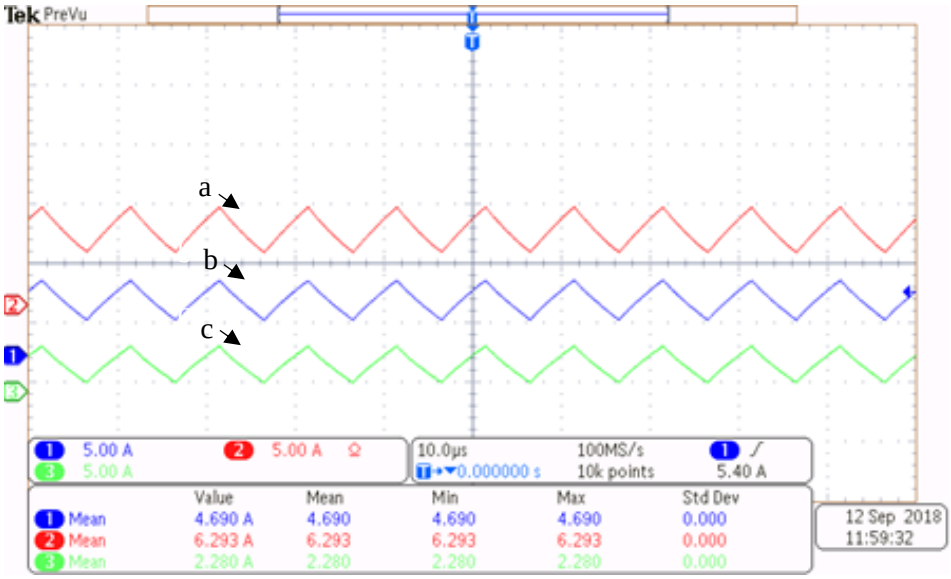


Figure 31 Experimental results for the proposed DC-DC IMMC operating at a reduced scale: (a), (b), and (c) are inductor currents I_{L2}, I_{L3}, and I_{L4}, respectively; y-axis: 5A/div, x-axis: 10µs/div.

4. A SINGLE-PHASE TRANSFORMERLESS MICROINVERTER WITH INTEGRATED BATTERY STORAGE SYSTEM FOR RESIDENTIAL APPLICATIONS[2]

4.1 Introduction

The transformerless microinverter shown in Figure 32(b) offers the optimum efficiency and size, as compared to its transformer-based counterparts (see Figure 32(a)). However, transformerless microinverters suffer from the requirement of a large passive power decoupling (PPD) DC link capacitor. The DC link handles the second harmonic power ripple caused by the single-phase inverter. Furthermore, the DC link design is bulky because it must account for the stringent requirement of a 1% DC bus voltage ripple [44]. Consequently, DC link capacitor selection is limited to the electrolytic capacitor, which has the highest permittivity and energy density. Unfortunately, electrolytic capacitors suffer from a high ESR, high ESL, short lifetime, loss of capacitance, and low RMS current capability.

As a result, several active power decoupling (APD) topologies have been proposed in the literature to address this concern. These topologies incorporate additional DC-DC or DC-AC stages to process the second harmonic power and allow for lower energy storage

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capacitors such as film-type capacitors [45, 61-64]. The efficient film capacitor enhances the overall converter reliability and allows for a failure rate nearly two orders of magnitude lower than that of aluminum electrolytic capacitors [42].

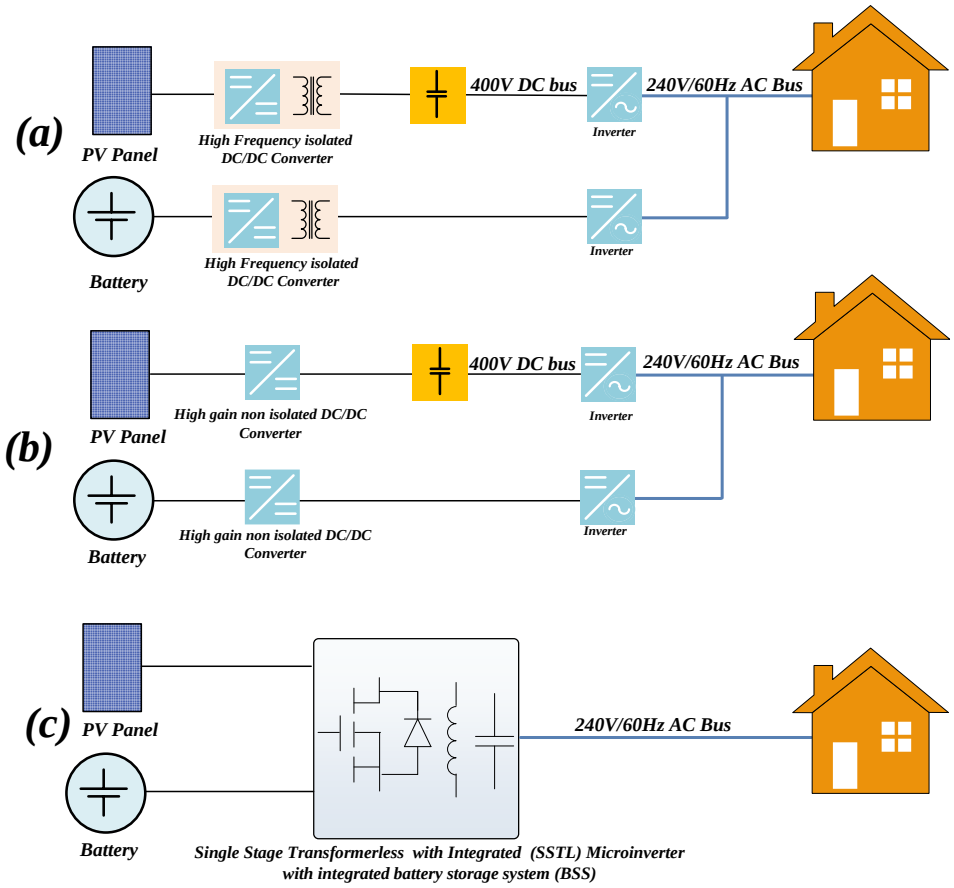

Figure 32 Evolution of the microinverter with additional battery storage electrical systems: (a) isolated microinverter topology introduced in the literature [40, 41], (b) transformerless topology proposed in the literature to enable non-isolated microinverters [44, 45], and (c) proposed SSTL microinverter with integrated BSS.

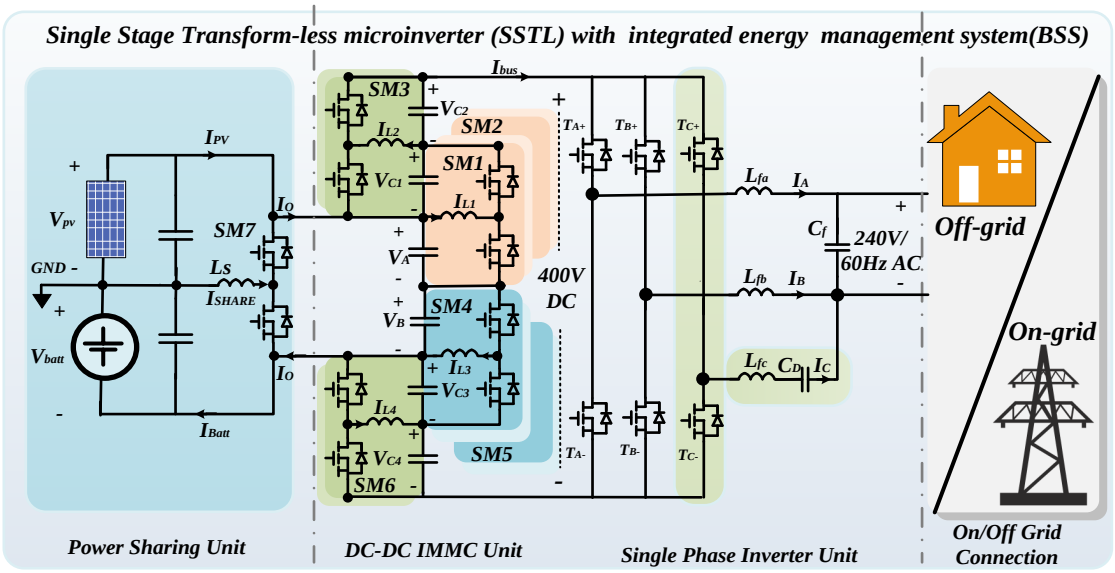

Figure 33 Proposed SSTL microinverter.

Another major consideration regarding microinverters is their ability to harvest power in varying weather conditions. Solar power's intermittent nature inevitably reduces the ability of a microinverter to harvest the huge amount of solar power that's available. Therefore, the hybrid PV/battery microinverter explored in [65, 66] used a transformer-based approach. This approach utilizes the trendy Li-ion battery and allows for the battery, power electronics, and PV to be integrated into a single unit. In [66] , on-grid and off-grid microinverter operations were investigated for transformer-based topologies, including dual active bridge and fly-back family of topologies. Thus, there is a knowledge gap regarding the hybrid PV/battery transformerless microinverter illustrated in this study.

In view of this, an SSTL microinverter with an integrated BSS is proposed, as shown in Figure 32(c). The detailed circuit topology of the proposed converter is shown in Figure 33. The proposed system is envisioned as a power semiconductor unit with a compact size that integrates three different functions into one. The first stage is the power sharing unit that manages the MPPT and battery charge/discharge operation. The second unit is a DC-DC IMMC employing a two-stage multilevel converter to boost the DC output to 400V. The 180^{o} phase shift control and symmetry of the upper and lower DC-DC IMMC units ensures DC link voltage ripple cancellation, as illustrated in Section 3. The IMMC unit is followed by a single-phase inverter with a built-in active decoupling stage, achieving a high-quality sinusoidal output of 240/120V. The active decoupling leg cancels the double-line frequency caused by the single-phase PWM inverter [45, 61-64]. Therefore, the active decoupling stage is controlled to match the power ripple of the grid to the reactive power of the decoupling capacitor. This function, along with the 180^{o} phase shift control of the DC-DC IMMC stage allows for full elimination of the bulky electrolytic DC link capacitor. The DC link energy storage requirement is impeded in minimized distributed film capacitors, which are an integral part of an IMMC unit. The SSTL microinverter was designed to adopt an on-grid off-grid operation and shows improved results in cases of nonlinear load conditions.

The proposed SSTL microinverter with integrated BSS has the following advantages:

- Integration of the PV and battery into a single topology with power sharing abilities and one controller.
- The DC-DC IMMC employs low voltage half bridge converters with film capacitors that form the dc-link. Furthermore, the 180^{o} phase shift control of the DC-DC IMMC, ensures the cancellation of the voltage ripple across the DC link.
- An active power decoupling stage in the DC-AC inverter compensates for the twice frequency component due to single output further reducing the DC link filter size.
- Effective operation in on-grid and off-grid cases.
- Bidirectional power flow allows for battery charge/discharge function.
- Full utilization of battery storage.
- Enhancement of inverter performance under nonlinear loads.
- Wide range of input voltages for different PV and battery ratings.

4.2 System architecture and operation principle of the proposed approach

As discussed in the previous section, the proposed SSTL with integrated BSS shown in Figure 33 is divided into three units: 1) power sharing, 2) DC/DC IMMC, and 3) inverter. The principles of operation for these units are briefly explained below.

4.2.1 Power sharing unit

The power sharing unit consists of a PV and battery with a center ground point. The PV system's negative terminal was selected to be the ground to avoid potential induced degradation (PID)[67-69].

4.2.1.1 Power sharing unit operation

The operation of the power sharing unit shown in Figure 33 is summarized in six modes, as shown in Figure 34 (similar to the power optimizer in [64]). The power sharing unit intelligently controls the magnitude and direction of I_{share} in accordance with the modes of operation shown in Figure 34, where:

$$I_{share} = I_{PVMax} \mp I_{Batt} \tag{22}$$

Mode 1 shows a scenario where the available PV power is 1pu, while the grid consumes 1pu base power. In this case, the full PV power is sent to the grid. Thus, I_{share} is regulated to match the PV current I_{share} as

$$I_{share} = I_{PVMax} \tag{23}$$

The 0pu and 1pu of the battery corresponds to an SoC of 40% and 80%, respectively. Therefore, the I_{share} is selected depending on optimum power harvesting without over-charging or under-charging the battery. Table 5 summarize all six modes of operation described in Figure 34.

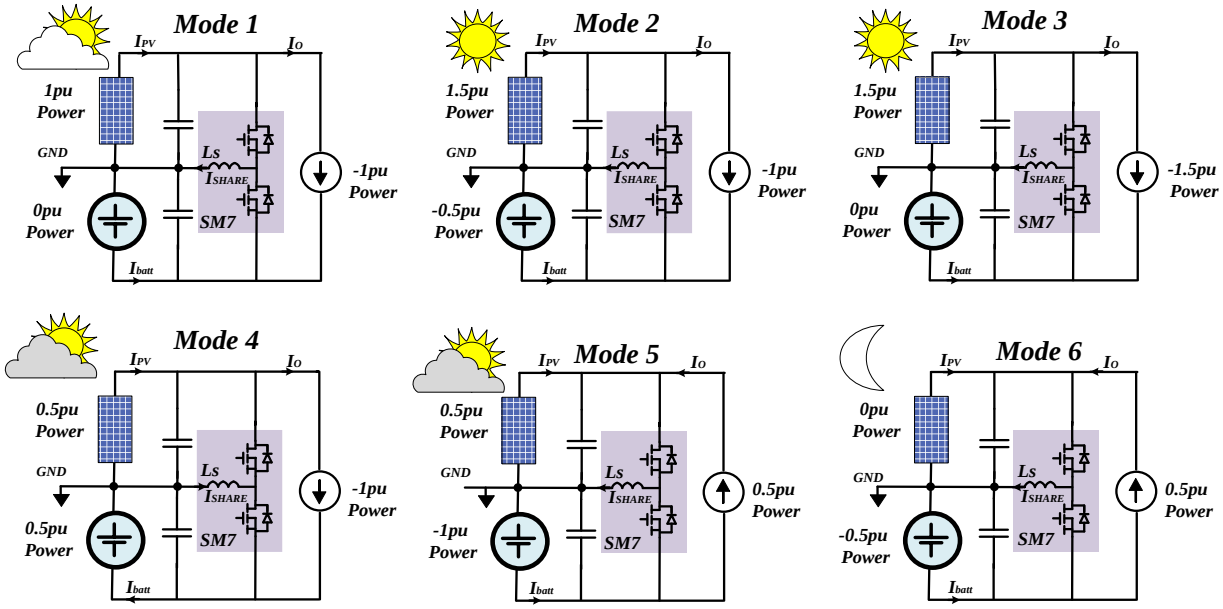

Figure 34 Shows the six modes of operation for the power sharing unit as detailed in Table 5.

Table 5 Six Main Modes of Operation of the Power Sharing Unit.

Mode #	Available PV, power in p.u.	Battery Power in p.u.	Grid power in p.u.	Required I_{share} reference
1	1	$0 \leq P_{batt} \leq 0.5$	-1	I_{PVMax}
2	$1 < P_{pv} \leq 1.5$	$-0.5 \leq P_{batt} < 0$	-1	$I_{PVMax} + I_{Batt}$
3	$1 < P_{pv} \leq 1.5$	$-0.5 \leq P_{batt} < 0$	-1.5	I_{PVMax}
4	$0.5 < P_{pv} < 1$	$0 < P_{batt} \leq 0.5$	-1	$I_{PVMax} - I_{Batt}$
5	$0 < P_{pv} \leq 0.5$	$-1 < P_{batt} \leq -0.5$	0.5	$-I_{PVMax} - I_{Batt}$
6	≈ 0	$-1 < P_{batt} < 0$	$0 \leq P_{grid} \leq 1$	I_{Batt}

Mode 2 illustrates an excess available PV power condition of 1.5pu, while the grid still consumes the equivalent 1pu of power. In this scenario, the excess 0.5pu of power is sent to charge the battery. To maintain the PV current at the MPPT, the current I_{share} is set to:

$$I_{share} = I_{PVMax} + I_{Batt} \tag{24}$$

In weather conditions similar to those of Mode 2, where access power of 1.5pu is available, Mode 3 can also be performed. In Mode 3, the full 1.5pu of power is sent to the grid. As a result, I_{share} needs to be regulated to match I_{PVMax}. Therefore, the I_{share} value is reduced compared to in Mode 2. This offers a minimized device rating, as well as a reduced inductor size L_s.

Mode 4 shows a weather condition where the available PV power is 0.5pu. In this situation, the battery supplies the remaining 0.5pu to fill the power grid shortage. Hence, the battery current I_{Batt} direction will be reversed and I_{share} needs to be regulated as:

$$I_{share} = I_{PVMax} - I_{Batt} = 0 \tag{25}$$

In Mode 5, the grid is turned to regenerative mode and supplies 0.5pu of power. The assumed available PV power is still 0.5pu. Therefore, the battery storage will be charged at a 1pu rate, and I_{Batt} will reverse its direction again. Hence, I_{share} needs to be controlled such that:

$$I_{share} = -I_{PVMax} - I_{Batt} \tag{26}$$

In Mode 6, the grid is still in regenerative operation and supplies 0.5pu of power. The available PV power is dropped to 0pu, due to the nighttime condition. Thus, all of the grid power will be utilized to charge the battery. Therefore, the battery will be charged at a 0.5pu rate and I_{share} needs to be controlled such that:

$$I_{share} = I_{Batt} \tag{27}$$

It should be noted that Mode 6 is preferable to Mode 5 for regenerative operation, due to its reduced I_{share} value.

Equations 27 and 28 define the required inductance value. In case of macheted PV and battery voltage rating, d_7 is selected to be 0.5. In general, the inductor current ripple Δi_{Ls} needs to be sufficiently low to ease the control of d_7.

$$V_{PV} = \frac{L_s \Delta i_{Ls}}{d_7} \tag{28}$$

$$V_{batt} = \frac{L_s \Delta i_{Ls}}{1 - d_7} \tag{29}$$

4.2.1.2 Controller of the power sharing unit

Generally, for all six modes, the duty cycle d_7 is used to calibrate the SM7, to track the suitable I_{share} in accordance with Table 5. The following formulas express the relationship between $I_{PVmax}, d_7, I_o,\ I_{share},$ and I_{batt}:

$$I_{PVmax} = (1 - d_7)(I_o) + (d_7)(I_o + I_{share}) \tag{30}$$

$$I_{batt} = (1 - d_7)(I_o - I_{share}) + (d_7)(I_o) \tag{31}$$

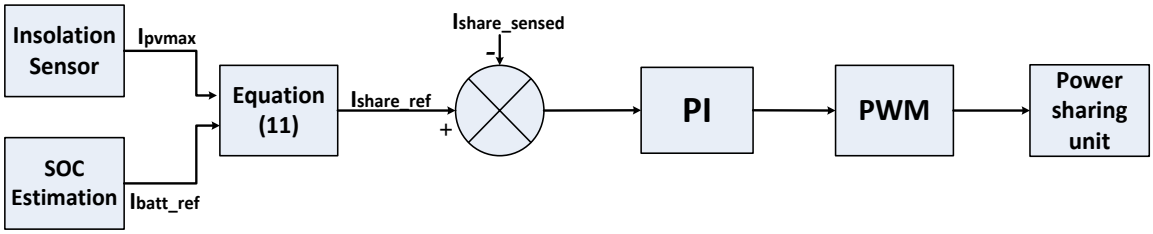

Figure 35 Controller of the power sharing unit.

Figure 35 shows a block diagram of the power sharing unit. The current I_o shown in Equations 30 and 31 is controlled by the inverter unit. Thus, it is assumed to be a known value. Moreover, the required battery current I_{Batt} is computed depending on the mode of operation, as shown in Table 5. The objective of the controller is to track the I_{PVmax} and maintain the battery's SoC within a 40% to 80% range, in order to offer an extended lifetime for the integrated storage system.

4.2.2 DC/DC IMMC unit

Figure 33 shows the DC-DC IMMC unit detailed in Section 3. This stage is synthesized with reduced voltage half-bridge GaN inverter blocks connected in series to support high-gain voltage DC conversion. The GaN half-bridge blocks are capable of switching at a high frequency (i.e., 100kHz). Thus, a compact size/weight in conjunction with high efficiency conversion is achieved. The IMMC units are divided into upper IMMC (SM1 and SM2) and lower (SM3 and SM4) subunits, where each boosts the input voltage from 50V (V_A) to 200V (V_{IMMC1}) to achieve a total of 400VDC (V_{BUS}). The upper IMMC average voltage is found using Equations 3 and 12, such that:

$$V_{IMMC1} = V_A \cdot \left(1 + \frac{d_1}{1-d_1} + \frac{d_1 \cdot d_2}{(1-d_1)(1-d_2)}\right) \tag{32}$$

$$V_A = \frac{(V_{PV} + V_{Batt})}{2} \tag{33}$$

where d_1 and d_2 are the duty cycles for SM1 and SM2, respectively, as displayed in Figure 33. The passive components L_1 to L_4 and $C_1$to C_2 are found using Equations 4 through 9. SM1 and SM3 have parallel configurations similar to what is shown in Figure 15, in order to allow for a modular design. The total voltage ripple of the upper and lower IMMC boost converters are thematically canceled, due to the 180^o phase shift control.

4.2.3 Single-phase inverter with integrated active decoupling unit

4.2.3.1 Operation of single-phase inverter with APD

The inverter unit shown in Figure 33 is synthesized with a single-phase PWM inverter with a built-in active decupling stage [61]. The active decoupling stage is required to process the double-line frequency and match the input DC power P_{ab} with the output AC power P_{ab}. The power ripple at the load port is defined as:

$$P_{ab}(t) = \frac{I_{a\_max}V_{ab\_max}}{2}(cos\theta_1 - \cos(2\omega t + \theta_1)) \tag{34}$$

Similarly, voltage, current, and power on the active decoupling subunit shown in Figure 33 can be found as [61]:

$$P_{cb}(t) = \frac{I_{c\_max}V_{cb\_max}}{2}(\cos(\theta_2 - \theta_3) - \cos(2\omega t + \theta_2 + \theta_3)) \tag{35}$$

To achieve double-line frequency ripple cancelation, the following equation must be satisfied:

$$i_a(t) \cdot v_{ab}(t) + i_c(t) \cdot v_{cb}(t) = P_{dc} = V_{bus} * I_{bus} \tag{36}$$

where P_{dc} needs to be maintained at a constant value. In [61], V_{cb_max} and I_{c_max} are calculated as follows:

$$V_{cb\_max} \approx \sqrt{\frac{I_{a\_max} V_{ab\_max}}{\omega C_d}} \tag{37}$$

$$I_{c\_max} \approx \omega C_d \, V_{cb\_max} \tag{38}$$

The phase angles θ_2 and θ_3 are found using:

$$\theta_3 \approx \theta_2 + \frac{\pi}{2} \tag{39}$$

$$\theta_2 \approx \theta_1 + \frac{\pi}{4} + \pi n$$

$$\text{where } n = 0, \pm 1, \pm 2, \pm 3 \tag{40}$$

With a proper active decoupling leg design side-by-side with a high switching frequency, the double-line frequency will be optimally eliminated. Consequently, the power sharing unit (SM7), DC-DC IMMC units (SM1 through SM6), and inverter unit are all merged into a single stage, without a bulky transformer or substantial DC link buffer requirements.

4.2.3.2 Controller structure of the single-phase inverter with APD

Figure 36 shows the controller structure for the DC to AC inverter unit with APD integration (shown in Figure 33). The lower part of Figure 36 illustrates the mechanism for controlling the inverter in both on-grid and off-grid operations. In the case of off-grid operations, the inductor current i_a shown in Figure 33 is needed as the main input to the controller. The i_a goes through stages of filters to create two orthogonal current components necessary for power factor phase angle identification. A suitable V_{cb} is generated based in Equation 37. Conversely, on-grid operation incorporates an additional phase locked loop (PLL) stage and PI controller to track the desired reference grid current. In addition, a power factor reference is deployed to allow for bidirectional power

operation, as well as reactive power injection. A smart control design tool is used to find the PI parameters. Figure 37 illustrates the gain and phase responses of the inverter circuit in the smart control tool created by Powersim. The selected proportional gain K_i and time constant T_i offers a stable response and effectively follows the grid current, as shown in the closed loop curve (in brown).

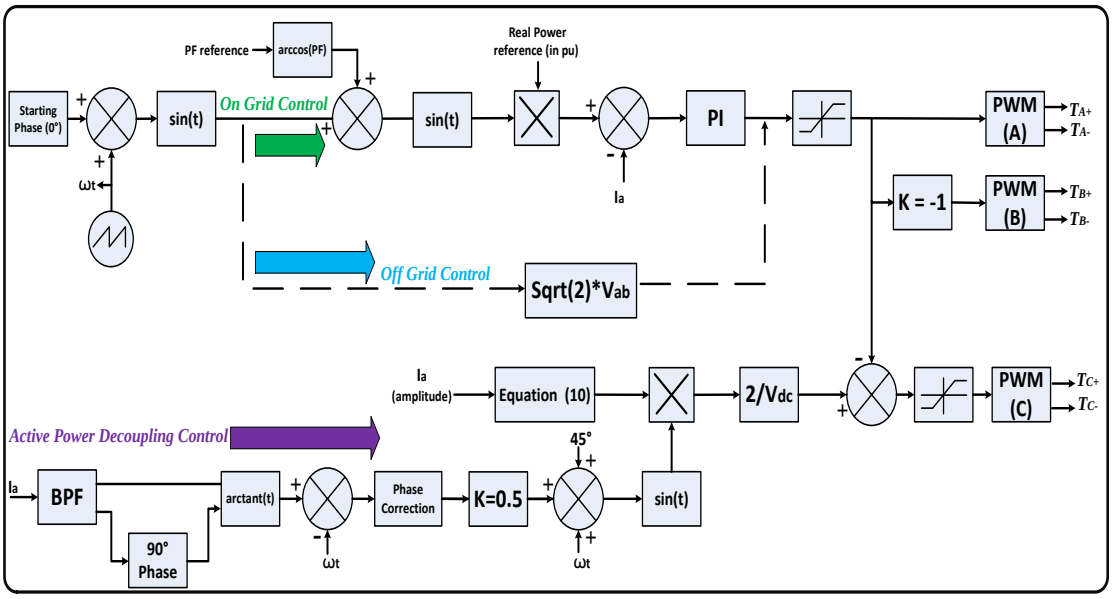

Figure 36 Overall control of the proposed SSTL microinverter with integrated BSS.

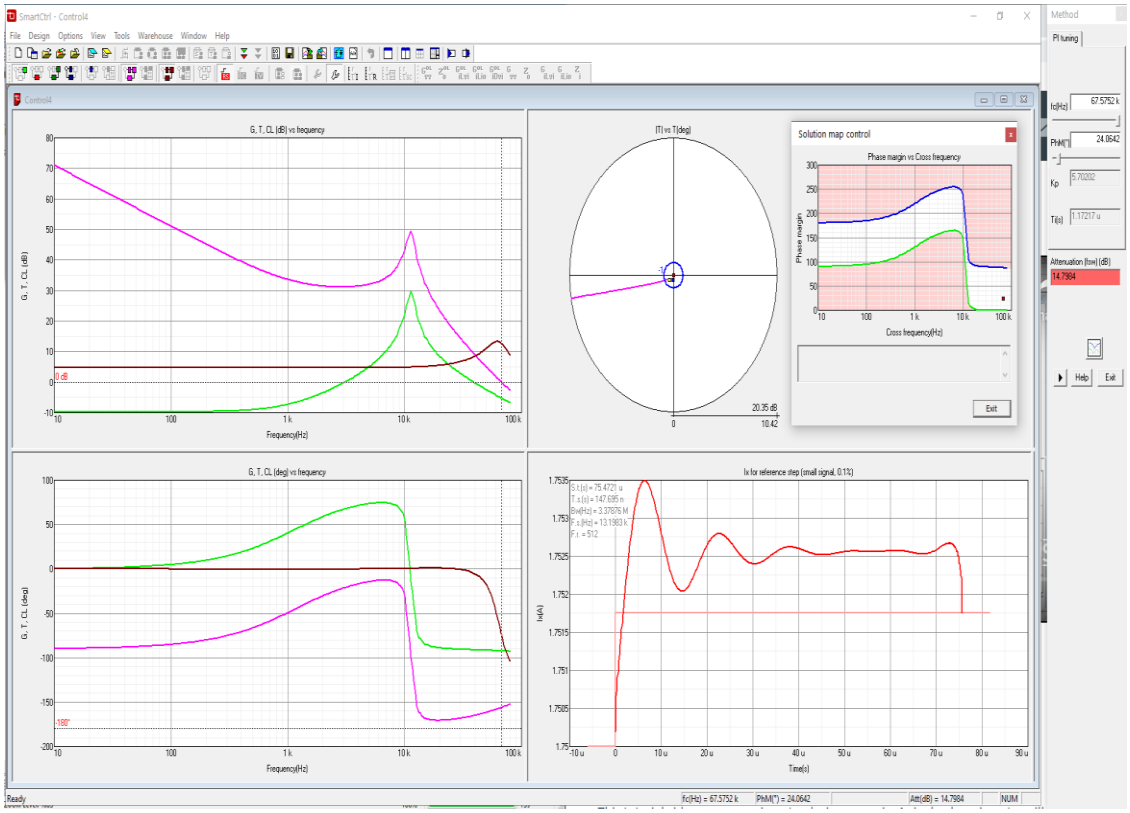

Figure 37 Smart control design used to find PI parameters.

4.3 Design example

In this section, a design example of a 420W (1pu) SSTL microinverter is illustrated. The design strategy began with selecting a suitable PV module and battery storage. Then, the IMMC and inverter stages were designed accordingly.

4.3.1 PV module and battery storage selection

Table 6 details the PV module and battery storage selected for the SSTL microinverter shown in Figure 33. A monocrystalline PV module called Helios 9T6, rated at 420W, was selected due to its high efficiency and high MPP voltage of ≈ 50V [59]. Moreover, the Helios 9T6 allowed for a high power density converter design, along with a lower step-up voltage. The battery storage DC voltage V_{batt} needed to match the PV MPP voltage to enable voltage ripple cancelation at the DC link. Therefore, a Samsung 50V 20.7Ah Li-ion battery pack was selected [70]. In this design, the battery storage was only allowed to supply/back up half of the rated power (210W). Moreover, the selected SoC range was 40% to 80% to optimize the charging/discharging function performed by SM7. The charging/discharging function for the Li-ion battery model selected was simulated in PSIM, as shown in Figure 38. Assuming no losses, the battery was found to be capable of supplying a PV module shortage of 210W for ≈ 2 hours. The weight of the battery storage was insignificant compared to the PV. This allowed the battery storage to be packed with the SSTL microinverter.

Table 6 Design Specifications for the PV Module and Battery Storage

Parameter	Value
Selected PV module	Helios 9T6 [59]
Maximum power, voltage, and current	420W, 49.5V, 8.5A
Selected battery storage	Samsung 50V 20.7Ah Li-ion battery pack [70]
Weight of the PV module and battery	69lbs, 11.4lbs

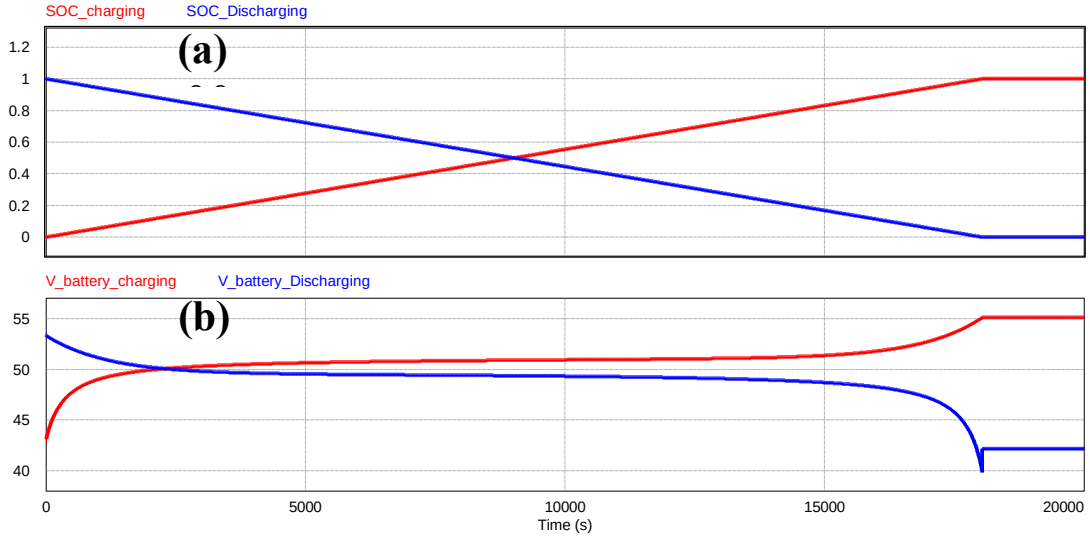

Figure 38 Simulation of the charging/discharging function for the selected Li-ion battery model: (a) SoC of charging and discharging operations and (b) respective battery voltages for charging and discharging cases.

4.3.2 Power sharing and IMMC stage design

The designs for SM1 to SM7 (shown in Figure 33) are detailed in Table 7. The PV module voltage V_{PV} and battery storage voltage V_{batt} can be described as:

$$V_{PV} = V_{batt} \approx 50V \quad (41)$$

Given Equations 32-33, the duty cycle d_1 of SM1 and SM7 was set at 60%, while the duty cycle d_2 was set at 50%. As a result, the capacitor voltages V_{c1} to V_{c4} were found to be:

$$V_{c1} = V_{c2} = V_{c3} = V_{c4} \approx 75V \quad (42)$$

Therefore, each IMMC unit boosted the voltage V_A to 200V, realizing a total of 400V V_{BUS}, as explained in Equations 12 and 33.

4.3.2.1 SM1 to SM7 switching device selection

GaN devices are known to be the most efficient for residential applications [71, 72]. Therefore, GaN based half bridge modules are chosen for this study. The selection was mainly based on the maximum voltage and current rating per submodule. SM7 processed the highest current of 9A (the PV MPP current) at Mode 2 with lowest device voltage stress of voltage stress of $\approx 100V$. Thus, the suitable device for the aforementioned SM7 rating is EPC2034 [73]. Conversely, SM1 through SM4 switched at a higher voltage stress of 2*$V_{c1} \approx 150V$. To accommodate a modular design, SM1 to SM6 needed to be identical. In this case, each switching device SM1 to SM6 was rated at 350V and 6A. Therefore, a EPC2050 was chosen[74]. However, the LMG 3410 GaN-based half bridge module was sufficient for testing various modes of operation in the present research [75].

4.3.2.2 SM1 to SM7 inductor selection

Since SM7 processed the highest current at Mode 2, the SM7 inductor saturation current needed to be designed at 20A. A 100kHz switching frequency was selected to enable an efficient but reduced size. Consequently, a 1.2mH inductor was chosen to achieve a current ripple of $\leq 5\%$ in the SM7. Also, 0.56mH inductance was selected for SM1 to SM6 to maintain a continuous conduction mode of operation and sufficiently reduce the current ripple, in accordance with Equations 4 and 5.

4.3.2.3 Selection of capacitors C_1 to C_4

This section explores the design equations for capacitors C_1 to C_4. Capacitors C_1 and C_3 can be expressed as:

$$\mathrm{C}_{1,3} = \frac{i_s(t) + d_2(t)i_{L2}(t) - i_{L2}(t)}{\frac{dV_{C1,3}}{dt}} \tag{43}$$

while capacitors C_2 and C_4 can be expressed as:

$$\mathrm{C}_{2,4} = \frac{i_o - (1 - d_2(\mathrm{t}))i_{L2}(t)}{\frac{dV_{C2,4}}{dt}} \tag{44}$$

Since the capacitor voltage ripple across V_{BUS} was cancelled, this enabled capacitors C_1 to C_4 to have more compact capacitor sizing. In this design, 10µF capacitors were selected for C_1 to C_4.

Table 7 Design Details for Power Sharing and DC-DC IMMC Units

Parameter	**Value**
Number of half-bridge submodules	7 (SM1- SM7) for IMMC and power sharing stages
Switching frequency	100kHz
Switching device for SM1 to SM6	EPC2050: 350 V, 26 A Enhancement-Mode GaN Power Transistor [74]
Switching device for SM7	EPC2034: Enhancement-Mode Power Transistor [73]
Inductor size per submodule (except SM7)	0.56mH
Inductor size for SM7	1.2mH
Capacitor size per submodule	10µF
DC bus voltage ($\boldsymbol{V_{BUS}}$)	400V

4.3.3 Single phase inverter unit design

The single phase inverter unit shown in Figure 33 was composed of six GaN switchig devices, an active decoupling capacitor, and passive output LC filter elements. The TI LMG 3410 half-bridge GaN was selected, since it fit with the 240V/120V 50/60Hz output voltage requirment [75].

Using Equation 37, the active decoupling capacitor C_d can be described as:

$$C_d = \frac{I_{a\_max} \cdot V_{ab\_max}}{\omega \cdot V_{cb\_max}^2} \tag{45}$$

With careful design, V_{ab_max} and V_{cb_max} were assumed to be equal in magnitude. Thus, Equation 46 is a simplified version of the C_d design. Hence, the I_{a_max} expressed in Equation 46 incorporates the current ripple ΔI_{a-PP} that is added to I_a.

$$C_d = \frac{I_{a\_max}}{\omega \cdot V_{ab\_max}} \tag{46}$$

Table 8 Design Details for the Inverter Unit

Parameter	**Value**
Switching frequency	100Khz
Switching device	3410 GaN based half bridge submodule manufactured by Texas Instruments [76]
Filter inductors $\boldsymbol{L_{fa}}$, $\boldsymbol{L_{fb}}$, and $\boldsymbol{L_{fc}}$	1.2mH
Filter capacitor $\boldsymbol{C_f}$	10µF
Decoupling capacitor size $\boldsymbol{C_d}$	20µF
DC bus voltage ($\boldsymbol{V_{BUS}}$)	400V

With regards to output filter sizing, three filter inductors were employed for each leg, as shown in Figure 33. The main inverter was operated in a unipolar PWM scheme to permit a smaller passive filter size. The filter inductor L_f was designed according to Equation 47.

$$L_{fa,b,c} = \frac{V_{DC}}{8 f_s \Delta I_{a\_pp}} \tag{47}$$

The filter capacitor C_f was required to keep the maximum peak-peak amplitude of switching frequency load ripple voltage below the limit $\Delta V_{AC\_out,pp\_max}$ given by Equation 47. It also needed to be sufficiently smaller than C_d. Therefore, Equation 48 is used to select C_f. Table 8 summarizes the design parameters selected for the inverter unit.

$$C_d > C_f > \frac{\Delta I_{a\_pp}}{8 f_s \cdot \Delta V_{aC\_out,pp\_max}} \tag{48}$$

4.4 Simulation results

Figures 39 to 46 show the simulation results for the SSTL microinverter with BSS (see Figure 33) in the various modes of operation expressed in Table 5 and Figure 34. Figure 39 shows Mode 1, where the PV fully supplies 420W (1pu) of power to the grid. Similarly, Figure 40 shows Mode 3, where 630W (1.5pu) is fed to the grid. Figure 41 expresses Mode 4, where the PV and battery equally supply 210W (0.5pu) of power to the grid, due to cloudy conditions. Figure 42 depicts Mode 6, where grid power charges the battery (e.g., at night). In this mode, the inverter's controller (shown in Figure 36) reverses the grid current direction to allow for a reverse power flow. Figures 43 and 44 demonstrate a detailed simulation for power sharing, IMMC, and inverter stages for Modes 1 and 5. High-quality sinusoidal inductor currents $I_a, I_b,$ and I_c were achieved, in line with the design requirements. A 240V 60Hz AC output was met with THD < 3%. Figures 45 and 46 show on-grid operation. The DC link current I_{dc} shown in Figure 33 doesn't contain a second harmonic, due to APD integration. Moreover, the magnitude and direction of I_{dc} is regulated via the inverter controller shown in Figure 36.

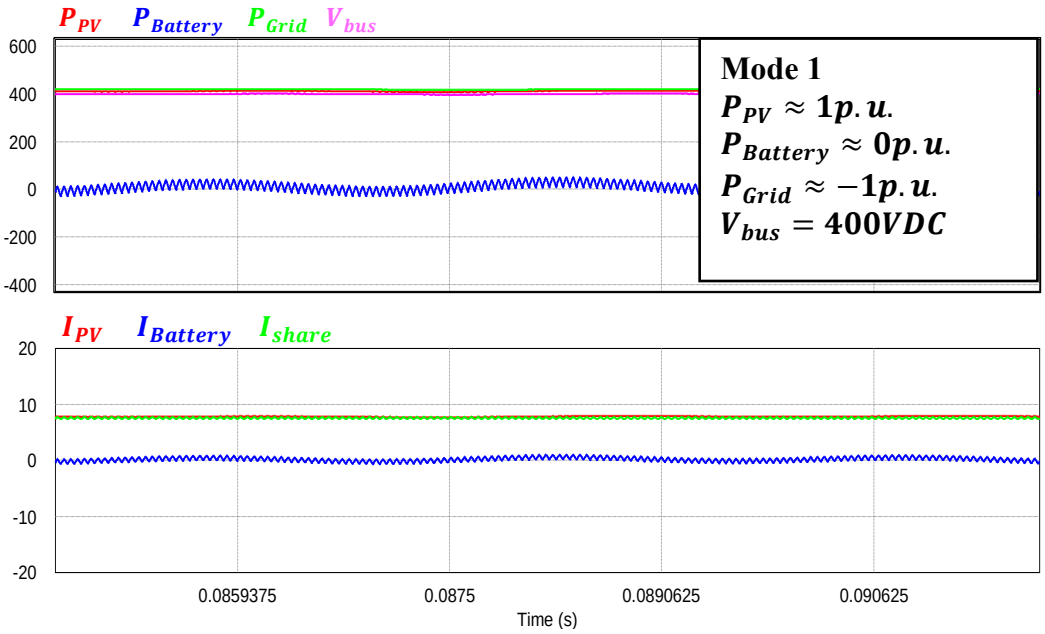

Figure 39 Simulation results of the SSTL microinverter with BSS for Mode 1. Note that the PV fully supplies 420W (1pu) of power.

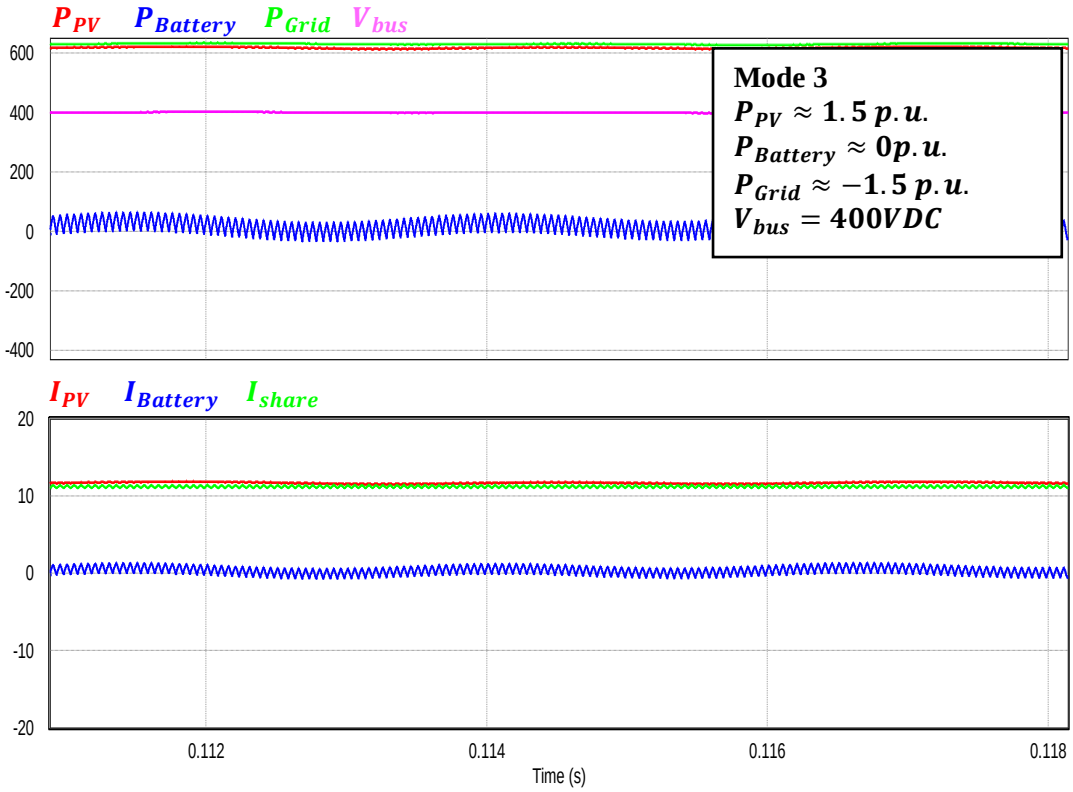

Figure 40 Simulation results of the SSTL microinverter with BSS for Mode 3. In Mode 3, the excess power is sent to the grid.

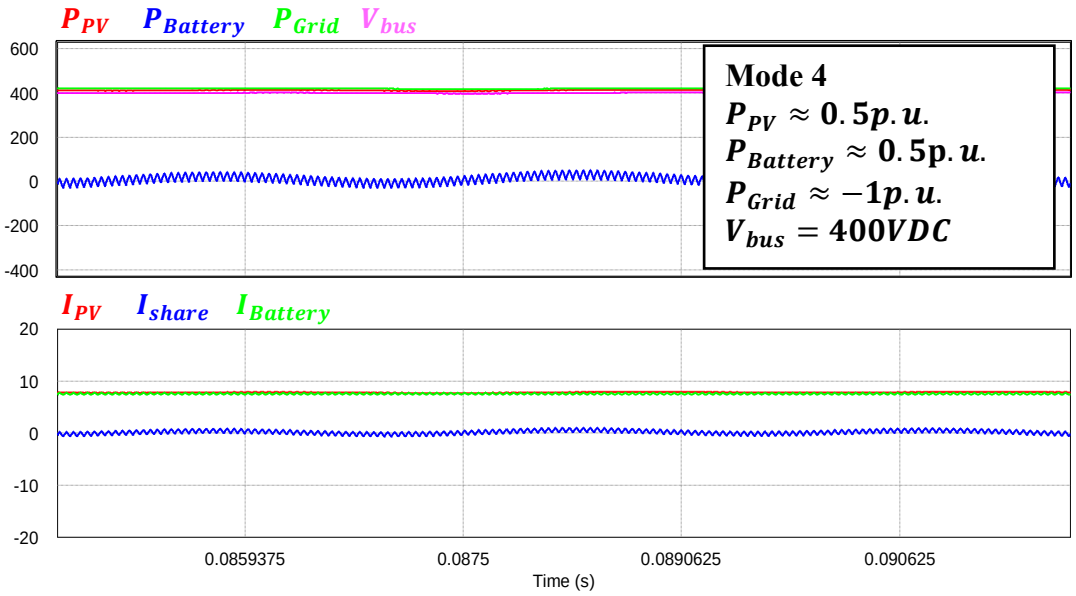

Figure 41 Simulation results of the SSTL microinverter with BSS for Mode 4. In Mode 4, both the PV and battery equally supply 210W (0.5pu) power to the grid, due to cloudy conditions.

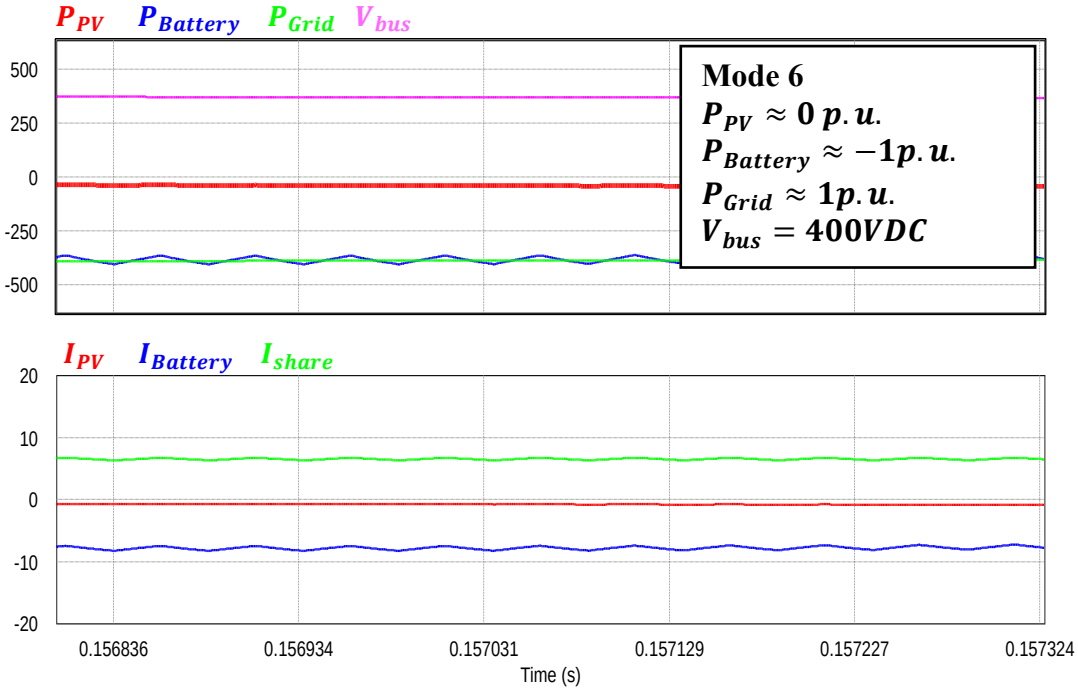

Figure 42 Mode 6, where grid power is charging the battery at night.

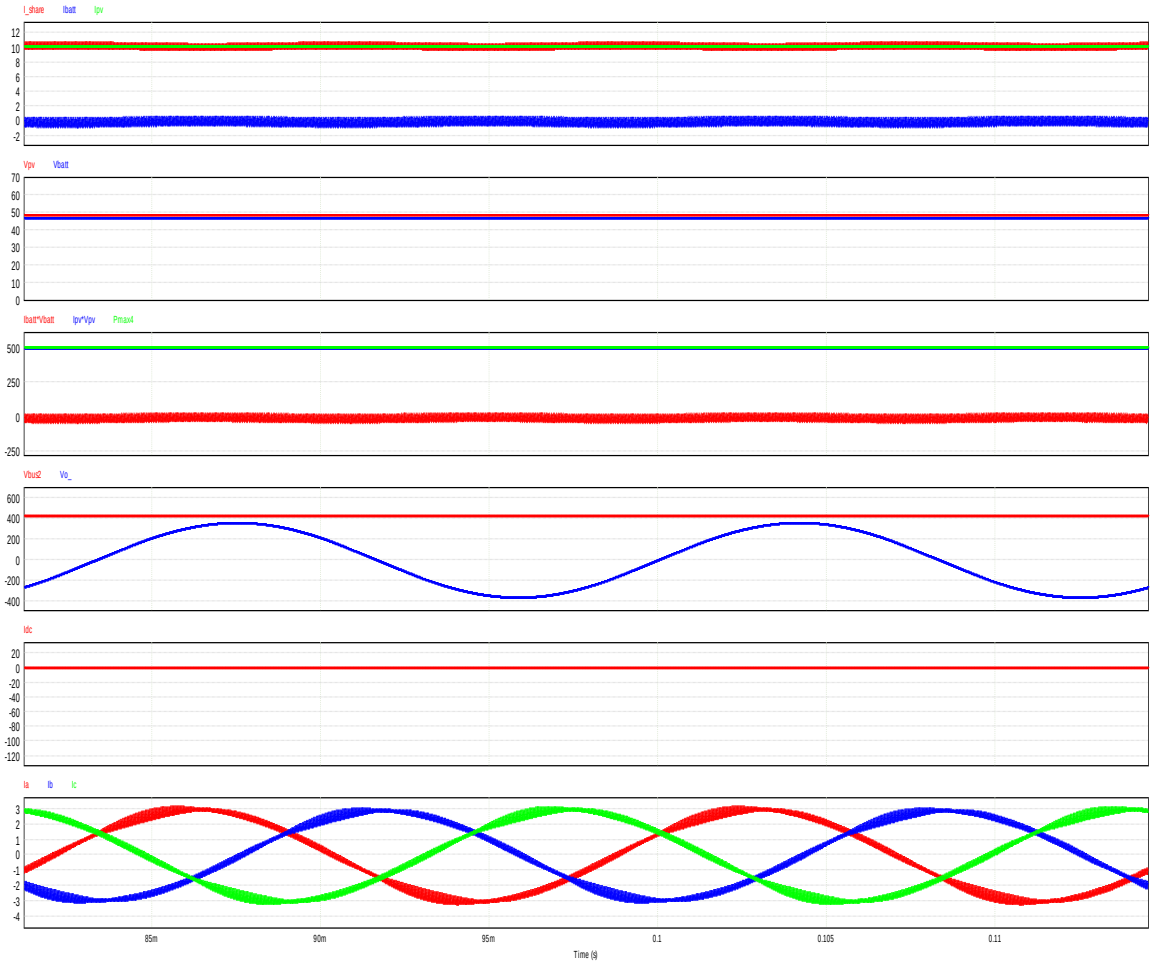

Figure 43 Simulation results for PV insolation of 1200 W/m2 conditions that complies with Mode 1 operation.

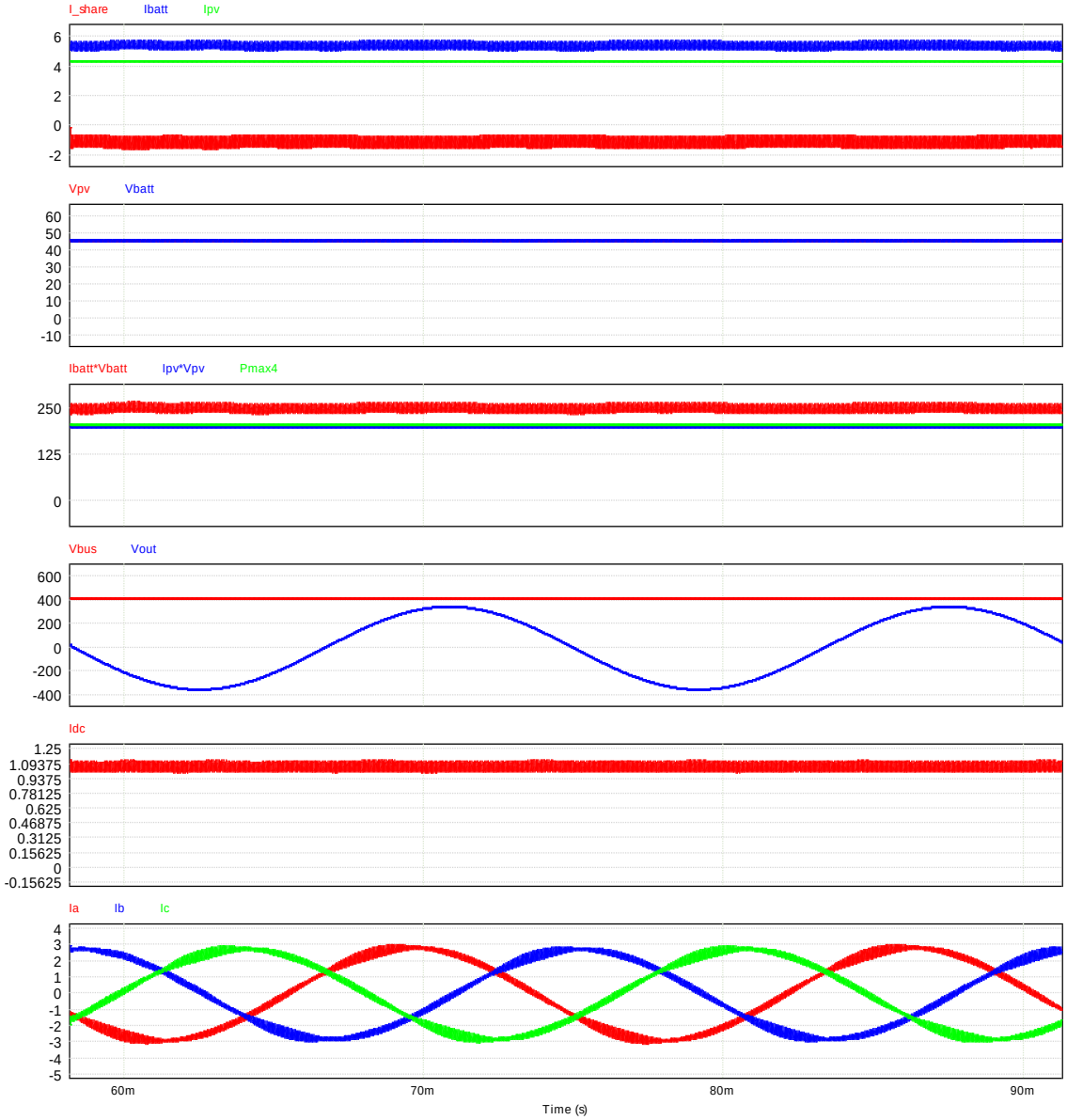

Figure 44 500 W/m2 insolation condition, which matches Mode 5.

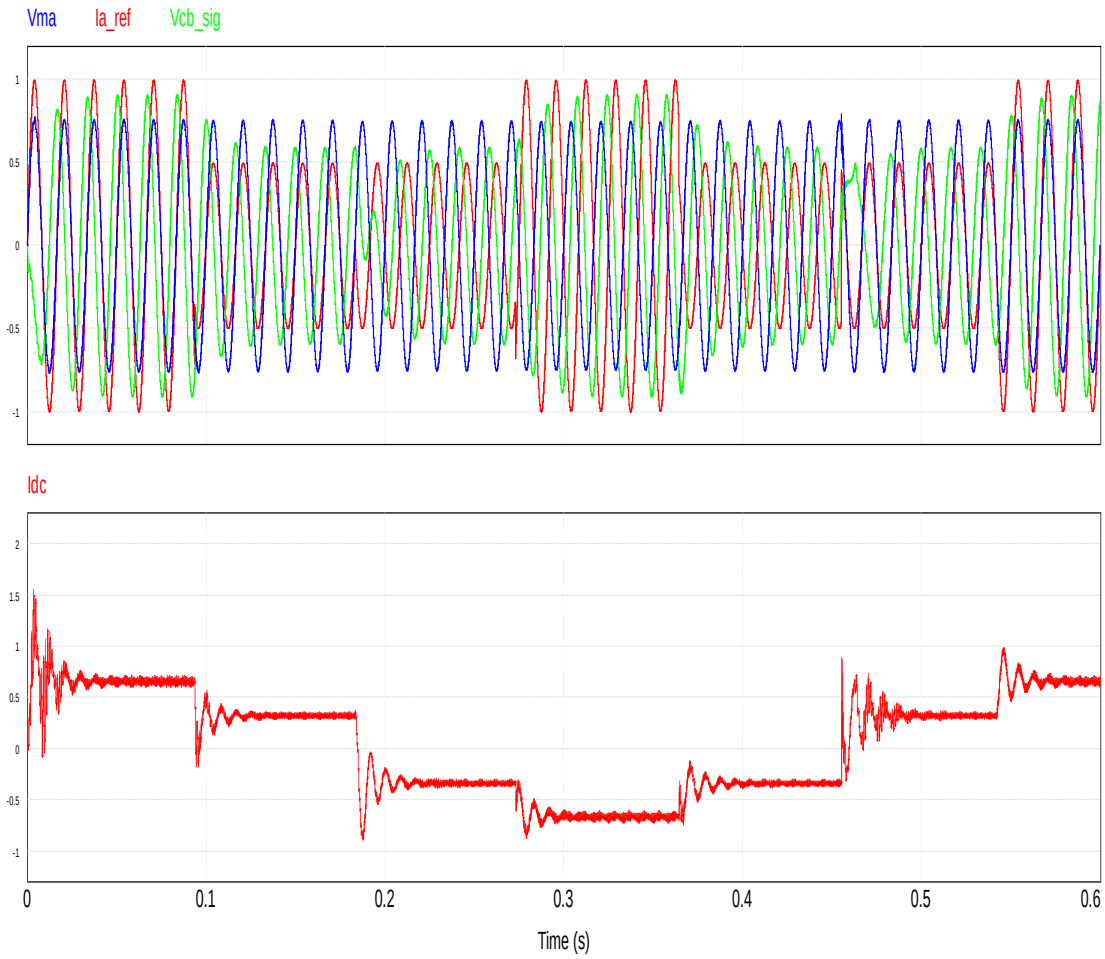

Figure 45 On-grid operation of the input-filtered DC current simulation. The bidirectional power flow operation was verified.

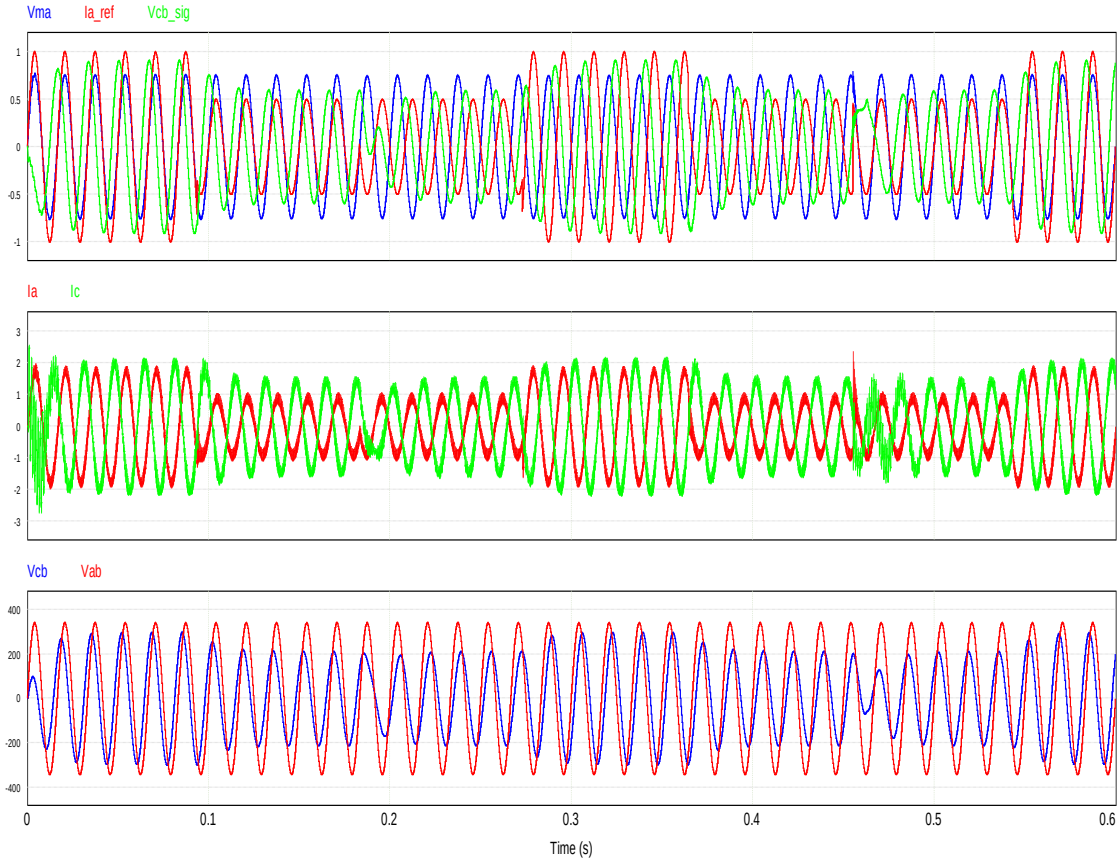

Figure 46 On-grid operation AC load current I_a and active decouple current I_c under various loading conditions.

4.5 Comparison of APD to PPD under various loading conditions

In this section, a graphical comparison between the APD and PPD used as inverter units in the SSTL microinverter is described. The DC link current I_{dc} was simulated for five different cases with a similar RMS load current I_a. Case 1 illustrates an inverter with no power decoupling (PD) stage for the resistive load, where the I_{dc} ripple is relatively high, as shown by the blue line in Figure 47. Case 2 depicts an inverter with a PPD stage for the resistive load. This case employed a bulky/lossy electrolytic DC link. However, it effectively processed the second-order ripple, as shown by the green line in Figure 47. Case 3 shows an inverter with an APD, which is an integral part of the proposed SSTL microinverter when accommodating a resistive load. It was confirmed that the APD matched the performance of the PPD in processing a second power ripple. Case 4 displays an inverter with no PD for the nonlinear diode rectifier load, as shown in Figure 48. This is was a worst-case scenario, where the I_{dc_rms} peaked. Case 5 shows an inverter with an APD that supplies a diode rectifier load identical to that in Case 4 (see Figure 48). The figure of merit is defined as γ, which expresses the ratio of the RMS to the average DC link current for the six cases:

$$\gamma = \frac{I_{dc_{rms}}}{I_{dc_{avg}}} \tag{49}$$

Therefore, Figure 49 was plotted to graphically demonstrate that the APD effectively matched the performance of the PPD when $\gamma \approx 1$. In addition, the APD showed an enhanced level of performance under a nonlinear load. Thus, γ was reduced by factor of 0.2 as compared to no PD.

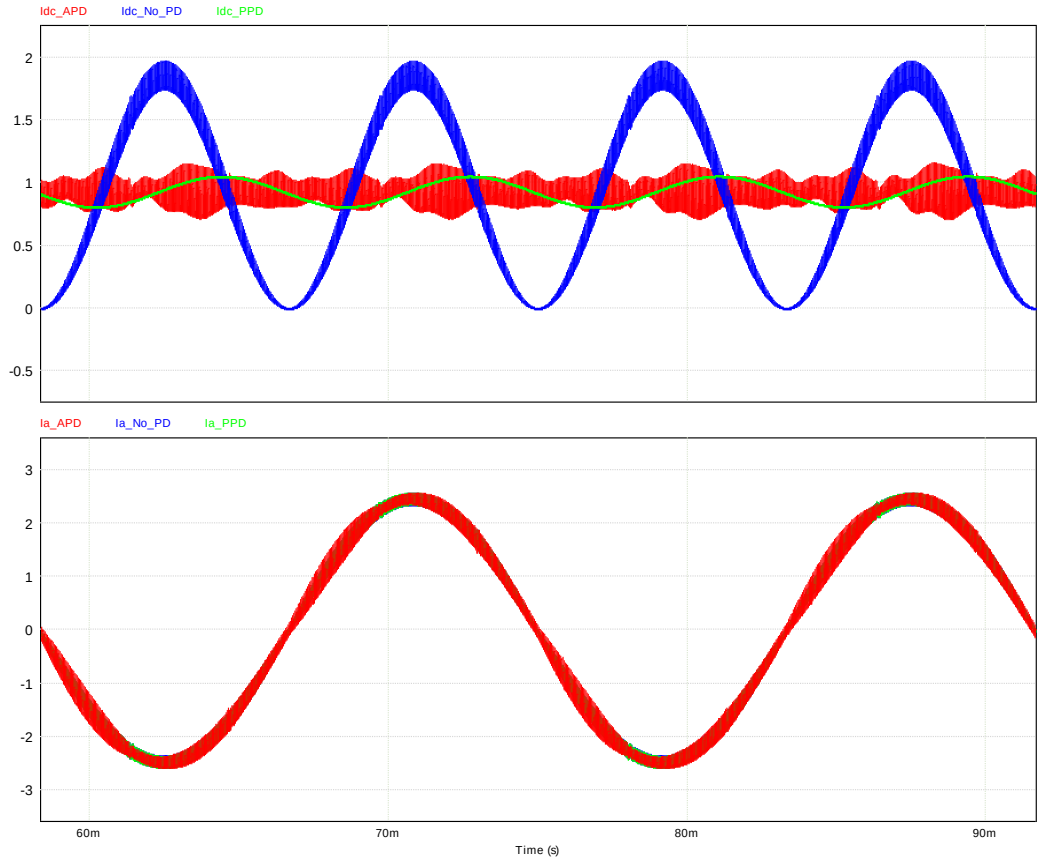

Figure 47 Comparison of the PPD and APD for a resistive load (100% loading).

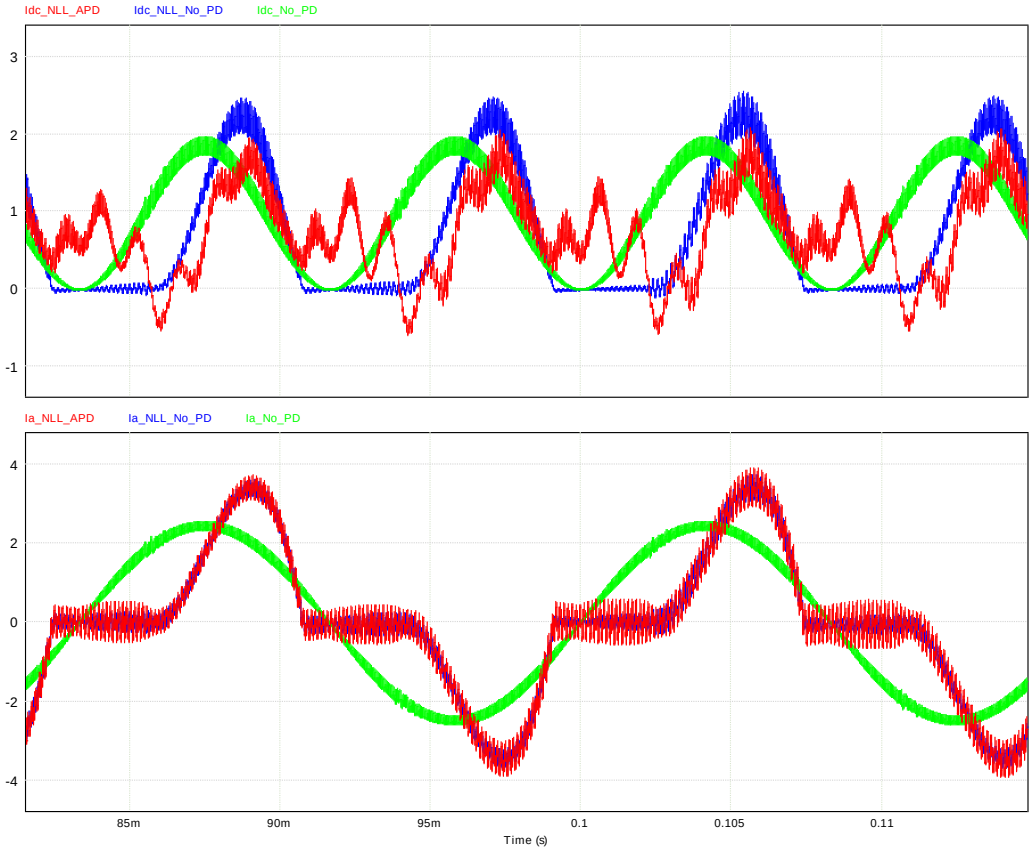

Figure 48 Comparison of the PPD and APD for a nonlinear load.

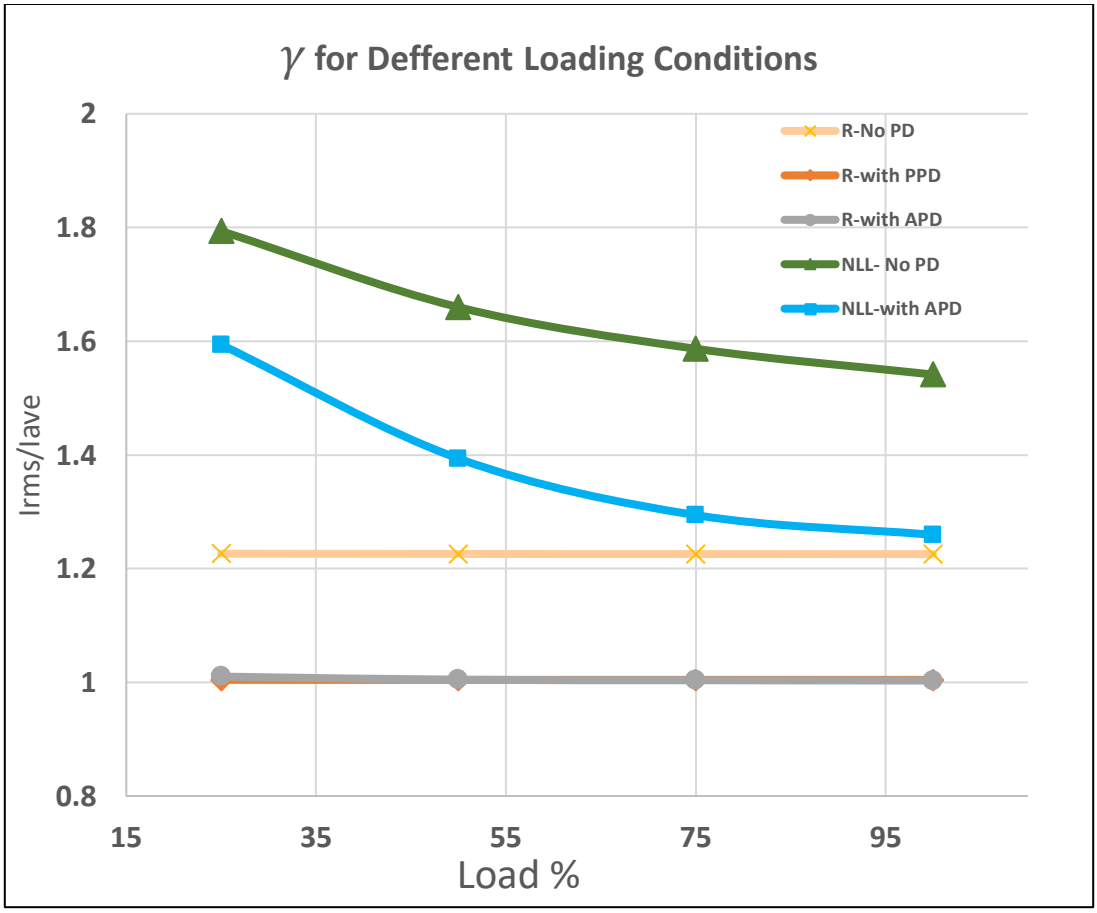

Figure 49 Comparison of the PPD and APD for linear and nonlinear loading conditions.

4.6 Experimental results

4.6.1 Preliminary experimental results

This section discusses the preliminary experimental results from a scaled-down laboratory prototype employing GaN switches. The experimental setup included the power sharing and IMMC stages shown in Figure 33. The inverter stage was simplified to a resistive load in which the grid was assumed to absorb power. The input voltages V_{PV} and V_{batt} were assumed to be ideal DC voltage supplies. A TIF28335 DSP designed by Texas Instruments in Dallas, TX, USA was employed as the PWM controller. The switching devices selected for this experiment were LMG3410-HB-EVM GaN. A power rating of 50W is chosen, as in the preliminary testing. Figures 50 and 51 show the experimental waveforms for the power sharing stage and DC-DC IMMC (SM1 through SM7), assuming Mode 4 operation. In this experiment, parallel modules were not implemented. Thus, SM2 and SM5 in Figure 33 were ignored. Figure 50(a) shows the high gain DC output V_{BUS} of 188V. By selecting a duty cycle of 0.5 for all submodules, the input voltage of 32V was boosted six times (188V). Figures 50(b) and 9(c) show the two DC currents supplied (I_{PV} and I_{batt} shown in Figure 33). It was verified that the power sharing unit (SM7) was controlled to absorb equal power from the DC sources. Figure 50(d) shows the shared current I_{share}. The I_{share} zero average value matches with those of Figure 34 and Table 5. Figures 51(a) through 51(c) show the current waveforms in the inductors (L_1, L_2, and L_7, respectively).

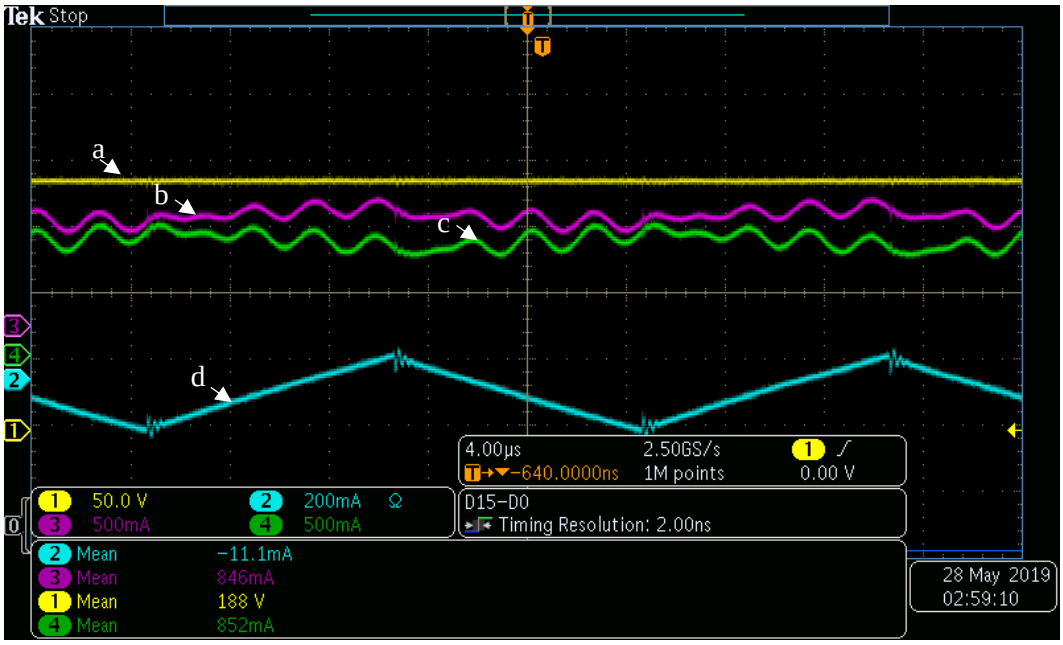

Figure 50 Preliminary experimental results for the proposed SSTL microinverter operating at a reduced voltage: (a) V_{BUS}, (b) I_{pv}, (c) I_{batt}, and (d) I_{Share}.

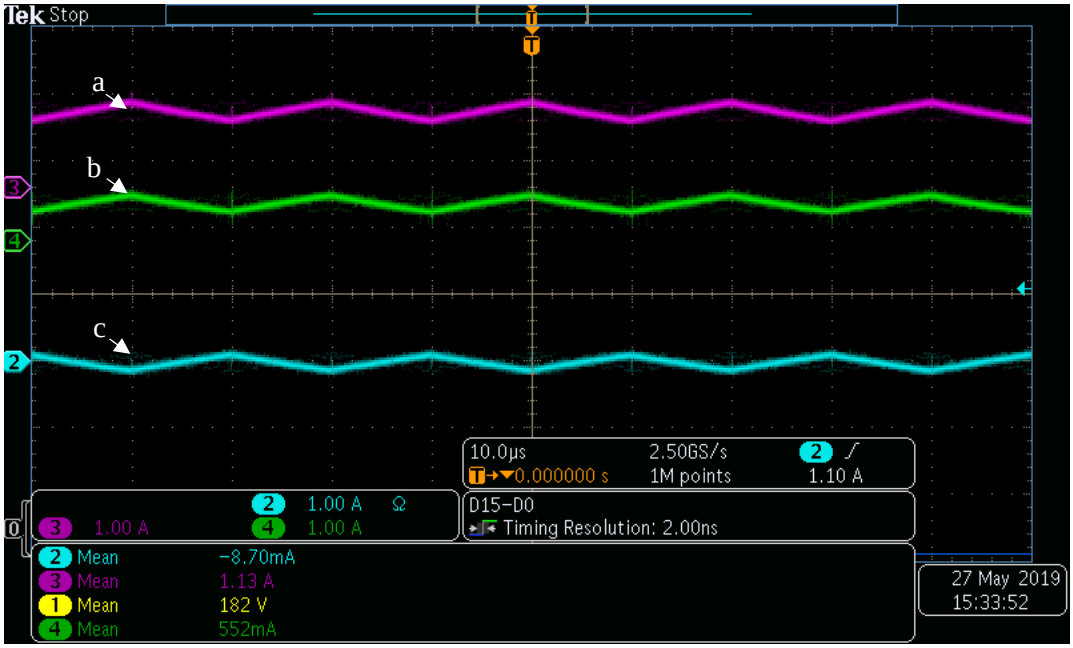

Figure 51 Experimental results of the proposed SSTL microinverter operating at a reduced voltage: (a) I_{L1}, (b) I_{L2}, and (c) I_{Share}.

4.6.2 Prototyping

After performing the preliminary setup discussed in Section 4.5.1, a fully rated 420W setup was prototyped as proof of concept for the SSTL microinverter. A PCB board was designed in Altium, as shown in Figures 52 to 55. Figure 52 illustrates the schematic screen of the SSTL microinverter. Figure 53 shows an actual PCB size print out to confirms the layout for SSTL microinverter elements. Figure 54 shows the two-layer layout of the PCB board. Figure 55 expresses a 3D view of the resulting board, which is ready for manufacturing. Figure 56 shows the final assembled SSTL microinverter after soldering all of the circuit components.

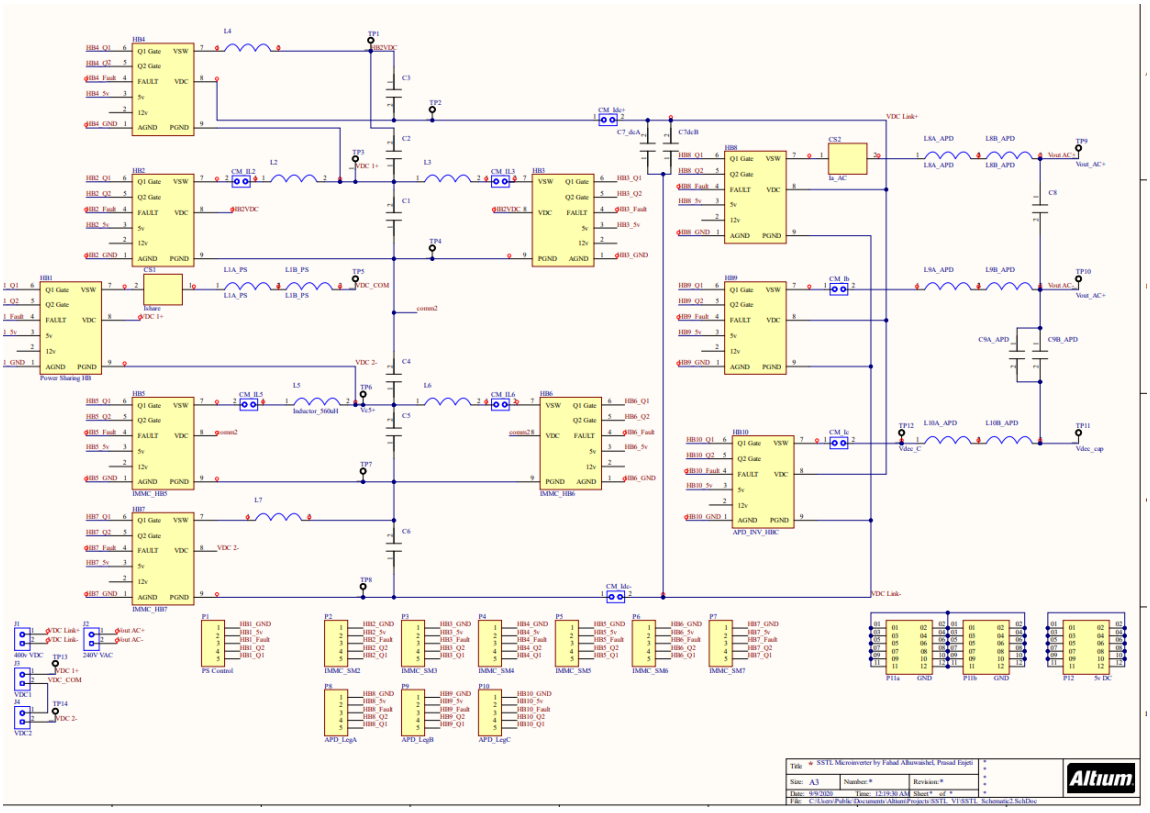

Figure 52 Altium schematic design for the SSTL microinverter prototype.

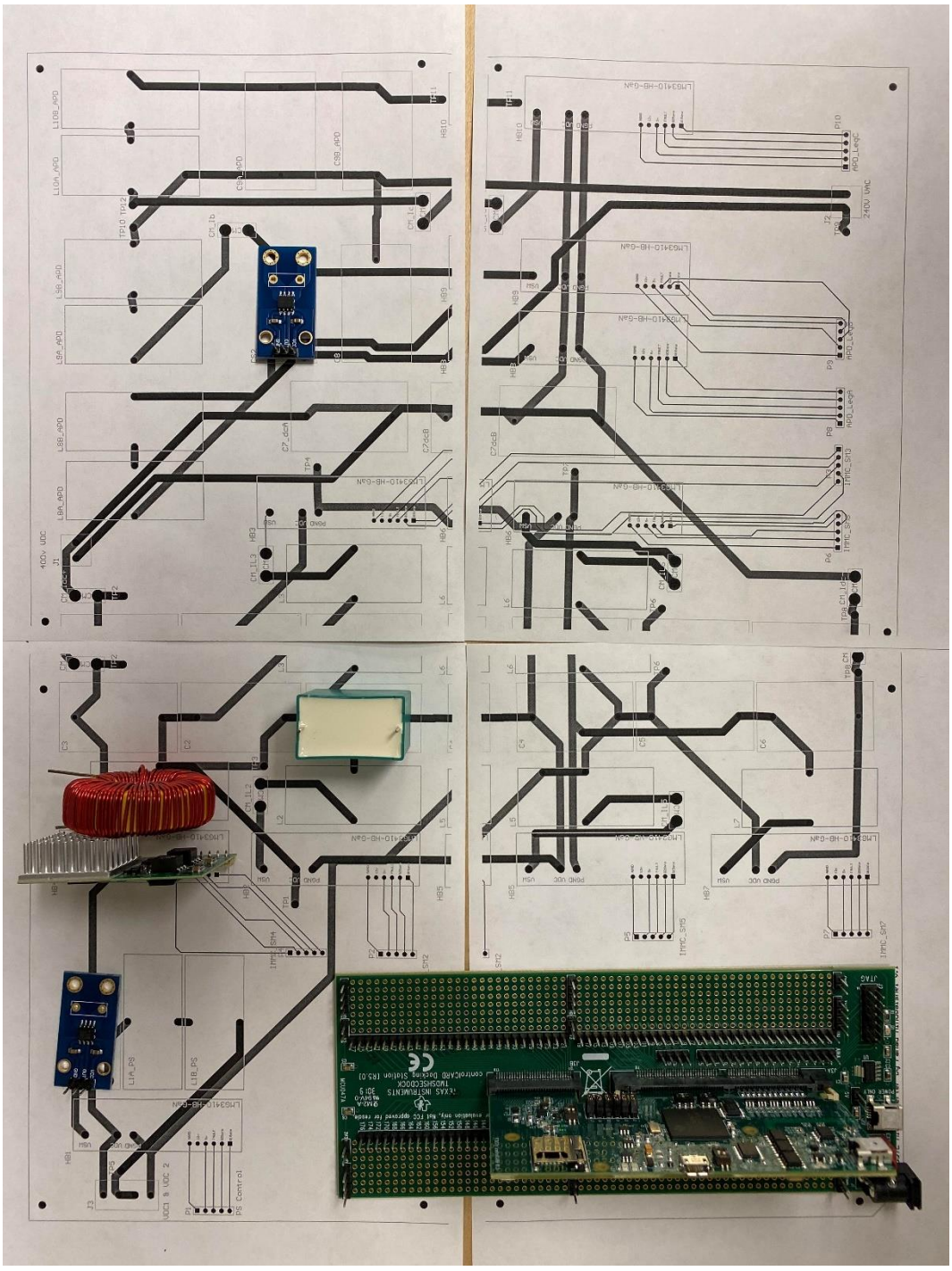

Figure 53 Shows an actual PCB size print out to confirms the layout for SSTL microinverter elements.

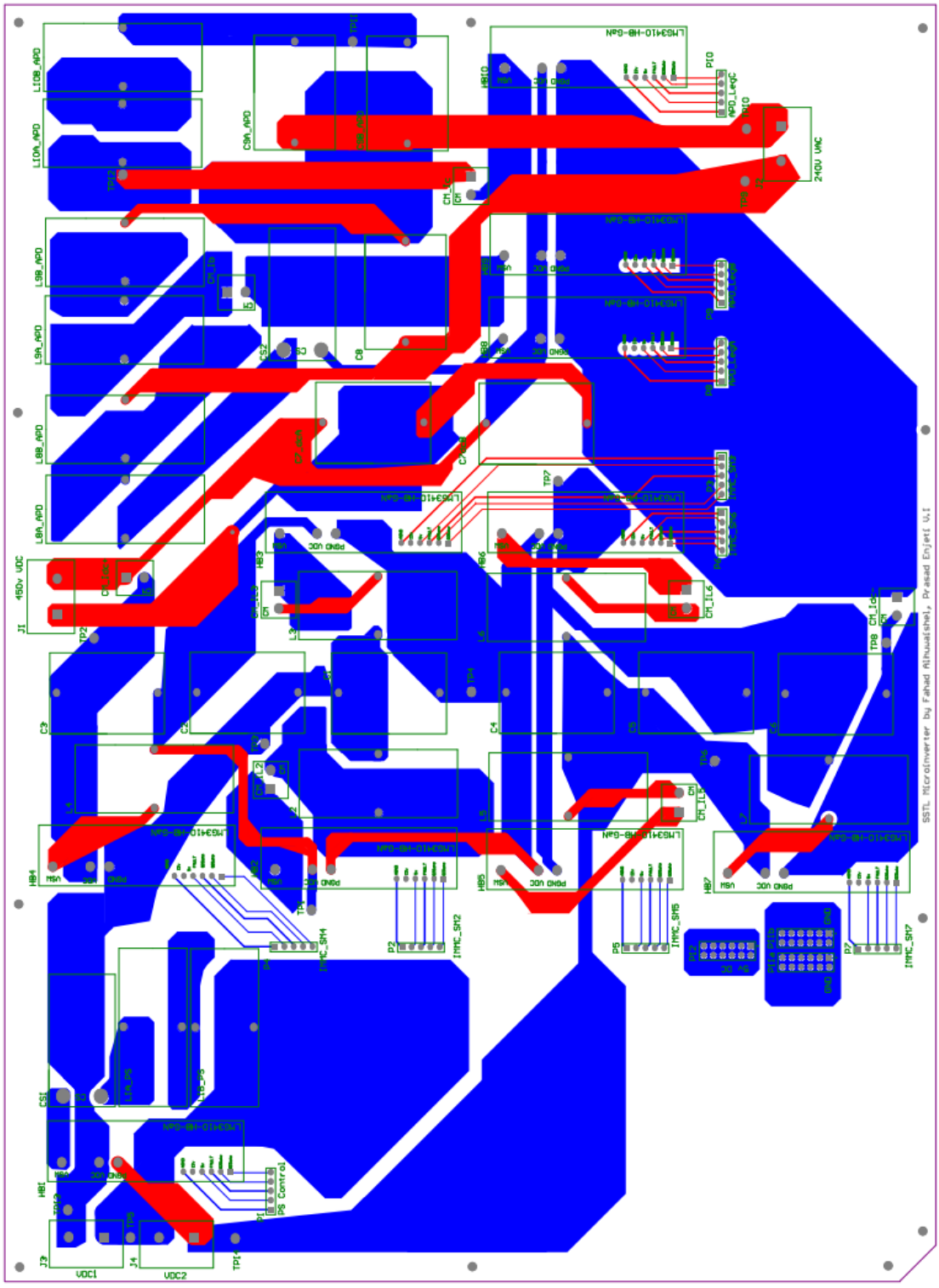

Figure 54 PCB design for the top (in red) and bottom (in blue) layers of the SSTL microinverter prototype.

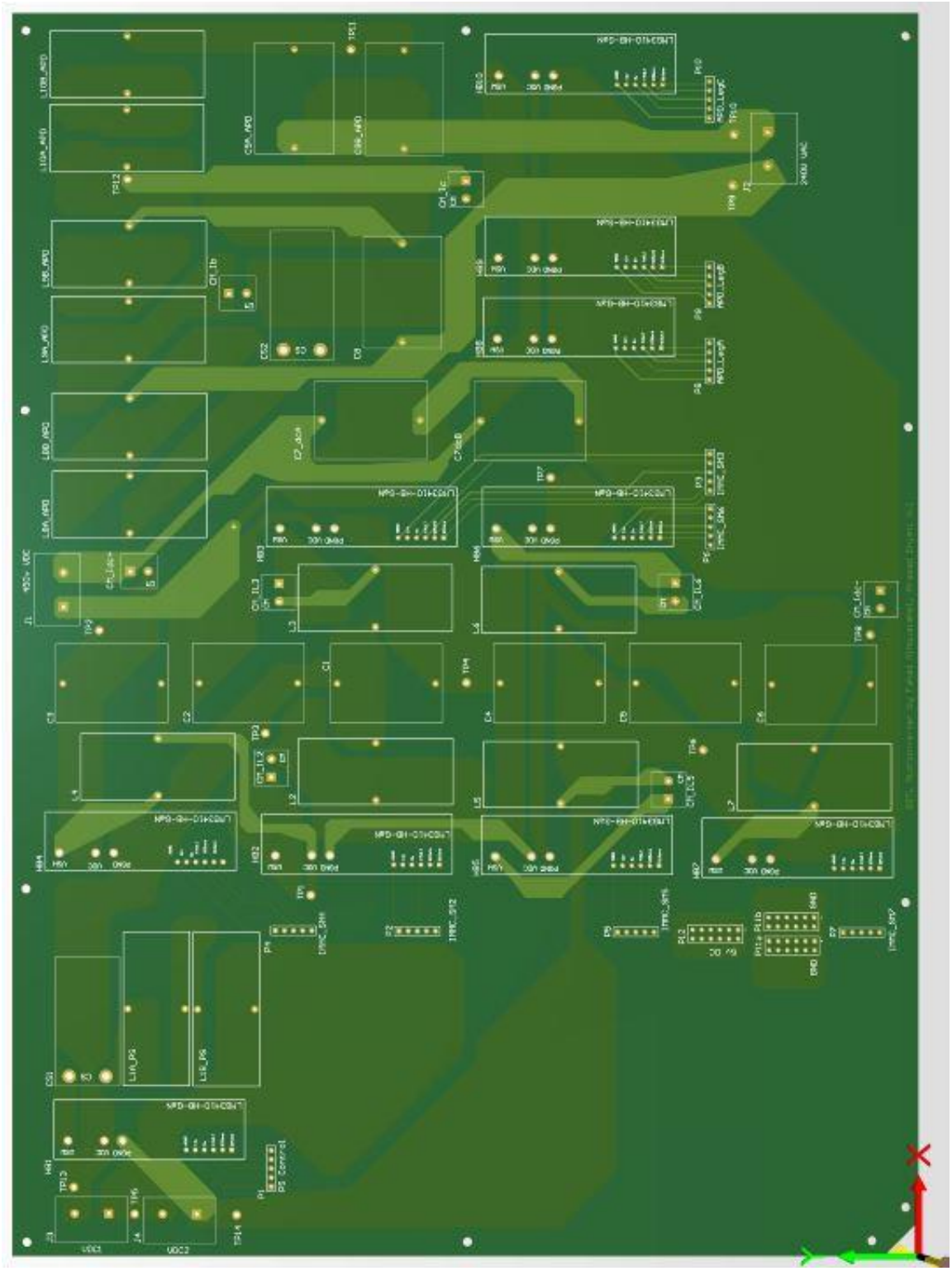

Figure 55 3D view of the PCB board of the SSTL microinverter prototype.

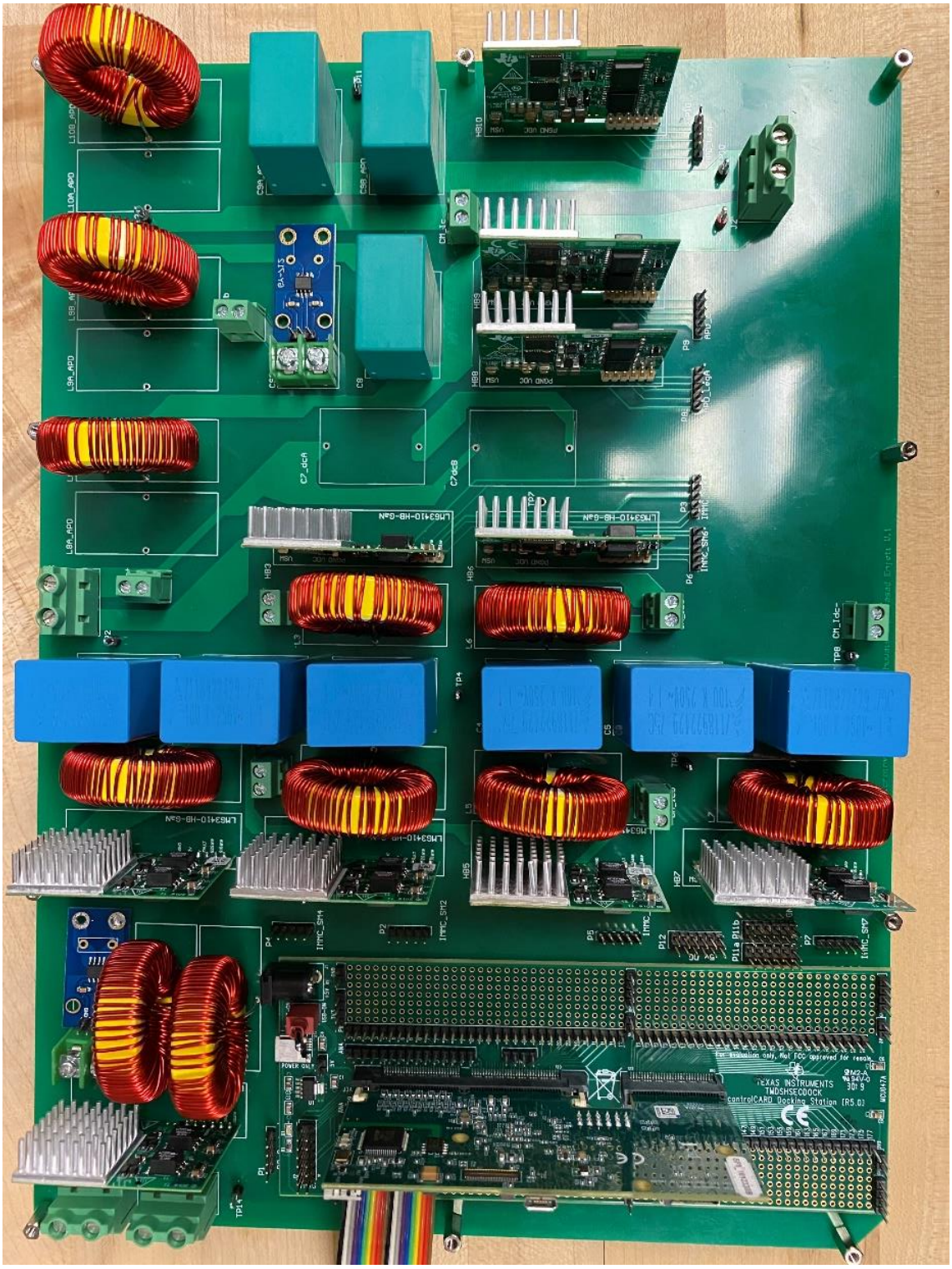

Figure 56 SSTL microinverter prototype after assembly.

4.6.3 Final experimental results

Results were obtained based on the SSTL microinverter design parameters shown in Tables 6 through 8. The PV panel and battery were assumed to be two DC power supplies of 70V and 30V ratings. The voltages were selected to be unequal to illustrate the ability of the SSTL microinverter to operate under different PV and battery voltage selections. This SSTL microinverter ability is illustrated in Equations 32 and 33. A TIF28379D DSP designed by Texas Instruments in Dallas, TX, USA was employed as the PWM controller. The switching devices selected for this experiment were LMG3410-HB-EVM GaN. A power rating of 340W was chosen for the test results. Figures 57 through 59 show the experimental waveforms for the power sharing stage and DC-DC IMMC (SM1 through SM7), assuming Mode 4 operation. Figure 57 shows the targeted high gain DC output V_{BUS} of 400V resulting from unequal input voltages: V_{PV} of 70V and V_{Batt} of 30V. By selecting a duty cycle of 0.6 for SM1, SM2, SM4, and SM5 and a duty cycle of 50% for SM3 and SM6, the input voltages of 70V and 30V were boosted to 400V.

Figure 58 shows the two DC currents supplied (I_{PV} and I_{batt} shown in Figure 33). It was verified that the power sharing unit (SM7) was controlled to absorb the desired power from the DC sources. Figure 58 shows the shared current I_{share} ; the I_{share} zero average value matches with those of Figure 34 and Table 5. In this case the absorbed power from DC supply #1 (assumed to be a PV) and DC supply #2 (assumed to be a battery) one is 70% and 30% of 340W load power respectively. Figure 58 shows the current waveforms in the inductors (L_1 and L_2). Figure 59 illustrates the SSTL microinverter AC voltage output and inductor current I_{PV} of THD < 5%. The RMS value of the voltage was within the 240/120 output voltage range of operation. The overall efficiency of tested SSTL microinverter prototype is $\approx 92\%$. The efficiency can be further improved using lower voltage/current rating half bridge submodules specified in Table 7 along with ZVS operation.

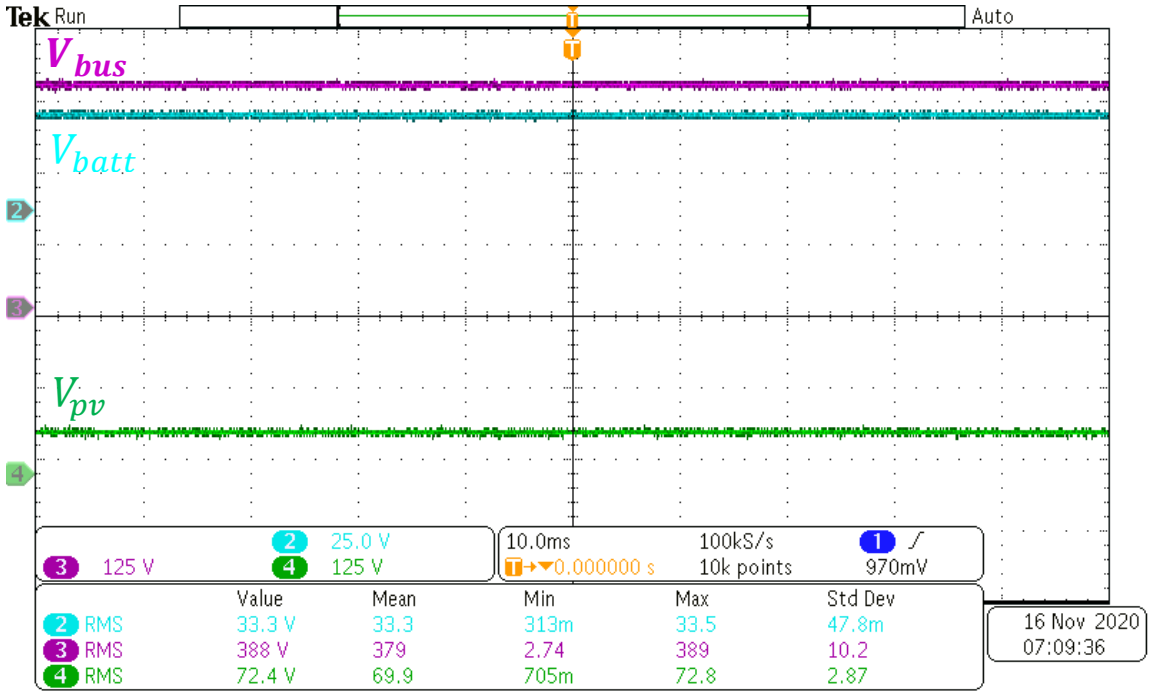

Figure 57 V_{pv} and V_{batt} with having voltages of 72.4V and 33.33V, respectively. It was confirmed that the V_{bus} of 400V was achieved with a low voltage ripple, despite the unequal of input voltage ratings.

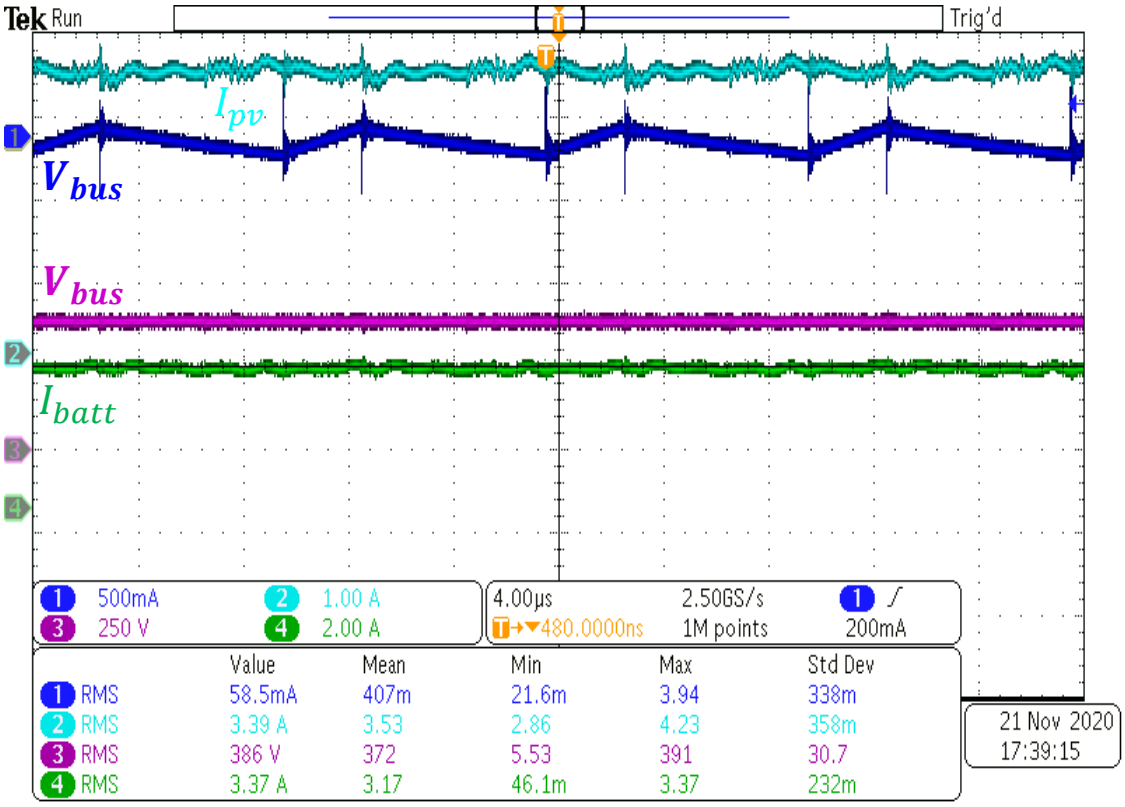

Figure 58 Hardware results for the SSTL microinverter.

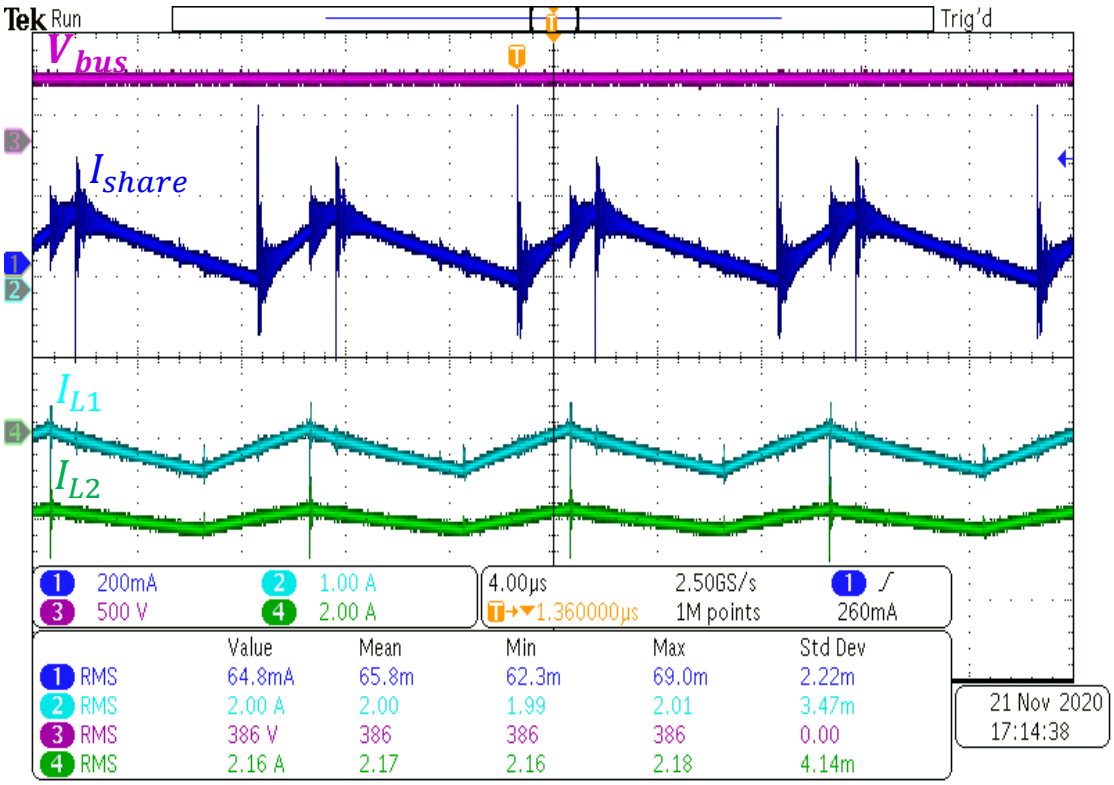

Figure 59 Hardware results showing the high-quality DC output of 386V from the 70V and 30V input voltages.

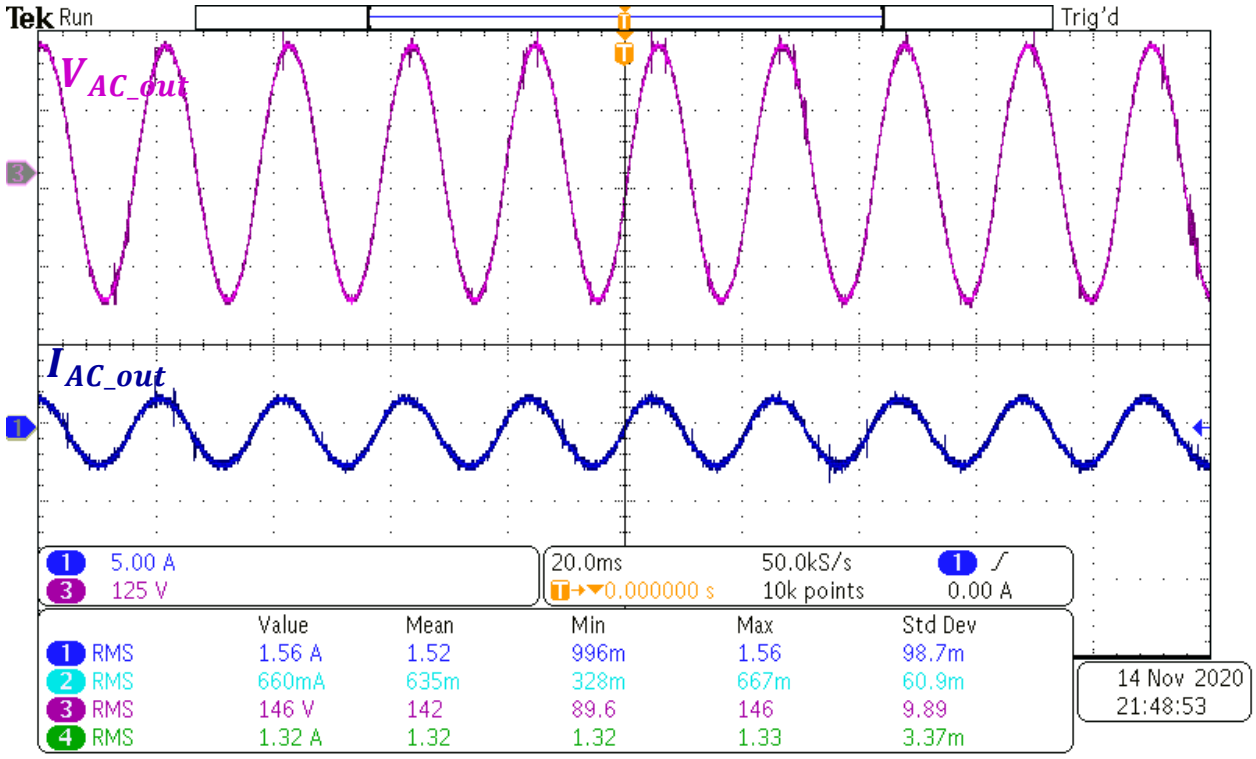

Figure 60 SSTL microinverter output AC voltage and output current I_a of THD < 5%.

5. TRANSFORMERLESS HYBRID PV INVERTER WITH INTEGRATED BATTERY ENERGY STORAGE[3]

5.1 Introduction

Hybrid PV battery systems are decentralized, smart, clean electricity systems that generate and store energy close to the point of consumption [7]. They offer an adaptive solution for utilities seeking to meet their power requirements [7]. Hybrid PV systems solve the intermittent nature of solar PV power and offer a reliable option when connected to a microgrid [77]. However, hybrid PV battery systems require at least one MPPT controller for PV and one SoC controller for the battery. Several MPPT techniques were reported in the literature to facilitate maximum power harvesting in different environmental conditions (see Figures 61(a) to 60(c)) [78-80]. Some MPPT techniques use either one current or one voltage sensor, while others use both voltage and current sensors. However, most MPPT techniques require both voltage and current sensors, due to their high MPP accuracy (e.g., the hill-climbing method).

Power management systems incorporate SoC controllers to prevent batteries from overcharging or undercharging. In particular, overcharging/undercharging new Li-ion BSSs can result in either damage to the battery or a reduction of battery life, and can even cause severe fire hazards leading to explosions [81]. Thus, a separate DC-DC converter

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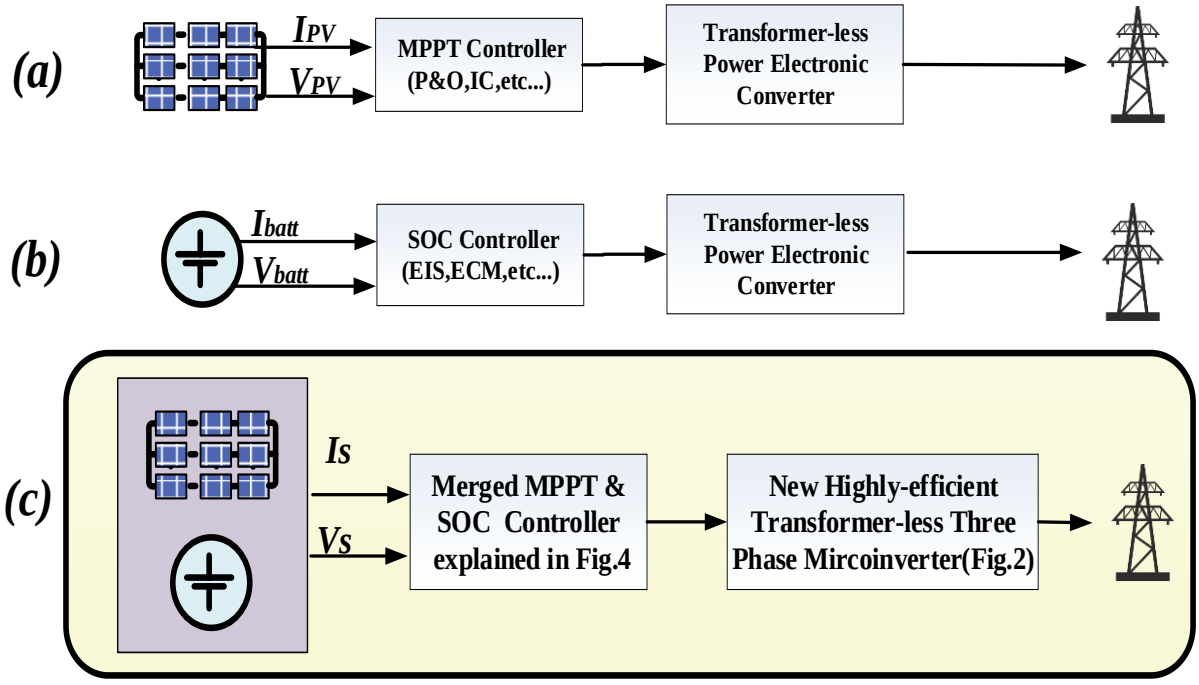

Figure 61 Evolution of the PV/battery system: (a) typical transformerless PV farm electrical system, (b) typical battery energy storage system when interfaced with the grid, and (c) proposed transformerless hybrid PV inverter with integrated energy storage.

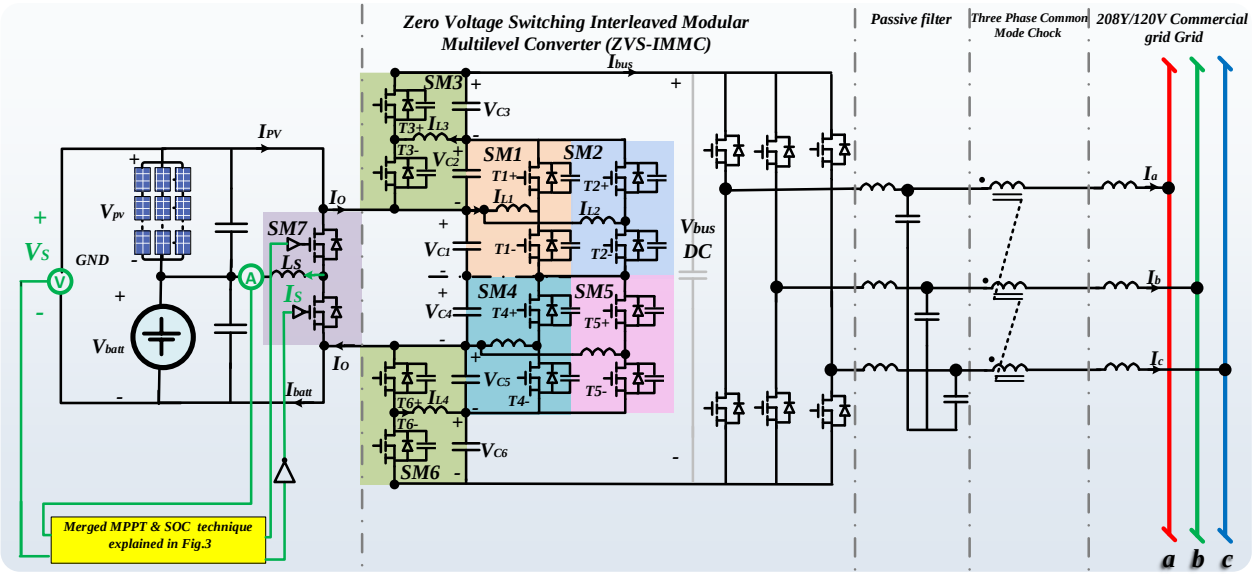

Figure 62 Proposed transformerless hybrid PV inverter with integrated battery energy storage.

with an independent SoC controller is required. The coulomb count (CC) estimation is the simplest SoC measurement method and involves only one current sensor. The CC method requires knowledge of the initial SoC and suffers from accumulative SoC estimation errors. Alternatively, open circuit voltage (OCV) needs one voltage sensor to manage SoC. In OCV, the battery requires a long resting time to achieve balance and obtain accurate OCV measurements [82, 83]. Consequently, several combined voltage/current sensing techniques have been explored to more accurately estimate SoC. These techniques add to the SoC controller's complexity and cost [81-83].

Attempts have been made to merge MPPT and SoC control for PV farms with integrated BSS to utilities [84-86]. These topologies involve a higher number of sensors, along with a large DC link buffer to handle the voltage ripple caused by the DC-DC converter stage. Moreover, the power converter design requires a transformer stage to match the inverter voltage with the grid voltage.

Furthermore, the DC-DC converter was designed to tolerate the full processed power. In addition, the DC-DC stage operates under a higher duty cycle range via a hard switching lossy operation. As a result, additional power losses occur, as in [84, 85], eventually constraining the power converter's scalability.

APsystems has introduced a three-phase microinverter [87], demonstrating the growing interest in three-phase microinverters for commercial grids and utility service applications. A three-phase microinverter is capable of processing a higher amount of power with a reduced footprint, due to the elimination of the bulky DC link buffer, along with other inherited advantages related to the three-phase design. The YC1000-3-208

microinverter [87] can accommodate up to four panels, resulting in a reduction in system complexity and installation time. However, three-phase microinverters have not been exploited for hybrid PV/battery systems interfaced with transformerless power conversion stages.

In view of this, a transformerless hybrid PV inverter with integrated battery storage is proposed in this research. The proposed converter is interfaced with a PV/battery system and commercial three-phase grid (see Figure 62). The DC-DC converter joins the operation of both the MPPT and SoC estimation in a single-stage half-bridge submodule (SM7). SM7 is followed by the IMMC operating in ZVS. The ZVS-IMMC can achieve a high-gain DC output with a high level of efficiency. The proposed power electronic converter facilitates a transformerless and compact commercial grid interface. The proposed inverter offers the following advantages:

- Combining MPPT and SoC functions into one stage.
- Reducing the number of PV/battery sensors.
- Eliminating the bulky DC link to interface the DC-DC converter with the three-phase inverter, replacing it with mini distributed DC link capacitors.
- Offering a transformerless power conversion stage with highly efficient operation.
- The DC-DC converter unit operates via a highly efficient ZVS technique.
- Full utilization of battery storage.
- Longer battery lifetime.
- Scalable modular topology.

5.2 Analysis of the proposed converter

Figure 62 shows the various states of the proposed converter. The solar PV and battery are connected in series and a half-bridge module SM7, along with inductance L_s, forms the power sharing stage. The power sharing stage incorporates a joint operation of MPPT and SoC in a single unit. Moreover, it has the advantage of a reduced number of required sensors; only a single voltage and single current sensor are needed. The power sharing controller is detailed in Section 5.3.

The power sharing stage is followed by the ZVS-IMMC stage, which boosts the PV/battery voltage to enable transformerless operation with efficient soft switching. This stage has the advantage of voltage ripple cancelation and distributed DC link capacitors to enable compact sizing of the passive elements. The ZVS-IMMC operation is detailed in Section 5.4. This stage is followed by the three-phase inverter stage, which converts the boosted DC input into three-phase AC output for utility interfacing. The three-phase inverter is followed by LC filters, which enable high-quality sinusoidal line currents. The filter is followed by a three-phase common mode choke to reduce leakage current. The operation of the inverter stage is detailed in Section 5.5. The design specifications for the proposed transformerless hybrid PV inverter with integrated battery storage (shown in Figure 62) were selected in accordance with the YC1000-3-208 microinverter [87], as will be described in Section 5.6.

5.3 Proposed merged MPPT and SoC controller

The half-bridge module SM7 (see Figure 62) is controlled with a duty cycle, such that simultaneous MPPT and SoC control in the battery is achieved. This is termed merged MPPT-SoC control and is detailed below. A new figure of merit is defined as:

$$P_s = V_s \cdot I_s \tag{50}$$

where V_s and I_s are the sensed voltage and current, respectively, and can be described as:

$$V_s = V_{batt} + V_{pv} \tag{51}$$

$$I_s = I_{pv} - I_{batt} \tag{52}$$

In Figure 62, SM7 is shown to perform both the MPPT and SoC control operations. Thus, V_s is the sum of the PV and battery storage voltages (Equation 50), while I_s is the difference between the PV and battery storage currents (as illustrated in Equations 52). If the available solar power is more than half the nominal power supplied to the grid, I_s must have a positive value. Consequently, I_{pv} will be more than I_{batt} and the PV will supply the majority of the power. In this case, the SM7 controller will track the maximum I_s by controlling the SM7 duty cycle. This operation must be performed without causing a voltage drop across the PV panels, since the rate of change in PV voltage V_{PV} is much faster than the rate of change in battery storage voltage V_{Batt} under different loading conditions. Thus, any rapid voltage drop (or increase) of V_S is mainly caused by V_{PV}. Consequently, tracking the maximum value of P_S (the product of V_S and I_s) matches the MPP. In another scenario, where the available solar power is less than half the nominal power supplied to the grid, I_s must have a negative value. As a result, I_{batt} will be more than I_{pv}. In this case, the battery will supply the majority of the power to the grid.

Similarly, SM7 is controlled to attain the maximum absolute value of P_s without causing a voltage drop in V_S. Given this fact, knowledge of the maximum P_s is sufficient to determine the MPPT for the PV panels. The duty cycle of 50% was selected as an initial condition for the MPPT-SoC controller since that is the midpoint of the controller's operation range. When using a physical PV model and Li-ion battery model in the PSIM, the optimum MPPT-SoC operation falls within a relatively narrow range of a 45% to 60% duty cycle across all insolation conditions. This low duty cycle control range ensures lower conduction losses for switches, along with faster controller response. Figure 63 shows a block diagram of the merged MPPT-SoC operation. The PV MPPT was achieved via perturb, observing the P_s duty cycle curve. If the rate of change of P_s is zero, the MPP is reached.

The SoC range is 40% to 80% to prevent the battery from overcharging or undercharging. In addition, this SoC range of operation prevents the battery from entering the nonlinear exponential operation zone; therefore, the relation between SoC and V_{Batt} can be further linearized. Equation 30 in Section 4 can be used to find I_s. Thus, the relationships among I_s, I_{PV}, and the duty cycle d_7 of SM7 are expressed as:

$$I_s = \frac{I_{PV} - (1 - d_7) I_o}{d_7} - I_o \tag{53}$$

The output current I_o is controlled via the following inverter stage, as shown in Figure 61. In the case of a fixed I_o, incrementing d_7 to a pre-known value of $d_7 + \Delta d_7$ in Equation 49 yields Equation 50, as follows:

$$I_s = \frac{I_{PV} - (1 - d_7 + \Delta d_7) I_o}{d_7 + \Delta d_7} - I_o \tag{54}$$

Similarly, Equation 31 in Section 4 can be used to find the relationships among I_s, I_{PV}, and the duty cycle d_7 of SM7:

$$I_s = I_o - \frac{I_{batt} - d_7 I_o}{1 - d_7} \tag{55}$$

Therefore, incrementing d_7 to a pre-known value of $d_7 + \Delta d_7$ in Equation 55 yields Equation 56, as follows:

$$I_s = I_o - \frac{I_{batt} - (d_7 + \Delta d_7) I_o}{1 - d_7 + \Delta d_7} \tag{56}$$

I_{batt} and I_{PV} can be found via Equations 53 to 56. Given I_{batt}, the SoC can be found using the CC method, as in [80, 83]:

$$SoC(t) = SoC(t_0) + \frac{1}{C_n} \int_{t_0}^{t+t_0} I_{batt}\,(d\tau) x\ 100\% \tag{57}$$

$SoC(t_0)$ and c_n are denoted as the initial SoC and nominal capacity, in that order. The CC method requires recalibration of $SoC(t_0)$ to reduce the accumulated error. Solar irradiance has a minor effect on voltage at the MPP V_{MPP} value. Conversely, the battery voltage V_{Batt} has a relatively slow voltage rate of change when controlled to operate close to the linear SoC range (i.e., 40% to 80%). Thus, when the measured V_S is more than 2.06 *V_{MPP}, the $SoC(t_0)$ is set to 80%. Similarly, the $SoC(t_0)$ is set to 40% if V_S is lower than 0.94 V_{Batt}. The aforementioned 2.06*V_{Batt} and 0.94 factors are assumed to be typical daytime power production. These factors depend on the type and size of the battery storage. For nighttime operation, the V_S is directly equal to V_{Batt}. At this point, the SoC can be estimated using the OCV estimation method [82, 83]. In addition, a V_{MP} given from the weather forecast can also be added to further maintain the SoC within the 40% to 80% range, as shown in Figure 63.

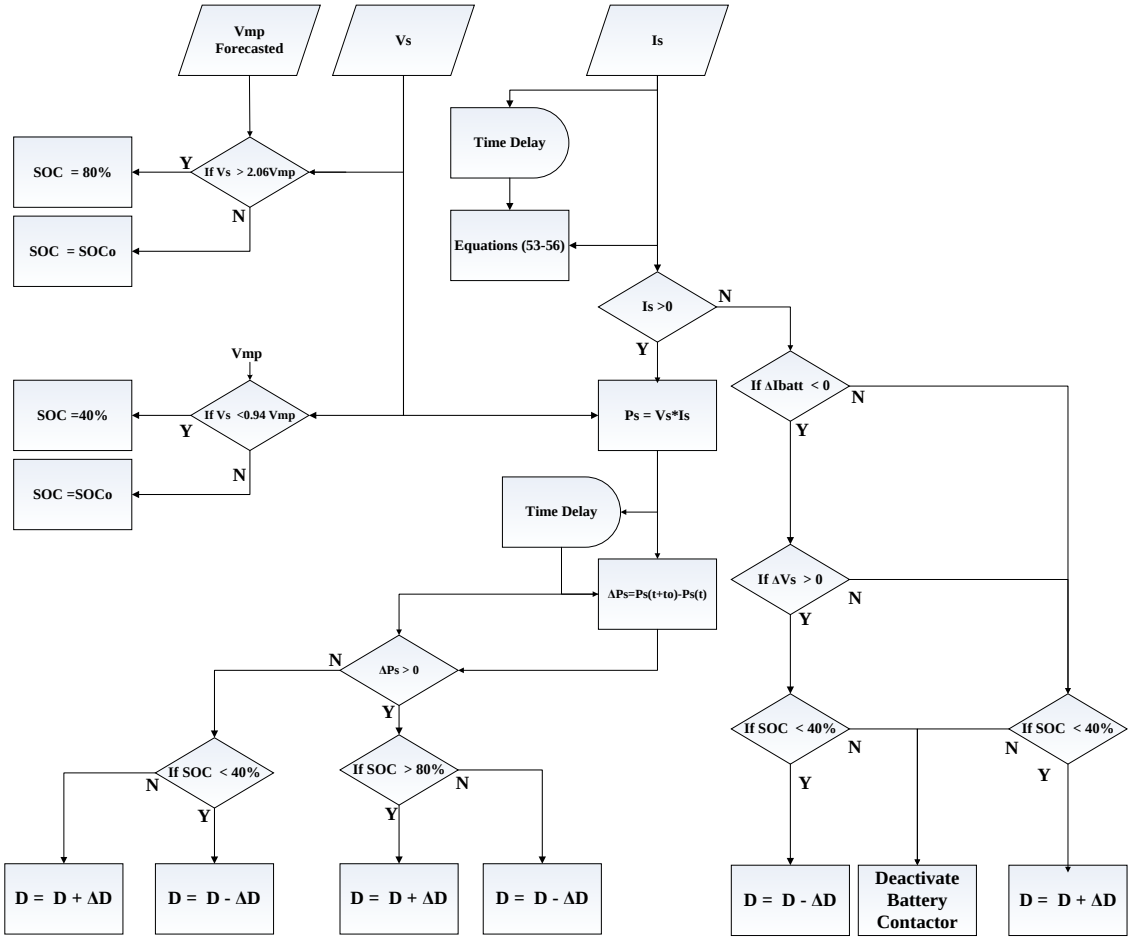

Figure 63 Control block diagram of the proposed converter for MPPT and SoC control.

5.4 Proposed ZVS-IMMC operation

Among the soft switching techniques, zero current switching (ZCS) suffers from turn-on losses caused by the internal capacitance of the switching device. This phenomenon is not presented in ZVS operation. Therefore, ZVS is generally preferred over ZCS, especially for applications with a high switching frequency.

This section discusses ZVS operation of the proposed converter (see Figure 62). Figures 64 and 65 illustrate the operation of the proposed ZVS-IMMC stage that follows the power sharing stage mentioned in the previous section. In the proposed topology, the ZVS-IMMC stage is composed of six submodules (i.e., SM1 to SM6) symmetrically distributed around the horizontal axis (see Figure 6). For simplicity, only the upper submodules (i.e., SM1 to SM3) are considered because the lower submodules (SM4-SM6) have similar operations. SM1 to SM3 have an identical control signal if the desired V_{bus} is triple the input voltage. Thus, SM1 is taken as a building block for the ZVS-IMMC, as shown in Figures 64 and 65.

Control of SM1 is based on the ZVS clamped capacitor technique [88-90]. This technique involves six states of operation, as shown in Figure 64. In State 1, T1- turns on at ZVS due to parallel capacitor C_{T1-} (shown in Figure 64). The voltage across T1- builds up slowly compared to its switching time. Then, T1- conducts positive I_{L1} until the maximum inductor current I_{L1max} is approached. In State 2, T1- is turned off at ZVS. Thus, both the T1- and T1+ switches are off. In this state, the C_{T1+} voltage is rapidly reduced to zero, while C_{T1-} charges rapidly to V_{c1}. In State 3, D1+ conducts and allows I_{L1} to decrease linearly until it reaches zero, which forces D1+ to turn off. In State 4, T1+

turns on and conducts a path for the negative I_{L1} current until it approaches the minimum inductor current I_{L1min}. In State 5, T1+ turns off at ZVS. Then, the C_{T1+} voltage charges rapidly to V_{c1}, while C_{T1-} discharges rapidly to V_{c1}. In State 6, the diode conducts a linearly increased negative I_{L1} current until the current reaches zero, where State 1 is again reached. With proper selection of inductors L_1, C_{T1+}, C_{T1+}, and C_1, the current I_{L1} waveform is achieved (see Figure 65). Hence, a GaN device does not have an antiparallel diode. Thus, an auxiliary Schottky SiC (or GaN) diode must be connected in parallel with the switch, as shown in Figure 65. Assuming that State 2 operates in a very short time, then:

$$V_{bus} = 2V_{c1}\left(1 + \frac{D_1}{1-D_1} + \frac{D_1}{1-D_1}\frac{D_3}{1-D_3}\right) \tag{58}$$

$$D_1 = \frac{t_{T1-} + t_{D1+}}{f} \tag{59}$$

$$D_3 = \frac{t_{T3-} + t_{D3+}}{f} \tag{60}$$

where t_{T1-} and t_{D1+} are the time of activation of T1- and D1+, respectively. Similarly, t_{T3-} and t_{D3+} are the time of activation of T3- and D3+, respectively.

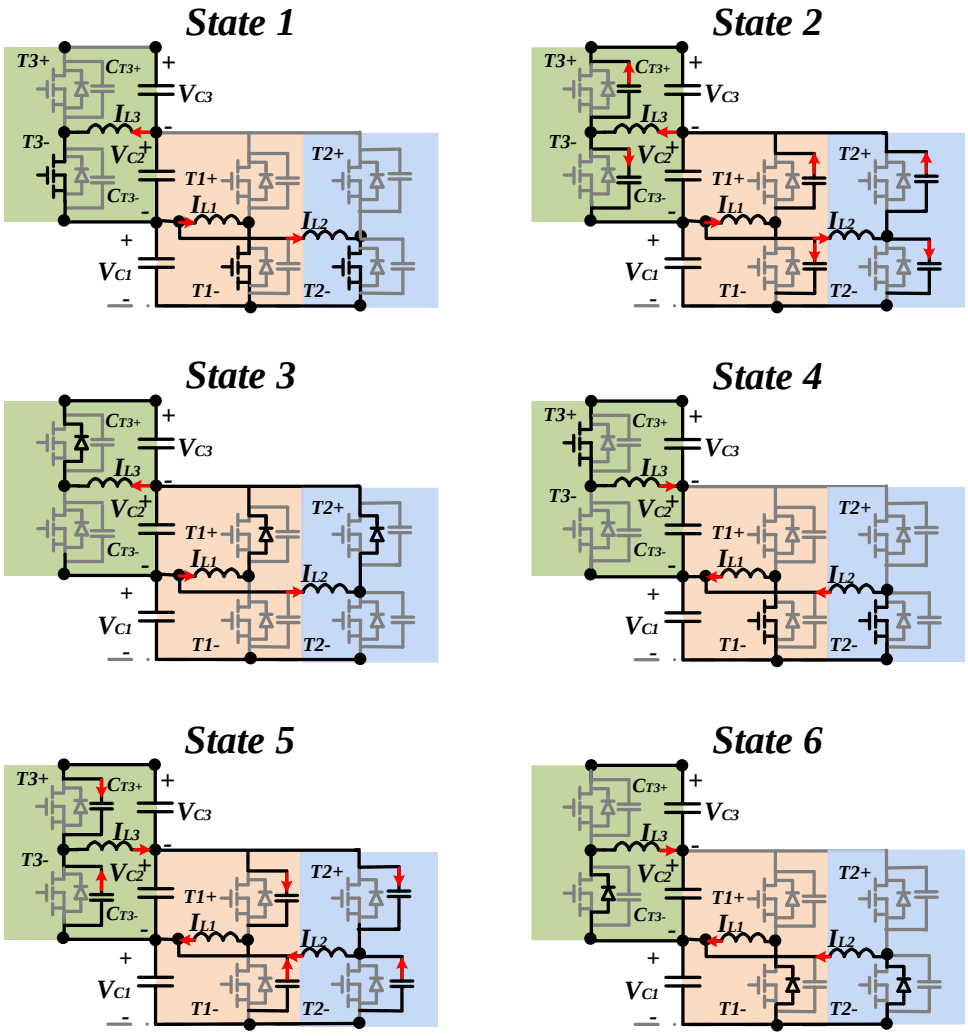

Figure 64 Operation states of the ZVS-IMMC DC-DC converter shown in Figure 61. Various states of ZVS operation are shown above and explained in Section IV.

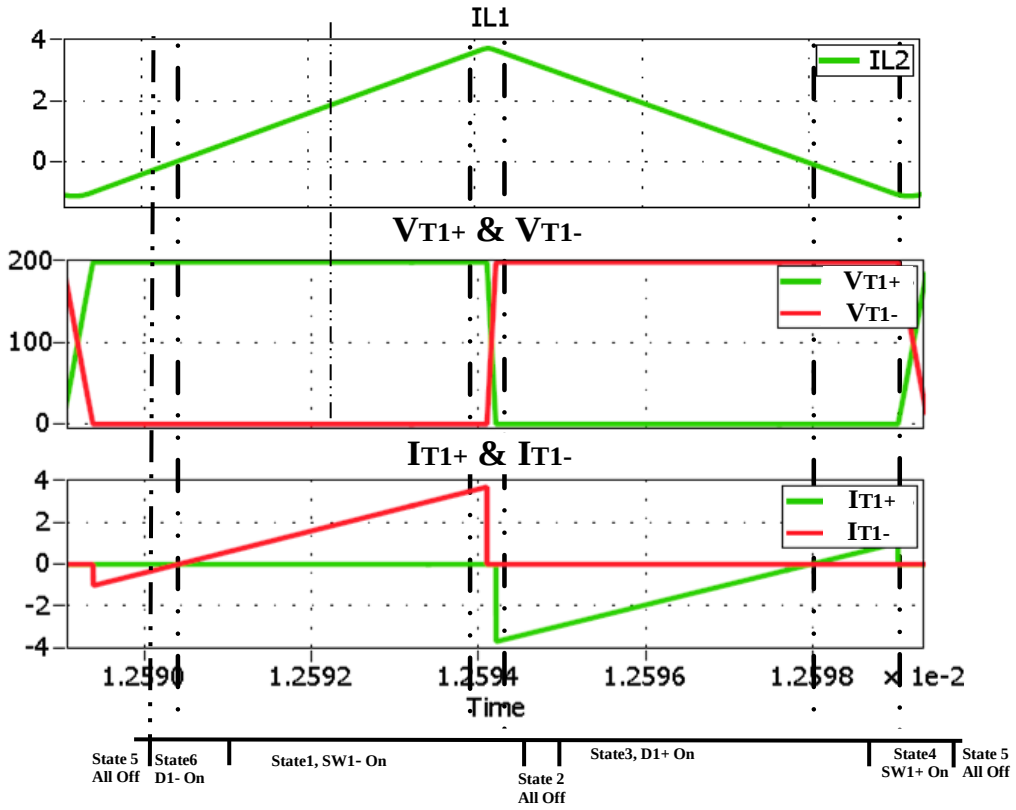

Figure 65 Waveforms of operation states of the ZVS-IMMC DC-DC converter shown in Figure 64.

5.5 Three-phase inverter stage

The proposed ZVS-IMMC, along with the merged MPPT and SoC controller, is interfaced with a three-phase inverter. For a balanced three-phase load, the bulky DC link buffer is no longer required. This is an inherent advantage of a three-phase inverter. Hence, the DC link is typically designed based on high switching frequency harmonics. The DC link is completely removed in the proposed approach and replaced with distributed compact capacitors C_1 to C_6 (see Figure 62). The inverter is operated at 100kHz with an SVPWM scheme to deliver optimum efficiency and size. The inverter is controlled via a DQ technique to control the power out of and into the grid. The inverter stage is followed by a three-phase LC filter to meet the 3% THD requirement specified in Table 9. The filter is followed by a three-phase common mode choke to reduce undesirable leakage current.

5.6 Design example

The design specifications selected are consistent with the YC1000-3 commercial three-phase microinverter manufactured by APsystems. The design parameters for the proposed topology are summarized in Table 1. One of the major advantages of the proposed topology is the integration of battery storage; thus, a 50V Li-ion battery was selected. Li-ion batteries have several advantages. They operate at a relatively high cell voltage and have a longer lifespan and lower self-discharge [91]. This has made them the industry choice for most recent high-energy density applications, especially in electric vehicles.

Table 9 Design Parameters for the Proposed Topology

Maximum Output Power (AC)	900W
MPPT Voltage Value for PV Panels	50V
Battery Storage Voltage	50V 20.7AH Li-ion ion battery pack [18]
3-Phase Output Voltage	120Y/208
Output Frequency	60Hz
Output Power Factor	> 0.99
Total Harmonic Distortion	< 3%

5.7 Simulation and experimental results of the proposed approach

This section illustrates the detailed software PSIM simulations of the proposed topology shown in Figure 62. Figures 66 and 67 show the operation of the proposed MPPT-SoC controller. It can be observed that the MPPT and suitable SoC were achieved for the given insolation profile. Also, the figure of merit P_s (defined as the product of V_s and I_s in Equation 50) matched with the optimum MPPT-SoC, as designed. The ZVS capacitor voltage-clamped operation of the ZVS-IMMC stage was simulated, as is shown in Figures 68 and 69. Figure 68 shows that the inductor currents I_{L1} to I_{L6} followed the ZVS capacitor-clamped waveform illustrated in Figure 65. Moreover, the capacitor voltages $V_{C1}$to V_{C6} all balanced at 50V, as was desired. Furthermore, the V_{bus} of 300V was achieved within a < 1% voltage ripple, consistent with Equation 58. Figure 69

verifies the ZVS operation of switches T1+ to T3+, where the corresponding gating signals of T1+ to T3+ turned the switches on and off at zero voltage. All other switches of the ZVS-IMMC stage operated similar to the ZVS shown Figure 65. Figure 70 depicts the operation of the three-phase inverter illustrated in Figure 62. Figure 70(a) verifies that a high-quality sinusoidal load current of 2.5% THD was achieved and interfaced with a 208Y/120 50Hz grid. Figure 70(b) shows the DC bus current I_{bus}. Figure 70(c) also shows the space vector modulation reference signals of the three-phase inverter stage control. Figure 71 illustrates the experimental results for the proposed approach, employing LMG3410-HB-EVM GaN devices for SM1 through SM7. In this setup, the proposed DC-DC converter shown in Figure 62 was tested in hard switching operation.

The input voltages V_{pv} and V_{batt} were assumed to be ideal DC voltage supplies. Hence, SM1 and SM2 were merged into one submodule, as were submodules SM4 and SM5, which was considered acceptable for hard switching operation. It was verified that the power sharing unit (SM7) was controlled to absorb equal power from the DC sources. In addition, by selecting the duty cycles (D1 and D2) to be 0.5 for all of the submodules, the input voltage of 32V was boosted six times (≈190V). The power rating of the tested prototype was 50W and the resulting efficiency 95.7%, despite the hard switching operation. The design parameters of the preliminary results are shown in Table 10.

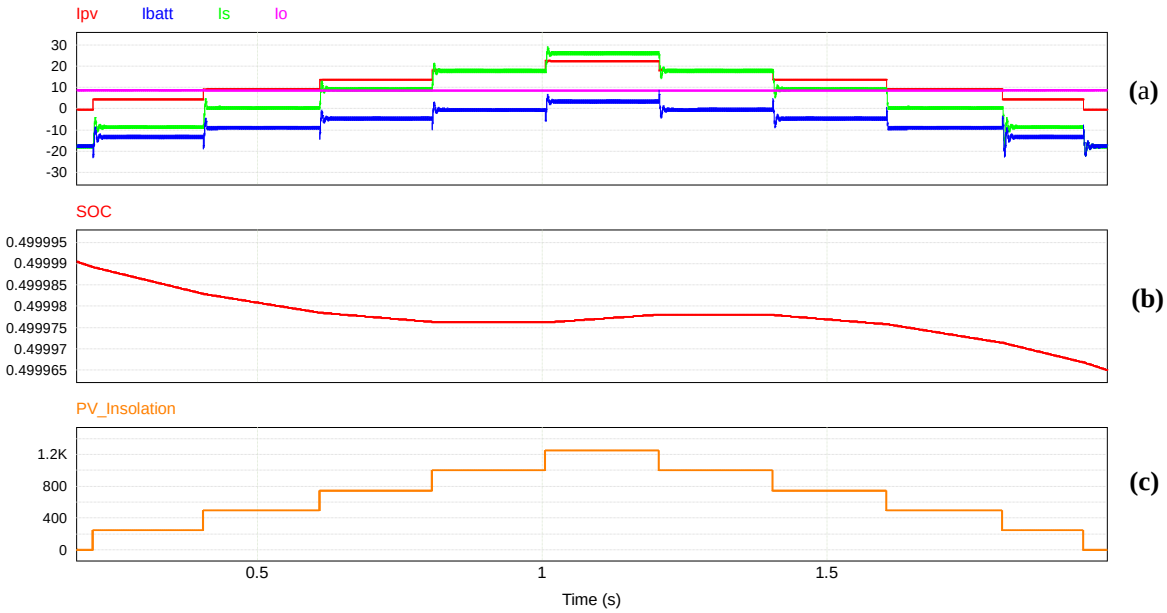

Figure 66 Operation of the PV/battery MPPT-SoC controller: a) the changes in currents $I_{pv}, I_{batt}, I_s,$ and I_o under different insolation levels; b) SoC curve of the 50V Li-ion battery storage; and c) the insolation profile applied in the 0 to 1,200W/m^2 range.

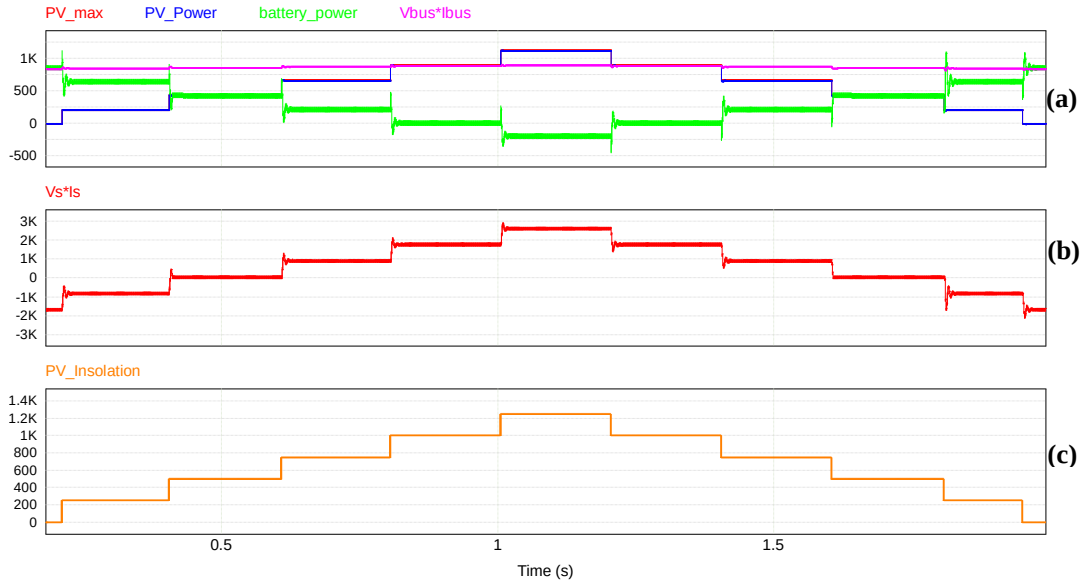

Figure 67 Operation of the PV/battery MPPT-SoC controller, showing that the figure of merit P_s in Equation 2 matched the optimum MPPT and SoC conditions: a) PV maximum possible power PV_max, PV harvested power PV_power, battery-stored power, and power injected into the grid (V_{bus}*I_{bus}); b) variations of P_s for the given insolation profile; and c) insolation profile applied in the 0 to 1200W/m^2 range.

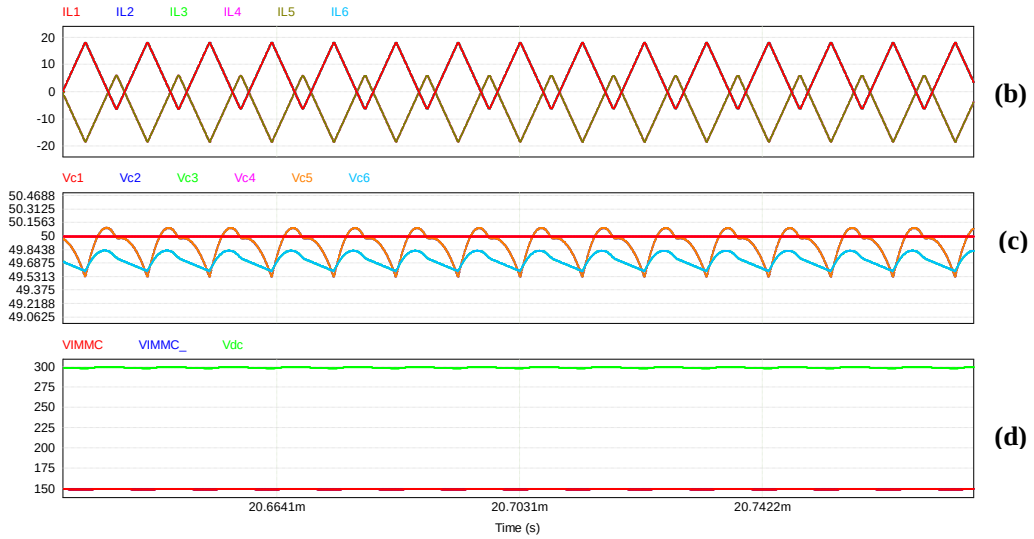

Figure 68 ZVS operation waveforms shown in Figure 62: a) inductor currents I_{L1} to I_{L6}, b) capacitor voltages V_{c1} to V_{c6} at 50V, and c) IMMC voltages V_{c1}+V_{c2}+V_{c3} and the overall DC bus voltage V_{bus}.

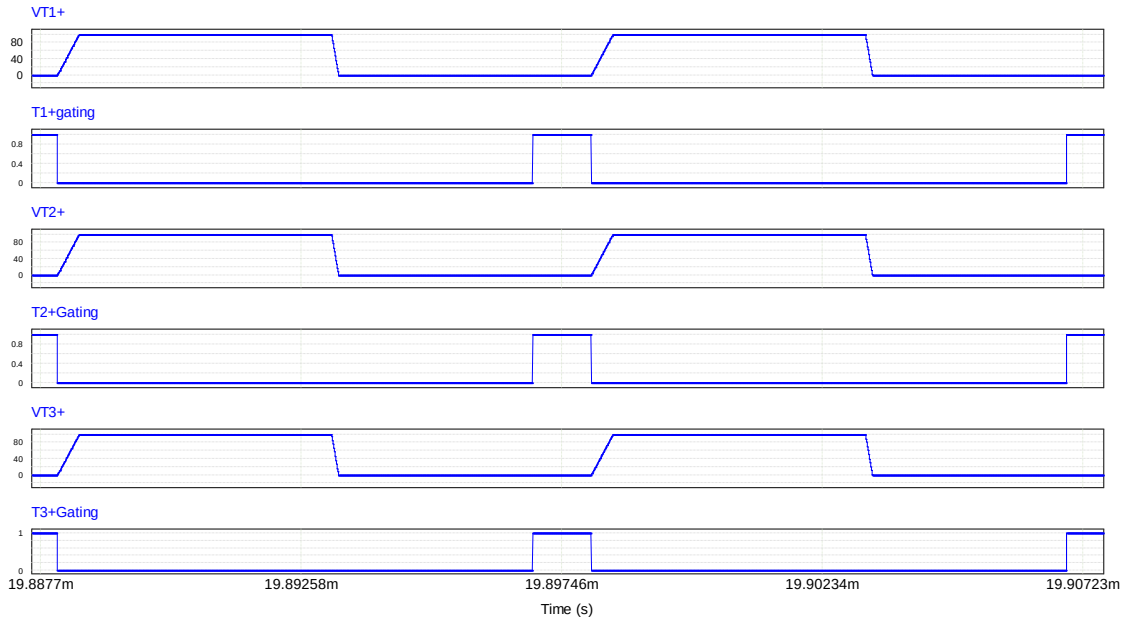

Figure 69 ZVS operation waveforms, showing the corresponding voltages and gating signals across switches T1+, T2+, and T3+.

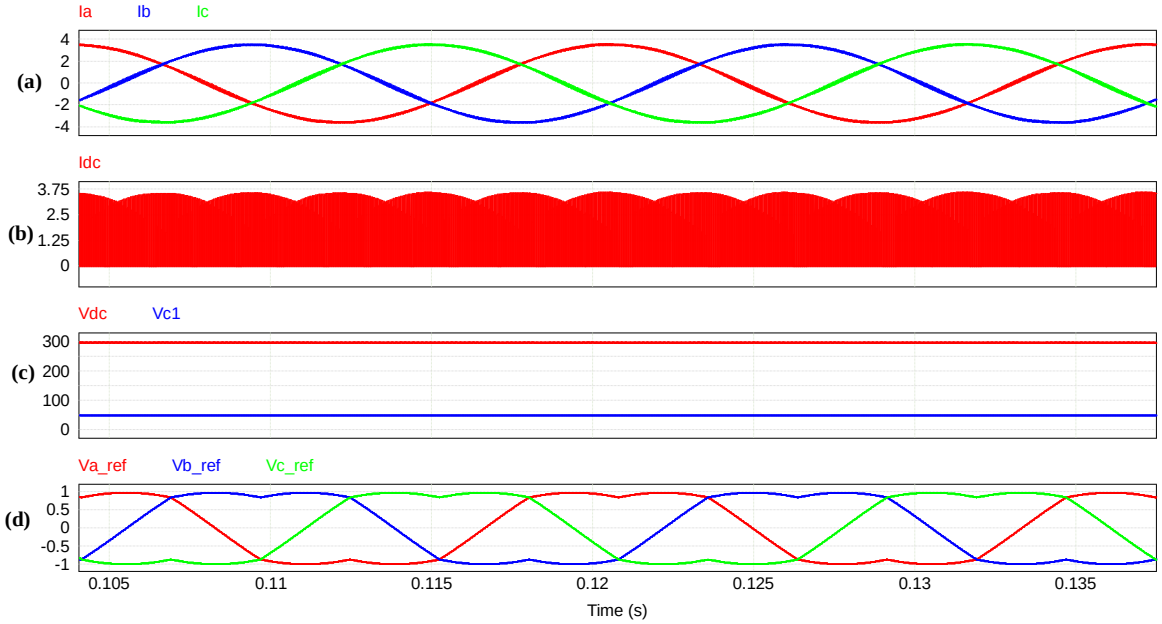

Figure 70 Three-phase inverter operation stage: a) line currents injected into the utility $I_a, I_b,$ and I_c; b) inverter input current I_{bus}; c) capacitor voltage V_{C1} of 50V and DC bus voltage V_{Bus} of 300V with less than 1% voltage ripple; and d) space vector modulation.

Table 10 Design Parameters for the Experimental Results

Parameter	Value
Input Voltage V_{PV}	32V
Output DC Bus Voltage V_{BUS}	190V
Inductor Values $L_1$to L_4	1.1mH
Capacitors Values C_1 to C_4	50µF
DC Link Capacitors	50µF
Switching Frequency	50kHz
Switching Device Using T_1 to T_4	LMG3410-HB-EVM GaN device rated 600V peak, 12A Peak
DC Load	50W
Efficiency	95.7%

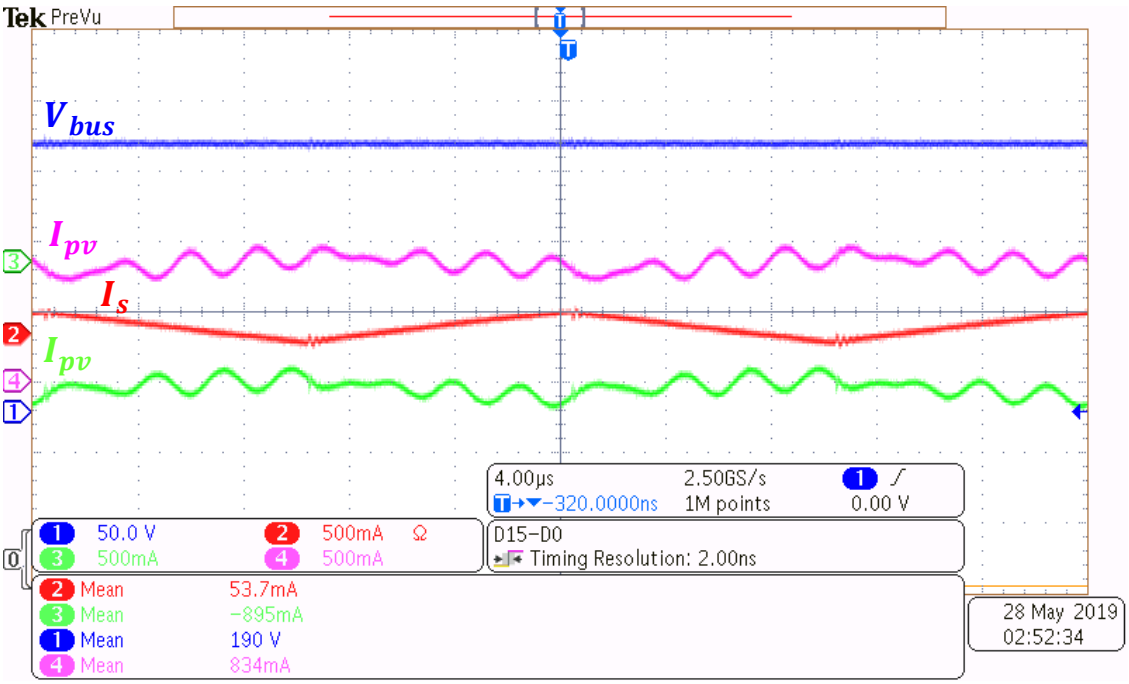

Figure 71 Preliminary hardware setup for the proposed approach for hard switching operation. V_{bus} depicts the DC bus voltage of 190V, I_{pv} shows the PV current, I_{batt} shows the battery current, and I_s indicates the inductor shared current, as illustrated in SM7.

6. IMPLEMENTATION OF DIGITAL WATERMARKING TECHNIQUE FOR CYBER-SECURITY OF PV INVERTER VIA HARDWARE-IN-THE-LOOP PLATFORM

6.1 Introduction to cyber-security for solar energy project at Texas A&M University

Cyber-security for solar energy is a collaborative project lead by Drs. Xie, Enjeti, and Kumar in the Electrical Engineering department in Texas A&M University. The project addresses the emerging risk of cyber-attack on solar energy, which is constituted mainly of microgrids via a dynamic watermarking technique [50, 92-94].

6.2 Cyber-attacks on residential inverter systems

PV inverter cyber-attacks have many cyber-intrusion points in emerging smart microgrid systems, as shown in Figure 72. In the case of residential applications, an attack could severely impact the PV inverter, as shown in Figure 73. This study utilizes the dynamic watermarking technique as a digital built-in pre-coded DSP, which acts as a physical cyber-security watermarking detection (CSWD) device. An attacker might target the inverter measurement signal, causing an inverter malfunction. The CSWD device is capable of injecting a watermarking signal e(k). Then, variance tests are continuously performed via a generated z(k) signal. The device can rapidly detect anomalies and inform the user about the risk of an intruder.

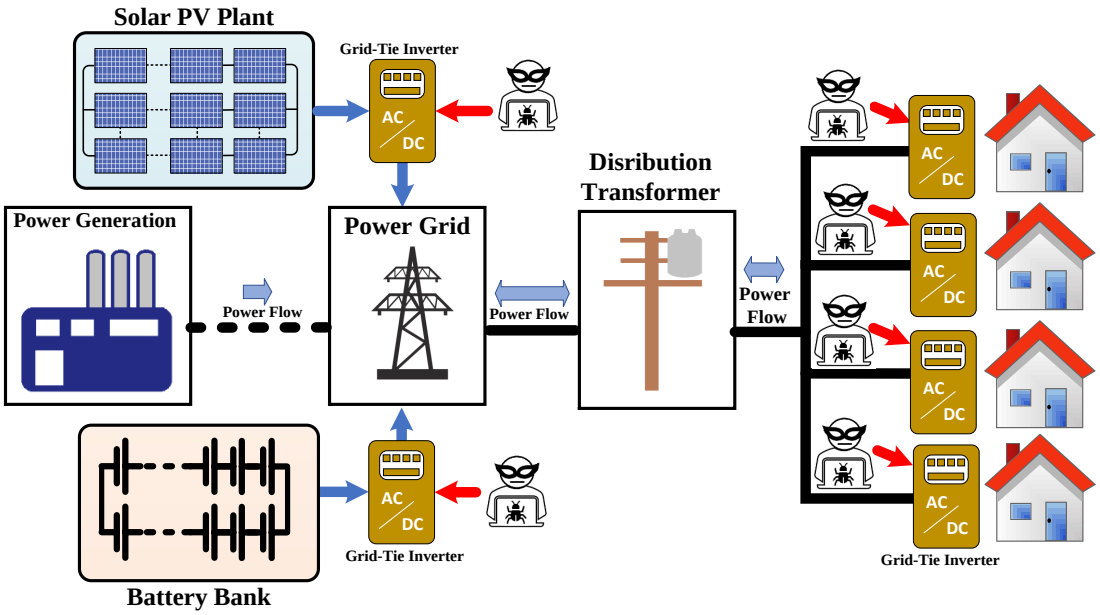

Figure 72 Several cyber-intrusion points in emerging microgrid systems.

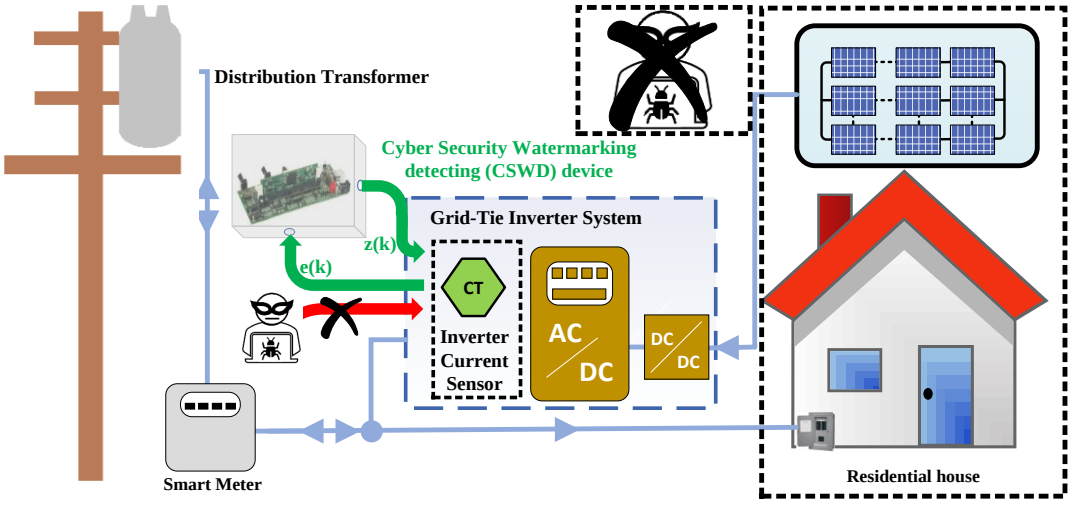

Figure 73 A view of cyber-security detection device used for a residential house.

6.3 Introduction to hardware-in-the-loop operation (HIL) using a PLECS RT box

HIL is a real-time simulation platform; it is widely accepted as a tool for complex computation systems such as power electronics converters [95-99]. HIL can emulate inverters by employing a sub-cycle algorithm [100]. This yields a high-fidelity inverter simulation that can interact in a lively fashion with a real DSP controller. The Plexim company has introduced an RT box system capable of performing HIL operations. The RT box can also work in rapid control prototyping mode, where it acts as a controller for the actual inverter. RT Box 1 operates a Xilinx Zynq Z-7030 system-on-chip that embeds two CPU cores on an FPGA. The FPGA fabric is used to control the ADCs and DACs of the analog channels and perform PWM generation and capture on digital channels. In this experiment, RT Box 1 was used to test a single-phase inverter for off-grid and on-grid operation.

6.4 Cyber-security testing framework for attacks on a single-phase inverter via HIL

Figure 74 describes the cyber-security testing framework for the experiment. The HIL platform was adopted to emulate a single-phase inverter. In Step 1, a low fidelity PSIM simulation was constructed in continuous mode. Step 2 expressed a discretized version of the simulation derived in Step 1, to allow for the delay caused by the ADC. In Step 3, a Simcoder tool was used in PSIM to allow for automatic code generation for the TI Code Composer Studio (CCS) software. CCS permits the use of the RAM debug mode to activate the variance tests or attacks via predefined global variables.

Step 4 involved building the single-phase inverter plant with grid. The constructed plant (inverter) was uploaded to RT Box 1 through the PLECS software. RT Box 1 allowed for viewing of the plant in real time in the PLECS software. Thus, if an attack was implemented, it could easily be viewed in PLECS. In Section 6.5, an off-grid single-phase inverter is implemented via HIL as a verification starting point. In Section 6.6, the on-grid single-phase inverter is derived. Thus, both the inverter and grid could be emulated in the PLECS RT box. In Section 6.7, an example of a cyber-attack called a "low-order harmonic injection attack" is described to demonstrate the effectiveness of the CWMD device via the above-described dynamic watermarking algorithm.

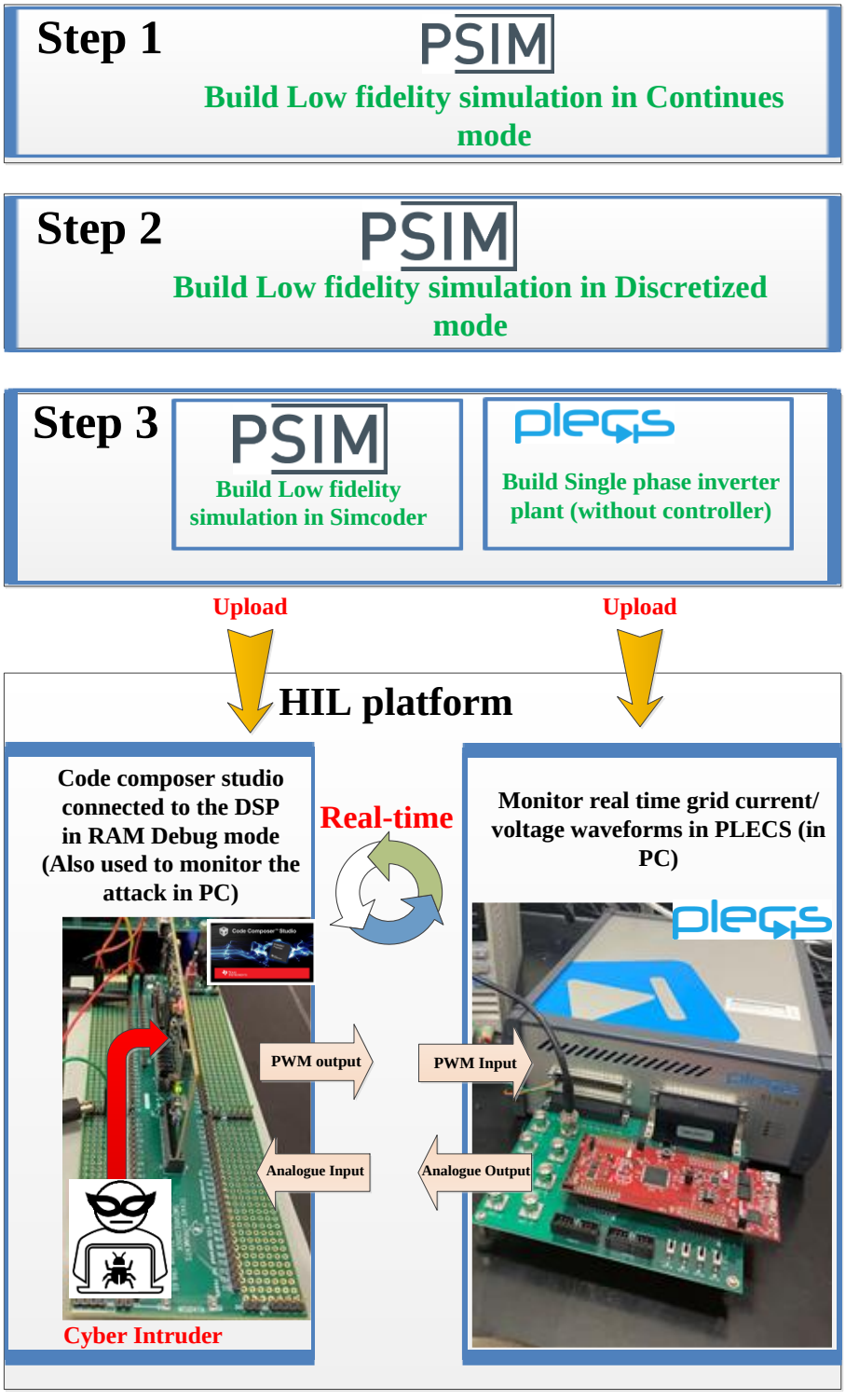

Figure 74 Cyber-security testing framework for the cyber-attack HIL platform.

6.5 Implementation of the off-grid single-phase inverter using a HIL RT box and TI DSB controller

In this experiment, an off-grid inverter was designed as a preliminary stage inverter to validate the RT box performance. The PSIM controller is described in Figure 75. It had a single inductor current sensor to control output via a PI controller with a sinusoidal reference. Four PWM digital outputs were used to drive the full-bridge inverter. Next, the Simcoder tool in the PSIM software was utilized to generate the TI CCS code. Then, CCS was employed to build and load the program in the TI-based DSP controller. A TIF28379D DSP designed by Texas Instruments in Dallas, TX, USA was employed as the DSP controller. Figure 76 shows the high-quality voltage for a resistive load and unfiltered inductor current, which in theory matched with normal off-grid single-phase inverter results.

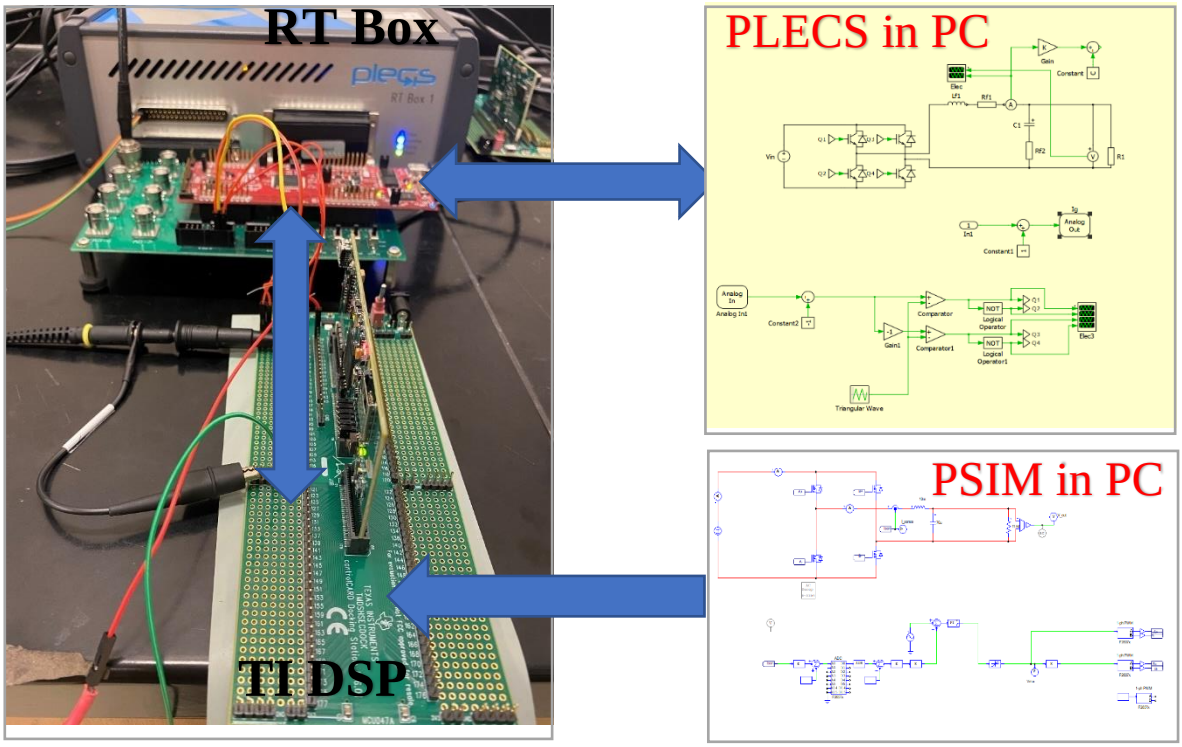

Figure 75 Off-grid inverter implementation in the HIL platform.

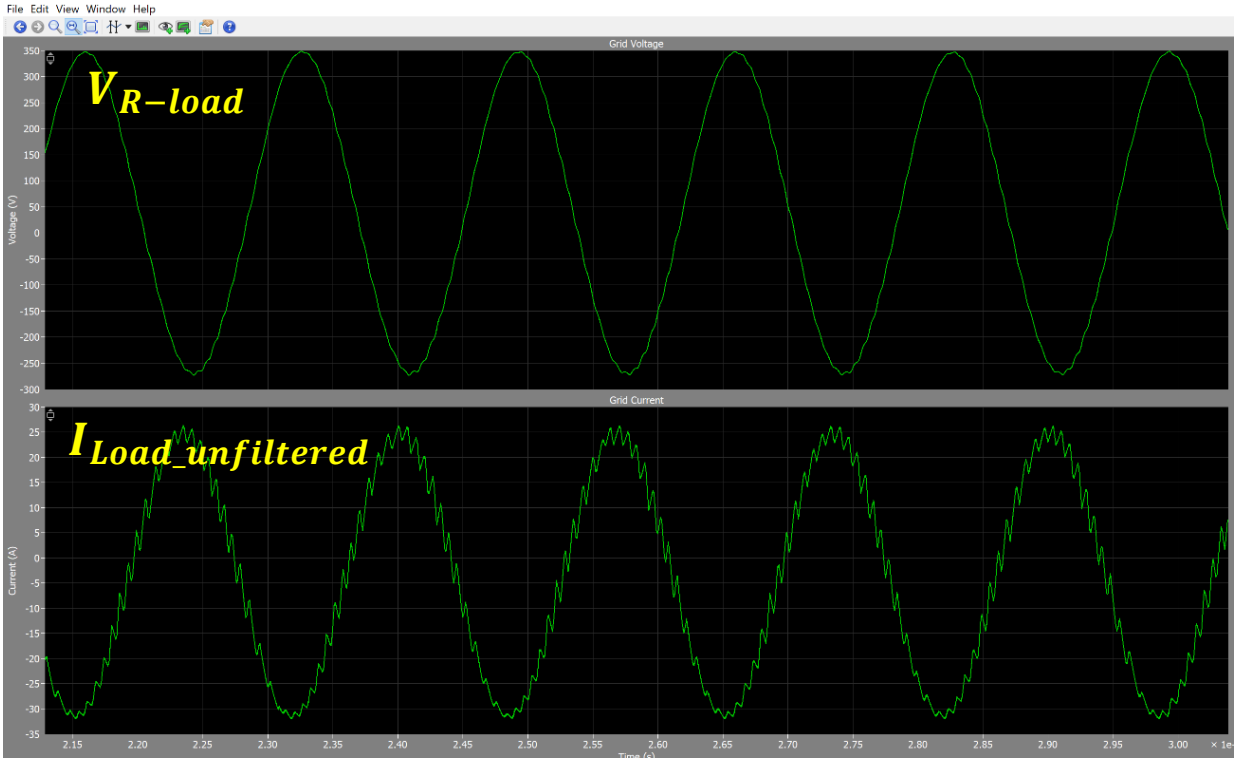

Figure 76 High-quality voltage for a resistive load and unfiltered inductor current.

6.6 Implementation of the on-grid single-phase inverter using a HIL RT box and TI DSB controller

In this experiment, an on-grid inverter was designed to validate the RT box performance in normal operation, as shown in Figure 77. The experiment was achieved per the cyber-security testing framework illustrated in Figure 74. Thus, Steps 1 through 3 were performed to prepare the HIL-emulated experimental setup. The design parameters for the on-grid inverter setup are detailed in Table 11. Figure 77(a) shows the PSIM closed-loop controller used for the inverter design. The controller had a voltage sensor for

performing PLL, using the grid voltage input. The controller included a grid current sensor to provide real and reactive power control via the Clarke and Park transform method. The input-sensed AC current ($\propto \beta$) was transformed to a DC signal in the dq frame. A PI controller was employed to track the grid current using the calculated DC grid current reference. Then, this DC current reference was calculated as per the specified real power of (1kW) shown in Table 11.

Next, the dq to $\propto \beta$ transformation was performed to create a modulating signal. The modulating signal was sent to the full-bridge inverter via four PWM digital outputs. The inverter was controlled with a unipolar PWM scheme to provide higher quality grid current. Similar to the off-grid inverter described in Section 6.4, the Simcoder tool in the PSIM software was utilized to generate the code needed for the TI CCS. After that, CCS was used to build and load the program in the TI-based DSP controller, as depicted in Step 3 and shown in Figure 74. Step 3 also required the full-bridge inverter circuit with the emulated grid to be uploaded into RT Box 1. The selected discretization step size was $1\mu s$, which was sufficient for the switching frequency of 10kHz shown in Table 11.

At this stage, the HIL platform was ready to be tested to check the normal real-time operation of the inverter, as per Figure 74. Consequently, the HIL operation was successfully implemented, as shown in Figure 78. Thus, the sinusoidal grid voltage was in phase with the grid current having a PF of ≈ 1, with an acceptable total harmonic distortion < 5%. In conclusion, the requirements specified in Table 11 were all met.

Table 11 Design Parameters for the Emulated On-grid Inverter Setup

Criterion	Value
Power Injected to the Grid	1kW
DC Link Input Voltage	200V
Output Voltage	120V AC
Output Frequency	60Hz
Output Power Factor	> 0.99
Total Harmonic Distortion	< 5%
Line Inductance	2.3mH
Switching Frequency	10kHz
Discretization Step Size (for RT Box)	$1\mu s$

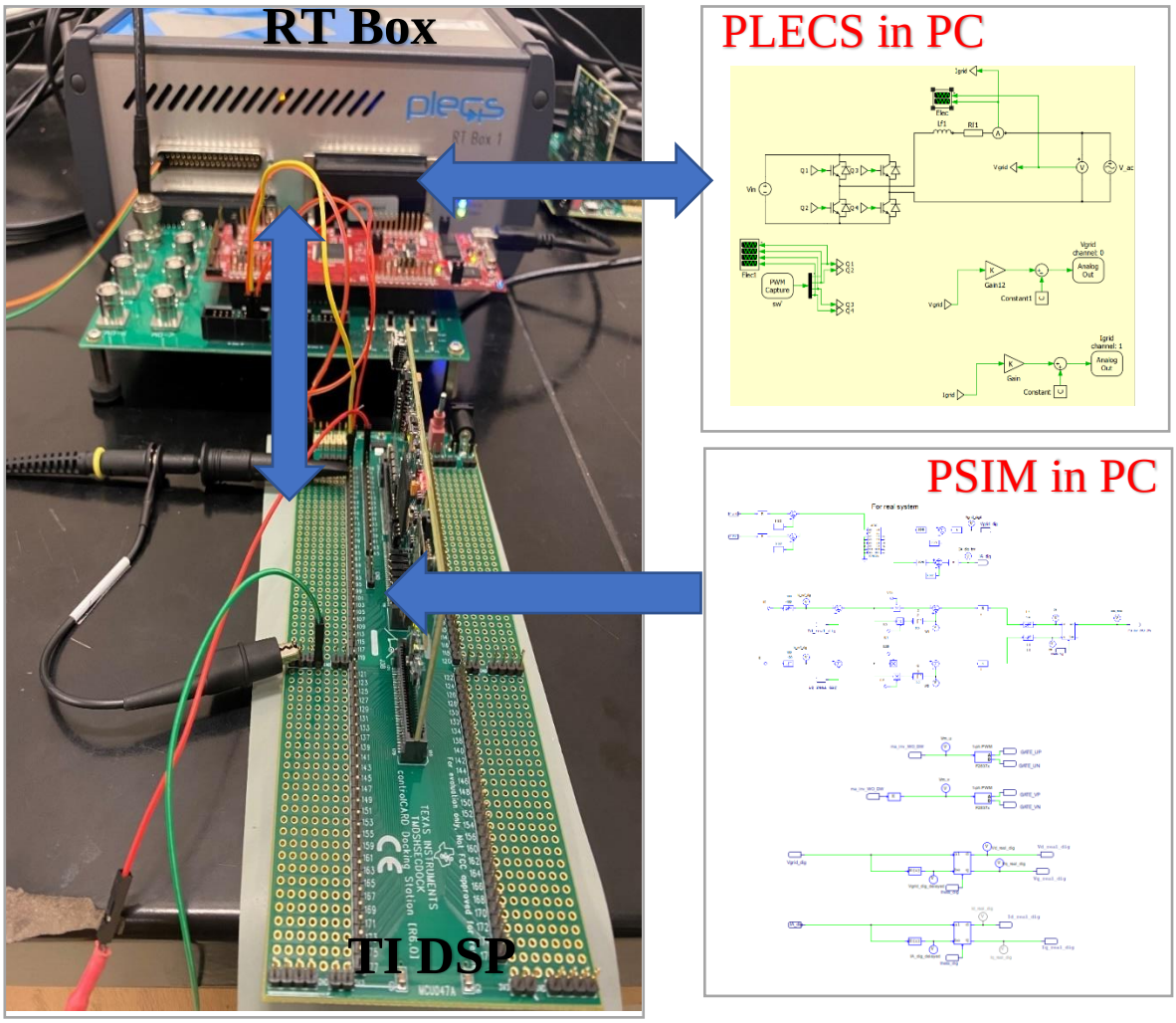

Figure 77 Implementation of the on-grid single-phase inverter via the HIL platform.

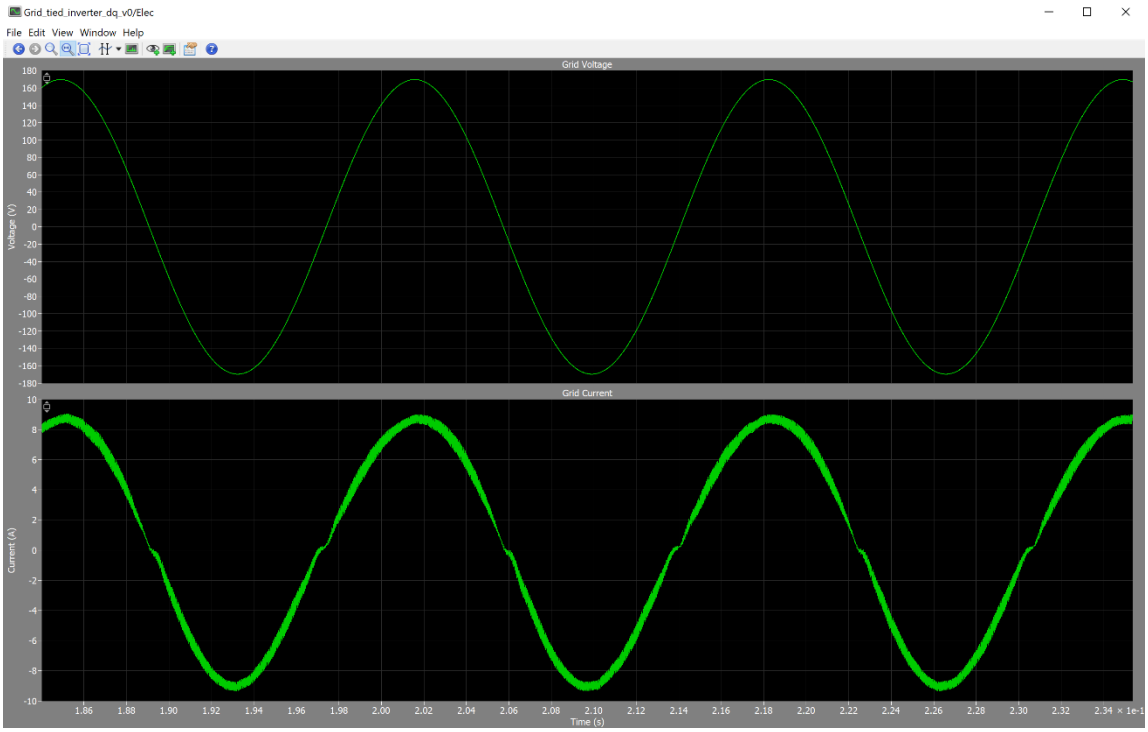

Figure 78 Sinusoidal grid voltage in phase with the grid current with an acceptable total harmonic distortion < 5%.

6.7 PV inverter performance in HIL under low-order harmonic injection attack

This section demonstrates an example of a cyber-attack on the on-grid inverter implemented in Section 6.6. The PV array and central DC-DC MPPT tracker were assumed to be a DC supply of 200V. In normal operation, the grid current measurement was genuine and feedback to the closed loop controller was as shown in Figure 78. Thus, the requirement of a high-quality sinusoidal current with PF ≈ 1 and THD of < 5% was met.

Figure 79 illustrates a cyber-attack on the measured grid current. The hypothetical attacker disconnected the genuine grid current measurement and replaced it with a manipulated current signal. Such a disconnection could be implemented physically or online. The manipulated current was assumed to include low-order harmonics (i.e., third- and fifth-order harmonics). This attack resulted in increasing power losses and decreasing power capacity of the inverter. It also distorted the grid current such that the 5% THD was no longer met.

Figure 80 demonstrates the dynamic watermarking technique. This method can be implemented to rapidly detect cyber-attack activity and inform resident owners. It involves injecting a random gaussian signal with a zero mean into the actuator. Normally, the grid current is continuously monitored via the Test 1 and Test 2 blocks. These tests are derived based on knowledge of the system identification matrix, as well as a good understanding of system performance. The tests generate an input signal into the dynamic watermarking detection algorithm (DWDA) block. The DWDA block outputs a variance signal that shows an increase above a pre-specified threshold value (in the event of malicious measurement). In this research, a low-fidelity simulation is shown in PLEC to demonstrate how variance exceeds the threshold value when a cyber-attack is initiated. Tests 1 and 2 were activated at a time of 0.3s, causing a slight increase in variance. The harmonic attack was activated at a time of 0.4s, where the variance significantly increased above the threshold value of 1.

Given the cyber-security testing framework shown in Figure 74, the next step was to implement the attack in the emulated HIL platform. The watermarking detection algorithm and Tests 1 and 2 were already uploaded in the DSP controller. Thus, the DSP acted as the cyber-security watermark detection (CSWD) device described in Figure 73. In addition, the low-order harmonic injection attack was prebuilt in the DSP controller, where it could be initiated manually using the ram debug window in the CCS software (as expressed in Figure 83). It was confirmed that the CSWD device successfully detected the low-order harmonic injection attack, where the variance increased significantly, above a threshold value of 0.4. This was also monitored in real time using RT Box 1, as demonstrated in Figure 85. Table 12 summarizes the advantages of the implemented CWMD device as compared to other cyber-security detection methods.

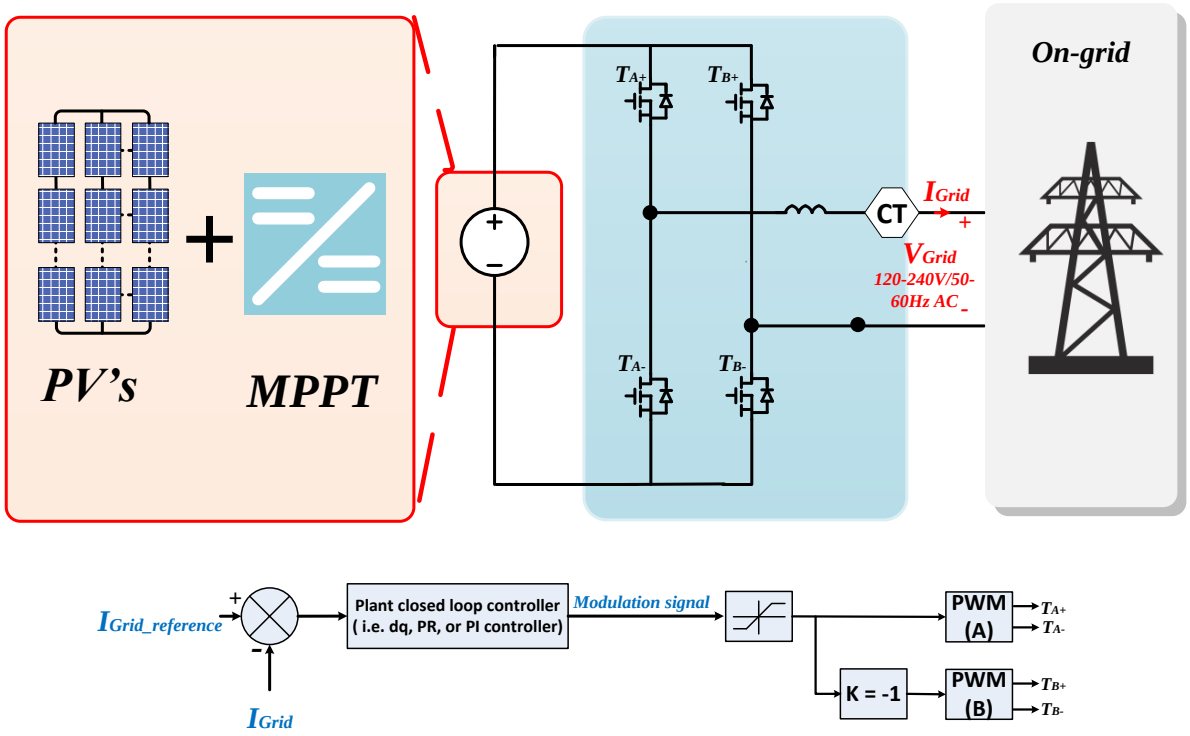

Figure 79 Inverter in normal operation, where the grid current measurement is genuine and there is feedback to the closed loop controller.

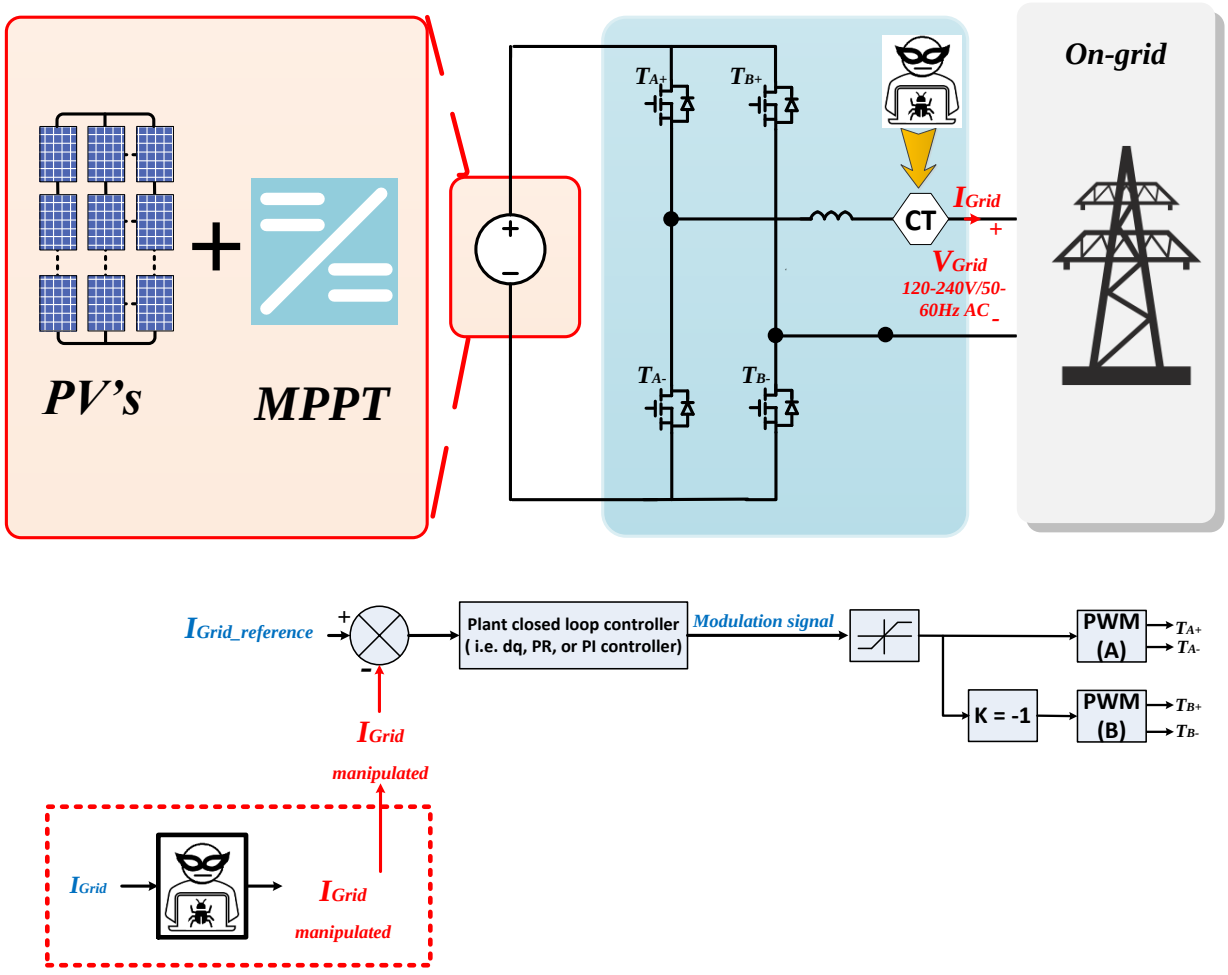

Figure 80 Cyber-attack on the measured grid current.

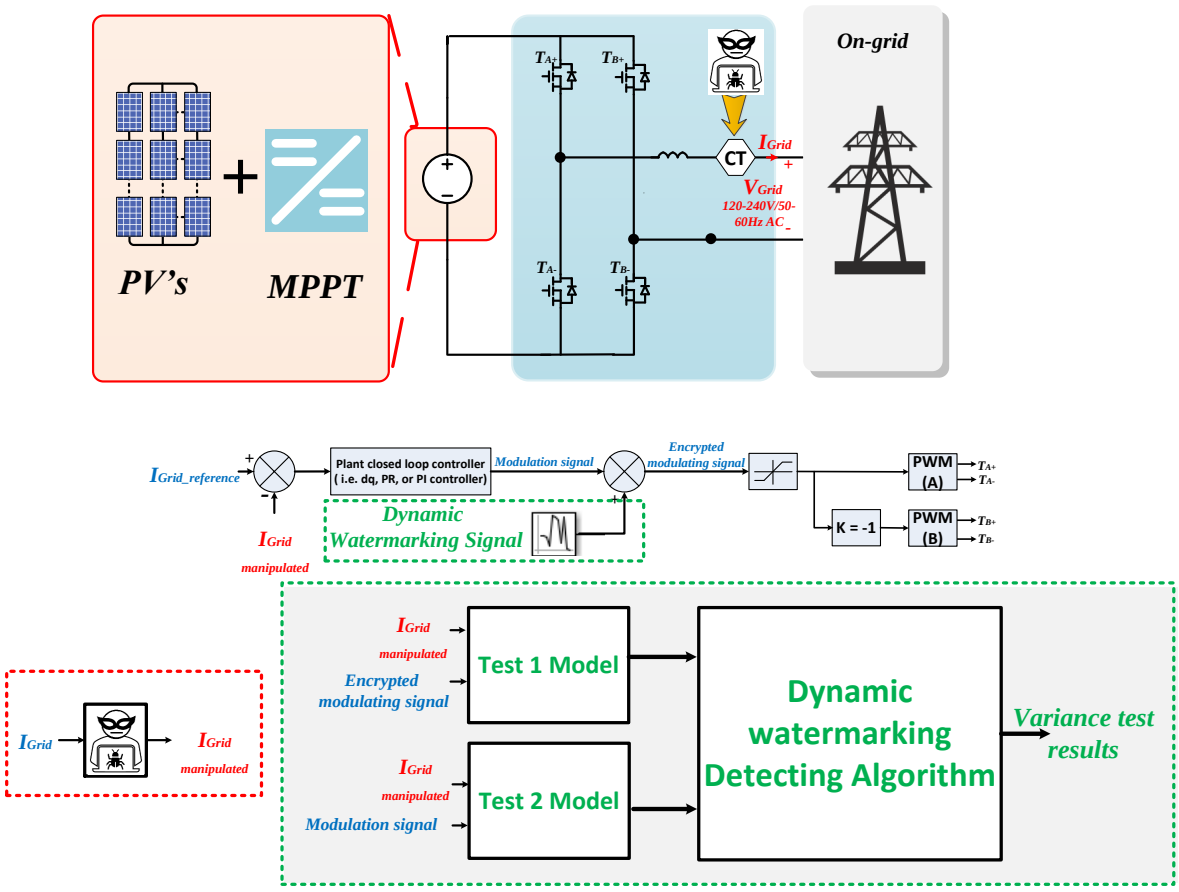

Figure 81 Inverter in cyber-attack secured operation with the integration of the implemented dynamic water marking technique, where the grid current measurement is vulnerable to intruders.

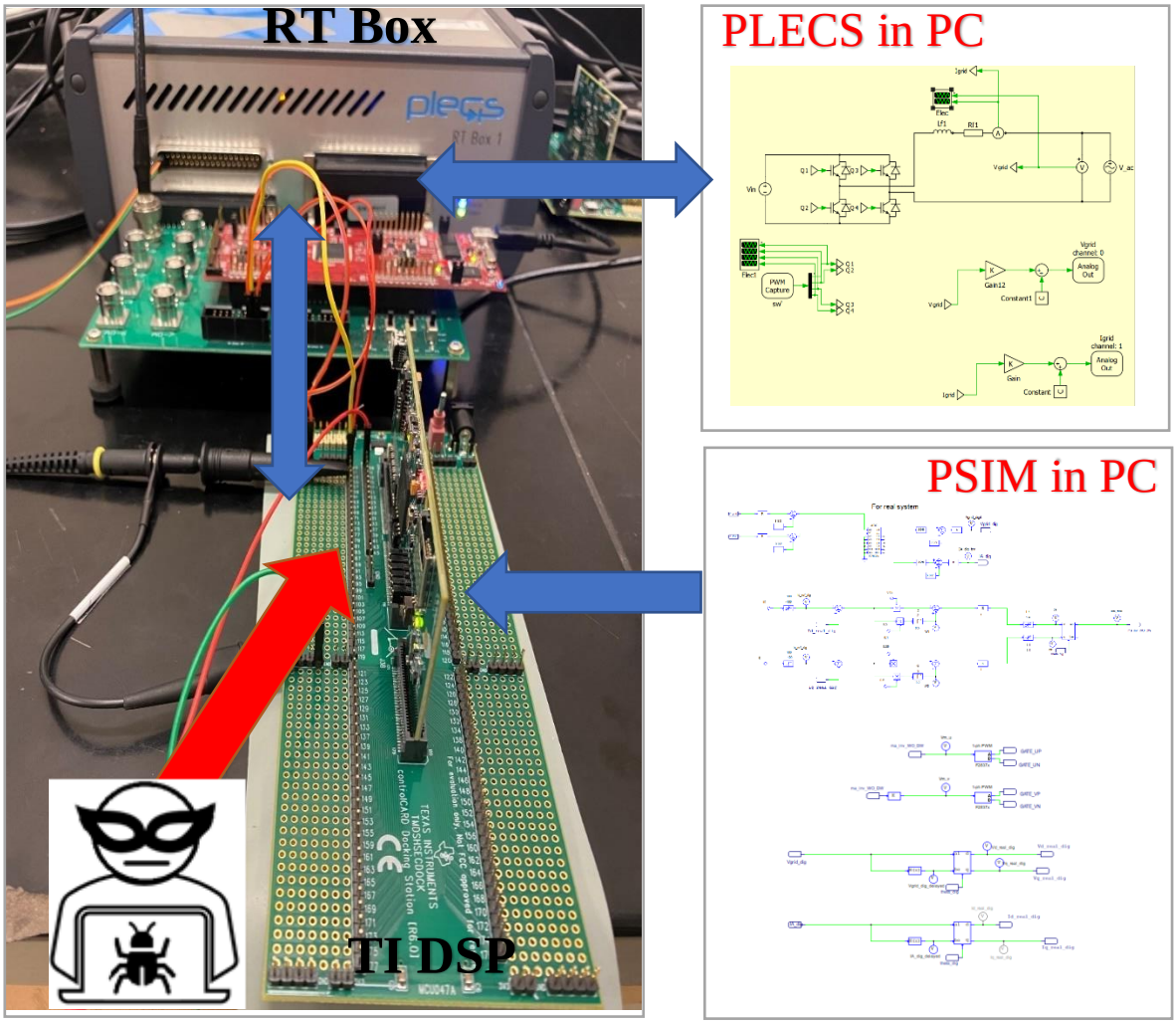

Figure 82 PV inverter performance in HIL under a harmonic attack.

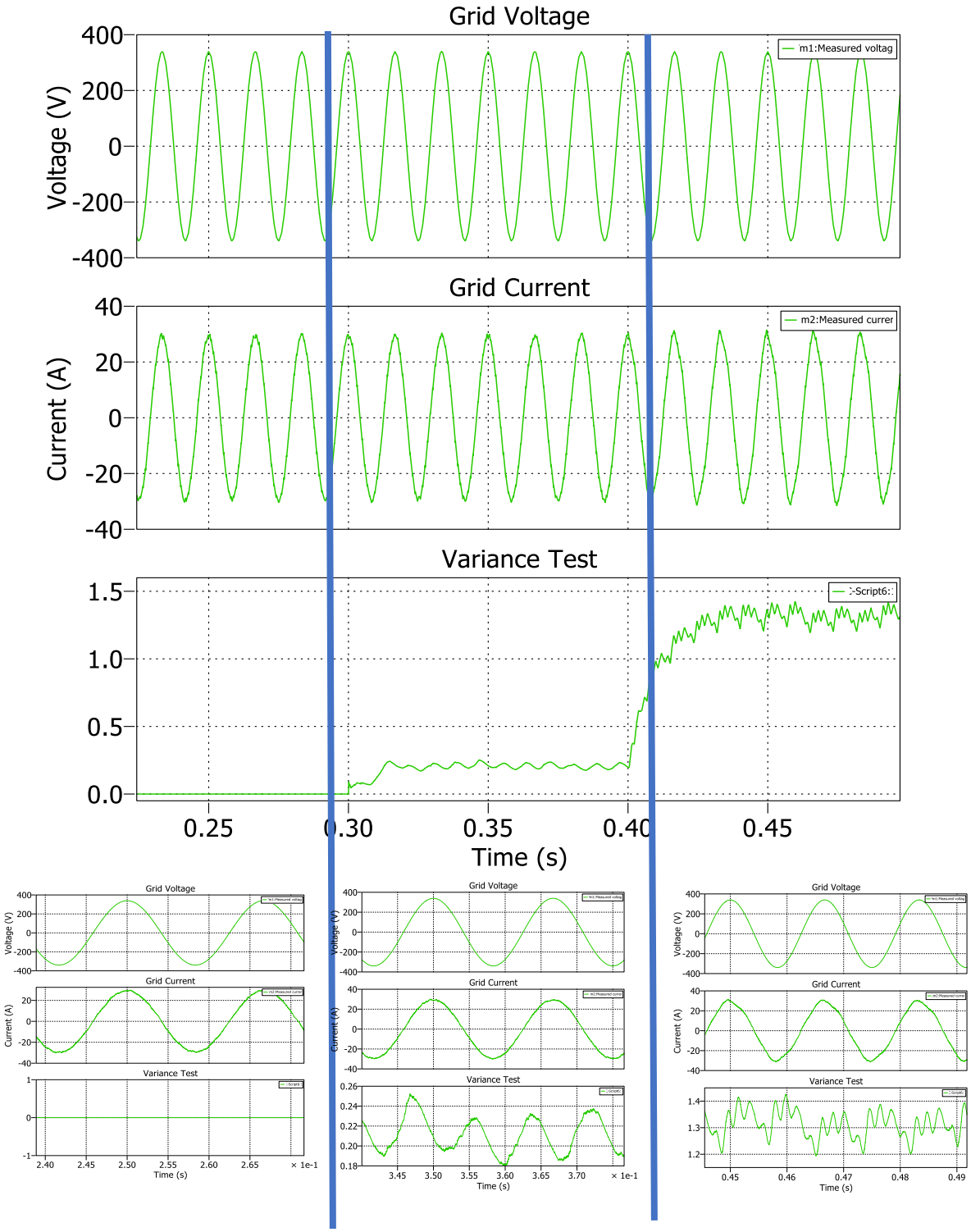

Figure 83 Simulation results for the harmonic attack: (a) Region of normal operation before applying Tests 1 and 2. (b) Region where Tests 1 and 2 were applied; in this region, the signal was genuine. (c) Region of harmonic attack where the signal was manipulated

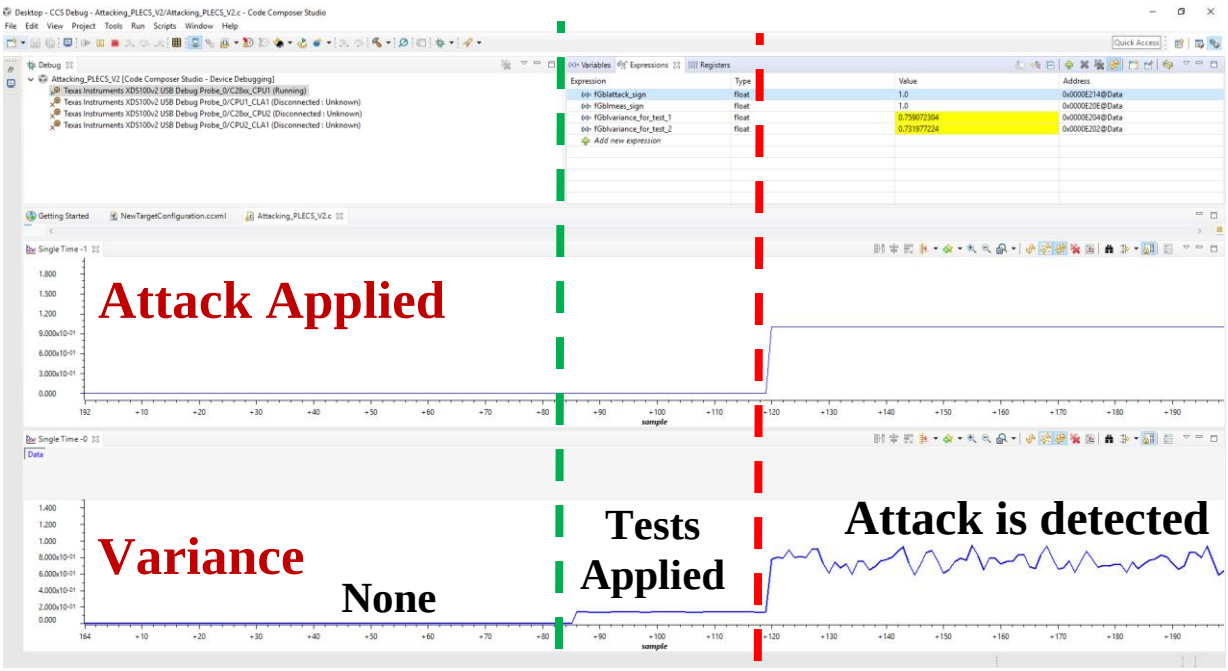

Figure 84 Debug window of CCS. Note that the variance tests effectively detected the low-order harmonic attack.

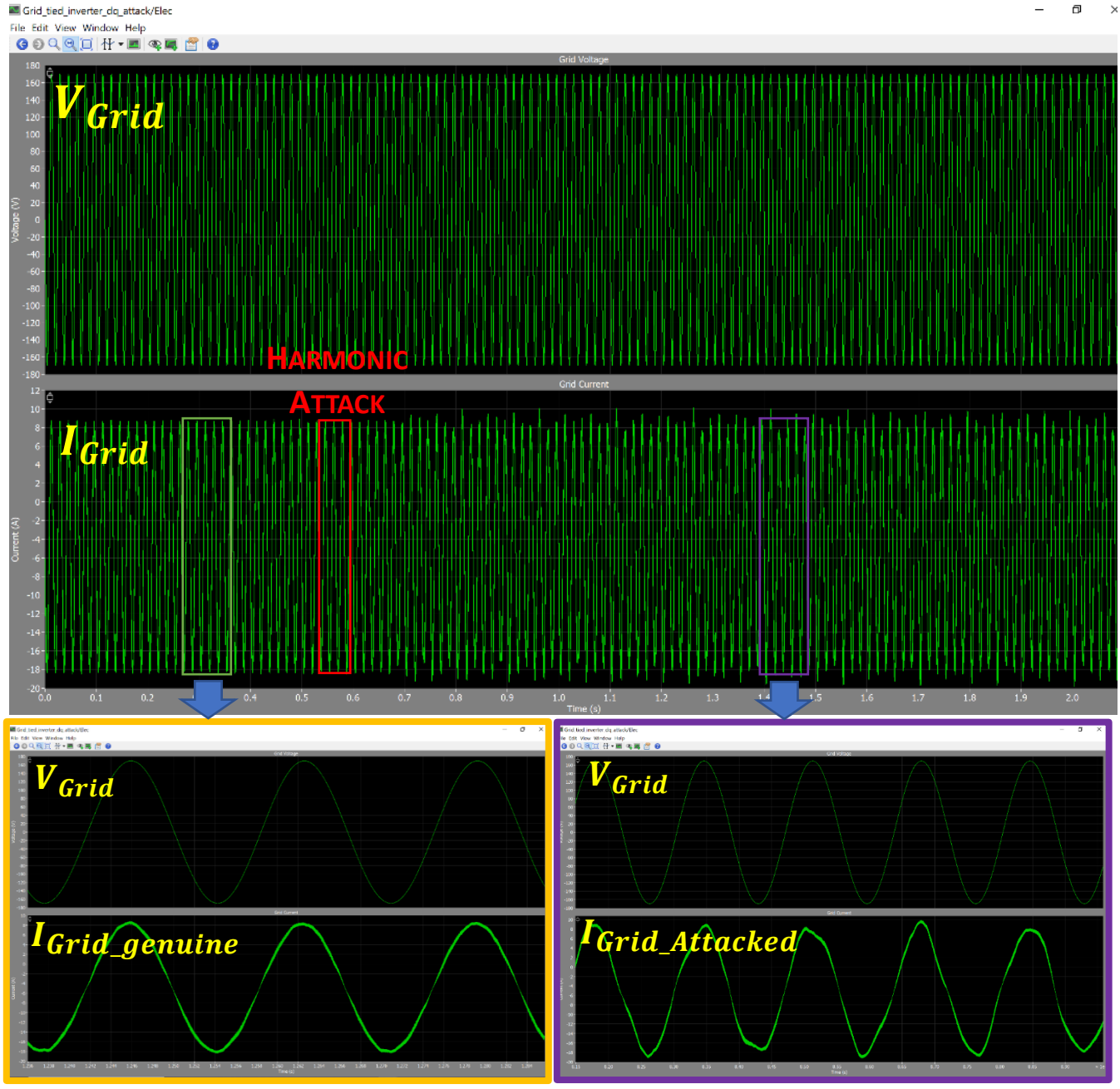

Figure 85 HIL results shown in PLECS software in real time. The orange region shows a genuine Igrid. The red region illustrates that a harmonic attack has been initiated.

Table 12 Comparison of CSWD device and Other Cyber-Security Approaches

Criterion (when under attack)	Alternative Approach	Our Approach
Cyber-attack Detection Time	**Slow/moderate**	**Very fast**
Ability to Detect Several Attack Types	**Limited**	**Able to detect several types of attacks (bias, toggle, noise, recording, stealth, etc.)**
Installation	**Costly and difficult**	**Affordable and easy to install**
Communication with Another Agent	**Required**	**Not required**
Inverter and Auxiliary Device Vulnerability to Attack	**Vulnerable**	**Resistant**

7. CONCLUSION

In this research, several new transformerless power electronics converters were discussed for utilities, commercial enterprises, and micro-grids. A medium voltage DC collection grid method for large-scale PV plants was proposed for utility power grids. A twin IMMC DC–DC boost converter topology, along with an integrated power sharing converter, was shown to control two solar PV plants. The power sharing stage addressed individual MPPTs under partial shading conditions. The IMMC DC–DC boost stage was composed of half-bridge converter modules stacked in series. The analysis, design, and detailed simulation results for the 1MW PV plant were discussed above.

It has been shown that two PV power plants can be operated at two different MPPT points. Although the capacitor voltage ripple was set to 15%, the output DC voltage ripple was less than 1%, due to the 180◦ phase shift operation of the upper and lower IMMC stages. Control of the proposed converter and performance under different solar insolation conditions showed stable operation. The simulation results of the proposed converter for various operating conditions were discussed above. The experimental results from a low-voltage laboratory prototype converter were presented to verify key results.

In addition, an SSTL microinverter with an integrated BSS was proposed. This topology was envisioned as a high switching frequency power semiconductor unit with compact passive elements and the ability to realize a 240V/60Hz AC output. The single-stage topology was composed of a power sharing unit, twin IMMC units, and a single-phase inverter with a built-in active decoupling leg. It was demonstrated that the DC link

capacitor value could be reduced due to a 180^{o} phase-shift operation of the DC-DC IMMC, along with the active decoupling stage within the inverter. The results from various operating modes of the proposed topology were discussed above. The experimental results from a prototype laboratory converter were explained to demonstrate the proposed topology.

The SSTL concept was also extended for a hybrid three-phase inverter commercial grid interface. The newly proposed merged SOC/MPPT algorithm, along with the ZVS IMMC operation, yielded highly efficiency operation.

In the end, implementation of a digital dynamic watermarking technique was introduced via a HIL platform. The technique was coded in the DSP controller as a hardware detector device tested in HIL. The detector device successfully recognized a low-order harmonic injection cyber-attack by initiating a significant increase in the output variance test reading.

REFERENCES

[1] EIA. "Net consumption of electricity worldwide from 1980 to 2017 (in billion kilowatt hours) [Graph]." https://www.statista.com/statistics/280704/world-power-consumption/ (accessed 7 Nov, 2020).

[2] O. Alsayegh, N. Saker, and A. Alqattan, "Integrating sustainable energy strategy with the second development plan of Kuwait," *Renewable and Sustainable Energy Reviews,* vol. 82, pp. 3430-3440, 2018/02/01/ 2018, doi: https://doi.org/10.1016/j.rser.2017.10.048.

[3] IRENA. "GLOBAL ENERGY TRANSFORMATION." https://www.irena.org/-/media/Files/IRENA/Agency/Publication/2018/Apr/IRENA_Report_GET_2018.pdf (accessed 2 Dec, 2019).

[4] K. Tashiro, H. Wakiwaka, S. Inoue, and Y. Uchiyama, "Energy Harvesting of Magnetic Power-Line Noise," *IEEE Transactions on Magnetics,* vol. 47, no. 10, pp. 4441-4444, 2011, doi: 10.1109/TMAG.2011.2158190.

[5] S. A. Pelaez, C. Deline, P. Greenberg, J. S. Stein, and R. K. Kostuk, "Model and Validation of Single-Axis Tracking With Bifacial PV," *IEEE Journal of Photovoltaics,* vol. 9, no. 3, pp. 715-721, 2019, doi: 10.1109/JPHOTOV.2019.2892872.

[6] IRENA. "RENEWABLE CAPACITY STATISTICS 2020." https://www.irena.org/-/media/Files/IRENA/Agency/Publication/2020/Mar/IRENA_RE_Capacity_Statistics_2020.pdf (accessed 7 Nov, 2020).

[7] SMA. "The new compact SUNNY HOME MANAGER 2.0." https://www.sma.de/en/products/monitoring-control/sunny-home-manager-20.html (accessed 21 Nov, 2019).

[8] H. Keshan, J. Thornburg, and T. S. Ustun, "Comparison of lead-acid and lithium ion batteries for stationary storage in off-grid energy systems," in *4th IET Clean Energy and Technology Conference (CEAT 2016)*, 14-15 Nov. 2016 2016, pp. 1-7, doi: 10.1049/cp.2016.1287.

[9] M. Torkashvand, A. Khodadadi, M. B. Sanjareh, and M. H. Nazary, "A Life Cycle-Cost Analysis of Li-ion and Lead-Acid BESSs and Their Actively Hybridized

ESSs With Supercapacitors for Islanded Microgrid Applications," *IEEE Access*, vol. 8, pp. 153215-153225, 2020, doi: 10.1109/ACCESS.2020.3017458.

[10] J. N. Russell Hensley, and Matt Rogers. "Battery technology charges ahead." McKinsey Quarterly. https://www.mckinsey.com/~/media/McKinsey/Business%20Functions/Sustainability/Our%20Insights/Battery%20technology%20charges%20ahead/Battery%20technology%20charges%20ahead.pdf (accessed 8 Nov, 2020).

[11] H. Zeng *et al.*, "Introduction of Australian 100MW Storage Operation and its Enlightenment to China," in *2018 China International Conference on Electricity Distribution (CICED)*, 17-19 Sept. 2018 2018, pp. 2895-2900, doi: 10.1109/CICED.2018.8592035.

[12] C. Simpson. "All The Details On Tesla's Giant Australian Battery." https://www.gizmodo.com.au/2017/07/all-the-details-on-teslas-giant-australian-batteryt/ (accessed 30 Dec, 2020).

[13] L. POWER. "LS Power Energizes Largest Battery Storage Project in the World, The 250 MW Gateway Project in California." https://www.lspower.com/ls-power-energizes-largest-battery-storage-project-in-the-world-the-250-mw-gateway-project-in-california-2/ (accessed 30 Dec, 2020).

[14] C. Katz. "The batteries that could make fossil fuels obsolete." BBC. https://www.bbc.com/future/article/20201217-renewable-power-the-worlds-largest-battery (accessed 30 Dec, 2020).

[15] P. Palmer, X. Zhang, E. Shelton, T. Zhang, and J. Zhang, "An experimental comparison of GaN, SiC and Si switching power devices," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 29 Oct.-1 Nov. 2017 2017, pp. 780-785, doi: 10.1109/IECON.2017.8216135.

[16] K. Shirabe *et al.*, "Efficiency Comparison Between Si-IGBT-Based Drive and GaN-Based Drive," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 566-572, 2014, doi: 10.1109/TIA.2013.2290812.

[17] P. Alemi, Y. Jeung, and D. Lee, "DC-Link Capacitance Minimization in T-Type Three-Level AC/DC/AC PWM Converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 3, pp. 1382-1391, 2015, doi: 10.1109/TIE.2014.2345354.

[18] K. Hasegawa, I. Omura, and S. Nishizawa, "Design and Analysis of a New Evaluation Circuit for Capacitors Used in a High-Power Three-Phase Inverter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 5, pp. 2679-2687, 2016, doi: 10.1109/TIE.2015.2511097.

[19] N. Zhao, G. Wang, D. Xu, L. Zhu, G. Zhang, and J. Huo, "Inverter Power Control Based on DC-Link Voltage Regulation for IPMSM Drives Without Electrolytic Capacitors," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 558-571, 2018, doi: 10.1109/TPEL.2017.2670623.

[20] D. E. Whitehead, K. Owens, D. Gammel, and J. Smith, "Ukraine cyber-induced power outage: Analysis and practical mitigation strategies," in *2017 70th Annual Conference for Protective Relay Engineers (CPRE)*, 3-6 April 2017 2017, pp. 1-8, doi: 10.1109/CPRE.2017.8090056.

[21] J. Qi, A. Hahn, X. Lu, J. Wang, and C. Liu, "Cybersecurity for distributed energy resources and smart inverters," *IET Cyber-Physical Systems: Theory & Applications*, vol. 1, no. 1, pp. 28-39, 2016, doi: 10.1049/iet-cps.2016.0018.

[22] J. A. Ansere, G. Han, L. Liu, Y. Peng, and M. Kamal, "Optimal Resource Allocation in Energy-Efficient Internet-of-Things Networks With Imperfect CSI," *IEEE Internet of Things Journal*, vol. 7, no. 6, pp. 5401-5411, 2020, doi: 10.1109/JIOT.2020.2979169.

[23] M. R. Islam, A. M. Mahfuz-Ur-Rahman, M. M. Islam, Y. G. Guo, and J. G. Zhu, "Modular Medium-Voltage Grid-Connected Converter With Improved Switching Techniques for Solar Photovoltaic Systems," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8887-8896, 2017, doi: 10.1109/TIE.2017.2652402.

[24] E. Gkoutioudi, P. Bakas, and A. Marinopoulos, "Comparison of PV systems with maximum DC voltage 1000V and 1500V," in *2013 IEEE 39th Photovoltaic Specialists Conference (PVSC)*, 16-21 June 2013 2013, pp. 2873-2878, doi: 10.1109/PVSC.2013.6745070.

[25] B. Hafez, H. S. Krishnamoorthy, P. Enjeti, U. Borup, and S. Ahmed, "Medium voltage AC collection grid for large scale photovoltaic plants based on medium frequency transformers," in *2014 IEEE Energy Conversion Congress and Exposition (ECCE)*, 14-18 Sept. 2014 2014, pp. 5304-5311, doi: 10.1109/ECCE.2014.6954128.

[26] E. Serban, M. Ordonez, and C. Pondiche, "DC-Bus Voltage Range Extension in 1500 V Photovoltaic Inverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 3, no. 4, pp. 901-917, 2015, doi: 10.1109/JESTPE.2015.2445735.

[27] H. Choi, M. Ciobotaru, M. Jang, and V. G. Agelidis, "Performance of Medium-Voltage DC-Bus PV System Architecture Utilizing High-Gain DC–DC Converter," *IEEE Transactions on Sustainable Energy*, vol. 6, no. 2, pp. 464-473, 2015, doi: 10.1109/TSTE.2014.2382690.

[28] M. Morjaria. "Advances in Utility-SCal PV Plants: Key Lessons Learned." https://site.ieee.org/scv-sust/files/slides/20171101-Advances-in-Utility-Scale-PV-Plants-Key-Lessons-Learned.pdf (accessed 22 Jun, 2018).

[29] W. Li, K. He, and Y. Wang, "Cost comparison of AC and DC collector grid for integration of large-scale PV power plants," *The Journal of Engineering*, vol. 2017, no. 13, pp. 795-800, 2017, doi: 10.1049/joe.2017.0440.

[30] D. Ahmadi, S. A. Mansouri, and J. Wang, "Circuit topology study for distributed MPPT in very large scale PV power plants," in *2011 Twenty-Sixth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 6-11 March 2011 2011, pp. 786-791, doi: 10.1109/APEC.2011.5744685.

[31] H. Krishnamoorthy, M. Daniel, J. Ramos-Ruiz, P. Enjeti, L. Liu, and E. Aeloiza, "Isolated AC–DC Converter Using Medium Frequency Transformer for Off-Shore Wind Turbine DC Collection Grid," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8939-8947, 2017, doi: 10.1109/TIE.2017.2652405.

[32] Y. Lian, G. P. Adam, D. Holliday, and S. J. Finney, "Medium-voltage DC/DC converter for offshore wind collection grid," *IET Renewable Power Generation*, vol. 10, no. 5, pp. 651-660, 2016, doi: 10.1049/iet-rpg.2015.0376.

[33] H. A. B. Siddique and R. W. D. Doncker, "Evaluation of DC Collector-Grid Configurations for Large Photovoltaic Parks," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 311-320, 2018, doi: 10.1109/TPWRD.2017.2702018.

[34] M. Kasper, D. Bortis, and J. W. Kolar, "Novel high voltage conversion ratio "Rainstick" DC/DC converters," in *2013 IEEE Energy Conversion Congress and Exposition*, 15-19 Sept. 2013 2013, pp. 789-796, doi: 10.1109/ECCE.2013.6646783.

[35] K. Filsoof and P. W. Lehn, "A Bidirectional Modular Multilevel DC–DC Converter of Triangular Structure," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 54-64, 2015, doi: 10.1109/TPEL.2014.2307004.

[36] ENPHASE. "Powerful technology at the heart of the Enphase system." https://enphase.com/en-us/products-and-services/microinverters (accessed 3 Nov, 2019).

[37] R. A. Amarin, Ghaith Haddad, Hussam Alatrash, and Imran Ahmed Bhutta, "Micro-Inverter Based AC-Coupled Photovoltaic Microgrid System with Wireless Smart-Grid Controls," USA Patent Appl. 14/181,009, 2014.

[38] MarketWatch. "Micro-Inverter Market Size, Share, Report, Analysis, Trends & Forecast to 2026." https://www.marketwatch.com/press-release/micro-inverter-market-size-share-report-analysis-trends-forecast-to-2026-2019-01-31 (accessed 3 Nov, 2019).

[39] TESLA. "Powerwall." https://www.tesla.com/powerwall (accessed 18 Nov, 2020).

[40] H. Chiu *et al.*, "A module-integrated isolated solar microinverter," *IEEE Transactions on Industrial Electronics,* vol. 60, no. 2, pp. 781-788, 2013, doi: 10.1109/TIE.2012.2206351.

[41] N. Kummari, S. Chakraborty, and S. Chattopadhyay, "An Isolated High-Frequency Link Microinverter Operated with Secondary-Side Modulation for Efficiency Improvement," *IEEE Transactions on Power Electronics,* vol. 33, no. 3, pp. 2187-2200, 2018, doi: 10.1109/TPEL.2017.2699945.

[42] P. T. Krein, R. S. Balog, and M. Mirjafari, "Minimum Energy and Capacitance Requirements for Single-Phase Inverters and Rectifiers Using a Ripple Port," *IEEE Transactions on Power Electronics,* vol. 27, no. 11, pp. 4690-4698, 2012, doi: 10.1109/TPEL.2012.2186640.

[43] T. Zhao, V. Bhavaraju, P. Nirantare, and J. Xu, "Evaluation of commercial scale transformerless solar inverter technology," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, 20-24 Sept. 2015 2015, pp. 5342-5348, doi: 10.1109/ECCE.2015.7310411.

[44] S. J. Castillo, R. S. Balog, and P. Enjeti, "Predicting capacitor reliability in a module-integrated photovoltaic inverter using stress factors from an environmental usage model," in *North American Power Symposium 2010*, 26-28 Sept. 2010 2010, pp. 1-6, doi: 10.1109/NAPS.2010.5618955.

[45] Y. Sun, Y. Liu, M. Su, W. Xiong, and J. Yang, "Review of Active Power Decoupling Topologies in Single-Phase Systems," *IEEE Transactions on Power Electronics,* vol. 31, no. 7, pp. 4778-4794, 2016, doi: 10.1109/TPEL.2015.2477882.

[46] M. Rajeev and V. Agarwal, "Analysis and Control of a Novel Transformer-Less Microinverter for PV-Grid Interface," *IEEE Journal of Photovoltaics,* vol. 8, no. 4, pp. 1110-1118, 2018, doi: 10.1109/JPHOTOV.2018.2825298.

[47] J. Roy and R. Ayyanar, "GaN based transformer-less microinverter with coupled inductor interleaved boost and half bridge voltage swing inverter," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 4-8 March 2018 2018, pp. 381-386, doi: 10.1109/APEC.2018.8341039.

[48] S. D. Roy and S. Debbarma, "Detection and Mitigation of Cyber-Attacks on AGC Systems of Low Inertia Power Grid," *IEEE Systems Journal*, vol. 14, no. 2, pp. 2023-2031, 2020, doi: 10.1109/JSYST.2019.2943921.

[49] T. Nguyen, S. Wang, M. Alhazmi, M. Nazemi, A. Estebsari, and P. Dehghanian, "Electric Power Grid Resilience to Cyber Adversaries: State of the Art," *IEEE Access*, vol. 8, pp. 87592-87608, 2020, doi: 10.1109/ACCESS.2020.2993233.

[50] T. Huang, B. Satchidanandan, P. R. Kumar, and L. Xie, "An Online Detection Framework for Cyber Attacks on Automatic Generation Control," *IEEE Transactions on Power Systems*, vol. 33, no. 6, pp. 6816-6827, 2018, doi: 10.1109/TPWRS.2018.2829743.

[51] S. Sahoo, Y. Yang, and F. Blaabjerg, "Resilient Synchronization Strategy for AC Microgrids Under Cyber Attacks," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 73-77, 2021, doi: 10.1109/TPEL.2020.3005208.

[52] H. Wang *et al.*, "Deep Learning-Based Interval State Estimation of AC Smart Grids Against Sparse Cyber Attacks," *IEEE Transactions on Industrial Informatics*, vol. 14, no. 11, pp. 4766-4778, 2018, doi: 10.1109/TII.2018.2804669.

[53] M. Chlela, D. Mascarella, G. Joós, and M. Kassouf, "Fallback Control for Isochronous Energy Storage Systems in Autonomous Microgrids Under Denial-of-Service Cyber-Attacks," *IEEE Transactions on Smart Grid*, vol. 9, no. 5, pp. 4702-4711, 2018, doi: 10.1109/TSG.2017.2667586.

[54] F. Li *et al.*, "Detection and Diagnosis of Data Integrity Attacks in Solar Farms Based on Multilayer Long Short-Term Memory Network," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 2495-2498, 2021, doi: 10.1109/TPEL.2020.3017935.

[55] D. J. S. Cardenas, A. Hahn, and C. C. Liu, "Assessing Cyber-Physical Risks of IoT-Based Energy Devices in Grid Operations," *IEEE Access*, vol. 8, pp. 61161-61173, 2020, doi: 10.1109/ACCESS.2020.2983313.

[56] B. O. S. AUTOMATION. "Standalone Li-Ion UPS from Bedrock Automation Sets New Performance and Cyber Security Standard for Industrial Control System Backup." https://bedrockautomation.com/standalone-li-ion-ups-from-bedrock-automation-sets-new-performance-and-cyber-security-standard-for-industrial-control-system-backup/ (accessed 9 Nov, 2020).

[57] M. MUNSELL. "10 Trends That Will Shape the Global Solar Market in 2018." gtm. https://www.greentechmedia.com/articles/read/solar-trends-2018-gtm-research#gs.e9TXsS0 (accessed 31 Jan, 2018).

[58] S. Lude *et al.*, "Optimization of the Technology Mix for the Shagaya 2 GW Renewable Energy Park in Kuwait," *Energy Procedia*, vol. 69, pp. 1633-1642, 2015/05/01/ 2015, doi: https://doi.org/10.1016/j.egypro.2015.03.120.

[59] ecodirect. "Helios 9T6-420 > 420 Watt Solar Panel." https://www.ecodirect.com/Helios-9T6-420-420W49V-PV-Panel-p/helios-9t6-420.htm (accessed 22 Jun, 2018).

[60] A. H. Wijenayake *et al.*, "Next-generation MVDC architecture based on 6.5 kV / 200 A, 12.5 mΩ SiC H-bridge and 10 kV / 240 A, 20 mΩ SiC dual power modules," in *2017 IEEE Electric Ship Technologies Symposium (ESTS)*, 14-17 Aug. 2017 2017, pp. 598-604, doi: 10.1109/ESTS.2017.8069343.

[61] A. S. Morsy and P. N. Enjeti, "Comparison of Active Power Decoupling Methods for High-Power-Density Single-Phase Inverters Using Wide-Bandgap FETs for Google Little Box Challenge," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 790-798, 2016, doi: 10.1109/JESTPE.2016.2573262.

[62] N. Saxena, I. Hussain, B. Singh, and A. L. Vyas, "Implementation of a Grid-Integrated PV-Battery System for Residential and Electrical Vehicle Applications," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 8, pp. 6592-6601, 2018, doi: 10.1109/TIE.2017.2739712.

[63] K. Alluhaybi, I. Batarseh, and H. Hu, "Comprehensive Review and Comparison of Single-Phase Grid-Tied Photovoltaic Microinverters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1310-1329, 2020, doi: 10.1109/JESTPE.2019.2900413.

[64] S. A. S. Al-Obaidi, K. C. Hodge, and P. Enjeti, "A Dual-Phase Output 4-Leg Inverter with Active Decoupling and Integrated Power Optimizer for Off-Grid Applications," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, 25-28 June 2018 2018, pp. 1-6, doi: 10.1109/PEDG.2018.8447594.

[65] F. Alhuwaishel and P. Enjeti, "A Single Stage Transformer-less Micro Inverter with Integrated Battery Storage System for Residential Applications," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 17-20 June 2019 2019, pp. 1-7, doi: 10.1109/COMPEL.2019.8769691.

[66] I. Batarseh and K. Alluhaybi, "Emerging Opportunities in Distributed Power Electronics and Battery Integration: Setting the Stage for an Energy Storage Revolution," *IEEE Power Electronics Magazine*, vol. 7, no. 2, pp. 22-32, 2020, doi: 10.1109/MPEL.2020.2987114.

[67] N. G. N. Irias, H. d. Paula, P. Pereira, E. N. Cardoso, and B. M. Lopes, "Degradation of photovoltaic panels induced by electric potential: Theoretical survey and computational study on the inverter operation influence," in *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, 29 Nov.-2 Dec. 2015 2015, pp. 1-6, doi: 10.1109/COBEP.2015.7420165.

[68] B. F. Nehme, T. K. Akiki, A. Naamane, and N. K. M. Sirdi, "Real-Time Thermoelectrical Model of PV Panels for Degradation Assessment," *IEEE Journal of Photovoltaics*, vol. 7, no. 5, pp. 1362-1375, 2017, doi: 10.1109/JPHOTOV.2017.2711430.

[69] J. Oh, S. Bowden, and G. TamizhMani, "Potential-Induced Degradation (PID): Incomplete Recovery of Shunt Resistance and Quantum Efficiency Losses," *IEEE Journal of Photovoltaics*, vol. 5, no. 6, pp. 1540-1548, 2015, doi: 10.1109/JPHOTOV.2015.2459919.

[70] "Samsung 50V 20.7Ah Lithium-ion Battery Pack with 5A charger" https://www.ebikessf.com/Samsung50V20.7Ah (accessed 7 June, 2019).

[71] S. Buetow and R. Herzer, "Characterization of GaN-HEMT in cascode topology and comparison with state of the art-power devices," in *2018 IEEE 30th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 13-17 May 2018 2018, pp. 196-199, doi: 10.1109/ISPSD.2018.8393636.

[72] T. K. Gachovska and C. Gerolami, "Comparison of Si and GaN-FETs in a VAR compensation application," in *2016 IEEE Electrical Power and Energy Conference (EPEC)*, 12-14 Oct. 2016 2016, pp. 1-3, doi: 10.1109/EPEC.2016.7771747.

[73] EPC. "EPC2034 - Enhancement Mode Power Transistor." https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2034.aspx (accessed 2 Jan, 2021).

[74] EPC. "EPC2050: 350 V, 26 A Enhancement-Mode GaN Power Transistor." https://epc-co.com/epc/Products/eGaNFETsandICs/EPC2050.aspx (accessed 2 Jan, 2021).

[75] T. Instrument. "LMG3410-HB-EVM." https://www.ti.com/tool/LMG3410-HB-EVM (accessed 20 Nov, 2020).

[76] G. Systems. "GS66506T 650V Enhancement Mode GaN Transistor." https://gansystems.com/gan-transistors/gs66506t/ (accessed 11 June, 2019).

[77] Y. Karimi, H. Oraee, and J. M. Guerrero, "Decentralized Method for Load Sharing and Power Management in a Hybrid Single/Three-Phase-Islanded Microgrid Consisting of Hybrid Source PV/Battery Units," *IEEE Transactions on Power Electronics,* vol. 32, no. 8, pp. 6135-6144, 2017, doi: 10.1109/TPEL.2016.2620258.

[78] B. Subudhi and R. Pradhan, "A Comparative Study on Maximum Power Point Tracking Techniques for Photovoltaic Power Systems," *IEEE Transactions on Sustainable Energy,* vol. 4, no. 1, pp. 89-98, 2013, doi: 10.1109/TSTE.2012.2202294.

[79] M. A. S. Masoum, H. Dehbonei, and E. F. Fuchs, "Theoretical and experimental analyses of photovoltaic systems with voltageand current-based maximum power-point tracking," *IEEE Transactions on Energy Conversion,* vol. 17, no. 4, pp. 514-522, 2002, doi: 10.1109/TEC.2002.805205.

[80] B. Subudhi and R. Pradhan, "Characteristics evaluation and parameter extraction of a solar array based on experimental analysis," in *2011 IEEE Ninth International Conference on Power Electronics and Drive Systems*, 5-8 Dec. 2011 2011, pp. 340-344, doi: 10.1109/PEDS.2011.6147269.

[81] J. Xu, C. C. Mi, B. Cao, J. Deng, Z. Chen, and S. Li, "The State of Charge Estimation of Lithium-Ion Batteries Based on a Proportional-Integral Observer," *IEEE Transactions on Vehicular Technology,* vol. 63, no. 4, pp. 1614-1621, 2014, doi: 10.1109/TVT.2013.2287375.

[82] M. A. Hannan, M. S. H. Lipu, A. Hussain, and A. Mohamed, "A review of lithium-ion battery state of charge estimation and management system in electric vehicle applications: Challenges and recommendations," *Renewable and Sustainable Energy Reviews,* vol. 78, pp. 834-854, 2017/10/01/ 2017, doi: https://doi.org/10.1016/j.rser.2017.05.001.

[83] R. Xiong, J. Cao, Q. Yu, H. He, and F. Sun, "Critical Review on the Battery State of Charge Estimation Methods for Electric Vehicles," *IEEE Access,* vol. 6, pp. 1832-1843, 2018, doi: 10.1109/ACCESS.2017.2780258.

[84] M. Rezkallah, A. Hamadi, A. Chandra, and B. Singh, "Real-Time HIL Implementation of Sliding Mode Control for Standalone System Based on PV Array Without Using Dumpload," *IEEE Transactions on Sustainable Energy,* vol. 6, no. 4, pp. 1389-1398, 2015, doi: 10.1109/TSTE.2015.2436333.

[85] O. Akeyo, V. Rallabandi, N. Jewell, and D. M. Ionel, "Improving the Capacity Factor and Stability of Multi-MW Grid Connected PV Systems with Results from a 1MW/2MWh Battery Demonstrator," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 23-27 Sept. 2018 2018, pp. 2504-2509, doi: 10.1109/ECCE.2018.8558253.

[86] S. Moury and J. Lam, "A Soft-Switched Power Module With Integrated Battery Interface for Photovoltaic-Battery Power Architecture," *IEEE Journal of Emerging and Selected Topics in Power Electronics,* vol. 8, no. 3, pp. 3090-3110, 2020, doi: 10.1109/JESTPE.2019.2916733.

[87] APsystems. "APsystems YC1000-3-208 Microinverter." https://usa.apsystems.com/portfolio-item/apsystems-yc1000-3-208/ (accessed 21 Nov, 2019).

[88] S. Sathyan, H. M. Suryawanshi, M. S. Ballal, and A. B. Shitole, "Soft-Switching DC–DC Converter for Distributed Energy Sources With High Step-Up Voltage Capability," *IEEE Transactions on Industrial Electronics,* vol. 62, no. 11, pp. 7039-7050, 2015, doi: 10.1109/TIE.2015.2448515.

[89] W. Chen and X. Ruan, "Zero-Voltage-Switching PWM Hybrid Full-Bridge Three-Level Converter With Secondary-Voltage Clamping Scheme," *IEEE Transactions on Industrial Electronics,* vol. 55, no. 2, pp. 644-654, 2008, doi: 10.1109/TIE.2007.907676.

[90] N. Mohan, Tore M. Undeland, and William P. Robbins, *Power electronics: converters, applications, and design*. John wiley & sons, 2003.

[91] G. L. Plett, *Battery management systems Volume I: Battery modeling. .* Artech House, 2015.

[92] B. Satchidanandan and P. R. Kumar, "On the Design of Security-Guaranteeing Dynamic Watermarks," *IEEE Control Systems Letters,* vol. 4, no. 2, pp. 307-312, 2020, doi: 10.1109/LCSYS.2019.2925278.

[93] W.-H. K. a. P. R. K. Jaewon Kim, "Cyber-security with dynamic watermarking for process control systems," presented at the AIChE Annual Meeting, 2019.

[94] J. Ramos-Ruiz *et al.*, "An Active Detection Scheme for Cyber Attacks on Grid-tied PV Systems," in *2020 IEEE CyberPELS (CyberPELS)*, 13-13 Oct. 2020 2020, pp. 1-6, doi: 10.1109/CyberPELS49534.2020.9311539.

[95] F. Li *et al.*, "Review of Real-time Simulation of Power Electronics," *Journal of Modern Power Systems and Clean Energy,* vol. 8, no. 4, pp. 796-808, 2020, doi: 10.35833/MPCE.2018.000560.

[96] A. Perić, H. Pauković, M. Miletić, and V. Šunde, "Development of voltage source converter using HiL simulation system," in *2019 42nd International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO)*, 20-24 May 2019 2019, pp. 168-173, doi: 10.23919/MIPRO.2019.8757020.

[97] C. S. Edrington, M. Steurer, J. Langston, T. El-Mezyani, and K. Schoder, "Role of Power Hardware in the Loop in Modeling and Simulation for Experimentation in Power and Energy Systems," *Proceedings of the IEEE,* vol. 103, no. 12, pp. 2401-2409, 2015, doi: 10.1109/JPROC.2015.2460676.

[98] G. Li, D. Zhang, Y. Xin, S. Jiang, W. Wang, and J. Du, "Design of MMC hardware-in-the-loop platform and controller test scheme," *CPSS Transactions on Power Electronics and Applications,* vol. 4, no. 2, pp. 143-151, 2019, doi: 10.24295/CPSSTPEA.2019.00014.

[99] O. Goñi, A. Sanchez, E. Todorovich, and A. d. Castro, "Resolution Analysis of Switching Converter Models for Hardware-in-the-Loop," *IEEE Transactions on Industrial Informatics,* vol. 10, no. 2, pp. 1162-1170, 2014, doi: 10.1109/TII.2013.2294327.

[100] J. Allmeling and N. Felderer, "Sub-cycle average models with integrated diodes for real-time simulation of power converters," in *2017 IEEE Southern Power Electronics Conference (SPEC)*, 4-7 Dec. 2017 2017, pp. 1-6, doi: 10.1109/SPEC.2017.8333566.