HIGH VOLTAGE AND HIGH CURRENT CMOS ACTIVE RECTIFIER WITH DIGITAL OFFSET COMPENSATION FOR IMPLANTABLE DEVICES

A Thesis

by

VIVEK REDDY NANDYALA

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Chair of Committee,	Aydin I. Karsilayan
Co-Chair of Committee,	Jose Silva-Martinez
Committee Members,	Gwan Choi
	Duncan M. Hank Walker
Head of Department,	Miroslav M. Begovic

December 2020

Major Subject: Electrical Engineering

ABSTRACT

A CMOS active rectifier for wirelessly powered implantable devices operating at a frequency of 100-500kHz, input voltage of 5-18V and a load current of 100mA-200mA is presented. The diodes used in the conventional rectifier are replaced by PMOS and NMOS transistors, which help in obtaining high power conversion efficiency and voltage conversion efficiency. The PMOS and NMOS transistors used for the rectification are high voltage devices 18v/5v (V_{DS}/ V_{GS}). Dedicated switching mechanisms are used for protection of the devices at higher voltages.

The NMOS transistors are operated as active diodes, using a high voltage differential common gate comparator with adjustable offset. The proposed comparators are implemented with a dynamic switched current offset mechanism to reduce the reverse current and a NOR gate based SR-latch is used to prevent the multiple pulsing. A calibration circuit is proposed to detect the reverse current present in the circuit and dynamically vary the amount of current offset added to the comparator to reduce the reverse current. ONC18TG18 CMOS technology, a 180nm process by ON semiconductor is used for the design of the rectifier. A peak PCE of 92% and VCE of 93.2% is obtained for a 50Ω loading.

ACKNOWLEDGEMENTS

I would like to thank Professor Aydin I. Karsilayan for providing the opportunity to extend my work at the internship into thesis. I would like to thank for his encouragement, support and guidance during the development of the thesis.

I would like to thank Vighnesh Das and David Genzer of Micro Systems Engineering Inc. / Biotronik for their support during my internship and also for encouraging and supporting the idea to extend my work at the internship into a thesis. I would like to thank Ismael Molina and Susan Garcia of Micro Systems Engineering Inc. / Biotronik for their support during my internship.

I would like to thank Dr. Jose Silva Martinez, Dr. Duncan Hank Walker and Dr. Gwan Choi for being the part of the committee. I would like to thank Dr. Sunil Khatri for accepting to be a substitute for the thesis defense. I would like to thank them for their guidance and reviewing the manuscript. Their time, encouragement and advice are greatly appreciated.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supported by the thesis committee consisting of Professors Aydin I. Karsilayan, Jose Silva Martinez, Gwan Choi of the Department of Electrical and Computer Engineering and Professor Duncan Hank Walker of the Department of Computer Science and Engineering.

This work is also supported by Vighnesh Das, David Genzer of Micro Systems Engineering Inc. / Biotronik.

Funding Sources

This study is supported by ECEN Summer Research Fellowship.

NOMENCLATURE

HV	High Voltage
LV	Low Voltage
PCE	Power Conversion Efficiency
PVT	Process Voltage Temperature
PDK	Process Design Kit
VCE	Voltage Conversion Efficiency
WPT	Wireless Power Transfer

TABLE OF CONTENTS

Page

LIST OF FIGURES

Page

LIST OF TABLES

1. INTRODUCTION

1.1. Motivation

Biomedical implants are devices that are placed inside the human body which are predominantly intended to replace the missing body parts or support a damaged body part or enhance an existing biological structure. They are manmade devices and are made from skin, bone, plastic, steel and other ceramic materials. The implants are placed permanently in the human body or removed when they are no longer needed. These implants come with surgical risks during the placement or removal.

The electrical implants include pacemakers, neuro stimulators, implantable sensors, etc. Implanted devices with functions such as neural stimulation and/or recording usually need power in the range of milli-Watt or higher [1]. Limitations are present on the size of the implants as they are placed inside the human body. The size constraints on the implants limit the use of a battery with a higher capacity. Hence conventional implants need frequent battery replacements. To avoid battery replacements, wireless power transfer (WPT) and energy harvesting techniques are used [2], which could deliver power in milli-Watt range.

Inductive coupling is widely used in WPT, particularly in the near field region. WPT is a key technology to recharge the medical devices. The architecture for the inductively coupled system [3], is shown in Figure 1.1. Inductive coil L_1 on the primary side is connected to an input source, couples the AC power to the coil L_2 on the secondary side.

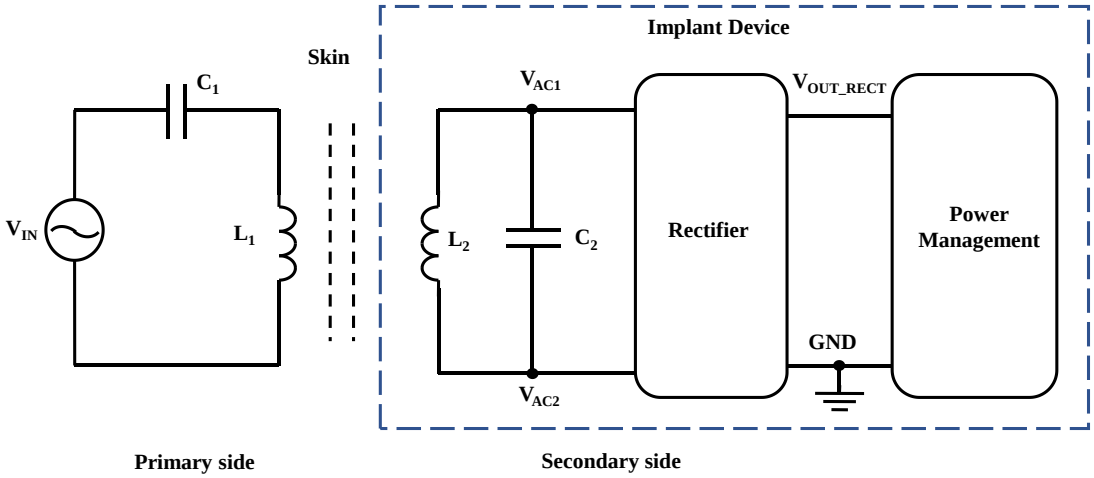


Figure 1.1 Inductive coupling based WPT for implantable devices

The typical frequency of operation for WPT in implants is 13.56MHz. The received power depends on the coupling coefficient between the primary (external) coil and the secondary (internal) coil, orientation of coils, distance between the primary and secondary coil, i.e., how deep the implants are placed below the skin tissue.

As the power transfer in WPT is AC in nature, the voltage obtained on the secondary side of the coil is also AC. A rectifier circuit is required to convert this AC voltage into a DC voltage. The rectifier circuit should be capable of handling a wide range of voltages [3], [4], [5] load currents and frequency. The power conversion efficiency (PCE) and voltage conversion efficiency (VCE) are used as figures of merit (FOM) to determine the effectiveness of the rectifier. The PCE and VCE are defined as

$$\mathrm{PCE} = \frac{\text{Output Power}}{\text{Input Power}} 100\% \tag{1.1}$$

$$\mathrm{VCE} = \frac{V_{\mathrm{OUT\_RECT}}}{V_{\mathrm{IN\_PEAK}}} 100\% \tag{1.2}$$

where V_{OUT_RECT}, V_{IN_PEAK} are the rectified output voltage and the amplitude of input AC signal, respectively.

1.2. Thesis Organization

Chapter 2 provides an insight on CMOS active rectifier working, its advantages and disadvantages over the traditional, passive and hybrid rectifier.

Chapter 3 presents a CMOS active rectifier with a current mode switched-offset comparator in ONC18TG18 180nm CMOS for wireless power transfer. A calibration circuit is proposed which introduces the required offset in the comparator for obtaining the maximum possible PCE.

This thesis is concluded in Chapter 4 which summarizes the research work.

2. RECTIFIER

The AC power obtained on the secondary side of WPT is typically used for recharging the battery of implant and also as a secondary source for the internal circuitry of the implant. To recharge the battery the voltage must be in DC form.

2.1. Passive Rectifier

In a passive rectifier, rectification is performed using traditional diodes. The four diodes are connected in a bridge configuration as shown in Figure 2.1 to convert the AC signal into a rectified DC output voltage. During the rectification, in each phase a pair of diodes D_1 and D_4 or D_2 and D_3 are responsible for conducting the current. These diode pairs operate in a forward bias condition in one phase and reverse bias condition in opposite phase.

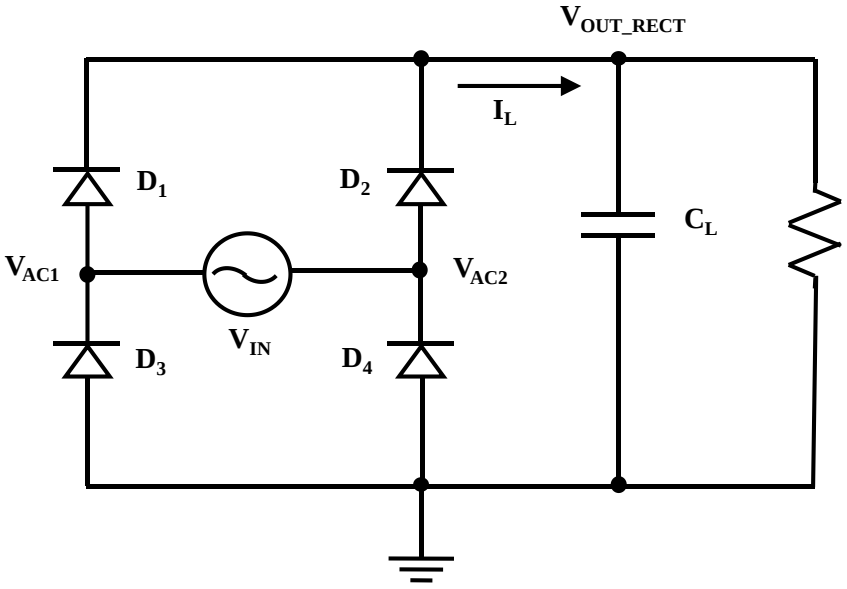


Figure 2.1 Schematic of passive rectifier

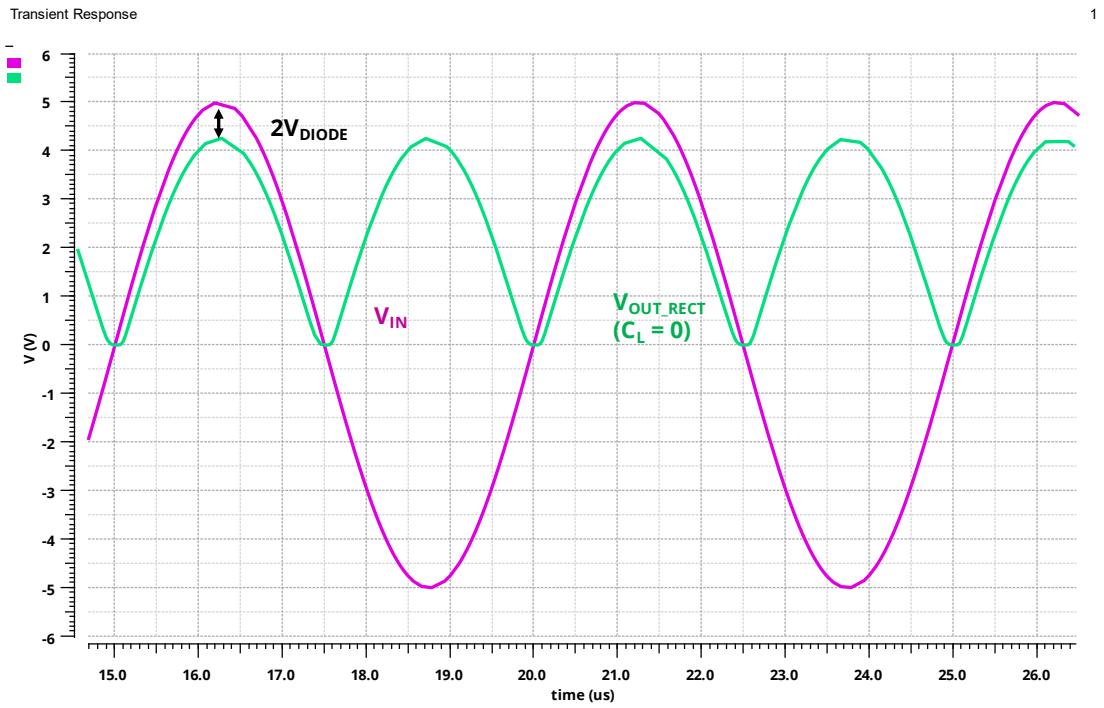


Figure 2.2 Transient simulation results of passive rectifier

Table 2.1 Specifications of typical passive rectifier

Voltage Range	0-30V
Maximum current	0.9A
Voltage drop	0.7-0.8V
Power Conversion Efficiency (PCE)	81%

The voltage drop observed in the passive rectifier is $2V_{DIODE}$ where V_{DIODE} is the forward voltage drop across diode. as seen in the Figure 2.2. The typical diodes have a forward voltage drop of 0.3-0.7V. Hence the effective voltage drop observed in the above rectifier is 0.6-1.4V. The forward voltage drop decreases the VCE and PCE and prevents

their application for lower input voltages. Another drawback of a passive rectifier is the fabrication of diodes and its integration into the existing system. The Table 2.1 depicts the specifications of a typical passive rectifier where the PCE observed is 81%.

2.2. Hybrid Rectifier

A pair of diodes are replaced by a pair of transistors in a hybrid rectifier. The NMOS transistors used are operated in a cross-coupled fashion to act as switches as shown in the Figure 2.3. The total voltage drop across the system changes from $2V_{DIODE}$ observed in the passive rectifier to $V_{DIODE} + V_{DS}$ as seen in the Figure 2.4 where V_{DS} is drain-source voltage across transistor.

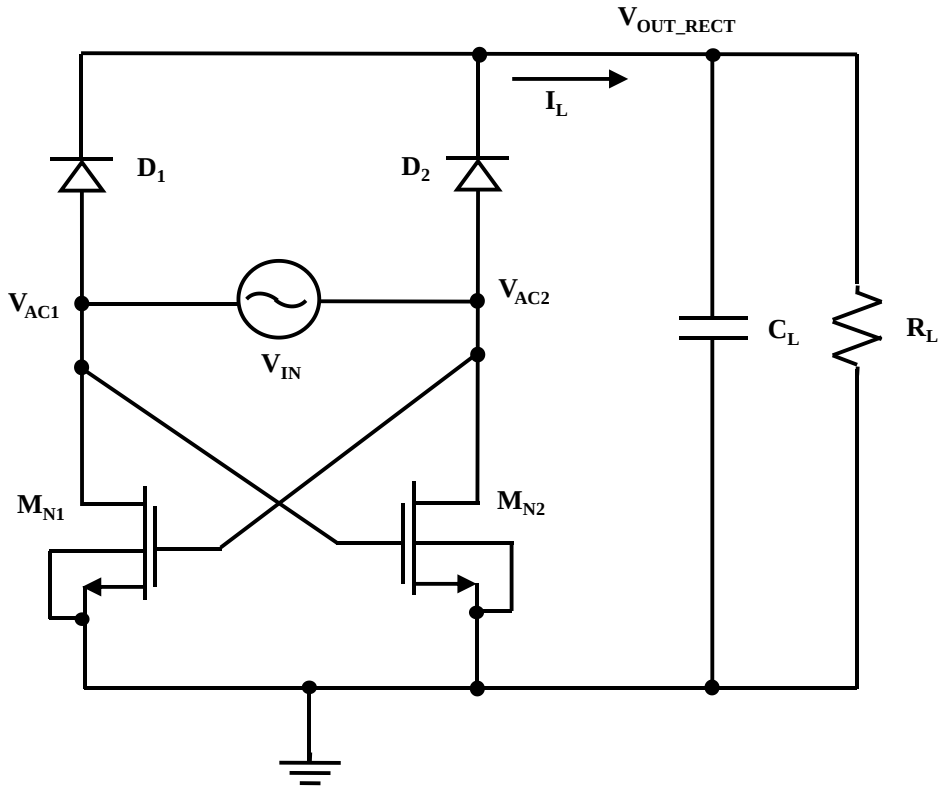


Figure 2.3 Schematic of hybrid rectifier

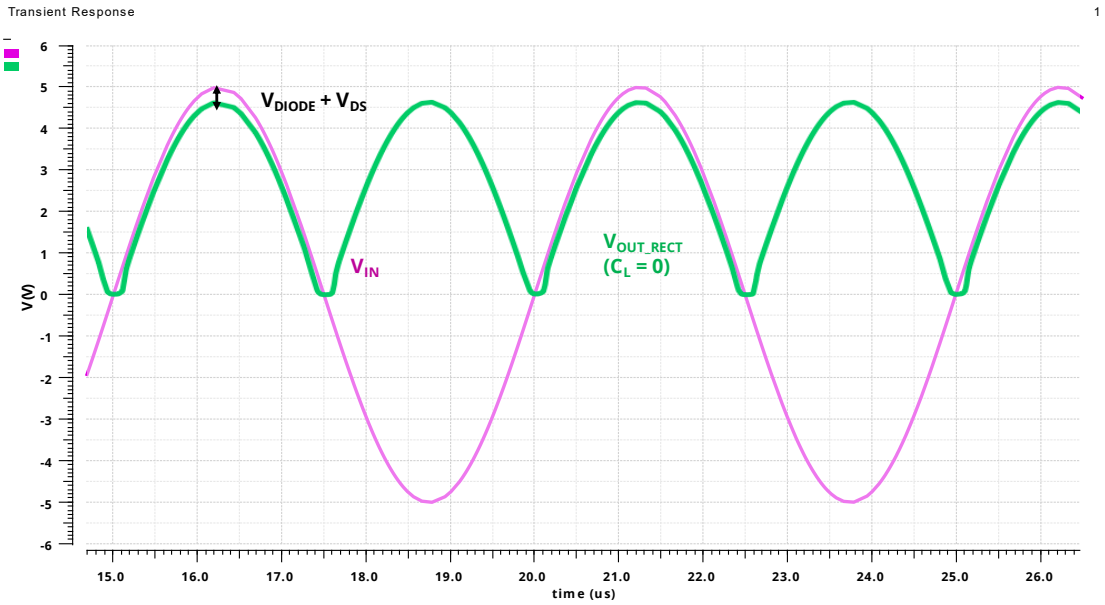


Figure 2.4 Transient simulation results of hybrid rectifier

Table 2.2 Specifications of hybrid rectifier

Voltage Range	0-20V
Maximum current	3.2A
Voltage drop	0.473V
Power Conversion Efficiency (PCE)	94%

The voltage drop across the MOSFETs can be reduced by increasing the width of the devices. The introduction of MOSFETs helps in reducing the voltage drop and increase the VCE and PCE of the system. In Figure 2.3, PMOS transistors can also be used in place of the NMOS transistors. As the mobility of the PMOS transistors is lower than the NMOS transistors, to achieve the required voltage drop, the size of the PMOS transistors required

would be higher than that of NMOS transistors. This increase in size of the transistors further increases the size of the chip. The Table 2.2 shows the specifications of a typical hybrid rectifier where the PCE observed is 94%. The major drawback of this rectifier is the fabrication of diodes and its integration into an existing system.

2.3. Active Rectifier

In an active rectifier, the diodes are replaced with active switching elements. Power MOSFETs are ideal active elements used for synchronous rectification as they have a very low on resistance, R_{DS} that may be as low as a few tens of mΩ or less. Active rectifiers are also known as synchronous rectifiers as the switching has to occur in synchronism with the input ac signal. The elimination of diodes in the circuit reduces the complexity in fabrication, and also the voltage drop observed in conventional rectifiers. The downside to synchronous or active rectifiers is that they require a control circuit to ensure the devices turn on synchronously. This control circuit typically includes a comparator circuit and other biasing current sources.

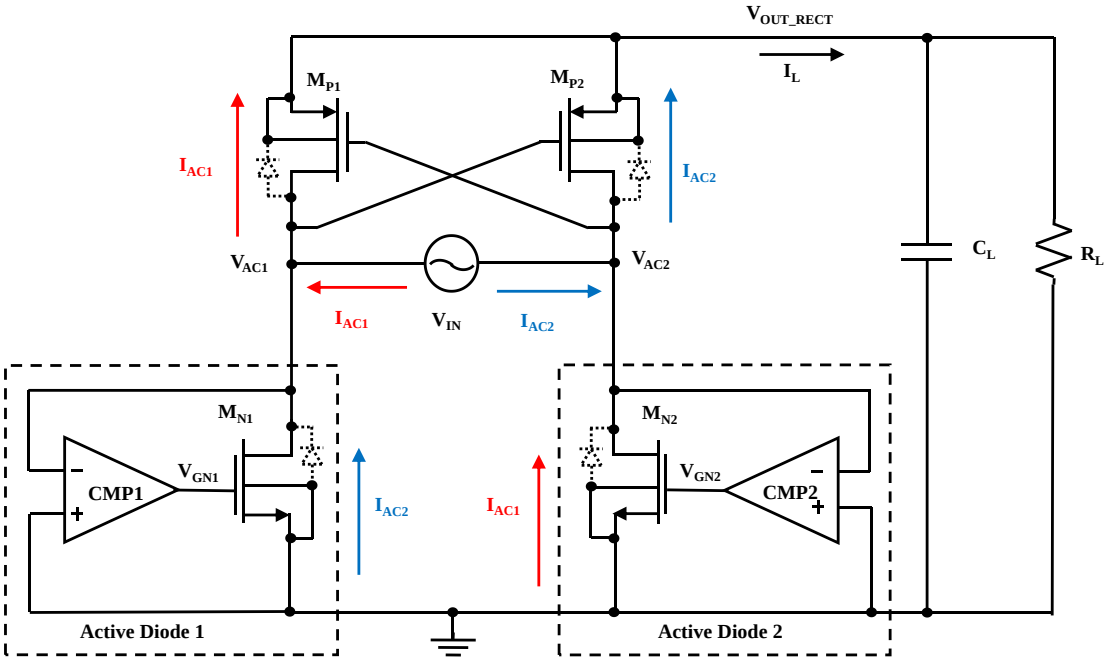


Figure 2.5 Schematic of active rectifier

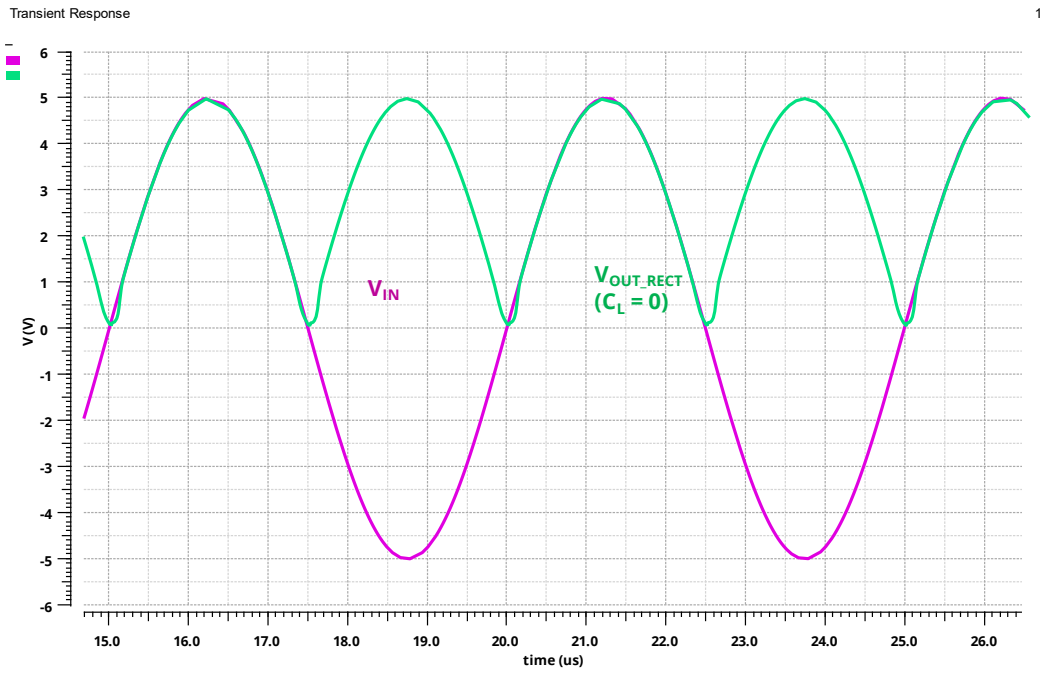


Figure 2.6 Transient simulation results of active rectifier

2.3.1. Operating Principle

An active rectifier is implemented in [3]- [4], using a pair of PMOS and NMOS transistors as shown in Figure 2.5. The PMOS transistors are connected in a cross coupled manner and the NMOS transistors along with comparators are operated as Active Diodes. The voltage drop in an active rectifier decreases from $2V_{DIODE}$ to $2V_{DS}$ as seen in Figure 2.6. To reduce the voltage drop across these transistor switches the size of the devices can be increased. The increase in size of the switches increases the gate capacitance. A buffer circuit is required to drive these switches.

The design in Figure 2.5 can be altered such that, PMOS devices along with comparator are used as active diodes and the NMOS transistors are connected in a cross coupled manner. As the size of PMOS devices are typically higher than the NMOS devices required for the same on resistance and required voltage drop, the buffer network required to drive these PMOS switches would consume more power and the higher gate capacitance increases the switching losses in the rectifier. Hence the NMOS devices are preferred over the PMOS devices to operate as active diodes.

The comparator in the above implementation of active diodes is powered up using the rectified output voltage V_{OUT_RECT}. During the initial phase when the rectified output voltage is low, the NMOS transistors are off and conduction takes place using their body diodes. The bodies of power transistors are simply connected to their sources, and the parasitic body-drain PN junction will help with the start-up process. As the output voltage increases, the control circuitry gets powered up and the NMOS switches are then controlled by the comparators. During the steady state operation care must be taken such

that the voltage drop across these switches is lower than the forward bias voltage required to turn on the body diodes, so that the conduction in steady state is through the switches and body diodes are turned off.

2.3.2. Reverse Current

The comparator and buffer network required to drive the NMOS switches introduce delay in the switching mechanism making these NMOS switches to turn on and off later. The delay observed during the turning on of the comparator would affect its conduction time. The delay during the turn off of the switches would result in reverse current in the circuit.

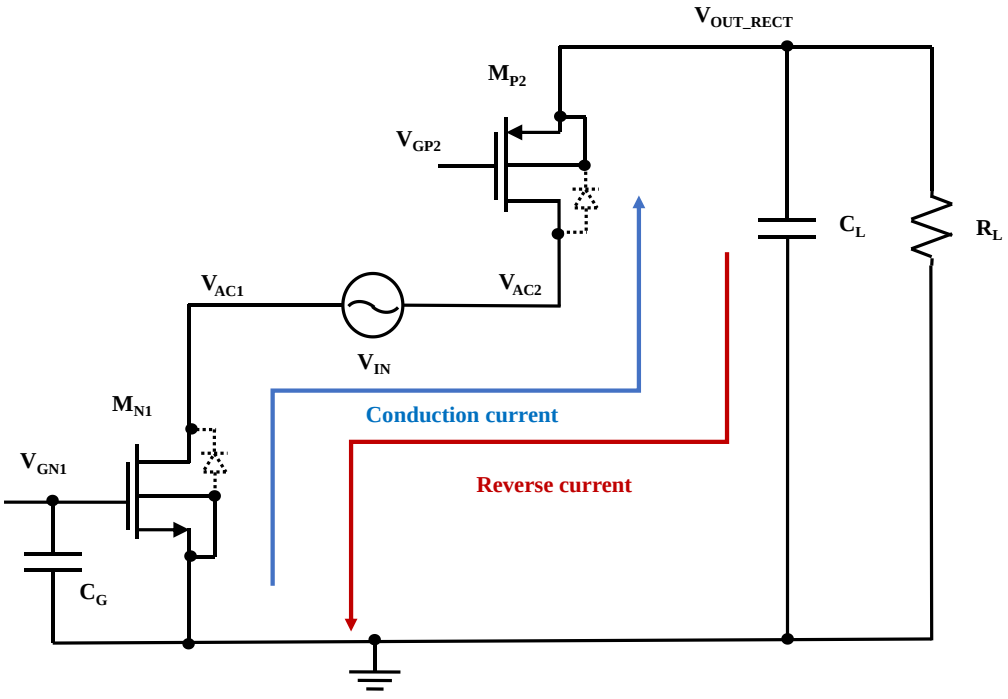


Figure 2.7 Schematic showing the reverse current

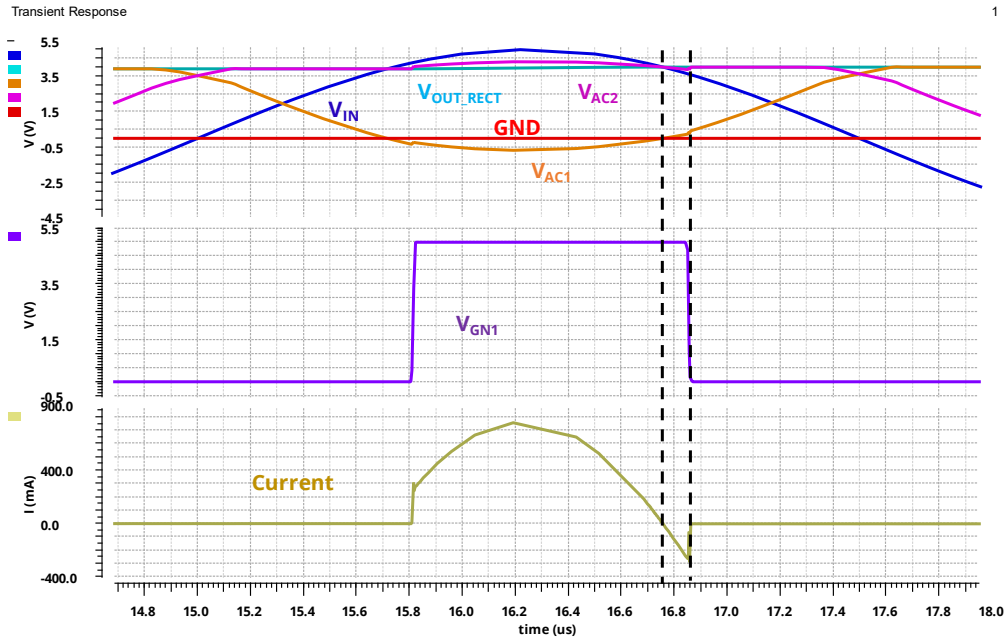


Figure 2.8 Transient simulation results of reverse current

The conduction current and reverse current have same path but flow in opposite directions as shown in the Figure 2.7. In the conduction current phase when $V_{AC2} > V_{AC1}$, when $V_{AC2} - V_{AC1} > V_{TH,}$ M_{P2} is on and when $V_{IN} > V_{OUT\_RECT}$, V_{AC1} swings below 0V i.e., $V_{AC1}<0$, the comparator turns on the transistor M_{N1} and the current flows from the input source V_{IN} to the load capacitor C_L. When $V_{IN} < V_{OUT\_RECT}$, V_{AC1} swings above 0V i.e., $V_{AC1} >0$, the comparator is turned off and no path is available for the current to flow. The delay during the falling edge makes the NMOS transistor M_{N1} to turn off later. This results in the flow of current from the load capacitor C_L into the source V_{IN} leading to reverse current in the system, which decreases the VCE and PCE of the system significantly. Figure 2.8 shows the presence of reverse current in the system because of the delay in the

comparator and buffer network. To achieve higher VCE and PCE we need to eliminate the reverse current in the system.

As the delay is inversely proportional to the supply voltage, the delay in the comparator and buffer network is more pronounced when the supply voltage is low and frequency is very high. To reduce the delay and reverse current in the rectifier different comparator architectures and offset introduction mechanisms have been proposed [3], [4], [6], [7].

2.3.3. Review of Common Gate Comparator

In [4], a CMOS active rectifier is proposed using a push-pull common gate comparator. To eliminate the reverse current in the rectifier a fixed current offset is introduced in the comparator using an unbalanced biasing scheme as seen in the Figure 2.9. The addition of an offset in the comparator turns off the M_{N1} and M_{N2} earlier so as to eliminate the reverse current in the rectifier. The addition of the fixed offset using the unbalanced biasing scheme [4], would also reduce the amount of conduction current time, which reduces the PCE of the system. The process, voltage and temperature (PVT) variations may vary the amount of reverse current present in the system, and as no offset adjustment techniques are presented, it may degrade the PCE of rectifier.

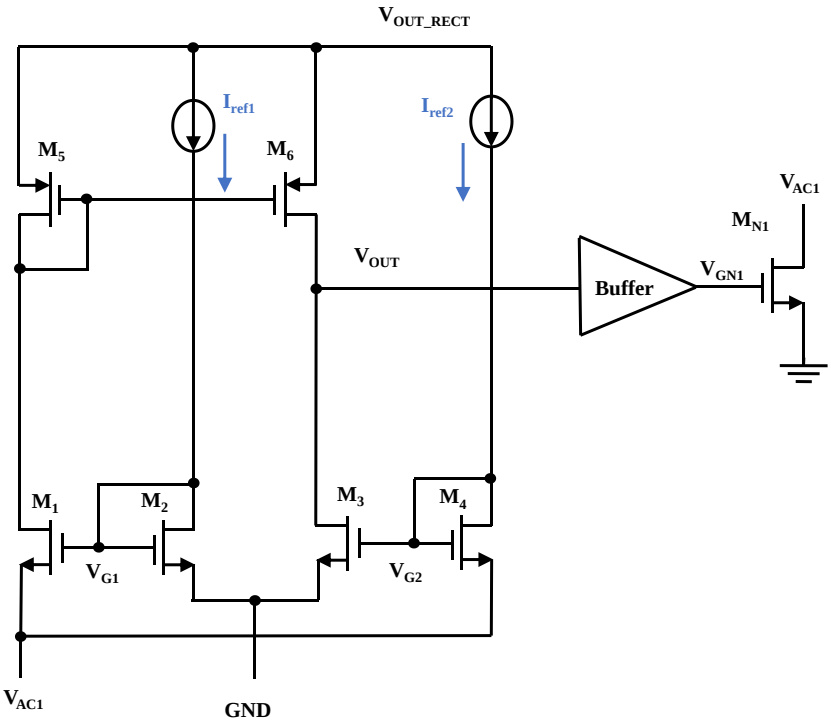


Figure 2.9 Schematic of push-pull common gate comparator with unbalanced biasing scheme

In [3], an active rectifier is proposed using a push-pull common gate comparator. A constant current offset is added to prevent the reverse current in the system using a switched offset mechanism seen in the Figure 2.10. In the switched offset mechanism, the offset is added such that it turns off the comparator earlier but not affecting the turn on phase. Figure 2.11 shows the addition of offset using the switched offset mechanism. This helps in improving the PCE of the system.

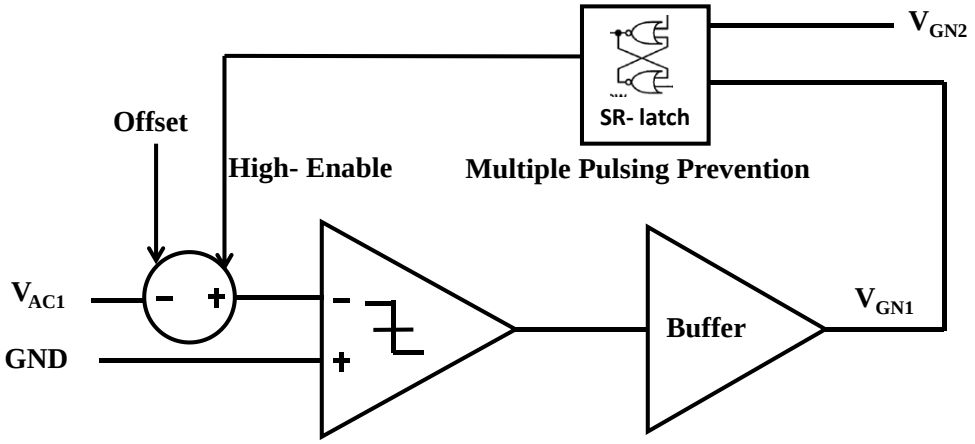


Figure 2.10 Schematic of switched offset introduction

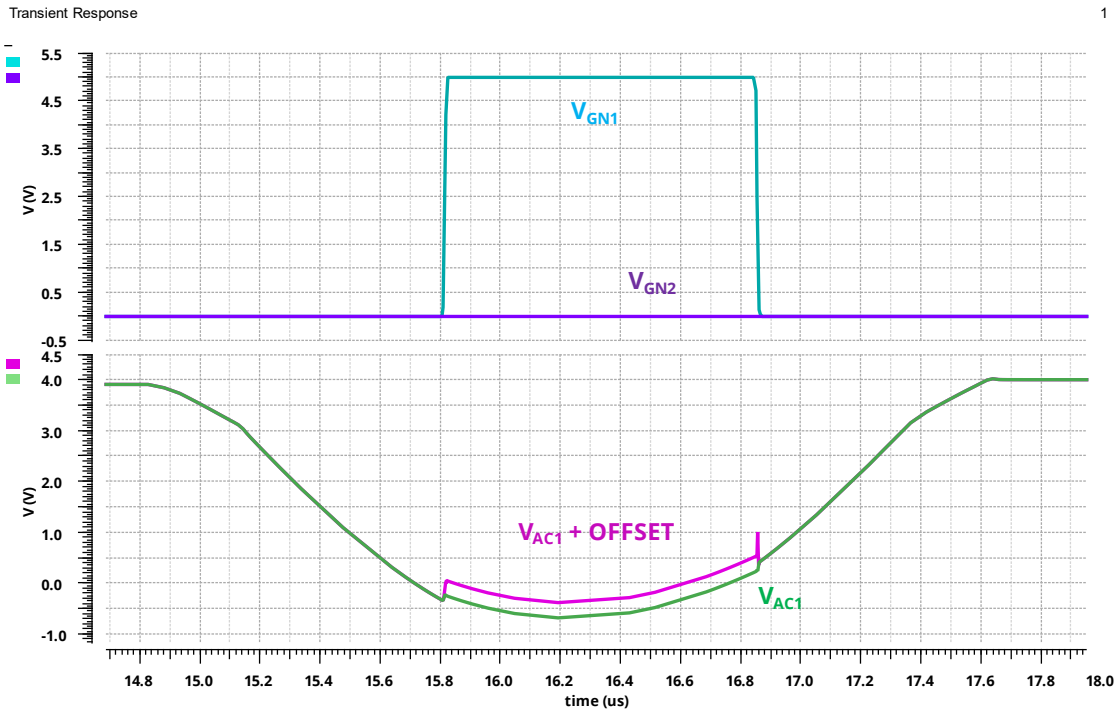


Figure 2.11 Transient simulation results of switched offset introduction

The addition of offset using the switched offset mechanism introduces the multiple pulsing problem in the rectifier as can be seen in the Figure 2.12 which degrades the PCE of the system. The multiple pulsing is removed by using a NOR gate based SR latch. Figure 2.13 shows the schematic of a push-pull common gate comparator with the switched offset introduction. No offset adjustment techniques are present, which may degrade the PCE of the system with PVT variations.

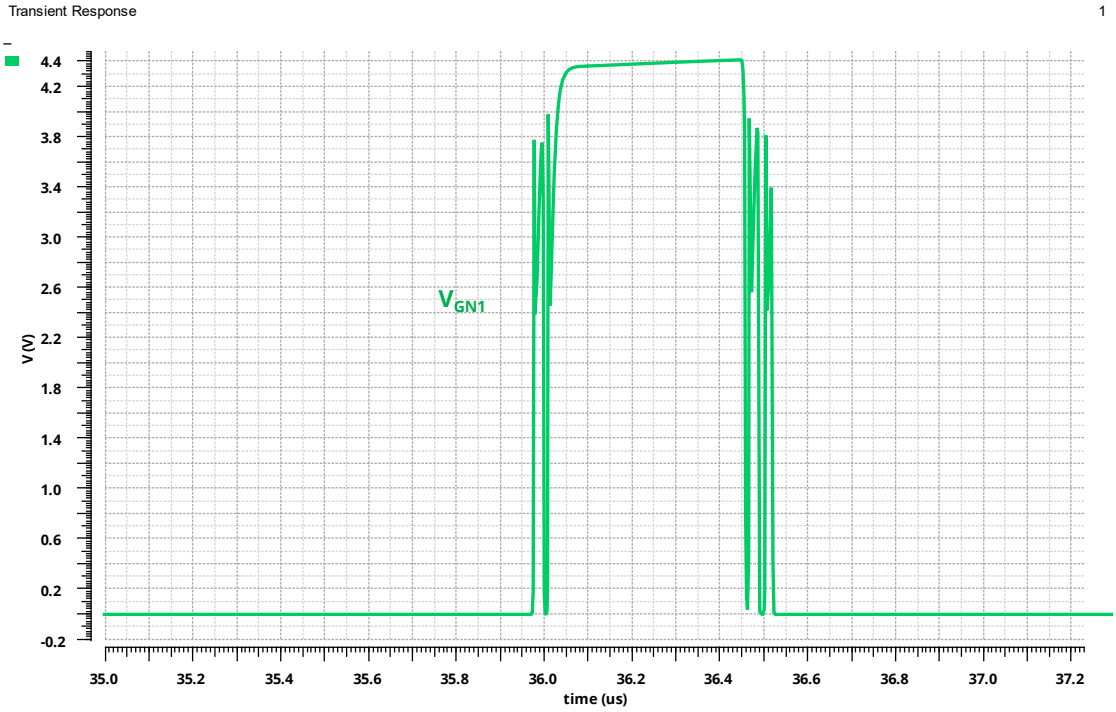


Figure 2.12 Transient simulation results of multiple pulsing in the rectifier

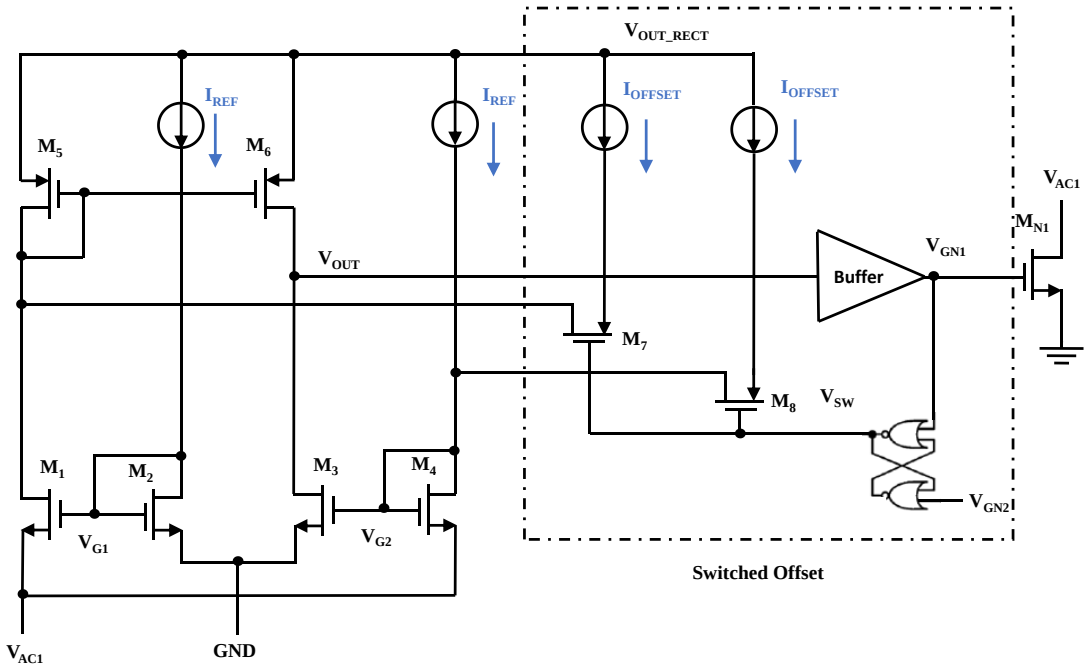


Figure 2.13 Schematic of push-pull common gate comparator with switched offset mechanism

In [7], a CMOS active rectifier is proposed. The reverse current is reduced using a voltage mode switched offset mechanism. Sampling based on-chip calibration circuit proposed adjusts the magnitude of offset voltages introduced in the comparator using a low-power dynamic logic-based switch controller. The NOR gate-based SR latch [3], is used for the prevention of multiple pulsing in the rectifier. As falling/ rising edge detectors are primarily used in the sampling process, these signals are more sensitive towards PVT variations.

3. PROPOSED ARCHITECTURE

Table 3.1 shows the specifications of the proposed CMOS active rectifier. The input voltage of the rectifier has high voltage transients up to 18V during the initial phase but later settles down to 5V. The frequency of the input voltage varies from 100-500 kHz. The load current of the rectifier is in the range of 100-200 mA. The specifications are developed in collaboration with Micro Systems Engineering Inc. / Biotronik.

Table 3.1 Target specifications of active rectifier

Parameter	Target Specifications
Frequency	100-500 kHz
Input Amplitude (V_{IN})	5V (typical) Transients up to 18V
Load Capacitor (C_L)	> 1µF
Rectified output Voltage (V_{OUT_RECT})	4.3-4.6 V
Load Current (I_L)	100mA
Power Conversion Efficiency (PCE)	> 90%

The CMOS active rectifier is designed in ON semiconductor 180nm process. The ONC18TG18 CMOS technology is used for the design of the rectifier. The technology serves as a platform for highly integrated high voltage mixed-signal process ideal for automotive, industrial and medical applications [8]. It is a low-cost industry compatible

180nm CMOS technology for manufacturing. The PDK is provided by Micro Systems Engineering Inc. / Biotronik. The Table 3.2 shows the different devices along with their characteristics that are used in the design of the active rectifier.

Table 3.2 Types of devices and their characteristics

Device Name	Maximum V_{GS} across the device	Maximum V_{DS} across the device
5v/5v device	5.5V	5.5V
18v/5v device	5.5V	19.8V
18v/18v device	19.8V	19.8V

3.1. Selection of Rectifier Switches

The PMOS and NMOS transistors in the CMOS active rectifier are operated as a switch. For high PCE and VCE during high load currents, the resistance of these switches should be reduced. The switch resistance R_{DS} is inversely proportional to the width of the transistor (W) and mobility (K) is given as

$$R_{DS} = \frac{1}{K\frac{W}{L}(V_{GS} - V_{TH})} \tag{3.1}$$

Figure 3.1 shows the schematic of the CMOS active rectifier, where the NMOS are operated as active diodes using ideal comparators and a load of 50Ω and a load capacitor of 1µF is used.

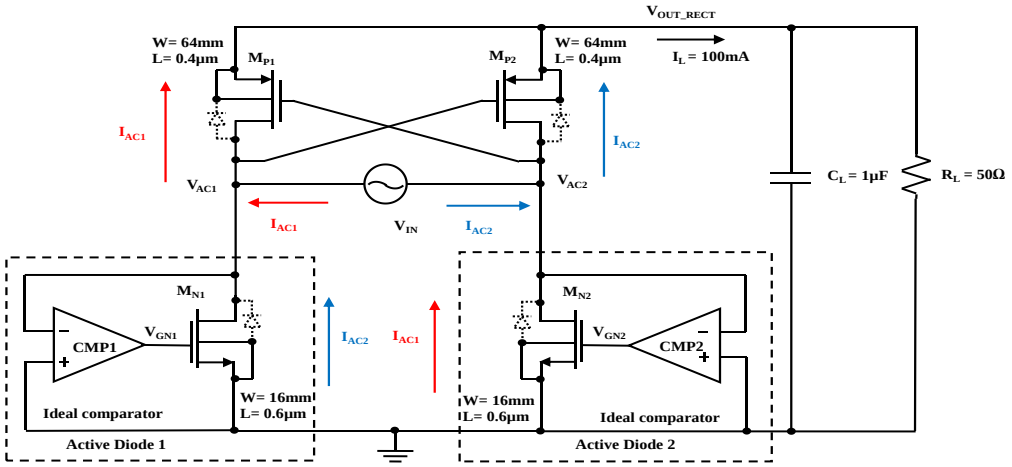
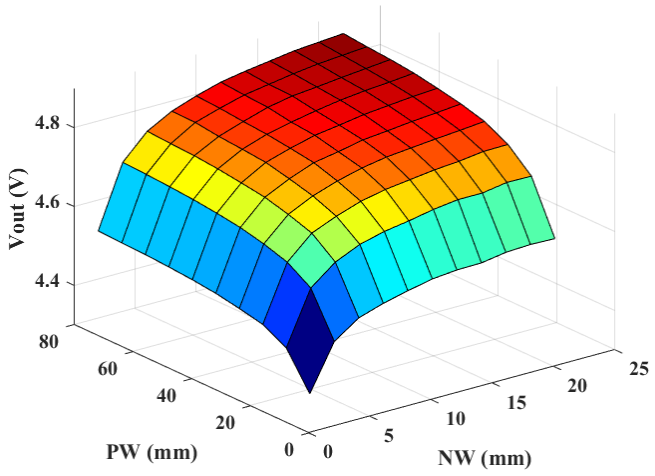
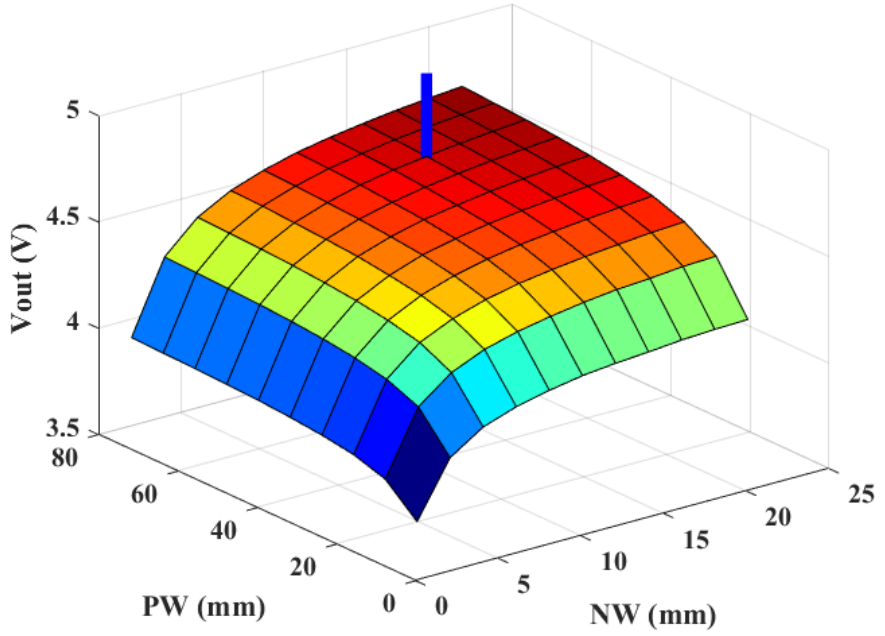


Figure 3.1 Schematic of active rectifier with ideal comparators

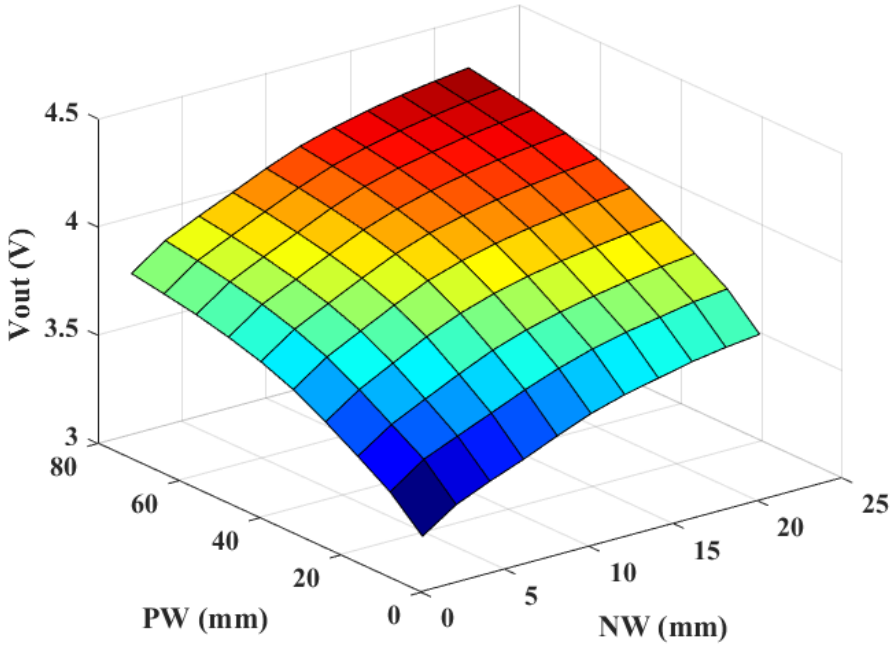


(a)

Figure 3.2 Rectified output voltage vs size of switches (a) 5v/5v devices and (b) 18v/5v devices and (c) 18v/18v devices

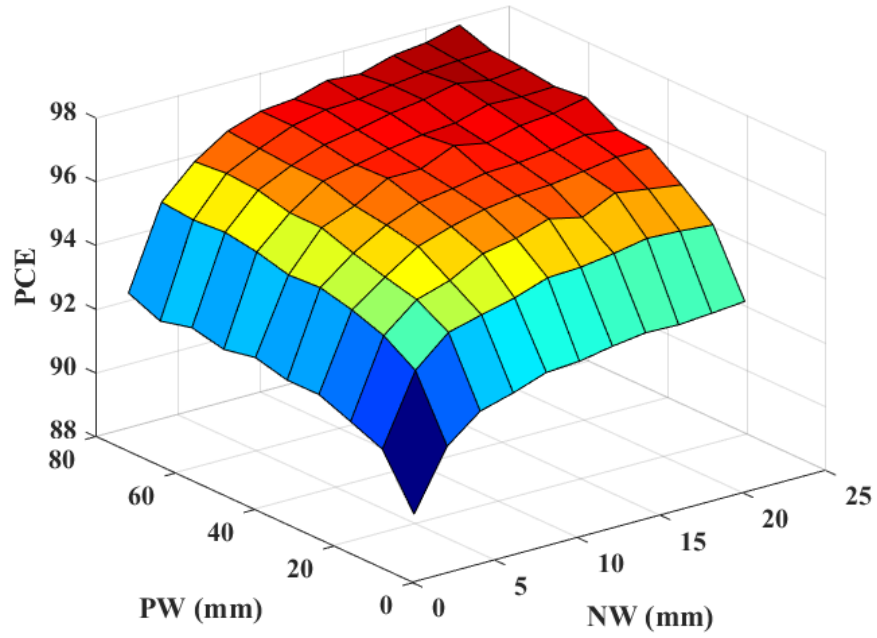


(b)

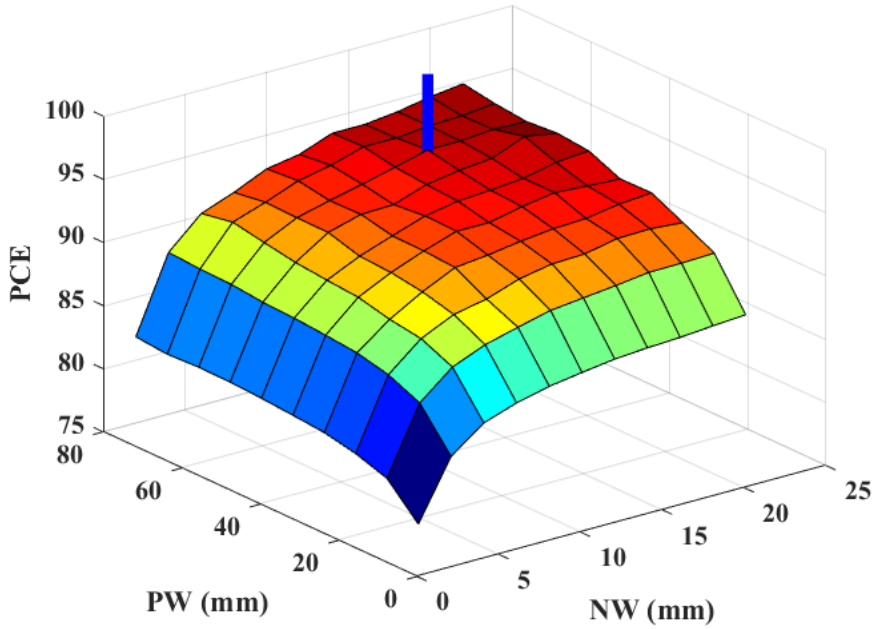


(c)

Figure 3.2 Continued

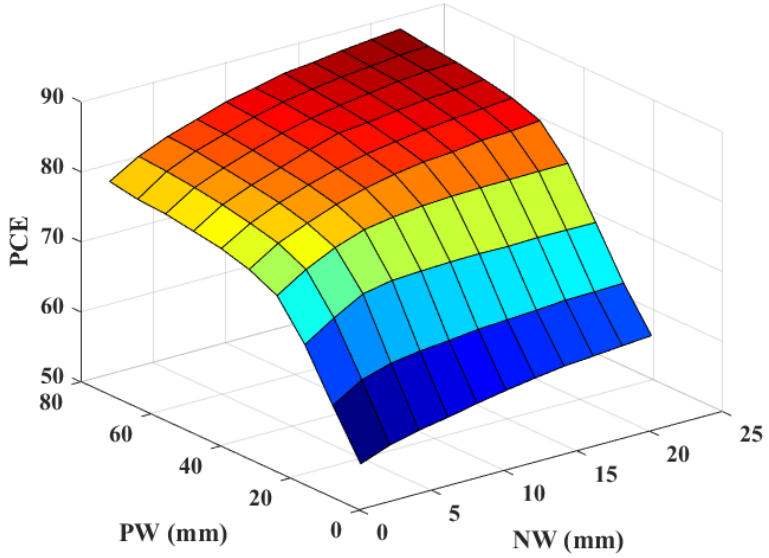


(a)



(b)

Figure 3.3 PCE vs size of switches for (a) 5v/5v devices and (b) 18v/5v devices and (c) 18v/18v devices



(c)

Figure 3.3 Continued

We observe that from the Figure 3.2 and 3.3, the PCE and the rectified output voltage increases as we increase the size of the PMOS and NMOS switches. The PCE and rectified output voltage obtained is highest in case of 5v/5v devices because of their higher mobility and the lowest in case of 18v/18v devices. But as the input transients can go up to 18V, these 5v/5v devices cannot be used. The 18v/5v devices helps in obtaining the required PCE and VCE and can also withstand the initial transients.

Table 3.3 Final switch sizes

Parameter	PMOS switch	NMOS switch
width of gate	100µ	50µ
number of gates	640	320
multiplier	1	1
length of gate	0.4 µ	0.6 µ

Table 3.4 PCE and V_{OUT_RECT} across corners with ideal comparators

Corners	V_{OUT_RECT} (v)	PCE
Typical_37C	4.646	93.37
Fast_-10C	4.711	95.53
Typical_-10C	4.67	94.7
Slow_-10C	4.611	93.53
Typical_ 65C	4.619	93.96
Slow_65C	4.585	93.37
Fast_65C	4.651	94.5
Slow_37C	4.614	93.87
Fast_37C	4.675	94.91

Table 3.3 shows the final size of the switches used in the design of the active rectifier. The width of PMOS and NMOS switches used are 64mm and 16mm, respectively. Table 3.4 shows the PCE and V_{OUT_RECT} obtained for the above-mentioned sizes across different corners. As the rectifier is designed for an implant, the temperature variation across which it is operated is from -10C to 65C with 37C being the nominal operating point temperature. The variation in PCE observed across the different corners is around 2.2%.

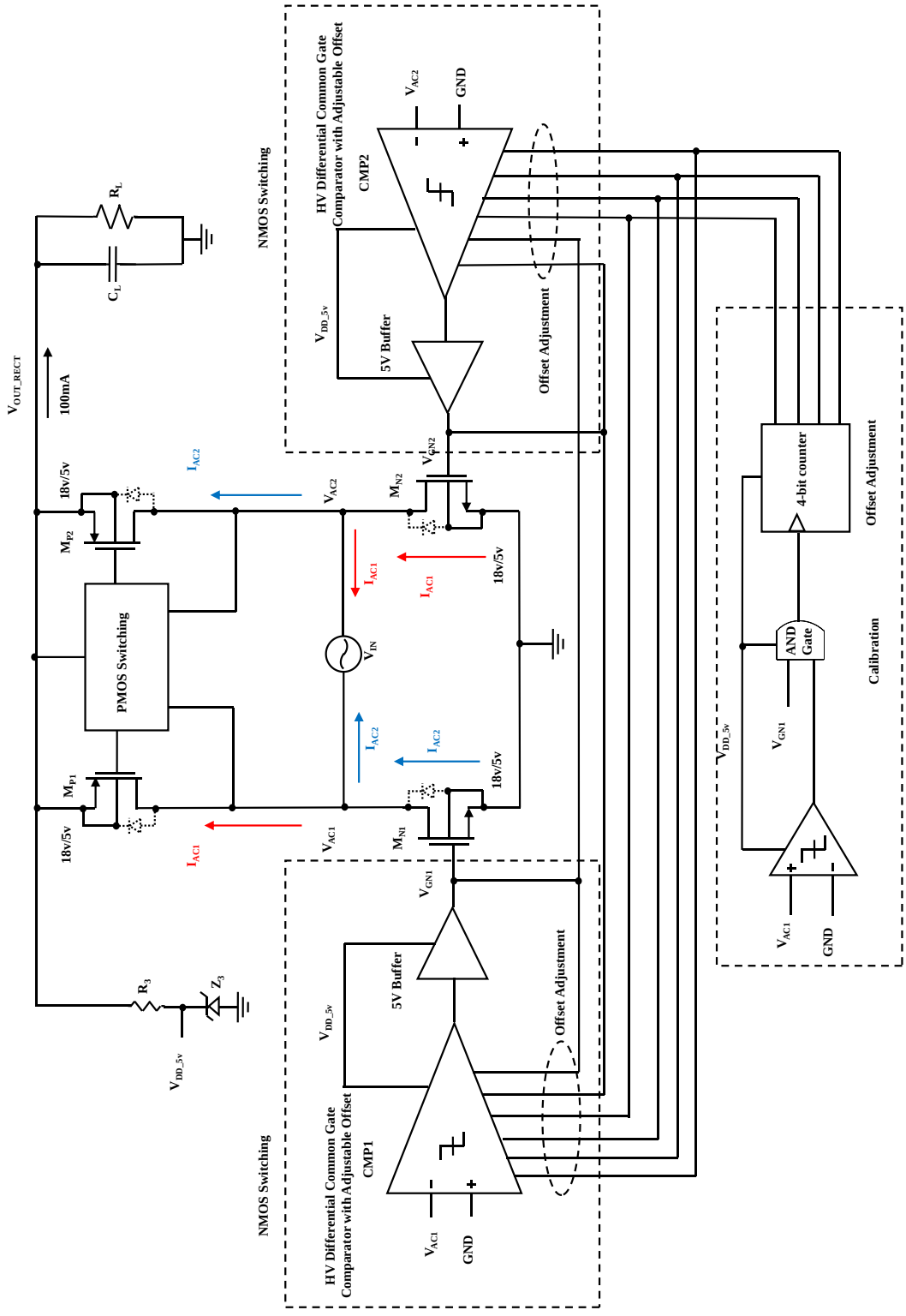


Figure 3.4 Schematic of proposed architecture

Figure 3.4 shows the proposed architecture of the active rectifier. It includes PMOS switching, NMOS switching and calibration blocks. The NMOS switching includes the HV differential common gate comparator with adjustable offset and the buffer network. The Zener Z_3 and Resistor R_3 network generates the supply voltage V_{DD_5V} required to power the NMOS switching and Calibration blocks. The input voltages higher than 5V are considered as high voltage (HV) domain and the voltages lower than 5V are considered as low voltage (LV) domain.

3.2. PMOS Switching

The PMOS switches are operated such that the source-gate potential across the 18v/5v devices is always lower than 5.5V, the breakdown voltage of the 18v/5v device as shown in Figure 3.5. When $V_{AC1} > V_{AC2}$, the gate voltage V_{GP1} is connected to the output of the Zener Z_1. In HV domain when the input voltage is higher than 5V, the Zener operates in reverse bias condition and the voltage observed across the Zener is its breakdown voltage, which is less than 5.5V. When the input voltage is in LV domain, the Zener is turned off and the voltage across the Zener is rectified output voltage V_{OUT_RECT}. During the other half cycle when $V_{AC2} > V_{AC1}$, the gate voltage V_{GP1} is connected to $V_{AC2,}$ and the PMOS is made to operate in cross coupled manner which helps in turning off the switch. The HV AC comparator is responsible for switching the voltages at the gate of PMOS switches.

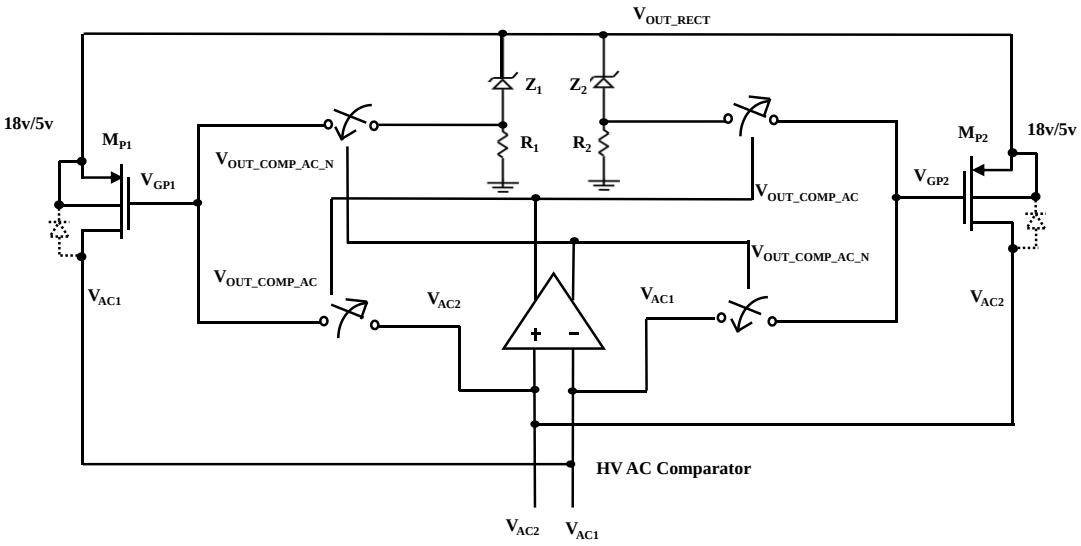


Figure 3.5 Schematic of PMOS switching

3.2.1. HV AC comparator

A differential amplifier in open loop configuration followed by a chain of inverters are used in the comparator as shown in Figure 3.6. When the input $V_{IN} \approx 0$, we have the signals V_{AC1} and V_{AC2} closer to the rectified output voltage V_{OUT_RECT}. The potential divider using the resistors R_1, R_2, R_3 and R_4 helps in to reducing the voltages V_{AC1} and V_{AC2} into the common mode operating region of the amplifier which helps in reducing the delay of the comparator.

The NMOS input transistors of the differential amplifier are 18v/18v devices as input can have voltage swing as high as 18V. The buffer network consisting of chain of inverters helps in generating rail-to-rail signals and better drivability. Figure 3.7 shows the transient simulations of the HV AC comparator.

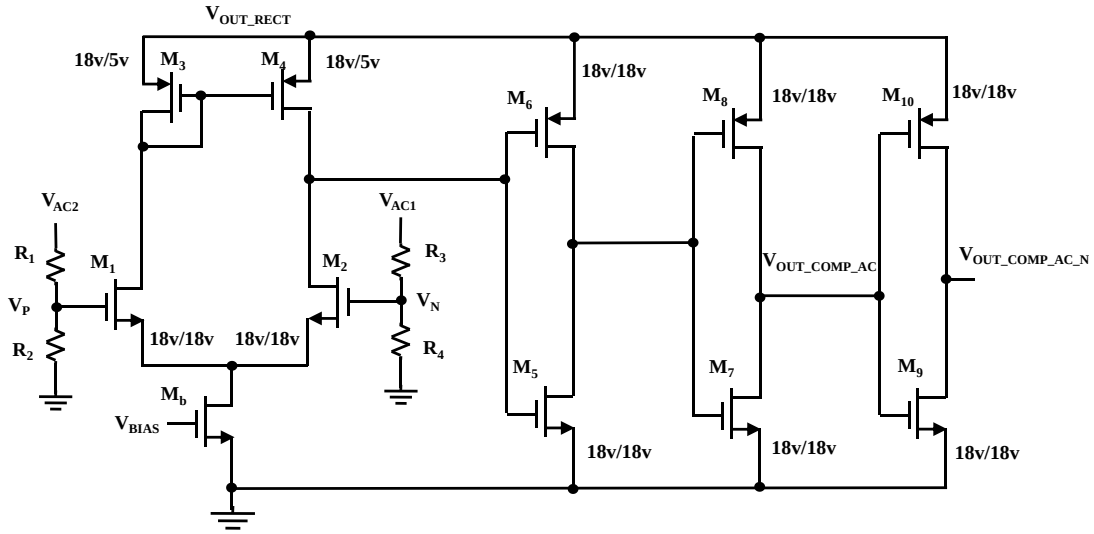


Figure 3.6 Schematic of HV AC Comparator

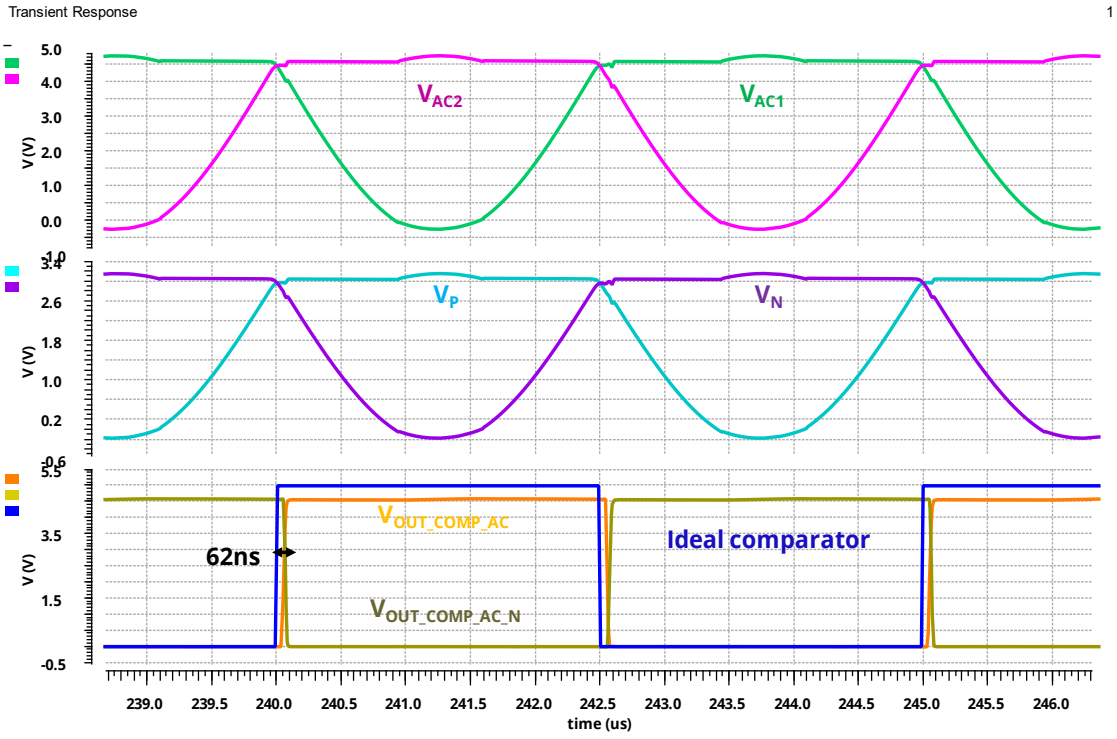
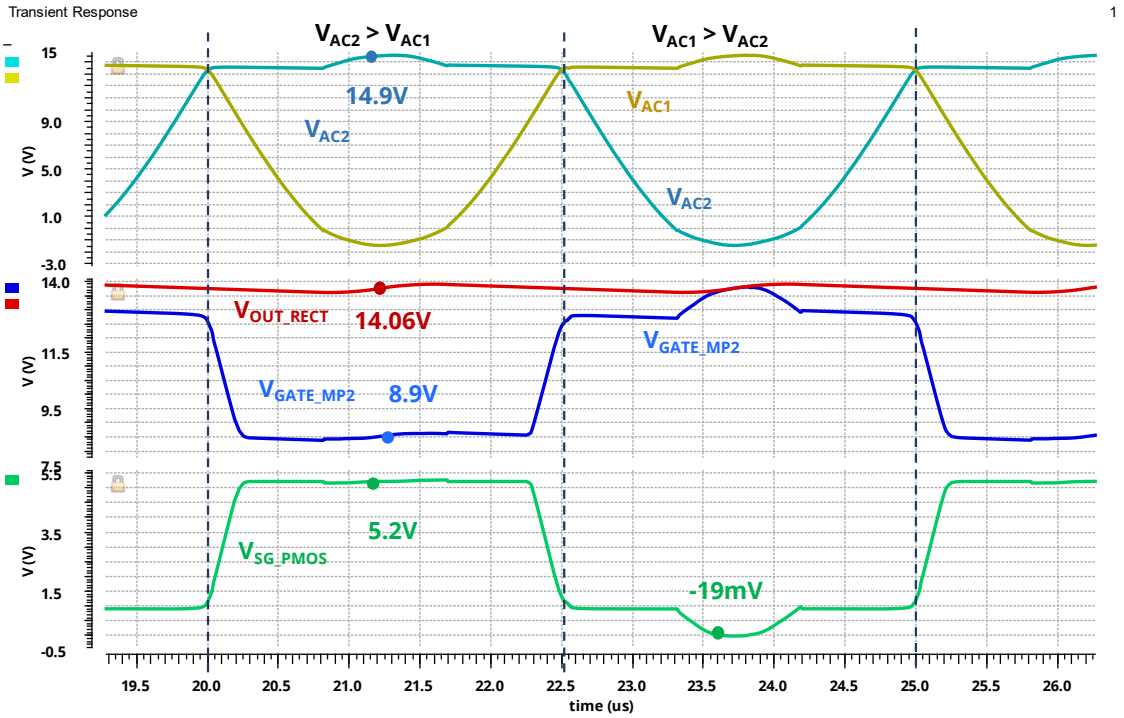


Figure 3.7 Transient simulation results of HV AC Comparator

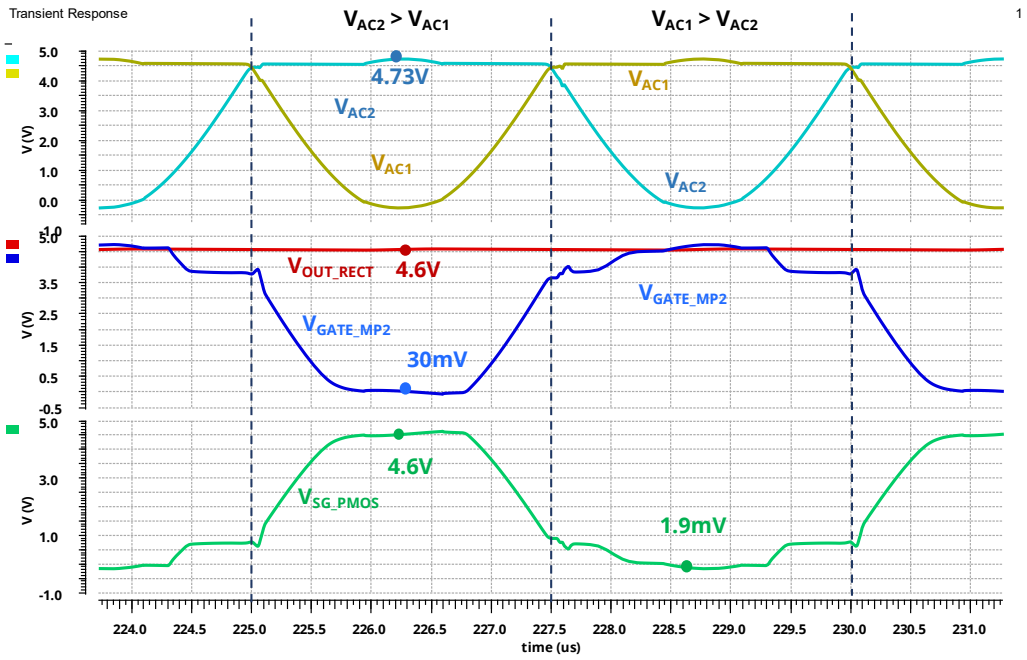
3.2.2. Simulation Results

The transient simulated waveforms in Figure 3.8(a) and (b) show the gate-source voltage across the PMOS transistor M_{P2}. When M_{P2} is on in HV domain the gate-source is 5.25V which is equal to the reverse breakdown voltage of the Zener, and in LV domain it is equal to the rectified output voltage. Figure 3.9 shows the gate-source voltage of the PMOS transistor M_{P2} across different corners and the gate-source voltage is always less than the breakdown value 5.5V.



(a)

Figure 3.8 Transient simulation results of PMOS switching (a) in HV domain at a nominal corner and (b) in LV domain at nominal corner



(b)

Figure 3.8 Continued

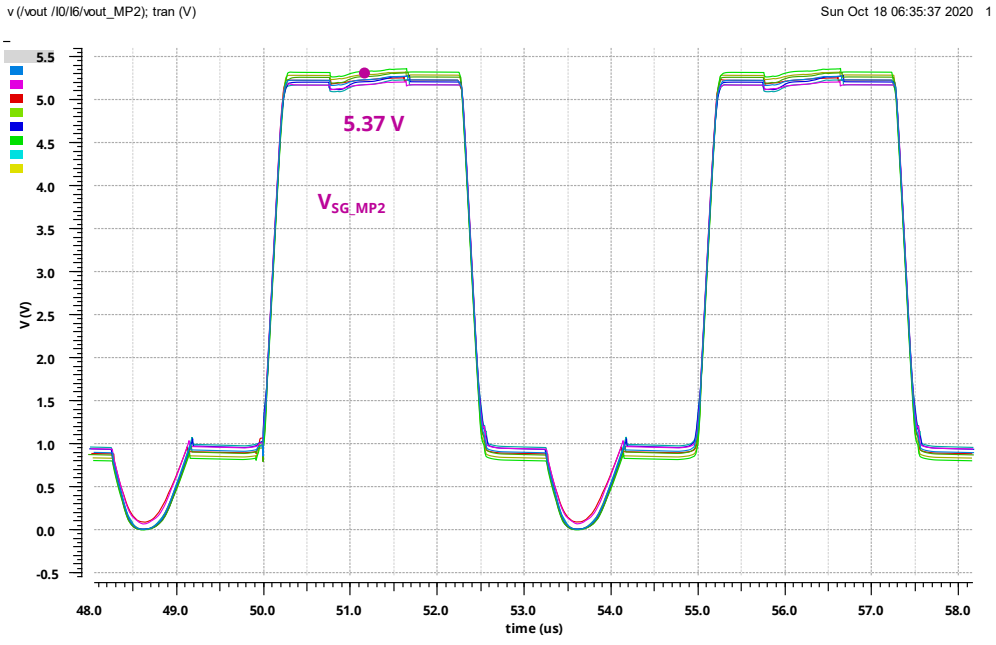


Figure 3.9 Transient simulation results of PMOS switching in HV domain across corners

3.3. NMOS Switching

The NMOS switches are operated as active diodes. The switching operation is performed as shown in Figure 3.10. The delay in the comparator CMP1 and 5V buffer introduces reverse current in the rectifier. Switched offset mechanism [3], is used to turn off the comparator earlier and reduce the reverse current.

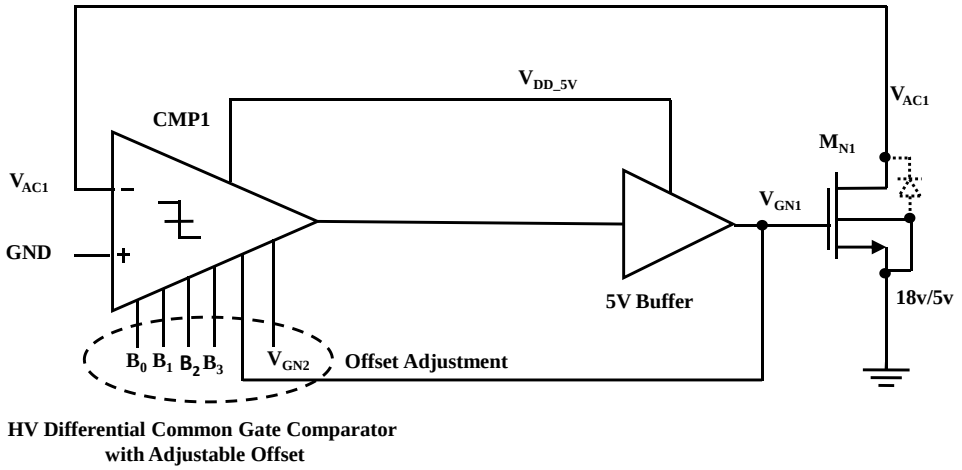


Figure 3.10 Schematic of NMOS switching

3.3.1. HV Differential Common Gate Comparator with Adjustable Offset

3.3.1.1. HV Push-Pull Common Gate Comparator

The push-pull common gate comparator used in [3], is modified as shown in Figure 3.11 for protecting the devices during high voltage transients. The input NMOS transistors used are 18v/18v devices as the node V_{AC1} can go as low as -18V. The 18v/5v devices M_9, M_{10} acts as current buffers to protect the devices M_6 and M_8.

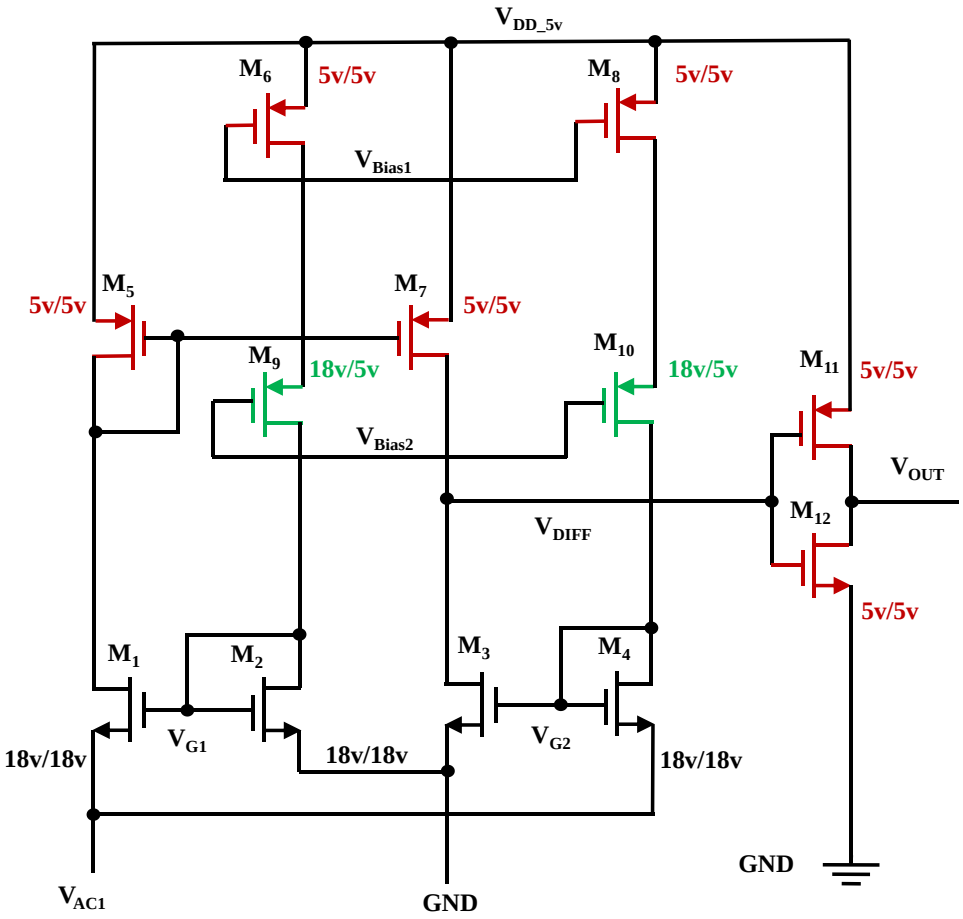


Figure 3.11 Schematic of HV push-pull common gate comparator

The push-pull common gate comparator suffers from a DC offset because of its asymmetric nature. The DC offset depends on the sizes of the PMOS and NMOS transistors and also the bias current in the comparator. The DC offset results in a delay in the comparator, which in turn affects the reverse current and PCE of the rectifier. Figure 3.12 shows the DC simulation results of the HV common gate comparator and a DC offset of 15mV is observed in the comparator.

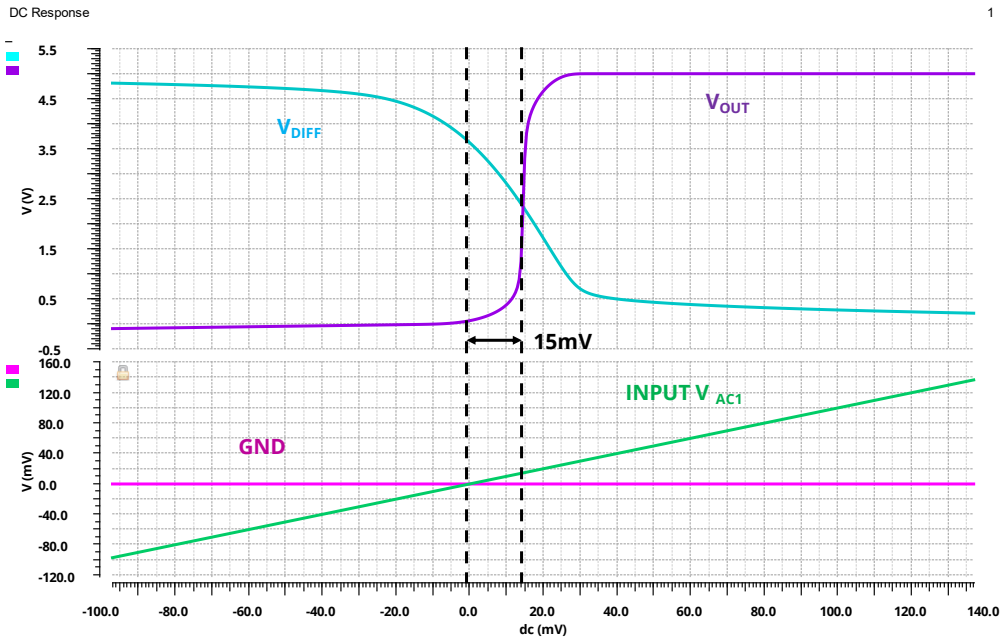


Figure 3.12 DC simulation results of HV push-pull common gate comparator

3.3.1.2. HV Differential Common Gate Comparator

The schematic of HV differential common gate comparator is shown in Figure 3.13. The proposed comparator generates two differential signals V_{OP} and V_{ON}. The differential amplifier converts these V_{OP} and V_{ON} signals into a single ended signal. The symmetric nature of the proposed architecture helps in the removal of the DC offset. The differential nature of the circuit reduces the rise and fall time of the output signal V_{DIFF} making it level insensitive. The input NMOS transistors used are 18v/18v devices as the node V_{AC1} can go as low as -18V. The 18v/5v devices M_{20} and M_{23} acts as current buffers to protect the devices M_{10} and M_{14} during high voltage transients, as these PMOS devices used for current mirrors are 5v to improve speed. M_{21} and M_{22} are used for matching with the devices M_{20} and M_{23}.

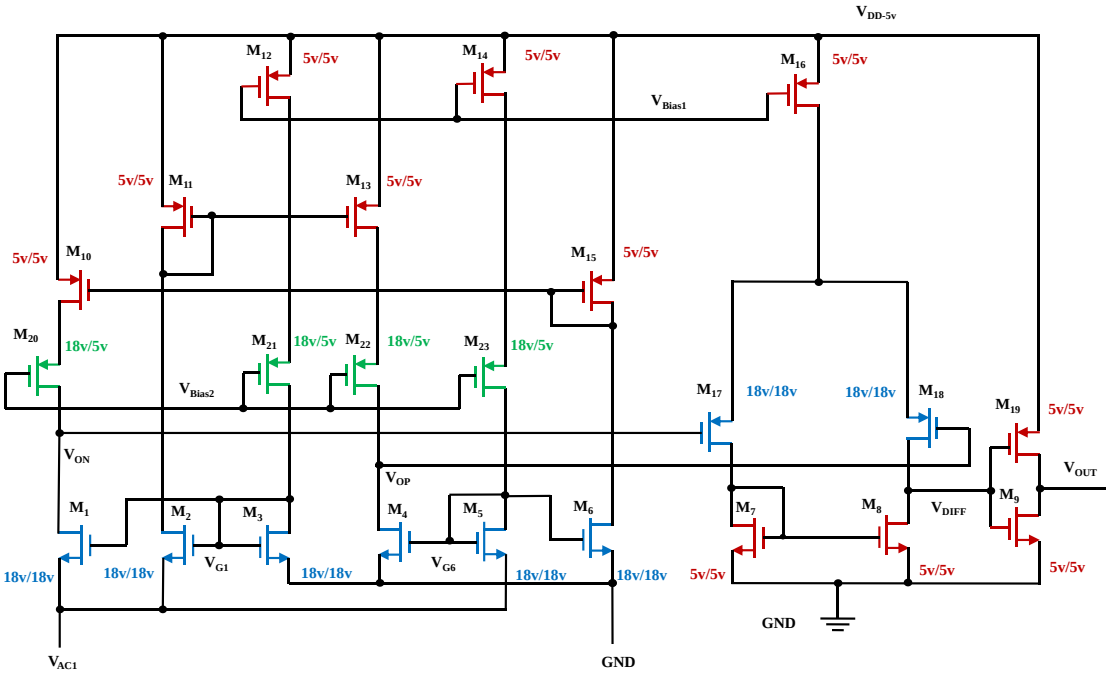


Figure 3.13 Schematic of HV differential common gate comparator

The proposed HV differential common gate comparator has higher power consumption when compared to the HV push-pull common gate comparator. The DC simulation results of the HV differential common gate comparator in the Figure 3.14 show no DC offset in the comparator. A delay of 26ns is observed at typical_37C corner and a maximum delay of 27.3ns is observed at slow_37C corner as seen in Figure 3.15 (a) and (b). The delay in the comparator can be further decreased by increasing the bias current in the comparator, which in turn increases the power consumption.

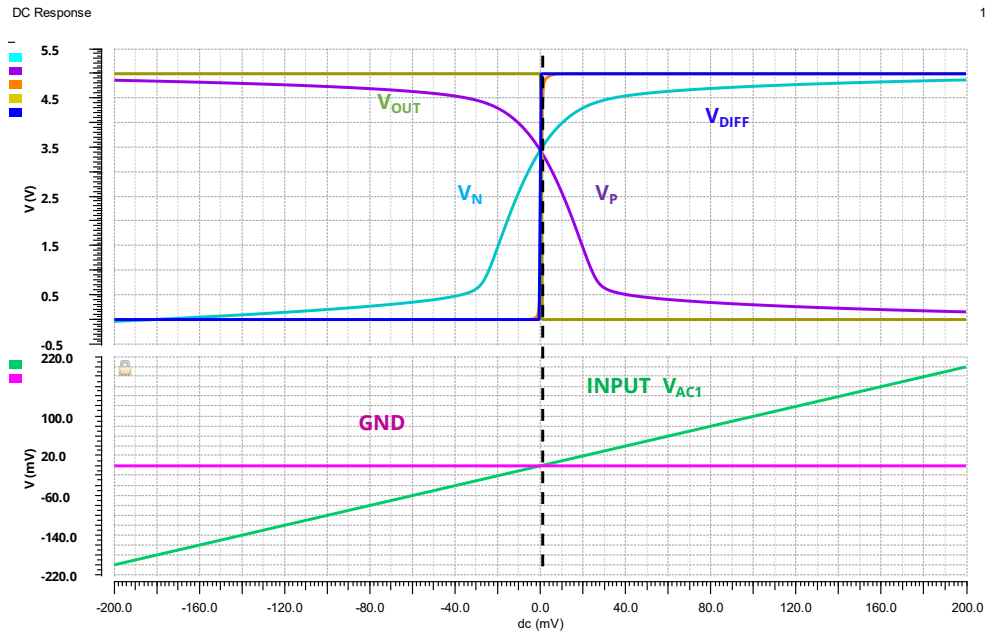
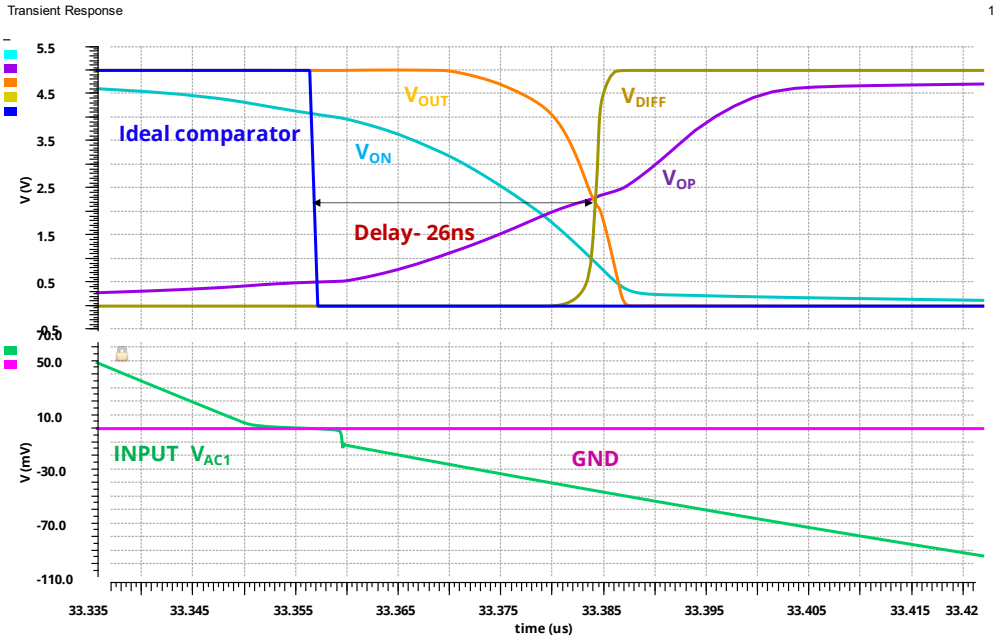
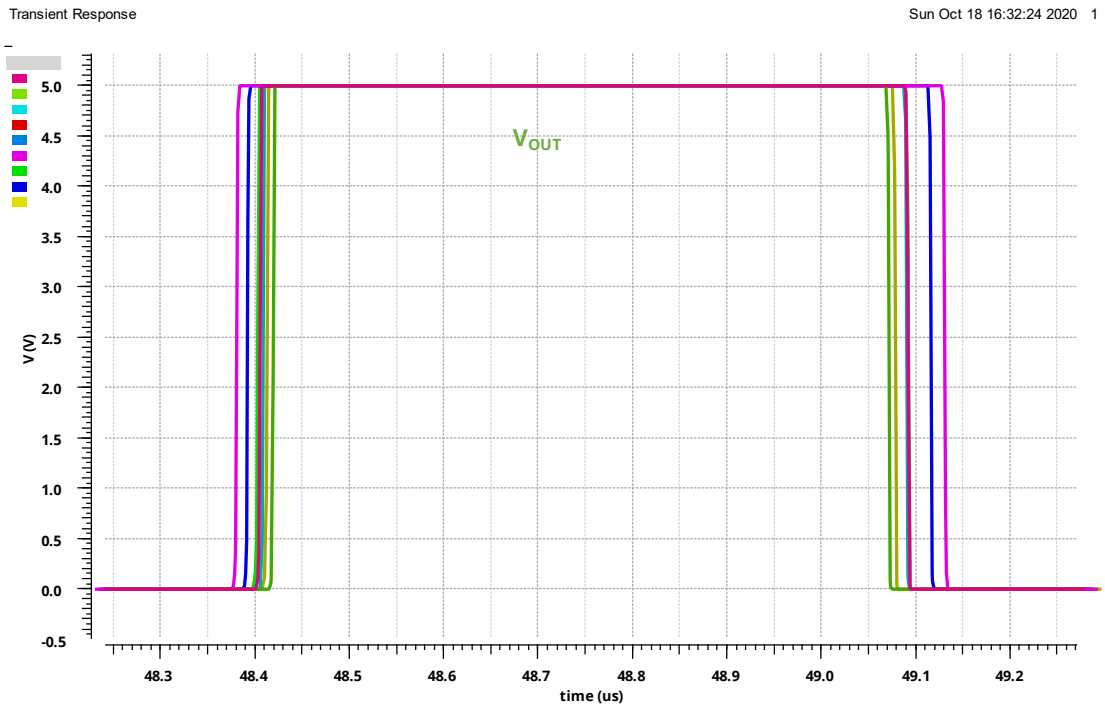


Figure 3.14 DC simulation results of HV differential common gate comparator



(a)

Figure 3.15 Transient simulation results of HV differential common gate comparator delay in nominal corner and (b) delay across the corners



(b)

Figure 3.15 Continued

3.3.1.3. Offset Introduction

The offset in the HV differential common gate comparator can be introduced by using the two current sources $I_{OFFSET1}$ and $I_{OFFSET2}$ as shown in the Figure 3.16. The two current sources help in generating a positive and negative DC offset as seen in Figure 3.17. The overall offset introduced in the comparator is given by

$$V_{OFFSET} = 0.5\left(\sqrt{\frac{2I_{REF}}{K_N\left(\frac{W}{L}\right)_N}}\right)\left(\sqrt{N_2+1}\right) - \sqrt{N_1+1}) \tag{3.2}$$

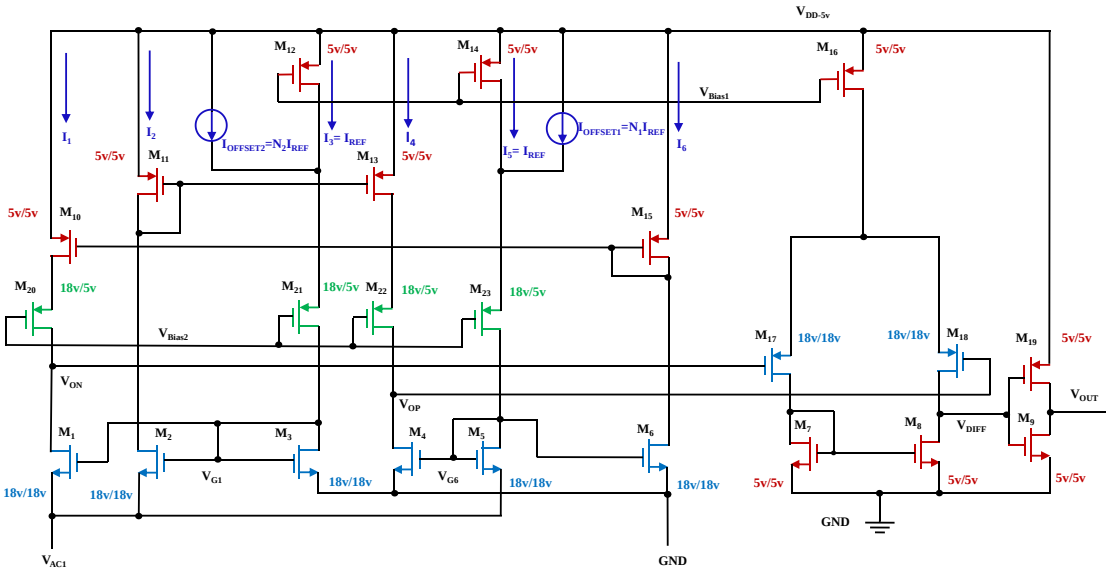


Figure 3.16 Schematic of offset introduction in HV differential common gate comparator

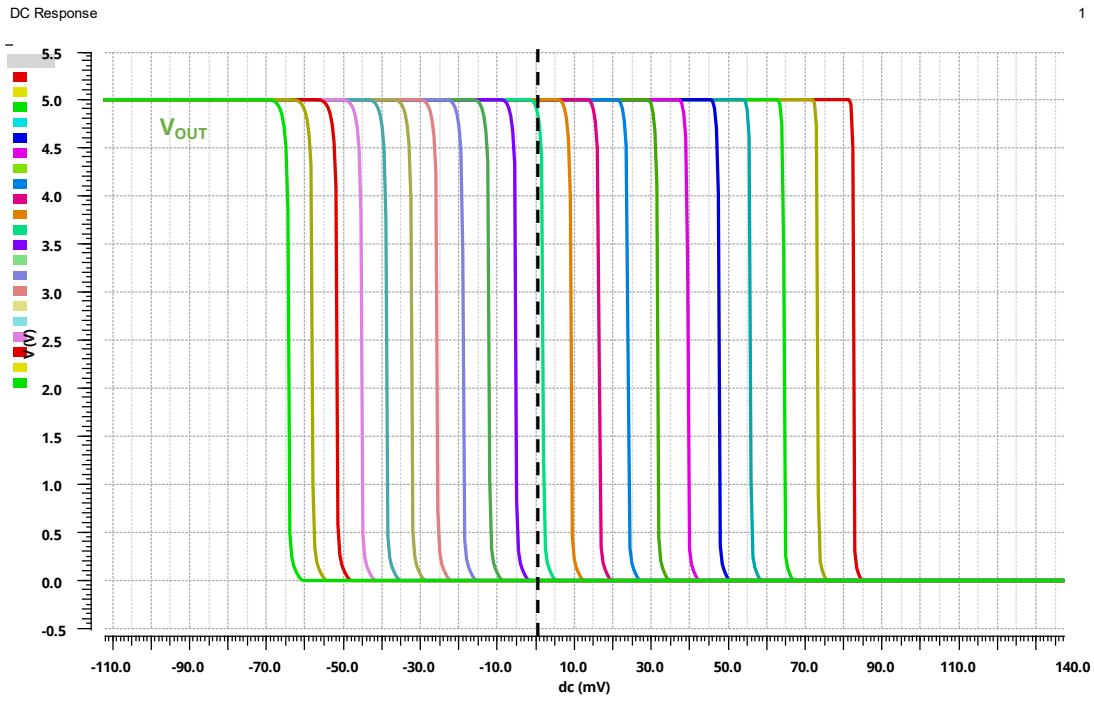


Figure 3.17 DC simulation results of offset introduction in HV differential common gate comparator

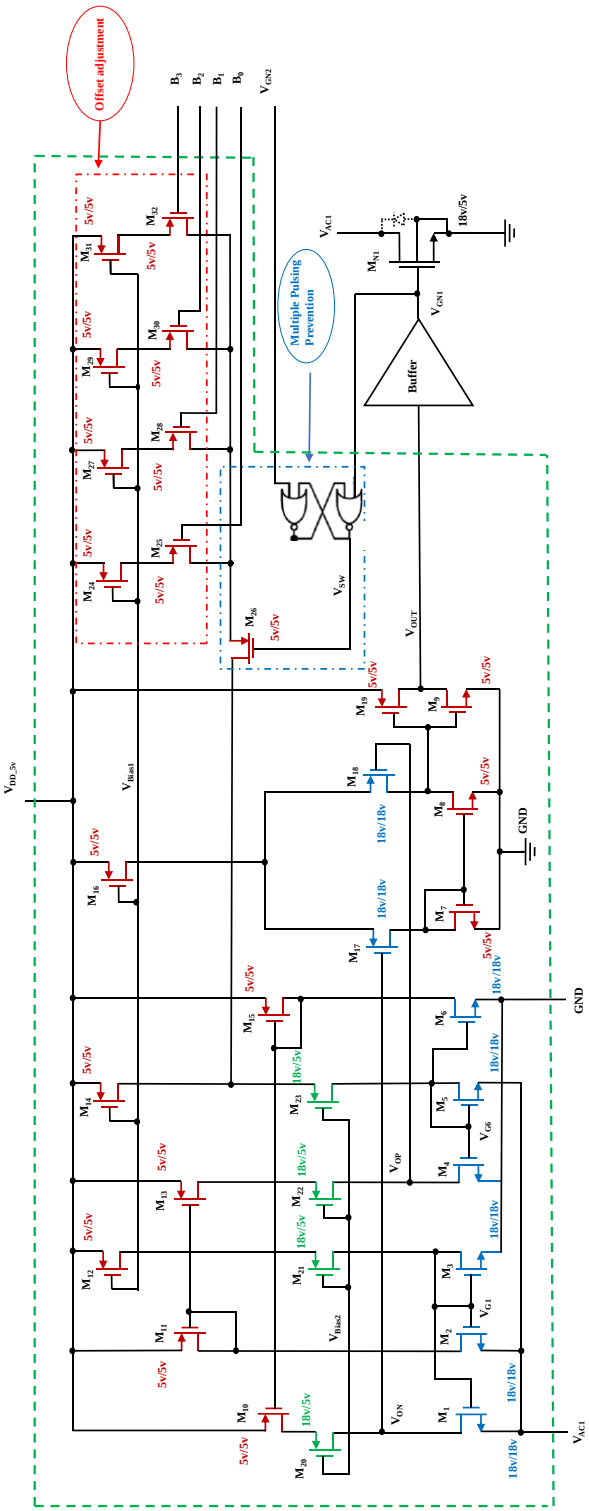
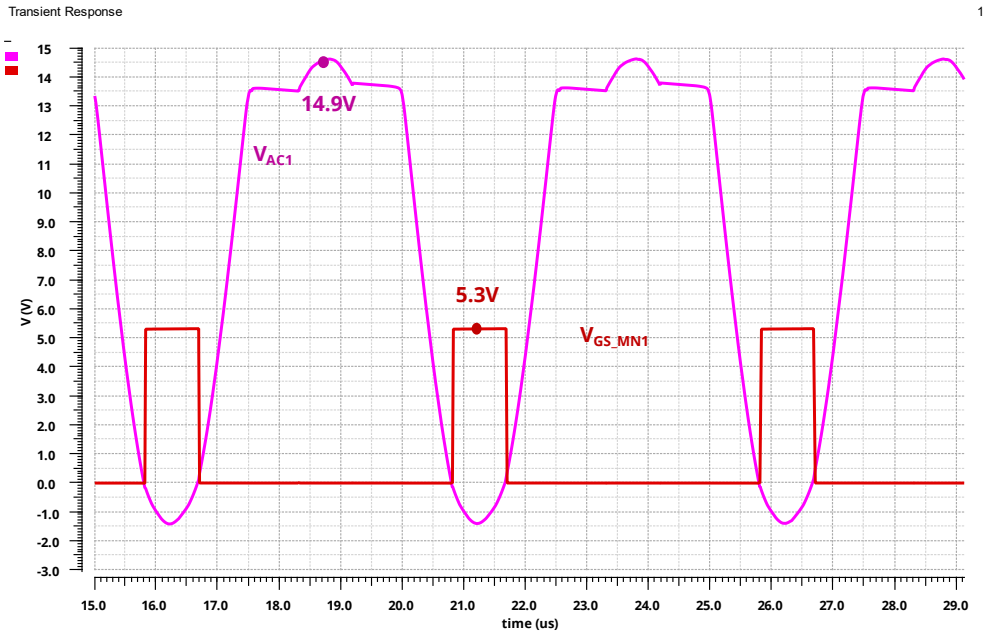


Figure 3.18 Schematic of HV differential common gate comparator with adjustable offset

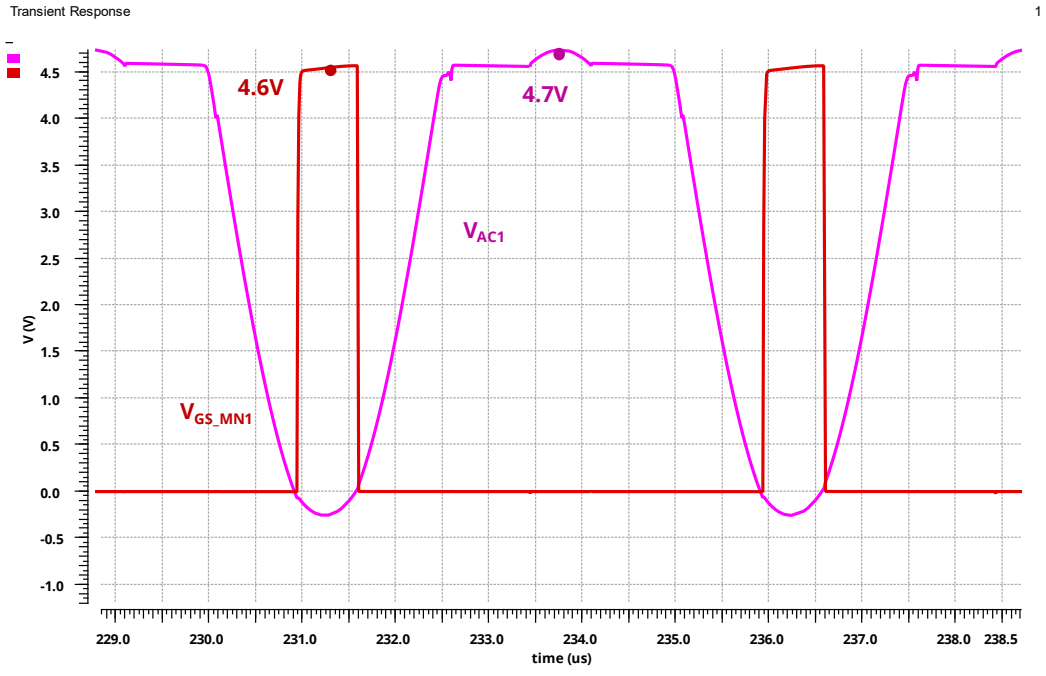
For the elimination of reverse current in the rectifier, a negative offset is required such that the comparator turns off earlier. Hence only the current source $I_{OFFSET1}$ shown in the Figure 3.16 is used in the design of comparator. Figure 3.18 shows the final schematic of the proposed HV differential common gate comparator with adjustable offset. The transistors M_{24}, M_{25}, M_{27}, M_{28}, M_{29}, M_{30}, M_{31} and M_{32} correspond to the offset adjustment. The offset is adjusted by the calibration circuit. The NOR gate-based SR-latch is added to prevent the multiple pulsing in the comparator as proposed in [3].

3.3.2. Simulation Results

The transient simulation results in the Figure 3.19 (a) and (b) and Figure 3.20 shows that the gate-source voltage of the NMOS transistor M_{N1} is always less than 5.5V in both HV and LV domain. A maximum voltage of 5.4V is observed across the gate-source of M_{N1} as seen in Figure 3.20.



(a)



(b)

Figure 3.19 Transient simulation results of NMOS switching in (a) HV domain and (b) LV domain

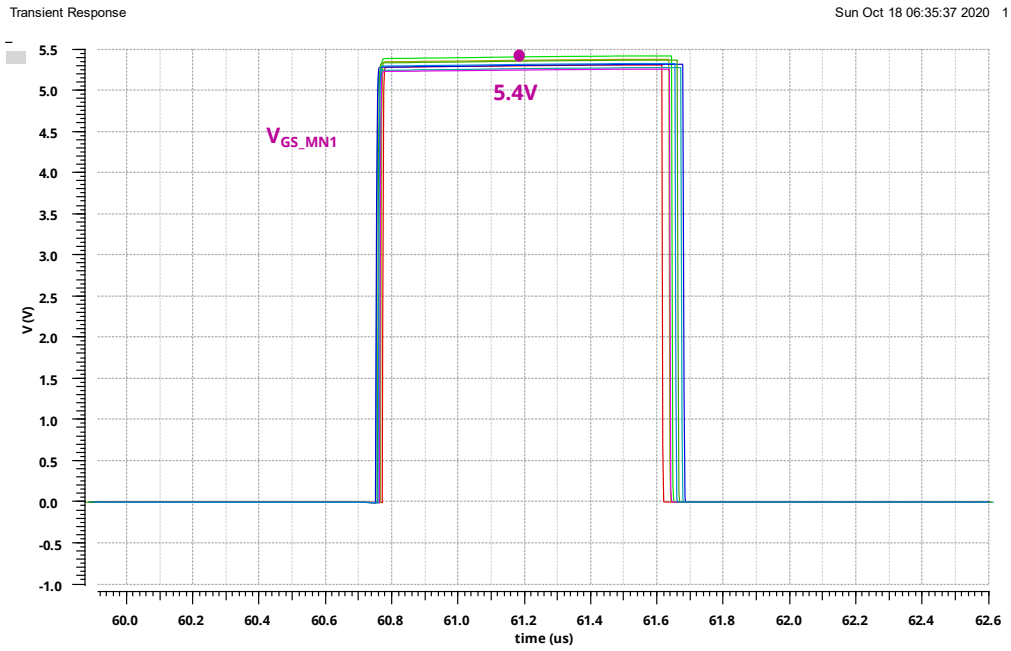


Figure 3.20 Transient simulation results across corners in HV domain

3.4. Calibration

The offset introduced in the HV common gate comparator to reduce the reverse current in the rectifier is determined by the calibration circuit shown in Figure 3.21. The presence of reverse current in the system can be realized by observing the V_{DS} drop across the NMOS switch M_{N1} i.e., by comparing the signals V_{AC1} and GND. The CMP_Calibration comparator and the HV differential common gate comparator with adjustable offset CMP_1 have the same inputs but connected to opposite polarities. If there was no delay in the CMP_1 and buffer network, the signals V_{GN1} and output of the CMP_Calibration comparator should be out of phase and no overlap should be present between these signals. The delay in the CMP_1 and buffer network results in an overlap between the signals V_{GN1} and the output of the CMP_Calibration comparator. The AND

gate generates an output high pulse when there is an overlap between these signals indicating the presence of reverse current in the rectifier.

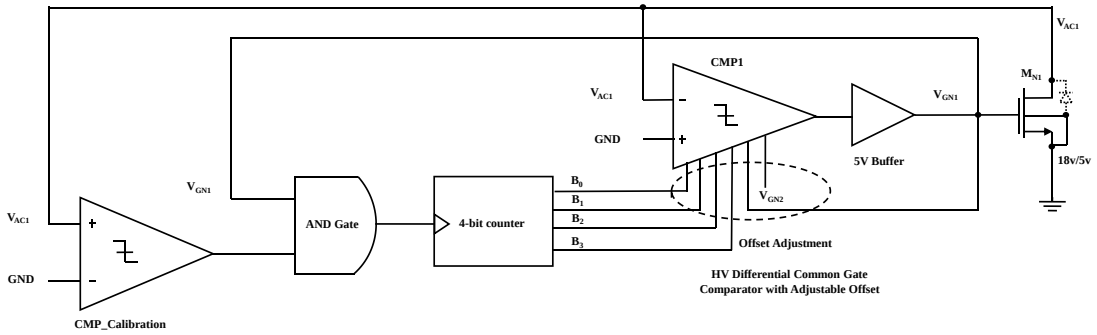


Figure 3.21 Schematic of calibration circuit

The output of AND gate is connected to the clock input of the 4-bit up counter. The counter output is connected to an offset introducing binary weighted transistors in the HV differential common gate comparator with adjustable offset. Ideally when sufficient offset is introduced in the comparator, the reverse current is eliminated in the rectifier and the output of the AND gate remains low and the counter output remains constant.

The effectiveness of the calibration network depends on the frequency of operation and delay observed in the CMP_Calibration comparator. As the delay in the CMP_Calibration comparator increases it can no longer detect the presence of reverse current in the system. Hence a minimum delay is required in the CMP_Calibration comparator to reduce the reverse current efficiently.

3.4.1. Simulation Results

The transient simulation results presented in Figure 3.22 shows the output of the counter and reverse current in the rectifier. The binary outputs of the 4-bit counter is converted into decimal values using an ideal summing block. We observe that the counter output increases and then remains constant when the calibration circuit no longer is able to detect the reverse current in the rectifier. Figure 3.23 (a) and (b) shows the transient simulation results of the rectifier with and without calibration circuit. With calibration, the average amount of reverse current in the system decreases from 2.6mA to 0.47mA. The peak reverse current decreases from -135mA to -55mA. The reverse current in the system is reduced by 81%.

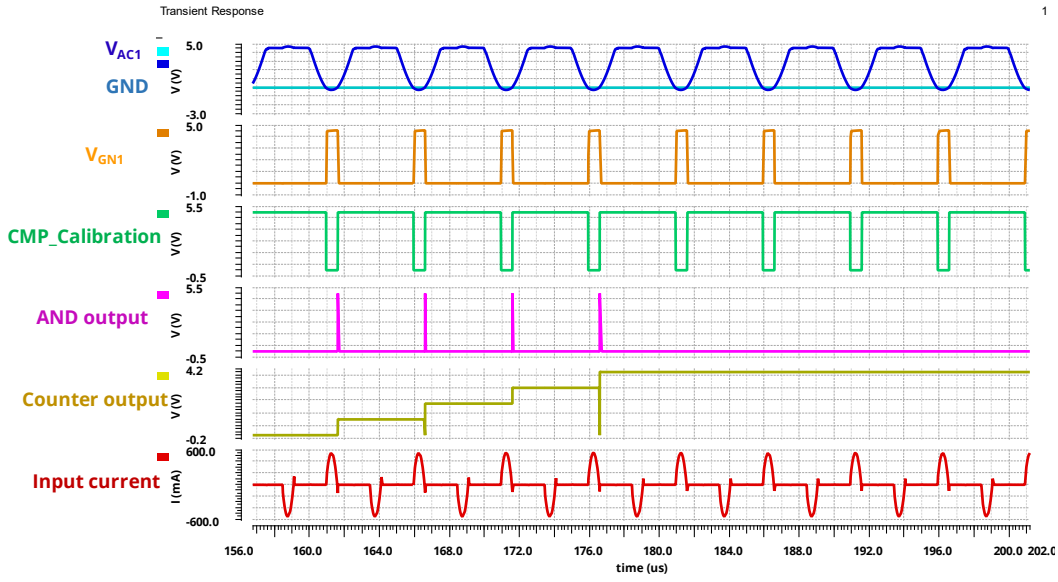
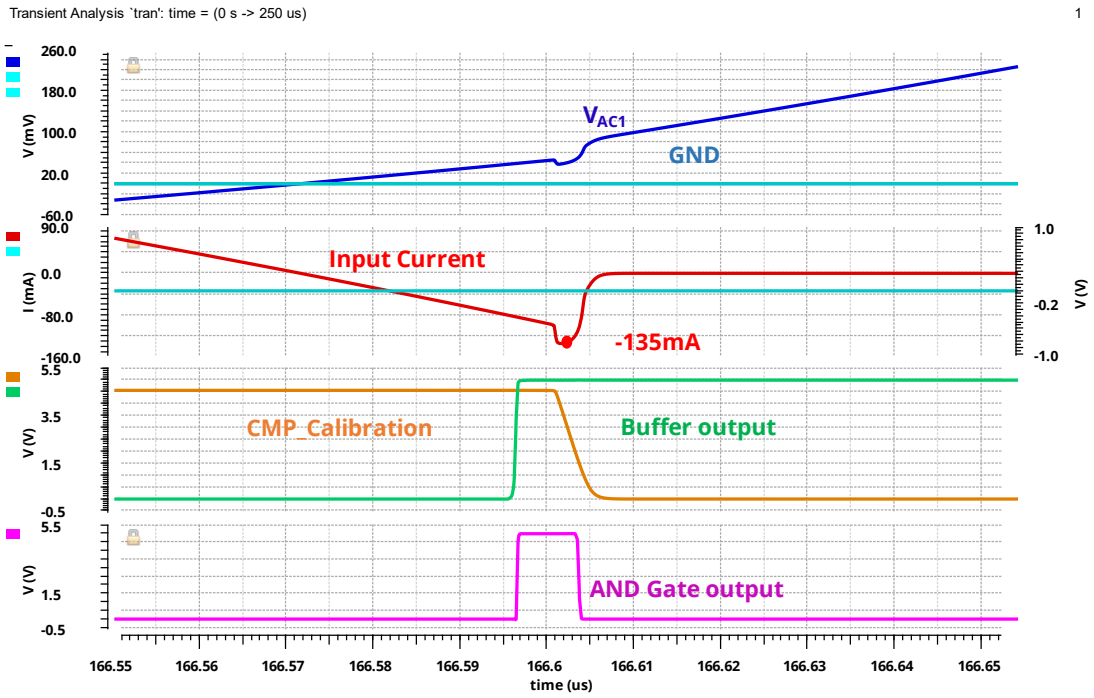
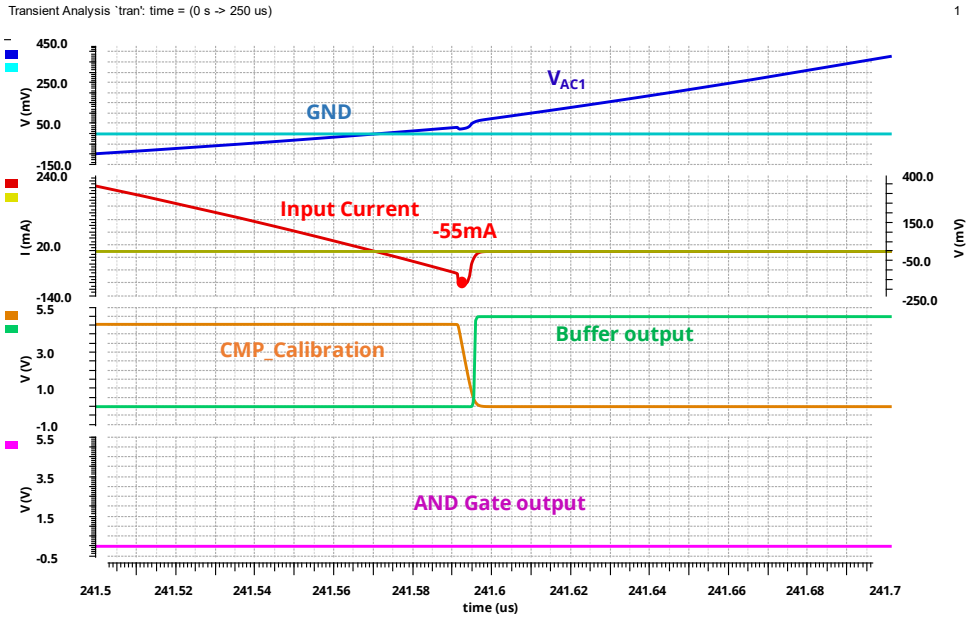


Figure 3.22 Transient simulation results of calibration circuit

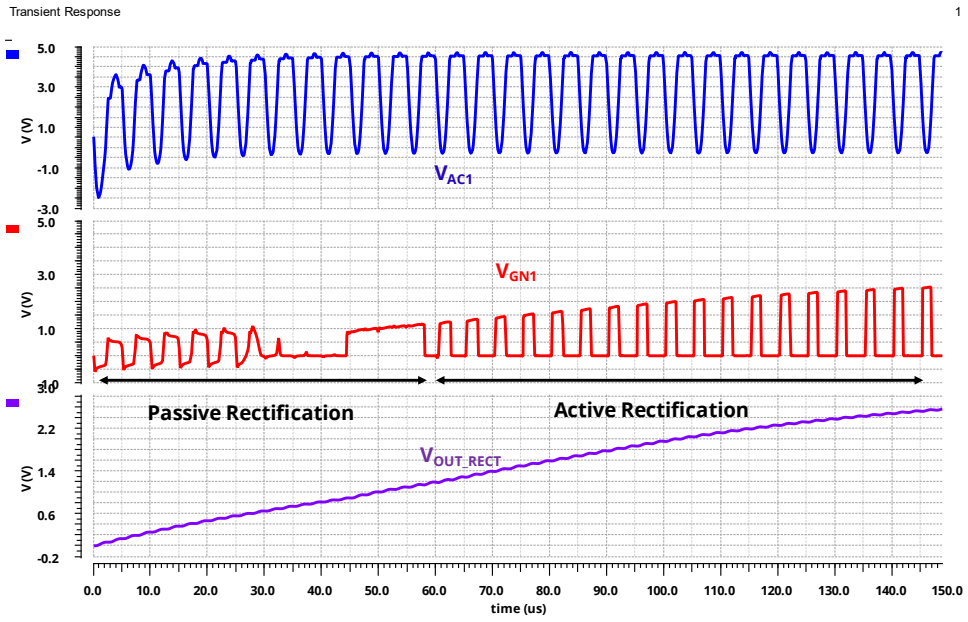


(a)

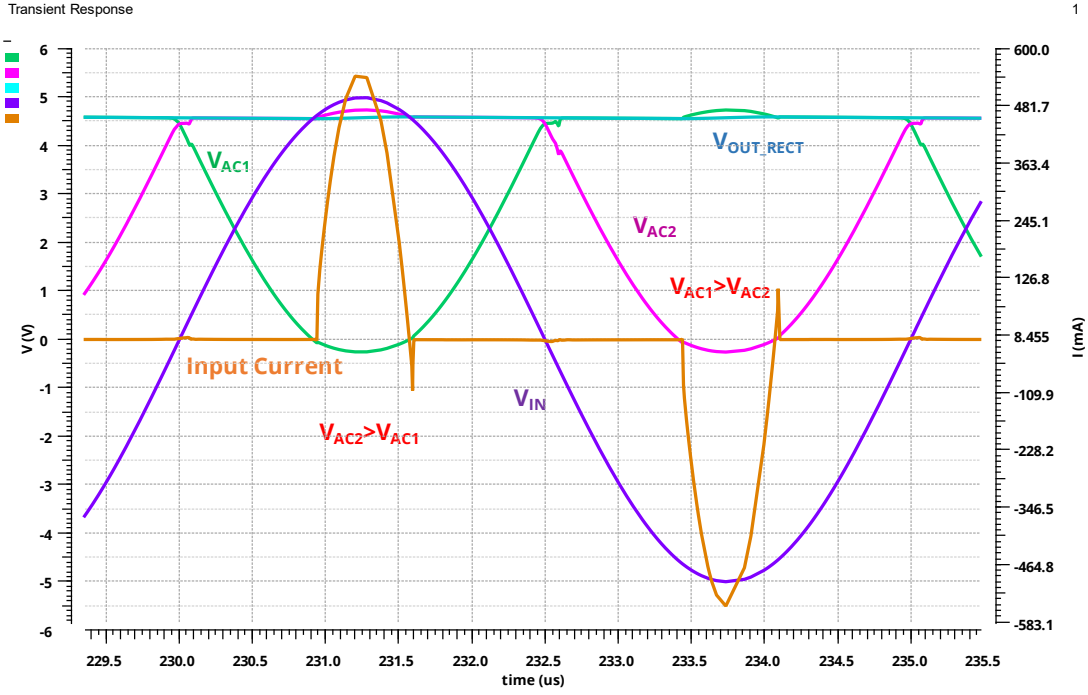


(b)

Figure 3.23 Transient simulation results showing the reverse current (a) without calibration and (b) with calibration



(a)



(b)

Figure 3.24 Simulated waveforms of active rectifier during (a) start-up (b) steady state

Figure 3.24 (a) and (b) shows the transient simulation results of the proposed active rectifier when the input voltage to the rectifier is 5V during the start-up and steady state operation. Figure 3.24 (a) show the operation of rectifier using body diodes during the start-up of the rectifier.

Table 3.5 Comparison of active rectifier with ideal comparator and final rectifier architecture across corners

Corner	Rectifier with Ideal Comparator		Final Rectifier architecture without Calibration		Final Rectifier architecture with Calibration	
	V_{OUT_RECT}	PCE	V_{OUT_RECT}	PCE	V_{OUT_RECT}	PCE
Typical_37C	4.646	93.37	4.573	91.01	4.588	91.7
Fast_ -10C	4.711	95.53	4.648	91.4	4.662	92
Typical_-10C	4.67	94.7	4.61	90.7	4.59	91.4
Slow_-10C	4.611	93.53	4.57	91.01	4.6	91.6
Typical_65C	4.619	93.96	4.541	90.41	4.556	91.1
Slow_65C	4.585	93.37	4.497	90.01	4.514	90.69
Fast_65C	4.651	94.5	4.578	89.79	4.593	91.54
Slow_37C	4.614	93.87	4.534	90.35	4.549	91.34
Fast_37C	4.675	94.91	4.607	90.31	4.62	91.56

From Table 3.5, we observe that the calibration circuit improves PCE by 0.6-1.5% across corners. We also observe that the reduction in PCE across the corners when the comparator is implemented at the transistor level is around 1.5-3% across the corners.

4. CONCLUSIONS

This thesis proposes a high voltage and high current CMOS active rectifier with digital offset compensation for implantable devices to integrate into a wireless charging system in biomedical implants. The proposed HV differential common gate comparator overcomes the limitations seen in the HV push-pull common gate comparator. The calibration circuit detects the reverse current and introduce the offset accordingly to reduce it. For an AC input voltage of 5V at frequency of 200kHz, the proposed active rectifier achieves a peak rectified output voltage of 4.662V and peak PCE of 92% for a load of 50Ω.

REFERENCES

[1] PDF, "High Dynamic Range CMOS Imager Technologies for Biomedical Applications," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 1, pp. 281-289, Jan. 2009.

[2] H. Cho, K. Noh, T. Ishikawa, D. Yang, E. Sánchez-Sinencio and H. Choo, "Powering portable electronics using vocal fold vibrations," *2017 IEEE 30th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 217-220, 2017.

[3] Y. Lu and w.-H. Ki, "A 13.56 MHz CMOS Active Rectifier With Switched-Offset and Compensated Biasing for Biomedical Wireless Power Transfer Systems," *https://ieeexplore.ieee.org/xpl/RecentIssue.jsp?punumber=4156126*, vol. 8, no. 3, pp. 334-344, 2014.

[4] S. Guo and H. Lee, "An Efficiency-Enhanced CMOS Rectifier With Unbalanced-Biased Comparators for Transcutaneous-Powered High-Current Implants," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 6, pp. 1796-1804, 2009.

[5] H.-M. Lee and M. Ghovanloo, "An Integrated Power-Efficient Active Rectifier With Offset-Controlled High Speed Comparators for Inductively Powered Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 8, pp. 1749-1760, Aug. 2011.

[6] J. Fuh, S.-K. Hsieh, F.-B. Yang and P.-H. Chen, "A 13.56MHz power-efficient active rectifier with digital offset compensation for implantable medical devices," *2016 IEEE Wireless Power Transfer Conference (WPTC)*, pp. 1-3, 2016.

[7] K. Noh, J. Amanor-Boadu, M. Zhang and E. Sánchez-Sinencio, "A 13.56-MHz CMOS Active Rectifier With a Voltage Mode Switched-Offset Comparator for Implantable Medical Devices," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 2050-2060, Oct. 2018.

[8] ON Semiconductor, "ONC18: G/MS," July 2016. [Online]. Available: https://www.onsemi.com/pub/Collateral/ONC18GMS-D.PDF.

APPENDIX A

ANALYSIS OF OFFSET INTRODUCTION IN COMPARATOR

A.1 Offset Introduction in HV Differential Common Gate Comparator

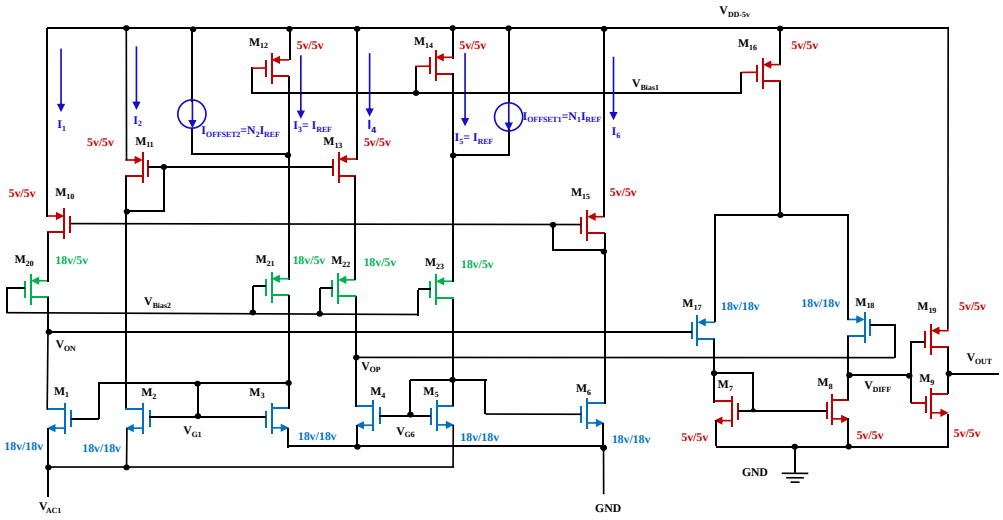


Figure A.1 Offset introduction in HV differential common gate comparator

The current sources $I_{OFFSET1}$ and $I_{OFFSET2}$ introduce the offset in the comparator as shown in Figure A.1. The currents through M_3 and M_5 determine the voltages at the nodes V_{G1} and V_{G6}. The equation A.2, A.3 shows voltage V_{G1} and V_{G6} obtained using the equation A.1

$$I = K_N \left(\frac{W}{L}\right)_N (V_{GS} - V_{TH})^2 \qquad (A.1)$$

$$V_{G1} = V_{TH} + \sqrt{\frac{2(N_2 + 1)I_{REF}}{K_N \left(\frac{W}{L}\right)_N}} \tag{A.2}$$

$$V_{G6} = V_{OFFSET} + V_{TH} + \sqrt{\frac{2(N_1 + 1)I_{REF}}{K_N \left(\frac{W}{L}\right)_N}} \tag{A.3}$$

For the node V_{ON} the voltage V_{AC1} at which the current through the source transistor M_{10} and the sink transistor M_1 are equal determine the offset observed at the node V_{ON}. The equations A.4, A.5, A.6 shows the voltage offset seen at the node V_{ON}.

$$I_1 = K_N \left(\frac{W}{L}\right)_N (V_{G1} - V_{OFFSET} - V_{TH})^2 = K_N \left(\frac{W}{L}\right)_N (V_{G6} - V_{TH})^2 \tag{A.4}$$

$$V_{OFFSET} = V_{G1} - V_{G6} \tag{A.5}$$

$$V_{OFFSET} = 0.5 \left(\sqrt{\frac{2I_{REF}}{K_N \left(\frac{W}{L}\right)_N}} \right) (\sqrt{N_2 + 1}) - \sqrt{N_1 + 1}) \tag{A.6}$$