CMOS WIRELESS RECEIVERS FOR EMERGING RF/MM-WAVE APPLICATIONS

A Dissertation

by

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ABSTRACT

With the advance of communication in people's everyday life and ever-increasing request for more wireless communication throughput, many involved fields are offering new communication architectures or revisit and modify the existing ones. In this thesis two of such systems are studied, analyzed, designed, implemented in CMOS technology, and measured as a proof of concept.

In the first project which is covered in Section 2, an in-band full-duplex (IBFD) radio frequency (RF) receiver is implemented. In a conventional communication system, in order to limit the transmitter leakage on the receiver, either time division duplexing or frequency division duplexing is employed. However, this comes at the cost of not utilizing the full spectrum at any given time. A wideband receiver is proposed that performs transmitter leakage suppression, therefore demonstrates communication wherein the entire band is used both by the transmitter and receiver, and ideally result in twice increase in the entirely allocated RF spectrum. The prototype chip is fabricated in 65 nm CMOS.

In the second project which is covered in Section 3, a 22.2-43 GHz wideband 28 nm CMOS low-noise amplifier (LNA) is designed and fabricated. The LNA uses a new proposed architecture, gate-drain mutually induced feedback LNA (GDMIF-LNA). The LNA shows a wideband noise and power matching at the input, and also an important drawback of other popular architecture (common source with inductive degeneration) which is ground path modeling, is overcommed in this architecture. The bandwidth coverage of the LNA is a record in CMOS multi-stages LNAs.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supervised by a dissertation committee consisting of Professor Kamran Entesari (chair), Professor Samuel Palermo, and Professor Raffaella Righetti of the Department of Electrical and Computer Engineering and Professor Dorrin Jarrahbashi of the Department of Mechanical Engineering.

All other work conducted for the dissertation was completed by the student independently.

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1. INTRODUCTION AND OVERVIEW

Sometime in Dec. 2001 the number of wireless service subscribers exceeded the number of wireline subscribers. The growth in wireless connective has exponentially increased ever since. In 2014, the number of mobile subscription exceeded the population of the planet earth while there were practically zero subscribers in 1981. This unprecedented increase basically from 0 to more than 7 billion in less than 4 decades shows extremely favorable wireless connection. Depicted in Fig. 1.1, it is highly desirable to connect objects and people all together. This is the main task of wireless networks, webs of webs, to accomplish in the next generations. The first four wireless generations of mobile GSM communication is depicted as an example in Fig. 1.2. With the highly anticipated 5G promise of substantial lower latency and higher throughput right around the corner, a big door of opportunities open up for realizing more connections between people and objects which was previously impeded by the hardware.

Figure 1.1: Wireless connectivity with no border.

A glance at the RF spectrum (Fig. 1.3) shows that all the bands are divided for different application. This paradigm for wireless connection although successful today, has a major drawback of not being scallable. Two different projects are discussed in this thesis which both try to address the RF frequency scarcity issue for future wireless. In the first project an in-band full-duplex receiver with self-interference suppression is proposed which effectively doubles the spectrum usage

Figure 1.2: The first four generations of mobile service.

efficiency. In addition, compared to the allocated band paradigm of communication which we use today, these wideband radios have the potential to choose the band by scanning a part of a spectrum and using an algorithm for band selection which improves spectrum efficiency. In the second project a new communication system which combines silicon photonics and integrated circuits. The main outcome is radios with substantial higher throughput compared to what is realizable today. They operate at 5G associated frequency band (22.2-43 GHz) and are capable of receiving and transmitting signals with bandwidths as large as 5 GHz. The focus of the second project is the receiver front-end and developing a wideband low-noise amplifier operating over 22.2-43 GHz.

RF spectrum scarcity and the ever-increasing demand for higher bandwidth has drawn tremendous attention to change the today's wireless communication paradigm. Full-duplex (FD) communication offers two-time higher exploitation of spectrum. Specifically, wideband FD paves the way for frequency allocation of a spectral efficient cognitive radio. The challenging task of the receiver in this scenario is to extract the desired signal in the presence of substantial unwanted TX leakage right on top of the desired band. In addition to have a mechanism for leakage cancellation, very linear receivers are suited for such radios so as to minimize the inter-modulation (IM) of the RX and TX-leakage in order to preserve the otherwise corrupted signal. Self-interference-cancellation (SIC) path from TX replica to RX interface needs to adjust the required magnitude scaling and phase-shift of TX replica in a highly linear way. Distorted adjustment creates *residue* after subtraction from TX-leakage. Both the residue and the undesired RX and TX-leaked IM prove to be very difficult, if not impossible, to cancel in subsequent stages (Fig. 1.4). Accordingly,

they can raise the noise floor to an unacceptable high level, and mask the desired signal. Passive cancellation techniques can maintain the cancellation path linearity requirements, hence avoid the residue problem, while keeping the added noise to TX replica to a low level, as compared to active counterparts.

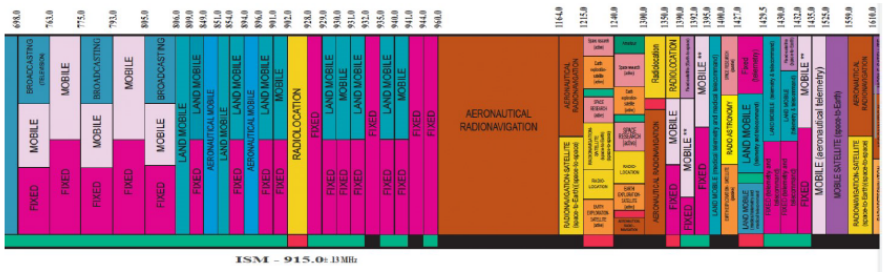


Figure 1.3: The allocated RF spectra and allocated bands.

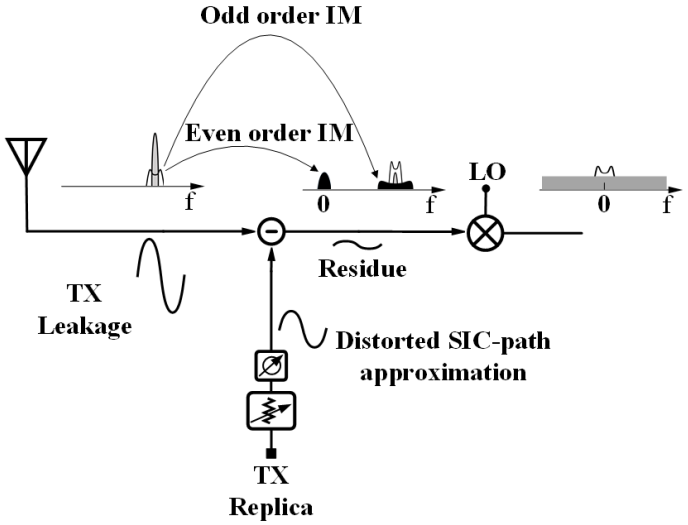


Figure 1.4: Nonlinearity mechanisms leading to noise floor degradation in a SIC direct-conversion receiver.

Different domains, namely propagation, RF, analog-baseband, and digital may be used for cancellation of leaked TX. In the RX chain, the earlier leakage cancellation occurs, not only the

nonlinearity related issues are mitigated, but also a more realistic duplicate of TX-leakage can be approximated. Effects such as TX PA nonidealities, and PA noise skirt can be captured at RF stage more accurately as compared to all back-end cancellation techniques. In this work, high RF down-converted cancellation is aimed. Due to linearity requirements of an FD-RX, mixer-first architecture is chosen, and voltage gain before baseband down-conversion is avoided. Unlike previous implementation trades between RX-linearity and noise performance, NF is not sacrificed at the cost of linearity, and an average 35 dB SIC in a single domain is achieved. This project is covered in details in section 2.

Future multi-function radios with ultra-wide instantaneous bandwidth and rapid dynamic tuning have great potential to enable increases in wireless broad-band communications, and co-existence of radar, radio astronomy, and sensing systems. RF photonics technology is a promising candidate to enable these widely tunable receivers with wide bandwidth over a broad spectral range with rapid dynamic tuning. This proposal's research goal is to develop novel chip-scale silicon photonic mm-wave receiver front-end architectures, with high-performance photonic filtering and modulation implemented in a SOI optical chip intelligently controlled by a nanometer CMOS chip to allow for rapid filter reconfiguration and jammer rejection. To accomplish this, the objectives are: (1) architecture definition of a silicon photonic mm-wave receiver with automatic jammer suppression, (2) development of novel silicon photonic optical filters capable of rapid electrical reconfiguration, (3) development of algorithms and hardware for optical band-definition bandpass filter tuning and dynamic notch filter placement for jammer rejection, (4) implementation of novel CMOS prototypes, which include filter tuning loops, modulator drivers with adaptive linearization, and front-end circuitry for testing with the proposed silicon photonic ICs. The design and implementation of the front-end LNA is the main focus of this thesis. A wideband mm-wave LNA is proposed and elaborated in section 3. It is shown that a pair of magnetically coupled inductors at gate-drain of a transistor creates a real impedance part proportional to the mutual inductor. This reactive feedback property is employed to realize an LNA input power matching. The implemented LNA architecture comprises three stages, namely, a cascode gate-drain mutually induced feedback

(GDMIF) stage, a cascode stage magnetically coupled to the following stage, and a differential pair with capacitive cross-coupled neutralization. The fabricated prototype in 28 nm bulk CMOS is functional over the bandwidth of 22.2 to 43 GHz, has maximum gain of 21.1 dB, achieves 3.5 dB minimum NF, and 4.5 dB average NF, has mid-band IIP_3 of -2 dBm, and consumes 18.5 mW power.

This thesis is organized as following:

Chapter 2 is devoted to the self-interference cancelling full-duplex receiver. State-of-the-art implementations and literature review is outlined in section 2.1. In section 2.2, the in-band-full-duplex radios' considerations are studied. The effect of nonidealities is discussed in section 2.3. The architecture of the proposed SI-canceling receiver is described in section 2.4. The linearity requirement is elaborated in section 2.5. The RX performance analysis is outlined in section 2.6. Section 2.7 illustrates circuit designs and implementation for building blocks. Section 2.8 presents the measurements performed on the chip, and conclusions are drawn in section 2.9.

In chapter 3 the radio over fiber system and the proposed LNA is elaborated. The radio over fiber system and the proposed wideband multi-function receiver is discussed in section 3.1. The gate-drain mutually induced feedback LNA (GDMIF-LNA) is elaborated in chapter 3 with details including analysis, design methodology, implementation, and measurements. The prior art and the basic idea of GDMIF-LNA is elaborated in section 3.2. The performance analysis, including gain, NF, and design for bandwidth is studied in section 3.3. Stability issues are discussed in section 3.4. The circuit realization is elaborated in section 3.5, and the comparison remarks are drawn in section 3.6.

Chapter 4 includes conclusion remarks and future suggestions for further study and investment on the two projects.

2. A WIDEBAND SELF-INTERFERENCE-CANCELING RECEIVER FOR IN-BAND FULL-DUPLEX WIRELESS

A wideband self-interference-canceling receiver achieving the linearity requirements of full-duplex is proposed. The receiver architecture is 8-phase passive mixer-first. In order to achieve self-interference cancellation, quadrature components from TX replica are created, their magnitude are scaled, and the approximated current is injected to the receiver. As a proof of concept the prototype is fabricated and measured in 65 nm bulk CMOS process. More than 35 dB cancellation is measured in a single RF down-converted domain. The NF in half-duplex (HD) mode is 3.3 dB with only 2 dB degradation compared to FD mode, 5.3 dB. The receiver has adjustable 30-to-50 dB conversion gain, consumes 20-58 mW power, and achieves +6 dBm of IB-IIP_3, and +27 dBm of OB-IIP_3.

2.1 Introduction and Literature Review

The urge to connect people and objects all together demands for substantial higher bandwidth, 1000 fold higher bandwidth has been envisioned [1], which the today's RF allocated spectra, and wireless system can not cope with it. While moving to mm-wave frequency bands, with all the oportunities and related challenges [2]–[4], may provide enough bandwidth at least for few next generations, RF spectra-efficient systems can also be a part of the solution.

In-band full-duplex (IBFD) communication utilizes the same band used for transmission as the receive band. As much as unorthodox the premise sounds, due to the tremendous TX spill over on the RX. However, as the transmitted signal is prior known in the communicating node, it is ideally possible to subtract any source of self-interference (SI), and many promising solutions have addressed the issue in the literature [5]–[16]. Twice usage of a band in the entirely allocated RF spectrum sounds very desirable. Specifically, combining IBFD with opportunistic band selection of a wideband radio which offers a spectra-efficient solution.

The issue of interference cancellation has been of importance in many related applications. For

instance continuous wave (CW) radars, send a tone for determining information about the radial velocity of an object. The reflected wave contains this information which can be retrieved from the doppler frequency shift (the antenna is depicted in Fig. 2.1). As the frequency offset is quite small, cancellation of the large transmitted signal at the receiver can improve the detectable range and the receiver sensitivity. As another application of self-interference cancellation, we can mention the system of repeaters used in tunnels (depicted in Fig. 2.2) for instance to improve the coverage at impenetrable environments. Since there are multi sources, such as repeaters, needed to cover an area, it is important to cancel the interference to ameliorate the issue of echoing.

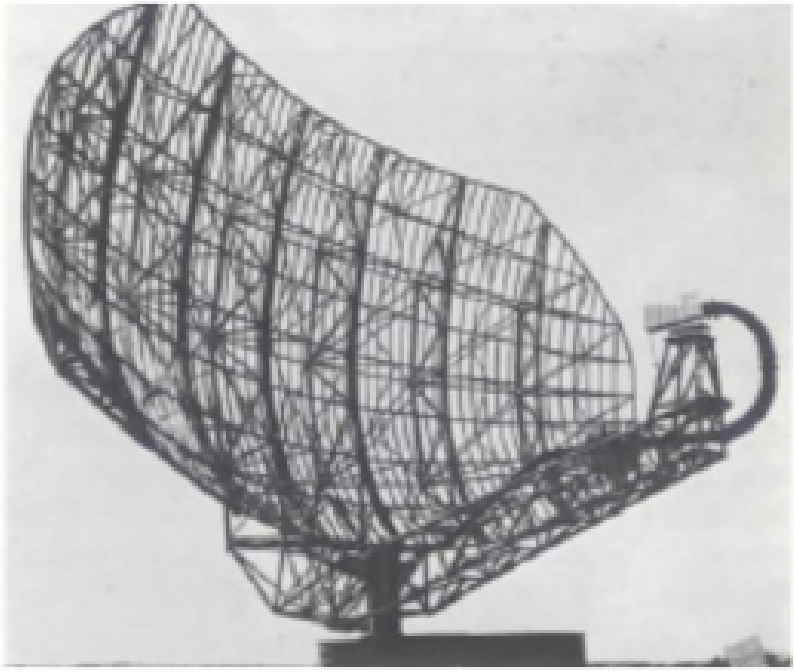


Figure 2.1: A CW radar antenna.

Competing with fully developed FDD communication systems, an IBFD receiver must well preserve the system performance while achieving substantial high level of SI suppression [17]. Characteristics such as NF and power consumption need to be maintained low enough. If the NF of receiver is deteriorated more than a certain limit in the FD mode, it would be beneficial in

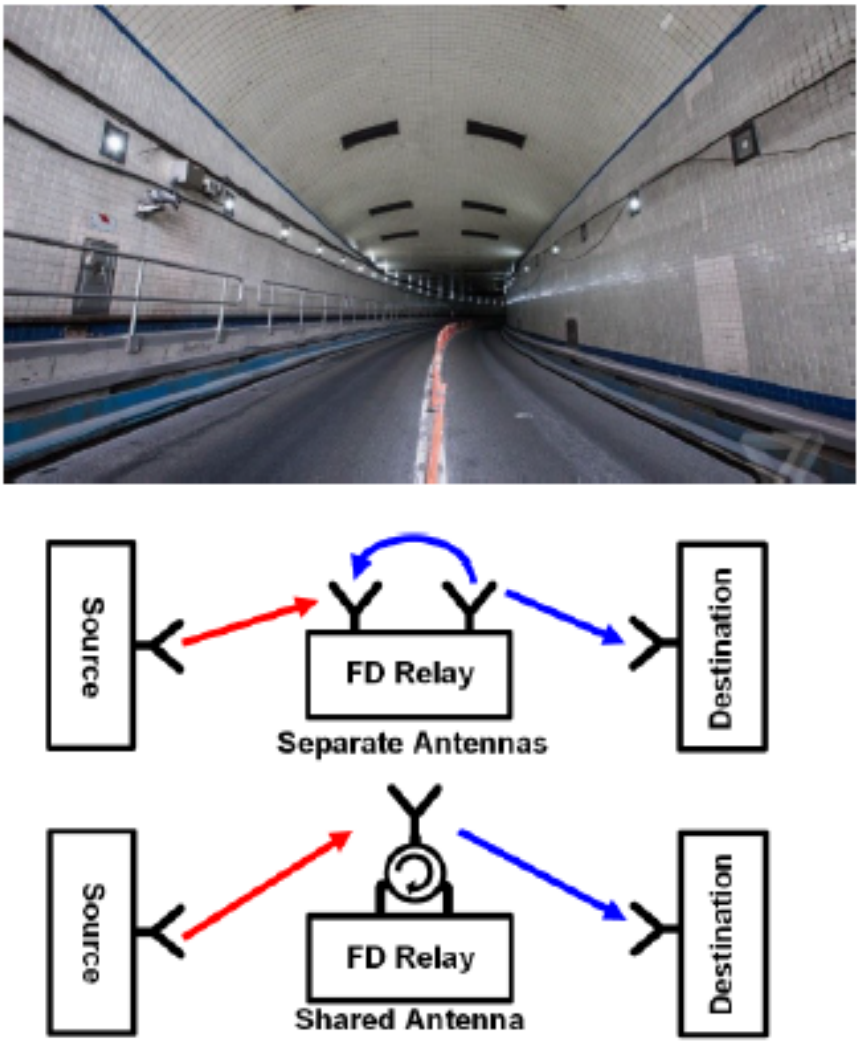


Figure 2.2: A CW radar antenna.

terms of data-rate to use half the bandwidth and send the packages with higher modulation rate in the channel with higher SNR, lower BW, and overall higher data-rate communication. The same argument holds for the power consumption, where it should be justified if the added power consumption due to the SI-canceler circuitry can be used to reduce the NF. Therefore, a large penalty in NF or power consumption can render FD system complexity redundant [18]. Furthermore, as RX is imposed to large in-band interference coming from TX, to preserve the otherwise masked by intermodulation terms desired signal, low level of linearity is not suited to this class of communi-

cation [19]–[22]. It is shown in this work that stringent in-band linearity requirement is demanded by FD which can easily limit the receiver sensitivity to an unacceptable high level.

By cadcading multiple all-pass filters, and exploiting the filters' group delay, high level of SI-cancellation (50 dB) over a wide modulation-BW in two main domains is achieved in [16]. However, due to the group-delay frequency dependency of all-pass filter, the used SI-cancellation mechanism is mostly effective for farily narrow RF-bandwidths (1.7-2.2 GHz), and does not lend itself to wideband solutions with the benefits discussed earlier. Using impedance transparency of N-path filters, two branches of LC-loaded N-path filters are used in [18] to achieve frequency equalization and non-flat frequency response emulating SI-channel over the modulation BW. Nonetheless, the implemented RF frequency range is still relatively narrow, and RX-linearity is inadequate for an FD RX (IB-IIP_3=-20 dBm). In [6], a wideband RX with linearity specifications suiting FD is described where SI-cancellation takes place by having sliced versions of the main receiver, connected to TX, and static phase rotator switches diverting the branches. Despite benefits to achieve the high BW and linearity, the SI-canceler 50 Ω input matching requirement to the external TX has rendered the use of same RX front-end architecture, repeated 31-times in the vector-modulator. This result in considerable noise injection from SI-cancellation path with large, 6 to 12 dB, NF penalty when the SI-canceler is activated. Recently, using a passive continuous vector modulator, an FD receiver with less than 1 dB NF degradation is proposed [23]. Despite the very small NF degradation, specifications such as the NF in FD mode (7 to 9 dB), IB-IIP_3 (less than -16 dBm across the band), and OB-IIP_3 of -2 dBm are far from targeted values in this work.

The architecture of the proposed SI-cancelling receiver is shown in Fig. 2.9. Using the Cartesian based synthesized SI, the SI-canceller RF-input matching is obtained with considerable less noise penalty compared to prior art; at the same time, high level of SI-cancellation is achieved in a single RF to BB cancellation domain. Targeting a wideband highly linear RX path, passive mixer-first architecture for the receiver front-end is chosen which has been shown to have a superior wideband linearity performance [24]. With the design of a very low noise TIA, a comparable with LNA-first architecture NF with superior linearity performance of mixer-first is achieved. In

addition to the RX path, the SI-canceler also demands a very high level of linearity for generating TX leakage approximation with minimal distortion. In this work, SI-approximation occurs by adjusting the magnitude of in-phase and quadrature components of TX replica. Capacitive atteuators are used for in-phase and quadrature magnitude adjustment, which manifest low added noise and high linearity compared to active counterparts. The SI approximated current is injected to the RX interface. This insures high linearity at RF, as voltage gain is entirely avoided in both the SI-canceler and likewise in the RX path.

The SI-cancelling receiver illustrated in [25], is elaborated here with details including: 1) analysis of FD receivers linearity requirement, the self-interference cancellation mechanism, and the noise performance. 2) Circuit-level implementation of the building blocks and the related design considerations. 3) Further measurements performed on the chip. In section 2.2, the in-band-full-duplex radios' considerations are studied. The effect of nonidealities is discussed in section 2.3. The architecture of the proposed SI-canceling receiver is described in section 2.4. The linearity requirement is elaborated in section 2.5. The RX performance analysis is outlined in section 2.6. Section 2.7 illustrates circuit designs and implementation for building blocks. Section 2.8 presents the measurements performed on the chip, and conclusions are drawn in section 2.9.

2.2 In-Band Full-Duplex Considerations

In order to bring the high power interference received at the receiver input to a lower than sensitivity level, cancellation in the range of 100 dB is needed. It can be reasoned that a practical and efficient cancellation needs multi-domains of cancellation as shown in Fig. 2.3. In this section, different sources of SI are studied. As the leakage can be significantly large, the interference canceler needs to cancel the SI in multiple stages to bring the overall residue to lower than RX sensitivity level.

2.2.1 Sources of SI and SI-Cancellation Domains

Considering an integrated communicating node in IBFD mode, as shown in Fig. 2.4, TX to RX leakage sources can be divided into different categories: 1) on-chip cross-talk and substrate

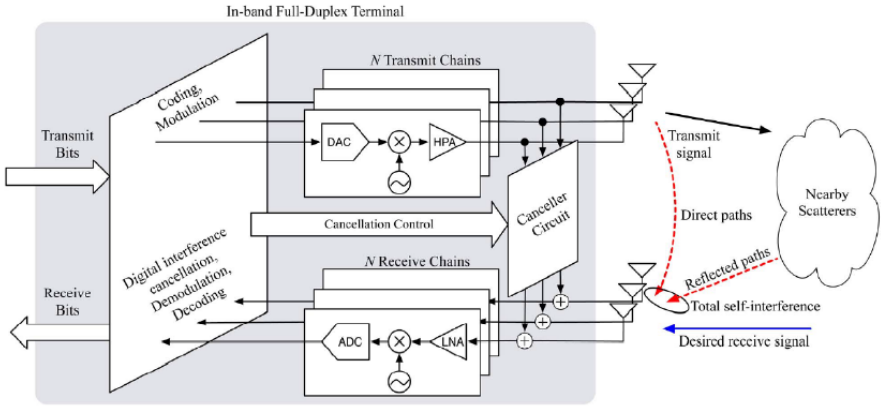


Figure 2.3: Multi-domains of cancellation needed to bring self-interference to a lower than sensitivity level.

leakage, 2) package and board leakage, 3) antenna leakage due to cross-talk or near-field coupling, and 4) environmental reflections from nearby scatterers. Assuming[1] NF of 6 dB, 10 MHz BW, and TX power of 10 dBm, the receiver noise floor will be -94 dBm. In the worst case scenario where a nearby object reflects most of the TX power back to RX, tremendous amount of SI isolation/cancellation, $>$120 dB, should be achieved in order to keep the overall post-cancellation SI at the back-end to lower than the RX sensitivity. Although it is desirable to push the entire SI cancellation processing to flexible digital domain, however, it is not a robust practical solution to achieve such high level of cancellation in a single stage [17]. Therefore, multiple domains must be used to divide the burden of cancellation. A number of popular interference cancellation techniques where the prior-known TX signal is subtracted from the RX is depicted in Fig. 2.5. In the propagation domain, crossed polarization antennas [7], adaptive reflecting impedance [8], and integrated circulator (in shared antenna systems) [9] are suggested. Aiming to subtract the SI, tapping the signal from TX to somewhere in RX, cancellation in RF [10], analog/BB, and digital [11] domain as well as inter-stage cancellation techniques, e.g., RF down-converted [5] and digital-to-analog/BB [12] are reported.

Considering on-chip cancellation domains, tapping the signal from PA output has the advantage

[1]Since there is no stipulated standard for IBFD, the specifications assumed here are based on FD requirements, limitations and other communication standards at similar frequency range.

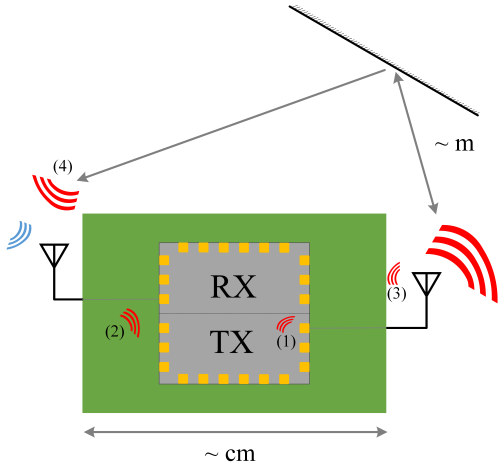


Figure 2.4: SI sources in an integrated IBFD communicating node. 1) on-chip TX-RX cross-talk and substrate leakage. 2) package and board leakage. 3) antenna leakage. 4) reflections from environmental scatterers.

of including all the TX chain non-idealities such as PA distortion and noise skirt. These effects are difficult to model or impossible to predict, due to their random nature, in other stages of TX. In this work, RF down-converted SI-cancellation is chosen to capture these effects.

2.2.2 Modulation Bandwidth Constraints

In order to constrain SI to a manageable level, the transmitted power can not be assumed very large. Therefore, IBFD is mostly suited for short range communication. Exploiting this feature and the twice usage of the spectrum that FD brings to the table, many efforts for SI cancellation in a large BW[2] is reported. Since the SI-canceler must also perform the cancellation over the entire BW of the signal, in the literature this is referred to as SI cancellation BW (SIC-BW) as a figure of merit for an IBFD system and a constraint for the modulation BW of FD transcievers.

Considering a modulated signal transmitted from the TX, this signal can be reflected from a nearby reflector and will be picked up by the RX. Depicted in Fig. 2.6, the transmitted signal undergoes a time delay denoted by τ here. The reflector has a frequency dependent reflection coefficient, $\Gamma = \alpha e^{j\theta}$. The SI is calculated as

[2]In this context the modulation BW of the BB transmitted and received signal is considered. Not to be confused with RF frequency.

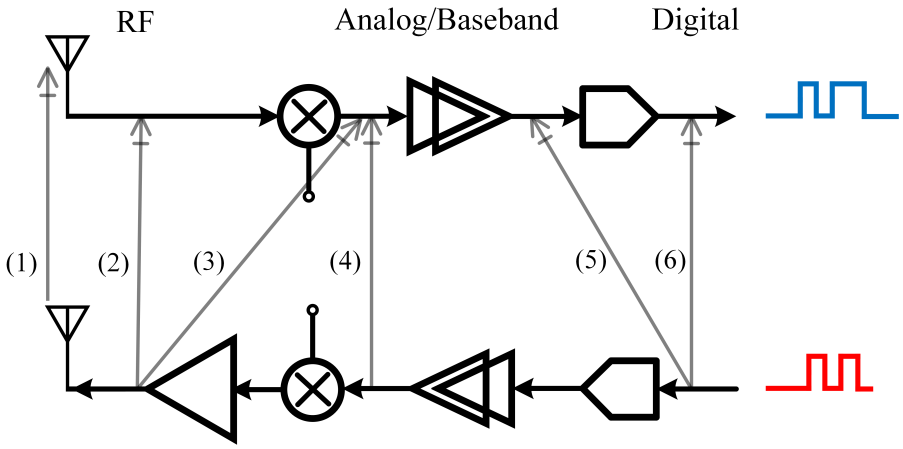


Figure 2.5: SI cancellation domains and implemented interference cancellation in the literature. 1) Propagation. 2) RF. 3) RF down-converted. 4) Analog/BB. 5) Digital-to-analog/BB. 6) Digital.

$$\mathrm{SI} = L\alpha A(t-\tau)\cos\big(\omega(t-\tau)+\varphi(t-\tau)+\theta\big). \tag{2.1}$$

Assuming isotropic antennas, the path loss is given by

$$L = \frac{\lambda^2}{16\pi^2 d_1 d_2} \tag{2.2}$$

where d_1 and d_2 are TX and RX distance from the reflector respectively, and λ is the carrier wavelength.

The goal here is to approximate the SI, knowing the transmitted signal. As there is no prior knowledge of scatterers, especially in hand-held device applications where the environment changes dynamically, this requires SI circuitry adjustment time slots during which the other communicating node turns off, and TX sends a pilot signal so as to update the received interference. The channel approximation takes place during these intervals. Generally, the SI approximation approaches are categorized into two classes, namely time-delay and phase shift. The true SI undergoes time delay, hence time-delay approach would be more accurate. It accounts for amplitude and phase dynamic which are varying by a rate depending on the modulation BW. As shown in Fig. 2.6, reflector also have a frequency dependent reflection which overall results in a complex dynamic

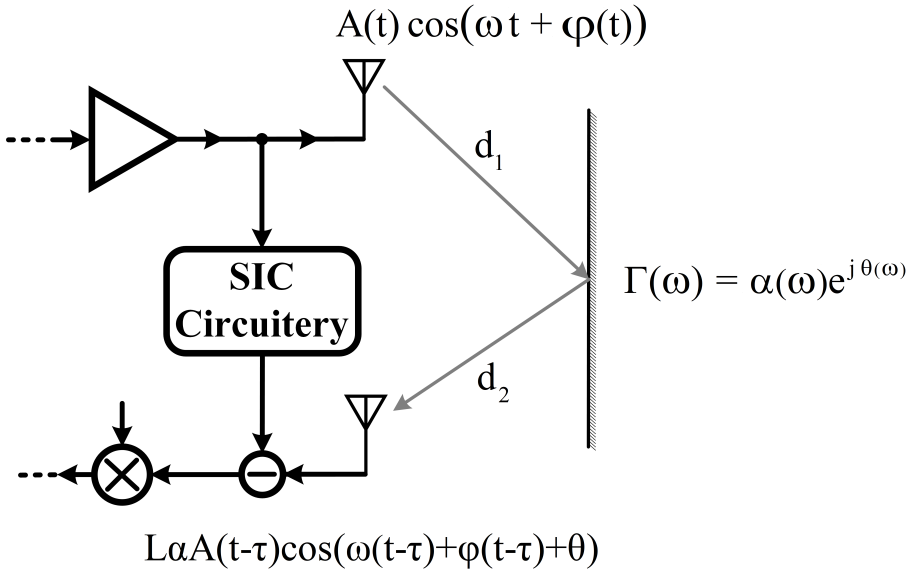


Figure 2.6: Generic view of a nearby reflector interfering with an IBFD transceiver.

frequency dependent function. In a real situation, there are multiple reflectors which make the task of approximating the overall SI and subtraction in RF/analog domain very complicated and inefficient as compared to flexible digital domain processing. As illustrated in Fig. 2.4, sources of reflection may potentially exist as near as on-chip cross-talk to as far as environmental reflectors. This translates into generation of time delays as large as nanosecond for reflectors which are only tens of centimeter away from the transceiver. Using off-chip solutions, nanosecond delays are implemented, and SI cancellation over a large BW has been achieved [13], [14]. However, daunting task of creating delays of this order has rendered on-chip state-of-the-art counterparts to maximum delay generation of 1.12 ns [15] which means for further delays where the dynamic of the modulated signal has an impact, the cancellation actually takes place very similar to the phase shift approach. That is, the multiplication of delay and angular frequency is used to produce the approximated SI phase shift as the the real time delay is out of reach.

In reality, multiple sources of SI exist, and they all appear at the RX. Summing over all the SI

and substituting $\mathrm{d_{i_{1,2}}} = \lambda \mathrm{f}\, \tau_{\mathrm{i_{1,2}}}$ in (2.2), the overall SI is given by

$$\mathrm{SI_t} = \sum_{i=1}^{m} \frac{\alpha_i}{4\omega^2 \tau_{i_1} \tau_{i_1}} A(t-\tau_i) \cos\big(\omega(t-\tau_i) + \varphi(t-\tau_i) + \theta_i\big). \tag{2.3}$$

The time delay appears in the denominator, as expected farther objects' interference reflection is attenuated due to the free space path loss. Now the transmitter signal at time $\mathrm{t} = \mathrm{t_0}$ is used to cancel the overall SI. Far objects experience more delay (τ_0), hence subtraction from the SI with the origin of transmission at $\mathrm{t} = \mathrm{t_0} - \tau_0$ can cause error. Yet this signal has gone through substantial loss and its magnitude is attenuated. Thus the transmitted signal is approximated by a constant envelope, and the phase shift approach can be used. The variations due to the modulation-BW is neglected in the front-end[3], and can be addressed by powerful digital domain process and subsequently will be canceled at the back-end.

2.3 IBFD Requirements and The Effect of Non-idealities

In the context of wideband receivers there are a number of system level treatments [26], [27] that are mostly applicable for a wideband IBFD receiver as well. In addition to these, IBFD has some unique requirements which are briefly studied here. A mixer-first receiver front-end is illustrated in Fig. 2.12. With a similar approach, linearity requirement for LNA-first, and other types of architectures can be derived which are shortly commented on.

Assuming the received signal comprises only around the carrier frequency components, namely the desired signal and the SI, $\mathrm{x(t)}$ is given by

$$x(t) = s(t)\cos(\omega_0 t + \phi(t)) + m(t)\cos(\omega_0 t + \theta(t)) \tag{2.4}$$

where the first term represents the desired signal and the second term is the leaked signal, after suppression in the propagation domain.

[3]The larger the time delay where amplitude and phase variations manifest itself more, the signal experiences more attenuation in the path. Assuming 20 MHz signal BW and 2 GHz carrier frequency, a perfect reflector at 37 cm distance can create a worst case $\pi/10$ error in the argument. The amplitude of this component will be attenuated by the free space path loss by 60 dB, and its overall effect is neglected in the front-end.

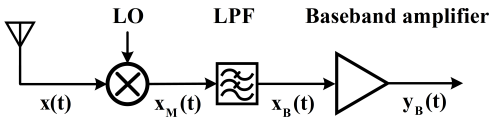


Figure 2.7: A mixer-first receiver front end.

In order to model nonlinearity effects related to the receiver, it is assumed that the filter and baseband blocks contribute negligible nonlinearity. They are designed with internal large loop gain feedback, hence their associated nonlineariy is reduced. The passband gain of the LPF is assumed to be 0 dB. The mixing action is modeled as [41], [42]

$$x_M(t) = (a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)) \cos(\omega_0 t). \tag{2.5}$$

Substituting (2.19) in (2.20), and assuming that the leaked signal is much larger than the desired signal, $\mathrm{x_B(t)}$ is approximately calculated as

$$x_B(t) \simeq \frac{a_1}{2} s(t) \cos(\phi(t)) + \frac{a_1}{2} m(t) \cos(\theta(t)) + \frac{3a_3}{4} s(t) m^2(t) \cos(\phi(t)) + \frac{3a_3}{8} m^3(t) \cos(\theta(t)). \tag{2.6}$$

It should be noted that the inter-modulation terms, not all included in (2.21), can potentially be larger than the desired signal. Therefore, they are capable of completely masking the desired signal. Removing these nonlinear terms is another important task which should be accomplished in digital domain. While in front-end stages the nonlinearity coefficients shall be kept as low as possible.

2.3.1 The Receiver Conversion-Gain

It can be verified from (2.21) that the conversion-gain of the receiver is a nonlinear function of the transmitted signal. Furthermore, both the amplitude and phase modulation of the leaked signal are varying this gain. In case where the transmitted signal is not adequately suppressed in prior

domains, the last term in (2.21) dominantly grows. This can lead to gain compression and receiver desensitization which highlights propagation domain isolation/cancellation importance. In fact, high level of transmitter isolation such as the duplexers proposed in [43]–[45] with more than 50 dB isolation can substantially reduce RX-chain linearity requirements to an attainable value.

2.3.2 Full Duplex Linearity Requirement

Aiming to extract system level linearity characteristic for an acceptable performance of the receiver, it is assumed that in order to have a detectable desired signal: *a receiver should be linear enough in FD mode that the last term in (2.21) does not grow larger than the first term which is the desired signal.* That is,

$$\left|\frac{a_1}{2}s(t)\right| > \left|\frac{3a_3}{8}m^3(t)\right|. \tag{2.7}$$

It is shown in Appendix A that by applying this condition, the in-band $\mathrm{IIP_3}$ of the mixer must satisfy

$$\mathrm{IB} - \mathrm{IIP_3} > 1.5P_T - 0.5P_{\mathrm{sen}} \tag{2.8}$$

all quantities in dBm, where $\mathrm{P_T}$ is the maximum SI power picked up by receiver. In the case of 10 dBm transmitted power and 40 dB isolation/cancellation in the propagation domain, $\mathrm{P_T}$ would be -30 dBm. $\mathrm{P_{sen}}$ denotes receiver sensitivity calculated as

$$P_{\mathrm{sen}} = -174\ \mathrm{dBm/Hz} + 10log(\mathrm{BW}) + \mathrm{NF} + \mathrm{SNR(min)}. \tag{2.9}$$

For a typical -90 dBm sensitivity, minimum requirement of IB-$\mathrm{IIP_3}$ is 0 dBm. A condition met with conservative transmit power and high propagation domain isolation/cancellation. Every 1 dB offset from this minimum will degrade receiver sensitivity by 2 dB. Assuming 40 dB isolation/cancellation in the propagation domain, the $\mathrm{IM_3}$ limited RX sensitivity as a function of IB-$\mathrm{IIP_3}$ is plotted in Fig. 2.13 for different levels of transmitter power. It is notable that the loss in

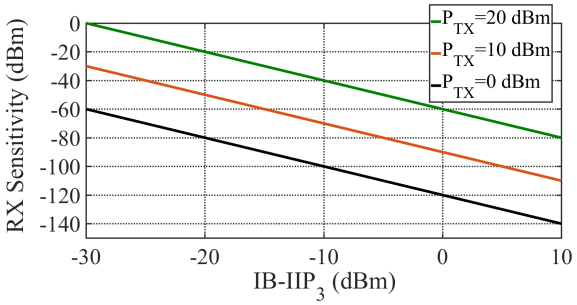


Figure 2.8: IM_3 limited sensitivity as a function of IB-IIP_3 for different levels of transmitted power, assuming 40 dB isolation/cancellation in the propagation domain.

sensitivity is so significant for relatively large TX powers that makes FD mostly suited for short-range communication. Furthermore, stringent linearity, specifically in-band linearity, is needed for FD receivers. Otherwise, the RX sensitivity would be unacceptably high.

It is noteworthy to mention that (2.23) represents the mixer linearity requirement of a mixer-first receiver which with a good approximation (neglecting baseband blocks nonlinearity) sets the entire receiver linearity. In the case for LNA-first receivers (generally gain stage preceding mixer), with a similar approach it can be shown that the IB-IIP_3 of the mixer is increased by the preceding gain stage. A very hard, if not impossible, condition to be met.

2.3.3 Harmonic Mixing

A fundamental trade-off in mixer design exists where a linear mixer is desired to avoid mixing the harmonics of LO with the RF signal. These components down-convert LO harmonics and increase the receiver susceptibility to blockers and increase the noise floor. On the other hand, linear mixers show a very poor noise and conversion-gain characteristics. A desirable feature of N-path front-end architecture, specially for 8 or larger number of phases, is the fairly valid fundamental LO approximation used in (2.20). The approximation of LO signal by 8-phase 12.5% duty cycle pulses, pushes the closest LO harmonic to $7 \times \mathrm{LO}$. As the nonlinear PA can potentially generate considerable amount of power in the harmonics, this feature mitigates the problem of harmonic mixing which otherwise could be a bottleneck for system performance.

2.3.4 Phase Noise

Here the LO phase noise is not included in the model. However, both in the context of wideband receivers [33], [34] and IBFD [35], phase noise is of prominent importance. Using the same LO for TX and RX chain makes the sources of noise highly correlated. This feature has been used in the literature [15] in order to alleviate noise floor degradation with the origin of TX noise skirt [37].

2.4 The Proposed SI-Cancelling Receiver Architecture

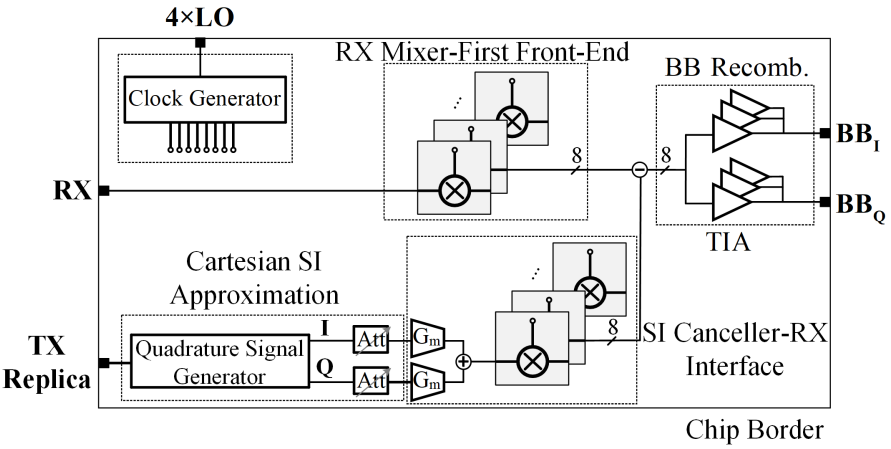


Figure 2.9: The proposed SI-cancelling receiver architecture.

The architecture of the proposed SI-cancelling receiver is illustrated in Fig. 2.9. The receiver front-end including the mixers and the following baseband TIAs is illustrated in Fig. 2.10. The receiver front-end structure is 8-phase passive mixer first. The mixer's (switch) ON-resistance and the TIA feedback resistor provide the input matching. The picked-up RF-current by the antenna is directed by the commutating switches. The RF-signal is down-converted by this process; as the down-converted to baseband currents pass through the TIA feedback resistors, the baseband voltages represented in phasor diagram of Fig. 2.10 are generated at the TIA outputs.

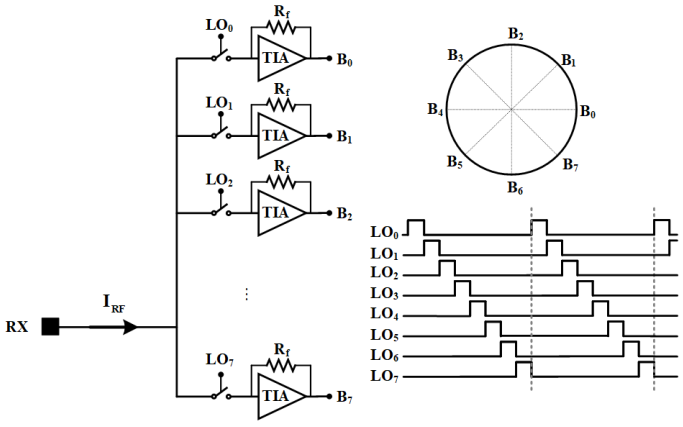


Figure 2.10: The receiver front-end. The eight non-overlapping clocked mixers and the following TIAs with down-converted baseband signals.

2.4.1 The SI-Canceler Path

The SI-cancellation path synthesizes approximation of SI. As illustrated in Fig. 2.9, first, the I/Q components are created from the TX replica. Following that, these components are scaled by capacitive attenuators. Active cancelers require less power to be coupled to the SI-canceler from TX, however, these circuits are susceptible to noise and nonlinearity which will directly add noise and distortion to the receiver. After magnitude adjustment of I/Q components, the voltages are converted to current using class-AB gm-cells which can be designed with fairly linear I-to-V characteristics [38]. The approximated SI current is down-converted by a similar to the front-end mixing process. Nonetheless, as the RF input matching constraint (to 50 Ω) here does not exist, the size of mixers can be chosen to optimize other specifications of the system. This degree of freedom is leveraged to minimize the injected current noise to the receiver with the origin of SI-path and increase SI-canceler path linearity. Both of which can be achieved by increasing the size of mixers, compared to RX mixers, which result in a lower switch resistance, hence a lower injected noise, and smaller voltage swing across the switches. The down-converted SI approximated current is subtracted from the receiver SI at the baseband, i.e., at the TIA inputs.

2.4.2 The Baseband Recombination

The eight down-converted signals need to be properly weighted to extract in-phase and quadrature baseband information while the harmonics of the LO are rejected, up to the 7th harmonic. The baseband voltages at the output of TIAs, as defined in Fig. 2.10, are weighted and summed to produce baseband in-phase and quadrature signals:

$$BB_I = B_0 + \frac{\sqrt{2}}{2}B_1 - \frac{\sqrt{2}}{2}B_3 - B_4 - \frac{\sqrt{2}}{2}B_5 + \frac{\sqrt{2}}{2}B_7 \tag{2.10}$$

$$BB_Q = \frac{\sqrt{2}}{2}B_1 + B_2 + \frac{\sqrt{2}}{2}B_3 - \frac{\sqrt{2}}{2}B_5 - B_6 - \frac{\sqrt{2}}{2}B_7 \tag{2.11}$$

which basically represent the projection of the phasor components into two perpendicular axes. The weighting factors ($\mathrm{W_i}$) accompanying branch-i baseband signal ($\mathrm{B_i}$) in effect shape the LO signal to approximate sinusoidal mixing waveform. Noting that for the down-converted baseband voltages

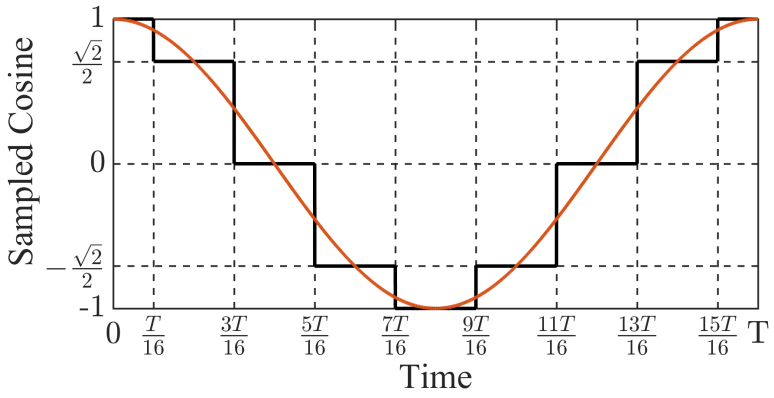
$$B_i(t) = R_f I_{RF}(t) LO_i(t) \text{ (for i} = 0, 1, 2, ..., 7) \tag{2.12}$$

Substituting in (2.10) and (2.11)

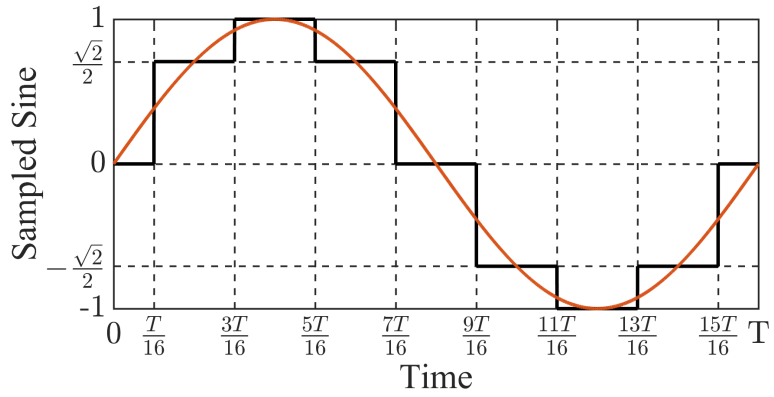
$$BB_I = R_f I_{RF}\Big[LO_0 + \frac{\sqrt{2}}{2}LO_1 - \frac{\sqrt{2}}{2}LO_3 - LO_4 - \frac{\sqrt{2}}{2}LO_5 + \frac{\sqrt{2}}{2}LO_7\Big] \tag{2.13}$$

$$BB_Q = R_f I_{RF}\Big[\frac{\sqrt{2}}{2}LO_1 + LO_2 + \frac{\sqrt{2}}{2}LO_3 - \frac{\sqrt{2}}{2}LO_5 - LO_6 - \frac{\sqrt{2}}{2}LO_7\Big]. \tag{2.14}$$

The effective mixing siganls (effective LO), the terms in brackets, are depicted in Fig. 2.11 which show two 3-bit sampled sinusoid with $\frac{\pi}{2}$ phase shift. This harmonic rejection property, introduced in [39], [40], greatly relaxes receiver susceptibility to out-of-band blockers at LO har-



(a)



(b)

Figure 2.11: In-phase and quadrature sampled mixing signals. (a) A 3-bit sampled cosine waveform. (b) A 3-bit sampled sine waveform.

monics. The sampled sine (SS) and sampled cosine (SC), illustrated in Fig. 2.11, are respectively odd and even function of time, by the choice of the time origin, as such, they can be represented by the following Fourier series representations

$$SC(t) = \sum_{n=1}^{\infty} a_n \cos(2\pi n f_{LO} t) \tag{2.15}$$

$$SS(t) = \sum_{n=1}^{\infty} b_n \sin(2\pi n f_{LO} t) \tag{2.16}$$

Table 2.1: Effective LOs Fourier series coefficients up to the 16th non-zero coefficient.

SC non-zero Fourier series coefficients	**SS non-zero Fourier series coefficients**
$\mathrm{a}_1 = 0.9745$	$\mathrm{b}_1 = 0.9745$
$\mathrm{a}_7 = 0.1392$	$\mathrm{b}_7 = -0.1392$
$\mathrm{a}_9 = -0.1083$	$\mathrm{b}_9 = -0.1083$
$\mathrm{a}_{15} = -0.0650$	$\mathrm{b}_{15} = 0.0650$

where the Fourier series coefficients are calculated as

$$a_n = \begin{cases} \frac{2(2-\sqrt{2})\,\sin\frac{n\pi}{8} + 2\sqrt{2}\,\sin\frac{3n\pi}{8}}{n\pi} & \text{for n: odd} \\ 0 & \text{for n: even} \end{cases} \tag{2.17}$$

and

$$b_n = \begin{cases} \frac{2\sqrt{2}\,\cos\frac{n\pi}{8} + 2(2-\sqrt{2})\,\cos\frac{3n\pi}{8}}{n\pi} & \text{for n: odd} \\ 0 & \text{for n: even} \end{cases} \tag{2.18}$$

It can be shown that[4] $|\mathrm{a_n}| = |\mathrm{b_n}|$. The nonzero Fourier series coefficients up to the 16th coefficient are illustrated in Table. 2.1.

2.5 Full-Duplex Linearity Requirements

IBFD has specific linearity requirements which are studied in this section. A mixer-first receiver front-end is illustrated in Fig. 2.12. With a similar approach, linearity requirement for LNA-first, and other types of architectures can be derived which are shortly commented on later in this section.

Assuming the received signal comprises only around the carrier frequency components, namely the desired signal and the SI, $\mathrm{x(t)}$ is given by

$$x(t) = s(t)\cos(\omega_0 t + \phi(t)) + m(t)\cos(\omega_0 t + \theta(t)) \tag{2.19}$$

[4]For $\mathrm{n} = 4\mathrm{k}+1$, $\mathrm{a_n} = \mathrm{b_n}$; and for $\mathrm{n} = 4\mathrm{k}+3$, $\mathrm{a_n} = -\mathrm{b_n}$ $\mathrm{k} \in \mathrm{W}$.

where the first term represents the desired signal and the second term is the transmitter leaked signal, after suppression in the propagation domain.

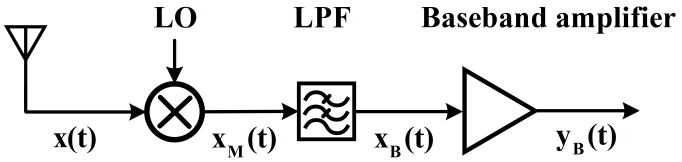


Figure 2.12: A mixer-first receiver front end.

In order to model nonlinearity effects related to the receiver, it is assumed that the filter and baseband blocks contribute negligible nonlinearity. They are designed with internal large loop gain feedback, hence their associated nonlineariy is reduced. The passband gain of the LPF is assumed to be 0 dB. The mixing action is modeled as [41], [42]

$$x_M(t) = (a_1 x(t) + a_2 x^2(t) + a_3 x^3(t)) \cos(\omega_0 t). \tag{2.20}$$

Substituting (2.19) in (2.20), and assuming that the leaked signal is much larger than the desired signal, $\mathrm{x_B(t)}$ is approximately calculated as

$$x_B(t) \simeq \frac{a_1}{2} s(t) \cos(\phi(t)) + \frac{a_1}{2} m(t) \cos(\theta(t)) + \frac{3a_3}{4} s(t) m^2(t) \cos(\phi(t)) + \frac{3a_3}{8} m^3(t) \cos(\theta(t)). \tag{2.21}$$

It should be noted that the inter-modulation terms can potentially be larger than the desired signal. Therefore, they are capable of completely masking the desired signal. It can be verified from (2.21) that the conversion-gain of the receiver is a nonlinear function of the transmitted signal. Furthermore, both the amplitude and phase modulation of the leaked signal are varying this gain. In case where the transmitted signal is not adequately suppressed in prior domains of cancel-

lation, the last term in (2.21) dominantly grows. This can lead to gain compression and receiver desensitization which highlights propagation domain isolation/cancellation importance. In fact, high level of transmitter isolation such as the duplexers proposed in [43]–[45] can substantially reduce RX-chain linearity requirements to an attainable value.

Aiming to extract system level linearity characteristic for an acceptable performance of the receiver, it is assumed that in order to have a detectable desired signal: *a receiver should be linear enough in FD mode such that the last term in (2.21) does not grow larger than the first term which is the desired signal.* That is,

$$\left|\frac{a_1}{2}s(t)\right| > \left|\frac{3a_3}{8}m^3(t)\right|. \tag{2.22}$$

It is shown in Appendix A that by applying this condition, the IB-IIP$_3$[5] of the mixer must satisfy

$$\mathrm{IB-IIP_3} > 1.5P_T - 0.5P_{\mathrm{sen}} \tag{2.23}$$

all quantities in dBm, where $\mathrm{P_T}$ is the maximum SI power picked up by receiver, and can be calculated by subtracting propagation domain cancellation/isolation from the TX power. For example, in the case of 0 dBm transmitted power and 30 dB isolation/cancellation in the propagation domain, $\mathrm{P_T}$ would be -30 dBm. $\mathrm{P_{sen}}$ denotes receiver sensitivity calculated as

$$P_{\mathrm{sen}} = -174\ \mathrm{dBm/Hz} + 10\log(\mathrm{BW}) + \mathrm{NF} + \mathrm{SNR(min)}. \tag{2.24}$$

For a typical -90 dBm sensitivity, minimum requirement of IB-IIP$_3$ is 0 dBm. A condition met with conservative transmit power and high propagation domain isolation/cancellation. Every 1 dB offset from this minimum will degrade receiver sensitivity by 2 dB. The $\mathrm{IM_3}$ limited RX sensitivity as a function of IB-IIP$_3$ is plotted in Fig. 2.13 for different levels of $\mathrm{P_T}$. It is notable that the loss in sensitivity is so significant for relatively large TX powers that makes FD mostly suited for short-range communication. Furthermore, stringent linearity, specifically in-band linearity, is needed for

[5]This is the conventional definition of the IB-IIP$_3$ in the two-tone test.

FD receivers. Otherwise, the RX sensitivity would be unacceptably high.

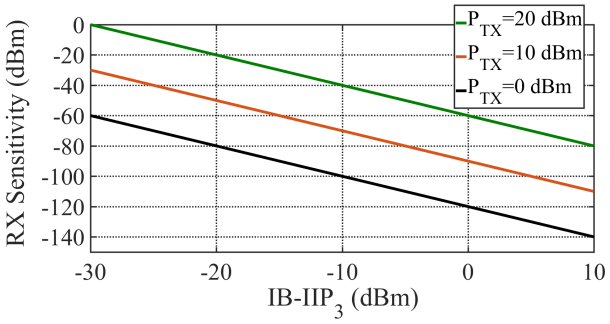


Figure 2.13: IM_3 limited sensitivity as a function of IB-IIP_3 for different levels of P_T (TX power subtracted by propagation domain isolation/cancellation).

It is noteworthy to mention that (2.23) represents the mixer linearity requirement of a mixer-first receiver which with a good approximation (neglecting baseband blocks nonlinearity) sets the entire receiver linearity. In the case for LNA-first receivers (generally gain stage preceding mixer), with a similar approach it can be shown that the IB-IIP_3 of the mixer is increased by the preceding gain stage. A very hard, if not impossible condition to be met.

2.5.1 Proof of The In-Band Linearity Requirement

The objective is to retrieve the desired signal in the presence of large SI. In such circumstance, considering (2.21), the desired signal after down-conversion should be larger than IM_3 products to be detectable. This set the condition

$$\left|\frac{a_1}{2}s(t)\cos(\phi(t))\right| > \left|\frac{3a_3}{8}m^3(t)\cos(\theta(t))\right|. \tag{2.25}$$

As there is no prior knowledge of the SI phase, considering $|\cos\,\theta| = 1$ allow us to design in the possible worst-case scenario. In addition, inasmuch as the RX structure retrieves both I, and Q components, the desired signal phase is also of no importance and both the magnitude and phase can be retrieved. Therefore, the RX third order nonlinear coefficient needs to satisfy

$$\left|\frac{a_1}{2}s(t)\right| > \left|\frac{3a_3}{8}m^3(t)\right|. \tag{2.26}$$

By definition the amplitude of $\mathrm{IIP_3}$ for a non-linear system such as described by (2.20) is calculated as

$$\mathrm{A_{IIP_3}} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|}\ (\mathrm{V}) \tag{2.27}$$

substituting in (2.26),

$$\mathrm{A^2_{IIP_3}} > \sqrt{\frac{\left\langle \mathrm{m^2(t)} \right\rangle^3}{\left\langle \mathrm{s^2(t)} \right\rangle}}. \tag{2.28}$$

The maximum rms of m(t) is when the maximum SI leakage is imposed to the receiver. This is obtained from propagation domain isolation/cancellation subtracted from TX power, which was named $\mathrm{P_T}$. The minimum rms of s(t) is the minimum received signal power which receiver shall detect, that translates to the receiver sensitivity ($\mathrm{P_{sen}}$). As such,

$$P_T = 10\log(10\left\langle \mathrm{m^2(t)} \right\rangle_{\mathrm{Max}})\ (\mathrm{dBm}) \tag{2.29}$$

$$P_{\mathrm{sen}} = 10\log(10\left\langle \mathrm{s^2(t)} \right\rangle_{\mathrm{min}})\ (\mathrm{dBm}) \tag{2.30}$$

which by substituting in (2.26), and using

$$\mathrm{IIP_3} = 10\log(10\mathrm{A^2_{IIP_3}})\ (\mathrm{dBm}) \tag{2.31}$$

proves (2.23).

2.6 The Performance Analysis

The entire diagram of the SI-canceler RX is illustrated in Fig. 2.14. The SI-canceler generates differential SI approximated currents ($\mathrm{SIC_p}$ and $\mathrm{SIC_n}$) and injects them to the RX interface which is composed of 8 branches. In the RX front-end section, each branch has a mixer connected to RX

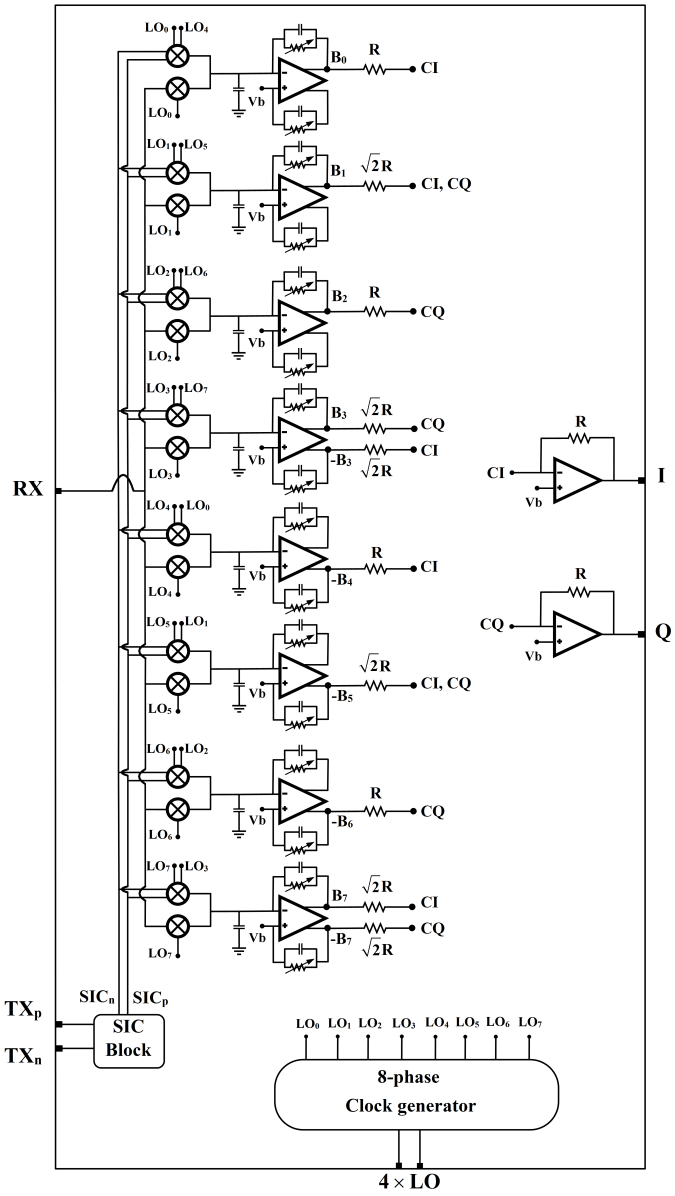


Figure 2.14: The complete SI-canceler RX diagram.

and is driven by an associated LO. The SIC currents at each corresponding branch are driven by differential LOs. Considering one of the branches, as depicted by Fig. 2.15, the $\frac{\mathrm{T_{LO}}}{2}$ apart LOs have fundamental Fourier series coefficients negative of each other. As a result, the SIC currents are subtracted from each other which performs differential to single-ended conversion. This net SIC current, $\mathrm{SIC} = \mathrm{SIC_p} - \mathrm{SIC_n}$, is subtracted from the RX, following the mixers.

Considering Fig. 2.15, in the vicinity of $\mathrm{f_{LO}}$ the received signal is comprised of the desired

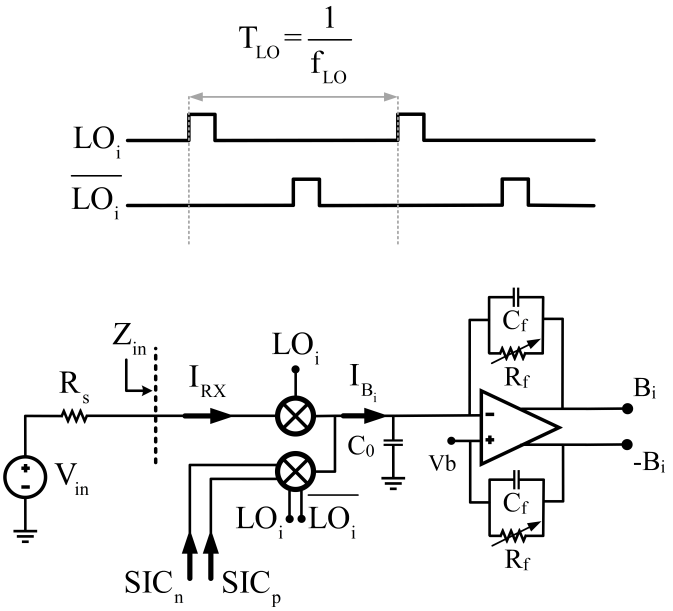


Figure 2.15: The i^{th} branch of the RX-SI-canceler interface with the associated LO signals.

signal (s) and a net SI leakage (l). At such frequencies, $\mathrm{Z_{in}}(\mathrm{f_{LO}}) = \mathrm{Z_0}$. Therefore, the current conducted by the i^{th} RX mixer is

$$I_{RX} = \frac{V_{in}}{Z_0} = s + l. \tag{2.32}$$

Following the mixers, both the RX and SIC currents are down-converted to the baseband. The capacitor at the TIA input ($\mathrm{C_0}$) short-circuits all other mixing components. Therefore, the baseband current which flows through the feedback resistor in the Fourier domain is given by

$$I_{B_i} = \sum_{\pm} \mathcal{F}_{i_{\pm 1}} \{S + [L - (SIC_p - SIC_n)]\}_{(f \mp f_{LO})} \tag{2.33}$$

where the upper case signals represent the Fourier transform and $\mathcal{F}_{i_{\pm 1}}$ is the fundamental Fourier coefficient of $\mathrm{LO_i}$ calculated as

$$\mathcal{F}_{i_{\pm 1}} = \frac{\sin(\frac{\pi}{8})}{\pi} e^{\mp j \frac{\pi(2i+1)}{8}}, \quad i = 0, 1, 2, ..., 7 \tag{2.34}$$

Assuming the SI approximation occurs perfectly, that is $\mathrm{L} = (\mathrm{SIC_p} - \mathrm{SIC_n})$, only the down-converted desired signal flows through the feedback resistor and creates the baseband voltages at the TIA outputs, which are

$$B_i = \sum_{\pm} \mathcal{F}_{i_{\pm 1}} R_f S_{(f \mp f_{LO})}. \tag{2.35}$$

These components are added with the weightings calculated in (2.10) and (2.11) to create the baseband I-, and Q-signals. Illustrated in Fig. 2.14, this process occurs by summing the required components by utilizing two op-amps. The weighting coefficients are realized by the ratio of the associated branch summing resistor. The sign is realized by choosing the required polarity of the differential-output TIA.

2.6.1 The Signal Analysis

The implementation of the receiver front-end incorporated with the SI-canceler interface is illustrated for a signle branch in Fig. 2.15. N-path, also known as M-phase structres are extensively studied in the literature [46]–[52] using LTV analysis. Andrew and Molnar also studied these receivers and proposed a useful LTI model [53], [54] for convenient yet accurate analysis of mixer-first receivers. However, here the SI-cancelling path added to the RX chain needs to be taken into account, therefore, the LTI equivalent model does not capture the whole picture. The LTV analysis is used here to gain insight from the system performance.

2.6.1.1 Receiver Input: Matching And Filtering Properties

The input of the receiver is modeled as depicted in Fig. 2.16. Each passive mixer is shown by a switch in series with a resistance. Only one of the eight switches is ON at a given time, with switch ON-resistance denoted by $\mathrm{R_{SW}}$, therefore all the eight resistors can be brought to the branch connected to RX. The impedance seen from each switch path is named $\mathrm{Z_{BB}}$. This impedance includes three parallel impedance terms: TIA, $\mathrm{C_0}$, and the SI-path loading. Due to the parallel capacitance, $\mathrm{Z_{BB}}$ only has non-zero values for baseband components. The parallel capacitor bypasses higher mixing products to the ground. The RX input impedance is calclated in [49], and around $\mathrm{f_{LO}}$ is

given by

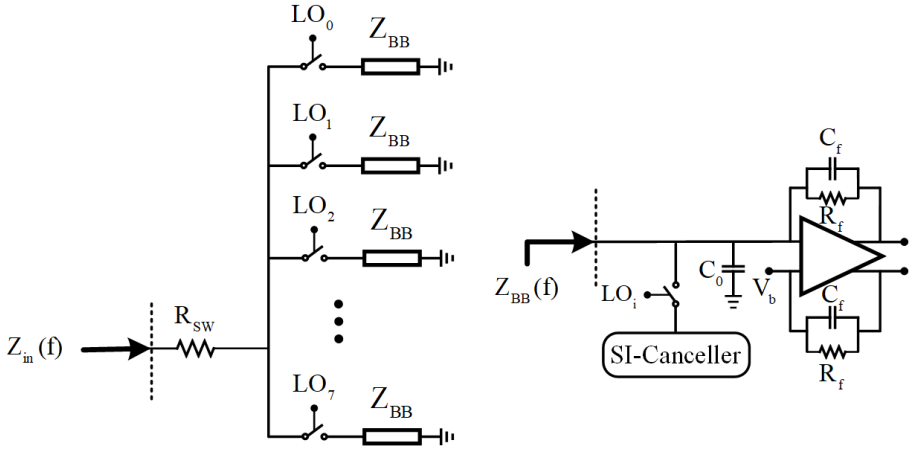


Figure 2.16: The receiver's input equivalent circuit model, and one of the 8-path BB impedance seen from the RX switch side.

$$Z_{in}(f) = R_{SW} + \frac{8\sin^2(\pi/8)}{\pi^2}[Z_{BB}(f - f_{LO}) + Z_{BB}(f + f_{LO})]. \tag{2.36}$$

As the out-of-band rejection increases by decreasing the switch resistance [49], $\mathrm{R_{SW}}$, from filtering point of view it is beneficial to satisfy the matching condition by choosing as small as possible switch resistance. However, decreasing $\mathrm{R_{SW}}$, requires bulky transistors which put an upper limit on the frequency of operation due to the parasitic capacitors. In addition, such bulky transistors require considerable power from LO circuitry to be driven. Having this trade-off in mind, switch on-resistance of 20 Ω is chosen. Fig. 2.17 shows the simulated receiver $\mathrm{S_{11}}$ at different frequencies with and without SI-cancellation path.

2.6.1.2 RX Conversion-Gain

The effective LO signals were discussed earlier and their Fourier series coefficients were calculated. Following that discussion, and considering the model shown in Fig. 2.18. The RX conversion gain from the vicinity of $\mathrm{f = f_{LO}}$ to the baseband, where the gain of the op-amp can be assumed very large, is calculated as

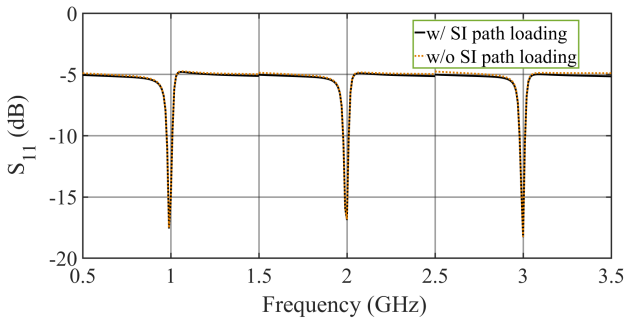


Figure 2.17: The simulated receiver tuned S_{11} at 1, 2, and 3 GHz, with and without SI-cancellation path. Each peak represents the receiver input matching at a carrier with 1 GHz bandwidth.

$$A_v = \frac{a_1 R_f}{2(Z_{in}(f) + R_S)(1 + j2\pi R_f C_f(f \mp f_{LO}))}\Bigg|_{f \simeq \pm f_{LO}} \tag{2.37}$$

The feedback capacitor appears as a first-order LPF in the transfer function with 3-dB bandwidth set to the RX BW, 10 MHz. The shunt capacitor (C_0) bypasses out-of-band signals to the ground while it is open-circuit for the in-band signals. Fig. 2.19 illustrates the simulated gain of the receiver with and without the loading of the SI-cancellation path at 2 GHz RF-frequency. As expected, the loading of the SI path has a negligible effect on the gain.

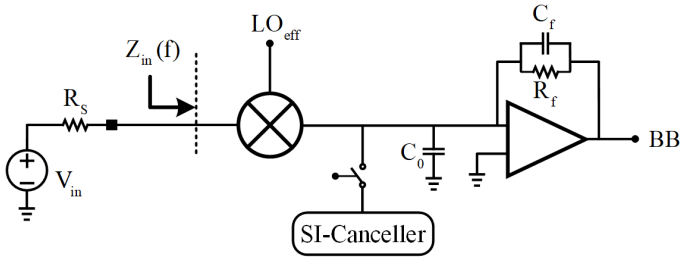


Figure 2.18: The effective RX down-conversion path.

2.6.2 Noise Analysis

The noise model of the receiver is depicted in Fig. 3.9. The dominant noise sources are illustrated which are: 1) RX-switch thermal noise ($\overline{V^2_{SW-RX}}$). 2) The op-amp input-referred noise

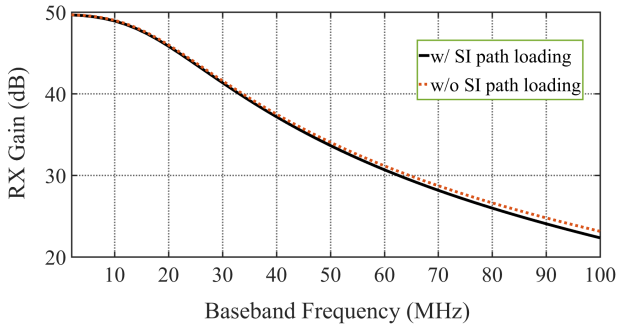


Figure 2.19: The simulated receiver gain at 2 GHz RF-frequency with and without the loading of the SI-cancellation path.

($\overline{V^2_{op}}$). 3) The feedback resistor thermal noise ($\overline{V^2_{R_f}}$). 4) The SI-canceler switch thermal noise ($\overline{V^2_{SW-SIC}}$); 5) and the SI-canceler injected noise ($\overline{I^2_{SIC}}$).

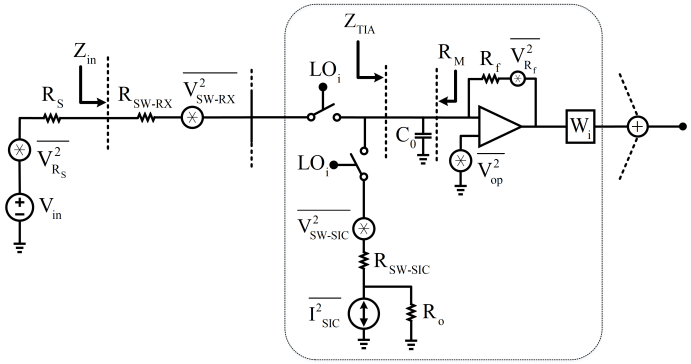


Figure 2.20: The model for noise analysis of the SI-canceler receiver. The $\mathrm{i^{th}}$ branch is depicted which is representative of the 8 branches. The dominant sources of noise are illustrated.

By definition, NF of a two-port network is given by

$$\mathrm{NF} = 1 + \frac{N_O}{N_{R_S}} \tag{2.38}$$

where $\mathrm{N_{R_S}}$ is the output noise due to the source resistance, and $\mathrm{N_O}$ is the output noise due to other noise sources, which is the sum of output noise from the aforementioned 5 noise sources. The output noise from each of the noise sources are calculated.

Not only input noise around LO but also all the other harmonics (with non-zero effective LO Fourier series coefficients) are down-converted, and appear at the baseband; therefore,

$$N_{R_S} = \overline{V_{R_S}^2}\, R_f^2 \sum_{n=1}^{\infty} \frac{|a_n|^2}{|R_S + Z_{in}|^2}. \tag{2.39}$$

2.6.2.1 RX-switch thermal noise

Similar to $\mathrm{R_S}$, the noise from RX-switch is given by,

$$N_{O,\mathrm{SW-RX}} = \overline{V_{\mathrm{SW-RX}}^2}\, R_f^2 \sum_{n=1}^{\infty} \frac{|a_n|^2}{|R_S + Z_{in}|^2}. \tag{2.40}$$

2.6.2.2 The op-amp input-referred noise

It can be shown that, assuming $(\mathrm{R_S} + \mathrm{R_{SW-RX}})\mathrm{C_0} \gg \mathrm{T_{LO}}$ [53], the resistance seen from the TIA to the mixer, as illustrated in Fig. 3.9, is given by

$$R_M = \frac{7}{8 f_{LO} C_0}. \tag{2.41}$$

Using this, the noise from the op-amps is calculated as

$$N_{O,\,op} = \overline{V_{op}^2}(1 + \frac{R_f}{R_M})^2 \sum_{i=0}^{7} |W_i|^2 \tag{2.42}$$

where $\mathrm{W_i}$ is the baseband recombination coefficient, calculated in (2.10), (2.11) for the associated $\mathrm{i^{th}}$ branch. For both $\mathrm{BB_I}$ and $\mathrm{BB_Q}$, $\sum_{\mathrm{i=0}}^{7} |\mathrm{W_i}|^2 = 4$.

2.6.2.3 The feedback resistor thermal noise

The feedback resistors' noise appear at the TIA output. Subsequently, each component is weighted by the recombination circuit. Thus,

$$N_{O,\,R_f} = \overline{V_{R_f}^2} \sum_{i=0}^{7} |W_i|^2. \tag{2.43}$$

$$N_{O,\mathrm{SW-SIC}} = \overline{V^2_{\mathrm{SW-SIC}}} \sum_{n=1}^{\infty} |\frac{a_n(R_S + R_{\mathrm{SW-RX}})R_f}{(Z'_{in} + R_o)(Z_{\mathrm{TIA}} + R_S + R_{\mathrm{SW-RX}})}|^2 \tag{2.44}$$

$$N_{O,\mathrm{SIC}} = \sum_{n=1}^{\infty} \overline{I^2_{\mathrm{SIC}}} |\frac{a_n(R_S + R_{\mathrm{SW-RX}})R_f R_o}{(Z'_{in} + R_o)(Z_{\mathrm{TIA}} + R_S + R_{\mathrm{SW-RX}})}|^2 \tag{2.45}$$

2.6.2.4 The SI-canceler switch thermal noise

the SI-canceler switch resistance has thermal noise components around LO as well as harmonics. The accumulated summation of these folded noise is calculated as (2.44).

2.6.2.5 the SI-canceler injected noise

similarly, the noise from the SI-canceler circuit is calculated as (2.45) where

$$Z'_{in}(f) = R_{\mathrm{SW-SIC}} + \frac{8\sin^2(\pi/8)}{\pi^2}[Z'_{BB}(f - f_{LO}) + Z'_{BB}(f + f_{LO})], \tag{2.46}$$

and

$$Z'_{BB} = Z_{\mathrm{TIA}}||(R_S + R_{\mathrm{SW-RX}}). \tag{2.47}$$

The detail for the derivation is explained in Appendix B.

The prediction of NF based on the analysis is compared with simulation in Fig. 2.21 for FD and HD mode which shows a close agreement, and verifies the analysis. For the HD mode, only the first three noise sources: RX-switch thermal noise, the op-amp input-referred noise, and the feedback resistor thermal noise is included. In the FD mode all the five noise sources are included.

2.6.2.6 SI- Cancellation Path Noise Contribution

In this section, the noise contribution of the SI-cancellation path is calculated. Fig. 3.9 shows the equivalent noise circuit with all the major noise sources included. For the calculation of SI-cancellation path noise contribution, this model is simplified to Fig. 2.22. Starting from calculation of $\mathrm{R_T}$: assuming a current stimulus is connected to the reference point, aiming to calculate $\mathrm{R_T}$. It

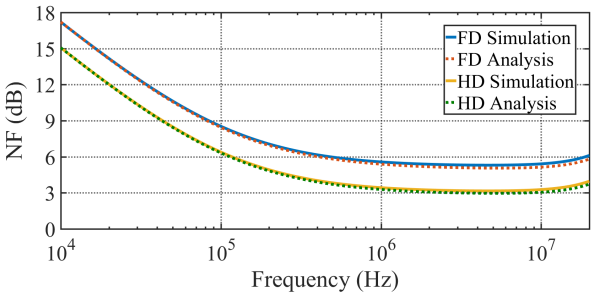


Figure 2.21: Comparison between analyzed NF in FD and HD mode with simulation.

is observed that in time-domain, irrespective of which RX-switch conducting the current, one of the 8 RX-switches passes the current to $\mathrm{R_S + R_{SW-RX}}$. Therefore,

$$R_T = R_S + R_{\mathrm{SW-RX}}. \tag{2.48}$$

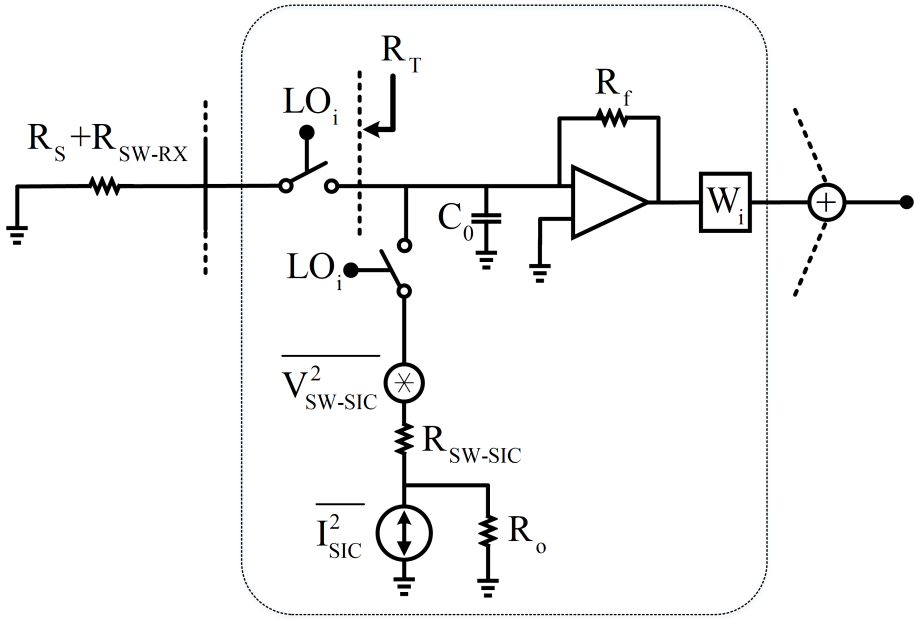


Figure 2.22: The model for noise calculation of the SI-cancellation path.

Making this observation, by analogy with the analysis for receiver input, the noise model is

equivalent to Fig. 2.23. Similar to receiver's input equation governs this model which was discussed in section IV regarding the input impedance and LO to BB gain of the RX, by substituting

$$Z'_{BB} = Z_{\mathrm{TIA}}||R_T \tag{2.49}$$

Same equations can be used. However, the noise sources in Fig. 2.23 have components both around LO as well as harmonics. Accounting for the LO and harmonics, the output noise due to the SIC-switch thermal noise is given by

$$N_{O,\,\mathrm{SW-SIC}} = \overline{V^2_{\mathrm{SW-SIC}}} \sum_{n=1}^{\infty} |\frac{a_n R_T R_f}{(Z'_{in} + R_o)(Z_{\mathrm{TIA}} + R_T)}|^2. \tag{2.50}$$

Similarly, the output noise due to the SI-canceller injected noise is given by

$$N_{O,\,\mathrm{SIC}} = \sum_{n=1}^{\infty} \overline{I^2_{\mathrm{SIC}}} |\frac{a_n R_T R_f R_o}{(Z'_{in} + R_o)(Z_{\mathrm{TIA}} + R_T)}|^2. \tag{2.51}$$

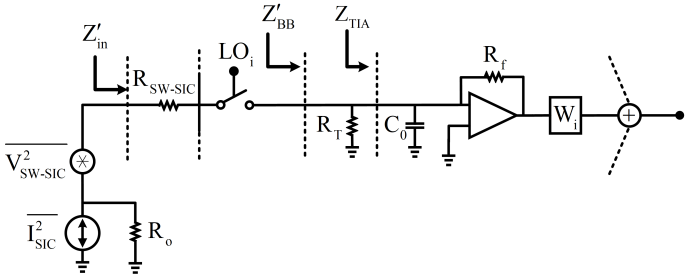


Figure 2.23: Noise model of the SI-cancellation path, using the analogy of the receiver input.

2.6.3 Design Considerations

From both the analysis and simulation it can be verified that reducing RX-switch resistance will reduce NF. This is expected by inspection as well. Since the RX-switch thermal noise components appear at the output with the noise folded terms whereas the feedback resistance thermal noise

only appears around the baseband frequency. In addition to this, as RX-switch resistance becomes smaller, there is a smaller voltage swing around it (as the RF current passes through it), resulting in higher switch linearity.

For the case of SI-canceler path mixers, the 50 Ω matching constraint does not exist. Therefore, wider transistors can be used. However, these large devices are power hungry to drive. They demand extra buffer stages following clock generation. It is beneficial to increase their size insofar as their noise contribution is by some margin less than RX-switches, in order to have an acceptable compromise between NF and power consumption. The parametric sweep study of noise contribution of SI-path mixer, and its contribution to the total output noise is illustrated in Fig. 2.24. The chosen size for the mixers are detailed in the next section.

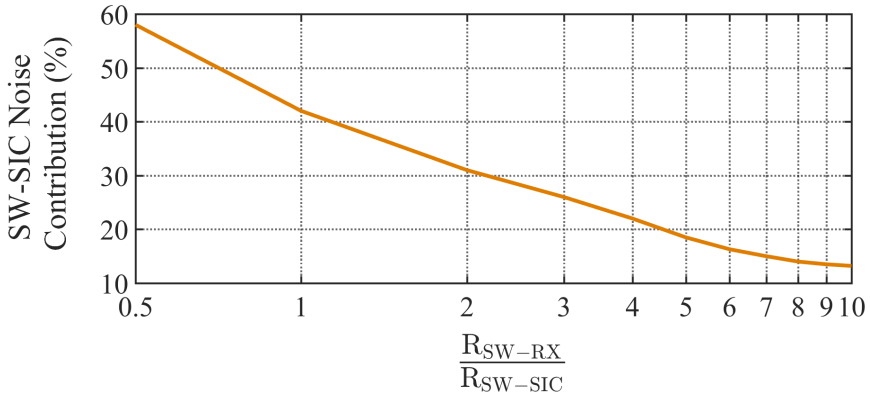


Figure 2.24: Contribution of SI-path switch thermal noise to the total output noise.

In addition to the SI-canceler switches, there is another noise source from the SI-canceler stage denoted by $\overline{I^2_{SIC}}$ in Fig. 3.9. The dominant contributors to this noise source are the Gm-cells (Fig. 2.25). Non-minimum length devices are used to increase the output resistance (R_O) and reduce the associated noise.

Simulation shows the noise of op-amp can be a bottle-neck for noise performance. Of crucial importance is the flicker noise of the op-amp. As there is no gain stage before the mixer, and RX

architecture is direct-conversion, it is very important to design a very low flicker noise op-amp which will be discussed in the next section.

2.7 The Circuit Implementation

The circuit and transistor level implementation, and related analysis of the building blocks are presented in this section.

2.7.1 The SI-canceler Performance

The implemented SI-canceler is illustrated in Fig. 2.25. The TX replica is passed through an RLC network to generate the in-phase and quadrature component. As the TX replica is from an off-chip source, it is needed to have RF-input matching. It is shown in [55] that this RLC network is capable of providing RF-input matching and generating quadrature signals over a wide bandwidth. The quadrature voltages, as named in Fig. 2.25, are related to each other as

$$\frac{V_I}{V_Q} = \frac{V_{I_p} - V_{I_n}}{V_{Q_p} - V_{Q_n}} = \frac{s^2 + \frac{R}{L}s - \frac{1}{LC}}{-s^2 + \frac{R}{L}s + \frac{1}{LC}}. \tag{2.52}$$

For covering the large targeted BW, a low-Q resonator is needed. As there is not much room to compromise on the TX replica input matching, this mostly translates to a large inductor value. With having the trade-off between I-Q generation precision, acceptable RF-input matching, and consumed area in mind, the following values are chosen for the RLC network: $\mathrm{R} = 260\,\Omega$, $\mathrm{L} = 16\,\mathrm{nH}$, and $\mathrm{C} = 1\,\mathrm{pF}$. Illustrated in Fig. 2.26, the magnitude response of $\frac{\mathrm{V_I}}{\mathrm{V_Q}}$ does not have frequency dependency. However, the phase response has around 20° variation in the frequency range of operation from the intended 90° phase.

Following the quadrature signal generator, the differential signals are applied to 7-bits capacitive attenuators. The magnitude of the components are adjusted in this stage, to synthesize the desired SI approximation in the Cartesian plane. Four attenuators are used for the respective branches with a similar structure. Nonetheless, the differential in-phase voltages ($\mathrm{V_{I_p}}$ and $\mathrm{V_{I_n}}$ as named in Fig. 2.25) are controlled with the same sets of controlling bit. Likewise the two differential quadrature branches are controlled with the same controlling bits.

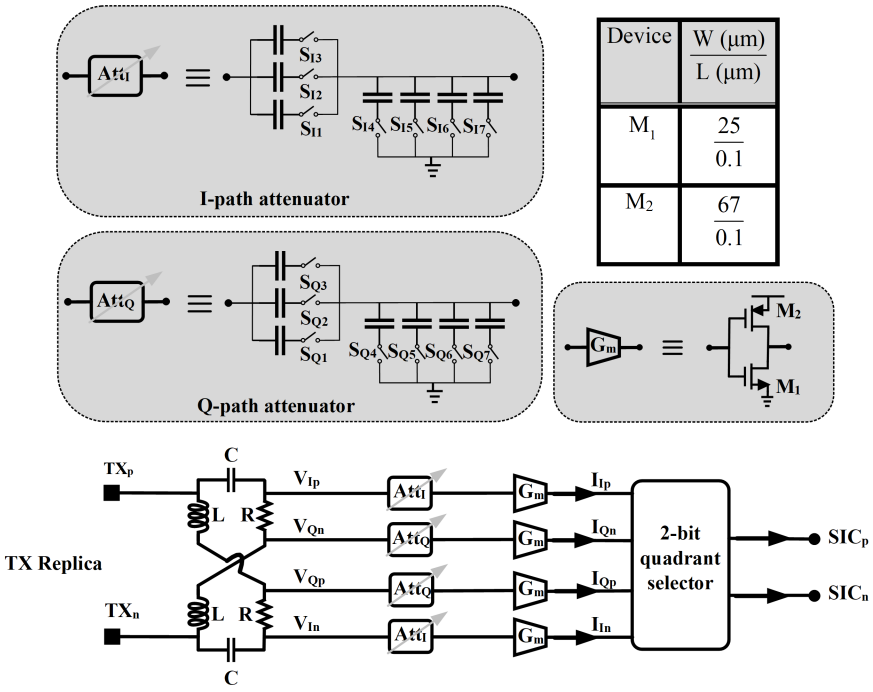
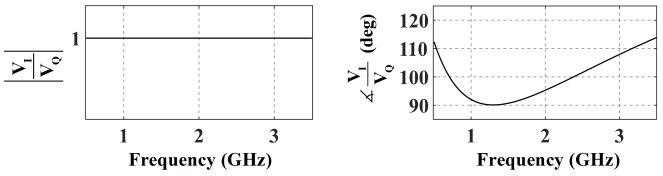


Figure 2.25: Realization of the SI-canceler. The TX replica is taken, the SI is synthesized and the differential SI approximated currents are injected to the RX interface.



(a) (b)

Figure 2.26: The magnitude and phase response of the RLC network. a) Magnitude response of $\frac{V_I}{V_Q}$ which does not vary with the frequency. b) Phase response of $\frac{V_I}{V_Q}$ which has around 20° variation from intended 90° in the frequency of operation.

In order to add the synthesized I/Q components and make the SI-canceler compatible with the RX-front-end, the voltages are converted into current. Gm-cell units based on class-AB transconductance is employed to this end. Accordingly, these four components are summed to generate the SI approximated currents ($\mathrm{SIC_p}$ and $\mathrm{SIC_n}$). The 2-bit quadrant selector does the task of summation, in addition to selecting which polarities for in-phase components ($\mathrm{I_{I_p}}$ or $\mathrm{I_{I_n}}$) needs to be added to which quadrature components; that is $\mathrm{I_{Q_p}}$ or $\mathrm{I_{Q_n}}$. These four outcomes are controlled by

two switches in the quadrature selector, the diagram is illustrated in Fig. 2.27. This arrangement covers the four quadrant of the Cartesian plane.

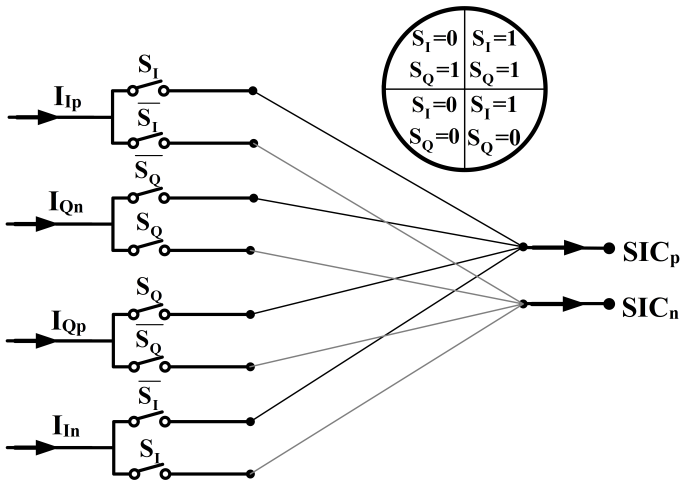


Figure 2.27: The 2-bit quadrant selector diagram.

2.7.1.1 The SI approximation synthesis and precision

The SI picked up by the receiver, induces current to the RX input ($\mathrm{I_{SI}}$). Assuming the maximum imposed SI power to the RX is $\mathrm{P_T}$ (the transmitted power subtracted by the propagation domain isolation/cancellation), the maximum magnitude of the SI induced current is $|\mathrm{I_{SI_{Max}}}| = \sqrt{\frac{2\mathrm{P_T}}{\mathrm{Z_0}}}$. Considering the cascaded stages of SI-canceler, depicted in Fig. 2.25, in such condition: the output current coming from each of the trans-conductance cell can have a magnitude as large as $\frac{\mathrm{I_{SI}}}{2}$, where the divide by two is due to the SI-canceler differential signaling which is doubled at the RX-SI canceler interface. The resolution of each branch current component is equal to the maximum current divided by 2 to the power of the number of attenuator bits (N). Therefore, the current resolution of trans-conductance cells is calculated as

$$I_{res} = \frac{\sqrt{P_T}}{5 \times 2^{N+1}}. \tag{2.53}$$

In the Cartesian plane created from I-, and Q-components, there are constellation points that

each can approximate a potential SI with an approximated vector (SI app). As shown in Fig. 2.28, this result in an error between the SI and the approximated SI. This error is defined as

$$\delta = \mathrm{SI} - \mathrm{SI\,app}, \tag{2.54}$$

where SI is the self-interference vector in the Cartesian plane, and SI app is the closest vector from origin to the constellation point which minimizes the resultant error. The maximum error is given by

$$\delta^{+}_{Max} = \frac{\sqrt{2P_T}}{5 \times 2^{N+2}}, \tag{2.55}$$

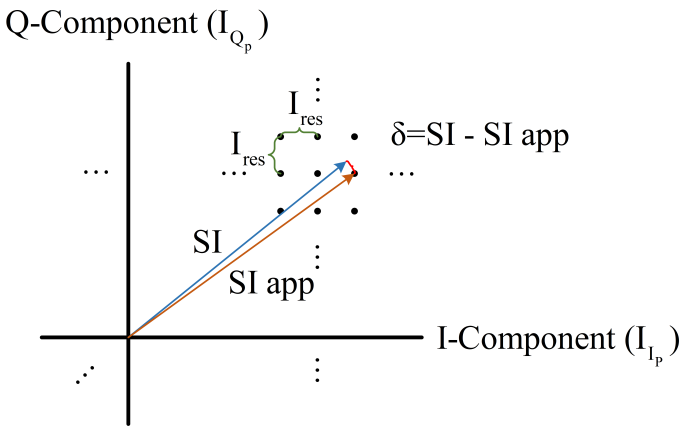


Figure 2.28: The generated self-interference constellation points in the first quadrant of the Cartesian plane. For an arbitrary SI in the first quadrant, the error (δ) vector is illustrated.

where $\delta^{+}_{\mathrm{Max}}$ shows the maximum error in the condition that I-, and Q-components are perpendicular. As shown in Fig. 2.26(b), the bases deviate from orthogonal throughout the frequency. In the case of deviation from orthogonal base vectors, the error increases as illustrated in Fig. 2.29. With a similar procedure, it can be shown that the maximum error for non-orthogonal bases is calculated as:

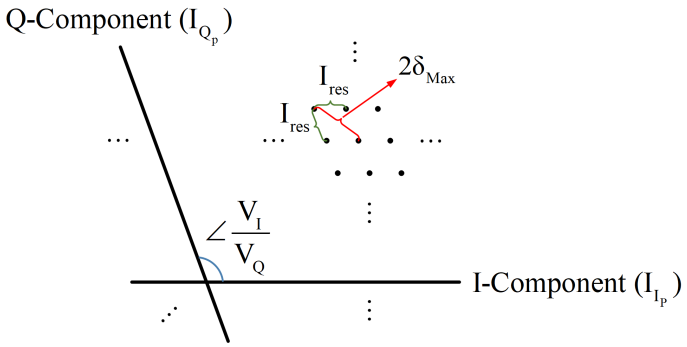


Figure 2.29: The Maximum error in the case of non-perpendicular bases components.

$$\delta_{Max} = \frac{\sqrt{2P_T}}{5 \times 2^{N+2}} \sqrt{1 + |\cos(\angle \frac{V_I}{V_Q})|}. \tag{2.56}$$

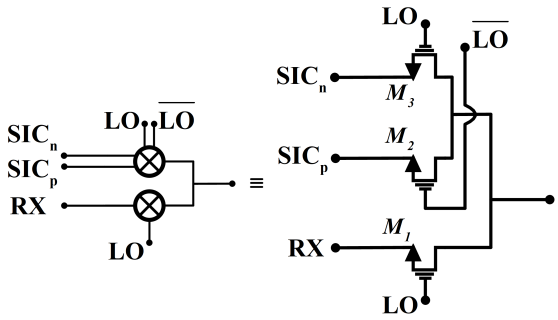
From Fig. 2.26(b), it is seen that the phase between the bases ($\frac{V_I}{V_Q}$) changes throughout the frequency, with a maximum variation at the edges. This result in variation in the amount of SI-cancellation across the LO frequency. From (2.55) and (2.56), SI-cancellation variation of $20\log(1 + \text{abs}(\cos\angle\frac{V_I}{V_Q}))$ is expected due to the phase response variation which reaches around 2.8 dB at the frequency edges. This is quite in-line with the measured SI-cancellation across LO frequency represented in the measurement section (Fig. 2.36).

2.7.2 RX Front-End And SI-Canceller Passive Mixers

The transistor level implementation of the RX front-end and SI-canceler passive mixers is shown in Fig. 2.30. As discussed earlier, for reducing the noise contribution of the SI-path, reduced mixer resistance is desirable. With a compromise between power consumption and this noise source, the sizing represented in Fig. 2.30 for each branch is chosen.

2.7.3 Multiphase Clock Generation

The multiphase clock generator schematic is illustrated in Fig. 2.31. Differential clocks at 4 times the LO are taken off-chip and are consequently divided to create the 8 non-overlapping LOs. It is important to ensure the LOs are non-overlapping and non of the two mixers are biased in a way which they conduct the RX current simultaneously (during the interval of LO transition) [56],



Device	W (μm) / L (μm)
M_1	32 / 0.06
M_2, M_3	180 / 0.06

Figure 2.30: The implementation of the receiver's mixers and down-conversion path of SI-canceler which illustrates one of the eight front-end branches.

[57]. Simulation shows that this can deteriorate both the RX gain and NF. The delay from the clock generation to the mixer should be the same for the 8 paths. Enough number of buffers are placed between stages to ensure power consumption is optimized while the next stage load is driven at the maximum operating frequency. The LO phase noise can also have an impact on NF, however, here it is mostly set by the off-chip clock. Nonetheless, it is important to have sharp zero-cross transitions for the generated LO signals, hence keeping the added phase noise to a minimum.

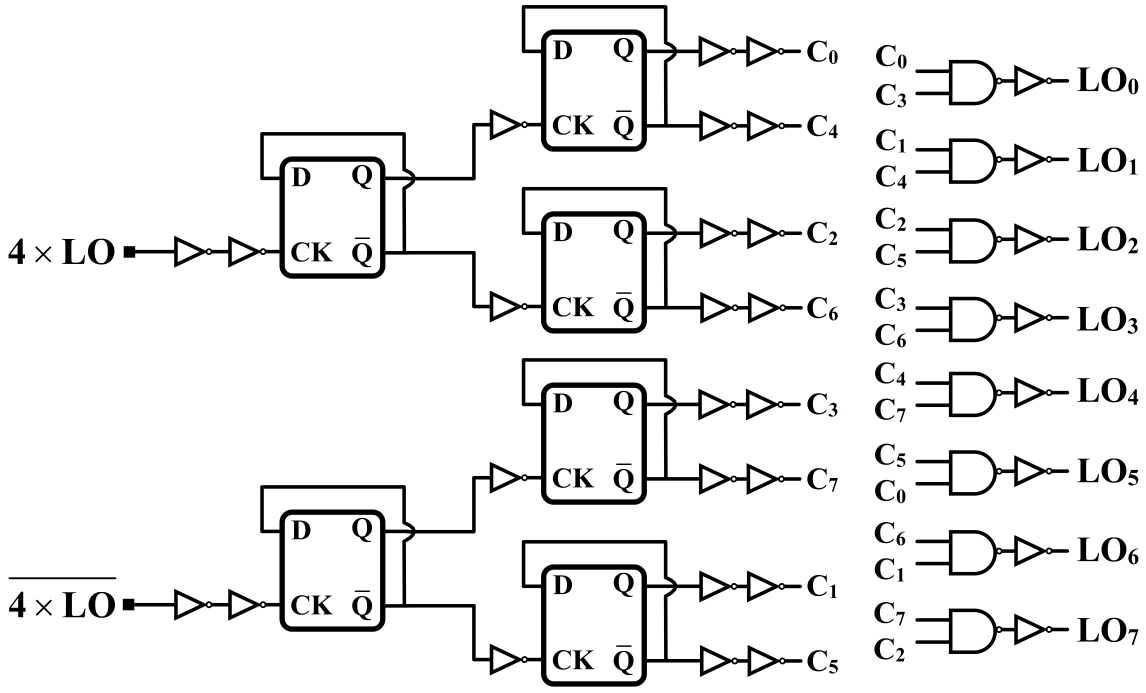


Figure 2.31: The 8-non-overlapping clock generator.

2.7.4 The Differential Op-Amp

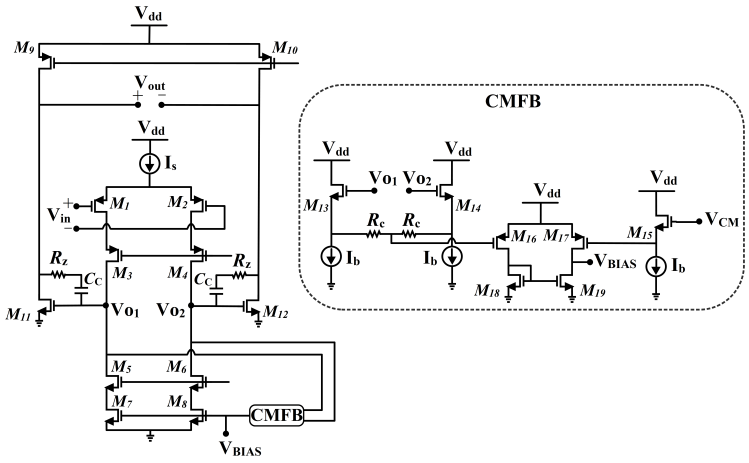
Within the entire receiver 10 op-amps are used, for implementation of the TIAs, and in the recombination circuit. They all have a structure similar to Fig. 2.32 with minor differences. In the recombination section, op-amps with higher voltage supply is used ($\mathrm{V_{dd}} = 2.4\,\mathrm{V}$) in order to achieve a higher voltage swing at the output. This also increases the RX linearity by a few dB.

As discussed earlier, mixer-first structure is chosen to address the FD linearity requirement. However, noise (specifically noise at close-in offsets) is compromised by this choice. Designing a very low flicker noise op-amp can alleviate the noise penalty. For this purpose, PMOS inputs are chosen. The length of input devices are non-minimum (240 nm). The widths are chosen substantially large to lower the flicker noise of the entire RX to a comparable level of an LNA-first architecture. There is no concern about the input parasitic capacitor, since they are absorbed by the capacitor at the TIA input ($\mathrm{C_0}$ in Fig. 2.15) and actually they are beneficial in making the RX filtering properties sharper or they can be used to reduce the external capacitor. Since there are 10 of these op-amps in the receiver, it is crucial to design them with minimum power consumption which mostly trades with the op-amp's bandwidth. The op-amp compensation is achieved by $\mathrm{C_C}$ and $\mathrm{R_z}$ which introduces an zero. This LHP zero widens the BW with no need to increase the power consumption.

The simulated input referred noise of the op-amp is illustrated in Fig. 2.33. It can be seen that the flicker noise is brought to a very low-level with the utilized scheme, while the majority portion of the information received is exposed to the noise in MHz region where the input referred noise of the op-amp is around 1.2 $\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}}$.

2.8 Measurement Results

As a proof of concept, the circuit is fabricated in 65 nm CMOS process. The chip micrograph is shown in Fig. 3.23. The measurements performed on the prototype is presented in this section.



Device	W (µm) / L (µm)
M_1-M_4	2592 / 0.24
M_5-M_8	864 / 0.24
M_9, M_{10}	96 / 0.24
M_{11}, M_{12}	28.8 / 0.24
M_{13}-M_{15}	4 / 0.06
M_{16}, M_{17}	4.8 / 0.24
M_{18}, M_{19}	9.6 / 0.24

Component	Value
R_c	10 KΩ
R_z	190 Ω
C_c	5.2 pF

Figure 2.32: Schematic of the differential op-amp.

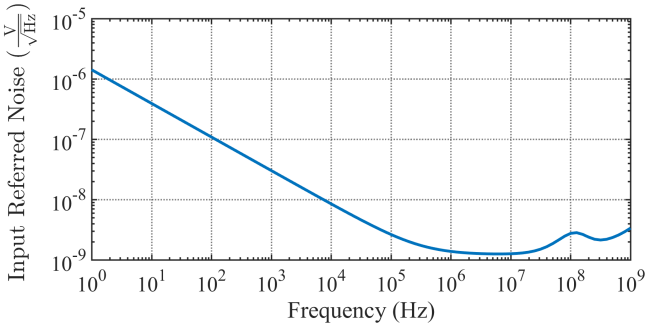


Figure 2.33: The simulated input referred voltage noise of the op-amp.

2.8.1 Test Set-up

The test arrangement for two-antenna SI-suppression measurement is shown in Fig. 2.35. The Rohde & Schwarz signal generator creates 64-QAM 10 MHz-BW modulated signals around the carrier from 0.5 GHz to 3.5 GHz. Using a directional coupler part of this signal feeds the input of the Cartesian synthesized SI, and the other port feeds the input of the antenna. The coupling between the two antennas can be controlled by placement (coupling) adjustment. As such, radiated signal undergoes different attenuation, time delay, and phase shift. The introduced SI at the input of the receiver, subsequently is cancelled by adjusting the Cartesian Synthesized SI. The power of the signal generator is swept to change SI power at the receiver input ranging from -25 dBm to -65

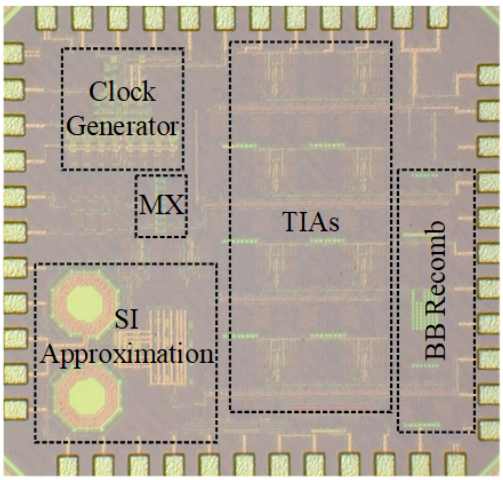


Figure 2.34: The die micrograph indicating building blocks. The chip dimension is $1.4 \times 1.3\ \mathrm{mm}^2$.

dBm. At the same time by adjusting the distance between the two antennas, group-delay is varied from 0.8 ns to 2.5 ns. The group delay and isolation between the two antennas are measured by connecting the two antennas to network analyzer.

Similar measurments are performed on the chip with the two antennas replaced with attenuator, phase-shifter (0° to 360°), and delay-line. In order to have a precise control on the phase-shift and the SI power at the receiver port.

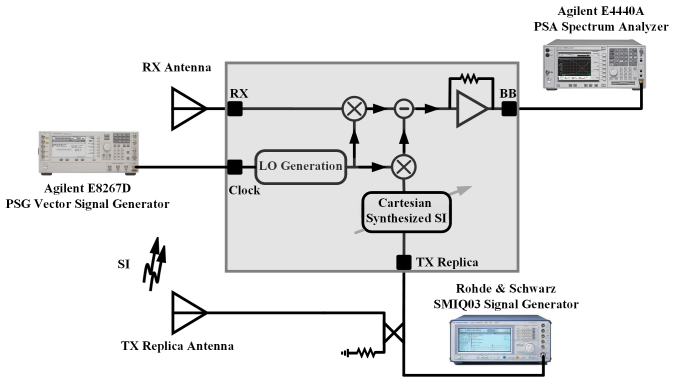


Figure 2.35: The test set-up for two-antenna self-interference suppression measurement.

Table 2.2: Summary of the two-antenna SI-supression measurement.

Group delay [ns]	0.8 – 2.5
SI magnitude at the RX port [dBm]	-65 – -25
SI-suppression [dB]	-36 – -34
Propagation domain isolation [dB]	20 – 40

2.8.2 SI-Cancellation

To measure the SI-cancellation, received signal is shut down, and 64-QAM signal with 10 MHz-BW is connected to the TX replica port. The same signal undergoes through different attenuation, time-delay and phase shift which characterizes the channel; then it is imposed to the receiver. The optimum setting for SI-canceler switches need to be found which translates into the minimum residue at the receiver output. For this purpose, a successive approximation algorithm is used which alternates between I and Q state at each step. The optimum state of switches result in the least residue at the receiver output. To quantitatively measure the cancellation, and omit the dependency on the SI power, the residual power is normalized to SI power, hence SI suppression can be evaluated. The result of the two-antenna SI-suppression measurement is summarized in Table 2.3. Variations of SI suppression across LO frequency is illustrated in Fig. 2.36. Both the two-antenna measurements and delay/phase-shift/attenuation measured data are used in this Figure. The variation of SI-suppression in frequency was expected due to the phase response of the RLC network. The lowest suppression is in the mid frequency range, which is around 3 dB lower compared to the low and high frequency edges.

As shown in Fig. 2.38a, more than 35 dB cancellation was measured for 100 samples of TX replica emulated by 10 MHz-BW 64-QAM signals, the power of the TX replica is normalized to 0 dB to illustrate the cancellation. The packaged chip and ports' connection are shown in Fig. 2.38b.

2.8.3 Noise Figure

In the HD mode, i.e., there is no imposed interference and SI-canceler is turned off, the measured NF versus the baseband frequency is shown in Fig. 2.37(a). For the case of FD mode, the

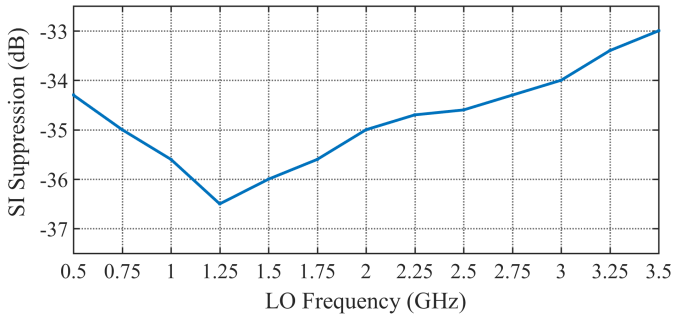


Figure 2.36: SI suppression across LO frequency. The suppression is varying from -36.5 dB to -33 dB.

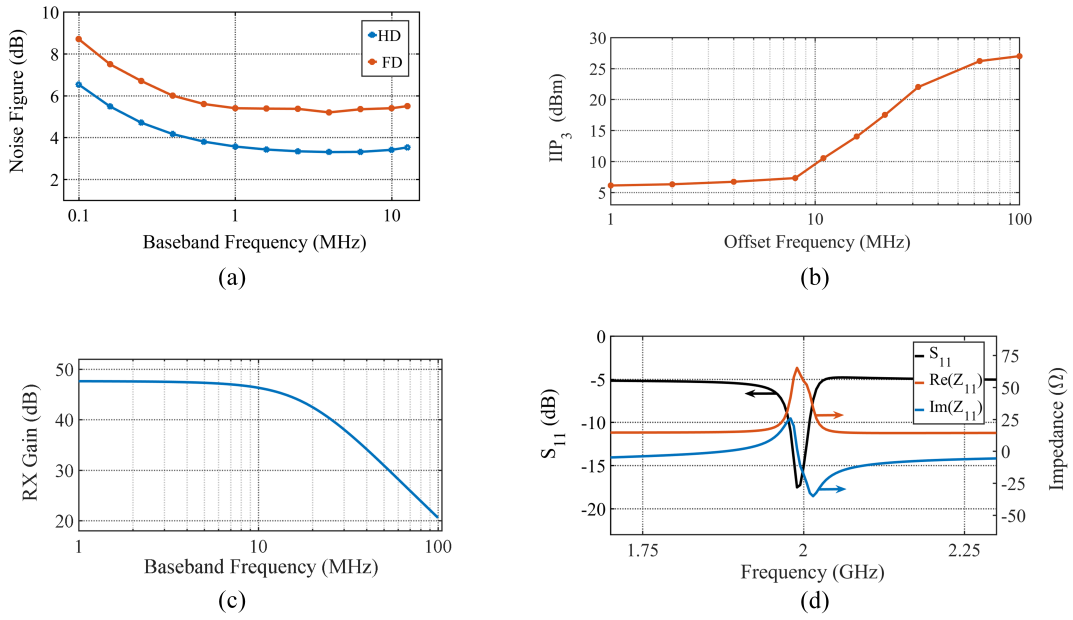


Figure 2.37: The receiver measurements at 2 GHz RF frequency. (a) NF in HD/FD mode versus the baseband frequency. (b) RX IIP_3 versus the offset frequency in the two-tone test with no cancellation (conventional IIP_3). (c) The RX conversion-gain. (d) The RX input port reflection and impedance characteristics.

situation can get somehow vague as there is a clear dependency on the level of SI power which is imposed on the receiver. When the level of SI is high, as such the residual post cancellation level is larger than the receiver noise floor, the measured intended NF in fact characterizes signal to residue level in the receiver output instead of signal to noise. NF in FD mode is measured and depicted in Fig. 2.37a. The difference between the two is the noise injected by the SI-canceler path. There is around 2-to-2.5 dB NF penalty in switching from HD to FD. Variations of NF at 1 MHz baseband

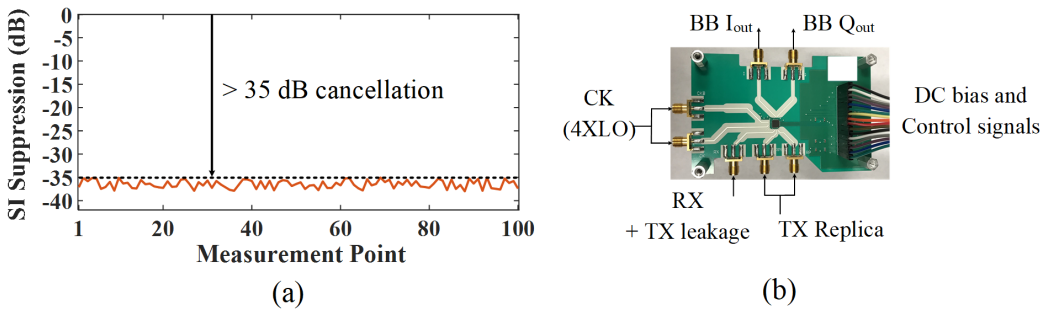


Figure 2.38: a) Self interference (SI) suppression of 100 samples of TX replica. b) Packaged chip, and ports' connection in SIC measurement set up.

across the LO frequency is shown in Fig. 2.39.

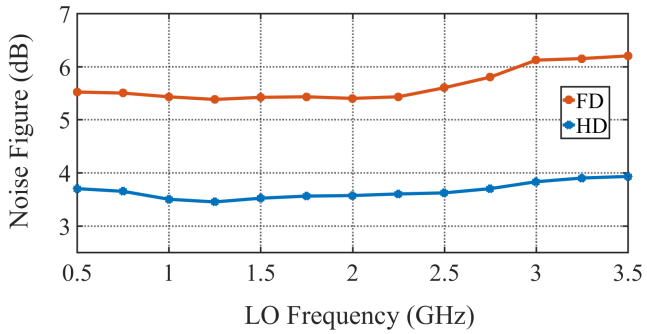


Figure 2.39: The receiver NF at 1 MHz offset across LO frequency.

2.8.4 Linearity

The two-tone test is performed on the chip at maximum gain setting. Uncalibrated IIP_2 of +70 dBm is measured. The IB-IIP_3 is +6 dBm in 1 MHz offset in the two-tone test without cancellation. By including the canceler effect in the FD mode, the effective IB-IIP_3 is +20 dBm. That means, in the two-tone test one of the tones is considered the as the SI and IIP_3 is measured while the canceller is suppressing that tone. The effective RX IIP_3 in FD mode as a function of the offset frequency is plotted in Fig. 2.40. The OB-IIP_3 is +27 dBm. The measured IIP_3 as a function of the offset from the 2 GHz carrier is illustrated in Fig. 2.37(b). The SI cancellation path has at least 25

dBm $P_{-1\,dB}$ over all different states.

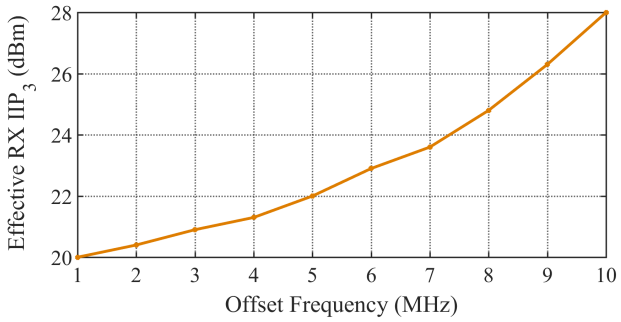


Figure 2.40: The receiver effective IIP_3 in FD mode versus the offset frequency in the two-tone test at 2 GHz RF frequency.

2.8.5 Input Matching

As discussed earlier, the input matching of the receiver is a function of the feedback resistor, op-amp open loop gain, and the mixer (switch) ON-resistance. All these are PVT dependent. In addition, it is crucial that receiver shows an acceptable input matching through the whole frequency of operation (0.5-to-3.5 GHz). To address this issue, two mechanisms are used. First, the feedback resistor value around the TIAs are controllable with four switches. In addition to this, the bias current of the op-amps are also variable; this allows changing the open-loop gain of the op-amps. Having this two degree of freedom, it is possible to have RF-matching while the RX gain can also vary. It should be noted that the variation in gain is only useful when the receiver is imposed to high level of SI power. In such circumstances, the receiver gain can be reduced to avoid saturation of the internal stages and desensitization of the receiver. In other situations, where the SI power is not considerable, the optimum bias point for the op-amps are used; the matching is achieved by tuning the feedback resistor. In such setting, the conversion-gain is illustrated in Fig. 2.37(c). Due to the narrow-band response of the front-end and subsequent gentle filtering, the BW is set at the intended value of 10 MHz. The receiver S_{11} and the input real and imaginary impedance is shown in Fig. 2.37(d) at 2 GHz frequency. The linearity, S_{11}, and conversion-gain are shown here only

Table 2.3: Measurement summary and comparison with recently published full-duplex receivers.

Specification	[2]	[3]	[6]	This work
RF frequency [GHz]	0.61-0.975	1.7-2.2	0.15-3.5	0.5-3.5
RX gain [dB]	28	20-38	24	30-50
OB-IIP3 [dBm]	+15.4	N/A	+22	+27
IB-IIP3 [dBm]	-18.4	-5	+8/ +16*	+6
NF in TDD mode [dB]	6.3	4	6.3	3.3
NF in FD mode [dB]	8	5/ 5.5**	10-12.3	5.3
Cancellation domain Number of cancellation domain(s)	Circulator + RF 2	RF + Analog BB 2	RF down-converted 1	RF down-converted 1
SI suppression [dB]	40	55	27	35
RX power consumption [mW]	72	22	23-56***	15-38***
Canceler power consumption [mW]	36	11.5	N/A	4-12
Supply voltage(s) [V]	1.2/2.4	1.2/1.8/2.4	1.2	1.2/2.4
Active area [mm^2]	0.94	3.5	2	1.5
Technology	65 nm CMOS	40 nm CMOS	65 nm CMOS	65 nm CMOS

* Negative conductance off/ on

** Estimated (from Fig. 22 of [3]), w/ and w/o LO sideband suppression

*** Includes LO generation power consumption

at 2 GHz. They are measured for different frequencies from 0.5 to 3.5 GHz and show very similar characteristics as shown here.

2.8.6 Comparison With Prior Art

Table 2.3 compares this work with recently published state-of-the-art SI-cancelling receivers. The RF-bandwidth covers wide range, and is limited from both ends to SI-cancelling I-Q generator phase precision. The measured linearity metrics addresses the discussed requirement of FD. Specifically, a low IB-IIP_3 can severely limit the sensitivity, and this is mitigated at architecture and circuit level. Compared to the prior art, rivaling with LNA-first architecture NF is achieved while the linearity of mixer-first is demonstrated. There is only 2 dB NF penalty in FD mode operation compared to the HD. Here only one domain of cancellation is used which addresses the issue of RX desensitization. Further cancellation at propagation and digital domains is needed for a practical link realization. Yet compared to similar realizations ([5], [23]) 8 dB higher self-interference suppression is achieved.

2.9 Conclusion

A wideband SI-cancelling receiver is proposed which by combining wideband operation with FD, can provide opportunistic and efficient usage of the band in the entirely allocated RF spectrum.

The linearity specification (IB-IIP_3) for feasible desired signal detection in presence of IM_3 terms was derived. By maintaining the RF signal in current mode a high linearity is achieved which is a bottleneck in an FD receiver performance. SI-cancellation is achieved by synthesizing the approximated SI in the Cartesian plane, and injecting the current to the RX after down-conversion. The performance of the receiver in system-level and circuit-level is studied, analyzed and measured which all are in a close agreement. This work achieves high level of receiver front-end cancellation in a single domain, hence prevent receiver from desensitization due to self-interference. Combined with other domains of cancellation, such as propagation and digital, a practical link with sufficient suppression can be realized.

Comparing the performance, NF is lower than any other reported mixer-first, and many of LNA-first receivers. Due to the interference cancellation mechanism, and high linearity of the receiver, there is only a small noise-distortion degradation in the presence of large TX-leakage, which shows a high dynamic range is achievable in FD wireless receivers.

3. A 22.2-43 GHZ LNA FOR RADIO-OVER-FABRIC IN 28 NM CMOS

3.1 Wideband Multi-Function Receivers

Wideband mm-wave multifunction receivers (f >30GHz) that can cover a broad spectral range, be rapidly reconfigured, and dynamically suppress jammers (Fig. 3.1) are essential for enhanced access to radio spectrum for a variety of applications, including wireless communications, radar, and sensing systems. However, ensuring robust operation in noisy wireless environments is challenging, as wideband receivers tend to be desensitized by large-signal blockers. Thus, reducing in-band interference due to jamming sources is critical for the integrity of these wireless systems. A potential solution is to employ spread-spectrum systems which are robust to jammers, provided that high quality factor (Q) filters capable of highspeed reconfiguration and operation at mm-wave frequencies can be realized. While this is not feasible with conventional electronic filter technology, RF photonic technology has the potential to enable widely tunable mm-wave receivers which possess both wide instantaneous bandwidth (BW) 5GHz over a broad spectral range (f >30 GHz) and the ability to dynamically suppress blockers. Rapid dynamic filter reconfiguration (sub-ms) and blocker cancellation (-10dBm) with 40dB out-of-band rejection will be essential to effectively utilize a wideband spectrum. Utilizing the innovative optical filter and CMOS circuit techniques proposed in this project will enable the efficient use of RF silicon photonic band-pass and notch filters to fulfill these requirements.

Applications such as wireless communications, radar, radio astronomy, and passive earth remote sensing can gain huge advantages from wideband multi-function transceivers. Transformative RF system and transceiver architectures are necessary to enable efficient coexistence of these applications over a broad spectral range. A major barrier to achieving this is that, with the potential increased instantaneous bandwidth of such a system, the role of front-end filtering in receivers becomes more critical to guarantee the necessary RF performance. Rapid dynamic filtering and interferer cancellation will be essential to enabling the efficient use of a wideband spectrum. Un-

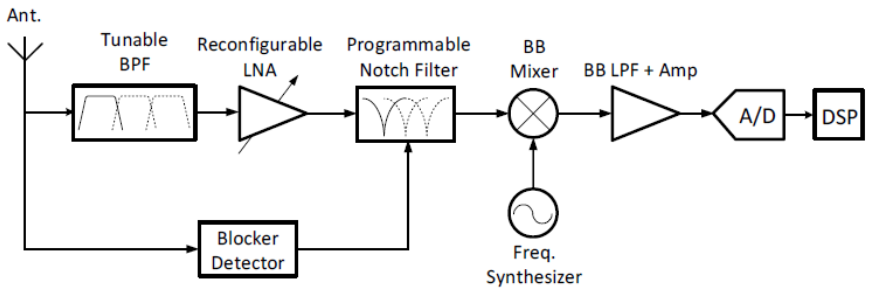


Figure 3.1: Wideband multi-function mm-wave receiver block diagram with dynamic jammer suppression (f >30 GHz).

fortunately, there are fundamental limitations to achieve the required level of frequency selectivity and tuning range and speed with conventional electrical filters within the size, weight, and power targets of radio systems with small form factors. RF photonics technology has the potential to enable widely tunable receivers with wide instantaneous bandwidth and rapid dynamic filtering over a broad range of the spectrum. Specifically, RF photonic filters are capable of achieving very high selectivity, multi- GHz tuning ranges, and rapid dynamic tuning. While RF photonic filters have traditionally been demonstrated with relatively large, bulky, discrete optical test-bench implementations, the emergence of silicon photonics has enabled the potential for these RF photonic filters to be implemented in the size, weight, and power requirements of radio systems with small form factors. However, major drawbacks in the potential utilization of reported silicon RF photonic filters are 1) lack of automatic calibration and adjustment of the initial filter response with the very high accuracy essential to maintain the filter response and/or provide rapid reconfiguration, 2) the non-linear effect of the photonic modulator, which can result in in-band interferers with strong RF blockers and impact both the filter and the entire receiver performance, and 3) achieving the required optical receiver sensitivity for acceptable noise figure. A promising solution is employing nano-scale electronics along with the silicon photonic filter and electro-optical modulator to perform the automatic photonic filter response calibration, modulator adaptive linearization, and optical front-end amplification.

There are fundamental limitations to achieving the required level of frequency selectivity and

tuning range and speed with conventional active or passive electrical filters within the size, weight, and power targets of radio systems with small form factors at mm-wave frequencies. Off-chip surface acoustic wave (SAW) filters have been widely adopted at the front end of many receivers in harsh RF environments. However, in multi-band or highly-dynamic RF environments, a complex high-speed tunable filter is required which is not feasible with existing SAW filters. Other technologies, such as off-chip MEMS or low-temperature co-fired ceramic (LTCC) filters, due to a limited Q-factor, are expected to have limited rejection for strong close-in jammers.

Existing on-chip or integrated front-end filtering solutions can be categorized into 1) high frequency integrated RF/analog tunable filters, and 2) SAW-less reconfigurable front-ends. Currently, highfrequency integrated analog filters cannot achieve the high selectivity and wide tuning requirements necessary for tunable receivers with wide instantaneous bandwidth due to low/moderate on-chip inductor Q-factors. Also, due to the active nature of these filters, their linearity is limited. SAW-less receivers have gained attention for single/multi-band wireless systems to mitigate SAW filters by proving dynamic bandpass filtering based on a reciprocal passive mixing technique, but it is extremely difficult to push their frequency of operation into the mm-wave range, as they need a clock with a frequency at least 4X higher than the desired radio frequency.

These limitations of electrical filters motivates the employment of RF photonic band-pass and notch filters, which can achieve higher Q, multi-GHz tuning ranges, and, with the innovative tuning schemes proposed in this work, sub-ms reconfiguration times. While RF photonic filters have traditionally been demonstrated with bulky, discrete optical test-bench implementations using array waveguide gratings, optical fiber Bragg gratings, and fiber Fabry-Perot filters, the emergence of silicon photonics has enabled the potential for these RF photonic filters to be implemented in the size, weight, and power requirements of radio systems with small form factors. Because of significant loss reduction and high waveguide refraction index, 200,000 Q factors and high integration density is achievable.

Major drawbacks of the reported silicon RF photonic filters include the difficulty of calibration and adjustment of the initial band-pass filter (BPF) response with very high accuracy and adjust-

ing the location of optical notch filters for the intelligent removal of blockers. Since silicon RF photonic BPFs with acceptable out-of-band rejection are at least 4th-order or higher, a significant number of photonic phase shifters inside the filter structure need to be very precisely tuned to position the filter poles and zeros to construct the filter response. A common procedure is to visually monitor the filter response using a spectrum analyzer and manually tune each phase shifter via trial-and-error to achieve the desired response. This is very time consuming, requires expensive lab equipment, and is also prone to human error for the required large number of filter poles and zeros. All these issues demand a more elegant way of adjusting the filter response within RF photonic receivers. Also, intelligent blocker detection within a wide instantaneous bandwidth (5GHz) using photonic ring resonators and dynamic suppression of blockers using photonic notch filters is a challenge that needs to be addressed properly. Other potential issues are associated with optical modulator linearity and the sensitivity of the front-end circuitry. A Mach-Zehnder modulator (MZM) is often used to modulate the received RF signal from the antenna onto an optical carrier before applying photonic filtering. Degradation of receiver performance is possible if large blockers are received along with the desired RF signal, as the MZM is located before the photonic filter and it is an inherently non-linear device. Thus, linearization techniques that employ integrated RF electronics before the MZM are necessary. Existing linearization approaches for electrooptical modulators, which include pre-distortion, feed-forward techniques, and novel modulator design, require complicated/bulky hardware to precisely control amplitude and delay for adequate error cancellation or they demand complex optical fabrication. Therefore, an integrated linearization technique with automatic calibration is desirable. A large percentage of a photonic receiverâĂŹs noise figure and gain is set by the front-end transimpedance amplifier (TIA) and it is extremely challenging to achieve the desired sensitivity performance at mm-wave frequencies. Thus, both an innovative photonic system architecture and novel TIA design techniques are required to enable the proposed silicon photonic mmwave receiver.

The goal of this proposal is to develop a novel chip-scale wideband frequency-agile silicon photonic mmwave receiver for spread spectrum communication that utilizes high-performance

band-pass photonic filtering along with automatic jammer suppression via reconfigurable optical notch filters. The photonic receiver is implemented in a 130nm SOI optical chip that is intelligently controlled by a 65nm CMOS chip to allow for automatic calibration and tuning of both photonic band-pass and notch filters with very high accuracy. Fig. 3.2 shows the system driver RF-photonic receiver, consisting of the two main parts. (1) The 65nm CMOS chip includes the antenna interface, MZM pre-distortion linearization stage, optical RF front-end (TIA), as well as the electrical circuitry for tuning the filter responses. (2) The 130nm SOI silicon photonic chip includes MZMs for E-O conversion, a 5GHz reconfigurable channel-select 4th-order BPF, ring resonator filters for jammer suppression and spectrum sensing, and waveguide photodetectors for O-E down-conversion and filter monitoring. A pre-distortion technique is proposed which calibrates the main MZM nonlinearity by implementing the inverse response of the modulator in the frequency range of interest. An external wideband frequency synthesizer is utilized for generation of different stimuli used in the calibration of the front-end predistortion stage, photonic filters, and RF down-conversion. After O-E conversion by an adaptivebandwidth TIA, an external DSP module detects and de-spreads the 0-5GHz baseband spread spectrum signal to measure the system BER.

3.2 Introduction and Literature Review

Today's LTE and LTE-A networks have managed to provide a high throughput by augmenting several frequency band chunks ranging from 462.5 MHz to 3800 MHz. With the 5G promise of substantially lower latency and higher throughput just around the corner, it is now evident that previous wireless systems are incapable to scale for meeting the exponentially increasing mobile trafic demand. Driven by highly anticipated 5G network, realization of different circuits and systems at the 5G associated frequency, from 24.25–42 GHz, has been extensively studied and developed by academia and industry over recent years. Low-noise amplifiers (LNAs) play a major role in determining a receiver signal to noise ratio (SNR) and the overall link budget. Specifically, realization of a low-cost, wideband LNA which can cover the whole, or some portion of 5G range has been recently given tremendous attention and solid efforts [58]-[62].

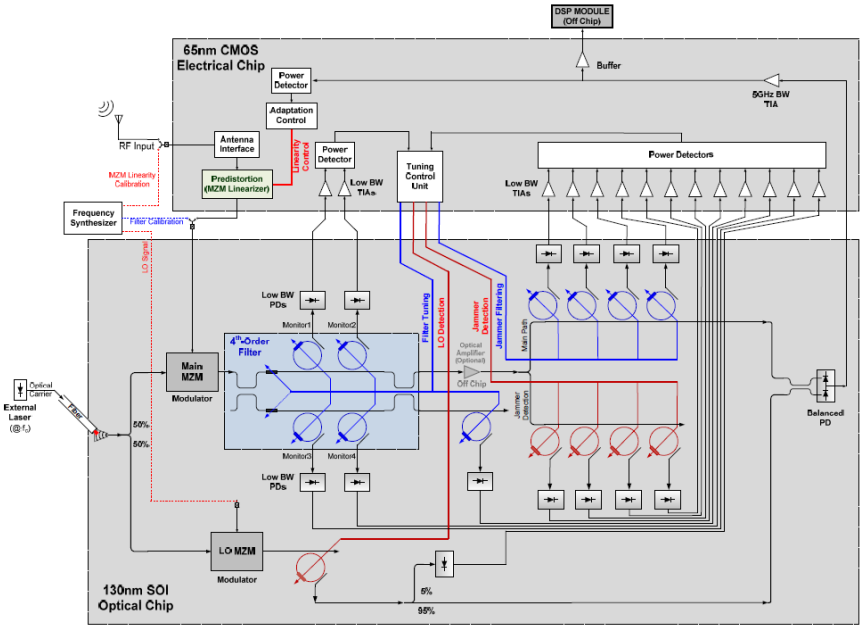


Figure 3.2: Wideband multi-function mm-wave receiver block diagram with dynamic jammer suppression (f >30 GHz).

A survey of recent publications show that almost all the proposed high performance mm-wave LNA architectures use a common source with inductive degeneration as the first stage [58]-[72]. The idea originally introduced in 1996 [73], to achieve a real impedance part equal to the inductive degeneration multiplied by the angular transient frequency in CMOS process. Inductive degenration is a reactive feedback which also suppresses the channel noise. In other words, it can achieve simultaneous noise and power matching (to 50 Ω impedance) at the LNA input. Ever since the introduction, there have been many efforts to improve the characteristics of this architecture such as bandwidth (BW), power consumption, stability, and noise performance. In mm-wave frequencies, this goal has been achieved mainly by using magnetic feedback, by means of coupled inductors creating feedback between different stages [74]-[77], or implementation at lower CMOS nodes, alternatively fully depleted silicon on insulator (FD-SOI) process, to leverage lower transistor intrinsic noise. Many of the proposed techniques trade one specific character at the cost of another or in some cases at the cost of stability. For instance, it is well-known that an inductor at the gate of a transistor creates a negative real-part seen from the source, hence pushes the device into unstable

region. At the same time, this approach can be used to extract more gain from a cascode stage, with the cascode device having an indcutor at its gate which is also magnetically coupled to other parts of the circuit [65]. The increase in gain, subsequently, will lower the noise contribution from following stage(s), but the improvement in gain and noise performance is achieved by an almost direct trade-off with stability [78].

The practical challenge of designing a common source with inductive degeneration LNA is accurate modeling of the inductor. As most silicon-based processes rarely provide accurate passive models for higher than 20 GHz frequency, most designers rely on electromagnetic (EM) simulations to characterize the passive circuits. In an EM set-up, one port of the inductor is connected to an ideal ground. This assumption proves to be troublesome as it does not take into account the current return-path from the assumed ground. On the other hand, accurate EM simulation with consideration of ground return path is very challenging. It is worthwhile to note that any error in the inductor value, for instance the added inductor in return-path, is multiplied by angular transient frequency of the transistor, a very large factor which also increases by moving to more advanced nodes [1]. Furthermore, RF techniques such as adding external capacitor at the gate-source [80] to reduce the angular transient frequency, has a very large penalty in NF [62], therefore has not been deployed for high-performance mm-wave LNAs. A practical solution for this issue is using differential common source with inductive degeneration architecture for the LNA which eliminates the need for high frequency ground return-path modeling [66], [68]. Nevertheless, the added loss of the balun at the LNA front-end, directly adds to the NF of the LNA, and deteriorates the NF at least by a few dBs.

A new LNA architecture is proposed with a robust technique for realization of the input power matching in mm-wave. The prototype fabricated in 28 nm bulk CMOS is operational over the bandwidth of 22.2 to 43 GHz which to the best of authors' knowledge is a fractinal bandwidth record (57 %) between the reported mm-wave multi-stages LNAs in bulk CMOS. The minimum NF reaches 3.8 dB, and simulation shows that the achieved NF is very close to the minimum

[1] Angular transient frequency of 28 nm CMOS is approximately $1.88 \times 10^{12}\ \frac{\text{rad}}{\text{s}}$, and it is 4.67 times higher in 10 nm CMOS [79].

achievable NF (with the noise optimum source admittance). Therefore, throughout the bandwidth simultaneous noise and power matching is obtained. The measured mid-band IIP_3 is -2 dBm, while consuming 18.5 mW power.

The gate-drain mutually induced feedback LNA (GDMIF-LNA) is elaborated here with details including analysis, design methodology, implementation, and measurements. The chapter is organized as follows. The prior art and the basic idea of GDMIF-LNA is elaborated in section 3.2. The performance analysis, including gain, NF, and design for bandwidth is studied in section 3.3. Stability issues are discussed in section 3.4. The circuit realization is elaborated in section 3.5, and the comparison remarks are drawn in section 3.6.

3.3 A Survey of Recently Published State-of-the-art LNAs

In this part 3 state-of-the-art published works are compared. All three paper are published in RFIC symposium, 2019.

The work published in [58] proposes a wide-band LNA from 24-43 GHz in 22-nm FD-SOI. The meain LNA architecture and the measured S-parameters are shown.

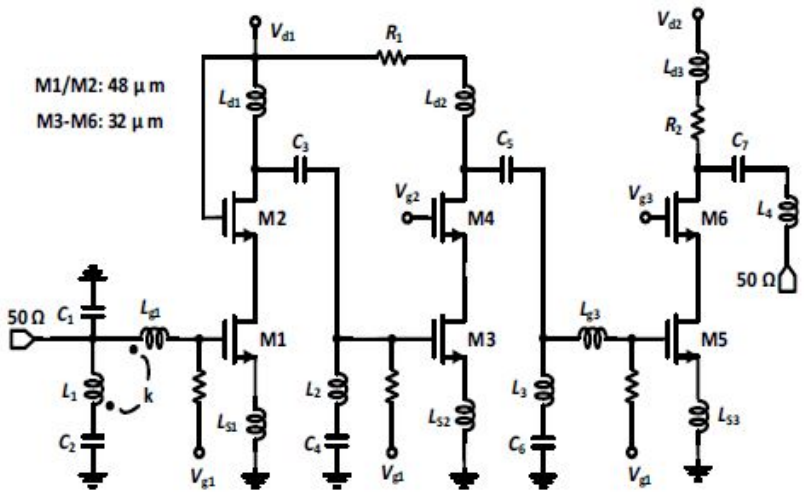


Figure 3.3: The schematic of the implemented LNA in [58].

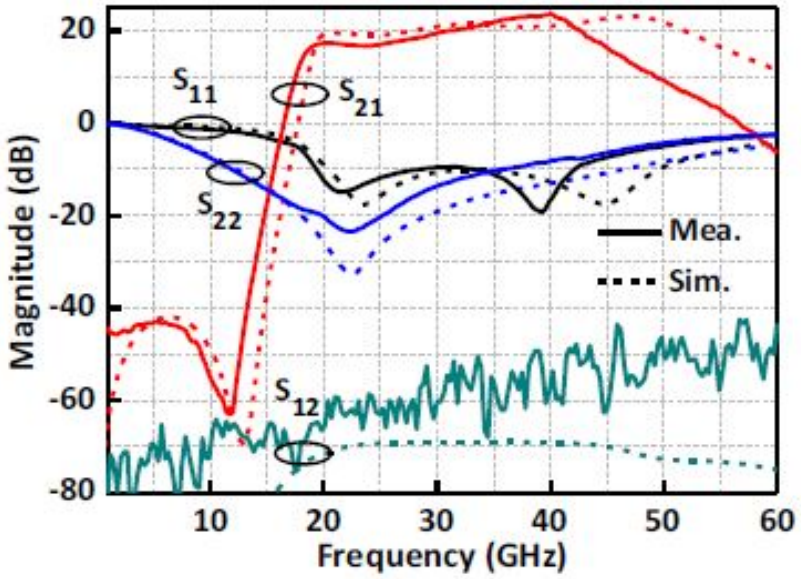


Figure 3.4: The measured and simulated S-parameters of the LNA in [58].

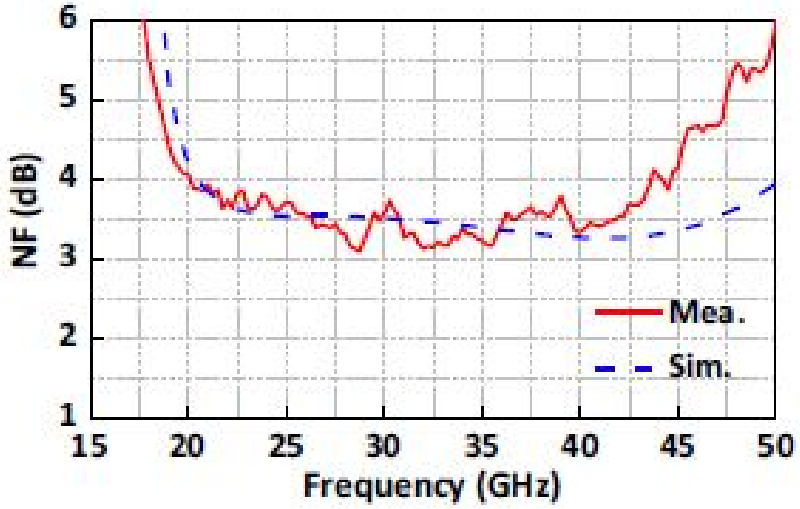


Figure 3.5: The measured and simulated NF of the LNA in [58].

Another architecture which is proposed in [59]. The schematic, s-parameter simulations and measurement and NF is shown in the following. The process is 22 nm FD SOI.

In [60] the bandwidth of 24.9-32.5 GHz is covered. The technology used in this work TSMC 65 nm CMOS. The schematic, S-parameter simulations and measurement and NF is shown in the

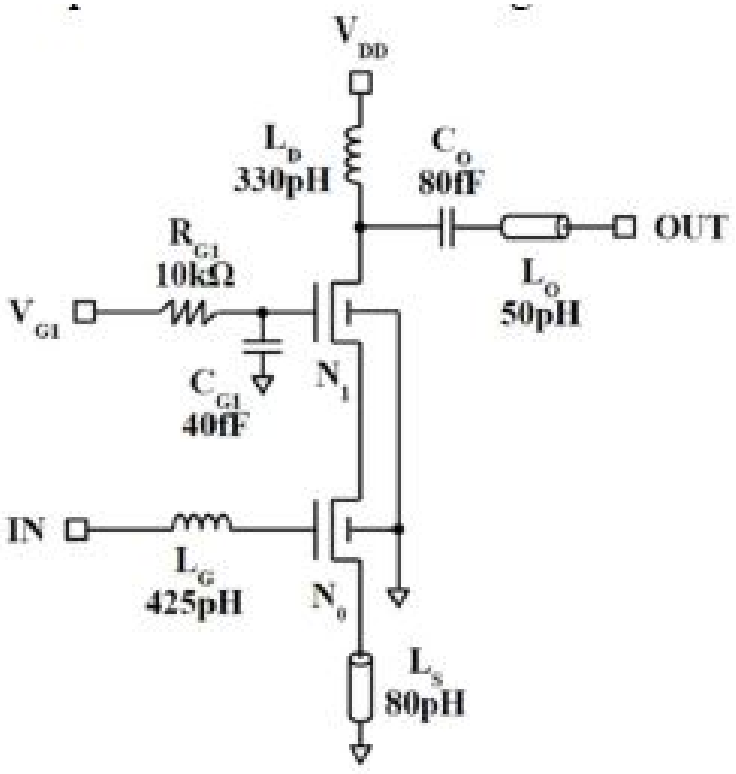


Figure 3.6: The schematic of the implemented LNA in [59].

following. The process is 22 nm FD SOI.

3.4 Gate-Drain Mutually Induced Feedback LNA

3.4.1 Prior Art

The LNAs discussed earlier [58]-[78], all use similar to the simplified input stage represented in Fig. 3.12. This stage basically provides the power matching at the LNA input. Illustrated in Fig. 3.12(a), the inductive degeneration (L_S) creates a real-part, and the gate parasitic capacitance of the transistor is tuned out by the gate inductor (L_G). The return current path is simply modeled as a lumped inductor. It is seen that the source to ground return path inductor (L_{RS}) is capable of changing the LNA input impedance. Realization of inductive degeneration as small as 15 pH has been reported [63] which shows a high sensitivity to L_{RS}. To alleviate the situation, decoupling capacitor (C_{DC}) can be deployed. Nonetheless, the distributed nature of such capacitors [2] makes

[2]Usually realized as an array of MOS capacitors to achieve the highest density.

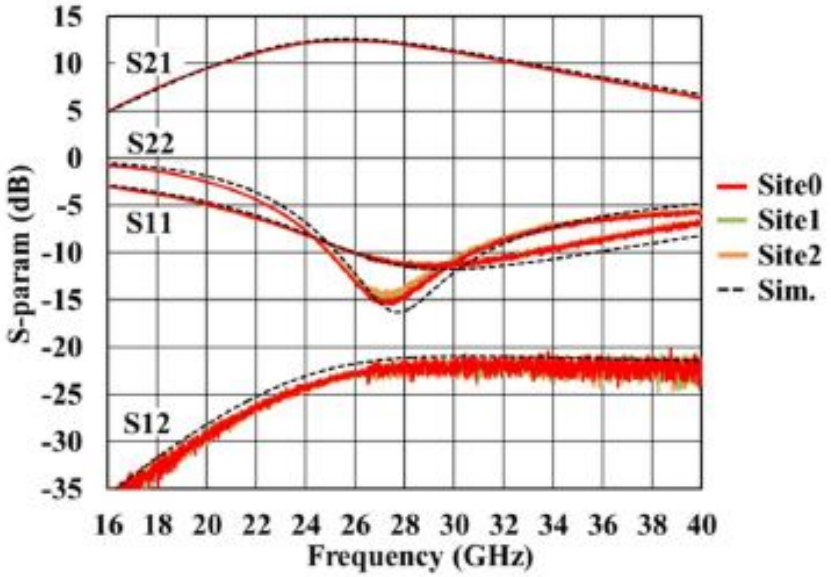


Figure 3.7: The measured and simulated S-parameters of the LNA in [59].

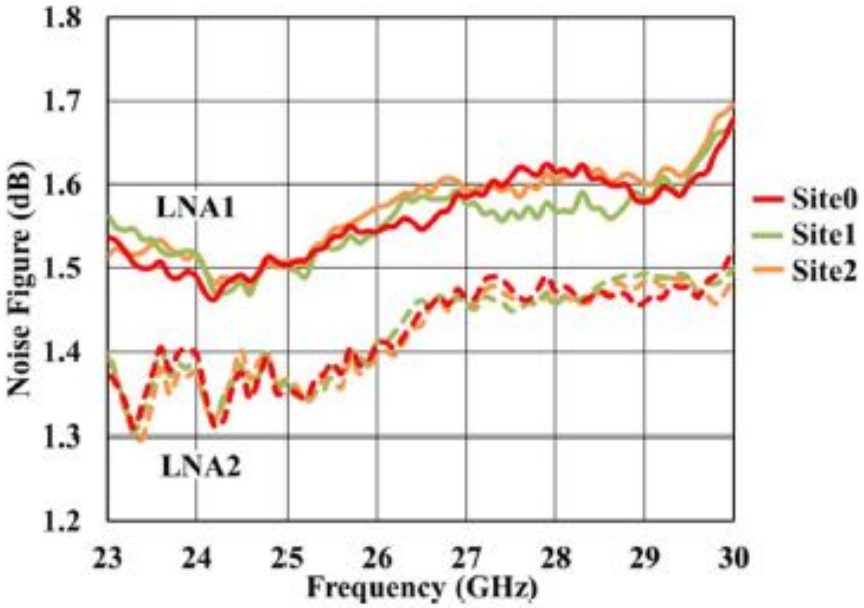


Figure 3.8: The measured and simulated NF of the LNA in [59].

an accurate modeling quite challenging. A more robust approach is a differential architecture (depicted in Fig. 3.12(b)) where due to the ac ground node, accurate high frequency model for the

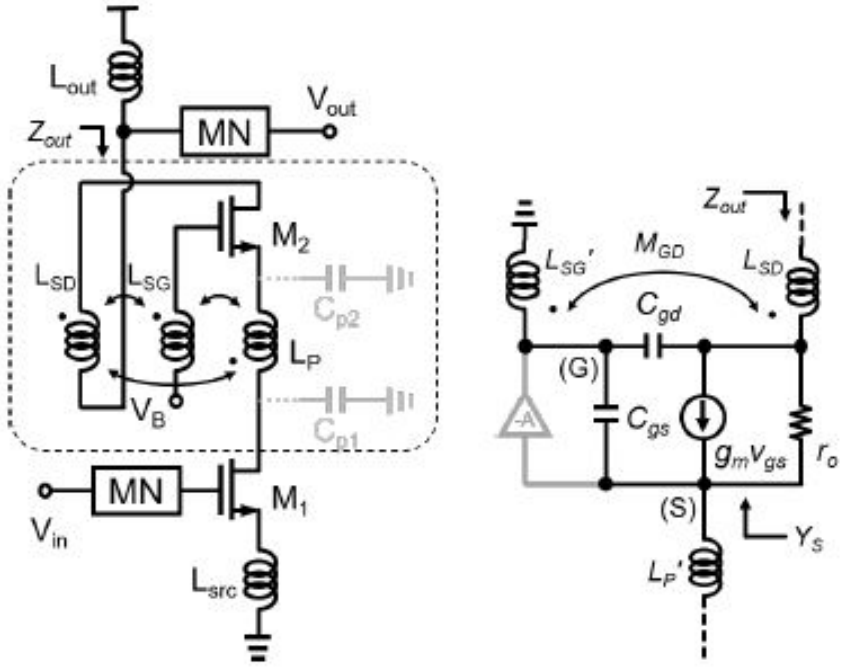


Figure 3.9: The schematic of the implemented LNA in [59].

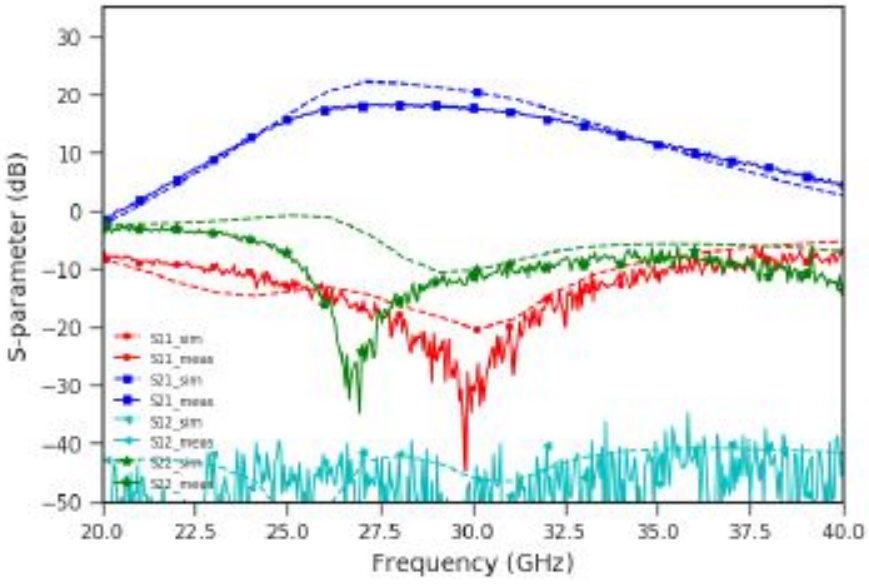


Figure 3.10: The measured and simulated S-parameters of the LNA in [60].

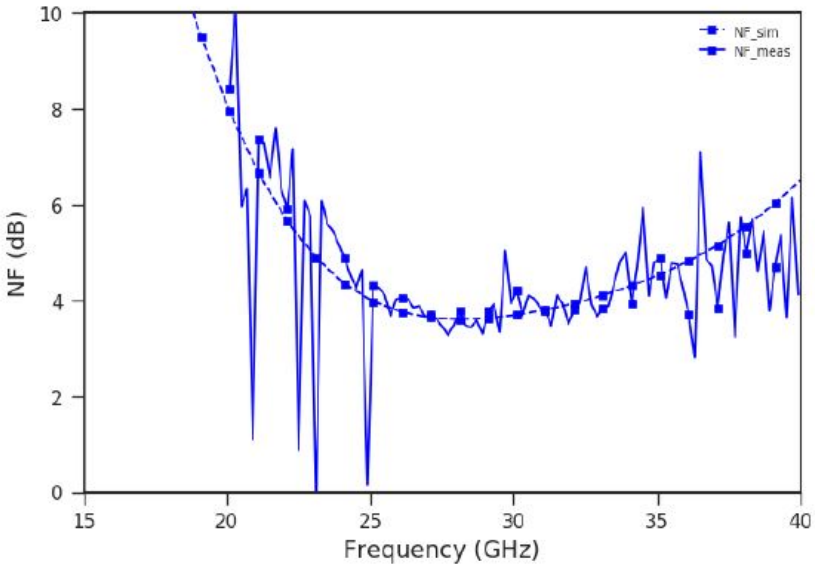


Figure 3.11: The measured and simulated NF of the LNA in [60].

ground return path is not needed. However, this has been achieved at the cost of NF deterioration by the balun loss.

3.4.2 The Proposed Architecture

The simplified GDMIF-LNA input stage is shown in Fig. 3.13(a). The circuit is a cascode with mutually induced inductors at the gate and drain. Considering a simple model of transistor[3] consisting of a transconductance (g_m) and a gate-source capacitance (C_{gs}), the gate and drain current are $V_{gs}C_{gs}s$ and $g_m V_{gs}$ respectively. Consequently, the mutual inductance can be replaced by two dependent voltage sources as illustrated in Fig. 3.13(b). The introduced feedback can also be viewed as a series-series feedback [81]. Thus, it is expected that both the input and output impedance of the amplifier is increased in magnitude compared to the no magnetic coupling case. At the amplifier's input, the feedback generates the real impedance part, and increases the impedance magnitude. Likewise at the output, the amplifier's output impedance is enhanced which results in more gain. For now, the feed forward path of the feedback network is assumed to have

[3]This is mainly to gain insight from the circuit by avoiding lengthy equations.

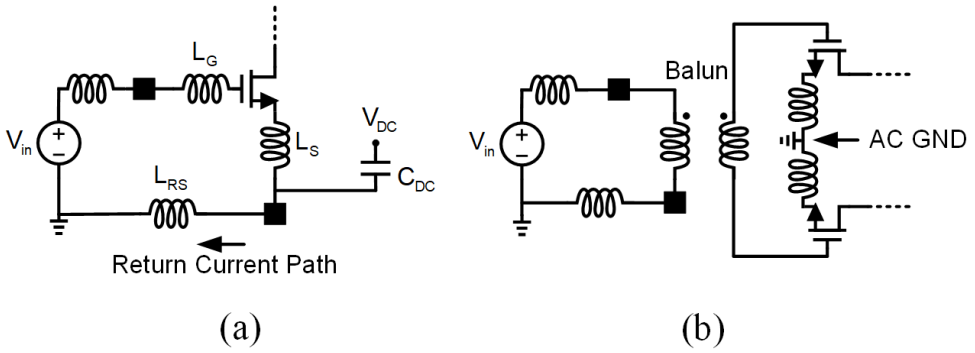


Figure 3.12: Simplified input stage of a common-source stage with inductive degeneration LNA. (a) Single-ended. The path from the off-chip input source ($\mathrm{V_{in}}$) to the chip is simply modeled by an inductor. (b) Differential. The high frequency current only flows between the differential pair. Accurate high frequency modeling of the current return path inside the chip and off-chip is not required here.

negligible effect compared to the main amplifier. That is, the drain-side dependent voltage source is neglected. This assumption is revisited in section IV. The gate dependent voltage source has an equivalent resistance which by definition is equal to the voltage divided by current, therefore,

$$r_g = \frac{M g_m V_{gs} s}{V_{gs} C_{gs} s}. \tag{3.1}$$

Replacing the angular transient frequency $\omega_{\mathrm{T}} = \frac{\mathrm{g_m}}{\mathrm{C_{gs}}}$, the equivalent resistor is calculated as

$$r_g = M\omega_T. \tag{3.2}$$

This shows that the loss-less magnetic feedback between gate-drain can generate a real impedance. This real-part impedance is a function of the mutual inductance which can be simulated to a high accuracy without being dependent on the ground path return current.

3.5 Performance Analysis

The proposed LNA architecture (depicted in Fig. 3.14) comprises 3 stages. The first stage is a GDMIF amplifier, wherein the input power matching is obtained. The input pad and ESD parasitic, modeled as a capacitor ($\mathrm{C_i}$) in parallel with the input port, lowers the input impedance. A shunt inductor ($\mathrm{L_p}$) in series with a large decoupling capacitor ($\mathrm{C_p}$) is used to boost the input

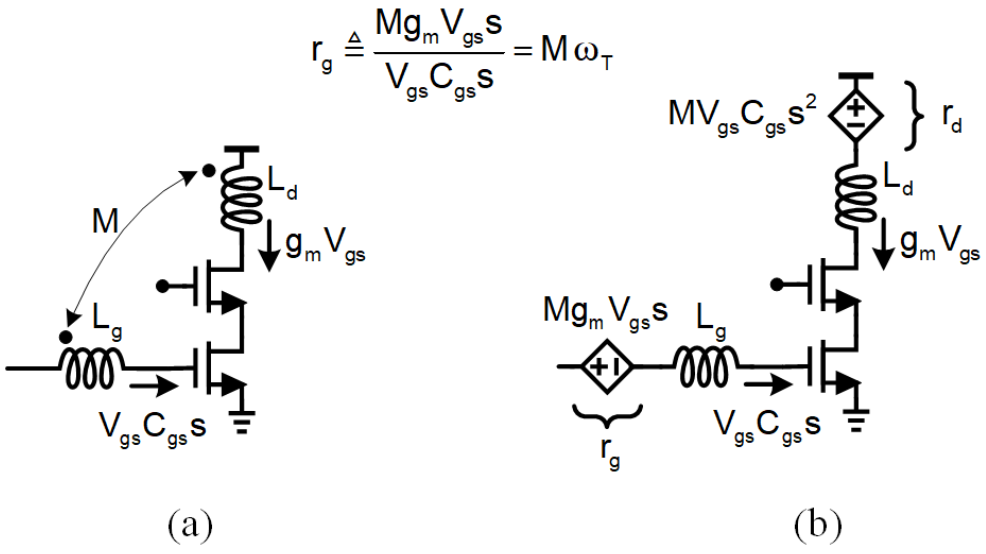


Figure 3.13: (a) The simplified architecture of the GDMIF stage. (b) The equivalent circuit derived by replacing mutual inductance with two dependent voltage sources.

impedance. This increases the voltage gain of the input matching network, hence lowers the noise degradation. The first stage is coupled to the second stage by a large capacitor (C_s) in series with an inductor (L_s) which serves as a series peaking. The second stage is a cascode with inductive load, magnetically coupled to the last stage. To achieve a better linearity performance and higher swing at the last stage, the third stage is a differential pair with gate-drain capacitive neutralization [82], [83]. The neutralization also results in a more stable behavior which is studied with more details in section IV. The 3rd stage is magnetically coupled to the single-ended output.

In the following, the operation frequency of the LNA is assumed to be from ω_L to ω_H, and the mid-band angular frequency is $\omega_M = \frac{\omega_L + \omega_H}{2}$.

3.5.1 Signal Analysis

The simplified AC model of the GDMIF-LNA (Fig. 3.14) is illustrated in Fig. 3.15. To gain insight into the factors that contribute the most to the design, a first-order analysis at mid-band frequency, with a number of simplifying approximations, is presented in the following for small signal voltage gain calculation.

In the first-stage, it is assumed that C_i is tuned out by L_p at the mid-band and also C_{gs1} is tuned

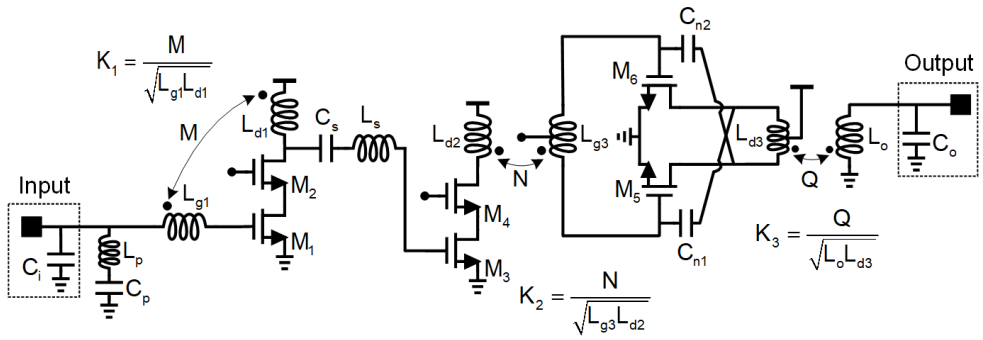


Figure 3.14: The proposed 3 stages GDMIF-LNA architecture. The input and output are both single-ended pads measured by ground-signal-ground (GSG) probes. The capacitors which model the pads and ESD parasitic are shown in parallel with the input (C_i) and output (C_o) ports.

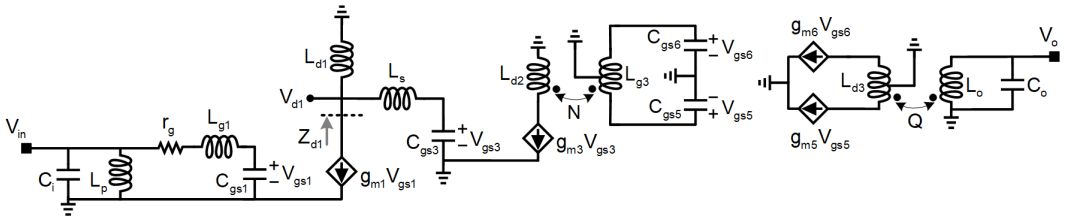


Figure 3.15: Simplified AC model of the GDMIF-LNA.

out by L_{g1}. Therefore,

$$V_{d1} = \frac{-g_{m1} V_{in} Z_{d1}}{r_g C_{gs1} s}, \tag{3.3}$$

as calculated in (3.2) $r_g = M\frac{g_{m1}}{C_{gs1}}$, Z_{d1} is the impedance seen from the drain of the first stage cascode, and $s = j\omega$. Z_{d1} is given by

$$Z_{d1} = \frac{L_{d1} s (L_s s + \frac{1}{C_{gs3} s})}{(L_s + L_{d1}) s + \frac{1}{C_{gs3} s}}, \tag{3.4}$$

where it has three zeros: At 0 and $\frac{\pm j}{\sqrt{L_s C_{gs3}}}$, and two poles located at $\frac{\pm j}{\sqrt{(L_s + L_{d1}) C_{gs3}}}$. Assuming that at the low edge of the band (ω_L) the value of L_s is chosen large enough to satisfy $\omega_L > \sqrt{\frac{1}{L_s C_{gs3}}}$, at the mid-band (3.4) is approximated by

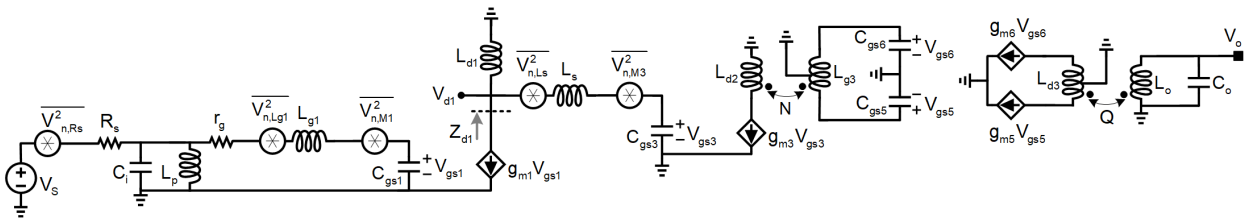


Figure 3.16: The simplified LNA noise circuit model with the four most contributing noise sources.

$$Z_{d1} \approx \frac{L_{d1} L_s s}{L_{d1} + L_s}, \tag{3.5}$$

which, as expected, denotes $\mathrm{L_{d1}} \parallel \mathrm{L_s}$. Substituting in (3.3), the gain of the first stage is given by

$$\frac{V_{d1}}{V_{in}} = \frac{-L_{d1} L_s}{M(L_{d1} + L_s)}. \tag{3.6}$$

Assuming L_{g3}-$C_{gs5,6}$ resonance frequency is higher than the high edge of the band ($\omega_{\mathrm{H}} < \sqrt{\frac{2}{\mathrm{L_{g3} C_{gs5}}}}$) and $\mathrm{L_o}$ tunes out $\mathrm{C_o}$, the gain is approximately given by

$$\frac{V_o}{V_{in}} = \frac{g_{m3} g_{m5} L_{d1} N Q}{C_{gs3} M(L_{d1} + L_s)}. \tag{3.7}$$

This shows that at mid-band, the first-order calculated gain is not a function of frequency. In practice, however, all the foregoing resonances do not take place at the same frequency which causes different peaks. It is noteworthy to mention that the presented simplified analysis is only for first-order calculations. The designed circuit needs simulation and elements tuning including accurate model of the transistors and passives which are discussed in the following sections.

3.5.2 Noise Analysis

There are several noise sources in the LNA circuit (Fig. 3.14). Noise simulation shows the contribution from all the noise sources. The main contributors to the noise, as depicted in Fig. 3.17, are: $\mathrm{M_1}$ channel noise, thermal noise due to the finite quality factor of $\mathrm{L_{g1}}$ and $\mathrm{L_s}$, and $\mathrm{M_3}$ channel noise. Fig. 3.16 shows the simplified LNA noise circuit model. The four most contributing

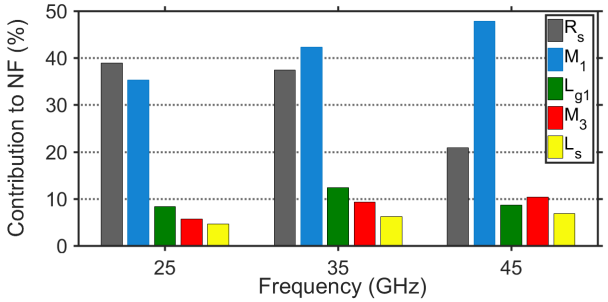


Figure 3.17: The simulated percentage of the main NF contribution, among different noise sources, at 25, 35, and 45 GHz.

noise contributors are depicted. $\mathrm{M_1}$ channel noise is $\overline{\mathrm{V^2_{n,M1}}} = \frac{4\mathrm{kT}\gamma}{\mathrm{g_{m1}}}$. Due to the finite quality factor of inductors, it is assumed that the equivalent series resistor has thermal noise of $\overline{\mathrm{V^2_{n,Lg1}}} = 4\mathrm{kTR_{Lg1}}$ and $\overline{\mathrm{V^2_{n,Ls}}} = 4\mathrm{kTR_{Ls}}$. $\mathrm{M_3}$ channel noise is $\overline{\mathrm{V^2_{n,M3}}} = \frac{4\mathrm{kT}\gamma}{\mathrm{g_{m3}}}$. The input source is depicted with the associated noise source $\overline{\mathrm{V^2_{n,Rs}}} = 4\mathrm{kTR_s}$. Referring these noise components to the input, using approximations used for the gain calculation, the noise factor at the mid-band is given by

$$NF = 1 + \frac{\gamma}{g_{m1}R_s} + \frac{R_{Lg1}}{R_s} + \left[\frac{M}{L_s}\right]^2 \left(\frac{\gamma}{g_{m3}R_s} + \frac{R_{Ls}}{R_s}\right). \tag{3.8}$$

This shows that the noise of the first stage have similar noise performance compared to the source-grounded common source with no mutual inductive coupling (between gate-drain) stage. Furthermore, the appearance of $\mathrm{g_{m1}}$ at the denominator suggests that there should be an optimal bias for the gate of first stage, trading off between maximizing $\mathrm{g_{m1}}$ and minimizing noise, wherein the optimum noise performance will be achieved.

The simulated[4] LNA NF and the minimum obtainable NF ($\mathrm{NF_{min}}$) from the LNA assuming noise optimal termination at the input (instead of $50\ \Omega$) is shown in Fig. 3.18. The proximity of the two shows that the optimum LNA NF impedance is transferred to $50\ \Omega$ by the introduced feedback at the input. In other words, simultaneous noise and power matching is achieved, most effectively over 27 to 40 GHz, and deviating at the edges of the band (22.2-43 GHz).

[4]For all the simulations, the circuit values illustrated in Fig. 3.21 is used.

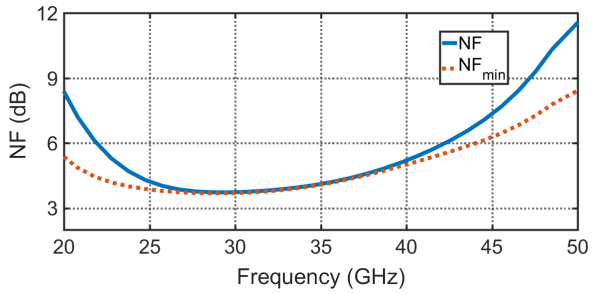


Figure 3.18: The simulated optimized LNA NF and the minimum obtainable NF (NF_{min}) from the LNA assuming optimal termination at the input (instead of 50 Ω).

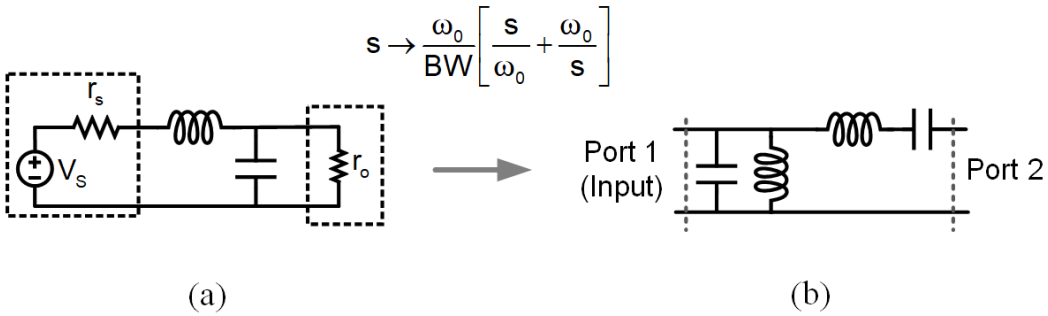


Figure 3.19: (a) A doubly terminated second-order LC-ladder low-pass filter, and the transformation to band-pass. (b) The transformed band-pass structure, and the ports definition.

3.5.3 Design Methodology for Bandwidth

The foregoing study does not address the design for bandwidth issue. Generally, an LNA needs to satisfy at least two requirements to achieve the specifications over a given bandwidth which are the input power matching ($|\Gamma| < -10$ dB) and the gain (variation less than 3 dB).

3.5.3.1 The Input Power Matching Bandwidth

Similar treatment proposed before for a common-emitter LNA with inductive degeneration [84] can be modified for the design of the GDMIF-LNA, in order to achieve the input power matching over a bandwidth.

Fig. 3.19(a) shows a doubly terminated LC low-pass filter. This response can be transformed to band-pass with the pass-band response from ω_L to ω_H. Defining $BW = \omega_H - \omega_L$ and

$\omega_0 = \sqrt{\omega_{\mathrm{H}}\omega_{\mathrm{L}}}$, the band-pass structure can be retrieved [85], as shown in Fig. 3.19(b). Since for a loss-less, reciprocal two-port network [86]:

$$|S_{11}|^2 + |S_{21}|^2 = 1, \tag{3.9}$$

near to 1 magnitude of S_{21} over the bandwidth, translates to achieving the input power matching. For instance, a Chebyshev response with 0.4 dB ripple in the pass-band, has $|\mathrm{S}_{11}| < -10\ \mathrm{dB}$ throughout the band. On the other hand, the transformed band-pass structure looks similar to the input of the LNA model, shown in Fig. 3.15 wherein the port 2 termination is assumed to be $\mathrm{r_g}$. This analogy is useful in the design procedure where all the values of the input stage, shown in Fig. 3.15, $\mathrm{C_i}$, $\mathrm{L_p}$, $\mathrm{L_{g1}}$, $\mathrm{r_g}$, and $\mathrm{C_{gs}}$ (the size of the transistor) can be calculated from the transformed band-pass structure. However, depending on the targeted frequency, it is possible that the calculated values are not robustly realizable (very small or very large) or they trade with other specification such as noise or power consumption. Additionally, the model used for the transistor and passives are quite simple and more sophisticated models are needed. Therefore, the calculated values from the transformed band-pass structure can be used as an initial value. The location of the poles and zeros of the band-pass filter, then can be mimicked by tuning the initial elements' value using a circuit simulator and more accurate models.

3.5.3.2 The Gain Bandwidth

By making offset between the aforementioned poles of the circuit, and allowing small ripples, it is possible to optimize the gain bandwidth response. The simulated S_{11} and S_{21} of the LNA is illustrated in Fig. 3.20. The lower edge of the gain drop happens mainly due to the input matching bandwidth limit (the zero due to $\mathrm{L_p}$-$\mathrm{C_p}$ resonance in Fig. 3.14), on the upper edge, however, the output of second-stage pole as well as the input matching pole cause a sharper drop in the gain. From the Chebyshev retrieved circuit, there were initially two ripples with minimum peaks in S_{11} located approximately at 32 and 40 GHz. After further optimization the first peak is moved to a slightly higher frequency, and the second peak caused a flat response (with the peak not being

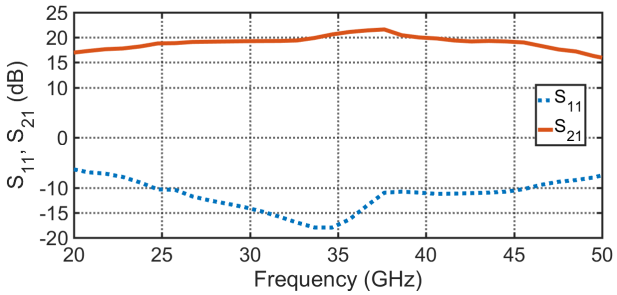


Figure 3.20: The simulated S_{11} and S_{21}.

easily detectable).

3.6 Stability

3.6.1 The GDMIF Amplifier Drain-Side Dependent Source

So far the dependent voltage source on the drain-side of the GDMIF amplifier, depicted in Fig. 3.13, was not considered. Calculating the equivalent resistor (defined in Fig. 3.13), the ratio between the voltage and the current is given by

$$r_d = \frac{MV_{gs}C_{gs}s^2}{g_m V_{gs}}. \tag{3.10}$$

Substituting $s = j\omega$ and $\omega_T = \frac{g_m}{C_{gs}}$, the equivalent resistor is calculated as

$$r_d = \frac{-M\omega^2}{\omega_T} \tag{3.11}$$

which is a negative real value for all frequencies. In fact, it can be shown that any gate-drain mutually induced feedback arrangement, creates a positive real-part on one side and a negative real-part on the other. However, the drain-side resistor magnitude is a factor of $\left(\frac{\omega}{\omega_T}\right)^2$ smaller than the gate-side equivalent resistor. Therefore, in the current case, the main effect of the drain-side negative real-part is to make the quality factor of the drain inductor (Q_{Ld}) in Fig. 3.13 larger. Nevertheless, the following inequality should be satisfied at all frequencies to have a net positive real-part:

$$\frac{M\omega\, Q_{Ld}}{L_d\, \omega_T} < 1. \tag{3.12}$$

In the fabricated prototype process, this was satisfied without the need to add *de-Q* series or parallel resistance. In general, this might not be the case and sufficient de-Q resistor should be added to make sure at all frequencies and over different process corners there is no stability issue.

3.6.2 Other Stability Considerations

Considering a common source stage (source grounded) with an inductor at the drain, it can be shown that the real-part of the input admittance, looking at the gate, is negative for frequencies below resonance frequency of the drain inductor and the gate-drain capacitance [80]. This is one of the main reasons of cascode structure popularity in mm-wave. In this work, for the first two stages, cascode structure is used to substantially alleviate this issue. For the last stage, however, using a cascode will reduce the voltage swing at the output by at least an overdrive voltage, hence puts an upper limit on $\mathrm{P_{1dB}}$. A differential common source with gate-drain capacitor neutralization will mitigate the stability issue. In addition, the transistors' even order nonlinearity terms will be canceled.

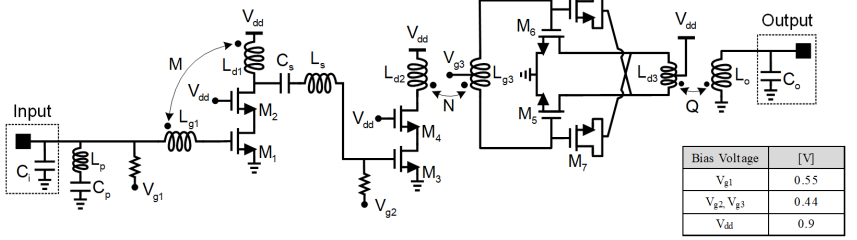
Stability simulation checks based on the Rollet's condition[5] [86] is used for each stage and the cascaded stages. For the third stage, which is differential, both the even mode (common mode) and the odd mode (differential mode) stability criteria based on the Rollet's condition is simulated which all pass the necessary stability condition, positive real impedance.

3.7 Circuit Realization

3.7.1 The Implementation Considerations

The schematic of the entire LNA is illustrated in Fig. 3.21. The input pad capacitor and the electrostatic discharge (ESD) parasitic capacitor is modeled by $\mathrm{C_i}$. At the output pad, no ESD protection is used, hence only the pad capacitor shows up. The used ESD protection diodes and the bus clamp are from the process standard library and they successfully pass the machine model

[5]This is a necessary condition, not sufficient.



Bias Voltage	[V]
V_{g1}	0.55
V_{g2}, V_{g3}	0.44
V_{dd}	0.9

Self or Mutual Inductance	[pH] (At 35 GHz)
L_p	221
L_{g1}	969
L_{d1}	280
M	125
L_s	636
L_{d2}	178
N	131
L_{g3}	345
L_{d3}	758
Q	774
L_o	1152

Device	W [nm] / L [nm]
M1, M2	21600 / 30
M3, M4	43200 / 30
M5, M6	36000 / 30
M7, M8	16200 / 30

Capacitor	[fF]
C_i	87
C_p	562
C_s	370
C_o	47

Figure 3.21: The entire LNA schematic along with the component values.

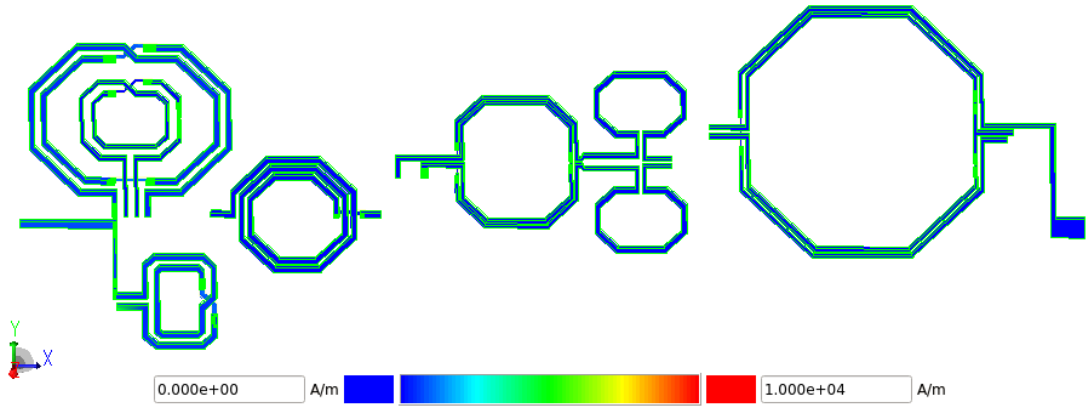


Figure 3.22: Whole EM simulation set up (ground shields hided for visibility). The contours illustrate the relative surface current density magnitude simulated at 35 GHz.

ESD test.

The inductors are simulated all together in Momentum ADS to account for the coupling between the inductors as shown in Fig. 3.22. The EM set-up has been double checked at low frequencies with the process provided models and cross checked with HFSS which all show a close agreement. Custom-designed density DRC fills which fulfill the minimum metal density requirements of the process are used nearby sensitive layout sections to alleviate the change in results due to the automatic metal density fill which could not be simulated with available resources.

To pass the electromigration requirements, stair-case interconnect for drain and source connections are used in the third and second stage. this result in a lower parasitic capacitance, specially between the drain and source.

3.7.2 Gate-Drain Capacitor Neutralization

Due to a better process matching obtainable between two transistors overlap capacitor (the overlap of the gate poly with the source and drain area), compared to a transistor overlap capacitor and a process capacitor, M_7 and M_8 are used to cancel the gate-drain capacitor of M_5 and M_6. The condition to keep M_5, M_6 in saturation, ensures that M_7, M_8 are off. Having M_5, M_6 in saturation and M_7, M_8 off, the ratio between the neutralization capacitor to the gate-drain capacitor of M_7, M_8 is given by $\frac{2\mathrm{W}_7}{\mathrm{W}_5}$ where W_5 and W_7 are the width of M_5 and M_7 respectively. This ratio, which can be considered as the percentage of neutralization, is kept to 90% in order to have a margin from a negative net capacitor at the input of the third stage.

3.8 Fabrication and Measurements

As a proof of concept, the prototype is fabricated in Taiwan semiconductor manufacturing company (TSMC) 28 nm bulk CMOS process. The chip micrograph is illustrated in Fig. 3.23. The custom-designed density DRC fill cells, mentioned earlier, which are manually placed near sensitive layout sections (mostly near the inductors), are visible from the micrograph. The photo of the designed PCB bottom and top (two layers) metalization is depicted in Fig. 3.24 and Fig. 3.25 respectively. The photo of the fabricated PCB is shown in Fig. 3.26. The supply voltage and DC biases are provided with 1.5 mil (diameter) gold bondwires. The inductance of bondwires are estimated to be less than 1 nH, although simulation shows that twice larger inductance can be tolerated without noticeable changes in the results. The PCB pads' finishing is electroless nickel electroless palladium immersion gold (ENEPIG) which makes low-loss and robust connection to gold bondwire. The chip is pasted on a printed circuit board (PCB) using non conductive epoxy (shown in Fig. 3.27). The input and output connections are ground-signal-ground (GSG) pads with 100 $\mu\mathrm{m}$ pitch. Standard GSG probes (cascade Microtech I40-A-GSG-100) are landed on the pads. The photo of the probe and probe calibration substrate are shown in Fig. 3.28 and Fig. 3.29 respectively. The probe under microscope set-up is shown in Fig. 3.30.

In the following, a few photos of the measurement set-up is presented. The probe station's

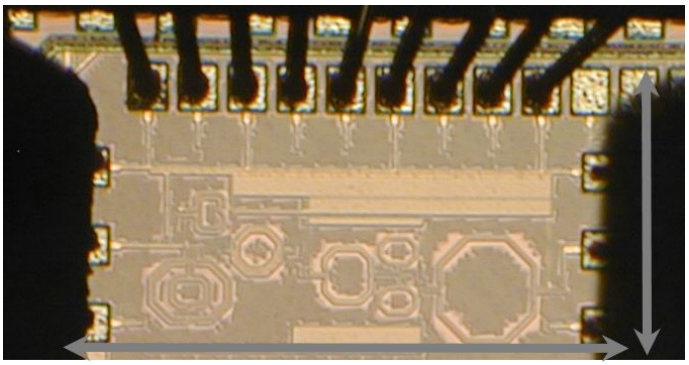


Figure 3.23: The chip micrograph. The total area (indicated by the arrows) is 809×412 μm^2. The active area (pads excluded) is 673×344 μm^2.

chulk is shown in Fig. 3.31. The whole measurement set-up is illustrated in Fig. 3.32. The connections to the VNA and bias tee is illustrated in Fig. 3.33 and Fig. 3.34, respectively.

3.8.1 Scattering-Parameters

The probes are connected via 2.4 mm cables to the vector network analyzer (VNA). The VNA which is used in all the measurements is ROHDE&SCHWARZ ZVA 67 which has four ports and operates over 10 MHz to 67 GHz. The photo of the VNA and its calibration kit is shown in Fig. 3.35 and Fig. 3.36, respectively. The set-up is calibrated up to the probes' tip (the reference plane is probes' tip). For the calibration, standard substrate with different terminations is used. Consecutively, terminations of short, open, load (50 Ω), and thru (SOLT) are performed on the probes, and the results are referenced in the VNA for calibration. The calibrated probes show input matching of better than -27 dB across 1-50 GHz with resolution bandwidth (RBW) of 100 Hz. In order to reduce the random noise in the data, multiple measurement data are averaged over 4 bonded chips which were randomly selected from the fabricated and diced dies. The simulated and measured scattering parameters of the LNA are shown in Fig. 3.37. The measured input matching of better than -10 dB is achieved over 22.2 - 46.8 GHz. Over the whole measured bandwidth (1 - 50 GHz), both the input and output matching are below 0 dB, which indicates that the real-part of the input (and output) impedance is positive, therefore, necessary condition of stability is passed. S_{12} is below -40 dB throughout the band which shows a decent isolation from the output to input.

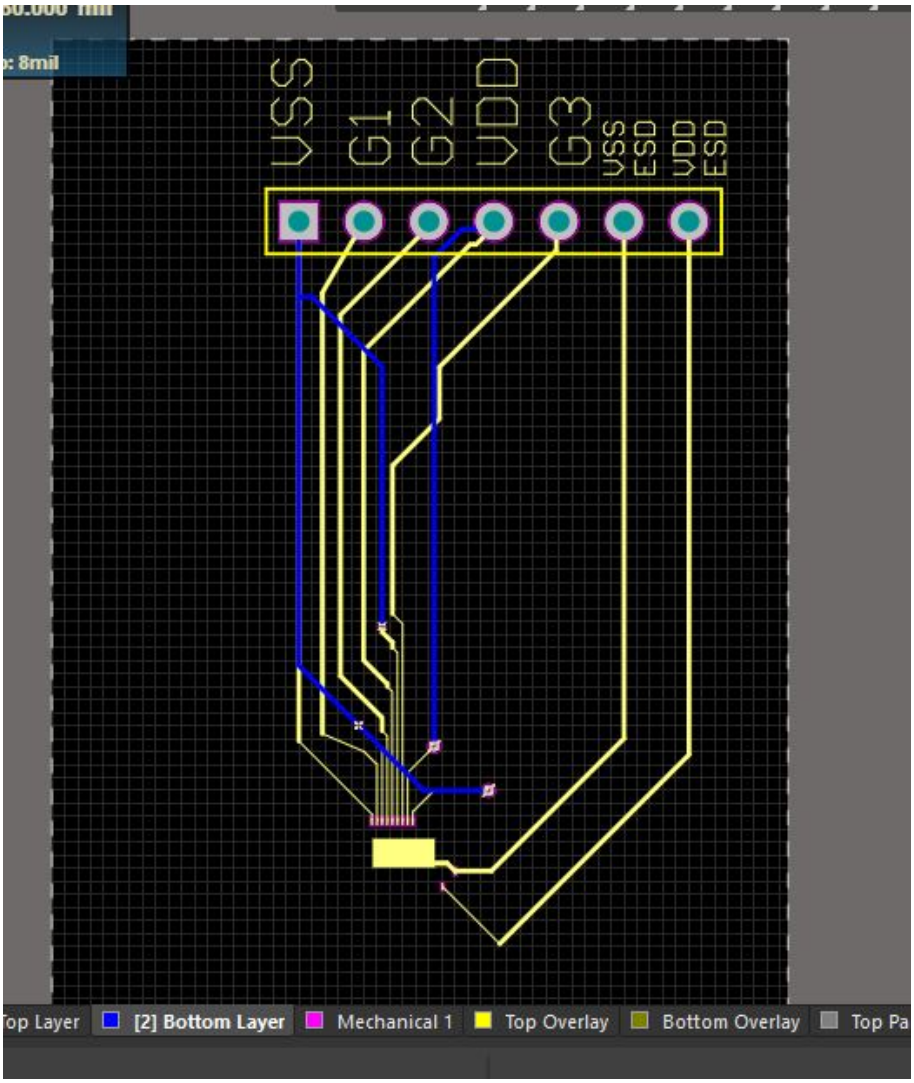


Figure 3.24: The bottom metalization of the designed PCB.

The gain (S_{21}) has a 21 dB peak at 25.5 GHz. The 3 dB gain BW then would be from 21.8 - 40 GHz. Nonetheless, by increasing the second and third stage voltage bias, it is possible to increase the gain at the higher edge of the band (by +2.5 dB), and achieve BW of 21.8 - 43 GHz. This comes at the cost of 6 mA higher current consumption from the 0.9 V supply. The measured resut of S_{22} shows better than -7 dB output matching at the lower edge which improves significantly towards the higher edge.

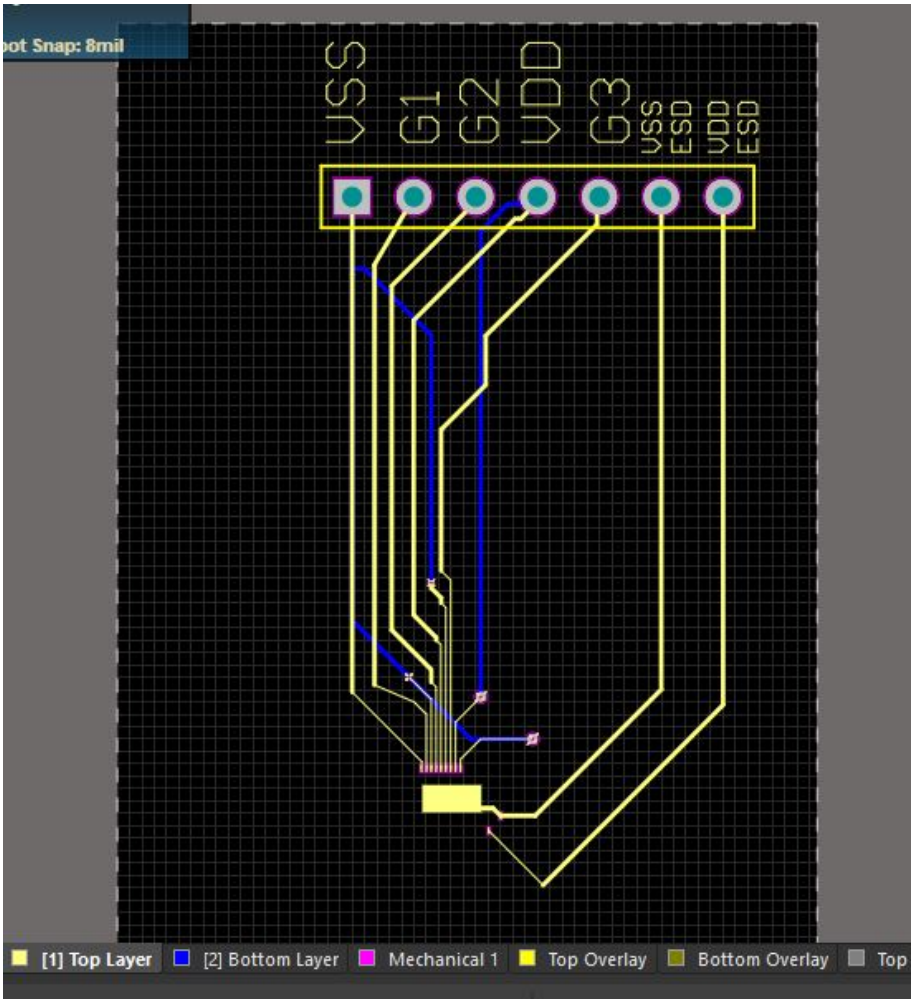


Figure 3.25: The top metalization of the designed PCB.

3.8.2 Noise

The NF is measured using Y-factor method. A commercial cold/hot noise source is used (PASTERNACK, PE85N1008, 100 MHz to 40 GHz noise source with nominal ENR of 15.5 dB. The noise source and the nominal ENR is depicted in Fig. 3.38 and Fig. 3.39, respectively). The measured ENR varies from 14.1 dB to 16.9 dB. For the NF measurement, the noise source is biased by the 28 V supply and the RF port is connected via probe to the input of the LNA. The output is screened at the spectrum analyzer (ROHDE&SCHWARZ FSV SIGNAL ANALYZER operating over 10 Hz - 40 GHz). The photo of the used spectrum analyzer is shown in Fig. 3.40. The two dominant sources of inaccuracy in this measurement are: spectrum analyzer NF, and the input

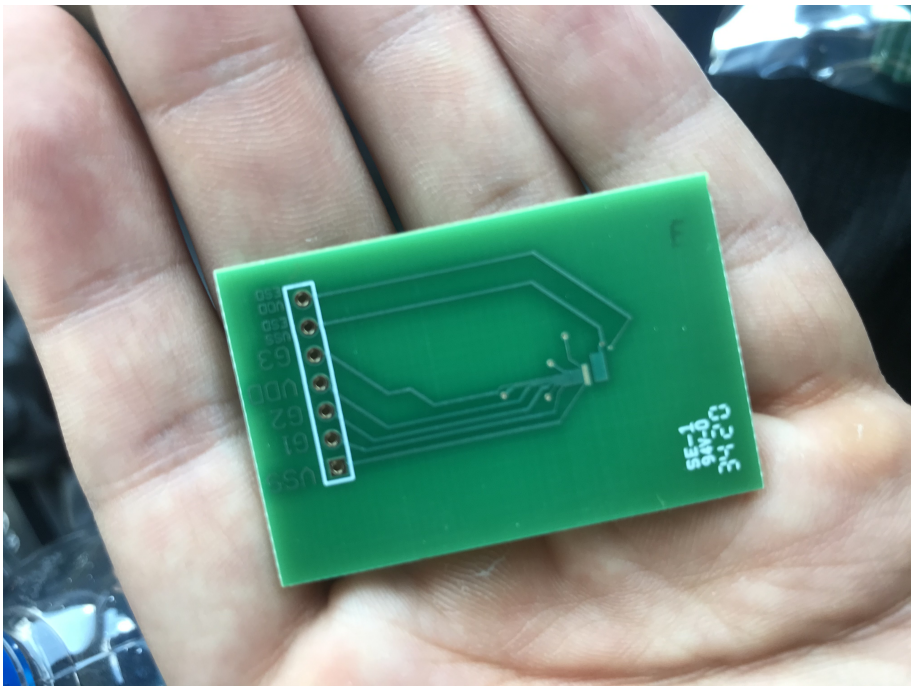


Figure 3.26: The fabricated PCB.

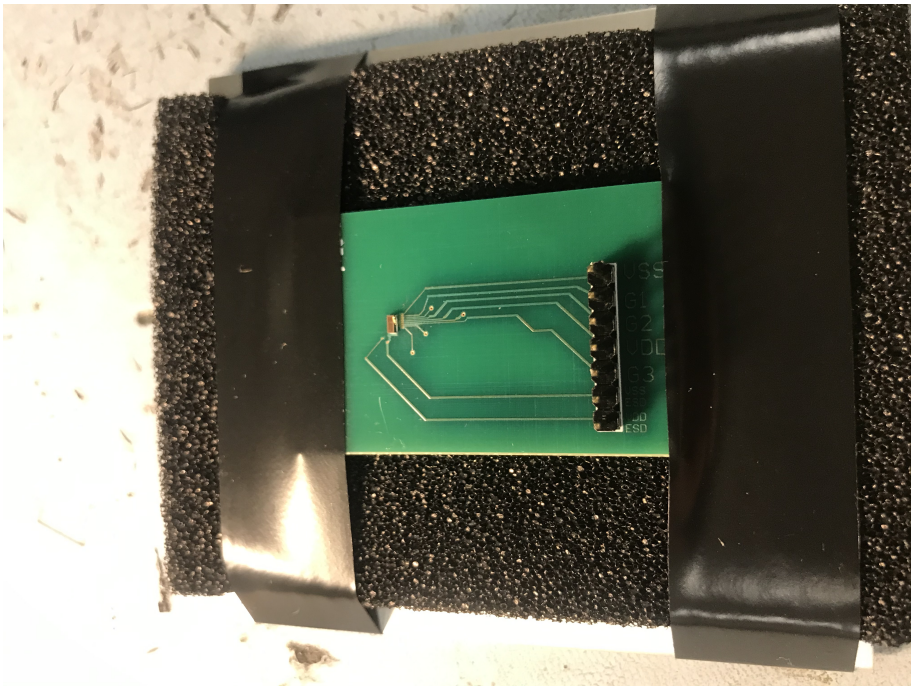


Figure 3.27: The taped chip on the PCB.

Figure 3.28: The used GSG probe in the protecting package.

connection loss. Both are measured, calibrated, and subtracted, as explained in the following. The NF of the spectrum analyzer is measured separately by the cold/hot source, and accordingly is subtracted. The loss of the input cables are also measured and the noise contribution[6] is subtracted at the measurement temperature (78°F, 298.7 K). The noise measurements performed in this work, has followed the steps suggested in [87]. The measured NF of the LNA is shown in Fig. 3.41. The measurement frequency is limited by the spectrum analyzer high edge operating frequency of 40 GHz.

3.8.3 Linearity

The VNA (ZVA 67) can provide tones with controllable frequency and amplitude in the continuous-wave (CW) mode of operation. Basically it can operate as a signal generator. A single tone is applied to the LNA input and the output power is monitored. The measurement and simulation results of the output 1-dB compression point ($\mathrm{OP}_{-1\mathrm{dB}}$) vs. frequency is shown in Fig. 3.43. Due to the 40 GHz high-edge limit of the spectrum analyzer, the measurements are performed up to 40

[6] In the hot mode.

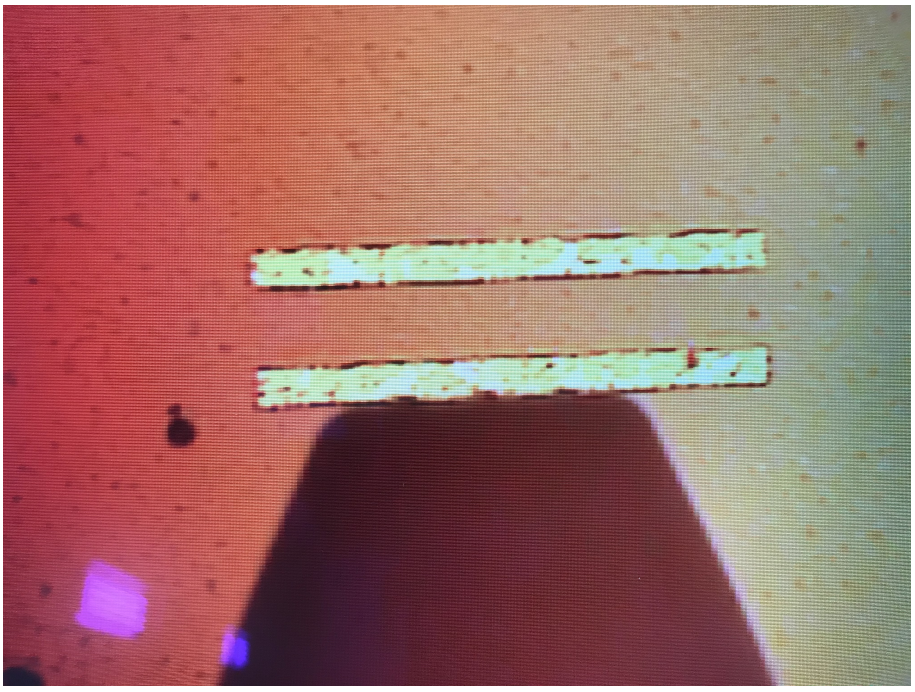


Figure 3.29: GSG probe calibration substrate (short).

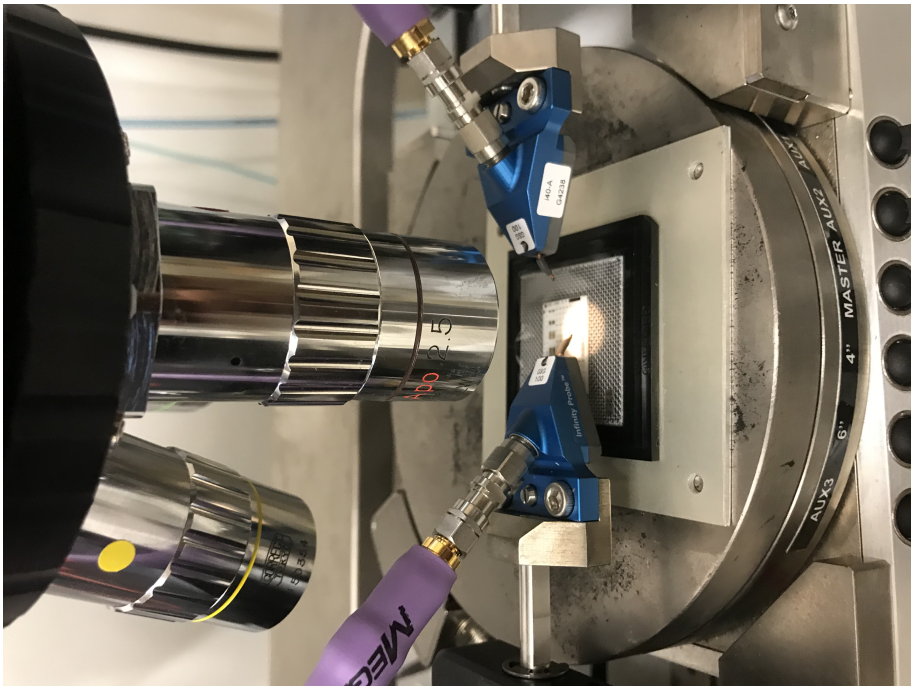


Figure 3.30: The probe and microscope set-up.

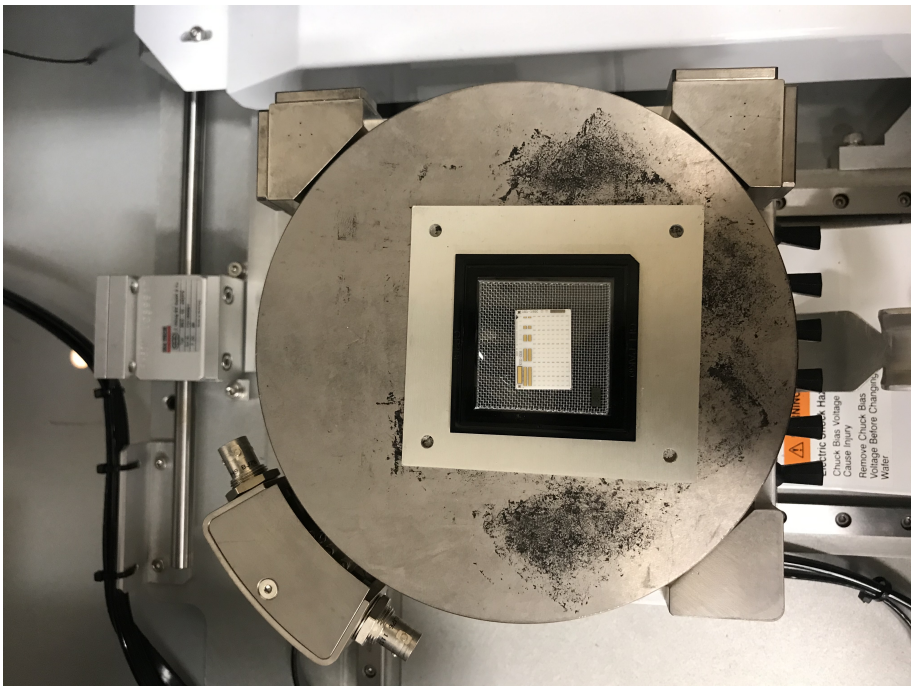


Figure 3.31: The chalk on the probe station. The main role is to provide vacuum to hold the measurement set-up securely.

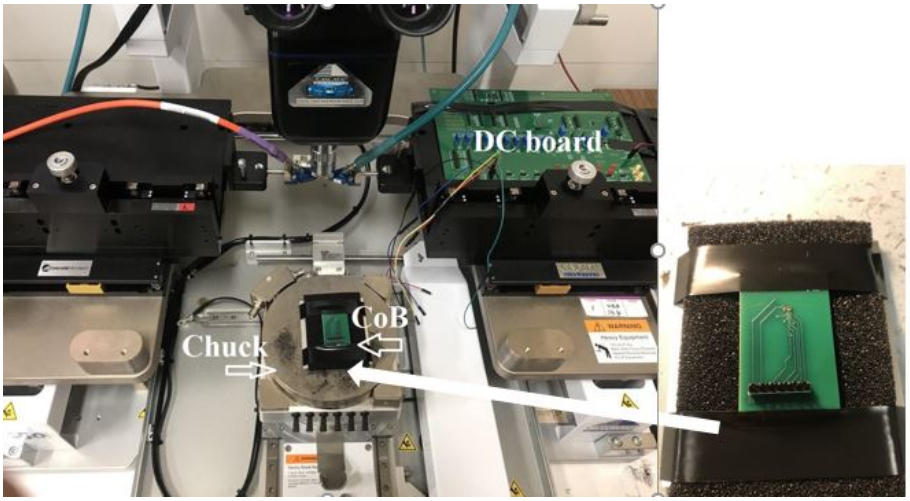


Figure 3.32: Measurement set-up.

GHz. For the two-tone test, the tones are generated from two ports of the VNA and are combined by a commercial combiner (CS1840K). The photo of the divider is depicted in Fig. 3.42. The third inter-modulation terms (IM_3) are observed at the spectrum analyzer. The measurement and

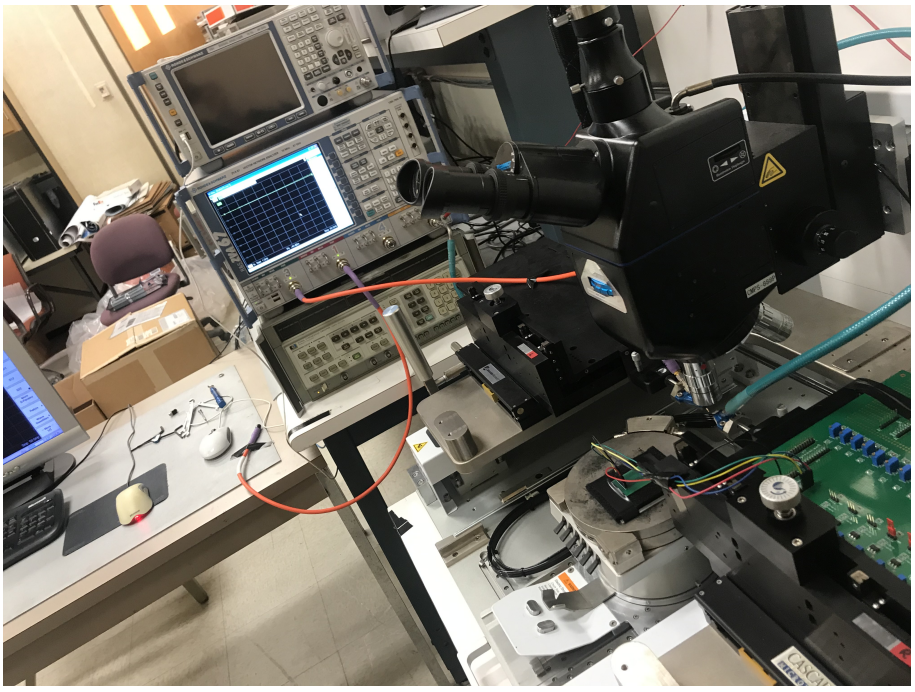


Figure 3.33: Measurement set-up, connection to the measurement devices.

Figure 3.34: The bias tee and connection to the VNA input.

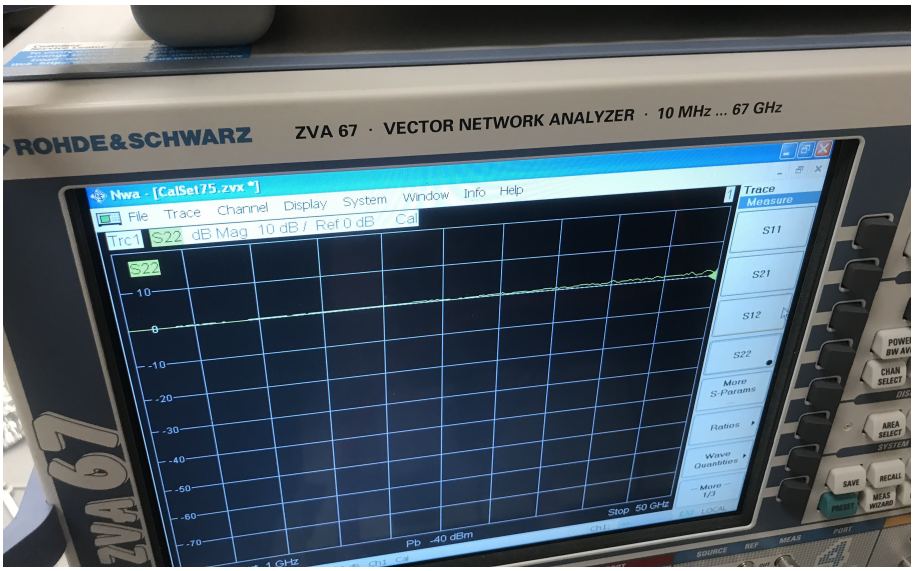


Figure 3.35: The used VNA.

simulation results of the IIP_3 vs. frequency is illustrated in Fig. 3.44. The offset between the two tones is 100 MHz for all center frequencies. Because of the wide BW of the LNA, the measured changes due to offset frequency is not considerable.

Table 3.1: Measurement summary and comparison with recently published mm-wave LNAs.

Specification	RFIC'19 [58]	RFIC'18 [66]	MWCL'18 [71]	This work
RF frequency [GHz] ‡	24-43	29-37	26-33	22.2-43
Peak Gain [dB]	23	28.5	27.1	21.1
NF [dB]	3.1-3.7	3.1-4.1	3.3-4.3	3.5-5.3 §
$\mathrm{OP}_{\text{-1 dB}}$ [dBm]	N/A	N/A	5	AVG=5.1, peak=6.4 † §
Power consumption [mW]	20.5	80	31.4	22.3
FoM* **[MHz]**	540	245	470	7857
$\mathrm{FoM}_2^{\odot}$ [$\frac{\mathrm{GHz}}{\mathrm{mm}^2}$]	2.45	1.17	1.8	35.7
IIP_3 [dBm]	-19.3 – -13.2	-12.5	-12.1	AVG=-3, peak=-1.9 † §
Supply voltage(s) [V]	1, 1.6	2	1.1	0.9
Active area [mm^2]	0.22	0.21	0.26	0.22
Technology	22 nm FD-SOI	0.25 μm SiGe BiCMOS	40 nm CMOS	28 nm CMOS

‡ Similar BW definition is used.

* $\mathrm{FoM} = \frac{\mathrm{Gain}\times\mathrm{BW}\times\mathrm{IIP}_3}{\mathrm{P_{DC}}\times(\mathrm{F}-1)}$.

$\odot$ $\mathrm{FoM}_2 = \frac{\mathrm{Gain}\times\mathrm{BW}\times\mathrm{IIP}_3}{\mathrm{P_{DC}}\times(\mathrm{F}-1)\times\mathrm{Area}}$.

† Average (AVG) and peak (peak) values through the BW.

§ Measured up to 40 GHz.

Figure 3.36: The calibration terminations (loads) of the VNA.

3.8.4 Comparison With Prior Art

Assuming the definition of an LNA bandwidth as the band wherein the input matching is better than -10 dB, and the maximum to minimum gain variation is less than 3 dB, the bandwidth of the measured LNA is from 22.2 - 43 GHz. The average gain through this bandwidth is 18.9 dB[7] (8.8 in linear scale) with 21 dB gain peak. This accounts to gain-bandwidth product of 8.8×20.8 which is 183 GHz. To the best of authors' knowledge this is a record among multi-stages[8] Ka-band (26.5

[7]Both the gain and power consumption are averaged in the high-gain/high-power mode.

[8]Distributed amplifiers can provide similar and higher gain-bandwidth product at the cost of significant higher power [88].

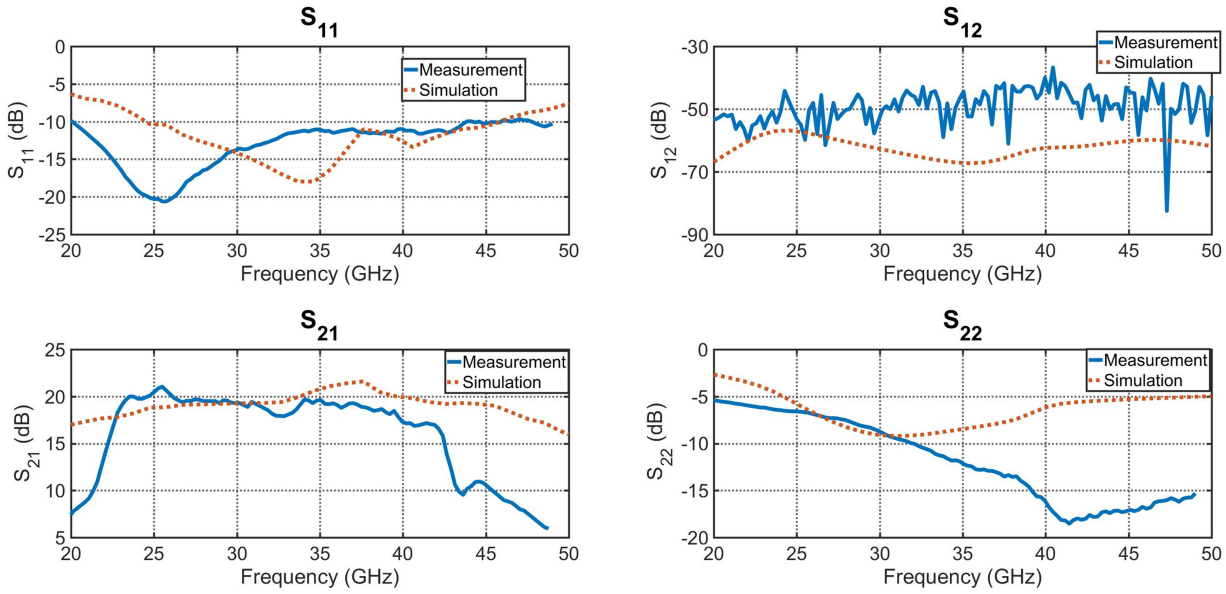


Figure 3.37: The measured and simulated scattering parameters of the LNA over 20-50 GHz.

Figure 3.38: The commercial 1-40 GHz noise source.

- 40 GHz) LNAs reported. A popular figure of merit (FoM) for LNAs characterization is defined

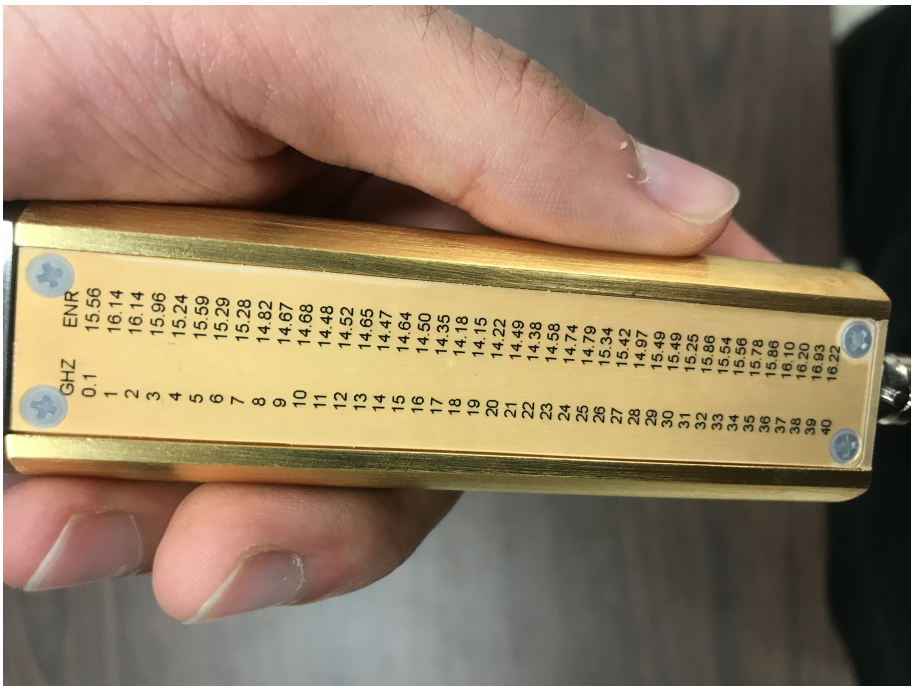


Figure 3.39: The characterized excess noise ratio (ENR) at different frequencies.

Figure 3.40: The used spectrum analyzer (Rohde & Schwarz FSV singnal analyzer).

as

$$\mathrm{FoM} = \frac{\mathrm{Gain}\,[\frac{\mathrm{V}}{\mathrm{V}}] \times \mathrm{BW}\,[\mathrm{Hz}]\ \times \mathrm{IIP_3}\,[\mathrm{mW}]}{\mathrm{P_{DC}}\,[\mathrm{mW}] \times (\mathrm{F}-1)}. \tag{3.13}$$

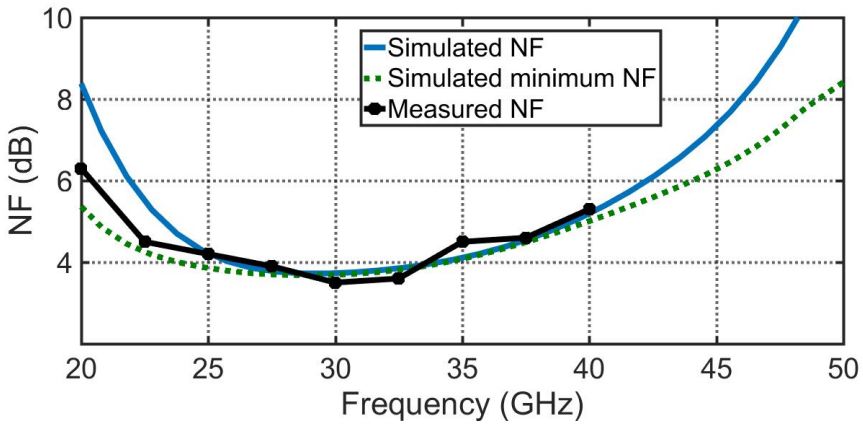


Figure 3.41: The simulated NF, the simulated minimum NF (with optimum source termination), and the measured NF. The measured NF higher edge is limited by the spectrum analyzer BW. The NF is measured over 20 - 40 GHz.

Figure 3.42: The commercial power combiner and divider (CS1840K).

Substituting average value for all these specifications through the BW, the FoM is calculated to be 7857 MHz. Compared with the recently published state-of-the-art, this is a record between both bulk CMOS and SOI reported Ka-band LNAs. The measurement summary and comparison with recently published mm-wave LNAs is shown in Table 3.1. The FoM (which includes linearity

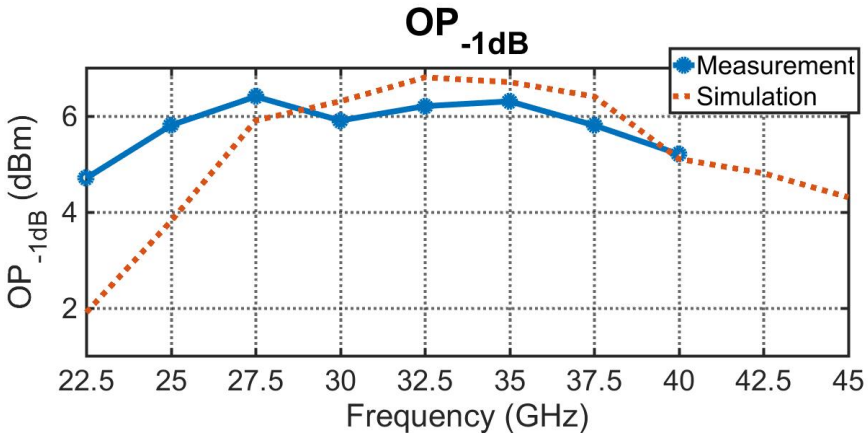


Figure 3.43: The measured and simulated output 1-dB compression point ($\mathrm{OP}_{-1\mathrm{dB}}$) versus frequency.

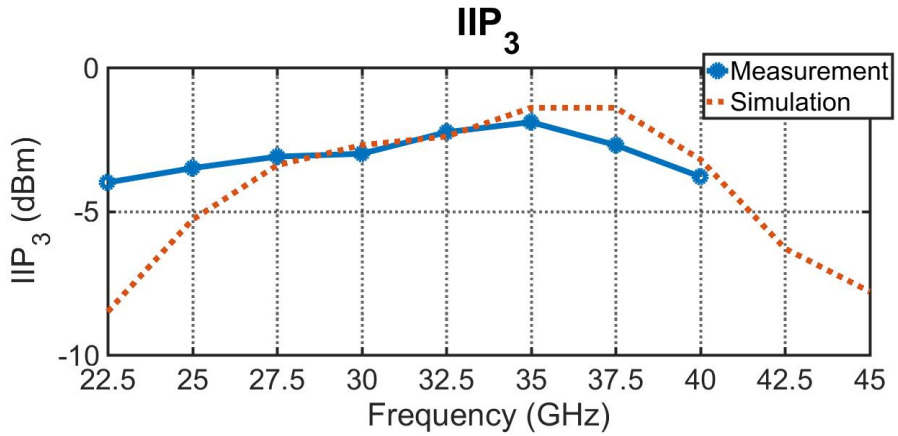


Figure 3.44: The measured and simulated result of the two-tone test in IM_3 measurement. IIP_3 versus RF frequency is depicted. The offset between the two tones is 100 MHz.

performance) is around an order of magnitude higher than the previous reported LNAs. The main reason for this is the high BW and high linearity, which is mainly achieved by the last stage architecture. The differential pair with the differential to single-ended transformer at the output (Fig. 3.21) eliminates even-order nonlinearity terms, hence improves the linearity performance compared to single-ended counterparts. There are two main drawbacks for this approach: the increase in the area (because of the transformers) and power consumption.

3.9 Conclusion

A new architecture for obtaining the input power matching at the LNA input is proposed. It is shown that this architecture is capable of achieving simultaneous power and noise matching over a large bandwidth. In the measured fabricated prototype, an average gain of 18.9 dB with the peak gain of 21 dB is measured over 22.2 to 43 GHz. The average power consumption is 21.7 mW. Minimum NF of 3.5 dB, and average NF of 3.9 dB is measured throughout the BW. Summarizing the measurement results with recently reported LNAs over similar BW, considerable higher FoM is achieved in comparison with CMOS, and FD-SOI of similar and lower nodes.

4. CONCLUSIONS AND FUTURE WORK

In the SIC full-duplex project, a wideband receiver with front-end self-interference suppression is proposed. The main goal of the cancellation is to avoid the front-end desensitization and saturation. Two important aspect of this work can be further invested. First, it is very interesting to implement and demonstrate a full transmit to receive link. This requires a transmitter and more domains of cancellation such as propagation domain and digital domain cancellation. Second interesting aspect is to combine the wideband property of the receiver with opportunistic band selection coming from cognitive radios literature. This will show an efficient and flexible radio in terms of spectrum usage. With utilization of more and more wireless cognitive, these type of spectra-efficient radios can be of huge importance in the future design of wireless networks. Although the usage of untapped mm-wave frequency range is highly invested for next generation of communication such as 5G, the complication due to scattering of waves in these frequency ranges and lower intrinsic performance of IC blocks such as gain and noise makes robust connection in a dynamic environment very challenging. Thus, utilization of RF frequency range (which is plays an important role also in 5G at sub 6-GHz range) is needed to enhance the connection much less sensitive to the environment. As it is well-known the light travels line-of-sight and is blocked by most non-transparent objects. The situation for RF frequency range electromagnetic waves is very different. As we have all experienced, it is possible to have wireless connection in an entirely closed room, as an example a phone call can be made in such a room with GSM standard which works at RF range. If there is no source of light in the room, however, the room remains dark. The mm-wave frequency wave are somewhere in between the RF frequency and visible light. Although they are much closer to the RF frequency, many of their scattering property shows that a practical wireless link works most reliably with a transmit and receive link in line of sight with the other communication node.

In spite of the interesting scattering property of RF frequency range electromagnetic waves, these frequencies are fundamentally limited by the BW they can provide and to meet the exponen-

tial need for wireless throughput, there is no choice but moving to higher and higher frequencies. LNAs are an important block in an receiver chain where the sensitivity of the receiver is mainly set by the LNA NF. The new architecture of the proposed GDMIF-LNA is shown to be capable of achieving wideband and low noise performance. The high FOM of this LNA shows that it can be used in different applications to provide a low-cost, robust, and high performance LNA. Regarding future work, the implementation of this LNA architecture at other frequency ranges and study of its behavior at RF frequency are the main remaining work that can be furthered studied and invested.

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