HIGH-K BASED METAL OXIDE DEVICE WITH LIGHT EMITTING APPLICATIONS

A Thesis

by

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ABSTRACT

The electrical and optical characteristics of the ZrHfO, WO_x, WO_x embedded ZrHfO solid state incandescent light emission devices (SSI-LED) have been explored. SSI-LED is made from the high-*k* MOS capacitor after the dielectric breakdown takes place in oxide layer. Therefore, the electrical properties such as interface defect density, oxide trapped charge density, equivalent oxide thickness, and leakage current density of SSI-LED have been investigated along with oxygen and nitrogen PDA to obtain excellent light emitting properties. Since ZrHfO high-*k* material has superb gate dielectric properties, e.g., high crystallization temperature, low interface state density, oxide trapped charges, and high effective *k* value, it has been used into MOS capacitor to obtain great performance. Applying the gate voltage above certain magnitude, i.e. breakdown voltage, the ZrHfO SSI-LED forms and emits the warm white light with high color rendering index (CRI, very close to 100) and low color correlated temperature (CCT) comparing to the commercial YAG:Ce white LED. On the other hand, the WO_x MOS capacitor as well as SSI-LED has been studied. The increased light intensity is observed due to the high emissivity coefficient of tungsten component; however, the reliability concern may arise from the high leakage current. Therefore, the three-layer WO_x embedded ZrHfO high-*k* stack is introduced. With the including of tungsten into ZrHfO bulk oxide, the great capacitor characteristics have been preserved, and emission intensity of SSI-LED has been increased as well. In addition, the environmental factors, i.e. humidity and temperature, and gate material influence on the MOS capacitor has been examined.

DEDICATION

This thesis is dedicated to my father Chun-Yi Lin, my mother Hsiu-Yun Wu, and my brother, Kuan-Fu Lin. My parents have been continually encouraging and supporting through every academic and personal endeavor in my life. Thanks mom and dad for always believing in me to strive for my dreams.

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Contributors

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TABLE OF CONTENTS

Page

ABSTRACT ii

DEDICATION iii

ACKNOWLEDGEMENTS iv

CONTRIBUTORS AND FUNDING SOURCES v

TABLE OF CONTENTS vi

LIST OF FIGURES ix

LIST OF TABLES xiii

CHAPTER I INTRODUCTION 1

1.1 High-*K* Gate Dielectrics 1
1.2 Zirconium-Doped Hafnium Oxide 2
1.3Light Emitting Device 3
1.3.1 General Background of the Light Emitting Device (LED) 3
1.3.2 Solid State Incandescent LED (SSI-LED) 6

CHAPTER II EXPERIMENTAL 8

2.1 Introduction 8
2.2 Process Flow of Solid State Incandescent Light Emission Device 8
2.3 Plasma Deposition and Annealing 12
2.3.1 RF Magnetron Sputtering System 12
2.3.2 Furnace Annealing 15
2.4 Electrical Characterization 16
2.4.1 Electrical Characterization System Setup 16
2.4.2 C-V Curve Measurement 18
2.4.3 J-V Curve Measurement 19
2.5 Optical Properties Characterization 20

CHAPTER III GATE ELECTRODE MATERIAL EFFECT ON CHARACTERISTICS OF ZIRCONIUM-DOPED HAFNIUM OXIDE MOS CAPCITOR 21

3.1 Introduction......21
3.2 Experimental......22
3.3 Electrical Properties of Molybdenum Gated MOS Capacitors......24
3.4 Electrical Properties of Copper Gated MOS Capacitors......27
3.5 Summary......30

CHAPTER IV ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K BASED SSI-LED......31

4.1 Introduction......31
4.2 Experimental......32
4.3 Electrical Properties Characterization......35
4.4 Optical Properties Characterization......39
4.5 Environmental Effect on Resistance......42
4.5.1 Low $|-V_g|$ range (-1 V to -5 V)......42
4.5.2 High $|-V_g|$ range (> |-10V|)......44
4.5.3 Temperature Effect on Resistance......45
4.5.4 High Humidity and High Temperature Annealing Effect......48
4.6 Summary......49

CHAPTER V TUNGSTEN OXIDE HIGH-K BASED SSI-LED......51

5.1 Introduction......51
5.2 Experimental......51
5.3 Electrical Properties Characterization......52
5.4 Optical Properties Characterization......55
5.5 Summary......57

CHAPTER VI TUNGSTEN OXIDE EMBEDDED ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K BASED SSI-LED......59

6.1 Introduction......59
6.2 Experimental......59
6.3 Electrical Properties Characterization......61
6.4 Optical Properties Characterization......64
6.5 Summary......69

CHAPTER VII COMPARISON OF THREE KINDS OF HIGH-*K* BASED SSI-LEDS......71

7.1 Introduction......71
7.2 Experimental......71
7.3 Electrical Properties Characterization......72
7.4 Optical Properties Characterization......79
7.5 Summary......86

CHAPTER VIII SUMMARY AND CONCLUSIONS 87

REFERENCES 92

LIST OF FIGURES

Page

Figure 1. Blackbody radiation curves for incandescent lamp operating at different power ratings. Shaded area shows visible light wavelength region. [9]............4

Figure 2. A p-n junction under (a) zero and (b) forward bias. E_C, E_f and E_v are the conduction band, Fermi and valence band energy. Filled circle and open circle represent electrons and holes, respectively.[15].......................................6

Figure 3. Illustration of white light generation using phosphor method (blue/UV LEDs + phosphors) and using RGB method (Red+Green+Blue LEDs).[15]....6

Figure 4. Fabrication process flow of the high-*k* gated MOS capacitor with light emission application..9

Figure 5. Sequence of lithographic processing steps, illustrated for a positive resist. 12

Figure 6. Schematic diagram of the RF magnetron sputtering system.[23] 14

Figure 7. Schematic configuration of magnetron control.[24] 15

Figure 8. Schematic diagram of the furnace annealing system. 16

Figure 9.Schematic diagram of electrical characterization system setup for (a) flat Al box and (b) probe system for electrical characterization.[23].....................17

Figure 10. Diagrams of device structure of (a) Mo gated MOS capacitor and (b) Cu gated MOS capacitor...23

Figure 11. *C-V* hysteresis curves of 400 µm diameter Mo gated capacitors (a) without and (b) with the PMA treatment. Measured at 1 MHz...................26

Figure 12. *J-V* curves of 400 µm diameter Mo gated capacitors (a) without and (b) with the PMA treatment. 27

Figure 13. *C-V* hysteresis curves of 400 µm diameter Cu gated capacitors (a) without and (b) with the PMA treatment. Measured at 1 MHz...................28

Figure 14. XPS spectra of 400 µm diameter Cu gated devices (a) without and (b) with PMA treatment...29

Figure 15. Current density-voltage (*J-V*) of 400 µm diameter Cu gated capacitors (a) without and (b) with PMA treatment. 30

Figure 16. Structure of ZrHfO high-*k* MOS capacitor...33

Figure 17. (a) Cross-sectional view of a nano-resistor device, (b) equivalent circuit of a nano-resistor...35

Figure 18. *C-V* hysteresis curves of ZrHfO sample with diameter of 300 μm. 36

Figure 19. Current density vs. stress gate voltage of ZrHfO samples with PDA in (a) nitrogen, and (b) oxygen. Sample diameter: 300 μm.................................38

Figure 20. Photos of ZrHfO sample with PDA in (a) nitrogen and (b) oxygen stressed for 1200 min with sample size of 300 μm diameter......................40

Figure 21. Dot number counted from light photos of ZrHfO samples prepared with PDA in (a) nitrogen, and (b) oxygen stressed for 1200 min. 41

Figure 22. Current as a function of stress time of ZrHfO samples with PDA in (a) nitrogen and (b) oxygen. Inset: Photos at various stress time.....................41

Figure 23. (a) *I-V* curve of a 200 μm device before and after nano-resistor formation, (b) resistances of 50 μm, 100 μm, 200 μm, and 300 μm nano-resistor devices for V_g = -2 V to -5 V. All devices measured at room temperature..43

Figure 24. (a) Resistances of nano-resistor devices measured in high $|-V_g|$ range at room temperature, (b) experimentally measured and predicted resistance vs. size curves..45

Figure 25. (a) Resistance vs. V_g curves of a 200 μm device in low $|-V_g|$ range measured at room temperature, 80℃, and 120℃, (b) resistance vs. temperature curves in high $|-V_g|$ range of different sized devices. 47

Figure 26. (a) Resistances of a 100 μm device in the low $-V_g$ range after 3 hrs and 7 hrs annealing, (b) resistances in the high $-V_g$ range of different sized devices annealed for 0, 3, and 7 hrs. Annealing condition: 80% relative humidity and 80℃. 48

Figure 27. *C-V* hysteresis curves WO_x samples fabricated under various post high-k deposition annealing ambient...53

Figure 28. *J–V* curves swept from 0 V to -10 V of the WO_X LEDs with PDA in (a) nitrogen, and (b) oxygen. Sample diameter: 300 μm.................................55

Figure 29. High-magnification photos of the WO_x samples prepared with PDA in (a) nitrogen and (b) oxygen atmosphere. Stress voltage: -12 V. 56

Figure 30. Current as a function of stress time of WO_x samples with PDA in (a) nitrogen and (b) oxygen. Inset: Photos at various stress time. 57

Figure 31. Schematic structure of WO_x embedded ZrHfO MOS capacitors. 60

Figure 32. *C-V* hysteresis curves of the samples with V_g swept from -3 V to +3 V to -3 V at 1 MHz. Dashed line: sample prepared with PDA in nitrogen atmosphere. Solid line: sample prepared with PDA in oxygen atmosphere. 62

Figure 33. *J-V c*urves of the WO_x embedded ZrHfO MOS capacitor prepared with PDA in (a) nitrogen and (b) oxygen ambient. 64

Figure 34. High-magnification photos of the samples prepared with PDA in (a) nitrogen and (b) oxygen atmosphere. 65

Figure 35. Current as a function of stress time of samples fabricated with PDA in (a) nitrogen and (b) oxygen. Inset: Photos at various stress time. 66

Figure 36. Dot number counted from light photos of samples prepared with PDA in oxygen at various stressed time. 67

Figure 37. Emission spectra of WO_x embedded ZrHfO samples. Dashed line: sample with PDA in nitrogen. Solid line: sample with PDA in oxygen. 69

Figure 38. *C-V* hysteresis curves of ZrHfO, and WO_x embedded ZrHfO samples with diameter of 300 μm. 73

Figure 39. *J-V* curves of (a) ZrHfO, (b) WO_x and (c) WO_x embedded ZrHfO samples of 300 μm diameter. (d) Schottky emission and (e) Poole-Frenkel fitting curves of ZrHfO, WO_x, WO_x embedded ZrHfO SSI-LEDs. 76

Figure 40. Photos of (a) ZrHfO, (b) WO_x and (c) WO_x embedded ZrHfO SSI-LEDs. All samples: 300 μm diameter. 80

Figure 41. Current as a function of stress time of (a) ZrHfO, (b) WO_x embedded ZrHfO, and (c) WO_x samples. Inset: Photos at various stress time. 80

Figure 42. Distributions of light dot diameters of (a) ZrHfO, (b) WO_x, and (c) WO_x embedded ZrHfO samples formed after stressed for various time. 82

Figure 43. Total number of bright dots distributed in ZrHfO, WO_x, WO_x embedded ZrHfO, and ultra-thin WO_x[82] based SSI-LEDs. 83

Figure 44. Light emission spectra of ZrHfO, WO_x, and WO_x embedded ZrHfO SSI-LEDs. 84

Figure 45. Color coordinates of ZrHfO, WO_x, and WO_x embedded ZrHfO SSI-LEDs in the CIE chromaticity chart. Color coordinate of the incandescent bulb is included for reference. 85

LIST OF TABLES

Page

Table 1. Coefficients calculated from *C-V* hysteresis curves of ZrHfO MOS capacitors prepared with PDA under N_2, and O_2. 37

Table 2. The breakdown voltage, leakage current density at -1V, and resistance of ZrHfO samples prepared with various atmosphere extracted from *J-V* measurement..38

Table 3. Coefficients calculated from *C-V* hysteresis curves of ZrHfO MOS capacitors prepared with PDA under N_2, and O_2. 53

Table 4. The breakdown voltage, leakage current density at -1V, and resistance of WO_x samples prepared with various atmosphere extracted from *J-V* measurement. 55

Table 5. Coefficients calculated from *C-V* hysteresis curves of WO_x embedded ZrHfO MOS capacitors prepared with PDA under N_2, and O_2 atmosphere. 62

Table 6. The coefficients extracted from *J-V c*urves of the samples prepared in various PDA ambient. 64

Table 7. Coefficients calculated from *C-V* hysteresis curves of ZrHfO, WO_x, WO_x embedded ZrHfO MOS capacitors...74

Table 8. Coefficients calculated from *J-V* curves of ZrHfO, WO_x, WO_x embedded ZrHfO capacitors..79

Table 9. The CIE color coordinates, CCT, and CRI of the ZrHfO, WO_x, and WO_x embedded ZrHfO SSI-LEDs. 85

CHAPTER I INTRODUCTION

1.1 High-*K* Gate Dielectrics

The thermally grown SiO_2 as a gate dielectric provides several advantages in complementary metal-oxide-semiconductor (CMOS) processing such as the thermodynamically and electrically stable, high-quality Si-SiO_2 interface and also good electrical isolation ability. These properties make the material system sustain the microelectronics industry ever since. Since the devices shrunk in size to achieve industry demand for a higher density of transistors on single chip, it leads to the decrease of channel length and gate dielectric thickness. The decrease of the thickness increases the gate capacitance as well as drive current, and therefore raising device performance. The drive current (*I*) of the nMOSFET can be described as the following equation:[1]

$$I = \frac{W}{L}\mu C_{ox}(V_{GS} - V_T)V_{DS} \quad [1]$$

, where L is the channel length, W is the width of the transistor channel, μ is the channel carrier mobility, C_{ox} is the capacitance of the gate dielectric in accumulation stage, V_{GS} is the gate to source voltage, V_T is the threshold voltage, and V_{DS} is the drain to source voltage. However, when the thickness becomes lower than 2 nm, because of direct tunneling of electrons, the gate leakage current will exceed 1A/cm^2 at 1V.[2] The drastically increase of the current results in high power dissipation and lower device reliability. For a metal-oxide semiconductor field-effect transistor (MOSFET) device, the source-drain current is related to the gate capacitance,

$$C = \epsilon_0 \kappa A/t \quad [2]$$

Where ϵ_0 is the permittivity of free space, κ is the relative permittivity, A is the area and t is the SiO_2 thickness. The tunneling effect states that the tunneling current reduces exponentially with the increasing distance; therefore, substituting the silicon dioxide gate dielectric with a high-k material will keep the same capacitance, but the lower current leakage.[3]

The good alternative gate dielectric candidates require several properties as follows: (a) permittivity, band gap, and band alignment to silicon, (b) thermodynamically stable with silicon layer due to their direct contact (c) electrically stable of bulk to avoid forming active defects (d) good interface quality of the interface with silicon, (e) compatibility with materials used in devices, (f) process compatibility to endure high processing temperature. These criteria show a considerable challenge for materials design and selection.[2]

1.2 Zirconium-Doped Hafnium Oxide

Hafnium oxide, whose static dielectric constant is 25 and band gap is 5.8 eV[3], is presently the preferred high-k oxide over zirconium oxide which has the same static dielectric constant as hafnium oxide but less thermal stability[4], i.e., ZrO_2 slightly reacts with Si and forming silicide.[5] Due to its exceptional high bulk modulus, high melting point, and high chemical stability and its high neutron absorption cross section, HfO_2 is important for the technology industry. For the electrical properties of HfO_2, frequency dependency of capacitance, leakage current, and life-time are studied. The leakage current density of

HfO2 thin films are four order of magnitude smaller than that of SiO_2 for the same equivalent oxide thickness (EOT).[5] Although hafnium oxide has the promising properties, the low crystallization temperature (<500˚C)[6] makes it easy to crystallize during the IC process. The crystalline in HfO2 films facilitates charge transfer through the oxide layer due to the existence of grain boundary, and therefore increases undesirable leakage current. It was suggested that the zirconium-doped hafnium oxide showed a much higher amorphous-to-polycrystalline transition temperature (>900˚C), a lower D_{it}, as well as a smaller EOT.[7-8] In this thesis, instead of hafnium oxide, the zirconium-dope hafnium oxide is utilized to serve as high-*k* dielectric layer in MOS capacitor.

1.3Light Emitting Device

1.3.1 General Background of the Light Emitting Device (LED)

Incandescent light bulb radiates a non-discrete spectrum due to thermally excited atoms by electrical resistive heating. Since there is a near-continuum of electron energy levels, the continuous spectrum in visible wavelength can be obtained from a solid heated red hot to over 850K. Tungsten's high melting point (3680K) and low vaporization pressure makes it used as common filament material. However, efficacy of incandescent lamp is low – less than 10% of radiated energy converted into the visible wavelength, while most remaining energy radiated as heat dissipation as shown in Figure 1.[9]

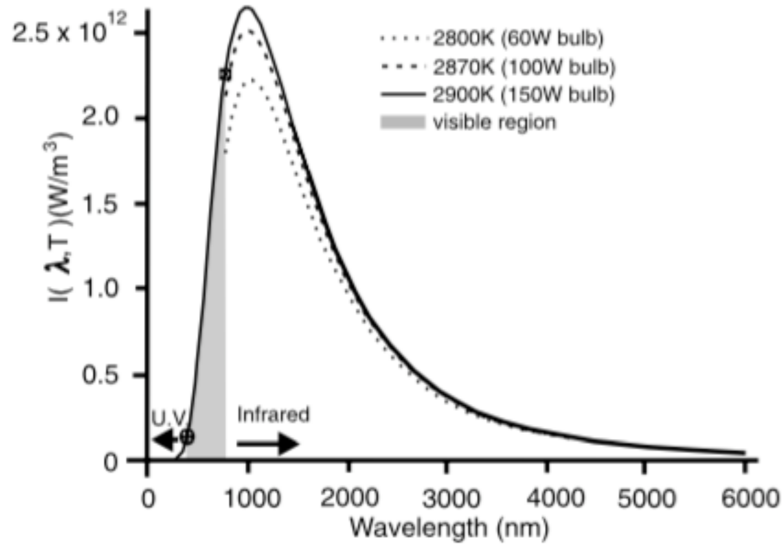


Figure 1. Blackbody radiation curves for incandescent lamp operating at different power ratings. Shaded area shows visible light wavelength region. [9](Reprinted with permission from Ref. 5. Copyright 1999 by The physics teacher.)

Fluorescent lamp was invented and offered a longer life and lower power consumption than incandescent source. Visible light comes out when the radiated ultraviolet light from excited electrons bound to mercury atoms strikes the fluorescent coating. It has higher luminous efficacy of 57.14 lm/W than incandescent bulb of 14.3 lm/W. Although the longer life and lower power consumption make fluorescent bulb become mainstream lighting method at that time, the poor color rendering index (CRI) and disposal related issues arising from toxic mercury vapor inhibit its marketability.[10-11]

To further reduce the energy consumption, light–emitting diode (LED) rises to the occasion. It is a p-n junction diode that emits the photons from recombination of electrons and holes in the forward biased as shown in Figure 2. It was suggested that the emitted

photon energy is approximately equal to the bandgap energy[12], the relationship between photon energy and emitted light can be expressed as following equation:

$$E_g = h\upsilon = \frac{hc}{\lambda} \quad [3]$$

, where E_g is band gap energy, h is Planck's constant 6.626×10^{-34} J/s, υ is photon frequency, c is light speed of 3×10^{8} m/s, λ is light wavelength. According to this equation, LED can only emit the light within a narrow wavelength range, and for that reason, to obtain white light emission, the multiple semiconductors combination or a layer of light-emitting phosphor on the semiconductor device are adapted, as shown in Figure 3.[13] The first commercially used white LED was produced by phosphor method: the blue light (460nm) emitting InGaN chip was coated with a cerium-doped yttrium aluminum garnet (YAG) phosphor layer in order to converted parts of the blue light into yellow.[14] Through the combination of the yellow with remaining blue light passing through the sufficiently thin phosphor layer, a cool white light is obtained. The RGB method is the mixing of red, green and blue LEDs to produce white light without applying phosphors. However, due to the narrower emission peaks of LEDs than those of most phosphors, the RGB-method produced white LED results in the poor color rendering.[15] Although the cold white LED is fine for many applications such as displays, lighting in cars, a warmer white light is more desirable for home lighting.

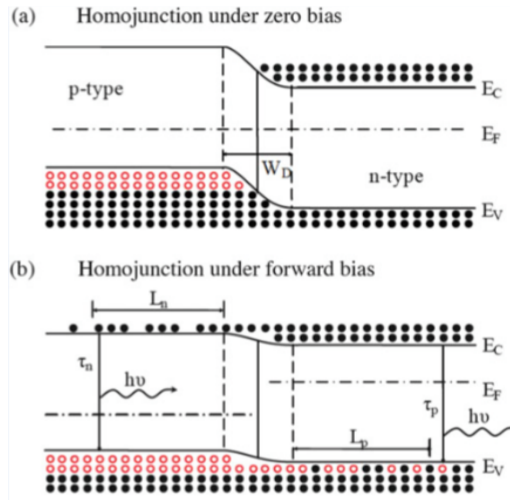


Figure 2. A p-n junction under (a) zero and (b) forward bias. E_C, E_f and E_v are the conduction band, Fermi and valence band energy. Filled circle and open circle represent electrons and holes, respectively.[15](Reprinted with Creative Commons Attribution 4.0 International Public License from Ref. 15. Copyright 2016 Springer.)

Figure 3. Illustration of white light generation using phosphor method (blue/UV LEDs + phosphors) and using RGB method (Red+Green+Blue LEDs).[15](Reprinted with Creative Commons Attribution 4.0 International Public License from Ref. 15. Copyright 2016 Springer.)

1.3.2 Solid State Incandescent LED (SSI-LED)

A solid state incandescent light emission device was reported by Kuo's group.[16-20] This kind of device can emit the broad band light from the high-*k* stack as a result of the

hard dielectric breakdown of a MOS capacitor fabricated on p-type silicon substrate. With the application of a negative gate voltage, holes are injected into dielectric layer, which generates a lot of defects in both the bulk and interface layers.[17, 21] When these defects are connected, the hard breakdown phenomenon takes place and nano-resistors are formed. Before the breakdown, the current flows through the high-*k* stack following the Schottky emission (at low voltage) and Poole-Frenkel (at high voltage) mechanisms.[22] After the dielectric breakdown, the current flows through nano-resistors following Ohm's law, i.e., showing the linear current vs. voltage (*I-V)* relationship. When a large current is passed through these nanoresistors, the broad warm white light is emitted due to the thermal excitation mechanism. Therefore, this kind of device was named the solid state incandescent light emitting device (SSI-LED)[16] On the other hand, in the low voltage operation region, the device shows the diode-like current-voltage (*I-V*) behavior because the current only flows in one direction to the gate electrode but not the other direction.[22] For SSI-LED, the fabrication procedure and device structure influence the conductive path formation as well as characteristics of the emitted light. In this thesis, the impacts of post-deposition annealing condition, operating environment and high-*k* material selection on the electrical and optical properties of SSI-LED have been investigated.

CHAPTER II

EXPERIMENTAL

2.1 Introduction

This chapter elaborates on the tools, equipment and other inputs used in the experimentation process. First, the overall fabrication process of high-*k* gate dielectric MOS capacitor will be introduced with a flow chart, including the parameters and coefficients of the materials. Second, the fundamental background of RF magnetron sputtering, annealing furnace, and RIE will be introduced. Third, the characterizations in regards to material, electrical and optical properties, such as XPS, *C-V*, *J-V*, and light emission spectrum will be involved.

2.2 Process Flow of Solid State Incandescent Light Emission Device

Figure 4 shows the flow chart of fabricating process of high-*k* based MOS capacitor or SSI-LED. In this thesis, all the memory devices will be fabricated on the <100> p-type Si substrate (resistivity 11-20 Ω·cm, doping concentration at 10^{15} cm^{-3}, supplied from MEMC) with the size of 1 inch×1 inch.

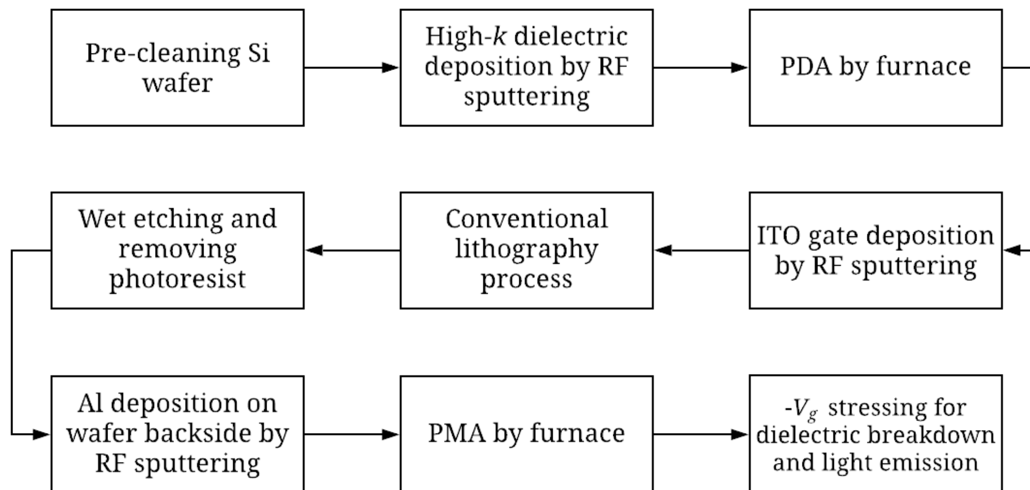


Figure 4. Fabrication process flow of the high-*k* gated MOS capacitor with light emission application.

The native oxide forms on the surface of a silicon wafer when the wafer is exposed to air. The silicon dioxide can be removed by a dipping into a dilute hydrofluoric acid (DHF, 2%) solution for 5 min. Since oxide is hydrophilic and pure silicon is hydrophobic, a non-wetting surface indicates clean of oxides. After checking for hydrophobicity of the Si surface, the sample was rinsed in running deionized water (DI, resistivity > 18 MΩ·cm) for 5 min. Then, blow drying with nitrogen gun, and the sample was directly placed into the load-lock system which is connected to the main chamber of the sputtering system.

In this thesis, the thin film stack was deposited by the RF magnetron sputtering system which has the power supply with a high voltage RF source often fixed at 13.56 MHz and the baseline condition of 6.4×10^{-6} Torr. Three types of gate dielectrics were utilized in the device, including ZrHfO, WO_x, and ZrHfO/WO_x multilayers. The ZrHfO film was

sputtered by a Zr/Hf (12/88 wt%) composite target in Ar/O_2 (1:1) at 60W and 5 mTorr for 12 min. The W (99.99%) target was sputtered in Ar/O_2 (1:1) at 60W and 5mTorr for 12 min to deposit the WO_x gate dielectric on *p*-Si wafer. For the ZrHfO/WO_x multilayer structure, the sputtering sequence was 3 min of ZrHfO and 2 min of WO_x deposited alternatively until the total deposition time for 12 min ZrHfO and 6 min WO_x were achieved. Involving the insulating targets in the fabrication process, the RF power supply was a better choice over the DC one, which can avoid charge-up effects and reduces arcing. Also, a pre-sputtering step was required in pure Ar ambient condition for 10-15 min to remove the oxide on the target surface before executing the deposition.

Next in line after the deposition is post deposition annealing (PDA) step using furnace tube for the purpose of densifying the as-deposited film, and repair damage induced from high energy ion bombardment to improve the electrical properties. Depending on the process, N_2 (99.999 %) or O_2 (99.993 %) are introduced into the furnace tube with flow rate of 600-1000 sccm at 900˚C for 3-5 min. Then, the gate electrode, such as indium tin oxide (ITO), copper and molybdenum, layer was deposited on the high-*k* gate dielectric stack. For the study of metal gate effect on MOS capacitor, the Mo (99.99 %) and Cu (99.99 %) electrode film was sputter deposited on top of the ZrHFO at 10mTorr and 80W. For the study of SSI-LED, the ITO transparent electrode gate was sputtered on top of various high-*k* stack with the resistivity around 650-700 μΩ·cm.

After depositing the gate electrode, the conventional lithography process was conducted to pattern the gate electrode layer into the various sizes of electrode. The 1.4-1.5 μm thick positive photoresist (AZ Electronics, AZ 5214-E) was coated on the ITO

surface by the spin coater (Chemat Technology, KW-4A) rotating at speed up to 4000 rpm. The sample was soft baked on hot plate at low temperature (90˚C) in air, which is aimed at enhancing adhesion, volatilization of solvents and solidification of photoresist. The low temperature avoids the degradation of the resist components. Then, the sample was directly covered with a patterned quartz mask and exposed to the UV light power density at 10 mW/cm^2 in the contact mode for 7 s in the aligner equipment, Quintel Q4000. After patterning, the sample was dipped in the developer (AZ Electronics, MIF 300) to wash away the exposed region, and treated with hard bake step in a 125˚C over for 5 min, which is aimed at strengthening of resist structure prior to etching. The various solutions were prepared for wet etching depending on materials. For ITO gate, the etching solution is aqua regia (HNO_3: HCl = 1:3); for Mo gate, the etching solution consisted of H_3PO_4: HNO_3 : CH_3COOH : H_2O (16 : 1 : 1 : 2). As for copper gate, it was etched with a room-temperature plasma-based process that is composed of the HCl plasma chlorination of the Cu film followed by the HCl solution dipping. The sample was dipped into stripper to remove the remaining photoresist and flushed with DI water to keep the surface clean.

After patterning and wet etching, the backside of Si wafer was scratched by the diamond pen to roughly remove the native oxide. A 150 nm thick Al layer was sputter deposited from the Al (99.999 %) target at 80W in pure Ar ambient condition on the backside of the Si wafer forming the ohmic contact. The post metal deposition (PMA) step are applied to the sample at 400˚C in the forming gas H_2/N_2 (1:9) atmosphere in order to passivate the oxygen deficiencies and dangling bonds in the device. Figure 5 shows the diagram of the general sequence of processing steps for typical photolithography process.

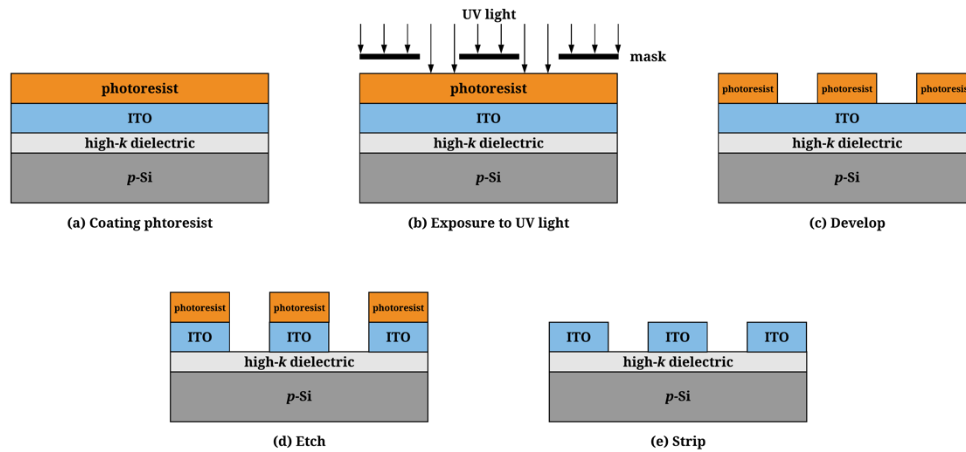


Figure 5. Sequence of lithographic processing steps, illustrated for a positive resist.

2.3 Plasma Deposition and Annealing

In this chapter, the fundamental background of RF magnetron sputtering system used for thin film deposition and furnace annealing will be introduced.

2.3.1 RF Magnetron Sputtering System

The RF (13.56 MHz) magnetron sputtering machine is utilized to deposit thin films, such as the high-*k* gate dielectric, gate electrode, and backside electrode of devices, in this thesis. The mechanical system is illustrated in Figure 6. The sputtering system is consisted of two chambers, which is load-lock and main chambers, with dual target sources, e.g., RF source for coating non-metallic material, and DC source for coating metallic film. Since the insulating dielectric materials are used in the research, the RF source is selected to prevent charge-up effect. The RF power supply is supplied with an auto-matching network for the purpose of minimizing the reflected power. Also, the minimum reflected

power can be achieved by manually adjusting the the capacitance of the impedance-matching network of the RF sputter system. The matching box connecting RF generator and guns is consisted of two adjustable capacitors, i.e., load capacitor (Cap. 1, 1000 pf in maximum) and tune capacitor (Cap. 2, 500 pf in maximum), and one fixed inductor. In the chamber, the substrate holder is electrically insolated from chamber and rotated at the speed of 10 rpm to provide better coating uniformity. The sputtering system is operated with cycling DI water chiller system (Neslab, CFT-33).

The two chambers are made of the stainless steel, and vacuum sealed with the fluoroelastomers (Viton) O-rings and Cu gaskets. When samples are located in the load-lock chamber with smaller volume of 15 L, the air pressure is pumped down to $\sim 10^{-5}$ Torr by the mechanical pump (Edwards, E2M8) and turbo pump (Pfeiffer, TPU 170) within 20 min. The aim is to allow samples to be transferred into the process chamber without venting the process chamber to atmosphere to reduce the potential for contamination in the main chamber. The samples are able to transfer from the load-lock chamber to process chamber when the gate valve is opened. After that, the process chamber is pumped down to the baseline condition 6.4×10^{-6} Torr by the mechanical pump (Alcatel, 2063 CP1) and turbo pump (Leybold, Turbovac 360).

There are three sputter 2" flex magnetron guns, and each of them is equipped with a shutter to mechanically start/shut off the deposition process. Two precision mass flow controllers (MFC) are installed to allow inlet of three types of gasses, i.e., one is for Ar (99.999%), and N_2 (99.999%) shares the same MFC with O_2 (99.993%). Therefore, depending on the

process, the system can provide three kinds of atmosphere which is pure Ar, mixed Ar/O_2, and mixed Ar/N_2.

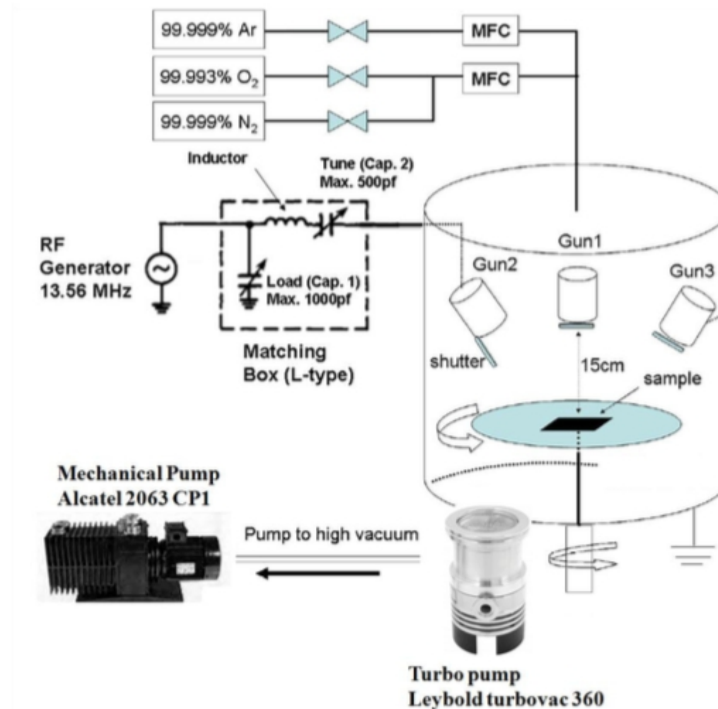


Figure 6. Schematic diagram of the RF magnetron sputtering system.[23](Reprinted with permission from Ref. 23 Copyright 2014 TAMU.)

By adding a closed magnetic field parallel to the target surface, the secondary electrons are confined in near the surface of the target. The ionization efficiency is then increased with the increase of plasma density, and leading to the high-rate sputtering. Figure 7 shows the schematic diagram of magnetron sputtering. The orthogonal electromagnetic field (E×B) which is generated from magnetic field provided by strong magnet underneath the

target and electric field provided from power source bound the movement path of electrons. Also, the electron movement becomes spiral around the target surface, and the probability of Ar gas colliding with electrons increases. Then, the target material is stroked by the generated ions and deposit on the substrate. Using the RF magnetron sputtering, it not only increases the deposition rate, but also prevents the damage caused by the high-energy electrons.

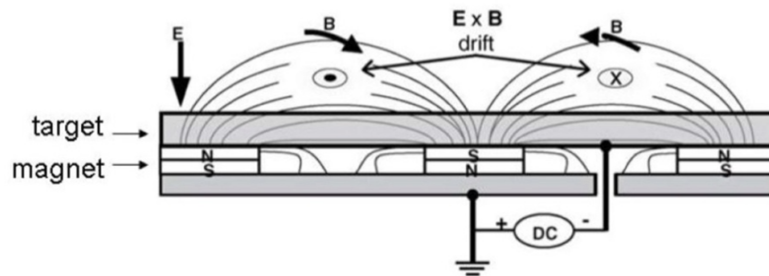


Figure 7. Schematic configuration of magnetron control.[24] (Reprinted with permission from Ref. 24. Copyright 2010 Elsevier.)

2.3.2 Furnace Annealing

Figure 8 shows the schematic diagram of the furnace annealing system. Three kinds of gases were used in the furnace annealing system, i.e., N_2 (99.999 %), O_2(99.9993 %), and forming gas (H_2/N_2 : 1/9). A PDA process is conducted in a tube in order to densify deposited films, change states of grown films, repair damage, and elliminate the defects. The sample is put into the quartz tube after high-*k* film deposition, and the tube is sealed

by flange. After that, the tube is pumped down, the gas is purged into the tube at fixed flow rate depending on the process, and set the desired temperature. By controlling the annealing temperature in various atmosphere, the electrical properties of the sample can be affected.

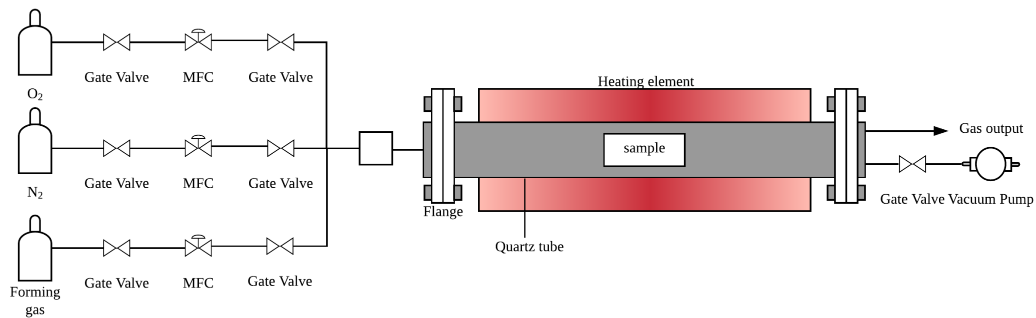


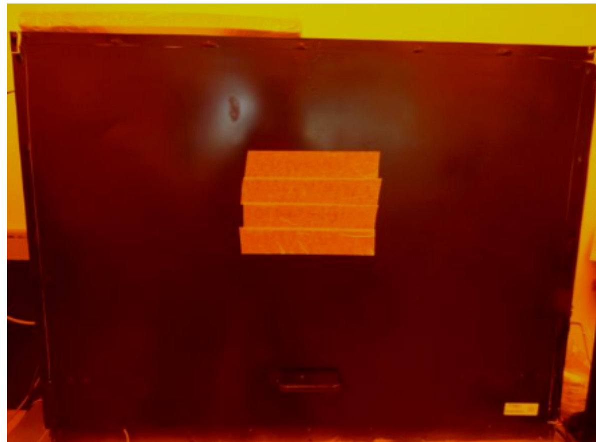
Figure 8. Schematic diagram of the furnace annealing system.

2.4 Electrical Characterization

2.4.1 Electrical Characterization System Setup

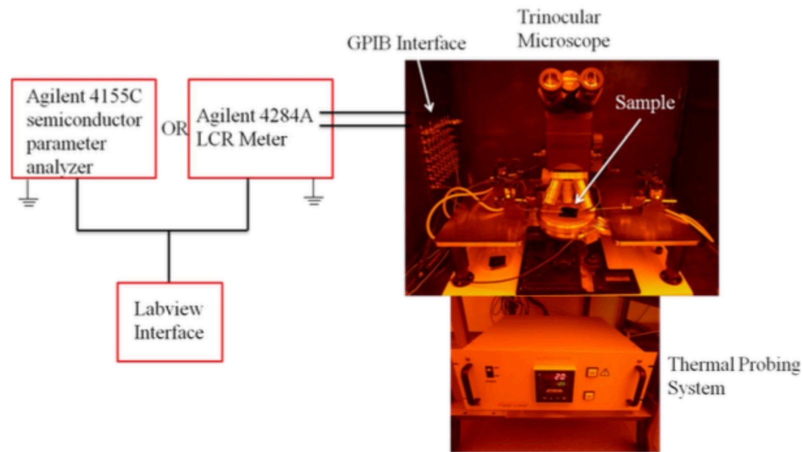
To investigate the electrical properties, i.e. gate dielectric performance and breakdown phemonon, of the high-*k* MOS capacitors and SSI-LED, several measurements such as frequency dependent capacitance-voltage (*C-V*), current density-voltage (*J-V*) were implemented. The outside grounded flat Al black box as shown in Figure 9(a) was utilized to minimize the disturbance created from surrounding environment such as light, noise,

heat, and vibration, when the experiments were conducted. The electrical measurements were carried out on the probe station (Signatone, S-1160) placed in the black box as shown in Figure 9(b). The gold alloy chunck was connected to a mechanical pump to create a vacuum which can prevent the sample from shifting. The probe used in station is made of tungsten with a diameter of 1μm. In addition, for temperature dependent measurements, a thermal probing system (Signatone, S-1060R) with maximum temperature up to 600˚C was connected to the chunck, and it can be cooled down by water cooling system. The electrical tests were controlled by connecting the measurement system to the National Instruments Labview 7 program through the GPIB interface.



(a)

Figure 9. Schematic diagram of electrical characterization system setup for (a) flat Al box and (b) probe system for electrical characterization.[23](Reprinted with permission from Ref. 23 Copyright 2014 TAMU.)



(b)

Figure 9. Continued.

2.4.2 C-V Curve Measurement

During the processing steps, defects or impurities generated in the gate oxide can trap charges and therefore affect electrical properties of MOS capcitors. The change of parameters, such as the metal-silicon workfunction difference, interface traps, mobile ions in the oxide, and fixed oxide charge can be obtained through analyzing *C-V* hysteresis curve deviation from ideal case.

The origin of interface trapped charge (Q_{it}) is lattice mismatch at the Si/dielectric interface, dangling bonds, existence of foreign impruity atoms at the silicon interface, and defects created by radiation. The defects results that the energy states located at interface can capture or emit charges, and degrades effect on device behavior. The increase of Q_{it} value indicates the reduction of carrier mobility at interface. The oxide trapped charge (Q_{ot}) is related to defects generated from ionizing radiation, and distributes throughout the gate

oxide film. The positive value of Q_{ot} shows the existence of hole-trapping centers in oxide layer, and the negative value indicates the electron-trapping sites in the oxide layer. Flat band voltage (V_{FB}) is an external voltage applied to compensate band bending effect due to the voltage difference between the metal gate and silicon surface. The zero surface potential without band bending phenomenon is called the flat band condition, which is often used as a reference state. The capacitance is calculated from the ratio of the variation in charge to the corresponding variation in the small-signal applied voltage, which can be expressed as following:

$$C = \frac{dQ}{dV} \text{ (F/cm}^2\text{)} \quad [4]$$

In this thesis, the NCSU CVC program by Hauser et al[25] is utilized to perform *C-V* measurement. The DC bias voltage is applied across the device while the measurement is carried out with a high frequency small sinusoidal AC signal of 0.25V. Commonly, the AC frequency of 1 MHzis used for measurement in the thesis. The DC bias sweep in the desired voltage range drives the device from, in sequence, accumulation region, depletion region, and inversion region. By analyzing the *C-V* curve, parameters, such as oxide thickness, V_{FB}, Q_{it}, and Q_{ot} can be derived from these three regions.

2.4.3 J-V Curve Measurement

The *J-V* characteristic curve performed in the thesis can be used to investigate electrical properties such as current transport mechanism, breakdown phenomenon, leakage current density, resistance calculation and charge trapping/detrapping phenomena in the devices. In each measurement, the DC bias sweep starts from zero to desired voltage. The *J-V* measurement can be realized through applying a DC bias across probe tip and the gold

alloy chunk, and receiving the current signals from the same probe tip. The voltage profile of the DC bias in this dissertation is in the ramp mode. The DC bias ramping with low speed of 0.01 V/s is adopted to minimize the displace current, which is able to make measured current more precise.

2.5 Optical Properties Characterization

The light emission spectrum measurement is carried out on the probe station in the Al black box as introduced in the section 2.4.1. The SSI-LED sample is placed on the chunk with a vacuum, and is applied with DC gate voltage from power supply (Agilent E3645A). The optical emission spectrometer (OES, StellarNet BLK-C-SR-TEC) is equipped with a 1 meter fiber optic cables and a receptor in silica core diameter of 1000 μm. Also, to prevent the machine from overheated, the thermo electric cooling (TEC) working based on the peltier effect is added to the system. The receptor is placed above of the sample surface, and the surface of it is parrallel to the ITO surface with the distance of 0.2 cm. To maximize photon collection, the integration time is set to 65 S and the average sampling is set at 1 in scope mode.

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CHAPTER III

GATE ELECTRODE MATERIAL EFFECT ON CHARACTERISTICS OF ZIRCONIUM-DOPED HAFNIUM OXIDE MOS CAPCITOR

3.1 Introduction

The high-*k* dielectric has been used to replace SiO_2 as the gate dielectric material in the scaling down of the metal-oxide-semiconductor (MOS) device. While the leakage current of the MOSFET with an ultrathin thermal SiO_2 gate dielectric, e.g., < 1.0 nm[26], has a very large leakage current density (*J*) of greater than 1A/cm^2, the device made of a proper high-*k* gate dielectric of the same equivalent oxide thickness (EOT) can have a leakage current density several orders of magnitude lower.[27-28] This is due to the high-*k* film's large band gap energy and large band offset with Si, which generates a potential barrier over 1 eV.[26, 29-30] However, one of the reliability concerns for the Hf-based dielectric is the low crystallization temperature, e.g., < 600˚C.[31] It was reported that the Zr-doped HfO_2 (ZrHfO) thin film has many advantages over the undoped HfO_2 thin film, such as higher crystallization temperature, higher permittivity, lower interface thickness, and lower interface density of states.[32-34] Previously, polycrystalline Si (poly-Si) was used as the gate electrode in MOSFETs because it can stand over 800˚C, and is compatible with SiO_2. However, in the case of the high-*k* gate dielectric material, it has poor bonding with the poly-Si gate electrode and forms an interface with high defects, which trap charges and reduces free charge carriers.[35] By replacing poly-Si with a metal gate electrode, a high

free carrier density, e.g., $1\times10^{20}/cm^3$, can be achieved and the phonon scattering effect can be decreased, which reduces the mobility degradation.[35]

MOS capacitors with the sputter deposited ultra-thin ZrHfO gate dielectric layer, i.e. EOT < 1 nm, and a metal gate electrode have been successfully demonstrated previously [28]. The capacitor's electrical properties, such as charge trapping capacity, interface state density, leakage current, and breakdown voltage, can be improved with the addition of other elements, such as molybdenum (Mo) or ruthenium (Ru).[36] The choice of the metal gate material can affect the threshold voltage of the device because of the work function effect.[37] Mo has been proved to be a promising alternative gate electrode material to SiO_2 in the formation of a high quality interface.[38] On the other hand, in addition to the high conductivity and high electromigration resistivity[39], copper (Cu) has a similar work function as that of Mo[40], which makes it a possible gate electrode material. In this paper, two kinds of metal gates, i.e., Cu and Mo, are separately deposited on top of the ZrHfO gate dielectric film to study the MOS capacitor properties.

3.2 Experimental

MOS capacitors were fabricated on dilute hydrofluoric acid cleaned *p*-type (10^{15} cm^{-3}) Si (100) wafers. The ZrHfO film was sputter deposited from a Zr/Hf (12/88 wt.%) target in Ar/O_2 (1:1) at 10 mTorr and 80 W for 12 min. The sample was subsequently treated with a post deposition annealing (PDA) step at 800°C under N_2 atmosphere for 5 min. Then, a 200 nm thick Cu or Mo electrode film was sputter deposited on top of the ZrHfO film at

10 mTorr and 80 W, i.e., 20 min for the former and 120 min for the latter. They were etched into round gate electrodes of 200 µm, 300 µm and 400 µm diameters defined with a lithography step. The Mo gate was wet etched with the ($H_3PO_4/HNO_3/CH_3COOH/H_2O$ 80:5:5:10 vol.) solution. The Cu gate capacitor was etched with a room-temperature plasma-based process that is composed of the HCl plasma chlorination of the Cu film followed by the HCl solution dipping.[41] After the photoresist was stripped, the sample was treated with a post metal annealing (PMA) step at 250°C under N_2 atmosphere for 10 min. Samples without the PMA treatment, i.e., controlled samples, were also prepared and characterized for comparison. The finished samples are shown in Figure 10.

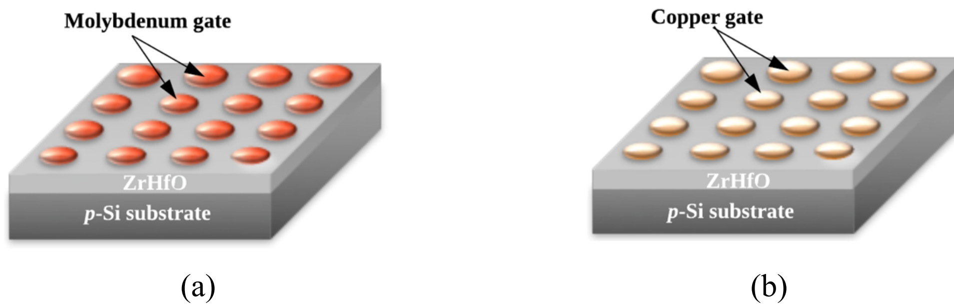


Figure 10. Diagrams of device structure of (a) Mo gated MOS capacitor and (b) Cu gated MOS capacitor.

The capacitance-voltage (*C-V*) curve of the capacitor was measured with the Agilent 4284 LCR meter. The EOT was calculated from the equation of

$$EOT = \frac{\varepsilon_0 \varepsilon_i A}{C_{ox}} \quad [5]$$

where ε_i is the dielectric constant of SiO_2 (~3.9), ε_0 is the permittivity of the free space (8.85×10^{-12} F/m), A is the area of the gate electrode, and C_{ox} is the oxide capacitance extracted from the *C-V* curves in the accumulation region. Electrical parameters, such as the flat band voltage (V_{FB}), interface density of states (D_{it}), and oxide trapping density (Q_{ot}) were extracted from the *C-V* curve using the NCSU CVC program.[42] The Q_{ot} was calculated by the following equation:[43]

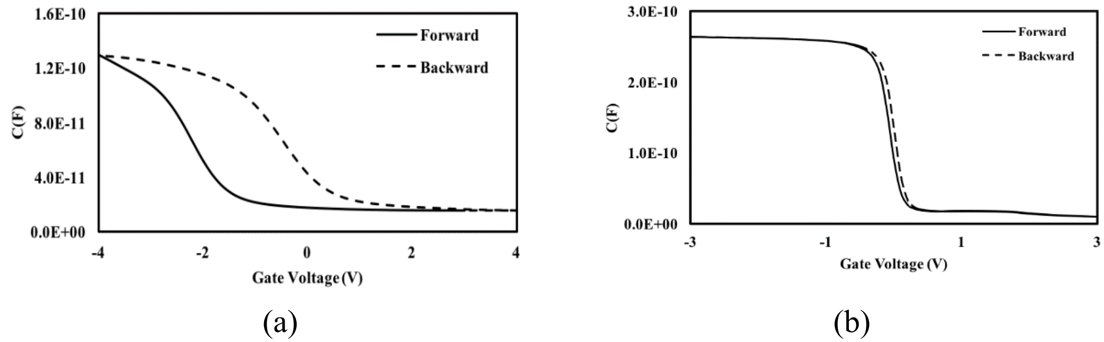
$$Q_{ot} = \frac{(C_{acc}\times\Delta V_{FB})}{q} \qquad [6]$$

where q is the electronic charge (1.6×10^{-19} C), C_{acc} is the accumulation capacitance/area, ΔV_{FB} is the magnitude of the flat band voltage shift. The elemental composition and chemical states of the gate electrode/high-k interface was characterized with the X-ray photoelectron spectroscopy (XPS) after stripping the gate electrode from the MOS capacitor.

3.3 Electrical Properties of Molybdenum Gated MOS Capacitors

Figure 11 shows the *C-V* hysteresis curves of Mo gated capacitors (a) without and (b) with the PMA step. The samples were measured with the gate voltage (V_g) swept from -3 V to 3 V (forward) and then back to -3 V (backward). All curves show the counterclockwise hysteresis phenomenon. The sample without the PMA treatment shows a large flat-band voltage shift (ΔV_{FB}) of 1.4881 V while the annealed sample shows a much smaller ΔV_{FB} of 0.083 V. The V_{FB} of the forward *C-V* curve of the sample without the PMA was -2.052 V. It changed to -0.056 V when the device experienced the PMA treatment. Therefore, the

low temperature PMA step reduced the hole trapping capability of the dielectric layer. In addition, the EOTs of the samples with and without PMA treatment are 11.2 nm and 20.9 nm, respectively. The Q_{ot}, which was calculated from the metal-semiconductor work function and flat band voltage of the C-V curve, decreased with the application of the PMA treatment from 9.61×10^{11} to 1.09×10^{11} cm^{-2}. The PMA step lowered the charge trapping density of the capacitor. The large oxide trapping density of the capacitor was probably from the long sputter deposition time of the Mo gate electrode. It was suggested that the increase of the sputtering voltage or sputtering time decreased the E_{00} value that is an important tunneling parameter in the metal-silicon junction since the kT/E_{00} value represents the relative importance of thermionic emission and tunneling.[44] It indicates the increase of the number of charge trapping centers at the interface. The surface of the high-k layer can be damaged by hot electrons during the long Mo sputtering time, i.e. 120 min.[45] Therefore, a large number of hole-like defects were generated in the high-k film or at the high-k/Si interface. In addition, it was reported that the Mo gate could react with high-k film to form new bonds that reduced the work function.[46] The barrier height between the gate electrode and the gate dielectric is critically dependent on the work function or the Fermi level of the gate metal. It affects the tunneling effect between the gate electrode and oxide traps in high-k layer.[47] The trapped electrons are more likely to stay in place and compensate the positive trapped charges when the level lies below the Fermi level of the metal. As a result, the 250˚C annealing step is effective in reducing the charge trapping density.



(a) (b)

Figure 11. *C-V* hysteresis curves of 400 μm diameter Mo gated capacitors (a) without and (b) with the PMA treatment. Measured at 1 MHz.

The PMA treatment also affects the leakage current of the device. Figure 12 shows *J-V* curves of Mo gated capacitors (a) without and (b) with the PMA step. For each device, the 1st measurement caused the hard breakdown of the dielectric film, which formed nano-resistors.[22, 48] The 2nd measurement curve confirmed the permanent formation of these conductive paths, i.e., the leakage current was much larger than that of the 1st measurement curve. In the 1st curve, as a negative gate voltage (V_g) is applied, the holes were injected from the *p*-Si substrate to the dielectric layer to generate defects. The leakage current was very low at the beginning. When the magnitude of the V_g was increased, the leakage current increased until reaching the voltage (V_{BD}) where it jumped by several orders of magnitude abruptly. The dielectric film was broken due to the connection of defects.[36, 49] The magnitude of V_{BD} of the device without the PMA was larger than that with the PMA, i.e., -13.6 V vs. -5.65 V. Also, the leakage current of the former was lower than that of the latter. These results are consistent with the EOT numbers.

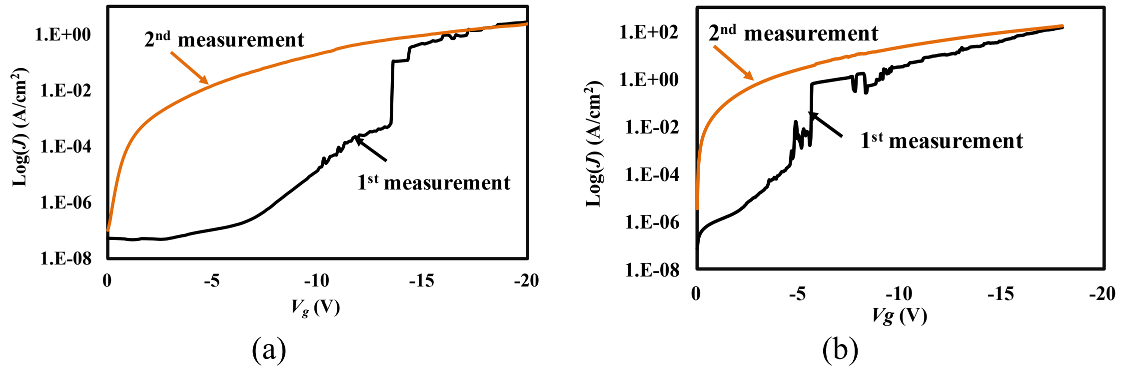
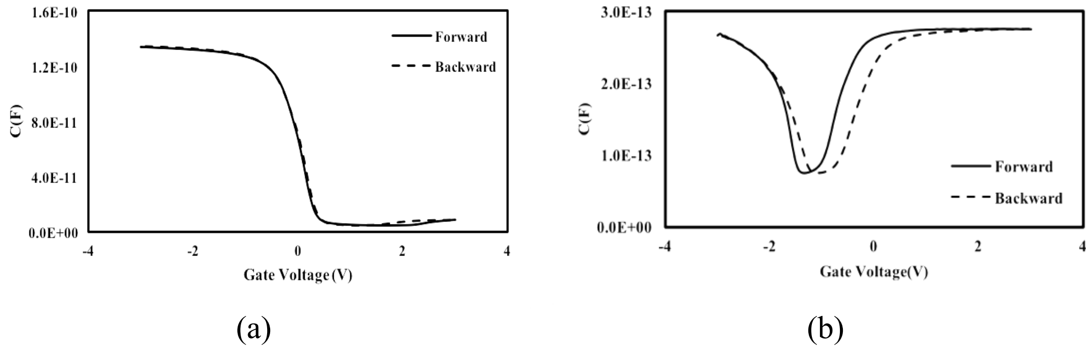


Figure 12. *J-V* curves of 400 μm diameter Mo gated capacitors (a) without and (b) with the PMA treatment.

3.4 Electrical Properties of Copper Gated MOS Capacitors

Figure 13 shows *C-V* hysteresis curves of Cu gated capacitors (a) without and (b) with the PMA step. Before PMA, as shown in Fig. 3(a), the *C-V* curve was similar to that of a good capacitor with V_{FB} of -0.357 V (forward) and -0.373 V (backward), EOT of 9.3 nm, and Q_{ot} of 1.07×10^{10} (cm^{-2}). The Q_{ot} is related to the presence of unsaturated bonds, vacancies, and unsatisfied atomic valences in the dielectric layer.[50] During the device operation, charge carriers, i.e., electrons and holes, may be trapped and attached to defects in the gate dielectric film, which further affects the gate-induced electric field at the dielectric/Si interface and raises the threshold voltage. However, the *C-V* curve of the PMA treated sample, i.e., in Fig. 3(b), showed the distorted shape. It resembled the low-frequency measured curve, i.e., formation of inversion layer at the $+V_g$. Also, the capacitance in the accumulation region was much lower than that of the device without the PMA treatment. Therefore, the PMA step affected the capacitor's material properties.



(a) (b)

Figure 13. *C-V* hysteresis curves of 400 µm diameter Cu gated capacitors (a) without and (b) with the PMA treatment. Measured at 1 MHz.

Since Cu can easily diffuse through a dielectric film[39], it is possible that Cu diffused to the high-*k* gate dielectric during the PMA step. Figure 14 shows the chemical states of Cu at the Cu/ZrHfO interfaces of capacitors (a) without and (b) with the PMA treatment. The peak at 933 eV corresponds to the binding energy of Cu $2p^{3/2}$ (933 eV) in the elemental and/or oxidized states.[51] It was reported that under thermal stress between 150˚C and 300˚C, copper atoms could penetrate through the thermal oxide into the bulk silicon to cause catastrophic effect on the capacitor characteristics.[39] They induce electric-defect centers near the interface and deteriorate the *C-V* characteristics. They can also generate deep-level states at the silicon/silicon dioxide interface, which results in the increase of the generation-recombination rate of minority carriers and the reduction of the minority carrier lifetime.[39] Therefore, the capacitance change of the Cu gated capacitor is related to the existence of Cu atoms in the high-*k* dielectric layer.

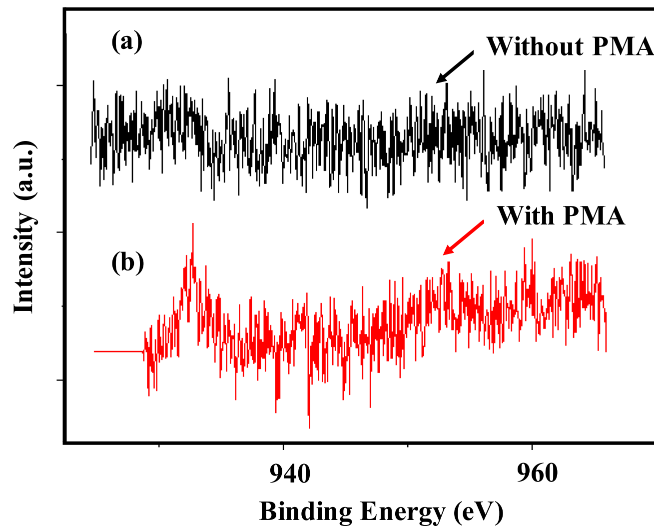


Figure 14. XPS spectra of 400 µm diameter Cu gated devices (a) without and (b) with PMA treatment.

J-V curves of Cu gated capacitors were also affected by the diffusion of Cu to the high-*k* film. Figure 15 shows *J-V* curves of Cu gate capacitors (a) without and (b) with the PMA treatment. The 1st measurement in Figure 15(a) shows several breakdown steps due to many defects in the gate dielectric film. The first breakdown occurred at around -6 V. However, the 1st measurement in Figure 15(b) shows one clear breakdown step at around -4.1 V. Some original defects in the gate dielectric film were probably removed by the PMA treatment. On the other hand, the leakage current of the PMA treated capacitor was larger than that of without the PMA treatment. This is consistent with the XPS measurement that Cu atoms were diffused into the gate dielectric layer to cause high leakage current and to facilitate the breakdown process.

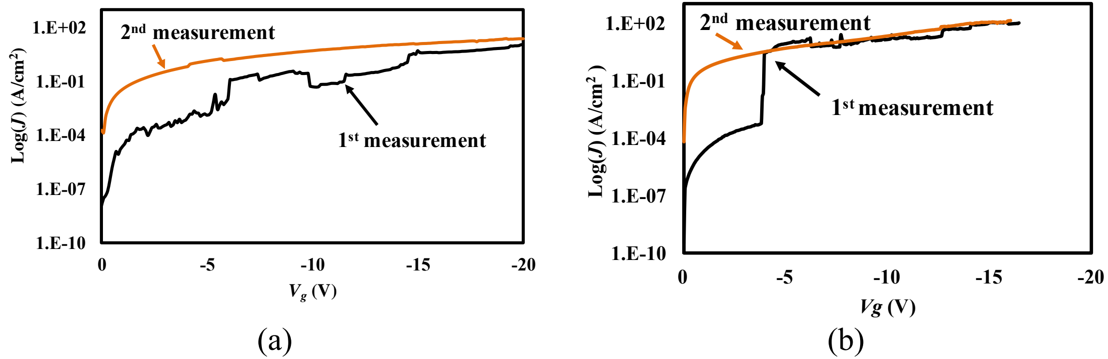


Figure 15. Current density-voltage (*J-V*) of 400 µm diameter Cu gated capacitors (a) without and (b) with PMA treatment.

3.5 Summary

Electrical properties, i.e., *J-V* and *C-V* characteristics, on 400 μm diameter Mo and Cu gated capacitors fabricated with the thermal annealing procedure were studied. For dielectric parameters, the properties of high-*k* layer in Mo gated devices were improved by PMA process due to the reduction of defects in the high-*k* film while those of Cu gated devices degraded from metal diffusion in the dielectric layer. As shown in *J-V* curves, the breakdown voltages of both metal gated devices decreased upon the application of PMA. The performance of the capacitor is influenced by the PMA treatment, which affects the reaction between the gate and the high-*k* gate dielectric as well as the removal of defects in the film and at the interface. Therefore, the selection of gate material is crucial to fabricate proper MOS capacitor.

CHAPTER IV

ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K BASED SSI-LED

4.1 Introduction

The high-*k* dielectric has been used to replace SiO_2 as the gate dielectric material in the scaling down of the metal-oxide-semiconductor (MOS) device. While the leakage current of the MOSFET with an ultrathin thermal SiO_2 gate dielectric, e.g., < 1.0 nm[26], has a very large leakage current density (*J*) of greater than 1A/cm^2, the device made of a proper high-*k* gate dielectric of the same equivalent oxide thickness (EOT) can have a leakage current density several orders of magnitude lower.[27-28] This is due to the high-*k* film's large band gap energy and large band offset with Si, which generates a potential barrier over 1 eV.[26, 29-30] However, one of the reliability concerns for the Hf-based dielectric is the low crystallization temperature, e.g., < 600˚C.[31] It was reported that the Zr-doped HfO_2 (ZrHfO) thin film has many advantages over the undoped HfO_2 thin film, such as higher crystallization temperature, higher permittivity, lower interface thickness, and lower interface density of states.[32-34]

The nanoresistors are formed in the high–*k* stack as a result of the hard breakdown of a MOS capacitor. Upon the application of a negative gate voltage ($-V_g$), holes are injected into dielectric layer, which generates a lot of defects in both the bulk and interface layers.[16, 22] When these defects are connected, the hard breakdown phenomenon occurs and nanoresistors are formed. Before the breakdown, the current flows through the high-*k*

stack following the Schottky emission (at low voltage) and Poole-Frenkel (at high voltage) mechanisms.[22] After the dielectric breakdown, the current flows through nanoresistors following Ohm's law, i.e., showing the linear current vs. voltage (*I-V*) relationship. When a large current is passed through these nano-resistors, the broad warm white light is emitted due to the thermal excitation mechanism. On the other hand, in the low voltage operation region, the device shows the diode-like current-voltage (*I-V*) behavior because the current only flows in one direction to the gate electrode but not the other direction.[22] Additionally, it can be used as an antifuse because the after-to-before dielectric breakdown current ratio is larger than 10^5.[22] Previously, electrical properties of the nanoresistor device were measured at room temperature under the atmosphere. Since the nanosized structure is easily subject to the environmental effect, e.g., oxidation in air[21, 52], it is important to understand how the temperature and humidity affect the electric resistance of the nanoresistor device.

4.2 Experimental

MOS capacitor samples were fabricated on a pre-cleaned *p*-type <100> silicon (10^{15} cm^{-3}) substrate in this chapter. For the zirconium hafnium oxide (ZrHfO) based device, the gate dielectric was sputter-deposited from the Zr/Hf (12/88 wt%) target in Ar/O_2 (100:100 sccm) at 5 mTorr and 60 W for 12 min. After oxide layer deposition, the sample was treated with a PDA step at 800˚C in nitrogen or oxygen atmosphere for 5 min, separately, in order to investigate the ambient effect on the sample performance. Then, an 80 nm thick

ITO with conductivity of 650 $\mu\Omega$-cm film was deposited on oxide layer and wet etched into round gate electrodes through aqua regia solution. Subsequently, the Al thin film was deposited at backside of the sample in Ar (100 sccm) at 5 mTorr and 80 W for 40 min. The completed sample was then annealed at 400˚C in forming gas (H_2/N_2 10/90) for 5 min. *C-V*, *J-V* characteristic curves, and light photos were measured with the same method as described in Chapter II. Figure 16 shows the structure of ZrHfO high-*k* MOS capacitor with aluminum backside electrode.

ImageJ, which is an open sourced Java-based image processing program developed at the National Institutes of Health and the Laboratory for Optical and Computational Instrumentation (LOCI), is utilized in high magnification photo for dot number analysis. First, the photo was converted to black and white image through the Thresholding method option. Then, the particle count can be calculated depending on size range, and circularity which is set as 0.5-1 in this thesis.

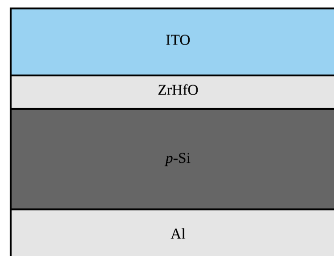


Figure 16. Structure of ZrHfO high-*k* MOS capacitor.

For the temperature and environmental effect on resistance of nanoresistor devices section, MOS capacitors of 50 μm, 100 μm, 200 μm, 300 μm, and 400 μm diameters were fabricated on a pre-cleaned p-type (10-5cm-3) <100> Si wafer. Each capacitor contains 1) a zirconium-doped hafnium oxide (ZrHfO) high-k gate dielectric (about 10 nm thick including the interface layer with Si), 2) an 80 nm thick ITO gate electrode, and 3) a Mo back side contact layer. The ZrHfO high-k film was sputter deposited on the Si wafer from a ZrHf (12/88 wt. %) composite target in Ar/O2 (1:1) at 5 mTorr and 60 W for 12 min. During the deposition process, an amorphous Hf-silicate interface layer (IL) was formed.[53] The ITO transparent gate electrode was sputter deposited on top of the ZrHfO film and wet etched into gate electrodes. A molybdenum (Mo) film was deposited on the back side of Si wafer. The complete capacitor was annealed at 400℃ in H_2/N_2 (1:9) for 5 min. Nanoresistors formed after hard dielectric breakdown and the equivalent circuit of a nanoresistor are shown in Figure 17. The current flows through, in sequence, the ITO gate electrode, the gate electrode/nano-resistor interface, the nanoresistor in ZrHfO, the interface between ZrHfO and IL, the nano-resistor in IL, the interface between IL and Si, the Si wafer, the interface between Si and the back metal, i.e., Mo, and the backside metal. The *I-V* curve of the nano-resistor device was measured between V_g = 0 V and -20 V at room temperature, 50˚C, 80˚C, 100˚C, and 120˚C, separately. Then, the sample was loaded in an environmental chamber (Associated Environment System BHD-403 7136) and annealed under the condition of 80% relative humidity and 80˚C. The sample was removed from the chamber after 3 and 7 hours, separately, to measure the *I–V* curve.

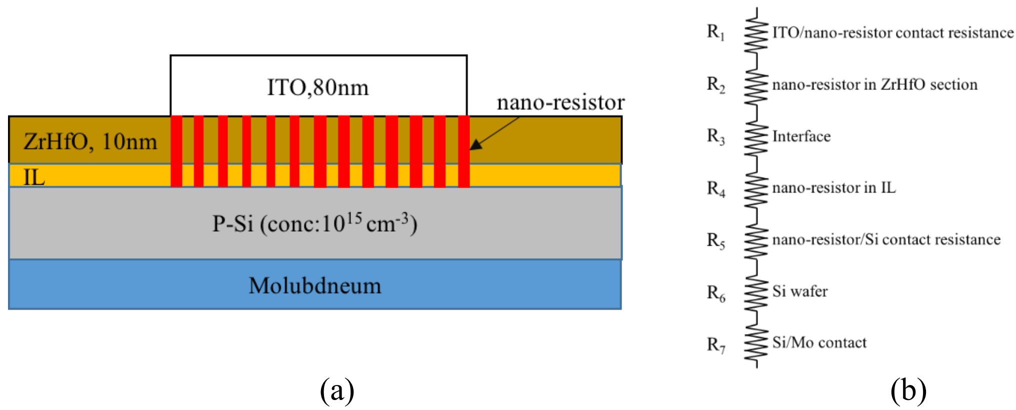


Figure 17. (a) Cross-sectional view of a nano-resistor device, (b) equivalent circuit of a nano-resistor.

4.3 Electrical Properties Characterization

Figure 18 shows the *C-V* hysteresis curves of ZrHfO samples prepared with post-deposition annealing (PDA) in nitrogen or oxygen atmosphere measured at gate voltage swept from -4 V to +4 V and then back to -4 V. The coefficients extracted from the *C-V* curves including capacitance in accumulation, equivalent oxide thickness (EOT), interface statee density (D_{it}), oxide trapped charges (Q_{ot}), and flat band voltage (V_{FB}) are shown in Table 1. The capacitance of sample prepared with PDA in O_2 atmosphere measured in accumulation regime is lower than that prepared with PDA in N_2 atmosphere, and thus the higher EOT of former is obtained, i.e. 6.59 and 11.4 for nitrogen and oxygen annealing, respectively. This is consistent with the reported that the a HfSiO intermixed layer is always formed between the bulk ZrHfO and the Si substrate after the PDA step[54-56], and

the oxygen annealing can lead to the growth of a thick interfacial layer.[57] In addition, both of the interface stated density D_{it}, oxide trapped charge density Q_{ot}, and hysteresis window ΔV_{FB} were lowered by O_2 annealing. It suggests that the oxidation can partially repair the damaged interface showing a good passivation oxide layer and thought to be able to remove vacancies, such as H or other defects in the bulk oxide.[57-59] For flat band voltage, after applying oxygen annealing, negative voltage shift was observed, which indicates that the negative charge in oxide or interface was passivated. The negative charge built at the surface is resulting from the acceptor defects generated from the low-lying dangling bond states, which is related to the amount of interface charge density.[57] Therefore, the lowered amount of D_{it} is also related to the change of the flat band voltage. From *C-V* characteristic curves, the oxygen annealing procedure is able to eliminate the defects in the high-*k* layer.

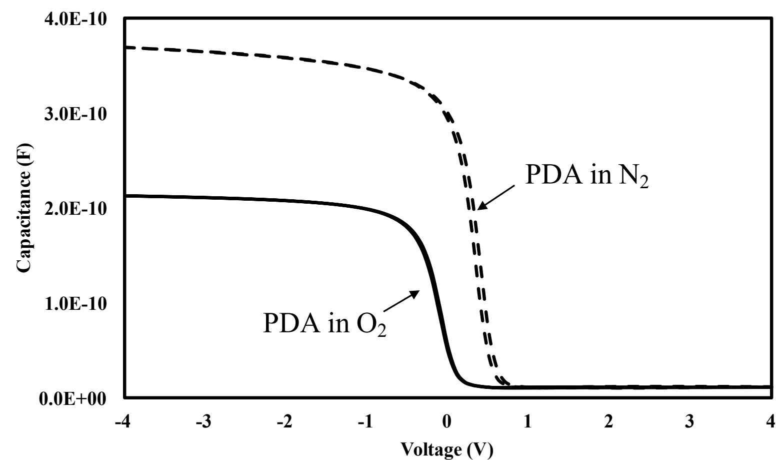


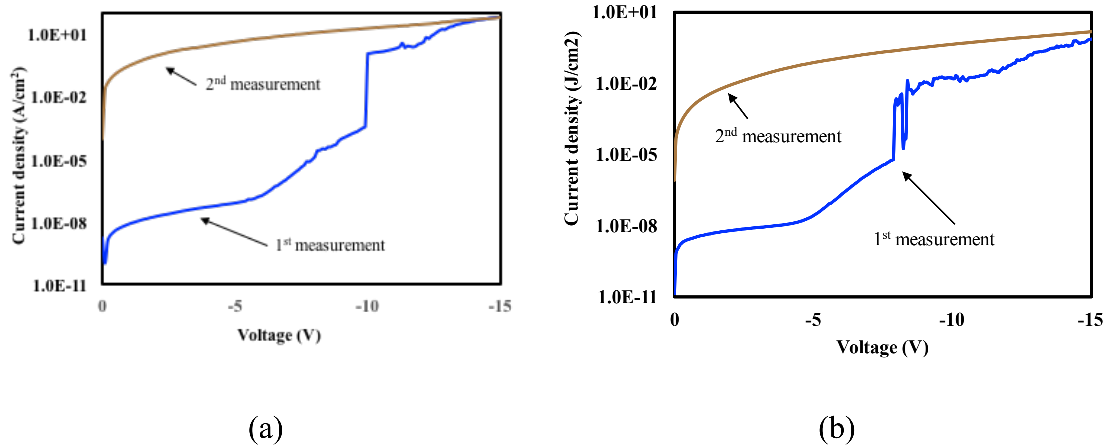
Figure 18. *C-V* hysteresis curves of ZrHfO sample with diameter of 300 µm.

Table 1. Coefficients calculated from *C-V* hysteresis curves of ZrHfO MOS capacitors prepared with PDA under N_2, and O_2.

Oxide material/ PDA ambient	C_{ox} (F)	EOT (nm)	D_{it} ($cm^{-2}eV^{-1}$)	Q_{ot} (cm^{-2})	V_{FB} (forward) (V)	V_{FB} (backward) (V)	ΔV_{FB} (V)
ZrHfO/ N_2	3.7×10^{-10}	6.59	2.08×10^{11}	1.92×10^{12}	0.6	0.56	-0.04
ZrHfO/ O_2	2.14×10^{-10}	11.4	9.57×10^{10}	1.49×10^{11}	0.1	0.09	0.011

Figure 19 shows *J-V* curves of the ZrHfO samples prepared with PDA in nitrogen and oxygen of 300 µm diameter with the gate voltage V_g being swept from 0 V to -15 V. For both of the samples, the *J-V* curves show two stage behavior before the breakdown takes place. At regime of the low $|-V_g|$ applied on ITO electrode, majority carriers, holes, accumulated at the Si-oxide interface are emitted through the high-*k* stacks following the Schottky emission (SE), field enhanced thermionic emission mechanism. At the larger $|-V_g|$ regime, the leakage current density increases following the Poole-Frenkel (P-F) conduction mechanism which involves Coulomb attraction between charged trap states and the emitted ions besides external electric field.[55] The increasing amount of holes are injected into the dielectric stacks with the increase of $|-V_g|$, and eventually it leads to the hard electrical breakdown at breakdown voltage as the sudden jump of leakage current density shown in the 1st measurement.[60] Then, the nanoresistors formed and served as conductive passage for current form permanently through interfacial layer and bulk oxide.[55] As shown in Table 2, the leakage current density, which measured at -1 V before breakdown, of the ZrHfO sample prepared with PDA in oxygen is lower than that of the

sample prepared with nitrogen annealing. It is attributed to the lowered defect density through the oxygen annealing process. The resistance calculated from *I-V* curves of samples prepared with nitrogen atmosphere was higher, i.e., 725.61 and 926.39 for PDA in nitrogen and oxygen, respectively. It may contribute from the higher density of defective sites in the device which favors the breakdown mechanism. Therefore, the more conductive paths forming in the device causes the decrease of device resistance.



(a) (b)

Figure 19. Current density vs. stress gate voltage of ZrHfO samples with PDA in (a) nitrogen, and (b) oxygen. Sample diameter: 300 µm.

Table 2. The breakdown voltage, leakage current density at -1V, and resistance of ZrHfO samples prepared with various atmosphere extracted from *J-V* measurement.

Oxide material/ PDA ambient	ZrHfO/ N_2	ZrHfO/ O_2
V_{BD} (V)	-9.9	-8.1
Leakage current density (J/cm^2) at -1 V	$-7.63x10^{-9}$	$-3.9x10^{-9}$
Resistance (Ω)	725.61	962.39

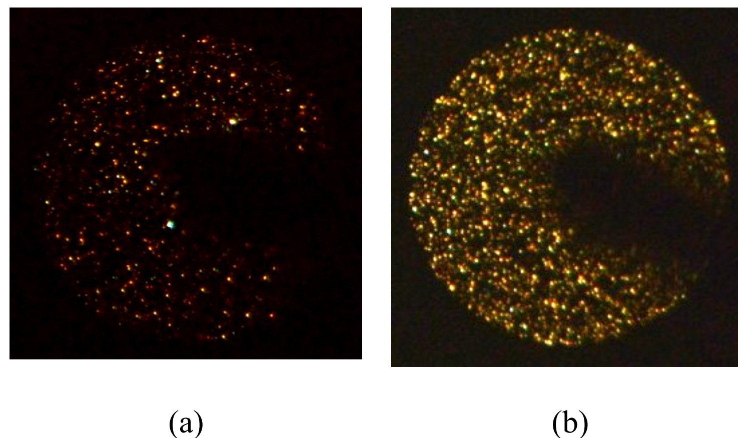
4.4 Optical Properties Characterization

Figure 20 shows the high magnification photos of ZrHfO samples prepared by PDA in nitrogen and oxygen with gate electrode of 300 μm diameter, and the shadow at right part of photo is the probe. The discrete dots are formed permanently after breakdown, and the corresponding bumps formed from the melting of ITO due to the high local temperature resulting from the current flow[61-62] are observed on the ITO surface, which can be considered as an evidence for the formation of conductive path.[53] Figure 20(a) shows the higher brightness than Figure 20(b), and it is because the larger resistance of the sample prepared with PDA in oxygen atmosphere can produce more heat according to Joule heating which is expressed as following equation:

$$P \propto I^2 R \qquad [7]$$

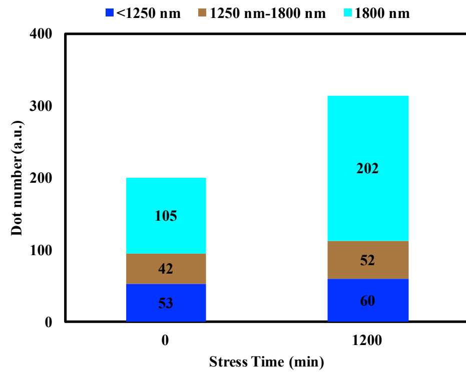
, where P is the power converted from electrical energy to thermal energy, I is the passage of an electric current through the resistor, and R is the resistance. The sample with larger resistance is able to generate the larger amount of heat to increase the temperature of the device, and the atoms in the nanoresistor are thermally excited. Those excited electrons due to the thermal kinetic energy can relieve by photonic emission, and therefore generate the light. As a consequence, the higher temperature of the device can generate more light in visible wavelength. In addition, the light dot number counted by ImageJ increased with the stress time for all the samples as shown in Figure 21. Since the program can not distinguish the dot lower than 1 pixel in the photo, and the smaller light dots might not be counted in this case, Figure 21 is not able to include the real number of light dots presented

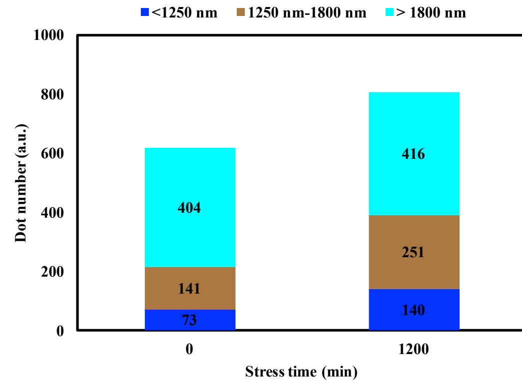
on ITO surface, but only gives a rough idea for the variation over the stressed time. The light dots grow in size and number, which can be explained through the breakdown mechanism promoted by escalating temperature of whole device during the application of voltage. Figure 22 shows the current vs. stress time curves of the samples fabricated in PDA in nitrogen and oxygen atmosphere, separately. Both of the samples do not degrade within the operation time, which indicates that the ZrHfO based SSI-LED performs stable. The inserted images in Figure 22 show that the dot number of device increase with the stress time. It is correlated with increasing current at the fixed gate voltage, i.e. the resistance decreases with the stress time due to the formation of nanoresistor.



(a) (b)

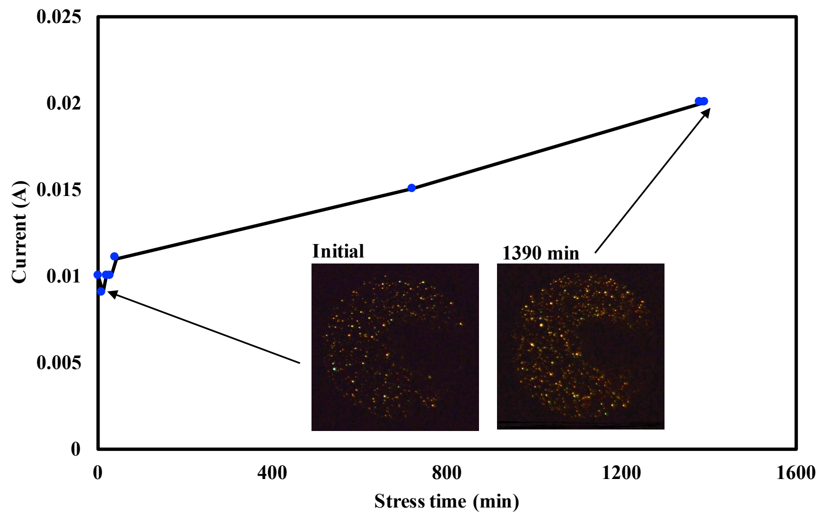
Figure 20. Photos of ZrHfO sample with PDA in (a) nitrogen and (b) oxygen stressed for 1200 min with sample size of 300 µm diameter.





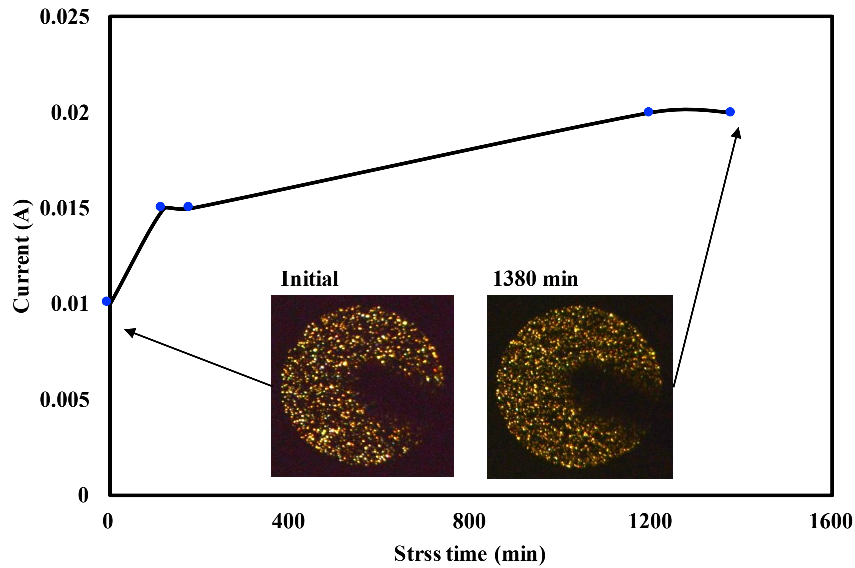
(a) (b)

Figure 21. Dot number counted from light photos of ZrHfO samples prepared with PDA in (a) nitrogen, and (b) oxygen stressed for 1200 min.



(a)

Figure 22. Current as a function of stress time of ZrHfO samples with PDA in (a) nitrogen and (b) oxygen. Inset: Photos at various stress time.



(b)

Figure 22. Continued.

4.5 Environmental Effect on Resistance

4.5.1 Low |-V_g| range (-1 V to -5 V)

Figure 23(a) shows the *I-V* curve of a 200 μm diameter nanoresistor device before and after the dielectric breakdown. The resistance of the device was extracted from the linear portion of the curve, i.e., between V_g = -10 V to -18 V. After the dielectric breakdown, the *I-V* curve in the low |- V_g| range is larger than that before dielectric breakdown. However, in the large |- V_g| range, the *I-V* curve remains the same for many measurements because of the permanent formation of nanoresistors.

Figure 23(b) shows resistances of 50 μm, 100 μm, 200 μm, and 300 μm diameter devices extracted from *I-V* curves between V_g = -2 V and -5 V at room temperature. The resistance decreases with the increase of the magnitude of the applied voltage in this range. From *Vg*= -2 V to -5 V, the resistances decreased by 58.2%, 57.2%, 48%, and 47.9% for the 50 μm, 100 μm, 200 μm, and 300 μm devices, separately. Since the total number of nanoresistors in the device increases with gate electrode size, the resistance of the device decreases with the increase of the size.

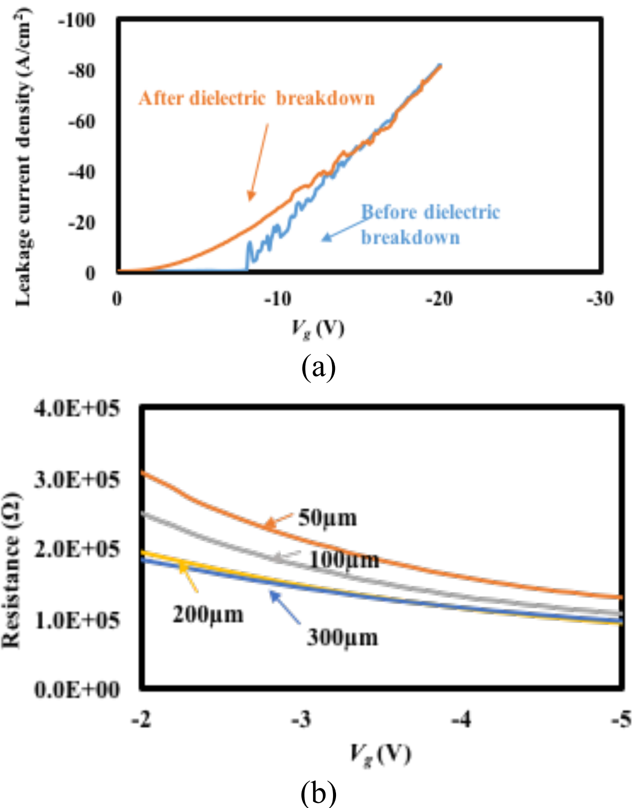


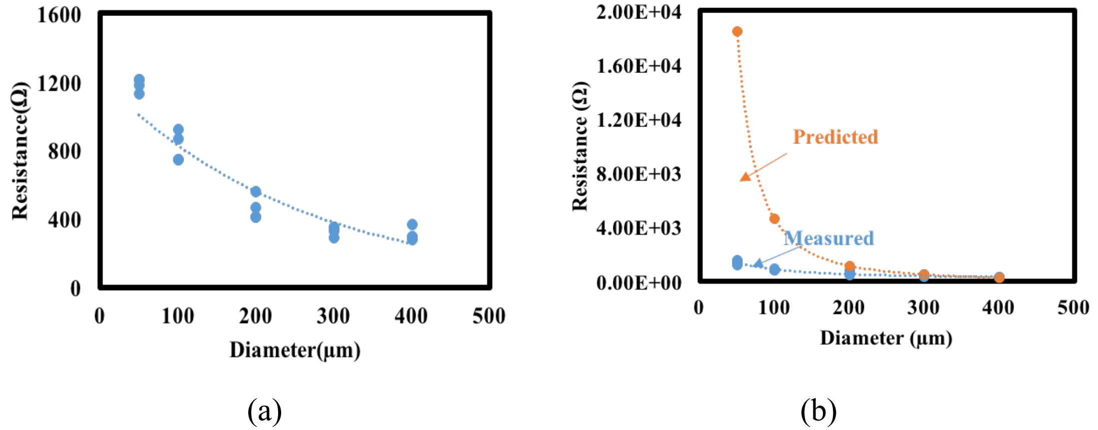
Figure 23. (a) *I-V* curve of a 200 µm device before and after nano-resistor formation, (b) resistances of 50 µm, 100 µm, 200 µm, and 300 µm nano-resistor devices for V_g = -2 V to -5 V. All devices measured at room temperature.

4.5.2 High $|-V_g|$ range ($> |-10V|$)

Figure 24(a) shows resistances extracted from the linear regions of *I-V* curves of various sized nanoresistor devices at room temperature. The resistance decreases nonlinearly with the increase of the diameter of the device. The resistance vs. device size relationship should follow the Pouillet's law of

$$R = \rho \cdot L/A \qquad [8]$$

where R is the resistance, ρ is the resistivity, L is the length, and A is the cross-sectional area. Assuming that nanoresistors in different devices are of the same resistivity and are evenly distributed across the gate electrode area, one can predict the resistance of a nanoresistor device from that measured from another device of a different size. For example, Figure 24(b) shows the resistance vs. device size curves predicted from the measured resistance of a 400 μm diameter device and from actual measurement. The prediction curve deviates from the measured data. The difference increases with the decrease of size of the device. It was reported that the density of nanoresistors near the edge of the gate was larger than that in the center region.[48] As the diameter of the device is reduced, the area ratio of the edge region to the total gate electrode increases. Therefore, the density of the nanoresistors increases with the shrinking of the device size, which results in the reduction of the resistance. Also, nanoresistors near the gate electrode edge may be of different sizes from those away from the edge, which further complicates the relationship between the resistance and the size of the nanoresistor device.



(a) (b)

Figure 24. (a) Resistances of nano-resistor devices measured in high |-V_g| range at room temperature, (b) experimentally measured and predicted resistance vs. size curves.

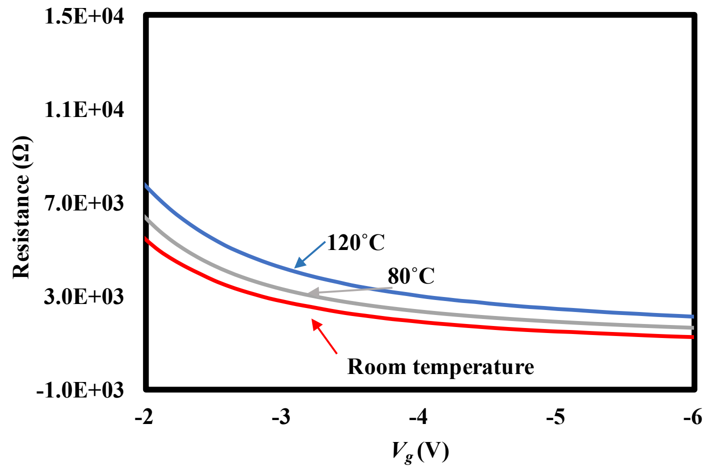
4.5.3 Temperature Effect on Resistance

Figure 25(a) shows resistance vs. V_g curves of a 200 μm size device measured in the low |-V_g| range at different temperatures. The resistance increases with the increase of the temperature. It was reported that the Si/nanoresistor contact follows the Schottky relationship. Also, the barrier height increases with the increase of temperature and decreases with the increase of the magnitude of the stress voltage, i.e. 0.6 eV and 0.56 eV for the -20 V and -40 V (10). In the low |-V_g| range, the Schottky barrier height is the main factor affecting the resistance. Due to the increase of the barrier height with the increase of the temperature, more energy for the electrons to pass through the current path is required. Thus, the resistance of the nanoresistors increases with the increase of the temperature. Figure 25(b) shows resistances vs. temperature curves of various sized nanoresistor devices at 50˚C, 80˚C, 100˚C, and 120˚C measured in the high |-V_g| range. For all devices, the resistance increases with the increase of the temperature. Since the

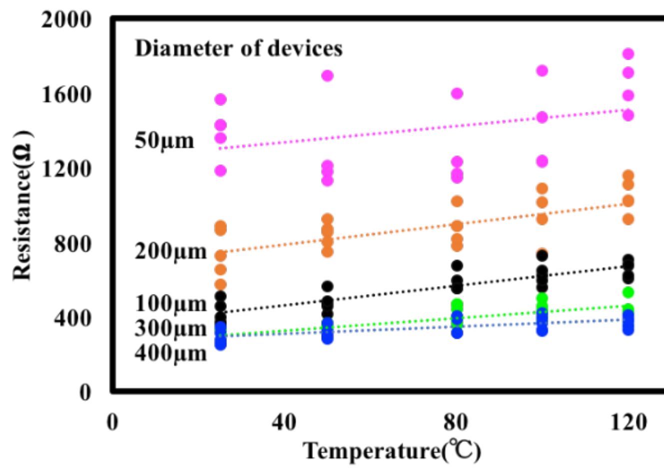
resistance is contributed by all elements in the current path, i.e., the ITO gate electrode, nanoresistors, interfaces, the Si wafer and the interface contact resistance, each of which can affect the result. For example, the resistance of molybdenum back electrode is calculated from the formula,

$$R = R_{ref} \times [1 + \alpha(T - T_{ref})] \qquad [\mathbf{9}]$$

where R is the conductor resistance at temperature T, R_{ref} is the conductor resistance at reference temperature T_{ref}, α is temperature coefficient of resistance for conductor material, T and T_{ref} are conductor temperature in degrees Celsius. At room temperature, the resistance of molybdenum is 53.4 nΩ, and 77.9 nΩ at 120℃. Although the Mo resistance is affected by the temperature[63], the value is much smaller than that of the nanoresistor device in Figure 29. The resistance of the *p*-type Si substrate changes little in the room temperature to 120˚C range, i.e. in the extrinsic region, an increase of temperature generates less increase of carrier concentration.[64] The resistance of ITO also remains in the same temperature range.[65] As for the contact resistance, the gate/nanoresistor contact appears ohmic and the nanoresistor/Si contact follows the Schottky relationship.[53, 66] Even though the barrier height increases with the increase of the temperature, i.e. 0.6 eV at 20℃ and 0.7 eV at 100℃ for 20 V, the rise cannot totally explain the increase of the resistance. Therefore, the temperature effect may be contributed by the dynamic formation process of nanoresistors as temperature increases.



(a)

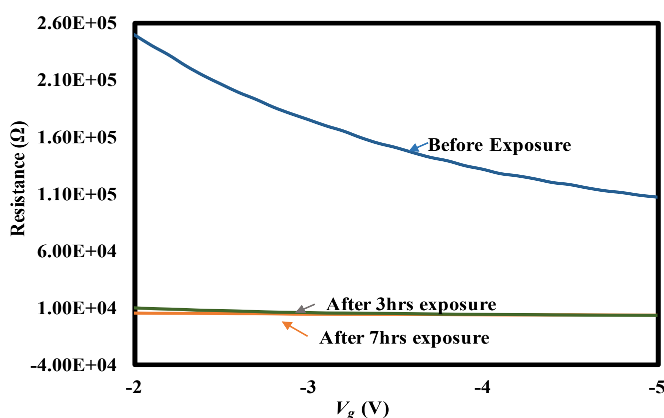


(b)

Figure 25. (a) Resistance vs. V_g curves of a 200 μm device in low $|-V_g|$ range measured at room temperature, 80℃, and 120℃, (b) resistance vs. temperature curves in high $|-V_g|$ range of different sized devices.

4.5.4 High Humidity and High Temperature Annealing Effect

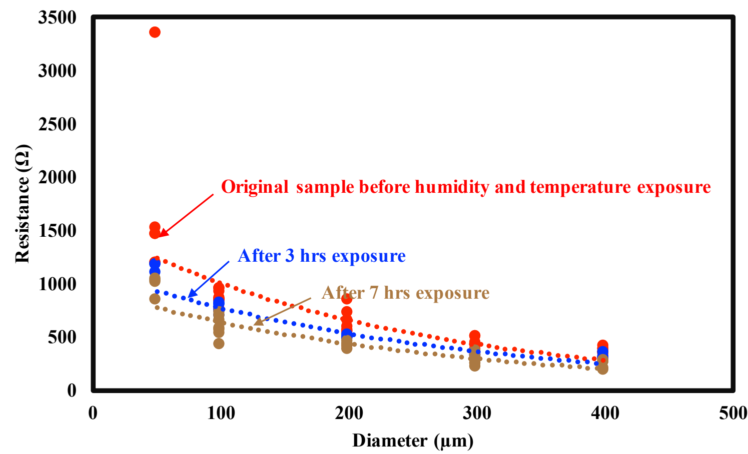
Figure 26(a) shows the resistance vs. V_g curves of a 100 μm device annealed under 80% relative humidity and 80℃ for different time periods measured in the low $|-V_g|$ range. The resistance decreased after the annealing. Figure 26(b) reveals that the resistance of the device in the high $|-V_g|$ range decreases with the increase of annealing time. Also, the change decreases with the increase of the device size. The diffusion of humidity caused the increase of the Si/nanoresistor interface layer thickness. On the other hand, when high gate voltage is applied, the strong electric field can ionize the interlayer water molecules diffusing in the high-k film, and leads to the yield of electrons and hydroxyl ions. Therefore, the resistance of nanoresistor decreases when the ambient relative humidity is high.[67]



(a)

Figure 26. (a) Resistances of a 100 µm device in the low -V_g range after 3 hrs and 7 hrs annealing, (b) resistances in the high -V_g range of different sized devices annealed for 0, 3, and 7 hrs. Annealing condition: 80% relative humidity and 80℃.

(a)



(b)

Figure 26. Continued.

4.6 Summary

Electrical properties, i.e., *I-V*, *C-V* curves and resistances, of ZrHfO based nanoresistor devices prepared with various fabrication procedure have been investigated. With oxygen annealing after high-*k* deposition, the interface quality was improved, i.e. D_{it} and Q_{ot} values were lowered, due to the removal of defects such as dangling bond states in the interface, while the EOT was increased resulting from the thickened interfacial layer. As a result, the leakage current density was improved, and the SSI-LED device became brighter. As for the environmental impact on resistance of SSI-LED, in the low $-V_g$ range, the resistance decreased with the increase of the device size due to the larger number of nanoresistors. Under the atmosphere, the resistance increased with the substrate

temperature and the decrease of the device size. The high humidity and high temperature annealing condition changed the composition and structure of all elements in the current path. Therefore, the resistance changed accordingly.

CHAPTER V

TUNGSTEN OXIDE HIGH-K BASED SSI-LED

5.1 Introduction

The conductive path as well known as nanoresistor formed after the dielectric breakdown took place in the MOS device, and the light emits from the thermal excitation in nanoresistor through the passage of current. It was suggested that the composition and structure of the nanoresistor affect the light emission characteristics of the device[22-23, 68-69]. Tungsten has been served as filament material in commercial incandescent light bulb due to high spectral emissivity ($\varepsilon_{\lambda} = 0.432$) as well as high melting point (3695 K), and tungsten oxide (WO_x) has been used as the gate dielectric layer in the thin film transistor.[70] Therefore, WO_x can be a potential substitution for the light emission layer in the SSI-LED. In this chapter, the electrical and optical properties of WO_x high-*k* device has been investigated.

5.2 Experimental

The MOS capacitor containing the tungsten oxide (WO_x) gate dielectric was fabricated on the dilute hydrofluoric acid pre-cleaned p-type silicon (100) wafer with doping concentration of 10^{15} cm^{-3}. The tungsten target (99.999 %) served as deposition source and was sputtered in Ar/O_2 (40:100 sccm) at 60 W for 12 min on substrate to form the WO_x

film. After oxide layer deposition, the sample was treated with a PDA step at 800˚C in N_2 atmosphere for 5 min. Then, an 80 nm thick ITO $\mu\Omega$-cm film was sputter-deposited on oxide layer and wet etched into round gate electrodes through aqua regia solution. Subsequently, the Al thin film was deposited at backside of the sample in Ar (100 sccm) at 5 mTorr and 80 W for 40 min. The completed sample was then annealed at 400˚C in forming gas (H_2/N_2 10/90) for 5 min. The capacitance-voltage (*C-V*) and current density-voltage (*J-V*) measurements were done as described in Chapter II. The high-magnification photos of the device were taken by Nikon D3200 24.2 MP CMOS digital camera.

5.3 Electrical Properties Characterization

This device shows typical MOS capacitor behavior when applying the small magnitude of gate voltage ($|V_g|$), i.e. lower than that of the breakdown voltage. Figure 27 shows the *C-V* curves of the sample measured at gate voltage swept from -4 V to +4 V and back to -4 V at 1 MHz. The coefficients from *C-V* curves related to dielectric properties of the device are listed in Table 3. The EOT of the oxygen annealed WO_x device is higher than that of the nitrogen annealed one. It can be explained by the increased interfacial layer through oxidation[71] or the reduced effective k value attributes to the composition change in the oxide stack.[28] The Q_{ot} value of the sample with oxygen PDA is much lower than that with nitrogen PDA one, i.e., 2.66×10^{11} and 2.34×10^{12}, respectively, which indicates the defect densities located in the bulk oxide can be reduced by removing oxygen vacancies.[28] The D_{it} of the oxygen annealed device is higher than that of the nitrogen annealed one. It was

suggested that the occupancy of the interface states is governed by the position of the Fermi level.[72] Since the stoichiometry of tungsten oxide may change after the oxidation process, it may roughen the interface or induce an unstable WO_x-Si interface which raise the Fermi level.

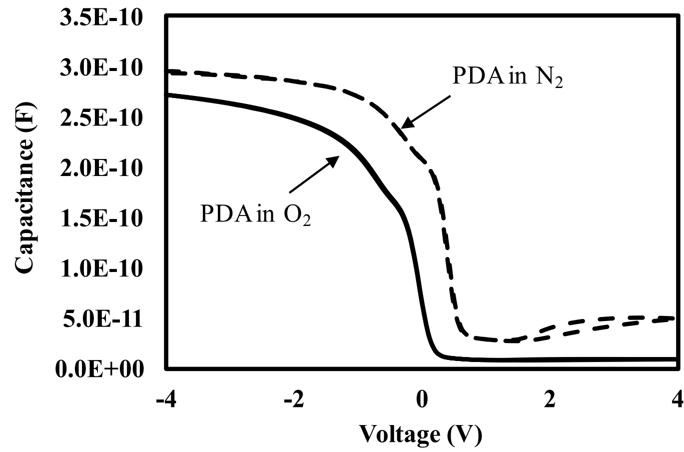
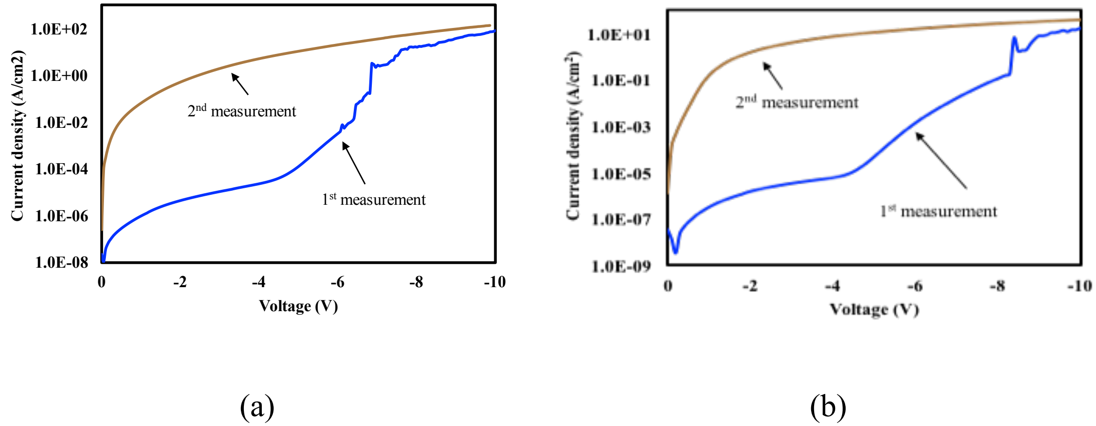


Figure 27. ***C-V*** **hysteresis curves WO_x samples fabricated under various post high-k deposition annealing ambient.**

Table 3. Coefficients calculated from *C-V* hysteresis curves of ZrHfO MOS capacitors prepared with PDA under N_2, and O_2.

Oxide material/ PDA ambient	C_{ox} (F)	EOT (nm)	D_{it} ($cm^{-2}eV^{-1}$)	Q_{ot} (cm^{-2})	V_{FB} (forward) (V)	V_{FB} (backward)(V)	ΔV_{FB} (V)
WO_x / N_2	2.94×10^{-10}	8.29	3.00×10^{12}	2.34×10^{12}	0.915	0.936	0.02
WO_x / O_2	2.71×10^{-10}	8.99	4.79×10^{12}	2.66×10^{11}	0.129	0.134	0.005

Figure 28 shows the *J-V* curves of nitrogen and oxygen annealed MOS devices with V_g swept from 0 V to -10 V. In the first measurement, the leakage current density presents a rapid increased at a certain voltage where is known as breakdown voltage (V_{BD}), i.e. -8.4 V and -6.85 V for nitrogen and oxygen annealed devices, respectively. The breakdown voltage can be affected by the thickened oxide or the imperfections in the thin film. With higher EOT and the oxide trapped charge density, the oxygen annealed device has higher V_{BD} than that of nitrogen annealed device. In addition, the larger leakage current density of the nitrogen annealed device may arise from the greater bulk oxide trap levels which contributes free electrons to the conduction band and increase the thin film conductivity. In the second measurement, the *J-V* curve is a smooth curve which behaves linear relationship at high $|-V_g|$ range, i.e. -6 V to -10 V. The resistance values calculated from linear portion of *I-V* curves are 238.54 Ω and 385.15 Ω for nitrogen and oxygen annealed samples, respectively. It indicates that the nitrogen annealed device performs more conductive after dielectric breakdown.



(a) (b)

Figure 28. ***J–V*** **curves swept from 0 V to -10 V of the WO_x LEDs with PDA in (a) nitrogen, and (b) oxygen. Sample diameter: 300 μm.**

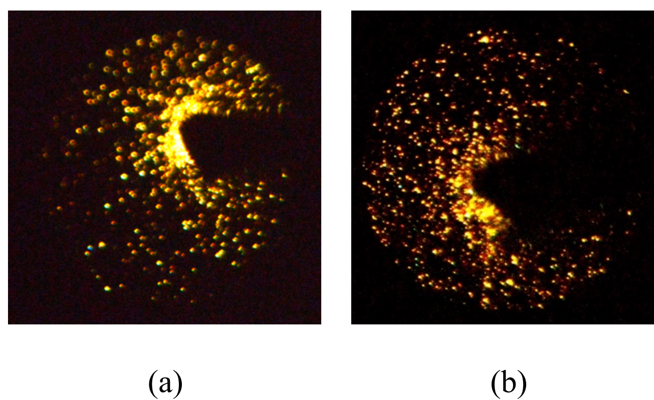
Table 4. The breakdown voltage, leakage current density at -1V, and resistance of WO_x samples prepared with various atmosphere extracted from *J-V* measurement.

Oxide material/ PDA ambient	**WO_x / N_2**	**WO_x/ O_2**
V_{BD} (V)	-6.85	-8.4
Leakage current density (J/cm^2) at -1 V	-7.95x10^{-7}	-3.47x10^{-7}
Resistance (Ω)	238.54	385.15

5.4 Optical Properties Characterization

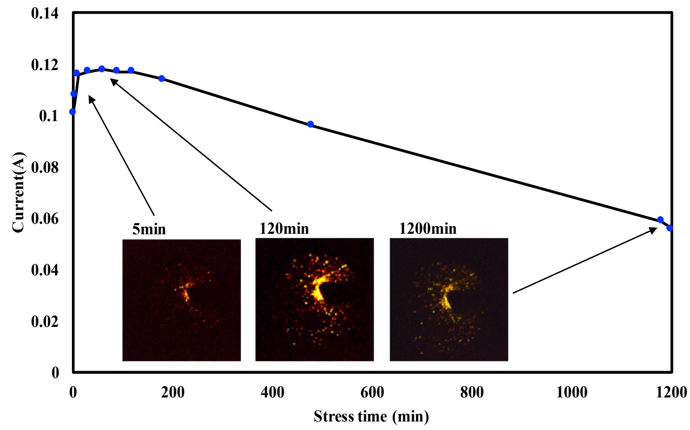
Figure 29 shows the high magnification photo of light emission pattern of nitrogen and oxygen annealed SSI-LEDs. The light emission pattern consisting of bright discrete dots demonstrates the unevenly distribution over ITO gate, i.e., the closer to the probe the higher the number density of bright dots, while the nitrogen annealed one shows less uniform than oxygen annealed one does. Unlike the conventional LED generating light

through the electron-hole or exciton-exciton recombination, the SSI-LED emits the light from the nanoresistor thermal excitation mechanism.[68, 71, 73-75] The number of bright dots in oxygen annealed SSI-LED appears to be slightly higher than that in nitrogen annealed device, which may attribute from the more visible light emission from higher resistance listed in Table 4. Figure 30 shows the time dependent current function for nitrogen and oxygen annealed SSI-LEDs with the inserted photos taken under various stress time. The nitrogen annealed device start to deteriorate after the device is stressed for 200 min, and brightness increases at first and then decreases along with the decline of current. On the other hand, the current of oxygen annealed device rises with stress time. It may result from the increasing amount of nanoresistor formed in oxide layer, or the change of individual nanoresistor resistance induced from difference in size or composition variance.[61, 68, 71, 73-75]

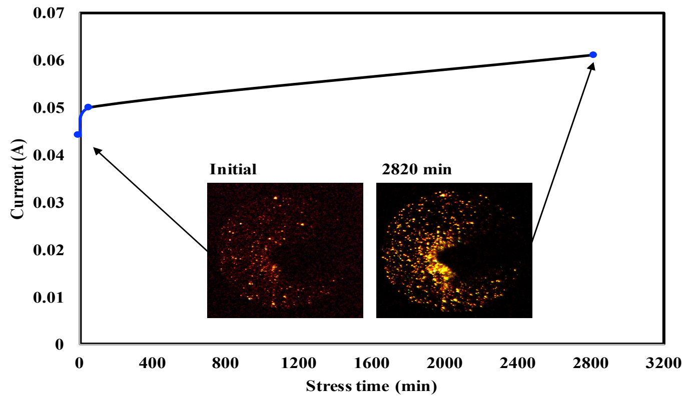


(a) (b)

Figure 29. High-magnification photos of the WO_x samples prepared with PDA in (a) nitrogen and (b) oxygen atmosphere. Stress voltage: -12 V.



(a)



(b)

Figure 30. Current as a function of stress time of WO_x samples with PDA in (a) nitrogen and (b) oxygen. Inset: Photos at various stress time.

5.5 Summary

The electrical and optical characteristics of SSI-LEDs fabricated from WO_x high-*k* MOS capacitors with various PDA ambient have been investigated. The oxidation process can

cause a thicker interfacial layer, lower bulk oxide trapped charge density, and a decreased leakage current density, and as a result, the oxygen annealed device does not deteriorate in short stress time. Furthermore, the oxygen annealed SSI-LED demonstrates a more uniform light emission pattern with higher number density of bright dot. Even though the PDA in oxygen procedure effect on WO_x dielectric layer is not apparent as that on ZrHfO dielectric material in Chapter IV, it can affect the capacitor properties with regards to device composition as well as material characteristics, and moreover, the SSI-LED performance.

CHAPTER VI

TUNGSTEN OXIDE EMBEDDED ZIRCONIUM-DOPED HAFNIUM OXIDE HIGH-K BASED SSI-LED

6.1 Introduction

The optical property of SSI-LED is affected by the composition and structure of the nanoresistor formed after dielectric breakdown in high-*k* layer. It was reported that the embedding of the nc-CdSe layer in the ZrHfO thin film significantly increased the light emission intensity.[61] While it was suggested that the WO_x gate dielectric SSI-LED showed great light emission performance in Chapter V, the leakage current of WO_x gate dielectric SSI-LED was higher than that of ZrHfO gate dielectric device. Therefore, the multiple WO_x layer were embedded into the ZrHfO gate dielectric to investigate the electrical and optical properties. In addition, the post-deposition annealing ambient on performance of the WO_x embedded ZrHfO high-*k* MOS capacitor was discussed in this chapter.

6.2 Experimental

All MOS capacitor samples were fabricated on a pre-cleaned *p*-type <100> silicon (10^{15} cm^{-3}) substrate in this chapter. For high-*k* deposition, ZrHfO and WO_x were deposited alternately layer by layer, and therefore the high-*k* stack consisted of four layers of ZrHfO and three layers of WO_x. Each of the ZrHfO layer was sputter-deposited from the Zr/Hf

(12/88 wt%) target in Ar/O_2 (100:100 sccm) at 5 mTorr and 60 W for 3 min. The tungsten target (99.999 %) served as deposition source and was sputtered in Ar/O_2 (40:100 sccm) at 60 W for 2 min for each of WO_x layer. Then, the sample was treated with a post-deposition annealing (PDA) step at 900˚C in nitrogen or oxygen atmosphere for 5 min, separately, in order to investigate the ambient effect. After that, an 80 nm thick ITO film was deposited on oxide layer and wet etched into round gate electrodes through aqua regia solution. Subsequently, the Al thin film was deposited at backside of the sample in Ar (100 sccm) at 5 mTorr and 80 W for 40 min. The completed sample was then annealed at 400˚C in forming gas (H_2/N_2 10/90) for 5 min. Figure 31 shows the schematic structure of the sample.

Electrical measurements, e.g., *J-V* and *C-V* curves, and spectrum measured with OES system was done as discussed in Chapter II, and the high-magnification photos were taken by Nikon D3200 24.2 MP CMOS digital camera.

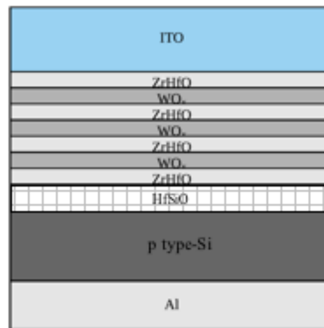


Figure 31. Schematic structure of WO_x embedded ZrHfO MOS capacitors.

6.3 Electrical Properties Characterization

Figure 31 shows *C-V* curves of the nitrogen annealed and oxygen annealed samples measure at 1 MHz with V_g swept from -3 V to +3 V (forward) to -3 V (backward). The coefficients related to the electrical properties of the device were calculated from the *C-V* hysteresis curves as shown in Table 5. The EOT value of oxygen annealed sample is higher than that of nitrogen annealed one. This phenomenon is similar as previous high-*k* MOS capacitor, and can be explained by the growth of a thick interfacial layer induced from the oxygen annealing process. [57] In addition, the small ΔV_{FB} which can be taken as hysteresis window of the oxygen annealed sample indicates the low charges trapped in the bulk high-*k* layer or at the interface between silicon and high-*k*. It is consistent with the lowered D_{it} and Q_{ot} of sample treated with oxygen annealing procedure. Also, the negative shift of flat band voltage of oxygen annealed sample indicates the reduce of negative charge trapped sites in the device. It is because the oxygen annealing procedure can remove the charged oxygen vacancies that have been suggested as the source of flat band voltage shifts.[76] Therefore, from *C-V* curves analysis, the annealing process conducted in oxygen ambient demonstrates the better performance than that in the nitrogen atmosphere.

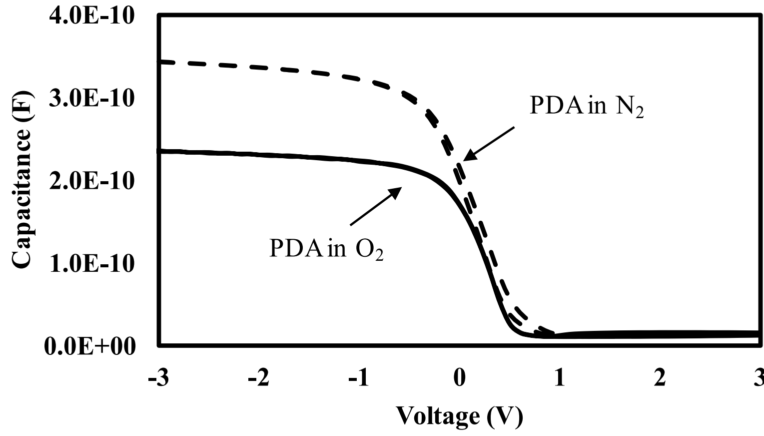


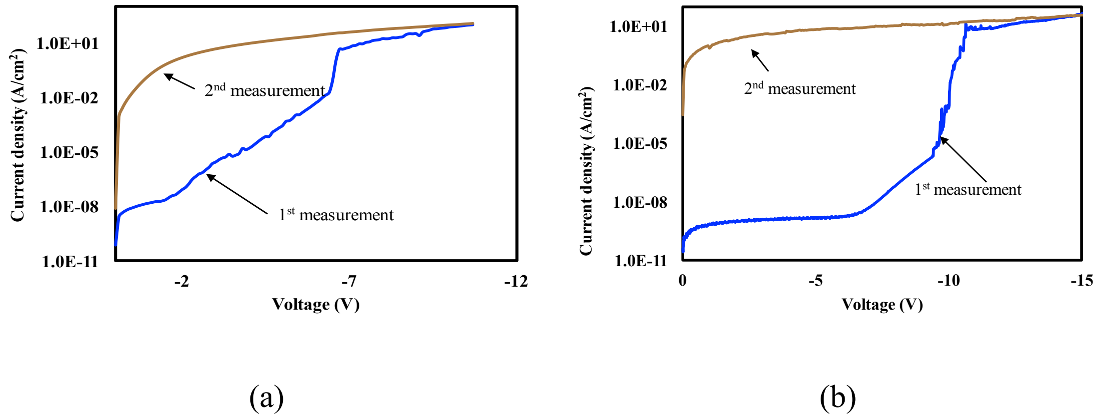
Figure 32. ***C-V*** **hysteresis curves of the samples with V_g swept from -3 V to +3 V to -3 V at 1 MHz. Dashed line: sample prepared with PDA in nitrogen atmosphere. Solid line: sample prepared with PDA in oxygen atmosphere.**

Table 5. Coefficients calculated from *C-V* hysteresis curves of WO_x embedded ZrHfO MOS capacitors prepared with PDA under N_2, and O_2 atmosphere.

Oxide material/ PDA ambient	C_{ox} (F)	EOT (nm)	D_{it} ($cm^{-2}eV^{-1}$)	Q_{ot} (cm^{-2})	V_{FB} (forward) (V)	V_{FB} (backward) (V)	ΔV_{FB} (V)
WO_x embedded ZrHfO/ N_2	3.44×10^{-10}	7.1	5.7×10^{11}	2.01×10^{12}	0.68	0.65	-0.03
WO_x embedded ZrHfO/ O_2	2.73×10^{-10}	10.3	2.84×10^{10}	9.81×10^{11}	0.49	0.49	0.001

Figure 33 show the *J-V* curves in the log scale of the samples prepared in various PDA ambient. Table 6 shows the coefficients extracted from Figure X, which are related to the electrical properties of the samples. For the 1st measurement, the obvious current jump

implying dielectric breakdown are observed at the gate voltage of -6.4 and -9.68 for the nitrogen annealed and oxygen annealed samples, respectively. The larger $|V_{BD}|$ of the former compared to that of the latter is due to the increased EOT as shown in Table 6. With thicker oxide layer, the oxygen annealed sample requires larger voltage to drive breakdown mechanism. In addition, the leakage current of the oxygen annealed capacitor is much lower than that of nitrogen annealed one. It is consistent with the lowered defective densities observed from *C-V* characteristic curve. The oxide annealed sample with the more passivated oxide and interfacial layer, the low leakage current density can be achieved. When the $|V_g|$ is further increased to be higher than the $|V_{BD}|$, the conductive paths are formed permanently and function like resistors that are thermally excited to emit light upon the passage of the high current. The average resistance of the oxygen annealed device is higher than that of the nitrogen annealed sample. According to the Joule’s heating and thermal excitation principle, the higher resistance is able to generate heat through the passage of the current, and thus it can emit the visible light in the shorter wavelength.



(a) (b)

Figure 33. *J-V* curves of the WO_x embedded ZrHfO MOS capacitor prepared with PDA in (a) nitrogen and (b) oxygen ambient.

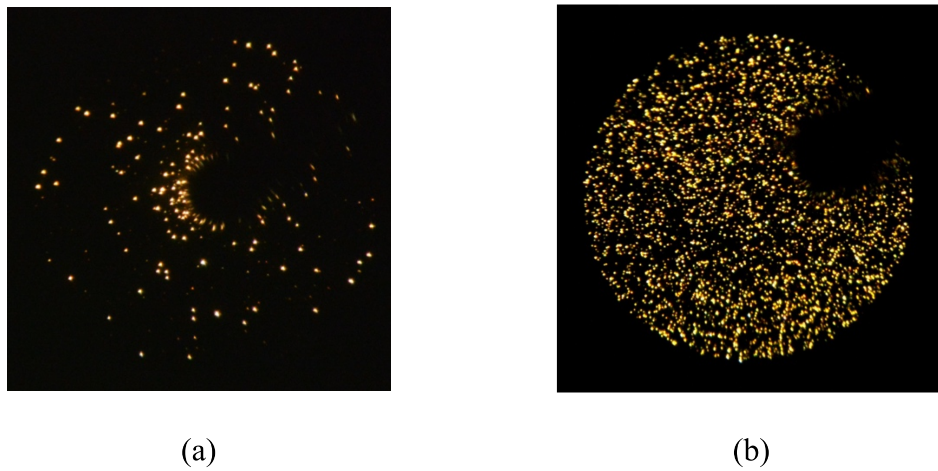
Table 6. The coefficients extracted from *J-V* curves of the samples prepared in various PDA ambient.

Oxide material/ PDA atmosphere	WO_x embedded ZrHfO/ N_2	WO_x embedded ZrHfO/ O_2
V_{BD} (V)	-6.4	-9.68
Leakage current density (J/cm^2) at -1 V	-1.48×10^{-8}	-7.78×10^{-10}
Resistance (Ω)	146.27	1192.7

6.4 Optical Properties Characterization

Figure 34 shows the high magnification photos of the WO_x embedded ZrHfO samples prepared in (a) nitrogen and (b) oxygen atmosphere after dielectric breakdown. In the round device with diameter of 300 μm, the light emission pattern is made up of many small discrete bright dots. As discussed previously, the light emits after the conductive paths formed due to the dielectric breakdown process. Even though the nitrogen annealed

sample has more defect sites located in the oxide layer which favors the dielectric breakdown, it results in the resistance too low to generate enough heat for the visible light emission. The uniform light pattern has been achieved through the oxygen annealing process.

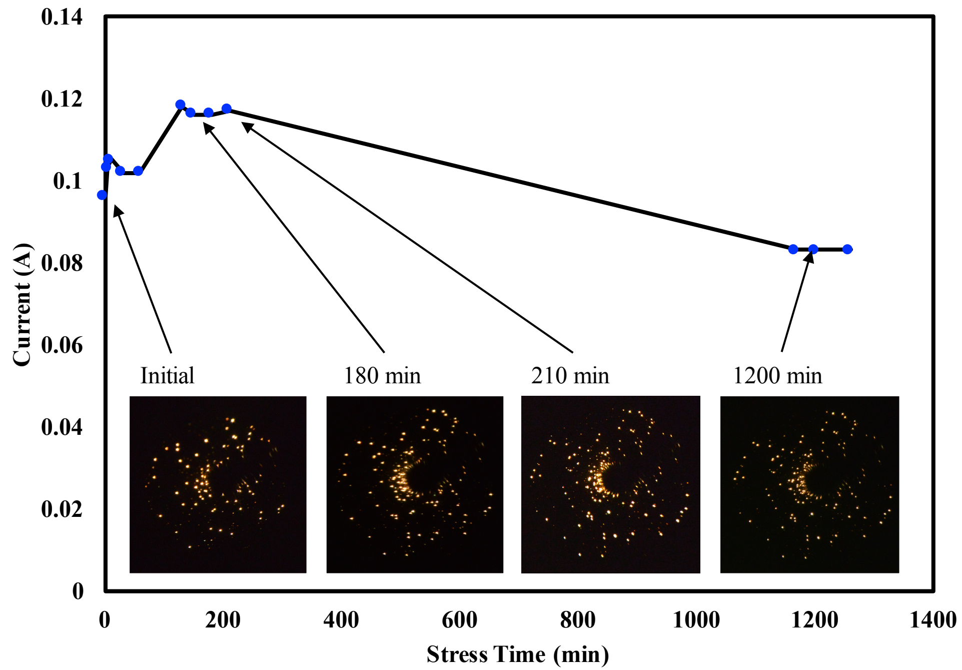


(a) (b)

Figure 34. High-magnification photos of the samples prepared with PDA in (a) nitrogen and (b) oxygen atmosphere.

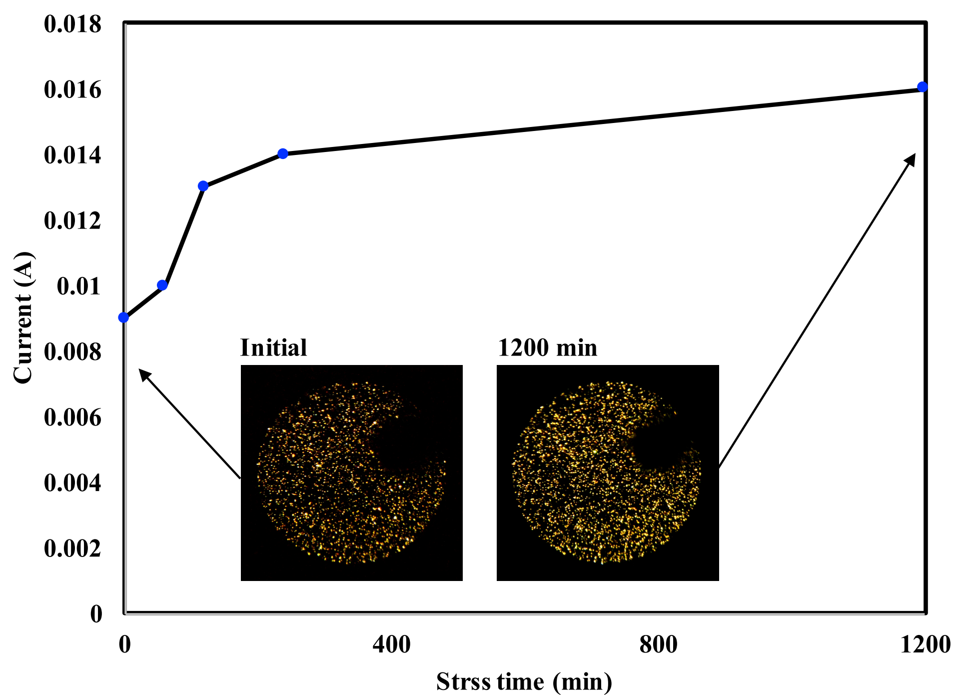
The time dependent current behavior of nitrogen and oxygen annealed SSI-LED were measured at the fixed gate voltage as shown in Figure 35. Figure 35(a) shows the current started to decrease when the nitrogen annealed device was stressed for 200 min, and the brightness of the device decreased accordingly, which means that the nitrogen annealed device deteriorate in short time. On the other hand, the current of oxygen annealed device increased in the time span. It may be explained by the increase of number of the bright

dot, which can be considered as conductive paths, as shown in Figure 36. The heat generates from the current flow through the conductive paths may facilitate the breakdown process in this case.



(a)

Figure 35. Current as a function of stress time of samples fabricated with PDA in (a) nitrogen and (b) oxygen. Inset: Photos at various stress time.



(b)

Figure 35. Continued.

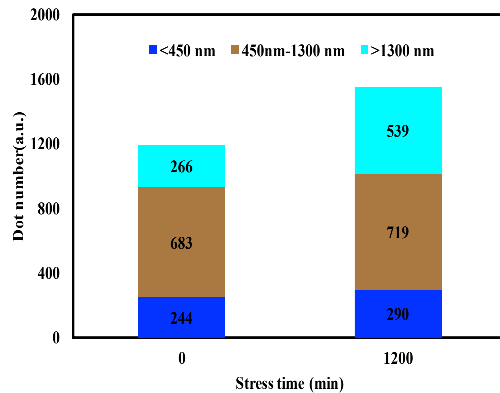


Figure 36. Dot number counted from light photos of samples prepared with PDA in oxygen at various stressed time.

Figure 37 shows the normalized emission spectra of WO_x embedded ZrHfO samples with nitrogen and oxygen PDA procedure. The continuous emission spectrum covers wavelength from 400 nm to 800 nm with the peak at 671 nm and 630 nm for nitrogen and oxygen annealed SSI-LEDs, respectively. The continuous emission spectrum is similar to the black-body radiation, but different from the conventional LED which has narrow spectrum corresponding to the photon energy released from electron-hole recombination. Assuming the black body radiation condition, the color correlated temperature (CCT) can be estimated from the following Wien' s equation:

$$T\lambda_{peak} = 2.898\times10^{-3} \qquad [10]$$

, where T is the temperature in Kelvin and λ_{peak} is the peak wavelength in nm. The CCT calculated from the corresponding peak wavelength are 4691 K and 4307 K for the WO_x embedded ZrHfO sample applied with PDA in O_2 and N_2 atmosphere, respectively. The enhanced temperature of WO_x embedded ZrHfO sample with PDA in O_2 atmosphere is consistent with the higer resistance listed in Table 6. The peak shift may induce from the composition difference in conductive paths.

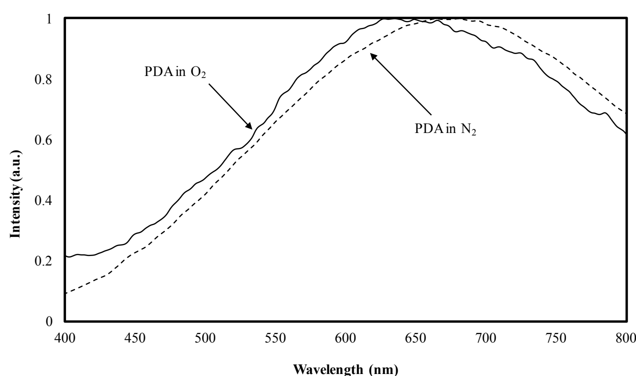


Figure 37. Emission spectra of WO_x embedded ZrHfO samples. Dashed line: sample with PDA in nitrogen. Solid line: sample with PDA in oxygen.

6.5 Summary

The electrical and optical properties of the WO_x embedded ZrHfO high-*k* MOS capacitors prepared with various PDA atmosphere were studied. Before the dielectric breakdown, both of the device show the typical capacitor behavior. While applying the gate voltage with the magnitude larger than breakdown voltage, they emit the light. From *C-V* characteristic curves, the oxygen annealing process works efficiently on reducing the charge trapping defective sites than the nitrogen annealing does. It directly affects not only on the electrical properties but also on the light emission characteristics of the SSI-LED. By passivating the charged oxygen vacancies through the oxygen annealing in furnace, the effectively lowered gate leakage current is obtained, and therefore it can avoid the SSI-LED degradation within the limited time span. In addition, the larger amount of conductive paths that can emit the broad band visible light is observed in the oxygen annealed device. The WO_x embedded ZrHfO high-*k* MOS device fabricated with PDA in

oxygen atmosphere demonstrates the good dielectric characteristics, as well as the excellent optical properties after dielectric breakdown.

CHAPTER VII

COMPARISON OF THREE KINDS OF HIGH-*K* BASED SSI-LEDS

7.1 Introduction

The broad band light emitting from the high-*k* based MOS capacitor was reported and named as SSI-LED.[17-20, 22] Various high-*k* dielectric materials, such as zirconium doped hafnium oxide (ZrHfO), tungsten oxide (WO_x), and 3 layer WO_x embedded ZrHfO, have been utilized in SSI-LED and performed a high quality as discussed in previous chapter. In this chapter, the electrical properties and light emission characteristics of three devices have been discussed.

7.2 Experimental

MOS capacitors were prepared on a DHF pre-cleaned *p*-type <100> silicon (10^{15} cm^{-3}) wafer in this chapter. For the zirconium hafnium oxide (ZrHfO) based device, the gate dielectric was sputter-deposited from the Zr/Hf (12/88 wt%) target in Ar/O_2 (100:100 sccm) at 5 mTorr and 60 W for 12 min. On the other hand, the tungsten oxide (WO_x) based sample, the tungsten target (99.999 %) served as deposition source and was sputtered in Ar/O_2 (40:100 sccm) at 60 W for 12 min. As for the WO_x embedded ZrHfO sample, ZrHfO and WO_x were deposited alternately layer by layer, and therefore the high-*k* stack consisted of four layers of ZrHfO and three layers of WO_x. After deposition, a post-

deposition annealing (PDA) step was conducted at 900˚C in O_2 atmosphere for 5 min in furnace. An 80 nm thick ITO was then deposited by RF-sputtering, and wet etched into 300 μm diameter round gate electrode with aqua regia solution. The Al thin film was deposited under Ar (100 sccm) atmosphere at 5 mTorr and 80W for 40 min as backside electrode for the purpose of forming ohmic contact. The post-metal annealing (PMA) step was carried out at 400˚C under forming gas (H_2/N_2 10/90) for 5 min. Annealing temperature stated here were demonstrated on the digital panel of furnace tube, which might be higher than the actual thermal equilibrium temperature inside of the furnace. The *C-V*, *J-V*, and OES measurements were performed by the same system introduced in Chapter II.

7.3 Electrical Properties Characterization

Figure 38 shows the *C-V* curves of the ZrHfO, WO_x, and WO_x embedded ZrHfO devices with V_g swept from -4 V in accumulation to +4 V in inversion and back to -4 V for hysteresis measurement at 1 MHz. The coefficients including EOT, D_{it}, Q_{ot}, V_{FB}, and ΔV_{FB}, extracted from the *C-V* curves are shown in Table 7. All of the device show the very small *C-V* hysteresis window. The highest D_{it} of WO_x SSI-LED can arise from the unsaturated W bonds near the insulator/semiconductor imperfect interface. On the other hand, the WO_x embedded ZrHfO device has the largest Q_{ot} value, which indicates the WO_x embedded layer increases the charge trapping capability of the bulk oxide layer. Moreover, the inclusion of three WO_x layer in the high-*k* stack should increase the physical thickness

as well as increasing EOT; however, calculated from capacitance in accumulation, the EOT of WO_x embedded ZrHfO device is lower than that of pure ZrHfO capacitor. It was reported that the embedding of CdS layer could suppress the the growth of HfSiOx interface layer since the oxygen diffusion to ZrHfO/Si interface is hindered. Therefore, the reduced of EOT value may also attribute to the inclusion of WO_x which inhibits the oxygen diffusion.

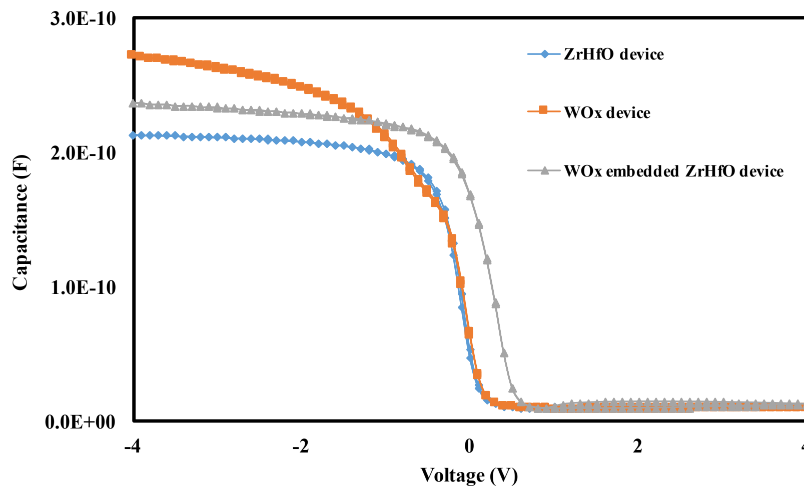


Figure 38. *C-V* hysteresis curves of ZrHfO, WO_x, WO_x embedded ZrHfO samples with diameter of 300 μm.

Table 7. Coefficients calculated from *C-V* hysteresis curves of ZrHfO, WO_x, WO_x embedded ZrHfO MOS capacitors.

Oxide material	C_{ox} (F)	EOT (nm)	D_{it} ($cm^{-2}eV^{-1}$)	Q_{ot} (cm^{-2})	V_{FB} (forward) (V)	V_{FB} (backward) (V)	ΔV_{FB} (V)
ZrHfO	2.14×10^{-10}	11.4	9.57×10^{10}	1.49×10^{11}	0.1	0.09	0.011
WO_x	2.71×10^{-10}	8.99	4.79×10^{12}	2.66×10^{11}	0.129	0.134	0.005
WO_x embedded ZrHfO	2.73×10^{-10}	10.3	2.84×10^{10}	9.81×10^{11}	0.49	0.49	0.001

Figure 39 shows *J-V* curves of the ZrHfO and WO_x embedded ZrHfO samples of 300 µm diameter with the gate voltage V_g being swept from 0 V to -15 V. For both of the samples, the *J-V* curves show two stage behavior before the breakdown takes place. Previously, it was suggested that the mechanism of charge transfer through the ZrHfO high-k stack following the Schottky emission (SE) at low electrical field and then the Poole-Frenkel (P-F) mechanism at the high electrical field.[77-78] The SE and P-F equations are expressed as:

$$(SE) \quad J = A^{*}\times T^{2}\exp\left[\frac{-q(\Phi_B-\sqrt{qV/4\pi\varepsilon d}}{kT}\right] \qquad [11]$$

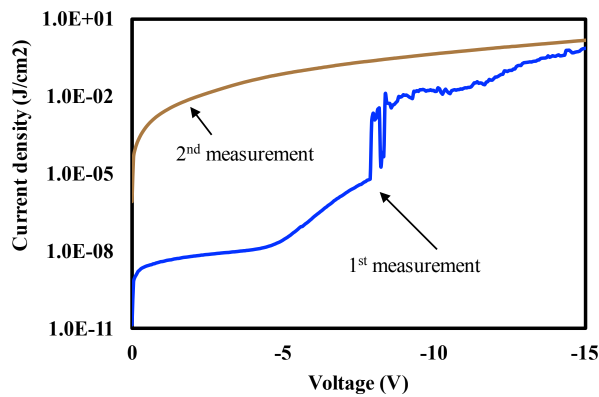
$$(P-F) \quad J\sim V\times\exp\left[\frac{-q(\Phi_B-\sqrt{qV/\pi\varepsilon d}}{kT}\right] \qquad [12]$$

where *J* is the emission current density, *T* is the temperature, *d* is the dielectric thickness, *V* is the applied voltage, *ε* is the insulator dynamic permittivity, Φ_B is the barrier height, m^* is the carrier effective mass, k is the Boltzmann constant, and A^* is the effective

Richardson constant. The fist measurement curves in Figure 39(a), (b) and (c) were redrawn into the SE and P-F fitting plots, as shown in Figure 39 (d) and (e).[77-78] All the samples fit well at the low electric field regime while the P-F relation is suitable in the high electric field regime. It was consistent with the literature report that the SE, also called as field enhanced thermionic emission, is relatively accurate for low electric field strength, while the P-F emission describes the electron transport in a large electric field.[79-80] As shown in Figure 39(d), the y-axis interception of ZrHfO, WO_x, and WO_x embedded ZrHfO SSI-LEDs are -31.68, -28.69, and -32.82, respectively. The WO_x sample has the lowest effective barrier height between the metal gate and the underneath high-*k* dielectric layer, and in addition, the similar y-axis interception value of ZrHfO and WO_x embedded ZrHfO samples indicates that the ITO/ZrHfO interface properties is not much influenced by the inclusion of thin WO_x embedded layer.[81] In the high electric field strength regime, the current transport is dominated by P-F emission mechanism that involves Coulomb attraction between charged trap states and the emitted ions besides external electric field.[55] The y-axis interception, i.e., implying the P-F barrier height, of ZrHfO, WO_x, and WO_x embedded ZrHfO SSI-LEDs are –38.54, -39.58, and -55.22, respectively. This means that inclusion of WO_x in ZrHfO affects the bulk conduction since the energy depths of traps contributed to the P-F conduction is increased.[55, 78]

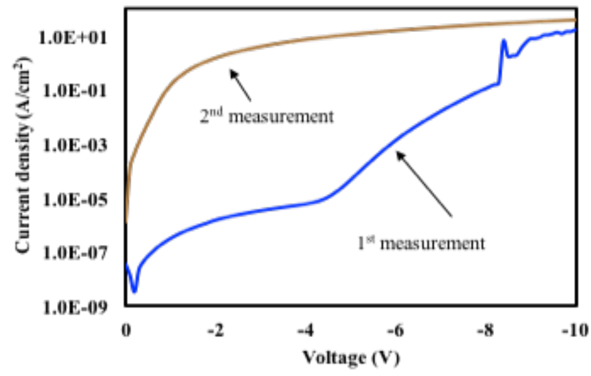
The increasing amount of holes are injected into the dielectric stacks with the increase of $|-V_g|$, and eventually it leads to the hard electrical breakdown at breakdown voltage as the sudden jump of leakage current density shown in the 1st measurement.[60] Then, the nanoresistors served as conductive passage form permanently through interfacial layer and

bulk oxide.[55] As shown in Table 8, the leakage current density measured at -1 V in 1st measurement of three samples are small, while the largest magnitude of WO_x sample indicates that the WO_x thin film is not as insulating as ZrHfO is to suppress gate leakage current. Through introducing multilayer deposition method, the high leakage current density can be effectively decreased. Moreover, the resistance calculated from the 2nd measurement of WO_x embedded ZrHfO SSI-LED implies that the device is able to generate most heat and thus the light in shorter wavelength.

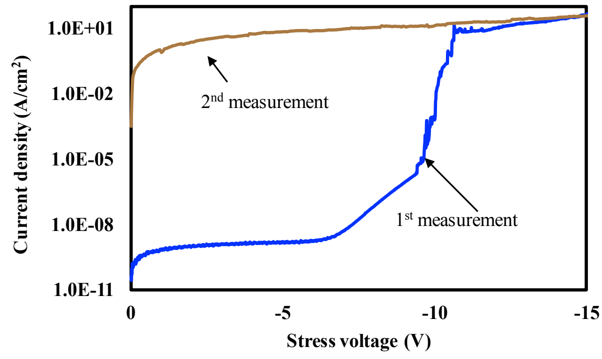


(a)

Figure 39. *J-V* curves of (a) ZrHfO, (b) WO_x and (c) WO_x embedded ZrHfO samples of 300 µm diameter. (d) Schottky emission and (e) Poole-Frenkel fitting curves of ZrHfO, WO_x, WO_x embedded ZrHfO SSI-LEDs.

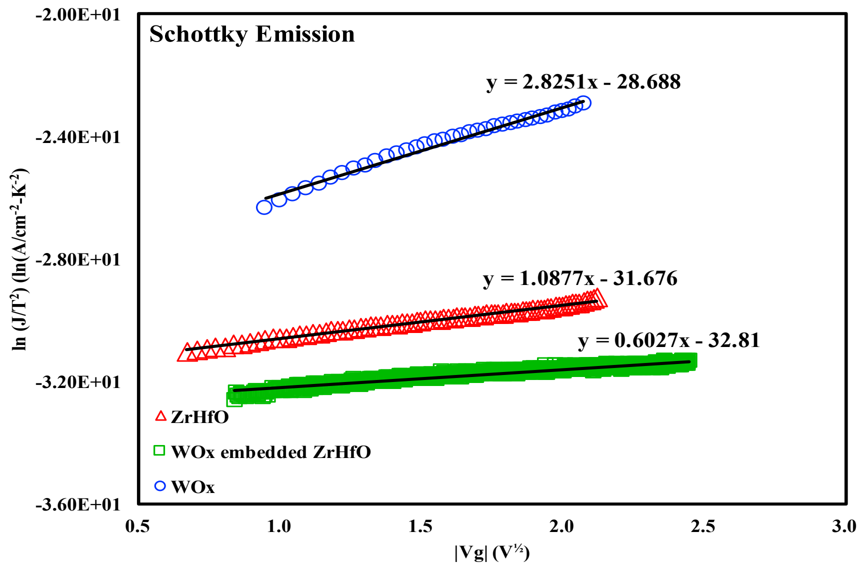


(b)

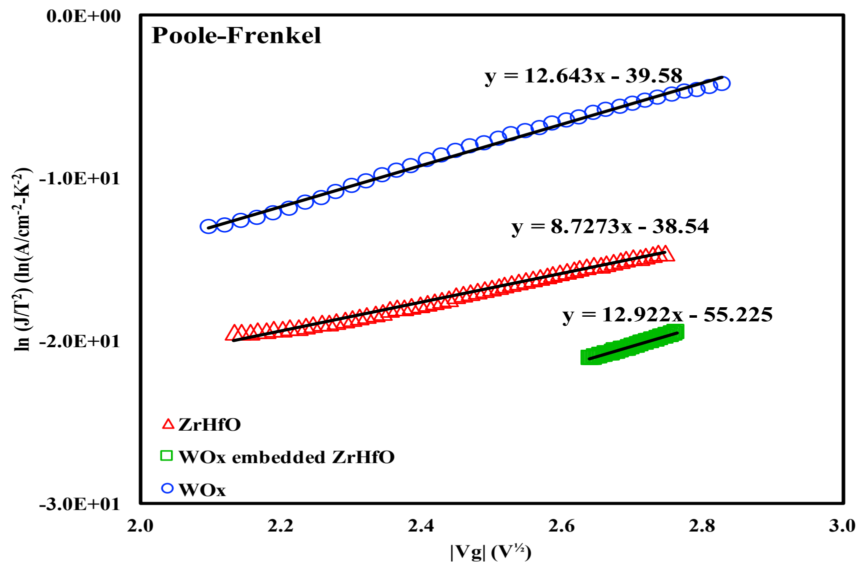


(c)

Figure 39. Continued.



(d)



(e)

Figure 39. Continued.

Table 8. Coefficients calculated from *J-V* curves of ZrHfO, WO_x, WO_x embedded ZrHfO capacitors.

Oxide material	ZrHfO	WO_x	WO_x embedded ZrHfO
V_{BD} (V)	-7.9	-8.4	-9.68
Leakage current density (J/cm^2) at -1 V	-3.89×10^{-9}	-3.47×10^{-7}	-7.63×10^{-9}
Resistance (Ω)	962.39	385.15	1192.7

7.4 Optical Properties Characterization

Figure 40 shows the high magnification photos of ZrHfO, WO_x embedded ZrHfO, and WO_x samples with gate electrode of 300 µm diameter. The discrete bright dots are formed permanently after breakdown. The number of bright dots in the WO_x embedded ZrHfO is larger than those in the others. From Figure 41(a) and (c), the number density of dot is increased with the embedding WO_x in the high-*k* stacks, which is consistent with the resistance listed in Table 8. Although WO_x sample has the lowest resistance, it can still emit the bright light, which may be explained by the composition difference, e.g., large amount of high emissivity W component involved in the conductive path. In addition, the ZrHfO based two SSI-LEDs show the more uniformly distributed light emission pattern than WO_x device does. Figure 41 shows the current vs. stress time curves of the ZrHfO, WO_x, and WO_x embedded ZrHfO samples, separately. All of them do not show the degradation phenomenon within the operation time, and furthermore, the current increase with stress time. The increase of current is from the new nanoresistor formation which

may be facilitated by the enhanced device temperature during the application of electric field.

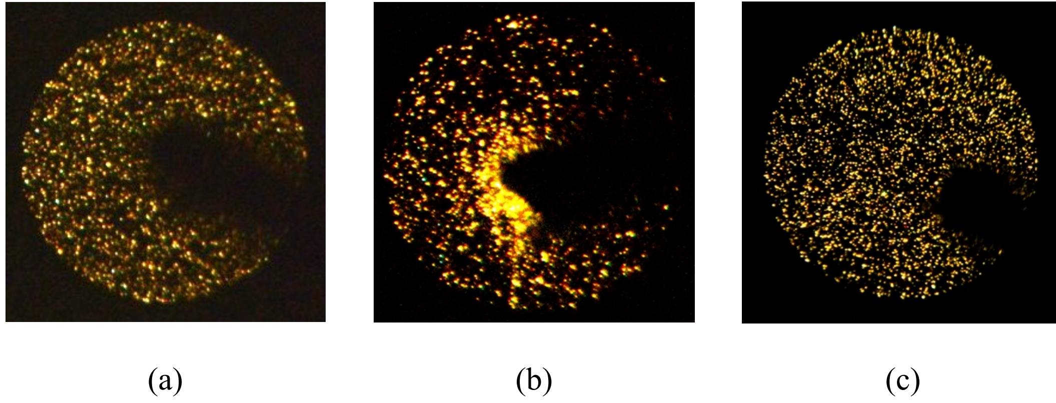
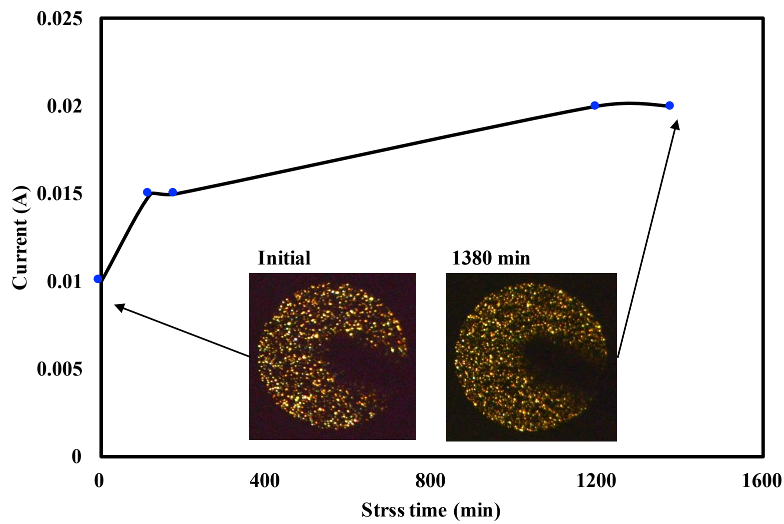
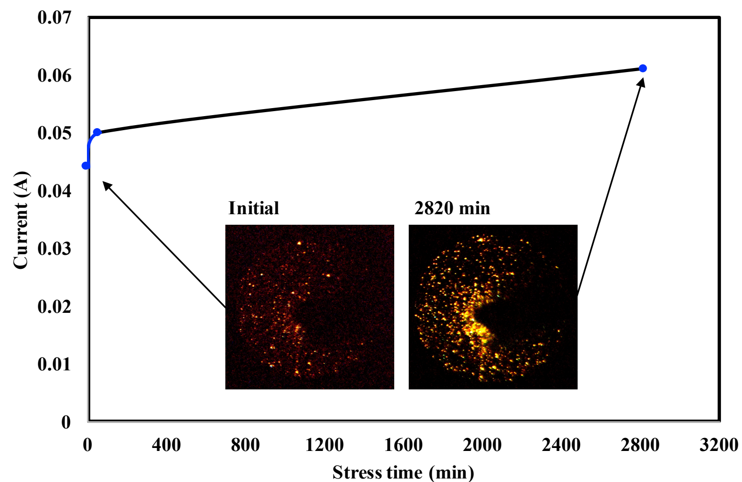


Figure 40. Photos of (a) ZrHfO, (b) WO_x and (c) WO_x embedded ZrHfO SSI-LEDs. All samples: 300 µm diameter.

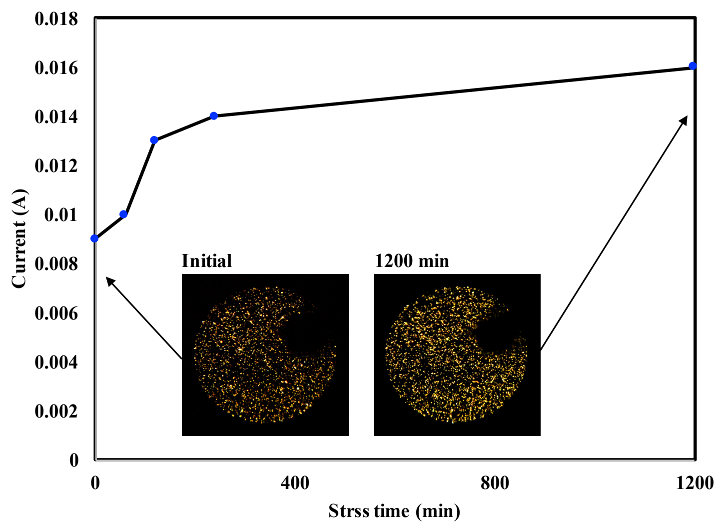


(a)

Figure 41. Current as a function of stress time of (a) ZrHfO, (b) WO_x embedded ZrHfO, and (c) WO_x samples. Inset: Photos at various stress time.



(b)



(c)

Figure 41. Continued.

Figure 42 shows the distribution of light dot diameters of ZrHfO, WO_x, and WO_x embedded ZrHfO samples formed at various stress time, and the dots were counted by ImageJ. The light dots grow in size and number with stress time, which can be explained

through the breakdown mechanism promoted by escalating temperature of whole device during the application of voltage. Figure 43 shows the total number of bright dots scattered on ITO gate of various device counted from high magnification photo. The WO_x embedded ZrHfO sample prepared with oxygen PDA achieves the largest amount of bright dots among three SSI-LEDs. Moreover, comparing to previously done research where the WO_x has been prepared in shorter deposition time and with nitrogen PDA[82], the device is more capable to form more bright dots, i.e., nanoresistors, has been achieved.

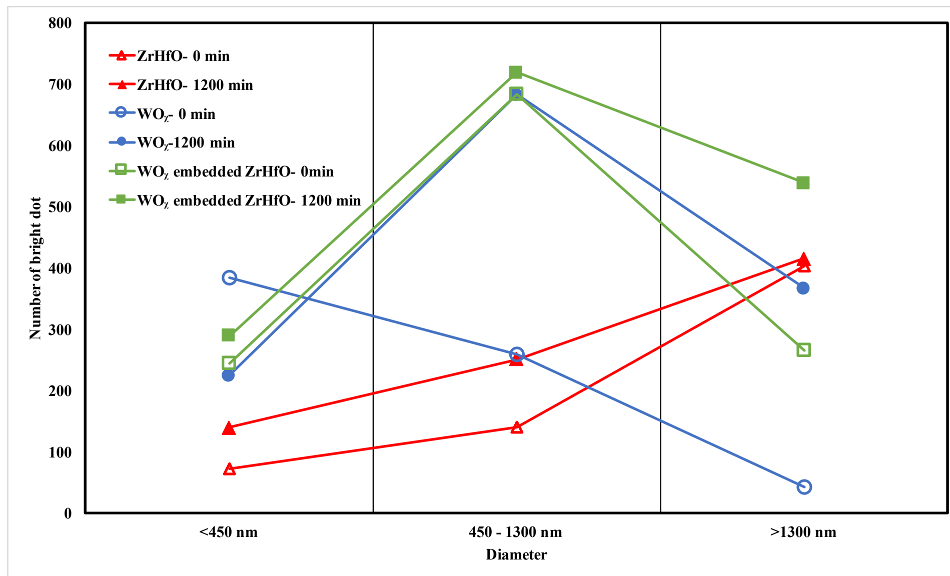


Figure 42. Distributions of light dot diameters of (a) ZrHfO, (b) WO_x, and (c) WO_x embedded ZrHfO samples formed after stressed for various time.

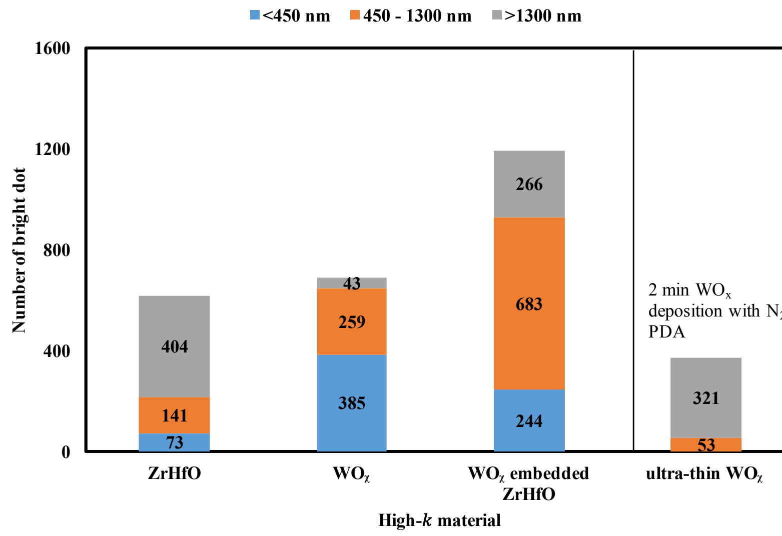


Figure 43. Total number of bright dots distributed in ZrHfO, WO_x, WO_x embedded ZrHfO, and ultra-thin WO_x[82] based SSI-LEDs.

Figure 44 shows the emission spectra of SSI-LEDs with ZrHfO, WO_x, WO_x embedded ZrHfO high-*k* stack. All samples emit broad band light spanning from near UV to infrared wavelength. The continuous spectrum is similar to the solar spectrum, i.e. black body radiation, in the visible wavelength region except the λ_{peak} locations, i.e. 638 nm, 687.15 nm and 663 nm for ZrHfO, WO_x, WO_x embedded ZrHfO devices, respectively. The strongest light emission intensity of WO_x SSI-LED is observed. Since the real materials emit energy at a fraction, e.g. emissivity, of black body energy levels, with the higher emissivity coefficient, the material can emit more thermal radiative energy as other grey body at the same temperature. It was suggested that the hemispherical emissivity of 99.99 % pure tungsten and hafnium-3 wt% zirconium are 0.434[83] and 0.30[84] at 2000 K,

respectively. Therefore, the inclusion of W component in conductive path may increase the light emission intensity of SSI-LED.

Figure 45 shows the CIE chromaticity chart according to the emission spectra of the SSI-LEDs in Figure 44, and the CCT and CRI were calculated correspondingly are listed in Table 9. All samples have high CRI R_a's, i.e. 96-98, which are close to that of the incandescent bulb based on black body emission due to the small distance between CCT and Planckian locus in chromaticity diagram. In addition, the CCT value of ZrHfO, WO_x, and WO_x embedded ZrHfO SSI-LED are 4333 K, 3956 K and 3850 K, respectively. With the inclusion of tungsten oxide component, the CCT decreases, meaning that the device appears to be warmer white light, i.e. containing more red right, and is closer to that of conventional incandescent bulb (2800 K). Containing more red light makes the SSI-LED useful with respect to reproduce the natural and vivid colors of objects in future application.

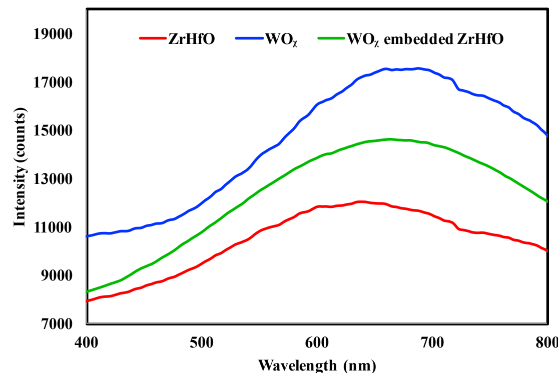


Figure 44. Light emission spectra of ZrHfO, WO_x, and WO_x embedded ZrHfO SSI-LEDs.

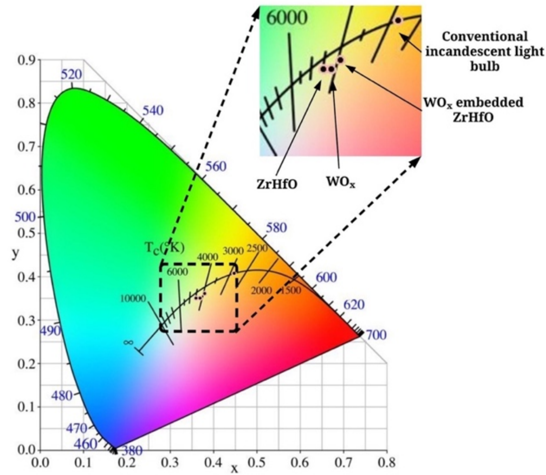


Figure 45. Color coordinates of ZrHfO, WO_x, and WO_x embedded ZrHfO SSI-LEDs in the CIE chromaticity chart. Color coordinate of the incandescent bulb is included for reference.

Table 9. The CIE color coordinates, CCT, and CRI of the ZrHfO, WO_x, and WO_x embedded ZrHfO SSI-LEDs.

High-*k* material	CIE x	CIE y	CCT (K)	CRI R_a
ZrHfO	0.36	0.351	4333	98
WO_x	0.37	0.351	3956	96
WO_x embedded ZrHfO	0.378	0.362	3850	98

7.5 Summary

In this chapter, the comparison of three devices has been investigated with respect to the *C-V*, *J-V*, and light emission pattern. Since the WO_x high-*k* bulk has a higher defect densities and higher leakage current comparing to the dielectric properties of ZrHfO device, the embedding of WO_x in ZrHfO stack shows the intermediate characteristics, i.e. lower the D_{it} and leakage current. In addition, the WOx embedded ZrHfO SSI-LED enable the uniform light emission, long operation time, and large number of bright dots, which makes it a desired device. Also, with the lower CCT (3850 K) and high CRI (98), the WO_x embedded ZrHfO device appears to be more redish-white than pure ZrHfO SSI-LED, which is closer to the performance of conventional tungsten incandescent light.

CHAPTER VIII

SUMMARY AND CONCLUSIONS

The electrical properties, optical properties, light emission characteristics of the SSI-LED made from ZrHfO, WO_x, and WO_x embedded ZrHfO high-*k* based MOS devices were explored in this thesis. All of the samples were RF sputtered-deposited on *p*-type silicon substrate, and thermal annealed in furnace tube afterwards in order to improve the quality. Several measurements, e.g., *C-V*, *J-V*, for electrical characteristics, and emission spectrum, high-magnification photo for optical characteristics, were utilized to study the device.

At first, the molybdenum and aluminum gate effect on the MOS capacitor has been studied. When it comes to the light emission application, ITO material served as transparent electrode let the light emitting out from high-*k* layer. On the other hand, the type of high-*k* stack, and parameters used in fabrication process play an important role for the device performance. Thus the ZrHfO, WO_x embedded ZrHfO, WO_x based MOS capacitors prepared with nitrogen or oxygen post-deposition annealing have been investigated. Besides, the device in small dimension can be easily subjected to operating environment, and hence the environmental factors such as humidity and temperature affecting electrical properties have been discussed.

The molybdenum and copper gated ZrHfO based high-*k* MOS capacitors fabricated with the thermal annealing procedure have been studied for the device properties. The capacitance in accumulation and the number of oxide charge trapping center which might

be induced from the long sputter deposition time and was calculated from the *C-V* curves of Mo gated device was improved through the post-metal deposition thermal annealing (PMA) treatment because of the reduction defective sites in the dielectric layer, while the capacitor characteristic of Cu gated device was degraded after the PMA treatment due to the metal diffusion into the dielectric layer. Therefore, the PMA procedure had a strong impact on the performance of the capacitor by affecting the reaction between the gate and the high-*k* gate dielectric and the removal of defects in the film and at the interface as well. Then, the light emission from the three types of high-*k* stack on the *p*-type Si wafer was introduced. The SSI-LED can be obtained from the high-*k* based MOS capacitor after the dielectric breakdown. When the negative gate voltage was applied on the gate electrode providing an external electric field, the holes were able to overcome the energy barrier between silicon substrate and oxide layer, and the defects in the bulk oxide were generated accordingly. The hard breakdown in dielectric layer took place since the defects connected together, and the conductive path formed afterwards allowing the passage of current. In other words, the conductive path could be viewed as a nanoresistor which existing in the interfacial and dielectric layer was able to generate light by thermal excitation mechanism. Due to the thermal excitation mechanism, the broad-band light emission spectrum is similar to black body radiation rather than electron-hole recombination mechanism of the conventional LED. The selection of dielectric material, the quality of interface, the thickness of high-*k* layer, magnitude of gate voltage, and the leakage current are factors affecting the light emission properties including shape, spectrum span, peak wavelength, etc. The WO_x embedded ZrHfO multilayered MOS capacitor was fabricated and analyzed

with respect to electrical and optical properties comparing to those of pure ZrHfO and pure WO_x based MOS capacitors. The defective sites in both bulk oxide and Si-oxide interface were raised from the embedding WO_x, while the small hysteresis window, i.e., ΔV_{FB} = 0.031 V, was observed. The higher defect density favors the breakdown mechanism, and thus the breakdown voltage decreased. The inclusion of WO_x layer also induced larger leakage current compared to the ZrHfO sample, which caused the brighter emission. The emission spectrum of WO_x embedded ZrHfO sample including the visible and near IR wavelengths was similar to the warm white light emitting from ZrHfO sample. Even though the embedding of WO_x increased the light intensity, the higher defect density caused shorter life-time and facilitated the Si diffusing through the whole stack to ITO layer, which led to the degradation in long wavelength region of emission spectrum. To refine the device, the oxygen annealing process (PDA) effect on the electrical and optical properties of the device has been investigated. The interface quality was improved since the defective sites were removed by oxygen annealing, and the EOT was increased due to the thickened interface layer. Thus, the longer life time comparing to the sample treated with nitrogen annealing was reached. Also, the larger number density of light dots was increased through the oxygen annealing.

The temperature, humidity, and size effects on resistance of the ZrHfO based MOS capacitor have been investigated. The resistance was calculated from the linear part of *I-V* curves, and it decreased with the increase of electrode size. It was because the more nanoresistors are formed in the device with larger electrode under same external electric field applied. The resistance also increased with the increase of the temperature. In the

low gate voltage range, the current response to voltage was sensitive to the Schottky barrier height which enhanced with the increase of the temperature. The sample was annealed under 80 % relative humidity and 80˚C for various time periods in order to study the temperature and humidity impact on resistance. The water molecules diffused into device was ionized when the strong electric field was applied. Consequently, induced electrons and hydroxyl ions which acted as charge carriers led to the decrease of resistance at the long annealing time.

Chapter III focuses on the material gated effect on the MOS capacitor. Since the heating treatment included in fabrication process, the reaction between the gate and the high-*k* layer makes the selection of gate material become crucial. Next, the SSI-LED consisting of three kinds of high-k stacks, e.g. ZrHfO, WO_x, WO_x embedded ZrHfO, have been studied. With the similar structure, the electrical properties of high-k based MOS capacitor are investigated to achieve good light emitting properties. In Chapter IV, V, VI, the three SSI-LEDs have been discussed with respect to the electrical properties, i.e. *C-V*, *J-V* and breakdown characteristics, optical properties, and the PDA ambient effect. The oxygen PDA step effectively decreases the defective sites in ZrHfO and WO_x embedded ZrHfO device by removing oxygen vacancies and passivation of interface dangling bonds. Therefore, the dielectric breakdown, leakage current, and resistance are affected. Moreover, the comparison of three SSI-LEDs with respect to dielectric properties, charge transfer mechanism, light emission intensity and light chromaticity have been discussed in Chapter VII. The ZrHfO SSI-LED has the least leakage current and defective sites while it emits the light of lower intensity. On the other hand, the high emission intensity has

been observed in WO_x device due to the larger emissivity of tungsten; however, it has the higher defect density which leads to the large leakage current. By embedding WO_x layer into ZrHfO bulk oxide, the warm-light emitting device, i.e. with low CCT and high CRI, that can improve the light intensity and also preserve low leakage current density has been achieved.

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