# ULTRA-LOW QUIESCENT CURRENT, FAST SETTLING CAPACITOR-LESS LOW DROPOUT REGULATOR

A Thesis

by

ROHIT BUPATHY SUDAN

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

| | |
|---|---|
| Chair of Committee, | Aydin I. Karsilayan |
| Co-Chair of Committee, | Jose Silva-Martinez |
| Committee Members, | Gwan Choi |
| | Duncan Henry M.Walker |
| Head of Department, | Miroslav Begovic |

August 2020

Major Subject: Electrical Engineering

## ABSTRACT

A $220\,nA$ ultra-low quiescent bias current capacitor-less low drop-out (CL-LDO) regulator with improved single transistor control (STC) and adaptive transformation is presented in this thesis. The STC-LDO handles light load currents $(0-20\,\mu A)$, whereas the adaptive transformation to 2-stage structure handles medium load currents $(20\,\mu A-5\,mA)$, and subsequent transformation of the LDO to a 3-stage structure handles high load currents $(5\,mA-100\,mA)$. The LDO provides a 0.9 V output voltage and can regulate up to a maximum of 100 mA from a power supply of 1.1 V. Complete load current range $(0-100\,mA)$ stability is achieved at a maximum load parasitic capacitance of $100\,pF$. For a rising load current transient $(0\,-\,100\,mA)$, the LDO achieves a recovery time of 101 ns, and an undershoot of 292 mV is observed at the output. For falling load current transient $(100\,mA\,-\,0)$, the LDO achieves a recovery time of 354 ns, and an overshoot of 42 mV is observed at the output. The structural transformation proposed in this thesis significantly improves the recovery time of CL-LDO, enabling fast transient response even under ultra-low quiescent bias current of $220\,nA$.

# DEDICATION

To my wonderful parents and my loving brother.

# ACKNOWLEDGMENTS

I would like to express my sincere appreciation to my research advisor Professor Aydin I. Karsilayan from the Department of Electrical and Computer Engineering, Texas A&M for supporting and guiding me throughout this research.

CONTRIBUTORS AND FUNDING SOURCES

## Contributors

This work was supervised by a thesis committee consisting of Professor Aydin I. Karsilayan [advisor], Professor Jose Silva-Martinez and Professor Gwan Choi of the Department of Electrical and Computer Engineering, and Professor Duncan Henry M.Walker of Department of Computer Science and Engineering.

All other work conducted for the thesis was completed by the student independently.

## Funding Sources

No outside funding was received for the research and writing of this document.

# NOMENCLATURE

| | |
|---|---|
| CL-LDO | Capacitor Less Low Drop-out |
| DOVSR | Distributed Overshoot Reduction Circuitry |
| ESR | Equivalent Series Resistance |
| FOM | Figure-of-Merit |
| FVF | Flipped Voltage Follower |
| GBW | Gain Bandwidth product |
| GM | Gain Margin |
| HP-LDO | High Power Low Drop-out |
| IoT | Internet of Things |
| LDO | Low Drop-out |
| LHP | Left Half Plane |
| LP-LDO | Low Power Low Drop-out |
| PM | Phase Margin |
| PSRR | Power Supply Rejection Ratio |
| PVT | Process, Voltage and Temperature |
| RHP | Right Half Plane |
| SoC | System-on-Chip |
| STC | Single Transistor Control |

TABLE OF CONTENTS

Page

LIST OF FIGURES

FIGURE Page

# LIST OF TABLES

TABLE Page

# 1. INTRODUCTION AND BACKGROUND

## 1.1 Introduction

Internet of Things (IoT) is considered to be the third revolution in computing, with the first revolution bringing computing to government and companies, the second revolution bringing computing to the public in the form of desktops, laptops, smartphones, etc. Tiny chips with sensors will now enable billions of devices around the globe that are connected to the internet, collecting and sharing data. These chips are expected to function entirely on a battery, and the operating life of a battery is given by

$$Battery\ Life = \frac{Battery\ Capacity}{Average\ Load\ Current} \tag{1.1}$$

Decreasing the average load current consumed by the application increases battery life. Making the device sleep longer also extends battery life, but with performance trade-offs. A technology that extends battery life without affecting performance (power management) becomes key in such ultra-low-power applications.

Fig. 1.1 shows the components of a typical IoT front-end hardware layer. The power management unit (PMU), an important part of the IoT System-on-Chip (SoC), has to deliver the necessary power to various blocks in an energy-aware methodology. Ultra-low-power operation is achieved in such SoCs where the system periodically wakes up, captures, and processes sensor data and subsequently goes back to sleep mode. Typically, being idle for the majority of the time, these systems are configured into standby mode. The expectation in such a system is that the PMU should hold the output voltage to the desired value with minimum power consumption.

Typically, LDO is the ideal PMU of choice for sensitive analog and mixed-signal circuits. With ultra-low power applications becoming prominent, the low quiescent power and fast wake-up feature of CL-LDOs can be leveraged in systems that require multiple power supply to power up individual local blocks. Such low power, fast wake-up CL-LDOs face the traditional design

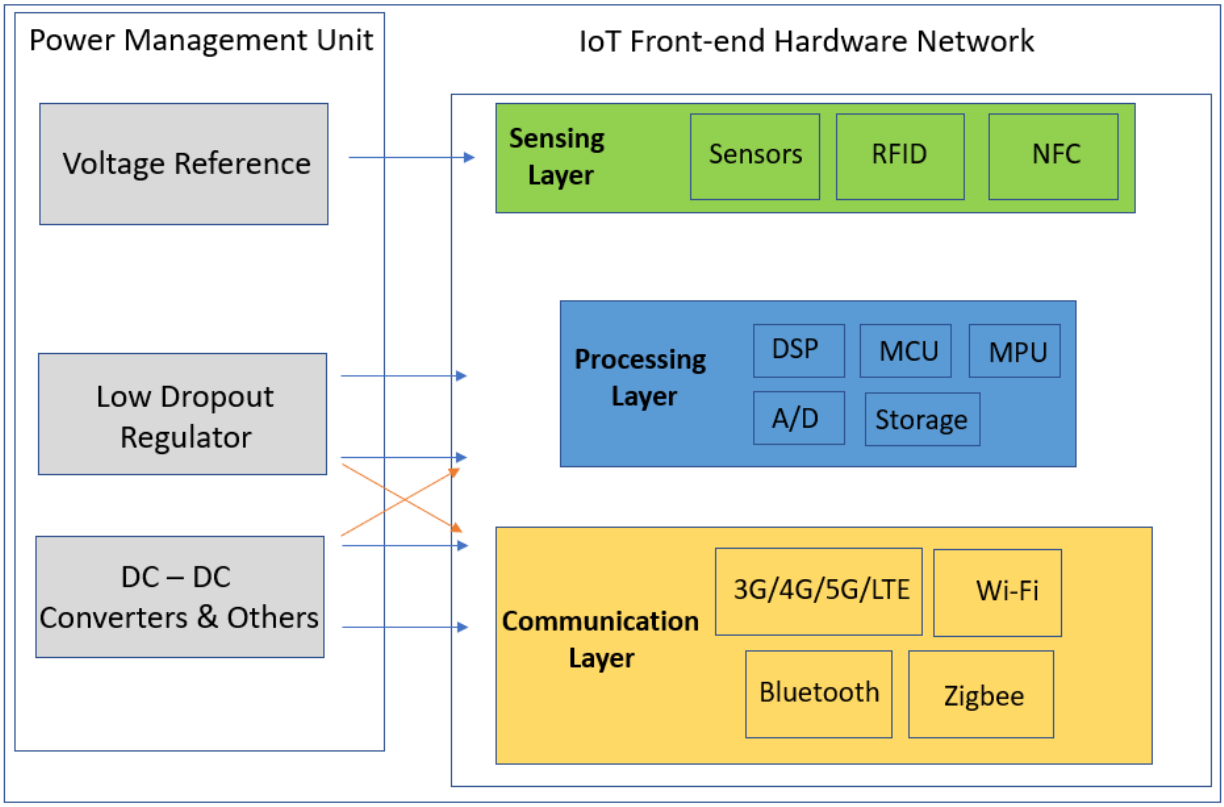


Figure 1.1: IoT interface Soc block diagram[1]

trade-offs were reducing the current consumption to sub 1-$\mu$A level compromises transient related figures of merit (FOM) as illustrated in Fig. 1.2. Additionally, providing loop stability for complete load current range becomes a key design issue, which needs to be handled at the circuit level with different frequency compensation schemes. This thesis addresses the above-stated design trade-off with the adaptive structural transformation between STC-LDO, 2-stage, and 3-stage cascaded topologies in CL-LDOs.

## 1.2 Background

Fig. 1.3 shows the typical block diagram of an LDO. It consists of a PMOS pass gate (power stage) to supply the necessary load current, $R_1$ and $R_2$ feedback resistors to scale the output voltage for comparison with $V_{REF}$. The error amplifier compares $V_{REF}$ with $V_{FB}$ and adjusts the pass gate voltage to supply the desired current demanded by the load whilst maintaining the output voltage

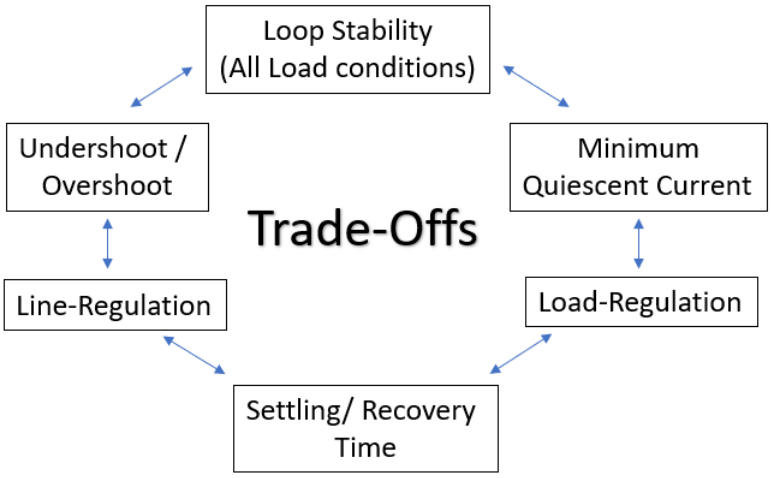


Figure 1.2: Design trade-offs in CL-LDOs

to

$$V_{OUT} = V_{REF}\left(1 + \frac{R_1}{R_2}\right) \tag{1.2}$$

### 1.2.1 Relevant Performance Metrics

Fig. 1.4 shows the typical circuit setup of LDO. The circuit in Fig. 1.4 will be used to introduce performance metrics that are widely used for the comparison in different CL-LDO topologies.

#### *1.2.1.1 Drop-out Voltage, Quiescent Current and Current Efficiency*

Drop-out voltage $(V_{DO})$ is the input to output differential voltage at which the circuit ceases to regulate against further reductions in $V_{IN}$ [2]. $V_{DO}$ is given by

$$V_{DO} = V_{IN} - V_O \tag{1.3}$$

Quiescent or ground current $(I_Q)$ is the difference between the input $(I_{IN})$ and output current $(I_O)$ of the LDO, and is given by

$$I_Q = I_{IN} - I_O \tag{1.4}$$

At no-load condition $(I_L = 0$ and $I_O = 0)$ , $I_{IN}$ consumed by the LDO is equal to $I_Q$. $I_L$ is the

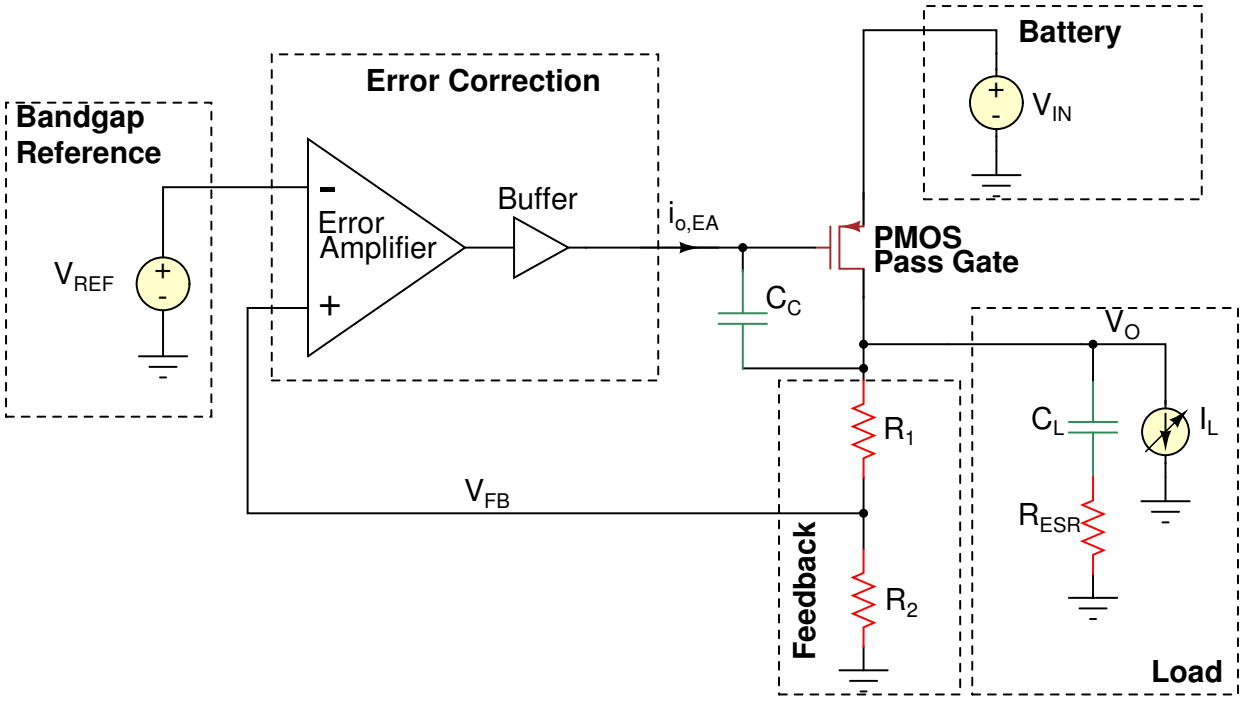


Figure 1.3: Typical block level view of an LDO

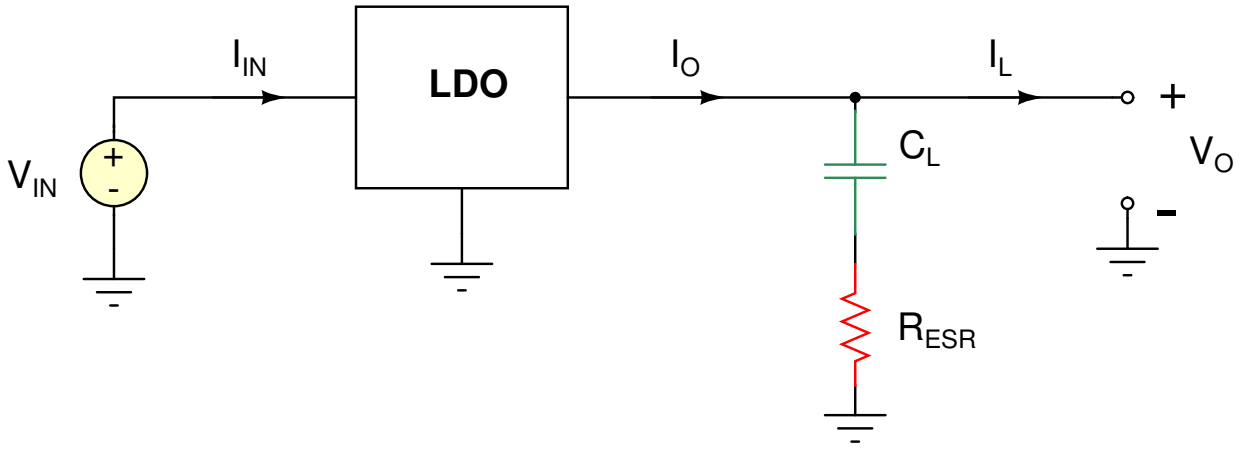


Figure 1.4: Typical circuit setup of an LDO

load current.

Current Efficiency $(\eta_I)$ is a measure of how efficient the LDO is in terms of power consumption

while regulating loads, and is given by

$$\eta_I = \frac{I_O}{I_{IN}} = \frac{I_O}{I_O + I_Q} \tag{1.5}$$

Generally, an increase in $I_Q$ of an LDO reduces current efficiency.

#### *1.2.1.2 Load and Line Regulation*

Steady-state output voltage variations resulting from DC load current changes is defined as the load regulation, and is given by

$$Load\ Regulation = \frac{\triangle V_O}{\triangle I_L} = \frac{R_{OL}}{1\ +\ \beta\ A_{EA}\ A_{PT}} \tag{1.6}$$

where $R_{OL}$, $\beta$, $A_{EA}$ and $A_{PT}$ is the open loop output resistance, is the feedback factor, is the gain of the error amplifier and is the gain of the pass transistor, respectively.

Steady state output voltage variations resulting from DC input voltage changes is defined as line regulation, and is given by

$$Line\ Regulation = \frac{\triangle V_O}{\triangle V_{IN}} = \frac{1}{\beta\ A_{EA}} \tag{1.7}$$

#### *1.2.1.3 Recovery Time*

The worst case recovery time $(t_R)$ of the LDO occurs when the load current varies from lowest value to maximum value or vice-versa. The delay associated with recovery has two major components, and is given by

$$t_R = t_{SR}\ +\ t_{BW} \tag{1.8}$$

where $t_{SR}$ is the delay associated with the slewing of the largest capacitor in the circuit (typically pass gate capacitance), and $t_{BW}$ is the delay associated with the finite bandwidth of the error

correction loop. The expression for $t_{SR}$ and $t_{BW}$ can be obtained from [3], and is given by

$$t_{SR} = \frac{C_p \ \triangle I_O}{g_{mp} \ \ i_{o,EA}} \tag{1.9}$$

$$t_{BW} = 4\,\tau = \frac{4}{2\pi f_{3dB}}(2\%\ settling\ error) \tag{1.10}$$

where $C_p$, $g_{mp}$, $i_{o,EA}$, $\triangle I_O$ and $f_{3dB}$ is the capacitance seen at the gate of PMOS pass transistor, is the small-signal transconductance of the PMOS pass transistor, is the maximum current that the error amplifier can supply in the event of a slew, is the change in the load current and is the small signal closed loop bandwidth associated with the LDO error control loop, respectively (see Fig. 1.3). From (1.8), (1.9) and (1.10) it can be seen that $t_R$ is directly propotional to $C_p$ and inversely propotional to $f_{3dB}$ and $i_{o,EA}$. $t_R$ can be reduced at the expense of reducing $C_p$ or increasing bias current.

### 1.3 Literature Review

In traditional LDOs, a large off-chip capacitor in the range of $\mu F$, along with an equivalent series resistance (ESR), is used to generate a left half-plane (LHP) zero, aiding in frequency compensation. This large capacitor also suppresses large overshoots and undershoots in the event of a fast load current transient. However, it is not practical to integrate such capacitors on-chip, which limits performance due to bond wire inductance and resistance, and increases printed circuit board area due to additional I/O pads needed for external connection. Therefore, capacitor-less LDOs (CL-LDO) have become popular for system-on-chip (SoC) applications [1], [4], [5]. In ultra-low quiescent current operation, the LDOs typically employ adaptive and dynamic biasing to boost the bandwidth, thereby aiming to improve transient figures of merit (FOM). Unfortunately, such multi-stage topologies encounter several challenges like increased settling time, degradation of phase margin (PM), and increased complexity of frequency compensation when the quiescent current is further reduced ($< 500\,nA$). Additionally, ESR zero available in traditional LDOs is not available in CL-LDOs, making frequency compensation at zero-load current even more challenging.

The CL-LDO in [6] consumes only 103 nA, but suffers from significant ringing and large settling time (400 $\mu$s). CL-LDO in [1] achieves loop stability at light load conditions ($I_L < 254\,\mu A$) using a combination of adaptive biasing and transistor degenerated compensation. As the quiescent current is pushed further lower, this topology, too, will fail as stability is dependent on the available quiescent bias current.

With the demand for SoC systems to move to a lower technology node with an additional push to further reduce the quiescent current consumption, the above-mentioned CL-LDO topologies would trade-off loop stability performance for loop gain, bandwidth, complexity, and other transient related FOMs.

The flipped voltage follower (FVF) structure from [5] addresses the above-stated problems. The main features that can be leveraged FVF structure in ultra-low bias conditions are their simple structure, eliminating the need for minimum load current, and improving stability at no-load conditions with competitive loop performance. The motivation of finding a topology that is stable at zero load current, independent of the available quiescent bias current and is competitive in terms of transient FOM, leads us into the FVF based adaptive biased structure with structural transformation proposed in this thesis.

### 1.4 Organization of the Thesis

Section 2 discusses the architecture proposed in this thesis. Section 3 provides an analysis of the circuit level implementation of the CL-LDO. Section 4 deals with the stability analysis of the CL-LDO across various load current ranges. Section 5 includes simulation results and compares its performance with the state-of-art CL-LDOs. Section 6 summarizes the research and includes conclusions drawn as a part of various design trade-offs. Appendix 1 includes process, temperature, and voltage (PVT) corner simulation results.

## 2. PROPOSED STRUCTURE

Fig. 2.1 shows the block diagram of the proposed LDO regulator structure. At light-load conditions ($I_L < 20\,\mu A$), single transistor control LDO (STC-LDO) regulator provides the necessary regulation, whereas the high-power LDO (HP-LDO) regulator is turned OFF. As the load current increases to moderate levels ($20\,\mu A < I_L < 5\,mA$), the HP-LDO regulator is activated, transforming the LDO regulator into a two-stage structure. Further increase of the load current ($I_L > 5\,mA$) activates the second gain stage within the HP-LDO, converting the overall topology to a three-stage LDO regulator. The distributed overshoot reduction (DOR) circuitry [1] is designed to handle loads with $dI_L/dt < 0$, where the initial $I_L$ is greater than 20 $\mu$A. As a result, the DOR circuit enables fast recovery by reducing the overshoot voltage. The STC-LDO block is active for the entire range of load currents (0-100 mA); therefore, its quiescent current level is critical for the overall operation of the LDO regulator.

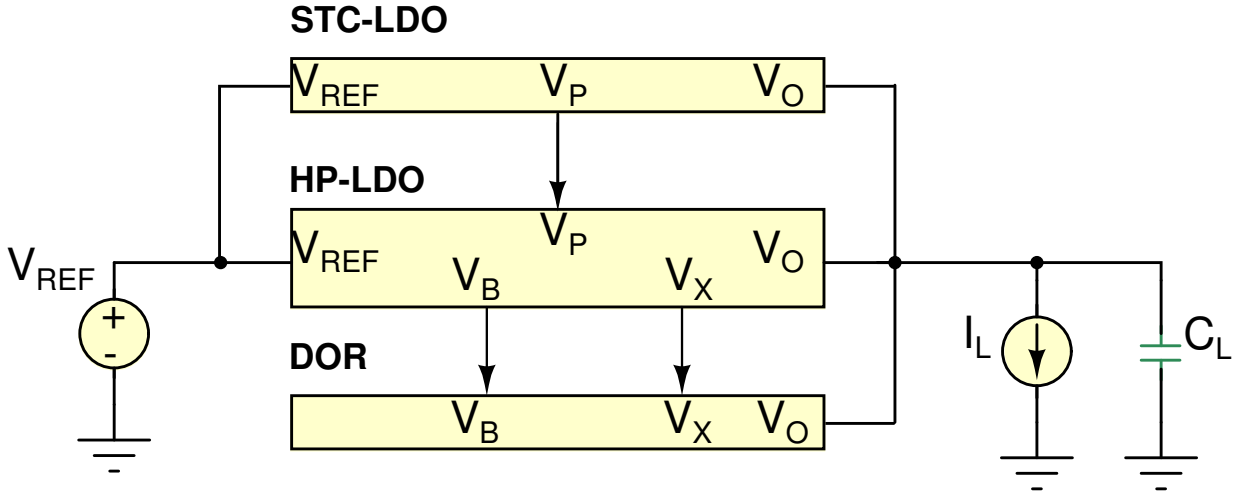


Figure 2.1: Structure of the proposed CL-LDO regulator

# 3. CIRCUIT IMPLEMENTATION

## 3.1 STC-LDO Regulator

Fig. 3.1 shows the STC-LDO regulator schematic. Since the transistors $M_{13s}$ and $M_{16s}$ form a current mirror, $I_{D16s}$ can be given by

$$I_{D16s} = \frac{(W/L)_{M16s}}{(W/L)_{M13s}} I_{D13s} = R I_{D13s} \tag{3.1}$$

where $R$ is set to 30 in the proposed design. $I_{D13s}$ is the sum of all currents connected to the diode-connected transistor $M_{13s}$, which is expressed as

$$I_{D13s} = I_{D2s} + I_{D3s} + I_{D4s} \tag{3.2}$$

In the above expression, $I_{D2s}$ is a fixed amount, set by $I_B$ and the $M_{1s} - M_{2s}$ current mirror ratio, whereas $I_{D3s}$ is set adaptively through the feedback from the $V_P$ node, and $I_{D4s}$ is dynamically adjusted by applying the high-pass filtered output voltage $V_O$ to the gate of $M_{4s}$. The dynamic current $I_{D4s}$ enables fast recovery of the STC-LDO regulator in the event of a rising load current transient. For the case of $dI_L/dt > 0$ and $I_{L,init} < 20\,\mu A$, the droop in voltage $V_O$ causes the current $I_{D4s}$ to increase due to the high-pass filter between $V_O$ and the gate of $M_{4s}$ composed of $C_{1s}$ and $R_B$ acting as a differentiator at low frequencies. As a result, an increase in $M_{13s}$ is observed, which also increases $I_{D16s}$ through current mirroring, therefore the current available to the pass transistor $M_{11s}$ increases. This operation further increases the closed-loop bandwidth of the STC regulation stage, enabling fast recovery of node $V_O$.

The control voltage generation circuit generates the preset output voltage $(V_O)$. From transistor $M_{12s}$, $V_{CTRL}$ can be obtained as

$$V_{CTRL} = V_O - V_{SG\ (M_{12s})} \tag{3.3}$$

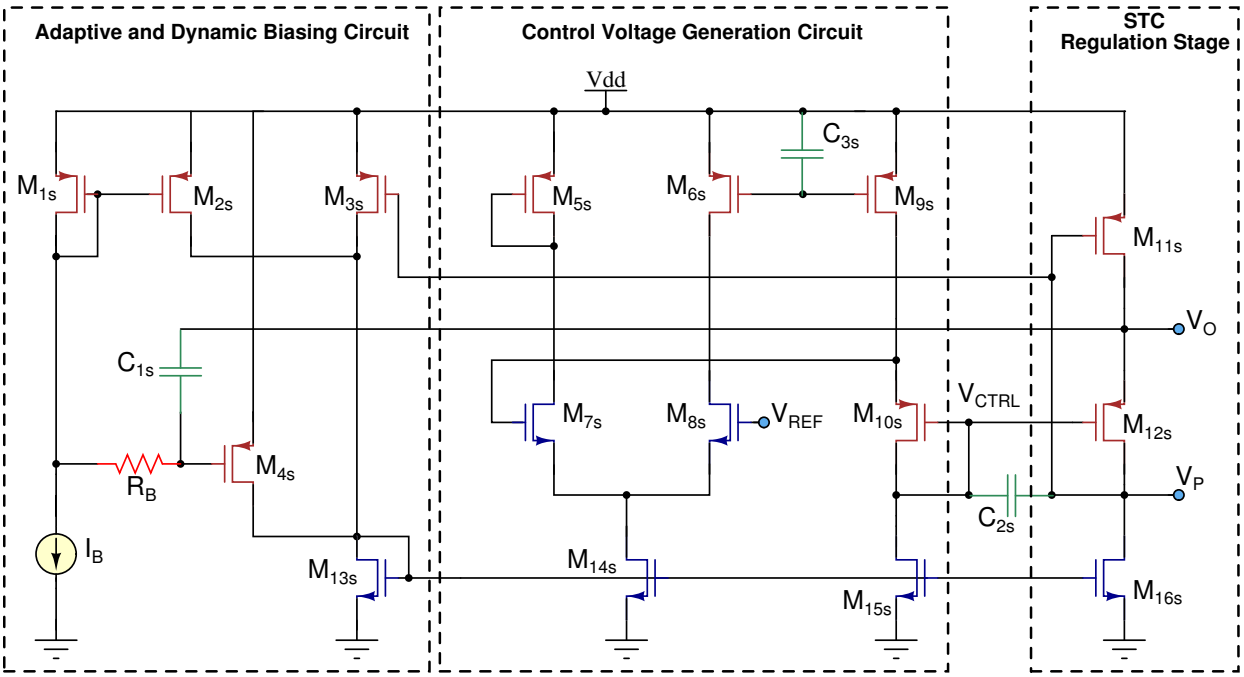


Figure 3.1: Schematic of STC-LDO regulator

From transistor $M_{10s}$, $V_{CTRL}$ is obtained as

$$V_{CTRL} = V_{REF} - V_{SG\ (M_{10s})} \tag{3.4}$$

From (3.3) and (3.4) if $V_{SG}$ of transistors $M_{12s}$ and $M_{10s}$ are matched then, $V_{OUT}$ is obtained as

$$V_O = V_{REF} \tag{3.5}$$

The preset output voltage is set close to $V_{REF}$ by biasing both $M_{12s}$ and $M_{10s}$ with the same current density. From Fig. 3.1 the regulation range inequality $Vdd < V_O + V_{SG\,(M_{11s})} - V_{SD,sat\,(M_{12s})}$ should be satisfied. For a $Vdd = 1.1\ V$ & $V_O = 0.9\ V$, appropriate choices of $V_{SG\,(M_{11s})}$ and $V_{SD,sat\,(M_{12s})}$ are made to satisfy the afore-mentioned inequality.

The third capacitor in Fig. 3.1, $C_{3s}$, provides the dominant pole of the amplifier in a unity-gain feedback configuration. Once a stable operation is guaranteed, the voltage reference $V_{REF}$ is

buffered to appear at the source terminal of $M_{10s}$.

Table 3.1 shows the sizes of all the component values used in the STC-LDO regulator. All transistors are realized using high threshold voltage devices. Capacitor $C_{3s}$ is realized as a MOS capacitor. Resistor $R_B$ is realized by biasing transistor in the triode region.

Table 3.1: STC-LDO component values

| Component | Size |
|---|---|
| $M_{7s}$ | $500\,n/500\,n$ |
| $M_{8s}$ | $500\,n/500\,n$ |
| $M_{5s}$ | $120\,n/500\,n$ |
| $M_{6s}$ | $120\,n/500\,n$ |
| $M_{9s}$ | $120\,n/40\,n$ |
| $M_{12s}$ | $9.48\,\mu/200\,n$ |
| $M_{10s}$ | $315\,n/200\,n$ |
| $M_{11s}$ | $70\,\mu/40\,n$ |
| $M_{3s}$ | $0.5\,n/2\,\mu$ |
| $M_{2s}$ | $6.2\,\mu/120\,n$ |
| $M_{1s}$ | $6.2\,\mu/120\,n$ |
| $R_B$ | $100\,k$ |
| $C_{3s}$ | $1\,p$ |
| $C_{1s}$ | $1\,p$ |
| $C_{2s}$ | $50\,fF$ |

## 3.2 HP-LDO Regulator

### 3.2.1 Regulator Core

Fig. 3.2 shows the schematics of the HP-LDO regulator, where the amplifier $A_1$ and $A_2$ schematics are shown in Figs. 3.3 and 3.4, respectively. The HP-LDO regulator design is based on [4], with circuit variations adopted to boost the recovery time of this CL-LDO. In moderate load conditions, transistors in amplifier $A_1$ along with the transistor $M_{3h}$ operate in the active region. Transistors in amplifier $A_2$ and the transistor $M_{4h}$ operate in the triode region and do not contribute to the gain when the load current is at moderate levels. For high-load conditions ($I_L > 5\,mA$),

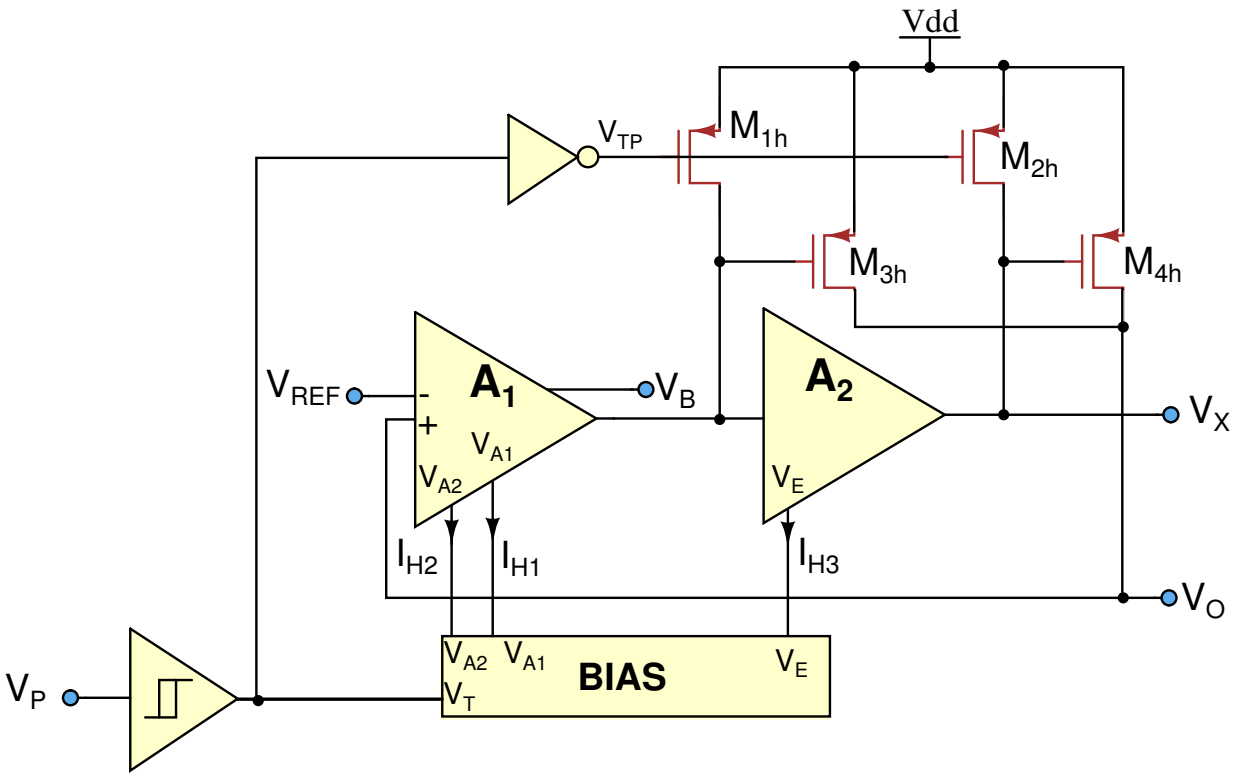


Figure 3.2: Schematic of HP-LDO regulator

$M_{4h}$, along with transistors in amplifier $A2$, enter the active region, and the LDO regulator transforms into a 3-stage structure, where $M_{3h}$ acts as a feedforward path. The bias currents to amplifier $A_1$ and $A_2$ is supplied by the bias circuit. Transistors $M_{1h}$ and $M_{2h}$ are switches to turn ON/OFF the pass transistors $M_{3h}$ and $M_{4h}$.

Amplifier $A_1$ is a folded cascode differential amplifier with wide swing cascode active load and amplifier $A_2$ is a non-inverting gain stage. The cascode current mirror in the active load of $A_1$ improves the gain from the first amplification stage. In light load conditions $(I_L < 20\,\mu A)$, $I_{H1}$ and $I_{H2}$ is turned OFF by the bias block. Therefore, the power consumption of $A_1$ at $I_L < 20\,\mu A$ is dominated by the leakage current flowing through its transistors. For $(I_L > 20\,\mu A)$, $I_{H1}$ and $I_{H2}$ are turned ON by the bias block and transistors in $A_1$ enter active region. Capacitor $C_{1a}$ is the compensation capacitor used to place the dominant pole of the HP-LDO regulator within $A_1$.

To illustrate the switching operation from STC-LDO to HP-LDO regulator (see Fig. 1.4),

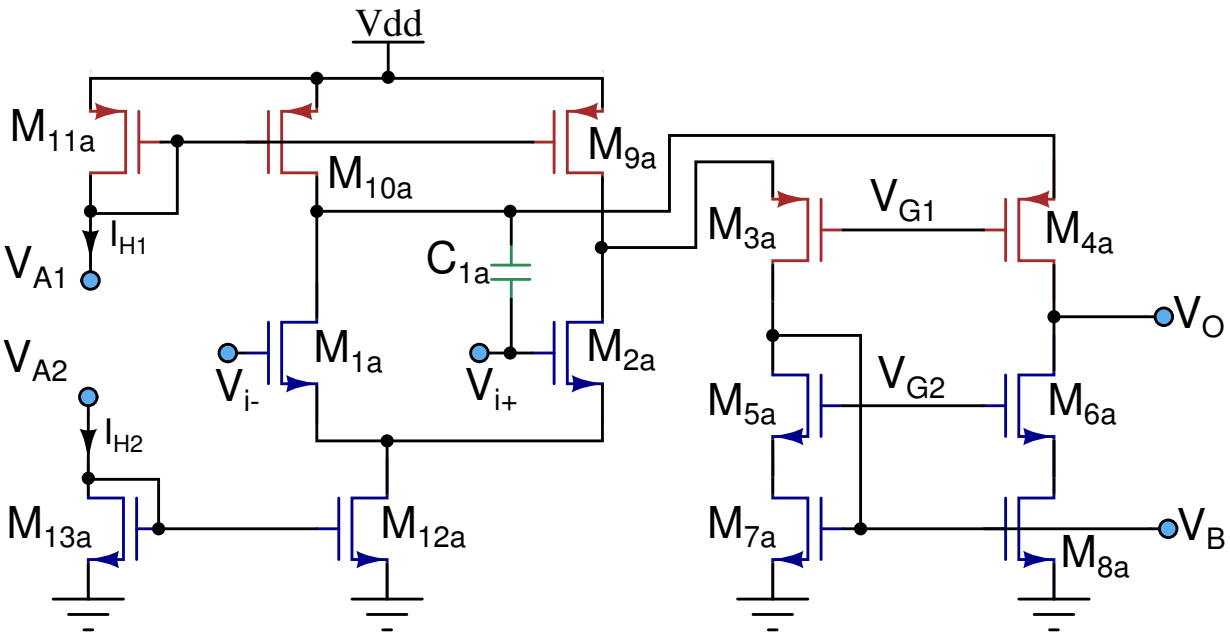


Figure 3.3: Schematic of amplifier $A_1$ in Fig. 3.2

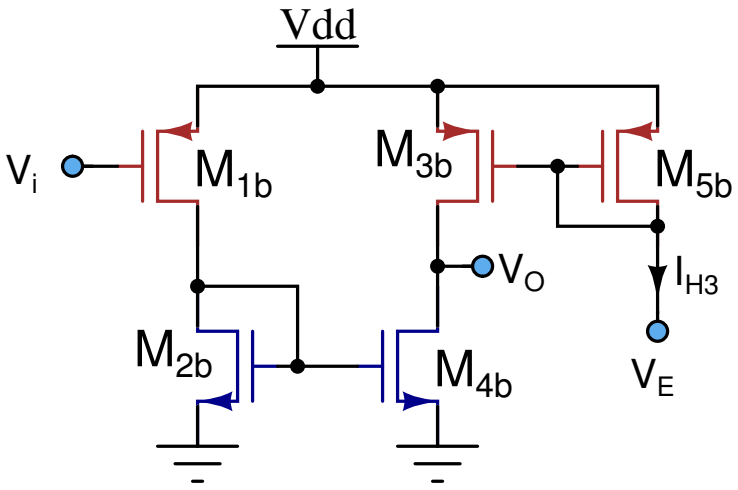


Figure 3.4: Schematic of amplifier $A_2$ in Fig. 3.2

consider the case where $I_L$ varies from 0 to 100 mA in 300 ns. At $I_L$ = 0, the HP-LDO regulator is turned OFF by the bias block, and the STC-LDO regulator is active. As $I_L$ increases, the voltage $V_P$ drops below the lower switching point voltage of the Schmitt trigger. Trip signal $V_T$ enables the bias circuit, thereby turning ON the HP-LDO regulator. For moderate load conditions,

only $M_{3h}$ and transistors in amplifier $A_1$ will be in the active region, where these transistors take about 22 ns to turn-on in the proposed design. Meanwhile, the STC regulation stage, which can operate up to 5 mA, handles the load currents when $dI_L/dt > 0$. The hysteresis band introduced by the Schmitt trigger makes sure that the voltage $V_P$ has to go above the high voltage switching point of the Schmitt trigger to turnoff $M_{3h}$ and transistors in $A_1$. The hysteresis band enables a smooth transition between the STC-LDO and the HP-LDO regulators. Additionally, the closed-loop output impedance of the HP-LDO regulator in moderate load conditions is less than that of the STC regulation stage. Therefore, the excess current demanded by the load is supplied by $M_{3h}$.

The subsequent transformation to a 3-stage topology is achieved by activating $M_{4h}$ and transistors in $A_2$. In moderate load conditions ($5\,mA > I_L > 20\,\mu A$), transistor $M_{3b}$ in $A_2$ operates in triode region as $I_{D(M_{4b})} < I_{H3}$. The drain voltage of $M_{3b}$ is pulled close to Vdd thereby turning off $M_{4h}$. $I_{D(M_{4b})}$ is set by current mirror between transistors $M_{2b}$ and $M_{4b}$. $I_{D(M_{2b})}$ is set by the adaptive scaling between transistors $M_{1b}$ and $M_{3h}$. In moderate load conditions, as $I_{D(M_{3h})}$ increases above 5 mA, $I_{D(M_{1b})}$ increases, and subsequently increasing $I_{D(M_{4b})}$. Transistor $M_{3b}$ enters active region and node $V_O$ of amplifier $A_2$ comes below Vdd thereby activating $M_{4h}$. Transistor $M_{4h}$ supplies the load current in the high load current range ($5\,mA < I_L < 100\,mA$). As the load current in $M_{4h}$ reduces, the HP-LDO regulator transforms into 2-stage, and subsequently, the STC-LDO regulator takes over in light load conditions by turning off the HP-LDO regulator section.

The HP-LDO is this work is not adaptively biased as in [1] and [4]. Adaptive and dynamic biasing (which helps in loop stability and improves transient response) is now handled in the STC-LDO. This gives a degree of freedom by decoupling adaptive biasing out of HP-LDO design, thereby designing the HP-LDO in a stand-alone fashion.

A scalable bandgap voltage reference ($V_{REF} = 0.9\,V$) [7] is used in this CL-LDO. A scalable $V_{REF}$ enables operation of both STC-LDO and HP-LDO regulator with $V_{REF} = V_O$, thereby eliminating the feedback resistors $R_1$ and $R_2$ (see Fig. 1.4) in the HP-LDO regulator. Therefore, the open loop unity gain frequency ($\omega_t$) of the HP-LDO regulator is increased by a factor of $\beta = R_2/(R_1 + R_2)$.

Table 3.2 shows the component values used in the core of HP-LDO regulator. Transistors $M_{3h}$ and $M_{4h}$ are realized using high threshold voltage native devices to reduce their static leakage current. All other transistors are realized using standard threshold voltage native devices.

Table 3.2: Core HP-LDO regulator component values

| Component | Size | Component | Size |
|---|---|---|---|
| $M_{1a}$ | $1\,\mu/1\,\mu$ | $M_{1b}$ | $7\,\mu/1\,\mu$ |
| $M_{2a}$ | $1\,\mu/1\,\mu$ | $M_{2b}$ | $6.66\,\mu/200\,n$ |
| $M_{3a}$ | $33\,\mu/1\,\mu$ | $M_{3b}$ | $20\,\mu/200\,n$ |
| $M_{4a}$ | $33\,\mu/1\,\mu$ | $M_{4b}$ | $6.66\,\mu/200\,n$ |
| $M_{5a}$ | $17\,\mu/1\,\mu$ | $M_{5b}$ | $20\,\mu/200\,n$ |
| $M_{6a}$ | $17\,\mu/1\,\mu$ | $M_{1h}$ | $10\,\mu/40\,n$ |
| $M_{7a}$ | $17\,\mu/1\,\mu$ | $M_{2h}$ | $10\,\mu/40\,n$ |
| $M_{8a}$ | $17\,\mu/1\,\mu$ | $M_{3h}$ | $400\,\mu/40\,n$ |
| $M_{9a}$ | $100\,\mu/1\,\mu$ | $M_{4h}$ | $8.94\,m/40\,n$ |
| $M_{10a}$ | $100\,\mu/1\,\mu$ | $C_{1a}$ | $2p$ |
| $M_{11a}$ | $100\,\mu/1\,\mu$ | $I_{H1}$ | $50\,\mu A$ |
| $M_{12a}$ | $16.67\,\mu/1\,\mu$ | $I_{H2}$ | $50\,\mu A$ |
| $M_{13a}$ | $16.67\,\mu/1\,\mu$ | $I_{H3}$ | $10\,\mu A$ |

### 3.2.2 Schmitt Trigger

A Schmitt trigger ensures that switching between the STC-LDO and the HP-LDO regulator is not abrupt and jittery. Fig. 3.5 shows the schematic of the Schmitt trigger. The size of transistor $M_{S1-S6}$ plays a key role in introducing a hysteresis band, and the following discussion provides details on the design of the Schmitt trigger.

Hysterisis in a Schmitt trigger is defined as

$$V_H = V_{SPH} - V_{SPL} \tag{3.6}$$

where $V_{SPH}$ and $V_{SPL}$ is the switching point high and switching point low, respectively. Consider the scenario where $M_{S2}$ is on the verge of turning on. Relationship between $V_P$ and $V_X$ can be

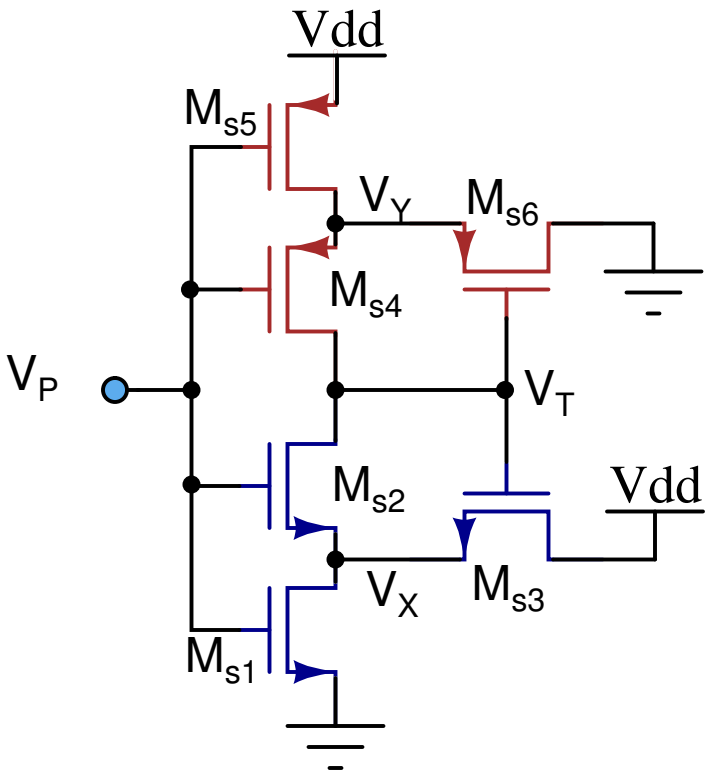


Figure 3.5: Schmitt trigger circuit

obtained from $V_{GS}$ of transistor $M_{S2}$.

$$V_P = V_{SPH} = V_{THN2} + V_X \tag{3.7}$$

Similarly, consider the scenario where $M_{S4}$ is on the verge of turning off. Relationship between $V_P$ and $V_Y$ can be obtained from $V_{SG}$ of transistor $M_{S4}$.

$$V_P = V_{SPL} = V_Y - V_{TH4} \tag{3.8}$$

When $M_{S2}$ is in the verge of turning on. The current flowing in both $M_{S1}$ and $M_{S3}$ are equal. Equating the drain currents of $M_{S1}$ and $M_{S3}$.

$$\frac{\beta_1}{2}(V_{SPH} - V_{THN1})^2 = \frac{\beta_3}{2}(Vdd - V_X - V_{THN3})^2 \tag{3.9}$$

gives

$$\frac{\beta_5}{\beta_6} = \frac{W_5\, L_6}{L_5\, W_6} = \left[\frac{V_{SPL}}{Vdd - V_{SPL} - V_{THP}}\right]^2 \tag{3.10}$$

Similarly, when $M_{S4}$ is on the verge of turning off. The current flowing in both $M_{S5}$ and $M_{S6}$ are equal. Equating the drain currents of $M_{S5}$ and $M_{S6}$.

$$\frac{\beta_5}{2}(Vdd - V_{SPL} - V_{THP5})^2 = \frac{\beta_6}{2}(V_Y - V_{THP6})^2 \tag{3.11}$$

gives

$$\frac{\beta_1}{\beta_3} = \frac{W_1\, L_3}{L_1\, W_3} = \left[\frac{Vdd - V_{SPH}}{V_{SPH} - V_{THN}}\right]^2 \tag{3.12}$$

Choosing the minimum channel length of 40 nm and using the design equations from (3.12) and (3.10), size of the components in Table 3.3 is obtained. Transistors were realized using high threshold voltage native devices ($V_{THN} = 0.51\,V$ and $V_{THP} = 0.52\,V$) to reduce static leakage current. The switching point high ($V_{SPH}$) is set at 0.75 V, and the switching point low is set at $V_{SPL}$ = 0.35 V. The 0.4 V margin ensures that there are no glitches in the output voltage of CL-LDO. Fig. 3.6 shows input-output characteristics of the Schmitt trigger used in this design. The targeted switch over point from STC-LDO to the HP-LDO regulator is at $I_L = 20\,\mu A$.

Table 3.3: Schmitt trigger component values

| Device | Size |
|---|---|
| $M_{S1}$ | $120\,n/40\,n$ |
| $M_{S2}$ | $120\,n/40\,n$ |
| $M_{S3}$ | $5\,\mu/40\,n$ |
| $M_{S4}$ | $150\,n/40\,n$ |
| $M_{S5}$ | $150\,n/40\,n$ |
| $M_{S6}$ | $120\,n/40\,n$ |

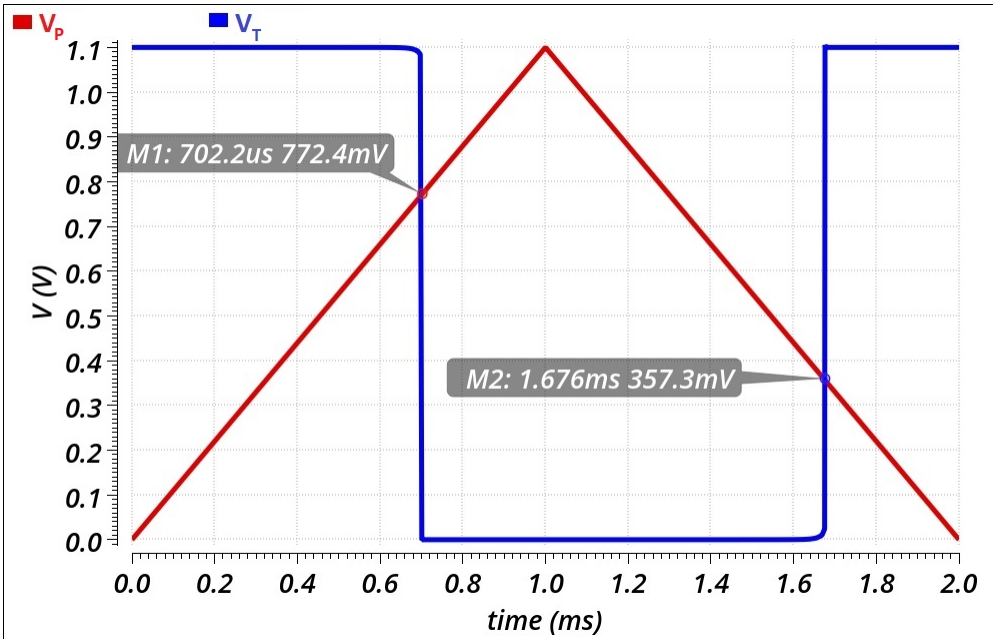


Figure 3.6: Schmitt trigger input output characteristics

### 3.2.3 Bias Circuits

Shown in Fig. 3.7 is the bias circuit used to control the HP-LDO regulator. The signal from Schmitt trigger output ($V_T$) is used to generate three independent current sources $I_{H1}$, $I_{H2}$, and $I_{H3}$. As voltage $V_T$ goes high transistor $M_{X3}$ turns on in saturation. Resistor $R_X$ and the ratio of $W_{M_{X1}}/L_{M_{X1}}$ fixes the drain current of $M_{X1}$. Subsequently, bias currents $I_{H2}$ and $I_{H3}$ are obtained by a simple current mirror.

$V_{T1}$ is a short pulse signal with a pulse width equal to "Delay," which is activated during the rising and falling edge of $V_T$. Additionally, depending on the level of $V_{T1}$, $I_{H1}$ is either equal to $I_{H11}$ or $I_{H11} + I_{H12}$. The increase in the value of $I_{H1}$ in the rising and falling edge of $V_T$, increases bandwidth, turn-on time and slew performance of the HP-LDO regulator in the event of large load current transients.

## 3.3 DOR

The DOR circuit schematic is shown in Fig. 3.8, which aims to reduce the overshoot when the load current changes suddenly. Consider a sudden load variation from $I_L$ = 100 mA to 0. Due to

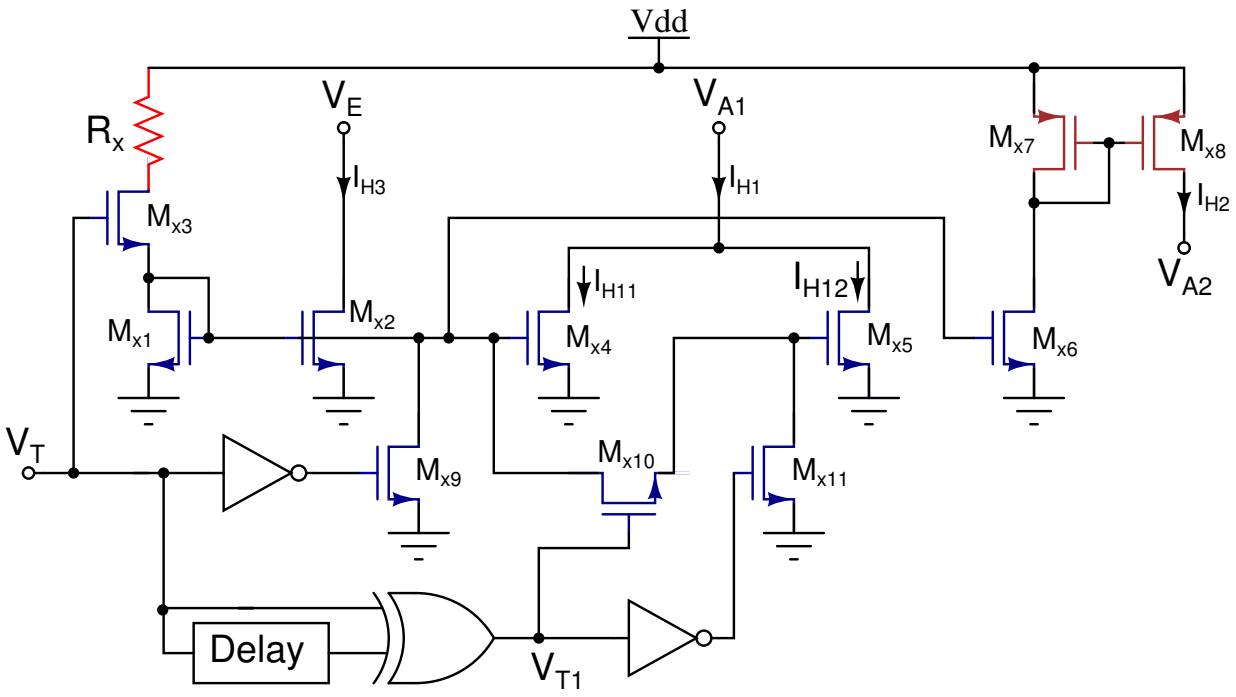


Figure 3.7: Schematic of the bias circuits used to control the HP-LDO regulator

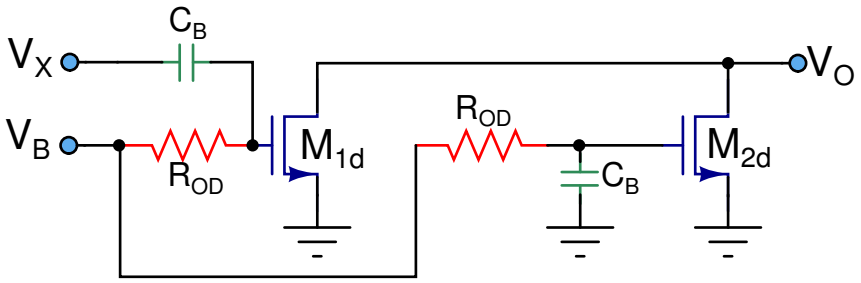


Figure 3.8: DOR circuit schematic

a sudden decrease in the load current, the excess current from $M_{4h}$ does not have a discharge path (see Fig. 3.2). Due to the finite bandwidth associated with the error correction loop of the HP-LDO regulator, the output voltage overshoots. The addition of a distributed overshoot reduction circuit suppresses this overshoot. The DOR circuitry [1] is designed to handle loads with $dI_L/dt < 0$, where $I_{L,init} > 20\,\mu A$. Transistor $M_{1d}$ along with $C_B$, and $R_{BIAS}$ provides the first fast local feedback. With the arrival of the delayed version of the signal to the gate of $M_{2d}$, the discharge

is sustained for a longer time [4]. This overshoot reduction mechanism significantly improves the recovery time of the LDO. The size of components used in DOR are as follows, $R_{OD} = 100\,k\Omega$, $C_B = 1\,pF$ and $(W/L)_{M_{1d,2d}} = 10\,\mu\,/0.6\,\mu$.

# 4. STABILITY ANALYSIS

The stability analysis is done for three separate load current ranges shown in Table 4.1. Additionally, the table summarizes the topologies that the CL-LDO adopts in various load current ranges. The values of $I_{ON1}$ and $I_{ON2}$ chosen for this particular design are $I_{ON1} = 20\ \mu A$ and $I_{ON2} = 5\ mA$. The maximum load current $(I_{L(max)})$ that the LDO can handle is 100 mA. The following section provides a detailed analysis of the small-signal loop stability of the CL-LDO for three cases, as shown in Table 4.1.

Table 4.1: Summary of the topologies (CL-LDO) at different load current ranges

| | **Load Current Range** | **Load Condition** | **Topology** |
|---|---|---|---|
| $Case1$ | $0 < I_L < I_{ON1}$ | Light | STC - LDO (single stage) |
| $Case2$ | $I_{ON1} < I_L < I_{ON2}$ | Medium | HP - LDO (two stage) |
| $Case3$ | $I_{ON2} < I_L < I_{L\ (max)}$ | High | HP - LDO (three stage) |

## 4.1 Case1

The STC-LDO regulator supplies the desired load current at light load current $(0 < I_L < I_{ON1})$ ranges (refer Fig. 3.1 for STC-LDO regulator schematic). The equivalent small-signal model for the STC-LDO regulator is shown in Fig. 4.1. Breaking the feedback loop at the gate of the pass transistor $M_{11s}$ and including the loading effect, the loop transfer function can be derived in two parts as illustrated in Fig. 4.1, Fig. 4.2 and Fig. 4.3, respectively. The variables $r_{oi}$ and $g_{mi}$ are the output impedance and the transconductance of transistors, respectively ($i$ can take any of the transistor subscripts as in Fig. 4.1). Solving for $V_O/V_{test}$, it can be seen that

$$\frac{V_O}{V_{test}} = -g_{m11s}\left(Z_1 \,||\, \frac{1}{s\,C_L}\right) \tag{4.1}$$

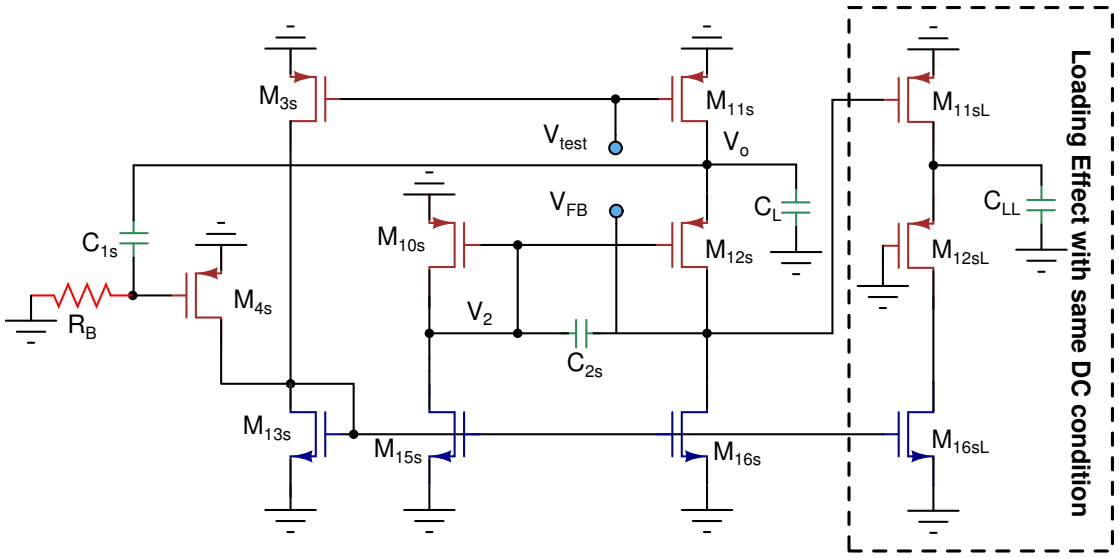


Figure 4.1: Loop stability analysis by including the loading effect

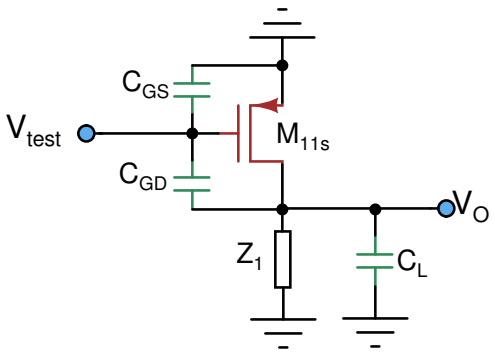


Figure 4.2: Stage1 small signal model

where $Z_1$ is given by

$$Z_1 = \frac{1}{g_{m12s}} \left(1 + \frac{r_{o16s}}{r_{o12s}}\right) \tag{4.2}$$

Substituting the value of $Z_1$ in (4.1), $V_O/V_{test}$ is obtained as

$$\frac{V_O}{V_{test}} = \frac{g_{m11s}\, r_{o11s}\, (r_{o16s} + r_{o12s})}{r_{o16s} + r_{o12s} + r_{o11s} + g_{m12s}\, r_{o12s}\, r_{o11s} + C_L\, r_{o11s}\, s\, (r_{o12s} + r_{o16s})} \tag{4.3}$$

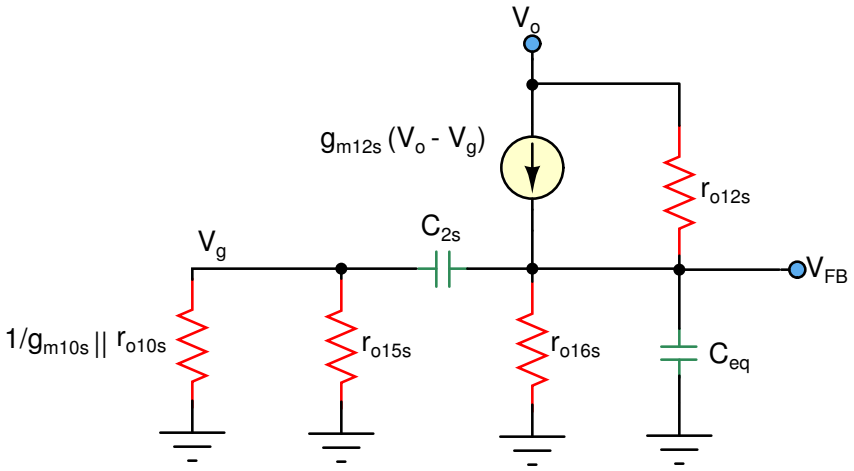


Figure 4.3: Stage2 small signal model

On the assumption that $g_{m12s}\ r_{o12s}\ r_{o16s}\ >>\ r_{16s},\ r_{o12s},\ r_{o11s}$, and simplifying (4.3) further, $V_O/V_{test}$ can be approximated as

$$\frac{V_O}{V_{test}} \approx \frac{\frac{g_{m11s}}{g_{m12s}}\left(1+\frac{r_{o16s}}{r_{o12s}}\right)}{1+s\,\frac{C_L}{g_{m12s}}\left(1+\frac{r_{o16s}}{r_{o12s}}\right)} \tag{4.4}$$

Solving for $V_{FB}/V_O$ (see Fig. 4.3) , the following is obtained.

$$\frac{V_{FB}}{V_O} = \frac{\left(g_{m12s}\,r_{o12s}+1\right)\left(s\,r_{o16s}\left(C_{2s}+C_{eq}\right)+g_{m10s}\,r_{o16s}+1\right)}{r_{o16s}\left[s^2\,r_{o12s}\,C_{eq}\left(C_{eq}+C_{2s}\right)+r_{o16s}^2\,r_{o12s}\left(g_{m10s}\,C_{eq}+g_{m10s}\,C_{2s}+g_{m12s}\,C_{2s}\right)s+g_{m12s}\,r_{o16s}^2\right]} \tag{4.5}$$

where $C_{eq}$ is the total capacitance seen at the gate of $M_{11s}$ and is given by

$$C_{eq} = C_{GSP} + \left(1+g_{mp}\left(Z_1||r_{o11s}\right)\right)C_{GSD} \tag{4.6}$$

The complete transfer function is obtained as a product of $V_O/V_{test}$ and $V_{FB}/V_O$.

$$TF = \frac{\frac{g_{m11s}}{g_{m12s}}\left(1+\frac{r_{o16s}}{r_{o12s}}\right)}{1+s\,\frac{C_L}{g_{m12s}}\left(1+\frac{r_{o16s}}{r_{o12s}}\right)}\ \frac{\left(g_{m12s}\,r_{o12s}+1\right)\left(s\,r_{o16s}\left(C_{2s}+C_{eq}\right)+g_{m12s}\,r_{o16s}+1\right)}{r_{o16s}\left[s^2\,r_{o12s}\,C_{eq}\left(C_{eq}+C_{2s}\right)+r_{o16s}^2\,r_{o12s}\left(g_{m10s}\,C_{eq}+g_{m10s}\,C_{2s}+g_{m12s}\,C_{2s}\right)s+g_{m12s}\,r_{o16s}^2\right]} \tag{4.7}$$

On the assumption that $C_L \gg C_{eq}$, the following system parameters are obtained.

The dominant pole $p_1$ and the non-dominant pole $p_2$ can be calculated as,

$$p_1 = \frac{-1}{C_L\, Z_1} \tag{4.8}$$

$$p_2 \approx \frac{-1}{C_{eq}\,(r_{o12s} \,||\, r_{o16s})} \tag{4.9}$$

The internally generated LHP zero is given by

$$z_{LHP} \approx \frac{-(g_{m10s}\, r_{o16s} + 1)}{r_{o16s}\,(C_{2s} + C_{eq})} \tag{4.10}$$

The low frequency gain $(A_{dc})$ of the STC-LDO regulator structure is expressed as

$$A_{dc} \approx \frac{g_{m11s}}{g_{m12s}} \left(1 + \frac{r_{o16s}}{r_{o12s}}\right) \left(g_{m12s} + \frac{1}{r_{o12s}}\right) (r_{o16s} \,||\, r_{o12s}) \tag{4.11}$$

From (4.11) it can be seen that the STC-LDO regulator has low loop gain in ultra-low bias current condition, which offsets the DC output voltage. The control voltage generation circuit addresses this issue by using an optimal biasing scheme (matched current densities).

Additionally, there is a third parasitic pole $(p_3)$ appearing at higher frequencies. The connection to the load has a stray parasitic resistance, which comes in series with $C_L$. This series connection of resistance $R_E$ and $C_L$ create LHP zero and improves phase margin. Nonetheless, the design of the STC-LDO regulator does not consider the ESR zero to stabilize the loop as the parasitic interconnect resistance is not well controlled.

From (4.8), (4.9) and (4.10), it can be observed that at $I_L = 0$, $p_1$ and $z_1$ are proportional to $\sqrt{I_{D16s}}$, whereas $p_2$ is proportional to $I_{D16s}$. Additionally, $g_{m11s}$ becomes very low, and $C_{eq}$ reduces to $C_{GS11s} + C_{GD11s}$. Also, $p_1$ is independent of the load current and $p_2$ appears as a high frequency pole. An equivalent single pole system can be obtained at $I_L = 0$, thus achieving a phase margin (PM) greater than or equal to $90°$. As $I_L$ increases, the Miller effect across the pass transistor $M_{11s}$ increases $C_{eq}$ and $p_2$ appears at lower frequencies. Internally generated zero $z_1$ partially cancels $p_2$, thereby achieving stability for $I_L < 20\,\mu A$. For $20\,\mu A < I_L < 5\,mA$, the

adaptive current $I_{M3s}$ plays a key role in maintaining stability of the STC-LDO regulation stage.

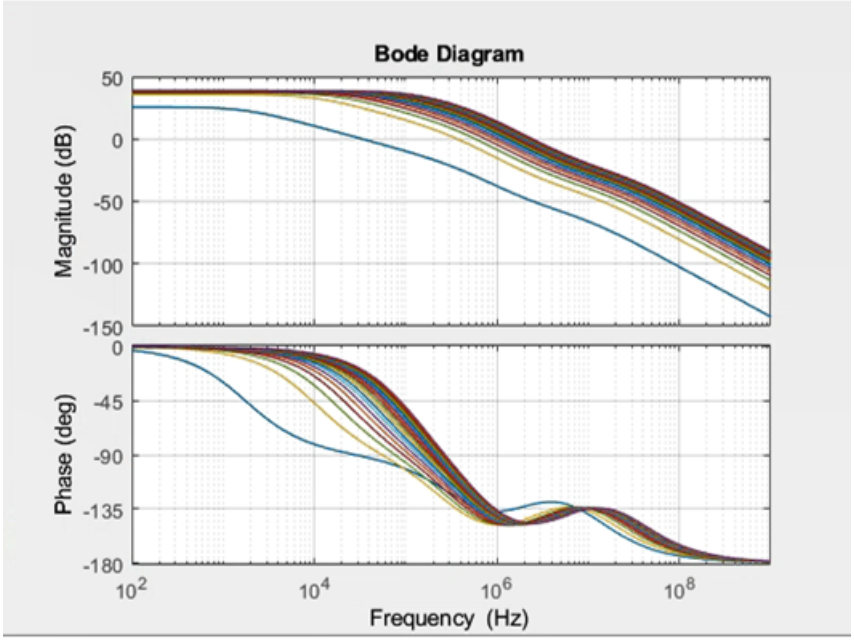


Figure 4.4: MATLAB simulation results from STC LDO ($I_L$ = 0 - 20uA). Captured small signal data from schematic level is used to generate the loop response.

The adaptive current biasing scheme also includes a simple current mirror between transistors $M_{11s}$ and $M_{3s}$ with the mirroring ratio given by

$$\frac{(W/L)_{M11s}}{(W/L)_{M3s}} = \frac{4000}{1} \tag{4.12}$$

In the case of a sudden increase in $I_L$, the pass gate voltage, $V_P$ reacts to this change, and subsequently $I_{D3s}$ and $I_{D16s}$ increase. With reduced output resistances of transistors in the STC-LDO regulation stage, $p_2$ and $z_1$ move to higher frequencies. In conclusion, the internally generated zero $z_1$ and adaptive biasing enable the STC-LDO regulator to achieve stability for a current load range of 0–5 mA.

Fig. 4.4 shows the Matlab level reconstructed loop magnitude and phase response by capturing the small-signal parameters at the schematic level. The results show good accuracy in the transfer

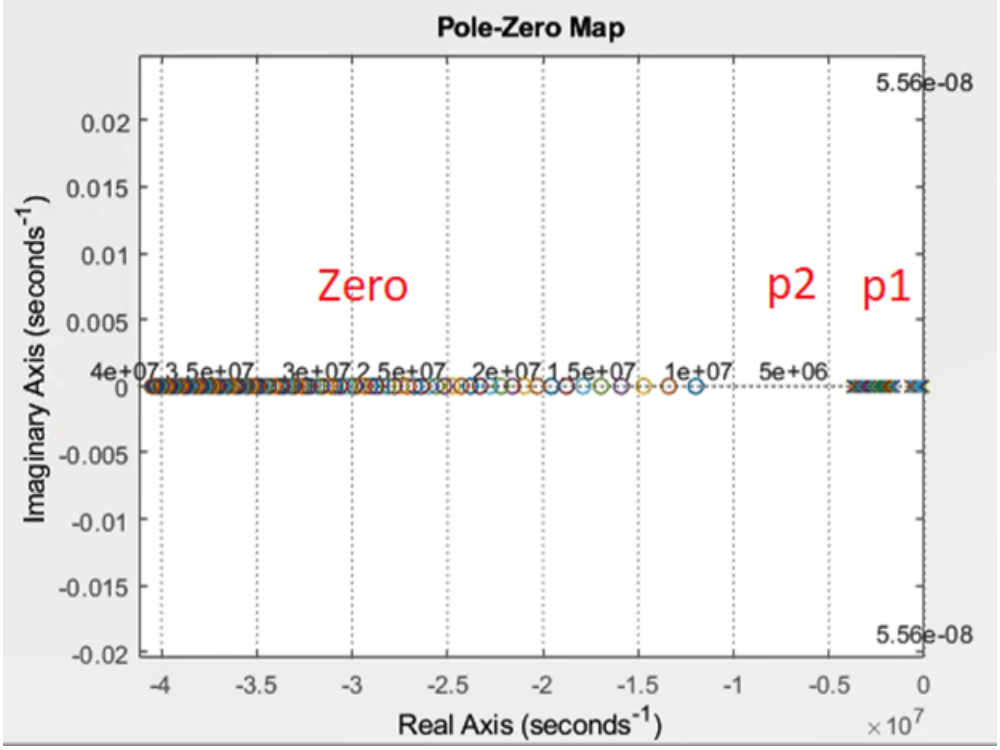


Figure 4.5: Simplified transfer function – pole zero map ($p_1, p_2, z_1$ )

function deduced. Fig. 4.5 shows the pole-zero map for the transfer function of the STC-LDO regulator. The movement of the system poles and zeros are captured for different load currents. In conclusion, for $0 < I_L < 5\,mA$, the STC-LDO regulator does not have complex poles and achieves competitive open-loop gain and GBW from light to medium load current conditions.

## 4.2 Case2

Fig. 4.6 shows the small-signal model when the LDO transforms into a 2-stage structure (refer Fig. 3.2, Fig. 3.3 and Fig. 3.4 for schematic of HP-LDO regulator). The loop transfer function of the structure shown in Fig. 4.6 can be deduced as

$$TF = -A_{dc}\frac{\left(1 + s\frac{C_{1a}}{g_{m4a}}\right)}{(1 + s\,C_{1a}\,g_{m3h}\,R_1\,r_{o3h})\,\left(1 + s\frac{C_L\,C_1}{C_{1a}\,g_{m3h}} + s^2\,\frac{C_L\,C_1}{g_{m4a}\,g_{m3h}}\right)} \tag{4.13}$$

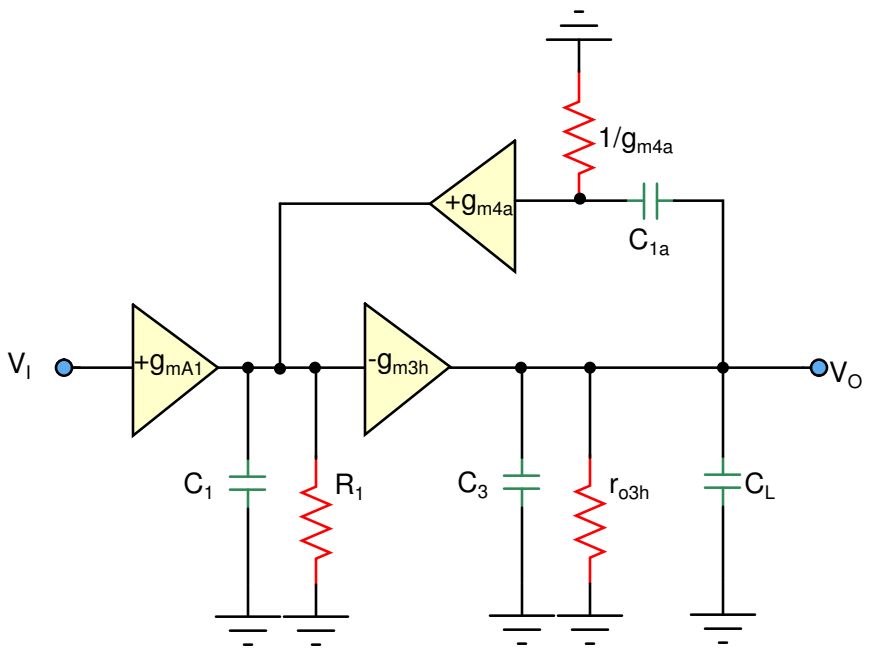


Figure 4.6: LDO transformation into a 2-stage structure (cascode compensation)

where $A_{dc}$ is the low frequency open loop gain, $C_{1a}$ is the compensation capacitor, $C_L$ is the load capacitance, $C_1$ is the output capacitance of amplifier $A_1$ , $g_{mA1}$ is the transconductance of amplifier $A_1$, $g_{m3h}$ is the transconductance of transistor $M_{3h}$, $g_{m4a}$ is the transconductance of transistor $M_{4a}$, $r_{o3h}$ is the ouput impedance of transistor $M_{3h}$, and $R_1$ is the output impedance of amplifier $A_1$ (refer Fig. 3.2, Fig. 3.3 and Fig. 3.4 for schematic of the HP-LDO regulator). The low-frequency open-loop gain is given by,

$$A_{dc} = g_{mA1}\ g_{m3h}\ R_1\ r_{o3h} \tag{4.14}$$

The dominant pole of the system is given by

$$p_1 = -\frac{1}{C_{1a}\ g_{m3h}\ R_1\ r_{o3h}} \tag{4.15}$$

The gain-bandwidth product (GBW) is given by

$$GBW = \frac{g_{mA1}}{C_{1a}} \tag{4.16}$$

The second non-dominant pole is given by

$$p_2 = \frac{-\, g_{m3h}\, C_{1a}}{C_1\, C_L} \tag{4.17}$$

The high frequency parasitic pole $p_3$ is given by

$$p_3 = -\frac{g_{m4a}}{C_{1a}} \tag{4.18}$$

High frequency zero $z_1$ is given by

$$z_1 = -\frac{g_{m4a}}{C_{1a}} \tag{4.19}$$

From (4.19) and (4.18), it can be seen that $p_3$ and $z_1$ cancel each other. Due to cascode compensation $p_2$ is pushed to higher frequencies by the cascode factor $C_{1a}/C_1$. Non-dominant $p_2 \propto \sqrt{I_L}$ and the worst case stability condition happens at $I_L = I_{ON1}\ (20\,\mu A)$.

### 4.3 Case3

The small-signal model of the transformed 3-stage structure is depicted in Fig. 4.7. The loop transfer function of the structure shown in Fig. 4.7 can be deduced as

$$TF = \frac{-A_{dc}\left(1 + s\frac{C_{1a}}{g_{m4a}}\right)\left(1 + s\frac{C_2\ g_{m3h}}{g_{mA2}\ g_{m4h}}\right)}{(1 + s\, C_{1a}\, g_{mA2}\, g_{m4h}\, R_1\, R_2\, R_3)\left(1 + s\frac{C_2\ g_{m3h}}{g_{m4h}\ g_{mA2}} + \frac{s^2\ C_1\ C_2}{g_{mA2}\ g_{m4h}\ g_{m4a}\ R_3}\right)\ (1 + s\ C_L\ R_3)} \tag{4.20}$$

where $R_1$ is the output impedance of amplifier $A_1$, $R_2$ is the output impedance of amplifier $A_2$, $R_3 = (r_{o3h}\,||\,r_{o4h})$ is the output resistance, $C_L$ is the load capacitance, $g_{mA1}$ is the transconductance of amplifier $A_1$, $g_{mA2}$ is the transconductance of amplifier $A_2$, $g_{m3h}$ is the transconductance of transistor $M_{3h}$, $g_{m4h}$ is the transconductance of transistor $M_{4h}$, $g_{m4a}$ is the transconductance of transistor $M_{4a}$, $C_{1a}$ is the compensation capacitor, $C_1$ is the output capacitance of amplifier $A_1$, $C_2$ is the output capacitance of amplifier $A_2$, $C_3$ is the output capacitance (refer Fig. 3.2, Fig. 3.3 and Fig. 3.4 for schematic of the HP-LDO regulator). The low-frequency gain open-loop gain $(A_{dc})$ is

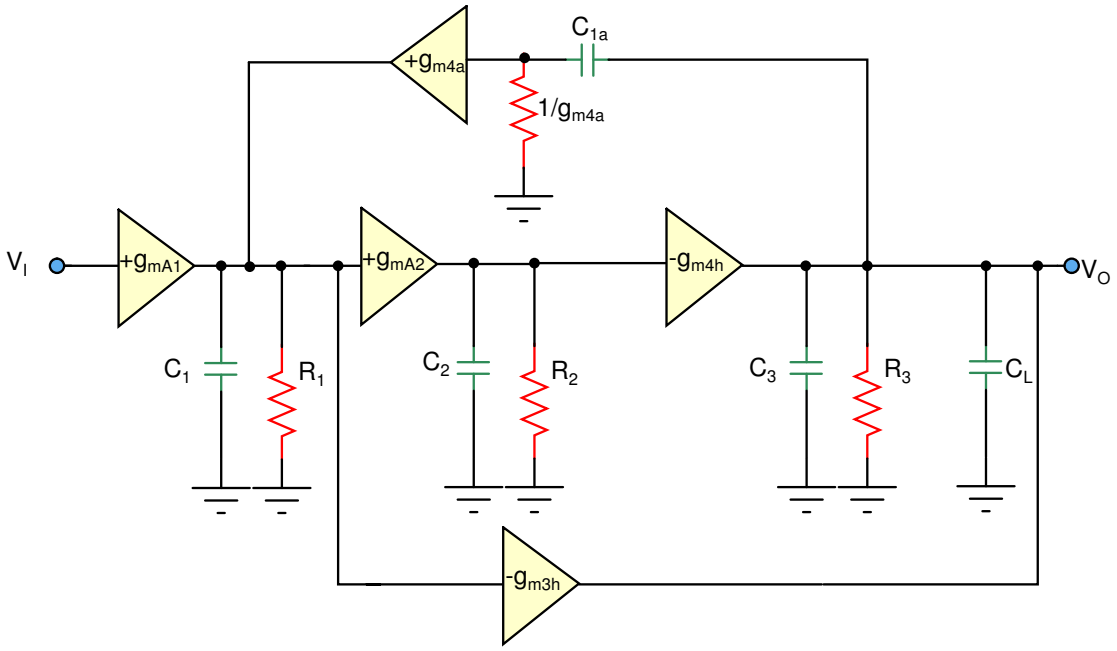


Figure 4.7: LDO transformation into a 3-stage structure

given by

$$A_{dc} = g_{mA1}\ g_{mA2}\ g_{m4h}\ R_1\ R_2\ R_3 \tag{4.21}$$

The dominant pole of the system is given by

$$p_1 \ = \ -\frac{1}{C_{1a}\ g_{mA2}\ g_{m4h}\ R_1\ R_2\ R_3} \tag{4.22}$$

The gain-bandwidth product is given by

$$GBW = \frac{g_{mA1}}{C_{1a}} \tag{4.23}$$

The structure has non-dominant complex poles and the corresponding Q factor is given by

$$Q = \sqrt{\frac{g_{mA2}\ g_{m4h}\ C_1}{g_{m3h}^2\ g_{m4a}\ C_2\ R_3}} \tag{4.24}$$

The magnitude of the parasitic poles is given by

$$|p_{2,3}| = \sqrt{\frac{g_{mA2}\ g_{m4h}\ R_3}{C_1\ C_2}} \tag{4.25}$$

From (4.25), it can be seen that the parasitic poles $p_{2,3}$ are located at high frequencies. With $Q \propto \sqrt{1/R_3}$ and the highest Q appearing at the highest load current condition, the optimized values were obtained by large $g_{m3h}$ and $g_{m4a}$, and a small $g_{mA2}$ making sure the loop response does not peak due to large $Q$. The fourth pole is given by

$$p_4 = -\frac{1}{C_L\ R_3} \tag{4.26}$$

As load current increases the $p_4$ is pushed to higher frequencies.The zeros in the system are given by

$$z_1 = -\frac{g_{m4a}}{C_{1a}} \tag{4.27}$$

$$z_2 = -\frac{g_{mA2}\ g_{m4h}}{C_2\ g_{m3h}} \tag{4.28}$$

$z_1$ is placed just beyond GBW to improve phase response. $z_2$ occurs and very high frequencies and does not affect the loop response.

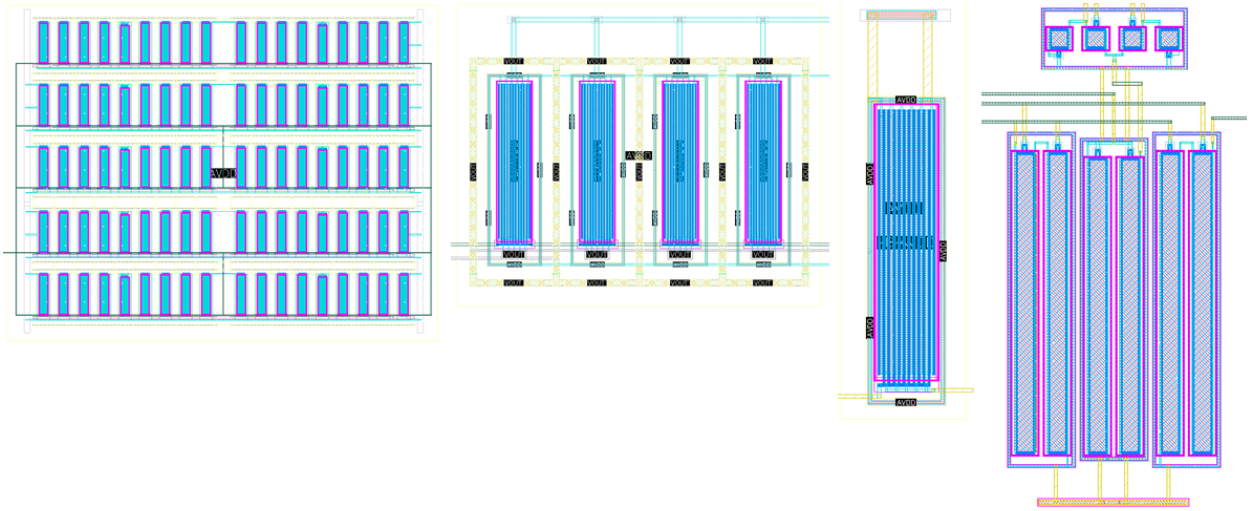

Figure 5.1: Layout

The layout of the critical parts of the circuit is shown in Fig. 5.1. Transistors $M_{4h}$, $M_{3h}$ and $M_{11s}$ which are the pass transistors of the STC-LDO and HP-LDO regulator contribute to the majority of parasitics because of their large size. The parasitic effects due to fringing capacitors (gate-source, drain-source, gate-drain) and the interconnect resistance primarily limit performance. Simulation results with post-layout extraction for the critical blocks are provided in this section.

Table 5.1 captures the block level current consumption. The quiescent current consumption at zero-load condition is dominated by the STC-LDO regulator ($< 170\,nA$). By using low leakage high threshold transistors, the pass gate ($M_{3h}$ and $M_{4h}$) leakage was restricted to $< 30\,nA$ when the high power structure is turned-off.

The loop gain and loop phase response for the entire load current range $(0 - 100\,mA)$ is shown in Fig. 5.2 and Fig. 5.3 respectively. It can be seen from the simulation results that the loop gain and GBW increases with an increase in load current. The structure achieves a loop gain (28 dB)

Table 5.1: Block level current consumption

| Block | Quiescent Current Consumption |
|---|---|
| | $Iq_{min}\ (nA)$ |
| STC-LDO | 166.2 0 |
| HP-LDO | 28.42 |
| Schmitt Trigger | 13.32 |
| BIAS | 19.3 |
| TOTAL | 227.24 |

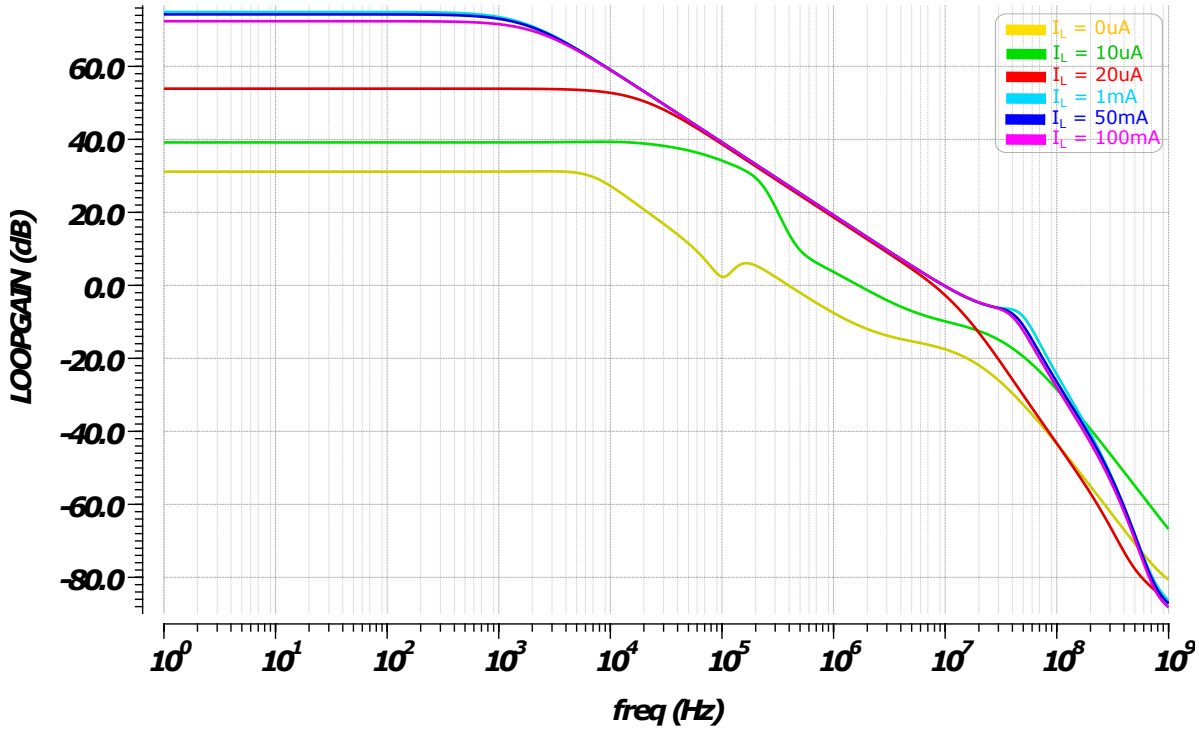


Figure 5.2: Loop gain vs frequency as a function of load current ($I_L$ = 0 to 100 mA)

with 100 nA of current in the output stage of the STC-LDO regulator. The loop gain recovers to 40 dB as the load current increases to 500 nA, which is comparable to the low-frequency loop gain reported in the literature [1],[4].

The transient response for the entire load current range $(I_L = 0 - 100\,mA)$ at the worst-case stability condition $(C_L = 100\,pF)$ is shown in the Fig. 5.4. Additionally, Fig. 5.5 captures the

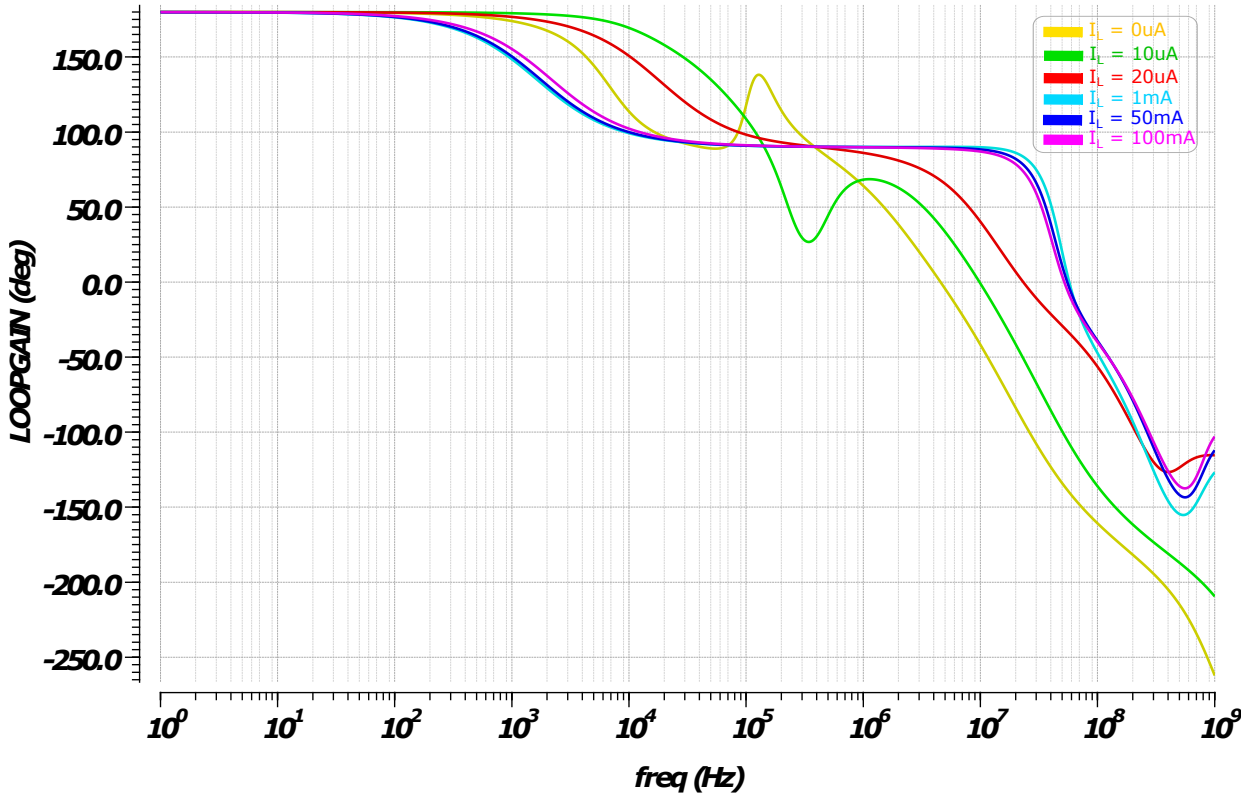


Figure 5.3: Loop phase vs frequency as a function of load current ($I_L$ = 0 to 100 mA)

output voltage transient response at various load current ranges. Results from Fig. 5.5 show that there is no ringing at light loads $(I_L = 100\ nA)$, confirming the improved phase margin.

The important stability margins such as gain, GM (Gain Margin), GBW, and PM across various load current ranges for STC-LDO and HP-LDO regulator are shown in Fig. 5.6 and Fig. 5.7 respectively. It can be seen that the CL-LDO is stable for the entire load current range $(I_L = 0 - 100\ mA)$ (see Fig. 5.6 and Fig. 5.7).

Root locus of the open loop transfer function (refer (4.7), (4.20) and (4.13)) at $0,\ 20\,\mu A$ and $100\,mA$ is shown in Fig. 5.8, Fig. 5.9, and Fig. 5.10 respectively. The absence of right half plane (RHP) zeros in the transfer functions yields an absolutely stable system.

The performance of the LDO in comparison with state of the art CL-LDO is shown in Table 5.2. The transient ($FOM_1$) is adopted from [1] for comparison.

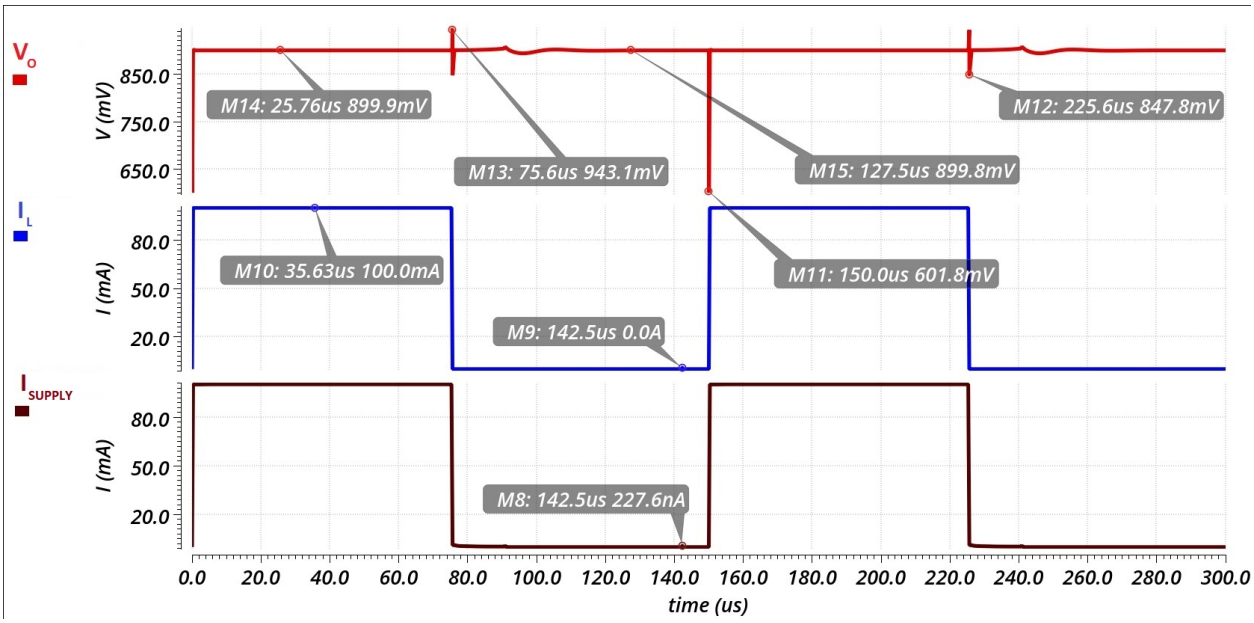


Figure 5.4: Load transient response simulation result (0 - 100 mA)

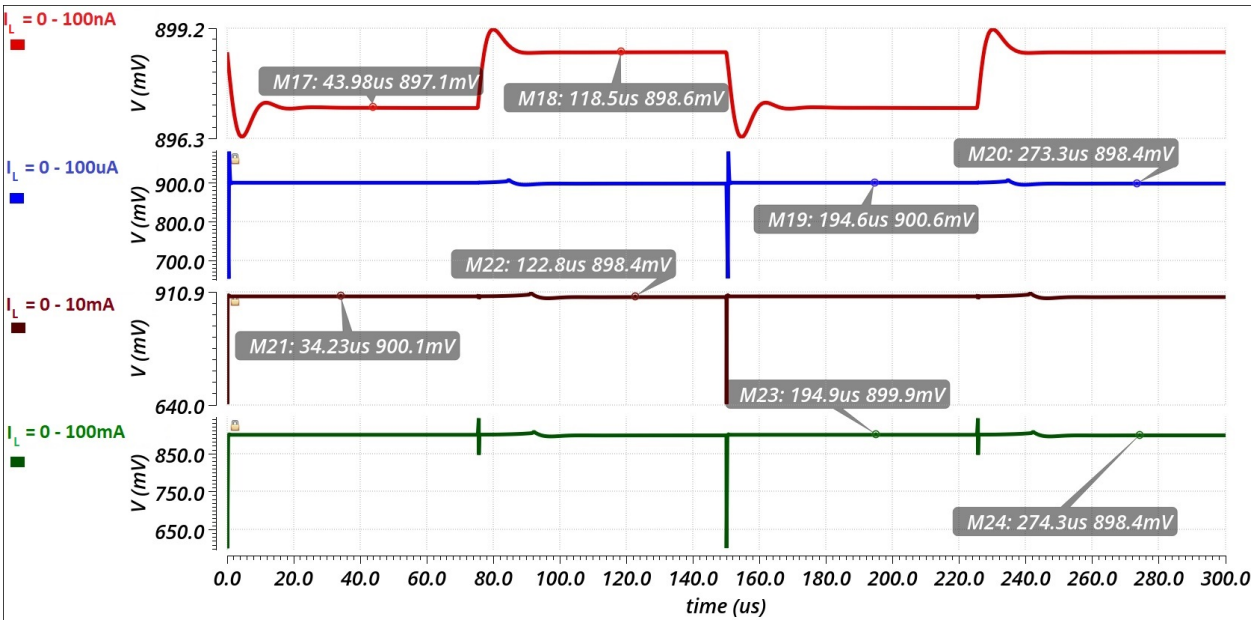


Figure 5.5: Transient response at different load currents

$FOM_1$ is defined as

$$FOM_1 = K \ \frac{\Delta V_O \ (I_{Qmin} \ + \ I_{Lmin})}{\Delta I_L} \tag{5.1}$$

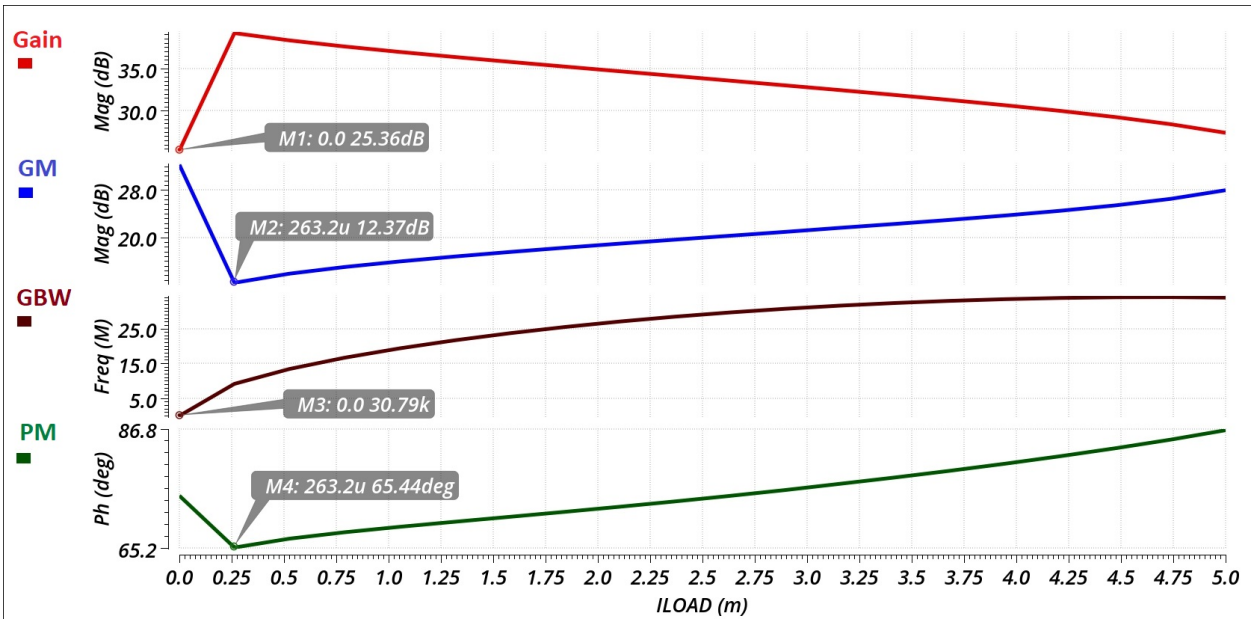


Figure 5.6: Gain, GM, GBW, PM as a function of load current (0 - 5 mA) for worst case $C_L = 100\ pF$ (STC-LDO regulator)

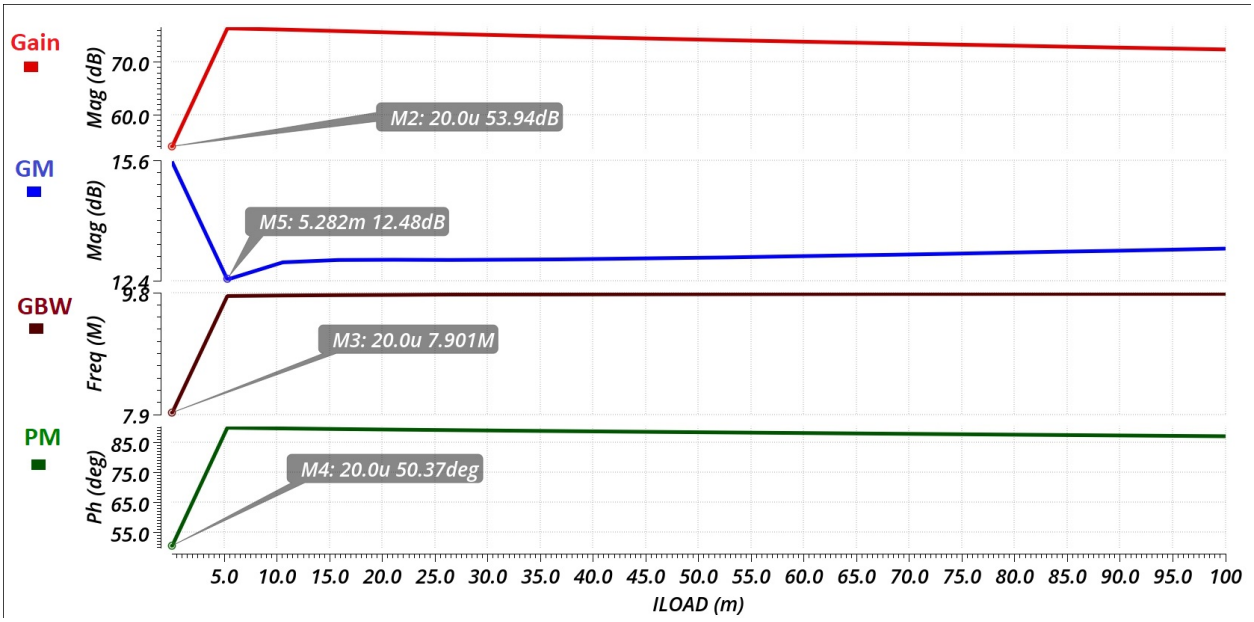


Figure 5.7: Gain,GM, GBW, PM as a function of load current (20 uA - 100 mA) for worst case $C_L = 100\ pF$ (HP-LDO regulator)

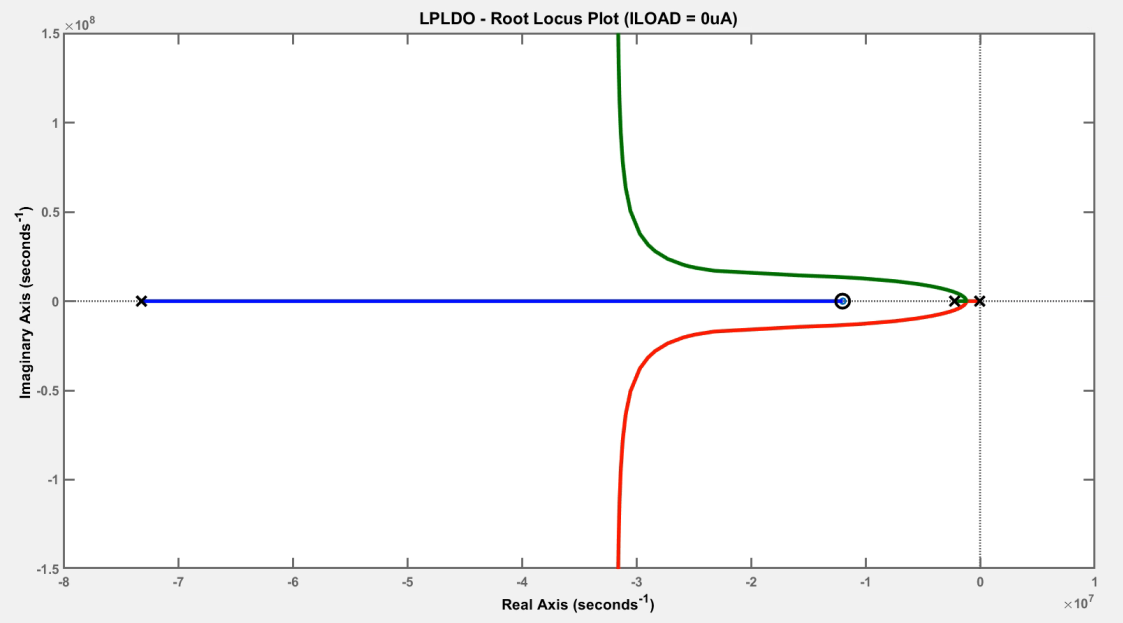


Figure 5.8: Root locus at $I_L$= 0 $\mu$A

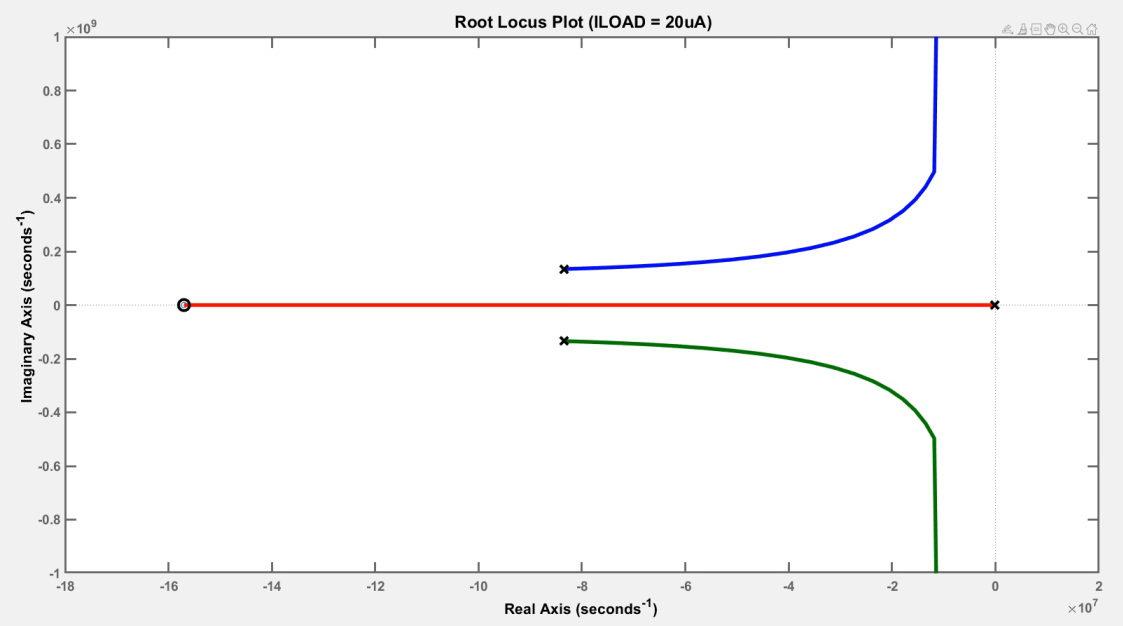


Figure 5.9: Root locus at $I_L$= 20 $\mu$A

where K is defined as

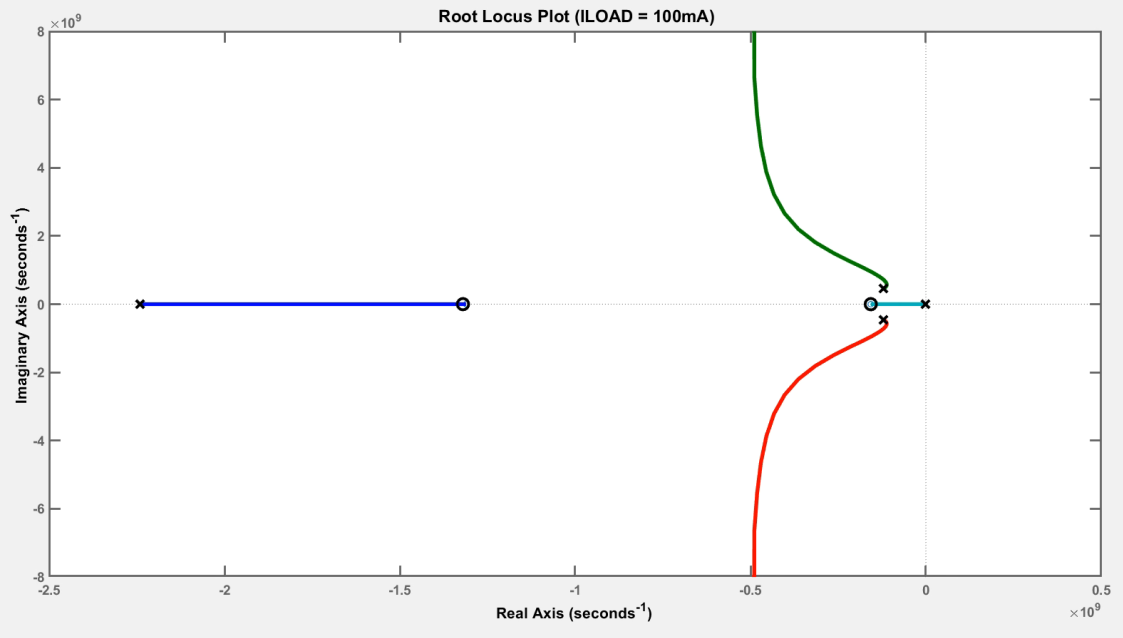


Figure 5.10: Root locus at $I_L$= 100 mA

$$K = \frac{The\ edge\ time\ of\ the\ compared\ work}{The\ smallest\ edge\ time\ in\ the\ comparison\ table} \tag{5.2}$$

The CL-LDO in this thesis shows a 5× improvement in the recovery time and simultaneously achieves a comparable $FOM_1$ to previous state-of-art CL-LDO [1]. This improvement was achieved by a combination of STC-LDO regulator, adaptively transformed 2-stage and 3-stage structures, and DOR. Fig. 5.11 and 5.12 shows the rising and falling transient response for a load current transition $0 - 100\,mA$ and vice-versa. Simulations show an overshoot of only 42 mV and a recovery time of 354 ns for $I_L$ = 0 - 100 mA load transient after the addition of distributed overshoot reduction circuitry.

The "Transient response vs. Power consumption" trade-offs for ultra-low-power systems are built into the $FOM_1$ (see Fig. 5.1). To reduce the undershoot to an acceptable 100 mV range requires 3× increases in the quiescent current consumption. Though the quiescent current is slightly higher than the quiescent current in [1], the CL-LDO still manages a 5× improvement in the recovery time.

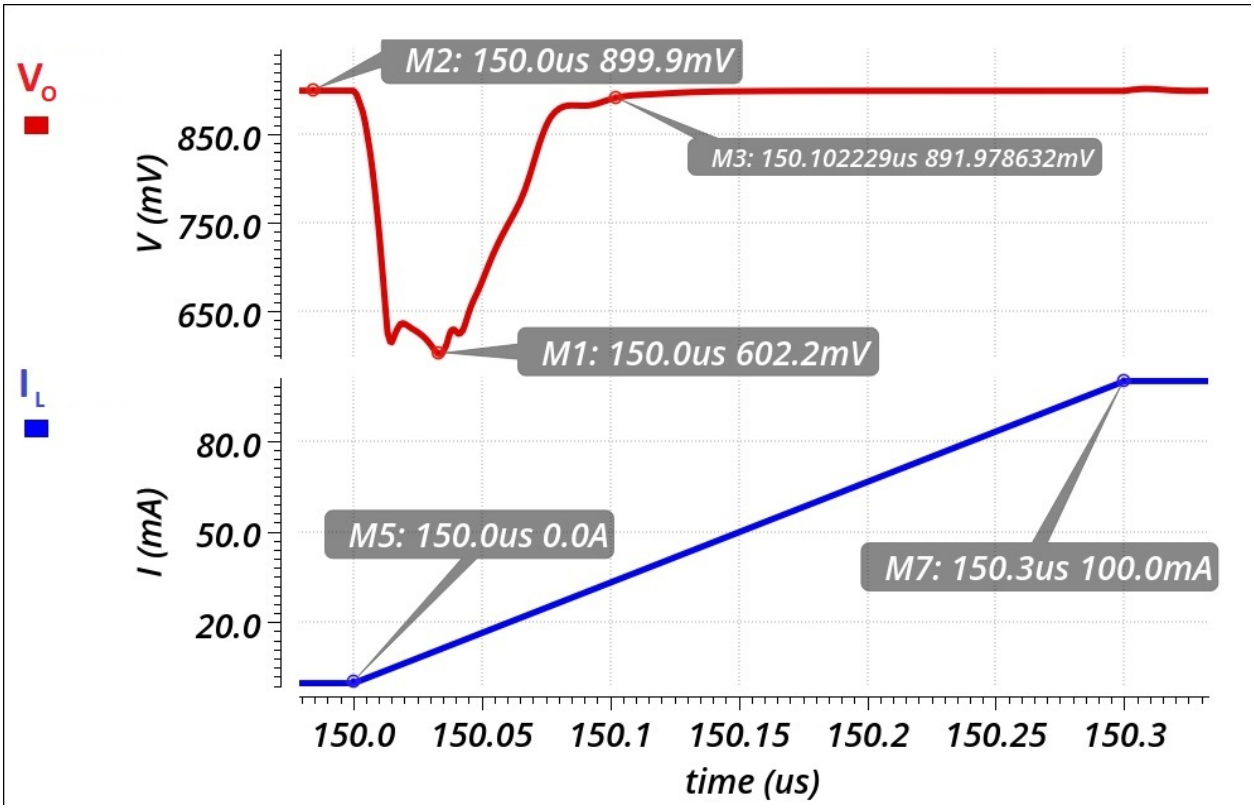


Figure 5.11: Load transient response - rising edge (0 - 100 mA)

Fig. 5.13 shows the PSRR results of the CL-LDO at full load current range. In comparison to the traditional LDO architecture shown in Fig. 1.3 , the CL-LDO in this thesis achieves superior PSRR performance. The compensation capacitor in the LDO in Fig. 1.3 acts as an AC short for moderate frequencies. The drain and the gate of the pass transistors are now connected and exhibit a diode-connected configuration at the output node. Any ripple at $V_{IN}$ appears directly at the gate of the pass transistor, and subsequently, to $V_O$ as the feedback loop maintains constant output current.

The CL-LDO in Fig. 3.2 incorporates a cascode compensation, which overcomes the above-stated supply rejection problem by decoupling the gate of the pass transistors ($M_{3h}$ and $M_{4h}$) from the compensation capacitor ($C_{1a}$), thereby yielding a significantly higher power supply rejection at moderate frequencies. The complete small analysis and the mathematics governing the above intuitive reasoning can be found in [8] - [9].

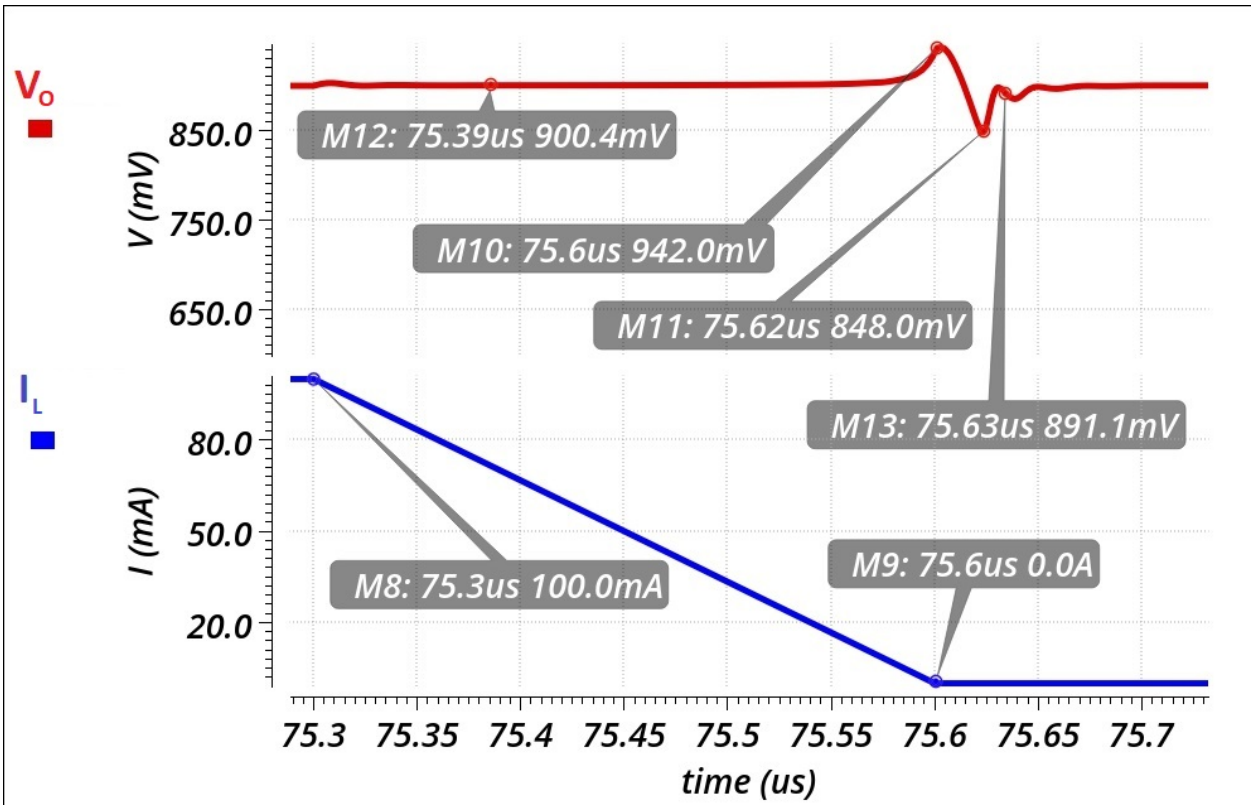


Figure 5.12: Load transient response - falling edge (100 mA - 0)

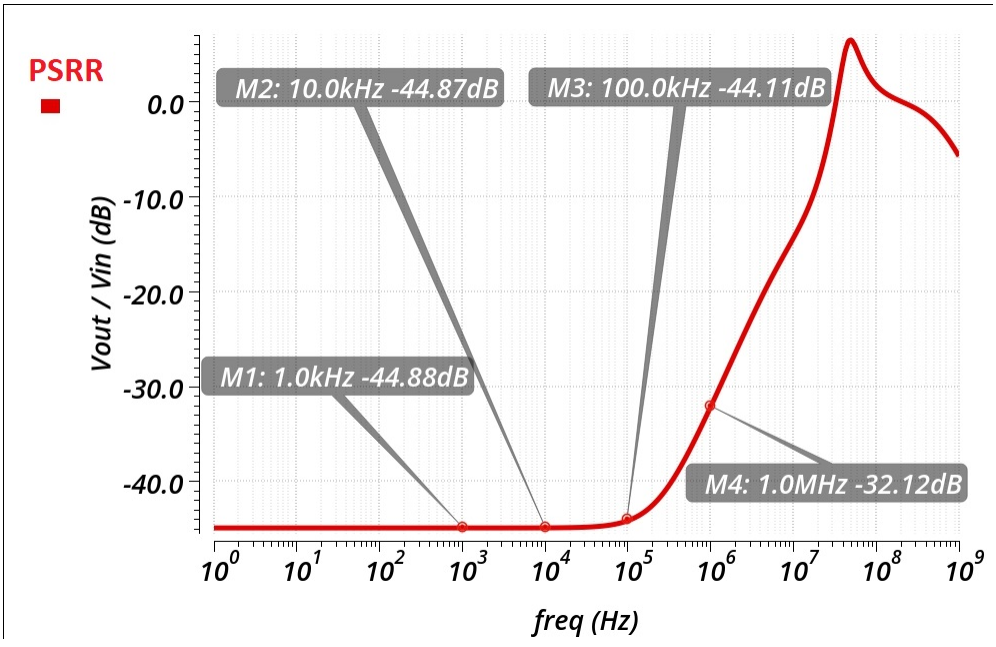


Figure 5.13: Power supply rejection ratio vs frequency at $I_L$ = 100 mA

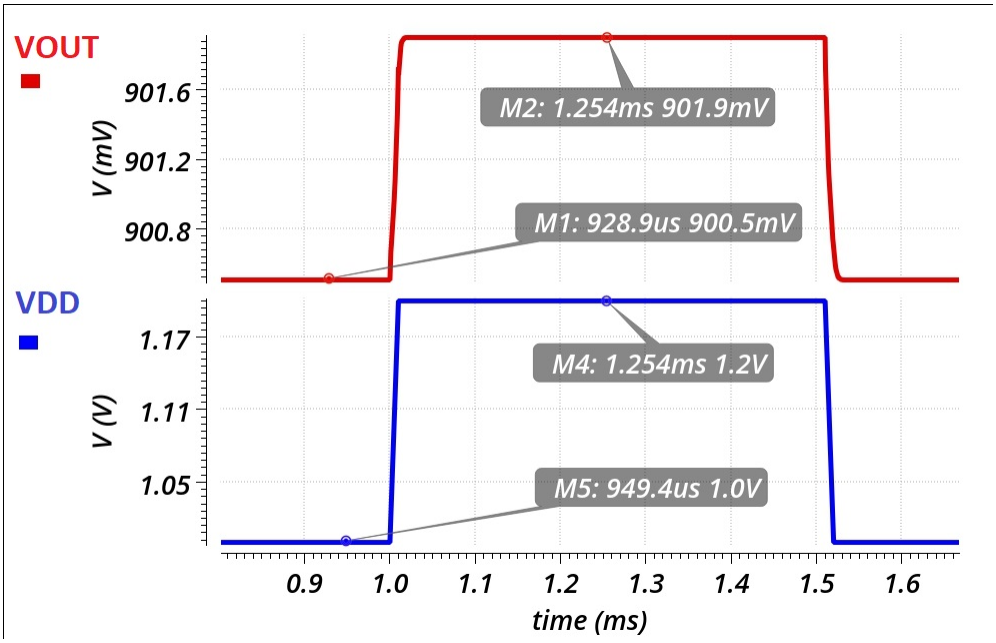


Figure 5.14: Line transient response at $I_L = 20\,\mu$A

Table 5.2: Performance comparison of the proposed LDO regulator with reported work

| *Parameter* | [10] | [11] | [12] | [4] | [13] | [14] | [15] | [16] | [17] | [18] | [1] | This work |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $Year$ | 2005 | 2010 | 2010 | 2012 | 2013 | 2014 | 2014 | 2016 | 2017 | 2018 | 2018 | 2020 |
| $CMOS\ Technology(nm)$ | 90 | 350 | 90 | 65 | 35 | 65 | 65 | 180 | 180 | 130 | 180 | 40* |
| $Chip\ Area(mm^2)$ | 0.01 | 0.145 | 0.019 | 0.017 | 0.04 | 0.0096 | 0.0133 | 0.07 | 0.033 | 0.008 | 0.055 | NA |
| $VDD\ (V)$ | 1.2 | 1.8 - 4.5 | 0.75 - 1.2 | 1.2 | 1.2 | 0.75 - 1.2 | 0.75 - 1.2 | 1.4 | 1.8 | 1 - 1.4 | 1.2 | 1.1 |
| $V_{OUT}\ (V)$ | 0.9 | 1.6 | 0.5 - 1 | 1 | 1 | 0.5 | 0.55 | 1.2 | 1.6 | 0.8 | 1 | 0.9 |
| $V_{DO}\ (V)$ | 0.3 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 | 0.2 |
| $I_{q(min)}\ (\mu A)$ | 6000 | 20 | 8 | 0.9 | 1.2 | 16.2 | 15.9 | 0.61 | 71 | 112 | 0.407 | 0.227* |
| $I_{q(max)}\ (\mu A)$ | 6000 | 20.9 | 8 | 82.4 | 14 | 16.2 | 487 | 141 | 101 | 112 | 245 | 233 |
| $I_{q(min)}(\mu A) + I_{L(min)}\ (\mu A)$ | 6000 | 20 | 3008 | 0.9 | 101.2 | 16.2 | 15.9 | 10.61 | 271 | 232 | 0.407 | 0.227* |
| $I_{L(min)}\ (\mu A)$ | 0 | 0 | 3000 | 0 | 100 | 0 | 0 | 10 | 200 | 120 | 0 | 0 |
| $I_{L(max)}\ (\mu A)$ | 100 | 100 | 100 | 100 | 100 | 50 | 50 | 100 | 100 | 25 | 100 | 0 |
| $C_T\ (pF)$ | NA | 7 | 7 | 9 | 2 | 4.1 | 9 | 12.7 | 0.73 | 6.5 | 4 | |
| $C_{OUT}\ (pF)$ | 600 | 100 | 50 | 100 | 100 | 100 | 470 | 100 | 100 | 25 | 100 | 100 |
| $Line\ Regulation\ (mV/V)$ | NA | 0.0574 | 3.78 | 4.7 | NA | 0.56 | 4 | 0.6 | NA | 2.25 | 0.283 | 4.8 |
| $Load\ Regulation\ (mV/mA)$ | 0.9 | 0.109 | 0.1 | 0.3 | NA | 6.67 | 0.18 | 0.27 | NA | 0.173 | 0.077 | 0.0379 |
| $PSRR\ (dB)\ Frequency\ (Hz)$ | NA | -40 @ 10k | -44 @ 1k | -58 @ 10k | NA | -46 @ 1k | -51 @ 1k | -26 @ 1M | -76 @ 1M | -57 @ 1M | -37.7 @ 1M | -32.12 @1M |
| $T_R\ (\mu sec)$ | 0.00054 | 9 | 4 | 6 | 2.7 | 1.2 | 0.25 | 7.7 | 0.2 | 0.19 | 1.56 | 0.354* |
| $\Delta\ V_{OUT}\ (mV)$ | 90 | 97 | 114 | 68.8 | 270 | 103 | 113 | 110 | 110 | 284 | 117 | 298 |
| $T_{edge}\ (ns)$ | 0.1 | 100 | 100 | 300 | NA | 100 | 100 | 1000 | 100 | 0.3 | 300 | 300 |
| $Edge\ Time\ Ratio\ (K)$ | 1 | 1000 | 1000 | 3000 | NA | 1000 | 1000 | 10000 | 1000 | 3 | 3000 | 3000 |
| $FOM1\ (mV)$ | 5.4 | 19.4 | 3429 | 1.86 | NA | 33.4 | 35.94 | 116.71 | 298 | 7.9 | 1.42 | 2.02 |
| $FOM2\ (mV)$ | 5.4 | 20.3 | 9.12 | 170 | NA | 33.4 | 1100.7 | 1551 | 11.1 | 3.8 | 854 | 1123 |
| $Current\ Efficiency\ (\%)$ | 99.43 | 99.97 | 99.99 | 99.91 | 99.98 | 99.96 | 99.04 | 99.85 | 99.89 | 99.5 | 99.75 | 99.77 |

# 6. SUMMARY AND CONCLUSION

The proposed CL-LDO is designed in 40 nm CMOS process. The adaptive structural transformation enables the CL-LDO to achieve a very good recovery time. Additionally, it decouples the HP-LDO regulator from adaptive bias and enables optimizing the other design parameters of the HP-LDO regulator in the high-load current range. Complete load current range $(0 - 100\,mA)$ stability is achieved at a maximum load parasitic capacitance of $100\,pF$. For a rising load current transient $(0 - 100\,mA)$, the LDO achieves a recovery time of 101 ns, and an undershoot of 292 mV is observed at the output. For falling load current transient $(100\,mA - 0)$, the LDO achieves a recovery time of 354 ns, and an overshoot of 42 mV is observed at the output. Overall, the structural transformation proposed in this thesis enables the CL-LDO to achieve a very good recovery time with a simultaneous 220 nA quiescent current and is balanced in performance in terms of PSRR (Fig. 5.13), line regulation (Fig. 5.14), and load regulation. In the future, the improvement of the low-frequency gain of the STC-LDO regulator can be a vital factor in extending the adaptive structural transformation to micro-power sensors.

# REFERENCES


[1] Y. Jiang, D. Wang, and P. K. Chan, "A quiescent 407-na output-capacitorless low-dropout regulator with 0–100-ma load current range," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 5, pp. 1093–1104, 2019.

[2] Bang S. Lee, "Understanding the Terms and Definitions of LDO Voltage Regulators," *Texas Instruments, Application Note*, 1999.

[3] G.A. Rincon-Mora, "Analog IC Design with Low-Dropout Regulators," *McGraw-Hill, Second Edition*, 2014.

[4] S. Chong and P. K. Chan, "A 0.9ua quiescent current output-capacitorless ldo regulator with adaptive power transistors in 65-nm cmos," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 4, pp. 1072–1081, 2013.

[5] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of single-transistor-control ldo based on flipped voltage follower for soc," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 5, pp. 1392–1401, 2008.

[6] Y. Hwang, M. Lin, B. Hwang, and J. Chen, "A 0.35um cmos sub-1v low-quiescent-current low-dropout regulator," in *2008 IEEE Asian Solid-State Circuits Conference*, pp. 153–156, 2008.

[7] I. Lee, D. Sylvester, and D. Blaauw, "A subthreshold voltage reference with scalable output voltage for low-power iot systems," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 5, pp. 1443–1449, 2017.

[8] D. B. Ribner and M. A. Copeland, "Design techniques for cascoded cmos op amps with improved psrr and common-mode input range," *IEEE Journal of Solid-State Circuits*, vol. 19, no. 6, pp. 919–925, 1984.

[9] B. K. Ahuja, "An improved frequency compensation technique for cmos operational amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 18, no. 6, pp. 629–633, 1983.

[10] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 4, pp. 933–940, 2005.

[11] E. N. Y. Ho and P. K. T. Mok, "A capacitor-less cmos active feedback low-dropout regulator with slew-rate enhancement for portable on-chip application," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 2, pp. 80–84, 2010.

[12] J. Guo and K. N. Leung, "A 6-$\mu$ w chip-area-efficient output-capacitorless ldo in 90-nm cmos technology," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1896–1905, 2010.

[13] X. Qu, Z. Zhou, B. Zhang, and Z. Li, "An ultralow-power fast-transient capacitor-free low-dropout regulator with assistant push–pull output stage," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 2, pp. 96–100, 2013.

[14] S. S. Chong and P. K. Chan, "A sub-1 v transient-enhanced output-capacitorless ldo regulator with push–pull composite power transistor," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 11, pp. 2297–2306, 2014.

[15] X. L. Tan, S. S. Chong, P. K. Chan, and U. Dasgupta, "A ldo regulator with weighted current feedback technique for 0.47 nf–10 nf capacitive load," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2658–2672, 2014.

[16] A. Maity and A. Patra, "Tradeoffs aware design procedure for an adaptively biased capacitorless low dropout regulator using nested miller compensation," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 369–380, 2016.

[17] S. J. Yun, J. S. Yun, and Y. S. Kim, "Capless ldo regulator achieving -76 db psr and 96.3 fs fom," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 10, pp. 1147–1151, 2017.

[18] S. Bu, J. Guo, and K. N. Leung, "A 200-ps-response-time output-capacitorless low-dropout regulator with unity-gain bandwidth >100 mhz in 130-nm cmos," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 3232–3246, 2018.

# APPENDIX A

## CORNER SIMULATIONS

The LDO was simulated across different process, temperature, and voltage (PVT) corners. The testing was restricted to check the sensitivity of the circuit and ensure that it was not too sensitive to PVT. Fig. A.1 shows the sample transient simulation results for $I_L = 0 - 100\ mA$ transition at a worst-case load capacitance $(C_L = 100\ pF)$.

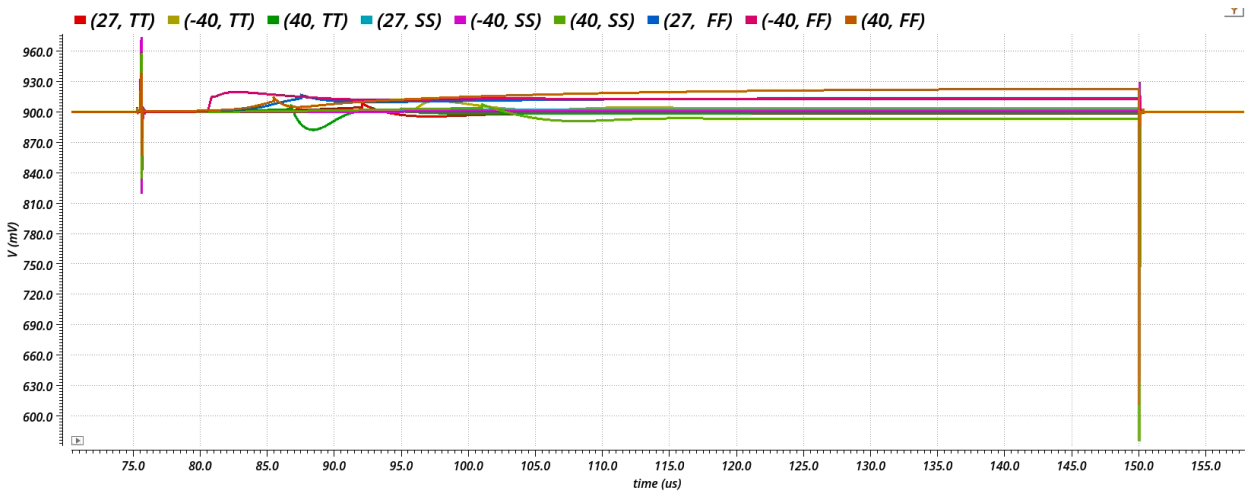


Figure A.1: Transient simulation results ($V_O$ vs time) as load current is switched from 0 to 100 mA, Temperature = -40° to 40°, VDD = 1.1 V