A SELF-CALIBRATED POWER DETECTOR AND CURRENT SENSOR FOR USE IN A POWER AMPLIFIER CONTROL CIRCUIT

A Thesis

by

JAMES KEITH LUNSFORD

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Chair of Committee,	Aydin Karsilayan
Co-Chair of Committee,	Jose Silva-Martinez
Committee Members,	Robert Nevels
	Jay Porter
Head of Department,	Miroslav Begovic

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ABSTRACT

The power amplifier in a transmitter, especially high-power transmitters, generally uses more power than any other component in the signal chain. As a result, large power savings can be achieved if the efficiency of the power amplifier is optimized. Additionally, power amplifiers in high-power transmitters generally experience substantial amounts of reliability-reducing stress such as high temperature operation. Given these considerations, a power amplifier control loop is proposed which will calculate various parameters of the amplifier, such as the power-added efficiency. This control loop will then adjust the input power and DC bias current of the power amplifier to maximize the efficiency while also ensuing the amplifier is not placed in a situation where its reliability is compromised. This thesis will discuss the design of two major blocks that are required in this control loop: a DC bias current sensor and a power detector.

The DC bias current sensor must accurately measure the DC bias of the power amplifier since this current is used to calculate the DC power dissipation for the power-added efficiency. In order to ensure the DC current sensor's output is accurate over a wide temperature range, a reference current calibration scheme is introduced. The fabricated current sensor is able to achieve a measurement accuracy of +/-1% over a current range from 100mA to 4A.

The power detector must measure the input and output power of the power amplifier since the power added efficiency takes into account the gain of the amplifier. The proposed power detector utilizes an on-chip reference generator in order to calibrate

the peak detector used and provide an accurate and absolute power level. The simulated power detector is able to provide an accuracy of +/-0.5dB over a dynamic range of 40dB. These two designs will be incorporated in the overall power amplifier control system in future work.

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TABLE OF CONTENTS

Page

ABSTRACT ii

ACKNOWLEDGEMENTS iv

CONTRIBUTORS AND FUNDING SOURCES vi

TABLE OF CONTENTS vii

LIST OF FIGURES ix

LIST OF TABLES xiii

1. INTRODUCTION 1

1.1. Motivation 1
1.2. Organization of the thesis 5

2. INTRODUCTION TO POWER DETECTORS AND CURRENT SENSORS 6

2.1. Power Detectors 6
2.1.1 RMS Power Detectors 9
2.1.2 Peak Power Detectors 15
2.2 Current Sensors 19

3. PROPOSED CURRENT SENSOR 27

3.1 Current Sensor Architecture 27
3.2.1 Problem Description 27
3.2.2 Architecture Overview 29
3.2 Implementation of Current Sensor 40
3.1.1 Input Buffer 40
3.1.2 ADC 48
3.1.3 Reference Current Source 58
3.1.4 Level-Shifting Capacitors 67
3.1.5 Digital Control Block 70
3.1.6 Startup Protection 71
3.1.7 Top-Level Simulations 74
3.3 Current Sensor Measurements 76

4. PROPOSED POWER DETECTOR 85

4.1 Power Detector Architecture 85
4.1.1 Problem Description 85
4.1.2 Architecture Overview 86
4.2 Implementation of Power Detector 93
4.2.1 Peak Detectors 93
4.2.2 Sine-Wave Generator 99
4.2.3 Amplifier 112
4.2.4 ADC 116
4.2.6 Digital Controller 117
4.2.5 Top-Level Simulations 117
4.3 Power Detector Measurements 119

5. SUMARY AND CONCLUSIONS 124

REFERENCES 126

LIST OF FIGURES

Page

Figure 1: Power Amplifier Control System Overview....3
Figure 2. Standard Transmitter Chain with Power Detector....4
Figure 3. Typical PA Current Measurement Setup....5
Figure 4. Comparison Between Various Power Definitions....9
Figure 5. Basic Translinear Loop....12
Figure 6. Peak Detector Schematic....13
Figure 7. Diode-based Peak Detector....16
Figure 8. Typical Series-Resistor Sensing Scheme....21
Figure 9. Basic Sense-FET Scheme....24
Figure 10. Capacitor-Based Current Sensor Operation....26
Figure 11. Copper Resistivity over Temperature....29
Figure 12. Current Sensor Architecture....30
Figure 13. Level Shifting Capacitors....31
Figure 14. ADC and Supporting Circuitry....32
Figure 15. Effect of Chopping on the DC Input Signal....33
Figure 16. Input Square Wave with Moving-Average Filter Responses....36
Figure 17. Input Noise and Output Noise after Moving-Average Filters....37
Figure 18. Reference Current Calibration Circuit....38
Figure 19. Fully-Differential Differential Difference Amplifier....42
Figure 20. FDDA Schematic....43
Figure 21. CMFB Circuit for FDDA....44
Figure 22. FDDA Buffer Bandwidth Results....45

Figure 23. FDDA Buffer Gain Error Results 46
Figure 24. Buffer Offset Simulations 47
Figure 25. Buffer Squared Input Noise 47
Figure 26. ADC Topology 48
Figure 27. Loop Filter Op-amp 51
Figure 28. CMFB Amplifier for Loop Filter Op-amp 52
Figure 29. Loop Filter Op-amp Bandwidth 52
Figure 30. Loop Filter Op-amp Phase Margin 53
Figure 31. Loop Filter Op-amp Gain 54
Figure 32. Strong-ARM Comparator 55
Figure 33. Falling Delay of Quantizer 56
Figure 34. Rising Delay of Quantizer 57
Figure 35. 1-bit DAC 57
Figure 36. Reference Current Source Schematic 58
Figure 37. Bandgap Voltage Reference Schematic 60
Figure 38. Chopper-Modulated Op-Amp 61
Figure 39. Bandgap Op-amp Offset 62
Figure 40. Bandgap Output Voltage 63
Figure 41. Reference Current Source Current Mirror 64
Figure 42. Reference Current Output 65
Figure 43. Maximum Temperature-Induced Error for each Monte-Carlo Iteration 66
Figure 44. Current Mirror Mismatch Error 66
Figure 45. V_{DD} Interface Chip 67
Figure 46. Interface Chip Schematic for Negative and Gate Supplies 69

Figure 47. Sensor Measurement Timing 70
Figure 48. Reference Current Source Protection 71
Figure 49. Buffer Interface Protection 73
Figure 50. VDD Static and Transient Clamps 73
Figure 51. Interface Voltages During Startup 74
Figure 52. Current Source PCB Schematic 76
Figure 53. Current Source PCB 77
Figure 54. Current Sensor PCB 78
Figure 55. Current Sensor Chip Micrograph 79
Figure 56. Current Sensor Status Bits 80
Figure 57. Sigma-Delta Output Bit stream 81
Figure 58. Detected Current from Current Sensor 81
Figure 59. Detection Error for DC Input 82
Figure 60. Detection Error for Various Input Current Ripple Amplitudes 83
Figure 61. Detection Error for V_{SS} Supply 84
Figure 62. Previous Power Detector Architecture 87
Figure 63. Peak Detector DC Output vs. Input Amplitude 88
Figure 64. Peak Detector Gain 90
Figure 65. PD Output Showing Significant Ripple 91
Figure 66. Proposed Peak Detector Architecture 92
Figure 67. Peak Detector 93
Figure 68. Peak Detector Outputs with Mismatch 97
Figure 69. Amplitude Detection Error due to Mismatch 98
Figure 70. Amplitude Detection Error with Offset Correction 99

Figure 71. DAC Topology 100
Figure 72. DAC Element 102
Figure 73. High-Crossing Switch Driver 103
Figure 74. DAC Bias Generator 104
Figure 75. DAC DNL 105
Figure 76. DAC INL 105
Figure 77. DAC Filter Output THD 106
Figure 78. DAC Output Amplitude Variation 107
Figure 79. Filter Schematic 107
Figure 80. Filter Op-amp 109
Figure 81. Differential to Single-Ended Converter 110
Figure 82. Rail-to-Rail Operational Amplifier 111
Figure 83. Filter Tuning Results 112
Figure 84. Amplifier with Gain Control Switches 114
Figure 85. Output Voltage for Instrumentation Amplifier 115
Figure 86. Gain for Instrumentation Amplifier 116
Figure 87. Error Distribution in Percent of Power Detector 118
Figure 88. Top-Level Simulation Error Results 119
Figure 89. Power Detector Test PCB 120
Figure 90. Measured Amplitude from Power Detector 121
Figure 91. Measurement Error for F=4GHz, PRF=10MHz 122
Figure 92. Measurement Error for PRF=1MHz, DC=50% 122
Figure 93. Measurement Error for F=4GHz, DC=5% 123

LIST OF TABLES

Page

Table 1. Comparison of RMS Power Detectors 14

Table 2. Current Sensor Topology Comparison 26

Table 3. Current Range and Accuracy Requirements 27

Table 4. Requirements for Input Buffer 41

Table 5. Current Sensor Post-Layout Simulation Results 75

Table 6. Power Detector Requirements 86

1. INTRODUCTION

1.1. Motivation

The current demand for transmitters in mobile communications exceeds 6 billion units per year, and it is expected that this demand will increase in the near future. Improving the power efficiency and yield of high-performance transmitters will have significant impact on the efficiency, reliability, and production cost of these transmitters and will ensure sustainable growth of the consumer electronics industry. The military sectors will also benefit from monitoring systems that are able to accurately measure power amplifier gain and bias current to optimize it for power efficiency in demanding applications with very high power levels. A major goal of this research is the design of robust yet efficient power and current monitoring systems with digital output that allow the use of digital methodologies to adjust various power amplifier (PA) parameters during operation.

Radio-frequency (RF) PAs are a vital component of wireless communication systems to-day, significantly impacting the daily lives of people around the world. However, significant challenges arise in PAs due to the large amount of power that they must output. Indeed, PAs have been described by many as an incredibly inefficient piece of hardware [1]. In mobile hand-sets, for instance, RF PAs can consume up to 65% of the total power when transmitting, playing a major role in the limitation of battery life [2]. Inefficiencies in RF PAs also directly correlate with the generation of waste heat, threatening the reliability of the system due to extreme temperature exposure. Whether embedded in a cellphone or a military defense radar, transmitters are integral to modern

infrastructure, and their efficiency has long been a major bottleneck of system performance. This work deals with the design of two BiCMOS sensors to accurately measure the DC bias current and input and output power levels of high power gain PAs delivering up to 28-54dBm power while operating in the range of 2-6GHz to cover multiple standards.

A PA control circuit which will measure in real-time the performance of the PA and dynamically adjust its operating conditions to optimize the efficiency of the system is proposed. The controller will treat the PA as a "black box", with no direct access to any PA nodes except its input and output paths. This PA control circuit will be integrated onto a single chip in order to maximize reliability and minimize the footprint as well as the manufacturing and assembly costs for the system. The proposed controller will measure the RF PA's input power, output power, drain current, gate current, and temperature. The system will pass the digital information from these sensors to a computational engine (CE), which will use the information to calculate the power-added efficiency (PAE) and estimate the peak channel temperature of the PA. The CE will use the same information to simultaneously maximize output power and PAE while maintaining gate current and channel temperature within acceptable limits. Again, the entirety of the controller will be implemented in a single integrated circuit (IC), separate the RF PA itself. See Figure 1 for a block diagram of the proposed system controlling a power amplifier. This research specifically will deal with the gate and drain current sensors as well as the input and output power sensors.

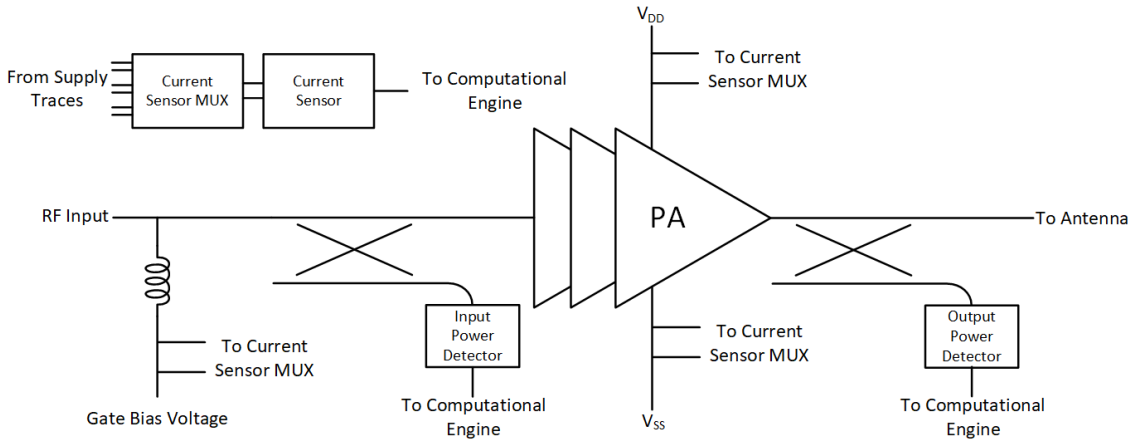

Figure 1: Power Amplifier Control System Overview

Figure 2 below shows the standard transmitter signal chain with the power amplifier driving the transmitter's antenna. A directional coupler is typically used to obtain a small portion of the PA's output power or input power which is then converted into a low frequency voltage using a power detector which, in turn, is digitized using a digital-to-analog converter. This digitized measure of the PA's output power is then processed by the digital baseband processor and the gain of the power amplifier is adjusted to provide the desired output power. This output power may be set based on the maximum output power possible to maintain the desired reliability of the power amplifier or it may be set based on the minimum power required to achieve a given accuracy or range for a radar or communication system.

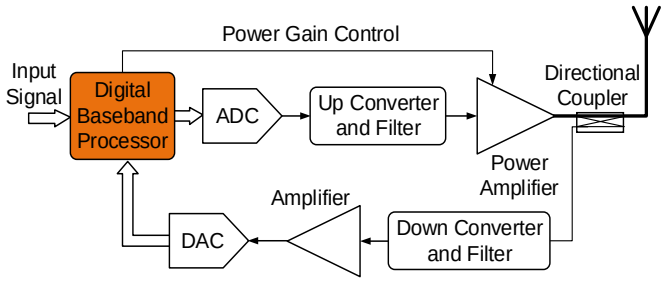

Figure 2. Standard Transmitter Chain with Power Detector

Not shown in Figure 2 above is the current sensor for the power amplifier. This is shown in more detail in Figure 3 below. Power amplifiers, especially those utilizing III-IV HEMT transistors with on-chip drain modulators, will generally have three different currents to be measured. The first is the supply current that feeds the main gain transistor of the PA, or the V_{DD} supply. The bias current through this supply can provide information on the power-added efficiency (PAE) of the PA. Indeed, knowing the PAE of the PA can allow the gate bias to be adjusted to achieve optimal (maximum) PAE. The second is the supply current associated with the on-chip drain modulator, or the (negative) V_{SS} supply [3]. The third current is associated with the gate bias supply which, during normal operation, should be low since the Schottky diodes associated with the gate input are typically reverse biased. However, certain conditions, such as those caused by amplifier gain variation over temperature, may cause a large forward bias current to flow through the gate [4]. It is therefore useful to monitor the current through the gate bias supply since large forward bias current through the gate of the PA's transistor can cause permanent damage or greatly reduce reliability.

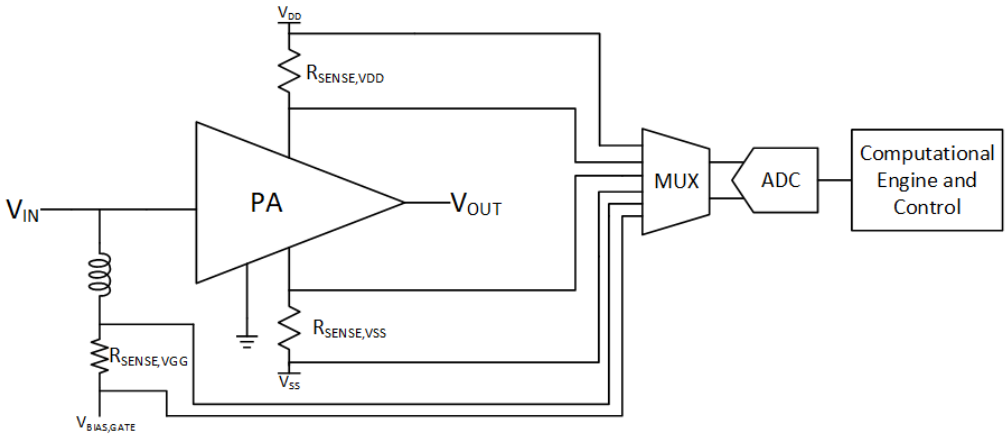

Figure 3. Typical PA Current Measurement Setup

1.2. Organization of the thesis

Section 2 of this thesis will present the fundamental principles of power detection and current sensing. Previous topologies as well as important performance characteristics for both will be presented.

Sections 3 and 4 of this thesis will discuss the architecture of the proposed current sensor and power detector, respectively. Motivation behind the various architectural decisions made will be presented as well as block-level simulations of the components required in the design. Top level simulations along with the various error sources in each design will be presented. Lastly, measurement results for each sensor will be presented.

Section 5 of this thesis will provide a summary and some conclusions.

2. INTRODUCTION TO POWER DETECTORS AND CURRENT SENSORS

This section will provide an overview of the processes of power detection and current sensing as well as the performance metrics used to characterize these systems. Various topologies previously reported for both systems will be discussed, and each topology will be compared in terms of its advantages and disadvantages in the application targeted by this research.

2.1. Power Detectors

The purpose of the power detector in a transmitter is to provide an estimate of the input and/or output power of the PA. If both the input and the output power are measured, the power gain of the PA can be calculated and can be adjusted to the desired or optimum value. Additionally, the power-added efficiency (PAE) of the PA can also be calculated. This will be discussed in section 2.2 below. Alternatively, the output power alone can be adjusted to the level required for the desired accuracy/range of the system, to the maximum reliable output power level, or to a level required by the communication standard the system is utilizing. Based on these varying requirements, there are two main types of measurements that various power detectors provide. The first measurement type is the RMS power which provides a measure of the average power at the output of the PA. The second type is the peak envelope power detector which provides an output that tracks with the power of the input signal's modulating envelope.

RMS power detectors are generally useful in communication systems utilizing modulation schemes with high modulation bandwidths. These communication systems are generally governed by standards that specify minimum or maximum output powers

based on the average power [5]. Additionally, the high modulation bandwidth of these systems generally means that peak envelope power detectors are unable to accurately track the modulation envelope of the input signal. Therefore, the average power, which inherently requires low-pass filtering, provides a more accurate measure.

On the other hand, peak envelope power detectors are generally useful in communication systems with lower modulation bandwidths or in other systems such as radar [9]. Indeed, peak power measurements can provide a much better estimation of the power radiated during a radar's "on" period which determines important radar characteristics such as the achievable range. Additionally, the peak power measurement also provides a good measure of the stress placed on the power amplifier. Therefore, if the purpose of the PA feedback loop found in Figure 2 is to improve the reliability of a high output-power PA, the peak power should be measured. Since the ultimate target application of this research is radar systems, the peak power will be measured. Nonetheless, since RMS power detectors are much more prevalent in the literature, the power detector presented in this research will be compared against RMS detectors and RMS detectors will be discussed in the following section.

Figure 4 below shows a comparison between the various power detector definitions. The signal being examined has a frequency of 100MHz and an amplitude of 100mV from time 0 to 0.4µs, an amplitude of 200mV from 0.4µs to 0.7µs, and an amplitude of 100mV from 0.7µs to 1µs. The instantaneous power is calculated using the input voltage and assuming this is referred to a 50Ω source. Therefore:

$$P_{inst} = \frac{V(t)^2}{50\Omega} \tag{1}$$

Since the incoming signal in real transmitter designs may be upwards of several GHz, it is impractical to attempt to measure the instantaneous power. Therefore, it is more reasonable to measure the average power, as described above. This power is measured by measuring the RMS voltage of the input signal and is also plotted in Figure 3 below. Since the RMS voltage is computed as an average over a period of time, the average power remains theoretically constant over this time. In practical systems, this is accomplished by lowpass filtering with a low bandwidth. The next power measure shown is the peak envelope power. Typically, the peak envelope power is obtained by measuring the peak power and ensuring the bandwidth of the filter following the peak power detector is high enough that it can track the modulation envelope of the signal. Therefore, the bandwidth of a peak envelope power detector must be higher than the modulation envelope but lower than the carrier signal's bandwidth [9]. This research will implement a peak hold power detector which measures the power at a particular point of the input signal and provides an output with the power at that point. In this case, the peak hold power at the end of the radar's "on" period will be provided.

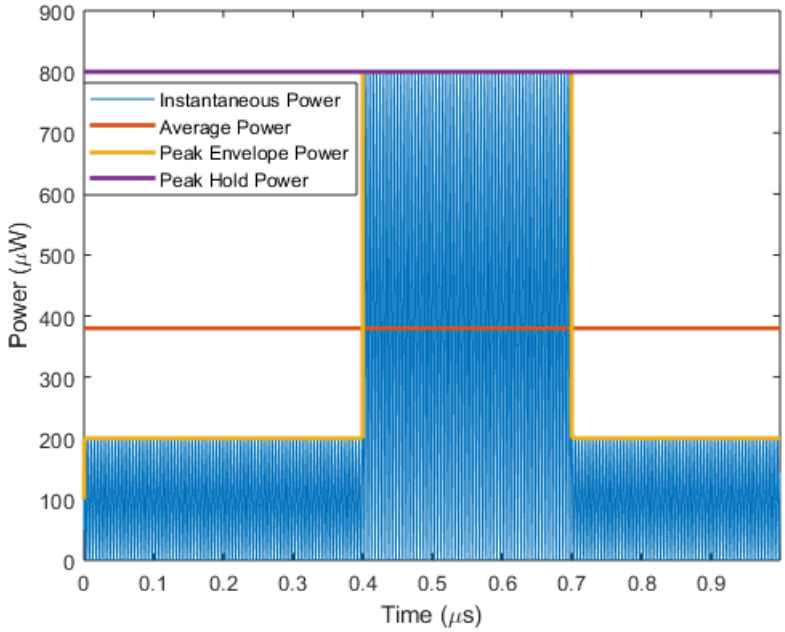

Figure 4. Comparison Between Various Power Definitions

2.1.1 RMS Power Detectors

The RMS power of a signal is obtained by first finding the RMS voltage of the signal [6]:

$$V_{rms} = \sqrt{avg[V^2(t)]} = \sqrt{\frac{1}{t_2 - t_1} \cdot \int_{t_1}^{t_2} |V(t)|^2 dt} \quad (2)$$

Where V(t) is the input voltage and t_1 and t_2 are the times during which the rms voltage is to be measured. The rms voltage can then be used to find the average power of the signal referenced to 50Ω:

$$P_{ave} = \frac{V_{rms}^2}{50\Omega} \quad (3)$$

We can see from (2) that there are two basic operations that must be performed to find the RMS value of the input voltage. First, the signal must be squared and then that

squared voltage must be averaged. Various RMS power detectors differ in the ways they perform these two operations.

There are also several performance metrics used to distinguish among the performance of various power detectors. One metric is the dynamic range achievable by the detector. This dynamic range defines the input range over which the output power estimate is valid. Therefore, it is important that an acceptable error be specified along with the dynamic range. For example, a dynamic range of 20dB with an error of 1dB indicates that the valid input range is 20dB wide (or over a factor of 100 in power), and within that 20dB range, the maximum error between the detector's output and its "ideal" output is 1dB. Another important measure of the power detector's performance is the operating frequency range over which the dynamic range is valid. While the requirement for the operating frequency may vary from application to application, RF power detectors for communication systems and radar must generally cover up to several GHz of range. A final measure of power detector performance is its power consumption. Since these power detectors may be used in battery-powered transmitters, the power consumption of the power detector should be as low as possible to ensure it does not have an adverse effect on the battery life of the device.

It is also important to note that the "ideal" output used in the dynamic range performance specification changes from detector to detector. For most power detectors [6-8], the output is simply a voltage. Therefore, the ideal output is obtained by measuring the output voltage over a wide range of input voltages and finding the linear range. A linear best-fit curve is then applied to this linear range and each measured point is

compared to this best-fit curve. Therefore, most detectors will require calibration when placed in the final system so that the baseband processor knows which output voltage corresponds to which input signal power level [9].

The RMS detector reported in [6] utilizes the square law characteristics of MOS transistors in strong inversion to perform the squaring operation and a low pass filter to perform the averaging. The input voltage is converted into a current that has terms proportional to the square of the input voltage:

$$i_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{in} - V_t)^2 = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{in}^2 - 2V_{in}V_t + V_t^2) \tag{4}$$

This design also utilizes the exponential behavior of MOS transistors in weak inversion to convert the output of the lowpass filter to a linear-in-decibel output:

$$i_{ds} = \frac{W}{L} I_{D0} exp\left(\frac{qV_{in}}{nkT}\right) \tag{5}$$

This linear-in-decibel output can then be used by the baseband processor to set the output power. This detector provides a linear output characteristic over a range of 20dB at 5.5GHz with a maximum error of 0.5dB.

Another RMS detector topology is reported in [7] and utilizes a translinear loop, which is described in detail in [10] and is shown in its basic form in Figure 5 below, to perform the squaring and averaging operations using one single loop. The output current of this circuit can be shown to be:

$$I_{out} = \frac{\frac{I_{in}^2}{I_{DC}}}{1 + \frac{sCV_T}{I_{DC}}} \tag{6}$$

From (6), we see that the input current is squared and is also low-pass filtered by the capacitor at the emitter of Q_3. Therefore, we see that the squaring and averaging operations are accomplished by this single translinear loop. This design achieves an impressive dynamic range of 40dB, but this dynamic range is only achieved at 1.3GHz. Indeed, translinear-based power detectors can generally only operate at lower frequencies.

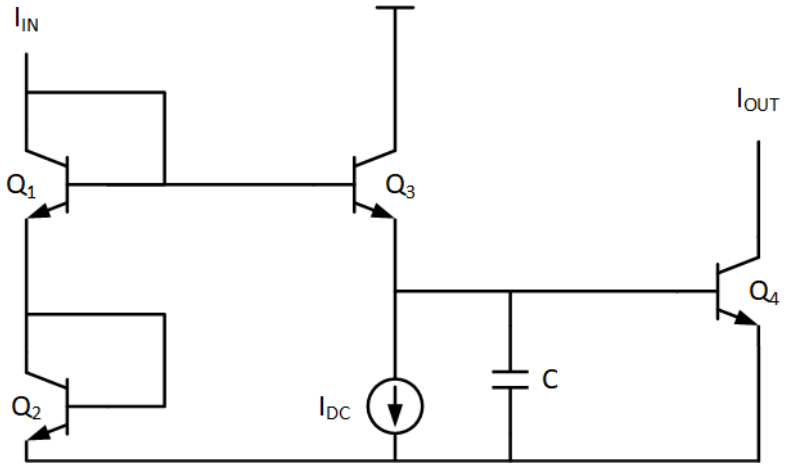

Figure 5. Basic Translinear Loop

Another RMS power detection design previously reported in [8] also utilizes the square-law behavior of MOS transistors in strong inversion to generate an output current proportional to the square of the input voltage. This current is then directed to a TIA which converts it into a voltage. The main contribution of this design is the implementation of segmenting gain amplifiers which boost low input signals into the dynamic range of the detector where the output characteristic is linear. This allows the dynamic range of the overall detector to be extended beyond the range of the detector by itself. As a result, a dynamic range of >40dB is achieved by this design at frequencies

ranging from 0.7 to 4GHz. This design also utilizes a temperature compensation bias circuit, so this dynamic range is valid over a wide temperature range.

A final RMS power detector is presented in [11]. This power detector, like the power detector in [8], segments the dynamic range to obtain a dynamic range much higher than the detector can achieve alone. In this case, however, the dynamic range is segmented using attenuators since accurate attenuators are more easily designed than accurate amplifiers. The core detector for this design is based on a bipolar power detector which can be found in Figure 6 below. While at high amplitudes, the output of this circuit is approximately equal to the peak input voltage shifted by a V_{BE} drop, at low input amplitudes, the output voltage of this peak detector is approximately equal to the square of the input voltage. Therefore, the peak detector can, over a small range, be used as an RMS detector. The peak detector will be discussed again later in this thesis since it is used in the power detector presented in this research.

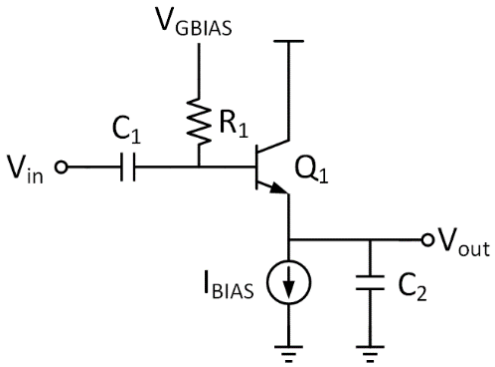

Figure 6. Peak Detector Schematic

The table below shows a comparison of the four previously discussed RMS power detectors with the performance metrics discussed above. There are several things to note in this comparison table. The first is that the translinear detector provides a very high dynamic range with very low error in a single segment. It is important to note, however, that this performance is only achieved up to 1.3GHz. It is also interesting to note that the peak-detector based RMS detector provides only 8dB of dynamic range within a single segment. This is because the peak detector provides a much better estimate of the amplitude of the input signal than it does the RMS value of the input signal. Based on the table below, the square-law detector provides a good tradeoff between the operating frequency and the dynamic range, but it requires segmentation to achieve a dynamic range above 20dB. Another important note is that none of these detectors provide an absolute power reading; each detector only outputs a voltage.

Table 1. Comparison of RMS Power Detectors

Detector	[6]	[7]	[8]	[11]
Topology	Square-Law	Translinear	Square-Law	Peak-Detector
Dynamic Range	20dB (0.5dB Error)	40dB (0.1dB Error)	40dB (4 Segments) (1dB Error)	40dB (5 Segments) (0.5dB Error)
Operating Frequency	0.1-8.5GHz	0-1.3GHz	0.7-4GHz	5.2GHz
Power Consumption	0.18mW	N.R.	11.8mW	N.R.

2.1.2 Peak Power Detectors

As mentioned in the discussion above, peak envelope power detectors provide an output that tracks with the input signal's modulating envelope:

$$P_{env} = \frac{(V_{env}(t)^2)}{50\Omega}, t_1 < t < t_2 \quad (7)$$

As seen in (7) above, peak power detectors must track the envelope power of the input signal. Therefore, the detector must be fast enough to track the modulating envelope of the input signal but must also limit the bandwidth of the output so that the high-frequency carrier at the input is sufficiently attenuated. As a result, most peak power detectors utilize either BJT or diode-based peak detectors [12-14]. A schematic of a BJT-based peak detector can be found in Figure 6 in the discussion above while a simplified schematic of a diode-based peak detector can be found in Figure 7 below. The operation of these two circuits is fairly similar. In the diode-based detector, if V_{in} rises more than the required diode turn-on voltage above V_{out}, V_{out} will begin to track V_{in} minus a diode voltage drop. If V_{in} then falls again, the diode will turn off, but V_{out} will begin to decrease as the capacitor discharges through the resistor. The output voltage will decrease with a slope equal to:

$$\frac{dV_{out}}{dt} = \frac{V_{out}}{RC} \quad (8)$$

Therefore, the output will exponentially decay to 0 with a time-constant of RC. If this RC time constant is very large compared to the period of the incoming signal, the voltage drop during the lower portion of the signal will be insignificant compared to the amplitude, and the output voltage will approximately equal the input amplitude minus a diode voltage

drop. The resistor is included in this circuit to set the DC voltage at the output since this DC voltage is ill-defined with only the capacitor and diode connected to this node. Since the input signal to the diode-based peak detector will be high frequency, the diode will need to be able to operate at sufficiently high frequency so that the output voltage can track the input voltage. Therefore, designs utilizing diode-based peak detectors typically use high-speed Schottky diodes.

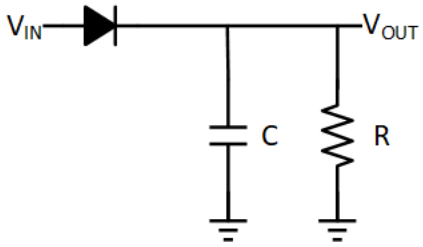

Figure 7. Diode-based Peak Detector

The operation of the BJT-based peak detector shown in Figure 6 is similar to the diode-based peak detector discussed above. In this circuit, the capacitor C_1 and the resistor R_1 form an ac-coupling network at the input of the peak detector so that the bias voltage of the base of Q_1 can be set independently from the DC bias of V_{in}. If the voltage at the base of Q_1 is sufficiently above the voltage at the emitter of Q_1, the BJT will turn on and the voltage at the output will track the voltage at the input minus a V_{BE} diode-voltage drop. Once the voltage at the base of Q_1 falls back below the required turn-on voltage, the transistor Q_1 will turn off and the output voltage will begin to decrease as I_{BIAS} discharges C_2 at a rate of:

$$\frac{dV_{out}}{dt} = \frac{I_{BIAS}}{C_2} \tag{9}$$

Once again, if C_2 is large and I_{BIAS} is small, the output voltage will not change much during the low period of the input signal, and the DC voltage at the output will be close to the peak voltage at the base of the BJT minus a V_{BE} voltage drop.

It is interesting to note that the diode-based and BJT-based peak detectors can be used as peak detectors or as RMS detectors [11]. The main difference between the two applications is that RMS detectors require high time constants in the detectors so that the output does not track with the envelope and provides a measure of the average power. In the case of peak envelope power detectors, the time constants are generally much smaller so that the output can track the modulating envelope of the input signal.

Peak power detectors generally utilize the same performance metrics as RMS power detectors. These include the dynamic range, or the input range over which the output of the peak power detector is valid, the frequency of operation, or the input frequency range over which the output of the peak power detector is valid, and the power consumption, which is important since many power detectors utilized are run off a battery supply and therefore should not dissipate excessive power.

One design based on a BJT peak detector is reported in [13]. This design utilizes one peak detector with the RF input and subtracts the output voltage of a matched peak detector with no input in order to compensate for temperature and process variations. The output voltage still has some dependence on temperature, however, and the output voltage decreases as the temperature increases. In order to solve this issue, this design utilizes a PTAT current source to generate a compensation current that is added to the output of the

peak detector circuit in order to boost the output voltage at higher temperatures to match the output voltage at lower temperatures. This compensation scheme, however, assumes that the temperature dependence of the peak detector output is linear, so the detector still shows some temperature-related errors at low input amplitudes. Additionally, the compensation factor is determined experimentally which requires post-fabrication calibration. While not explicitly reported, this design appears to achieve a dynamic range of approximately 20dB.

One issue with the BJT peak detector is its non-linearity for small input amplitudes. As the input amplitude decreases, the magnitude of the ripple at the output during the low portion of the input begins to approach the amplitude of the input signal. Therefore, the output does not linearly track with the input amplitude which introduces some errors if a linear relationship between the input amplitude and the output voltage is assumed. The design in [15] alleviates this issue by utilizing a replica peak detector and generating a compensation current to correct for this non-linearity. This extends the linear range of the peak detector to approximately 26dB.

The design specified in [16] represents a typical peak power detector available on the market. This detector achieves an accuracy of 0.5dB at full input power and an accuracy of 1.5dB at low input power. The detection range is from -16dBm to 5dBm which represents a 21dB dynamic range. As mentioned before, an important characteristic of most power detectors is their error over a wide temperature range since the devices they are used in can be subject to many different environmental conditions. This detector achieves a 0.3dB detection error over a temperature range from -40° to 85°.

One common issue with all of the power detectors mentioned thus far is that they do not output an absolute power detection reading. All of these designs output a voltage that must be digitized by the baseband processor in the loop in Figure 2 which must then convert that output voltage into an appropriate power reading. For varying input frequencies, temperatures, process variations, and non-linearities, this conversion of the output voltage into an appropriate power reading often requires extensive post-fabrication calibration and storage of data into read-only-memories in either the detector or the baseband processor [9]. This research seeks to greatly reduce the amount of calibration and data storage required by moving much of that calibration on-chip. The architecture required to accomplish this task will be discussed in detail in Section 3.

2.2 Current Sensors

The purpose of the current sensor in the transmitter is to measure the bias current of the PA, the bias current of the PA's modulator, and the gate current of the PA. One purpose in measuring the bias current of the PA is to calculate the PA's power-added efficiency (PAE). This is defined as:

$$PAE = 100 \times \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{10}$$

From (10), we see that the output power, input power, and DC power consumption of the PA must be known to compute the PAE. In the final system, the PAE will be used as one of the parameters to be optimized by the computational engine. The DC bias current can be adjusted through the gate bias voltage while the input power can be adjusted through an input attenuator to attempt the combination of these two parameters that provides the maximum PAE while also taking into account the reliability of the PA [17]. This DC

power includes the bias current for the PA's gain transistor as well as the bias current for the PA's modulator. Therefore, both currents will be measured by the current sensor. Also important is the PA gate current. If there is excessive PA gate current, the reliability of the PA will be greatly reduced [4]. Therefore, the computational engine will also attempt to minimize the gate current of the PA in order to maximize its reliability.

There are several metrics used to measure the performance of current sensors. Since these current sensors often interface to very high supply voltages, the sensor should be able to handle a large common-mode range at its input. Also important is the gain error which is a measure of how accurately the sensor measures the input current over its full input current range. This gain error may be due to temperature or process variations in the series resistance or errors in the amplification and readout circuitry. The next metric is the offset of the current sensor which is generally due to errors in the readout circuitry. Many current sensors will include offset-cancellation circuits to reduce this as much as possible. The resolution of the detector, which determines the minimum current step that can be accurately measured, is also generally determined by the accuracy of the readout circuitry. Finally, the power consumption of the sensor is important as many of these current sensors operate in battery-powered environments. Therefore, the power consumption should be reduced as much as possible to ensure the battery life is as long as possible.

There are several current-sensing topologies that can be utilized to measure the various currents in the PA. One is the series sense-resistor topology whose basic schematic is shown in Figure 8 below. This topology requires a sense resistance to be

placed in series with the current that is to be measured. If the resistance of the sense resistor is well-known, the voltage across it provides information on the desired current:

$$I = \frac{V_{sense}}{R_{sense}} \tag{11}$$

Therefore, the sense voltage can be digitized and used by the computational engine in its efficiency calculations and adjustments. There are some issues with this topology, however. One issue is that the addition of the sense resistor in series with the current to be measured leads to additional power loss in the system, especially if the current or the sense resistance is large. Therefore, for systems where large currents must be measured, the sense resistance must be very small. As a result, the signal-to-noise ratio (SNR) of the voltage across the resistor may be very low which will affect the accuracy of the current sensing operation. In some systems, any additional sense resistance is unacceptable, and the sense voltage will either need to be obtained without any additional resistor added, or the current estimate will need to be obtained another way.

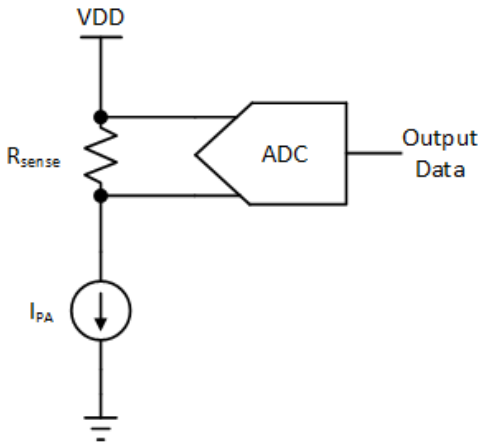

Figure 8. Typical Series-Resistor Sensing Scheme

The design reported in [18] utilizes a delta-sigma modulator to digitize the voltage across a 10mΩ shunt resistor that is implemented on-chip. The on-chip shunt resistor occupies an extremely large area and is subject to electromigration which changes its resistance over time [19]. In order to compensate for variations in temperature causing variations in the sense resistance, a PTAT voltage reference is used to generate a compensation voltage which is added to the input voltage. This allows the sensor to achieve a gain error of just 0.9% over a wide temperature range with a single-temperature trim with a 40μA offset. The use of a sigma-delta along with averaging also allows the SNR of the input signal to be improved since random noise caused by the sense resistance is averaged and its effective RMS value is decreased. Therefore, the sensor achieves an effective resolution of 13-bits with a conversion time of 2ms. As discussed before, most current sensors must interface to high-voltage supplies. In this design, this is accomplished by utilizing a high-voltage CMOS process with high-voltage transistors utilized at the input interface of the ADC. This allows the standard-voltage ADC to interface to voltages from 0V up to 25V.

Other current sensors, such as the one reported in [20], are intended for use in switching power converters and utilize sense-FETs placed in parallel with the transistor current to be measured. The basic sense-FET scheme utilized in a buck-converter is shown in Figure 9 below. The current through M_P is to be measured, so another PFET transistor, M_{PS}, with a lower number of fingers is placed in parallel to this transistor. Therefore, the current through M_{PS} should be some ratio of the current through M_P. However, the current

through the transistors, taking into account channel-length modulation, can be approximated as:

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \quad (12)$$

Therefore, in order to ensure the ratio of the currents through M_P and M_{PS} are well-known, the drain voltages of M_P and M_{PS} should be equal. This is accomplished using the transistor M_{N1} and the operation amplifier (op-amp) shown in Figure 9 below. Therefore, the voltage across R_S can be measured to find the current through M_{PS} which can then be multiplied by the ratio of current through M_P and M_{PS} to find the current through M_P. The design reported in [20] extends the basic sense-FET scheme mentioned above to allow the sensor to measure the current through both M_P and M_N. This design achieves a gain accuracy of 3.2% at a maximum load current of 2A and a settling of 6ns. No ADC is included to digitize the voltage across R_S, so it is difficult to compare the power consumption of this sensor with others. Since the sense-FET is integrated with the current to be measured, the CM input range is not important for this design. One major drawback of this topology, and the reason it was not used in this research, is the sense-FET must be matched to the transistor through which the current must be measured. Since the idea of this PA control system is to treat the PA as a black box, it is not possible to properly match a transistor to the PA's internal transistors.

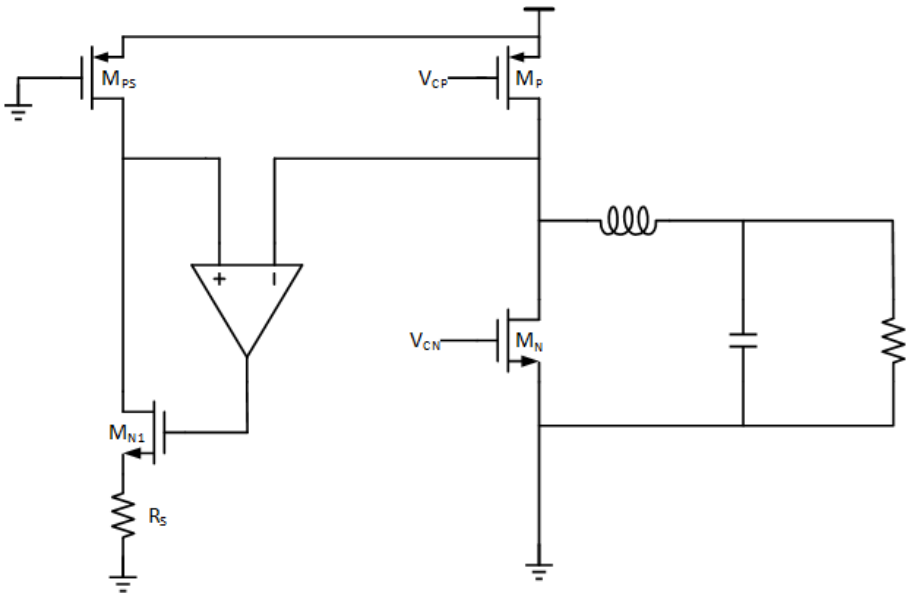

Figure 9. Basic Sense-FET Scheme

A final current sensing topology is described in [21]. This current sensor is targeted for use in buck and boost converters, such as the one shown in Figure 9 above. During the time when the switch formed by M_P in Figure 9 is on, the filter capacitor at the output is charging. When the switch formed by M_P turns off and the switch formed by M_N turns on, the capacitor at the output is discharging. During this time, the discharge rate can be approximated as:

$$\frac{dV_o}{dt} = \frac{i_L}{C_L} \tag{13}$$

Where i_L is the current required by the load of the converter and C_L is the output capacitor. Therefore, if the slope of the output voltage is measured during this period, the current can be calculated by multiplying this slope by the filter capacitance. The design in [21] utilizes a concept similar to the single-slope ADC. Two points on the output voltage curve are sampled with a known time in between them and held on capacitors. One capacitor is then

discharged by a known current until the voltage on that capacitor equals the voltage on the other capacitor. A counter is used during this time to digitize the difference between the two voltages. Since the difference between the two voltages as well as the time between the two samples is known, the slope can be calculated. This is shown in Figure 10 below. This slope is then multiplied by the capacitance to calculate the load current for the converter. This design achieves an impressive maximum error of 0.4% but consumes a total power of approximately 18mW. This design utilizes level-shifting capacitors at the input of the detector and can, with proper protection circuitry, handle high common-mode input voltages and interface with very large supply voltages. The conversion time of the sensor is 500ns which allows for very fast sensor measurements to be taken. The resolution of the detector is 8-bits. While the conversion time and resolution are good for this topology, the sensor relies on accurately knowing the value of the filter capacitor in the buck converter. In [21], the value of the discharging current source is trimmed to provide the proper absolute output current at room temperature. Many capacitors, however, have strong temperature dependence and can vary by up to +/-15% across a range from -40°C to 85°C. Therefore, this circuit would need some sort of temperature compensation circuit to provide satisfactory performance across a wide range of temperatures. The issue with this solution, however, is that the capacitance does not necessarily vary linearly with temperature. As a result, the compensation circuit may need to account for non-linear changes in the capacitance with respect to temperature.

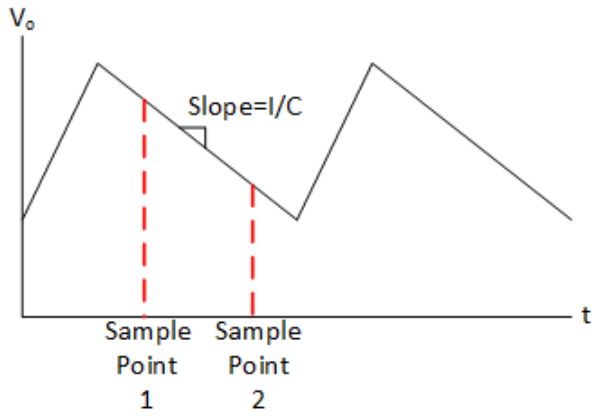

Figure 10. Capacitor-Based Current Sensor Operation

Table 2 below shows a summary of the current sensors discussed above. The series-R topology provides the lowest power consumption but has higher gain error than the capacitor-based sensor. The capacitor-based sensor, however, is not measured over a wide temperature range and will require a complex compensation circuit to achieve adequate performance. The sense-FET sensor integrates very well with monolithic buck converters but exhibits high gain error. The power consumption is not reported for this design

Table 2. Current Sensor Topology Comparison

Sensor	[18]	[20]	[21]
Topology	Series-R	Sense-FET	Capacitor
Gain Error	0.9%	3.2%	0.4%
Common-Mode Range	0-25V	N.A.	0-50V
Power Consumption	16.35µW	N.R.	18mW

3. PROPOSED CURRENT SENSOR

3.1 Current Sensor Architecture

This research presents a current sensor that is based on the series-R currents sensor topology introduced in the previous section. First, the various requirements of the current sensor will be defined. Next, an overview of the current architecture will be presented.

3.2.1 Problem Description

The current sensor has several requirements that are set in order to ensure the computational engine can accurately calculate the PAE and control the gate input current. First, the sensor must measure three supply currents: the positive (V_{DD}) at a voltage of around 40V. This is the supply that provides the bias current to the PA. The bias current flowing through the PA flows to ground (not the negative supply). Next is the negative supply (modulator supply) at a voltage of around -6V. This supply provides a negative voltage required for the drain-modulator on the PA chip and the current for the drain-modulator flows from the positive supply to the negative (V_{SS} supply). Finally, there is the gate supply which ranges from 0V to -5V and sets the bias voltage for the gate of the PA's main transistor. The current ranges and required accuracies are shown in the table below. The measurements for all three supplies must be obtained within 1ms.

Table 3. Current Range and Accuracy Requirements

Supply	V_{DD}	V_{SS}	V_{GG}
Current Range	1A-4A	-250mA to 100mA	-250mA to 100mA
Accuracy Requirement	1%	10mA	10mA

In addition to the currents listed above, the detector will also need to take into account the fact that the PA is modulated using pulse modulation. Therefore, during periods where the pulse is off, the PA will have no current flowing through it. This pulse modulation is characterized by a pulse repetition frequency (PRF) and a duty cycle (DC). The PRF can range from 50kHz to 10MHz while the duty cycle can range from 5% to 50%. The supply node of the PA, however, is well-bypassed, and the current flowing to the PA will have a DC component with some ripple around this DC level. Therefore, the detector will need to adequately filter this ripple component at the PRF out in order to provide an accurate DC current estimate. If the peak current is desired, the average current can simply be divided by the duty cycle to find the peak current.

There are several other constraints placed on the current sensor so that it can be useful in the PA control circuit. The first is that the sensor must interface to the 40V supply used for the PA. Since the ground of the PA is connected directly to a ground plane on the PCB through several vias, there is nowhere to insert a sense resistance to accurately measure the current. As a result, the current sensor must perform "high-side sensing" on the positive supply of the PA. Additionally, to reduce power supply noise and improve efficiency, a large current-sense resistor cannot be used in series with the PA's power supply. Indeed, a 10mΩ is targeted in this design. Therefore, the current sense voltages at the input of the sensor will be very small and any noise introduced by the sensor will lead to large detection errors. As a result, the SNR of the sensing measurement will need to be improved in some manner. Lastly, it is not even desirable in this system to introduce a discrete current sense resistance in series with the PA's power supply. As a result, the

PCB trace connecting the PA to its power supply will be utilized for current sensing. This PCB trace will be approximately 10mΩ at room temperature, but this sense resistance can vary greatly with temperature. This is seen in Figure 11 below which shows the resistivity of a copper trace over a wide temperature range. The resistivity of the copper changes as much as 28% from room temperature to either temperature extreme. Therefore, the current sensor will require some form of temperature compensation in order to provide an accurate estimate of the supply current.

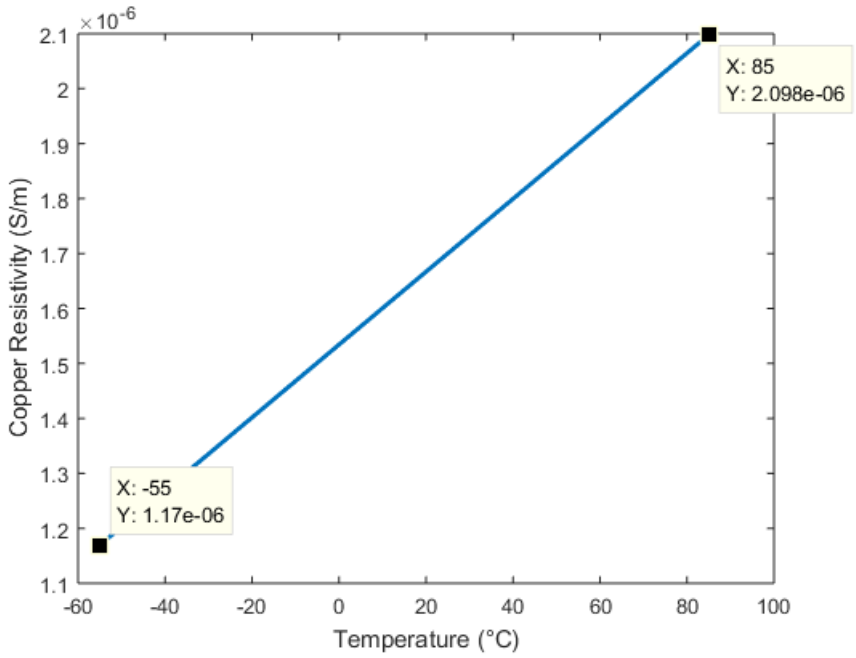

Figure 11. Copper Resistivity over Temperature

3.2.2 Architecture Overview

The current sensor architecture is shown in Figure 12 below. Only the positive and negative supplies are shown for simplicity, but the gate supply sensor section is

identical to the negative supply sensor section since these supplies have identical accuracy requirements. The overall design consists of a level-shifting capacitor chip which will shift the high supply voltage to a level suitable for use in a standard CMOS process, an oversampling ADC which will measure the voltage across the sense resistance for each supply, and a reference current source that will pass a well-known current through the sense trace to estimate its resistance.

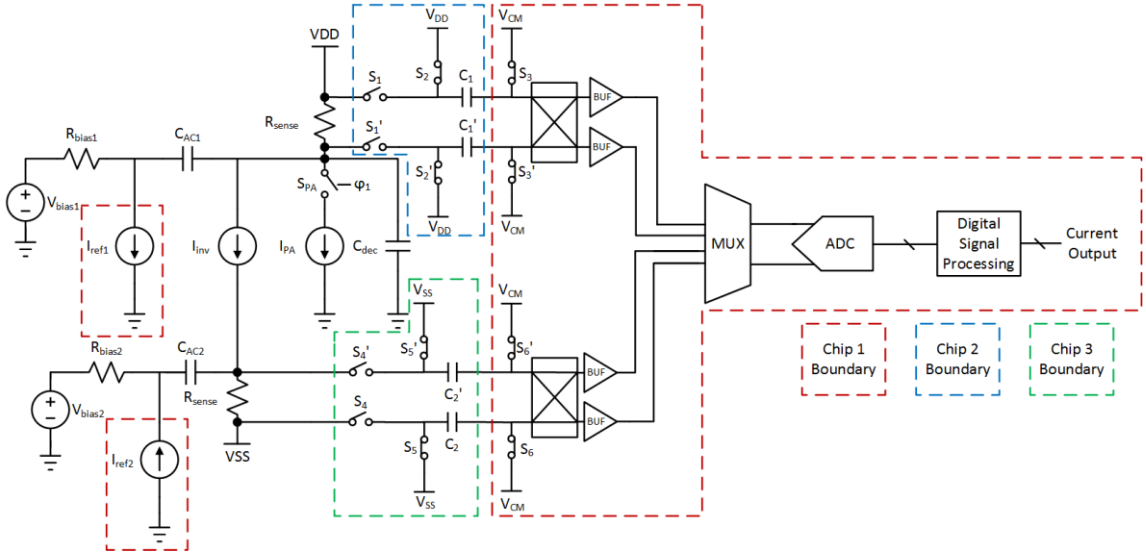

Figure 12. Current Sensor Architecture

Figure 13 below shows the level-shifting capacitors in more detail. During the charging phase, switches S_2 and S_3 are closed while switch S_1 is opened. This charges the capacitors such that the voltage on the right side of C_1 is a common-mode voltage suitable for the standard CMOS process used while the voltage on the left side is the high-supply voltage. Since the switches $S_{1,2}$ and S_3 operate at such different voltages, these switches must reside on separate chips. Chip 1 is powered by a standard 1.8V

supply. As a result, the common-mode voltage chosen for chip 1 is 0.9V. Chip 2, on the other hand, is powered by a 40V supply. Therefore, the capacitors are charge to a voltage of approximately 39.1V.

Since a standard CMOS process is still used for this chip, a negative supply that is approximately 1.8V below 40V must be generated. This is accomplished by using diode-connected transistors, and more details can be found in the next section. During the time when S_2 and S_3 are closed, the differential input to the buffer is 0V.

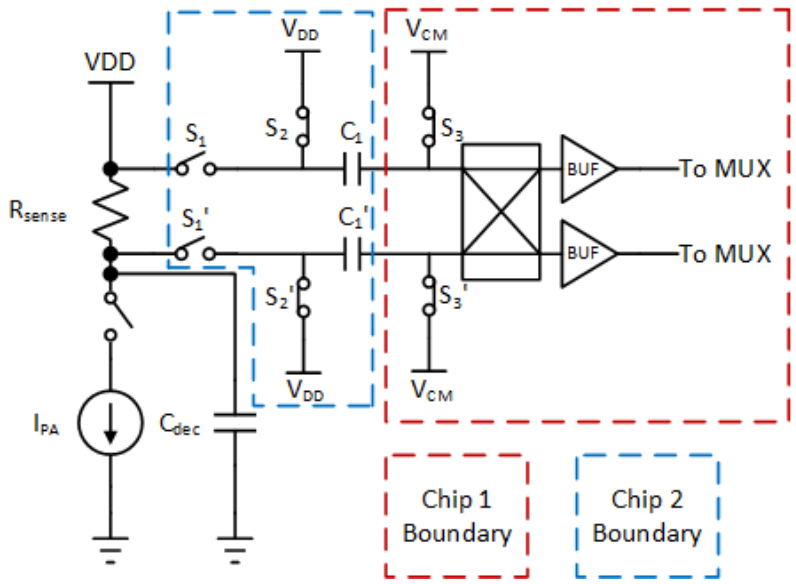

Figure 13. Level Shifting Capacitors

After sufficient time for the capacitor to charge has elapsed, switch S_3 is opened followed by S_2. This is done to ensure that charge injection from the switches to the level-shifting capacitors is minimized. Once these switches are opened, switch S_1 is closed and the voltage appearing at the input of the buffers is the differential voltage across the sense

resistance but shifted down by the voltage stored on the level-shifting capacitors. The buffer leading to the MUX must have a high impedance input to ensure the charge on the capacitors remains constant during the measurement period. Additionally, while the switches may allow some leakage current through, the capacitors are recharged at the beginning of each measurement cycle.

Figure 14 below shows an overview of the circuits contained on Chip 1. The input of this section comes from the level shifting capacitors and goes to the buffer. The buffer provides some gain to ensure that the ADC can properly digitize the small input signals coming from the small sense resistance. The buffer outputs for each supply are multiplexed so that one ADC can be used to digitize each input. The output of the ADC is then processed to determine the current estimate.

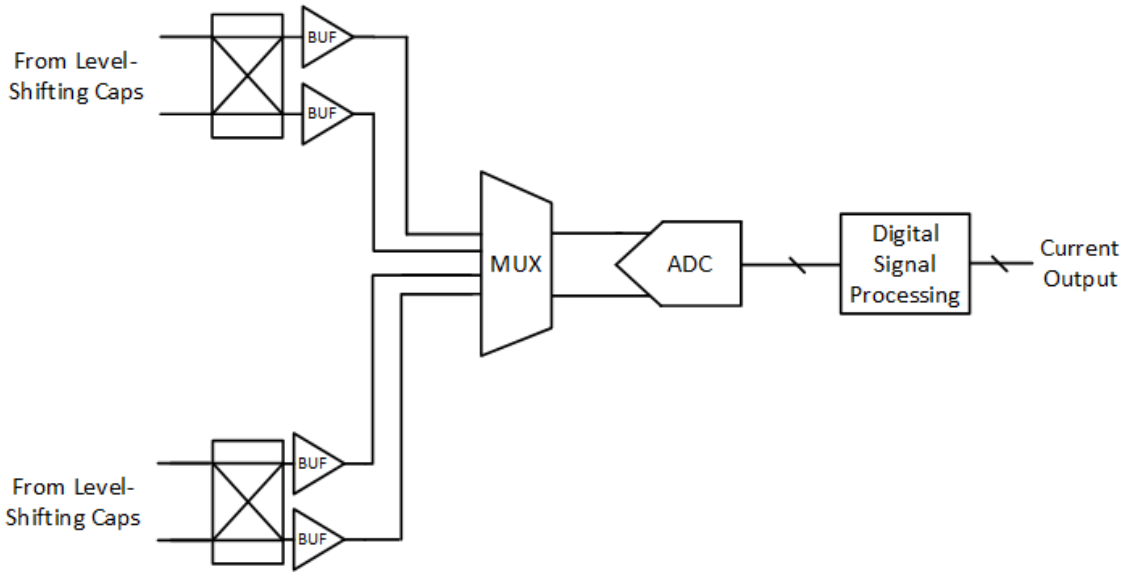

Figure 14. ADC and Supporting Circuitry

One issue in DC current measurement is that low frequency noise and offsets can greatly impact the accuracy of the current estimate. Especially in CMOS current sensors, flicker noise will play a significant role in determining the accuracy of the detector. In order to decrease the effect of offsets and flicker noise, a chopping modulator is added at the input of the buffers. This modulator switches the polarity of the input signal at a rate of 25kHz. This moves the desired DC information up to 25kHz where it is less impacted by offsets and flicker noise in the buffer, MUX, or ADC. This is demonstrated in Figure 15 below. In analog chopping systems, an identical chopping modulator is added to the output of the amplifier in order to move the low-frequency information back down to its original frequency position. In this case, however, the chopping de-modulation is performed in the digital signal processing.

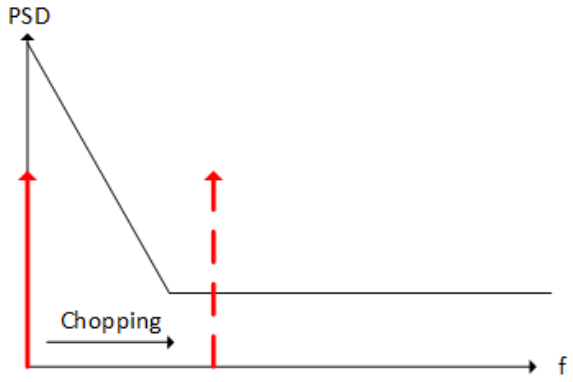

Figure 15. Effect of Chopping on the DC Input Signal

One can also examine the advantage of chopping by considering the output of the ADC during each chopping period. When the input polarity is not reversed, the output

voltage is the sense voltage plus the offset voltage of the buffer and ADC as well as an error due to flicker noise.

$$V_+ = V_{sense} + V_{OS} + \epsilon_{flicker}(t_o) \tag{14}$$

When the input polarity is reversed, T_{chop} seconds later, the output voltage will be:

$$V_- = V_{sense} + V_{OS} + \epsilon_{flicker}(t_o + T_{chop}) \tag{15}$$

The digital signal processor will take the difference between (14) and (15) to obtain an estimate of the sense voltage:

$$V_{out} = V_+ - V_- = 2V_{sense} + \left(\epsilon_{flicker}(t_o) - \epsilon_{flicker}\left(t_o + T_{chop}\right)\right) \tag{16}$$

We note first and foremost that the offset of the buffer and ADC is eliminated by the chopping. This is important since the input voltage is so small, and the offset would greatly limit the accuracy of the current estimate if it was allowed to corrupt the signal. We also note that slow-varying flicker noise will also be eliminated. This is because, for slow-varying flicker noise:

$$\epsilon_{flicker}(t_o) = \epsilon_{flicker}\left(t_o + T_{chop}\right) \tag{17}$$

Therefore, flicker noise well below the chopping frequency (<5kHz) will not have a significant impact on the accuracy of the current sense estimate.

Another design challenge in the ADC is how components at the PRF will be eliminated in the final output measurement. Since the current through the sense resistor will have a DC component as well as (possibly large) components at the PRF and multiples of the PRF, the digital signal processing will need to eliminate these components in order to obtain an accurate measure of the DC component. This can be easily achieved by using a moving average filter with the following impulse response:

$$h[n] = \begin{cases} \frac{1}{M}, 0 \leq n \leq M-1 \\ 0, \quad otherwise \end{cases} \tag{18}$$

Therefore, the output of an M-tap moving average filter at any given time is simply the average of the M previous samples, including the current sample. In order to visualize how this eliminates the tones at the PRF and multiples of the PRF, the filter response is plotted below for M=50 and a sampling rate of 500MHz. Also plotted is a 10MHz square wave which has components at 10MHz, 30MHz, 50MHz, and so on. We note that the period of the 10MHz square wave is the same as the averaging period for the 50-tap moving-average filter since $\frac{500MHz}{50} = 10MHz$. We see that the first notch of the moving-average filter falls at 10MHz and eliminates the 10MHz component. Other notches in the filter fall at multiples of the 10MHz component and will therefore eliminate them as well. Also shown in the frequency response for a moving average filter for M=100. This filter also eliminates the desired components. Therefore, in order to eliminate the frequency components caused by the pulse modulation, the digital signal process just needs to average a number of samples that is an integer multiple of the number of samples in one period of the pulse modulation.

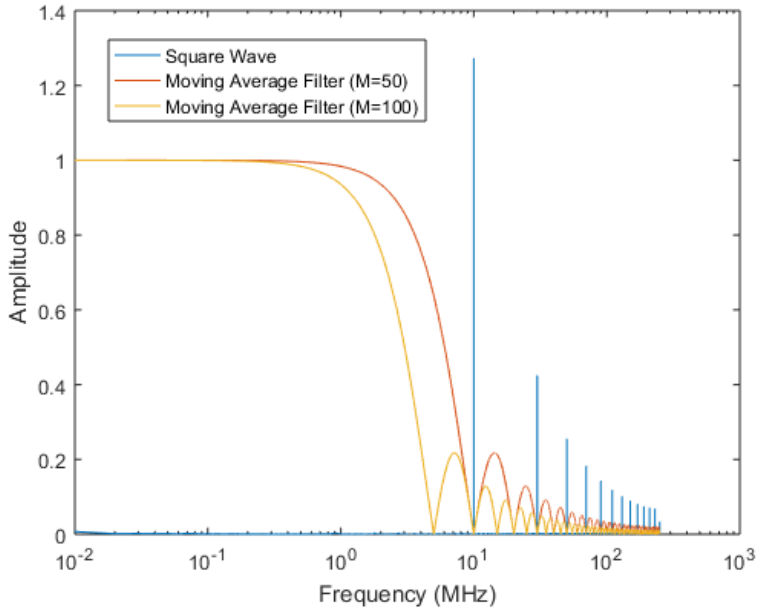

Figure 16. Input Square Wave with Moving-Average Filter Responses

Another important property of the moving-average filter is its ability to decrease the effective noise at the output of the digital signal processor. Assuming that the input noise is white, the application of an M-tap moving-average filter improves the SNR by a factor of M while preserving the DC value since the magnitude response of the filter at DC is unity. Therefore, the poor SNR of the signal after it has passed through the ADC and the buffer can be improved greatly by averaging a large number of samples from the output of the ADC. This is illustrated in Figure 17 below. The input spectrum is white across the full frequency range. The noise power clearly decreases at higher frequencies when the moving average filter is applied and is decreased more drastically when a larger moving-average filter is applied.

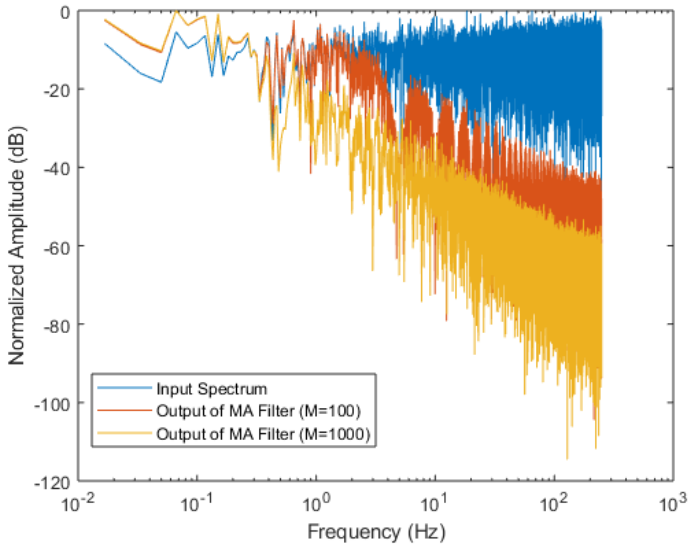

Figure 17. Input Noise and Output Noise after Moving-Average Filters

This noise reduction property is verified by calculating the relative noise powers of the three signals shown in Figure 17 above. The noise power at the input is $3.249nV^2$ while the noise power at the output of the 100-tap moving-average filter is $39.42pV^2$ and the noise power at the output of the 1000-tap moving-average filter is $3.5pV^2$. Therefore, we see that the 100-tap moving average filter improves the SNR by a factor of 82 and the 1000-tap moving-average filter improves the SNR by a factor of 928. These values are close to the values predicted above. Therefore, an oversampling sigma-delta ADC is utilized in this design to digitize the voltage across the sense resistor.

Another concern in the design of the current sensor is estimating the resistance of the PCB trace. As discussed previously, the current sensor requires some form of compensation circuit to ensure that changes in the sense resistance over temperature are

taken into account. This is accomplished using the reference current calibration circuit shown in Figure 18 below.

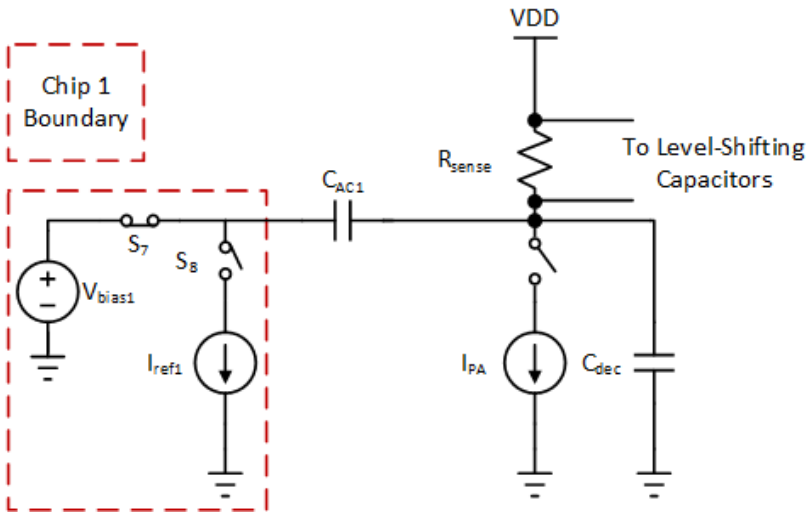

Figure 18. Reference Current Calibration Circuit

The purpose of this circuit is to apply a known current to the sense resistance so that the ADC can measure the voltage drop and use the known current value and the voltage drop value to compute an estimate of the sense resistance. Since this reference current source must also interface to the high-voltage supply, another level-shifting capacitor C_{AC1} is used. During the charging period, switch S_7 is closed while switch S_8 is open. This charges the capacitor such that the voltage at the current source is set to 1.8V. Once this charging cycle is complete, switch S_7 is opened and switch S_8 is closed. This allows the current I_{ref1} to flow through the coupling capacitor and through the sense resistance. During this period, the capacitor begins to charge to an even greater voltage.

Therefore, the voltage across the current source begins to decrease once it is activated at a rate of:

$$\frac{\Delta V}{\Delta t} = \frac{I_{ref1}}{C_{AC1}} \tag{19}$$

Therefore, the current source cannot remain activated indefinitely and will need to be periodically recharged during the measurement cycle. A large 1µF capacitor is used at this interface to ensure a sufficiently long reference current pulse can be used.

The voltage drop measured during the reference calibration period must be used by the sensor when calculating the final current. First, we measure the voltage drop caused by the reference current:

$$\Delta V = I_{REF} R_{SENSE} \tag{20}$$

It is assumed that there is no period during which the PA current is not flowing through the sense resistor. Therefore, this voltage drop must be measured by taking the voltage drop across the sense resistor with only the PA active (V_{PA}) and subtracting it from the voltage drop across the sense resistor with the PA and the reference current source active (V_{PA+REF}):

$$\Delta V = V_{PA+REF} - V_{PA} = I_{REF} R_{SENSE} \rightarrow R_{SENSE} = \frac{V_{PA+REF} - V_{PA}}{I_{REF}} \tag{21}$$

We can therefore calculate the PA current using the Pa measurement and the sense resistance:

$$I_{PA} = \frac{V_{PA}}{R_{SENSE}} = \frac{V_{PA}}{V_{PA+REF} - V_{PA}} \cdot I_{REF} \tag{22}$$

Therefore, the digital signal processor only needs to combine the PA measurement and the PA plus reference current source measurement along with the known reference current value to calculate the current flowing through R_{SENSE}.

Besides measuring the sense resistance, the reference current source measurement provides another very useful property. Suppose that the ADC or buffer has a gain error of ε. Therefore, the ideal PA and reference measurements will both be multiplied by (1+ε) at the output of the ADC. Therefore, the PA current will be measured as:

$$I_{PA} = \frac{V_{PA}(1+\epsilon)}{V_{PA+REF}(1+\epsilon)-V_{PA}(1+\epsilon)} \cdot I_{REF} = \frac{V_{PA}}{V_{PA+REF}-V_{PA}} \cdot I_{REF} \quad (23)$$

As a result of the reference current source measurement, the gain error in the ADC or the buffer is eliminated in the final current calculation and therefore does not affect the accuracy of the current sensor. Additionally, since the chopping scheme eliminates the effects of buffer and ADC offsets and this technique eliminates gain errors, the main accuracy requirements are moved to the quantization performance of the ADC and the accuracy of I_{REF}. Therefore, most design effort is focused in these two places. One thing to note, however, is that any non-linearity in the system will cause current measurement errors as the reference current calibration only cancels linear gain errors.

3.2 Implementation of Current Sensor

3.1.1 Input Buffer

The purpose of the input buffer is to boost the DC voltage at the input to a level suitable for the ADC to digitize. Therefore, the input buffer provides a gain of approximately 10V/V for the incoming signal. As mentioned before, the exact gain of the buffer is not critical as any gain variations are compensated by the reference current

calibration. There are several other important parameters for the input buffer. Firstly, the input buffer must be very linear since non-linear errors in the buffer are not cancelled by the calibration scheme. Additionally, the buffer must present a large (ideally infinite) input impedance as it is not desirable to bleed any charge off of the level-shifting capacitors at the input of the detector. The buffer should also have relatively low noise as high input-referred noise in the buffer will corrupt the input signal. As mentioned before, however, the effective noise of the buffer will be greatly decreased by the averaging at the output of the ADC. Lastly, the buffer should have a reasonable bandwidth to ensure that when the reference current source is activated, the buffer output does not take excessive time to rise to the new output value. Table 1 below shows the requirements for the buffer.

Table 4. Requirements for Input Buffer

Parameter	Required Value
Gain	~10V/V
Bandwidth	>1.5MHz
Noise	$<50\mu V_{rms}$
Gain Error	<0.1%

Based on the buffer requirements discussed above, the fully-differential difference amplifier (FDDA) shown in Figure 19 is used [22]. This amplifier provides fully differential gain with a high input impedance and is therefore very suitable for this application. This amplifier is similar to the single-ended non-inverting operational amplifier configuration and provides a gain equal to:

$$A_V = 1 + \frac{R_2}{R_1} \tag{24}$$

Therefore, we choose R_2 to be 90kΩ while R_1 is 10kΩ. This provides the desired nominal gain of 10V/V.

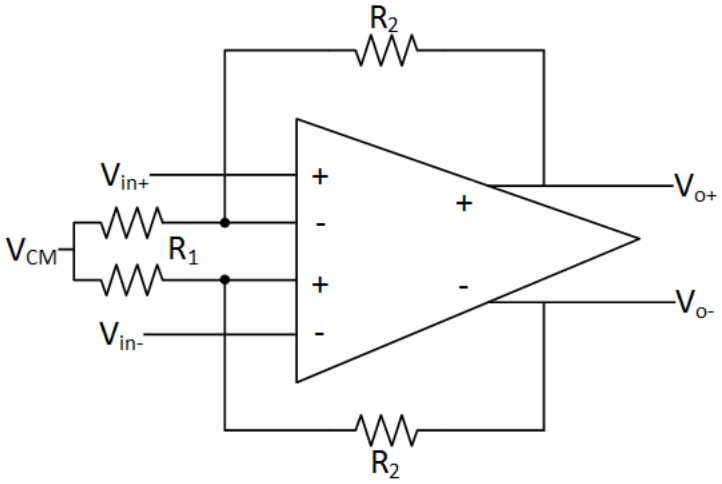

Figure 19. Fully-Differential Differential Difference Amplifier

The FDDA is implemented using the schematic in Figure 20 below. The implementation is a fully differential, Miller-compensated op-amp with a zero nulling resistor and two differential pairs at the input to implement the differential-difference operation. We select the transconductance of the input transistors, $g_{m1\text{-}4}$, and the miller capacitor C_M to provide a gain-bandwidth (GBW) of approximately 20MHz. Therefore, with process and temperature variations, the bandwidth of the buffer should remain above 1.5MHz. Next, we select the size and bias of transistor M_7 to ensure the second pole of the amplifier is at least twice the GBW of the amplifier. This, in combination with selecting the value of R_z to move the RHP zero formed by C_M to infinity, ensures that the

phase margin remains above 60°. Lastly, the sizes of M_5 and M_6 are sized with long lengths and relatively short widths to decrease their transconductance and ensure they do not contribute excessive noise.

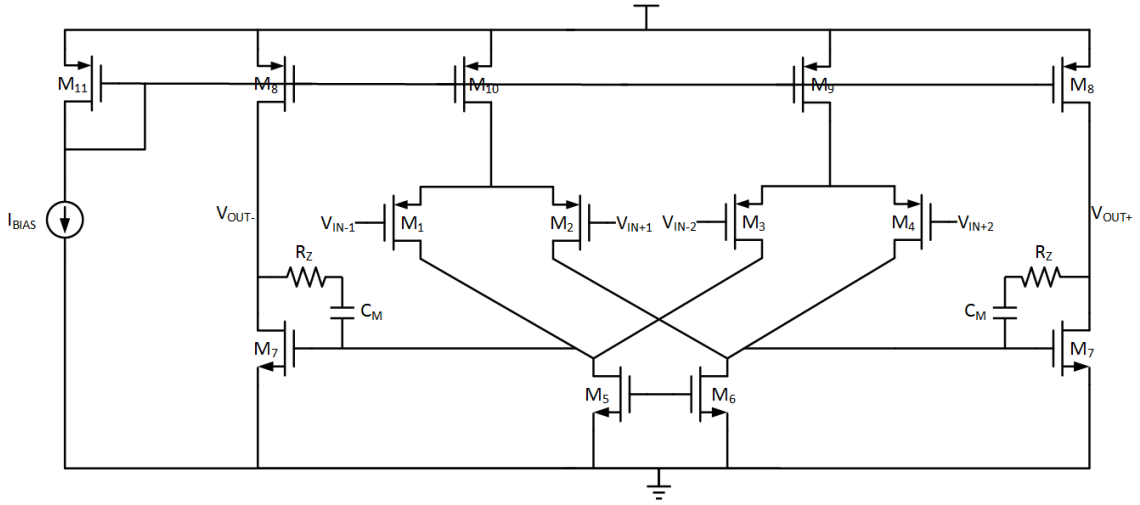

Figure 20. FDDA Schematic

Since the output common-mode level of the FDDA is not well-defined, a common-mode feedback (CMFB) circuit is required. The CMFB amplifier used is shown below in Figure 21. This circuit does not resistively load the output of the amplifier and compares the common-mode output of the FDDA to the desired voltage, V_{CM}. This amplifier then adjusts the voltage V_{CMFB}, which is connected to M_5 and M_6 in Figure 20 to adjust the common-mode output. M_{17} is sized such that the current density (I_D/(W/L)) is equal to the current density of M_3 and M_4. This ensures that there is no offset in the output common-mode voltage.

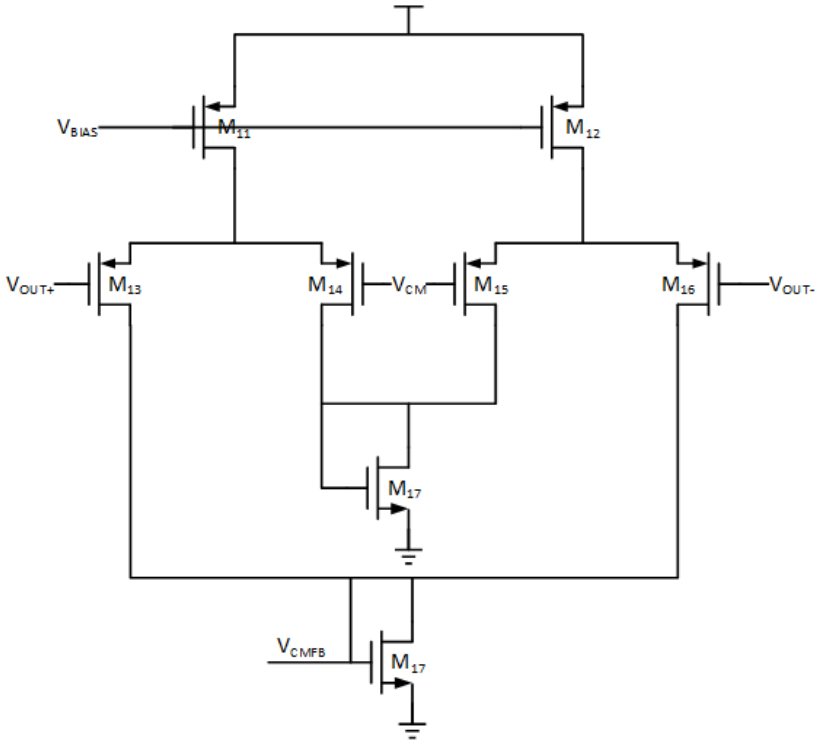

Figure 21. CMFB Circuit for FDDA

The FDDA was laid out to ensure minimal offset due to process or temperature gradients. The input transistors M_{1-4} are carefully laid out in a common-centroid array to ensure minimal offset and to ensure the transconductance of the input differential pairs are equal. Additionally, any other transistor pairs requiring matching are common-centroided along with the miller capacitors and the zero-nulling resistors.

The buffer's post-layout performance was verified using Monte-Carlo simulations with the inclusion of process variations, temperature variations, and mismatch variations. Figure 22 below shows the histogram for the bandwidth of the FDDA. The BW data set is at room temperature while the BW_low data set is at -55°C and the BW_high data set is at 85°C. The bandwidth of the buffer remains above the desired 1.5MHz for all cases.

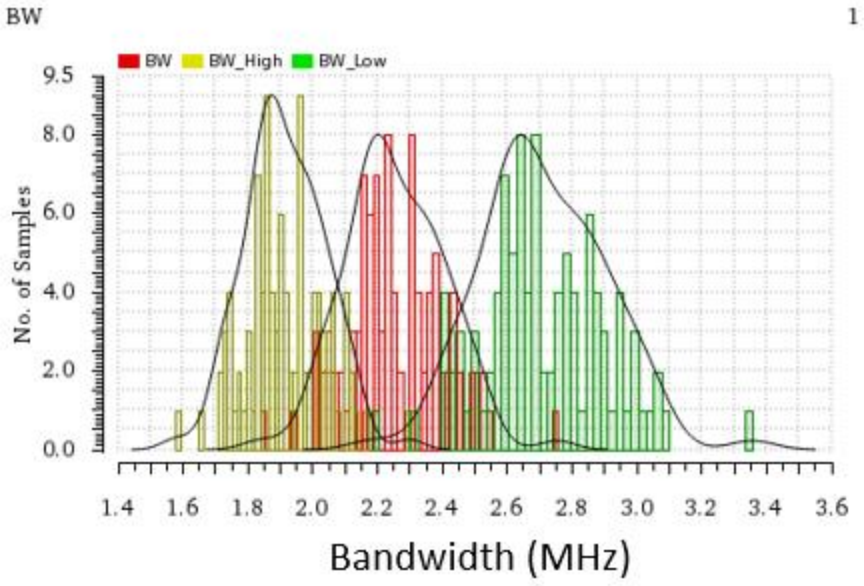

Figure 22. FDDA Buffer Bandwidth Results

Next, the gain error from 10V/V is measured across the full expected input range (-40mV to 40mV). The worst-case gain error is around 0.15% which is well enough below the required 1% current measurement error. The main gain error comes from non-linearities in the FDDA. Because the input differential pairs are each connected to the differential input or output voltages, there is a somewhat large differential input voltage. Although the transistors $M_{1\text{-}4}$ in Figure 20 are sized to ensure a high overdrive voltage which improves linearity, there is still some performance degradation. This is shown in Figure 23 below.

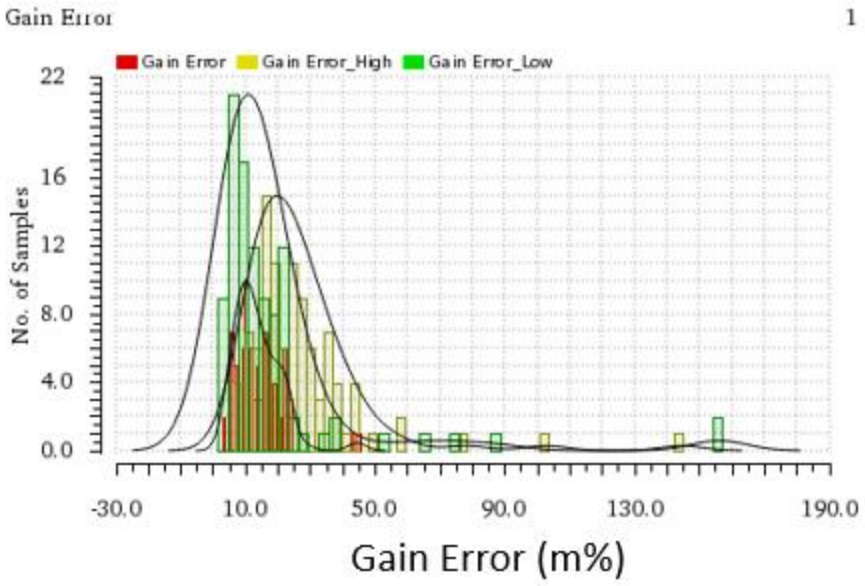

Figure 23. FDDA Buffer Gain Error Results

Next, the input-referred offset of the buffer is simulated. While the error caused by this offset is eliminated by the chopping scheme, it does increase the required range of the ADC or require reference-voltage trimming in the ADC. Therefore, it is useful to have an idea of the offset voltage of the buffer. The results of the Monte-Carlo offset simulations are shown in Figure 24 below. The maximum input-referred offset is around 6mV which corresponds to a maximum output offset of approximately 60mV. Therefore, the ADC reference voltages will need to be adjusted so that the input range is higher to account for this offset.

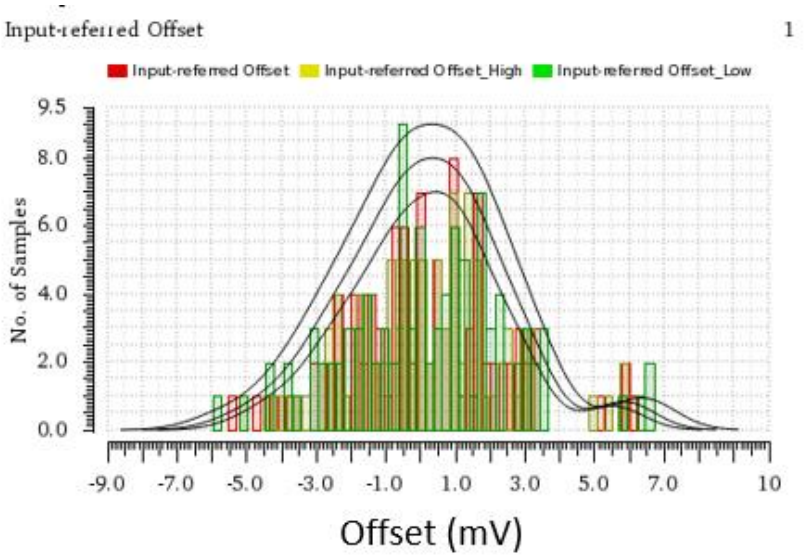

Figure 24. Buffer Offset Simulations

Next, the noise of the buffer is simulated and is shown in Figure 25 below. This simulation is performed at 85°C and at the slow corner.

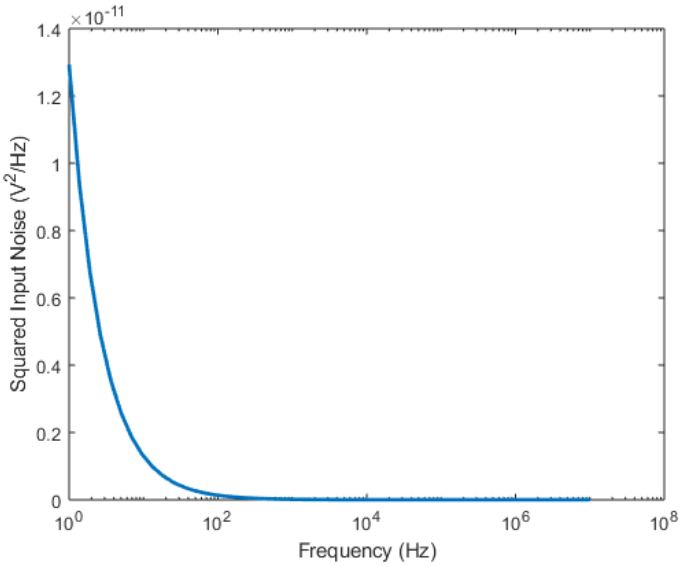

Figure 25. Buffer Squared Input Noise

The integrated input-referred noise from 5kHz (due to the chopping) up to 1.5MHz, which is the noise-bandwidth of the ADC's signal transfer function, is 44μV. The DSP at the output of the ADC will average 40,000 samples which provides an effective input-referred noise of 200nV. Therefore, the maximum 3-σ peak-to-peak noise is 600nV which represents an error 0.2% relative to the voltage drop caused by the reference current source. Therefore, the buffer should provide sufficient noise performance for the desired accuracy. The buffer consumes a total of 500μW from the 1.8V supply.

3.1.2 ADC

The mono-bit first-order sigma-delta ADC topology used in this design is shown in Figure 26 below. A mono-bit topology is used to ensure that non-linearities in the ADC do not affect the accuracy of the current measurement.

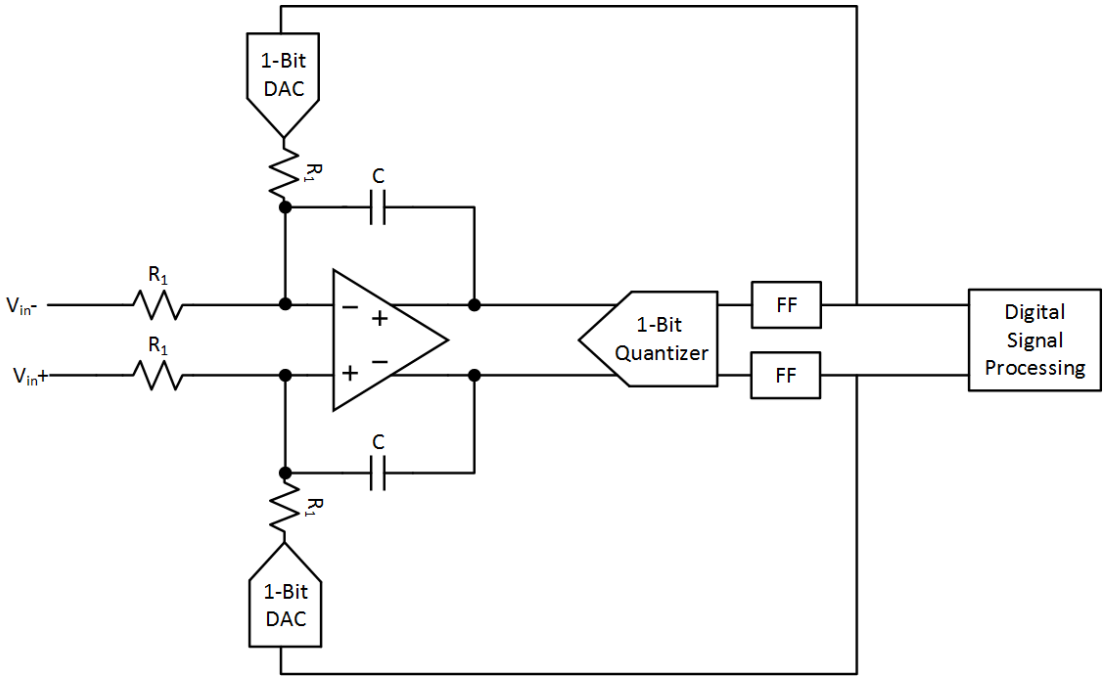

Figure 26. ADC Topology

The loop filter gain can be found to be the following, assuming an ideal op-amp:

$$H(s) = \frac{1}{R_1 C s} \tag{25}$$

From this, the signal transfer function is:

$$STF = \frac{H(s)}{1+H(s)} = \frac{1}{sR_1C+1} \tag{26}$$

Therefore, the ADC provides a gain of unity at DC and attenuates high frequency components. The bandwidth of the STF is set to 1MHz. We can also find the transfer function from the quantization noise of the 1-bit quantizer to the output:

$$NTF = \frac{1}{1+H(s)} = \frac{sR_1C}{1+sR_1C} \tag{27}$$

The noise transfer function has a zero at the origin and a pole at the cutoff frequency of the integrator in the loop filter. Therefore, the sigma-delta modulator shapes the quantization noise of the 1-bit ADC up to higher frequencies. This is useful in this application because the moving average filter applied at the output of the ADC will attenuate much of this high-frequency noise. Therefore, although a 1-bit ADC is used, the effective resolution of the ADC can be much higher.

The analysis in [23] provides an expression for the error between the output of the ADC and the mean value of the input signal when an integrating filter is applied. This bound is given by:

$$\left|\bar{u} - \frac{1}{N} D_{out}[N]\right| \leq \frac{1}{N} \tag{28}$$

In this equation, u is the normalized input signal, N is the number of samples averaged at the output, and D_{out} is the output of the sigma-delta modulator and has a value of either 0 or 1. Therefore, we see that the effective quantization error of the ADC is reduced by

increasing the number of samples averaged at the output. Additionally, as discussed before, the noise from the buffer is also reduced by increasing the number of samples averaged at the output.

From (26), we can find the minimum number of ADC samples required, and therefore the minimum ADC sampling rate, to achieve the desired 1% accuracy for the V_{DD} supply. The following analysis assumes that the reference current is 30mA. Therefore, the voltage difference created by the reference current must be measured with an accuracy of better than 1%. In order to ensure sufficient margin, an accuracy of 0.5% is assumed. First, we calculate the maximum quantization error voltage using (28).

$$\epsilon \leq \frac{V_{FS}}{N} \tag{29}$$

Next, we calculate the expected voltage drop caused by the reference current source:

$$\Delta V = 10m\Omega \cdot 30mA = 300\mu V \tag{30}$$

We assume that this voltage is multiplied by the ideal buffer gain of 10 before it reaches the ADC. Additionally, the maximum voltage at the input of the buffer when 4A of current are flowing through the current sense resistor is 40mV. Therefore, V_{FS} will need to be approximately 800mV to account for the positive and negative polarities during chopping. Therefore:

$$\frac{\epsilon_{max}}{3mV} < 0.5\% \rightarrow \frac{800mV}{N \cdot 3mV} < 0.5\% \rightarrow N \sim 50000 \tag{31}$$

Therefore, in order to ensure sufficient accuracy, the PA and reference outputs should be sampled for 100µs with a sampling rate of 500MHz.

The op-amp used in the loop filter is shown in Figure 27 below. This op-amp is a Miller-compensated fully differential amplifier with zero-nulling resistors. Because the

integrator bandwidth is only 1MHz, the GBW of the op-amp does not need to be large. Therefore, a minimum GBW of 40MHz is targeted. The transistor lengths are chosen to provide a gain of at least 74dB, and the compensation network is designed to provide a phase margin of at least 60 degrees across all temperature and process variations.

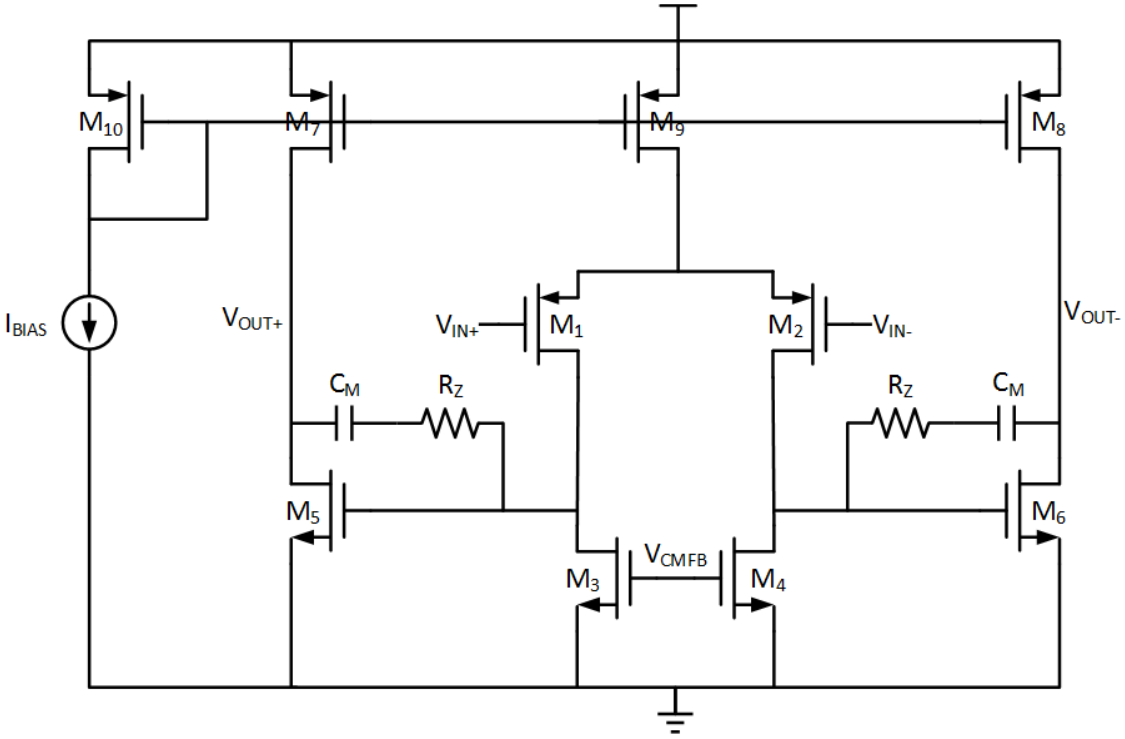

Figure 27. Loop Filter Op-amp

Figure 28 also shows the CMFB amplifier used by the op-amp. This CMFB amplifier is very similar to the CMFB amplifier used in the buffer and will not be discussed here.

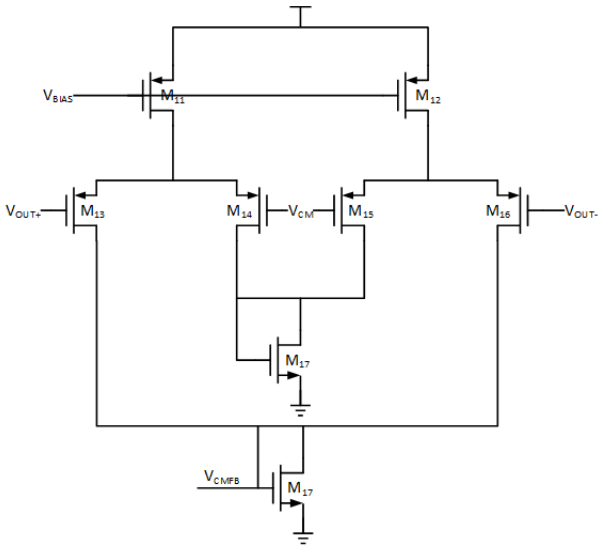

Figure 28. CMFB Amplifier for Loop Filter Op-amp

Figure 29 below shows the GBW of the op-amp across 100 Monte Carlo iterations with the same temperature variations described in the buffer section. The GBW remains above 40MHz across all variations.

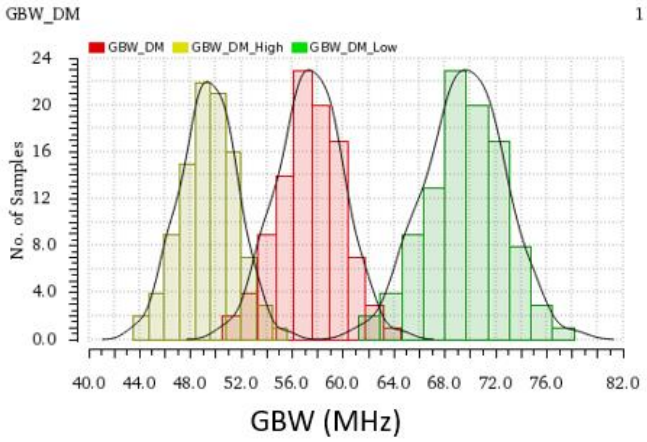

Figure 29. Loop Filter Op-amp Bandwidth

Figure 30 below shows the phase margin of the amplifier for the same 100 iterations. The phase margin remains above 60 degrees for all cases.

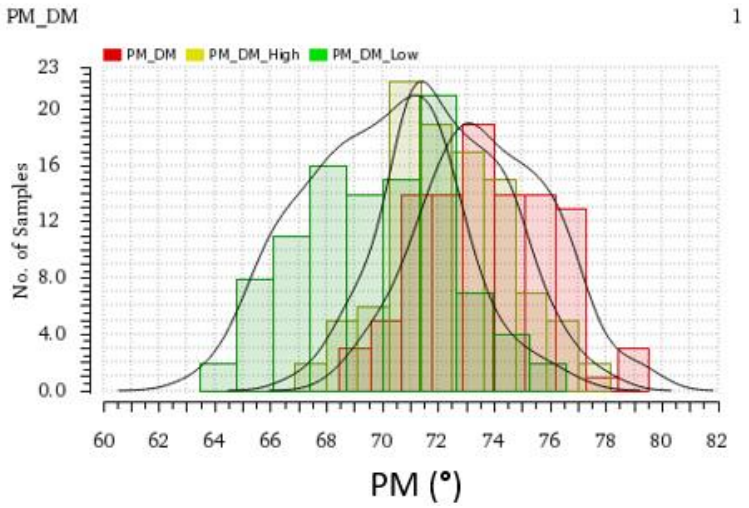

Figure 30. Loop Filter Op-amp Phase Margin

Lastly, the gain of the op-amp is measured. The gain of the op-amp sets the minimum input signal that can be properly processed by the sigma-delta. Therefore, a high gain is crucial to digitize small input signals. Therefore, the minimum gain for the op-amp is approximately 74dB. As seen in Figure 31 below, this is achieved for all Monte-Carlo iterations.

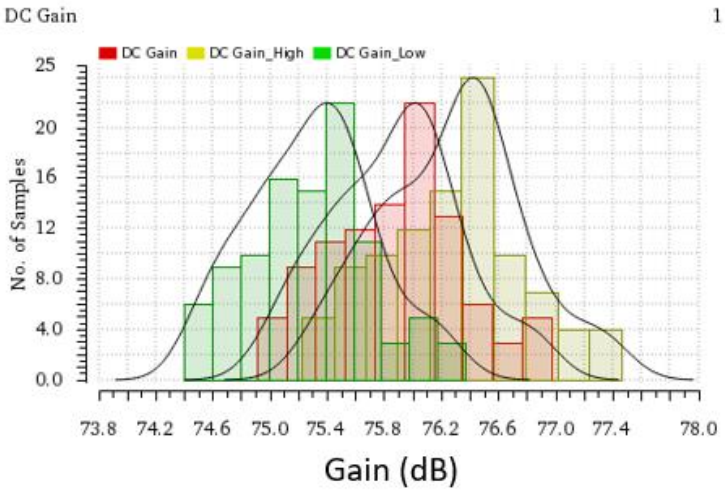

Figure 31. Loop Filter Op-amp Gain

The offset of the op-amp does not greatly affect the performance of the ADC as the error due to offset is eliminated by the chopping scheme. Nonetheless, Monte-Carlo iterations indicate that the maximum op-amp offset is approximately 4.5mV.

Next, the design of the ADC's 1-bit quantizer is discussed. The quantizer is implemented using the strong-ARM latch shown in Figure 32 below. The strong-ARM comparator provides full CMOS output levels with no static power consumption and a fast decision time. There are four phases of operation for the strong-ARM latch. The first is when the CLK signal is low and M_5 is turned on. During this time, the output nodes and the drain nodes of the input transistors are pulled up to V_{DD} in order to reset the latch. According to the analysis in [24] CLK goes high, M_1 supplies current to the differential pair formed by the M_2 transistors. This phase is called the sampling phase. At this point, the output voltages begin to be pulled down and this phase is called the sampling phase. Once the output drops sufficiently low and the PMOS transistors M_4 begin to turn on, M_3

and M_4 form a positive feedback loop that regenerates the differential output voltage and pulls the two outputs to either V_{DD} or ground. The duration of the sampling period is proportion to the output capacitance and is inversely proportional to the current supplied by M_1. Therefore, the speed of the latch can be improved by sizing M_1 larger to provide more current when CLK is high to the differential pair. This obviously comes at the cost of higher power consumption.

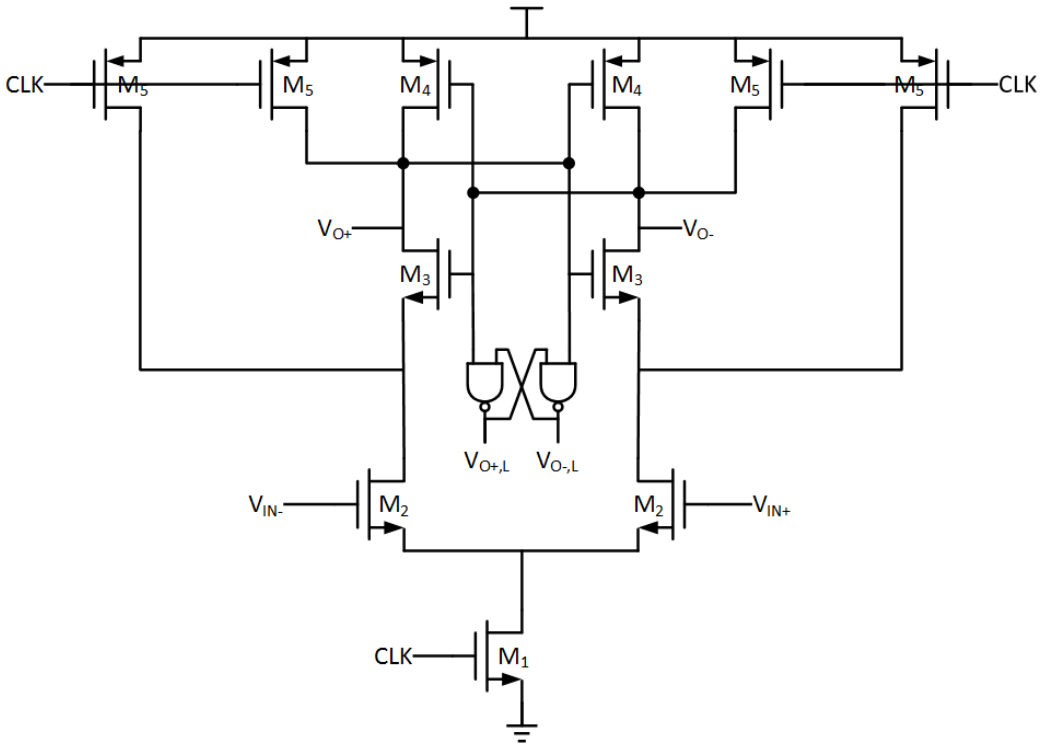

Figure 32. Strong-ARM Comparator

The Strong-ARM comparator above was simulated to ensure it was sufficiently fast for the desired 500MHz sampling rate. The output of the comparator must reach a valid state before the falling edge of the clock when it is latched into the flip-flops

following the comparator. Therefore, since the comparator provides an output on the rising edge of the clock, the comparator should provide a valid output within 1ns. Figure 33 below shows the falling delay of the comparator. The falling delay is defined as the time elapsed between the clock rising edge passing through 50% of its final value to the digital output of the strong-ARM comparator reaching 90% of its final value. As seen in Figure 33 below, the quantizer reaches a valid output within a maximum of approximately 500ps which is well within the desired 1ns.

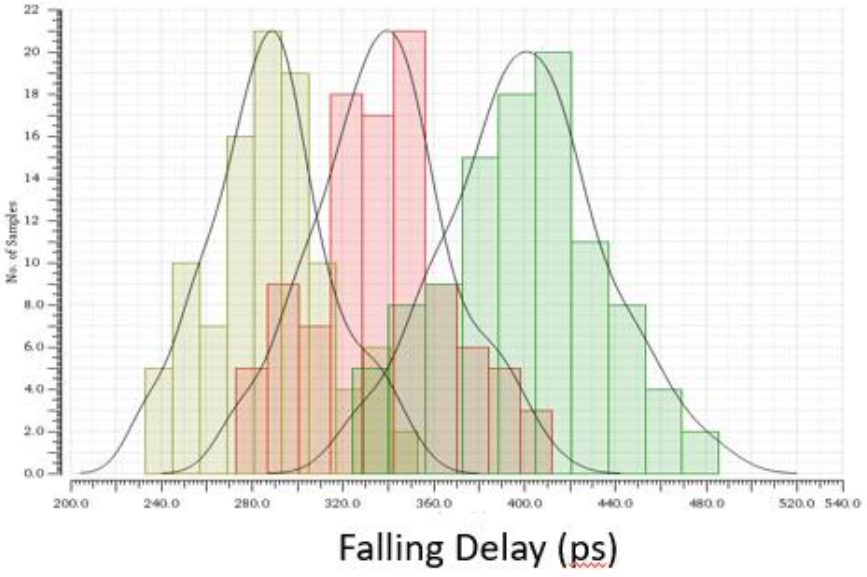

Figure 33. Falling Delay of Quantizer

Figure 34 below shows the rising delay of the quantizer. Again, the rising delay reaches a maximum of 440ps and is well within the desired maximum of 1ns.

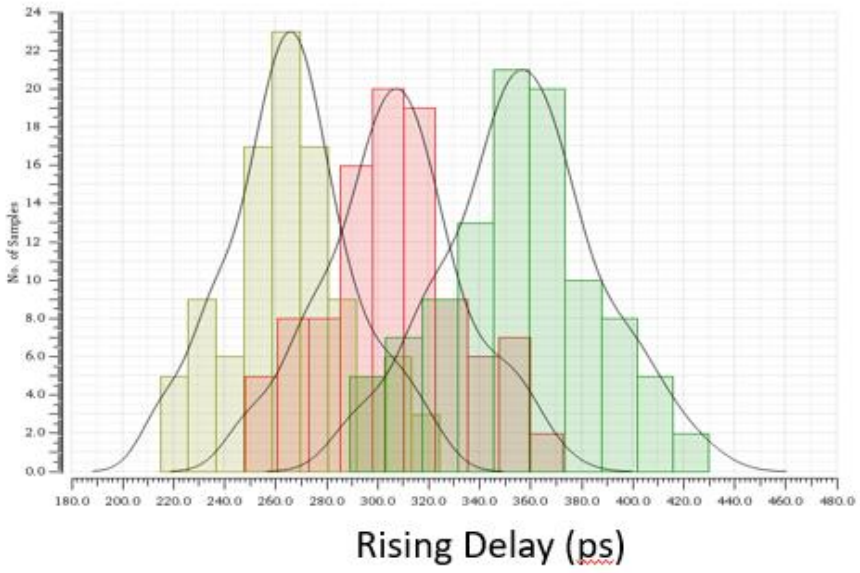

Figure 34. Rising Delay of Quantizer

The 1-bit DAC in the ADC is implemented using two CMOS transmission-gate switches that are driven by the flip-flops at the output of the quantizer. The switches select between a high and low reference voltage that are set by off-chip references for testing purposes.

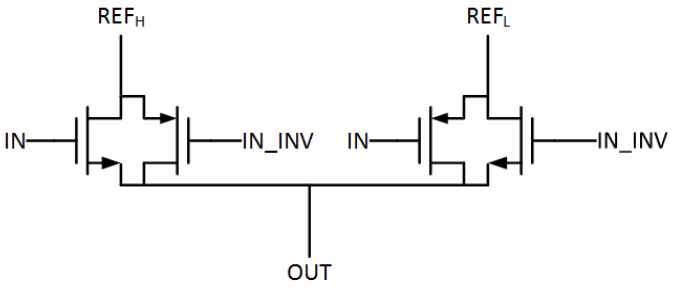

Figure 35. 1-bit DAC

3.1.3 Reference Current Source

The reference current source used to generate the calibration current is shown in Figure 36 below.

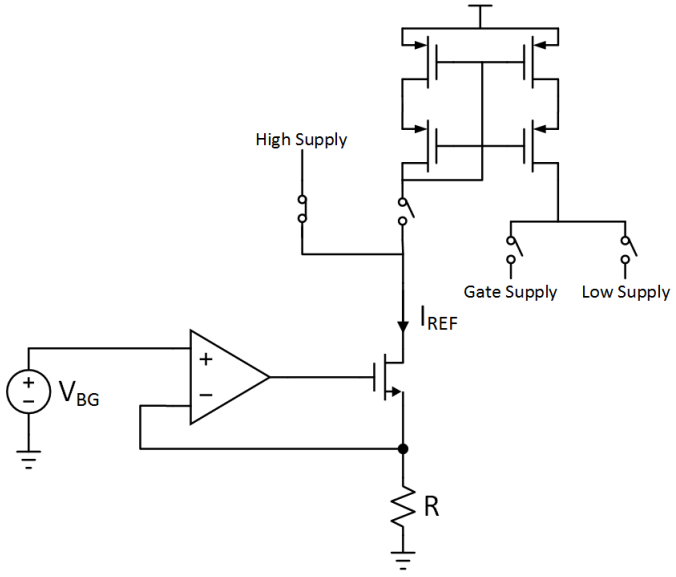

Figure 36. Reference Current Source Schematic

This reference current source utilizes a voltage reference and a resistor to generate the calibration current. The op-amp in Figure 36 above adjusts the gate voltage of the NMOS transistor to ensure that the positive and negative terminals of the op-amp are equal. Therefore, the current through the NMOS transistor is adjusted such that the current times the resistance is equal to the bandgap voltage. Therefore, the generated current is:

$$I_{REF} = \frac{V_{BG}}{R} \tag{32}$$

From the equation above, we see that both the bandgap voltage and the resistor value should be very accurate in order to provide an accurate reference current. Indeed, as

mentioned in the explanation of the current sensor's architecture, the accuracy of the reference current is one of the main components determining the accuracy of the overall sensor. Therefore, an accurate and temperature-stable voltage reference (a bandgap voltage reference) is used to provide V_{BG}. An accurate external resistor is also used since the resistance of on-chip resistors varies greatly with process variations.

As mentioned above, one of the main components of the reference current source is the bandgap voltage reference. This voltage reference must provide a temperature-stable voltage that is largely independent of process variations and mismatch. The schematic of the chosen bandgap voltage reference is shown in Figure 37 below and is based on the design in [25]. The op-amp adjusts the gate of the PMOS transistor until the inputs of the op-amp are equal. Additionally, since R_1 is the same in both branches, the current through both branches is also the same. Therefore, the voltage across R_2 is equal to the difference in the base-emitter junction voltages of the two PNP BJT transistors:

$$V_{R2} = V_{BE,Q1} - V_{BE,AQ_1} = V_T \ln(A) \tag{33}$$

Where A is the ratio of the area for the two BJT transistors. Therefore, the current through R_2 is simply V_{R2}/R_2. Since the current through both branches is the same, the output voltage is:

$$V_{BG} = V_{BE,Q1} + I_{R2}R_1 + 2I_{R2}R_3 = V_{BE,Q1} + \frac{V_T \ln(A)}{R_2} \cdot (R_1 + 2R_3) \tag{34}$$

Therefore, we note that the output voltage contains two terms. One is a the V_{BE} voltage of Q_1 which decreases as temperature increases. The other is proportional to the thermal voltage, V_T, which increase as temperature increases. Therefore, if the resistor ratio for the second term is chosen properly, the inverse temperature dependence of the first term

can cancel out the proportional temperature dependence of the second term and a temperature-stable reference can be obtained. The resistor values are chosen such that R_1 and R_3 are 80kΩ while R_2 is 25kΩ. These values provide minimal temperature variation.

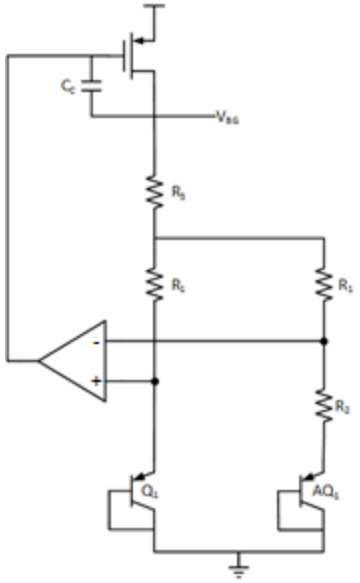

Figure 37. Bandgap Voltage Reference Schematic

The above analysis assumes That the input offset of the comparator is equal to 0V. In reality, the offset of the comparator will be added to the ideal voltage across R_2. Therefore, the output voltage will with an op-amp offset of V_{OS} will be:

$$V_{BG} = V_{BE,Q1} + I_{R2}R_1 + 2I_{R2}R_3 = V_{BE,Q1} + \frac{V_T \ln(A)+V_{OS}}{R_2} \cdot (R_1 + 2R_3) \qquad (35)$$

We see that the offset voltage is also multiplied by the same resistor ratio as the thermal voltage. Therefore, a 1mV op-amp offset spread will lead to a 9.6mV spread for the bandgap output. Therefore, the op-amp offset spread should be reduced as much as possible. As a result, the chopper-modulated op-amp topology shown in Figure 38 is used.

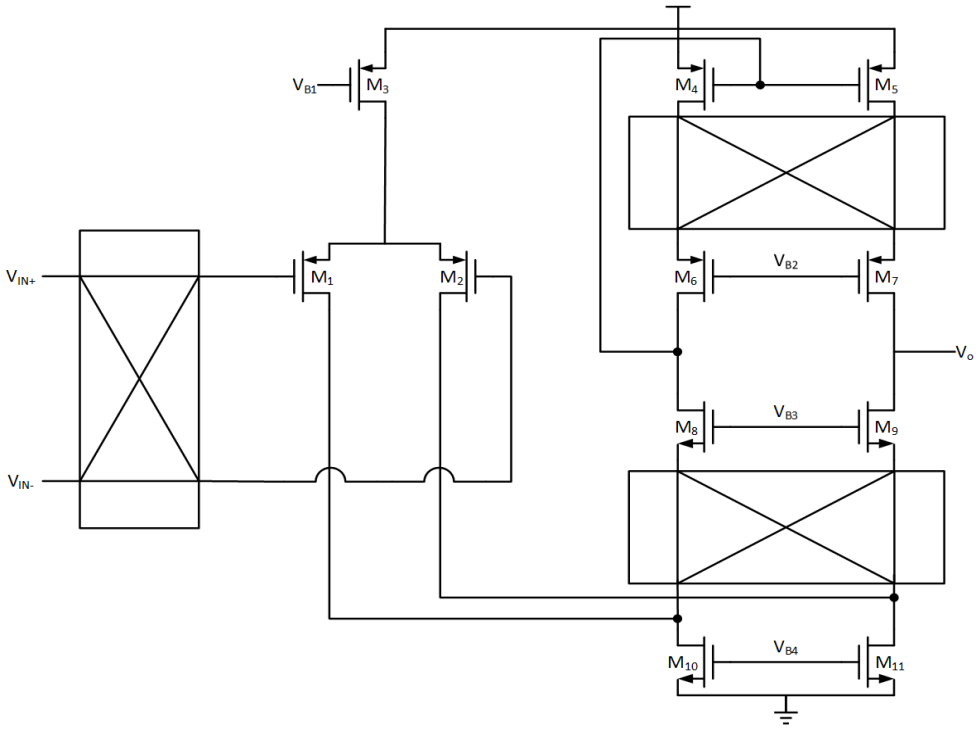

Figure 38. Chopper-Modulated Op-Amp

This op-amp contains a chopper modulator at the input and two chopper modulators in the signal path. Since the inputs to M_1 and M_2 as well as the drains of M_{10} and M_{11} are fully differential, their offset can be completely eliminated by the chopper modulators [25]. The transistors M_4 and M_5, however, have inherent asymmetry due to the diode-connection of M_4. Therefore, the offset introduced by mismatch in these transistors cannot be completely eliminated. This offset, however, can be reduced by reducing the threshold-voltage mismatch between the two transistors by ensuring that they have a large area. The op-amp offset across 100 Monte-Carlo runs across the full operational temperature range is shown in Figure 39 below. The offset spread is approximately 210µV which will contribute an error spread of +/-0.084% from the

nominal value of approximately 1.2V. Therefore, the op-amp offset variation should not lead to excessive errors in the bandgap output voltage.

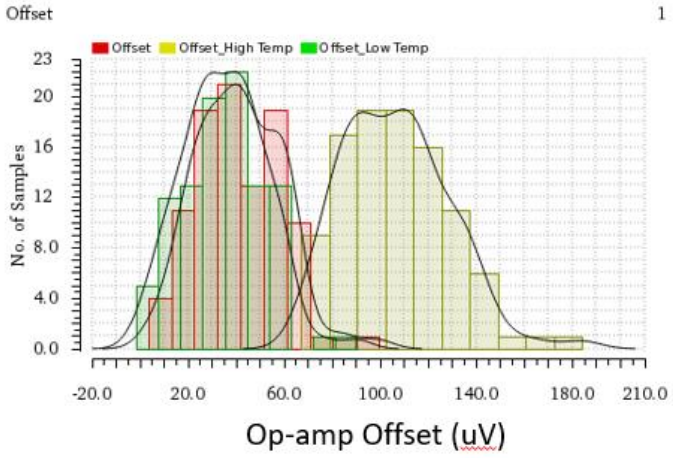

Figure 39. Bandgap Op-amp Offset

Figure 40 below shows the bandgap output voltage across process variations, mismatch, and temperature variations. The voltage is spread over a range from 1.189V to 1.21V which represents an error of +/-0.875%. While this error is close to the maximum error tolerance for the overall sensor, the discussion below will show that a single temperature trim can greatly improve the accuracy if needed.

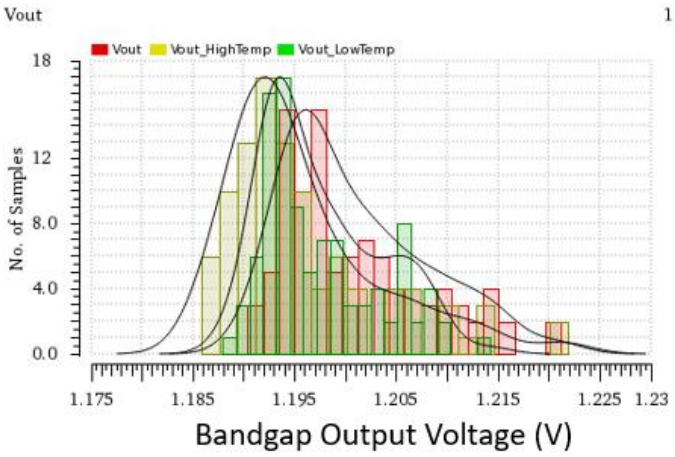

Figure 40. Bandgap Output Voltage

The op-amp used in the reference current source is the same op-amp utilized in the bandgap since the offset spread of the op-amp in the reference current source will also lead to reference current errors.

The reference current source also contains a cascoded current mirror to change the direction of the reference current. This is required because the negative and gate supplies require the current to be sourced rather than sunk by the reference current source. The current mirror used to achieve this is shown in Figure 40 below. A cascode current source is used to ensure the output current of the current mirror does not change as the level shifting capacitor for the reference current source is charged and the voltage at the input of the reference current source for the gate and low supplies increases. This also helps to improve the matching between the two branches. Large transistors are used since a 30mA current must be mirrored. Additionally, the large transistors help to improve matching in the midst of random process mismatches between the two current mirror branches.

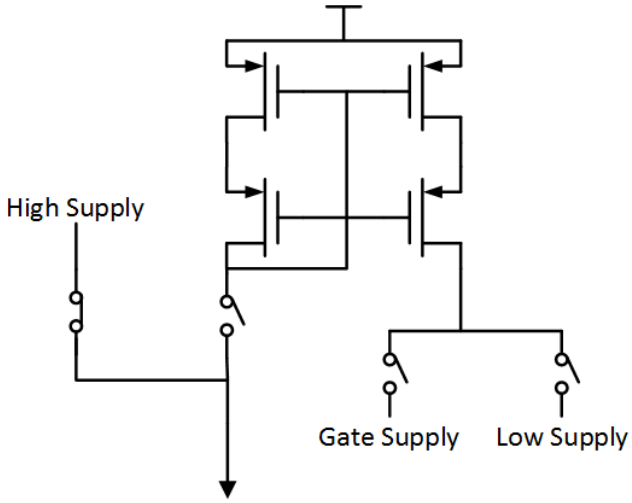

Figure 41. Reference Current Source Current Mirror

Also shown in Figure 41 above are the switches used to direct the reference current to the various sense resistors. When the V_{DD} supply is being measured, the high supply switch is closed while the current mirror switch is opened. This allows the reference current source to sink the reference current through the V_{DD} sense trace. When the other two supplies are being measured, the high supply switch is opened while the current mirror switch is closed. The switch for the desired supply is then closed so that the reference current source can source the reference current through the V_{SS} or V_{GG} sense traces. These switches are implemented using CMOS transmission gates with large-width transistors to ensure resistive voltage drops across the switches are minimized.

Figure 42 below shows the reference current across temperature, process, and mismatch variations. The reference current varies from 30.48mA to 31mA which represents an error spread of approximately +/-0.84%. This error spread is very close to the maximum tolerable 1% error for the sensor and matches the error expected based on

the bandgap Monte-Carlo simulations. It is interesting to note, however, that the reference current does not change drastically with temperature.

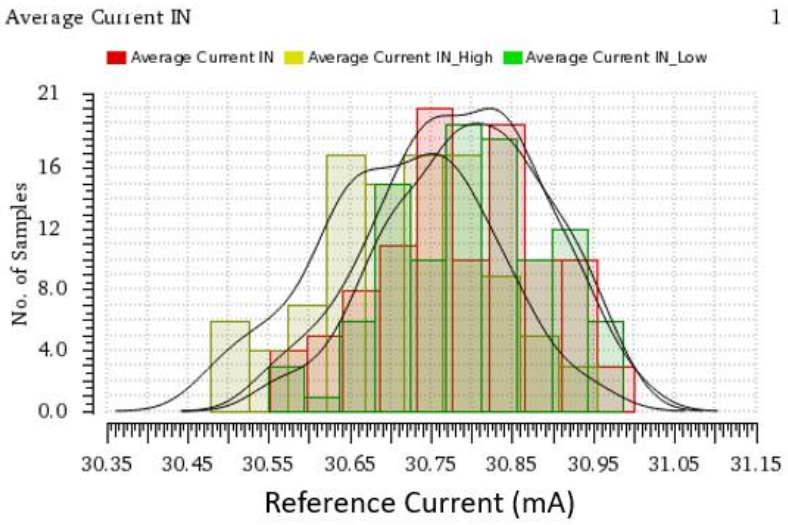

Figure 42. Reference Current Output

With the above observation that the reference current does not appear to change drastically with temperature, the maximum current variation over temperature from the current value at room temperature is plotted for each Monte-Carlo iteration in Figure 43 below. This graph provides the expected maximum error in the reference current source if a single-temperature trim is applied to the current sensor. The maximum current error is 0.084mA which represents an error of approximately 0.28% from the mean of 30.1mA. Therefore, a single-temperature trim can greatly improve the accuracy of the reference current source.

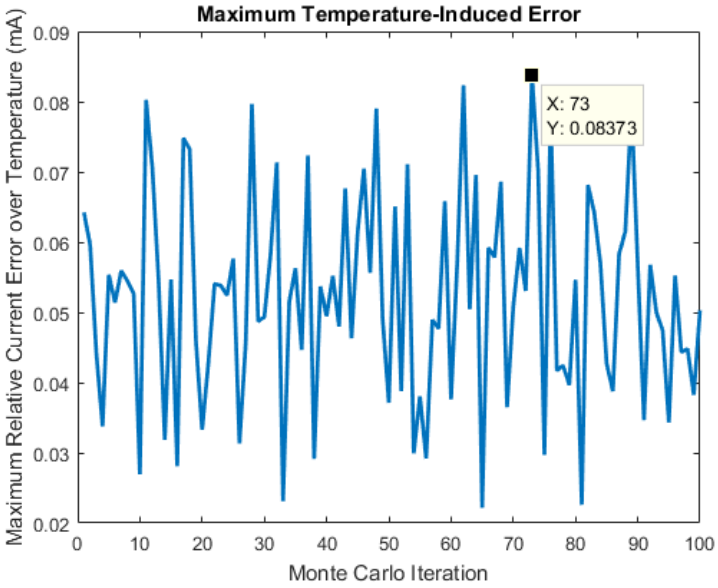

Figure 43. Maximum Temperature-Induced Error for each Monte-Carlo Iteration

Lastly, the current mirror utilized in the reference current source is simulated. The results are shown in Figure 44 below. The maximum mismatch error is approximately 0.13%. Because the V_{SS} and V_{GG} supplies have lower current measurement accuracy requirements (a maximum accuracy of 4% is required), this error is tolerable.

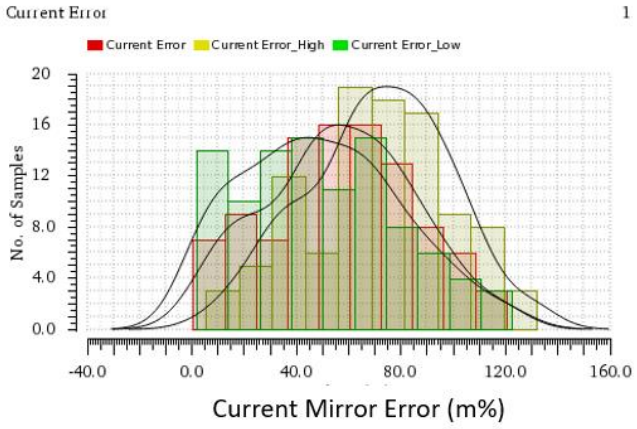

Figure 44. Current Mirror Mismatch Error

3.1.4 Level-Shifting Capacitors

While the concept of the level-shifting capacitors was discussed previously, this section will present some implementation details for the chips that implement these level-shifting interfaces. The schematic for the chip implementing the interface for the V_{DD} supply is shown in Figure 45 below. This chip includes a substrate bias generator which consists of three diode-connected transistors along with an external resistor and capacitor. The voltage drop across the three diode-connected transistors is approximately 1.8V so the voltage $V_{SS,SW}$ provides a substrate bias voltage as well as a lower supply for the inverter. The resistor and capacitor must sustain around 38.2V and must therefore be implemented using external components. The purpose of the capacitor is to provide low-pass filtering for the substrate bias voltage.

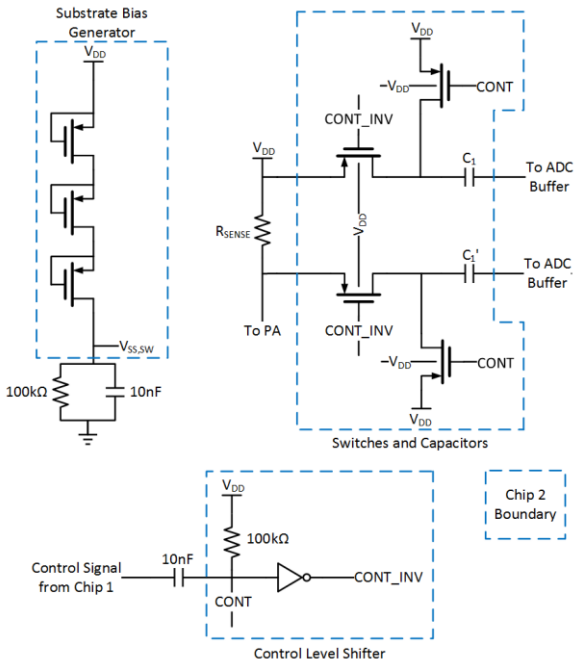

Figure 45. V_{DD} Interface Chip

Also implemented on this chip are the switches used for the level-shifting capacitor charging. These are implemented by the PMOS transistors found in Figure 45 above. When the signal CONT is low, the capacitors are charged to the voltage discussed in the previous section. When the signal CONT goes high, the signal CONT_INV goes low and the sense voltage is passed through to the level shifting capacitors. This control voltage comes from the digital controller on the main chip and must therefore be shifted up to a voltage suitable for the interface chip. This is accomplished using an external 10nF capacitor and a 100kΩ resistor connected to the V_{DD} supply voltage. The control signal voltage from the main chip is normally high. Therefore, the signal CONT is normally high which means the switches connecting the sense resistor to the level shifting capacitor are normally on. When the capacitors must be recharged, the control signal goes low which forces CONT to go low as well. This activates the charging switches and deactivates the other switches. Since the charging period is only a few micro-seconds and the time constant of the AC-coupling is a milli-second, the voltage at CONT does not experience excessive droop.

The level-shifting capacitors are implemented using metal-metal capacitors with a breakdown voltage of approximately 100V. All metal layers are used in the capacitors stack with metal layers 1, 3, and 5 forming one plate of the capacitor, and metal layers 2, 4, and 6 forming the other capacitor plate. The total capacitance is approximately 30pF. The absolute value of this capacitance is not critical to the accuracy of the sensor, but the level shifting capacitor does form a capacitive divider with the input capacitance of the

buffer on the main chip. Therefore, the sense voltage is multiplied by the gain of this divider:

$$V_{sense,buf} = V_{sense} \cdot \frac{C_{shift}}{C_{shift}+C_{buf}} \tag{36}$$

Since the drain-bulk capacitance of the capacitor-charging transistors on the main chip is non-linear, the level-shifting capacitance, C_{shift}, should be much larger than the total input capacitance of the buffer. This ensures that the non-linear capacitance does not introduce significant non-linearities into the reference current measurement.

The interface chip schematic for the negative and gate supplies are shown in Figure 46 below. This chip is very similar to the chip used for the V_{DD} interface with the PMOS switches replaced with NMOS switches and the substrate bias generator connected with the V_{SS} supply as the "ground supply" and the three diode-connected transistors creating a positive supply that is used in the inverter.

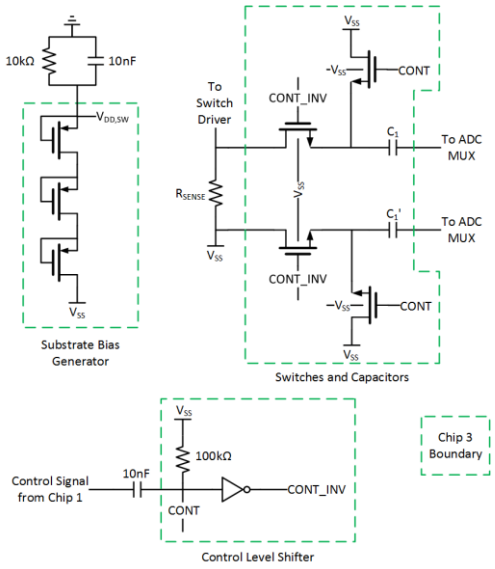

Figure 46. Interface Chip Schematic for Negative and Gate Supplies

3.1.5 Digital Control Block

The digital control block uses a 1MHz clock and a counter to generate the various used to control the level-shifting capacitors, the multiplexor at the input of the ADC, and the reference current source. The figure below shows the basic timing of the various supply measurements. First, the V_{DD} supply is measured. The measurement period includes a capacitor charging period, a PA measurement period, and a reference current measurement period. The high supply takes the longest measurement time since the accuracy requirements for the high supply are the most stringent. The gate supply and the low supply both take less time since fewer ADC output samples are required to achieve the 4% (worst-case) accuracy requirement. The gate supply and the low supply use identical timings.

Figure 47. Sensor Measurement Timing

A Verilog description of the digital control block was created, and this Verilog code was used to generate a synthesized netlist which was then automatically placed and routed using a standard cell library.

3.1.6 Startup Protection

The purpose of the level-shifting capacitors is to ensure the voltage at the input of the buffer is at a safe level for the standard CMOS process used in this design. Although during normal operation these capacitors fulfill their purpose, it cannot be assumed that the capacitors will be properly charged when the system is turned on. Therefore, the 40V supply rising up at system startup will tend to pull the voltages at the level-shifting capacitor interfaces to very high voltages that will damage the chip. Therefore, passive charging and discharging paths are required to ensure the chip is not damaged on startup.

One such charging path is shown in Figure 48 below. When the V_{DD} supply rises and C_{AC1} is not charged, the voltage at the reference current source output will also begin to rise. Once the diode stack becomes forward-biased, current will begin to flow through the diode stack and will charge the capacitor C_{AC1}. Therefore, the diode stack will clamp the input voltage of the reference current source to a safe voltage.

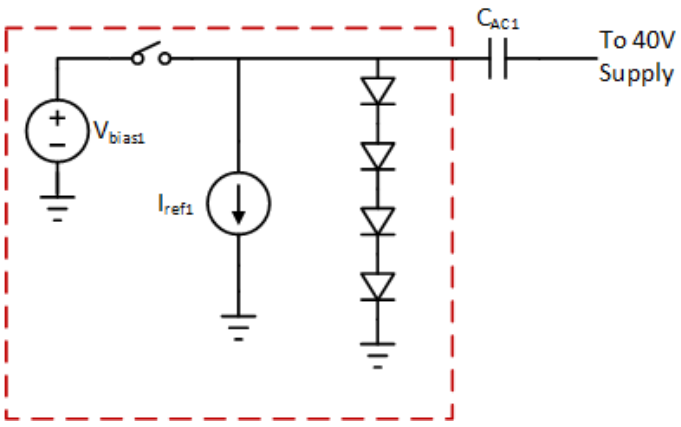

Figure 48. Reference Current Source Protection

The main concern in the design of the diode clamp is the amount of current it will need to sink. Lab measurements show that the power supply rises from 0V to 40V with a rise time of 100µs. Therefore, the current through the level shifting capacitor with a constant voltage on one side is:

$$I = C \cdot \frac{dV}{dt} = 1\mu F \cdot \frac{40V}{100\mu s} = 400mA \tag{37}$$

Therefore, the series resistance of the diode stack should be sufficiently low such that this current does not cause a large voltage at the input of the reference current source. The process's ESD diodes are used since these provide very low series resistance. Since a stack of four diodes is used, the clamp begins to turn on at 2.4V of forward bias which should not affect normal circuit operation. In addition to this diode clamp, the transistors interfacing with the level-shifting capacitor in the reference current source are thick-oxide 3.3V supply transistors. These transistors have a much higher breakdown voltage than the standard 1.8V transistors used in the rest of the design.

Based on the above discussion, the level shifting capacitor interface at the input of the buffer will also need to be protected. In this case, the capacitor is much smaller and the current through the capacitor to maintain a constant voltage at the buffer input during supply startup is much smaller. Therefore, a typical ESD diode is used to protect this input node. This diode is connected to V_{DD} and will become forward-biased if the input voltage rises above approximately 2.5V. The ESD diode is able to handle the amount of current required to maintain a safe voltage at the input of the buffer. This same protection scheme is also used for the switch control interfaces and is shown in Figure 49 below.

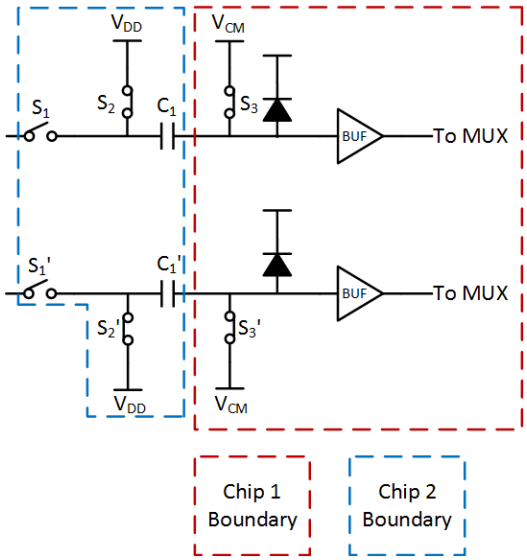

Figure 49. Buffer Interface Protection

Ideally, the V_{DD} supply will be high when the 40V supply begins to rise, but this may not necessarily be the case. Therefore, a static clamp is added to ensure the low-voltage supply does not rise too high during startup if the power supply for it is in a high-impedance state. This static clamp, in addition to the typical transient "BigFET" clamp is shown in Figure 50 below.

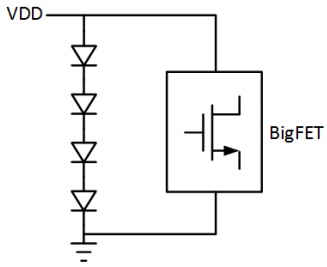

Figure 50. VDD Static and Transient Clamps

Some simulations were run at the maximum expected operating temperature and slow process corners to ensure the protection schemes described above are able to adequately handle the startup condition. In this simulation, the 1.8V supply for the main chip is activated 1µs after the 40V supply for the PA begins to rise at a rate of 0.4V/µs. The results are shown in Figure 51 below. During the initial period, the transient ESD clamp holds the main chip supply voltage low which keeps many of the other interface voltages low as well. After the transient clamp deactivates, however, the static clamp begins to hold main chip supply voltage to approximately 2.8V. All other voltages within this time remain below the breakdown voltages for their respective interfaces. Therefore, the protection circuit should be adequate for this application.

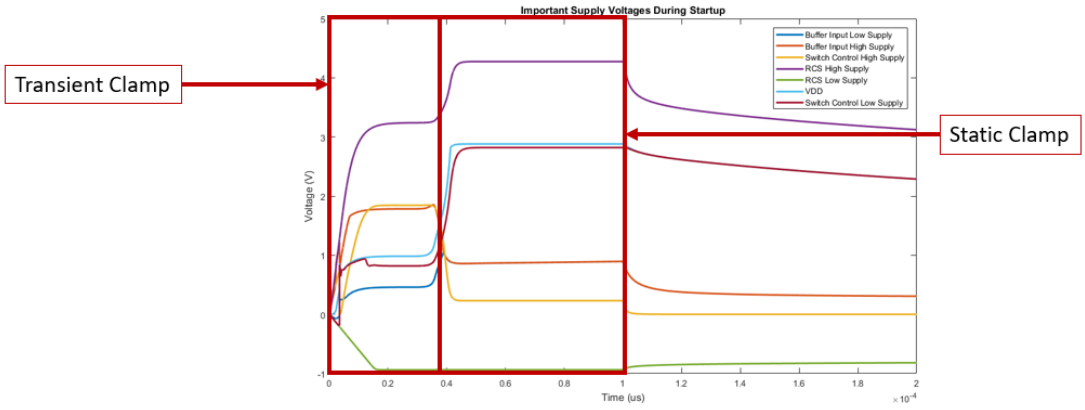

Figure 51. Interface Voltages During Startup

3.1.7 Top-Level Simulations

Some top-level post-layout simulations have been run to verify the performance of the current sensor. The PRF of the PA current is varied from 10kHz to 10MHz while the

duty cycle is varied from 5% to 50% with a peak PA current of 2A. This varies the average PA current from 100mA to 1A and the modulator current is assumed to be 95mA. These top-level simulations do not include variations in the reference current source or any error due to noise, so these errors must be added in later. The current sense resistance for these simulations is 10mΩ. Table 5 below shows the results of the simulations.

Table 5. Current Sensor Post-Layout Simulation Results

PRR	DC	Expected Current (A)	Current Estimate (A)	Simulated Error (%)
10kHz	5%	0.195	0.194	0.515
	50%	1.095	1.09811	0.284
1MHz	5%	0.195	0.19506	0.032
	50%	1.095	1.0976	0.238
10MHz	5%	0.195	0.1959	0.461
	50%	1.095	1.0987	0.337

With errors due to quantization and buffer non-linearities present in the results presented above, the maximum measurement error of 0.515% is close to the expected maximum error. This error is composed of a 0.5% error due to the quantization error and 0.075% due to the buffer nonlinearity. The maximum expected reference current source error of 0.28% and the maximum expected noise error of 0.2% are added to the maximum measurement error in Table 5 above to obtain an expected absolute maximum error of

0.995% which is within the desired 1% error. In Section 3.3, laboratory measurements supporting the simulation results shown in this section will be presented.

3.3 Current Sensor Measurements

The laboratory measurements for the current sensor utilize two printed circuit board (PCBs). The first PCB implements three current sources that are used to generate the desired input test current for the three supplies. This board also houses two current sense resistors for each supply. The first is a PCB trace that has a nominal resistance of approximately 10mΩ at room temperature and the second is a 0.1% accurate 10mΩ resistor. This accurate resistor is included only for debugging purposes. A basic schematic for this PCB is shown in Figure 52 below. The current source is implemented using a high current output op-amp and an accurate sense resistor. The differential voltage at the input of the op-amp is set to obtain the desired current. The current is confirmed using a digital multimeter before the measurement from the current sensor is obtained.

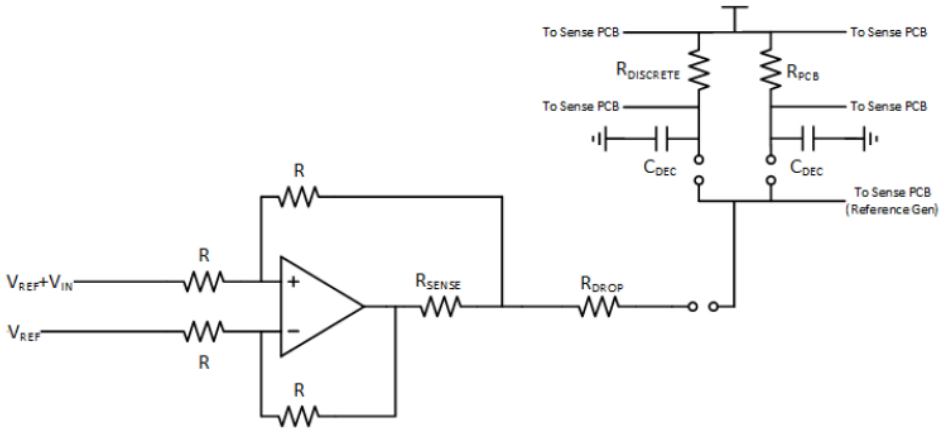

Figure 52. Current Source PCB Schematic

A photograph of the current source PCB is shown in Figure 53 below. Large heatsinks are used for the current-generating op-amps since these must sink or source up to 4A.

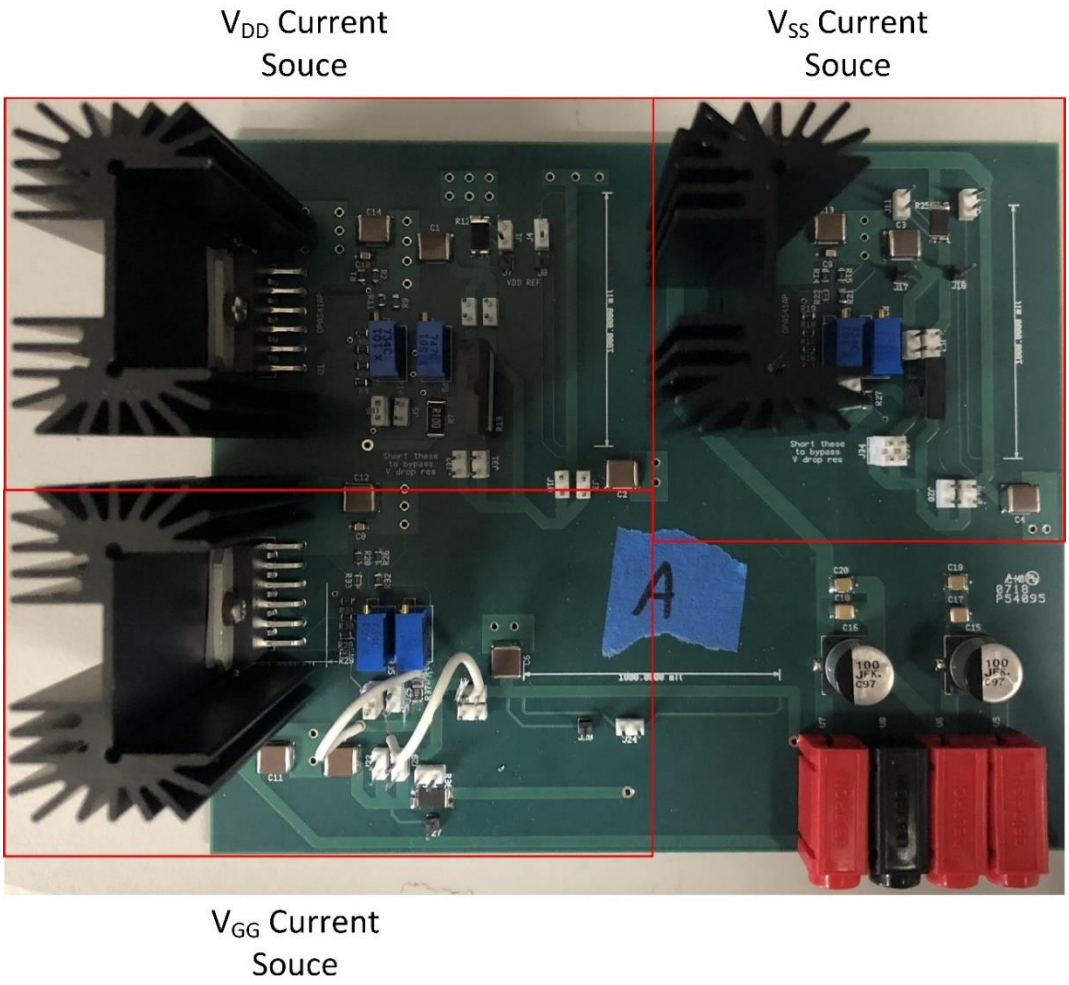

Figure 53. Current Source PCB

The second PCB houses the fabricated current sensor, the interface chips, and any external components required for these chips. The 500MHz output of the current sensor's

ADC along with the current status of the measurement is read using a high-speed oscilloscope. Because 50Ω drivers were not included on-chip, high-speed drivers were implemented using discrete op-amps with high GBW. The voltage across the sense resistor on the first PCB is routed to the PCB housing the current sensor using jumper wire. Additionally, the reference current from the current sensor is routed to the sense resistor through another jumper wire. The various bias voltages and bias currents required by the current sensor are set using potentiometers and are adjusted to provide the required nominal values. The required 500MHz sampling clock is provided by a high-speed function generator. Figure 54 below shows a photograph of the current sensor PCB.

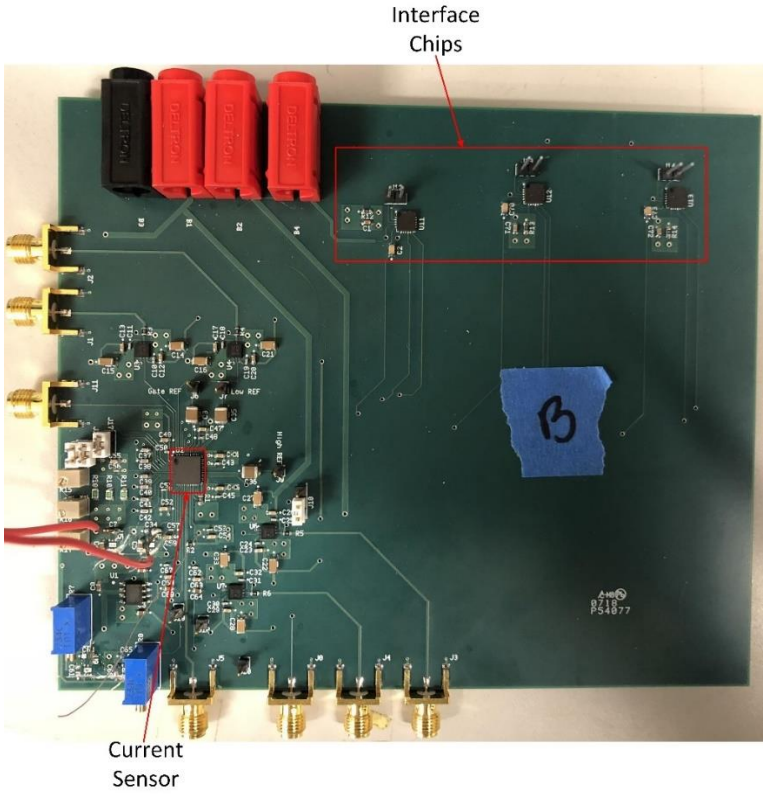

Figure 54. Current Sensor PCB

The chip described above is fabricated in TowerJazz's 0.18µm process. A chip micrograph is shown in Figure 55 below with the major sections of the chip labeled. The total area, including padframe, is 2mm by 2mm. The reference current source takes up most of the utilized chip area as the transistors in the reference current source must be large to accommodate the large current.

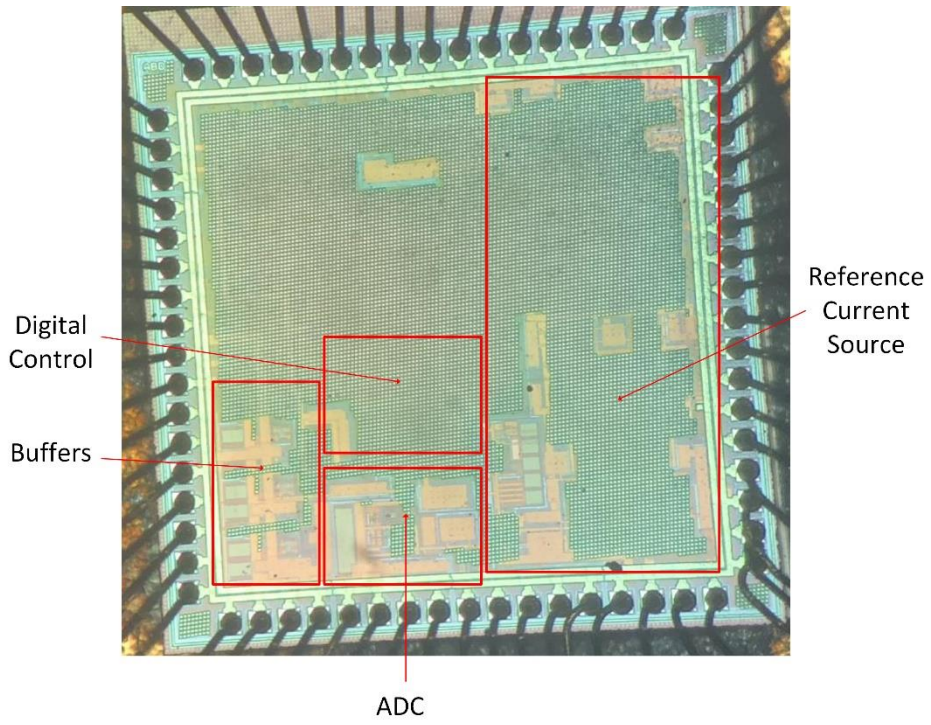

Figure 55. Current Sensor Chip Micrograph

The testing of current sensor begins with the V_{DD} supply since this supply has the highest accuracy requirement. The input DC current is swept from 100mA to 4A while the supply voltage is 40V. The output of the ADC as well as the bits that indicate the status of the measurement are obtained using a high-speed oscilloscope. Figure 56 below

shows the output status bits for a full measurement cycle. When status bit 0 is high, the PA measurement is being performed. When both status bit 1 is high, the reference current source measurement is being performed. There are four reference current source measurements performed for each supply each measurement cycle and each measurement is performed for 25µs. Four separate measurements must be performed to recharge the level-shifting capacitor for the reference current source periodically.

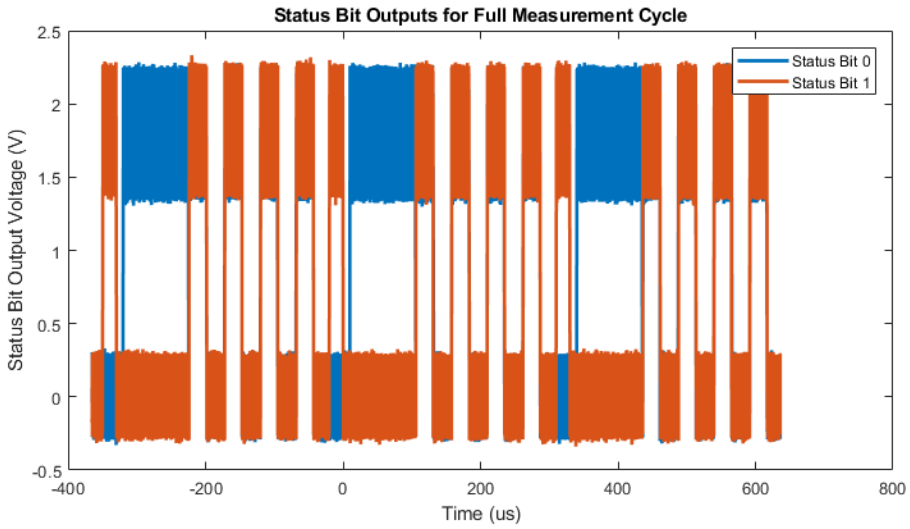

Figure 56. Current Sensor Status Bits

The output of the ADC during the charging time (when the offset of the current sensor may be measured) is shown in Figure 57 below along with the sampling clock for the ADC. The output has a duty cycle near 50% which indicates that the offset of the current sensor is small. Nonetheless, any measured offset is cancelled by the chopping modulation at the input of the buffer. This output bit stream is saved to a file by the high-speed oscilloscope and is processed in MATLAB to find the detected current.

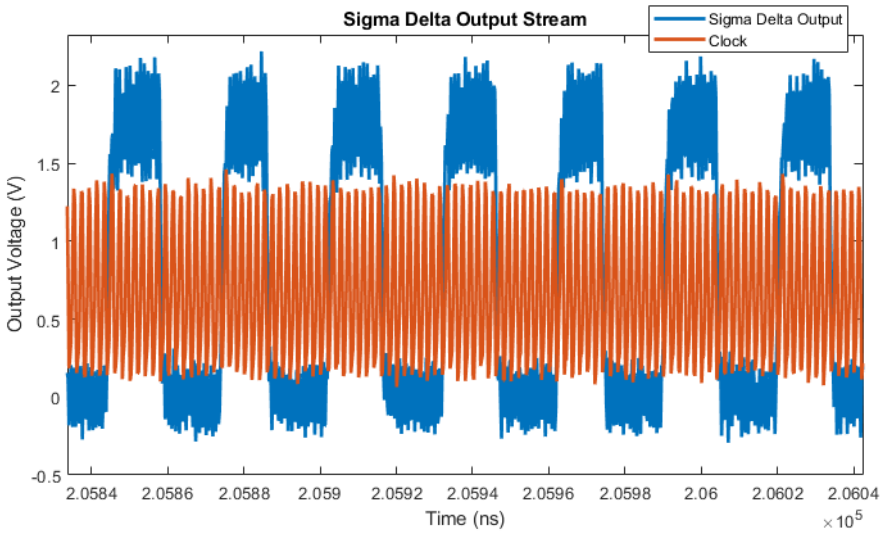

Figure 57. Sigma-Delta Output Bit stream

Figure 58 below shows the detected current of the current sensor for an input current ranging from 100mA to 4A. Also plotted is the ideal measurement curve. The detected current shows a very linear relationship with the input current and Figure 58 shows little error between the ideal and the measured curve.

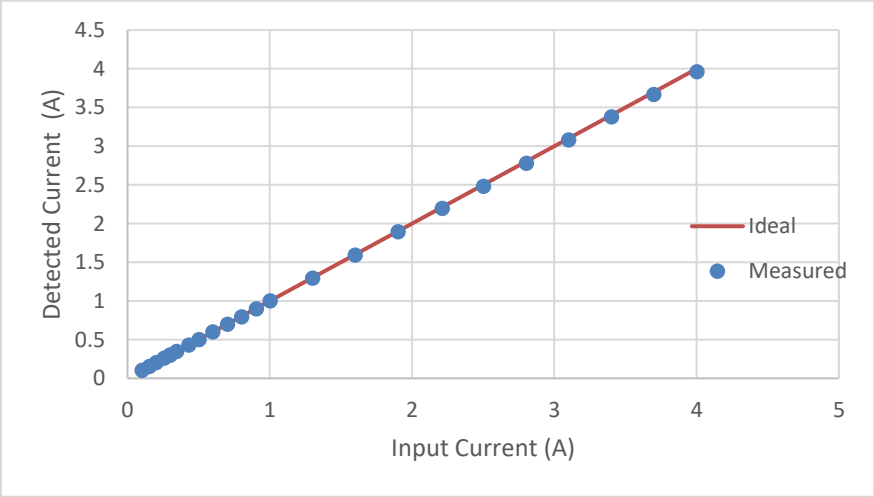

Figure 58. Detected Current from Current Sensor

This low error is confirmed in Figure 59 below which plots the percent error between the detected current and the input current as measured by the multimeter. The error remains below 1% across the full input range but gets close to this maximum value at an input current of 4A. This is because the reference voltages of the ADC are set such that the full-scale input is slightly above 4A to accommodate the reference current. Therefore, when the input current rises to this level, noise at the input of the ADC that rises above the full-scale level is not properly averaged out. Therefore, the measurement error will be larger. Nonetheless, the accuracy may be improved by utilizing a larger measurement period. The random variations in the measurement error from point to point are caused by quantization error in the ADC as well as the noise of the current sensing system.

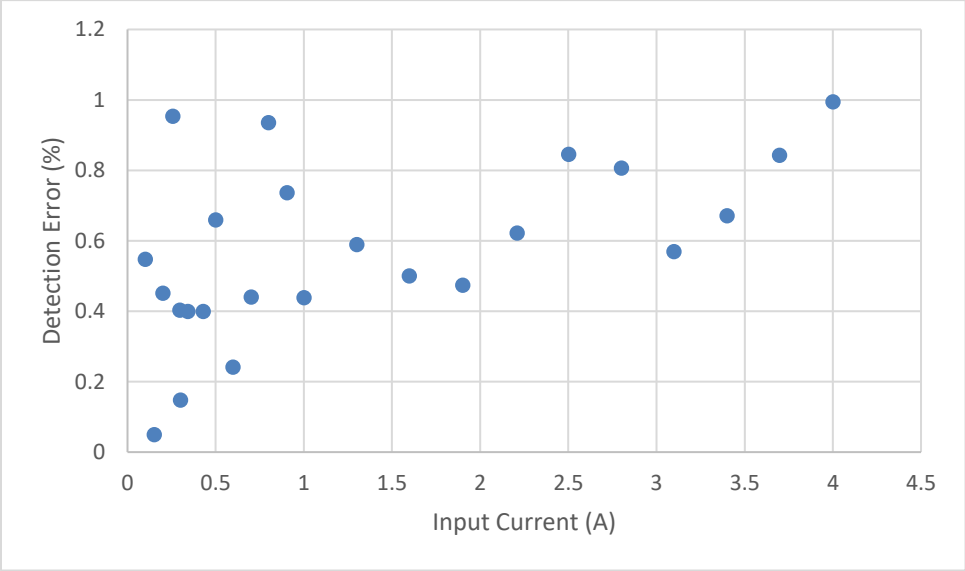

Figure 59. Detection Error for DC Input

To ensure the moving average filter implemented in MATLAB can effectively eliminate the impact that ripple on the input current has, a DC input current of 1A is used and the amplitude of the 50kHz current ripple around this DC input current is varied from 0A to 100mA. The detection error is shown in Figure 60 below. The detection error does not vary beyond the expected amount when the noise of the current sensor itself is considered. Therefore, it clear that the digital filtering can effectively remove the input tone at 50kHz.

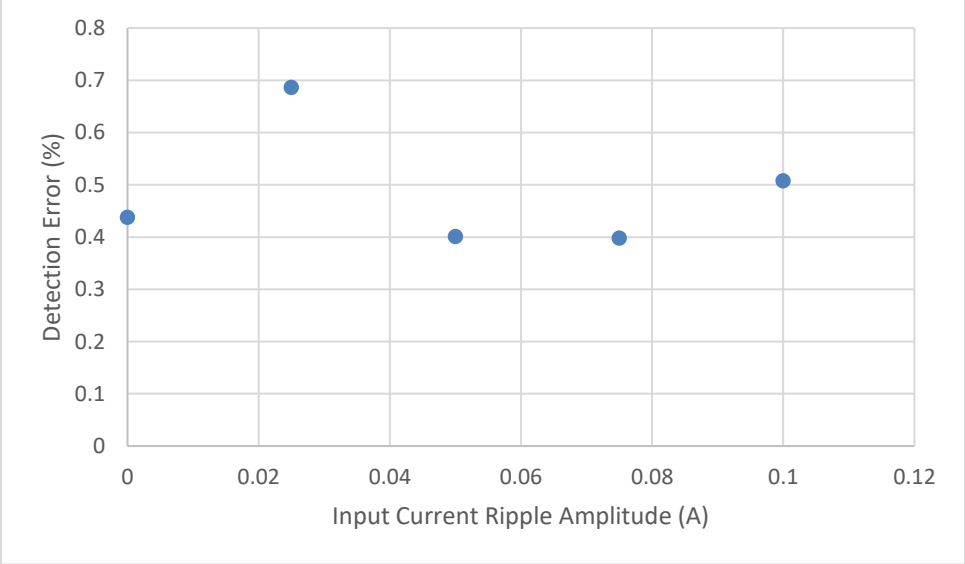

Figure 60. Detection Error for Various Input Current Ripple Amplitudes

Figure 61 below shows the absolute detection error for input currents ranging from -250mA to 100mA for the V_{SS} supply. All points have absolute detection errors within the required 10mA.

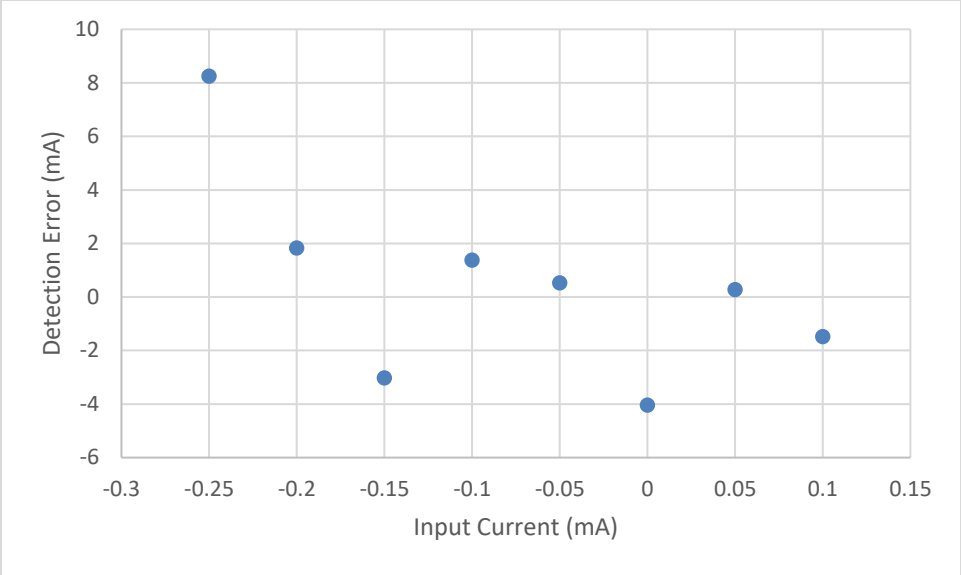

Figure 61. Detection Error for V_{SS} Supply

4. PROPOSED POWER DETECTOR

4.1 Power Detector Architecture

4.1.1 Problem Description

The purpose of the power detector is to measure the power of the incoming pulse-modulated wave at the end of the pulse's "on" time. This peak hold power at the end of the pulse's "on" time is measured to ensure the output power of the PA is within a desired range and to calculate the PAE of the PA. Since the PAE is one of the primary parameters to be optimized by the proposed PA control loop, the power detector must provide an accurate estimate of the input and output powers. The input carrier wave is between 2GHz and 4GHz and the pulse modulation has a PRF ranging from 50kHz to 10MHz and a DC ranging from 5% to 50%. Therefore, the power detector will have to a handle a reasonably wide input frequency range as well as a wide range of pulse modulation parameters. The input to the peak detector comes from a directional coupler attached to the input or the output of the PA. With a 40dB coupler placed at the output of the PA, the input power of the detector ranges from -10dBm to 10dBm. With a 20dB coupler placed at the input of the PA, the input power of the detector also ranges from -10dBm to 10dBm. Therefore, the detector will need to have a dynamic range of 20dB with a maximum detection error of +/-0.5dB to provide the desired accuracy in calculating the PAE. Additionally, the detector will need to provide a power estimate within 1ms an should provide an absolute power measurement to ensure the computational engine for the PA control loop does not require excessive calibration to obtain a power estimate from the output of the power detector. These requirements are summarized in Table 6 below. It is important to note

that a 0.5dB error in the power corresponds to an error in the detected amplitude of approximately 6%.

A previously fabricated power detector design was able to meet the above specifications and will be discussed briefly in this section. The detector proposed in this research improves upon the previous design and is designed to achieve a dynamic range of 40dB with the same detection error, input frequency range, and maximum detection time. The previous power detector's measurements will also be discussed in Section 4.3.

Table 6. Power Detector Requirements

Parameter	Requirement
Dynamic Range	~40dB
Maximum Detection Error	+/-0.5dB
Input Frequency	2-4GHz
Detection Time	<1ms
PRF	50kHz-10MHz
Duty Cycle	5%-50%

4.1.2 Architecture Overview

In order to understand some of the design choices made in the new power detector, the previous detector's architecture must be discussed. This architecture is shown in Figure 62 below.

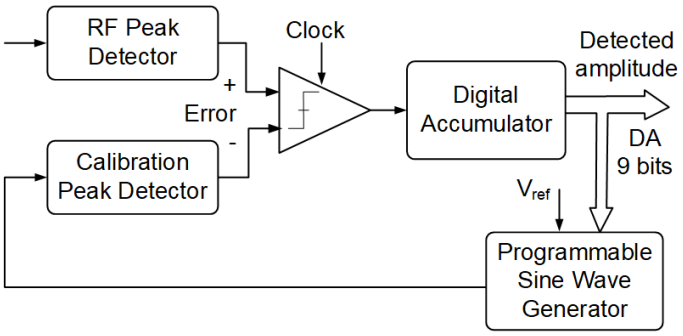

Figure 62. Previous Power Detector Architecture

The detector consists of a BJT-based RF peak detector whose input is the signal from the directional coupler and a calibration peak detector whose input is a variable-amplitude sine-wave generated on the power detector chip. As discussed previously, the output DC level from the peak detector increases as the input amplitude increases. The generated sine-wave has a frequency much lower than the input signal but has an amplitude that can be accurately set by a 9-bit digital input signal. In order to provide an accurate measure of the input power, the digital accumulator implements a successive approximation algorithm. This algorithm begins by setting the MSB of the 9-bit amplitude control word to "1" and all other bits to "0". This sets the amplitude at the output of the programmable sine wave generator to its mid-scale value. The output of the two peak detectors are then sampled at the end of a pulse period and compared using a clocked comparator. If the RF peak detector output is higher, the input amplitude is higher than the current reference amplitude. Therefore, the MSB is kept at a value of "1" and the bit below the MSB is set to "1" and another comparison is made. On the other hand, if the RF peak detector output is lower than the calibration peak detector's output, the input amplitude is lower than the current reference amplitude. Therefore, the MSB is set to "0"

and the bit below the MSB is set to "1" and another comparison is made. After 9 comparison cycles, all bits in the successive approximation register are resolved and the detected amplitude can be read from the output of the digital accumulator. Therefore, this power detector system provides calibration of the peak detector on-chip and does not require additional calibration of the baseband processor.

There are several error sources that affect the accuracy of the power detector shown in Figure 62. One is the offset of the comparator. Any offset in the comparator leads to an offset between the input amplitude and the output amplitude once all bits in the successive approximation register are resolved. The comparator offset can be referred back to the input amplitude by dividing by the peak detector gain at the RF input amplitude. The gain is defined as the change in the peak detector's output DC level divided by the change in input amplitude. Therefore, the slope of the line in the plot showing the output DC level plotted against the input amplitude in Figure 63 below provides the peak detector gain.

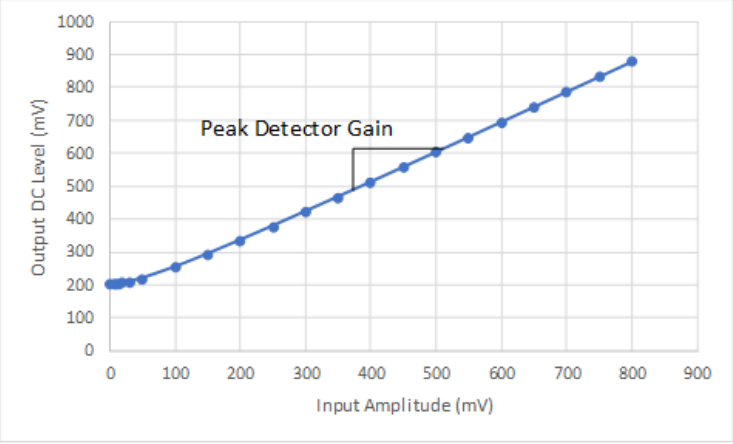

Figure 63. Peak Detector DC Output vs. Input Amplitude

It is interesting to note that the peak detector gain is relatively constant at high input amplitudes but begins to decrease for lower input amplitudes. This phenomenon is clearer in Figure 64 below which plots the slope of the curve in Figure 63 against the input amplitude. The reasoning for this drop in the peak detector gain will be discussed in the next section describing the implementation of the new power detector. Nonetheless, this decrease in the peak detector gain leads to large errors at low input amplitudes in the presence of offset in the comparator in Figure 62. For example, suppose the comparator has a reasonably low offset of 100μV. At an input amplitude of 100mV, the peak detector's sensitivity is approximately 0.735V/V. Therefore, the error introduced by the comparator offset is:

$$\epsilon = \frac{V_{OS}}{H_{PD}V_{amp,in}} \cdot 100 = \frac{100\mu V}{0.735 \cdot 100mV} \cdot 100 = 0.136\% \tag{38}$$

This amplitude error corresponds to a power detection error of 0.012dB and does not significantly affect the accuracy of the detector. However, if the input amplitude to the detector is 10mV, the error is:

$$\epsilon = \frac{100\mu V}{0.143 \cdot 10mV} \cdot 100 = 7\% \tag{39}$$

This error corresponds to a power detection error of 0.587dB which is already above the maximum detection error allowable for the overall detector. Therefore, if the dynamic range of the detector is to be extended to include lower input amplitudes, offset in the comparison between the input and reference peak detectors must be reduced.

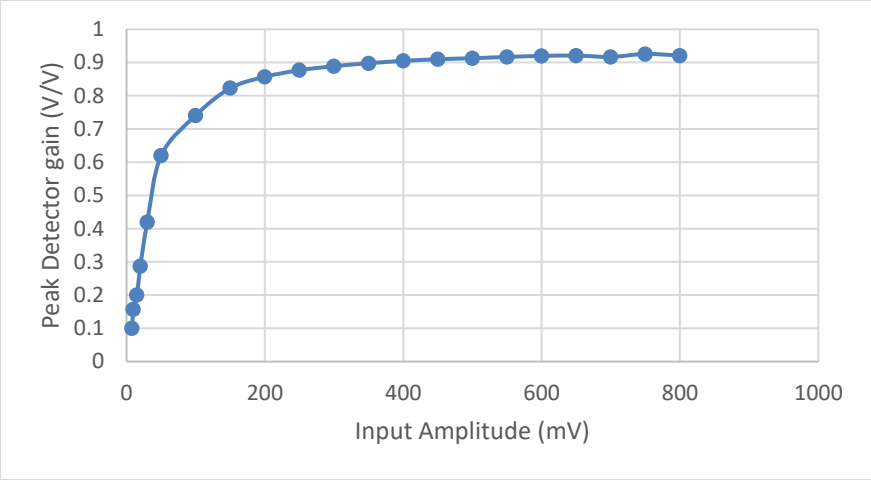

Figure 64. Peak Detector Gain

The next major source of error in the previous architecture was the accuracy of the amplitude at the output of the sine-wave generator. This accuracy is mainly determined by the number of bits allocated to the amplitude control in the generator. Increasing the number of bits improves the accuracy of the amplitude control but also increases the complexity and area of the sine-wave generator. Therefore, the number of bits in the previous power detector design was chosen to ensure the amplitude step for one LSB in the sine-wave generator caused a maximum error of 2.5% at the lowest input amplitude:

$$LSB = \frac{A_{high} - A_{low}}{2^N - 1} = \frac{500mV - 37.5mV}{2^N - 1} < 37.5mV \cdot 0.025 \rightarrow N > 8.95 \qquad (40)$$

Therefore, the sine-wave generator was designed to have a 9-bit amplitude control. To extend the input range of the power detector to lower input amplitudes, the number of amplitude control bits in the sine wave generator must be increased. This is because, at low input amplitudes, the old detector's amplitude step of 906µV represents an unacceptable error in the detection output. For example, at a 10mV input amplitude, this

step represents a 9.06% error in the amplitude or a 0.75dB. The number of control bits in the sine wave generator will need to be increased to achieve a larger dynamic range.

The final major source of error in the previous power detector was ripple at the output of the two peak detectors. While the ideal peak detector output is a constant DC voltage, the discussion on BJT-based peak detectors mentioned that the output voltage begins to discharge during the low portions of the input sine wave. Therefore, there is some voltage ripple on the output of the peak detectors. This is illustrated in Figure 65 below which shows the DC output of the peak detector with noticeable ripple. In the previous detector design, the peak detector output is sampled at the end of a pulse period. Therefore, the ripple adds significant uncertainty to the detected amplitude. The new detector solves this issue by sampling the two peak detector waveforms throughout the pulse period (even when the pulse is off) and averaging the samples similarly to the averaging done in the current sensor. Therefore, the high-frequency ripple components are heavily attenuated and do not impact the accuracy of the power measurement.

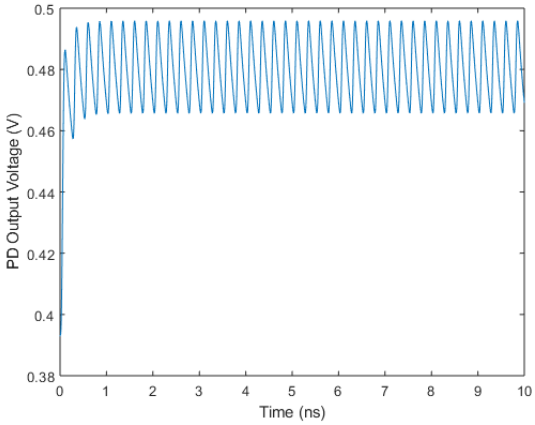

Figure 65. PD Output Showing Significant Ripple

With these considerations in mind, the architecture in Figure 66 is proposed for the new power detector. There are three main changes which help improve the accuracy of the new detector. The first is the increase in the number of amplitude bits in the sine-wave generator. Indeed, the sine-wave generator architecture is completely changed from the previous detector. The next change is the addition of the Sigma-Delta ADC which measures the output of the two peak detectors rather than a simple comparator. Lastly, an offset measurement period is introduced so the offset between the peak detector outputs, the offset of the amplifier, and the offset of the ADC can be measured and subtracted out during the comparisons.

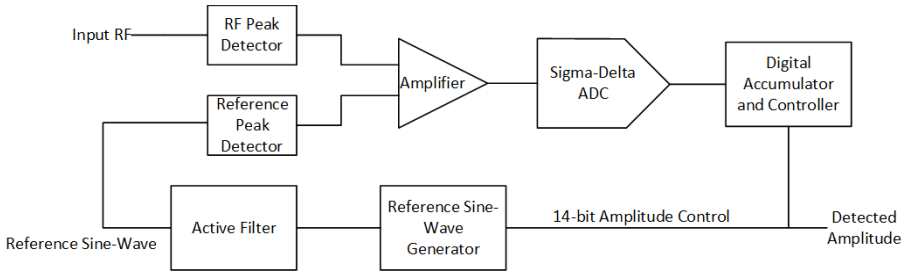

Figure 66. Proposed Peak Detector Architecture

The digital accumulator is still implemented using a successive approximation register and will therefore require 14 comparisons to complete the search for the input amplitude. During each measurement cycle, the offset of the peak detectors (caused by mismatch between the detectors) as well as the offset of the amplifier and the sigma-delta are measured and will be subtracted out from the comparison by the controller. After measuring the offset, the same successive approximation algorithm is performed. During each comparison for the successive approximation, the amplifier subtracts the reference

peak detector output from the RF peak detector output and the number of "1" output bits from the sigma delta is counted. The offset measurement is then subtracted from this count. If the number of "1" output bits is higher than half the number of total output bits from the sigma-delta then the RF peak detector output is larger than the reference peak detector output and the current bit is set to "0". Otherwise the current bit is set to "1". This process continues until all 14 bits are resolved. With the averaging of the sigma-delta ADC, the quantization noise and effect of other error sources, such as power detector ripple and offset, can be greatly reduced. Additionally, the increased number of amplitude control bits in the sine-wave generator will help extend the dynamic range to much lower input amplitudes.

4.2 Implementation of Power Detector

4.2.1 Peak Detectors

Figure 67 below shows the peak detector used in the power detector. Its operation was briefly described in Section 2.1.2 but will be expanded on here. The input to the RF peak detector ranges from 2GHz to 4GHz while the input to the reference peak detector ranges from 12.5MHz to 25MHz.

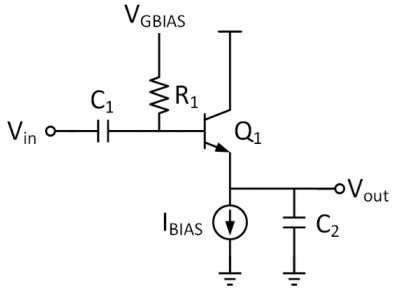

Figure 67. Peak Detector

For large input signals when the base of the transistor is more than a V_{BE} voltage drop above the output voltage, Q_1 turns on and begins to charge the capacitor C_2 so that the output voltage tracks the input voltage. Once the input voltage reaches a peak and begins to fall, however, the transistor Q_1 turns off. At this point, the bias current source, I_{BIAS}, begins to discharge C_2. If the bias current is small and the capacitor, C_2, is large, the rate of this discharge will be slow. As discussed previously, this discharge rate is:

$$\frac{dV_{out}}{dt} = -\frac{I_{BIAS}}{C_2} \tag{41}$$

If the signal has a slope that is significantly higher than this discharge rate, the output voltage will not track the input voltage. Instead, the output voltage will linearly discharge until the signal rises high enough again to activate Q_1 and charge C_2 so that the output voltage rises and tracks the input waveform. Therefore, if the discharge rate is low, the output DC voltage will approximately be linearly related to the input amplitude. This is confirmed in [26] which shows analytically that the output voltage for large input amplitudes is approximately:

$$V_o = V_{amp} - V_T ln\sqrt{\frac{2\pi V_1}{V_T}} \tag{42}$$

This is confirmed in Figure 64 shown previously which shows that the slope of the peak detector's transfer curve is relatively constant for input amplitudes above 300mV. For small amplitudes, however, the slope of the signal begins to approach the discharge rate of the peak detector. Therefore, rather than the constant discharge rate, the output is instead a buffered version of the input signal. At this point, the output DC level remains

relatively constant even as the input amplitude changes. As a result, the gain of the peak detector drops dramatically.

In this design, the capacitor C_2 is chosen to be 500fF while the bias current is chosen to be 100μA. This provides a good tradeoff between the speed of the detector and the gain of the detector at low input amplitudes. With these numbers, the discharge rate of the detector is 200V/μs. The maximum slope of an input sine-wave at 4GHz and an amplitude of 300mV is 7.5V/ns. Therefore, we see that the maximum slope of this sine wave is much larger than the discharge rate of the detector which allows the detector to provide a high input-amplitude to DC output level gain. On the other hand, the maximum slope of an input sine-wave at 4GHz and 50mV is 1250V/μs which is much closer to the discharge rate of the detector. Therefore, the output is able to more accurately track the input signal during the discharge period and the DC output voltage does not change much with changing input amplitude. Therefore, the gain of the peak detector is low near this amplitude.

The AC coupling components C_1 and R_1 are chosen to ensure the pole of the high-pass filter formed by C_1 and R_1 is well below the input frequency of each detector. The transistor Q_1 in each detector is implemented using a silicon-germanium (SiGe) heterojunction bipolar transistor (HBT). These HBTs provide very good high-frequency performance with minimal bias current and parasitic capacitances.

From the above analysis we can conclude that the gain of the peak detector at low input amplitudes can be increased by either decreasing the bias current in the peak detector or increasing the size of the output capacitor. Both of these, however, decrease the speed

of the detector. Since the detector must react quickly for the minimum-duration modulation pulse (10MHz PRF and 5% duty cycle), there is a lower pound on the rise time of the detector. Therefore, the chosen bias current and capacitor size provide a good tradeoff between the speed of the detector and the gain of the detector at low input amplitudes. If slower pulses were used, the gain of the detector could be increased at the expense of the rising speed of the output.

As mentioned previously, the discharging of the output capacitor during the low period of the input leads to some ripple on the output voltage. According to [26], this ripple is approximately:

$$\Delta V_o = -\frac{I_{BIAS}}{C_2} \cdot \frac{1}{f_{in}} \tag{43}$$

Where f_{in} is the input frequency. Therefore, for the chosen values of I_{BIAS} and C_2 at 4GHz, the expected voltage ripple is 50mV. This voltage ripple occurs at a frequency of 4GHz and will be heavily attenuated by the amplifier following the peak detectors and the ADC.

The next step in the design of the peak detectors is determining the proper capacitor size for the reference peak detector which operates at a much lower frequency. Based on the previous discussion, the discharge rate relative to the maximum slope of the signal should be equal for both detectors to ensure they have equal output DC values. We set the bias current in both detectors to be equal to ensure they have the same DC V_{BE} voltage drop. Therefore, since both detectors have sinusoidal waves at their input:

$$\frac{I_{BIAS,RF}}{C_{2,RF}} \cdot \frac{1}{V_{amp} \cdot 2\pi \cdot f_{RF}} = \frac{I_{BIAS,REF}}{C_{2,REF}} \cdot \frac{1}{V_{amp} \cdot 2\pi \cdot f_{REF}} \rightarrow C_{2,REF} = C_{2,RF} \cdot \frac{f_{RF}}{f_{REF}} \tag{44}$$

Since the ratio between f_{RF} and f_{REF} is 160, the capacitor in reference peak detector is chosen to be 80pF.

A final issue in the design of the peak detectors is the random mismatch that will inevitably exist the two peak detectors due to random process variations. Some Monte-Carlo simulations with mismatch have been run to understand the nature of the error that mismatches between the two peak detectors produces. Figure 68 below shows the output from the two peak detectors for one Monte-Carlo iteration with large mismatch. It is interesting to note that one peak detector's output is simply a shifted version of the other peak detector's output.

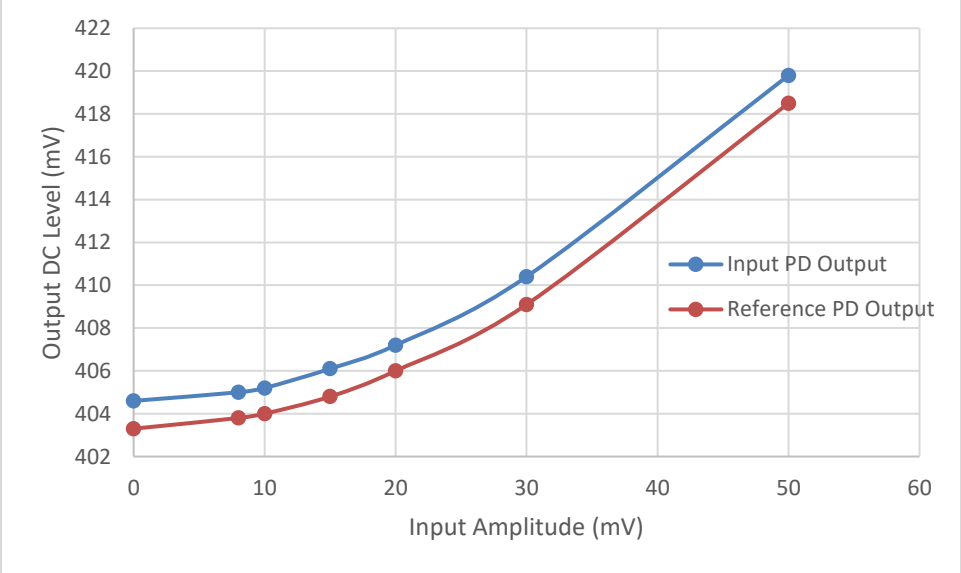

Figure 68. Peak Detector Outputs with Mismatch

This shift in the peak detector output voltage is due to mismatch in the base-emitter voltage of the two HBTs used in the two peak detectors. At low input amplitudes, this offset leads

to very large errors in the detected amplitude since the peak detector gain is low at low input amplitudes. This large error can be seen in Figure 69 below.

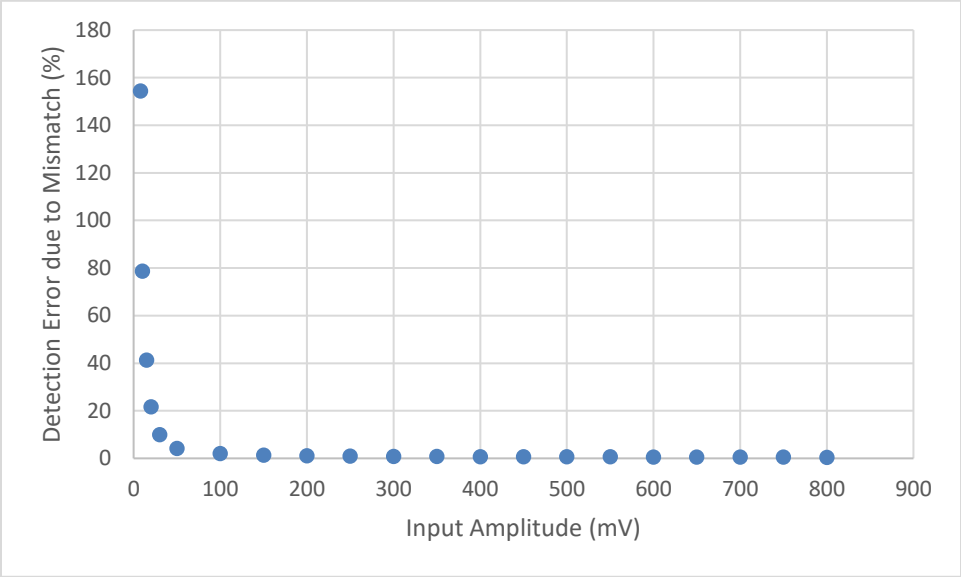

Figure 69. Amplitude Detection Error due to Mismatch

As mentioned during the architecture discussion, the power detector will utilize an offset measurement period to improve the power detection accuracy. During this time, a large transistor connected to ground will short the RF input of the detector, and the reference sine wave generator will be deactivated such that the output amplitude is 0V. Therefore, the output of the peak detectors will be the bias set at the gate of the detectors minus the base-emitter voltage drop. As a result, the mismatch in the base-emitter voltage will be measured during the offset-measurement period and will be subtracted during the final comparison of the two peak detector outputs. Figure 70 below shows the amplitude detection error with the mismatch but with the offset subtracted from the measurement.

The maximum measurement error is now approximately 0.4% which corresponds to a power detection error of approximately 0.035dB. The residual error is due to other mismatches in the detectors besides the base-emitter voltage mismatch but is small enough that it should not greatly affect the accuracy of the detector.

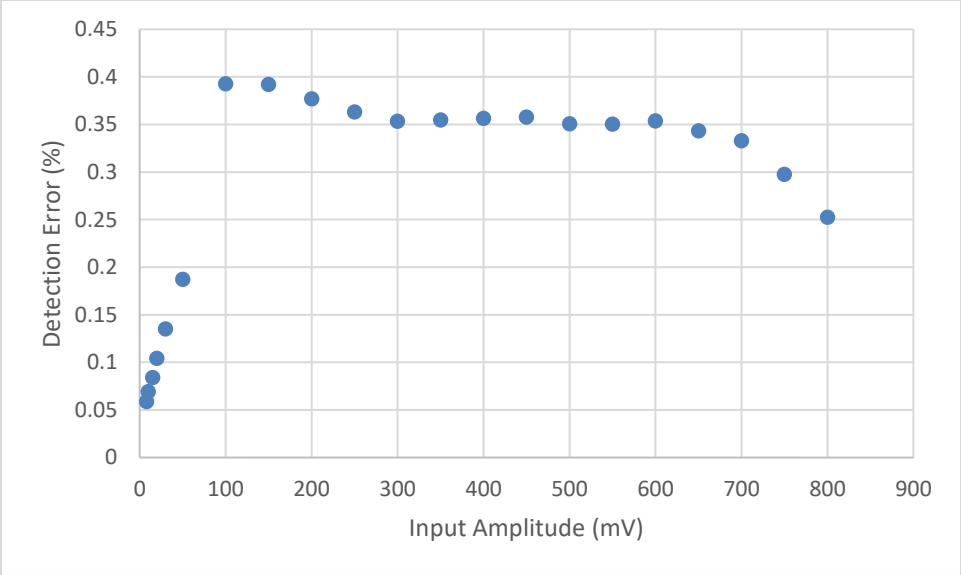

Figure 70. Amplitude Detection Error with Offset Correction

4.2.2 Sine-Wave Generator

As discussed previously, the sine-wave generator must output a 25MHz sine wave with very accurate amplitude. Therefore, a DAC with a high output sample rate but good accuracy is required. Previous current-steering DACs have been reported to provide good accuracy and dynamic performance at high sample rates [27]. Good dynamic performance is achieved by improving the linearity of the DAC as much as possible. In most cases, this is achieved by splitting the DAC up into two segments. The first segment which

implements the least significant bits and is implemented using a binary-weighted current mirror array. Binary weighted DACs, however, experience large differential non-linearity (DNL) at the mid-code transition (when the MSB switches from "0" to "1") because the MSB element must be extremely well-matched to all of the other elements in order to achieve a DNL that is less than 0.5 LSBs. Therefore, the MSBs of the DAC are implemented using a thermometer-coded DAC which greatly reduces the matching requirements for the current-source elements. Figure 71 below shows the overall topology of the DAC. A 14-bit DAC is chosen to ensure the amplitude accuracy error due to the finite LSB size is less than 1% of the minimum amplitude of 8mV that will be detected. The upper 6 bits of the DAC are implemented using 63 identical unit elements while the lower 8 bits of the DA are implemented using binary-weighted units. The input data for the DAC comes from a digital block that generates an adjustable-amplitude digital sine wave based on the amplitude control bits coming from the main digital controller.

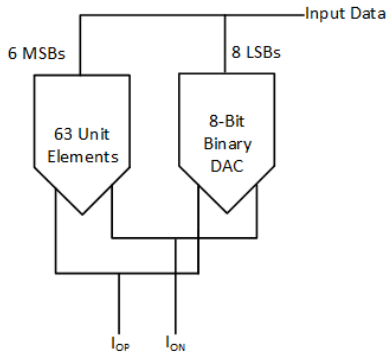

Figure 71. DAC Topology

The elements in the DAC are implemented using the schematic in Figure 72. Each element contains a cascode current source formed by M_1 and M_2 that sets the current for that element. Because matching between the elements is critical to the performance of the DAC, M_1 is a large transistor. Indeed, in order to reduce threshold voltage mismatch between the current sources in the various elements, M_1 should have a large length. We can see this by examining the square-law equation for the NMOS transistor:

$$I_{DS} = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L}(V_{GS} - V_{TH})^2 \rightarrow \frac{dI_{DS}}{dV_{TH}} = \sqrt{2 I_D \mu_n C_{ox} \left(\frac{W}{L}\right)} \tag{45}$$

Therefore, we see that the sensitivity of the current mirror's output current to variations in the threshold voltage can be reduced by increasing the length of the transistor. Additionally, the variation in the threshold voltage is inversely proportional to the square-root of the area of the transistor:

$$\sigma_{V_{TH}} \propto \frac{1}{\sqrt{WL}} \tag{46}$$

Therefore, we see that increasing the length of the transistor also decreases the threshold voltage mismatch. Therefore, M_1 is chosen to have a very long length of M_1. Therefore, M_1 has a fairly large parasitic drain capacitance associated with it. In order to ensure the output impedance of the DAC is high at the sampling frequency (250MS/s), the cascode transistor M_2 is added and is much smaller than M_1. The cascode transistor boosts the impedance at the drain of M_1 which is mainly dominated by the drain capacitance. This helps to improve the dynamic performance of the DAC at high frequencies [28]. Additionally, the cascode transistor also helps to improve matching between the DAC element current sources formed by M_1.

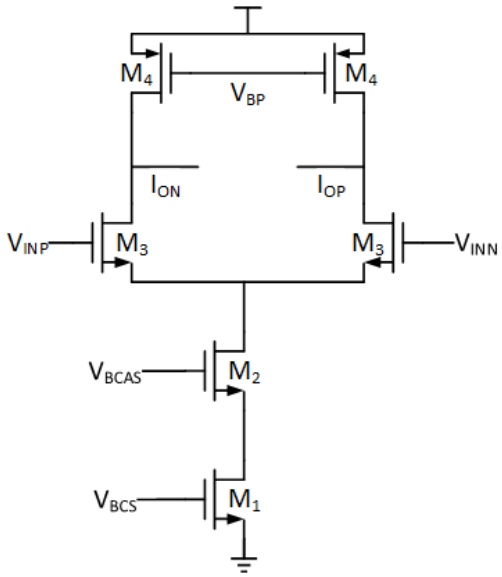

Figure 72. DAC Element

Current is each element is switched to the positive or negative output based on the input data. The switches M_3 are sized to provide a reasonable voltage drop across them when the current from M_1 is flowing through them. This is required to ensure the cascode transistor M_2 remains in saturation. The output of the DAC is connected to a virtual ground at the input of a fully-differential operational amplifier. Therefore, the output voltage is set to 0.9V. In the worst case, the current mirror requires at least 0.5V across it. Therefore, the input transistors are sized to provide a voltage drop of approximately 300mV to ensure sufficient headroom to account for process and temperature variations. The transistors M_4 are biased to provide half-scale current.

In order to achieve the best possible dynamic performance, the switches formed by M_3 should never be off at the same time. This ensures that the current source is always on and does not cause excessive glitching in the output current when it turns on and off.

Therefore, standard CMOS drivers cannot be used to drive the gates of M_3. Therefore, the high-crossing gate driver seen below in Figure 73 is used [29]. This driver switches the output between two voltage levels V_{HIGH} and V_{LOW}. The transistors M_1 and M_2 are sized larger than M_3 and M_4 to ensure the rising transition of the output is faster than the lower transition. This ensures that at least one switching transistor in Figure 72 above is activated at any given time which, in turn, ensures that the drain node of the current source does not discharge during switching transitions.

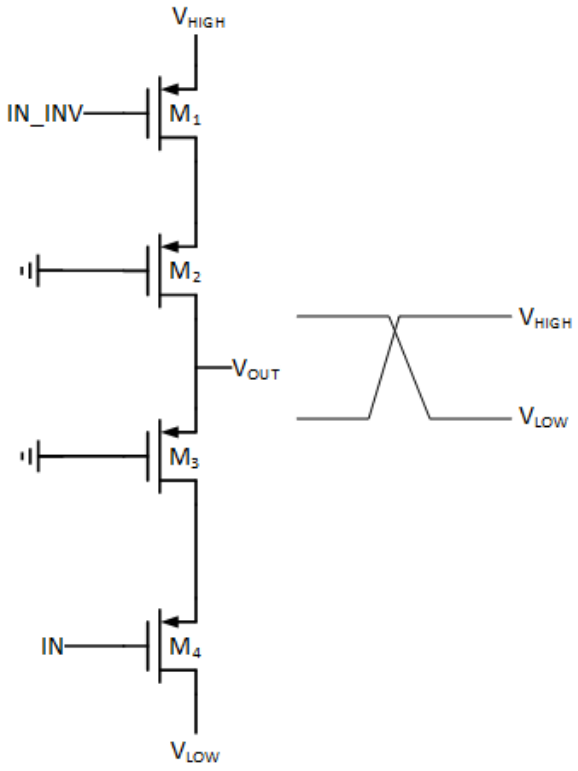

Figure 73. High-Crossing Switch Driver

The bias current for each element is set using a global bias network based on the bandgap voltage reference discussed in the current sensor section. As seen in Figure 74 below, an operational amplifier is used to adjust the gate voltage of M_1 such that the bandgap reference output is placed across a resistor R. This resistor is matched to the resistors used in the amplifier following the DAC that convert the output current of the DAC into a voltage. Therefore, the bias current of the DAC tracks with variations in the absolute resistor values on-chip such that the amplitude should remain relatively constant. The current through M_1 is mirrored to M_2 and is passed through M_3 and M_4 to generate the bias voltages for the DAC elements. The number of fingers in the current source of each element is chosen to provide the desired current. The bandgap utilized in the bias generator is the same bandgap described in the current sensor section and has a maximum error of approximately 0.875%.

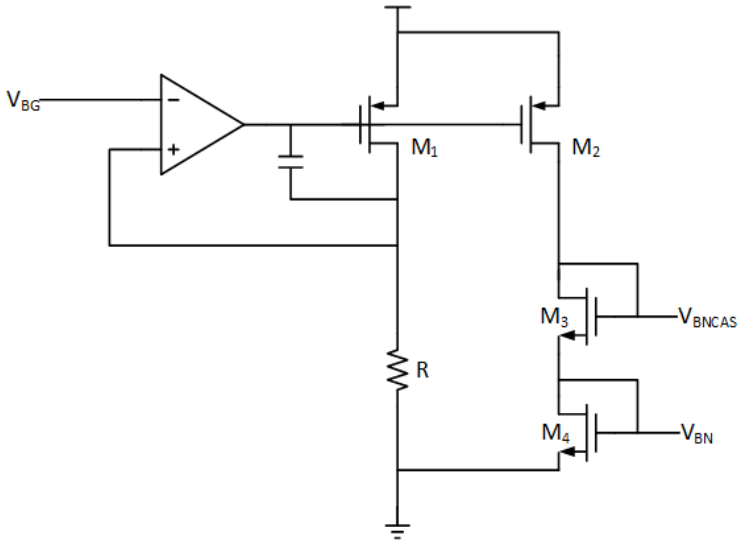

Figure 74. DAC Bias Generator

Figure 75 below shows the DAC's DNL for five Monte-Carlo iterations with mismatch enabled. The maximum DNL is below 0.5LSB which indicates that the dynamic performance of the DAC should be sufficient for this application. Also shown in Figure 76 is the INL of the DAC over the full input code range

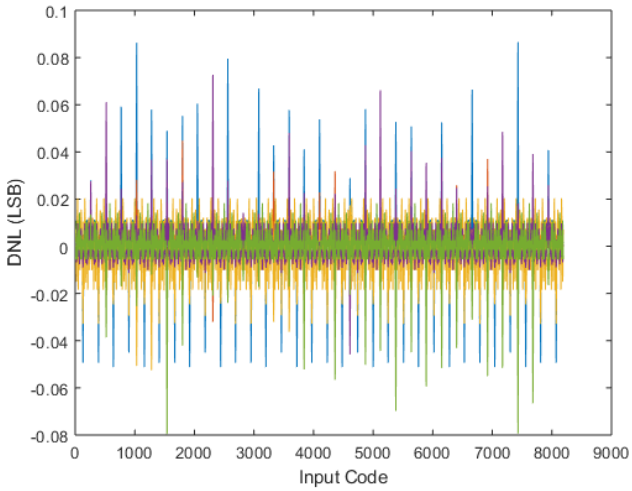

Figure 75. DAC DNL

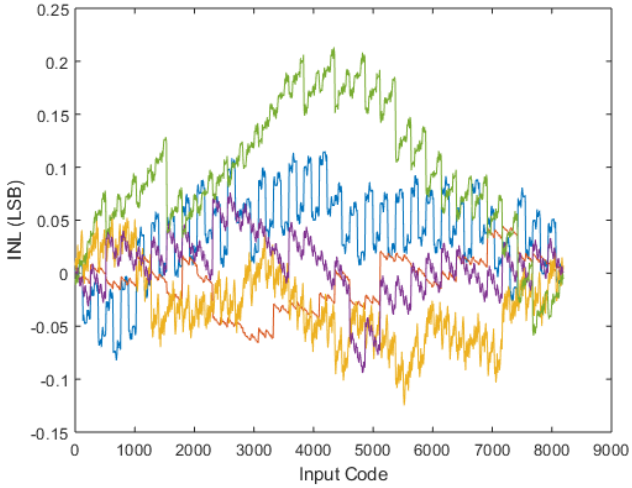

Figure 76. DAC INL

This is confirmed in Figure 77 below which shows a histogram of the DAC's output THD after being converted into a voltage by the filter that follows the DAC. The amplitude at the output of the amplifier is 800mV which is the highest amplitude that will be produced by the sine-wave generator. The worst-case THD is approximately 0.225% which should not greatly affect the accuracy of the detector.

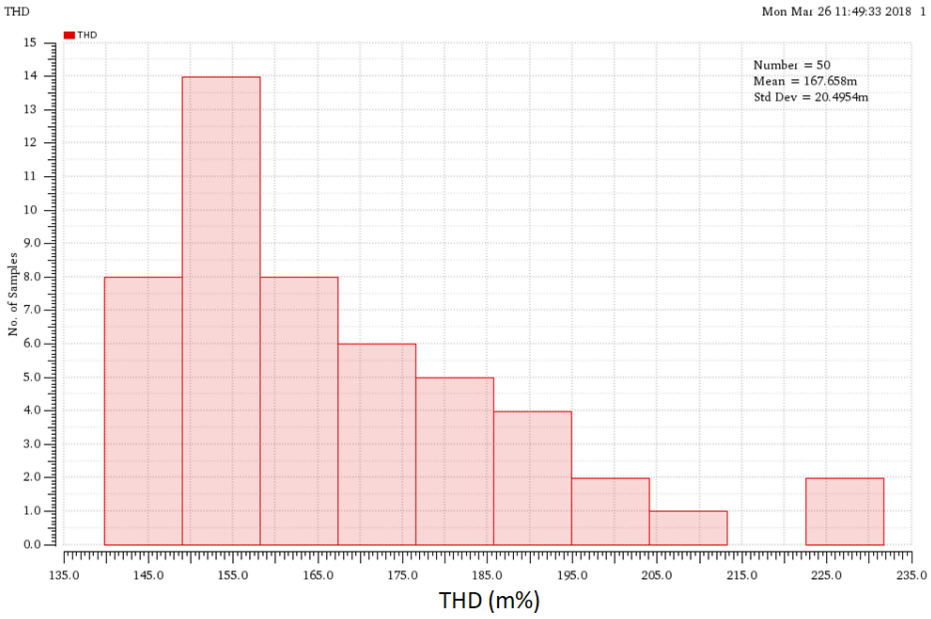

Figure 77. DAC Filter Output THD

Figure 78 below shows a histogram of the output amplitude when the amplitude control is set to 8mV. The variation in the output amplitude is primarily caused by mismatch in the current sources in each element of the DAC. The standard deviation of the amplitude is approximately 21µV which corresponds to a relative 3-σ error of 0.79%.

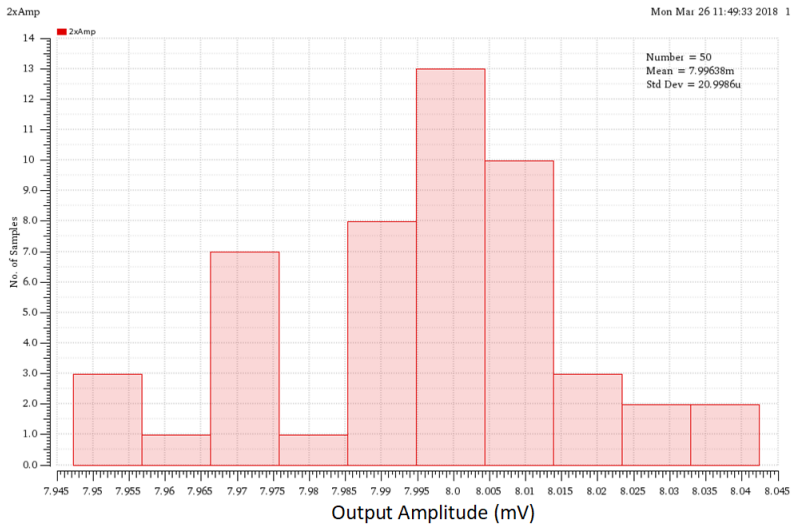

Figure 78. DAC Output Amplitude Variation

Because the current-mode output of the DAC is a 25MHz sine-wave sampled at 250MS/s, there are significant components at 225MHz, 275MHz, 475MHz, 525MHz, and so on. Therefore, a low-pass filter must follow the DAC in order to remove these undesired components. It is also important that the filter have very well-defined gain to ensure that the output amplitude of the sine-wave generator is accurate. The chosen filter topology is shown in Figure 79 below and is based on the multiple-feedback single-amplifier biquad.

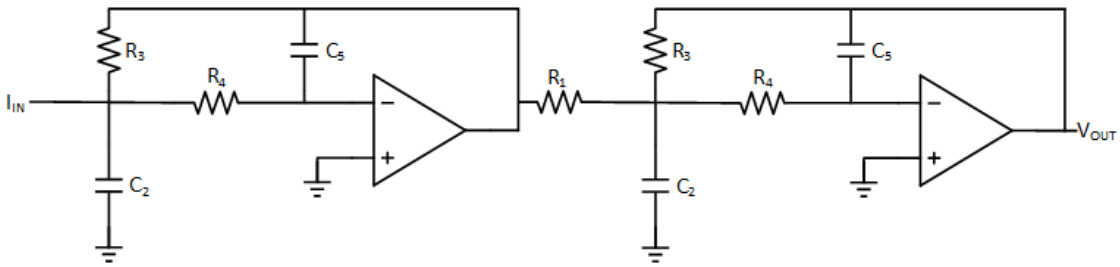

Figure 79. Filter Schematic

The filter is implemented as a fully-differential filter since the current output of the DAC is differential. Each of the filter stages in the figure above implements a second-order filter with natural frequency and Q given by:

$$\omega_o = \sqrt{\frac{1}{R_3 R_4 C_2 C_5}}, Q = \sqrt{\frac{C_2}{C_5} \cdot \frac{G_3 G_4}{(G_1+G_4)^2}}, G = \frac{1}{R} \quad (47)$$

The first stage of the filter also implements a transimpedance amplifier with transimpedance gain given by R_3. The second stage implements a voltage amplifier with DC gain given by R_3/R_1. The transimpedance gain of the first stage is chosen to provide the desired output swing given the maximum output current of 2mA while the voltage gain of the second stage is chosen to be unity. The resistors in the second stage are set to 500Ω. Therefore, C_2 is set to be four times higher than C_5 to provide a Q of 1. The capacitor values are chosen to provide the desired natural frequency of 42.5MHz. Therefore, C_5 is nominally set to 3.75pF while C_2 is nominally set to 15pF.

The amplifier used in the filter is shown in Figure 82 below and is based on the design in [30]. The operational amplifier is a two-stage feedforward-compensated amplifier. The first stage is a cascoded differential pair loaded with a cascoded active load. This stage is self-biased by the common-mode resistors to provide a stable common-mode output voltage. The second stage is composed of two pseudo-differential pairs driven by the input voltage and the output voltage from the first stage. Therefore, the feedforward compensation is implemented by transistors M_6. The bias voltage of M_6 is set separately from the input common-mode voltage using an AC-coupling network. The second stage utilizes an active common-mode feedback with a simple single-stage amplifier along with transistors M_8 to set the output common-mode voltage to V_{CM} which is set to 900mV. The

worst-case GBW at slow corners is approximately 500MHz with a phase margin of 55 degrees when loaded with the capacitors from the filter. The DC gain of the amplifier is approximately 60dB and the power consumption is 6.3mW. A large power consumption is required to provide the desired GBW of at least 500MHz while also ensuring a good phase margin. A relatively high GBW is required to ensure GBW variations with process and temperature do not affect the quality factor of the filter. This would, in turn, affect the gain accuracy of the filter. Additionally, the distortion of the amplifier is reduced by the loop gain of each stage at the input frequency of 25MHz. Therefore, the filters should have some gain at this frequency to ensure the distortion in the output is low.

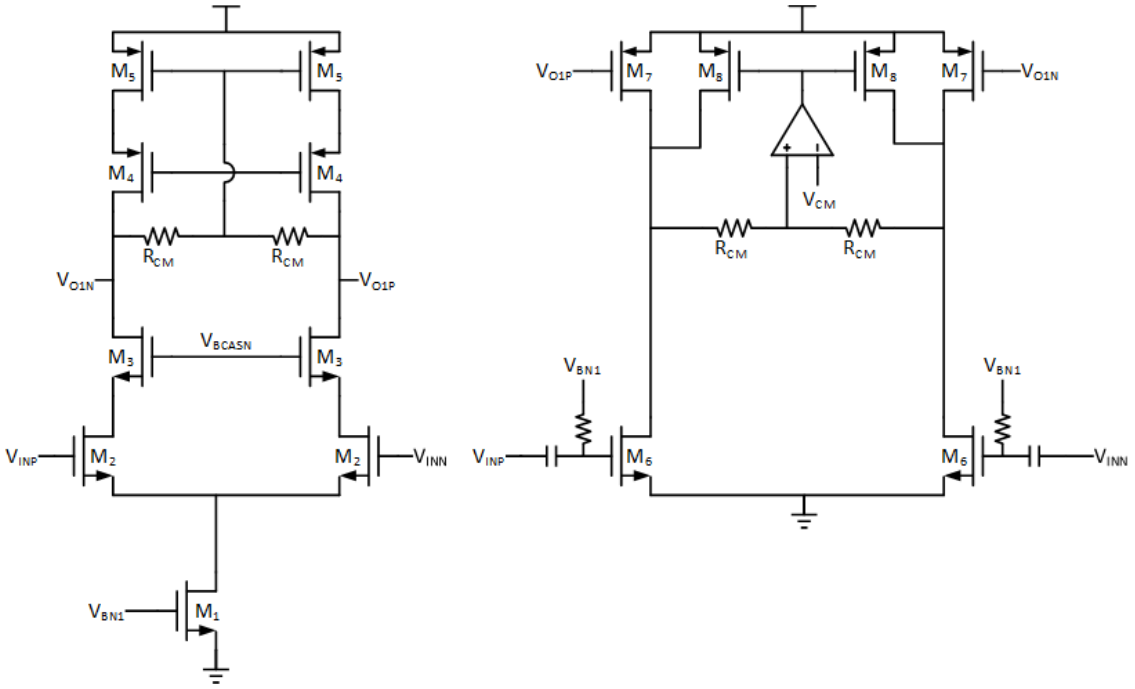

Figure 80. Filter Op-amp

Due to the peak detector's single-ended input, the differential output of the filter must be converted into a single-ended output. This is accomplished using the single-output, differential-input amplifier shown in Figure 83 below. The resistors for the inverting input are twice as large to match the input impedance of the two inputs. Because the maximum output amplitude from the filter is 800mV (which corresponds to a 1.6V peak-to-peak signal) and the supply voltage is 1.8V, the operation amplifier in Figure 83 will need to be able to handle rail-to-rail output swings.

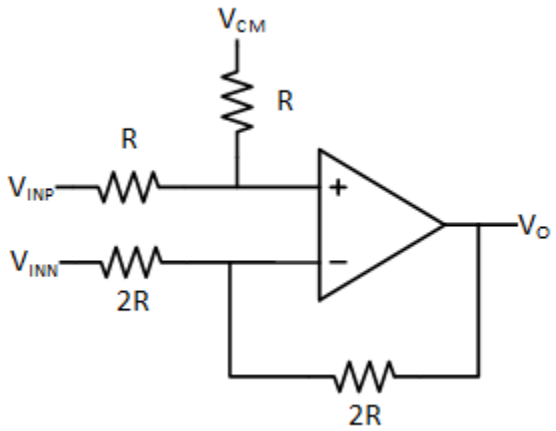

Figure 81. Differential to Single-Ended Converter

The operational amplifier is implemented using the schematic in figure 84 below. The first stage of the op-amp is implemented using a folded cascode stage. The folded section of the cascode has a floating current source that is used to bias the rail-to-rail output stage formed by M_7 and M_8. Ahuja compensation is used to compensate the amplifier and ensure it is stable for the desired load. This operational amplifier provides a high DC gain of 72dB with a gain-bandwidth product of 600MHz in the worst case. The phase margin

of the op-amp is 45 degrees and it consumes a power of 5.4mW due to the power-hungry class-AB output stage. The amplifier is able to output the 1.6V peak-to-peak signal required at the maximum output amplitude.

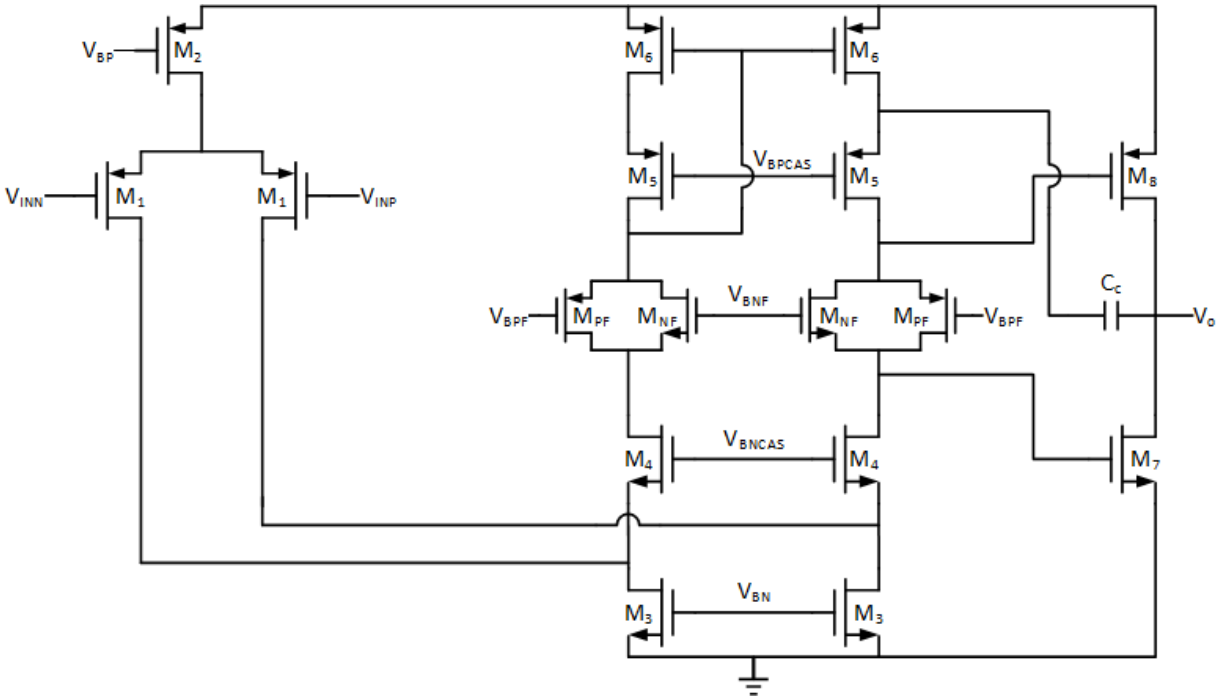

Figure 82. Rail-to-Rail Operational Amplifier

Some Monte-Carlo simulations were run on the filter tuning loop to measure the amount of gain error expected at the output of the filter. The results are shown in Figure 85 below. The maximum gain error when compared to the nominal case for all 50 Monte Carlo iterations is approximately 0.95%. This error can be improved through a number of methods. One is to decrease the unit capacitor size in the variable capacitors. This will, however, increase the number of unit capacitors required and will increase the complexity of variable capacitors. Another option is to improve the GBW of the op-amps used in the

filter. This will, however, increase the power consumption as well. Between the filter's gain error, the bandgap error, and the error due to mismatch in the DAC, the filter has a maximum expected error of 2.6%. This error leaves sufficient headroom for other sources of error such as error in the peak detector output and quantization error in the sigma-delta ADC.

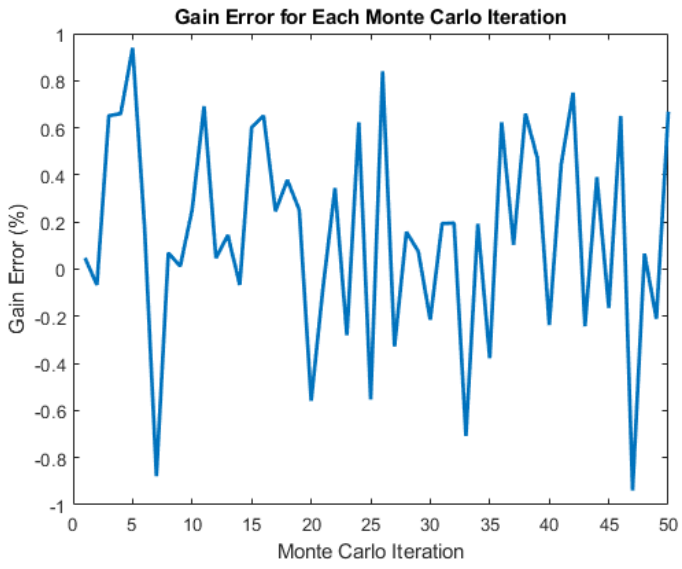

Figure 83. Filter Tuning Results

4.2.3 Amplifier

The purpose of the amplifier in the power detector loop is to provide a large gain at low input amplitudes to ensure the quantization error in the ADC does not cause excessive errors. Suppose, for example, the ADC can measure a voltage range of 700mV and samples the output of the amplifier for 20μs at a sampling rate of 500MS/s. Since the

ADC in this power detector is identical to the ADC used in the current sensor, the ADC's quantization error is a maximum of:

$$\epsilon < \frac{800mV}{500MHz \cdot 20\mu s} = 80\mu V \tag{48}$$

At the lowest input amplitude of 8mV the gain of the peak detector is approximately 0.1V/V. Therefore, if the gain of the amplifier is unity, the ADC quantization error will lead to an amplitude error of 800µV. This corresponds to an error of 10% or 0.83dB. Therefore, even with a relatively long sampling time the quantization error of the ADC leads to large detection errors. If, however, the gain of the amplifier is larger than unity the ADC quantization error will be divided by the amplifier gain and the peak detector gain when referring to the input amplitude. If the amplifier provides a gain of 20V/V, the quantization error mentioned above will lead to an error of only 0.04dB which is below the maximum detection error.

The amplifier should not load the output of the peak detector and must therefore have a high-impedance input interface. While the amplifier is required to provide high gain at lower input amplitudes, it should also be able to decrease this gain at higher input amplitudes to ensure the input of the ADC is within the range it can properly digitize. Therefore, the gain of the buffer should also be coarsely programmable. Indeed, simulations show that input amplitudes below 30mV can benefit greatly from the gain discussed above, but the gain can be unity above this amplitude. The top-level amplifier schematic is shown in Figure 86 below. This amplifier is based on the instrumentation amplifier and contains two non-inverting amplifiers at the input that present a high impedance input interface. The outputs of these non-inverting amplifiers go to a fully

differential amplifier that provides further gain as well as a full differential output that can interface with the ADC. The gain of the non-inverting input amplifiers is 5V/V which provides values of 25kΩ and 12.5kΩ for R_2 and R_1, respectively. The gain of the fully differential amplifier is 4V/V which provides values of 80kΩ and 20kΩ for R_4 and R_3, respectively. Therefore, the total gain of the amplifier with the switches open is 20V/V. R_5 is chosen to provide unity gain when the switches are closed. Therefore, its value is 26.67kΩ. When the switches are closed, the gain of the overall amplifier is ideally unity.

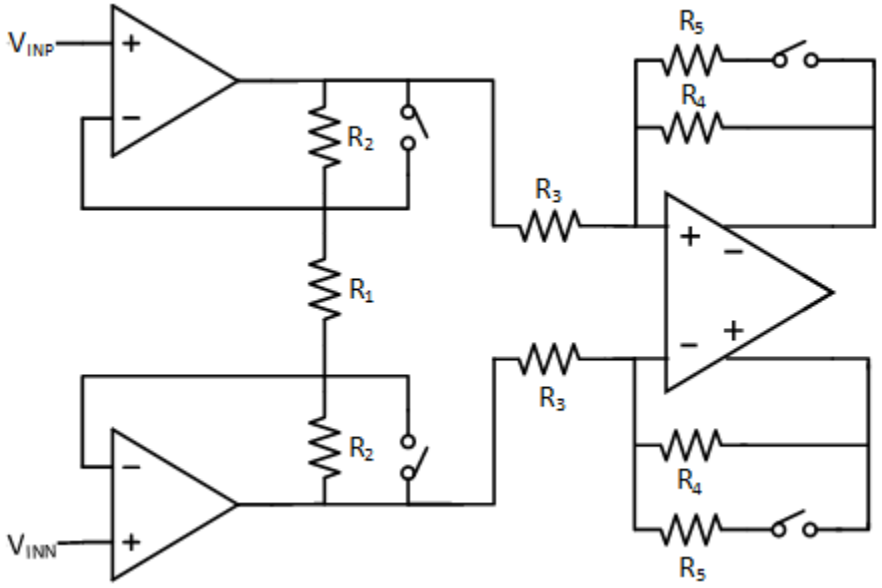

Figure 84. Amplifier with Gain Control Switches

The switches in Figure 86 above are implemented using CMOS transmission gate switches and provide low series resistance and distortion. Figure 87 below shows the output voltage of the buffer with the high gain activated for a DC input voltage ranging from -500mV to 500mV. At low differential input voltages, the output provides a linear

output response. At input voltages above 40mV, however, the output begins to saturate and the gain of the buffer drops. This is shown more clearly in the plot of the gain of the amplifier shown in Figure 88. The output DC voltage of the peak detector for a 30mV input amplitude is approximately 6mV. With the added input-referred offset of the amplifier (which is a maximum of 7mV) as well as typical peak detector offset voltages (which are a maximum of 5mV), the maximum input signal with a 30mV input amplitude is well below the 40mV where saturation begins. Also shown in both figures are the output voltage and gain for the same input range but with the low-gain mode activated. The amplifier provides stable gain across the full input range when the switches are activated.

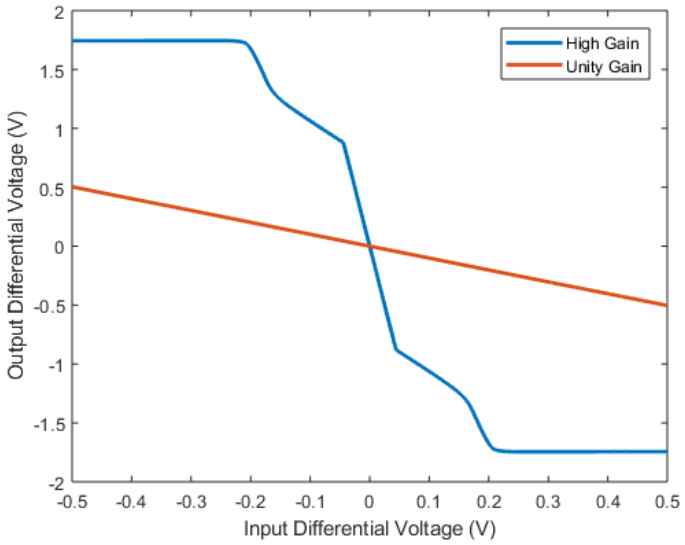

Figure 85. Output Voltage for Instrumentation Amplifier

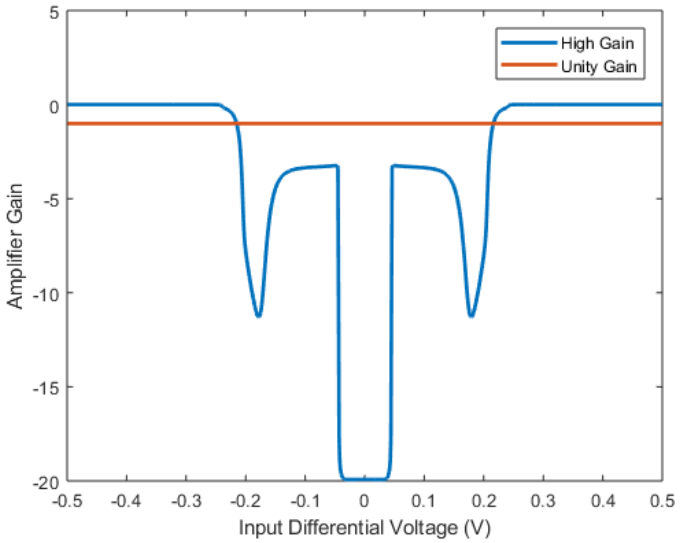

Figure 86. Gain for Instrumentation Amplifier

4.2.4 ADC

As mentioned previously, the ADC in the power detector will be the same ADC used previously in the current sensor. Therefore, the primary design challenge for the ADC in the power detector is determining the minimum sample time required to ensure the detection error due to quantization noise in the ADC is sufficiently low. In this design, the ADC sample time is chosen to provide a maximum error of 0.5% due to quantization error. The worst-case point is at the lowest input amplitude of 8mV where the sensitivity of the detector is approximately 0.1V/V. Therefore, the minimum sampling time can be calculated as:

$$T_{samp} > \frac{800mV}{8mV} \cdot \frac{1}{0.1 \cdot 500MHz \cdot 0.005} \cdot \frac{1}{10} = 40\mu s \tag{49}$$

Therefore, a sampling time of 20µs is used for all input amplitudes. Since the detector requires 14 comparisons to completely resolve all bits of the detected amplitude, the total

measurement time should be around 300μs. This leaves plenty of time in the 1ms measurement window for other tasks such as measuring the offset and tuning the filter.

4.2.6 Digital Controller

The purpose of the digital controller is to collect the output bits from the ADC and adjust the amplitude control bits for the sine-wave generator according to the method described in the description of the power detector's architecture. After all 14 amplitude control bits are resolved, the digital controller also sets an end of cycle signal, so the amplitude can be read out and converted into a power. The digital controller also sets the gain control bit for the amplifier based on the current amplitude control value. This controller was implemented using a synthesized Verilog description and was auto placed and routed.

4.2.5 Top-Level Simulations

Figure 89 below shows the distribution of error in the detection of the amplitude in the power detector. We expect that the sine-wave generator will contribute 2.6% error in the worst case which represents a significant portion of the total error allowance. Mismatch between the peak detector responses at 25MHz and 4GHz are assumed to contribute a maximum of 1% error and, as discussed previously, the quantization error of the ADC should only contribute 0.5% error at the lower input amplitudes. This leaves plenty of room for error due to noise which is assumed to be approximately 1% based on the sensitivity of the peak detectors at the minimum input amplitude and noise simulations of the amplifier. Therefore, a total maximum amplitude detection error of around 5.1% is expected which corresponds to a 0.432dB power detection error.

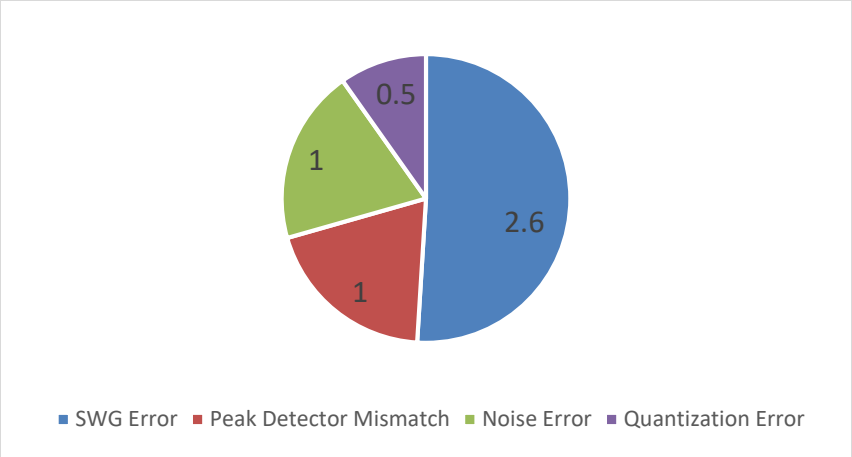

Figure 87. Error Distribution in Percent of Power Detector

Some top-level simulations of the power detector at transistor level were run. The input frequency during these simulations is 4GHz and the input amplitude is varied over a 40dB range from 8mV to 800mV. The plot of the power measurement error for three corners is shown in Figure 90 below. The three corners are the nominal corner, a slow corner, and a fast corner. The error is fairly constant across the full input range for each corner but does increase slightly at low input amplitudes for the slow corner and the nominal corner. This is due to the quantization error and noise error causing larger measurement errors at lower input amplitudes where the peak detector gain is lower. The error curves seem to shift when moving between corners. This is because the sine-wave generator output amplitude, which depends on the bandgap voltage used in the bias generator, is multiplied by a particular percent error when shifting between corners. Essentially, since the bandgap's output voltage shifts by a certain percent due to process variations, the output amplitude of the sine-wave generator will shift by that same percent and will cause a shift in the measurement error.

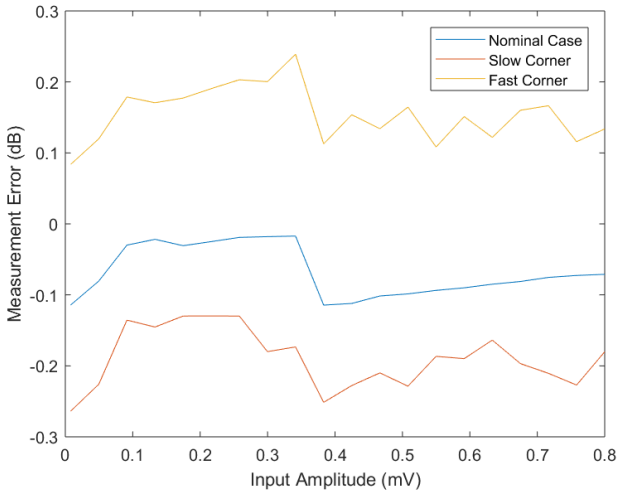

Figure 88. Top-Level Simulation Error Results

4.3 Power Detector Measurements

Because the power detector presented in Section 4.2 is not yet fabricated, measurement results for the previous power detector discussed in Section 4.1 are presented. The PCB used to test the power detector is shown in Figure 91 below. A pulse-modulated RF input signal is generated by a high-frequency vector signal generator and the modulated RF signal as well as the modulating envelope signal are routed to the PCB through SMA cables. A 200MHz clock is also generated by a function generator and is used by the on-chip sine-wave generator. Several bias voltages and bias currents are set using potentiometers on the board. The digital output of the power detector is read using a logic analyzer.

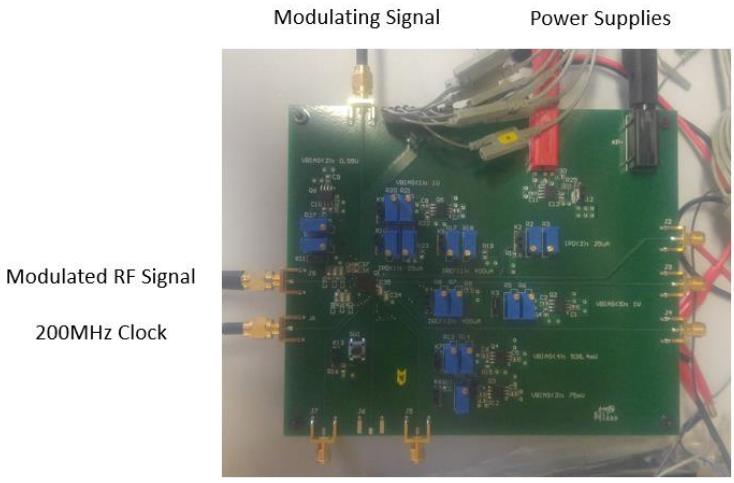

Figure 89. Power Detector Test PCB

The input signal amplitude is varied from 28.1mV (which corresponds to an input power of -15dBm) to 1.122V (which corresponds to an input power of -15dBm) at a PRF of 1MHz, a carrier frequency of 4GHz, and a duty cycle of 50%. Note that this input signal amplitude is effectively divided by 2 at the input of the power detector due to the 50Ω output impedance of the signal generator and the 50Ω input impedance of the power detector. Figure 92 below shows the measured amplitude at the output of the power detector plotted against the input amplitude. The measured amplitude tracks well with the ideal amplitude over much of the range but begins to deviate from the ideal amplitude as the input amplitude rises above the full-scale range the detector is capable of processing.

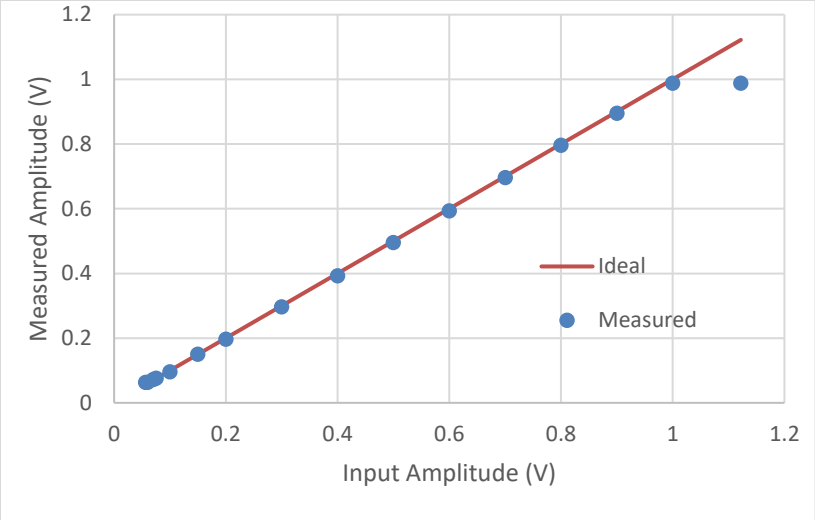

Figure 90. Measured Amplitude from Power Detector

The error of the detector is more easily visualized by converting the amplitude error into an equivalent power error in dB. Figure 93 below shows the power measurement error in dB plotted against the input power in dBm. The input power covers a 26dB range and the maximum measurement error over this range is 1dB. A maximum measurement error of 0.5dB is achieved over a range of approximately 24dB. These measurements are made at an input frequency of 4GHz and a PRF of 10MHz.

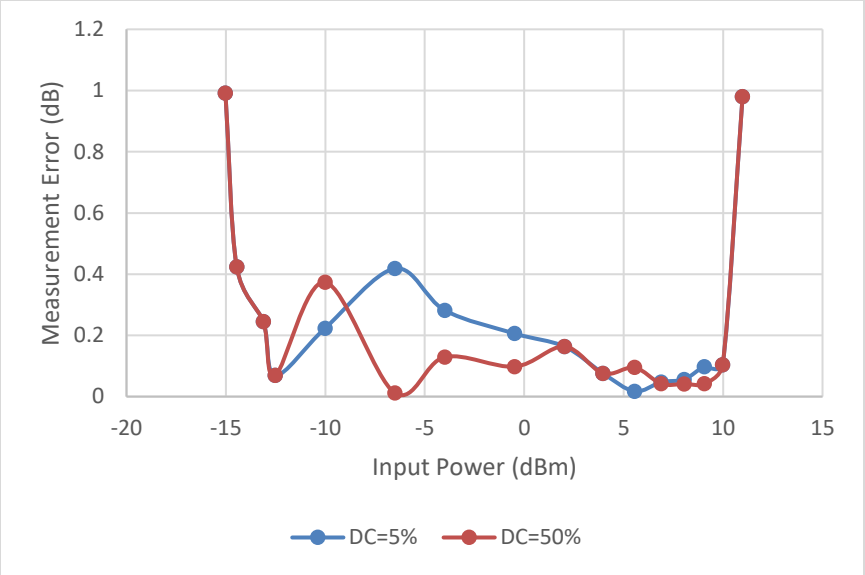

Figure 91. Measurement Error for F=4GHz, PRF=10MHz

Figure 94 below shows the measurement error for various carrier frequencies. The detector has the same dynamic range and error as discussed above.

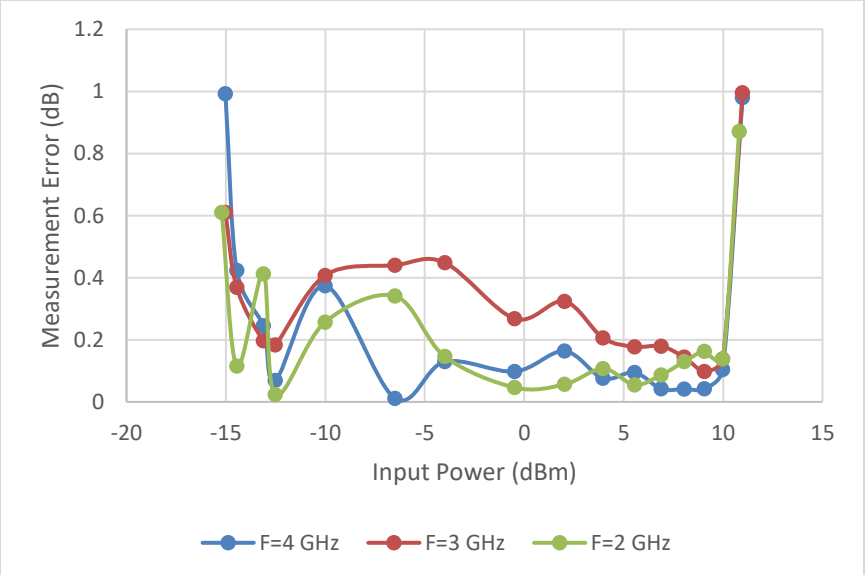

Figure 92. Measurement Error for PRF=1MHz, DC=50%

Lastly, Figure 95 below shows the measurement error for various PRFs. The results are similar to those seen in Figures 94 and 93 above.

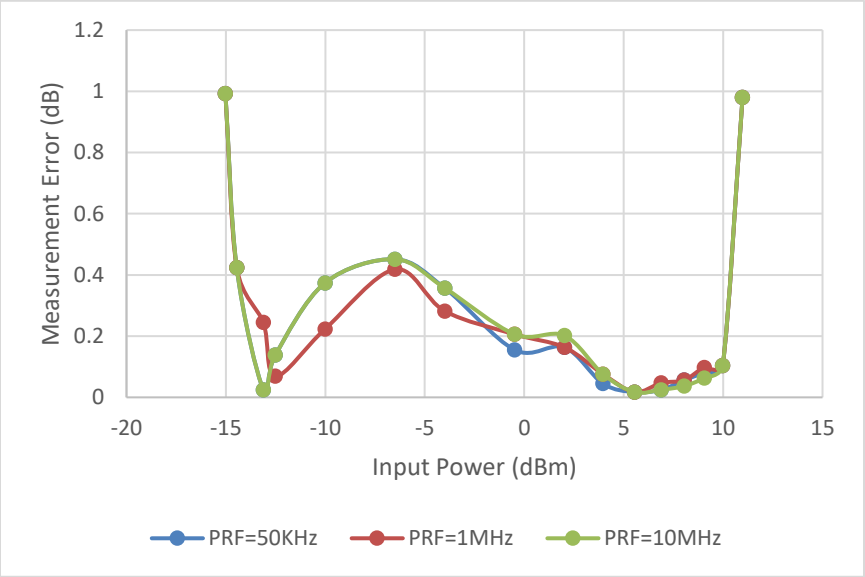

Figure 93. Measurement Error for F=4GHz, DC=5%

5. SUMARY AND CONCLUSIONS

Power amplifiers are ubiquitous in today's society and yet often operate in sub-optimal conditions. Indeed, these amplifiers often require careful adjustment of operating points in order to achieve optimum efficiency and reliability. In order to properly adjust these operating points on-the-fly during the operation of the transmitter, several parameters such as the input power, output power, and bias current of the power amplifier must be measured. This thesis has proposed two designs that seek to measure these parameters with the precision required to accurately optimize the power-added efficiency and reliability of a power amplifier.

The first design introduced was a DC bias current sensor which is required to calculate the DC power consumption of the power amplifier. The main contribution of this current sensor is the introduction of a reference current calibration measurement that allows the current sensor to measure the resistance of the sense resistor. This allows the current sensor to utilize a sense resistor that changes greatly with temperature without introducing excessive current sensing errors. In this thesis, a PCB trace is used as the sense resistor. Therefore, the current sensor described in this thesis can be used in a wide variety of situations a DC current must be sensed and a PCB trace of reasonable resistance (>10mΩ) is available.

The second design introduced was a power detector operating at 2-4GHz which is required to measure the input and output power of the power amplifier. The main contribution of the previous power detector is that it provides an absolute power measurement. Therefore, excessive calibration of the baseband circuitry that utilizes the

power detector's output is not required. The main contribution of the power detector presented in this thesis is the extension of the input dynamic range over which a maximum 0.5dB error can be achieved to 40dB with a single segment. This range can be further increased by using accurate amplifiers or attenuators to create multiple segments which is done in many other power detectors to achieve wide dynamic range. This wide dynamic range allows the power detector to be used in systems with much wider input and output power ranges or it can be used in multi-standard systems where the output power can change greatly from standard to standard.

Further work on this power amplifier control system will involve designing the computational engine that will take the current sensor and power detector outputs and combine them to calculate and optimize the efficiency of a power amplifier.

REFERENCES

[1] D. Talbot. (2012, May 30). *Efficiency Breakthrough Promises Smartphones that Use Half the Power*. Available: https://www.technologyreview.com/s/506491/efficiency-breakthrough-promises-smartphones-that-use-half-the-power/

[2] M. Integrated. (2005, May 30). *RF Power Reduction for CDMA/WCDMA Cellular Phones*. Available: https://www.maximintegrated.com/en/app-notes/index.mvp/id/3434

[3] C. T. Rodenbeck *et al.*, "Design of Robust On-Chip Drain Modulators for Monolithic Pulsed Power Amplifiers," *IEEE Microwave and Wireless Components Letters*, vol. 23, no. 5, pp. 267-269, 2013.

[4] O. Axelsson, M. Thorsell, K. Andersson, and N. Rorsman, "The Effect of Forward Gate Bias Stress on the Noise Performance of Mesa Isolated GaN HEMTs," *IEEE Transactions on Device and Materials Reliability*, vol. 15, no. 1, pp. 40-46, 2015.

[5] 3GPP, "LTE; Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception, 2016,"

[6] Y. Zhou and M. Y. W. Chia, "A Low-Power Ultra-Wideband CMOS True RMS Power Detector," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 5, pp. 1052-1058, 2008.

[7] Y. Qizhang, W. R. Eisenstadt, R. M. Fox, and Z. Tao, "A translinear RMS detector for embedded test of RF ICs," *IEEE Transactions on Instrumentation and Measurement,* vol. 54, no. 5, pp. 1708-1714, 2005.

[8] J. Choi *et al.*, "Wide Dynamic-Range CMOS RMS Power Detector," *IEEE Transactions on Microwave Theory and Techniques,* vol. 64, no. 3, pp. 868-880, 2016.

[9] A. Technologies, "Fundamentals of RF and Microwave Power Measurements,"

[10] J. Mulder, W. A. Serdijn, A. C. Van Der Woerd, and A. H. Van Roermund, "Dynamic translinear circuits—An overview," in *Research perspectives on dynamic translinear and log-domain circuits*: Springer, 2000, pp. 5-20.

[11] T. Zhang, W. R. Eisenstadt, R. M. Fox, and Q. Yin, "Bipolar Microwave RMS Power Detectors," *IEEE Journal of Solid-State Circuits,* vol. 41, no. 9, pp. 2188-2192, 2006.

[12] Z. Tao, W. R. Eisenstadt, and R. M. Fox, "A novel 5GHz RF power detector," in *2004 IEEE International Symposium on Circuits and Systems (IEEE Cat. No.04CH37512)*, 2004, vol. 1, pp. I-897-900 Vol.1.

[13] J. Zhou, J. Klaren, and C. J. Persico, "Integrated power detector with temperature compensation," ed: Google Patents, 2003.

[14] B. Kobayashi, L. Zhang, M.-C. F. Chang, and P.-M. D. Chow, "Integrated power detector with temperature compensation for fully-closed loop control," ed: Google Patents, 2010.

[15] G. A. Kurtzman and S. P. Hoggarth, "Wide linear range peak detector," ed: Google Patents, 2008.

[16] M. Integrated. (2007, June 1). *MAX2204 RF Power Detector*.

[17] D. FitzPatrick. (2013, June 2). *RF and Microwave Amplifier Power Added Efficiency, Fact and Fiction*. Available: http://www.microwavejournal.com/ext/resources/Webinars/2013a/SLIDES_RFMWamp_6nov13.pdf

[18] L. Xu, J. H. Huijsing, and K. A. A. Makinwa, "A +/-4A high-side current sensor with 25V input CM range and 0.9% gain error from -40C to 85C using an analog temperature compensation technique," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 324-326.

[19] S. H. Shalmany, D. Draxelmayr, and K. A. A. Makinwa, "A 36-A Integrated Current-Sensing System With a 0.3% Gain Error and a 400-uA Offset From -55C to +85C," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 4, pp. 1034-1043, 2017.

[20] Y. Zhou, Y. Zheng, and K. N. Leung, "Fast-response full-wave inductor current sensor for 10 MHz buck converter," *Electronics Letters*, vol. 54, no. 6, pp. 379-381, 2018.

[21] E. Martí-Arbona, D. Mandal, B. Bakkaloglu, and S. Kiaei, "A High-Voltage-Compliant Current-to-Digital Sensor for DC-DC Converters in Standard CMOS Technology," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2180-2188, 2017.

[22] S. C. Huang, M. Ismail, and S. R. Zarabadi, "A wide range differential difference amplifier: a basic block for analog signal processing in MOS technology," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 40, no. 5, pp. 289-301, 1993.

[23] J. Markus, P. Deval, V. Quiquempoix, J. Silva, and G. C. Temes, "Incremental Delta-Sigma Structures for DC Measurement: an Overview," in *IEEE Custom Integrated Circuits Conference 2006*, 2006, pp. 41-48.

[24] J. Kim, B. S. Leibowitz, J. Ren, and C. J. Madden, "Simulation and Analysis of Random Decision Errors in Clocked Comparators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 8, pp. 1844-1857, 2009.

[25] G. Ge, C. Zhang, G. Hoogzaad, and K. A. A. Makinwa, "A Single-Trim CMOS Bandgap Reference With a 3σ Innacruacy of +/-0.15% From -40C to 125C," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 11, pp. 2693-2701, 2011.

[26] R. G. Meyer, "Low-power monolithic RF peak detector analysis," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 1, pp. 65-67, 1995.

[27] D. A. Mercer, "Low-Power Approaches to High-Speed Current-Steering Digital-to-Analog Converters in 0.18um CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 8, pp. 1688-1698, 2007.

[28] C. H. Lin *et al.*, "A 12 bit 2.9 GS/s DAC With IM3 < -60 dBc Beyond 1 GHz in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3285-3293, 2009.

[29] K. Falakshahi, C. K. K. Yang, and B. A. Wooley, "A 14-bit, 10-Msamples/s D/A converter using multibit ΣΔ modulation," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 607-615, 1999.

[30] C. Briseno-Vidrios, A. Edward, A. Shafik, S. Palermo, and J. Silva-Martinez, "A 75-MHz Continuous-Time Sigma-Delta Modulator Employing a Broadband Low-Power Highly Efficient Common-Gate Summing Stage," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 3, pp. 657-668, 2017.