

A HIGH FREQUENCY MULTILEVEL BOOST POWER FACTOR CORRECTION  
APPROACH WITH GaN SEMICONDUCTORS

A Thesis

by

KEVIN CALLAHAN HODGE

Submitted to the Office of Graduate and Professional Studies of  
Texas A&M University  
in partial fulfillment of the requirements for the degree of

MASTER OF SCIENCE

Chair of Committee,	Prasad Enjeti
Committee Members,	Hamid Toliyat
	Scott Miller
	Harry Hogan
Head of Department,	Miroslav M. Begovic

May 2020

Major Subject: Electrical Engineering

Copyright 2020 Kevin Callahan Hodge

## ABSTRACT

This work details a generalized multilevel power factor correction approach that utilizes low voltage GaN semiconductors, reduces inductor voltage, increases inductor current ripple frequency, and reduces capacitor voltage ratings to achieve a high power density and high efficiency design. The multilevel topology is fully modular and can be scaled to higher voltage levels while utilizing low voltage switching devices and capacitors, which can improve power density and efficiency. The topology also reduces the voltage stress across the input inductor to a fraction of the output voltage using fractional voltage levels and multiplies the effective inductor current ripple frequency compared to the traditional boost power factor correction circuit. These improvements allow a drastic reduction in the size of the input inductor. A review of GaN devices and recent advances in power factor correction topology design is conducted. The operating zones of the topology are described in detail as well as the switching states of the topology. A feedback controller design guide is presented for continuous conduction mode boost power factor correction. The switching control is designed for a topology with any number of levels and the multiplication of the inductor current ripple frequency is explained. Simulation results are presented to confirm the controller design and response under various loading conditions and source variations. A detailed design example describes the derivation of design equations for passive components and a guide for selecting appropriate high frequency passive components and designing capacitance and inductance values. Finally, hardware results are presented and future work concerning the topology is discussed.

## DEDICATION

This thesis is dedicated to my parents, Mickiel and Danielle, and my brothers, Logan and Gregory, who supported me throughout my educational career and to my fiancé, Julia, whose encouragement and support helped me reach this goal.

## ACKNOWLEDGEMENTS

I would like to thank my research advisor and committee chair, Dr. Prasad Enjeti, for his guidance throughout the last three years to bring this thesis to fruition. I would like to thank my committee members, Dr. Hamid Toliyat, Dr. Scott Miller, and Dr. Harry Hogan each for their individual contributions to my educational experience and for their help throughout this process.

I would also like to thank all of my lab mates, but especially Erick Pool and Fahad Alhuwaishel, who continually offered encouragement and always challenged me to think harder and expand my knowledge of power electronics and Sinan Al-Obaidi, who helped me build my fundamental understanding of Power Electronics when I first joined the Power Quality Lab.

Finally, I would like to again thank my family and my fiancé for their continuing love and support in everything that I do.

## CONTRIBUTORS AND FUNDING SOURCES

### **Contributors**

This work was supervised by a thesis committee consisting of my advisor, Professor Prasad Enjeti, Professor Hamid Toliyat, and Professor Scott Miller of the Department of Electrical and Computer Engineering and Professor Harry Hogan of the Department of Mechanical Engineering.

Figure 5 was created by Stephen L. Colino and Robert A. Beach of Efficient Power Conversion (EPC) [1]. Table 1 was created by Qingyun Huang and Alex Q. Huang of the University of Texas [2].

All other work conducted for the thesis was completed by the student independently.

### **Funding Sources**

Graduate study was supported by a fellowship from Texas A&M University.

## NOMENCLATURE

DC	Direct Current
AC	Alternating Current
GaN	Gallium Nitride
Si	Silicon
SiC	Silicon Carbide
WBG	Wide Bandgap
PFC	Power Factor Correction
PI	Proportional Integral
EMI	Electromagnetic Interference
THD	Total Harmonic Distortion
DPF	Displacement Power Factor
DTF	Distortion Power Factor
FFT	Fast Fourier Transform
RMS	Root-Mean-Squared
PWM	Pulse Width Modulation
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
CRM	Critical Conduction Mode
PCB	Printed Circuit Board

# TABLE OF CONTENTS

	Page
ABSTRACT.....	ii
DEDICATION.....	iii
ACKNOWLEDGEMENTS.....	iv
CONTRIBUTORS AND FUNDING SOURCES .....	v
NOMENCLATURE .....	vi
TABLE OF CONTENTS.....	vii
LIST OF FIGURES .....	ix
LIST OF TABLES .....	xiii
1. INTRODUCTION .....	1
1.1 Power Factor Correction.....	1
1.2 Review of Standards .....	6
1.3 Importance of GaN Semiconductors.....	8
1.4 Current State of GaN Semiconductors.....	9
1.5 A Review of PFC Approaches.....	13
1.6 Research Objectives.....	21
1.7 Overview.....	22
2. PROPOSED TOPOLOGY.....	24
2.1 Operating Principle.....	24
2.2 Capacitor Voltage Balancing.....	30
2.3 PI Control Design .....	40
2.4 Switching Control Design.....	56
2.5 Simulation Results .....	66
3. DESIGN EXAMPLE.....	73
3.1 DC-Link Capacitor Selection and Sizing.....	73
3.2 Inductor Selection and Sizing .....	80
3.3 Switch and Diode Ratings.....	83
3.4 Design Example.....	87

	Page
4. HARDWARE RESULTS .....	91
4.1 PCB Design.....	91
4.2 Test Setup.....	94
4.3 Digital Control Implementation.....	96
4.4 Figures of Merit .....	97
5. CONCLUSION.....	101
5.1 Conclusions.....	101
5.2 Future Work.....	102
REFERENCES .....	103
APPENDIX.....	107



## LIST OF FIGURES

	Page
Figure 1. Diode Rectifier with a DC-Link Capacitor.....	2
Figure 2. Diode Rectifier with a DC-Link Capacitor Input Voltage and Current.....	3
Figure 3. Diode Rectifier with a DC-Link Capacitor Input Current FFT .....	4
Figure 4. Boost PFC .....	6
Figure 5. Specific Ron vs. Breakdown Voltage (Reprinted).....	11
Figure 6. Bridge-less Boost PFC.....	14
Figure 7. Totem-Pole PFC.....	16
Figure 8. FCML Totem-Pole PFC.....	18
Figure 9. Proposed Topology (3-Level).....	20
Figure 10. Proposed Topology (5-Level).....	20
Figure 11. Positive Switching States .....	25
Figure 12. Sine Wave Zones and States.....	27
Figure 13. Capacitor Balancing Equivalent Circuit.....	30
Figure 14. Input Current for $D_{\max} = 1.00$ .....	33
Figure 15. Currents of Switches 1-6 for $D_{\max} = 1.00$ .....	33
Figure 16. Input Current for $D_{\max} = 0.95$ .....	34
Figure 17. Currents of Switches 1-6 for $D_{\max} = 0.95$ .....	34
Figure 18. Input Current Overlaid for $D_{\max} = 0.98$ (Blue), 0.99 (Red), 1.00 (Green) .....	35
Figure 19. Input Current for $L_m = 0 \mu\text{H}$ .....	37
Figure 20. Currents of Switches 1-6 for $L_m = 0 \mu\text{H}$ .....	37

Figure 21. Input Current for $L_m = 100 \mu\text{H}$ .....	38
Figure 22. Currents of Switches 1-6 for $L_m = 60 \mu\text{H}$ .....	38
Figure 23. Input Current for $L_m = 1200 \mu\text{H}$ .....	39
Figure 24. Currents of Switches 1-6 for $L_m = 1200 \mu\text{H}$ .....	39
Figure 25. Boost State.....	42
Figure 26. Charge State.....	43
Figure 27. Current Control Loop .....	47
Figure 28. Overall Control Loop .....	48
Figure 29. Duty Cycle to Inductor Current Transfer Function .....	50
Figure 30. $k_p$ vs $k_i$ .....	52
Figure 31. Magnitude (Top) and Phase (Bottom) Bode Plots for $k_i = 100, 1k, 5k,$ 10k, 15k, 25k, 30k, 40k, 50k.....	52
Figure 32. Duty Cycle to Inductor Step Response for $k_i = 10k, 15k, 25k, 30k$ .....	53
Figure 33. Duty Cycle to Output Voltage Step Response .....	54
Figure 34. Circuit Simulation Inductor Current for Various $k_i$ Values .....	55
Figure 35. Circuit Simulation Inductor Current for $k_i = 100, 25k, 50k$ .....	56
Figure 36. 3-Level Proposed Topology with Legs Labeled .....	57
Figure 37. Switching Control Logic Term Generation Block Diagram for an n-Level Topology.....	59
Figure 38. Switching Control Logic Block Diagram for an n-Level Topology .....	60
Figure 39. $V_S$ and $V_{AC}$ and Operating Zones for a 5-Level Topology .....	63
Figure 40. $V_S$ and $V_{AC}$ and Operating Zones for a 3-Level Topology .....	65
Figure 41. Output Voltage and Inductor Current for Full to Half Load Step for 3-Level Topology.....	66
Figure 42. Output Voltage and Inductor Current for Half to Full Load Step for	

3-Level Topology.....	67
Figure 43. Output Voltage and Input Current for Full to Half Load Step for 5-Level Topology.....	68
Figure 44. Output Voltage and Input Current for Half to Full Load Step for 5-Level Topology.....	68
Figure 45. Input/Output Voltage and Inductor Current for a Voltage Drop for 3-Level Topology.....	69
Figure 46. Input/Output Voltage and Inductor Current for a Voltage Drop for 5-Level Topology.....	70
Figure 47. Input/Output Voltage and Inductor Current for a Voltage Sag for 3-Level Topology.....	71
Figure 48. Input/Output Voltage and Inductor Current for a Voltage Sag for 5-Level Topology.....	71
Figure 49. Diode Rectifier with Pure Resistive Output .....	74
Figure 50. Diode Rectifier Diode and Output Currents .....	75
Figure 51. Capacitor Voltage Differences for Various ESR Values on a 3-Level Topology.....	78
Figure 52. Capacitor Voltage Differences for Various Capacitance Values on a 3-Level Topology.....	79
Figure 53. Input and Output Voltage and Input Current for (a) 265V and (b) 85V Input Voltage.....	89
Figure 54. Fractional Capacitor Voltages .....	90
Figure 55. Prototype PCB Schematic .....	91
Figure 56. Prototype PCB Layout.....	92
Figure 57. Final Prototype PCB.....	93
Figure 58. Test Setup .....	94
Figure 59. Prototype Input Current and Voltage .....	98
Figure 60. Prototype Output Current and Voltage.....	99

Figure 61. Prototype Output Voltage and Fractional Voltage Level ..... 100

## LIST OF TABLES

	Page
Table 1. 600V FETs Comparison (Reprinted) .....	10
Table 2. 600V vs 200V GaN Comparison .....	12
Table 3. Zones, States, Switches, and Voltage Levels Reference .....	29
Table 4. Maximum Duty Cycle Effect on Switch and Input Currents.....	35
Table 5. Midpoint Inductor Effect on Switch and Input Currents .....	40
Table 6. Switching States, Zones of Operation, and Voltages Based on Leg States for a 3-Level Topology.....	58
Table 7. Leg States and $V_{AC}$ Voltages for a 5-Level Topology.....	61
Table 8. Switch Currents for 100W Example with Various ESR Values.....	85
Table 9. Switch Currents for 100W Example with Various Capacitance Values.....	86
Table 10. Design Example Specifications .....	87

# 1. INTRODUCTION

## 1.1 Power Factor Correction

Low power factor can result from non-linear or highly reactive loads, such as diode rectifiers or motors that are connected to the grid. Low power factor will increase losses on the grid by increasing the apparent power and therefore the  $I^2R$  losses and decreasing the allowable real power that can be transmitted within power line ratings [1]. There are many applications where power factor correction (PFC) is necessary and required by standards and regulations that will be reviewed in the next section.

### 1.1.1 Power Factor

Power factor is a measure of the real power being delivered versus the apparent power on the system. The real power is the power that is useful and will eventually be delivered to the load. However, apparent power consists of both real and reactive power and it is the apparent power that determines the minimum ratings of the system. Therefore, the power factor should be as close to one as possible in order to avoid needlessly overrated components in the system.

In power systems, where voltage amplitude is held constant, increasing power factor will increase the current amplitude required to deliver the same amount of real power in the system. This is undesirable because it will cause higher losses in the system. This is because power is delivered through long cables that have some small amount of resistance and losses on these power delivery systems increase as  $I^2R$ . Because of this, the voltage on these power lines is stepped up to very high levels using large transformers in order to minimize the amount of current necessary to deliver power. Additionally, power lines are only able to carry a certain amount of current, so if the power factor of the system is low the amount real power that can be delivered by the system

will be significantly reduced. Therefore, regulations have been put in place that require many devices connected to the grid to maintain a minimum power factor.

Diode rectifiers are the most prevalent grid connected low power factor converter and is used in many applications from DC power supplies to light bulbs [2]. The reason the diode rectifier causes low power factor is because current is drawn in bursts to charge a DC-Link capacitor, which results in a very non-sinusoidal input current. The schematic for a diode rectifier with a DC-Link capacitor is shown in Figure 1.

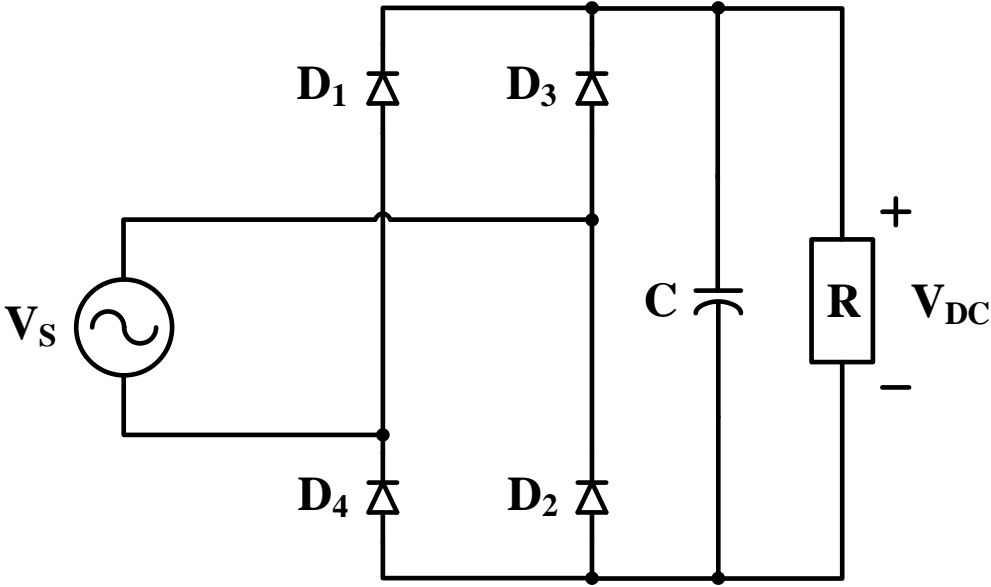


Figure 1. Diode Rectifier with a DC-Link Capacitor

The ideal load for perfect power factor is a resistor which will result in sinusoidal input current and any load that causes the current to deviate from that linear relationship between voltage

and current results in power factor that is less than one. The source voltage and current for a diode rectifier are shown in Figure 2.

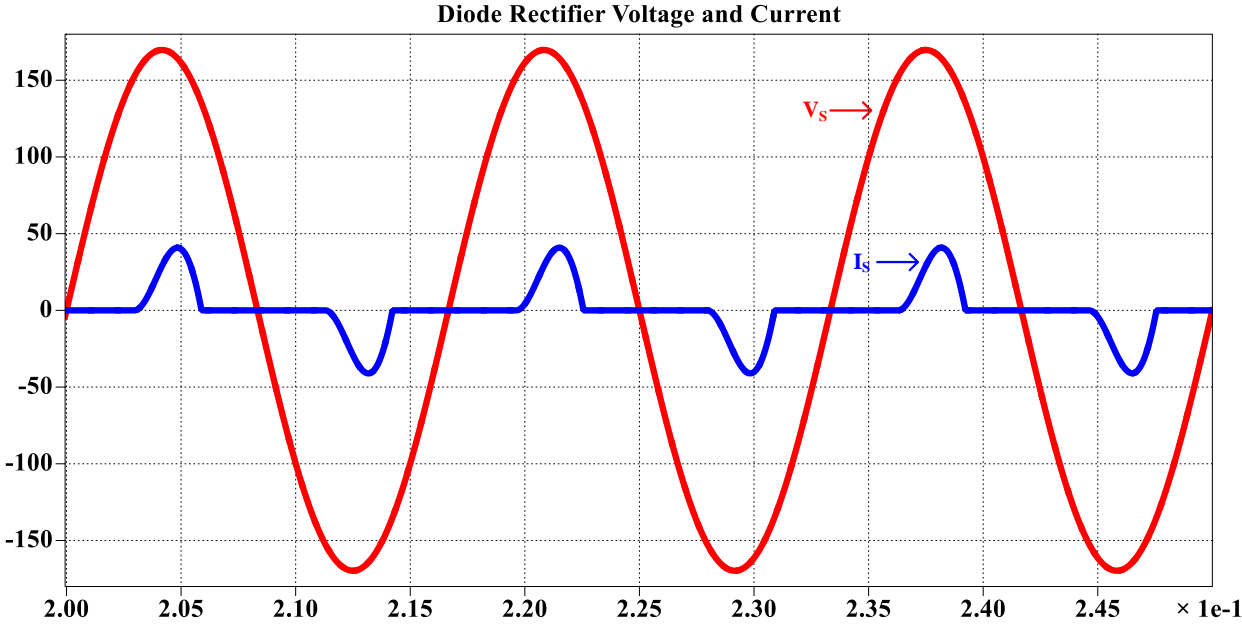


Figure 2. Diode Rectifier with a DC-Link Capacitor Input Voltage and Current

The harmonics of the current are shown in a Fast Fourier Transform (FFT) graph of the current in Figure 3. The odd harmonics (3<sup>rd</sup>, 5<sup>th</sup>, 7<sup>th</sup>, ...) are the prevalent because the waveform is an odd function. However, on the DC side, the function is even, and the even harmonics are more prevalent. The fundamental is the “1<sup>st</sup> harmonic” and the vector sum of the RMS values of all odd harmonics including the fundamental is the total root-mean-squared (RMS) current. The distortion power factor (DPF) is the ratio of the fundamental RMS to the total RMS values. This means the DPF will always be between 0 and 1. Total harmonic distortion (THD) is the ratio of the vector



sum of the RMS values of all harmonics excluding the fundamental to the RMS value of the fundamental. This means that the THD will be between 0 and positive infinity and is often given as a percentage.

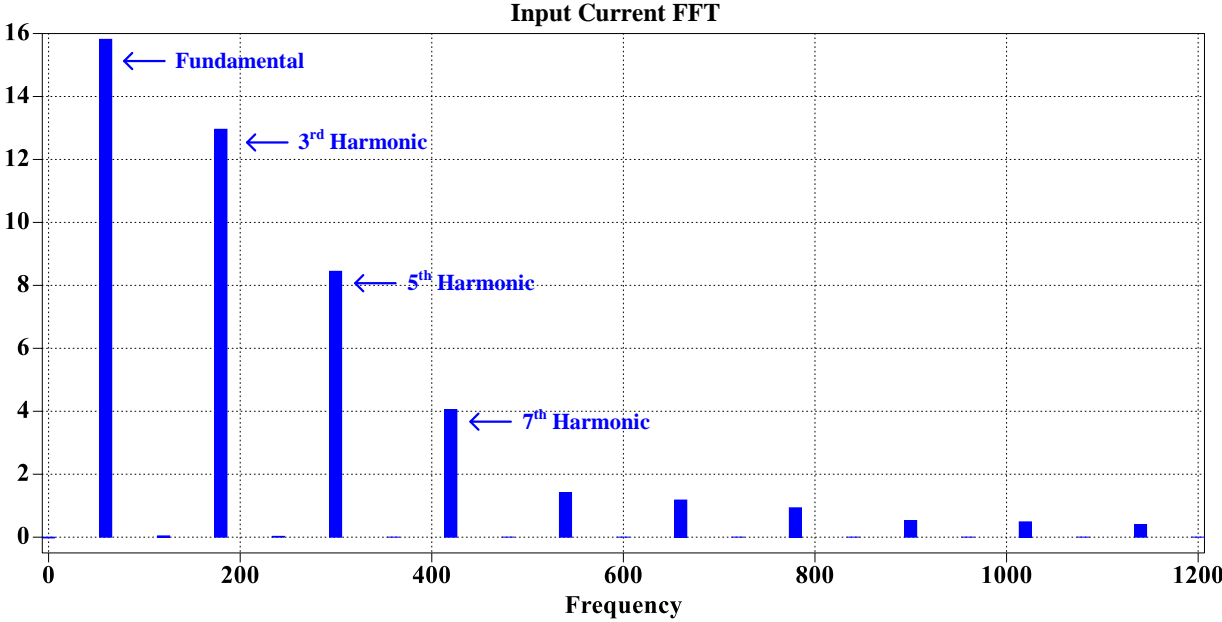


Figure 3. Diode Rectifier with a DC-Link Capacitor Input Current FFT

Motors are an example of a load that results in low power factor. Many motors are also supplied by a diode rectifier to generate a DC-Link and an inverter that uses the DC-Link to produce variable frequency and amplitude voltage that drives the motor. Motors are core components of air conditioning systems and have many industrial applications. Many of these types of loads use PFC circuits to increase the power factor of the load to satisfy standards and reduce ratings. Electronics also require DC power supplies, which must generate DC voltage using

a rectifier. Datacenters are a large and growing component of total energy consumption in the United States and in the world [3]. Because datacenters operate constantly and consume a large amount of power, high efficiency, reliable, and high power density PFC designs are of particular value for their operation.

### 1.1.2 Power Factor Correction

To address the problems introduced above, PFC circuitry can be added to existing AC-DC rectifiers or new AC-DC topologies can be made to achieve PFC. There are many types of PFC circuits that can be either active or passive. Passive PFC circuits are those that do not contain switching devices. The general strategy of passive PFC circuits is adding passive components (inductors, capacitors, resistors, and diodes) to force the input current to align more closely with the input voltage. The advantages of this approach are that it does not require control or switching devices which can increase the complexity and cost of a design and does not produce any high frequency electromagnetic interference (EMI). The disadvantages are the components are often designed for a single operating condition, the passive components are bulky in order to deal with low frequency oscillations, and the output voltage is not regulated [4].

Active PFC circuits are those that make use of switching devices to improve power factor and regulate output voltage. The traditional active PFC circuit is the boost PFC converter. The schematic of the boost PFC converter is shown in Figure 4. The boost PFC converter consists of a boost converter attached to the DC side of a diode rectifier. The boost converter is controlled draw current from the AC source in the same manner as a resistor, which would result in perfect power factor. At the same time, the output voltage of the boost converter is regulated at some DC value that is larger than the peak value of the AC source.

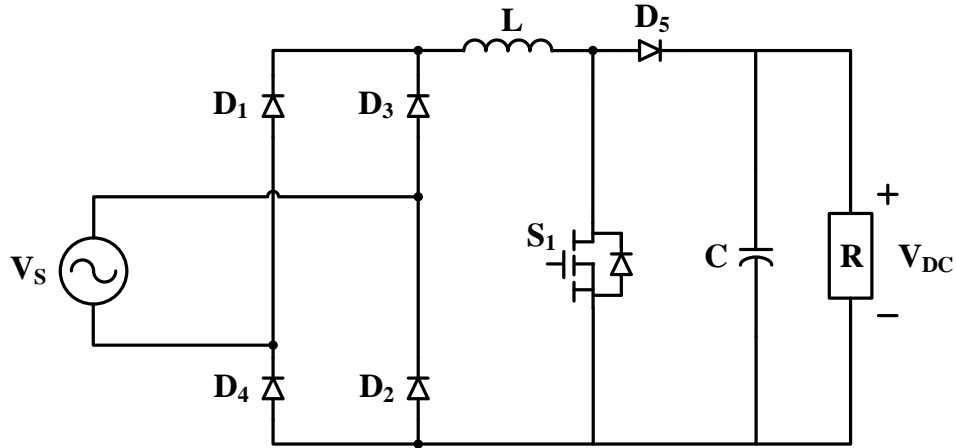


Figure 4. Boost PFC

The advantages of the boost PFC converter are that it has a low part count, relatively simple control, and can be retrofitted to systems that already exist relatively easily. For these reasons, it is the most common PFC circuit. The disadvantages are that the passive components can still become quite large, the diodes in the circuit can contribute a significant amount of losses from voltage drops and at high switching frequency, and component ratings can become quite large for high power converters. A more extensive review of multilevel PFC topologies will be conducted in section 1.6.

## 1.2 Review of Standards

There are many standards that govern the minimum power factor and maximum harmonic injection of grid connected devices. However, the most common standards are IEC 61000-3-2 [5] and Energy Star® [6]. IEC 61000-3-2 is an international standard that limits the amount of harmonic currents that can be injected into the grid by class of device and by the order of harmonic. Energy Star® is a set of standards governed by the United States Environmental Protection Agency (EPA) that requires a minimum power factor for all loads above a certain power level. There are

### 1.2.1 Harmonic Currents

Harmonic currents are currents that oscillate at some multiple of the fundamental frequency. Harmonic currents contribute to apparent power, but do not contribute to real power. Therefore, as the magnitude of harmonic currents increase relative to the fundamental current, the power factor of the circuit will decrease. Power factor is defined as the ratio of real power to apparent power, but it can also be split into two components, which are displacement power factor (DPF) and distortion power factor (DTF). DPF describes the phase difference between the input current and the input voltage. The DPF is often described by  $\cos\theta$ , where  $\theta$  is the phase difference between the input voltage and input current. This is why highly inductive loads contribute significantly to power factor. DTF describes how well the shape of the input current matches the shape of the input voltage. DTF is often described as the ratio of the RMS value of the fundamental frequency to the total RMS value. The total RMS value is a theoretically infinite vector sum of all harmonic multiples of the fundamental frequency. In reality, this sum is calculated to about 40 harmonic multiples. The IEC 61000-3-2 standard specifies which of these multiples is measured and gives specific limits for each of these multiples.

### 1.2.2 Differences Between Standards

As mentioned above, the IEC 61000-3-2 only accounts for DTF, which implies the DPF can be quite significant without penalty. However, the Energy Star regulation gives a general power factor limit of 0.9 that all devices above 100W must satisfy. These standards seem to approach the same problem from different directions. In fact, it is possible to design a passive PFC circuit that will pass the test for one standard and not the other and vice versa [7]. This is more of an interesting point than a true critique of either standard because if an active PFC circuit is

designed, it can easily pass both standards. In effect, these standards heavily encourage active PFC circuits and are the reason why active PFC circuits are such a common subject in research today.

### **1.3 Importance of GaN Semiconductors**

GaN devices are a type of wide bandgap switching (WBG) device. WBG devices are so called because they have a higher breakdown critical electric field ( $E_c$ ) than silicon (Si) devices, which are the industry standard [8]. The  $E_c$  is an important material property of the device because it is this property and channel length that determine the blocking voltage of a switching device. If a device has a lower  $E_c$ , then the channel length must be longer to achieve the same blocking voltage. Increasing channel length has the dual effect of increasing on-resistance ( $R_{on}$ ) and increasing device capacitance. Therefore, WBG devices can have a much smaller package size than Si devices and, due to decreased device capacitance, can switch at higher frequencies, both of which result in higher power density. Specific figures of merit relating to device capacitance are given in the next section.

Si devices consist of several regions that are doped positively (P) and negatively (N) and form NPN or PNP devices. The interface between P and N regions is called a PN junction. When a voltage is applied to the gate of a Si device, an inversion layer forms in the middle blocking material of the device allowing current to flow in a conductive channel from one end to the other. When the device turns off, the charges stored to create the inversion layer take a certain amount of energy to recombine and cause a small amount of current to flow in the opposite direction of normal conduction to close the conductive channel. This current is called reverse recovery current and the losses associated with this phenomenon are called reverse recovery losses. GaN devices do not have PN junctions and therefore do not require the same recombination energy to close the

conductive channel. Because of this, GaN devices have no reverse recovery current or reverse recovery losses.

The fact that WBG devices do not have reverse recovery losses is significant for developing multilevel topologies. Multilevel topologies, like the flying capacitor multilevel totem-pole PFC or the proposed topology, would require soft switching to function with Si devices due to the negative effect reverse recovery losses have on multilevel topologies [9]. However, because GaN devices can switch very quickly and do not have reverse recovery losses, multilevel topologies can achieve a very high efficiency, very power dense PFC circuit even with hard switching.

#### **1.4 Current State of GaN Semiconductors**

Low device capacitance values inherent to GaN devices are a major reason why GaN devices are of such interest in high switching frequency power devices. There are three figures of merit, presented in [8] [10] [11] that describe the performance of high speed, high power switches and they describe maximum switching speed, switching losses, and reverse recovery losses. Lower figure of merit values are better. The input capacitance is described as follows  $C_{iss} = C_{gs} + C_{gd}$ . There are two forms of the switching speed figure of merit, which are  $R_{on}C_{iss}$ , which is not dependent on the voltage, and  $R_{on}Q_{iss}$ , which is dependent on voltage. The output charge is  $Q_{oss} = C_{o(er)}V_o$ . This is the energy stored in the output capacitance which is calculated by the output capacitance times the output voltage. The switching loss figure of merit that describes the relative loss of hard and soft switching is given by  $R_{on}Q_{oss}$ . The final figure of merit describes the reverse recovery losses of the device. The reverse recovery loss is the loss of the switch that occurs due to evacuation of the minority carriers of a bipolar junction when the device is turned off. This evacuation causes a small amount of current to flow in the reverse direction for a small amount of time before the blocking voltage is established [12]. GaN devices do not function in this way and

do not have minority carriers, so there is no reverse recovery loss associated with turning the device off. This is one of the major advantages of GaN because it allows converters to operate at very high efficiency even under hard-switching conditions [13].

Table 1. 600V FETs Comparison (Reprinted)\*

Technology	Part No	$R_{on}$ (m $\Omega$ )	$C_{iss}$ (nF)	FOM1 ( $R_{on}C_{iss}$ )	$Q_{oss}$ ( $\mu$ C)	FOM2 ( $R_{on}Q_{oss}$ )	$Q_{rr}$ ( $\mu$ C)	FOM3 ( $R_{on}Q_{rr}$ )
Si SJ	IPT60R028G7 [14]	28	4.82	135	0.074	2.072	8.7 (100A/us, 400V)	243.6
SiC MOS	SCT3030 [15]	30	1.53	45.9	0.084	2.55	0.13 (1100A/us, 600V)	3.9
E-Mode GaN FET	GS66516T [16]	25	0.52	13	0.113	3.25	0	0
	PGA26E07BA [17]	56	0.405	22.68	0.045	2.52	0	0
Cascode GaN FET	TPH3207WS [18]	35	2.2	77	0.11	3.85	0.18 (1000A/us, 400V)	6.125

Table 1 compares the on resistance, device capacitances, and three figures of merit among 600V switching devices of different materials. The devices characteristics shown are for a state of the art Si super junction (SJ) switch, a SiC switch, and various GaN switches. For FOM1, the GaN devices are significantly faster than the Si SJ switch and most are faster than the SiC switch. For

---

\* Reprinted with permission from “Review of GaN Totem-Pole Bridgeless PFC” by Qingyun Huang and Alex Q. Huang, 2017. CPSS Transactions on Power Electronics and Applications, Vol. 2, No. 3, 187-196, Copyright 2017 by CPSS.

FOM2, the state of the art Si SJ switch outperforms all other switches due to its low output capacitance but suffers from a very large reverse recovery losses as illustrated by FOM3.

Silicon Carbide (SiC) devices are another type of WBG switching device that is currently capable of producing higher blocking voltage devices than GaN devices. However, this advantage is temporary because theoretical maximum blocking voltage capability of GaN devices is higher than SiC and both are larger than Si. The theoretical limit of each material is shown in Figure 5.

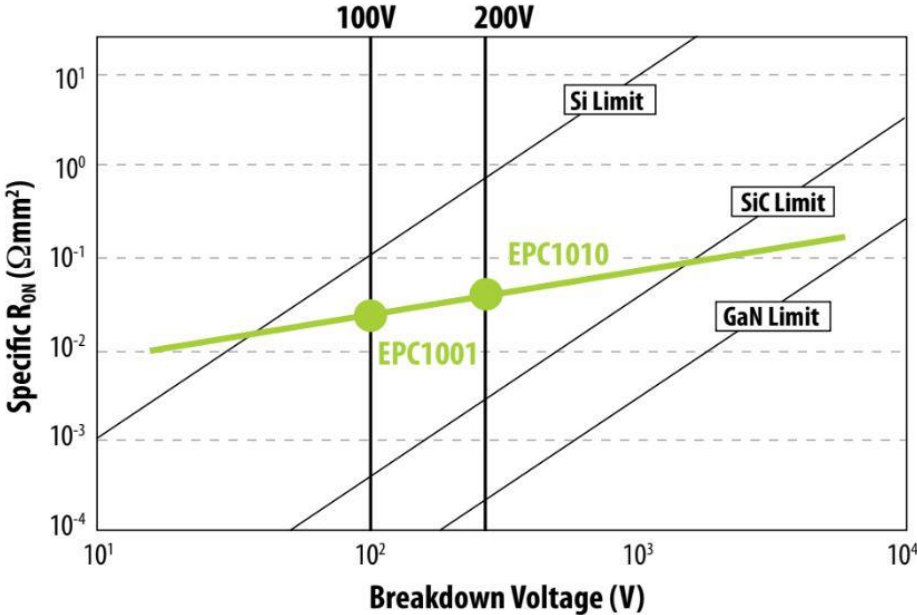


Figure 5. Specific  $R_{on}$  vs. Breakdown Voltage (Reprinted)\*

\* Reprinted with permission from “Fundamentals of Gallium Nitride Power Transistors” by Stephen L. Colino and Robert A. Beach, Ph.D., 2019. Copyright 2019 by EPC.



The specific  $R_{on}$  value is a measurement of the resistance of the conduction channel multiplied by the area of the channel. This figure captures the advantages of lower on resistance and smaller channel size, which also result in smaller device capacitances. These advantages are especially apparent in low voltage GaN semiconductors.

#### 1.4.1 Low Voltage GaN Semiconductors

The breakdown or blocking voltage of a semiconductor is determined both by the critical electric field ( $E_c$ ) and the channel length of the device. As shown in Figure 5 in the previous section, reducing the breakdown voltage of a device will significantly reduce the on resistance and required channel length of the device. This reduction has compounding benefits because reducing the package size of the device also results in lower device capacitance values. Finally, low voltage GaN devices are simply more advanced at this point than higher voltage GaN devices and therefore can achieve higher performance. This point is illustrated in Table 2.

Table 2. 600V vs 200V GaN Comparison

Technology	Part No	$R_{on}$ (m $\Omega$ )	$C_{iss}$ (nF)	FOM1 ( $R_{on}C_{iss}$ )	$Q_{oss}$ ( $\mu$ C)	FOM2 ( $R_{on}Q_{oss}$ )	$Q_{rr}$ ( $\mu$ C)	FOM3 ( $R_{on}Q_{rr}$ )
E-Mode GaN FET (600V)	GS66516T [16]	25	0.52	13	0.113	3.25	0	0
	PGA26E07BA [17]	56	0.405	22.68	0.045	2.52	0	0
E-Mode GaN FET (200V)	EPC2034	7	0.955	6.67	0.075	0.525	0	0

The 200V enhancement-mode GaN FET from EPC has reasonable improvement on the FOM1 for switching speed of two times to nearest device. However, for FOM2, which describes the switching losses of the device, the improvement is more than five times the nearest 600V device. This is in addition to the obvious improvement of the on resistance of more than three times the nearest device, which will reduce the conduction losses of the converter. These benefits combined can easily justify using a multilevel topology in order to increase efficiency and increase the switching speed of the converter, which will also increase power density.

## **1.5 A Review of PFC Approaches**

As mentioned in section 1.1, the strengths of the boost PFC topology are in its simplicity and small part count. The weaknesses are the large component ratings, large component size, diode voltage drops, and diode performance at high switching frequency. Each PFC technique reviewed in this section addresses one or more of the weaknesses of the boost PFC topology and introduces new trade-offs.

### **1.5.1 Bridge-less Boost PFC**

The bridge-less boost PFC was one of the first topologies that reduced the number of semiconductors in the PFC topology to increase the efficiency of the circuit [19]. This started the research into the field in earnest. The bridge-less boost PFC has a lower part count than the boost PFC topology. The topology also has fewer semiconductors on the current path, which increases efficiency by reducing the number of conduction losses and voltage drops. Finally, the topology brings the inductor to the AC side, which is beneficial because the inductor is not required to carry DC current in addition to the ripple current, so the size can be reduced. Additionally, locating the inductor on the AC side, helps filter EMI. A schematic of the bridge-less boost PFC is shown in Figure 6.

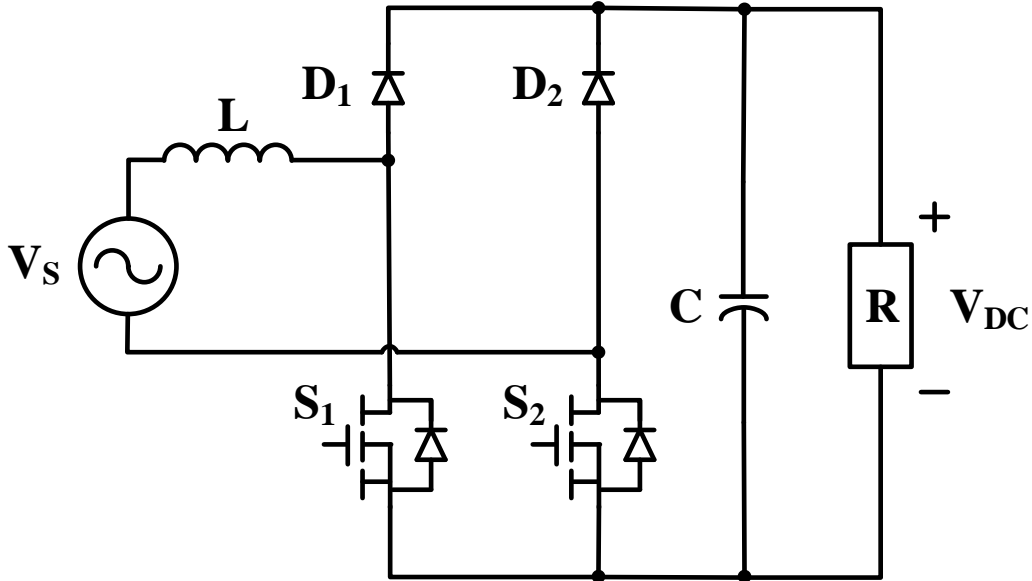


Figure 6. Bridge-less Boost PFC

One weakness of the bridge-less boost PFC is that the inductance value remains equivalent to the boost PFC, which is quite large. Additionally, all switching components are required to block the full DC voltage. Another weakness is that both diodes are required to switch at high frequency, which increases the reverse recovery losses and requires high switching frequency diodes. The EMI performance of this circuit is also a weakness. The EMI issue stems from the fact that the inductor is connected to the slow switching path for half of the line frequency cycle [20]. Because of this, there is a significant amount of noise on the parasitic capacitor from the output ground to the input AC ground. If the inductor is attached only to the fast switching leg, then the EMI issue is eliminated. There are variants of the topology that eliminate this EMI issue.

### 1.5.2 Totem-Pole PFC

The totem-pole PFC topology is receiving a significant amount of interest from both the research and industry communities for its ability to improve power density, efficiency, and

potentially reduce costs by implementation with GaN devices [8] [9] [10] [11] [21]. The fundamental limitation barring the use of the totem-pole topology without GaN devices is the reverse recovery issue of typical power switching devices, which have PN junctions as described in section 1.3. However, with this issue is overcome, the totem-pole PFC has the fewest number of switching devices of any PFC topology. The topology functions by switching one leg (S1 and S4) at very high frequency while the other leg (S2 and S3) switch at the much lower line frequency. Additionally, because GaN devices are still relatively expensive compared with traditional power switching devices, it has been noticed that Si-based power switching devices can be used on the lower switching frequency leg because reverse recovery behavior is not significant at lower frequencies and this reduces the cost of the system. The main advantage of this topology is that for the same efficiency, GaN devices on the totem-pole PFC can switching several times faster, which will reduce size and cost of the inductor and EMI filter. Additionally, the conduction resistance is lower for GaN devices and the lower frequency active switches when compared to diodes, which results in higher efficiency. These improvements result in higher power density, which ultimately lowers PCB costs. A schematic of the totem-pole PFC is shown in Figure 7.

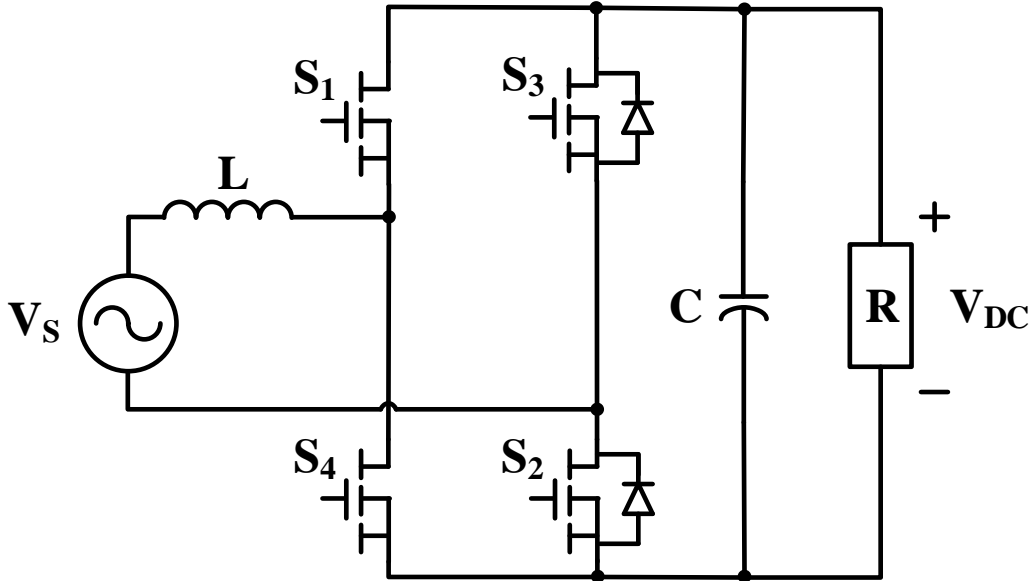


Figure 7. Totem-Pole PFC

One weakness of the topology is that all switching devices and the DC-Link capacitor needs to be rated for the full DC-Link voltage. This is especially an issue for the switches because blocking voltage and on resistance trade off directly and the package size will also increase for larger blocking voltage, which will increase device capacitance and therefore switching losses. The inductor can be decreased in size relative to the traditional boost PFC, but the effective switching frequency of the inductor current is limited to the switching frequency of the switching devices. Additionally, the maximum voltage stress on the inductor is the full DC voltage, which makes the inductor ripple quite large for higher DC-Link voltages.

### 1.5.3 Generalized Multilevel Converter

An early generalized multilevel approach was introduced in [22] and was introduced as an inverter and a bidirectional magnetic-less DC-DC converter. Because the converter is a multilevel converter, it has the benefits of reduced switch blocking voltages and reduced inductor voltage

stress. Additionally, the structure of the topology also allows for reduced capacitor stresses, which resulted in significant size reduction for higher power levels. The converter was designed to function with a DC voltage supply on the DC side to regulate capacitor voltages. The design was a generalization of many kinds of multilevel topologies such as a diode clamped or flying capacitor multilevel topology. The generalized converter was called the “P2-Cell” converter. The main benefit was that the fractional voltage levels were automatically balanced, whereas other multilevel topologies required isolated circuits to balance voltage levels above 3-level topologies. The schematic of the “P2-Cell” converter is very similar to the proposed topology, although the devices used and the control implemented are different.

One weakness of this design are the switches used, which have reverse recovery characteristics that do not allow high-frequency reverse current conduction, which means topology could not have been used as a PFC circuit. Additionally, the control did not leverage the benefit of effective switching frequency multiplication to reduce the inductor size. In addition, the topology required regulation of the DC-Link voltage, even though it was able to regulate fractional voltages.

#### 1.5.4 Flying Capacitor Multilevel Totem-Pole PFC

The flying capacitor multilevel (FCML) totem-pole PFC topology is detailed in [11]. This topology leverages the benefits of a totem-pole PFC with the additional advantages of a multilevel topology and keeps the part count relatively low and significantly improves power density. The topology also makes use of GaN devices on the high frequency leg and Si-based power switching devices on the low frequency leg for the same reason as the totem-pole PFC and receives the same higher switching frequency and higher efficiency benefits as the totem-pole. However, an  $n$ -level topology uses fractional voltage levels to reduce the voltage stress on the inductor to  $1/(n - 1)$  of the DC-Link voltage, which can theoretically reduce the size of the input inductor to  $1/(n - 1)$  of

the totem-pole PFC. Additionally, the switching scheme of the topology allows for an effective switching frequency ( $f_{sw}$ ) that is  $n-1$  times greater than the  $f_{sw}$  on each device, which can theoretically reduce the size of the input inductor by an additional  $1/(n - 1)$ . The topology only requires  $2 * (n - 1)$  GaN switches and two Si-based power switching devices to achieve an  $n$ -level topology. The GaN switches on the high frequency leg only have a reduced voltage stress of  $1/(n - 1)$  of the DC-Link voltage, which allows this topology to use low voltage GaN devices, which, as mentioned in section 1.5.2, will increase the efficiency of the topology. A schematic of the FCML totem-pole PFC is shown in Figure 8.

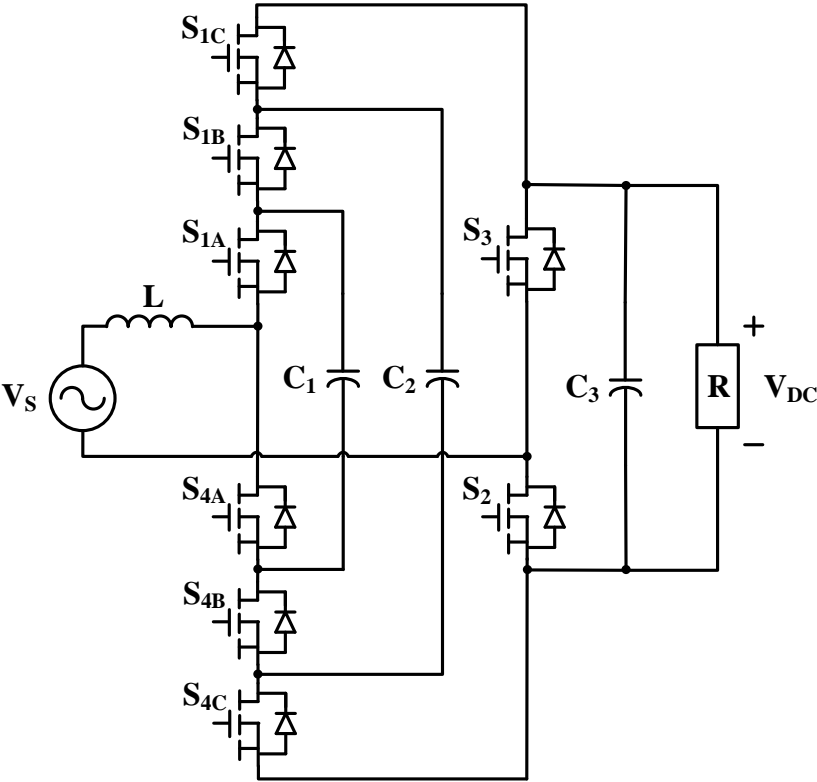


Figure 8. FCML Totem-Pole PFC

One weakness of this topology is that in addition to the DC-Link capacitor,  $n - 2$  “flying” capacitors that do not regulate DC-Link voltage are required to form the fractional voltage levels. Additionally, the DC-Link capacitor must be rated for the full DC voltage, which results in much larger DC-Link capacitors for higher voltages. The fractional voltage levels are also not regulated typically, so they are not accessible for powering lower voltage loads.

#### 1.5.5 Proposed Topology

The proposed topology builds on the totem-pole PFC and FCML totem-pole PFC topologies and adds circuitry to reduce DC-Link capacitors voltage ratings. The energy capacity of the output is maintained but is stored more heavily in the capacitance of the DC-Link capacitors, which allows power density improvements. Additionally, the design is “fully modular”, meaning that the building block components can be designed for any voltage level and the number of levels can be scaled up to meet the requirements of the topology. The topology also offers access to fractional voltage levels, which are regulated. This can be advantageous for topologies that immediately buck the DC-Link voltage. A 3-level version of the proposed topology is shown in Figure 9 and a 5-level version of the proposed topology is shown in Figure 10.



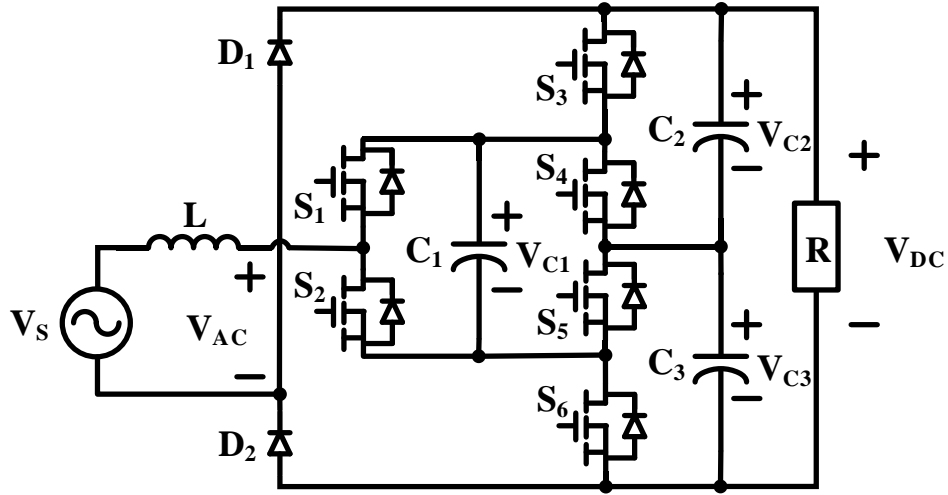


Figure 9. Proposed Topology (3-Level)

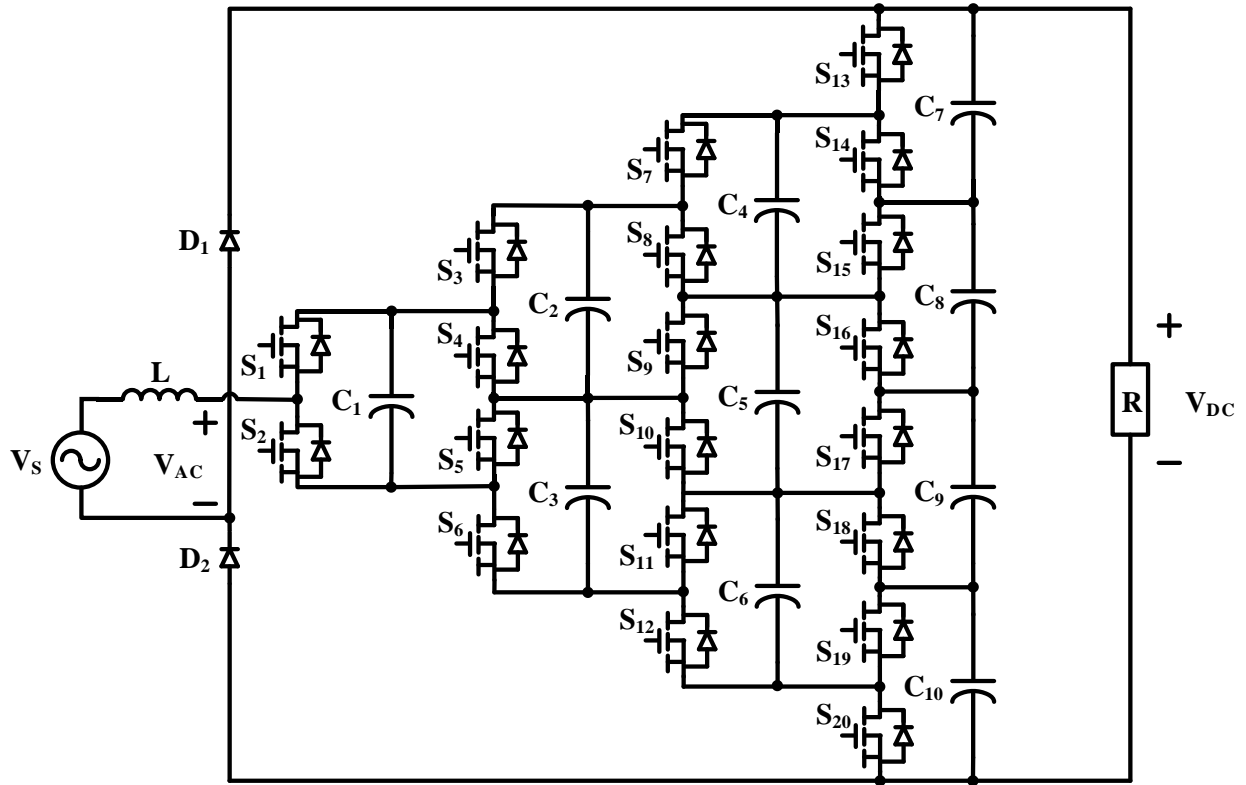


Figure 10. Proposed Topology (5-Level)

## 1.6 Research Objectives

The objective of this work is to develop a generalized multilevel boost PFC approach for AC-DC power conversion that improves the power density over the traditional boost PFC. Boost power factor correction involves controlling the duty cycle of a boost converter to control the input current and output voltage of the circuit. Because of this, the largest components in the topology are the passive components that regulate the input current and output voltage, which are the input inductor and DC-Link capacitor, respectively. These components can grow quite large due to high voltage stress for a traditional boost PFC circuit and this can also reduce efficiency. In order to improve the power density and efficiency of the circuit, lower voltage rating components should be used. A multilevel converter is one that distributes the voltage stress across more components, which reduces the amount of voltage stress to fractional levels on each component. For this reason, a multilevel boost power factor correction topology can increase efficiency and decrease the size of the converter. Additionally, the generalized multilevel boost PFC converter can be controlled to increase the effective switching frequency of the current through the input inductor by a factor dependent on the number of levels in addition to reducing the voltage stress on the inductor to a fractional level, which greatly reduces the size of the input inductor. Finally, the switching control automatically balances DC-Link capacitor voltages, which improves reliability and allows access to fractional DC voltages.

The zones of operation of the multilevel converter will be explained and the capacitor balancing operation will be analyzed. A closed loop controller design methodology for the topology that can be applied to any variant of the topology will be developed which includes a switching strategy. The closed loop controller will be a proportional integral (PI) controller with two loops for controlling voltage and current as is standard in traditional Boost PFC control design

as well as in many power electronics topologies. The specific switching control block diagram for a three-level topology will be provided as well as a procedure for producing higher level switching controllers.

A design guide for sizing components will also be provided. The component sizing will be based on the sizing of components for a traditional Boost PFC and depend on the structure of the modular design. Due to the reliance of the sizing on traditional Boost PFC components, a review of the sizing practices for the traditional Boost PFC topology is also conducted. Different versions of the proposed topology will be tested in simulation software under different loading conditions.

A physical circuit will be designed using Altium and the design will be tested for the characteristics listed above. The control will be designed on power electronics simulation software and use the code generation functionality to implement the PI controller on a microcontroller. The design will be implemented using a Texas Instruments Delfino controller and Texas Instruments GaN Half-Bridge modules. The physical results will be compared to simulation results and used to confirm design guide values and theory.

## **1.7 Overview**

Section 1 gives relevant background information on subjects that will be covered. The negative effects of power factor are explained and the relevant regulations on power factor are explained and compared. The relevance of GaN devices to power factor correction (PFC) is described and the current state of the technology is explored. A review of relevant work in the field of PFC topologies is conducted and the advantages of the proposed topology are explained.

Section 2 introduces the new topology and describes the switching states and zones of operation. There is a discussion of the voltage balancing function of the topology and how to

minimize current spikes of the topology. Design of the switching control of the topology is discussed and a review of PI control design for a boost PFC topology is presented. Simulation results are presented for different loading conditions.

Section 3 presents a design example of the topology and describes potential applications of the topology and the requirements necessary to meet the demands of these applications. There is discussion of the necessary passive components for the topology, mainly the input inductor and DC-Link capacitor. The current and voltage ratings of the switches and (if used) diodes for the topology are investigated and simulation results confirming design values are presented.

Section 4 describes the hardware design process and presents hardware results. The PCB design is discussed, and component testing is reviewed. The PI loop tuning process is reviewed and figures of merit of the topology are analyzed.

Section 5 draws conclusions from the experimental work about the topology and its applications. Future work on the topology is discussed as well as how this research fits into the field of PFC and power electronics in general.

## 2. PROPOSED TOPOLOGY

### 2.1 Operating Principle

As mentioned in section 1.6, the advantages of the proposed topology are increased power density and efficiency due to reduced voltage stress on the input inductor, output capacitors, and switching components. Additionally, the effective switching frequency of ripple current on the input inductor is  $n - 1$  times the switching frequency, where  $n$  is the number of levels of the topology. Fractional voltages are well regulated, which improves capacitor lifespan and allows fractional voltages to be accessed if needed.

In this section, the switching states of the topology are described in detail and then the zones of operation in which those switching states are used are explained. A quick reference table is also provided that describes which switches and diodes are active for every switching state and in which modes the switching states occur.

#### 2.1.1 Switching States

This section details the switching states of the 3-level circuit. Figure 11 shows the “positive” switching states. An AC source ( $V_S$ ) is connected on the left along with an AC side inductor and the load is connected across  $C_2$  and  $C_3$  on the right. All states are for the positive cycle of  $V_S$  and thus  $D_2$  is always active.

Figure 11(b) shows the “zero state” (State 1). The reason it is called the zero state is because the voltage across  $V_{AC}$  is zero. This is because  $S_2$ ,  $S_6$ , and  $D_2$  (highlighted in red) are all conducting. Another important point about this state is that  $C_1$  and  $C_3$  are connected in parallel, which occurs because  $S_4$  and  $S_6$  are conducting. This means that if there is any voltage difference between  $C_1$  and  $C_3$  before this state, there will be a rush of current from the capacitor with higher voltage to the capacitor with lower voltage. This will balance the voltage across the two capacitors

automatically. Techniques for limiting the amount of current required for balancing is discussed in section 2.2.

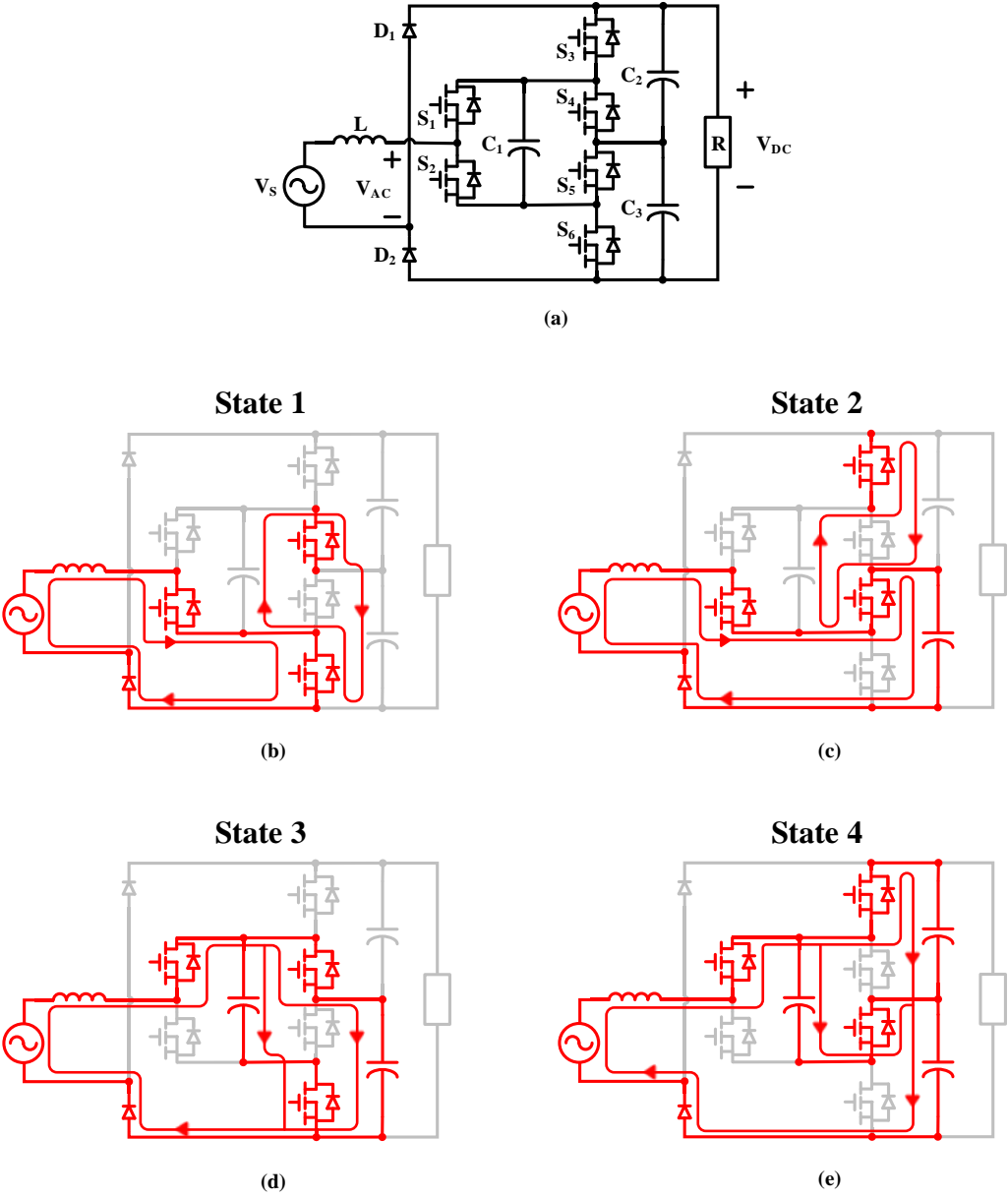


Figure 11. Positive Switching States

Figures 11(c) and 11(d) show the two states that will yield  $\frac{1}{2} V_{DC}$  (which is equal to  $V_C$ ) across  $V_{AC}$ . In state 2,  $V_{AC}$  is connected across  $C_3$ . Additionally,  $C_1$  and  $C_2$  are connected in parallel, so the voltage across these capacitors will be balanced. In state 3,  $V_{AC}$  is connected across  $C_1$  in parallel with  $C_3$ ,  $C_1$  and  $C_3$  will be balanced.

Figure 11(e) shows the state that yields  $V_{DC}$  across  $V_{AC}$  (State 4).  $V_{AC}$  is connected across  $C_1$  and  $C_2$  in parallel and in series with  $C_3$ . Due to the fact the  $V_C$  is exactly  $\frac{1}{2} V_{DC}$ , the series voltage across  $C_2$  and  $C_3$  (and thus the load) is  $V_{DC}$ . This is somewhat intuitive because the voltage across the load must be equal to  $V_{DC}$  because it is defined as such and  $C_2$  and  $C_3$  are both constantly balanced with  $C_1$ , so their voltages must be equivalent as well.

The states represented above are the four states for the positive half cycle of  $V_S$ . The negative half cycle uses the same four switch configuration to achieve 0,  $-\frac{1}{2} V_{DC}$ , and  $-V_{DC}$  across  $V_{AC}$ . The negative switch states 5, 6, 7, and 8 are identical to 1, 2, 3, and 4 respectively, but  $D_1$  is conducting instead of  $D_2$  because  $V_S$  is negative. Because  $D_1$  is conducting, the voltages across  $V_{AC}$  will be negative and may have a different magnitude.

### 2.1.2 Zones of Operation

The converter shown in Figure 11 is a 3-level converter. This may not be intuitive because there are two positive voltage levels ( $\frac{1}{2} V_{DC}$  and  $V_{DC}$ ), two negative voltages which are equal and opposite in magnitude to the positive voltage levels, and the zero-voltage level, which gives a total of five voltage levels. However, for a PFC topology only the positive voltage levels and the zero-voltage level are counted. An inverter with the same number of voltage levels would be called a 5-level inverter.

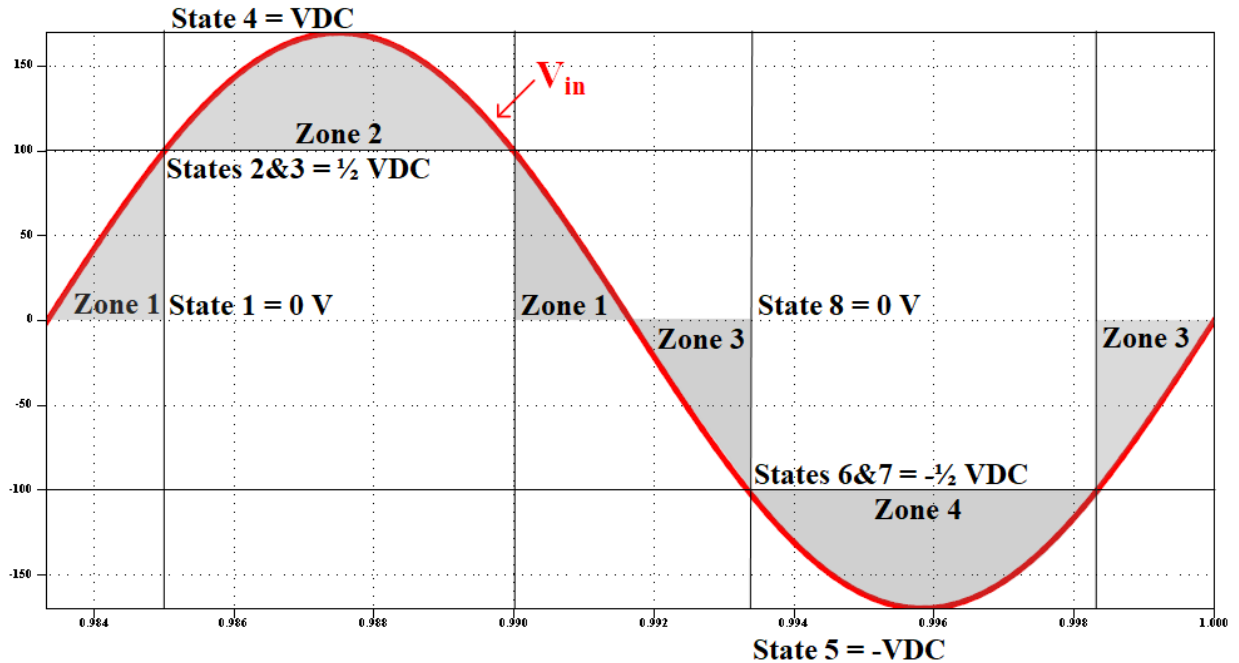


Figure 12. Sine Wave Zones and States

For the positive half cycle, the two positive voltage levels ( $\frac{1}{2} V_{DC}$  and  $V_{DC}$ ) and the zero-voltage level are used to create two zones of operation (Zone 1 and 2) shown in Figure 12. These zones are defined by maximum and minimum voltage levels. In each zone, there are one or more “boost” states and one or more “charge” states. During the boost state, a positive voltage is applied across the inductor, which causes a positive change (or boost) in the current in the inductor. During the charge state, a negative voltage is applied across the inductor, which causes negative change in the current in the inductor and the excess current is used to charge the output capacitor. The switching state known as the boost and charge state will change between different zones of operation.



Zone 1 is active between zero and  $\frac{1}{2} V_{DC}$  voltage levels as shown in Figure 12. The boost state of this zone is state 1 (0V) and the charge states are state 2 and state 3 ( $\frac{1}{2} V_{DC}$ ). State 1 is the charge state because the input voltage ( $V_S$ ) subtracted from  $V_{AC}$  will be positive. State 2 and 3 are boost states because  $V_S$  subtracted from  $V_{AC}$  will be negative. Because there are multiple charge states, each must be utilized for an equivalent amount of time during the zone to balance the voltage across every capacitor. The easiest way to do this is to alternate between the two charge states after each boost state. The maximum voltage across the inductor for this zone is  $\frac{1}{2} V_{DC}$ .

Zone 2 is active between  $\frac{1}{2} V_{DC}$  and  $V_{DC}$  voltage levels. The boost states of this zone are state 2 and state 3 ( $\frac{1}{2} V_{DC}$ ) and the charge state is state 4 ( $V_{DC}$ ). Again, state 2 and state 3 must be utilized for an equivalent amount of time to balance capacitor voltages. Notice that the charge states of zone 1 are the boost states of zone 2. This is because  $V_S$  voltage is now greater than the voltage of state 2 and state 3 ( $\frac{1}{2} V_{DC}$ ), which means a positive voltage will be applied across the inductor in these states, thus satisfying our original definition of a boost state. The maximum voltage across the inductor in this zone of operation is also  $\frac{1}{2} V_{DC}$ . This may seem counterintuitive because  $V_S$  is higher than  $\frac{1}{2} V_{DC}$  in this zone, but the voltage across the inductor is defined by the difference between  $V_S$  and  $V_{AC}$ . Because both these values are between  $\frac{1}{2} V_{DC}$  and  $V_{DC}$ , the maximum value of their difference is  $\frac{1}{2} V_{DC}$ .

Zone 3 is active between zero and  $-\frac{1}{2} V_{DC}$  voltage levels. The boost state of this zone is state 8 (0V) and the charge states are state 6 and state 7 ( $-\frac{1}{2} V_{DC}$ ). Similarly to zone 1, state 6 and state 7 must be used for an equivalent amount of time to balance voltage levels. This zone is the negative complement of zone 1. The maximum voltage across the inductor for this zone is  $\frac{1}{2} V_{DC}$ .

The fourth zone is active between  $-\frac{1}{2} V_{DC}$  and  $-V_{DC}$  voltage levels. The boost states of this zone are state 6 and state 7 ( $-\frac{1}{2} V_{DC}$ ) and the charge state is state 5 ( $-V_{DC}$ ). Again, State 6 and state 7 must be used for an equal amount of time to balance voltage levels. This zone is the negative complement of zone 2. The maximum voltage across the inductor for this zone is  $\frac{1}{2} V_{DC}$ .

Table 3. Zones, States, Switches, and Voltage Levels Reference

State	Zone(s)	Active Switches and Diodes	VAC Voltage
1	Zone 1 (boost state)	D2, S2, S4, S6	0
2	Zone 1 (charge state) Zone 2 (boost state)	D2, S2, S3, S5	$\frac{1}{2} V_{DC} (V_C)$
3	Zone 1 (charge state) Zone 2 (boost state)	D2, S1, S4, S6	$\frac{1}{2} V_{DC} (V_C)$
4	Zone 2 (charge state)	D2, S1, S3, S5	$V_{DC}$
5	Zone 4 (charge state)	D1, S2, S4, S6	$-V_{DC}$
6	Zone 3 (charge state) Zone 4 (boost state)	D1, S2, S3, S5	$-\frac{1}{2} V_{DC} (-V_C)$
7	Zone 3 (charge state) Zone 4 (boost state)	D1, S1, S4, S6	$-\frac{1}{2} V_{DC} (-V_C)$
8	Zone 3 (boost state)	D1, S1, S3, S5	0

## 2.2 Capacitor Voltage Balancing

This section describes the voltage balancing operation of the proposed topology and some of the design considerations that arise from quickly connecting capacitors in parallel. Additionally, methods are presented to limit the negative impacts of this operation. Further discussion on capacitor design is conducted in section 3.1 in order to limit current spikes.

### 2.2.1 Balancing Operation

The method of balancing capacitors in the circuit is to connect them in parallel, which means there will be a current spike through the capacitors and the switches that connect them. The magnitude of this spike is dependent on the voltage difference between the capacitors and the total impedance on the path connecting the capacitors. An equivalent circuit is shown in Figure 13.

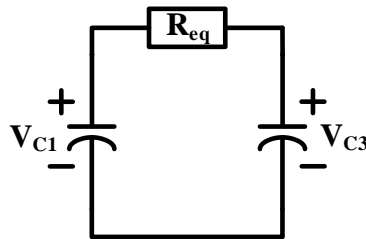


Figure 13. Capacitor Balancing Equivalent Circuit

The capacitors on the output leg of the topology will always be discharging current to the load and because of this will need to be regularly charged by other capacitors in the topology or by the source directly. Due to the configuration of the topology, every fractional voltage level mode will have at least one capacitor that cannot be charged directly by the source. A capacitor

that fits this description will be referred to as an off-capacitor. The off-capacitor(s) will change as the topology operates in different zones. For example, if the 3-level topology is operating in zone 1, where the input voltage is between 0 V and  $\frac{1}{2} V_{DC}$ , the off-capacitor will be  $C_2$ . However, if the 3-level topology is operating in zone 3, where the input voltage is between 0 V and  $\frac{1}{2} V_{DC}$ , the off-capacitor will be  $C_3$ . Finally, if the 3-level topology is operating in zone 2 or 4, where the magnitude of the input voltage is between  $\frac{1}{2} V_{dc}$  and  $V_{DC}$ , there is no off-capacitor, because all capacitors can be charged by the source.

The issue that arises is that the off-capacitor will drift away from the other capacitors very quickly when the duty cycle becomes very high. This is because the off-capacitor is only charged when the switching signal is low and when the duty cycle becomes very high, the off-capacitor is charged much less often. This means that when the off-capacitor is connected to another capacitor the voltage difference between the capacitors will be very large and the current will spike in order to balance the capacitors. However, because the duty cycle is so high, the capacitor may not be balanced even though the current into the off-capacitor is very high, so the current spikes may continue until the end of the mode of operation. If this current spike is large enough, it will require a larger current rating for components, driving up the cost of the circuit.

There are many methods of mitigating high peak switch currents, but two will be addressed in this section. The first is to limit the maximum duty cycle range to something less than 100% to prevent the capacitor voltages from drifting very far apart close to the input voltage zero crossing. The second is to add inductors to the midpoints of each half-bridge in the topology to limit current spikes.

The maximum peak switch current is the highest current value through any one of the six switches in the three-level topology tested. The maximum peak switch current is the one of interest

because it will determine the minimum ratings of the switches. The input current THD is also an important metric because the goal of PFC is to attain high power factor and large THD will reduce the power factor of the circuit.

### 2.2.2 Limiting Maximum Duty Cycle

Limiting maximum duty cycle from the PI controller trades off between lowering input current THD and reducing current spikes. The second solution is to limit the maximum value of the duty cycle. This option is warranted when capacitors have very low ESR values and large current spikes occur in the switch currents near the input voltage zero crossing. A maximum value of the duty cycle will occur very close to the zero crossing of the input voltage waveform because the PI controller will try to boost the low voltage value by a very large amount causing the duty cycle to become large. When the duty cycle becomes very large, the amount of time the off-capacitor is charged becomes very low and thus the voltage of the off-capacitor will drift away from the other capacitors in the circuit. One simple way to avoid this is to limit the maximum value of the duty cycle so that the voltage of the off-capacitor is not allowed to drift very far and thus the peak current is minimized. However, the consequence of limiting the duty cycle is that the input current will not be controlled while the duty cycle is limited. Additionally, when the duty cycle is no longer above the limit and controller starts controlling the input current again, the step response of the controller will cause an overshoot and a small amount of ringing further distorting the input current waveform. This will cause the THD of the input current waveform to increase.

As mentioned previously, this spike only appears when the ESR value is very low, so the simulation tests are run with an ESR value of 20 m $\Omega$ , which is 100 times smaller than the expected ESR for an electrolytic capacitor of this voltage rating and capacitance. Figures 14-18 show the simulation results for a different  $D_{\max}$  values.

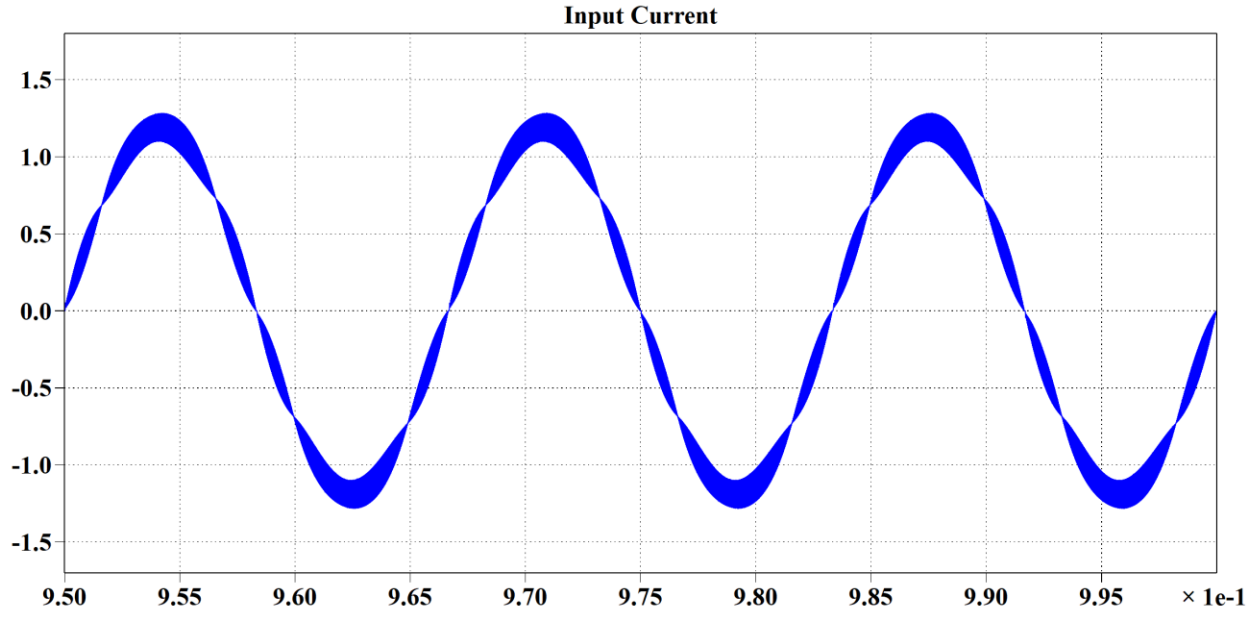


Figure 14. Input Current for  $D_{\max} = 1.00$

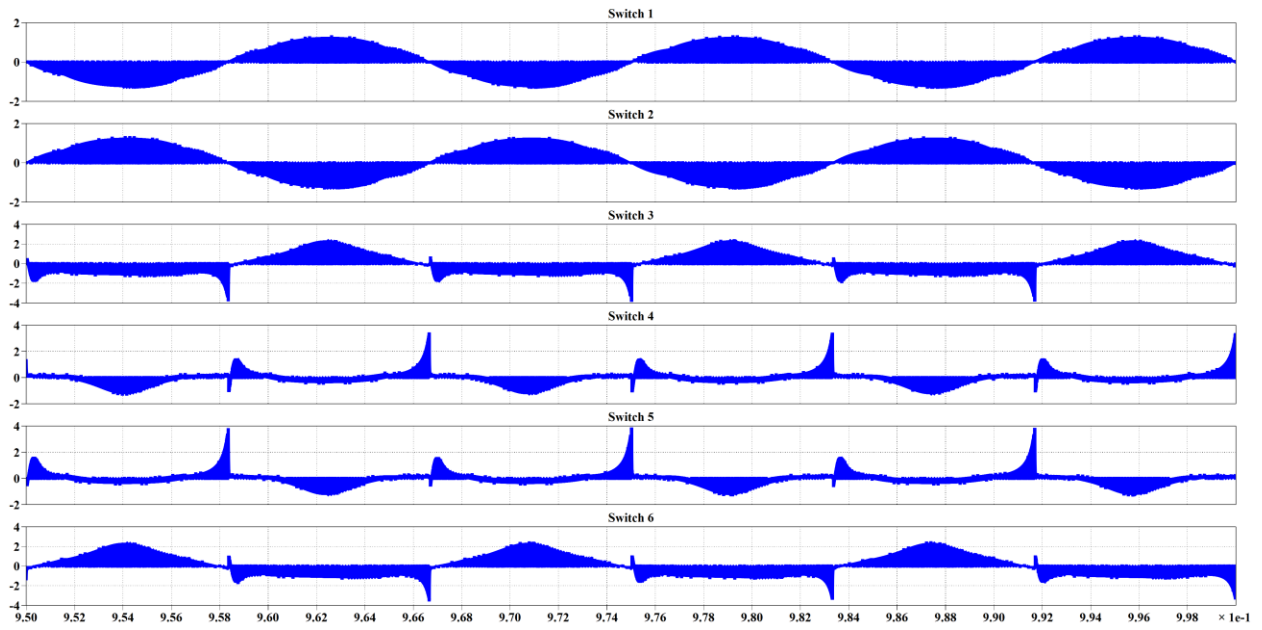


Figure 15. Currents of Switches 1-6 for  $D_{\max} = 1.00$

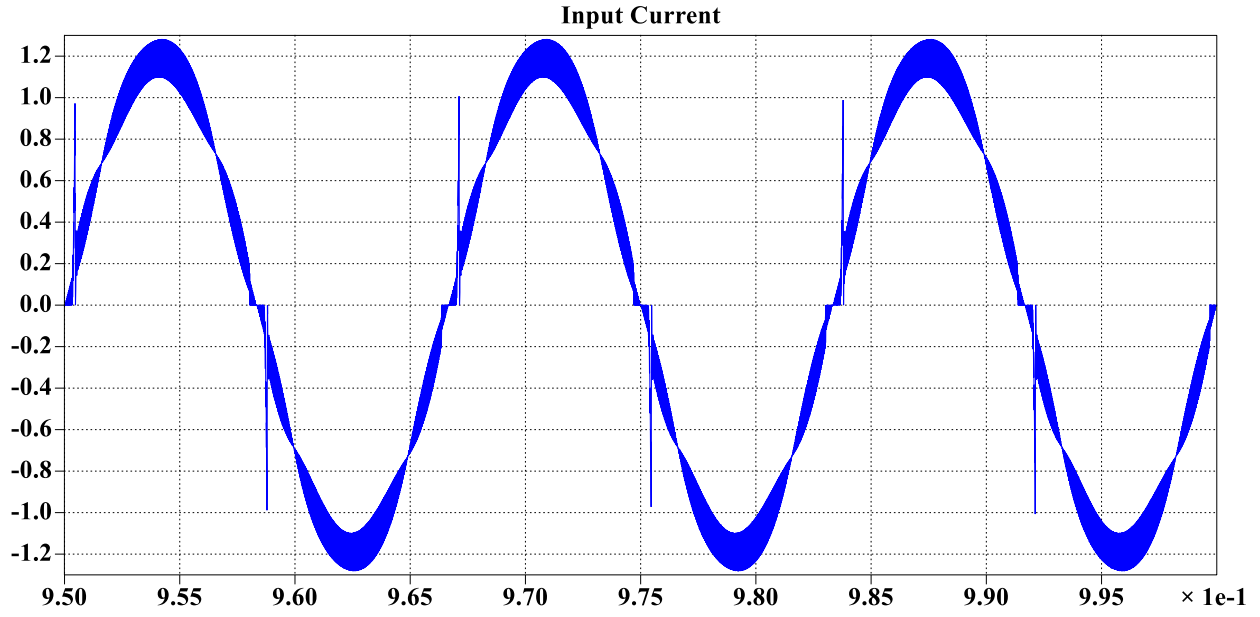


Figure 16. Input Current for  $D_{\max} = 0.95$

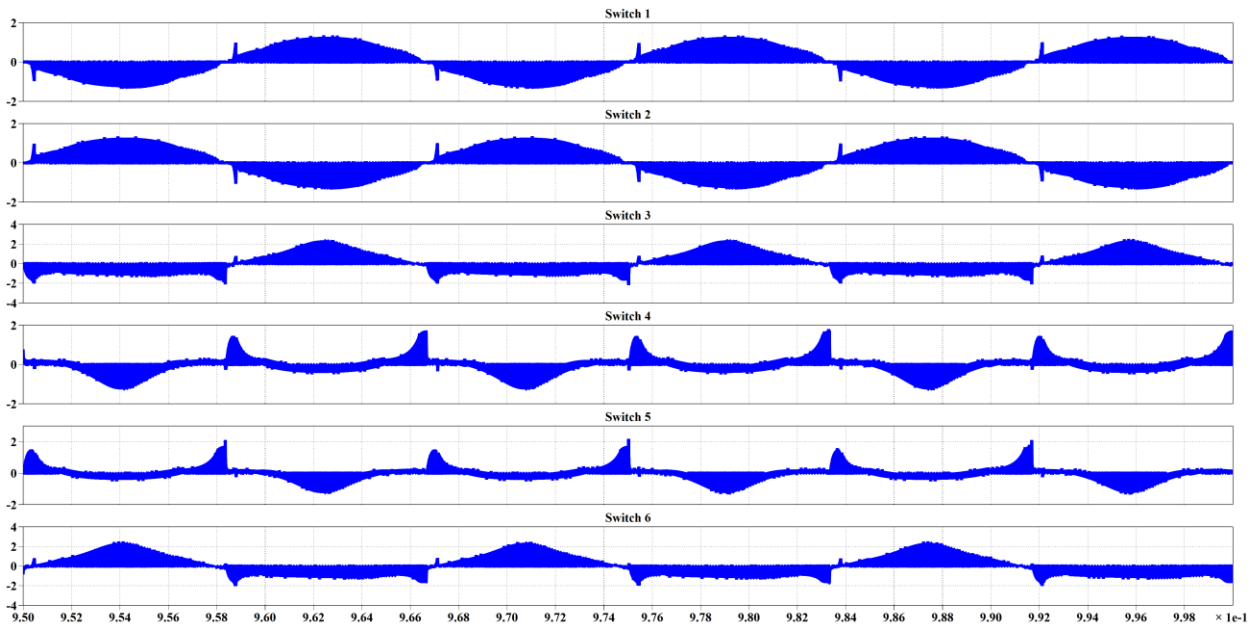


Figure 17. Currents of Switches 1-6 for  $D_{\max} = 0.95$

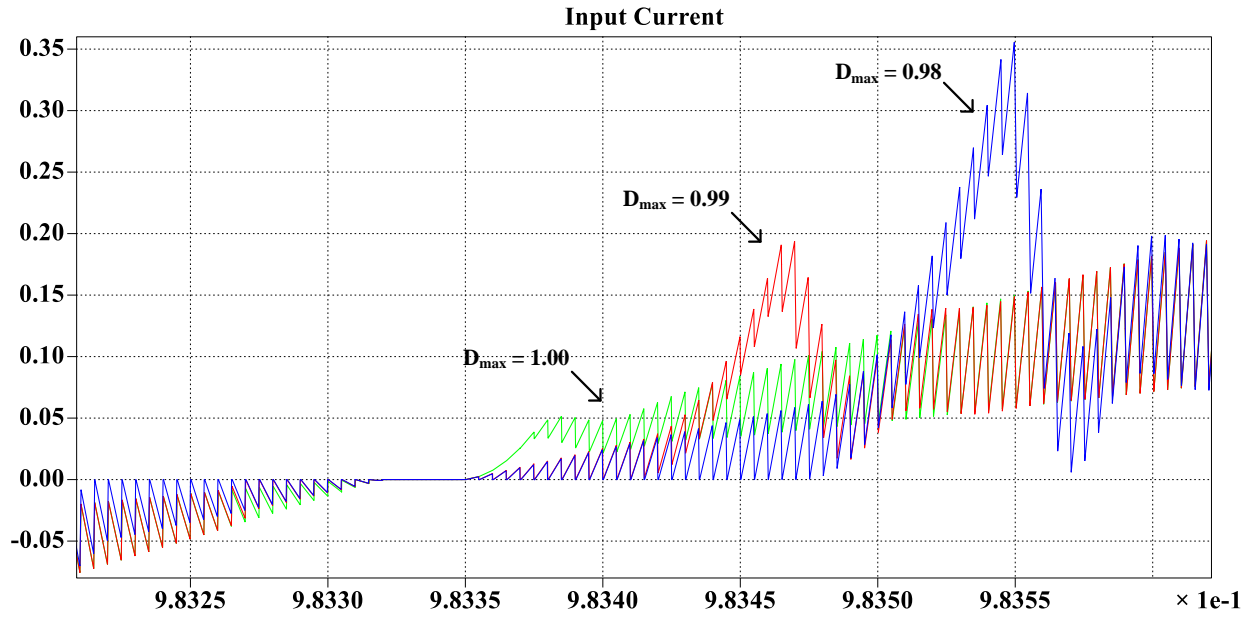


Figure 18. Input Current Overlaid for  $D_{\max} = 0.98$  (Blue), 0.99 (Red), 1.00 (Green)

Table 4. Maximum Duty Cycle Effect on Switch and Input Currents

Dmax	Maximum Peak Switch Current (A)	Input Current THD (%)
1.00	3.88	5.74
0.99	3.75	5.77
0.98	3.39	5.89
0.97	2.94	6.21
0.96	2.52	6.82
0.95	2.36	7.82



Table 4 shows peak switch current and input current THD for several  $D_{\max}$  values. Small changes in  $D_{\max}$  have a large effect on the input current waveform. A limit of 0.95 will cause a current spike that is almost as high as the peak input current.

### 2.2.3 Adding Inductors on Each Half-Bridge Midpoint

The idea of this method is to add inductors with value  $L_m$  to the midpoints of every half-bridge in order to limit the amount of current that can flow between capacitors when they are charging. For small inductors, which are inductors that have an inductance that is smaller than 10% of the inductance of the input inductor, this method will increase the amount of current that flows through the half-bridges and capacitors, which will increase the cost of the system by requiring high current rating devices. For large inductors, which are inductors that have an inductance that is larger than 10% of the inductance of the input inductor, the THD and maximum peak switch current can be improved. This does come at a cost of adding size and cost to the system and may increase the losses by introducing extra parasitic resistance and resonance into the system. The results of several of the tests are shown in Figures 19-24.

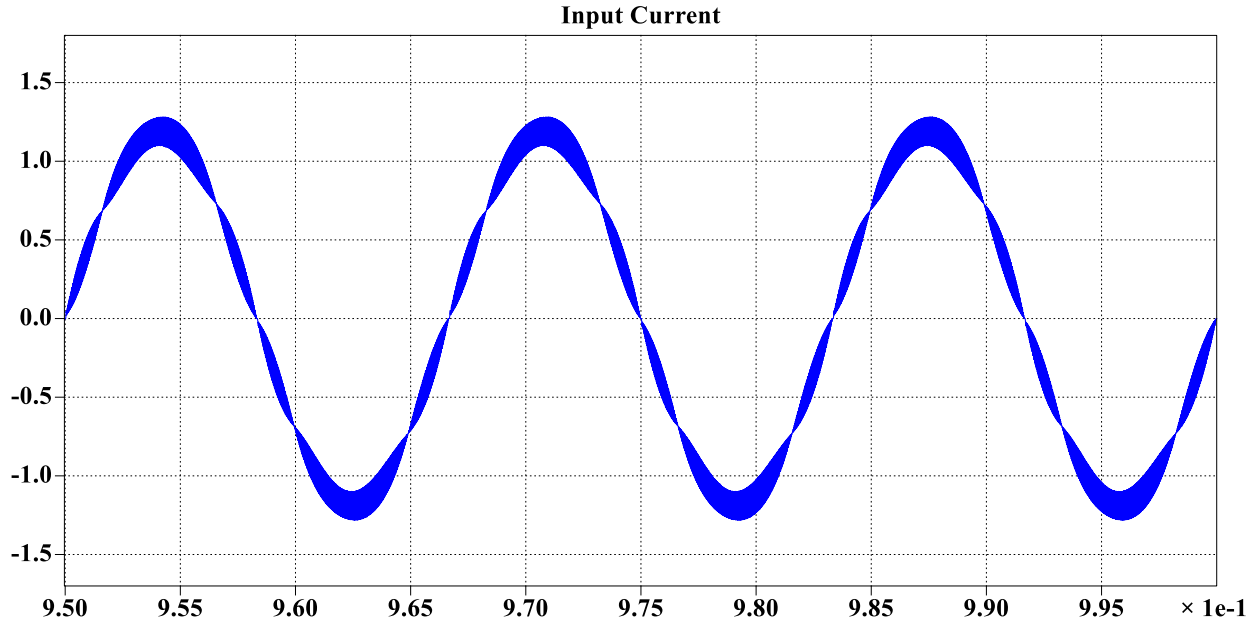


Figure 19. Input Current for  $L_m = 0 \mu\text{H}$

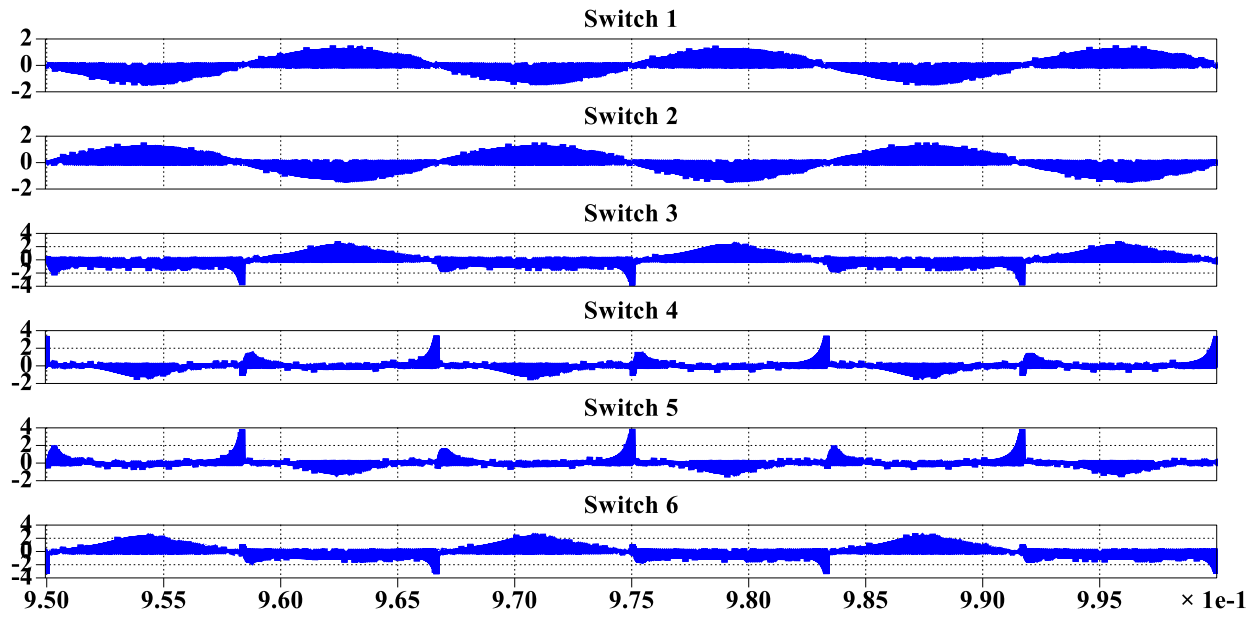


Figure 20. Currents of Switches 1-6 for  $L_m = 0 \mu\text{H}$

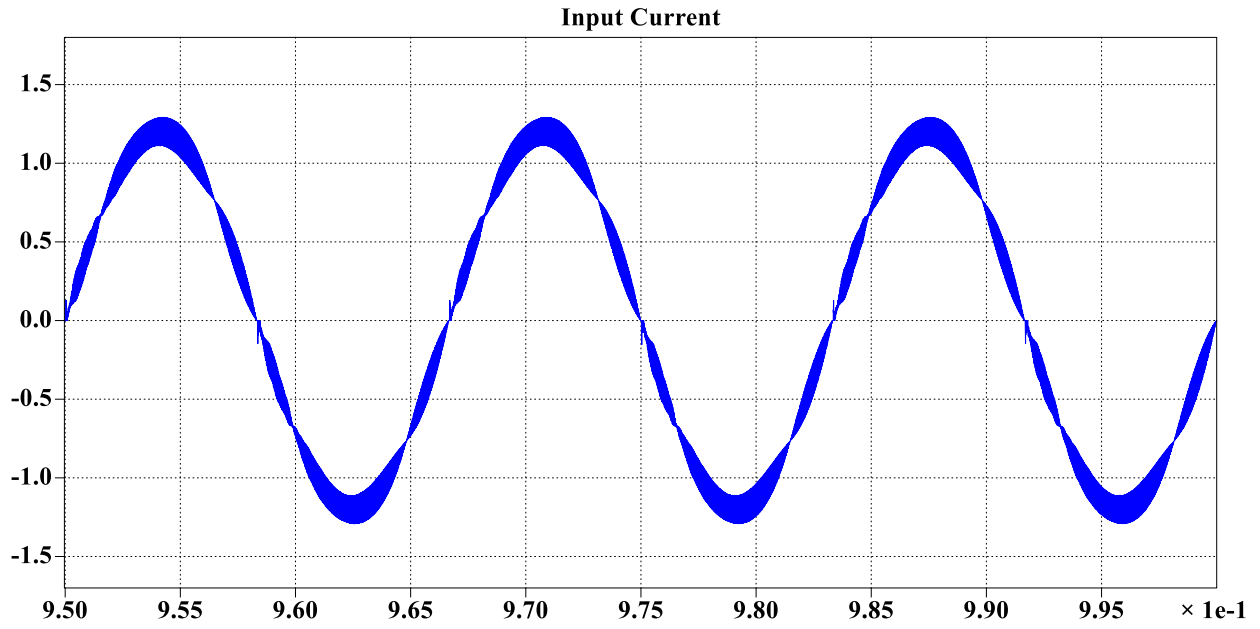


Figure 21. Input Current for  $L_m = 100 \mu\text{H}$

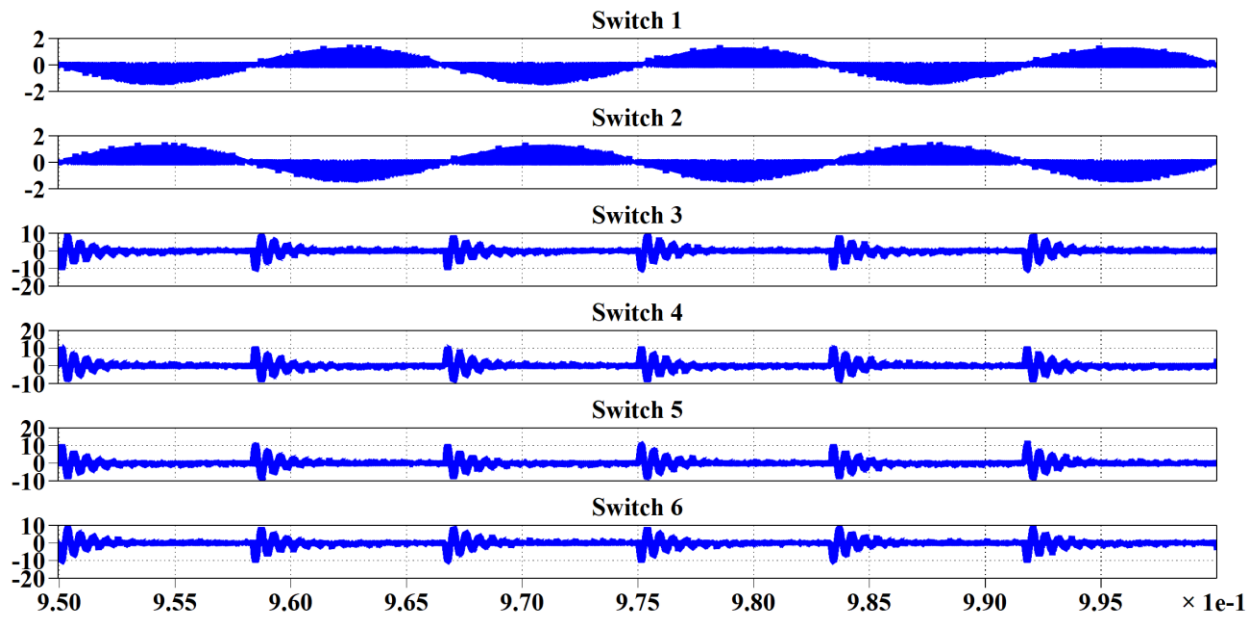


Figure 22. Currents of Switches 1-6 for  $L_m = 60 \mu\text{H}$

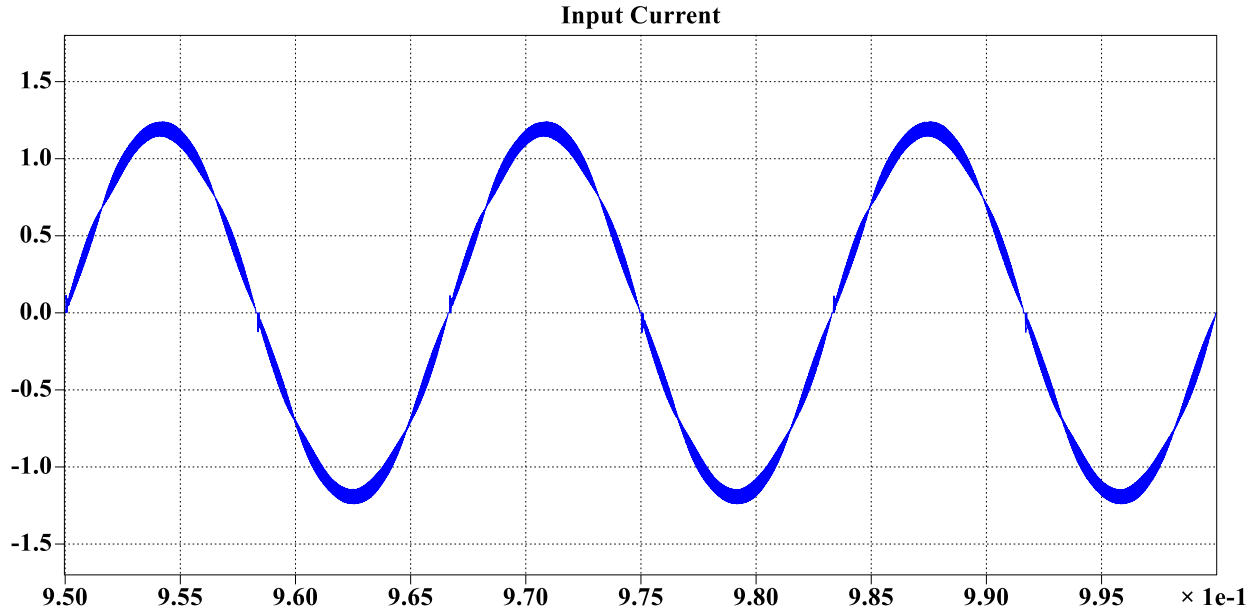


Figure 23. Input Current for  $L_m = 1200 \mu\text{H}$

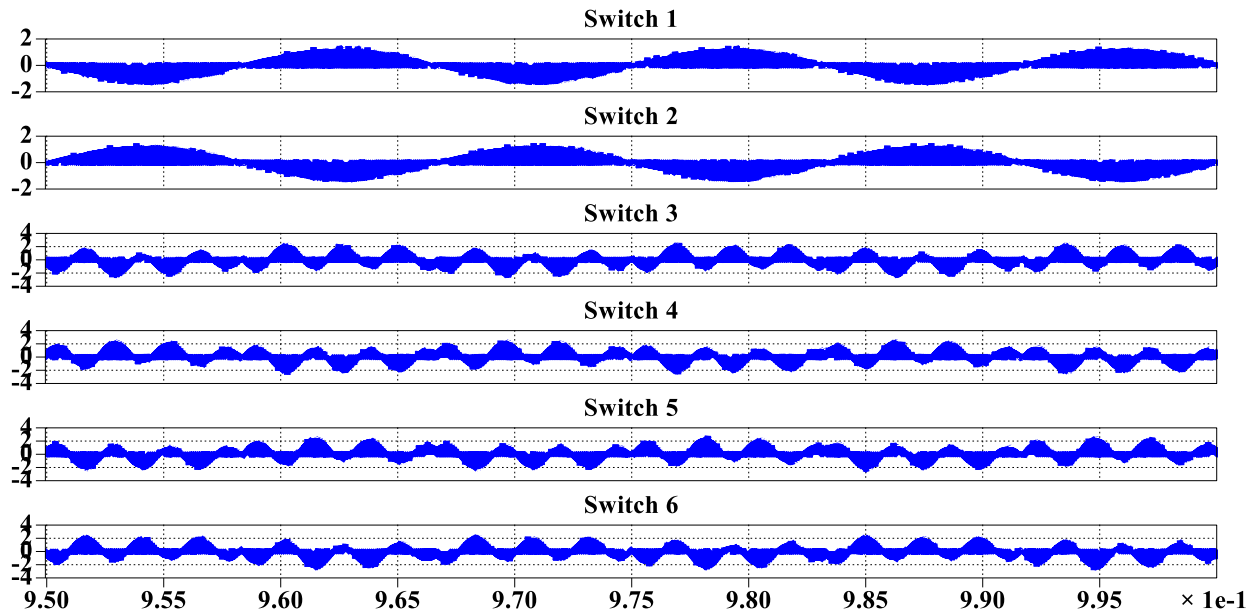


Figure 24. Currents of Switches 1-6 for  $L_m = 1200 \mu\text{H}$

The midpoint inductors appear to have a resonant frequency with the DC-Link capacitors of each half-bridge. If this resonant frequency is well tuned, it may allow for zero voltage switching. However, this will require more investigation. The benefits of adding inductance on the midpoint of each half-bridge do not seem to appear until the inductor becomes very large. Table 5 shows the peak switch current, input current THD, and RMS switch current for several values of  $L_m$ .

Table 5. Midpoint Inductor Effect on Switch and Input Currents

$L_m$ Inductance ( $\mu\text{H}$ / % of L)	Maximum Peak Switch Current (A)	Input Current THD (%)	Maximum RMS Switch Current (A)
0 / 0%	3.86	5.74	0.638
0.6 / 0.1%	14.2	5.68	1.64
30 / 5%	15.2	5.58	1.74
60 / 10%	11.1	5.45	1.73
600 / 100%	6.73	3.90	2.44
1200 / 200%	2.39	2.94	0.863

### 2.3 PI Control Design

Two proportional integral (PI) controllers are necessary to control a PFC topology. The first is the current PI controller, which is fast because it controls the inductor current, which is an AC signal oscillating at the line frequency. The second is the voltage PI controller, which is slow because it controls the output/capacitor voltage, which is a DC signal. The fundamental reason why two PI controllers are needed is because two quantities are being controlled. The reason both

quantities can be controlled by a single control signal (the duty cycle) is because the frequencies of the controllers are very different. [23] gives a detailed explanation of the state equation set up and PI control design.

The purpose of the switching control block is to take a single input, which is the duty cycle for a traditional boost PFC, and output however many switching signals are necessary to control the generalized multilevel PFC. For this reason, the PI controllers for the generalized multilevel PFC are designed in the same manner as the traditional boost PFC controllers with only a few exceptions. The first step to designing PI controllers is to develop the transfer functions from the control input to the variables of interest. The next step is making an educated guess of the PI controller  $k_p$  and  $k_i$  coefficients. The final step is to tune the values in simulation and in hardware.

### 2.3.1 Transfer Functions

The first step to developing transfer functions for the control loops is to develop the state equations. In order to simplify the design process, assumptions are made about the behavior of the control loop across the eight switching states. The first is that the switching states are symmetric for each half of the input voltage sine wave. This is a reasonable assumption because input current and output will affect the inductor voltage and capacitor currents in a very similar manner, although the current will flow through different switches and different capacitors to achieve the same behavior. Another assumption is that the input and output capacitance will be constant for properly sized capacitors. This is reasonable for the output capacitance because every possible connection will give the same capacitance, but the input capacitance will vary. However, this variance does not have a large effect on the control loop and can be accounted for during tuning of the control loop, so it can be ignored. This will allow the control to be simplified to two generic switching states and the same design process can be followed as the traditional boost PFC and using the output of

that controller, the duty cycle can be adjusted by the switching controller to control every switch in the topology.

The first generic switching state is the boost state. The boost state occurs when the switch in the traditional boost PFC is turned on. In this state, the voltage across the inductor is positive and is the absolute value of the input voltage. The value of the input voltage will always be taken as the absolute value, so the notation will be dropped in all equations. The current through the capacitor will be determined by the output voltage and the output resistance. Figure 25 shows the boost state of the boost PFC converter.

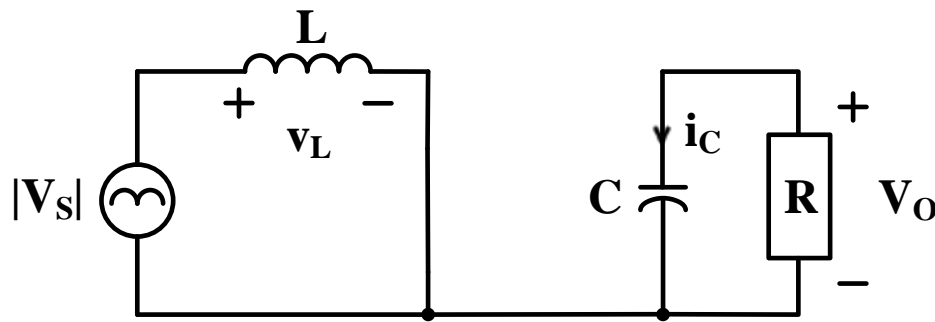


Figure 25. Boost State

$$v_L = v_s = L \frac{di_L}{dt} \quad (1)$$

$$i_C = -\frac{V_o}{R} = C \frac{dv_o}{dt} \quad (2)$$

Equation 1 describes the voltage across the inductor and equation 2 describes the current through the capacitor during the boost state. The value C is determined by the number of levels in

the topology and the actual capacitance value, which will be explained in section 3.2. Figure 26 shows the charge state of the boost PFC converter. The voltage across the inductor in this state is negative and is the difference between the output voltage and the absolute value of the input voltage. The current through the capacitor is the difference between the inductor current and the output voltage over the output resistance.

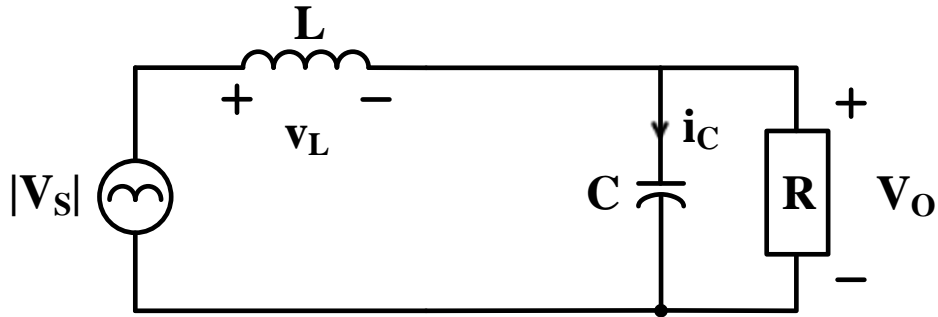


Figure 26. Charge State

$$v_L = v_s - V_o = L \frac{di_L}{dt} \quad (3)$$

$$i_C = i_L - \frac{V_o}{R} = C \frac{dv_o}{dt} \quad (4)$$

Equation 3 describes the voltage across the inductor and equation 4 describes the current through the capacitor during the charge state. From these two sets of equations, two state equation matrices can be set up. The first set of equations, given in equation 5, will describe the system when the switch is on, which will occur for a time  $DT$ , and the second set of equations, given in equation 6, will describe the system when the switch is off, which will occur for a time  $(1 - D)T$ .



$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_s \quad (5)$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1}{L} \\ \frac{1}{C} & \frac{-1}{RC} \end{bmatrix} \begin{bmatrix} i_L \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} v_s \quad (6)$$

Now that these state equations have been developed, they can be dealt with in a more general way. The state variables,  $i_L$  and  $v_o$ , can be grouped into a single vector called  $x$ . Additionally, the matrices scaling the state variables and the input will be renamed  $A$  and  $B$ . These changes are reflected in equations 7 and 8 for equations 5 and 6 respectively.

$$\dot{x} = A_1 x + B_1 v_s \quad (7)$$

$$\dot{x} = A_2 x + B_2 v_s \quad (8)$$

It is readily apparent that  $B_1$  and  $B_2$  are identical, so they will be renamed as  $B$ . The equations can now be combined using the duty cycle ( $d$ ) as the final state variable. This combination is shown in equation 9.

$$\dot{x} = (dA_1 + (1 - d)A_2)x + Bv_s \quad (9)$$

Each state variable and the input can be represented as a constant or “zero order” term and a first order time-varying term. This is because the circuit is assumed to be at a steady-state operating point in order to be controlled. The time-varying terms will be represented as  $\hat{x}$ . This deconstruction is shown in equation 10.

$$\dot{X} + \hat{x} = ((D + \hat{d})A_1 + (1 - (D + \hat{d}))A_2)(X + \hat{x}) + B(V_s + \hat{v}_s) \quad (10)$$

First, the zero order term of the derivative of the state variables will be zero because the derivative of a constant is zero. Next, the terms will be sorted into zero order, first order, and second order based on how many first order terms are present in each multiplication. Zero order

terms are in equation 11, first order terms are in equation 12, and second order terms are in equation 13.

$$0 = (DA_1 + (1 - D)A_2)X + BV_s \quad (11)$$

$$\hat{x} = (DA_1 + (1 - D)A_2)\hat{x} + B\hat{v}_s + (A_1 - A_2)X\hat{d} \quad (12)$$

$$0 = (A_1 - A_2)\hat{d}\hat{x} \quad (13)$$

First order terms are much smaller than constant value terms by assumption, so the second order terms that consist of two first order term multiplied together will be much smaller than all other terms and can be ignored. Additionally, all zero order terms are constant when the circuit is operating in steady-state and will not contribute to the differential equation and thus can be ignored. However, the DC operating point will occur when the DC terms are equal to zero, so equation 11 can be used to solve for the steady-state operating values of the state variables and this is done in equation 14. Finally, the matrices multiplying the state variable matrix and the duty cycle are renamed in equation 15.

$$X = [(DA_1 + (1 - D)A_2)]^{-1}BV_s \quad (14)$$

$$\hat{x} = A\hat{x} + B\hat{v}_s + K\hat{d} \quad (15)$$

Finally, these values can be arranged into transfer functions. The transfer function from the input voltage to the state variables can be found by taking the Laplace transform of equation 15, setting the small signal duty cycle to zero, and solving for the small signal state variables divided by the small signal input voltage. This solution is given in equation 16 and the transfer two transfer functions derived are shown in equations 17 and 18, where  $s$  is the Laplace variable in the frequency domain.

$$\left. \frac{\hat{x}}{\hat{v}_s} \right|_{\hat{d}=0} = (sI - A)^{-1}B \quad (16)$$

$$\frac{\hat{i}_L}{\hat{v}_s} = \frac{\frac{1}{L} \left( s + \frac{1}{RC} \right)}{s^2 + \left( \frac{1}{RC} \right) s + \frac{(1-D)^2}{LC}} \quad (17)$$

$$\frac{\hat{v}_o}{\hat{v}_s} = \frac{\frac{1}{LC} (1-D)}{s^2 + \left( \frac{1}{RC} \right) s + \frac{(1-D)^2}{LC}} \quad (18)$$

The transfer function from the duty cycle to the state variables can be found by again taking the Laplace transform of equation 15, setting the small signal input voltage to zero, and solving for the small signal state variables divided by the small signal duty cycle. This solution is given in equation 19 and the transfer two transfer functions derived are shown in equations 20 and 21, where  $s$  is the Laplace variable in the frequency domain.

$$\left. \frac{\hat{x}}{\hat{d}} \right|_{\hat{v}_s=0} = (sI - A)^{-1}K \quad (19)$$

$$\frac{\hat{i}_L}{\hat{d}} = \frac{\frac{V_s}{L(1-D)} \left( s + \frac{2}{RC} \right)}{s^2 + \left( \frac{1}{RC} \right) s + \frac{(1-D)^2}{LC}} \quad (20)$$

$$\frac{\hat{v}_o}{\hat{d}} = \frac{\frac{-V_s}{RC(1-D)^2} \left( s - \frac{R(1-D)^2}{L} \right)}{s^2 + \left( \frac{1}{RC} \right) s + \frac{(1-D)^2}{LC}} \quad (21)$$

The transfer functions given in equations 17, 18, 20, and 21 will be used in the next sections to build the control loop model and design the PI controller constants.

### 2.3.2 Current and Voltage Loops

The current control loop is the faster of the two control loops. One of the assumptions made above was that the small signal values were oscillating about a DC operating point, but the current is tracking an AC signal. Therefore, it must be very fast so that the 60 Hz AC signal appears to be a DC signal to the controller. However, the control loop also cannot be so fast that it adjusts that

control value significantly between switching times. A general rule of thumb for the designing the current control loop is that the crossover frequency of the closed loop control should be less than 10% of the switching frequency, which is usually several magnitudes higher than the line frequency of 60 Hz [23]. The current control loop block diagram is shown in Figure 27.

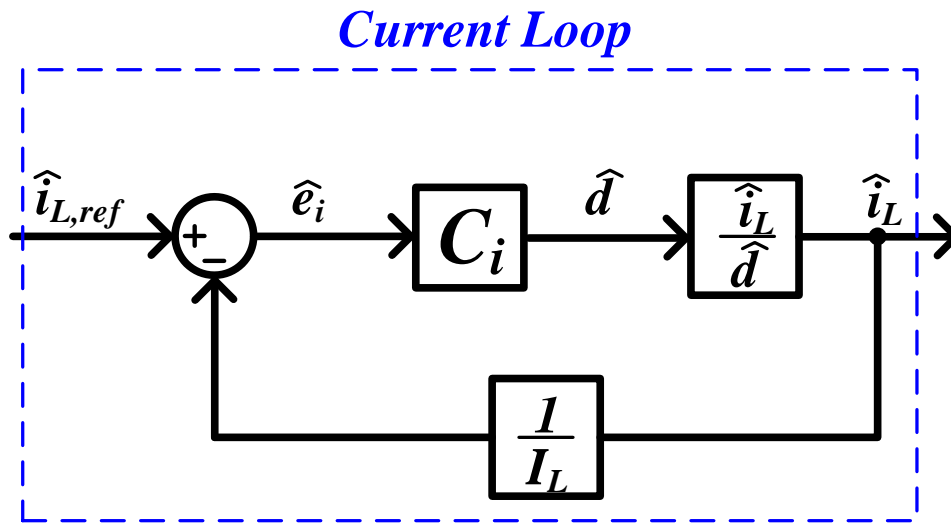


Figure 27. Current Control Loop

The reference inductor current ( $\hat{i}_{L,ref}$ ) is the input into the controller and must be generated by tracking the input voltage. Subtracting the normalized inductor current ( $\hat{i}_L/I_L$ ) from the reference gives the current error ( $\hat{e}_i$ ), which is the input to the current PI controller ( $C_i$ ). The output of the PI controller then goes to the circuit, which is modeled by the transfer function given in equation 20, which was developed in the previous section. The PI controller is designed to keep

the error as close to zero as possible. The general equation for a PI controller is given in equation 22.

$$C = \frac{k_p s + k_i}{s} \quad (22)$$

If  $k_p$  is factored out, then it is clear that the equation has one pole at zero and one zero at  $-k_i/k_p$  and a DC gain of  $k_p$ . The DC gain and the zero value must be set to force the gain of the closed-loop control to be unity until the crossover frequency and force the crossover frequency to be significantly more than the line frequency but less than 10% of the switching frequency.

The voltage control loop is the slower of the two loops and is the outer loop. The voltage controller must be much slower than the current controller or the two loops will interfere with each other. The voltage control loop can be as slow as desired, but the crossover frequency is usually less than 10% of the current control loop crossover frequency. The overall control loop is shown in Figure 28.

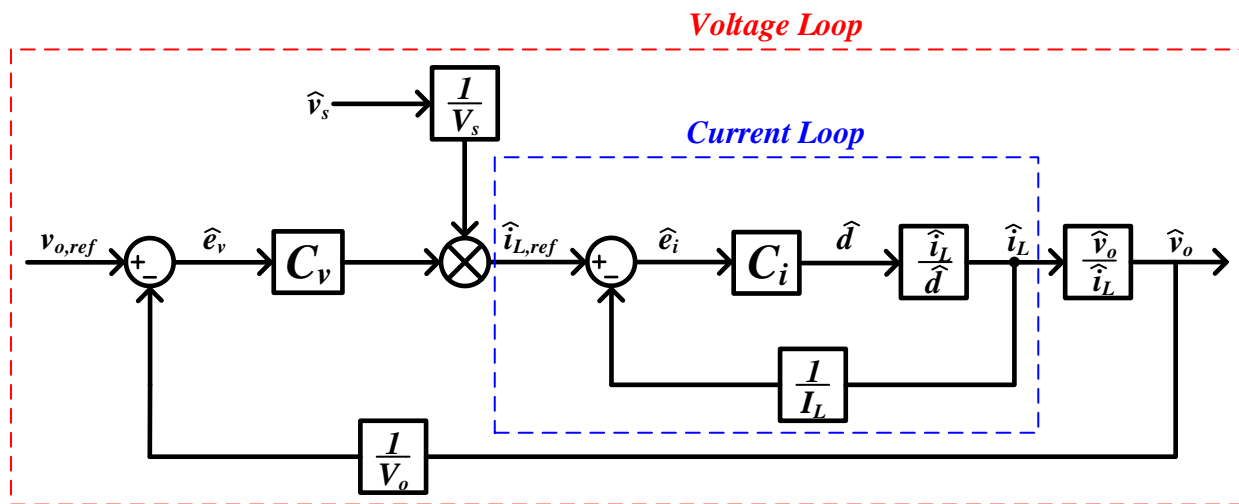


Figure 28. Overall Control Loop

The reference output voltage ( $v_{o,ref}$ ) is a constant value that is set to 1 in this case to achieve the steady-state output voltage. The normalized output voltage ( $\hat{v}_o/V_o$ ) is subtracted from the reference to give the voltage error ( $\hat{e}_v$ ), which is the input to the voltage PI controller ( $C_v$ ). The output of the voltage PI controller is then multiplied by the normalized input voltage ( $\hat{v}_s/V_s$ ) to generate the reference inductor current. This value is then fed into the current control loop and the output of the current control loop is fed into another transfer function that models the physical circuit. This transfer function was not developed in the previous section but can easily be derived by dividing equation 18 by equation 17 or by dividing equation 21 by equation 20. The resultant transfer function is given in equation 23.

$$\frac{\hat{v}_o}{\hat{i}_L} = \frac{\frac{1}{C} (1 - D)}{s + \frac{1}{RC}} \quad (23)$$

### 2.3.3 Designing PI Controllers

The circuit modeling equations require knowledge of the passive component values, the input and output voltage, and the effective load resistance. The design guide in section 3 will describe how these values should be designed. This section will describe the design goals of the PI controllers and how to properly design them.

The current control loop should be designed first. The current controller is the inner loop and must have a very high crossover frequency as mentioned in previous sections. The goal of the current loop PI controller is forcing the gain of the closed loop system to be very close to unity until the crossover frequency, which should also be set by the PI controller. The open loop transfer function is shown in Figure 29.

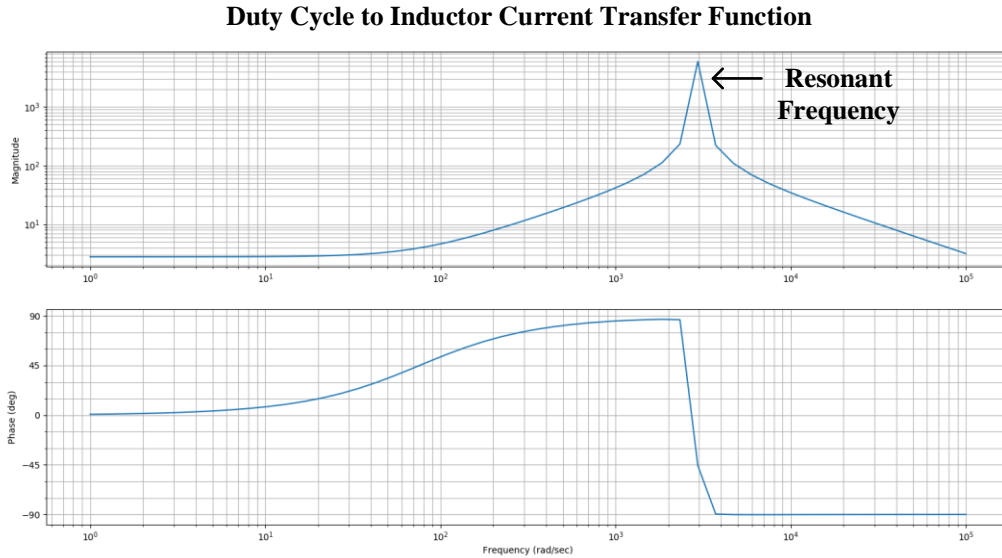


Figure 29. Duty Cycle to Inductor Current Transfer Function

The transfer function from duty cycle to inductor current has one zero and two poles, which means the end behavior will be a single pole because the zero and one pole will cancel out. All poles and zeroes are on the Left-Hand Plane (LHP). However, before this end behavior is reached, there is a resonant frequency which for this circuit occurs around 3 kHz. The PI controller should cancel this resonant frequency and bring the corner frequency to around 20 kHz. This can be achieved by setting the absolute value of the multiplication of the transfer function and the controller equation evaluated at the desired corner frequency to one and solving for  $k_i$  and  $k_p$  values that will satisfy this requirement.

First, the equality constraint is given in equation 24, where  $C(j\omega_c)$  and  $P(j\omega_c)$  are the controller function and transfer function evaluated at the corner frequency. This constraint will cause the closed loop transfer function to be  $\frac{1}{2}$  at the desired corner frequency.

$$|P(j\omega_c)C(j\omega_c)| = 1 \quad (24)$$

Next, the equality can be re-written with the controller equation expanded, as in equation 25, and then solved for  $k_p$  as in equation 26.

$$k_p^2 + \left(\frac{k_i}{\omega_c}\right)^2 = \frac{1}{|P(j\omega_c)|^2} \quad (25)$$

$$k_p = \sqrt{\frac{1}{|P(j\omega_c)|^2} - \frac{k_i^2}{\omega_c^2}} \quad (26)$$

The  $\omega_c$  term dividing the  $k_i$  term comes from the  $s$  term in the controller function. When taking the absolute value of the controller function or the transfer function, the imaginary and real parts are found separately and added using the sum of squares. Finally,  $k_p$  is found as a function of  $k_i$ . This function can be plotted for many values of  $k_i$  and this plot is shown in Figure 30 for  $k_i$  from 0 to 50,000 (or 50k). This plot describes the combined  $k_p$  and  $k_i$  that will result in a corner frequency of  $\omega_c$ . If  $k_i$  is set to a value above 50k or below 0, there will not be a  $k_p$  value that will set the corner frequency at the desired value of 20 kHz. The goal of setting  $k_i$  is to be within these limits and find a value that minimizes THD on the input current, which will be achieved by balancing response time with overshoot on the closed loop step response.



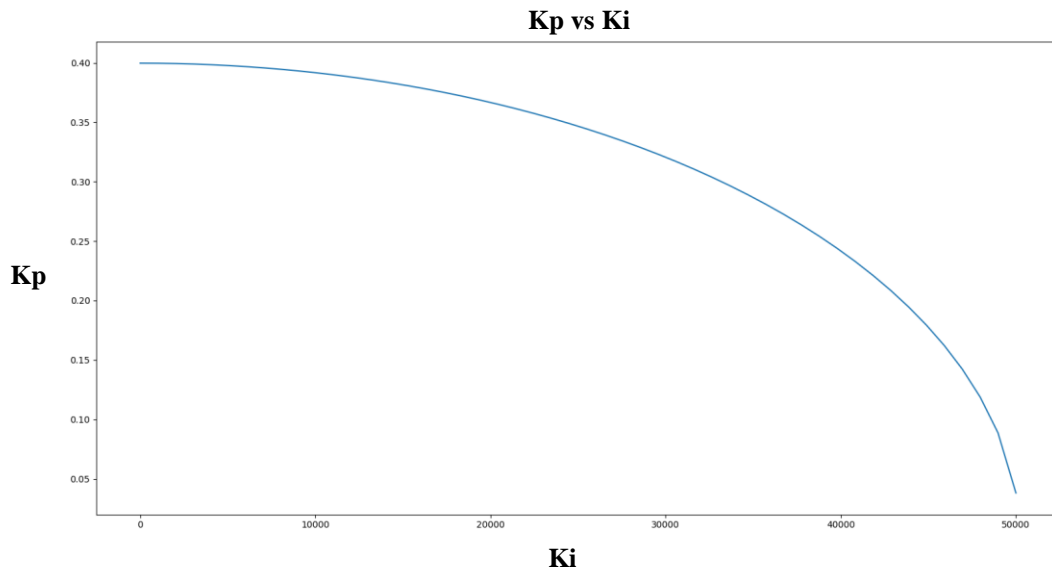


Figure 30.  $k_p$  vs  $k_i$

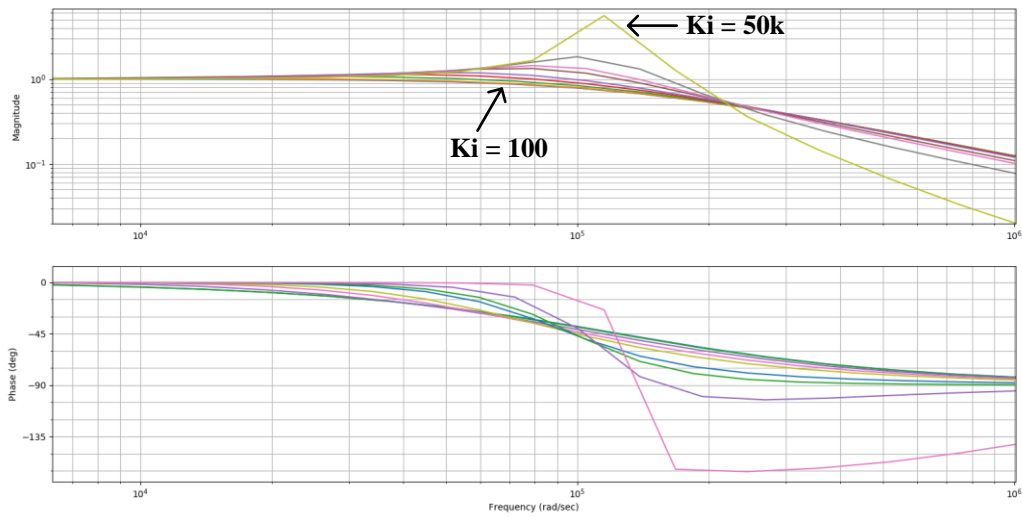


Figure 31. Magnitude (Top) and Phase (Bottom) Bode Plots for  $k_i = 100, 1k, 5k, 10k, 15k, 25k, 30k, 40k, 50k$

Figure 31 shows magnitude and phase bode plots for values across the spectrum of possible  $k_i$  values. As  $k_i$  increases to 50k, the resonance on the magnitude bode around the corner frequency increases substantially and unity gain crossing also increases somewhat, although it will still be reasonably close to the corner frequency. As  $k_i$  decreases to 100, there is no resonance around the corner frequency, however, the unity gain crossing frequency occurs much earlier, which will significantly slow the response of the control loop.

Next, the most extreme options will be eliminated and  $k_i$  values of 10k, 15k, 25k, and 30k with  $k_p$  values calculated using equation 26 will be used to plot a step response as shown in Figure 32.

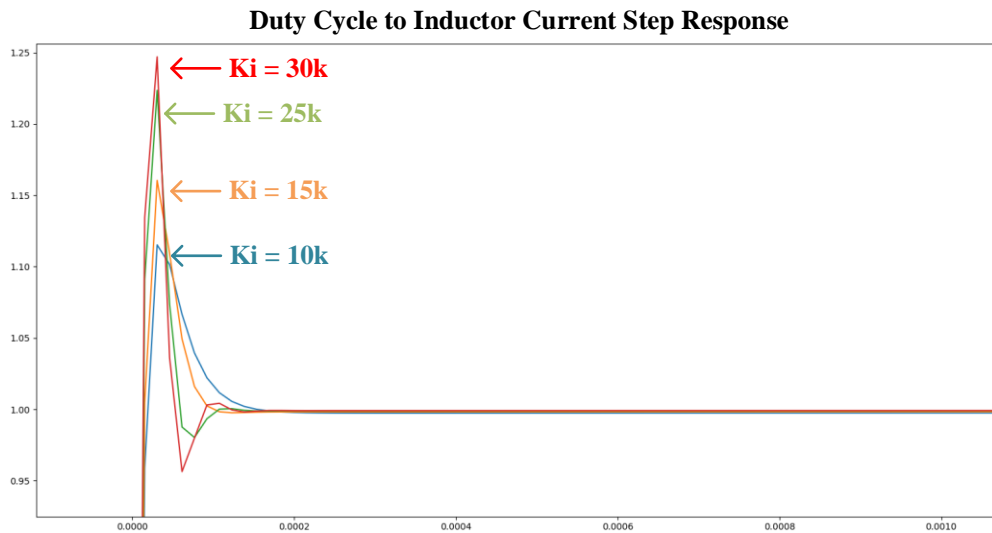


Figure 32. Duty Cycle to Inductor Step Response for  $k_i = 10k, 15k, 25k, 30k$

The step responses of the  $k_i$  values plotted have an increased overshoot as  $k_i$  increases and have a faster response time as  $k_i$  increases. In order to select the optimal value, the values will need to be tuned in simulation software. This will be carried out in the next section.

The voltage PI values are designed in a similar manner, however, because there is no speed requirement for the voltage controller, the crossover frequency will be designed for 2 kHz and the  $k_i$  value is chosen to be a value that has no overshoot. The step response of the chosen  $k_i$  value of 25 is shown in Figure 33.

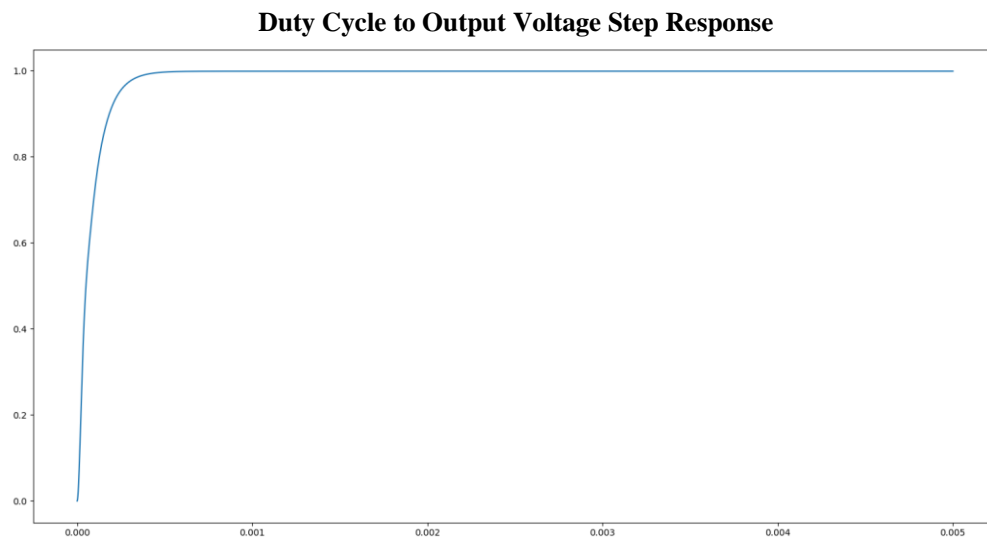


Figure 33. Duty Cycle to Output Voltage Step Response

### 2.3.4 Tuning

Using the  $k_i$  values selected from the previous section, several simulations are run with different current PI controller values to assess their performance and shown in Figure 34. For  $k_i$  values of 25k and 30k, the values are almost identical, and they are very difficult to distinguish on the graph, which means our final value can be somewhere between these values. The lower frequency values appear to have a response time that is too slow, which results in an inductor current ripple that is almost twice the value of the optimal inductor current ripple. For reference,  $k_i$  values of 100 and 50k are plotted against the optimal  $k_i$  value of 25k in Figure 35. If  $k_i$  is increased to 50k, then the overshoot and ringing will cause a large amount of ripple. However, if  $k_i$  is reduced to 100, the current ripple will still increase, but will increase because of the slow tracking speed of the PI controller, which will cause lower frequency oscillations.

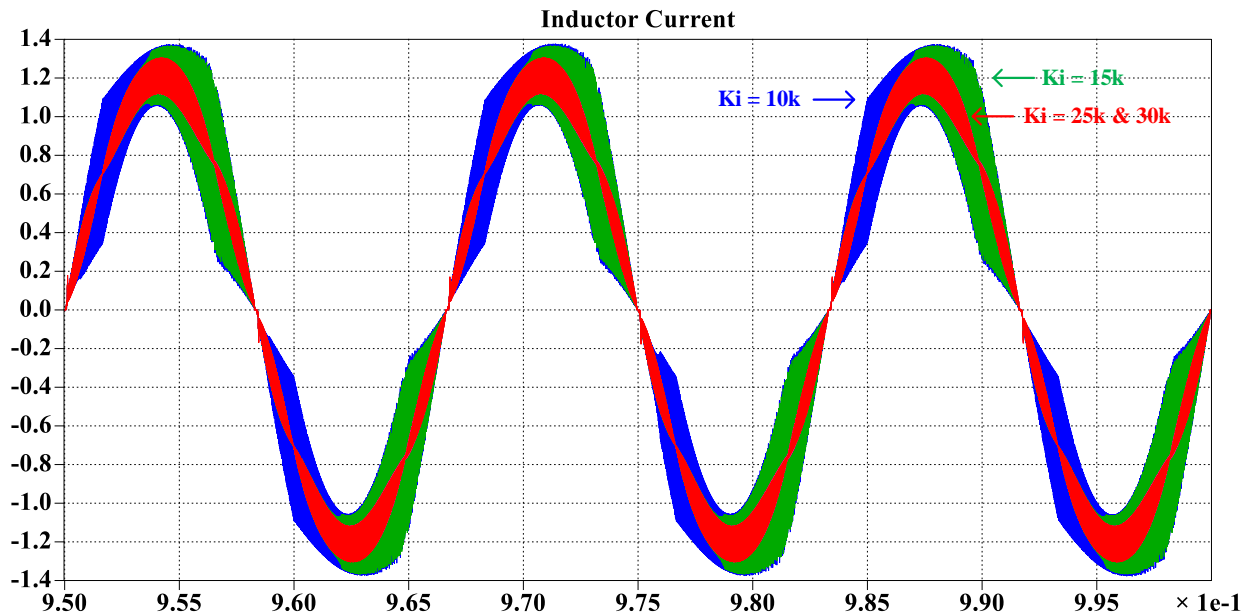


Figure 34. Circuit Simulation Inductor Current for Various  $k_i$  Values

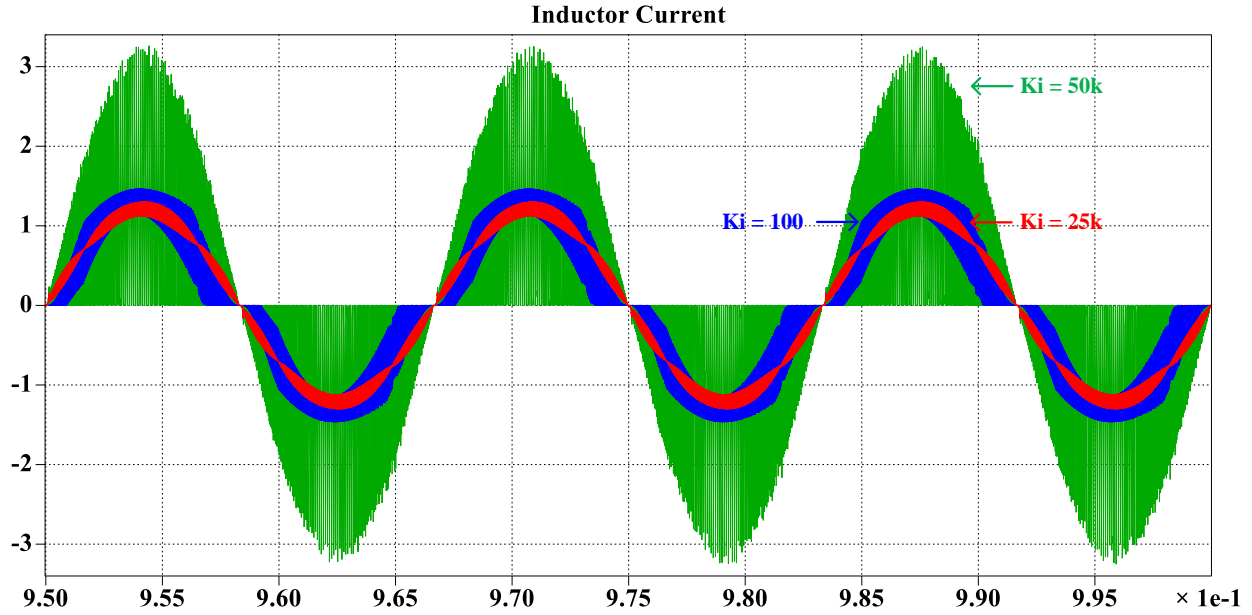


Figure 35. Circuit Simulation Inductor Current for  $k_i = 100, 25k, 50k$

The python code used to design the PI controllers for the current and voltage loops and generate the graphs included in this section is included in the appendix.

## 2.4 Switching Control Design

This section describes the function and design of the switching controller. The switching controller takes the duty cycle control signal from the PI controller and the input voltage as an input and outputs PWM switching signals for each switch in the topology. The design of this controller design is modular and can be scaled up to higher level topologies. Both 5-level and 3-level topologies are used as examples throughout the section. This section also describes the logic that allows the effective switching frequency to be doubled for inductor current.

### 2.4.1 Switching Controller

The first step in the control design is to recognize that for an  $n$ -level topology, there will only be  $n$  distinct switching signals and their complements. This is because all half-bridges on a single leg will be controlled in the exact same manner. With  $n$  binary switching signals, there are  $2^n$  possible switching combinations. Several of these possible switching combinations result in the same voltage being produced across  $V_{AC}$ . A 3-level topology with both legs labeled is shown in Figure 36.

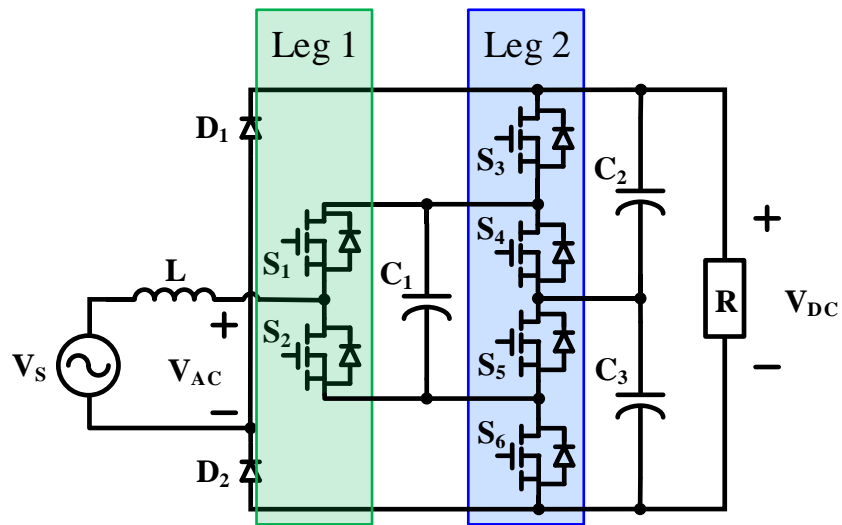


Figure 36. 3-Level Proposed Topology with Legs Labeled

Leg one contains  $S_1$  and  $S_2$ .  $S_1$  and  $S_2$  will be controlled in opposition, which means if the state of  $S_1$  is known, then the state of  $S_2$  will be known. This means that the state of the first leg can be entirely described by  $S_1$ . Leg two contains  $S_3$ ,  $S_4$ ,  $S_5$ , and  $S_6$ . If the state of  $S_3$  is known,

then  $S_4$  and  $S_6$  will have the opposite state and  $S_5$  will have the same state. This means that the state of the second leg can be entirely described by  $S_3$ . Table 6 shows the voltages across  $V_{AC}$ , the switching states which occur, and the zones of operation for each leg state depending on whether  $V_S$  is positive or negative.

Table 6. Switching States, Zones of Operation, and Voltages Based on Leg States for a 3-Level Topology

Leg States ( $S_1, S_3$ )	$V_{AC}$ ( $+V_S, -V_S$ )	States ( $+V_S, -V_S$ )	Zones ( $+V_S, -V_S$ )
(0, 0)	0 V, $-V_{DC}$	1, 5	1, 4
(0, 1)	$\frac{1}{2} V_{DC}, -\frac{1}{2} V_{DC}$	2, 6	1, 2, 3, 4
(1, 0)	$\frac{1}{2} V_{DC}, -\frac{1}{2} V_{DC}$	3, 7	1, 2, 3, 4
(1, 1)	$V_{DC}, 0$ V	4, 8	2, 3

Therefore, in order to know which leg state must be used, the sign of the input voltage must be known. To simplify the discussion, the binomial term  $a$  will be used to describe if the input voltage is greater than zero and  $\bar{a}$  will be used to describe the complement. Next, a term will be needed to determine if adjusted duty cycle ( $d'$ ) is more than  $1/(n - 1)$ . This term will normally indicate the positive input voltage operating region and will limit the current spike that results from transitioning between regions. This term will be called  $b$  and its complement will be called  $\bar{b}$ . Finally, a regression term will be used to track the duty cycle input from the PI controller. This term will be called  $c$  and its complement will be called  $\bar{c}$ . The duty cycle must be modified slightly

so that that it is kept between 0 and  $1/(n - 1)$ . This is because of the frequency doubling feature of the topology, which will cause each switch to be active for  $1/(n - 1)$  of the duty cycle which will result in the same effective duty cycle. The block diagram of the part of the controller that generates these terms is given in Figure 37.

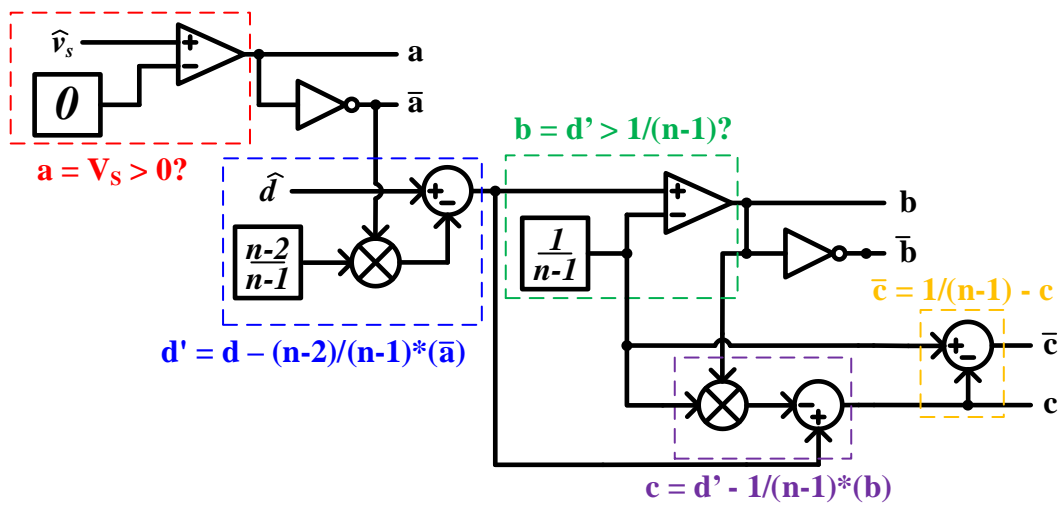


Figure 37. Switching Control Logic Term Generation Block Diagram for an n-Level Topology

Using the terms generated by the logic term generation, a pseudo-logic gate network is built that sets the proper duty cycle value for input to a PWM block. This logic network is given in Figure 37. It should be noted that the PWM carrier should have a maximum value of  $1/(n - 1)$  and a minimum value of 0. Each group of AND gates has at least one regression term. Due to this fact, the logic gates cannot be binary logic gates, or they would discard the continuous value of



the regression term and output a binary value. Therefore, the AND gates are in fact multiplication gates and the OR gates are in fact addition gates.

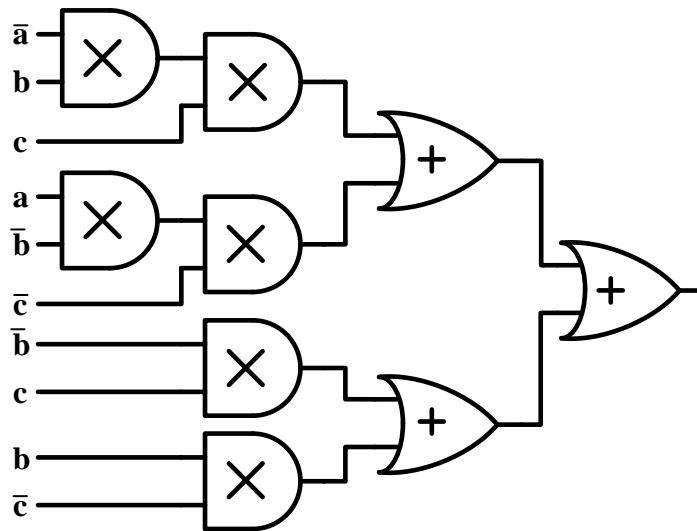


Figure 38. Switching Control Logic Block Diagram for an n-Level Topology

Finally, these logic gates are feed to a PWM block that consists of a triangular carrier oscillating at the switching frequency and a comparator that compares the PWM input to the carrier. The same logic is used to generate the PWM input value for all leg states in the topology. However, the PWM carriers are each offset  $360/(n - 1)$  degrees from each other. This offset results in a multiplication of the effective switching frequency of the topology as described in the following section.

## 2.4.2 Multiplying Effective Switching Frequency

The fundamental reason why the effective switching frequency of the topology is  $(n - 1)$  times higher than the switching frequency of each half-bridge is due to the  $360/(n - 1)$  offset of the PWM carriers for each leg state signal. This offset results in the voltage across  $V_{AC}$  changing at  $(n - 1)$  times the switching frequency, which results in the inductor current ripple having a frequency of  $(n - 1)$  times the switching frequency.

Table 7. Leg States and  $V_{AC}$  Voltages for a 5-Level Topology

Leg States ( $S_1, S_3, S_7, S_{11}$ )	$V_{AC}$ ( $+V_S, -V_S$ )
(0, 0, 0, 0)	0 V, $-V_{DC}$
(0, 0, 0, 1), (0, 0, 1, 0), (0, 1, 0, 0), (1, 0, 0, 0)	$\frac{1}{4} V_{DC}, -\frac{3}{4} V_{DC}$
(0, 0, 1, 1), (0, 1, 0, 1), (1, 0, 0, 1), (0, 1, 1, 0), (1, 0, 1, 0), (1, 1, 0, 0)	$\frac{1}{2} V_{DC}, -\frac{1}{2} V_{DC}$
(0, 1, 1, 1), (1, 0, 1, 1), (1, 1, 0, 1), (1, 1, 1, 0)	$\frac{3}{4} V_{DC}, -\frac{1}{4} V_{DC}$
(1, 1, 1, 1)	$V_{DC}, 0$ V

For a topology of any level, there will be many redundant states to produce a single fractional voltage level across  $V_{AC}$ . Table 7 lists the leg states and the associated voltage levels for

a 5-level topology. As for the 3-level topology, there are  $n - 1$  leg states that produce each fractional voltage across  $V_{AC}$ . This means that each state can be turned on  $1/2$  of the time required to achieve the set duty cycle. Additionally, each fractional voltage level can be enabled using a separate leg state signal, which means if all switches are operating at a frequency of  $f_{sw}$ , then  $V_{AC}$  changes at a rate of  $(n - 1)f_{sw}$ .

In order to achieve the frequency multiplication, the effective duty cycle that is input to the PWM blocks must remain between 0 and  $1/(n - 1)$ . This is achieved by offsetting the PWM blocks and allowing the PI controller to automatically adjust the required duty cycle values.

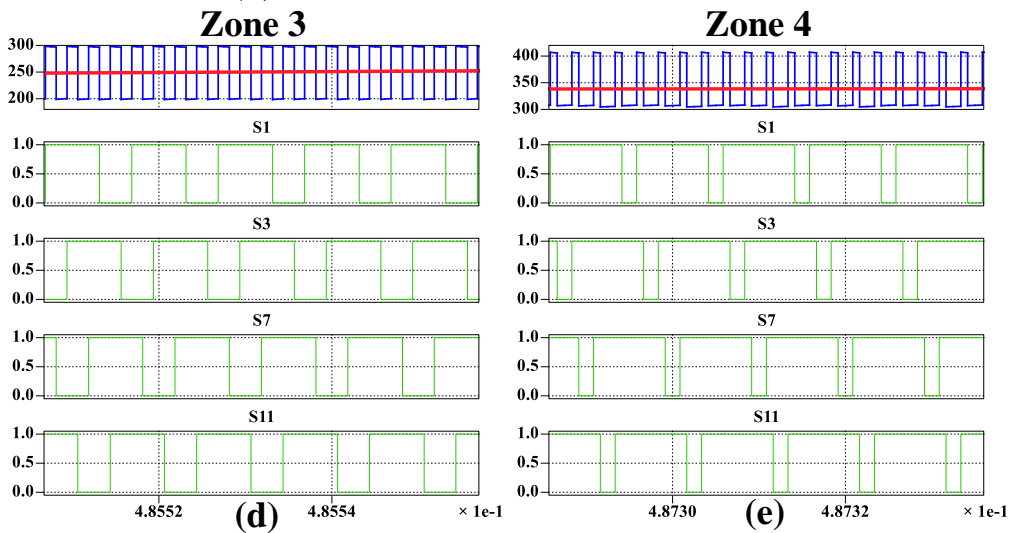
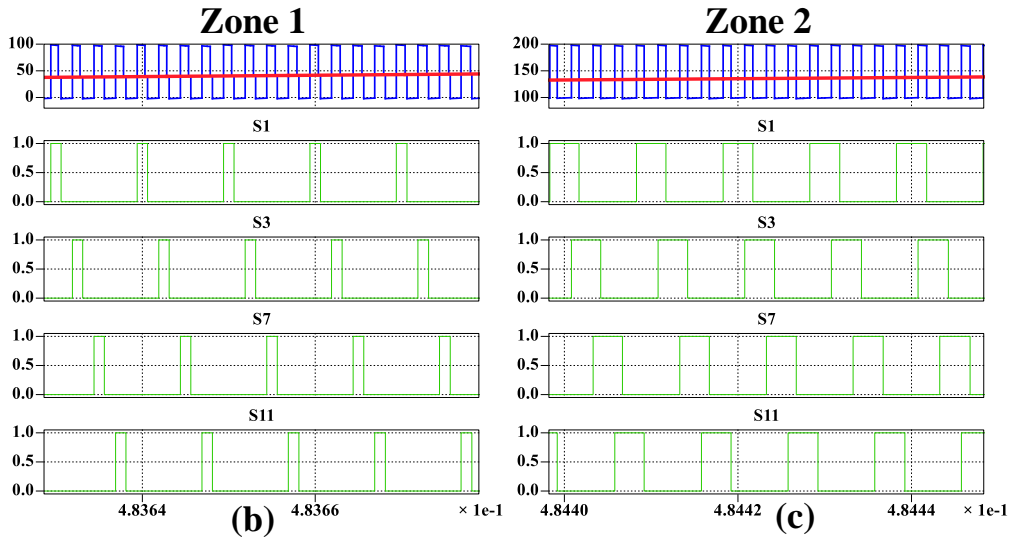
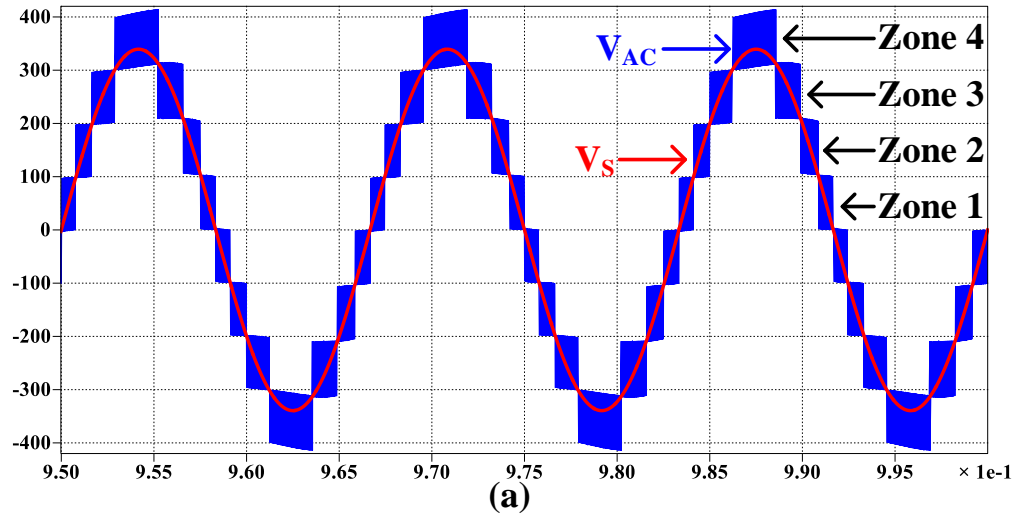
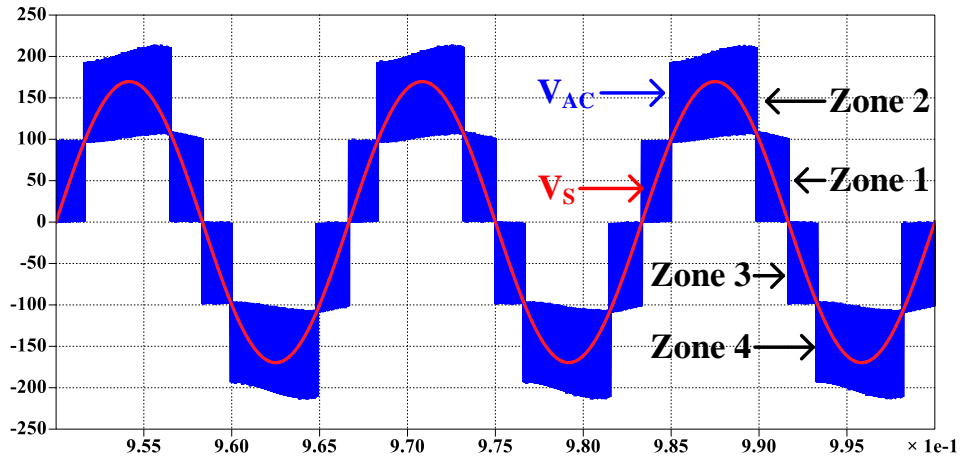


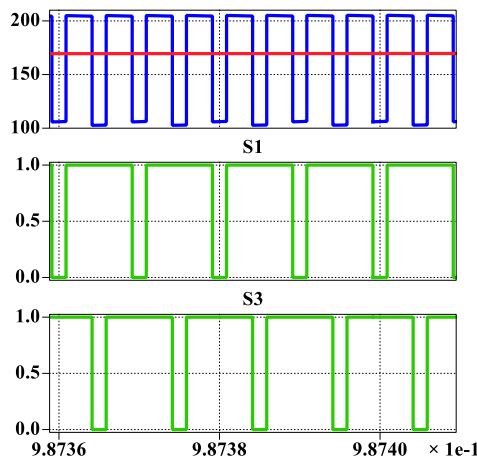
Figure 39.  $V_S$  and  $V_{AC}$  and Operating Zones for a 5-Level Topology

Figure 39(a) shows the input voltage ( $V_S$ ) and  $V_{AC}$  and identifies the operating zones of the circuit. Figures 39(b, c, d, e) show a zoomed view of the leg signals in each operating zone and corresponding  $V_{AC}$  changes. The zones of operation can roughly be split up based on how many leg signals are overlapping, or on at the same time. In zone 1, shown in Figure 39(b), no leg signals are on at the same time and the leg states shown in row 1 and 2 of Table 7 are used to generate the desired duty cycle. Additionally,  $V_{AC}$  switches at a rate of 4 times the rate of each individual leg signal. In zone 2, shown in Figure 39(c), at least one leg signal is on at all times and  $V_{AC}$  is in a high state when multiple leg signals are overlapping. In zone 3, shown in Figure 39(d), at least two signals are on at all times and  $V_{AC}$  is high when three signals are on at the same time. This means that leg states shown in rows 3 and 4 of Table 7 are used to generate the  $V_{AC}$  voltages. Finally, in zone 4, shown in Figure 39(e), there are always at least three leg signals active and the image can be viewed as the inverse of the zone 1. This is because instead of no leg signals being on at the same time as in zone 1, no leg signals will be off at the same time. Figure 40 shows a similar figure for a 3-level topology.



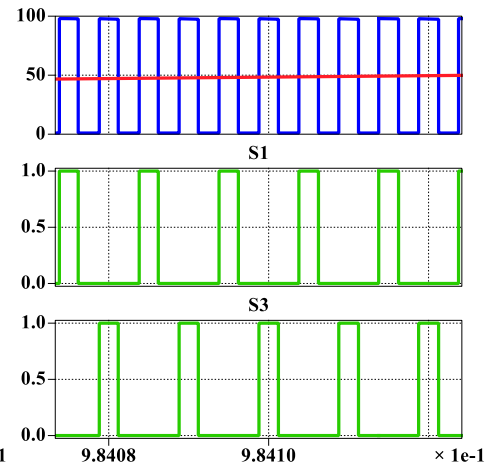
(a)

**Zone 1**



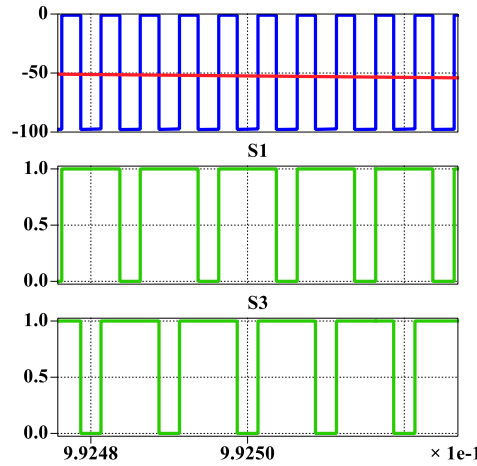
(b)

**Zone 2**



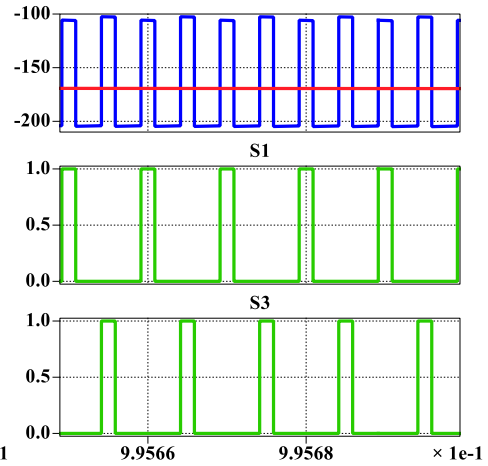
(c)

**Zone 3**



(d)

**Zone 4**



(e)

Figure 40.  $V_S$  and  $V_{AC}$  and Operating Zones for a 3-Level Topology

## 2.5 Simulation Results

In this section, the topology will be tested in simulation. Two variants of the topology will be tested which are the 3-level and 5-level versions. The first set of tests will examine the effect of changing the load suddenly, often called a “load step”. The test will be conducted with low to high load step and a high to low load step for both versions. The second set of tests will examine the effect of changing the input voltage suddenly, often called a “voltage spike” or “voltage sag”.

### 2.5.1 Changing Load Conditions

The first tests are performed on the 3-level topology. The load is step from full load, which is 100W in this case, to half load, which is 50W in this case. The results are shown in Figure 41.

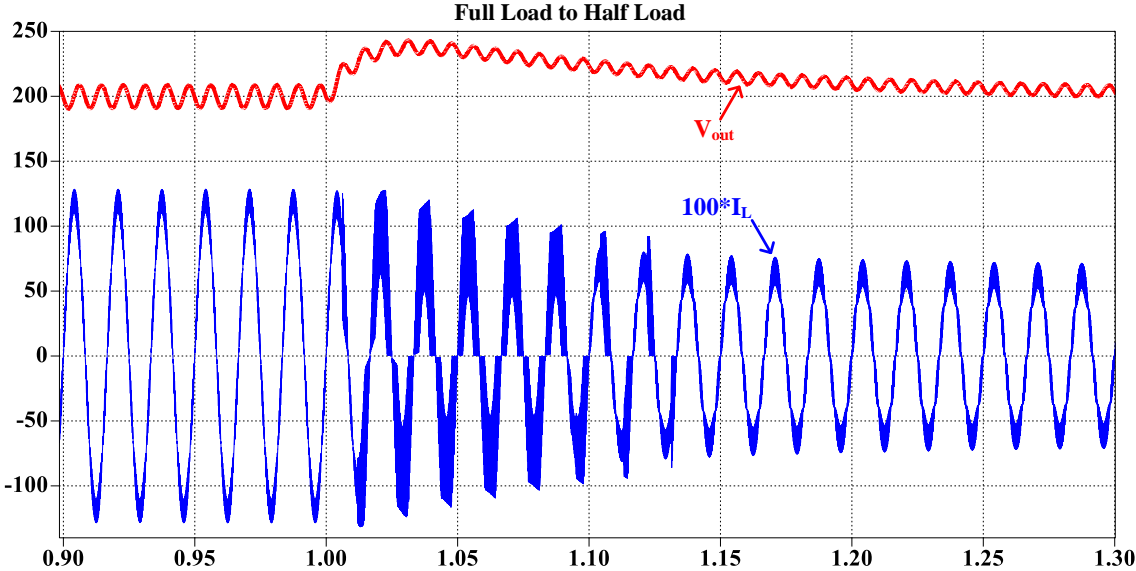


Figure 41. Output Voltage and Inductor Current for Full to Half Load Step for 3-Level Topology

The transient lasts about 10 line frequency cycles and the voltage overshoot is less than 50 volts. The input current is briefly non-sinusoidal, but quickly returns to a more sinusoidal shape. The second load step is also on the 3-level topology and is the reverse case from half load to full load load step for the same power level. The results are shown in Figure 42.

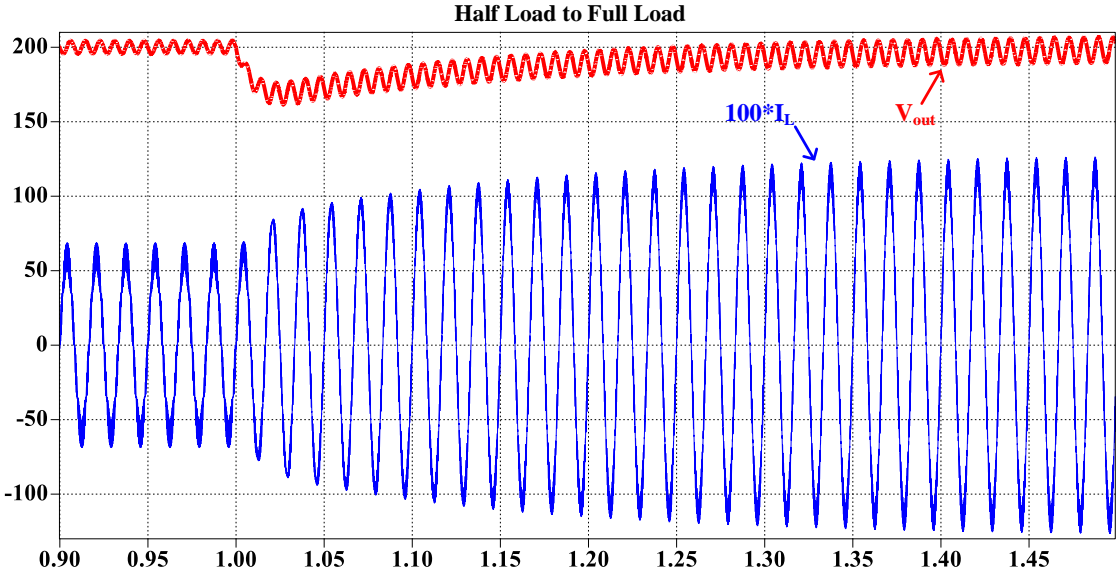


Figure 42. Output Voltage and Inductor Current for Half to Full Load Step for 3-Level Topology

The transient lasts more than 20 line frequency cycles, which is more extreme than the down load step. However, the input current remains sinusoidal for the entire transient. The next test is a down load step on the 5-level topology. The full load power is again 100W and the half load power is 50W. The results are shown in Figure 43. The results of a full load to half load step for the 5-level topology are shown in Figure 44.



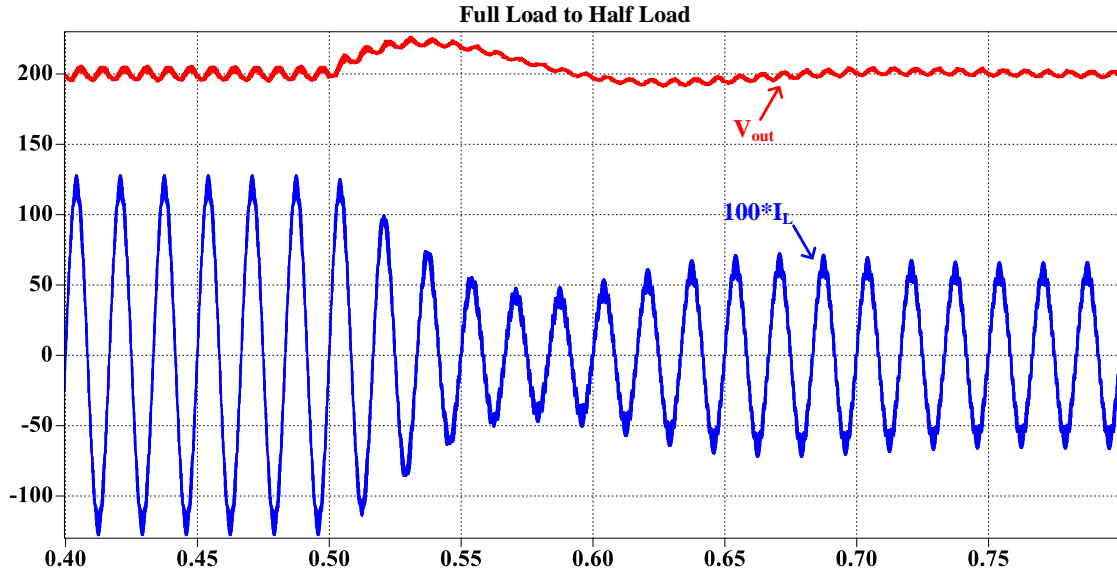


Figure 43. Output Voltage and Input Current for Full to Half Load Step for 5-Level Topology

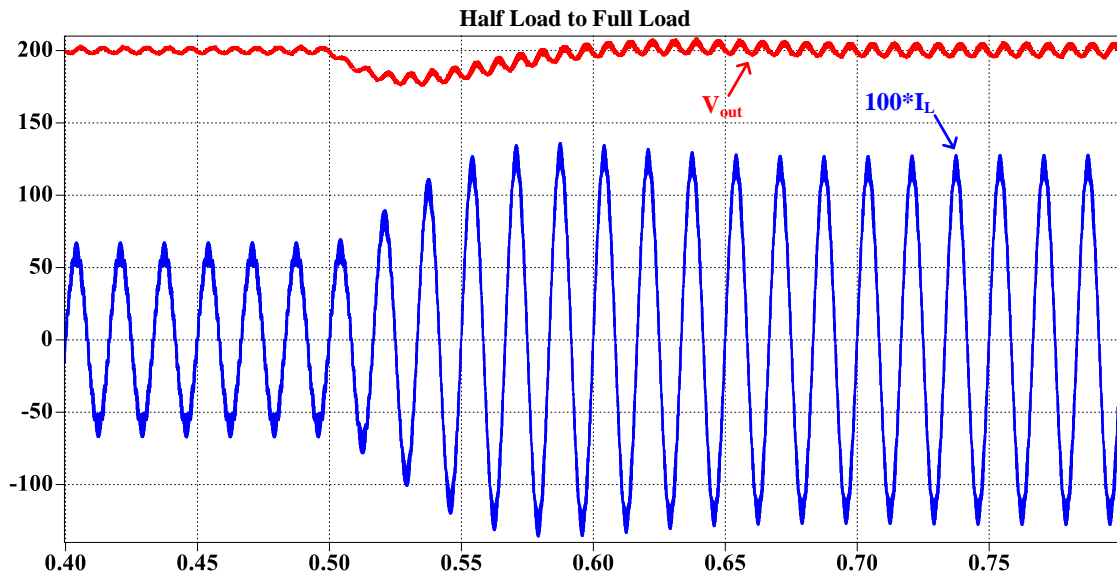


Figure 44. Output Voltage and Input Current for Half to Full Load Step for 5-Level Topology

The transient response for the full to half load step lasts about 10 line frequency cycles as in the 3-level topology, but the 5-level topology is able to maintain sinusoidal current throughout the transient. The transient response for the half to full load step also lasts about 10 cycles, which is faster than the 3-level transient response, indicating that the controller is a bit more responsive.

### 2.5.2 Changing Source Conditions

Boost PFC circuits are often designed for a wide input range and must be able to handle temporary voltage sags, which are when the input voltage drops to some lower value inside the operating input voltage range for several line frequency cycles and returns to full value. Additionally, PFC circuits must be able to withstand voltage drops, which are when the input voltage goes to zero for a short period. Often, DC-Link capacitors are designed to power the load during voltage drops for a certain number of line frequency cycles.

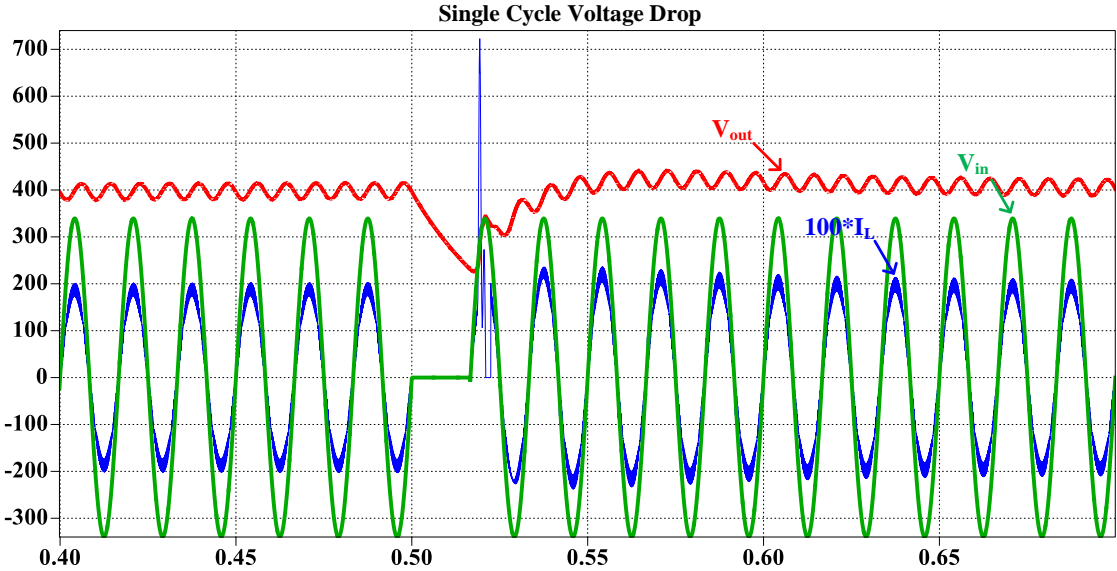


Figure 45. Input/Output Voltage and Inductor Current for a Voltage Drop for 3-Level Topology

The circuits tested in this section are 3.2kW circuits with 240Vrms rated inputs and universal input ranges of 85V~265V. The first test is a single cycle voltage drop on the 3-level and 5-level topologies. The results are shown in Figures 45 and 46.

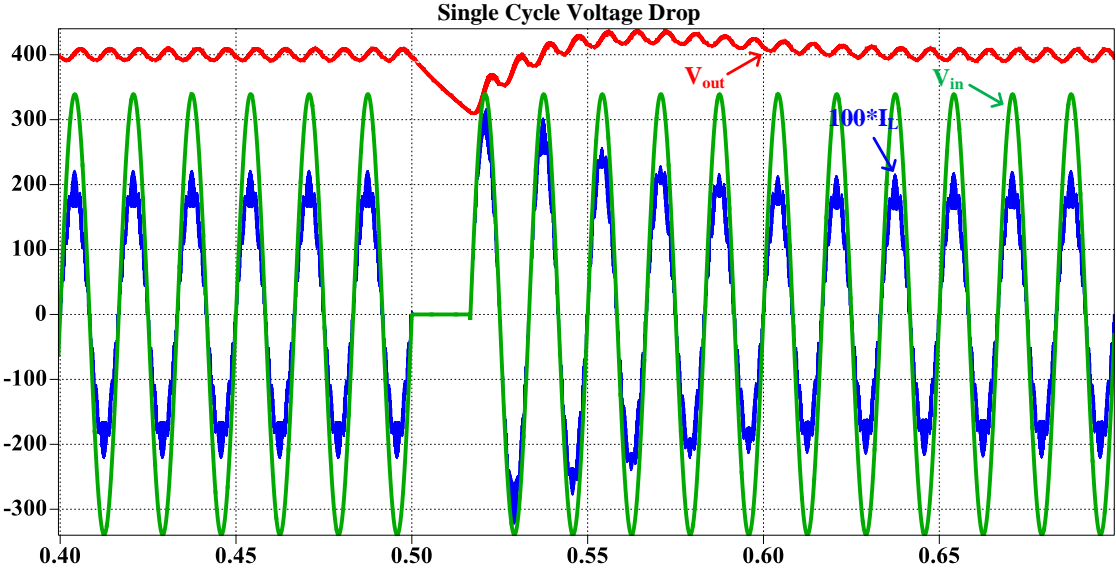


Figure 46. Input/Output Voltage and Inductor Current for a Voltage Drop for 5-Level Topology

The recovery time of the 5-level topology is slower than the 3-level topology, but the 5-level topology does not experience an input current spike. The current spike on the 3-level topology is more than 3 times the peak input current. The second test is a three cycle voltage sag on the 3-level and 5-level topologies. The results are shown in Figures 47 and 48.

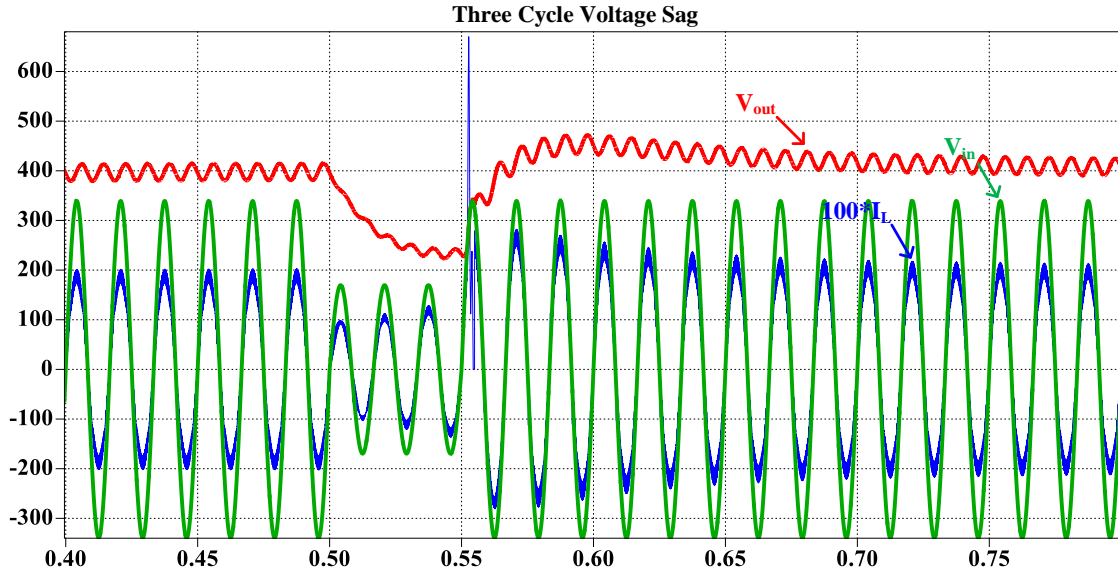


Figure 47. Input/Output Voltage and Inductor Current for a Voltage Sag for 3-Level Topology

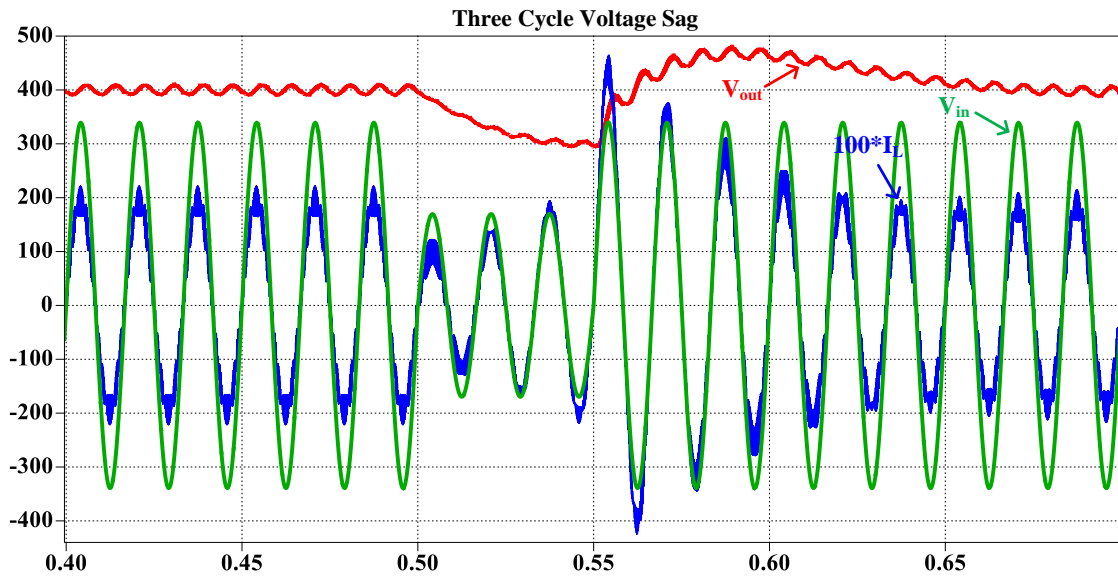


Figure 48. Input/Output Voltage and Inductor Current for a Voltage Sag for 5-Level Topology

The 5-level topology takes about the same amount of time to recover as the 3-level topology, however, this likely because the voltage drop is considerably less for the 5-level topology. Again, the 3-level topology experiences a large input current spike, but the 5-level topology also has a current overshoot of about twice the peak current.

These tests were performed with PI control loops that were not tuned and the responses could certainly be improved if the values were adjusted. The response of the output voltage loop would benefit from a faster response time, which could eliminate the current spike from the 3-level topology. These characteristics should be considered when tuning the PI loops.

## 3. DESIGN EXAMPLE

### 3.1 DC-Link Capacitor Selection and Sizing

The main purpose of DC-Link capacitors is to stabilize the DC voltage at the output of boost PFC rectifiers and even diode rectifiers. The sizing of the DC-Link capacitor is inversely proportional to the ripple voltage on the DC voltage. These capacitors typically occupy a very large amount of space on the converter. Reducing the size of the DC-Link capacitor is a very important key to increasing the power density of a boost PFC rectifier. For a given material and construction, the size of the capacitor is determined by two main factors: voltage rating and capacitance value. The voltage rating will tend to increase the size of the capacitor more than the capacitance value, so decreasing the voltage rating while increasing the capacitance value is a reasonable trade-off. There are typically two types of capacitors that are connected to the DC-Link, which are low frequency filtering capacitors and high frequency filtering capacitors. The design of both of these types of capacitors are described in this section.

#### 3.1.1 Choosing a High-Frequency Capacitor

High frequency capacitors are usually small value film capacitors that are placed as close as possible to the switching devices in order to minimize the EMI noise generated by the device. Film capacitors tend to be better high frequency filtering capacitors because they have much lower ESR and maintain their capacitance values at higher frequencies than electrolytic capacitors. Film capacitors can also be used as DC-Link filtering capacitors, but film capacitors are much bulkier and more expensive per unit of capacitance and voltage rating than an electrolytic capacitor of the same capacitance and voltage rating, so film capacitors are rarely used for this. However, for high

frequency filtering, small film capacitors can be used in parallel with large electrolytic capacitors to filter low and high frequency noise at an effective price point and minimal size.

### 3.1.2 Traditional PFC Capacitor Sizing

The main purpose of the low frequency DC-Link filtering capacitor for single-phase PFC circuits is to attenuate the second harmonic current. The second harmonic current is particularly large in single-phase AC-DC converters because the rectification performed by the switching devices essentially doubles the frequency of the line current on the DC side. The easiest way to see this is to use a diode rectifier, shown in Figure 49, as an example.

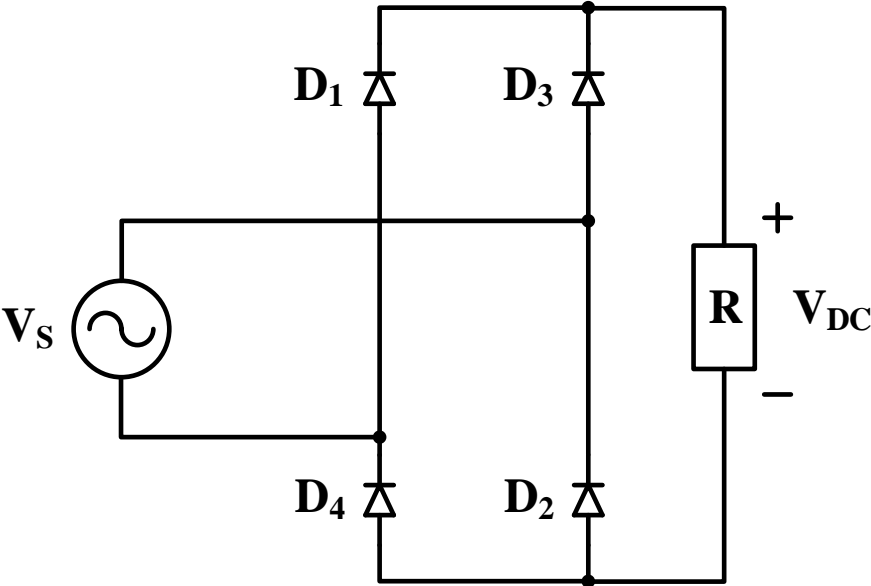


Figure 49. Diode Rectifier with Pure Resistive Output

In a diode rectifier, when the 60 Hz input voltage sine wave is positive and a purely resistive load (which is what a PFC load should look like) is attached to the output of the diode rectifier, current will be flowing through  $D_1$  and  $D_2$ . These diodes will always conduct current on the positive side of the input voltage sine wave and be zero when the input voltage sine wave is negative and the current through these diodes will have a frequency of 60 Hz. When the input voltage is negative, current will be flowing through  $D_3$  and  $D_4$ . Similarly to  $D_1$  and  $D_2$ , these diodes will always conduct on the negative side of the input voltage sine wave and be zero when the input voltage sine wave is positive and the current through these diodes will have a frequency of 60 Hz. Finally, the output will experience the sum of the currents through these diodes offset by 180 degrees. When the current through one set of diodes is equal to zero, the other diodes will be conducting. This results in an output current that has a frequency of 120 Hz shown in Figure 50.

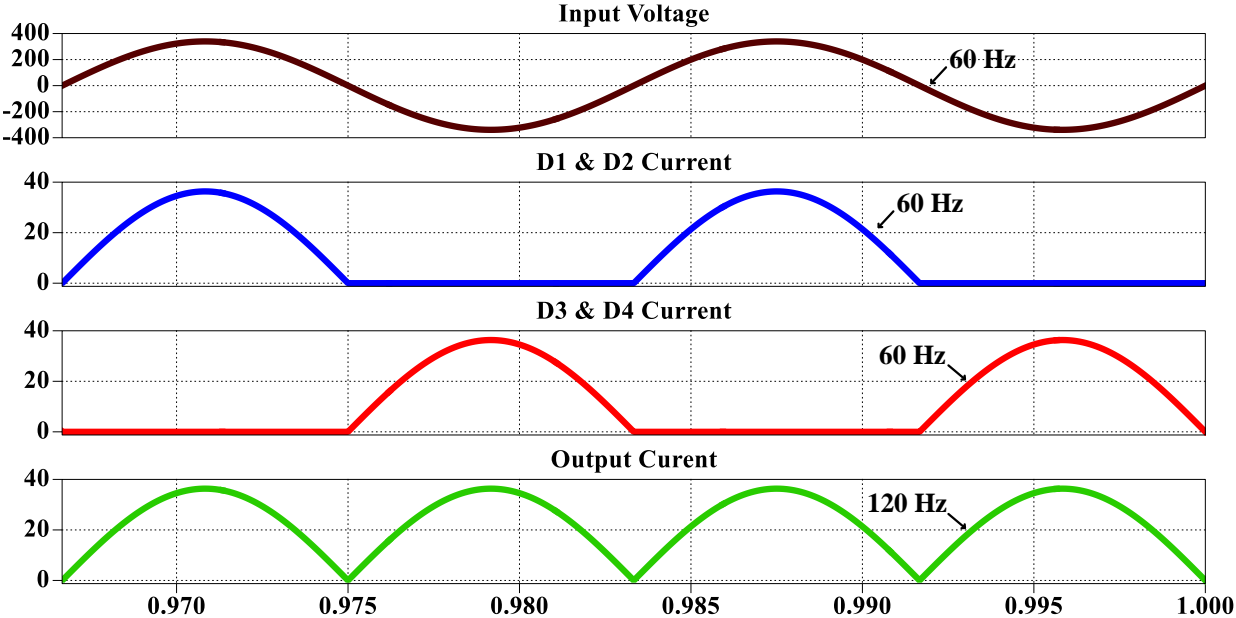


Figure 50. Diode Rectifier Diode and Output Currents



Because of this fundamental behavior that all AC-DC converters exhibit, the DC-Link capacitors are sized to limit the size of the second harmonic, which is also called the “double line frequency ripple”. We will assume that the load is entirely resistive for the purposes for the purposes of sizing the DC-Link capacitor. The size of the second harmonic voltage ( $V_2$ ) will be determined by the size of the second harmonic current ( $I_2$ ) and the capacitive impedance at the output. This relationship is shown in equation 27.

$$V_2 = \frac{I_2}{2 * (2\pi f_{line})C} \quad (27)$$

The second harmonic current can be represented as the reactive component of the output power divided by the output voltage, which is given in equation 28. The second harmonic voltage will be determined by the size of the output capacitor and thus can be represented as a fraction of the total output voltage as in equation 29.

$$I_2 = \frac{P_o}{V_o} \cos (2 * (2\pi f_{line}) * t) \quad (28)$$

$$V_2 = \frac{\Delta V_o}{V_o} \quad (29)$$

The cosine term can be dropped from equation 28 because magnitude is the only term of interest for determining the output voltage ripple. By substituting the magnitude of equation 28 and equation 29 into equation 27 and solving for the capacitance, the sizing equation for the traditional boost PFC rectifier output capacitor can be found and is given by equation 30.

$$C = \frac{P_o}{2 * (2\pi f_{line})\Delta V_o V_o} \quad (30)$$

### 3.1.3 Sizing the DC-Link Capacitor for the Proposed Topology

For the proposed topology, the effective output capacitance is less than the capacitance value of each capacitor. If all capacitors are assigned the same capacitance value, then they must

be multiplied by some variable that depends on the number of levels of the converter. The capacitance seen by the output is always the same for the proposed topology no matter state the converter is currently in. To see this, we will examine a three-level converter. There are eight total states for three-level converter of the proposed topology. Four of these states only differ in which diode is conducting, which has no effect on how capacitors in the topology are connected to the output, so we will only consider the four positive cycle states. For states 1 and 3, the only difference is whether switch 1 or switch 2 is turned on, which does not affect how the capacitors are connected to the output. The same is true for states 2 and 4. However, states 1 and 2 do connect the capacitors in the circuit to the output differently. During state 1,  $C_1$  is connected in parallel with  $C_3$ , but during state 2,  $C_1$  is connected in parallel with  $C_2$ . However, the equivalent capacitance of both of these configurations is the same if all capacitors are sized as some value  $C$ . The equivalent capacitance for an  $n$ -level topology is given by equation 31.

$$C_{eq} = C / \left(1 + \frac{1}{2} + \frac{1}{3} + \dots + \frac{1}{n}\right) = C/k \quad (31)$$

In order to account for this lower effective capacitance, the capacitance of each capacitor must be sized up by a factor of  $k$  in order to have the same capacitor performance at the output.

#### 3.1.4 Designing Capacitor Values for Peak Switch Current

There are two very important values to consider when choosing a DC-Link capacitor, which are the capacitance value and the equivalent series resistance (ESR) of the capacitor. As mentioned previously, if the voltage difference between two capacitors that are connected in series is large, then the short circuit current will be large. Therefore, if a capacitor with very low ESR, such as a film capacitor, is used as a DC-Link capacitor, the current spikes that would occur when the DC-Link capacitors are balanced would be very large. This might require larger current rating components and would certainly reduce the lifespan of the components that experienced the spike

currents. However, if very high ESR capacitors are used, they can significantly reduce the efficiency of the system. A possible compromise solution to this issue is connecting multiple capacitors in parallel to achieve reasonable figures for both peak switch currents and efficiency.

If the DC-Link voltage has a smaller ripple voltage, the voltage difference between capacitors will also be smaller. Because of this, more tightly regulated DC-Link voltages will increase efficiency and reduce peak current ratings of components. The voltage difference between capacitors for a 100W design for different ESR values is shown in Figure 51.

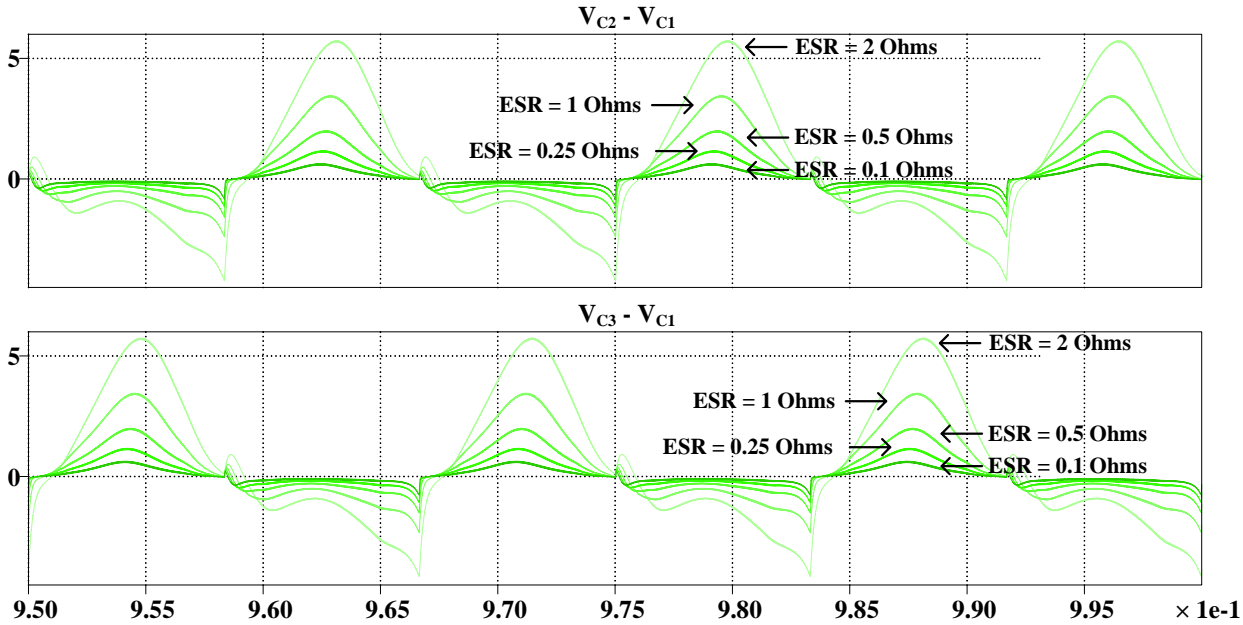


Figure 51. Capacitor Voltage Differences for Various ESR Values on a 3-Level Topology

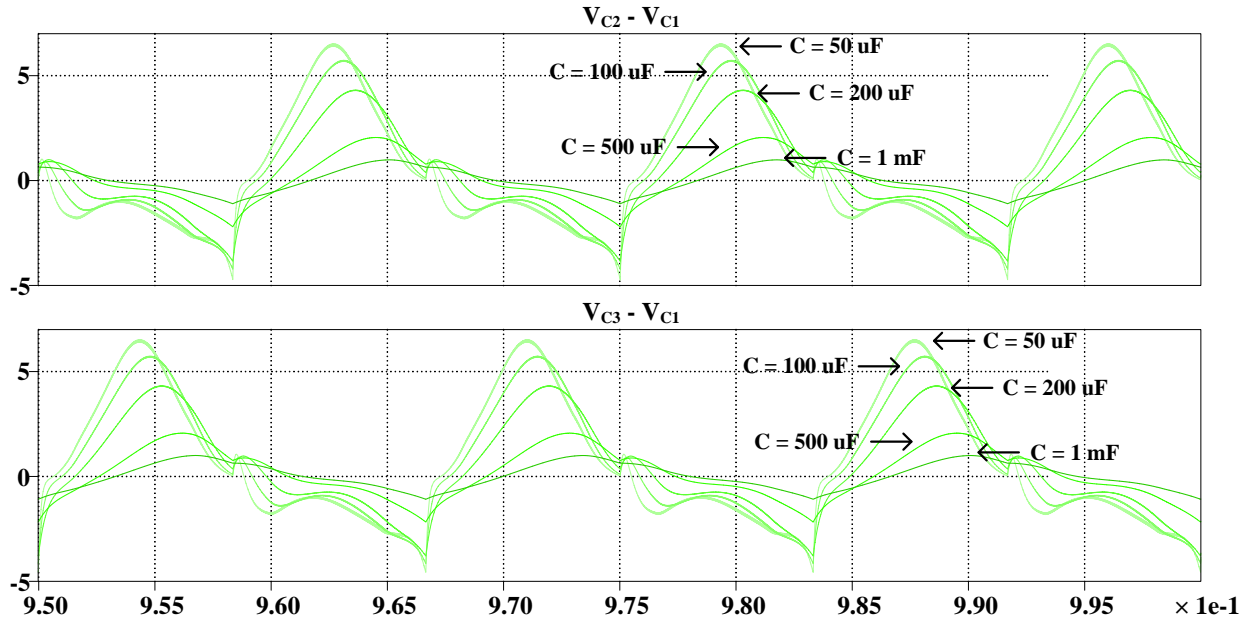


Figure 52. Capacitor Voltage Differences for Various Capacitance Values on a 3-Level Topology

Figures 51 and 52 show the voltage difference between the leg 2 capacitors and the leg 1 capacitor. As mentioned previously, the voltage difference is smaller for larger capacitance values and smaller ESR values. The reason why the voltage difference is small for a smaller ESR is because there is a large amount of current flowing between the DC-Link capacitors and the switches that connect them which is balancing the capacitors. This helps stabilize capacitor voltage, but also significantly increases switch current ratings. However, the reason why the voltage difference is small for larger capacitance values is because the voltage is not allowed to drift very far from the DC value.

## 3.2 Inductor Selection and Sizing

Inductor sizing is an important topic for PFC circuit design. For traditional boost PFC circuits, the input inductor is a significant portion of the total size of the converter [24]. One reason for the large size of the input inductor is that the inductance value must be sized for the minimum input current. This is an issue because of the wide input voltage range that most PFC circuits must be able to handle, which requires a very large inductance value at high input voltage and low input current, called “high-line” operation [25]. The large inductance value is required in order to maintain high power factor and avoid discontinuous conduction mode (DCM) operation. DCM operation can be used in certain scenarios but is undesirable if the controller of the circuit is designed to operate in continuous conduction mode (CCM).

In order to address the large inductance value required for high-line operation, a special type of inductor core is used for PFC applications. This type of inductor is called a “swinging choke” or powder core inductor and is much smaller than a “linear” inductor of the same inductance value [26]. The swinging choke is so called because the inductance value drops significantly as the input current through the inductor increases. This means that the inductance value will be much higher during high-line operation, which will help avoid DCM operation. Additionally, care must be taken to obtain an inductor that meets the high-line requirement at the high-line current and meets the rated voltage requirement at the rated current because these inductance values will vary significantly.

### 3.2.1 Choosing a High Frequency Inductor

GaN devices are allowing PFC circuits to operate at higher frequencies and inductor core materials are required to operate at higher frequencies with higher current. A good choice for switching frequencies up to 100 kHz is a powdered iron core toroid inductor such as Kool Mu or

High Flux [11]. However, for frequencies above 100 kHz, ferrite core materials, such as MnZn, can be used to obtain higher efficiency with lower core losses [27]. This material is suitable for switching frequencies up to 5 MHz and can handle currents as high as 32 A without the need for an external heatsink. Finally, an inductor designed using MnZn core material can be more compact than the powdered iron core material for the right application. Either of these options is suitable for the proposed topology.

### 3.2.2 Traditional PFC Inductor Sizing

For a traditional boost PFC rectifier, the current ripple is given using the same equation as a boost converter shown in equation 32.

$$\Delta i_{L,max} = \frac{DV_{in}}{f_{sw}L} \quad (32)$$

However, it is not obvious what value of duty cycle or input voltage should be used to obtain the worst-case ripple for the traditional boost PFC rectifier. First, we will investigate the duty cycle. It is well known that for a boost converter, the relationship between duty cycle and input voltage is given by equation 33.

$$\frac{V_o}{V_{in}} = \frac{1}{1-D} \quad (33)$$

Equation 33 also holds for a boost PFC rectifier and a multilevel boost PFC rectifier. However, in these cases, the input voltage and duty cycle are time varying functions. Duty cycle is controlled to satisfy the above equation and can be re-written as in equation 34 with  $d$  and  $V_{in}$  representing duty cycle and input voltage as time varying functions and  $V_o$  remaining constant.

$$d = 1 - \frac{V_{in}}{V_o} \quad (34)$$

Because the duty cycle and the input voltage are the only time varying functions, finding the maximum value of the multiplication of those two numbers will also give the maximum value of  $\Delta i_L$ . To solve this, duty cycle and input voltage are first multiplied together.

$$d * V_L = V_{in} \left(1 - \frac{V_{in}}{V_o}\right) \quad (35)$$

$$V_{in} = V * \sin(t) \quad (36)$$

In order to find the maximum value, the derivative of  $d * V_L$  is set equal to zero. Then, the solution of this equation will give the value of  $V_{in}$  that maximizes  $\Delta i_L$ .

$$\frac{d}{dt} (d * V_L) = \frac{d}{dt} \left( V * \sin(t) - \frac{V^2}{V_o} * \sin^2(\omega t) \right) = 0 \quad (37)$$

$$V * \cos(t) = \frac{2V}{V_o} \omega V * \cos(\omega t) \sin(\omega t) \quad (38)$$

$$V * \sin(t) = \frac{V_o}{2} \quad (39)$$

$$V_{in} = \frac{V_o}{2} \quad (40)$$

Plugging this value of  $V_{in}$  into the original duty cycle and inductor ripple equation yields the sizing equation, if  $V_{in,peak} > V_o/2$  given by equation 41. If  $V_{in,peak}$  is not greater than  $V_o/2$ , then plug in  $V_{in,peak}$ .

$$L = \frac{V_o}{4f_{sw}\Delta i_L} \quad (41)$$

### 3.2.3 Sizing Inductor for the Proposed Topology

For a multilevel converter, the answer is slightly different. In a traditional boost PFC, the maximum voltage on the inductor is  $V_o$ . However, in a 3-level converter, the voltage across the

inductor never exceeds  $V_o/2$ . Additionally, in a 4-level converter, the voltage across the inductor never exceeds  $V_o/3$ . This relationship is true for all  $n$ -level converters and is given by equation 42.

$$V_{L,max} = \frac{V_o}{(n - 1)} \quad (42)$$

This relationship also holds for a traditional boost PFC rectifier, which is simply a 2-level converter. To complete the derivation, simply substitute  $V_{L,max}$  in for  $V_o$  in the derivation of maximum  $d * V_L$ . The  $V_{in}$  value that maximizes current ripple is given by equation 43.

$$V_{in} = \frac{V_o}{2(n - 1)} \quad (43)$$

The duty cycle that will maximize the minimum inductance equation will again be 0.5. Finally, the switching frequency must be multiplied by  $n - 1$  to account for the inductor current ripple frequency multiplication that is achieved by the topology. Equation 44 is the solution for minimum inductor size for an  $n$ -level generalized multilevel PFC rectifier.

$$L_{min} = \frac{V_o}{4(n - 1)^2 f_{sw} \Delta i_{L,max}} \quad (44)$$

### 3.3 Switch and Diode Ratings

An important design consideration is the current and voltage ratings of diodes and switches in the topology. The diode and switch voltage ratings are a somewhat simple discussion as they closely match the output voltage and are very similar across like devices. However, the switch current ratings are not uniform across all switches and they also do not depend entirely on the input or output current. This is because of the unique voltage balancing feature of the topology. The ESR of the DC-Link capacitors and the  $R_{ds,on}$  values of switches are design parameters that will determine the switch currents.



### 3.3.1 Voltage Ratings

The voltage ratings for the diodes and switches in the topology can be addressed somewhat simply because the maximum ratings only depend on the output voltage. The maximum diode voltage ratings are simply the DC-Link voltage plus the maximum voltage ripple. This is because the diodes will be conducting if the input current flowing through each diode and will only block voltage when the other diode is conducting. Because the voltage on the other diode must be close to zero volts, the voltage on the blocking diode must be equal to the voltage across the DC-Link. This means the maximum voltage across the diodes is the maximum voltage on the DC-Link.

The maximum voltage ratings on the switches are also quite straightforward. The maximum voltage on any switch will simply be the maximum voltage on the capacitor that is connected to the half-bridge that the switch is connected to. Because the voltage on every half-bridge is identical, the maximum voltage on all switches will be the same. This maximum voltage is simply the maximum voltage of the DC-Link over  $n - 1$ . This is due to the multilevel operation of the topology which keeps the voltage across all capacitors very close to the DC-Link voltage over  $n - 1$ . Because the half-bridge switches always act in opposition, they only need to block the voltage across the half-bridge capacitor when the other switch is conducting.

### 3.3.2 Current Ratings

In this section, the diode and switch current ratings are considered. Simulation results are presented and correlated for various values of capacitance and capacitor ESR values. Additionally, the variation of current rating for switches throughout the topology is addressed.

The first point to address is that the switch current ratings for each switch position are different but are mirrored across the topology. For example, in a 3-level topology, switches 1 and 2, 3 and 6, and 4 and 5 all have very similar current ratings. This implies that switches mirrored

across the midpoint of the topology have the same current ratings, which is supported by simulation results. The 3-level topology will be taken as an example.

The line frequency diodes and the switches on the first leg will have a similar current rating as the input inductor. This means the vector sum of RMS currents through the first leg switches and the diodes will be equal to the RMS current through the inductor and the peak currents will be the same as the inductor. This is because no capacitor balancing current flows through the first leg switches or the diodes. The outermost switches on the second leg (3 and 5) will have similar RMS and peak current ratings from capacitor balancing currents, the input inductor current, and the output current. Finally, the innermost switches on the second leg (4 and 5) will have similar RMS and peak current ratings largely due to capacitor balancing currents and from the output current.

Table 8. Switch Currents for 100W Example with Various ESR Values

Capacitor ESR ( $\Omega$ )	Switch 1/2 RMS Current (A)	Switch 1/2 Peak Current (A)	Switch 3/6 RMS Current (A)	Switch 3/6 Peak Current (A)	Switch 4/5 RMS Current (A)	Switch 4/5 Peak Current (A)
0.1	0.596	1.283	0.636	2.802	0.224	2.567
0.25	0.597	1.285	0.635	2.181	0.225	1.957
0.5	0.599	1.289	0.633	2.124	0.224	1.579
1	0.601	1.297	0.627	1.995	0.227	1.337
2	0.607	1.311	0.606	1.770	0.242	1.248

An example simulation with 100W power, 120V input, and 200V output is analyzed to assess the effect of changing capacitor ESR values and capacitance on the switch currents. The RMS and absolute peak switch currents for all switches are listed for various capacitor ESR values in Table 8. The RMS and absolute peak switch currents for all switches are listed for various capacitance values in Table 9.

Table 9. Switch Currents for 100W Example with Various Capacitance Values

Capacitance ( $\mu\text{F}$ )	Switch 1/2 RMS Current (A)	Switch 1/2 Peak Current (A)	Switch 3/6 RMS Current (A)	Switch 3/6 Peak Current (A)	Switch 4/5 RMS Current (A)	Switch 4/5 Peak Current (A)
1000	0.599	1.290	0.351	0.933	0.345	0.990
500	0.601	1.295	0.415	0.991	0.327	0.937
200	0.604	1.303	0.543	1.17	0.277	1.161
100	0.607	1.311	0.607	1.269	0.241	1.248
50	0.609	1.321	0.634	1.960	0.226	1.357

Tables 8 and 9 demonstrate the significant impact capacitor design has on the current ratings of switches in the topology. Most PFC capacitor designs will not be affected by these results because film capacitors are rarely used as DC-Link capacitors due to their high cost and low power density, so the ESR values are rarely a concern. Additionally, most capacitors are designed for a very small output voltage ripple which will again result in switch current ratings that are well controlled.

### 3.4 Design Example

Table 10. Design Example Specifications

Output Voltage	400V
Input Voltage (RMS)	85V ~ 265V
Power	100W
Maximum Input Current Ripple @ 240V	30%
Switching Frequency	100 kHz
Maximum Output Voltage Ripple	1.5%
Number of Levels	3

Table 10 gives the design specifications of the design example. The maximum output voltage ripple is given as a percentage and this percentage is taken from the rated output voltage of 400V. This means the second harmonic ripple on the output voltage should be no more than 4V at full power. Using equation 30, given in section 3.1, the equivalent capacitance is calculated in equation 45.

$$C = \frac{(100)}{2 * (2\pi 60)(6)(400)} = 55.3 \mu F \quad (45)$$

Next, the actual capacitance will be calculated using equation 31, also given in section 3.1 and the final calculation is given in equation 46.

$$C = \left(1 + \frac{1}{2}\right) * 55.3 = 83.3 \mu F \quad (46)$$

The chosen value for each DC-Link capacitor is 100  $\mu F$  and the suggested voltage rating is at least 20% higher than the rated DC voltage which is 480V.

The maximum input current ripple is 30% of the peak current at 240V input voltage. The ripple at this condition is 0.177 A. Using equation 44, given in section 3.2, the inductance is calculated in equation 47.

$$L_{min} = \frac{(400)}{4(3 - 1)^2(100000)(0.177)} = 1.41 \text{ mH} \quad (47)$$

The peak is calculated as the maximum amplitude of the input current plus one half of the current ripple, which is 1.913A. Current rating of the input inductor should be large enough to avoid saturation of the core and the inductance value should be at least 1.41 mH at the rated current.

Finally, the circuit is simulated in PLECS to confirm the results. The worst-case output voltage ripple occurs at the maximum input voltage and is shown in Figure 53(a). The highest THD current occurs at the maximum output voltage, which is also shown in Figure 53(a). The peak current occurs at the minimum input voltage, shown in Figure 53(b).

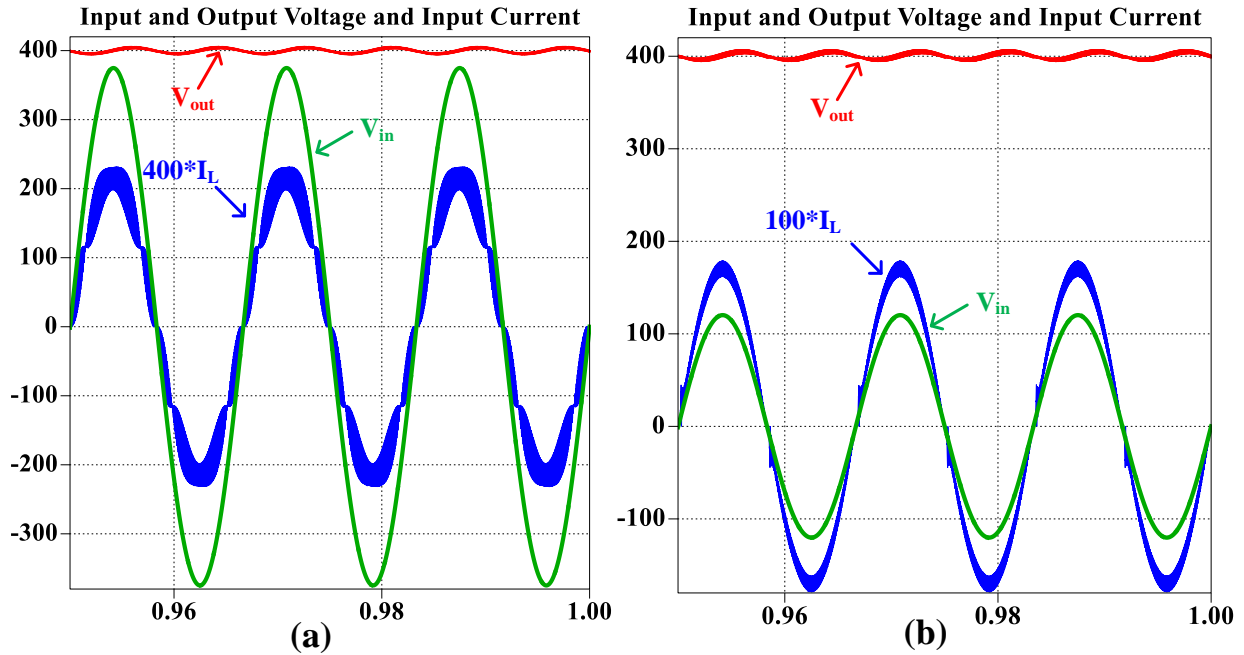


Figure 53. Input and Output Voltage and Input Current for (a) 265V and (b) 85V Input Voltage

The output voltage is less than 5V for the worst-case condition and the input current ripple is less than 30% for the worst-case scenario. The peak current is about 1.9 A for the worst-case scenario. These readings confirm the design values. Finally, Figure 54 shows the fractional capacitor voltages are well regulated at less than 1.5% ripple.

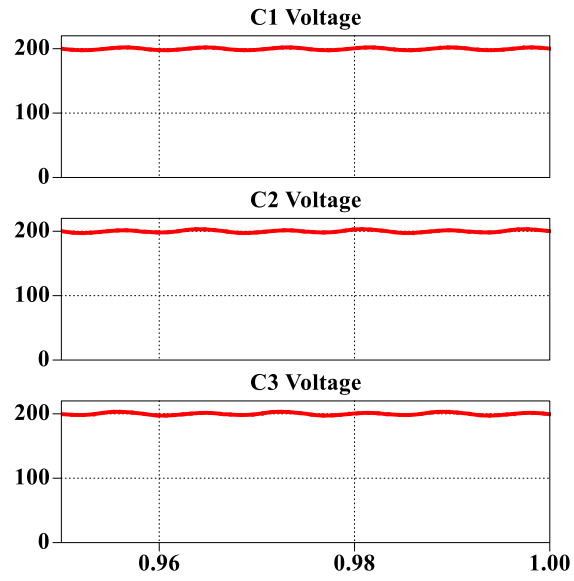


Figure 54. Fractional Capacitor Voltages

## 4. HARDWARE RESULTS

### 4.1 PCB Design

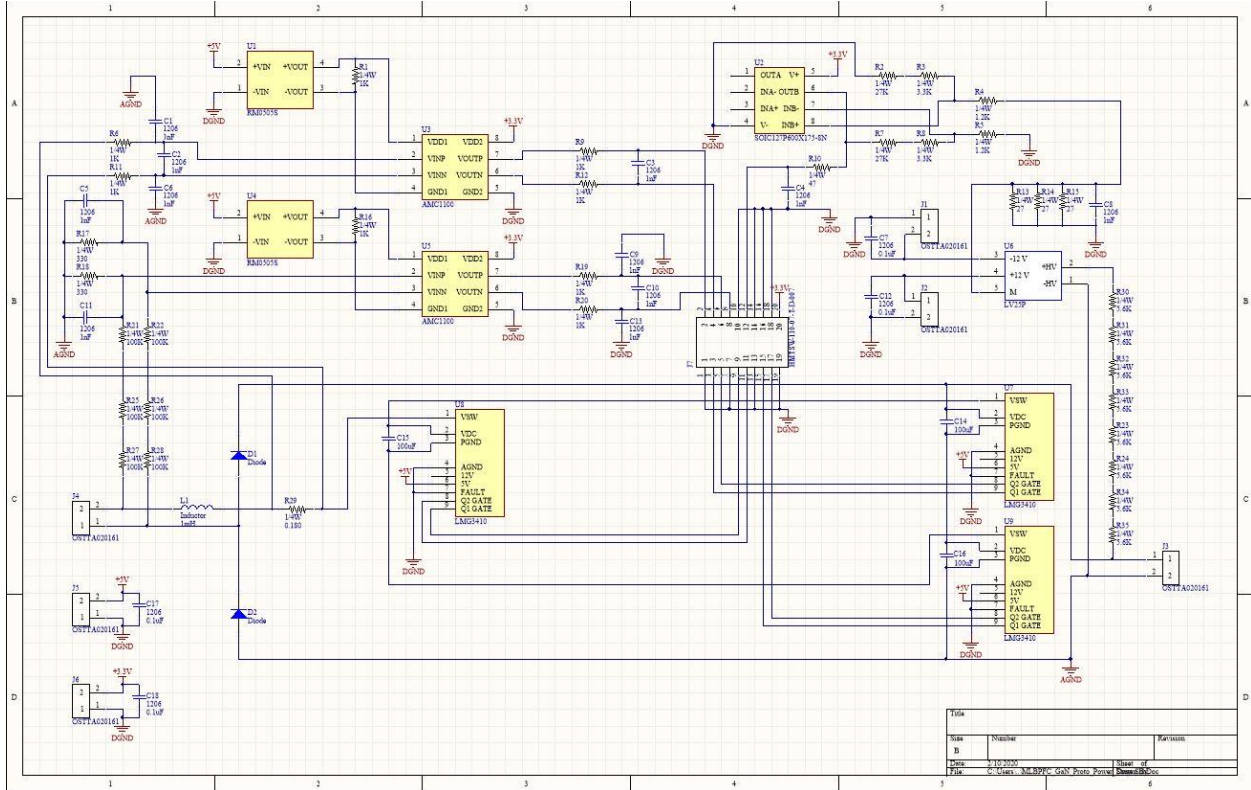


Figure 55. Prototype PCB Schematic

The printed circuit board (PCB) was designed in Altium and the schematic is shown in Figure 55. Isolated voltage sensors were used for both the input current and input voltage and an isolated voltage transducer was used to sense the output voltage. The use of isolation circuits contributed a significant amount to the losses of the prototype, especially the output voltage sensor,



but the isolation was deemed necessary to protect the controller and any computers that were attached to the circuit. The digital ground was therefore able to be completely isolated from the power circuit. Additionally, 5V DC-DC isolated converters were necessary to power the isolated voltage sensing circuits. 3.3V, 5V, and +/- 15V supplies are required for the prototype to function.

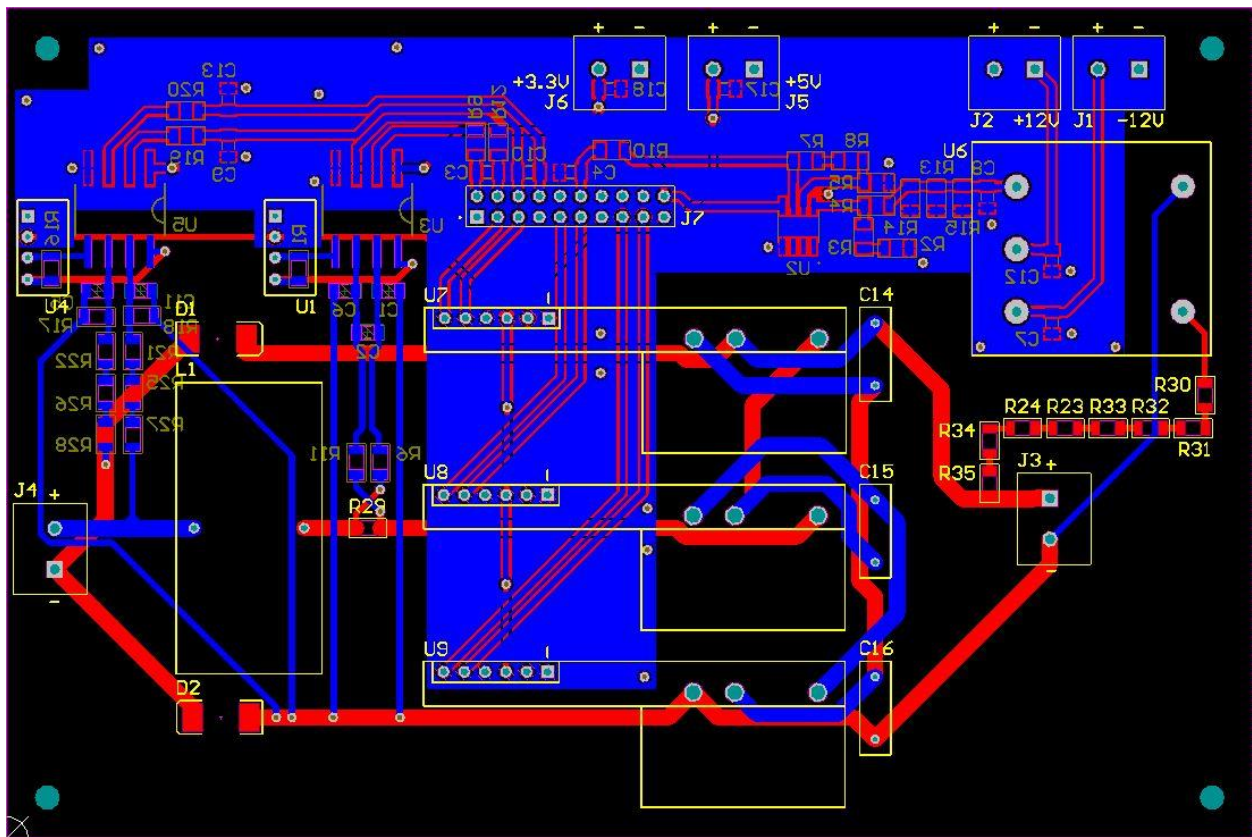


Figure 56. Prototype PCB Layout

In order to keep the design simple, a sense resistor was used to measure the input current of the circuit. This contributed to losses, but also made the current sensing circuit simpler to design and acted as a fuse to prevent high current from damaging the switching devices. The final PCB layout of the prototype is shown in Figure 56.

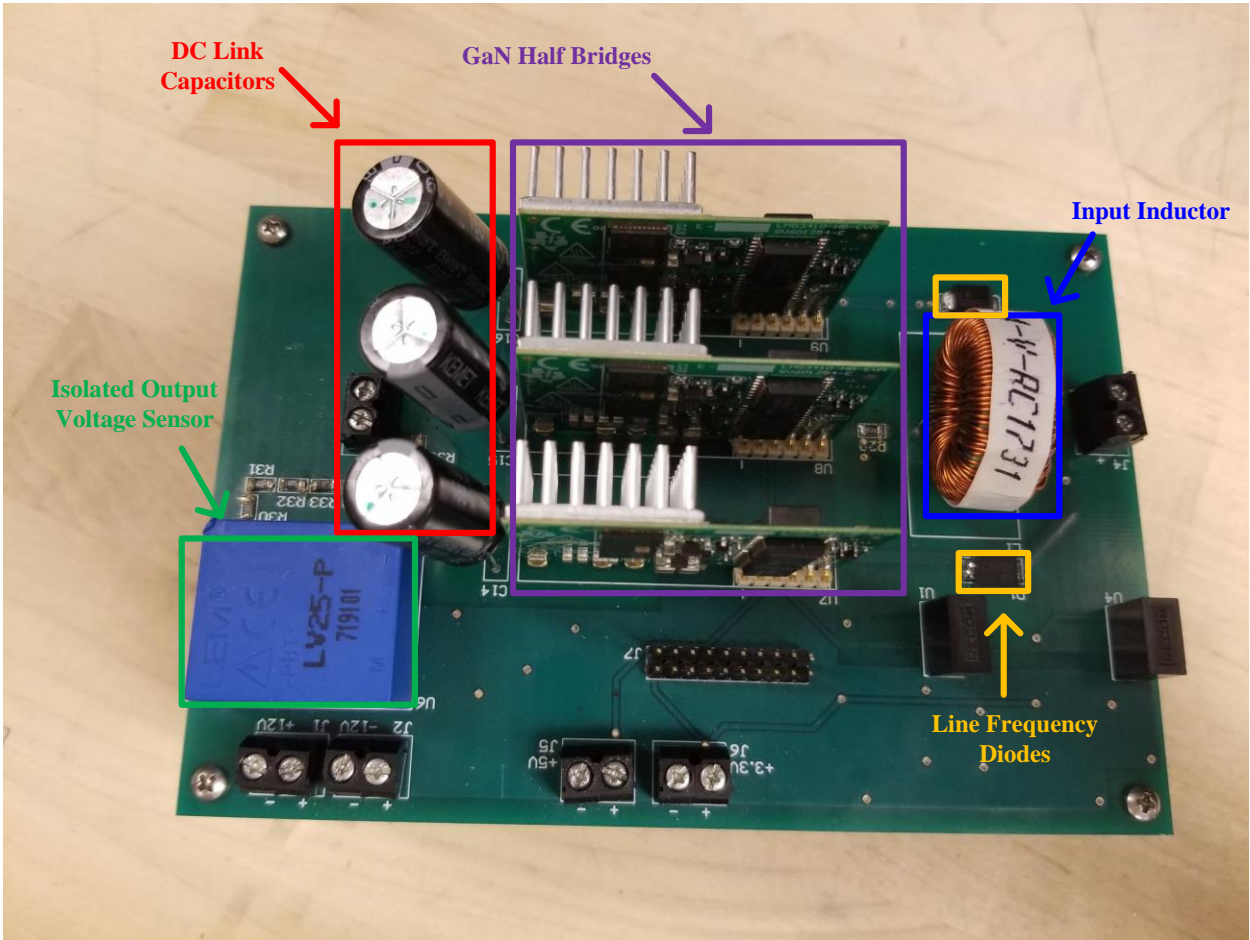


Figure 57. Final Prototype PCB

After the board was printed, the board was populated, and small practical changes were made to the design. For example, the sense resistor values were changed slightly in order to ensure the measured values remained within the controller Analog-to-Digital Converter (ADC) range. The final populated PCB prototype used for testing is shown in Figure 57.

#### 4.2 Test Setup

The test setup is shown in Figure 58. As mentioned previously, a 5V supply and +/- 15V supplies are necessary for the prototype to function. Additionally, the controller and EMI filter are externally attached to the prototype.

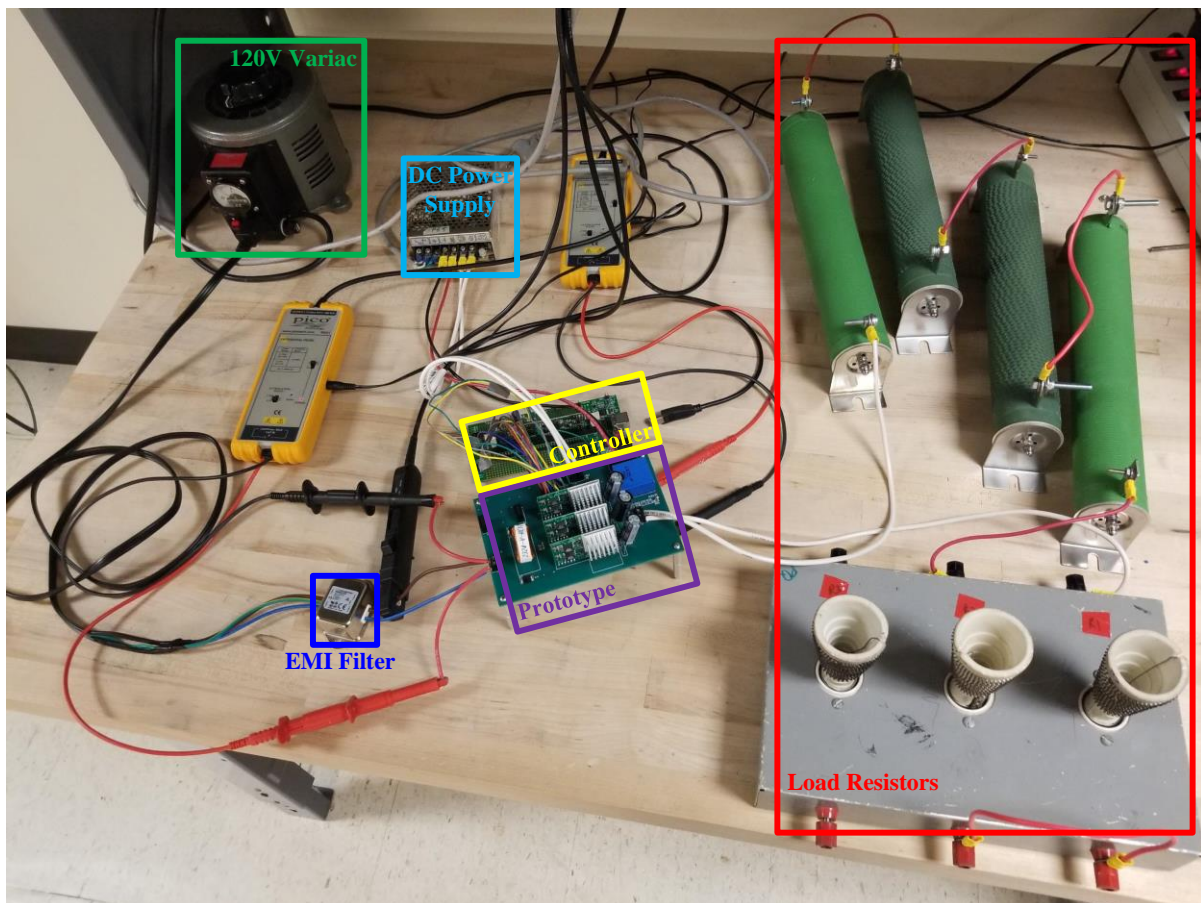


Figure 58. Test Setup

A 120V variac was used to soft start the topology. This was achieved by slowly ramping up the voltage at the input of the topology. This is so the DC-Link capacitors will charge up to the DC-Link value slowly. If care is not taken to slowly charge the DC-Link, the inrush current could be several times the rated current and could damage some components. The controller is designed to limit the DC voltage when the input voltage is low.

Electromagnetic Interference is caused by high frequency switching devices in power electronics circuits and is emitted by magnetic components. There are standards limiting the amount of EMI that can be conducted in the power line and the amount that can be emitted by the device. EMI can interfere with digital control signals within the same package as the power converter or those outside the device. EMI noise can be measured using a Line Impedance Stabilization Network (LISN). This device can indicate the level of the EMI noise and the frequency of the EMI noise which needs to be attenuated.

EMI filters are usually placed directly at the input of the power connections to the power converter and the output of the EMI filter is then fed to the power converter. Some EMI filters are attached to the power line that connects to the board that the power converter is built on. The EMI filter is the main EMI noise attenuation method, but there are other techniques that can help to reduce EMI that can be integrated into the design of the power converter. One of these techniques is adding film capacitors to each half-bridge module of the proposed topology to filter out EMI noise generated by the switching devices. Another is to choose a topology with an input inductor on the AC side to provide increased input inductance to filter EMI noise generated by the topology. An EMI filter was added to the front end of the topology to limit the noise experienced by the circuit. A larger EMI filter will result in cleaner input voltage and current waveforms.

Sensing circuits are an important part of controlling a PFC topology. The three sensing circuits in the prototype tracking the input voltage, input current, and output voltage. The output voltage sensing circuit is tracking a DC value and thus the delay in the sensing circuit will likely not affect the control of the DC value greatly. However, because the input voltage and current are AC waveforms, the delay in the sensing circuits are more important. The delay of the sensing circuits is determined by the filtering components and the controller. If the filter capacitors are very large, the delay may limit the response of the controller. The delay of the digital controller typically is not a significant contributor to the delay of the sensing circuit, but if the controller is operating in the megahertz frequency, this may become a larger issue. The current PI loop cutoff frequency should be designed with this delay in mind. If the response of the current loop is poor, the cutoff frequency should be lowered to account for the sensing delay.

### **4.3 Digital Control Implementation**

The control signals are generated by a Delfino microcontroller unit (MCU) made by Texas Instruments. This controller was chosen for rapid prototyping by using the code generation feature of the power simulation software PSIM. However, the control method for this topology is relatively simple and can be implemented on any controller that can control a typical boost PFC topology. The only consideration necessary for higher level topologies is ensuring the controller has a sufficient number of PWM outputs for each switch in the topology. For a 3-level converter, this is 6 signals. However, for a 5-level converter, this is 20 PWM signals.

#### **4.3.1 Code Generation**

A PSIM simulation was used to model the sensing circuits and determine the delay of the filtering components and the delay of the controller. When the circuit was functioning correctly in simulation, the software was able to generate code for the Texas Instruments Delfino

TMS320F28335 microcontroller. Using code composer studio, the code was loaded onto the controller and the control was tested on the topology. The values could quickly be tuned by editing the PSIM simulation or directly changing values in the code composer studio code.

The code generation feature of PSIM is very useful for rapid prototype design but is limited by the use of a special code composer studio library that is only used by PSIM. There is other software that has code generation features such as MATLAB/SIMULINK and PLECS with the PLECS RT Box. More testing will need to be done to assess the merits of each of these programs and identify the limitations.

#### **4.4 Figures of Merit**

The figures of merit for the topology are the power factor of the input and the output voltage ripple. Additionally, the fractional voltage level is shown and confirmed to be correct. The input voltage and current are required to observe the input power factor. The ideal input current and voltage will be sinusoidal in shape and perfectly aligned in order to minimize distortion power factor (DTF) and displacement power factor (DPF) respectively. The output voltage should be regulated at the designed value and the voltage ripple should be within the designed value.

The first figure of merit is the input current and voltage shown Figure 59. The current and voltage are almost perfectly aligned which will result in very high power factor. The input current waveform is also sinusoidal in shape. This prototype is meant to be a proof of concept and there is room for improvement on the shape of the input current. The input current has a significant amount of noise on the waveform due to hardware challenges listed in section 4.2. This waveform will improve with simple modifications.

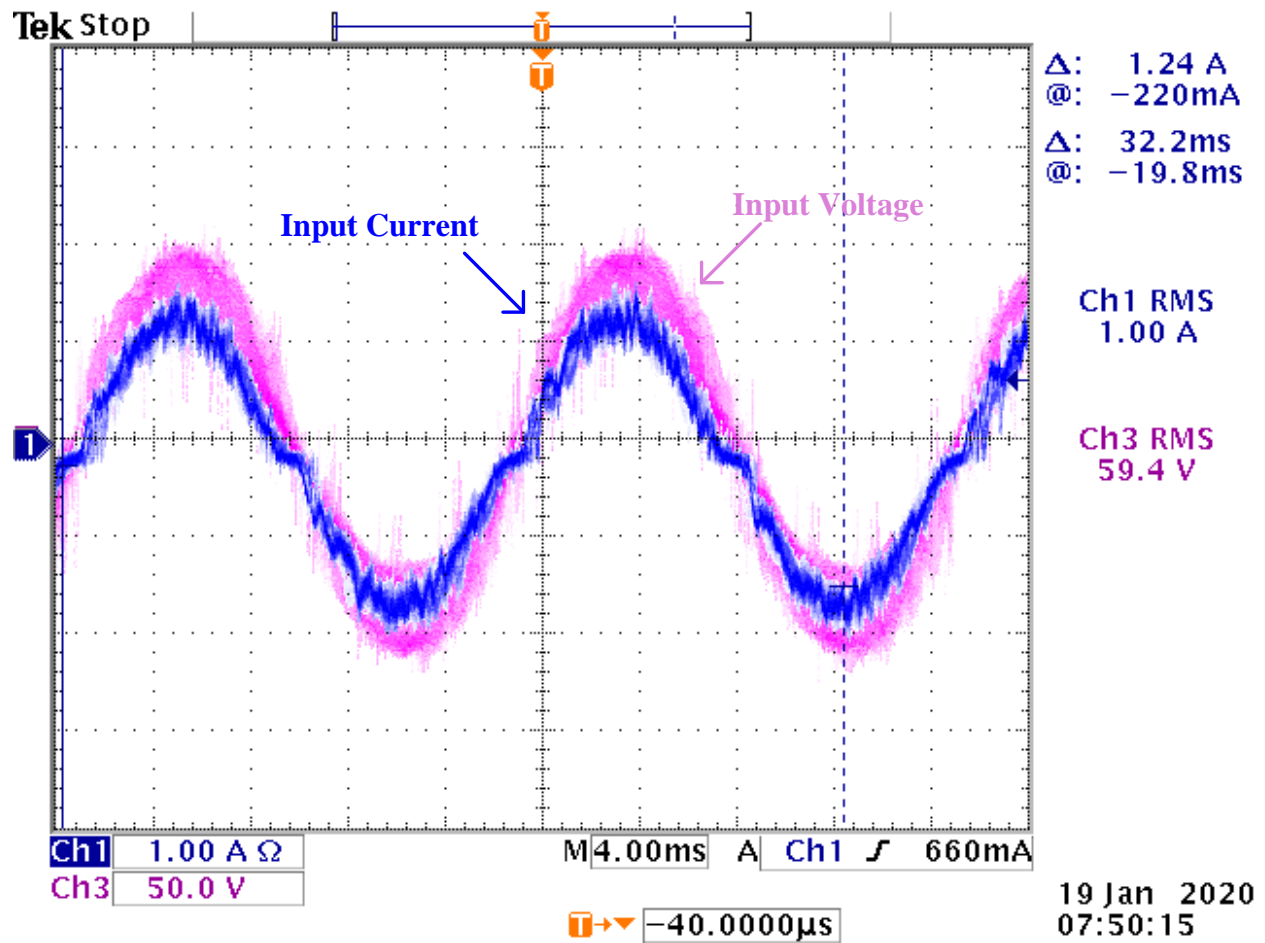


Figure 59. Prototype Input Current and Voltage

The power factor of the input was 0.98 and the THD of the input current was 13%. The maximum efficiency of the topology was 95.9%. The DPF is very high because the input current and voltage are closely aligned, but the DPF is slightly lower due to the distortion of the input current. Overall, the power factor achieved is good, but can be improved.

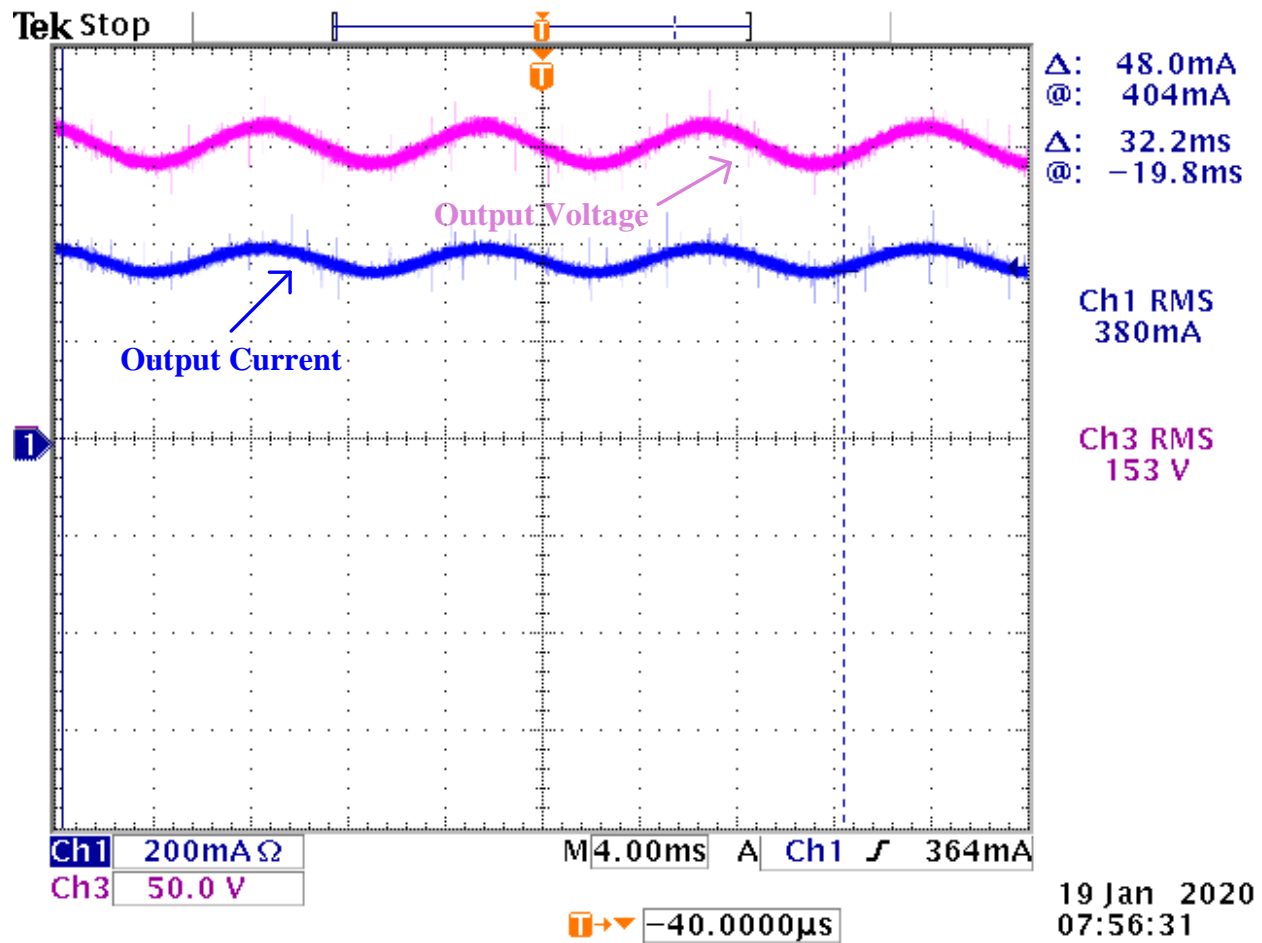


Figure 60. Prototype Output Current and Voltage

The output voltage and current are shown for the prototype in Figure 60. The circuit was designed for a relatively high ripple voltage of 10V and this measurement confirms that the prototype meets the specification. Additionally, the prototype regulated the DC voltage close to the reference DC output voltage of 150V.



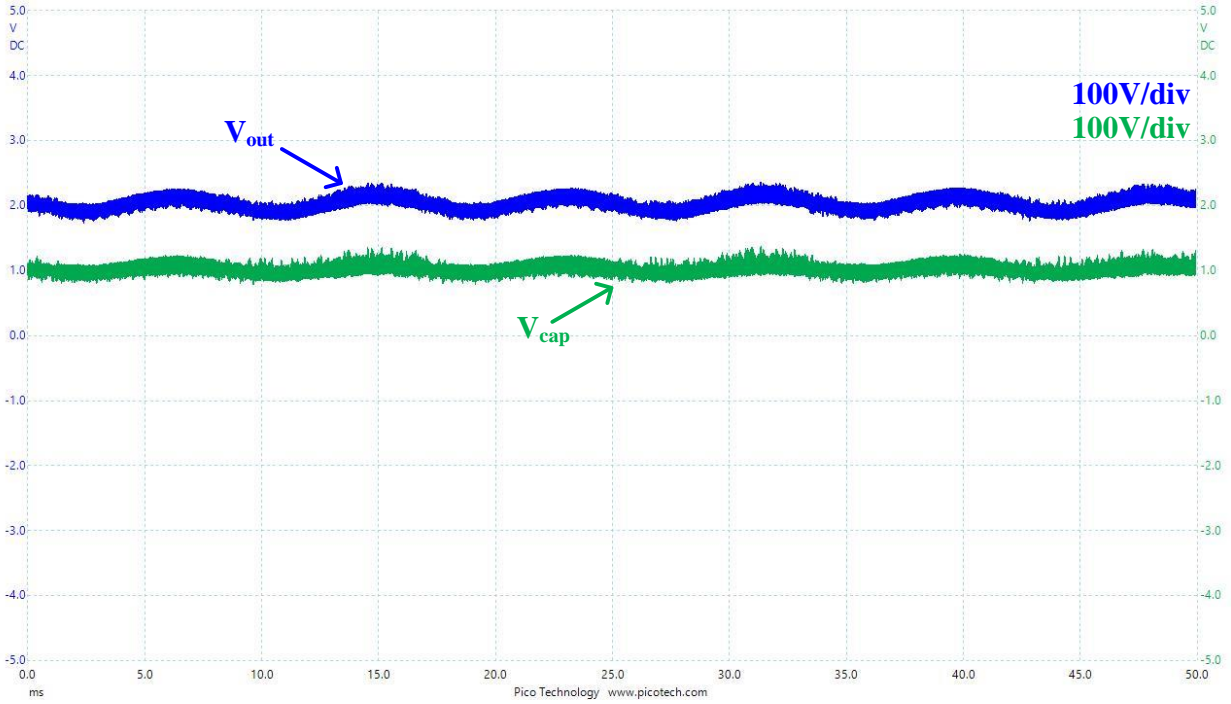


Figure 61. Prototype Output Voltage and Fractional Voltage Level

The output voltage and fractional voltage level of the topology is shown in Figure 61. The fractional voltage is one half of the output voltage, as expected, and is well regulated. The output voltage was increased to 200V from 150V in the previous test. This means the fractional voltage level is regulated at 100V.

## 5. CONCLUSION

### 5.1 Conclusions

A generalized multilevel boost PFC converter was presented that allowed the use of low voltage GaN devices to improve power density and efficiency. The benefits of low voltage GaN devices were explained and compared to higher voltage GaN devices and types of devices. A review of the previous literature was conducted, and the limitations of previous topologies were explained. A description of the zones of operation was presented and the method of capacitor balancing was discussed. Methods for improving capacitor balancing operation were presented. A review of PI control of boost PFC topologies was presented and python code for designing the controller constants was provided. The switching control of the topology was discussed and the extension of the control to higher level versions of the topology was explained as well as the frequency multiplication operation. The design of the DC-Link capacitors for a traditional boost PFC converter and the proposed topology was presented. A derivation of the minimum inductance equation for a traditional boost PFC converter and the proposed topology was presented that illustrated the substantial improvement in inductor sizing that the proposed topology achieves. Additionally, voltage and current ratings of switching components were discussed. A design example was presented, and simulation results confirmed the validity of the design values. The PCB design and sensing circuits were described and the PCB diagrams from Altium were presented. The experimental setup was shown, and some challenges of the design were discussed. The digital implementation of the controller was discussed. Finally, hardware results were presented as a proof of concept of the design.

## 5.2 Future Work

Future work should include adding active switches to the slow switching leg of the topology to increase efficiency. Further work on this concept should include scaling the topology to a greater number of levels. A prototype of a 3-level topology was presented, but a 5-level topology can easily be implemented using the design equations and descriptions from this work. An examination of the optimal number of levels should be conducted to find the best number of levels for a given design. This would make choosing the number of levels of the topology a design parameter rather than something that is decided before the design process begins. Next, the design of an EMI filter for the topology should be explained. This path of EMI filter design is exciting because if the filter can be designed well enough, the input inductor may be eliminated, which would allow for a more power dense solution. DC-DC converters have entered this territory with “magnetic-less” topologies. This is particularly appealing for PFC topologies because magnetic components are usually the largest components in the design. Next, a soft start approach using the proposed topology should be examined. This would involve operating the GaN devices on the fast switching leg like SCRs in order to slowly ramp up the voltage at the output in order to avoid inrush current. This is important because dedicated inrush current circuits usually must be designed for higher power PFC circuits because the current at start up is very large. If the topology can implement soft start without the need for extra components, this could be a major advantage over traditional boost PFC. Finally, an investigation of adding inductors to the midpoints of each half-bridge in the topology should be conducted. This is of interest because it could enable soft switching with the topology which would allow the switching frequency to be increased to a much higher level at the same efficiency level. Increasing switching frequency will allow for further reduction in the size of the input inductor.

## REFERENCES

- [1] D. M. Jones, "Power Factor Correction on Distributed Systems," in *Pacific Coast Convention of the American Institute of Electrical Engineers*, Portland, 1920.
- [2] T. T. Vu and G. Young, "Implementation of Multi-level Bridgeless PFC Rectifiers for Mid-Power Single Phase Applications," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, 2016.
- [3] A. Shehabi, S. Smith, D. Sartor, R. Brown, M. Herrlin, J. Koomey, E. Masanet, N. Horner, I. Azevedo and W. Lintner, "United States Data Center Energy Usage Report," Berkeley, 2016.
- [4] H. Z. Azazi, E. E. EL-Kholy, S. A. Mahmoud and S. S. Shokralla, "Review of Passive and Active Circuits for Power Factor Correction in Single Phase, Low Power AC-DC Converters," in *Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10)*, Cairo University, 2010.
- [5] International Electrotechnical Commission, "IEC Webstore," 26 January 2018. [Online]. Available: <https://webstore.iec.ch/publication/28164>.
- [6] ENERGY STAR, "energystar.gov," 31 October 2008. [Online]. Available: [https://www.energystar.gov/ia/partners/prod\\_development/revisions/downloads/FinalSpecV2.pdf?8fd5-1967](https://www.energystar.gov/ia/partners/prod_development/revisions/downloads/FinalSpecV2.pdf?8fd5-1967).
- [7] I. Cohen and B. Lu, "High Power Factor and High Efficiency—You Can Have Both," Texas Instruments, 2008.

- [8] A. Q. Huang, "Wide Bandgap (WBG) Power Devices and Their Impacts On Power Delivery Systems," in *IEEE International Electron Devices Meeting*, San Francisco, 2016.
- [9] L. Zhou, Y. Wu, J. Honea and Z. Wang, "High-efficiency True Bridgeless Totem Pole PFC based on GaN HEMT: Design Challenges and Cost-effective Solution," in *PCIM Europe*, Nuremburg, 2015.
- [10] Q. Huang and A. Q. Huang, "Review of GaN Totem-Pole Bridgeless PFC," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 187-196, 2017.
- [11] Q. Huang, Q. Ma, P. Liu, A. Q. Huang and M. de Rooij, "3kW Four-Level Flying Capacitor Totem-Pole Bridgeless PFC Rectifier with 200V GaN Devices," in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, 2019.
- [12] STMicroelectronics, "Calculation of turn-off power losses generated by an ultrafast diode," 2017.
- [13] S. L. Colino and R. A. Beach, "Fundamentals of Gallium Nitride Power Transistors," Efficient Power Conversion Corporation, 2019.
- [14] Infineon, *IPT60R028G7 Datasheet*, 2016.
- [15] Rohm, *SCT3030AL Datasheet*, 2017.
- [16] GaN Systems, *GS66516T Datasheet*, 2017.
- [17] Panasonic, *PGA26E07BA Datasheet*, 2017.
- [18] Transphorm, *TPH3207WS Datasheet*, 2016.

- [19] R. Martinez and P. N. Enjeti, "A High-Performance Single-phase Rectifier with Input Power Factor Correction," *IEEE Transactions on Power Electronics*, vol. 11, no. 2, pp. 311-317, 1996.
- [20] P. Kong, S. Wang and F. C. Lee, "Common mode EMI noise suppression in bridgeless boost PFC converter," in *APEC 07 - Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition*, Anaheim, 2007.
- [21] R. Zhang, S. Liu, B. Li, N. Zhao, G. Wang and D. Xu, "Totem-pole Bridgeless Boost PFC Converter Based on GaN HEMT for Air Conditioning Applications," in *IEEE Conference on Energy Internet and Energy System Integration*, Beijing, 2018.
- [22] F. Z. Peng, "A Generalized Multilevel Inverter Topology with Self Voltage Balancing," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, pp. 611-618, 2001.
- [23] G. E. Mejia-Ruiz, N. Munoz-Galeano and J. M. Lopez-Lezama, "Modeling and development of a bridgeless PFC Boost rectifier," *Revista Facultad de Ingeniería*, no. 82, pp. 9-21, 2017.
- [24] I. Moon, C. F. Haken, E. K. Saathoff, E. Bian, Y. Lei, S. Qin, D. Chou, S. Sedig, W. H. Chung and R. C. N. Pilawa-Podgurski, "Design and Implementation of a 1.3 kW, 7-Level Flying Capacitor Multilevel AC-DC Converter with Power Factor Correction," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, 2017.
- [25] S. Abdel-Rahman, F. Stuckler and K. Siu, "PFC boost converter design guide," Infineon Technologies AG, Munich, 2016.
- [26] ABB, "Reducing AFD-caused Harmonics at Partial Load Conditions," ABB Inc., New Berlin, 2005.

[27] T. Brander, A. Gerfer, B. Rall and H. Zenkner, *Trilogy of Magnetics*, Waldenburg: Wurth Elektronik, 2010.

## APPENDIX

### CURRENT AND VOLTAGE CONTROL LOOP DESIGN PYTHON CODE

The code in this appendix is written for python 3.6 and the libraries required to run the code are control, matplotlib, numpy, and scipy. A description of how the code should be used is given in section 2.3. The text of the two files for the current and voltage loops is included on the following pages.



```
"""
```

```
Title: MLBPFC_Current_Loop.py
```

```
Author: Kevin Hodge
```

```
Date: 02/01/2020
```

```
"""
```

```
import control as ctrl
```

```
import matplotlib.pyplot as plt
```

```
import numpy as np
```

```
import scipy as sci
```

```
plt.close()
```

```
# Relevant Circuit Values
```

```
Vs = 120 # RMS Value
```

```
P = 100
```

```
Vo = 200
```

```
D = 1-Vs/Vo
```

```
R = Vo**2/P
```

```
L = 0.000636
```

```
C = 0.000066 # Equivalent Value
```

```
# Transfer Function from Duty Cycle to Inductor Current
```

```

Gi = ctrl.tf([R*C*Vs/(R*L*C*(1-D)), 2*Vs/(R*L*C*(1-D))],[1, 1/(R*C), (1-D)**2/(L*C)])
#ctrl.bode(Gi)
#ctrl.rlocus(Gi)

# Set Cutoff Frequency of Current Control Loop (usually <= fsw/10)
wc = 2*np.pi*20000

# Select ki value that makes unity gain crossing match crossover frequency
ki_bound = np.linspace(0, 50000)

P = ctrl.evalfr(Gi, wc)
Pr = sci.real(P)

kp_bound = np.sqrt(1/(Pr**2)-ki_bound**2/wc**2)

#fig1 = py.figure()
#ax1 = fig1.add_subplot(111)
#ax1.plot(ki_bound,kp_bound)
#ax1.set_xlabel('ki')
#ax1.set_ylabel('kp')
#ax1.set_title('Kp vs Ki')

py.figure()
for i in [100, 1000, 5000, 10000, 15000, 25000, 30000, 40000, 50000]:
    # Calculate kp based on ki value
    ki = i # 25000

```

```

kp = np.sqrt(1/(Pr**2)-ki**2/wc**2)

# Plug Constants into Controller and Construct Feedback System

C = ctrl.tf([kp, ki], [1, 0])

GiCL = ctrl.feedback(ctrl.series(C,Gi),1)

#ctrl.rlocus(GiCL)

#ctrl.bode(GiCL)

# Plot Continuous Step Reponse

T = np.linspace(0,0.05,3251)

yout,Tc = ctrl.step_response(GiCL,T)

#py.figure()

py.plot(yout,Tc)

print("Current kp: ", kp)

print("Current ki: ", ki)

```

```
"""
```

```
Title: MLBPFC_Voltage_Loop.py
```

```
Author: Kevin Hodge
```

```
Date: 02/01/2020
```

```
"""
```

```
import control as ctrl
```

```
import matplotlib.pyplot as plt
```

```
import numpy as np
```

```
import scipy as sci
```

```
plt.close()
```

```
# Relevant Circuit Values
```

```
Vs = 120 # RMS Value
```

```
P = 100
```

```
Vo = 200
```

```
D = 1-Vs/Vo
```

```
R = Vo**2/P
```

```
L = 0.000636
```

```
C = 0.000066 # Equivalent Value
```

```
# CURRENT LOOP
```

```

Gi = ctrl.tf([R*C*Vs/(R*L*C*(1-D)), 2*Vs/(R*L*C*(1-D))],[1, 1/(R*C), (1-D)**2/(L*C)])
wci = 2*np.pi*20000
Pir = sci.real(ctrl.evalfr(Gi, wci))
kii = 25000
kpi = np.sqrt(1/(Pir**2)-kii**2/wci**2)
Ci = ctrl.tf([kpi, kii], [1, 0])
GiCL = ctrl.feedback(ctrl.series(Ci,Gi),1)

# VOLTAGE LOOP
# Transfer Function from Voltage PI to Ouput Voltage
Gv = ctrl.tf([R*(1-D)],[R*C, 1])
GvGiCL = ctrl.series(GiCL,Gv)
#ctrl.bode(GvGiCL)
#ctrl.rlocus(GvGiCL)

# Set Cutoff Frequency of Voltage Control Loop (usually <= fsw/100)
wc = 2*np.pi*2000

# Select ki value that ensures no overshoot
ki_bound = np.linspace(0, 15000)
Pr = sci.real(ctrl.evalfr(Gv,wc))
kp_bound = np.sqrt(1/(Pr**2)-ki_bound**2/wc**2)
#fig1 = py.figure()

```

```

#ax1 = fig1.add_subplot(111)

#ax1.plot(ki_bound, kp_bound)

#ax1.set_xlabel('ki')

#ax1.set_ylabel('kp')

#ax1.set_title('Kp vs Ki')

# Calculate kp based on ki value

ki = 25

kp = np.sqrt(1/(Pr**2)-ki**2/wc**2)

# Plug Constants into Controller and Construct Feedback System

C = ctrl.tf([kp, ki], [1, 0])

GvCL = ctrl.feedback(ctrl.series(C,GvGiCL),1)

#ctrl.bode(GvCL)

#ctrl.rlocus(GvCL)

# Plot Continuous Step Reponse

T = np.linspace(0,0.005,32501)

yout,Tc = ctrl.step_response(GvCL,T)

#py.figure()

py.plot(yout,Tc)

print("Voltage kp: ", kp)

print("Voltage ki: ", ki)

```