MEMRISTOR ENGINEERING: MODELING, FABRICATION, AND CHARACTERIZATION

A Dissertation

by

ALEXANDRE YASUO YAMAMOTO

Submitted to the Office of Graduate and Professional Studies of
Texas A&M University
in partial fulfillment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

Chair of Committee,	H. Rusty Harris
Committee Members,	Jun Kameoka
	Peng Li
	M. Suhail Zubairy
Head of Department,	Miroslav M. Begovic

December 2019

Major Subject: Electrical Engineering

Copyright 2019 Alexandre Yasuo Yamamoto

ABSTRACT

Memristors are the predicted fourth fundamental passive element of circuits, connecting a previously missing relationship between charge q and flux-linkage ϕ. It was first fabricated by a team led by Stanley Williams in 2008 and since many examples have been fabricated, but there is still much debate over how to properly model these devices, what is the physical mechanism for their behavior and even whether or not current examples can be considered the theoretical Memristor predicted by Leon Chua in 1971.

This dissertation shows that barriers preventing injection of charges to the switching medium are likely the cause of exponential terms in model, and this phenomenological cause for the differences found between manufactured devices and the theoretical device can be simply translated by diodes in series with an "ideal" Memristor. These non-idealities can be modeled by devices familiar to circuit designer such as diodes, and by using common tools such as SPICE, an effective model is provided for simulation of Memristors.

To try and clear the confusion over what an ideal Memristor is, a new unit of memristance is proposed, being named after Leon Chua: the Chua [Ch], representing the SI units of Ω/C. It is shown that this new way of describing Memristors by their own merit is valid and derives from the same reciprocity that suggested the existence of the device in the first place, being validated against several fabricated examples. This theory also explains some difficulties in measuring these devices, namely the fact that measurement and forming of the memristance are not completely independent and the fact that there is an inverse square dependency with the area; effectively explaining why memristive devices were found only when process nodes shrunk enough that the effects were more obvious.

Finally, this work proposes a structure that is simultaneously a HEMT and a Memristor, and cannot simply be explained by an association of one of each device; this is because the threshold voltage of the transistor appears to change proportionally to the state variable of the Memristor, effectively correlating the devices and causing an amplification of the change in resistance of the

memristor. This fact enables the creation of a memristive synapse that could be used in future neuromorphic circuitry, being more efficient than currently proposed 1T1M circuits.

DEDICATION

To my mother and father, who gave me life; and to my wife, who gave me reasons to live it.

ACKNOWLEDGMENTS

I owe the greatest thanks of all to my mother, Ana Virginia de Moraes, and my father, Lauro Koichi Yamamoto; they supported all of my weird choices throughout my life and didn't disown me when I decided to go to graduate school. I also cannot understate the support given to me by my wife, Emily Nicole Bartz, for being such a wonderful person and companion in this journey. None of this would ever be possible without their support and love.

To my advisor, Dr. H. Rusty Harris, I am thankful for all of the guidance and good laughs I had. Your always upbeat guidance provided an excellent environment to conduct research, and allowed me to reach a level of teaching and research I wasn't aware I was capable of. Thank you for pushing me out of my comfort zone.

As for my committee, I would like to thank Dr. Peng Li for the help with my early research career and the flexibility shown at the end of it. To Dr. Jun Kameoka, I owe gratitude for being such a good teacher and for showing me by example on how to be a good instructor. I would also like to thank Dr. Suhail Zubairy for being receptive on the idea of Memristors and providing such good feedback and encouraging words during my preliminary examination.

Additionally, this section would never be complete without my lab-mates. Michael Babb, you have helped me a lot throughout my time here with suggestions on my research despite having a herculean task of your own and I only wish I could have helped you as much as you helped me. William Baker, thank you so much for all the hard work you put in, both with helping the research and providing a very casual and fun atmosphere in the lab. Abhiram Dinavahi, thank you for all the help with theory and definitely thank you for willing to take over from where I left off; I truly believe the field will be better off with you in it. Sravani Jaligama, I appreciate all of the talks we had and all the words of encouragement you have given me. Jung Hwan, you are a truly awesome person and an inspiration for me; I honestly have no idea how you keep it all together with the incredibly hard work and dedication you have shown to me. I thank you for the example you have given me. Shuvodip, thank you for the laughs and the companionship during your time

here. Jae Woo, thank you for teaching me how Aggiefab works and the ins and outs of most obscure equipment in the fab. Feyza Berber, thank you for teaching me how to stand my ground and providing a new angle of view of academia. Andrew Schall, thank you for showing me where my previous research can lead; you have provided me many reasons to believe in myself and on the future of my work. Chen Gong, thank you for showing me how productive a graduate student can be in such a short time.

To Larry Rehn, Gregory Jordan, Etan Morse, Sam Mote, Chelsey Bullock, Jim, Dennis, and all others in Aggiefab that just kept the place running, thank you for all the support and hard work in keeping all machines working so I could fabricate my devices. Robert Atkins, thank you so much for keeping the academic laboratories in check and for all the support during my years as a TA of ECEN472. You made my work that much more enjoyable and classes would not have run smoothly without your help.

Due to space constraints, I decided to only thank those who were most present during my time at Texas A&M university. I do wish to thank all of those who have crossed my life up to this point; Know that I remember and am thankful to all of you.

Finally I would like to thank my dog and cat for simply existing in my life. Thank you Dr. Turing and Monseigneur Baudrillard for being there for me through thick and thin.

CONTRIBUTORS AND FUNDING SOURCES

Contributors

This work was supported by a dissertation committee consisting of Professors Harlan Rusty Harris, Jun Kameoka, and Peng Li of the Department of Electrical and Computer Engineering and Professor Muhammad Suhail Zubairy of the Department of Physics.

The data analyzed for the Tungsten-doped Memristor was provided in part by Michael Everett Babb of the Department of Electrical Engineering. The HEMT used for the analysis in chapter 6 was fabricated by Derek Wade Johnson.

All other work conducted for the dissertation was completed by the student independently.

Funding Sources

Graduate study was supported by a teaching assistantship from Texas A&M University.

NOMENCLATURE

1T1M	1-Transistor-1-Memristor
2DEG	2-Dimensional Electron Gas
BOE	Buffered Oxide Etch
CF	Conductive Filament
D	Switching medium thickness
HEMT	High Electron Mobility Transistor
I_S	Diode Saturation Current
I_d	HEMT Drain current
I_g	HEMT Gate current
I_s	HEMT Source current
LOR	Lift-Off Resist
MIIM	Metal-Insulator-Insulator-Metal
MIM	Metal-Insulator-Metal
MIS	Metal-Insulator-Semiconductor
MOS	Metal-Oxide-Semiconductor
n	Diode Ideality Factor
R_{INIT}	Memristor initial resistance
R_{ON}	ON-state resistance
R_{OFF}	OFF-state resistance
ReRAM	Resistive Random-access Memory
SI	Système International d'unités (International System of Units)

SV	State Variable
μ_V	Drift velocity
V_0	Diode built-in voltage
V_T	HEMT Threshold voltage
V_d	HEMT Drain voltage
V_g	HEMT Gate voltage
V_s	HEMT Source voltage
w	State Variable

TABLE OF CONTENTS

Page

ABSTRACT ii

DEDICATION iv

ACKNOWLEDGMENTS v

CONTRIBUTORS AND FUNDING SOURCES vii

NOMENCLATURE viii

TABLE OF CONTENTS x

LIST OF FIGURES xii

LIST OF TABLES xviii

1. INTRODUCTION 1

   1.1 The Tail End of Moore's Law 1
   1.2 Non-Von Neumann Computing 3
   1.3 Purpose of This Work 3

2. MEMRISTOR 5

   2.1 Physical Device Discovery 7
   2.2 Memristance Mechanisms 9
   2.3 Forming Cycle 11
   2.4 Density 13
   2.5 Current Modeling and Simulation 13

3. NON-IDEALITY AND MODELING 15

   3.1 Fitting Procedure 21
   3.2 Resulting Fits 23
   3.3 Nonlinear Parasitics Effects 27

4. MEMRISTANCE CHARACTERIZATION 37

   4.1 Symmetry Between Fundamental Circuit Elements 37
   4.2 Memristor Linearity 42
   4.3 Alternative Memristance Calculation Method 45

4.4 Association of Memristors 50
4.4.1 Series Association of Memristors 50
4.4.2 Parallel Association of Memristors 52
4.4.3 Volumetric Analysis of Memristance 54
4.4.4 Large Size Memristors: Electromigration as Memristance Mechanism 56
4.4.5 Conductive Filament Analysis 58
4.5 Linear Memristor Model Validation 59
4.5.1 Single Memristor Simulations 60
4.5.2 Series Memristor Simulations 62
4.5.3 Parallel Memristor Simulations 62
4.5.4 Parasitics Effect on Memristance Measurement 63

5. TESTING MEMRISTANCE 65

5.1 MIM Crossbar Memristor 65
5.2 Commercial Samples 67
5.3 Test Setup 68
5.3.1 Fabricated MIM Crossbar Memristor 69
5.3.2 Carbon-doped Chalcogenide 73
5.3.3 Tungsten-doped Chalcogenide 75
5.3.4 Overall Picture 77

6. MEMTRANSISTOR - 1T1M STRUCTURE 79

6.1 Device Structure 79
6.2 Memristance 80

7. CONCLUSION AND OUTLOOK 88

REFERENCES 90

LIST OF FIGURES

FIGURE Page

1.1 Trends in microprocessors until 2017 showing exponential transistor count growth while other performance figures start to plateau. Reprinted from [11] with permission under MIT License. 2

2.1 Graph illustrating how passive devices connect charge, current, flux and voltage. Art by Parcly Taxel used under CC-BY-SA 3.0. 5

2.2 (a) i-v plane of a Memristor, showing the pinched hysteresis at the origin and symmetric hysteresis areas in the first and third quadrant. (b) q-ϕ plane of the same Memristor, showing non-linearity. 6

2.3 i-v plot of a simulation of the first fabricated Memristor. 8

2.4 Sketch structure of the first fabricated Memristor. 8

2.5 (a) Sketch of a simple memristive device depicting an oxygen-deficient layer and its boundary. The location of the boundary w relative to the total thickness D is dubbed State Variable (SV). (b) Analogy with a potentiometer. 9

2.6 (a) and (b) i-v plot of a typical forming cycle for a metal-oxide Memristor. (c) Process sketch showing an initial middle layer going from insulator to switching medium due to application of a breakdown voltage. 12

3.1 Illustration of non-linearities present in many fabricated devices. (1) Non-linear current-voltage relationship in saturation. (2) Pinch point away from origin. (3) Asymmetry of hysteresis loops between quadrants. (4) High leakage currents that do not change SV. (a) Low cost Memristor based on TiO_2, adapted from [21]. (b) TaO_X Memristor, adapted from [71]. (c) Memristor crossbar array, adapted from [72]. (d) Memdiode for neuromorphic circuitry, adapted from [70]. 15

3.2 Band diagrams of a MIM Memristor. (a) Work function mismatch causing direct tunneling under certain bias conditions. (b) Work function mismatch causing a barrier to appear for injection of charges through the switching medium. 16

3.3 Simulations of a diode in series with a Memristor. (a) Circuit representation. (b) First quadrant response for varying built-in potentials: from left to right, 0.3V, 0.5V, 0.7V and 1V. (c) First quadrant response for varying ideality factors. 17

3.4 Simulations of a diode in parallel with a Memristor. (a) Circuit representation. (b) Response for varying built-in potentials: from left to right, 0.3V, 0.5V, 0.7V and 1V. (c) Response for varying ideality factors. 19

3.5 Simulations of a combination of diodes with a Memristor. (a) Diode in parallel with Memristor. (b) Diode in parallel with Memristor-diode. 20

3.6 Full device model for fabricated Memristors including parasitic diodes. 21

3.7 Illustration of the parallel leakage path on the diode curve and first approximations for parasitics variables. Upper inset shows the equivalent circuits and lower inset shows impact of changing ideality factor on parallel diode. 22

3.8 Memdiode for neuomorphic applications fit. (a) Fit overlaid in original published data adapted from [70] for comparison. (b) Simulation in LTSpice using the proposed model showing separate branch currents. In this case $n_{D_{S_1}} = 1.7$, $V_{0_{D_{S_1}}} = 0.75V$, $n_{D_{P_1}} = 1.6$, $V_{0_{D_{P_1}}} = 1.2V$, $R_{ON} = 7k\Omega$, $R_{OFF} = 800k\Omega$, $\mu_v = 0.8ncm^2s^{-1}V^{-1}$. 23

3.9 Crossbar array for neuromorphic applications fit. (a) Fit overlaid in original published data adapted from [72] for comparison. (b) Simulation in LTSpice using the proposed model. In this case $n_{D_{S_1}} = 1.5$, $V_{0_{D_{S_1}}} = 0V$, $R_{ON} = 800k\Omega$, $R_{OFF} = 1M\Omega$, $\mu_v = 0.5ncm^2s^{-1}V^{-1}$. 24

3.10 Low cost titanium oxide Memristor fit. (a) Fit overlaid in original published data adapted from [21] for comparison. (b) Simulation in LTSpice using the proposed model. In this case $n_{D_{P_1}} = 7$, $V_{0_{D_{P_1}}} = 0V$, $n_{D_{P_2}} = 3.7$, $V_{0_{D_{P_2}}} = 0V$, $n_{D_{S_1}} = 1.7$, $V_{0_{D_{S_1}}} = 0V$, $n_{D_{S_2}} = 3$, $V_{0_{D_{S_2}}} = 0V$, $R_{ON} = 10k\Omega$, $R_{OFF} = 300k\Omega$, $\mu_v = 20pcm^2s^{-1}V^{-1}$. 25

3.11 MIM Memristor fit. (a) Fit overlaid in original published data adapted from [71] for comparison. (b) Simulation in LTSpice using the proposed model. In this case $n_{D_{S_1}} = 2$, $V_{0_{D_{S_1}}} = 0.25V$, $n_{D_{S_2}} = 1$, $V_{0_{D_{S_2}}} = 0.5V$, $n_{D_{P_2}} = 4.1$, $V_{0_{D_{P_2}}} = 1.4V$, $R_{ON} = 10\Omega$, $R_{OFF} = 7k\Omega$, $\mu_v = 1.04ncm^2s^{-1}V^{-1}$. 26

3.12 Current-Voltage characteristic of a fitted ferroelectric Memristor adapted from [79]. Dashed lines show the simulated model. 27

3.13 Methodology for calculating hysteresis area in a quadrant. Arrow points to maximum excitation voltage. (a) Integration of first half of positive swing (zero to maximum voltage). (b) Integration of second half of positive swing (maximum voltage back to zero). (c) Resulting hysteresis area due to simple subtraction of areas. 28

3.14 Magnitude of hysteresis area versus frequency for a Memristor. 28

3.15 Magnitude of hysteresis area versus frequency for a Memristor which exhibits many non-idealities such as saturation. 29

3.16 i-v curve for a frequency of 1Hz for Memristor of Fig. 3.15. 30

3.17 Magnitude of hysteresis area versus frequency for the Memristor of Fig. 3.14 altered by anti-parallel diodes of $n = 1$ in series with it. 31

3.18 Result of the simulation showcasing hysteresis area change because of anti-parallel diodes in series with a Memristor. 32

3.19 Result of the simulation showcasing hysteresis area change because of anti-parallel diodes in parallel with a Memristor. 33

3.20 Result of the simulation showcasing pinch point change for a variety of ideality factors. (a) Circuit being simulated. (b) Simulation result. (c) Zoom of pinches with arrow pointing to pinch. 34

3.21 Result of the simulation showcasing pinch point change as function of series diodes ideality factor and driving frequency. 35

4.1 (a) i-v plane of a NTC thermistor that self-heats, showing hysteresis. (b) q-ϕ plane of the same thermistor. 37

4.2 (a) i-v plane of a capacitor with an initial condition of 0.5V. (b) Conductance-i plane of the same capacitor. 38

4.3 (a) 3D plot of a capacitor showing projection in Conductance-i plane. (b) 3D plot of a capacitor showing projection in i-v plane. (c) Conductance-i plane projection. (d) i-v plane projection. 39

4.4 (a) 3D plot of an inductor showing projection in Ω-i plane. (b) 3D plot of an inductor showing projection in i-v plane. (c) Ω-i plane projection. (d) i-v plane projection. 40

4.5 (a) 3D plot of a Memristor showing projection in Ω-i plane. (b) 3D plot of a Memristor showing projection in i-v plane. (c) Ω-i plane projection. (d) i-v plane projection. 41

4.6 (a) 3D plot of a NTC thermistor showing projection in Ω-i plane. (b) 3D plot of a NTC thermistor showing projection in i-v plane. (c) 3D plot of a NTC thermistor showing projection in Ω-v plane. 42

4.7 Ideal memristor showing linearity. 44

4.8 Practical memristor showing linearity region and saturation regions. 45

4.9 Ω-I plane of an ideal Memristor showing instantaneous resistance change. 47

4.10 (a) i-v and (b) Ω-i plane of a manufactured Memristor. 47

4.11 (a) i-v curve of the parallel plate capacitor shown in (b). 48

4.12 Histogram of detected capacitances showing peak at $15.3nF$. 49

4.13 Histogram of detected memristances showing peak at $8GCh$ 50

4.14 Series association of memristors. 51

4.15 Equivalent Memristor arising from the series association of Memristors with characteristics $M_1q + R_1$ and $M_2q + R_2$ 52

4.16 Parallel association of two identical Memristors. 52

4.17 Parallel association of n identical Memristors. 53

4.18 Memristor MIM structure showing "quantized" memristance block removed. 55

4.19 Copper interconnect subject to a DC and 1MHz AC current over time. Reprinted with permission from [84]. 57

4.20 Copper interconnect subject to a AC current over time showing linear dependence between charge and resistance. Reprinted with permission from [84]. 58

4.21 (a) Memristor structure showing single CF. (b) Longer CF. (c) Multiple CF. (d) Single CF with lower mobile ions. 59

4.22 Memristor test setup on LTSpice. 60

4.23 (a) i-v curve of the simulated Memristor using Biolek's model. (b) Ω-q curve of the same memristor showing linear and saturation region. 61

4.24 (a) i-v curve of the simulated Memristor using Biolek's model for three different variations in test parameters. (b) Ω-q curve of the same Memristor showing linear and saturation region for three different variations in test parameters. 61

4.25 (a) i-v curve of the simulated Memristors in series using Biolek's model. (b) Ω-q curve of the same Memristors showing linear and saturation region. 62

4.26 (a) i-v curve of the simulated Memristors in parallel using Biolek's model. (b) Ω-q curve of the same Memristors showing linear and saturation region. 63

4.27 (a) i-v curve of the simulated Memristors with and without a $1nF$ parallel capacitor at $1kHz$. (b) Ω-q curve of the same configurations. 64

5.1 Sketch of fabrication sequence. Not to scale. 65

5.2 Fabricated crossbar structure with contact pads for probing. 66

5.3 Two packaged memristor devices with eight Memristors each. Top: Tungsten doped Chalcogenide. Bottom: Carbon doped Chalcogenide. 67

5.4 Circuit of the test setup. 68

5.5 Methodology for the calculation of history of charge through the device. 69

5.6 (a) i-v curve of the fabricated MIM Memristor. (b) Ω-q curve of the same Memristor showing linear region, saturation regions and other non-idealities. 69

5.7 (a) i-v curve of the fabricated MIM Memristor corrected to remove non-idealities. (b) Ω-q curve of the same Memristor showing linear regions of same slope. 70

5.8 Analysis of memristance as measured using a sinusoidal voltage source in multiple frequencies for the fabricated MIM Memristor. 71

5.9 Time variance of memristance due to the formation of new conduction paths resulting in lower memristance. 72

5.10 Number of new channels as a function of time. 73

5.11 (a) Ω-i and Ω-q curve of the Carbon Knowm device. (b) i-v curve of the same Memristor for the third quadrant. 74

5.12 Analysis of memristance as measured using a sinusoidal voltage source in multiple frequencies for the Carbon-doped chalcogenide device. 75

5.13 (a) i-v curve of the Tungsten Knowm device. (b) Ω-q curve of the same Memristor. 76

5.14 (a) Corrected i-v curve of the Tungsten Knowm device. (b) Ω-q curve of the same Memristor corrected. 76

5.15 Analysis of memristance as measured using a sinusoidal voltage source in multiple frequencies for the Tungsten-doped chalcogenide device. 77

5.16 Analysis of mean measured memristance in multiple frequencies for all devices, with every measurement of Memristance shown. 78

5.17 Analysis of mean measured memristance in multiple frequencies for all devices, with average of Memristance measurements for every frequency shown. 78

6.1 Sketch of fabricated HEMT device with metal-oxide gate insulator. 80

6.2 Position of the Memristor inside of the HEMT after forming cycle. 81

6.3 Semilog plot of I_d-V_g for the HEMT before and after a single forming cycle. Inset: gate current versus voltage showing increase in leakage currente after forming. 82

6.4 Second forming cycle. 83

6.5 Semilog plots of I_d-V_g for the HEMT showcasing threshold voltage and gate leakage modification with further forming cycles. Numbers indicate amount of forming cycles applied before measurement.......... 83

6.6 Memristance i-v for the HEMT. Source and Drain were tied and used as a second contact.......... 84

6.7 Memristance Ω-q for the HEMT. Source and Drain were tied and used as a second contact.......... 85

6.8 Neuromorphic circuit that generates spikes proportional to input current I_{IN}. 86

6.9 Results of exciting the neuromorphic circuit of Fig. 6.8 with I_{IN} pulses of magnitude $20\mu A$, $150\mu A$, $200\mu A$, and $300\mu A$. For this simulation: $C = 1nF$, $R1 = R2 = 1M\Omega$, and $V = -10V$. Dotted line in last graph added to show position of first peak, illustrating that peak size is increasing.......... 87

LIST OF TABLES

TABLE Page

2.1 Comparison between memory technologies. 13

1. INTRODUCTION

Modern day computing was made possible due to many interesting properties of silicon. For many years the increase in transistor density [1] coupled with other techniques has enabled an exponential speedup in processing power; this has provided us the ability to solve more and more complex problems while at the same time improving accessibility due to the reduced costs.

One area that has greatly benefited from the growth in computing power is machine learning [2], which has the ambitious goal of solving any problems that a human would be capable of while being faster and more efficient (a very useful reference of the current state of the art is given by Steve Furber [3], comparing large scale neuromorphic systems to the human brain). It could be argued that computers are already more efficient than humans for a variety of tasks (such as playing chess [4]), but currently that is not true of *every* task. As a superficial analysis we can look at the raw computational power of a human brain in operations per second: estimates put that value between 10^{12} to 10^{14} operations per second [5].

Comparing that to the amount of instructions per second of a modern processor (around 10^{11}) the value does not seem much larger, but the current computational paradigm requires many instructions to mimic a single brain operation. Comparing the number of instructions needed for a single synapse (around 100 floating point operations [6]) yields a much lower bound of 10^{8} synapses for a single modern day processor and 10^{11} for large scale systems. Since a human brain typically contains 10^{15} synapses [3] we are currently still at least six orders of magnitude away from obtaining the same complexity as a human brain in a single chip; there is also the added complexity of efficiency, since a human brain consumes around 20W of power, which is also orders of magnitude lower than the power used by artificial systems [3].

1.1 The Tail End of Moore's Law

Smaller and application specific machine learning algorithms have had significant progress with the computational power already available in numerous areas from speech recognition to

autonomous vehicles [7]. Still demand for larger algorithms and the introduction of new paradigms is more than enough to push for larger processing capabilities and memory densities; in the past this hasn't been much of an issue since we were comfortable in the knowledge that transistor density was still progressing at an exponential pace. For the past few decades Eq. 1.1 defined the transistor count:

$$T_N \approx T_0 2^{\frac{N}{2}}. \tag{1.1}$$

In this equation T_N is the number of transistors at year n and T_0 is the number of transistors at year zero. In the coming years this may no longer be the case [8, 9, 10, 11]: the enhancement in transistor density is starting to reach fundamental physical limitations. There is still room for improvement; we've been pushing these limits for some time now and keep developing clever new ways to stack more computational power in less area, and the graph in Fig. 1.1 shows that the transistor count keeps increasing to this date, due mainly to the increase in the number of cores, while all other performance aspects have started to reach their maximum level.

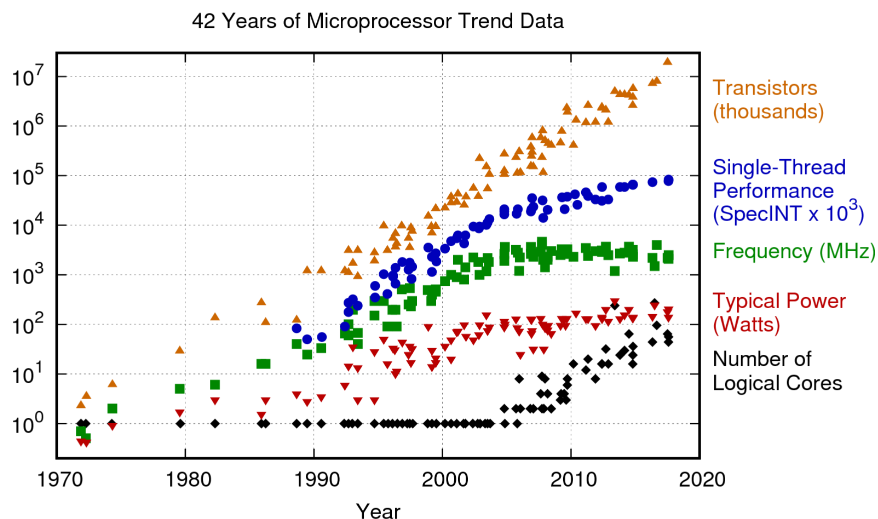

Figure 1.1: Trends in microprocessors until 2017 showing exponential transistor count growth while other performance figures start to plateau. Reprinted from [11] with permission under MIT License.

Thus it is starting to look like that this stacking will sooner rather than later reach its limit and we will need emerging technologies to keep the processing power increasing in an exponential fashion without having an improvement in device density.

1.2 Non-Von Neumann Computing

How we build the vast majority of our computation devices also has a role in this issue. The Von Neumann architecture [12] has shaped computers as we know them; under this paradigm data operations are severely limited by the necessity of fetching the data and the instruction separately, to then after the operation have to save the data back. This limitation is known as the Von Neumann bottleneck [13, 14] and a report places that there are algorithms for which the majority of the time a CPU will actually be waiting for the memory [15]. It is important to mention that many of the machine learning algorithms are also bound by this architecture even though the originating point - the neuron - does not abide by it; this has inspired many designs for neuromorphic computing [16, 17] that can operate on data directly.

To solve some of these problems it was proposed that the Memristor could be applied to new paradigms in computation [18]. It exhibits switching speeds as low as nanoseconds [19] (and in a few cases even below that [20]), reliability [19], cost [21, 22], extremely low switching energy [23], and density [22, 24] that already have found applications not only in neuromorphic computing [25], but in many other fields [26, 27, 28, 29].

1.3 Purpose of This Work

The groundwork for understanding Memristors was provided by Leon Chua in 1971 [30], by outlining constraints and providing examples (albeit done with the help of active components) of what should be the fourth fundamental passive element in circuit theory. His original work was interpreted and reproduced since to narrow the classification some [31, 32], but there is still much debate on what exactly is a Memristor [33, 34] going sometimes as far as say that no examples have been found or that the Memristor itself is not a fundamental passive circuit element. Efforts of modeling the electrical characteristics of fabricated devices have also been met with mixed

success [35, 36, 37, 38].

This work aims to provide a new understanding of how to describe Memristors and to solidify how to engineer and model them; both for specific application design and to understand phenomenological effects that change its behavior. It starts by reviewing the current state of the art in the area and some of the major applications, followed by how currently manufactured structures differ from a hypothetical ideal case; then it explores how to model those differences, what should the ideal case be, and outline the idea for memristance units. Finally, it proposes a novel memristive structure that can act as a Memtransistor - a transistor with a Memristor - that has an underlying High Electron Mobility Transistor (HEMT) which allows it to produce more compact and fast electronic neural networks.

2. MEMRISTOR

In 1971, Leon Chua [30] noticed that from the standpoint of circuits there are four fundamental variables: current i, voltage v, charge q and flux-linkage ϕ. Relations between these are well-known for most cases; between voltage and current we have the resistor, between charge and voltage we have the capacitor and between the flux-linkage and current we have the inductor. There is then a void between flux-linkage and charge: thus Chua postulated that a device must exist to fill it. Fig. 2.1 shows the relationship between the fundamental variables and the circuit elements that connects them.

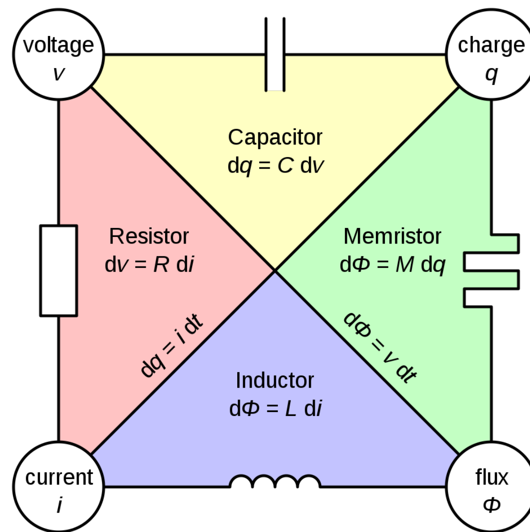

Figure 2.1: Graph illustrating how passive devices connect charge, current, flux and voltage. Art by Parcly Taxel used under CC-BY-SA 3.0.

Chua postulated that this device could be charge-controlled or flux-controlled. The former device would display a relation between flux-linkage and charge dictated by $M(q) = \frac{d\phi(q)}{dq}$ and the latter $W(\phi) = \frac{dq(\phi)}{d\phi}$. These constituent equations give rise to many characteristics that can be used to identify Memristors [31, 39, 32], of which the most known is the pinched hysteresis loop

present in the voltage-current plane. The cause for this is a change in resistance due to the history of charge and/or flux-linkage through the device, which is why the device is dubbed "memory resistor". This hysteresis loop is also known as a "figure 8", shown in Fig. 2.2(a). Additionally the charge-flux-linkage plane is required to not be linear as shown in Fig. 2.2(b).

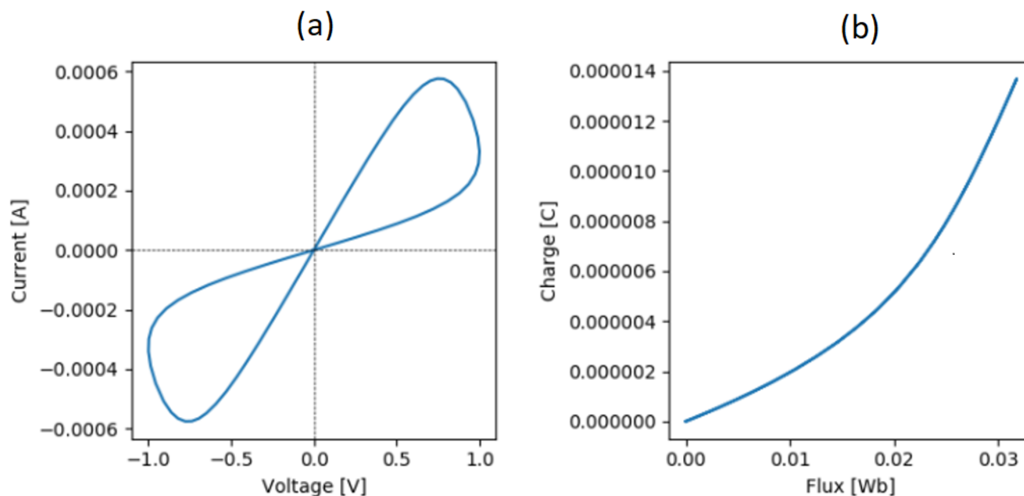

Figure 2.2: (a) i-v plane of a Memristor, showing the pinched hysteresis at the origin and symmetric hysteresis areas in the first and third quadrant. (b) q-ϕ plane of the same Memristor, showing non-linearity.

The applications of this device as memory are very obvious [40, 41], but there are many other functions it can perform: chaotic circuits [42, 43, 44] and cryptography [45, 46] are some of the examples. A particular interest for this work however are its applications in neuromorphic computing [47, 48, 49].

This is because it is reasonable to expect that fundamental elements have good integration densities; in principle it would be easier to achieve greater densities, for instance, of resistors and capacitors than it would be of an amplifier (since one amplifier contains multiple fundamental elements). Thus if a Memristor (or small set of Memristors) can represent a single synapse [49] then

such devices manufactured to current transistor density levels would far outpace current machine learning algorithms performed in a classical computer, driving many on this field of research.

2.1 Physical Device Discovery

The initial theory allowed for a particularly large margin in implementation; it mostly outlined features that would be present in such device leaving most of the constituent equations open and awaiting development. Chua even demonstrated practical implementations of circuits that displayed memristive qualities but they were active, making use of amplifiers and other non-linear devices. Thus since the original proposal of such a device in 1971 researchers were working on developing a two-terminal passive Memristor, with the first major breakthrough appearing in 2008 when a device [50] was fabricated that complied with all of the constraints and thus is called the first Memristor. It is worth noting that the i-v curve of this device looked very different from the expected result illustrated by Fig. 2.2(a); major differences include the existence of an upper and lower boundary for possible instant resistances (R_{OFF} and R_{ON} respectively) and a sharp transition between these two boundaries. These cause the original "figure 8" curve to resemble more the triangular plot of Fig. 2.3.

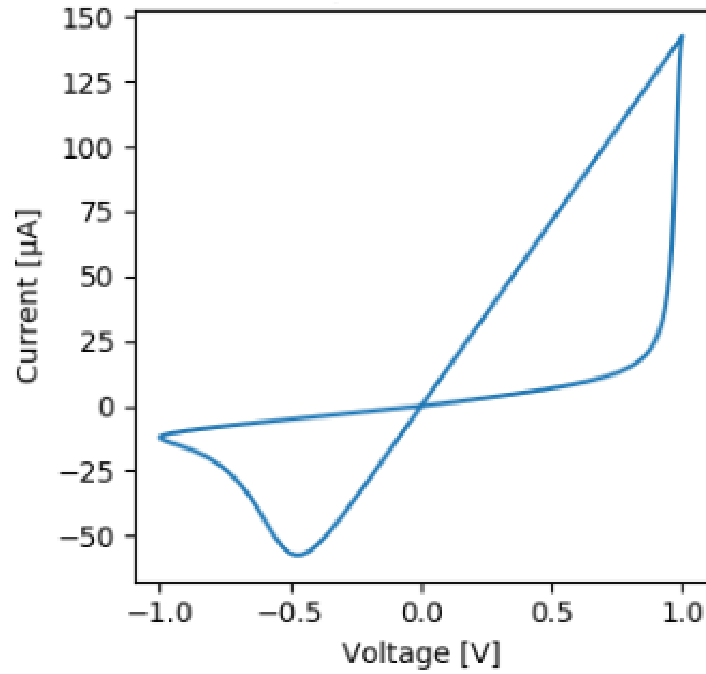

Figure 2.3: i-v plot of a simulation of the first fabricated Memristor.

This device, whose structure is shown in Fig. 2.4, was built using a MIM structure of two platinum contacts separated by a titanium dioxide medium. The mechanism for memristance in this device is believed to be oxygen vacancies [50] contained in the insulator, introduced by its joule heating; since it is then the material responsible for the appearance of a memristance, it is referred to as the *switching medium*.

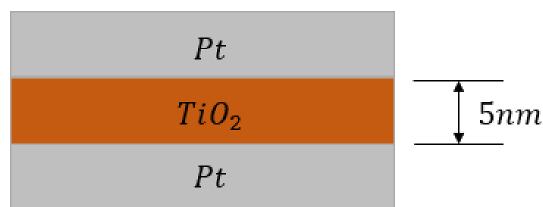

Figure 2.4: Sketch structure of the first fabricated Memristor.

2.2 Memristance Mechanisms

To better understand the causes for these differences one must first understand the mechanism for memristance. There is still some debate to all of the factors that can cause this change in resistance [33, 51, 52, 53, 54] and even to whether all of them can be considered memristance as defined by Chua [33, 34, 54], but many metal oxide Memristors1 operate under the theory that oxygen vacancies are created in the oxide [50] and their drift (or movement of the boundary between stoichiometric and oxygen-deficient oxide) causes a variation in instant resistance between two terminals.

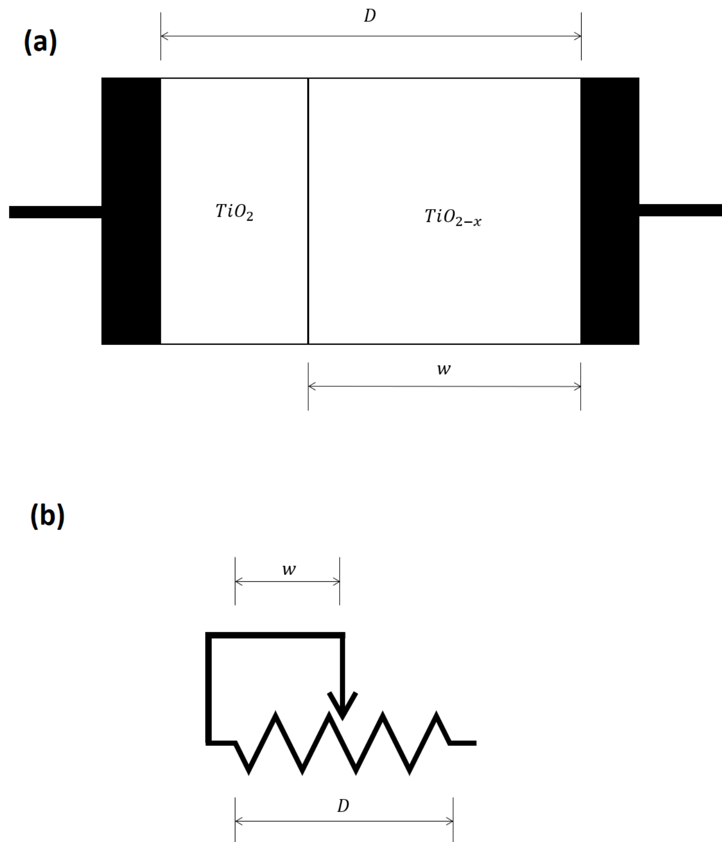

Figure 2.5: (a) Sketch of a simple memristive device depicting an oxygen-deficient layer and its boundary. The location of the boundary w relative to the total thickness D is dubbed State Variable (SV). (b) Analogy with a potentiometer.

The SV w is then the independent variable whose evolution controls all of the aspects of a Memristor. In this particular case, the SV is simply the position of the boundary between stoichiometric and oxygen-deficient layers as seen in Fig. 2.5(a) and a useful analogy is to think of this device as a potentiometer with a center contact having a position w relative to the total length of the resistive strip D which changes as current flows in the potentiometer itself.

In this scenario and considering a resistive strip which provides a linear change in resistance relative to the distance of the center contact to the extremities, the i-v characteristic of the potentiometer would be as in Eq. 2.1, where R_{total} is the maximum resistance and t is time.

$$v = \frac{w(t)}{D} i R_{total}. \tag{2.1}$$

There are two main predicted methods that cause a change in w: the history of charge q and the history of flux-linkage ϕ through the device. In the former case we then aptly classify the Memristor as *charge controlled* and in the latter *flux controlled*. The vast majority of demonstrated devices appear to be charge controlled and the apparent scarcity of truly passive and magnetic controlled Memristors has led to claims that no Memristor has been found yet [33]. These rebuttals will be discussed at a later chapter.

In the case of the charge controlled Memristor then, the SV and consequently the instant resistance is a function of the history of the charge that has gone thorough the device, arriving then at Eq. 2.2.

$$\begin{cases} v = R(w(t))i. \\ w(t) = f(q(t)). \end{cases} \tag{2.2}$$

The evolution of $R(w(t))$ is heavily dependent on its type; for linear ionic drift for instance, Eq. 2.3 fully describes the Memristor by simply multiplying the charge through the device by a factor which depends on the total thickness of the switching layer and the mobility of the dopant μ_V.

$$\begin{cases} v = R(w(t))i. \\ R(w(t)) = \left[\frac{R_{ON}w(t)}{D} + R_{OFF}\left(1 - \frac{w(t)}{D}\right)\right]. \\ \frac{dw(t)}{dt} = \frac{\mu_V R_{ON} i(t)}{D} \implies w(t) = \frac{\mu_V R_{ON} q(t)}{D}. \end{cases} \tag{2.3}$$

Many other mechanisms for memristance have been documented: the previous example concerns drift of ions - more specifically oxygen vacancies [55] - through an amorphous TiO_2 film, but memristance has been also observed as the change in a conductive filament which can be formed by Joule heating [56, 57] or electrochemical redox [58, 59], metal-dopant movement inside chalcogenides [60], trapping of metallic nanoparticles in a polymer [61], conformational changes in single molecules [62], and Mott transitions of an insulator [63]. It is important to stress at this point that each of these mechanisms produces a different evolution of the state variable (due to different phenomenological mechanisms) and thus they have different governing equations; no one global model existed to this point that describes the Memristor.

2.3 Forming Cycle

In certain cases, the switching medium require activation after the fabrication process using a cycle referred to as a forming cycle (FC). During this cycle a high voltage with a low compliance current is applied to the Memristor in order to inject enough energy via Joule heating into the oxide layer such that oxygen atoms are freed from the insulator and can then move depending on the history of charge through the device. An example of such cycle is shown in Fig. 2.6.

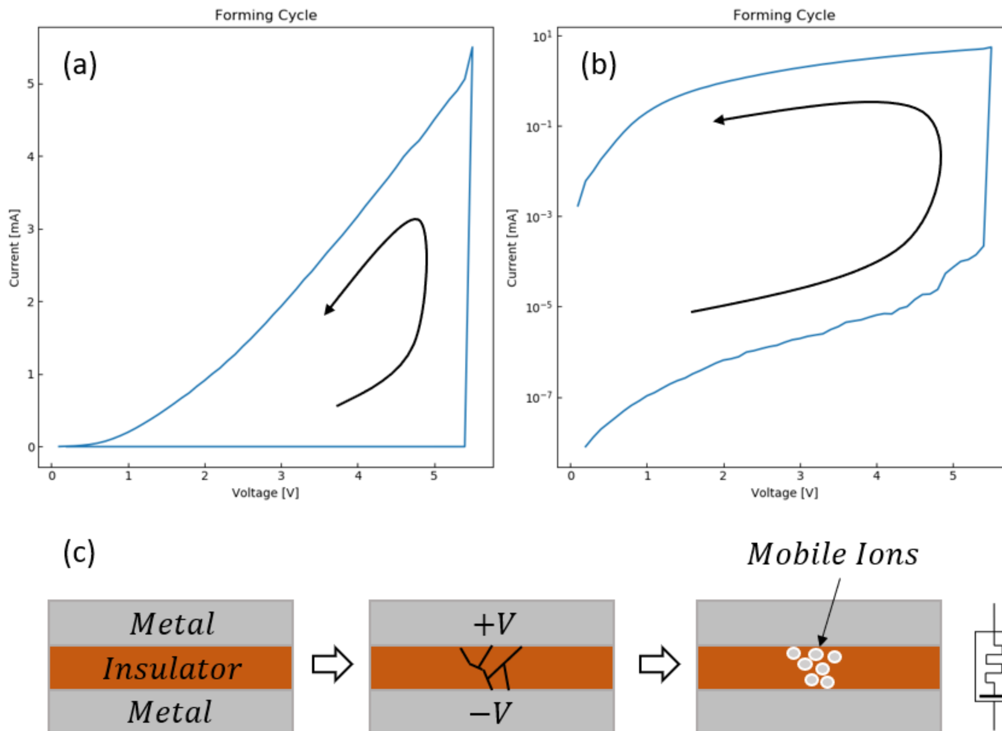

Figure 2.6: (a) and (b) i-v plot of a typical forming cycle for a metal-oxide Memristor. (c) Process sketch showing an initial middle layer going from insulator to switching medium due to application of a breakdown voltage.

In some devices, the FC is reversible by applying an even larger power: this higher temperature instead of creating defects and freeing dopants actually anneals the device and returns it to the original insulating state. These are denominated *unipolar* since switching between high and low resistance state can be accomplished with a signal that does not need to change polarity. As for *bipolar* devices, in general the forming cycle is irreversible; once done, the original insulating characteristic of the switching medium cannot be obtained again and resistance change is simply due to reversing the polarity (and thus the drift) of the applied field. In principle nothing prevents a device of being able to operate both as a unipolar and bipolar device, though usually only one mode of operation is chosen. Devices that do not require a FC are denominated forming-free. For the remainder of this work, unless otherwise noted, Memristors are either forming-free or are being

tested after the forming cycle has been applied to the devices.

2.4 Density

The simplicity and versatility of the structure allows it to achieve great densities, reported being as high as 3.125 $Gbit/mm^2$ [64]; this is an improvement of more than an order of magnitude from DRAM, which for a 20nm process can achieve a density of around 0.15 $Gbit/mm^2$ [65]. Table 2.1 compares current integration density of Memristors as used in memory versus other technologies.

Technology	DRAM	SRAM	NAND Flash	ReRAM (Memristor)
Feature size [nm]	20 [65]	10 [66]	12 [67]	35 [64]
Density [Gbit/mm^2]	0.15 [65]	$\approx$ 0.02 [66]	2 [67]	3 [64]
Read time [ns]	< 10 [68]	< 10 [68]	25000 [68]	$\approx$ 10 [68]
Write time [ns]	< 10 [68]	< 10 [68]	200000 [68]	$\approx$ 10 [68]
Endurance [cycles]	> 10^{15} [68]	> 10^{15} [68]	> 10^{15} [68]	10^5 [68]
Retention time	16ms [68]	N/A	years	years [68]

Table 2.1: Comparison between memory technologies.

These performance figures that can already be achieved in memory applied to neuromorphic chips would represent a fantastic improvement in computational power.

2.5 Current Modeling and Simulation

In order to properly design systems that utilize Memristors it is necessary to model their behavior accurately. This is also particularly important since a proper model will also account for and explain the underlying physical effects responsible for the appearance of a memristance. There are currently many models for Memristors, as each model attempts to fit and explain a particular memristance mechanism [35]; one that stands out models the change in instant resistance measured as being bounded and non-linear [36, 69]. This changes Eq. 2.3 to Eq. 2.4 where p is a positive integer:

$$
\begin{cases}
x(t) = \frac{w(t)}{D}. \\
v = R(x)i. \\
R(x) = \big[R_{ON}w(t + R_{OFF}\big(1 - x\big)\big]. \\
\frac{dx(t)}{dt} = \frac{\mu_V R_{ON} i(t) f(x)}{D}. \\
f(x) = 1 - (2x - 1)^p.
\end{cases}
\tag{2.4}
$$

This window function $f(x)$ guarantees that the velocity of mobile ions approaches zero as the state variable approaches either limit. This model explains the relation between the change in resistance, movement in the boundary of a doped region, and applied current to a level that has it being considered one of the main models for a Memristor. Biolek [36] further solidified its adoption by providing a translation from this mathematical model to SPICE, enabling a widely-used tool to be applied to these new devices.

3. NON-IDEALITY AND MODELING

Despite being widely accepted, the Biolek model fails to fit to many fabricated Memristors that do not display the expected current-voltage plane "figure 8" but still check when compared against the expected fingerprints [31]. Some examples are shown in Fig. 3.1 and exhibit four main characteristics that illustrate the necessity for an expansion of this model: pinch point not at origin [70, 71], non-linear current-voltage relationship in saturation [70, 72, 71, 21], asymmetry of hysteresis loops between quadrants [70, 72, 71], and high leakage currents that do not appear to change the SV[70, 71].

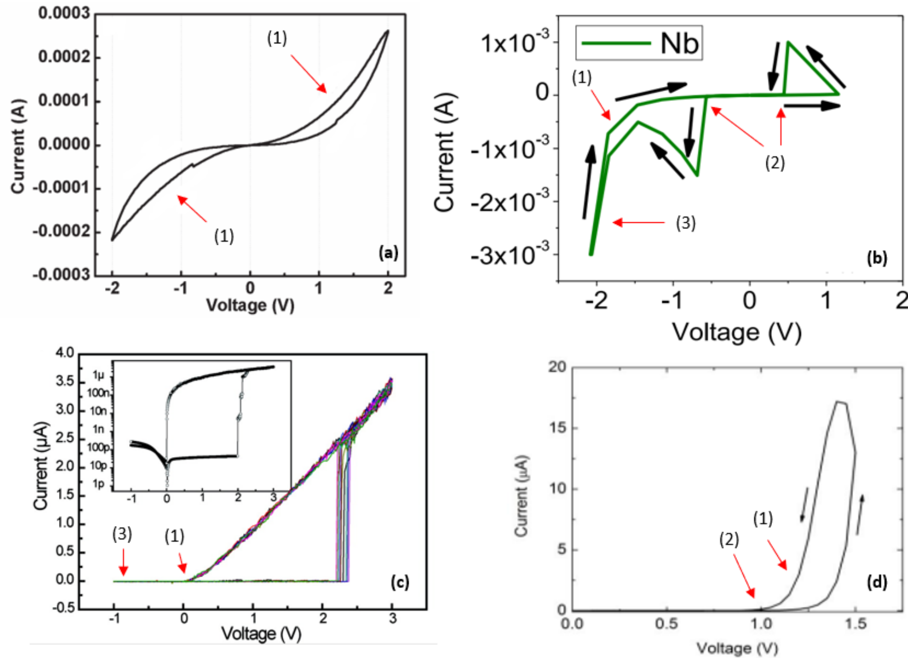

Figure 3.1: Illustration of non-linearities present in many fabricated devices. (1) Non-linear current-voltage relationship in saturation. (2) Pinch point away from origin. (3) Asymmetry of hysteresis loops between quadrants. (4) High leakage currents that do not change SV. (a) Low cost Memristor based on TiO_2, adapted from [21]. (b) TaO_X Memristor, adapted from [71]. (c) Memristor crossbar array, adapted from [72]. (d) Memdiode for neuromorphic circuitry, adapted from [70].

Some of these behaviors were individually explained by previous models [38, 35, 73]; all of them contain non-linear behavior but in general these models make an effort to fit to experimental data observed from fabricated devices, at times neglecting the physical effect that introduces these non-linearities. As a consequence, their major shortcoming is not being able to fit to a variety of devices and driving conditions, being constrained to a single fabricated device under specific bias. Of particular interest is the fact that many of these models have exponential terms in them resembling the current-voltage characteristics of a diode. This is because by analyzing the structure of most Memristors, MIM with two different metals and a metal oxide as an insulator, one arrives at the band diagram shown in Fig. 3.2.

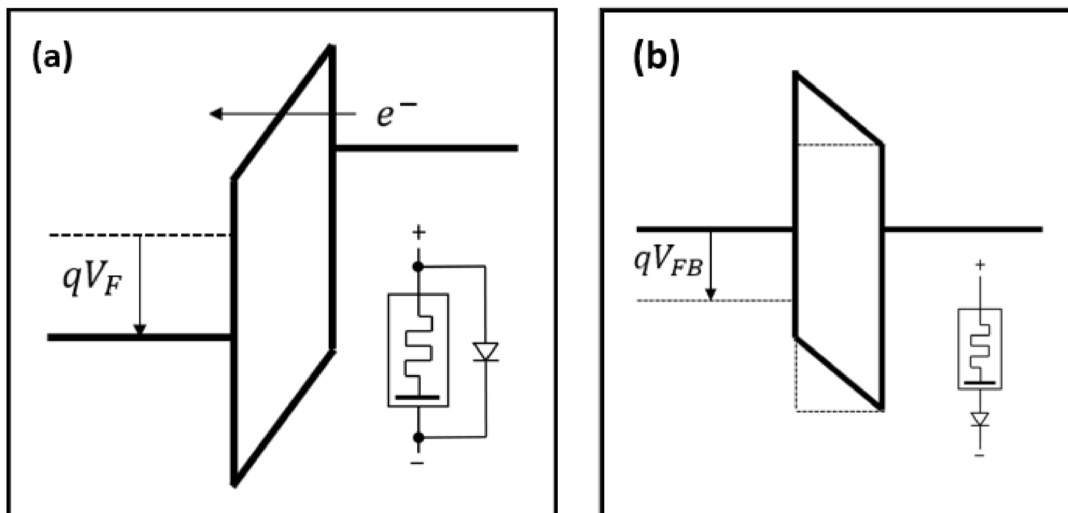

Figure 3.2: Band diagrams of a MIM Memristor. (a) Work function mismatch causing direct tunneling under certain bias conditions. (b) Work function mismatch causing a barrier to appear for injection of charges through the switching medium.

These non-linearities are a consequence of the ability of charges to move in and out of the switching layer and between contacts. The structure of the device then plays a major role in how these leakage and non-idealities show in the Memristor: thinner insulating layers will exhibit direct tunneling of charges from one contact to the other as seen in Fig. 3.2(a). In both in the case of CF or

dopant drift Memristors, at least one of the contacts will be further from the portion of the insulator with the mobile species; this effectively introduces a diode in series with an ideal Memristor, as seen in Fig. 3.2(b). Additionally, a work function mismatch may introduce asymmetries between positive and negative bias (effectively causing different diodes to appear depending on the bias and thus, an asymmetry in the format of the hysteresis).

The presence of these parasitics will heavily alter the i-v characteristics of a Memristor. A similar study was done using passive elements [74], showcasing how the hysteresis area may change due to the addition of capacitors and inductors at different frequencies. That study never included or attempted to explain the non-linear phenomenon however, so it is useful then to explore the effects of various diode configurations with a Memristor. For the following cases the Biolek [36] model was used since it is a very good representation of a non-linear dopant drift, the mechanism which is believed to be the cause for the memristance in metal-oxide switching layers. The first case of interest is where there is an asymmetry to the Memristor structure that results in a diode in series as pictured in Fig. 3.3(a).

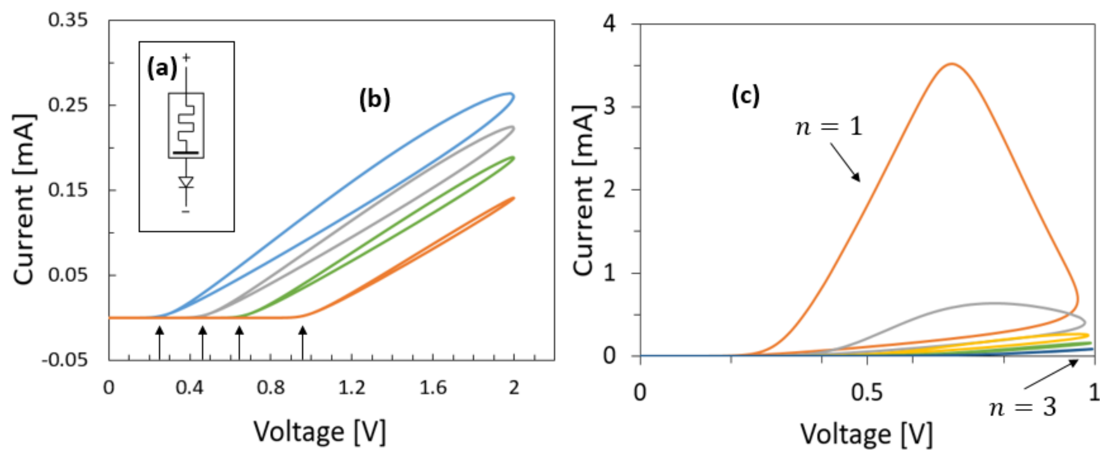

Figure 3.3: Simulations of a diode in series with a Memristor. (a) Circuit representation. (b) First quadrant response for varying built-in potentials: from left to right, 0.3V, 0.5V, 0.7V and 1V. (c) First quadrant response for varying ideality factors.

This is the case for when the Memristor is fabricated with top and bottom electrodes with a

large work function mismatch, if the distance between electrodes is large enough such that there is always a layer in the switching medium which remains insulating (and thus charges must tunnel to the conductive part), for Memristors with a complex structure such as MIIM or Chalcogenides so that charges only affect the switching layer after a certain bias, or for which the mechanism of memristance is a Mott transition. This is because a large potential is required to move switching material charges or to activate relevant transitions. A direct consequence is that if the mismatch is large enough the device will operate only in the first quadrant (unipolar) since no reverse current takes place; in such cases, another mechanism must be present in order to relax the Memristor back to its original state. For instance, in Mott transition Memristors that mechanism is simply the cooling of the switching medium by removing the bias; in some other unipolar devices the CF is destroyed via Joule heating induced by a large stimulus.

What can be seen then in Fig. 3.3(b) is that the built-in voltage V_0 of the series diode has a major impact in the perceived pinch point of the current-voltage plane. The larger the V_0, the further away from the origin the pinch point will be in the first quadrant; not only that, but it also obviously causes a voltage drop that limits charge and flux at the ideal Memristor such that the hysteresis area is smaller for the same driving voltage. Fig. 3.3(c) showcases the impact of different ideality factors. Higher ideality factors strangle the available flux and current for the memristive device, lowering significantly the hysteresis area. Of note is that ideality factors higher than 2 were simulated; this is due to the fact that when fitting to practical devices, many times these values were observed. This has been observed before in both Si [75, 76, 77] and GaN [78] with a variety of causes, so it is reasonable to assume that devices that were not manufactured specifically to be diodes could have such high ideality factors. One can extend this analysis for a second anti-parallel diode, where the curves will extend to the third quadrant with similar effects.

In some cases the switching material is thin enough (or the bias large enough) such that charges can pass through it without affecting the SV, acting as a leakage current. This situation is best represented by the parallel diode shown in Fig. 3.4(a).

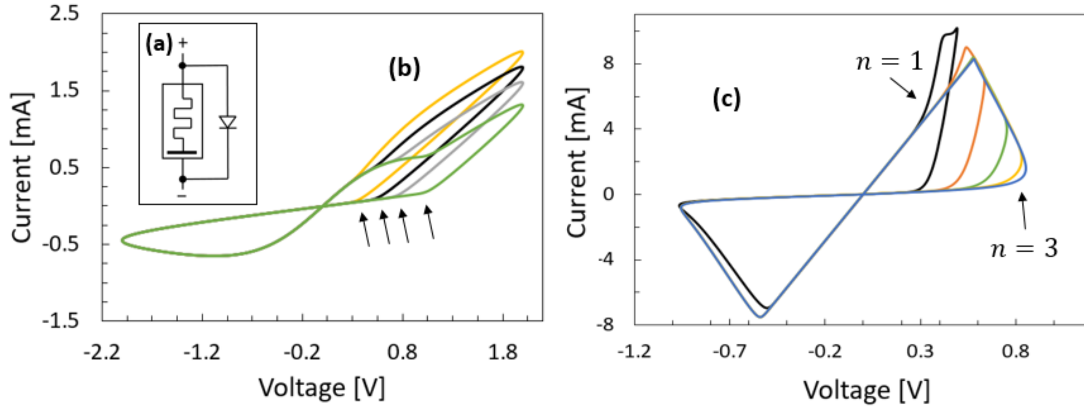

Figure 3.4: Simulations of a diode in parallel with a Memristor. (a) Circuit representation. (b) Response for varying built-in potentials: from left to right, 0.3V, 0.5V, 0.7V and 1V. (c) Response for varying ideality factors.

Once again due to the asymmetric characteristic of the parasitic property, changes in a single quadrant are seen while another quadrant is largely unaffected. The largest impact of a parallel diode is the existence of a secondary path for charges to pass which do not alter the SV of the Memristor. This causes significant alteration on the shape of the hysteresis area in a manner which is inversely proportional to the ideality factor and can cause one to incorrectly identify when the Memristor is changing states; the rise in current is usually associated with the Memristor "turning on" (changing to a lower resistance state), while one can clearly see from Fig. 3.4 (b) and (c) that for various cases, even though the state variable is at a point where it hasn't started changing yet, current is already at significant levels.

Similarly to the case in Fig. 3.3, hysteresis area is significantly altered and an assymetry is introduced between the first and third quadrant. It is possible to neglect the effects of this parasitic however by simply driving the device at levels below where tunneling would occur.

While devices have been observed that can be explained by either only a series diode or a parallel diode, in many cases a combination of both is more adequate. Fig. 3.5 shows two possible combinations of two diodes that result in significant change in the shape and magnitude of the hysteresis area.

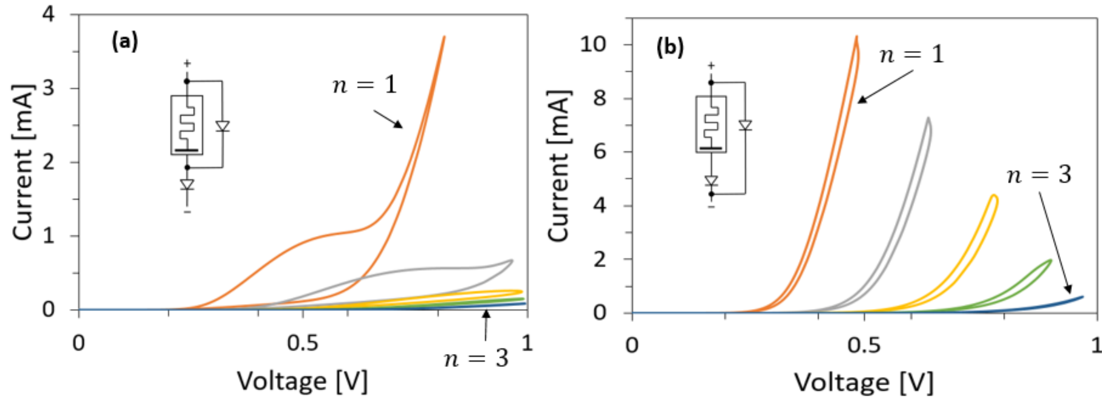

Figure 3.5: Simulations of a combination of diodes with a Memristor. (a) Diode in parallel with Memristor. (b) Diode in parallel with Memristor-diode.

The reader can utilize the knowledge acquired from these simulations to extrapolate for other cases where the alterations are on the third quadrant; all that is necessary is to switch the polarity of the diodes being used. Multiple different combinations of diodes can be used to explain the non-idealities in a Memristor, but there is a format which phenomenologically explains them while remaining relatively simple and effective. It is shown in Fig. 3.6. In it, there are four diodes: two (D_{S_1} and D_{P_1}) are responsible for the changes in the first quadrant (positive bias) while the other two (D_{S_2} and D_{P_2}) are responsible for changes in the third quadrant (negative bias). D_{P_1} and D_{P_2} represent the tunneling current that passes from one metal contact to another in a MIM structure without changing the SV of the switching medium; in general they should be similar diodes, but use of different metals and geometries for each contact may cause them to be significantly different. D_{S_1} and D_{S_2} represent the barrier that exists between each contact and the mobile ions in the switching medium; these will almost always significantly different from each other since usually one contact will be closer to the mobile ions than the other. All of these parasitics are largely affected by all of the process in manufacturing a Memristor, including the forming cycle. The same device subject to a different forming cycle should see differences in the parasitic components.

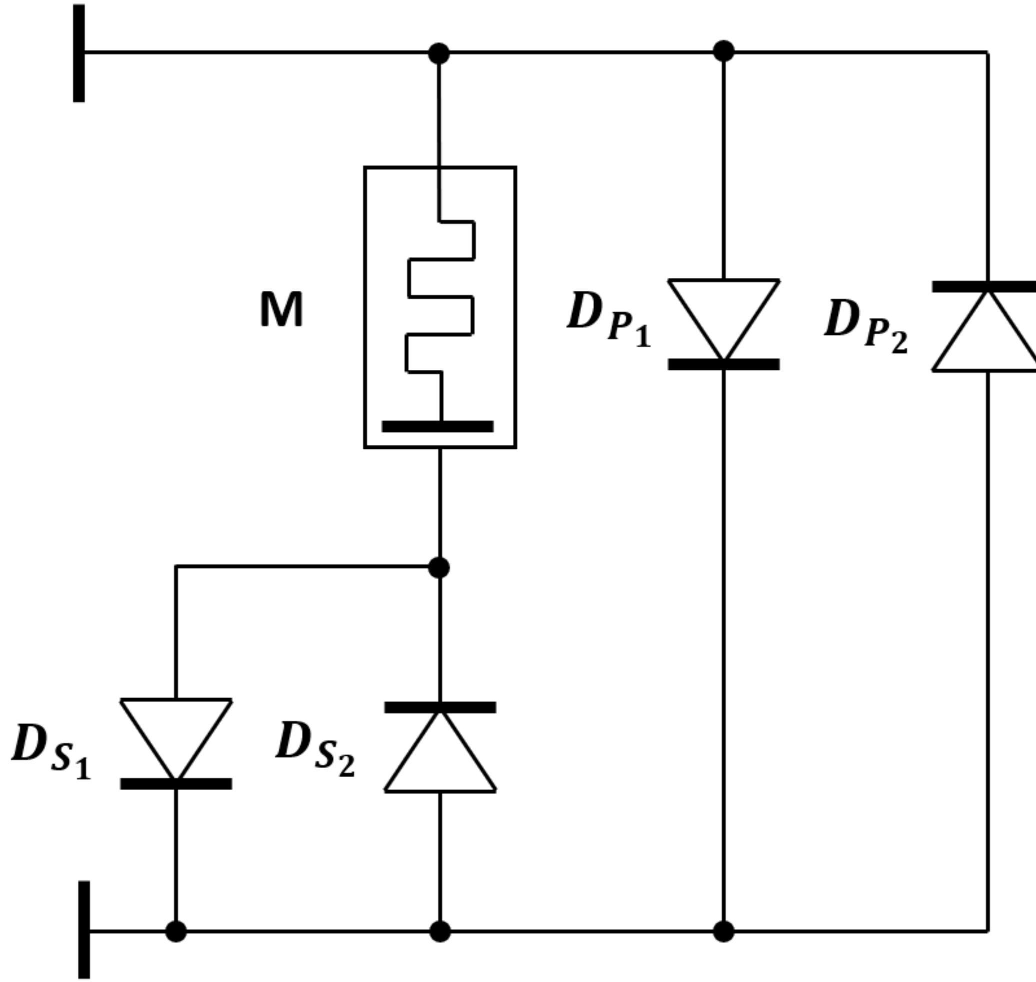

Figure 3.6: Full device model for fabricated Memristors including parasitic diodes.

3.1 Fitting Procedure

To validate the model one can use it to simulate various fabricated devices. Fitting to experimental data is done by iteratively modifying all of the parasitic diodes and comparing the result to the original data: there are five parameters that should be used for the Memristor (R_{ON}, R_{OFF}, R_{INIT}, μ_V, and D) and three for each parasitic diode (V_0, I_S, and n). The leakage conduction path diodes D_{P_1} and D_{P_2} are usually the easiest to fit since they do not alter the state variable and thus appear outside of the hysteresis area. Fig. 3.7 shows how the high currents at the peaks of voltage actually correspond very closely to the parallel conduction path.

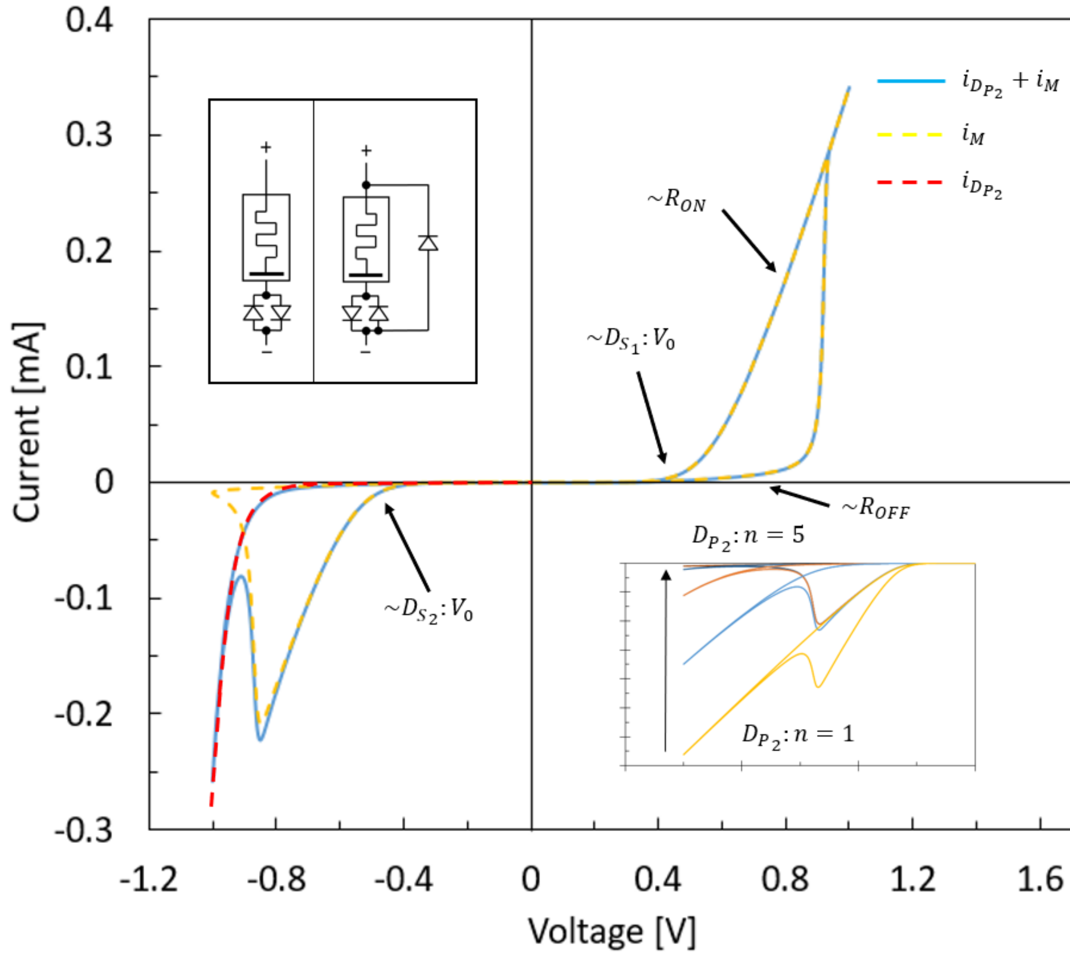

Figure 3.7: Illustration of the parallel leakage path on the diode curve and first approximations for parasitics variables. Upper inset shows the equivalent circuits and lower inset shows impact of changing ideality factor on parallel diode.

Both V_0 for the diodes and R_{ON} and R_{OFF} (or at times R_{INIT}) for the Memristor can be defined closely from the i-v plot as well. All other variables are defined iteratively by analyzing the error between the simulation and the empirical data and doing a gradient descent for each in turn. It is worth mentioning that this method did not always converge, requiring at times manual fitting by trial and error.

3.2 Resulting Fits

Using this model and fitting methodology, Fig. 3.8 shows a Memristor fabricated with Nb_2O_5 for use in neuromorphic circuitry. It showcases how the pinch point is not only away from zero but actually extends all the way to the threshold, exactly as a diode would. For clarity and to further the understanding of how the diodes change the device, the individual currents through both branches are shown as well as the current of the overall device. One can see how a single diode in series with the Memristor fails to explain the device, requiring a second diode in parallel.

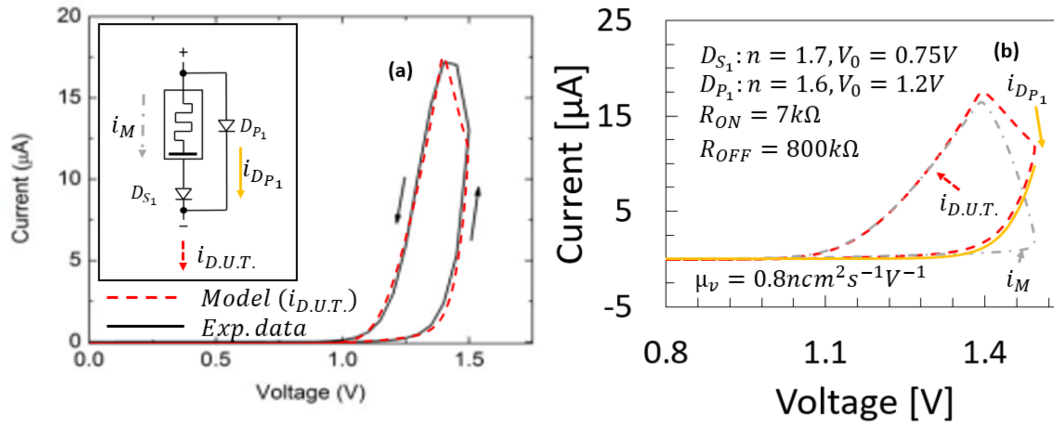

Figure 3.8: Memdiode for neuomorphic applications fit. (a) Fit overlaid in original published data adapted from [70] for comparison. (b) Simulation in LTSpice using the proposed model showing separate branch currents. In this case $n_{D_{S_1}} = 1.7$, $V_{0_{D_{S_1}}} = 0.75V$, $n_{D_{P_1}} = 1.6$, $V_{0_{D_{P_1}}} = 1.2V$, $R_{ON} = 7k\Omega$, $R_{OFF} = 800k\Omega$, $\mu_v = 0.8ncm^2s^{-1}V^{-1}$.

For unipolar Memristors, only a single quadrant has a hysteresis. This is the case of Fig. 3.9, where the asymmetry in the switching material and electrodes can be explained by placing a single "ideal" Memristor in series with a diode. It is important to note in these cases that other methods must be available to modify the state variable of the Memristor back to the original state if it is intended for the device to switch between states. To better illustrate this Fig. 3.9 shows in green how a bipolar Memristor without a the series diode has a hysteresis area in the third quadrant which

"resets" the SV back to the initial state. The presence of the diode (and thus of hysteresis only on the first quadrant) imply that there is no way to force reverse current and thus return the Memristor to that state if the switching medium is bipolar.

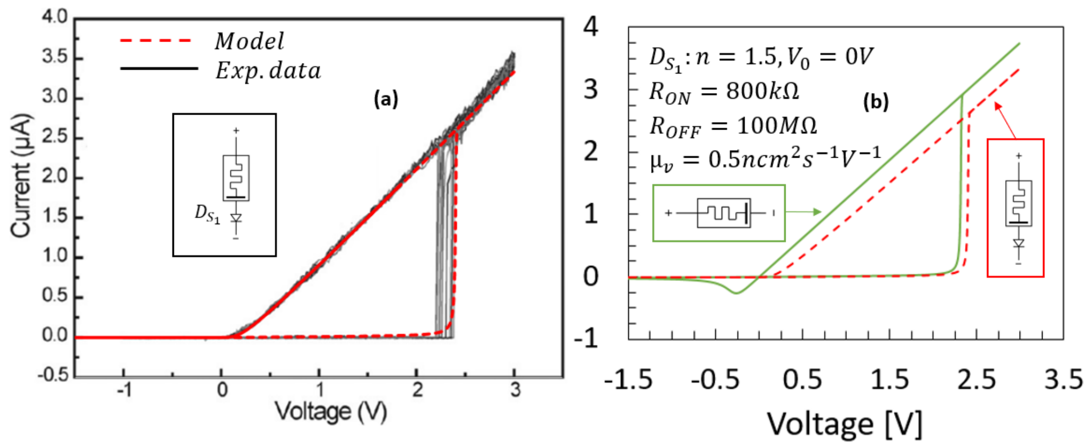

Figure 3.9: Crossbar array for neuromorphic applications fit. (a) Fit overlaid in original published data adapted from [72] for comparison. (b) Simulation in LTSpice using the proposed model. In this case $n_{D_{S_1}} = 1.5$, $V_{0_{D_{S_1}}} = 0V$, $R_{ON} = 800k\Omega$, $R_{OFF} = 1M\Omega$, $\mu_v = 0.5ncm^2s^{-1}V^{-1}$.

Fig. 3.10 shows a Memristor fabricated with two W electrodes and a TiO_2 switching material; this shows how since the device is more symmetric hysteresis now shows in the first and third quadrant making the Memristor *bipolar*. Thus diodes are needed for both forward and reverse conduction, and while the expectation would be for both sets of diodes to be identical because of symmetry, the top and bottom electrodes do not have the same area. This leads to the differences seen in the parameters.

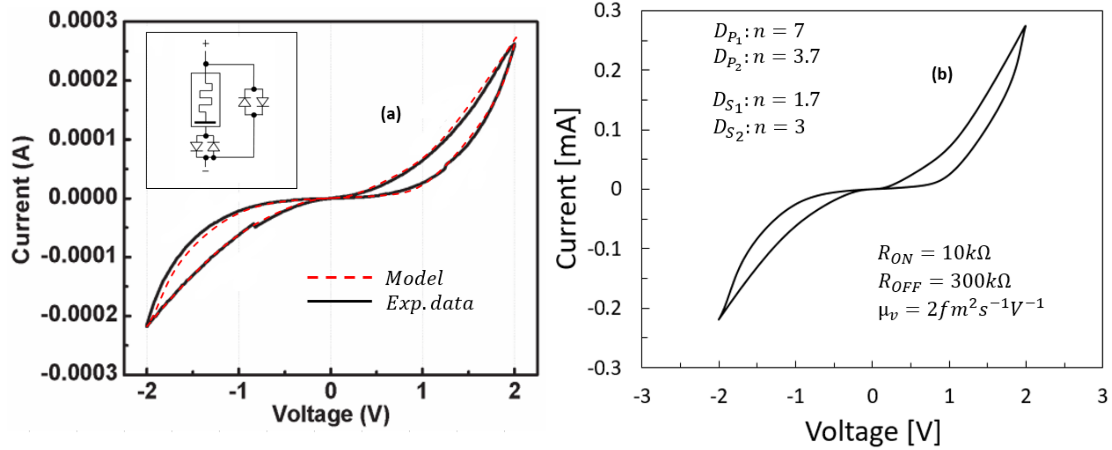

Figure 3.10: Low cost titanium oxide Memristor fit. (a) Fit overlaid in original published data adapted from [21] for comparison. (b) Simulation in LTSpice using the proposed model. In this case $n_{D_{P_1}} = 7$, $V_{0_{D_{P_1}}} = 0V$, $n_{D_{P_2}} = 3.7$, $V_{0_{D_{P_2}}} = 0V$, $n_{D_{S_1}} = 1.7$, $V_{0_{D_{S_1}}} = 0V$, $n_{D_{S_2}} = 3$, $V_{0_{D_{S_2}}} = 0V$, $R_{ON} = 10k\Omega$, $R_{OFF} = 300k\Omega$, $\mu_v = 20pcm^2s^{-1}V^{-1}$.

The necessity for parallel leakage diodes is seen best in Fig. 3.11. This showcases perfectly where there is an asymmetry between first and third quadrant that resembles Fowler-Nordheim tunneling. This is due to the switching material and electrodes being just right so that charges can tunnel directly from one electrode to the other raising the current while not altering the state variable of the Memristor.

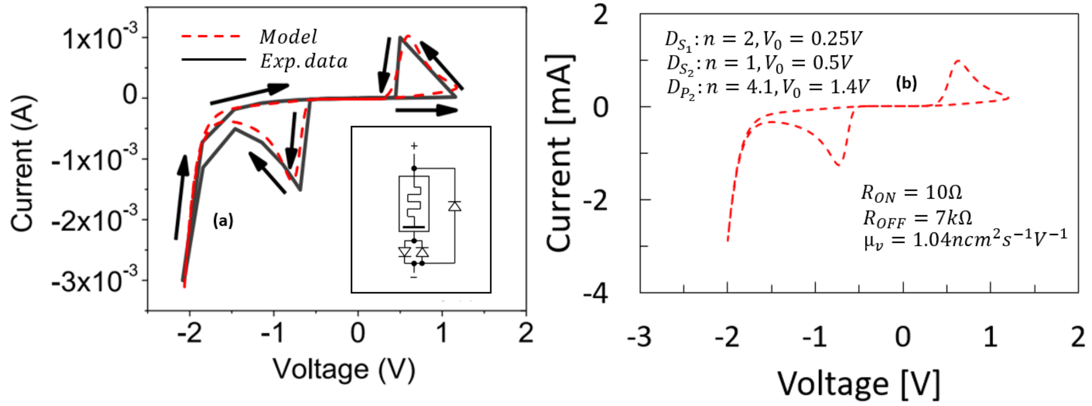

Figure 3.11: MIM Memristor fit. (a) Fit overlaid in original published data adapted from [71] for comparison. (b) Simulation in LTSpice using the proposed model. In this case $n_{D_{S_1}} = 2$, $V_{0_{D_{S_1}}} = 0.25V$, $n_{D_{S_2}} = 1$, $V_{0_{D_{S_2}}} = 0.5V$, $n_{D_{P_2}} = 4.1$, $V_{0_{D_{P_2}}} = 1.4V$, $R_{ON} = 10\Omega$, $R_{OFF} = 7k\Omega$, $\mu_v = 1.04ncm^2s^{-1}V^{-1}$.

Interestingly the model can be used to fit devices where memristance arises from alternate materials such as the ferroelectric Memristor [79] shown in Fig. 3.12. It is worth noting that in this case the model did not fit without alterations between both frequencies; rather it required an individual fit for each frequency, which is reasonable given that the model used assumes a nonlinear dopant drift for the switching material while the actual mechanism for this Memristor is much different.

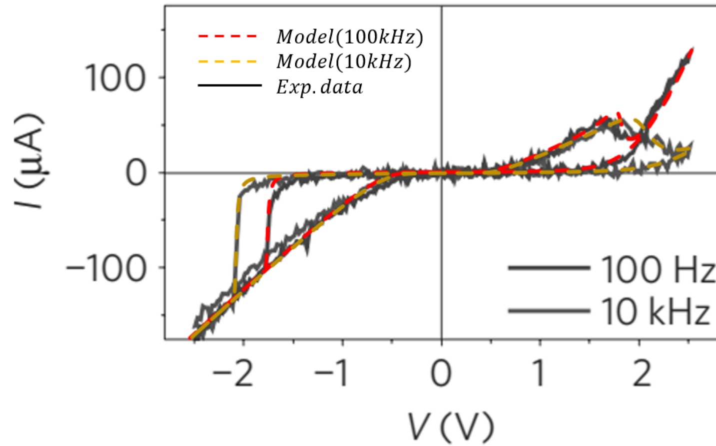

Figure 3.12: Current-Voltage characteristic of a fitted ferroelectric Memristor adapted from [79]. Dashed lines show the simulated model.

It still showcases the power of this model, since it can fit to many Memristors that do not have the non-linear dopant drift model at its core.

3.3 Nonlinear Parasitics Effects

These parasitics are a direct consequence of the physics at play in the manufactured devices. In the absence of a process to obtain Memristors without parasitics, it is very useful to better understand their effect on the device. We begin this study by looking at the impact in hysteresis area, defined as being the area enclosed by the pinched loop. There are essentially two hysteresis areas for a Memristor since they should pinch at zero: one in the first quadrant and one in the third. Evaluating this area is important since it is a metric for the Memristor and should in theory have a *peak* area at a single frequency [31]. Fig. 3.13 shows how this calculation can be done in the first quadrant (with the third quadrant being a simple extension of the method) by separating the loop into two sections: the first is from the origin until the point of maximum voltage and the second is from the point of maximum voltage back to the origin. By taking the difference of the area under the curve for these sections one can find the area enclosed by the "figure 8".

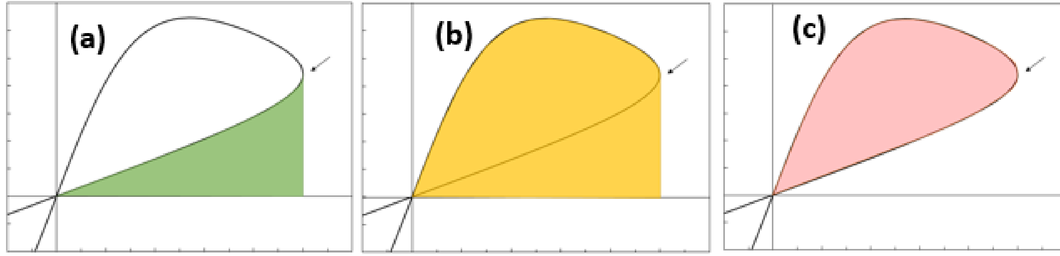

Figure 3.13: Methodology for calculating hysteresis area in a quadrant. Arrow points to maximum excitation voltage. (a) Integration of first half of positive swing (zero to maximum voltage). (b) Integration of second half of positive swing (maximum voltage back to zero). (c) Resulting hysteresis area due to simple subtraction of areas.

Fig. 3.14 shows the hysteresis area of both quadrants of an ideal Memristor as simulated by the Biolek model. One can clearly see a peak as predicted in [31] with a monotonic decrease in area with increasing frequency, to a point where the area is negligible.

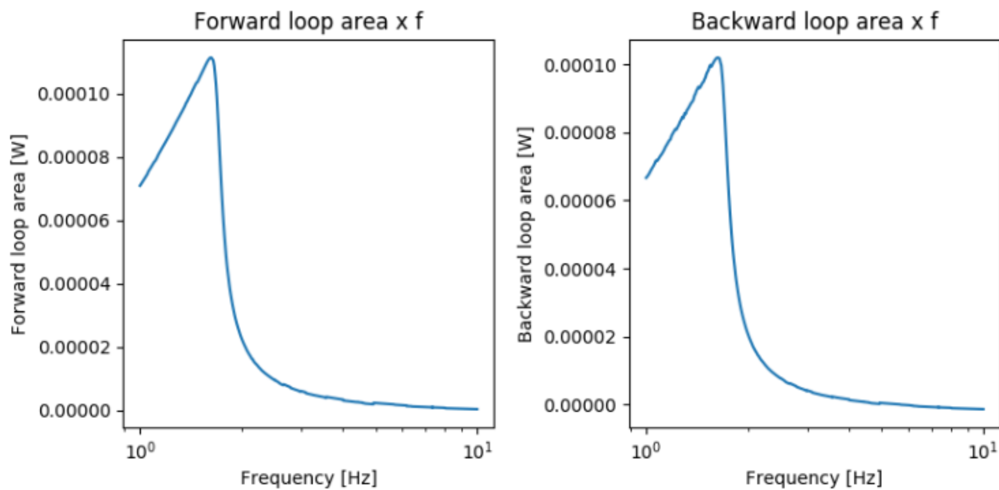

Figure 3.14: Magnitude of hysteresis area versus frequency for a Memristor.

In theory if the Memristor is being driven symmetrically then the area for first and third quadrants should match; this is true as long as other major effects (such as forming, saturation, and

parasitics) are negligible. This is not always the case; Fig. 3.15 shows how in certain cases, shape and magnitude of the area will drastically change due to non-idealities.

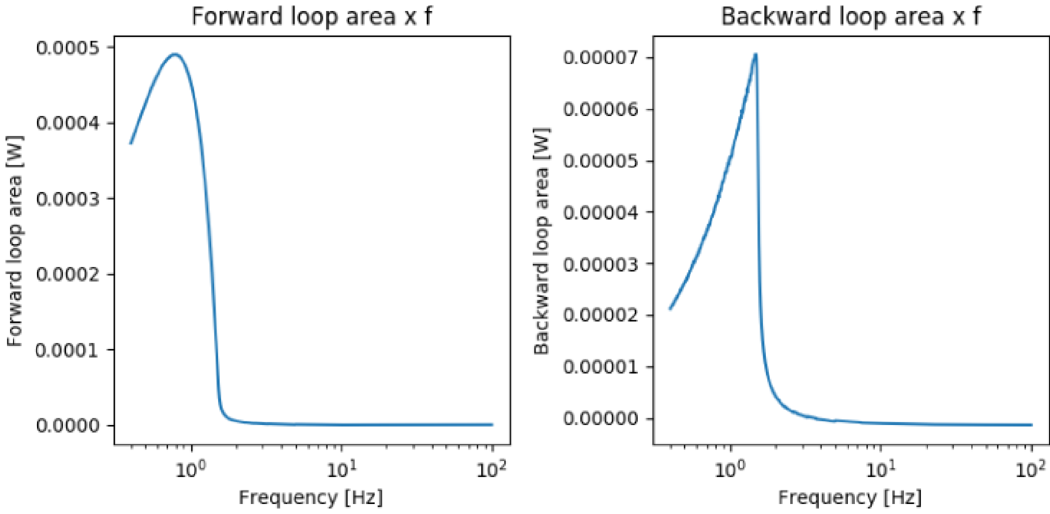

Figure 3.15: Magnitude of hysteresis area versus frequency for a Memristor which exhibits many non-idealities such as saturation.

Fig. 3.16 shows how the i-v curve looks for the Memristor of Fig. 3.15. The first quadrant shows a large area of hysteresis while the third quadrant shows a significantly lower area.

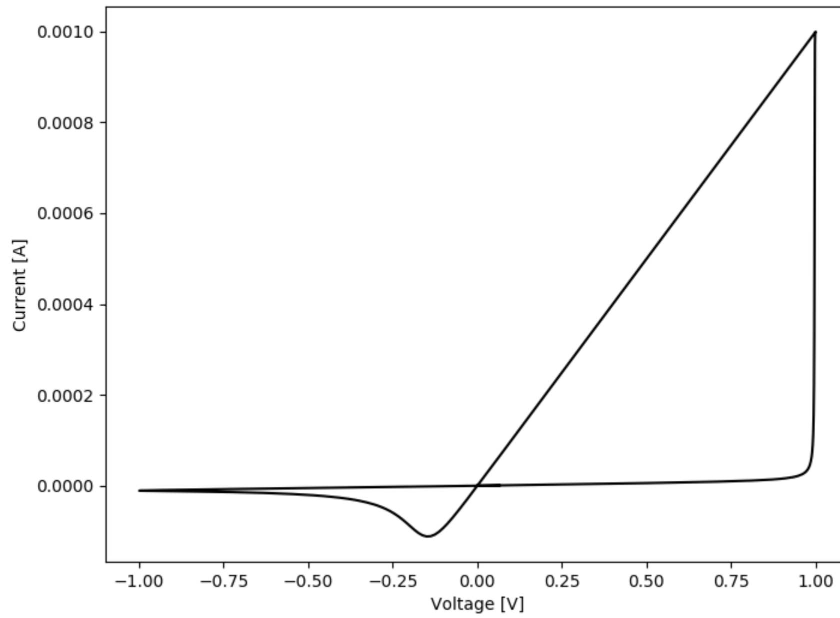

Figure 3.16: i-v curve for a frequency of 1Hz for Memristor of Fig. 3.15.

This is further enhanced by looking at how diodes change the area, shown in Fig. 3.17. In it, we can see how their addition in series with the Memristor lowers the area profile significantly (which is expected since they will lower the current that passes through the device) and also *changes the frequency for which the peak area appears*. This is particularly interesting because this means that the area of the hysteresis loop, which has a use in the characterization of the device [80], depends both on switching medium and the parasitic diodes that are inherently present in the fabricated device.

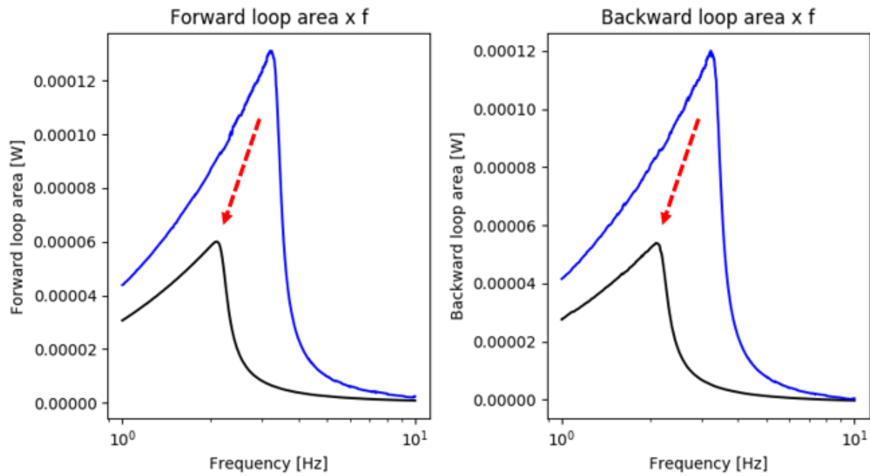

Figure 3.17: Magnitude of hysteresis area versus frequency for the Memristor of Fig. 3.14 altered by anti-parallel diodes of $n = 1$ in series with it.

A more complete analysis is shown in Fig. 3.18 and presents the same findings: the peak frequency area changes depending on the ideality factor of the parasitic diodes in series with the Memristor (those that represent the barrier height in transferring charges to the switching medium). Fig. 3.19 shows the effects of a parallel diode, which appear to cause similar effects.

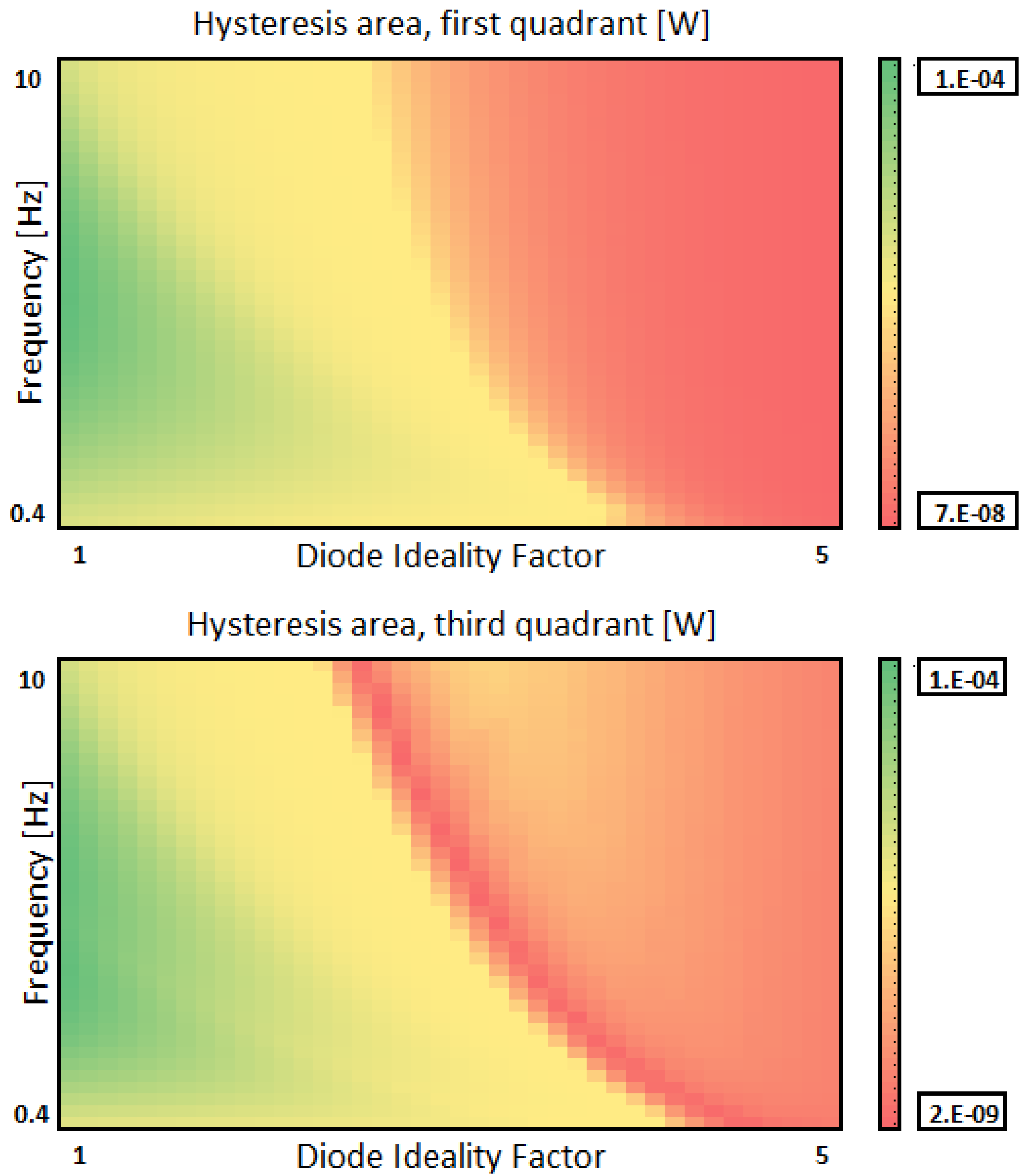

Figure 3.18: Result of the simulation showcasing hysteresis area change because of anti-parallel diodes in series with a Memristor.

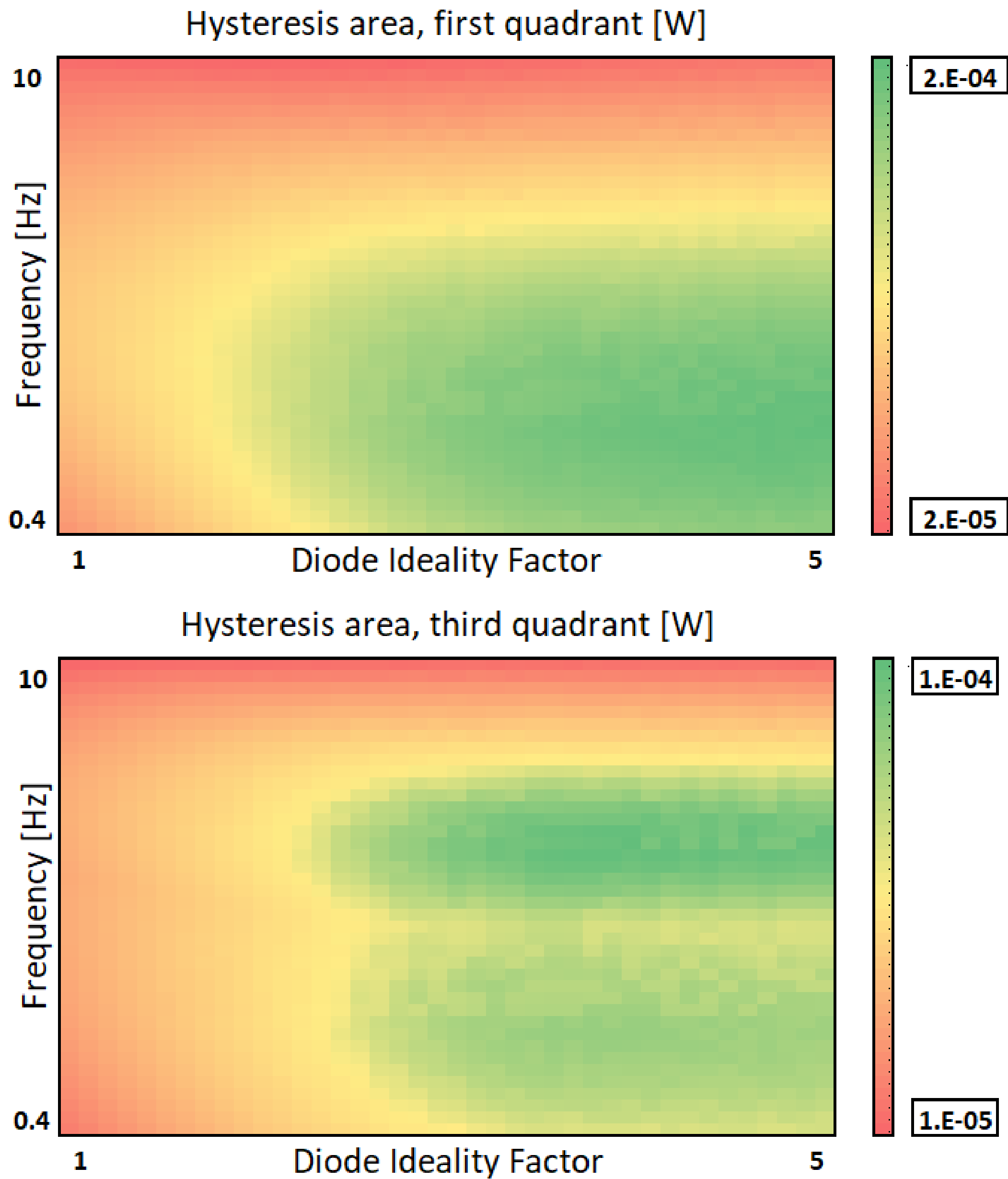

Figure 3.19: Result of the simulation showcasing hysteresis area change because of anti-parallel diodes in parallel with a Memristor.

One of the characteristic fingerprints of the Memristor is that the pinch (where the rotation of the i-v curve changes from clockwise to counter-clockwise and vice-versa) should be at the origin [31]; some tests however may show that even though there is a pinch, it is not at zero. This work has already demonstrated how embedded diodes in the structure can shift this point by a certain

voltage, but some high frequency tests produce shifts both in voltage and in current. This is usually because of reactive parasitics [74] (usually capacitive due to the nature of the device). Series diodes however seem to amplify this behavior, as illustrated by Fig. 3.20.

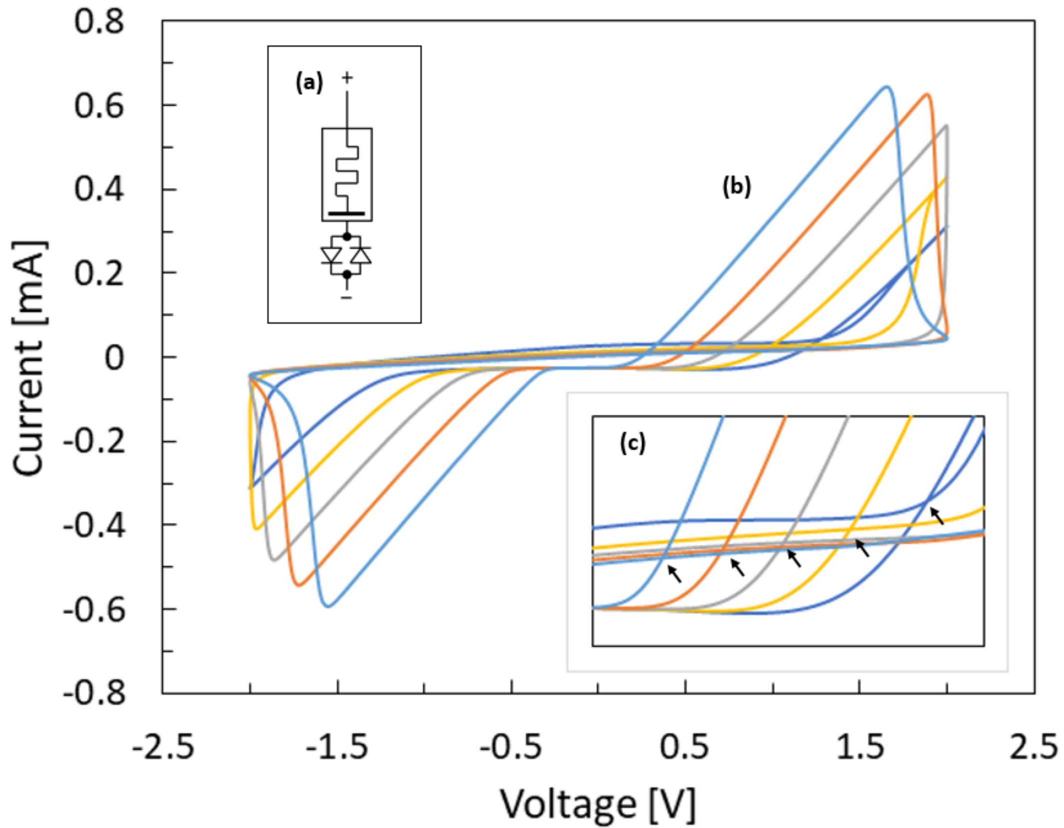

Figure 3.20: Result of the simulation showcasing pinch point change for a variety of ideality factors. (a) Circuit being simulated. (b) Simulation result. (c) Zoom of pinches with arrow pointing to pinch.

Fig. 3.21 show how this pinch point shifts due to frequency and diode ideality factor for the series case.

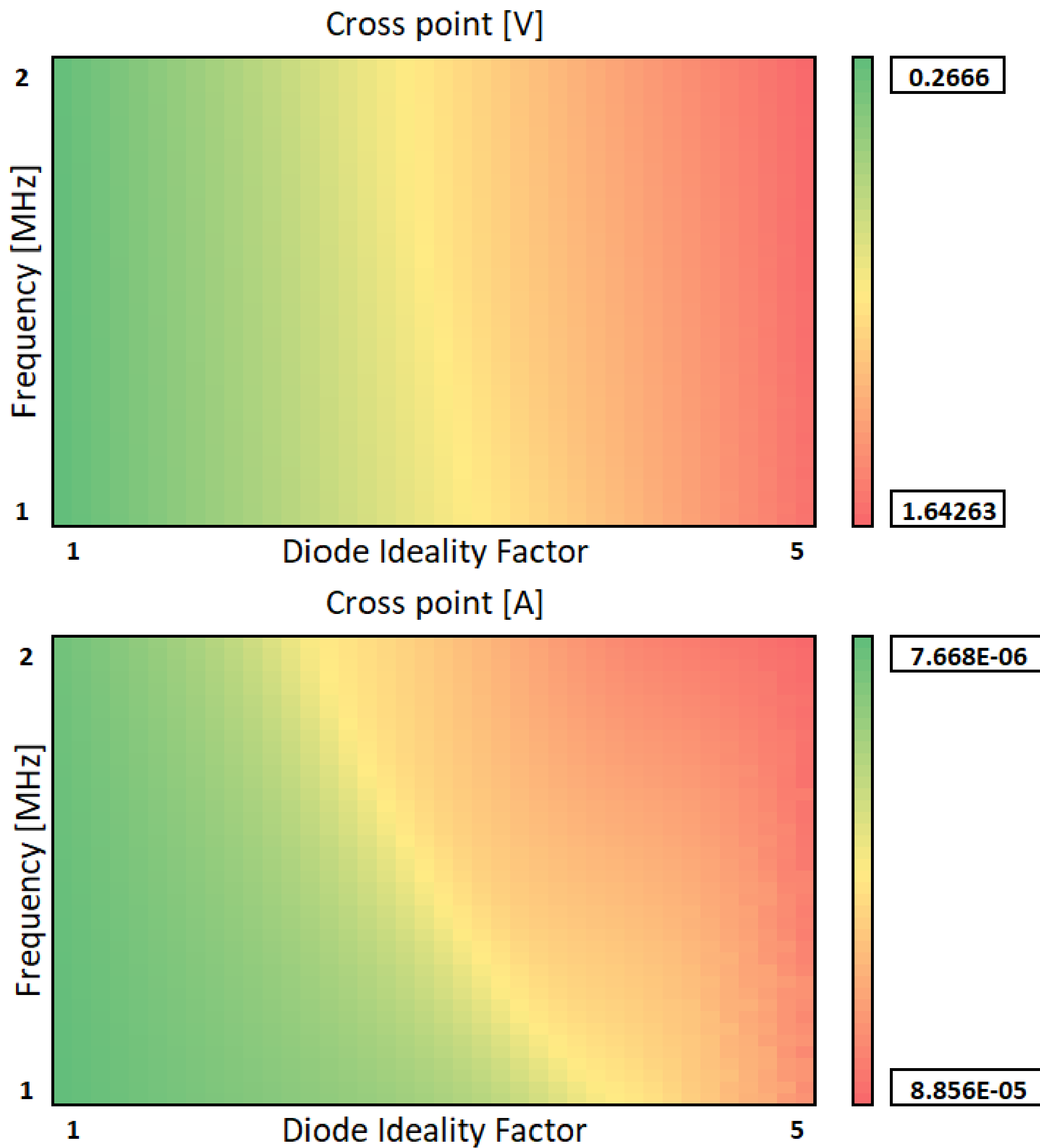

Figure 3.21: Result of the simulation showcasing pinch point change as function of series diodes ideality factor and driving frequency.

As expected, the voltage shift in the pinch point is due almost exclusively due to the diode, although there is a contribution by the frequency as noted by the slight slope in the heat map. The current shift however responds proportionally to both frequency and the diode ideality factor. This is particularly interesting because it can be used to characterize the parasitic diodes in a fabricated memristor: by evaluating the amount of shift in both voltage and current of the shift point for

certain frequencies, it is possible to determine the presence of a diode.

Thus the characteristics of the parasitic diodes manufactured with the Memristor play a fundamental role in its operation and cannot be ignored. As a result, manufacture of devices should also pay attention to both the material choices and switching mechanisms to properly engineer the device instead of focusing solely on the Memristor.

The ability of a simple underlying model such as the non-linear dopant drift to fit to a variety of other devices by the addition of parasitics raises both the question of whether it is possible to characterize most (if not all) devices using a unique standard tailored to Memristors and whether there is a fundamental linearity that hasn't been found yet.

4.1 Symmetry Between Fundamental Circuit Elements

It is worth noting that the "figure 8" displayed in Fig. 2.2(a) may look familiar to the reader to a certain extent. This is because if sufficient power is applied to a self-heating thermistor, the i-v curves of Fig. 4.1(a) will be obtained.

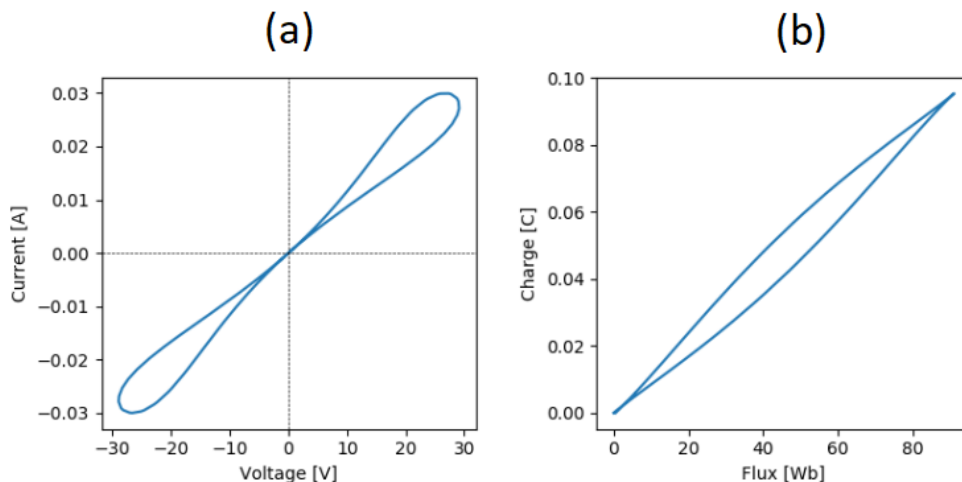

Figure 4.1: (a) i-v plane of a NTC thermistor that self-heats, showing hysteresis. (b) q-ϕ plane of the same thermistor.

The i-v characteristic does appear similar, and the device even passes some of the fingerprints for Memristors [31]; there are however a few fundamental differences between these devices. The first and perhaps most important being that the state variable that controls the change in resistance

is temperature; this enables the device to return to its initial state (in this case likely the room temperature state) simply by ceasing to apply power. Second, the state variable can only change unidirectionally: it is impossible to decrease the temperature by applying a reverse bias. These differences are visible in Fig. 4.1(b) which shows how the q-ϕ plane is no longer bijective, meaning the state of the system cannot be described simply by the history of charge and flux-linkage alone, requiring another variable (in this case temperature).

Other fundamental elements however can display similar figures; this reinforces the argument for symmetry, where different elements can display analogous characteristics in alternate planes. For instance, capacitors are linear in the q-v plane while resistors are linear in the i-v; this is important because if the Memristor is a fundamental element, it also must have symmetries to all of the other elements. To illustrate this point, Fig. 4.2 showcases a capacitor with an initial condition being driven by a sinusoidal current source.

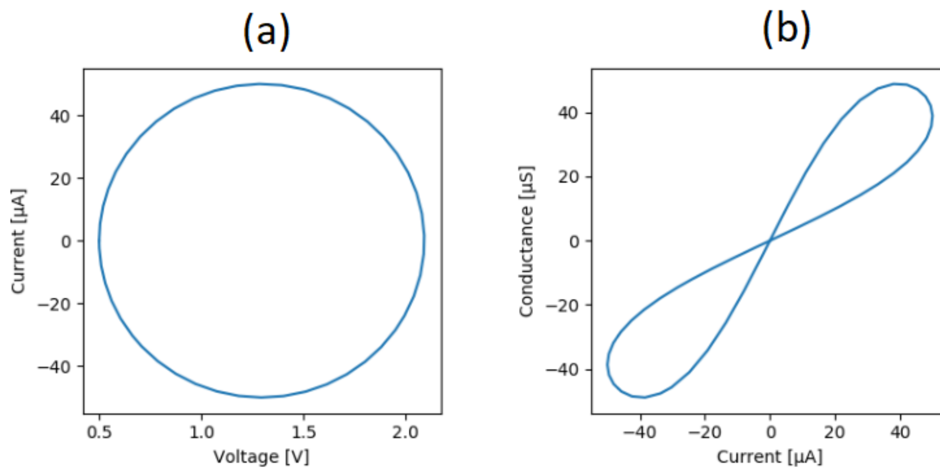

Figure 4.2: (a) i-v plane of a capacitor with an initial condition of 0.5V. (b) Conductance-i plane of the same capacitor.

Fig. 4.2(a) shows that the current and voltage are out of phase by exactly 90 degrees, which is why the result is a circle. In Fig. 4.2(b) however one can easily see how a linear device can display

a "figure 8" when looked in a different plane. Fig. 4.3 shows these curves when plotted together in three dimensions and their projections.

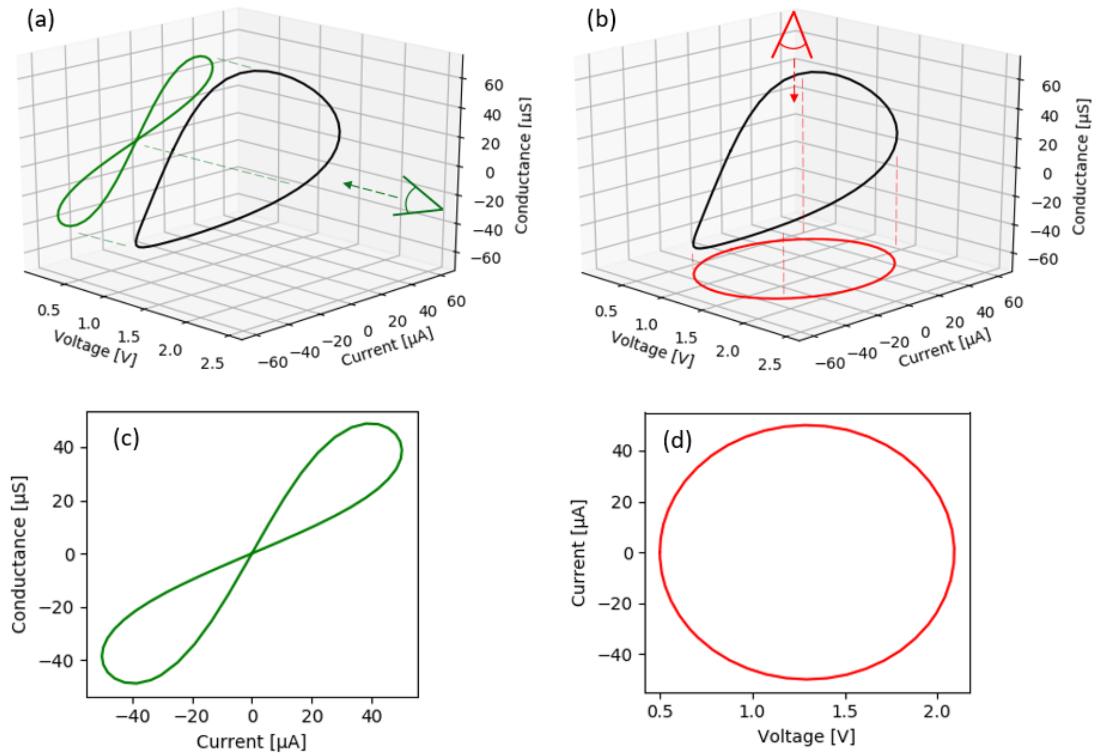

Figure 4.3: (a) 3D plot of a capacitor showing projection in Conductance-i plane. (b) 3D plot of a capacitor showing projection in i-v plane. (c) Conductance-i plane projection. (d) i-v plane projection.

The situation is analogous to the inductor as can be seen in Fig. 4.4, which has an initial current and is being driven by a sinusoidal voltage source. There are significant differences in the fact that now the figure 8 appears in another plane (the Ω-v plane); this is mainly due to the nature of the fundamental element, the driving source, and how it behaves according to its initial condition. It still maintain the same features seen in Fig. 4.3 in different axes.

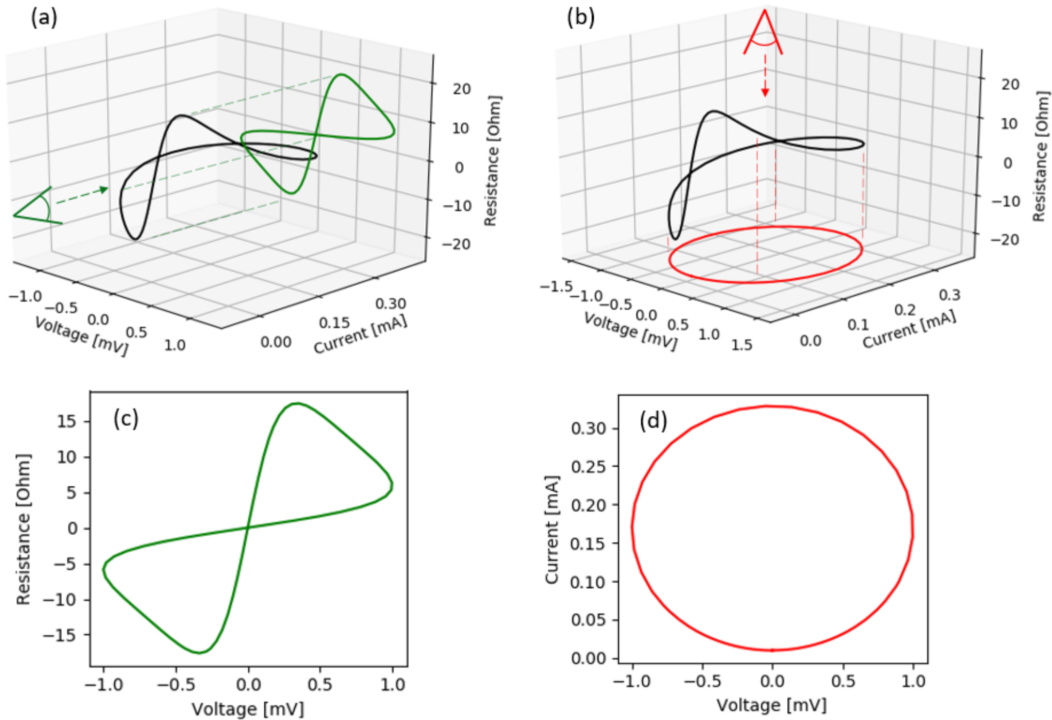

Figure 4.4: (a) 3D plot of an inductor showing projection in Ω-i plane. (b) 3D plot of an inductor showing projection in i-v plane. (c) Ω-i plane projection. (d) i-v plane projection.

So if the Memristor is indeed fundamental it is reasonable to expect that it will be similar to Figs. 4.3 and 4.4. Fig. 4.5 shows the case of a charge-controlled Memristor with an initial resistance being driven by a sinusoidal current source. One can easily see that once again the projections are similar but occur in alternate axes. In this sense one can visualize different fundamental elements as set rotations in this three-dimensional plane. The case of the flux-controlled Memristor is analogous.

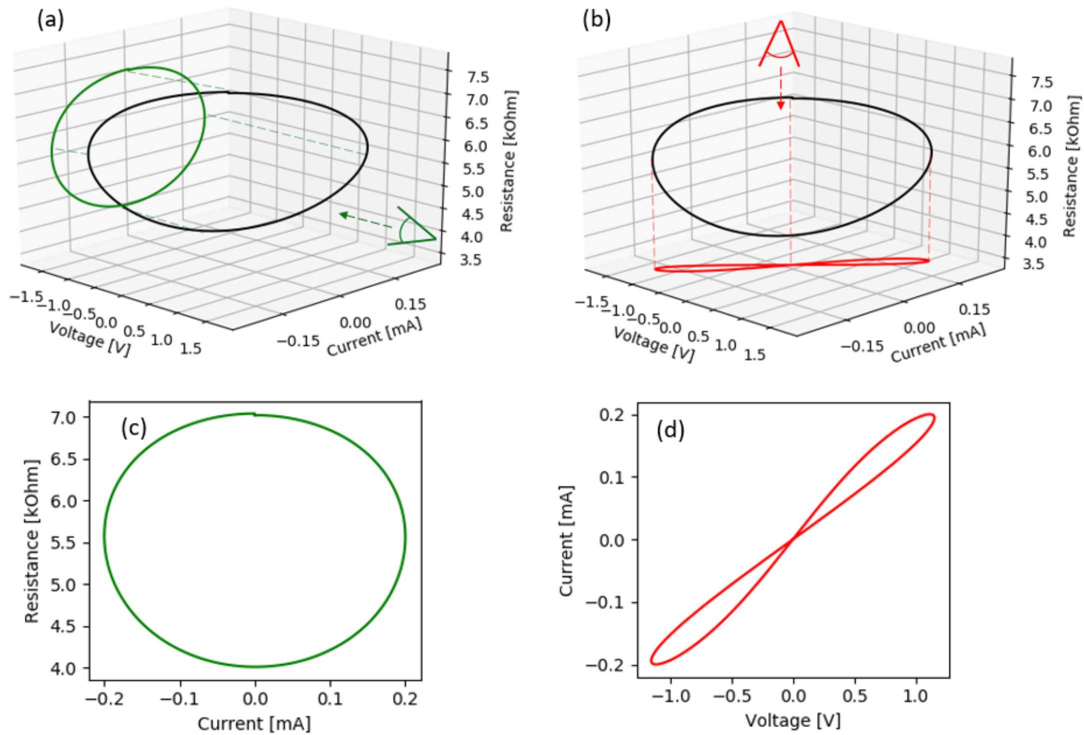

Figure 4.5: (a) 3D plot of a Memristor showing projection in Ω-i plane. (b) 3D plot of a Memristor showing projection in i-v plane. (c) Ω-i plane projection. (d) i-v plane projection.

This can be confusing at first because the first two devices are known to be linear: for the capacitor, $q = Cv$ where C is the capacitance in Farads; for the inductor, $\phi = Li$ where L is the inductance in Henrys. However for the Memristor no linearity was ever required for it to exist; many of the constituent equations actually demand non-linearity. This fact was brought up by Abraham [34] in a rebuttal that states "linearity is central to being fundamental". Fig. 4.5 however implies that there must be some sort of linearity as it generates curves analogous to linear devices.

In this context it may also be interesting to look at a device that is not fundamental, such as the thermistor shown in Fig. 4.1, in the same light to illustrate how the symmetries are not maintained in this case. Fig. 4.6 shows the same three-dimensional plot illustrating how the symmetry now does not exist on the device, which actually displays "figure 8" plots in all planes.

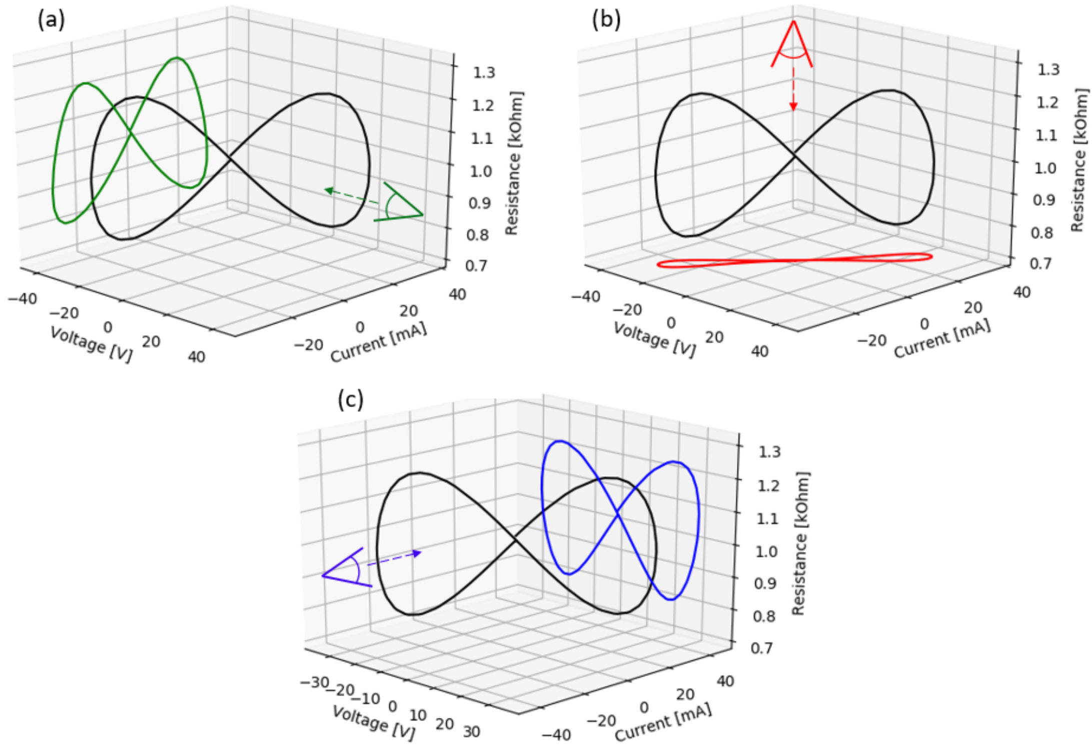

Figure 4.6: (a) 3D plot of a NTC thermistor showing projection in Ω-i plane. (b) 3D plot of a NTC thermistor showing projection in i-v plane. (c) 3D plot of a NTC thermistor showing projection in Ω-v plane.

4.2 Memristor Linearity

If there is indeed a linearity to the fourth fundamental element, we must still abide by the most fundamental relationship (in this case of a charge-controller Memristor):

$$M(q) = \frac{d\phi(q)}{dq}. \tag{4.1}$$

In this equation $\phi = \int_{-\infty}^{t} v(\tau)d\tau$ is the flux-linkage and $q = \int_{-\infty}^{t} i(\tau)d\tau$ is the charge history through the two-terminal device. It is already established that $M(q)$ cannot simply be a constant. Suppose for instance that $M(q) = R_1$: this would yield a simple resistor and has already been explored by previous work [34]. It is important to note here that there are infinitely many choices of the function $M(q)$; however since the main argument is that a linearity must exist somewhere

we pick

$$M(q) = M_1 q + R_1, \tag{4.2}$$

where M_1 and R_1 are constants. This yields

$$\int M_1 q + R_1 dq = \int d\phi. \tag{4.3}$$

$$\frac{M_1 q^2}{2} + R_1 q + K_1 = \phi + K_2. \tag{4.4}$$

$$\frac{d}{dt}(\frac{M_1 q^2}{2} + R_1 q + K_1) = \frac{d}{dt}(\phi + K_2). \tag{4.5}$$

$$M_1 q i + R_1 i = v. \tag{4.6}$$

$$v = (M_1 q + R_1) i. \tag{4.7}$$

Thus the device operates as a resistor whose resistance depends on an internal state variable: the history of charge that has passed through the device. This will produce a pinched hysteresis as seen in Fig. 2.2. More importantly however it allows us to classify and identify the Memristor with respect to the magnitude of M_1, as it is done with all of the other fundamental elements. A similar analysis can be done for flux-controlled Memristors, which would result in

$$i = (W_1 \phi + \frac{1}{R_1}) v. \tag{4.8}$$

Memristors that have this linearity can thus be described by finding the values of M_1 and R_1. The unit for M_1 is $\frac{\Omega}{C}$ and this work proposes that it be named Chua $[Ch]$ after the original work that predicted its existence [30]. A typical graph for identifying these quantities is shown in Fig.

4.7.

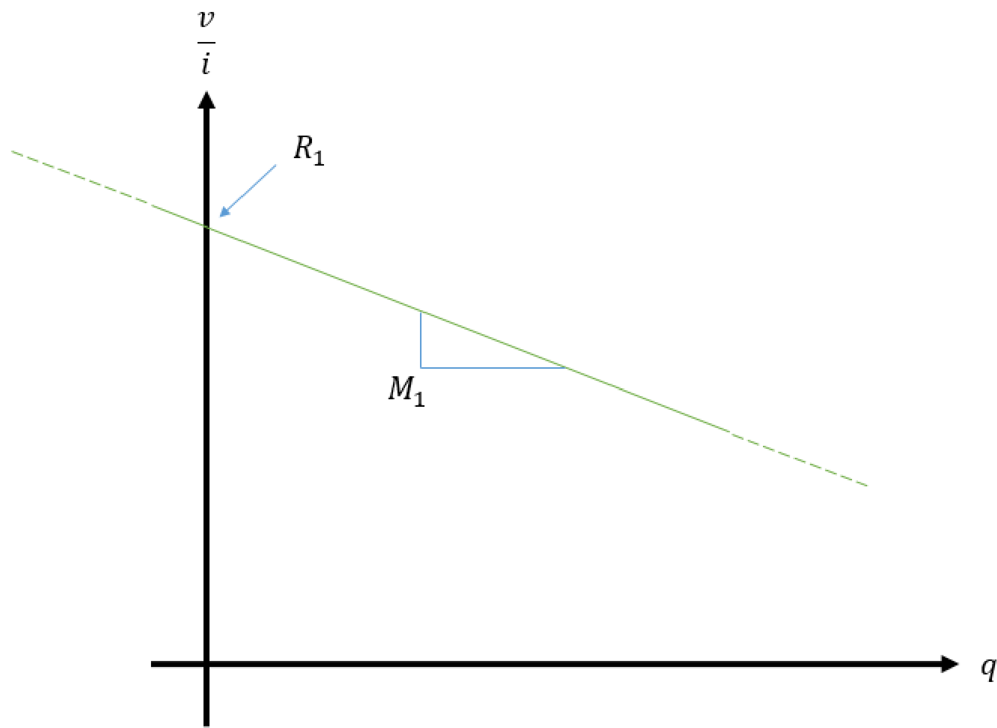

Figure 4.7: Ideal memristor showing linearity.

This outlines also a few interesting characteristics of an ideal Memristor: there are regions of the graph for which the instant resistance $\frac{v}{i}$ is negative; there is no DC steady-state, since the function is unbounded (although undefined for zero values of current); and as frequencies approach infinity, the resistance will converge towards R_1, which or the remainder of this dissertation will be referred to as the initial state of the Memristor. With the exception of the negative resistance, these characteristics had already been outlined as hallmark characteristics of a Memristor [31].

Because this negative resistance should not occur (at least from a steady-state perspective) it is clear that a better practical approach for the Memristor would be to consider it to be piece-wise linear. Fabricated Memristors will operate between two regions: a high-resistance state R_{OFF} and

a low-resistance state R_{ON}. Fig. 4.8 shows how a piece-wise linear graph would show for such a device.

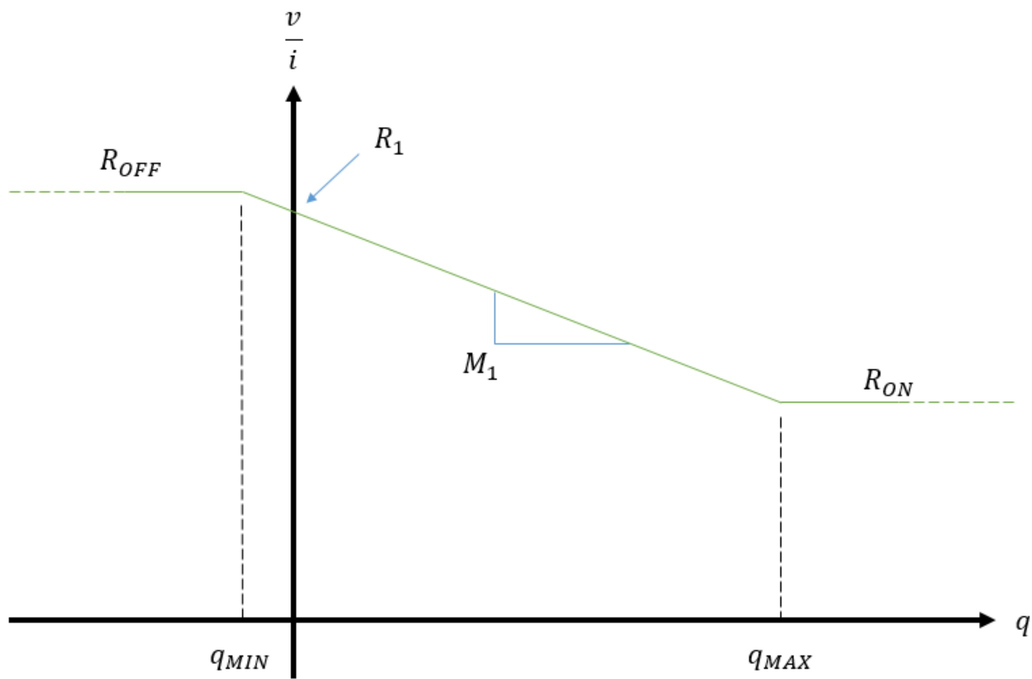

Figure 4.8: Practical memristor showing linearity region and saturation regions.

Thus only for values of charge history between q_{MIN} and q_{MAX} is there any memristive action. Values outside of those ranges will result in a simple resistor. This Memristor can then be described by:

4.3 Alternative Memristance Calculation Method

Obtaining the memristance value M_1 from a Ω - q graph is then trivial, but there are additional methods for obtaining the memristance. Capacitance, for instance, can be obtained from the i-v graph when the element is driven by a sinusoidal voltage source using the reactance formula

$$X_C = \frac{1}{2\pi f C}. \tag{4.9}$$

By knowing the maximum current (or difference between minimum and maximum current) we can then obtain the value of the capacitance in the circuit. A similar method can be obtained for the charge-controlled Memristor being driven by a sinusoidal current source. Suppose $i = Asin(2\pi ft)$; using Eq. 4.8 we arrive at the formula for the Memristor instant resistance

$$R(t) = M_1 q(t) + R_1. \tag{4.10}$$

Thus by using $q(t) = \int_{-\infty}^{t} i(\tau)d\tau$ we then arrive at:

$$R(t) = \frac{-M_1 Acos(2\pi ft)}{2\pi f} + R_1. \tag{4.11}$$

The appearance of the cosine explains why the curve in this plane will be a circle. It also states that the maximum resistance observed will be

$$R_{MAX} = \frac{M_1 A}{2\pi f} + R_1. \tag{4.12}$$

So then the difference between maximum and minimum resistance will be

$$\Delta R = R_{MAX} - R_{MIN} = (\frac{M_1 A}{2\pi f} + R_1) - (\frac{-M_1 A}{2\pi f} + R_1). \tag{4.13}$$

$$\Delta R = \frac{M_1 A}{\pi f}. \tag{4.14}$$

Take then the Memristor curve of Fig. 4.9. By calculating the difference between the maximum and minimum resistance and knowing the amplitude and frequency of the source signal, it is possible to derive the memristance M_1 in a fashion similar to how it is done in capacitors and inductors.

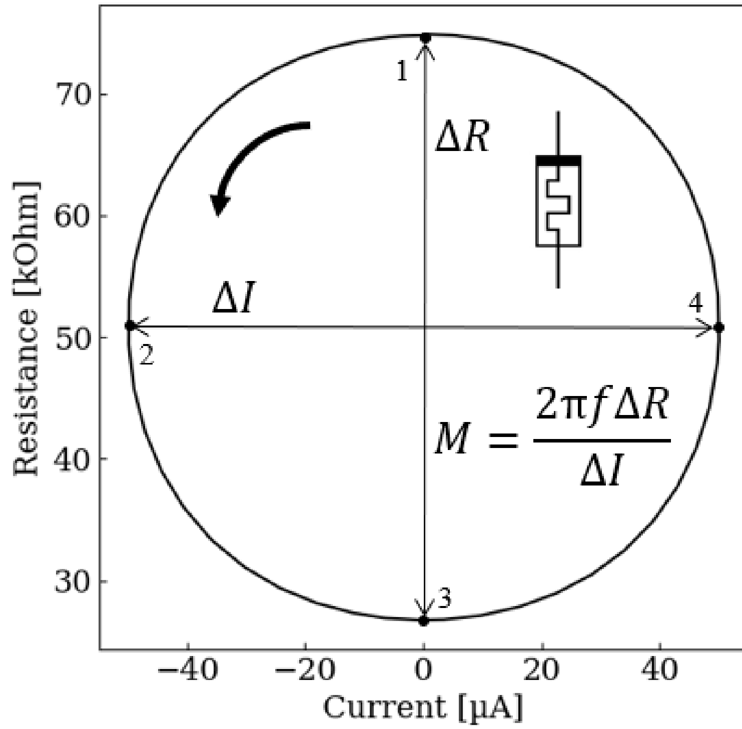

Figure 4.9: Ω-I plane of an ideal Memristor showing instantaneous resistance change.

As with all other real world fundamental circuit elements however Memristors are not ideal; an I-V and $\Omega - I$ curve for a practical device will be closer to the one shown in Fig. 4.10 which exhibits non-linearities.

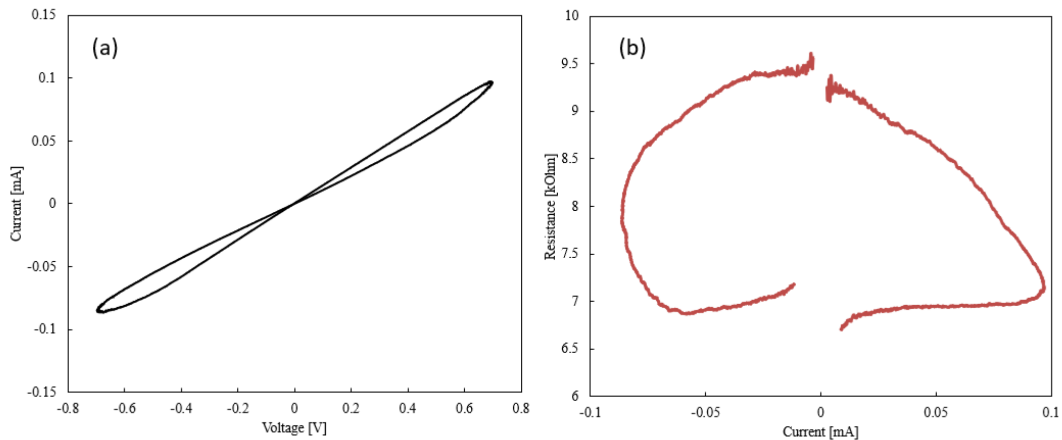

Figure 4.10: (a) i-v and (b) Ω-i plane of a manufactured Memristor.

The phenomenological reasons and how to model these non-linearities was addressed in the previous chapter, and it is still possible to calculate the value of the Memristor even in these cases. To illustrate how we look at the case of a non-ideal capacitor which has a maximum voltage (after which it just conducts through a leakage path without accumulating more charges) shown in Fig. 4.11.

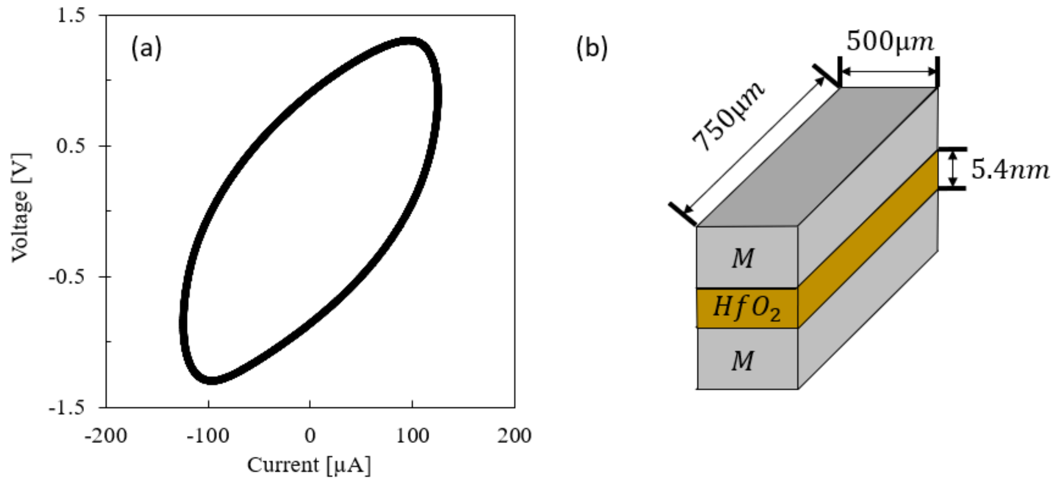

Figure 4.11: (a) i-v curve of the parallel plate capacitor shown in (b).

It is trivial to calculate the capacitance by using the formula for parallel plate capacitors:

$$C = \frac{\epsilon_r \epsilon_0 A}{d}. \tag{4.15}$$

In it, C is the capacitance in Farads, ϵ_r is the relative permittivity of the dielectric, ϵ_0 is the permittivity of vacuum, A is the plate area, and d is the distance between plates. For the dimensions in Fig 4.11(b) and using a ϵ_r for HfO_2 of 25, we arrive at a capacitance of $15.4nF$. If however the methodology for calculating capacitance, it could still be calculated from the i-v provided. The methodology is fairly simple, albeit heavily computational: find the maximum voltage and current, normalize voltage and current to the previously found maxima, separate the data in arbitrary

sequences of points and then fit a circle to these points using a least squares method; then build a histogram of radii found, if the radius for which there are most counts is not exactly equal to 1, re-normalize voltage or current proportional to the found radius and repeat until the radius found is exactly equal to 1. This will generate the histogram of Fig. 4.12

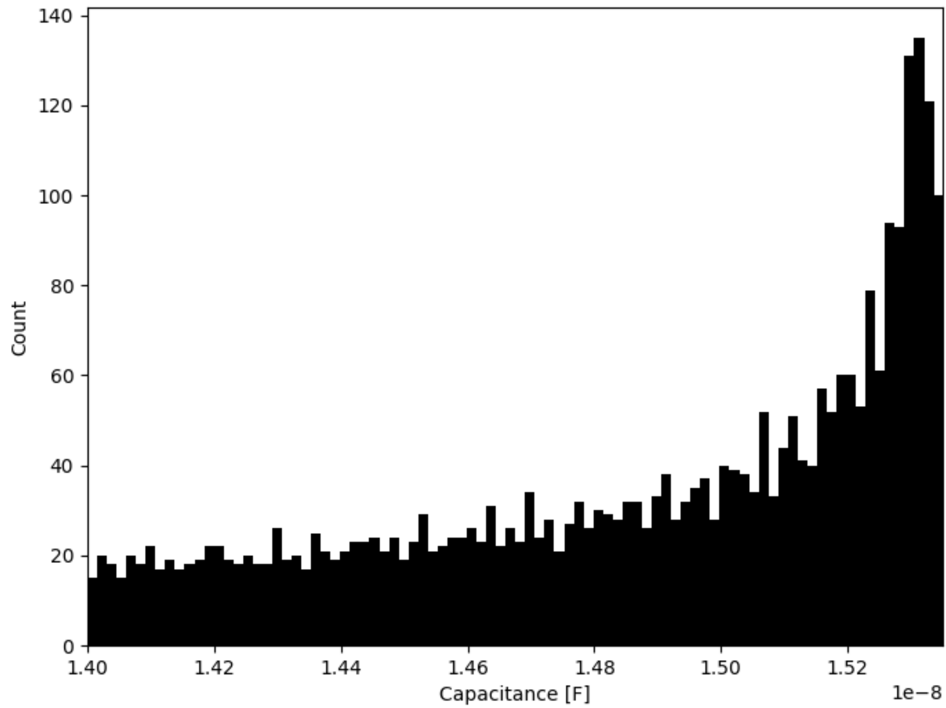

Figure 4.12: Histogram of detected capacitances showing peak at $15.3nF$.

The histogram is already converted from radii to capacitance. One can clearly see that the value found, $15.4nF$ is close to the calculated from Eq. 4.15. Repeating this procedure on the Memristor of Fig. 4.10 yields the histogram of Fig. 4.13, which provides a memristance of approximately $8GCh$. This is a value slightly under the value calculated using the slope method ($10GCh$), likely due to the amount of non-linearities present in the positive cycle.

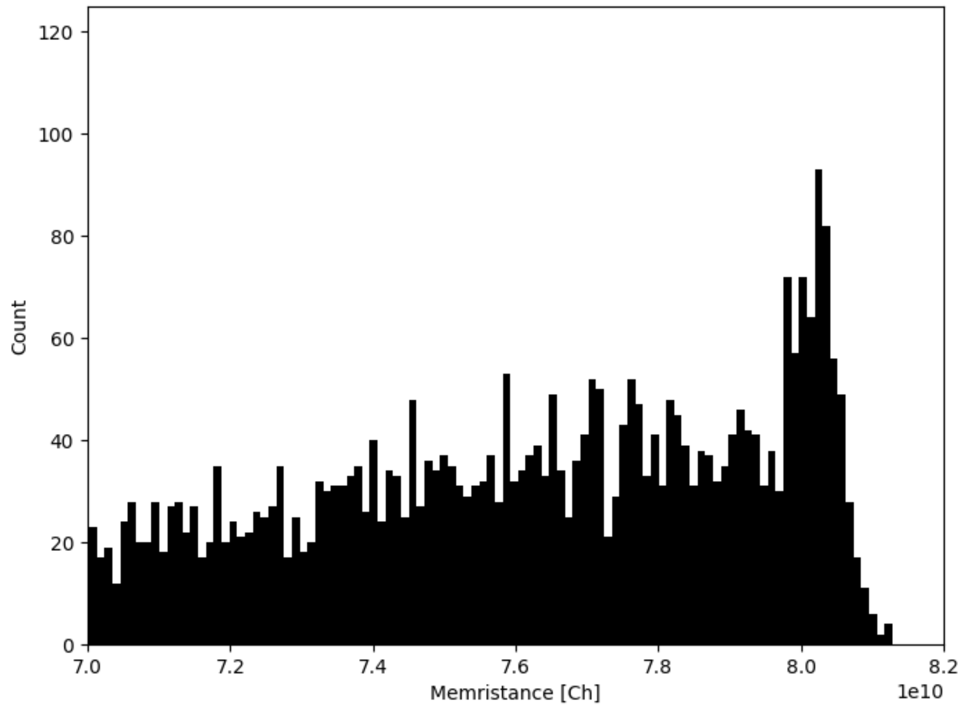

Figure 4.13: Histogram of detected memristances showing peak at $8GCh$

This method was derived for completeness and to further emphasize the symmetries that exist between the Memristor and other fundamental elements.

4.4 Association of Memristors

In this context it is also useful to determine then how does this new fundamental passive circuit element associates in series and in parallel.

4.4.1 Series Association of Memristors

The series association is the simplest. Assume two different Memristors associated in series as shown in Fig. 4.14.

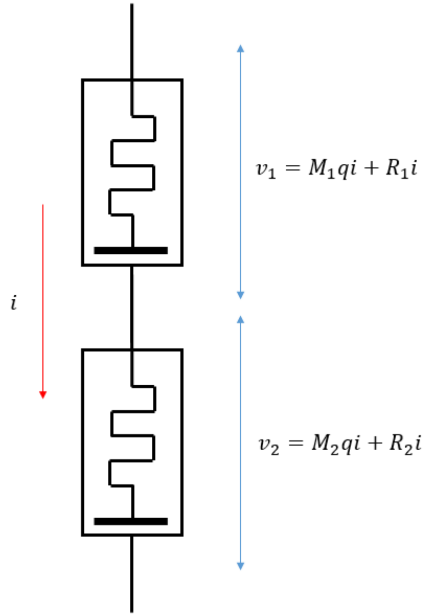

Figure 4.14: Series association of memristors.

In this case the current for both is the same and thus the charge history is the same: $q = q_1 = q_2$. The voltage will be divided between them such that $v = v_1 + v_2$. Thus:

$$\begin{cases} v_1 = (M_1q + R_1)i \\ v_2 = (M_2q + R_2)i \\ v = v_1 + v_2 \end{cases} \tag{4.16}$$

$$v = (M_1q + R_1)i + (M_2q + R_2)i \tag{4.17}$$

$$v = [(M_1 + M_2)q + (R_1 + R_2)]i \tag{4.18}$$

So the series association of two Memristors acts very similarly as two series resistors; the resulting memristance M_{series} is $M_1 + M_2$ and the initial condition R_{series} is $R_1 + R_2$. This Memristor is shown in Fig. 4.15.

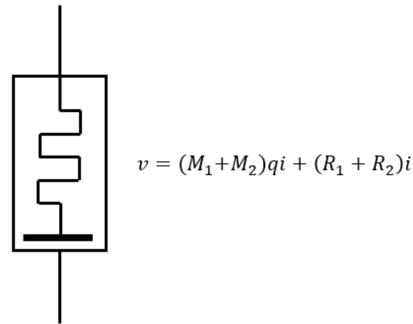

Figure 4.15: Equivalent Memristor arising from the series association of Memristors with characteristics $M_1q + R_1$ and $M_2q + R_2$

4.4.2 Parallel Association of Memristors

The parallel scenario is more complex so it helps understanding if we begin this work by assuming two identical Memristors in parallel as shown in Fig. 4.16.

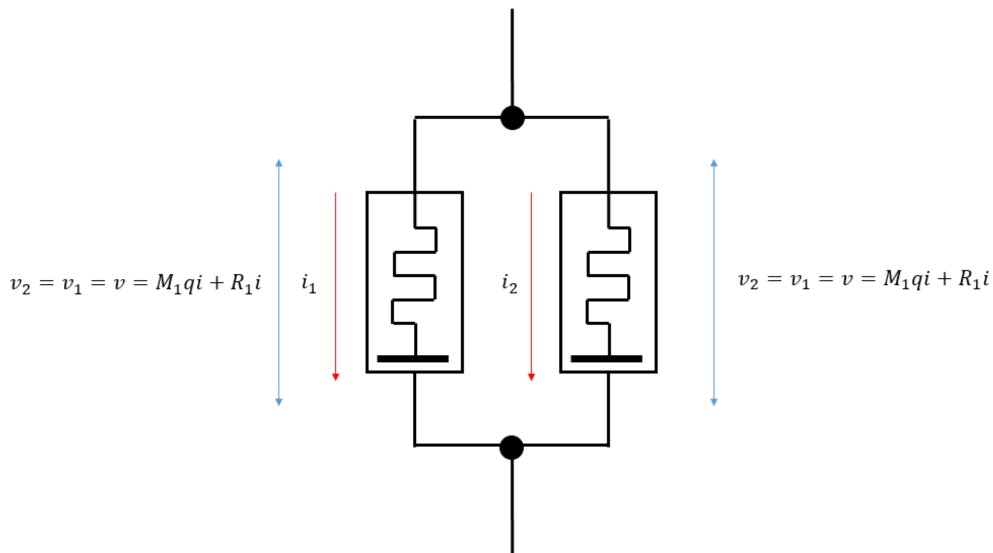

Figure 4.16: Parallel association of two identical Memristors.

In this case $v_1 = v_2 = v$ and since they are identical it also follows that $i_1 = i_2 = \frac{i}{2}$. Thus:

$$q = 2q_1 = 2q_2 \tag{4.19}$$

$$v_1 = v = M_1 q_1 i_1 + R_1 i_1 \tag{4.20}$$

$$v = \frac{M_1}{4} qi + \frac{R_1}{2} i \tag{4.21}$$

Of note in the resulting Eq. 4.21 is that this device is now equivalent to a single Memristor of a quarter of the slope and half the initial resistance. The latter result should not be a surprise: the initial state of the Memristor behaves exactly as a resistor would so it is natural to think of the resulting state to be simply the parallel association of resistors (in this case $\frac{R_1}{2}$).

This result can be expanded for n Memristors in parallel. In this case:

$$q = nq_n \tag{4.22}$$

$$v = \frac{M_1}{n^2} qi + \frac{R_1}{n} i \tag{4.23}$$

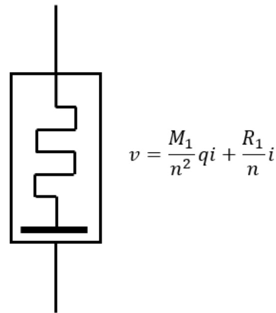

Figure 4.17: Parallel association of n identical Memristors.

The general case for two completely different Memristors is more complex. There is the possibility of approaching this problem in a density manner such as is done with other fundamental elements, in which case each Memristor can be represented as a parallel association of an original Memristor. Thus, the parallel association of two Memristors would be

$$v = \frac{M_O}{(n_1 + n_2)^2} qi + \frac{R_O}{(n_1 + n_2)} i \tag{4.24}$$

This assumes the existence of an "originating" Memristor M_O such that:

$$\begin{cases} M_1 = \frac{M_O}{n_1^2} \\ M_2 = \frac{M_O}{n_2^2} \\ R_1 = \frac{R_O}{n_1} \\ R_2 = \frac{R_O}{n_2} \end{cases} \tag{4.25}$$

Clearly that is not true for all possible Memristors. Take for instance the case where two Memristors are identical but one is placed at a slightly different initial condition, or: $M_1 = M_2$, $R_1 = R_2 + \delta$. Due to this very simple difference, now there is no possible originating Memristor M_O since due to $M_1 = M_2$ then $n_1 = n_2$ but $\frac{R_1}{n_1} \neq \frac{R_1+\delta}{n_1}$. It is possible that for practical cases the difference δ is negligible, but a more general formula for the parallel case would be beneficial.

4.4.3 Volumetric Analysis of Memristance

Derivation of the general formula for the series and parallel case allows prediction of the values of memristance for a certain volume, similarly how it is done for resistors: $R = \rho L/A$ where ρ is the material's resistivity, L is the length of the material, A is the area . Take for instance the general MIM structure of a Memristor shown in Fig. 4.18.

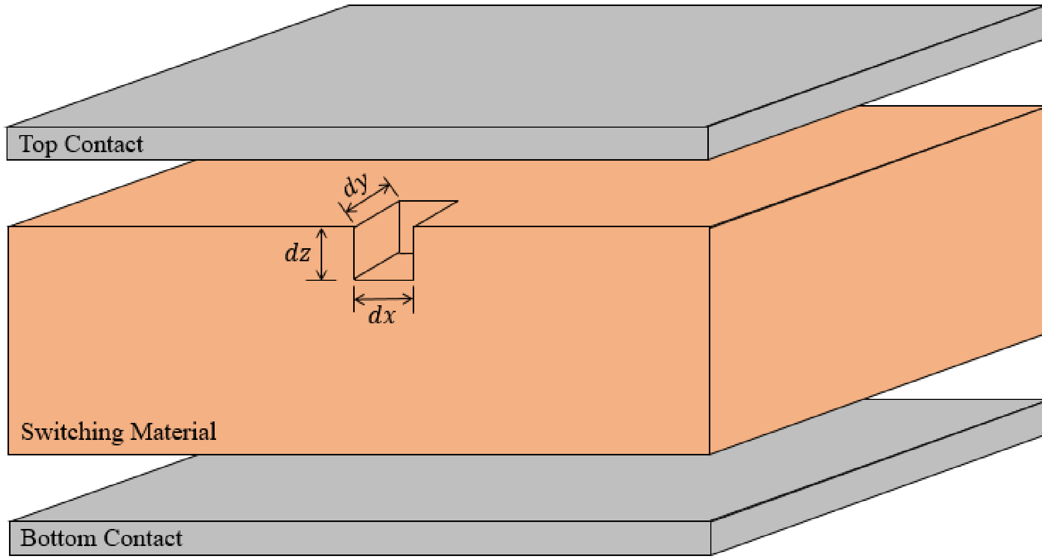

Figure 4.18: Memristor MIM structure showing "quantized" memristance block removed.

Imagine that we can take out infinitesimal portions of the switching material (such that the memristance of each infinitesimal part is in fact the Memristivity, a fundamental material property) and connect them in series and parallel such that the resulting structure is the Memristor; one could calculate then the value of memristance and relate it to the physical dimensions. Consider the memristance of this infinitesimal block to be M_ρ with no initial condition. Associated in series (z direction), and in parallel (x and y direction) the total memristance will then be:

$$M \propto \frac{M_\rho L}{A^2}. \tag{4.26}$$

This outlines a particularly interesting prediction of the theory presented by this work: *the reason memristance appears for many nano-scale devices [50] is due to the small feature sizes*. Since memristance goes down with the square of the area, large area devices will exhibit a memristance so low that frequencies in the order of mHz or even μHz would be necessary to detect any change in resistance. While one might think that an increase in switching material thickness would be able to balance that, the increase in thickness also changes how thick the barrier is for charges to jump

from one of the contacts to the switching medium, negating the effect.

In essence then, building a Memristor that reacts fast enough to be measured as one is a delicate balancing act that was not possible previously until we reached modern manufacturing processes. This is not to say Memristors cannot be manufactured large; they simply exhibit a change in resistance that is too slow to be detected or useful for most purposes.

4.4.4 Large Size Memristors: Electromigration as Memristance Mechanism

If Memristors can theoretically be large, this leads to the inevitable conclusion that they could have been built a long time ago; Chua himself argued that this is the case [81] (although he uses the looser initial definition of a Memristor). It so happens that there is a mechanism that acts over large enough distances to be able to produce large Memristors: Electromigration. Usually it is explored in the context of metal interconnects [82], although it was previously mentioned as a memristance mechanism [83].

It is usually analyzed only as a method of failure, but the characteristics are incredibly similar to a Memristor [84]: change in resistance proportional to the history of charge through, and bipolar behavior such that inverting the polarity *reverses* the increase in resistance. Fig. 4.19 shows a study of electromigration in copper interconnects and displays the same fingerprints of a Memristor.

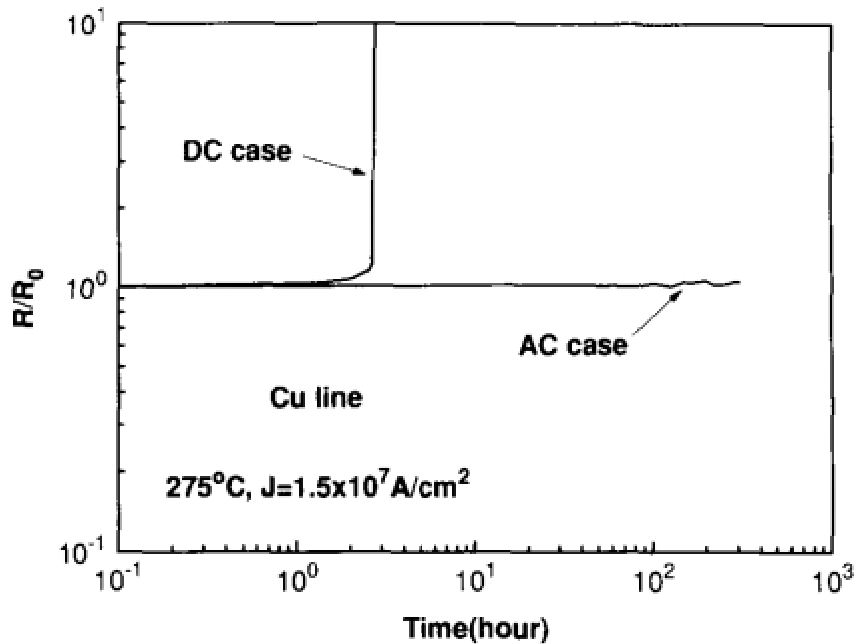

Figure 4.19: Copper interconnect subject to a DC and 1MHz AC current over time. Reprinted with permission from [84].

The situation is even clearer when the interconnect is subject to currents of different polarity. In Fig. 4.20 the same switching of resistances is seen, with a linear relationship between charge and resistance, although there are actually two different slopes (one when the resistance increases and one when the resistance decreases). This is to be expected, since the device wasn't tested as a Memristor and as such the driving current is being held for a longer time than what is necessary for the mobile charges to return to their original position; this causes a mixture of forming of new charges and Memristance, effectively altering the perceived memristance of the device.

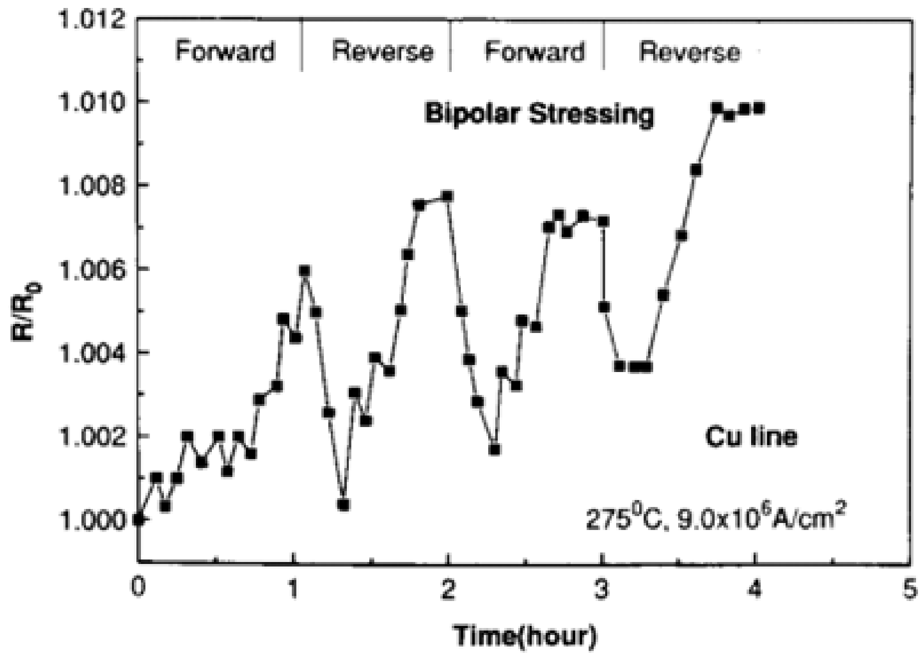

Figure 4.20: Copper interconnect subject to a AC current over time showing linear dependence between charge and resistance. Reprinted with permission from [84].

This is further evidenced by the fact that a single polarity reversal has two slopes: a Memristance slope (negative slope) and a forming slope (positive slope). Memristance can be calculated from both, and for this particular graph yields $M = -337\mu Ch$ and $M = 718\mu Ch$. As such, a simple interconnect *is a Memristor*, although it should be noted that the memristance is very low since the timescale for very small resistance changes is in the order of hours [84]. Additionally, the problem with electromigration is that usually it does not have boundaries; since it is not constrained to a certain shape, alteration of resistance may not appear bipolar.

Since electromigration is a generally undesired behavior, one could consider it then a *parasitic Memristor*.

4.4.5 Conductive Filament Analysis

In some cases, the bulk of the switching medium does not actually switch; this is the case for CF Memristors, where a forming cycle actually electroforms a filament embedded inside of a metal

oxide. In this case then, only the geometry of the conductive filament itself can be used to derive the memristance of the device. Thus, the same structure can have wildly varying Memristances depending on the forming cycle as illustrated by Fig. 4.21.

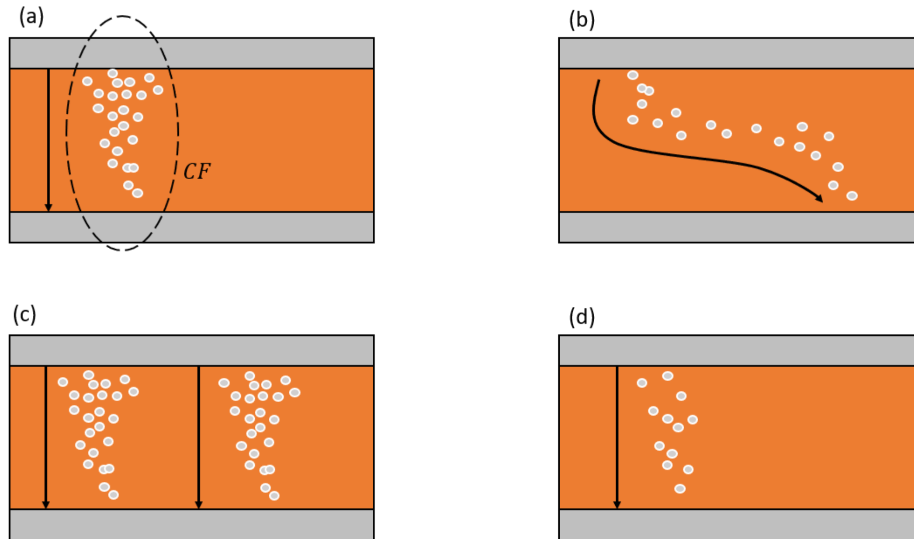

Figure 4.21: (a) Memristor structure showing single CF. (b) Longer CF. (c) Multiple CF. (d) Single CF with lower mobile ions.

The situation is further complicated by the fact that simple operation of the device can alter the geometry of the CF or form new ones. As such, Memristance in these devices will likely be a range, instead of a single constant; this will be revisited in the next chapter. To prevent this, it is necessary to constrain the physical measurements of the device, once again reinforcing the idea that in general, small area devices will perform more ideally.

4.5 Linear Memristor Model Validation

To verify the validity of the developed practical model outlined various simulation tests were performed against the Biolek model [36] - since it is widely accepted as a good representation of memristors with nonlinear dopant drift.

4.5.1 Single Memristor Simulations

The test setup is shown in Fig. 4.22 and was built usint LTSpice [85]. The memristor used in the circuit has the parameters: $R_{OFF} = 100k\Omega$, $R_{ON} = 1k\Omega$, $R_{init} = 50k\Omega$, $D = 10nm$, $p = 1$, $\mu_v = 10fm^2s^{-1}V^{-1}$. Initially we test using a sinusoidal voltage source with an amplitude of $1V$ and frequency of $1Hz$.

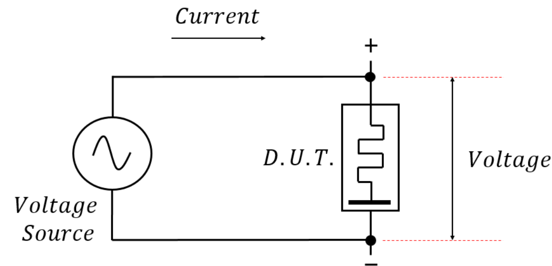

Figure 4.22: Memristor test setup on LTSpice.

This yields the graphs shown in Fig. 4.23. The similarities between this simulation and the fabricated HP Memristor can easily be seen; more noteworthy however is how much the plot is similar to the theoretical one shown in Fig. 4.8. The transition from linear region to saturation is not sharp, which seems reasonable since if that were to be the case the function would be non-differentiable and thus less practical, but it is still a good approximation. Two parameters used in the model can be easily extracted: the R_{ON} saturation and the initial condition R_{init}.

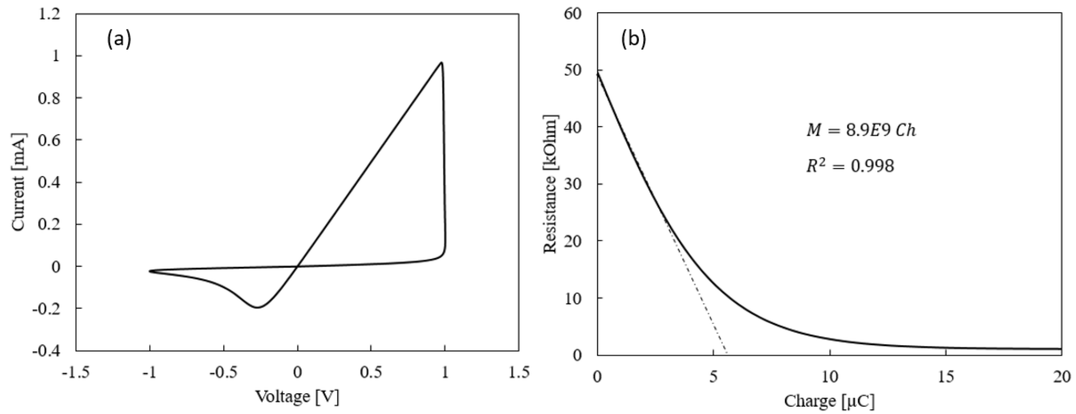

Figure 4.23: (a) i-v curve of the simulated Memristor using Biolek's model. (b) Ω-q curve of the same memristor showing linear and saturation region.

To verify that the values obtained for the memristance M do not vary with excitation and initial conditions Fig. 4.24 shows three other curves that change source amplitude, source frequency, and initial condition.

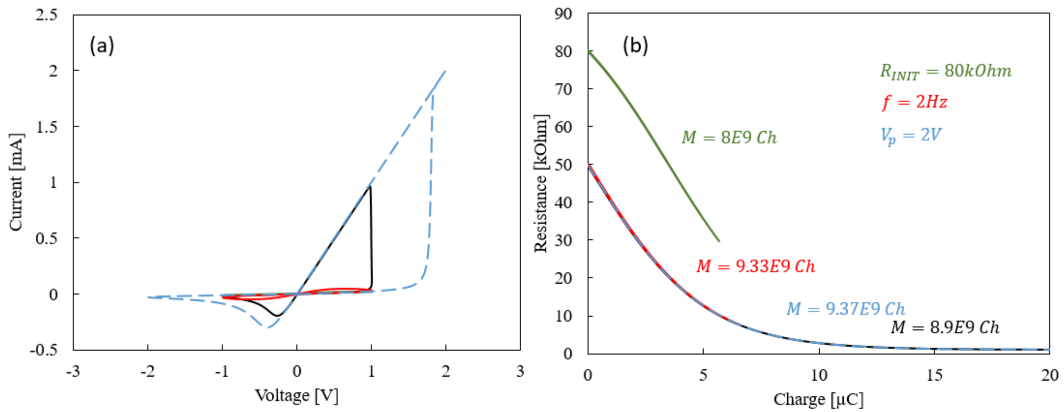

Figure 4.24: (a) i-v curve of the simulated Memristor using Biolek's model for three different variations in test parameters. (b) Ω-q curve of the same Memristor showing linear and saturation region for three different variations in test parameters.

It can be clearly seen that there is a small change in the calculated memristance, mostly due

to the non-linearities close to the saturation. These results still support the developed theory that Memristors can be sufficiently described by four parameters: their *memristance* M; their *initial state* R_{INIT}; their *upper saturation bound* R_{OFF}; and their *lower saturation bound* R_{ON}.

4.5.2 Series Memristor Simulations

Fig. 4.25 shows the simulation result for two equal Memristors ($R_{OFF} = 100k\Omega$, $R_{ON} = 1k\Omega$, $R_{init} = 50k\Omega$, $D = 10nm$, $p = 1$, $\mu_v = 10fm^2s^{-1}V^{-1}$) in series.

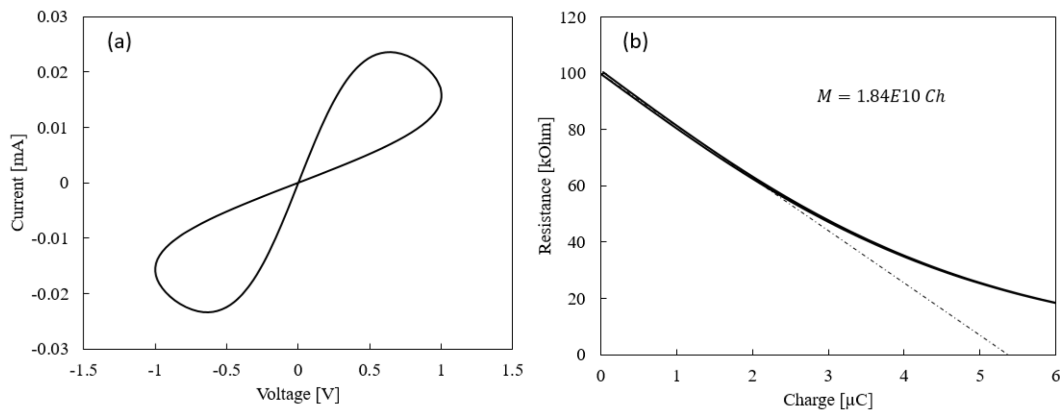

Figure 4.25: (a) i-v curve of the simulated Memristors in series using Biolek's model. (b) Ω-q curve of the same Memristors showing linear and saturation region.

The memristance is then similar to the predicted value of twice the memristance of a single one. It not exactly double however, once again due to non-idealities close to the saturation point.

4.5.3 Parallel Memristor Simulations

The same is done for two Memristors in parallel. The results are shown in Fig. 4.26.

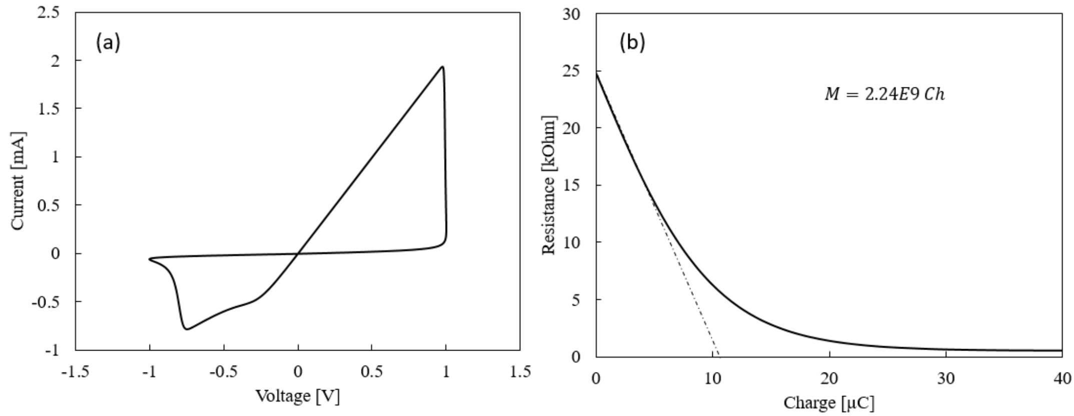

Figure 4.26: (a) i-v curve of the simulated Memristors in parallel using Biolek's model. (b) Ω-q curve of the same Memristors showing linear and saturation region.

It can be clearly seen that the memristance is close to the expected value of a fourth of the value for an individual Memristor. These results provide a validation to the theory outlined in this work.

4.5.4 Parasitics Effect on Memristance Measurement

The previous chapter has explored how parasitics can change perceived characteristics of the Memristor from hysteresis area to the location of the pinch point. Similarly here, they also alter the shape of the Ω-q curve, making it more challenging to determine the correct value of memristance for a switching material. Fig. 4.27 demonstrates the changes done by a simple $1nF$ capacitor in parallel with a Memristor at a frequency of $1kHz$. For the particular case of capacitors and inductors, the alteration is proportional to the frequency; avoiding this interference altogether is possible by taking the measurement of Memristance at a frequency for which the reactance can be neglected, but this may not always be possible. As an example, low frequencies (necessary in this case to isolate the effects of a parallel capacitance) tend to saturate and re-form the Memristor, and shouldn't be used to reliably measure Memristance. For MIM Memristors, the main source of reactive parasitic will be a parallel plate capacitor due to the two metal layers; this particular parasitic can be artificially removed by estimating the capacitance and removing the current to the capacitor in the measured data.

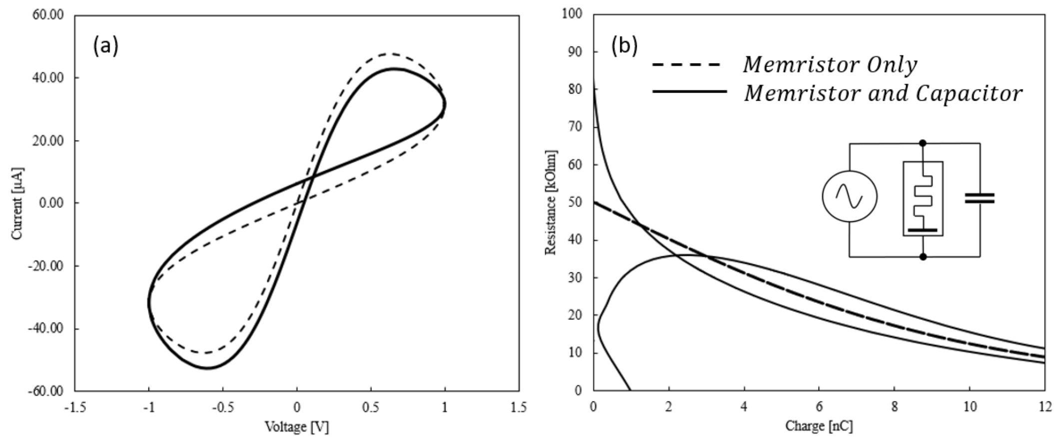

Figure 4.27: (a) i-v curve of the simulated Memristors with and without a $1nF$ parallel capacitor at $1kHz$. (b) Ω-q curve of the same configurations.

This should also bring the pinch point back to the origin. Parasitic diodes are more difficult to eliminate, but can be by fitting the data to the model described previously and analyzing the resulting fit Memristor without the parasitics.

While validating the Memristor model was fairly straightforward due to the abundance of experimental data in publications, the requirement for specific data acquisition to test the linearity of Memristors outside of simple simulations and the validity of the unit of memristance meant Memristors had to be acquired or fabricated so that this specialized testing could be done.

5.1 MIM Crossbar Memristor

For a non-linear dopant drift Memristor, a simple MIM structure composed of the same metal contacts was chosen. The insulator is a metal-oxide, and the fabrication sequence is shown in Fig. 5.1.

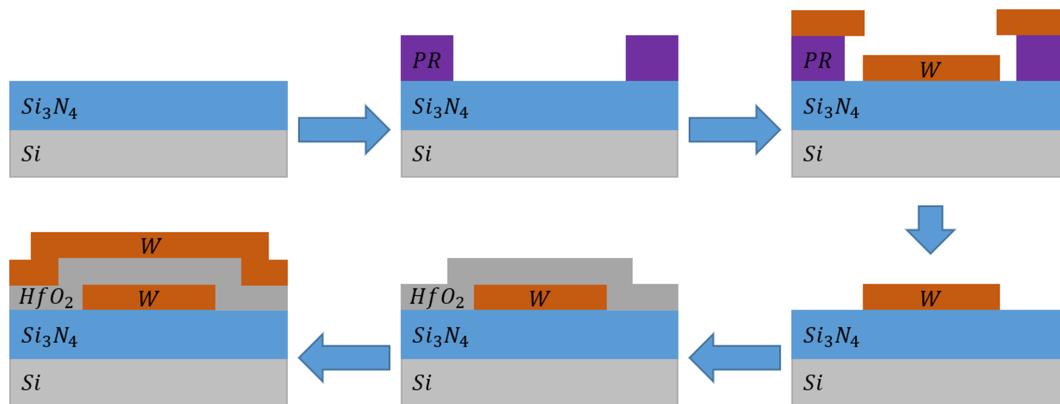

Figure 5.1: Sketch of fabrication sequence. Not to scale.

The process is started with a Si substrate for mechanical support. $100nm$ of Si_3N_4 are deposited using PECVD for insulation of the substrate to prevent any current sneak paths. Lithography is performed using a simple mask and using AZ5214 as a positive resist; while using AZ5214 as a negative resist or with the addition of a Lift-Off Resist (LOR) may have been more adequate for the situation, anecdotally we found no yield problems with the use of the simpler procedure. Then, $100nm$ of Tungsten is sputtered and lifted off using Acetone. Tungsten was chosen as

a metal that is not magnetic, easy to lift off, and does not oxidize easily. Then, the switching medium, HfO_2 is deposited using 50 cycles of ALD. While this should have yielded roughly $5nm$ of oxide, measured results have shown that in reality thickness was closer to $10nm$. Finally, the top contact of metal is lifted off similarly using the same mask misaligned by 90 degrees. The HfO_2 that remains on top of the bottom electrode is etched away using BOE for 7 minutes, with the top electrode serving as a hard mask against etching the parts that will serve as the switching material. This yields the structure shown in Fig. 5.2. The intersection area where the switching material resides is approximately $10\mu m$ x $10\mu m$.

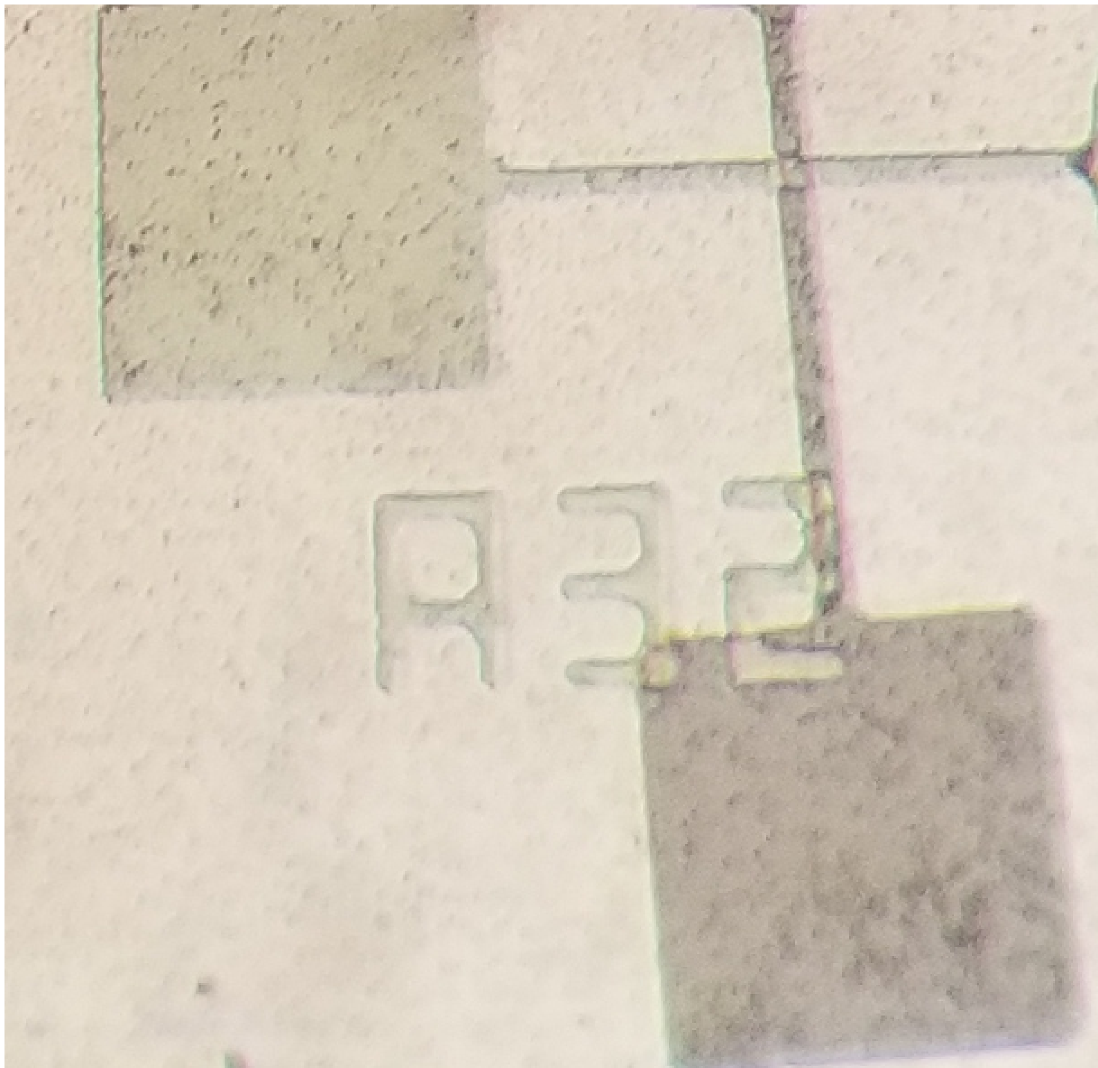

Figure 5.2: Fabricated crossbar structure with contact pads for probing.

It is useful to stress at this point that the oxide was not annealed; while the deposit introduces some vacancies and other defects and in the manufacture of a high-k dielectric gate for instance this would be done, this is desirable from the point of view that in the specific fabrication of a Memristor: it causes a forming cycle to no longer be necessary. The annealing also would prevent the oxide from being etched in BOE, adding complexity to the fabrication process.

5.2 Commercial Samples

In order to test a variety of devices with different physical mechanism of memristance, commercial samples of Chalcogenide Memristors [86] were acquired from Knowm Inc. Two samples were acquired, a Carbon doped Chalcogenide and a Tungsten doped Chalcogenide: they are shown in Fig. 5.3.

Figure 5.3: Two packaged memristor devices with eight Memristors each. Top: Tungsten doped Chalcogenide. Bottom: Carbon doped Chalcogenide.

Both devices are "burn and learn" quality, which means up to four of the Memristors in each package may not be working due to defects in process. According to the manufacturer most of

these defects come from the wire bonding procedure and thus these defective Memristors are easy to identify. During testing roughly 4 of the 16 were not functional.

5.3 Test Setup

To test the Memristors, the test setup shown in Fig. 5.4 was used. Two precision 280Ω resistors are used in order to measure both current entering and exiting the device. While since it is a two-terminal device both currents should (and indeed are) the same, this was done for redundancy.

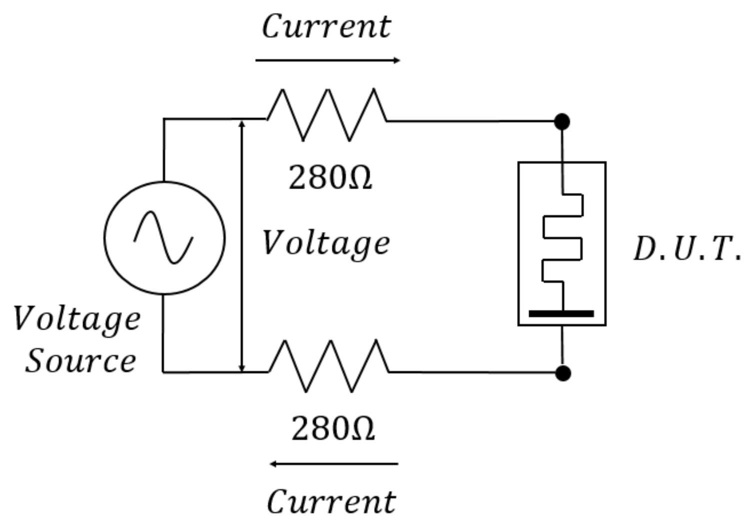

Figure 5.4: Circuit of the test setup.

The amplitude of the voltage source was kept constant and only the frequency was varied. To generate the Ω-q graph, both of these quantities had to be calculated from the data acquired: instant resistance R was calculated simply by v/i; history of charge had to be integrated from the discrete set of current points as shown in Fig. 5.5.

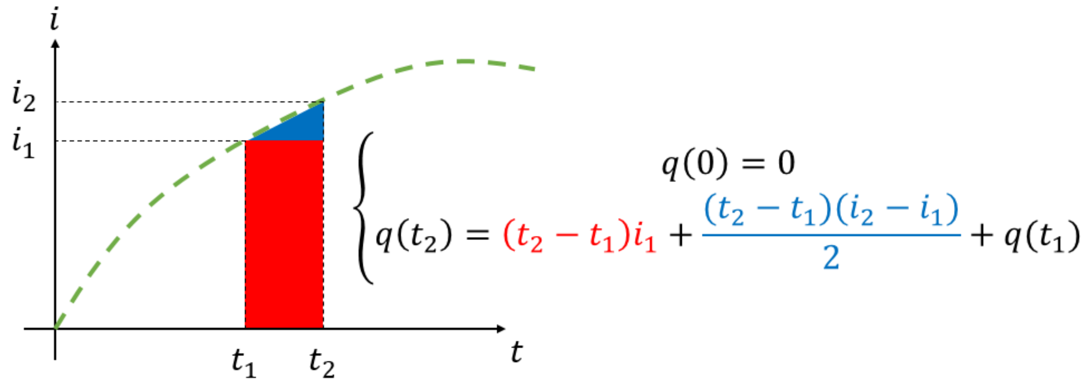

Figure 5.5: Methodology for the calculation of history of charge through the device.

5.3.1 Fabricated MIM Crossbar Memristor

Testing of the fabricated devices required lower frequencies due to the fairly high parasitic capacitance; beyond $8Hz$, the pinch point would shift significantly from the origin in the i-v graph, rendering analysis of the memristance unreliable. Fig. 5.6 shows the i-v and Ω-q for a frequency of $1Hz$.

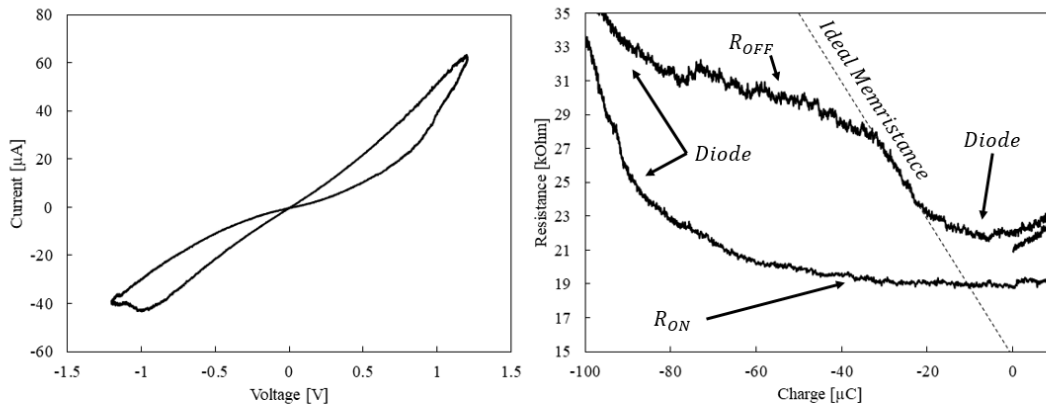

Figure 5.6: (a) i-v curve of the fabricated MIM Memristor. (b) Ω-q curve of the same Memristor showing linear region, saturation regions and other non-idealities.

It can be clearly seen that both deviate from the ideal case, with diodic behavior appearing.

A memristance can still be extracted, but only in the negative cycle due to less interference from potential barriers and leakage. To counter this, one can use the model previously described to eliminate the series and parallel diodes present in the device, and thus arrive at the curves of Fig. 5.7.

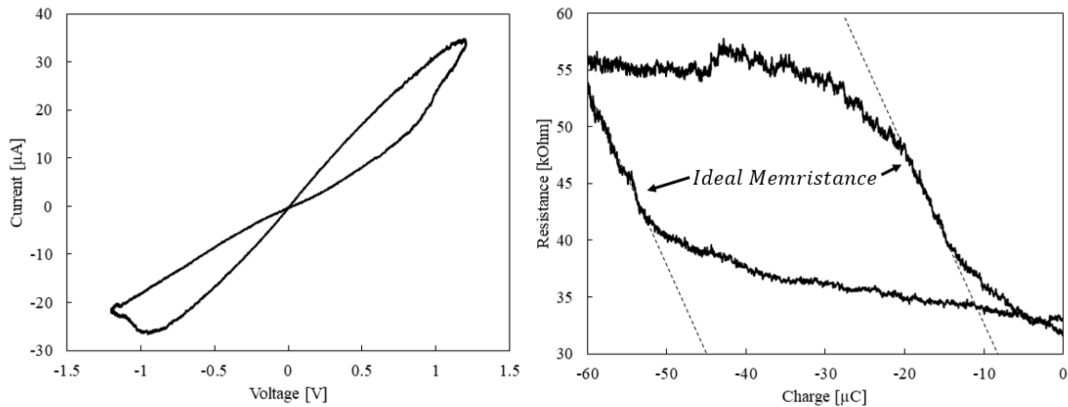

Figure 5.7: (a) i-v curve of the fabricated MIM Memristor corrected to remove non-idealities. (b) Ω-q curve of the same Memristor showing linear regions of same slope.

While still not perfect, now the device shows a memristance slope of same value on the first and third quadrant sweeps. While time consuming, this is the more accurate method for determining memristance. Fig. 5.8 shows the result of the simple analysis over various cycles in multiple frequencies.

Initially the data does not appear to support the idea that there is a single value of memristance; values vary widely not only for different frequencies, but even when being measured at the same frequency: in the worst case scenario ($8Hz$), memristance varies by almost two orders of magnitude. This actually occurs because the switching medium has a CF that has the freedom to diffuse in three dimensions: as explained previously, the conductive channel can change shapes and even quantity of mobile ions, changing the memristance measured according to these changes.

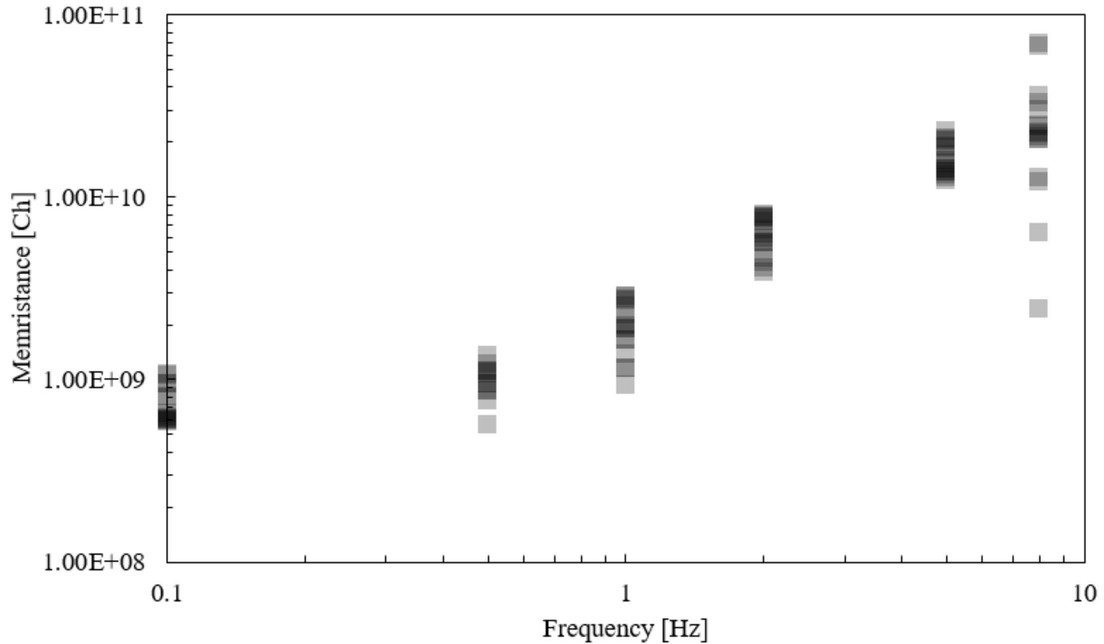

Figure 5.8: Analysis of memristance as measured using a sinusoidal voltage source in multiple frequencies for the fabricated MIM Memristor.

As an immediate consequence of this, only Memristors whose mechanism does not allow for such freedom (or a Memristor whose physical dimensions would be restrictive enough to confine the mobile ions in a single dimension) would display more stable memristance. The fabricated device has a fairly large area, allowing plenty of opportunities for both changes in shape of the CF and the formation of new ones. This is supported by Fig. 5.9, where the measured memristance is now plotted with respect to the time of actual measurement. In it, one can see how the measurement of the device also contributes to its continuing forming; even data for the same frequency follows the general trend described by the fit, suggesting that there is indeed the formation of new conduction channels over the time of the testing.

Since each new channel can be considered a parallel Memristor, the general memristance should be $\propto 1/n^2$, where n is the number of channels. Thus, one can estimate the generation of additional conduction channels by the general fit.

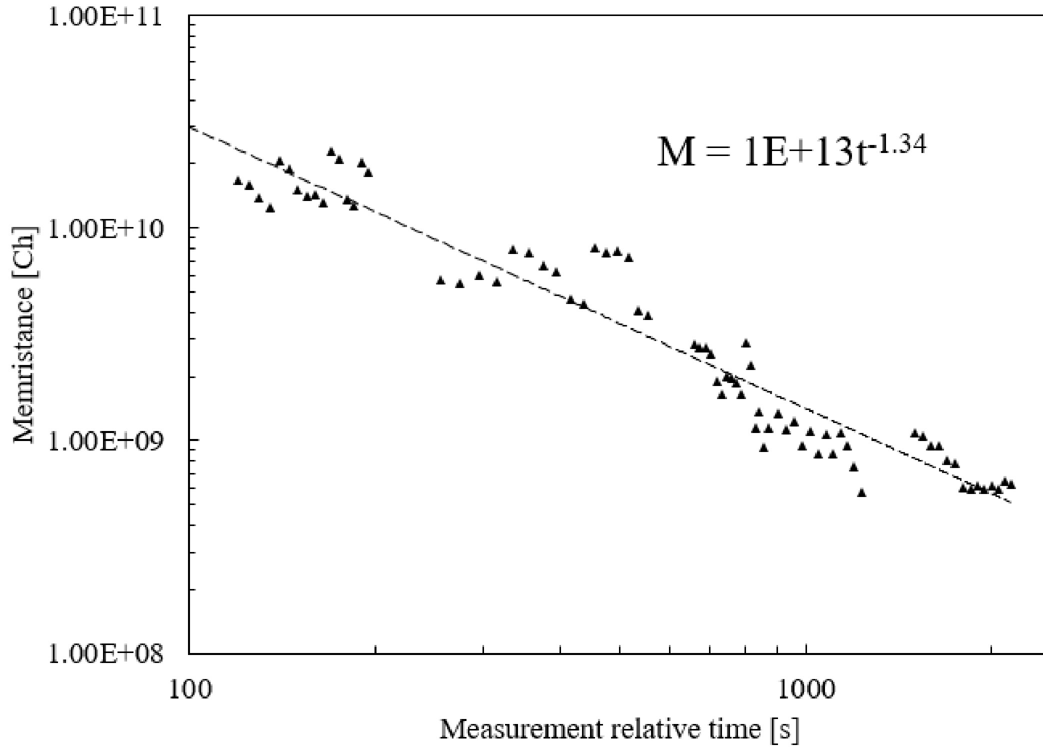

Figure 5.9: Time variance of memristance due to the formation of new conduction paths resulting in lower memristance.

Equating the fit $t^{-1.34}$ to n^{-2} where n is the number of CFs we arrive at Eq. 5.1:

$$n = t^{0.67}. \tag{5.1}$$

Thus for the fabricated MIM crossbar, the formation of new channels relative to time can be plotted resulting in Fig. 5.10. It also can lead to the generation of a τ_{CF}, which is the time constant associated with how long it takes for the measurement to significantly affect the Memristor by generating a new CF. In this example, for the first few seconds $\tau_{CF} \approx 3s$; this means effective measurements should take much less than 3 seconds to complete.

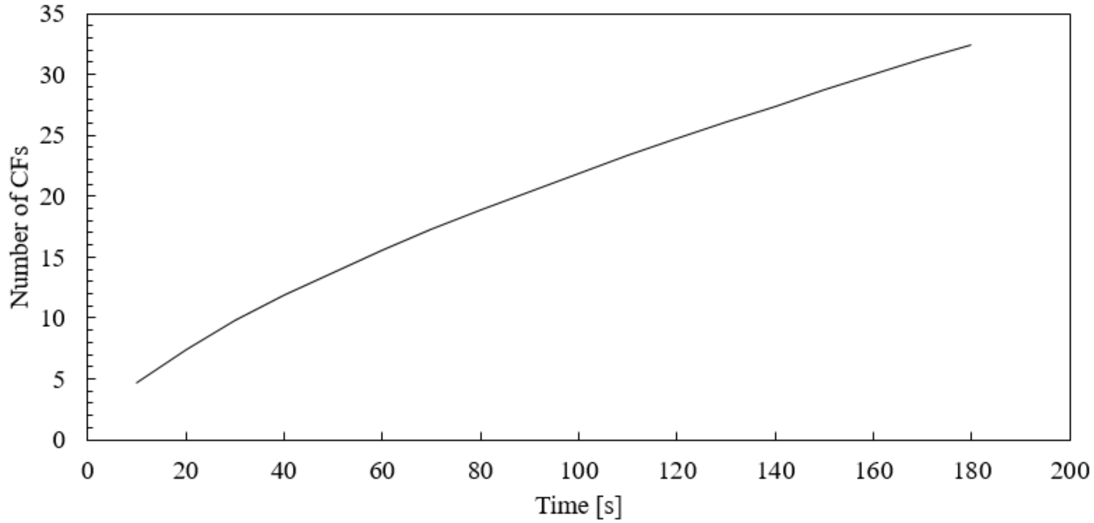

Figure 5.10: Number of new channels as a function of time.

Eventually, the switching material would be completely saturated with conduction channels and the memristance should plateau. It is unclear however how long this would take or whether or not this process could result in the destruction of the device due to effects such as heating.

These tests showcase the importance of developing the testing methodology of Memristors properly. An ideal test would not further form the device, either using the smallest possible excitation or the shortest possible time. It may also be possible to destructively test devices in order to characterize them (as was done in this example), provided process variations do not affect the values of memristance significantly.

5.3.2 Carbon-doped Chalcogenide

Testing of the Carbon-dopes Chalcogenide obtained from Knowm Inc. provided much more stable results, although some of the general trends were still observed. Fig. 5.11 shows the i-v, Ω-i, and Ω-q curves for it measured at $100Hz$. It is trivial to notice the circle pattern in the Ω-i curve, the linearity of Ω-q and how the i-v properly resembles a "figure 8".

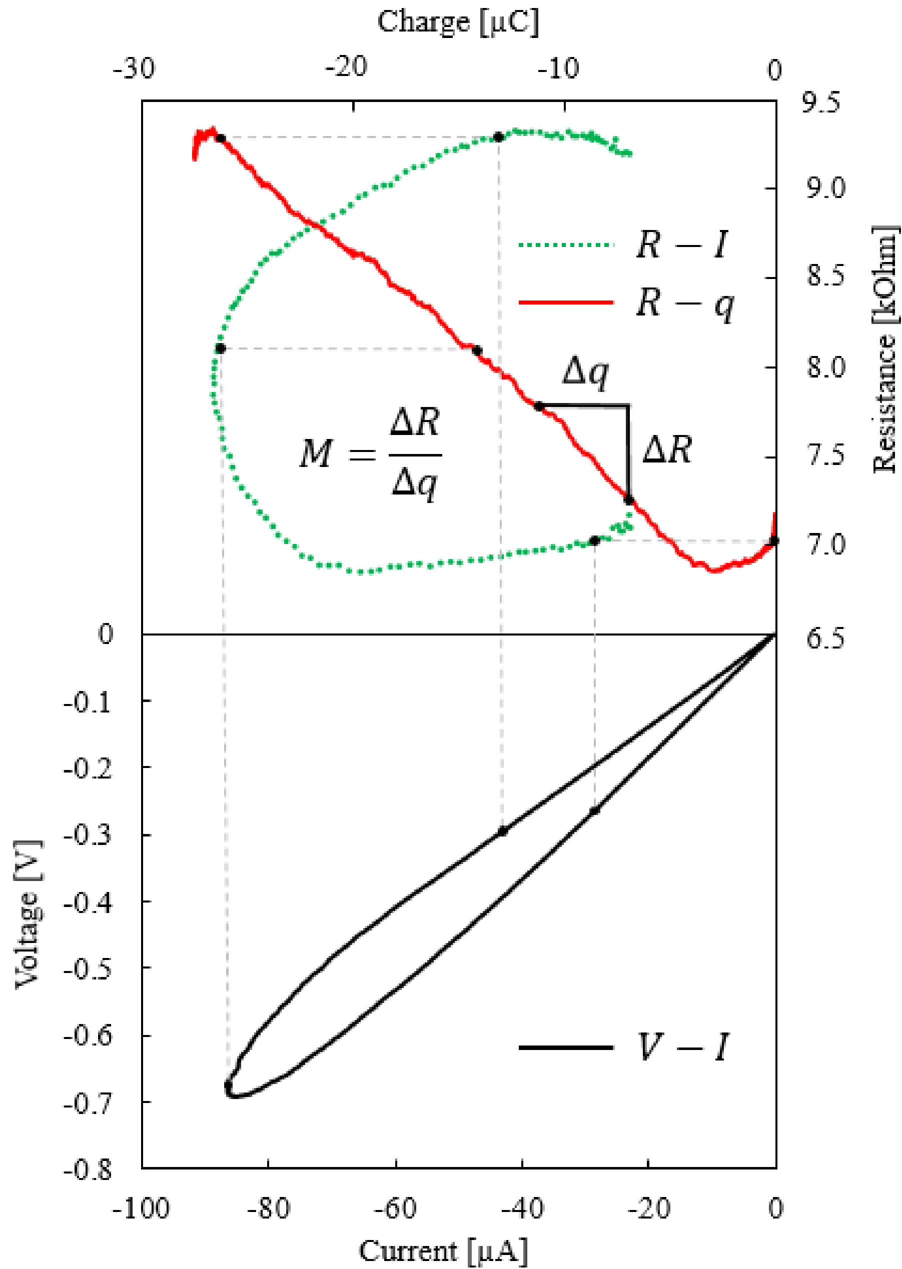

Figure 5.11: (a) Ω-i and Ω-q curve of the Carbon Knowm device. (b) i-v curve of the same Memristor for the third quadrant.

The absence of exponential non-idealities meant that the data does not need to be corrected in order to extract Memristances; unfortunately however the very low energy required to move carbon atoms also meant that excitation and frequencies were bound to a very limited range. The memristance measurement results are shown in Fig. 5.12.

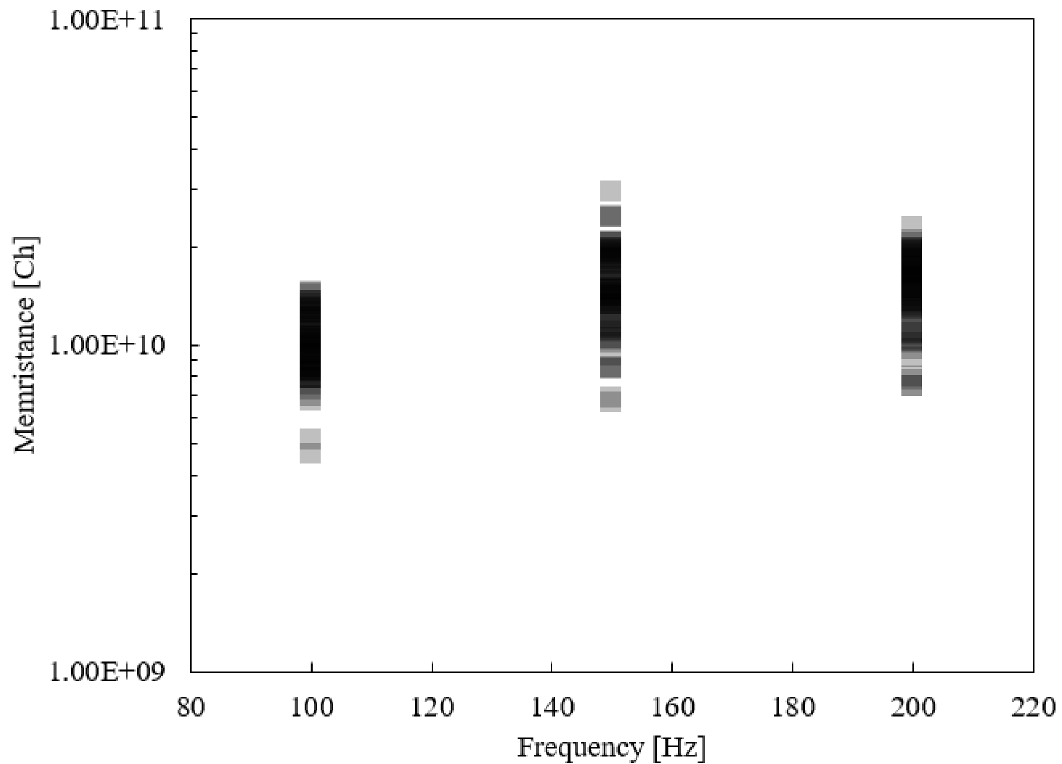

Figure 5.12: Analysis of memristance as measured using a sinusoidal voltage source in multiple frequencies for the Carbon-doped chalcogenide device.

Memristance still varies by almost an order of magnitude, although it appears to be confined within the same margins; this suggests there is still conductive channel volumetric variation between cycles. The value also did not appear to drift with time of measurement, which is consistent with the idea that the mechanism for this type of Memristor does not encourage the forming of new channels (since they are embedded dopants in a chalcogenide, their quantity should be fixed at manufacture), as opposed to metal-oxides which can form new oxygen ions.

5.3.3 Tungsten-doped Chalcogenide

The Tungsten-doped Chalcogenide, also manufactured by Knowm Inc., appears to require a higher energy to move the ions; it compensates for it having a much faster device. Fig. 5.13 shows the i-v and Ω-q curves demonstrating a significant effect of exponential non-idealities.

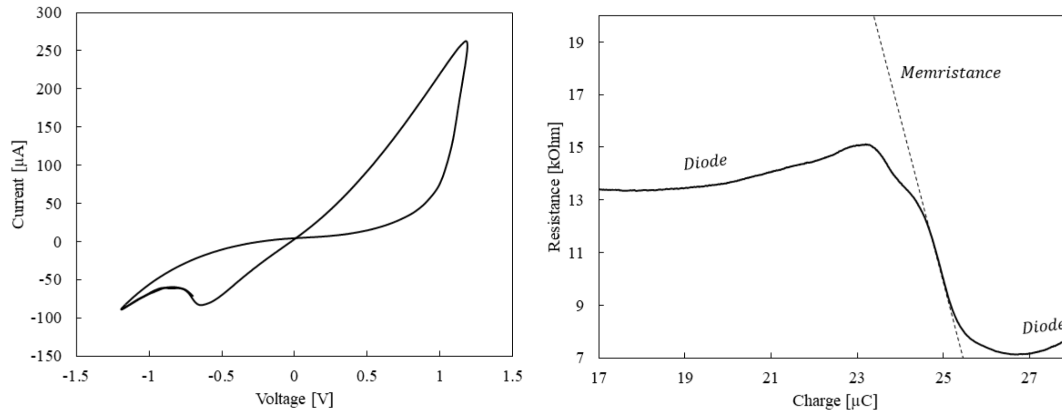

Figure 5.13: (a) i-v curve of the Tungsten Knowm device. (b) Ω-q curve of the same Memristor.

Similarly to previous cases, these can also be corrected in order to calculate memristance more adequately. A corrected example is shown in Fig. 5.14; while it is clear not all parasitics were eliminated, analysis was clean enough to be considered valid.

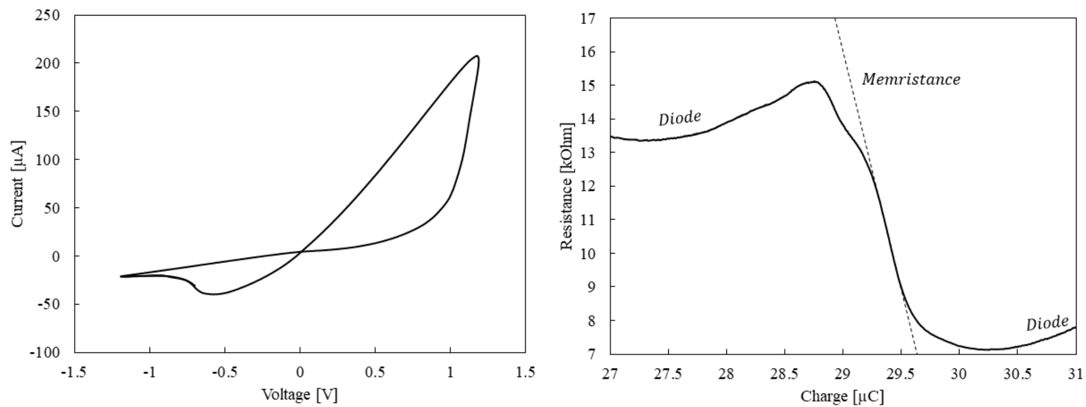

Figure 5.14: (a) Corrected i-v curve of the Tungsten Knowm device. (b) Ω-q curve of the same Memristor corrected.

Due to the faster speed of the device, it was able to be tested at a much higher frequency enabling the collection of more data. Fig. 5.15 shows that the measured memristance is stable,

although the variance in every frequency appears to span over almost two orders of magnitude as was the case with previous devices.

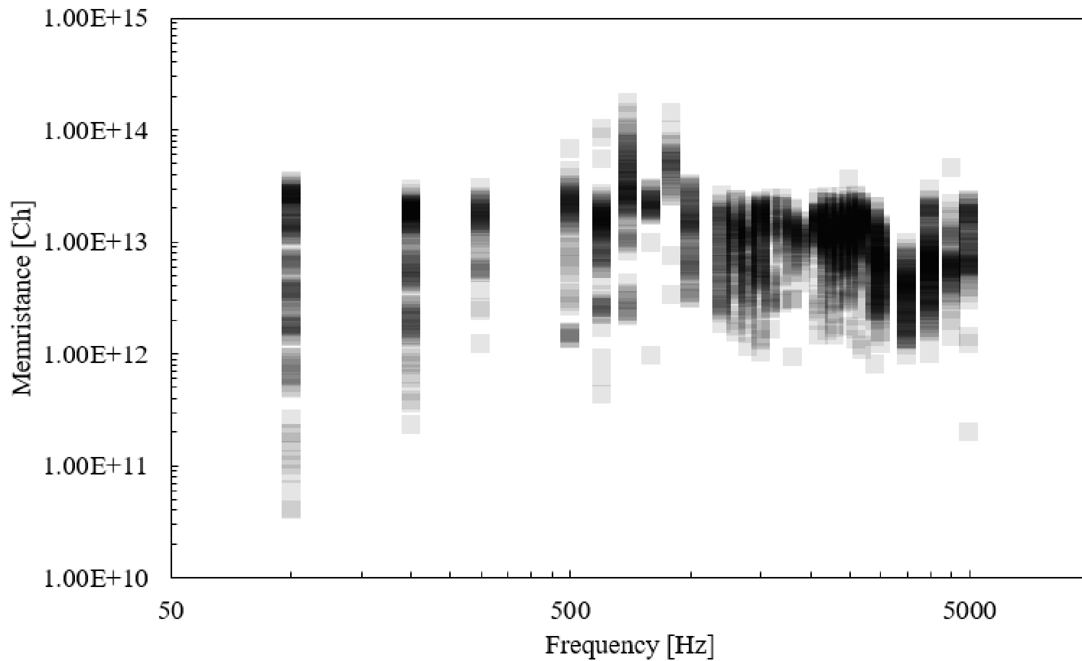

Figure 5.15: Analysis of memristance as measured using a sinusoidal voltage source in multiple frequencies for the Tungsten-doped chalcogenide device.

5.3.4 Overall Picture

Fig. 5.16 shows the mean value of Memristance found for all three Memristors in a single graph. Mean Memristance for both Carbon and Tungsten are reasonably constant, and are calculated as the average of all data regardless of frequency. These values should relate to the mobility of the switching material active species and the geometry of the CF; ideally one of these parameters would be known such that the other could be derived from the Memristance, but unfortunately for this work both were unknowns. Fig. 5.17 shows the same graph, but with the points now representing the mean of the measurements for every frequency for a better visualization.11

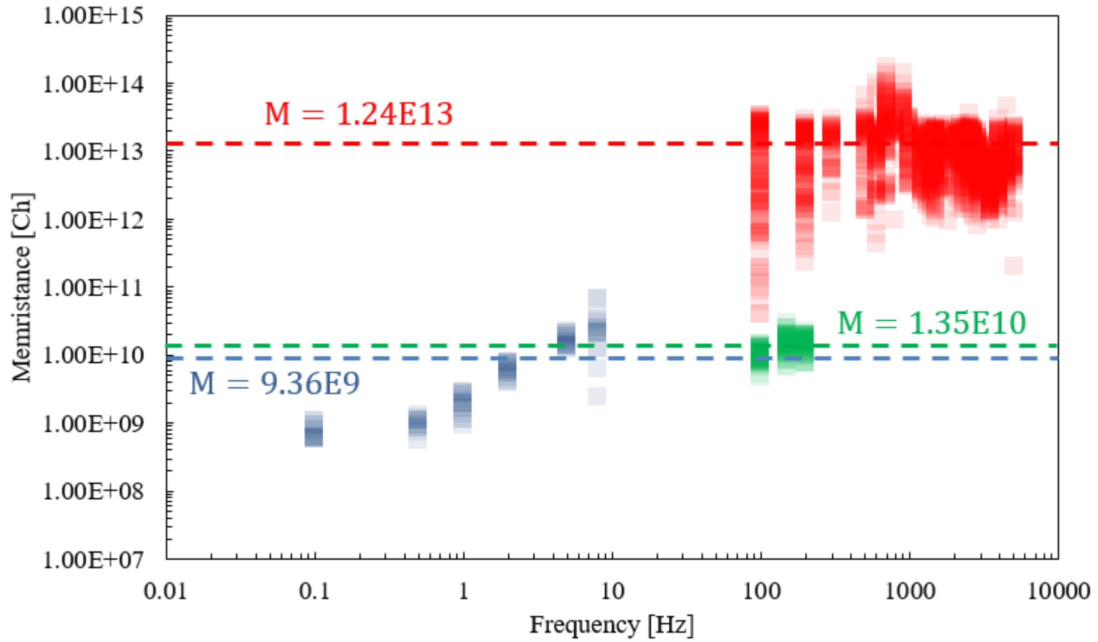

Figure 5.16: Analysis of mean measured memristance in multiple frequencies for all devices, with every measurement of Memristance shown.

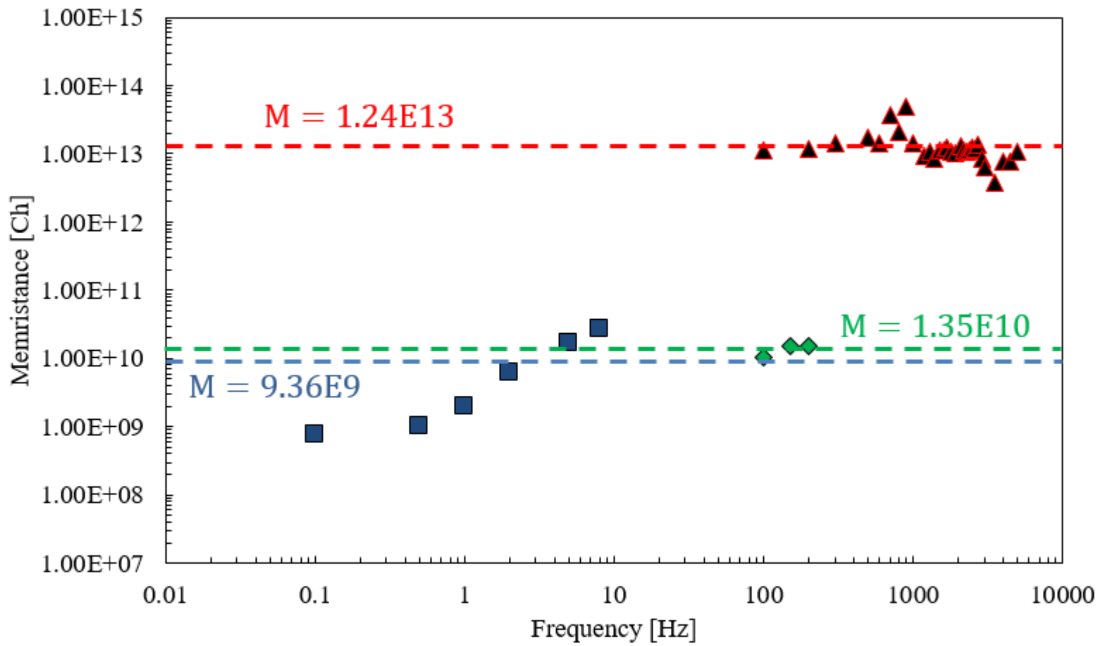

Figure 5.17: Analysis of mean measured memristance in multiple frequencies for all devices, with average of Memristance measurements for every frequency shown.

6. MEMTRANSISTOR - 1T1M STRUCTURE

By themselves, Memristors are a very powerful component. Many types have been used for a variety of applications, and their semblance to a synapse has not gone unnoticed by the scientific community [25, 87, 88]; used either alone or with supporting circuits to showcase their capabilities as a component in neuromorphic circuitry [89].

In this context, the integration of Memristors with Transistors is common [90] in order to introduce certain non-linearity and amplifications that are necessary for operation. This chapter studies the impact of manufacturing both the Memristor and transistor in a single stack, effectively reducing the complexity of a 1T1M structure and exploring the memristive properties of a high-k material already used in the process.

6.1 Device Structure

All of the previous work in the manufacture of this type of device was done by Derek Johnson [91, 92], albeit without the focus in producing Memristors and only focusing on the resulting HEMT. As a matter of fact, a memristive characteristic was not observed at all in the initial device (although charge trapping, which could possible be another memristance mechanism, was observed).

The fabrication process is outlined in previous work [92], but the device sketch is reproduced in Fig. 6.1 for easier reference. Transistor aside, the memristive structure is now a MIS instead of the more common MIM, and actually contacts to a 2DEG. These will affect the Memristor (since it is already established that metal contacts affect the Memristor behavior [71]) and all the effects in an eventual two terminal device with same structure can be subject of future work.

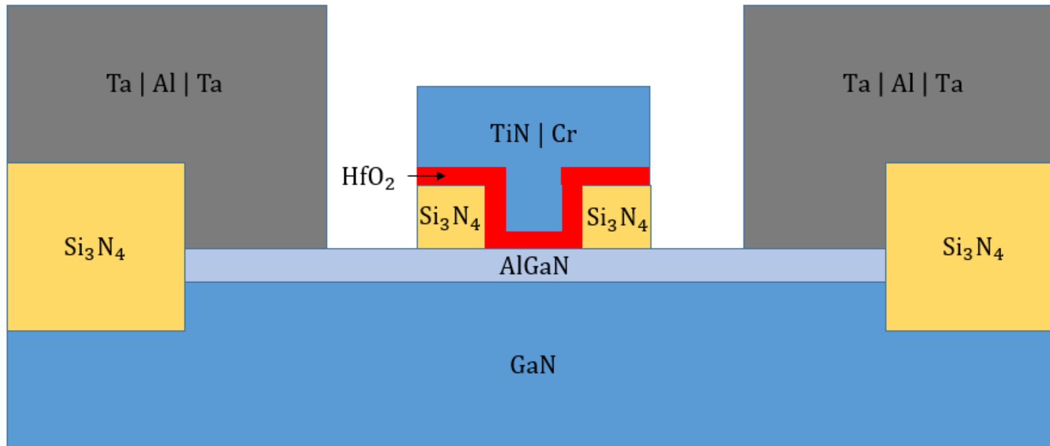

Figure 6.1: Sketch of fabricated HEMT device with metal-oxide gate insulator.

6.2 Memristance

The process for manufacturing this HEMT requires that the HfO_2 be annealed, which is in general undesirable in the context of Memristors as this eliminates many mobile charges that are used as a switching mechanism. In order to reintroduce them, the transistor has to pass through the forming cycle of Fig. 2.6. In it, the gate is biased with a positive voltage (much higher than the threshold voltage, which is usually negative) to a point where significant current passes through the gate oxide to the 2DEG, effectively transforming the gate oxide into a switching layer. Treated as a separate effect, this would introduce a "leakage Memristor", which would be tied to the 2DEG. A simple schematic with the position of the Memristor is shown in Fig. 6.2. This forming cycle appears to be asymmetric (which is to be expected due to the structure), since it does not appear to occur for the same magnitude of negative bias as it does for the positive. The introduction of oxygen vacancies inside of the dielectric has an impact on the threshold voltage of the device as mobile charges [93].

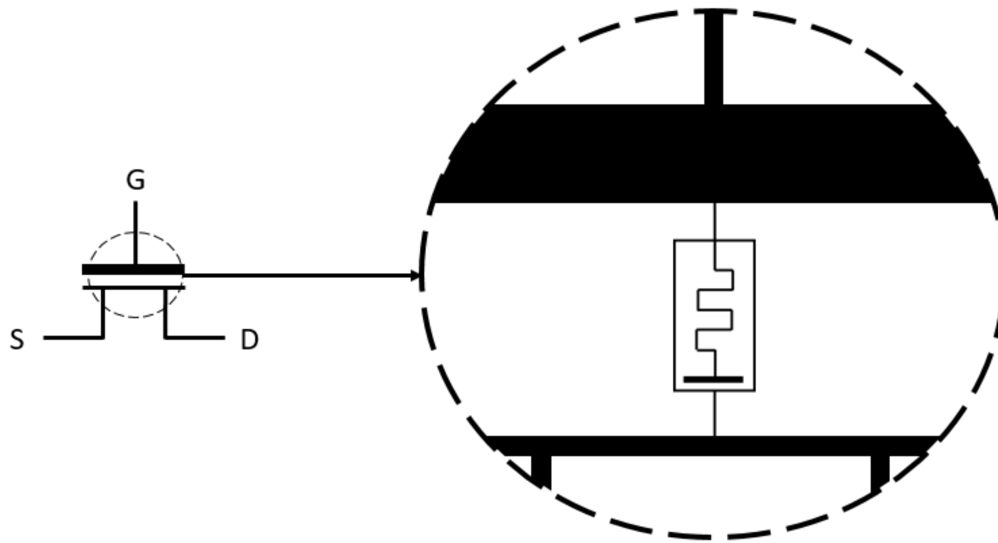

Figure 6.2: Position of the Memristor inside of the HEMT after forming cycle.

An immediate shift in the threshold voltage can be seen in Fig. 6.3, changing by approximately $+0.5V$ or 10%. A corresponding increase in leakage current of the gate is also observed: an increase of roughly 20%, corresponding to the new conduction path that was created by the forming cycle. Part of the responsibility for the observed V_T shift is also due to the trapping of charges in the $AlGaN$ as shown in previous research [92], but that alone would not account for the increase in gate current. This effectively ties the threshold voltage of the HEMT to the SV of the Memristor, since the placement of the mobile ions has a profound impact on the formation and extinction of the 2DEG [92]. Devices which integrate Memristors with a transistor are dubbed then Memtransistors and have been shown in previous work [94] and an elegant analysis was provided by Blaise Mouttet [95]. The work provided here has three main differences: the location of the Memristor, the high mobility provided by the 2DEG allowing for faster switching times, and the simplified structure that can make use of current high-k manufacturing techniques.

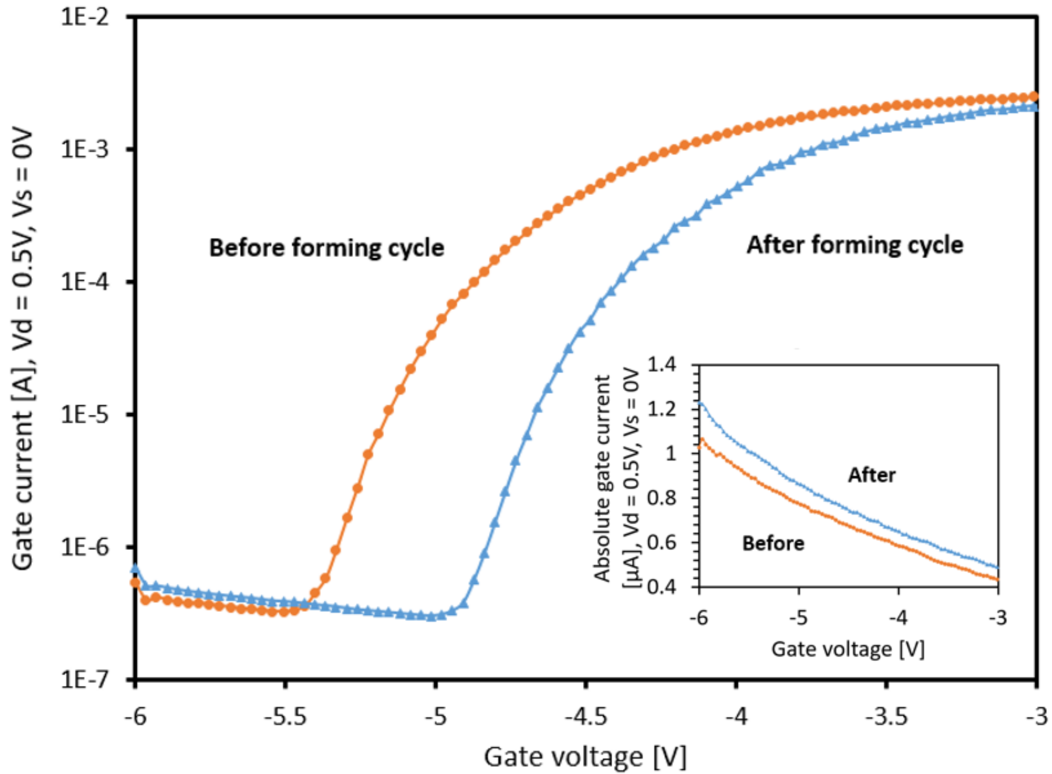

Figure 6.3: Semilog plot of I_d-V_g for the HEMT before and after a single forming cycle. Inset: gate current versus voltage showing increase in leakage currente after forming.

Since the Memristor is not located between the source and the drain, the transistor can conduct large currents with little correlation to the current value of the SV or Memristance. Fig. 6.4 shows a second forming cycle that is drastically altering the value of both SV and Memristance by adding new mobile ions to the oxide. The changes introduced by repeating this process can be seen in Fig. 6.5, which showcases that although the leakage current is greatly increased and threshold voltage also shifts by almost a volt, the maximum current remains within the same order of magnitude with a slight decrease (which is compatible with the shift in V_T).

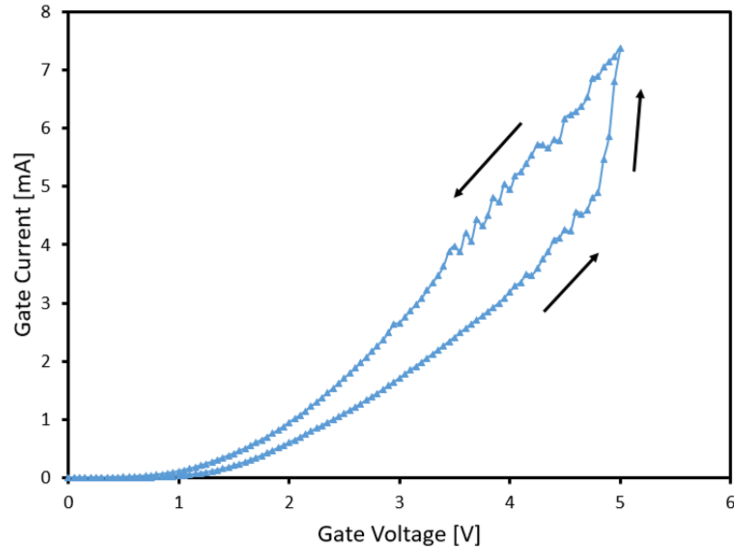

Figure 6.4: Second forming cycle.

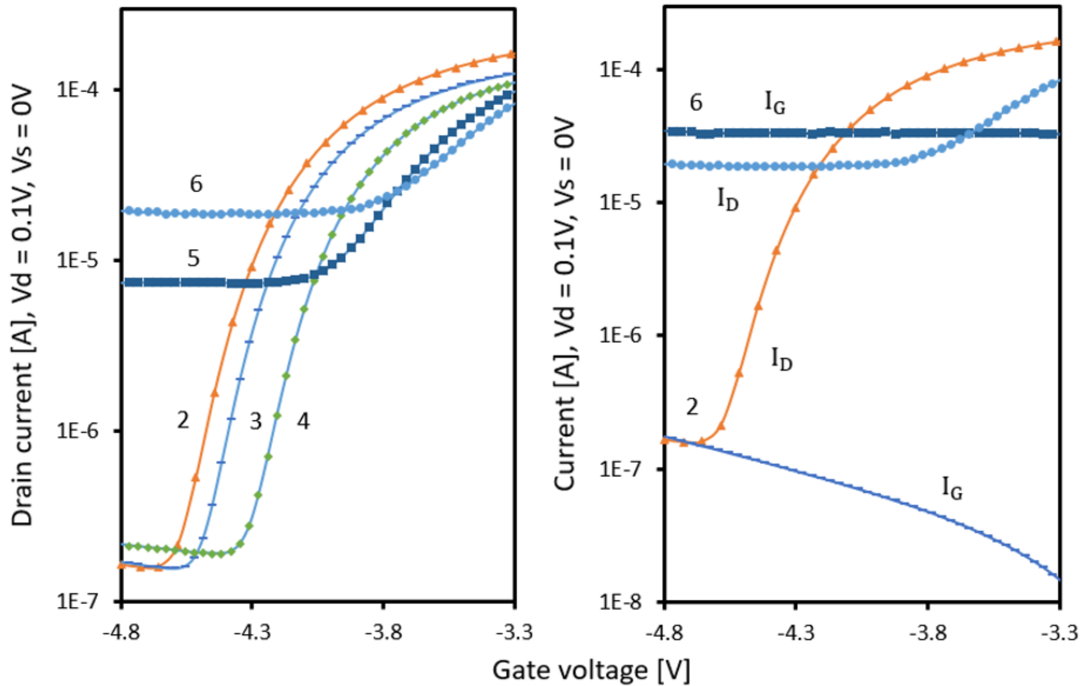

Figure 6.5: Semilog plots of I_d-V_g for the HEMT showcasing threshold voltage and gate leakage modification with further forming cycles. Numbers indicate amount of forming cycles applied before measurement.

To better analyze this Memristance, source and drain were tied together as a single second terminal; this allows the acquisition of the i-v curve shown in Fig. 6.6, which should be familiar at this point.

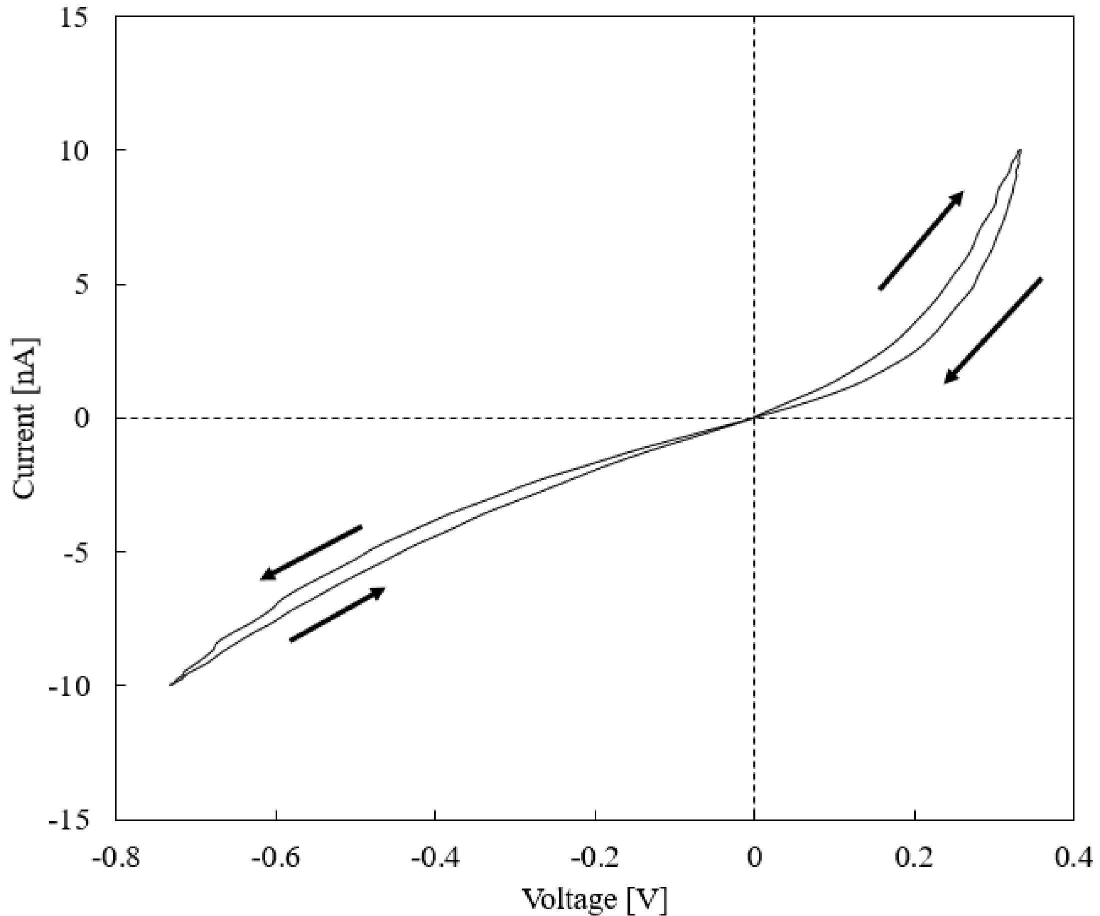

Figure 6.6: Memristance i-v for the HEMT. Source and Drain were tied and used as a second contact.

This curve was taken after the first forming cycle and before any further forming cycles were done to the device. To also prevent any further creation of mobile charges, excitation current used was well below an order of magnitude of the ones seen during the first forming cycle, which resulted in a very slow reaction time; the frequency required to achieve a measurable hysteresis loop was $100\mu Hz$. The hysteresis loop seen is clearly very asymmetrical (this is expected due to

the asymmetrical structure of the HEMT) and also requires correction due to previously explored parasitics. The corrected Ω-q graph for the calculation of Memristance is shown in Fig. 6.7.

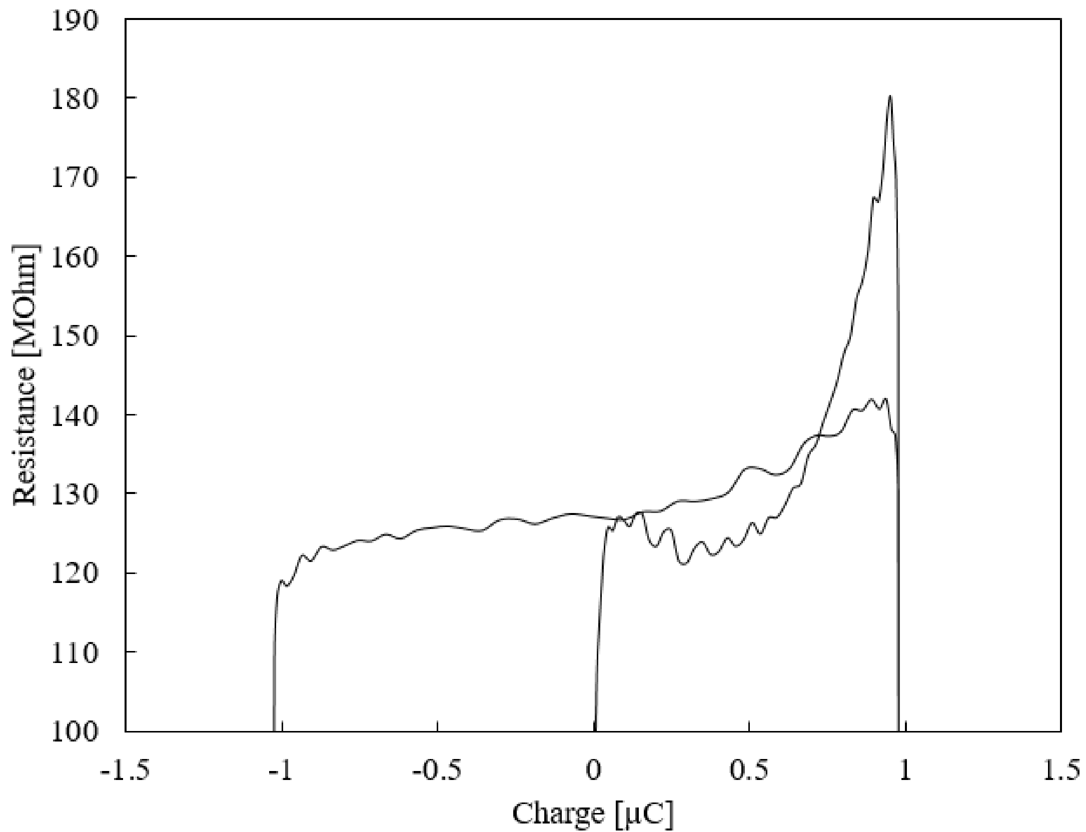

Figure 6.7: Memristance Ω-q for the HEMT. Source and Drain were tied and used as a second contact.

It can be easily noted that there is still some non-linear parasitic present, but in the negative cycle it has been almost completely eliminated. The Memristance was thus calculated as being $\approx 9TCh$ using the negative cycle data, although this value may vary significantly as seen before. This high value suggests that there is a very small CF present after forming (since the larger MIM device exhibited much lower Memristance), which is likely since these measurements were done after the very first forming, when resistance between the gate and the 2DEG was very high.

This Memristance present in a transistor can be made to integrate a firing neuron that exhibits

plasticity. A proof of concept circuit is shown in Fig. 6.8 and was simulated to show how the neuron circuit behaves with an incoming pulse train.

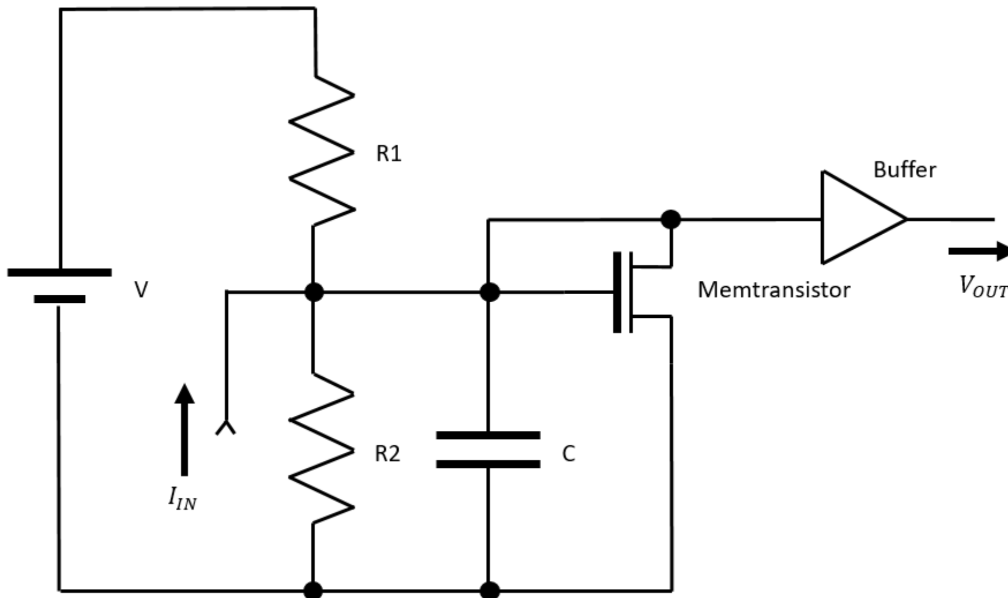

Figure 6.8: Neuromorphic circuit that generates spikes proportional to input current I_{IN}.

The results shown in Fig. 6.9 showcase a behavior that resembles the Hodgkin–Huxley model [96] with currents higher than a certain threshold exciting the circuit to maintain or amplify a train of pulses while currents below the threshold exhibit an attenuation.

Of notice is the fact that the currents and voltage levels are much different than the ones usually seen in neuromorphic computing. Initially this is not a problem since bias levels can be adjusted so that the circuit still operates as expected of a neuromorphic circuit only with different levels. This of course causes a difference in the power used, and the device can be optimized to perform better by adjusting the structure.

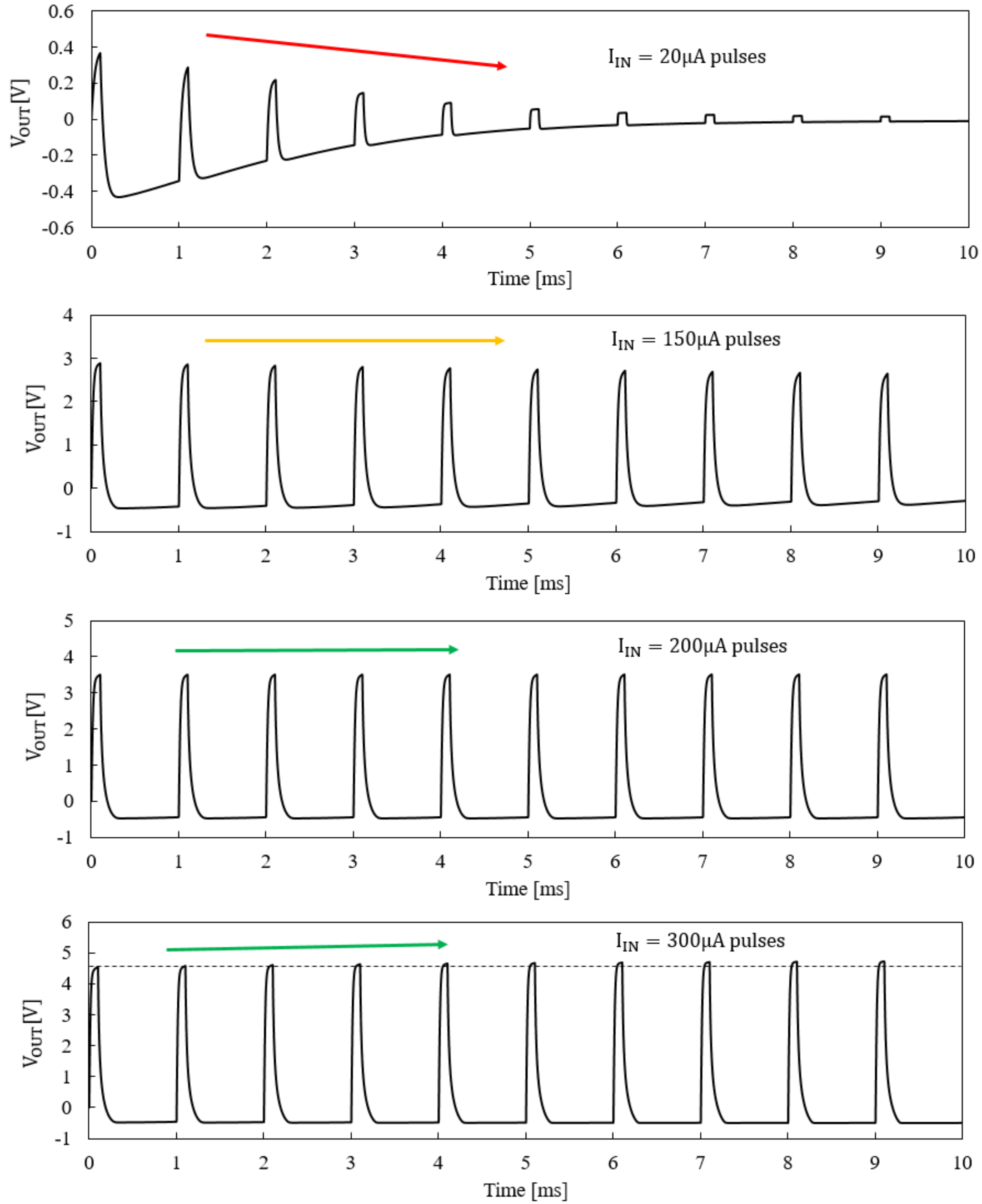

Figure 6.9: Results of exciting the neuromorphic circuit of Fig. 6.8 with I_{IN} pulses of magnitude $20\mu A$, $150\mu A$, $200\mu A$, and $300\mu A$. For this simulation: $C = 1nF$, $R1 = R2 = 1M\Omega$, and $V = -10V$. Dotted line in last graph added to show position of first peak, illustrating that peak size is increasing.

7. CONCLUSION AND OUTLOOK

The fabrication of the first Memristor in 2008 was not simply a physical realization of the theory proposed by Leon Chua, but the foundation of an interesting new paradigm that may keep the exponential growth of computational power for years to come. This work hopes to provide the necessary foundation for the area of Memristor engineering, providing a brief review of the current state of the art and developing tools and mathematical models to aid in the description, modeling and application of the fourth fundamental passive circuit element.

As with any other practical device, the physical Memristors exhibit many parasitics that currently cannot be neglected in the device due to characteristics in the mechanism of the switching medium and device construction. However, they can be modeled by the simple addition of well-known diodes: this allows a simpler understanding of these parasitics and a great flexibility in their modeling. Additionally, it was also shown that these parasitics may alter how we see memristance altogether, since they change many variables that were used as fundamental metrics of a device. This has then proven to be a powerful tool for modeling many types of previously published Memristors, fitting closely to experimental data.

The main contribution of this work is the development of a theory that allows for the Memristor to finally be seen as a fundamental passive device by outlining the location of the linearity and providing then a measurement of memristance, the *Chua*, that can be used as a classification of Memristors and represents the change in resistance due to the history of charge through the device. Additionally, the theoretical model makes interesting predictions: memristance scales with the inverse square of area, causing inherently large devices to exhibit a memristance too low to be measured. This is the fundamental reason Memristors were not discovered until recently, though they existed in various forms previously; it was only now that lithography techniques were advanced enough to produce devices with the adequate dimensions to be clearly detected. The increasing shrinking of devices should, then, also produce more ideal devices in the near future.

Analysis of fabricated devices provides confirmation that a device can be classified with re-

gards to its Memristance M and initial resistance R, although a large variance was observed; this variation was explained as being caused by further forming of oxygen vacancies on the device and geometric differences in the path of the CF, and it is clear that further study is required in this area to both properly explain these phenomenological causes and to properly fabricate an ideal Memristor.

Finally, a Memtransistor is proposed that combines the desired plasticity requirements provided by a Memristor with the amplification supplied by a HEMT. This structure is simpler than previously proposed devices and combined with the Memristance study provided here, allows for a greater degree of flexibility.

REFERENCES

[1] G. Moore, "Cramming more components onto integrated circuits," *IEEE Solid-State Circuits Newsletter*, vol. 11, no. 5, pp. 33–35, 2006.

[2] M. J. Kearns, *The computational complexity of machine learning*. MIT Press, 1990.

[3] S. Furber, "Large-scale neuromorphic computing systems," *Journal of Neural Engineering*, vol. 13, no. 5, p. 051001, 2016.

[4] M. Newborn, *Kasparov versus Deep Blue: Computer chess comes of age*. Springer Science & Business Media, 2012.

[5] R. C. Merkle, "Energy limits to the computational power of the human brain," *Foresight Update*, vol. 6, 1989.

[6] A. Lansner, "Associative memory models: from the cell-assembly theory to biophysically detailed cortex simulations," *Trends in Neurosciences*, vol. 32, no. 3, pp. 178–186, 2009.

[7] M. I. Jordan and T. M. Mitchell, "Machine learning: trends, perspectives, and prospects," *Science*, vol. 349, no. 6245, pp. 255–260, 2015.

[8] L. B. Kish, "End of moore's law: thermal (noise) death of integration in micro and nano electronics," *Physics Letters A*, vol. 305, no. 3-4, pp. 144–149, 2002.

[9] R. R. Schaller, "Moore's law: past, present and future," *IEEE Spectrum*, vol. 34, no. 6, pp. 52–59, 1997.

[10] R. Colwell, "The chip design game at the end of moore," in *2013 IEEE Hot Chips 25 Symposium (HCS)*, pp. 1–16, IEEE, 2013.

[11] K. Rupp, "42 years of microprocessor trend data (2018)," *URL https://www.karlrupp.net/2018/02/42-years-of-microprocessor-trend-data/*, 40.

[12] J. Von Neumann, "First draft of a report on the edvac, 1945," *Contract No. W-670-ORD-492, Moore School of Electrical Engineering, Univ. of Penn., Philadelphia. Reprinted (in*

part) in Origins of Digital Computers: Selected Papers, Springer-Verlag, Berlin Heidelberg, pp. 383–392, 1982.

[13] J. Backus, *Can programming be liberated from the von Neumann style?: a functional style and its algebra of programs*. ACM, 2007.

[14] J. Backus, "Acm turing award lecture," *Commun. ACM*, vol. 21, no. 8, 1978.

[15] G. Bell, R. Sites, W. Dally, D. Ditzel, and Y. Patt, "Architects look to processors of future," *Microprocessor Report, Microdesign Resources*, vol. 10, no. 10, 1996.

[16] P. A. Merolla, J. V. Arthur, R. Alvarez-Icaza, A. S. Cassidy, J. Sawada, F. Akopyan, B. L. Jackson, N. Imam, C. Guo, Y. Nakamura, *et al.*, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science*, vol. 345, no. 6197, pp. 668–673, 2014.

[17] A. Calimera, E. Macii, and M. Poncino, "The human brain project and neuromorphic computing," *Functional Neurology*, vol. 28, no. 3, p. 191, 2013.

[18] W. Lu, "Memristors: going active," *Nature materials*, vol. 12, no. 2, p. 93, 2013.

[19] E. J. Merced-Grafals, N. Dávila, N. Ge, R. S. Williams, and J. P. Strachan, "Repeatable, accurate, and high speed multi-level programming of memristor 1t1r arrays for power efficient analog computing applications," *Nanotechnology*, vol. 27, no. 36, p. 365202, 2016.

[20] A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro, and R. S. Williams, "Sub-nanosecond switching of a tantalum oxide memristor," *Nanotechnology*, vol. 22, no. 48, p. 485203, 2011.

[21] Y.-T. Li, S.-B. Long, H.-B. Lv, Q. Liu, Q. Wang, Y. Wang, S. Zhang, W.-T. Lian, S. Liu, and M. Liu, "A low-cost memristor based on titanium oxide," in *Solid-state and Integrated Circuit Technology (ICSICT), 2010 10th IEEE International Conference on*, pp. 1148–1150, IEEE, 2010.

[22] I. Baek, C. Park, H. Ju, D. Seong, H. Ahn, J. Kim, M. Yang, S. Song, E. Kim, S. Park, *et al.*, "Realization of vertical resistive memory (vrram) using cost effective 3d process," in *2011 International Electron Devices Meeting*, pp. 31–8, IEEE, 2011.

[23] J. P. Strachan, A. C. Torrezan, G. Medeiros-Ribeiro, and R. S. Williams, "Measuring the switching dynamics and energy efficiency of tantalum oxide memristors," *Nanotechnology*, vol. 22, no. 50, p. 505402, 2011.

[24] W. G. Kim, H. M. Lee, B. Y. Kim, K. H. Jung, T. G. Seong, S. Kim, H. C. Jung, H. J. Kim, J. H. Yoo, H. D. Lee, *et al.*, "Nbo 2-based low power and cost effective 1s1r switching for high density cross point reram application," in *2014 Symposium on VLSI Technology (VLSI-Technology): Digest of Technical Papers*, pp. 1–2, IEEE, 2014.

[25] M. D. Pickett, G. Medeiros-Ribeiro, and R. S. Williams, "A scalable neuristor built with mott memristors," *Nature Materials*, vol. 12, no. 2, p. 114, 2013.

[26] S. Shin, K. Kim, and S.-M. Kang, "Memristor applications for programmable analog ics," *IEEE Transactions on Nanotechnology*, vol. 10, no. 2, pp. 266–274, 2010.

[27] M. Itoh and L. O. Chua, "Memristor oscillators," *International Journal of Bifurcation and Chaos*, vol. 18, no. 11, pp. 3183–3206, 2008.

[28] İ. C. Göknar, F. Öncül, and E. Minayi, "New memristor applications: Am, ask, fsk, and bpsk modulators," *IEEE Antennas and Propagation Magazine*, vol. 55, no. 2, pp. 304–313, 2013.

[29] S. Kvatinsky, D. Belousov, S. Liman, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Magic—memristor-aided logic," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 11, pp. 895–899, 2014.

[30] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on Circuit Theory*, vol. 18, pp. 507–519, September 1971.

[31] S. P. Adhikari, M. P. Sah, H. Kim, and L. O. Chua, "Three fingerprints of memristor," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, pp. 3008–3021, Nov 2013.

[32] D. Biolek, Z. Biolek, V. Biolková, and Z. Kolka, “Some fingerprints of ideal memristors,” in *Circuits and Systems (ISCAS), 2013 IEEE International Symposium on*, pp. 201–204, IEEE, 2013.

[33] S. Vongehr and X. Meng, “The missing memristor has not been found,” *Scientific Reports*, vol. 5, p. 11657, 2015.

[34] I. Abraham, “The case for rejecting the memristor as a fundamental circuit element,” *Scientific Reports*, vol. 8, no. 1, p. 10972, 2018.

[35] A. Ascoli, F. Corinto, V. Senger, and R. Tetzlaff, “Memristor model comparison,” *IEEE Circuits and Systems Magazine*, vol. 13, no. 2, pp. 89–105, 2013.

[36] Z. Biolek, D. Biolek, and V. Biolkova, “Spice model of memristor with nonlinear dopant drift.,” *Radioengineering*, vol. 18, no. 2, 2009.

[37] K. Zaplatilek, “Memristor modeling in matlab & simulink,” in *Proceedings of the European Computing Conference*, pp. 62–67, 2011.

[38] S. Kvatinsky, E. G. Friedman, A. Kolodny, and U. C. Weiser, “Team: Threshold adaptive memristor model,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 211–221, 2013.

[39] L. Chua, “Resistance switching memories are memristors,” *Applied Physics A*, vol. 102, pp. 765–783, Mar 2011.

[40] Y. Ho, G. M. Huang, and P. Li, “Nonvolatile memristor memory: Device characteristics and design implications,” in *Proceedings of the 2009 International Conference on Computer-Aided Design*, ICCAD ’09, (New York, NY, USA), pp. 485–490, ACM, 2009.

[41] M. A. Zidan, H. A. H. Fahmy, M. M. Hussain, and K. N. Salama, “Memristor-based memory: The sneak paths problem and solutions,” *Microelectronics Journal*, vol. 44, no. 2, pp. 176–183, 2013.

[42] B. Muthuswamy and P. P. Kokate, "Memristor-based chaotic circuits," *IETE Technical Review*, vol. 26, no. 6, pp. 417–429, 2009.

[43] B. Bao, Z. Ma, J. Xu, Z. Liu, and Q. Xu, "A simple memristor chaotic circuit with complex dynamics," *International Journal of Bifurcation and Chaos*, vol. 21, no. 09, pp. 2629–2645, 2011.

[44] B. Muthuswamy, "Implementing memristor based chaotic circuits," *International Journal of Bifurcation and Chaos*, vol. 20, no. 05, pp. 1335–1350, 2010.

[45] P. Koeberl, Ü. Kocabaş, and A.-R. Sadeghi, "Memristor pufs: a new generation of memory-based physically unclonable functions," in *Proceedings of the Conference on Design, Automation and Test in Europe*, pp. 428–431, EDA Consortium, 2013.

[46] J. Rajendran, G. S. Rose, R. Karri, and M. Potkonjak, "Nano-ppuf: A memristor-based security primitive," in *2012 IEEE Computer Society Annual Symposium on VLSI*, pp. 84–87, IEEE, 2012.

[47] H. Kim, M. P. Sah, C. Yang, T. Roska, and L. O. Chua, "Neural synaptic weighting with a pulse-based memristor circuit," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 148–158, 2012.

[48] D. Chabi, Z. Wang, C. Bennett, J.-O. Klein, and W. Zhao, "Ultrahigh density memristor neural crossbar for on-chip supervised learning," *IEEE Transactions on Nanotechnology*, vol. 14, no. 6, pp. 954–962, 2015.

[49] S. P. Adhikari, C. Yang, H. Kim, and L. O. Chua, "Memristor bridge synapse-based neural network and its learning," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 23, no. 9, pp. 1426–1435, 2012.

[50] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, pp. 80–83, May 2008.

[51] Y. Li, Y. Zhong, J. Zhang, X. Xu, Q. Wang, L. Xu, H. Sun, and X. Miao, "Intrinsic memristance mechanism of crystalline stoichiometric ge2sb2te5," *Applied Physics Letters*, vol. 103, no. 4, p. 043501, 2013.

[52] J. D. Greenlee, C. F. Petersburg, W. Laws Calley, C. Jaye, D. A. Fischer, F. M. Alamgir, and W. Alan Doolittle, "In-situ oxygen x-ray absorption spectroscopy investigation of the resistance modulation mechanism in linbo2 memristors," *Applied Physics Letters*, vol. 100, no. 18, p. 182106, 2012.

[53] E. Gale, "Tio2-based memristors and reram: materials, mechanisms and models (a review)," *Semiconductor Science and Technology*, vol. 29, no. 10, p. 104004, 2014.

[54] P. Meuffels and R. Soni, "Fundamental issues and problems in the realization of memristors," *arXiv preprint arXiv:1207.7319*, 2012.

[55] J. J. Yang, M. D. Pickett, X. Li, D. A. Ohlberg, D. R. Stewart, and R. S. Williams, "Memristive switching mechanism for metal/oxide/metal nanodevices," *Nature Nanotechnology*, vol. 3, no. 7, p. 429, 2008.

[56] B. Choi, D. S. Jeong, S. Kim, C. Rohde, S. Choi, J. Oh, H. Kim, C. Hwang, K. Szot, R. Waser, *et al.*, "Resistive switching mechanism of tio 2 thin films grown by atomic-layer deposition," *Journal of Applied Physics*, vol. 98, no. 3, p. 033715, 2005.

[57] D. Kim, S. Seo, S. Ahn, D.-S. Suh, M. Lee, B.-H. Park, I. Yoo, I. Baek, H.-J. Kim, E. Yim, *et al.*, "Electrical observations of filamentary conductions for the resistive memory switching in nio films," *Applied Physics Letters*, vol. 88, no. 20, p. 202102, 2006.

[58] T.-N. Fang, S. Kaza, S. Haddad, A. Chen, Y.-C. Wu, Z. Lan, S. Avanzino, D. Liao, C. Gopalan, S. Choi, *et al.*, "Erase mechanism for copper oxide resistive switching memory cells with nickel electrode," in *2006 International Electron Devices Meeting*, pp. 1–4, IEEE, 2006.

[59] D. Lee, D.-j. Seong, I. Jo, F. Xiang, R. Dong, S. Oh, and H. Hwang, "Resistance switching of copper doped moo x films for nonvolatile memory applications," *Applied Physics Letters*, vol. 90, no. 12, p. 122104, 2007.

[60] M. Kozicki, M. Yun, L. Hilt, and A. Singh, "Applications of programmable resistance changes in metal-doped chalcogenides," *Pennington NJ USA: Electrochem. Soc*, vol. 99, pp. 298–309, 1999.

[61] L. D. Bozano, B. W. Kean, M. Beinhoff, K. R. Carter, P. M. Rice, and J. C. Scott, "Organic materials and thin-film structures for cross-point memory cells based on trapping in metallic nanoparticles," *Advanced Functional Materials*, vol. 15, no. 12, pp. 1933–1939, 2005.

[62] Z. Donhauser, B. Mantooth, K. Kelly, L. Bumm, J. Monnell, J. Stapleton, D. Price, A. Rawlett, D. Allara, J. Tour, *et al.*, "Conductance switching in single molecules through conformational changes," *Science*, vol. 292, no. 5525, pp. 2303–2307, 2001.

[63] S. Kumar, J. P. Strachan, and R. S. Williams, "Chaotic dynamics in nanoscale nbo 2 mott memristors for analogue computing," *Nature*, vol. 548, no. 7667, p. 318, 2017.

[64] H. S. Yoon, I.-G. Baek, J. Zhao, H. Sim, M. Y. Park, H. Lee, G.-H. Oh, J. C. Shin, I.-S. Yeo, and U.-I. Chung, "Vertical cross-point resistance change memory for ultra-high density non-volatile memory applications," in *2009 Symposium on VLSI Technology*, pp. 26–27, IEEE, 2009.

[65] C.-K. Lee, Y.-J. Eom, J.-H. Park, J. Lee, H.-R. Kim, K. Kim, Y. Choi, H.-J. Chang, J. Kim, J.-M. Bang, *et al.*, "23.2 a 5gb/s/pin 8gb lpddr4x sdram with power-isolated lvstl and split-die architecture with 2-die zq calibration scheme," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 390–391, IEEE, 2017.

[66] Z. Guo, D. Kim, S. Nalam, J. Wiedemer, X. Wang, and E. Karl, "A 23.6-mb/mm^2 sram in 10-nm finfet technology with pulsed-pmos tvc and stepped-wl for low-voltage applications," *IEEE Journal of Solid-State Circuits*, no. 99, pp. 1–7, 2018.

[67] R. E. Fontana, S. R. Hetzler, and G. Decad, "Technology roadmap comparisons for tape, hdd, and nand flash: implications for data storage applications," *IEEE Transactions on Magnetics*, vol. 48, no. 5, pp. 1692–1696, 2012.

[68] T. Perez and C. A. De Rose, "Non-volatile memory: Emerging technologies and their impacts on memory systems," *Porto Alegre*, 2010.

[69] Y. N. Joglekar and S. J. Wolf, "The elusive memristor: properties of basic electrical circuits," *European Journal of Physics*, vol. 30, no. 4, p. 661, 2009.

[70] J. C. Shank, M. B. Tellekamp, and W. A. Doolittle, "A scalable non-electroformed memdiode for neuromorphic circuitry," in *Device Research Conference (DRC), 2016 74th Annual*, pp. 1–2, IEEE, 2016.

[71] N. Ge, M. Zhang, L. Zhang, J. J. Yang, Z. Li, and R. S. Williams, "Electrode-material dependent switching in tao x memristors," *Semiconductor Science and Technology*, vol. 29, no. 10, p. 104003, 2014.

[72] K.-H. Kim, S. Gaba, D. Wheeler, J. M. Cruz-Albrecht, T. Hussain, N. Srinivasa, and W. Lu, "A functional hybrid memristor crossbar-array/cmos system for data storage and neuromorphic applications," *Nano Letters*, vol. 12, no. 1, pp. 389–395, 2011.

[73] J. P. Strachan, A. C. Torrezan, F. Miao, M. D. Pickett, J. J. Yang, W. Yi, G. Medeiros-Ribeiro, and R. S. Williams, "State dynamics and modeling of tantalum oxide memristors," *IEEE Transactions on Electron Devices*, vol. 60, no. 7, pp. 2194–2202, 2013.

[74] M. P. Sah, C. Yang, H. Kim, B. Muthuswamy, J. Jevtic, and L. Chua, "A generic model of memristors with parasitic components," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 891–898, 2015.

[75] E. C. Garnett and P. Yang, "Silicon nanowire radial p- n junction solar cells," *Journal of the American Chemical Society*, vol. 130, no. 29, pp. 9224–9225, 2008.

[76] M. Kroon and R. van Swaaij, "Spatial effects on ideality factor of amorphous silicon pin diodes," *Journal of Applied Physics*, vol. 90, no. 2, pp. 994–1000, 2001.

[77] B. Tian, X. Zheng, T. J. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang, and C. M. Lieber, "Coaxial silicon nanowires as solar cells and nanoelectronic power sources," *Nature*, vol. 449, no. 7164, p. 885, 2007.

[78] J. M. Shah, Y.-L. Li, T. Gessmann, and E. F. Schubert, "Experimental analysis and theoretical model for anomalously high ideality factors (n» 2.0) in algan/gan pn junction diodes," *Journal of Applied Physics*, vol. 94, no. 4, pp. 2627–2630, 2003.

[79] A. Chanthbouala, V. Garcia, R. O. Cherifi, K. Bouzehouane, S. Fusil, X. Moya, S. Xavier, H. Yamada, C. Deranlot, N. D. Mathur, *et al.*, "A ferroelectric memristor," *Nature Materials*, vol. 11, no. 10, p. 860, 2012.

[80] Z. Biolek, D. Biolek, and V. Biolková, "Computation of the area of memristor pinched hysteresis loop," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 9, pp. 607–611, 2012.

[81] L. Chua, "If it's pinched it's a memristor," *Semiconductor Science and Technology*, vol. 29, no. 10, p. 104001, 2014.

[82] P. S. Ho and T. Kwok, "Electromigration in metals," *Reports on Progress in Physics*, vol. 52, no. 3, p. 301, 1989.

[83] A. Shkabko, M. Aguirre, I. Marozau, T. Lippert, and A. Weidenkaff, "Measurements of current-voltage-induced heating in the al/srtio 3- x n y/al memristor during electroformation and resistance switching," *Applied Physics Letters*, vol. 95, no. 15, p. 152109, 2009.

[84] J. Tao, N. W. Cheung, and C. Hu, "Electromigration characteristics of copper interconnects," *IEEE Electron Device Letters*, vol. 14, no. 5, pp. 249–251, 1993.

[85] G. Brocard, *The LTSpice IV Simulator: Manual, Methods and Applications*. Würth Elektronik, 2013.

[86] K. A. Campbell, "Self-directed channel memristor for high temperature operation," *Microelectronics Journal*, vol. 59, pp. 10–14, 2017.

[87] H. Mostafa, A. Khiat, A. Serb, C. G. Mayr, G. Indiveri, and T. Prodromakis, "Implementation of a spike-based perceptron learning rule using tio2- x memristors," *Frontiers in Neuroscience*, vol. 9, p. 357, 2015.

[88] V. Demin, V. Erokhin, A. Emelyanov, S. Battistoni, G. Baldi, S. Iannotta, P. Kashkarov, and M. Kovalchuk, "Hardware elementary perceptron based on polyaniline memristive devices," *Organic Electronics*, vol. 25, pp. 16–20, 2015.

[89] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Letters*, vol. 10, no. 4, pp. 1297–1301, 2010. PMID: 20192230.

[90] K. D. Cantley, A. Subramaniam, H. J. Stiegler, R. A. Chapman, and E. M. Vogel, "Neural learning circuits utilizing nano-crystalline silicon transistors and memristors," *IEEE Transactions on Neural Networks and Learning Systems*, vol. 23, no. 4, pp. 565–573, 2012.

[91] D. W. Johnson, R. T. Lee, R. J. Hill, M. H. Wong, G. Bersuker, E. L. Piner, P. D. Kirsch, and H. R. Harris, "Threshold voltage shift due to charge trapping in dielectric-gated algan/gan high electron mobility transistors examined in au-free technology," *IEEE Transactions on Electron Devices*, vol. 60, no. 10, pp. 3197–3203, 2013.

[92] D. W. Johnson, "Si-cmos-like integration of algan/gan dielectric-gated high-electron-mobility transistors," *Doctoral Dissertation*, Texas A&M University, 2014.

[93] E. H. Nicollian, J. R. Brews, and E. H. Nicollian, *MOS (metal oxide semiconductor) physics and technology*, vol. 1987. Wiley New York et al., 1982.

[94] V. K. Sangwan, H.-S. Lee, H. Bergeron, I. Balla, M. E. Beck, K.-S. Chen, and M. C. Hersam, "Multi-terminal memtransistors from polycrystalline monolayer molybdenum disulfide," *Nature*, vol. 554, no. 7693, p. 500, 2018.

[95] B. Mouttet, "Memristive systems analysis of 3-terminal devices," in *2010 17th IEEE International Conference on Electronics, Circuits and Systems*, pp. 930–933, IEEE, 2010.

[96] A. Hodgkin and A. Huxley, “A quantitative description of membrane current and its application to conduction and excitation in nerve,” *Bulletin of Mathematical Biology*, vol. 52, no. 1-2, pp. 25–71, 1990.